

DESCRIPTION

The 82S126 (Open Collector Outputs) and the 82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S126 and 82S129 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, B or F. For the military temperature range (-55°C to +125°C) specify S82S126/129, F only.

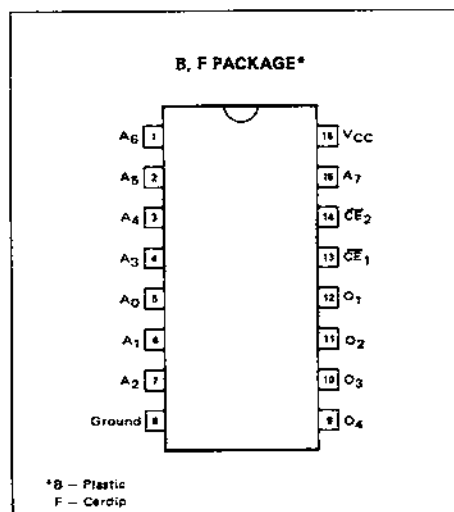
FEATURES

- ORGANIZATION — 256 X 4
- ADDRESS ACCESS TIME:
S82S126/129 — 70ns, MAXIMUM
N82S126/129 — 50ns, MAXIMUM
- POWER DISSIPATION — 0.5mW/BIT TYPICAL
- INPUT LOADING:
S82S126/129 — (-150μA) MAXIMUM
N82S126/129 — (-100μA) MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
OPEN COLLECTOR — 82S126
TRI-STATE — 82S129
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

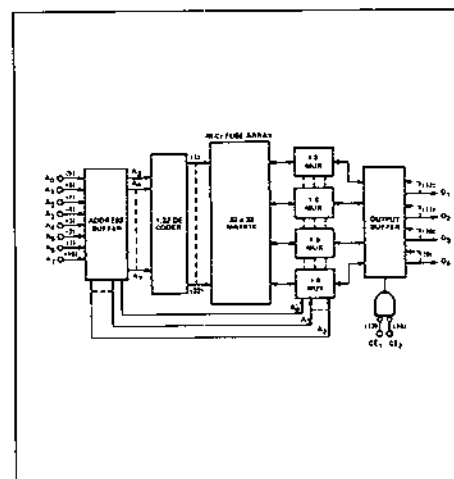
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

PIN CONFIGURATION



BLOCK DIAGRAM



SIGNETICS 1024-BIT BIPOLAR PROGRAMMABLE ROM (256 X 4 PROM) = 82S126, 82S129

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power Supply Voltage	+7	V _{dc}
V _{IN} Input Voltage	+5.5	V _{dc}
V _{OH} High Level Output Voltage (82S126)	+5.5	V _{dc}
V _O Off-State Output Voltage (82S129)	+5.5	V _{dc}
T _A Operating Temperature Range (N82S126/129) (S82S126/129)	0° to +75° -55° to +125°	°C
T _{stg} Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS S82S126/S82S129 -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
N82S126/N82S129 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ¹	S82S126/129			N82S126/129			UNIT
		MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V _{OL} "0" Output Voltage	I _{OUT} = 16mA			0.5			0.5	V
I _{OLK} Output Leakage Current (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V _{OUT} = 5.5V			80			40	μA
I _{O(DF)} Hi-Z State Output Current (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V _{OUT} = 5.5V			80			40	μA
	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V _{OUT} = 0.5V			-60			-40	μA
V _{OH} "1" Output Voltage (82S129)	$\overline{CE}_1 = \overline{CE}_2$ = "0", I _{OUT} = -2.0mA, "1" STORED	2.4			2.4			V
C _{IN} Input Capacitance	V _{IN} = 2.0V, V _{CC} = 5.0V		5			5		pF
C _{OUT} Output Capacitance	V _{OUT} = 2.0V, V _{CC} = 5.0V		8			8		pF
I _{IL} "0" Input Current	V _{IN} = 0.45V			-150			-100	μA
I _{IH} "1" Input Current	V _{IN} = 5.5V			50			40	μA
V _{IL} "0" Level Input Voltage				.80			.85	V
V _{IH} "1" Level Input Voltage		2.0			2.0			V
I _{CC} V _{CC} Supply Current			105	125		105	120	mA
V _{IC} Input Clamp Voltage	I _{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
I _{OS} Output Short Circuit Current (82S129)	V _{OUT} = 0V	-15		-85	-20		-70	mA

SWITCHING CHARACTERISTICS S82S126/129 -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
N82S126/129 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
		MIN	TYP ²	MAX	MIN	TYP ²	MAX	
Propagation Delay								
T _{AA} Address to Output	C _L = 30pF		35	70		35	50	ns
T _{CD} Chip Disable to Output	R ₁ = 270Ω		15	35		15	20	ns
T _{CE} Chip Enable to Output	R ₂ = 600Ω		15	35		15	20	ns

NOTES

1. Positive current is defined as into the terminal referenced.

2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

SIGNETICS 1024-BIT BIPOLAR PROGRAMMABLE ROM (256 X 4 PROM) ■ 82S126, 82S129
PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		MIN	TYP	MAX		
Power Supply Voltage						
V _{CCP} ¹	To Program	I _{CCP} = 350 ± 50mA (Transient or steady state)	8.5	8.75	9.0	V
V _{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V _{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V _S ³	Verify Threshold		0.9	1.0	1.1	V
I _{CCP}	Programming Supply Current	V _{CCP} = +8.75 ± .25V	300	350	400	mA
Input Voltage						
V _{IH}	Logical "1"		2.4		5.5	V
V _{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I _{IH}	Logical "1"	V _{IH} = +5.5V			50	μA
I _{IL}	Logical "0"	V _{IL} = +0.4V			-500	μA
V _{OUT} ²	Output Programming Voltage	I _{OUT} = 200 ± 20mA (Transient or steady state)	16.0	17.0	18.0	V
I _{OUT}	Output Programming Current	V _{OUT} = +17 ± 1V	180	200	220	mA
T _R	Output Pulse Rise Time		10		50	μs
t _p	CE Programming Pulse Width		1		2	ms
t _D	Pulse Sequence Delay		10			μs
T _{PR}	Programming Time	V _{CC} = V _{CCP}			2.5	sec
T _{PS}	Programming Pause	V _{CC} = 0V	5			sec
T _{PR} ⁴					33	%
T _{PR} + T _{PS}	Programming Duty Cycle					

PROGRAMMING PROCEDURE

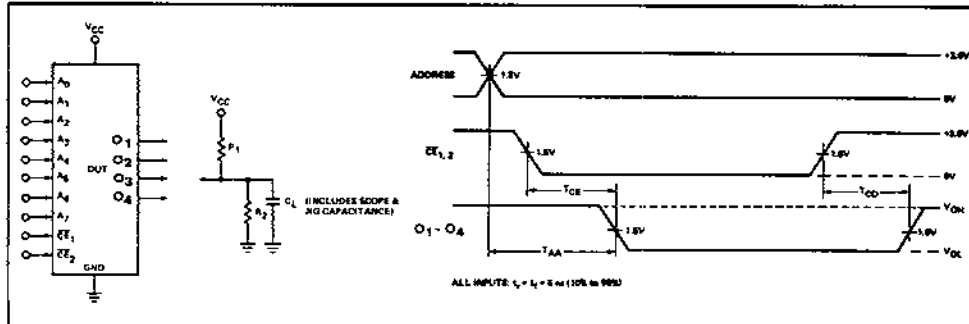
1. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} .
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$.
3. After $10\mu\text{s}$ delay, apply $V_{OUT} = +17 \pm 1\text{V}$ to the output to be programmed. Program one output at the time.
4. After $10\mu\text{s}$ delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After $10\mu\text{s}$ delay, remove $+17\text{V}$ from the programmed output.
6. To verify programming, after $10\mu\text{s}$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu\text{s}$ delay, repeat steps 2 through 7 to program all other address locations.

NOTES:

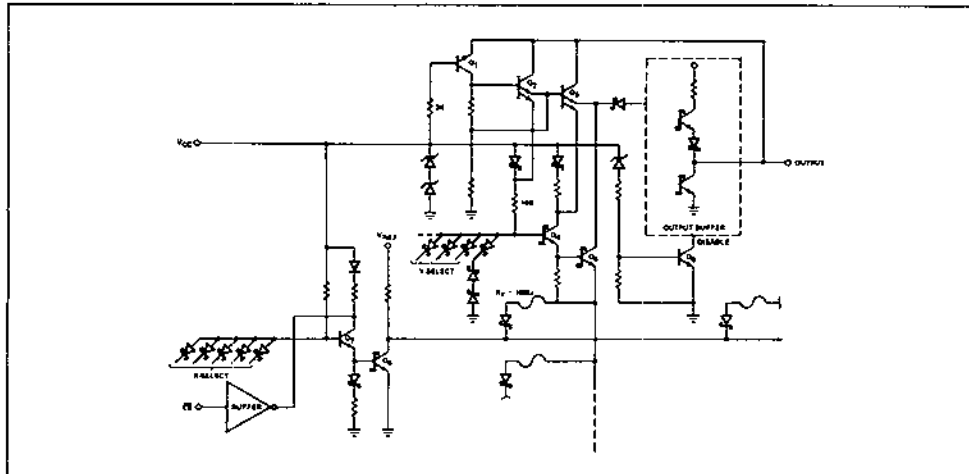
1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 4ms.

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AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE

