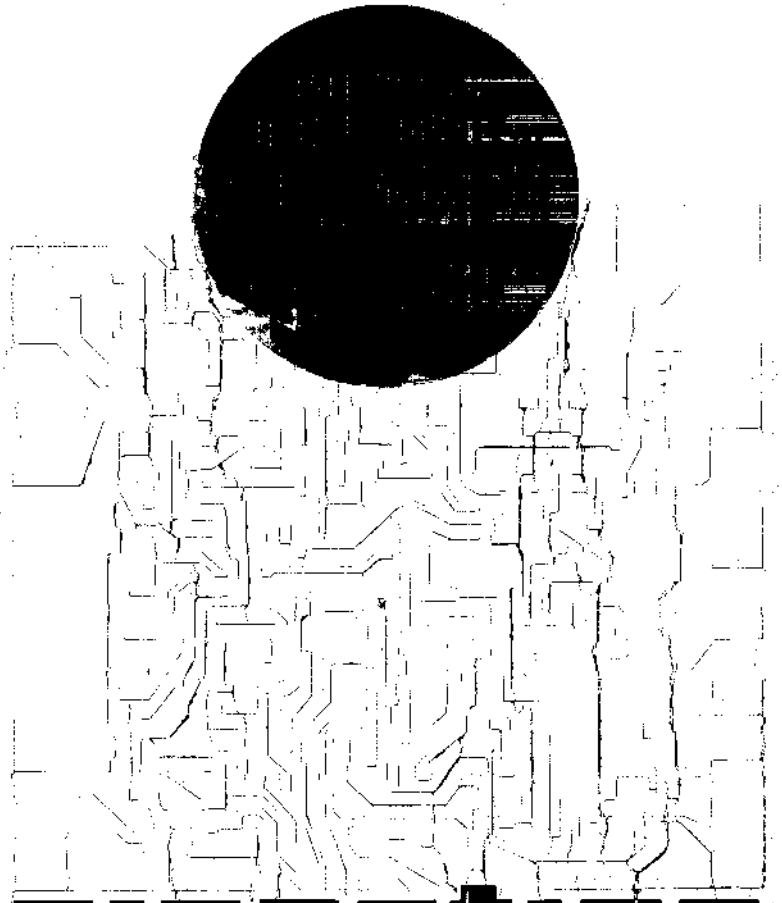

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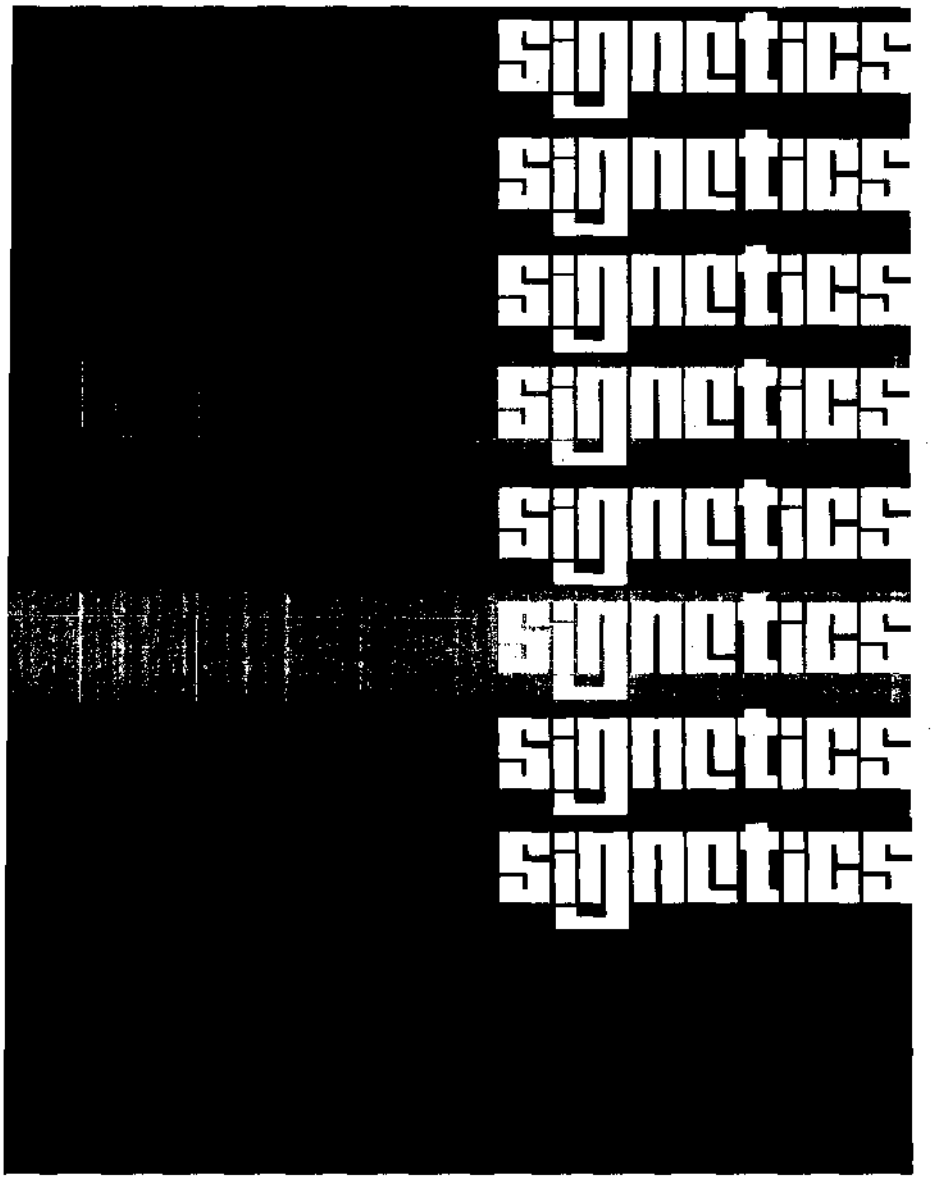

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* Nixie is a Burroughs Company trademark

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MILITARY PRODUCTS

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Class A, B and C of MIL-STD-883 are available on a standard basis from Signetics. This standardization

1 Simplifies or eliminates the need for customer spec generation,
2 Reduces cost with economies of scale,
3 Greatly reduces lead times with distributor inventories,
4 Reduces the need for minimum purchase orders due to distributor inventories.

Signetics designation for these classes are:

MIL-STD-883, Level A = RA
MIL-STD-883, Level B = RB
MIL-STD-883, Level C = RC

The RA, RB and RC flow are identical to that specified by MIL-STD-883. A detailed listing is in Section 8. These parts are distinguished from standard product as follows:

1. Individual serial number on each circuit (class A only)
2. The first letters of a part number are either RA (class A), RB (class B) or RC (class C); (i.e., RA 5400W)
3. Individual device variable parametic test data is supplied with each shipment. (class A only)
4. Generic data from GP B and C testing is available.

RA, RB, RC flow is available on all parts in the following product families:

5400
54H00
54S00
8000
8200
Linears
10100 (-30°C to +85°C only)

MILITARY PRODUCTS

JAN 38510 FAMILY

JAN 38510 PART NUMBERS - WHAT THEY MEAN

M38510	XXX	XX	X	X	X
Calls out MIL-M-38510 JAN I.C.	Refers to detail spec. 001, 002, 003	Refers to one of the devices on the detail spec. 01, 02, 03	Device class. Refers to level A, B, or C of MIL-STD-883	CASE OUTLINE A-1/4"X1/4" Flat Pack B-1/4"X1/8" Flat Pack C-Dual-In-Line 14 pin D-1/4"X3/8" Flat Pack E-Dual-In-Line, 16 pin F-16 pin Flat Pack G-8 lead metal can H-1/4"X14" lead Flat Pack I-10 lead metal can J-3/8"X5/8", 24 pin Flat Pack K-Dual-In-Line, 24 pin	LEAD MATERIAL A-Kovar or alloy 42 with hot solder dip B-Kovar or alloy 42 with tin plate C-Kovar or alloy 42 with gold plate

(JAN 38510 FAMILY)					
Slash Sheet	Device Type	Class	Case Outline	Lead Material & Finish	Basic Product
001	01	B, C	D, C	B, C	5430
001	02	B, C	D, C	B, C	5420
001	03	B, C	D, C	B, C	5410
001	04	B, C	D, C	B, C	5400
001	05	B, C	D, C	B, C	5404
001	06	B, C	D, C	B, C	5401
001	07	B, C	D, C	B, C	5405
001	08	B, C	C	B, C	5403
002	01	B, C	D, C	B, C	5472
002	02	B, C	D, C	B, C	5473
002	03	B, C	C	B, C	54107
002	04	B, C	E	B, C	5476
002	05	B, C	D, C	B, C	5474
002	06	B, C	D, C	B, C	5470
003	01	B, C	D, C	B, C	5440
003	02	B, C	D, C	B, C	5437
003	03	B, C	D, C	B, C	5438
004	01	B, C	D, C	B, C	5402
005	01	B, C	D, C	B, C	5450
005	02	B, C	D, C	B, C	5451
005	03	B, C	D, C	B, C	5453
005	04	B, C	D, C	B, C	5454
006	02	B, C	E	B, C	5483
007	01	B, C	D, C	B, C	5486
008	01	B, C	D, C	B, C	5406
008	02	B, C	D, C	B, C	5416
008	03	B, C	D, C	B, C	5407
008	04	B, C	D, C	B, C	5417
009	01	B, C	C	B, C	5495
009	02	B, C	E	B, C	5496
009	03	B, C	D, C ①	B, C	54164
010	01	B, C	E	B, C	5442
010	02	B, C	E	B, C	5443
010	03	B, C	E	B, C	5444
010	04	B, C	E	B, C	5445
010	05	B, C	E	B, C	54145
011	01	B, C	J, K ②	B, C	54181
012	01	B, C	D, C	B, C	54121
012	03	B, C	E	B, C	54123
013	01	B, C	D, C	B, C	5492
013	02	B, C	D, C	B, C	5493
013	03	B, C	E	B, C	54160
013	04	B, C	E	B, C	54161
013	05	B, C	E	B, C	54162
013	06	B, C	E	B, C	54163
022	01	B, C	D, C	B, C	54H72
022	02	B, C	D, C	B, C	54H73
022	03	B, C	D, C	B, C	54H74
023	01	B, C	D, C	B, C	54H30
023	02	B, C	D, C	B, C	54H20
023	03	B, C	D, C	B, C	54H10
023	04	B, C	D, C	B, C	54H00
023	05	B, C	D, C	B, C	54H04

① Not available in DB

② Not available in JB

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signetics

54/74 PRODUCT
SPECIFICATIONS

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54/74 Functional Index

SCHOTTKY (Continued)

54/7400 PRODUCT INFORMATION

GENERAL DESCRIPTION

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7V
Input Voltage, V_{in} (See Note 1	5.5V
Interemitter Voltage (See Note 2)	5.5V
Resistor Node Voltage, 54121, 74121 (See Note 1)	-5.5V to 7V
Operating Free-Air Temperature Range:	
Series 54 Circuits	-55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Output sink current tests 1 output at a time.

Series 54/74 Logic Family
The 54/74XX logic family is medium speed TTL, and high speed TTL integrated circuits. The family includes a multiple number of functions in a variety of packages. The 54XX devices are characterized for the full military temperature range of -55°C to +125°C. The 74XX devices are characterized for the limited temperature range of 0°C to +70°C.

INPUT CLAMPING DIODES
Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if -12mA of current is drawn.

DESIGN CONSIDERATIONS

Logic Definition
Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:
LOW VOLTAGE = LOGICAL "0"
HIGH VOLTAGE = LOGICAL "1"

Unused Inputs
For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4V but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package load, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to a supply voltage. Preferably, this voltage should be between 2.4V and 5.5V.
b. Connect unused inputs to a used input if maximum fanout of the driving output will not be exceeded. Each input presents a full load in the logical "1" state to the driving output.

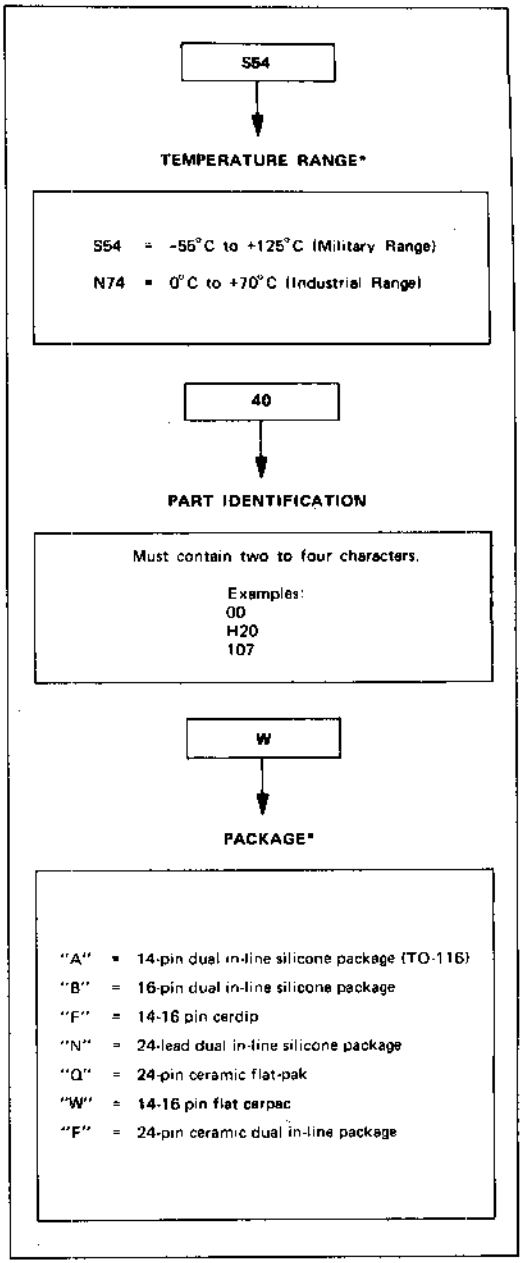
Input-Current Requirements
Input-current requirements reflect worst-case V_{CC} and temperature condition. Currents into the input terminals are specified as positive values.

54/74 Logic
Each input of the multiple-emitter input transistor that utilizes a 4 KΩ resistor requires no more than -1.6 mA flow out of the input at a logical "0" voltage level; therefore, one load (N = 1) for 54/74 logic is -1.6 mA maximum. Each input requires current into the input at a logical "1" voltage level. This current is 40μA maximum for each emitter input.

Fanout Capability
Fanout reflects the ability of an output to sink current from a number of loads (N) at a logical "0" voltage level and to supply current at a logical "1" voltage level. Each standard 54/74 output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate (54/7440) is capable of sinking current or supplying current to 30 loads (N = 30).

ELECTRICAL CHARACTERISTICS
These are guaranteed over the applicable operating free-air temperature range, unless otherwise noted, as shown in Section 2 of the handbook.

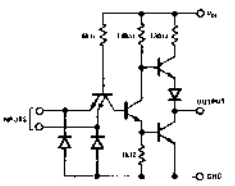
NOTE
Any product available in an A or B package can also be supplied in the F cerdip package.



*Availability of a circuit device in a particular package and temperature range is indicated on the appropriate device. Electrical Characteristics Data Sheet is shown in Section 2 of this handbook.

Manufacturer reserves the right to make design and process changes and improvements.

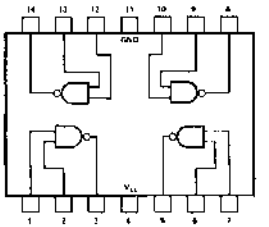
SCHEMATIC (each gate)



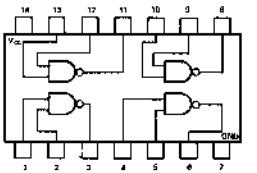
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5400 Circuits		4.5	5	5.5	V
N7400 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5400 Circuits	−55	25	125	°C
	N7400 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5400	−20		−55	mA
				N7400	−18		−55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		11	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

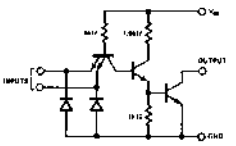
signetics QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S5401 N7401

S5401–A,F,W • N7401–A,F

DIGITAL 54/74 TTL SERIES

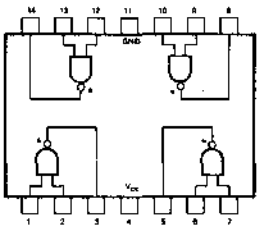
SCHEMATIC (each gate)



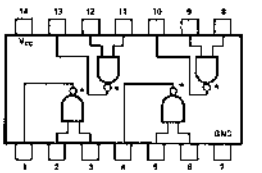
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



* No pull-up provided

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5401 Circuits		4.5	5	5.5	V
N7401 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5401 Circuits	-55	25	125	°C
	N7401 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	$V_{in(0)}$ = 0.8V			250	µA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			40	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX	V_{in} = 0		4	8	mA

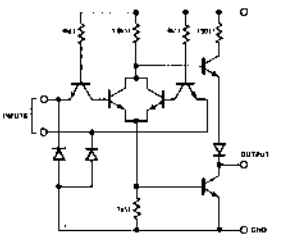
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 4 kΩ		35	45	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

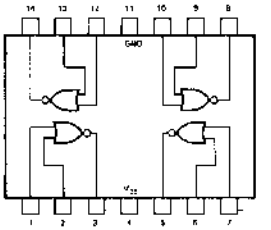
SCHEMATIC (each gate)



NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



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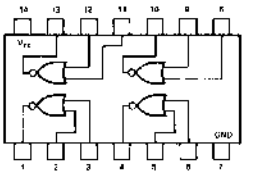


RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5402 Circuits	4.5	5	5.5	V
	N7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5402 Circuits	-55	25	125	°C
	N7402 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output Current†	V_{CC} = MAX		S5402 N7402	-20 -18		-55 -55	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		8	16	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

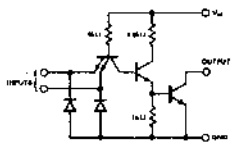
signetics QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S5403 N7403

S5403–A,F • N7403–A,F

DIGITAL 54/74 TTL SERIES

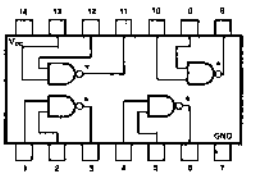
SCHEMATIC (each gate)



NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

A,F PACKAGE



* No pull-up provided

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5403 Circuits		4.5	5	5.5	V
N7403 Circuits		4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5403 Circuits	-55	25	125	°C
	N7403 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN,	V_{in} = 0.8V			0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 2V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	8	mA

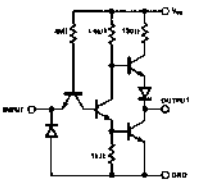
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C,

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	16	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 4 kΩ		35	46	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

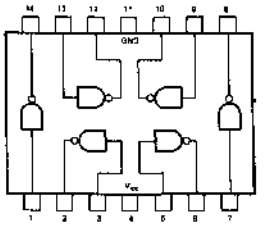
SCHEMATIC (each inverter)



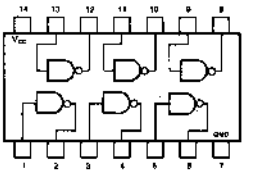
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5404 Circuits	4.5	5	5.5	V
	N7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5404 Circuits	-55	25	125	°C
	N7404 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400µA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	µA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5404	-20		-55	mA
				N7404	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

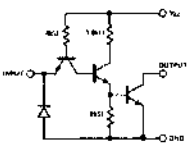
PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		6	12	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

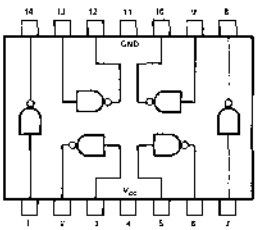
SCHEMATIC (each inverter)



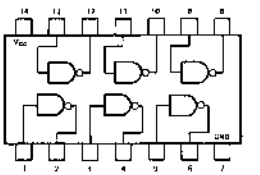
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5405 Circuits	4.5	5	5.5	V
	N7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5405 Circuits	-55	25	125	°C
	N7405 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = 5V, T_A = 25°C	V_{in} = 5V,		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = 5V, T_A = 25°C	V_{in} = 0,		6	12	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 4 kΩ		40	65	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C

signetics

HEX INVERTER BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5406–A,F,W • S5416–A,F,W • N7406–A,F • N7416–A,F

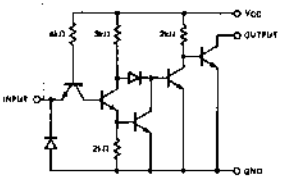
DIGITAL 54/74 TTL SERIES

S5406 S5416 N7406 N7416

DESCRIPTION

The 54/7406 and 54/7416 Hex Inverter Buffer/Drivers features standard TTL inputs with inverted high voltage, high current, open collector outputs for interface with MOS, lamps or relays. The 54/7406 minimum output breakdown is 30 volts and the 54/7416 minimum output breakdown is 15 volts.

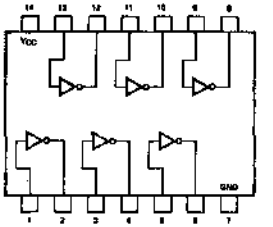
SCHEMATIC (each inverter)



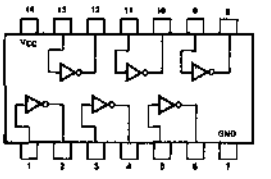
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A, F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5406, S5416			N7406, N7416			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, V_{OH}: S5406, N7406			30			30	
S5416, N7416			15			15	V
Low-level output current, I_{OL}			30			40	mA
Operating Free-air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_I = 0.8V, V_{OH} = MAX			250	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2V, I_{OL} = MAX			0.7	V
		V_{CC} = MIN, V_I = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V			40	µA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_I = 5V		27	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 110 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF, R_L = 110 Ω		14	23	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.

signetics

HEX BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5407
S5417
N7407
N7417

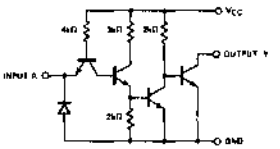
S5407–A,F,W • S5417–A,F,W • N7407–A,F • N7417–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7407 and 54/7417 Hex Buffer/Driver features standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays. The 54/7407 minimum output is 30 volts and the 54/7417 minimum output is 15 volts.

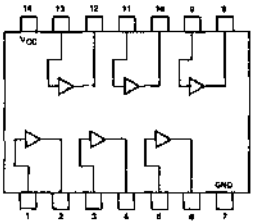
SCHEMATIC (each buffer/driver)



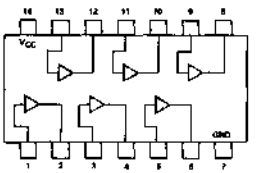
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5407, S5417			N7407, N7417			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, V_{OH}: S5407, N7407			30			30	
S5417, N7417			15			15	V
Low-Level Output Current, I_{OL}			30			40	mA
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_I = 2V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 0.8V, I_{OL} = MAX			0.7	V
		V_{CC} = MIN, V_I = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_I = 5V		29	41	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_I = 0		21	30	mA

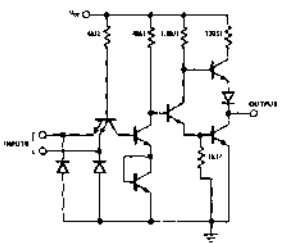
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 110Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 110Ω		20	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

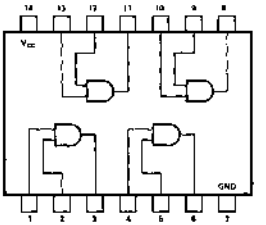
SCHEMATIC (each gate)



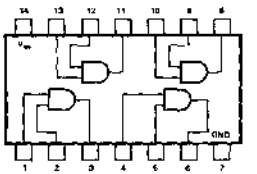
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5408 Circuits	4.5	5	5.5	V
	N7408 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5408 Circuits	−55	25	125	°C
	N7408 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −800µA	V_{in} = 2.0V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 0.8V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX	V_{in} = 0.4V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	µA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5408 N7408	−20 −18		−55 −55	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 5V		10	15	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		18	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		12	19	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		17.5	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C
† Not more than one output should be shorted at a time.

signetics

QUAD 2-INPUT AND GATE WITH OPEN COLLECTOR OUTPUTS

S5409 N7409

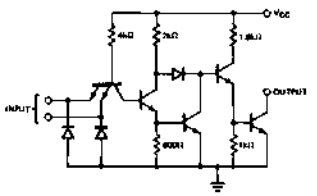
S5409—A,F,W • N7409—A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7409 Quad 2-Input AND Gate with open collector outputs provides the capability of expanding AND logic functions.

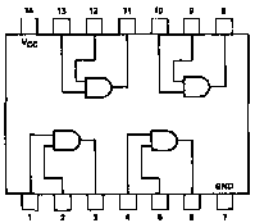
SCHEMATIC (each gate)



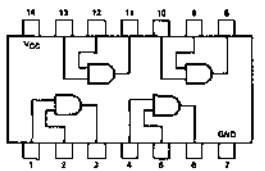
NOTE: Component values shown are nominal

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5409			N7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2V, V_{OH} = 5.5V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_I = 5V		10	15	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_I = 0		18	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 400 Ω		16	24	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (Cont'd)

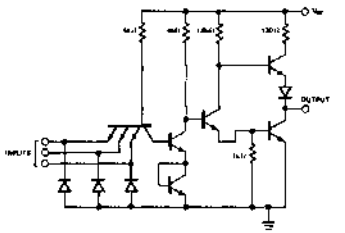
	PARAMETER	TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		3	6	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		11	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

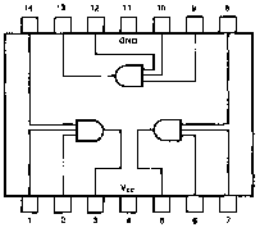
SCHEMATIC DIAGRAM



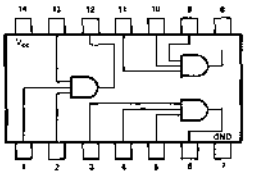
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5411 Circuits	4.5	5	5.5	V
	N7411 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5411 Circuits	-55	25	125	°C
	N7411 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800µA	V_{in} = 2.0V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 0.8V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX	V_{in} = 2.4V				40	µA
		V_{CC} = MAX	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5411	-20		-55	mA
				N7411	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 5V		7.5	12	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		13.5	20	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		12	19	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		17.5	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C
† Not more than one output should be shorted at a time.

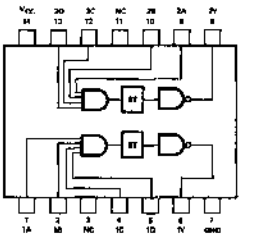
DESCRIPTION

The 5413 and 7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800mV.

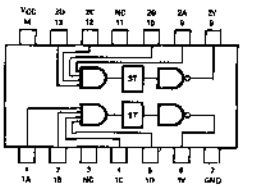
An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3% over the temperature range of −55°C to 125°C and the upper threshold changes by 1% over the same range. The 5413/7413 can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It can not be triggered from straight dc levels.

These circuits are fully compatible with most other TTL, DTL, or MSI circuits. The 5413 is characterized for operation over the full military temperature range of −55°C to 125°C; the 7413 is characterized for operation from 0°C to 70°C.

W PACKAGE



A, F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		5413			7413			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Fan-Out From Each Output, N	High Logic Level			20			20	
	Low Logic Level			10			10	
Operating Free-Air Temperature Range, T_A		-55	0	125	0	25	70	°C
Maximum Input Rise and Fall Times		No Restriction			No Restriction			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_{CC} = 5V		1.5	1.7	2	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5V		0.6	0.9	1.1	
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5V		0.4	0.8		V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12mA			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800μA	V_I = 0.6V,	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_I = 2V,		0.22	0.4	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5V,	$V_I = V_{T+}$		−0.65		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5V,	$V_I = V_{T-}$		−0.85		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V		-1	-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,		-18		-55	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	V_I = 0		14	23	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	V_I = 4.5V		20	32	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 400Ω		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 400Ω		15	22	ns

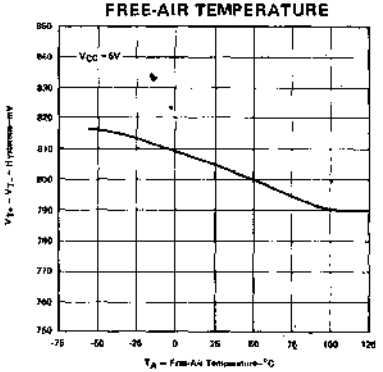
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

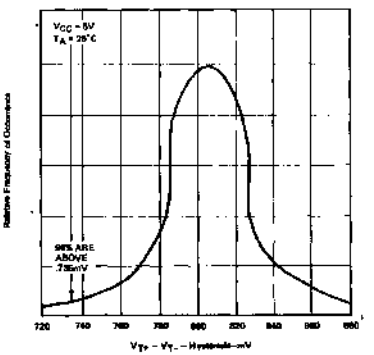
† Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

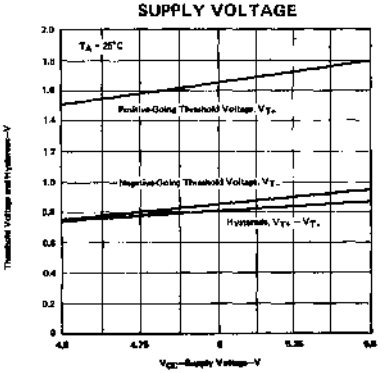
HYSTERESIS
VS
FREE-AIR TEMPERATURE



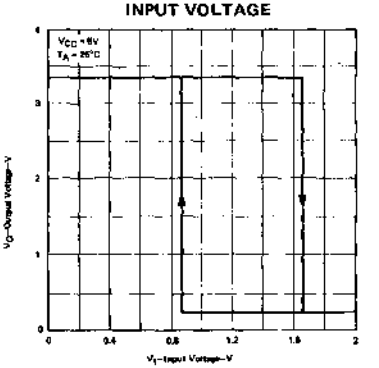
DISTRIBUTION OF UNITS
FOR HYSTERESIS



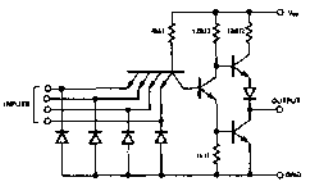
THRESHOLD VOLTAGES AND HYSTERESIS
VS
SUPPLY VOLTAGE



OUTPUT VOLTAGE
VS
INPUT VOLTAGE



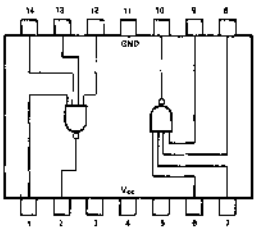
SCHEMATIC (each gate)



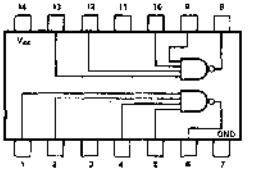
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5420 Circuits	4.5	5	5.5	V
	N7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5420 Circuits	-55	25	125	°C
	N7420 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		S5420	-20		-55	mA
				N7420	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		2	4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

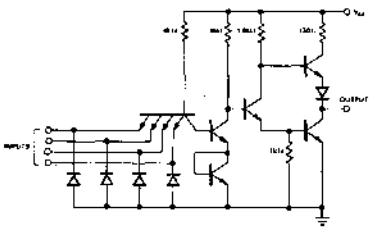
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

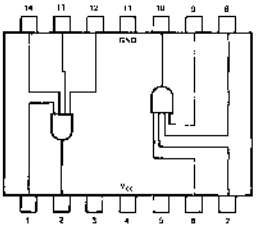
SCHEMATIC DIAGRAM



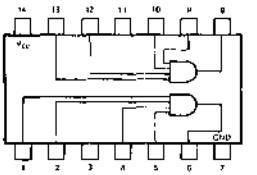
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5421 Circuits	4.5	5	5.5	V
	N7421 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5421 Circuits	-55	25	125	°C
	N7421 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800μA	V_{in} = 2.0V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 0.8V			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output	V_{CC} = MAX,		S5421	-20		-55	mA
				N7421	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 5V		5	8	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		9	13	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		12	19	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		17.5	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

signetics QUAD 2-INPUT HIGH VOLTAGE NAND GATE

S5426
N7426

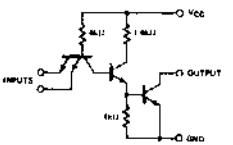
S5426—A,F • N7426—A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7426 Quad 2-Input NAND Gate features standard TTL inputs with high voltage (15 volts) open collector outputs for interface with MOS, lamps or relays.

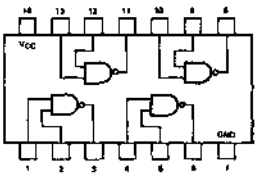
SCHEMATIC (each gate)



Note: Component values shown are nominal.

PIN CONFIGURATION

A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5426			N7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, V_{OH}			15			15	V
Low-Level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = 1mA	15			V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8V, V_{OH} = 12V			50	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_I = 0		4	8	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_I = 5V		12	22	mA

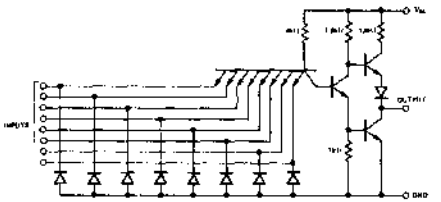
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 1kΩ		16	24	ns
t_{PHL}	Propagation delay time high-to-low-level output	C_L = 15pF,	R_L = 1kΩ		11	17	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

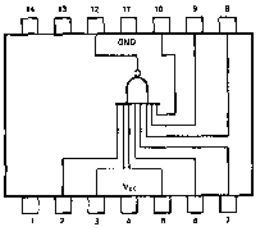
SCHEMATIC DIAGRAM



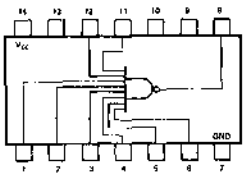
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5430 Circuits	4.5	5	5.5	V
	N7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5430 Circuits	-55	25	125	°C
	N7430 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,		S5430	-20		-55	mA
				N7430	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		3	6	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		1	2	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DESCRIPTION

The S5437/N7437 is a NAND Gate (output low only when all inputs are high) the same as N7400 except that it will drive 3 times as many loads. The S5438/N7438 and S5439/N7439 are also NAND Gates but have open-collectors similar to N7403.

The S5437/N7437, S5438/N7438 and S5439/N7439 contain four 2-input NAND gates in a package with a guaranteed fan-out of 30-series 54/74 loads in both the logical "1" (1.2mA), and logical "0" (48mA) states. The S5438/N7438 and S5439/N7439 have an open collector output for "WIRE-AND" applications but still retain the high sink current capability of the S5437/N7437.

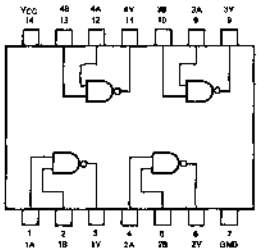
ABSOLUTE MAXIMUM RATINGS (over operating temperature ranges unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7V
Supply Voltage (See Note 1)	5.5V
Intermitter Voltage (See Note 2)	5.5V
Output Voltage (See Notes 1 and 3): S5438/N7438, S5439/N7439	5.5V
Operating Free-Air Temperature Range: S5437/S5438/S5439	-55°C to 125°C
N7437/N7438/N7439	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

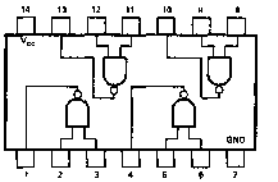
NOTES:
1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emmiter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

PIN CONFIGURATIONS

A, F, W PACKAGE
54/7437/38

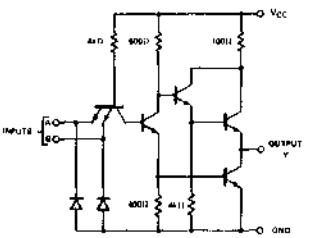


A, F PACKAGE
54/7439

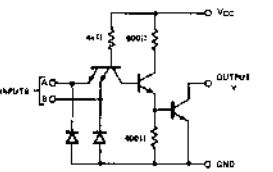


SCHEMATICS (each buffer)

S5437, N7437 (Totem-Pole Output)



S5438, N5438, S5439, N7439 (Open-Collector Output)



RECOMMENDED OPERATING CONDITIONS

	S5437, S5438, S5439			N7437, N7438, N7439			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			30			30	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = 1.2mA	V_{IL} = 0.8V	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 48mA	V_{IH} = 2V		0.22	0.4	V
I_I	Input current at max. input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-20 -18		-55 -55	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		9	15.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		34	54	mA

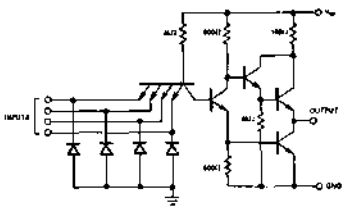
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER 54/7437		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 45pF, R_L = 133Ω		13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output			8	16	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

PARAMETER 54/7438/39		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 45pF, R_L = 133Ω		14	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output			11	18	ns

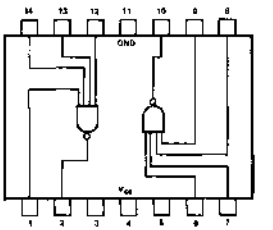
SCHEMATIC (each gate)



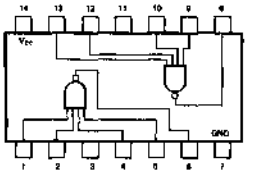
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5440 Circuits	4.5	5	5.5	V
	N7440 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				30	
Operating Free-Air Temperature Range, T_A:	S5440 Circuits	-55	25	125	°C
	N7440 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -1.2mA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 48mA	V_{in} = 2V,			0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		S5440	-20		-70	mA
				N7440	-18		-70	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	6.8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 133Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 133Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DESCRIPTION

The N7441B Nixie* Decoder/Driver is a one-out-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes.

It may also be utilized in driving relays or other high voltage interface circuitry. The element is designed using TTL techniques and is therefore completely compatible with DTL and TTL elements.

The specially designed output drivers provide the necessary stable output state. There are no input codes where all outputs are "off" or where more than one output can be turned "on".

RECOMMENDED OPERATING CONDITIONS

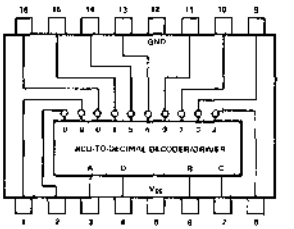
Supply Voltage V_{CC} (See Note 1)	4.75 to 5.25V
Maximum Voltage on any Output	70V

NOTE:

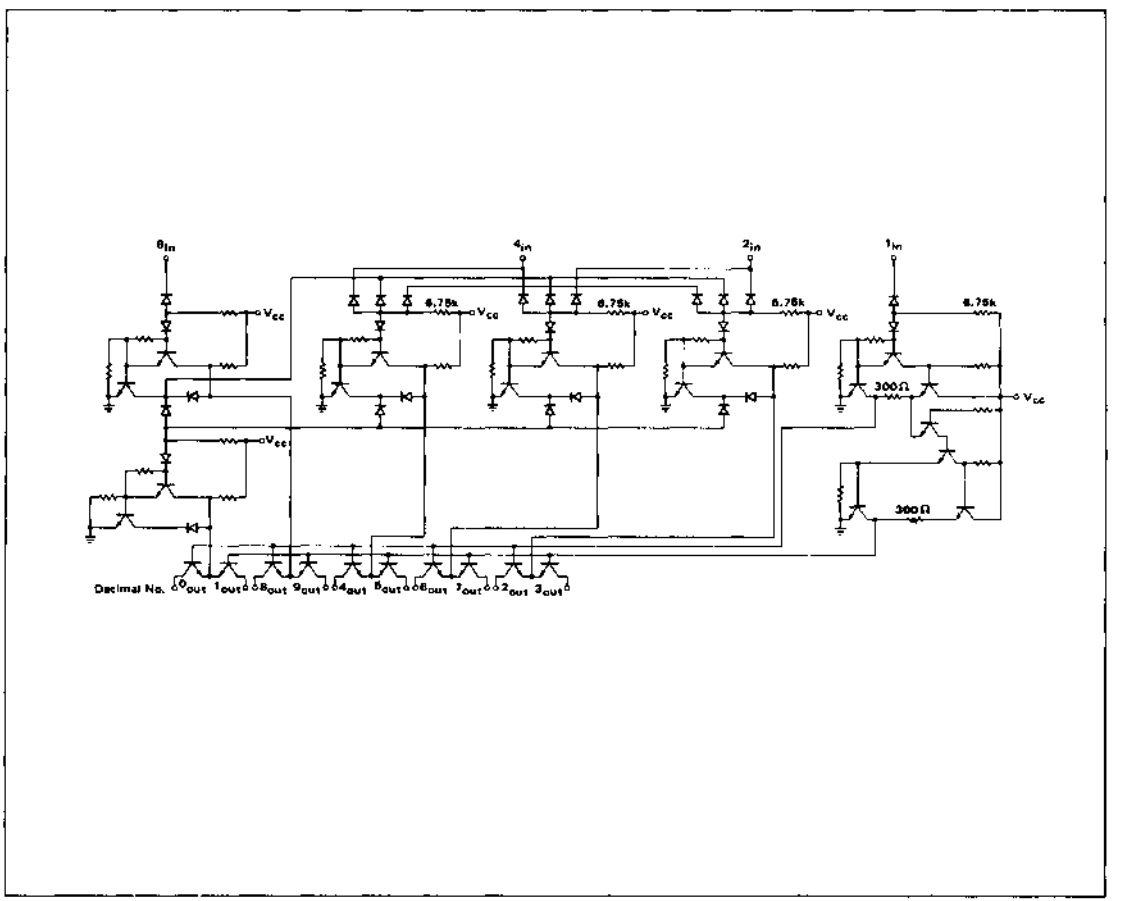
1. These voltage values are with respect to network ground terminal.

PIN CONFIGURATION

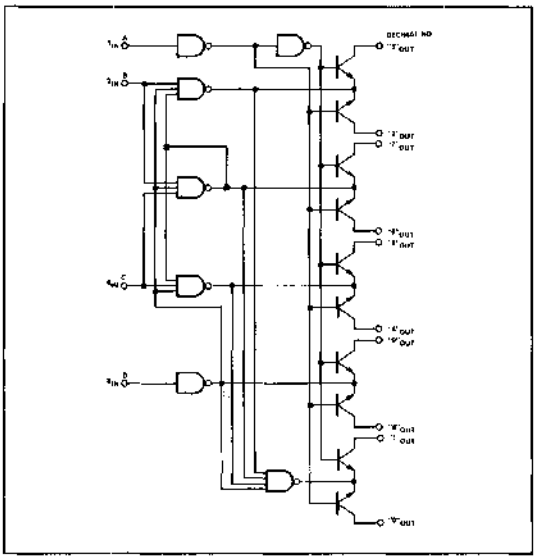
B PACKAGE



SCHEMATIC DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

† All other inputs are off.

ELECTRICAL CHARACTERISTICS, $T_A = 0^0$ C to 70^0 C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP*	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	V_{CC} = 4.75V		2			V
$V_{in(0)}$	Logical 0 input voltage	V_{CC} = 4.75V				0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.75V,	I_{on} = 7mA			2.5	V
I_{off}	Off-state reverse current	V_{CC} = 5.25V,	V_{out} = 55V			50	µA
		V_{CC} = 5.25V,	V_{out} = 70V			2	mA
$I_{in(1)}$	Logical 1 level input current at B, C, or D	V_{CC} = 5.25V,	V_{in} = 2.4V			40	µA
		V_{CC} = 5.25V,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at A	V_{CC} = 5.25V,	V_{in} = 2.4V			80	µA
		V_{CC} = 5.25V,	V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at B, C, or D	V_{CC} = 5.25V,	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A	V_{CC} = 5.25V,	V_{in} = 0.4V			−3.2	mA
I_{CC}	Supply current	V_{CC} = 5.25V			21	42	mA

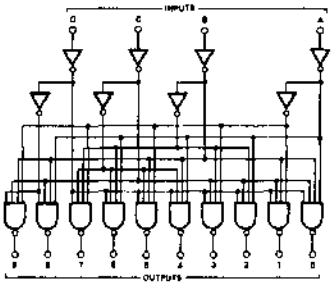
* All typical values are at V_{CC} = 5V, $T_A = 25^0$C.

*Trademark Burroughs Corporation.

DESCRIPTION

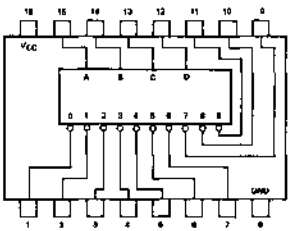
The 54/7442 BCD-to-Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7442 decodes a four bit BCD number to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5442/N7442 BCD INPUT

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5442 Circuits	4.5	5	5.5	V
N7442 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5442	-20		-55	mA
			N7442	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5442		28	41	mA
			N7442		28	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

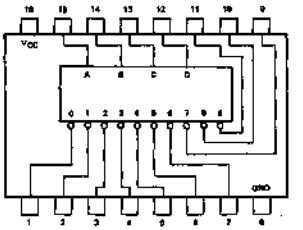
† Not more than one output should be shorted at a time.

DESCRIPTION

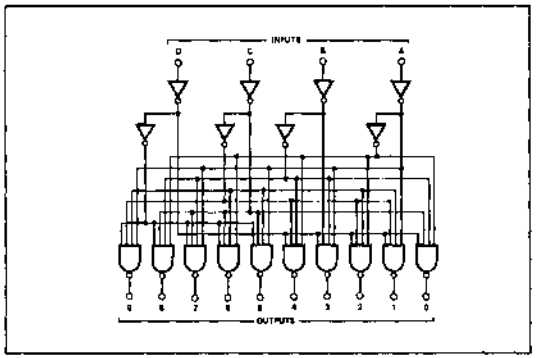
The 54/7443 Excess 3 Code to Decimal Decodar is a TTL MSI array utilized in decoding and logic conversion application. The 54/7443 decodes excess 3 code numbers to one of ten outputs.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

S5443/N7443 EXCESS INPUT

D	C	B	A
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5443 Circuits	4.5	5	5.5	V
N7443 Circuits	*4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5443	−20		−55	mA
			N7443	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5443		28	41	mA
			N7443		28	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

EXCESS 3-GRAY-TO-DECIMAL DECODER

S5444
N7444

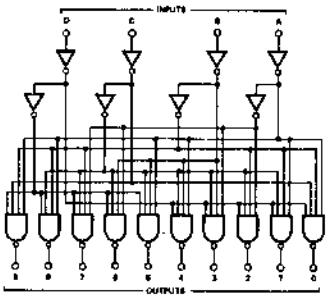
S5444–B,W • N7444–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

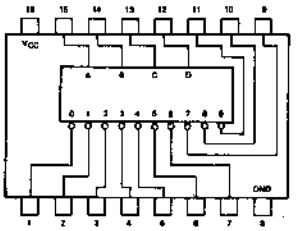
The 54/7444 Excess-3-Gray Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7444 decodes excess three gray code to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5444/N7444 EXCESS 3 GRAY INPUT

D	C	B	A
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
0	0	0	0
0	0	0	1
0	0	1	1

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5444 Circuits	4.5	5	5.5	V
N7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$		V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5444	-20		-55	mA
			N7444	-18		-55	mA
I_{CC}	Supply Current	V_{CC} = MAX,	S5444		28	41	mA
			N7444		28	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

BCD-TO-DECIMAL DECODER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5445 S54145 N7445 N74145

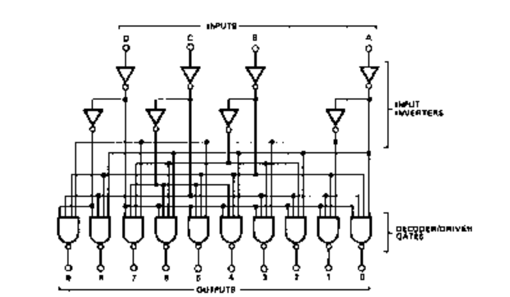
S5445–F,W • S54145–F,W • N7445–B • N74145–B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7445 and 54/74145 BCD-to-Decimal Decoder/Driver is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The 54/7445 minimum output breakdown is 30 volts and the 54/74145 minimum output breakdown is 15 volts.

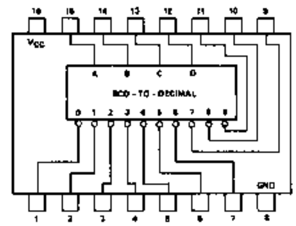
LOGIC DIAGRAM



NOTE: 1. These voltage values are with respect to network ground terminal.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S5445, S54145 Circuits	4.5	5	5.5	V
	N7445, N74145 Circuits	4.75	5	5.25	V
Voltage on any Output	S5445, N7445 Circuits			30	V
	S54145, N74145 Circuits			15	V

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
V_{on}	On-state output voltage	V_{CC} = MIN, I_{sink} = 80mA		0.5	0.9	V
		V_{CC} = MIN, I_{sink} = 20mA			0.4	V
V_{off}	Off-state output voltage (S5445 or N7445)	V_{CC} = MAX, I_{off} = 250 μA	30			V
V_{off}	Off-state output voltage (S54145 or N74145)	V_{CC} = MAX, I_{off} = 250 μA	15			V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, S5445, S54145		43	62	mA
		V_{CC} = MAX, N7445, N74145		43	70	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time logical 1 level	C_L = 15pF, R_L = 100 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF, R_L = 100 Ω			50	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

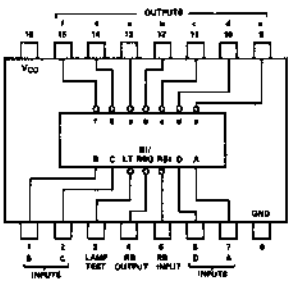
The 7446 and 7447 BCD-to-Seven Segment Decoder/Driver are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

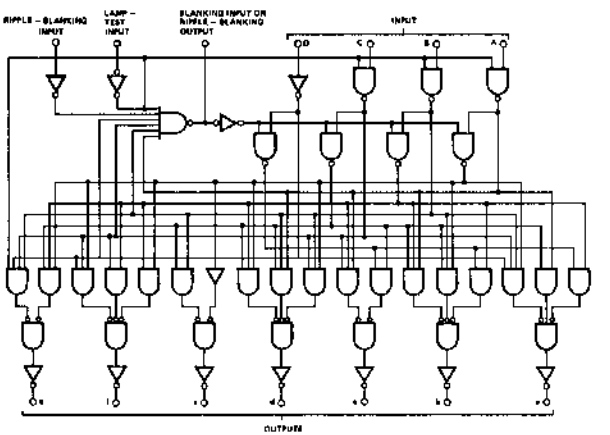
The 7446 and 7447 provide bare collector output transistors for directly driving lamps. The output transistor breakdown of the 7446 is 30 volts and the 7447 is 15 volts.

PIN CONFIGURATION

B PACKAGE



LOGIC DIAGRAM



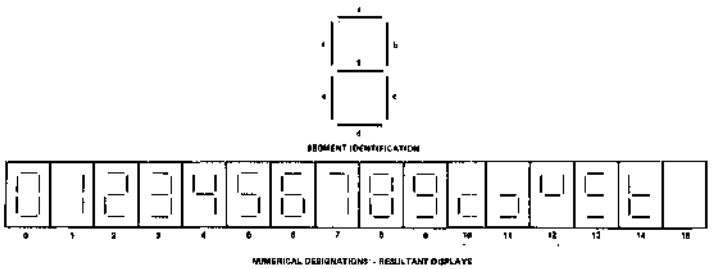
TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:

1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

SEGMENT IDENTIFICATION



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): N7446, N7447 Circuits	4.75	5	5.25	V
Continuous Voltage at Outputs a through g: N7446 Circuits			30	V
N7447 Circuits			15	V
Normalized Fan-Out From Outputs a through g to Series 54/74 loads: N7446, N7447 Circuits			12	
Normalized Fan-Out From BI/RBO Node to Series 54/74 loads: N7446, N7447 Circuits			5	
Output Sink Current, I_{sink}: N7446, N7447 Outputs a through g			20	mA
N7446, N7447, BI/RBO Node			8	mA

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any point	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	V_{CC} = MIN			0.8	V
V_{on}	On-state output voltage at outputs a through g	V_{CC} = MIN, I_{sink} = 40mA		0.27	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	V_{CC} = MIN, I_{sink} = 8mA		0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g (S5446 and N7446 only)	V_{CC} = MAX, I_{off} = 250 A	30			V
V_{off}	Off-state output voltage at outputs a through g (S5447 and N7447 only)	V_{CC} = MAX, I_{off} = 250 A	15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	V_{CC} = MIN, I_{load} = 200 A	2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V			40 1	uA mA
I_{OS}	Short-circuit output current at BI/RBO node	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	V_{CC} = MAX N7446, N7447		53	90	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	C_L = 15pF, R_L = 280 Ω			100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

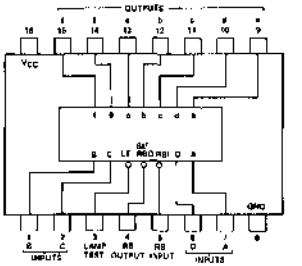
The 7448 BCD-to-Seven Segment Decoder/Driver is a TTL monolithic device consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

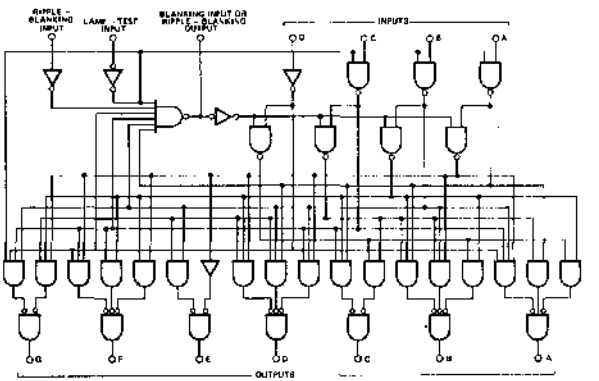
The 7448 has resistor pull up on the outputs to provide source current to drive interface elements.

PIN CONFIGURATIONS

B PACKAGE



LOGIC DIAGRAM



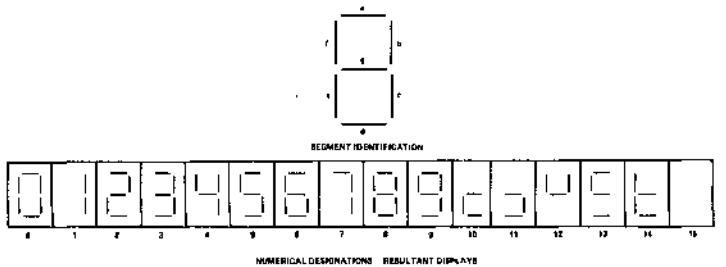
TRUTH TABLE

	INPUTS							OUTPUTS							
FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	x	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	x	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	x	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	x	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	x	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	x	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	x	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	x	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	x	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	x	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	x	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	x	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	x	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	x	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	x	1	1	1	1	1	0	0	0	0	0	0	0	
BI	x	x	x	x	x	x	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	x	x	x	x	x	1	1	1	1	1	1	1	1	4

NOTES:

1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition), all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 1.

SEGMENT IDENTIFICATION



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): N7448 Circuit	4.75	5	5.25	V
Normalized Fan-Out From Outputs a through g to Series 54/74 loads: N7448 Circuits			4	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads: N7448 Circuits			5	
Output Sink Current, I_{sink}: N7448 Outputs a through g			6.4	mA
N7448 BI/RBO Node			8	mA

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	V_{CC} = MIN			0.8	V
$V_{out(0)}$	Logical 0 output voltage at any output	V_{CC} = MIN, I_{sink} = MAX		0.27	0.4	V
$V_{out(1)}$	Logical 1 level output voltage at outputs a through g	V_{CC} = MIN, I_{load} = -400 μA	2.4	4.2		V
$V_{out(1)}$	Logical 1 level output at BI/RBO node	V_{CC} = MIN, I_{load} = 200 μA	2.4	3.7		V
I_{load}	Load current available at outputs a through g	V_{CC} = MIN, V_{out} = 0.85V	-1.3	-2		mA
$I_{in(0)}$	Logical 0 level input current of any input except BI/RBO node.	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current at any output	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	S5448		53	76	mA
		N7448		53	90	mA

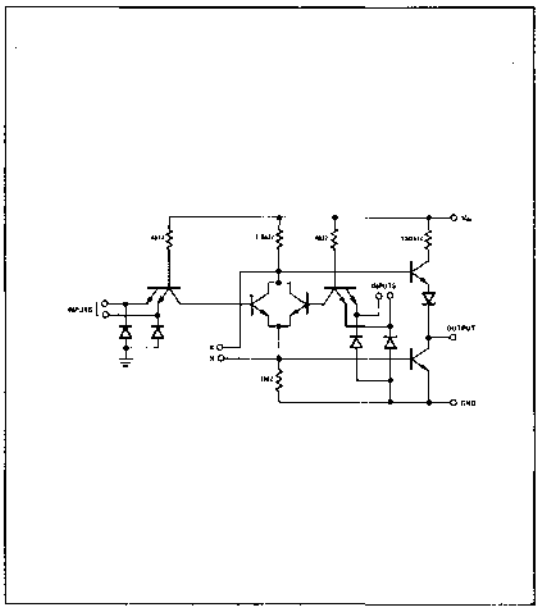
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	C_L = 15pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	C_L = 15pF			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	C_L = 15pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	C_L = 15pF			100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

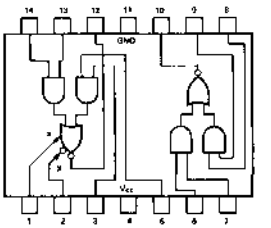
** All typical values are at V_{CC} = 5V, T_A = 25°C.

SCHEMATIC (each gate)

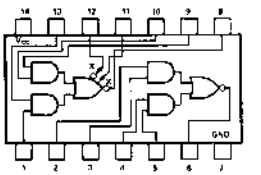


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the S5451 and N7451.
5. A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	S5450, S5451 Circuits	4.5	5	5.5	V
	N7450, N7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5450, S5451 Circuits	-55	25	125	°C
	N7450, N7451 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5450, S5451	-20		-55	mA
				N7450, N7451	-18		-55	
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V			7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0			4	8	mA

ELECTRICAL CHARACTERISTICS (S5450 circuits) using expander inputs, V_{CC} = 4.5V, T_A = -55° C

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA, R_1 = 0	I_1 = 0.41mA,			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -0.15mA	I_1 = 0.15mA,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA, R_1 = 138Ω	I_1 = 0.3mA,		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (N7450 circuits) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

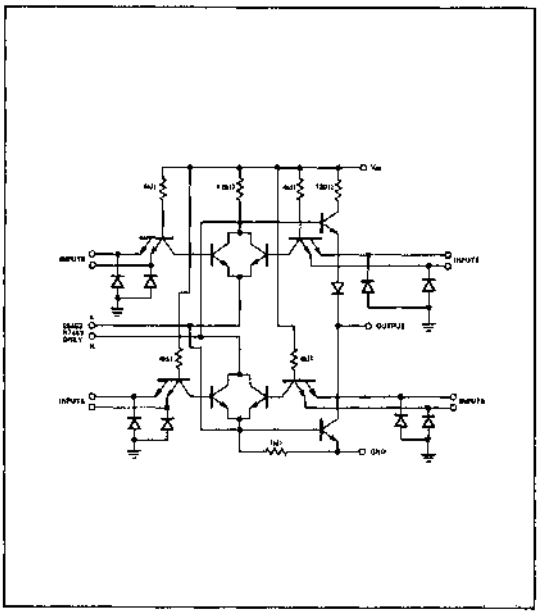
PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA, R_1 = 0	I_1 = 0.62mA,			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -270μA	I_1 = 270μA,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA, R_1 = 130Ω	I_1 = 0.43mA,		0.22	0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

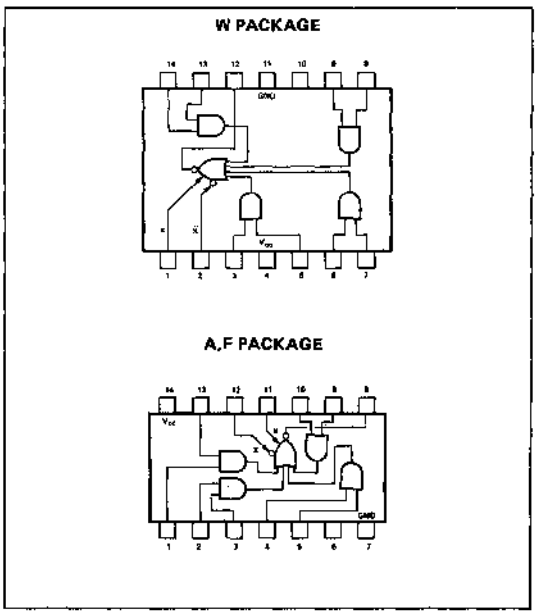
PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS



NOTES:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the S5454 and N7454.
5. A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5453, S5454 Circuits	4.5	5	5.5	V
N7453, N7454 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A: S5453, S5454 Circuits	-55	25	125	°C
N7453, N7454 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = 5.5V		S5453, S5454	-20		-55	mA
				N7453, N7454	-18		-55	
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V			5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0			4	8	mA

ELECTRICAL CHARACTERISTICS (S5453 circuits) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA				2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA,	I_1 = 0.41mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -0.15mA	I_1 = 0.15mA,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA,	I_1 = 0.3mA,	R_1 = 138Ω		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (N7453 circuits) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

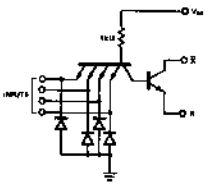
PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA				3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA,	I_1 = 0.62mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -270μA	I_1 = 270μA,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA,	I_1 = 0.43mA,	R_1 = 130Ω		0.22	0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
** All typical values are at V_{cc} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

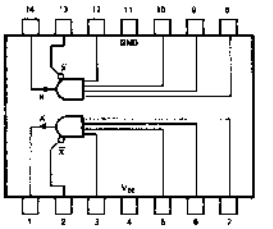
SCHEMATIC (each expander)



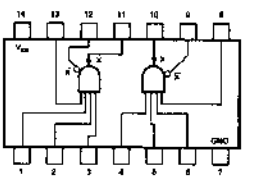
NOTES:
1. Connect to X input of S5450 or S5453 circuit.
2. Connect to $\overline{X}$ input of S5450 or S5453 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S5450 or one S5453 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = –55°C to 125°C)

	PARAMETER	TEST CONDITIONS			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.5V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, R = 1.1 kΩ,	V_{in} = 2V, T_A = –55°C	V_1 = 1V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 1.2 kΩ,	V_{in} = 0.8V, T_A = –55°C	V_1 = 4.5V,			150	μA
I_{on}	On-state output current	V_{CC} = 4.5V, T_A = –55°C	V_{in} = 2V,	V_1 = 1V,	–0.3			mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 0.4V				–1.6	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

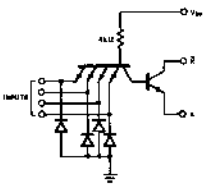
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 2.4V				40	µA
		V_{CC} = 5.5V,	V_{in} = 5.5V				1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V,	V_{in} = 5V,	V_1 = 0.85V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.5V,	V_{in} = 0,	V_1 = 0.85V		2	4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through S5450 or S5453 circuit)	C_L = 15pF,	R_L = 400Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through S5450 or S5453 circuit)	C_L = 15pF,	R_L = 400Ω		15	30	ns

** All typical values are at V_{CC} = 5V, T_A = 25°C.

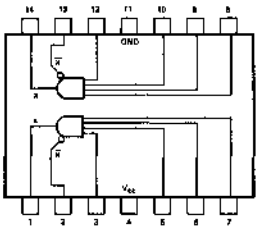
SCHEMATIC (each expander)



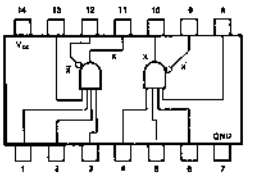
NOTES:
1. Connect to X input of N7450 or N7453 circuit.
2. Connect to $\overline{X}$ input of N7450 or N7453 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.75 to 5.25V
Maximum number of expanders that may be fanned-in to one N7460 or one N7453 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.75V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.75V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.75V, R = 1.1 kΩ,	V_{in} = 2V, T_A = 0°C	V_I = 1V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.75V, R = 1.2 kΩ,	V_{in} = 0.8V, T_A = 0°C	V_I = 4.5V,			270	μA
I_{on}	On-state output current	V_{CC} = 4.75V,	V_{in} = 2V,	V_I = 1V	-0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 2.4V				40	μA
		V_{CC} = 5.25V,	V_{in} = 5.5V				1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.25V, V_{in} = 5V, V_1 = 0.85V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.25V, V_{in} = 0 V_1 = 0.85V		2	4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through N7460 or N7463)	C_L = 15pF, R_L = 400Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through N7460 or N7463)	C_L = 15pF, R_L = 400Ω		15	30	ns

** All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

TRUTH TABLE

LOGIC

J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

$J = J_1 J_2 J^*$ $K = K_1 K_2 K^*$

n is time prior to clock

n+1 is time following clock

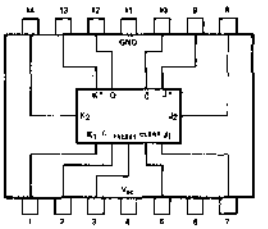
† Both outputs in 0 state

POSITIVE LOGIC

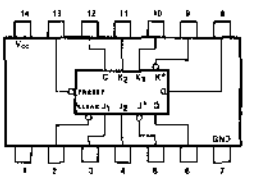
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

PIN CONFIGURATIONS

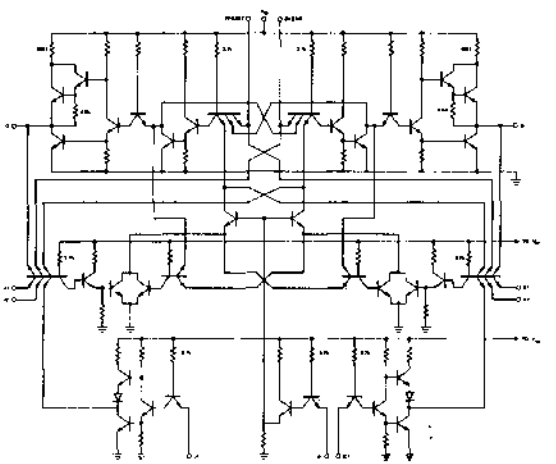
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



NOTE: Component values are typical.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5470 Circuits	4.5	5	5.5	V
	N7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5470 Circuits	−55	25	125	°C
	N7470 Circuits	0	25	70	°C
Normalized Fanout from each Output, N				10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$			5	150	ns
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5470	−20		−75	mA
				N7470	−18		−75	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			13	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	35		MHz
t_{setup}	Minimum Input Setup time	C_L = 15pF,	R_L = 400Ω		10	20	ns
t_{hold}	Minimum input hold time	C_L = 15pF,	R_L = 400Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	18	50	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DESCRIPTION

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

TRUTH TABLE

LOGIC

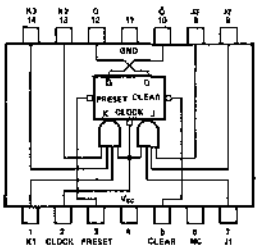
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:

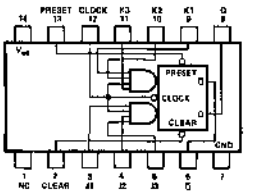
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC = No Internal Connection.

PIN CONFIGURATIONS

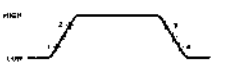
W PACKAGE



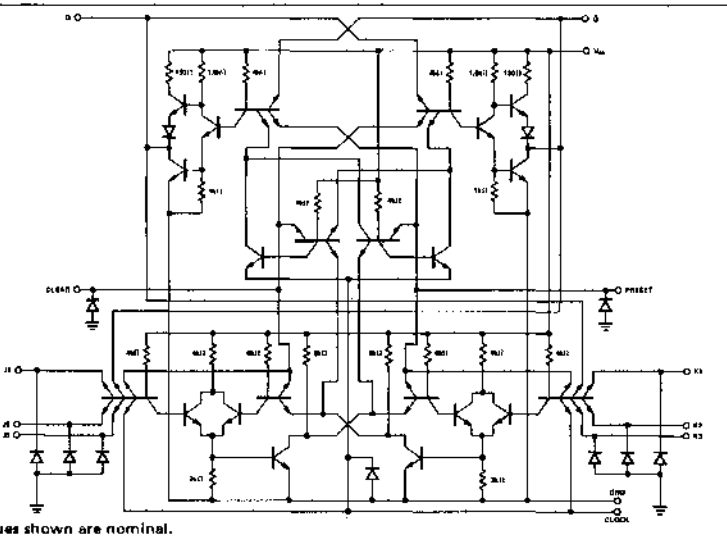
A,F PACKAGE



CLOCK WAVEFORM



SCHEMATIC DIAGRAM



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5472 Circuits	4.5	5	5.5	V
	N7472 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5472 Circuits	-55	25	125	°C
	N7472 Circuits	0	25	70	°C
Normalized Fan-Out From each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5472	-20		-57	mA
				N7472	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			10	20	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DESCRIPTION

The S5473/N7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

TRUTH TABLE

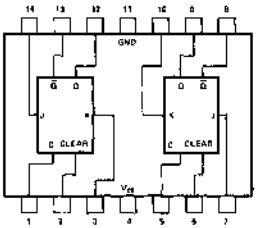
LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

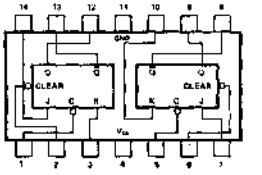
NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

PIN CONFIGURATIONS

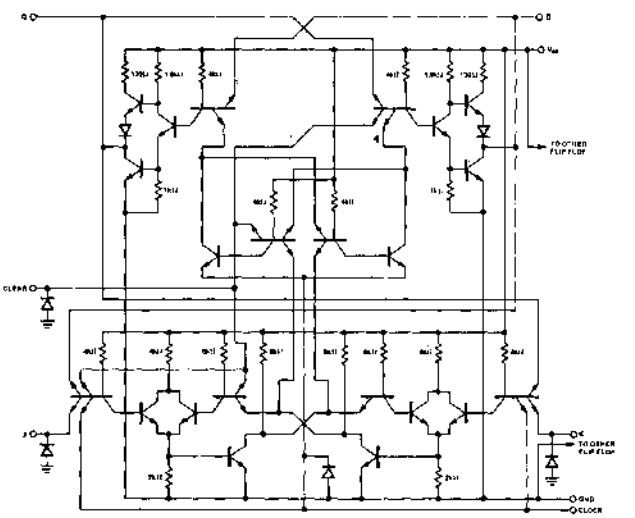
W PACKAGE



A,F PACKAGE



SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5473 Circuits		4.5	5	5.5	V
N7473 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5473 Circuits	-55	25	125	°C
	N7473 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(Clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN,					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5473	-20		-57	mA
				N7473	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{CC}=5V, T_A=25° C, N=10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25° C.
† Not more than one output should be shorted at a time.

DESCRIPTION

The S5474/N7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

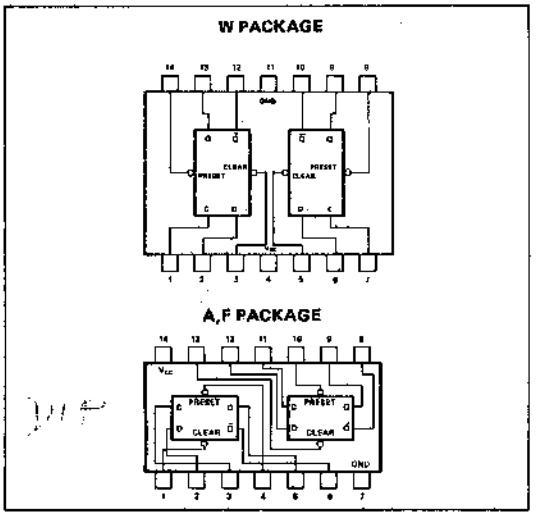
TRUTH TABLE

D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

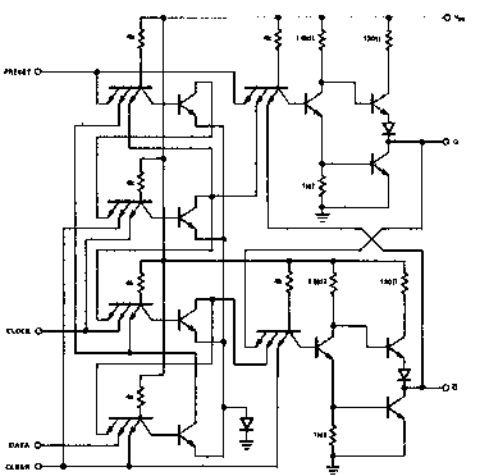
† Both outputs in 1 state
n is time prior to clock
n+1 is time following clock

PIN CONFIGURATIONS



POSITIVE LOGIC – Low input to preset sets Q to logical 1. Low input to clear sets Q to logical 0; Preset and clear are independent of clock

SCHEMATIC DIAGRAM



NOTE: 1/2 of unit shown. Component values are typical.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5474 Circuits		4.5	5	5.5	V
N7474 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5474 Circuits	-55	25	125	°C
	N7474 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V				120	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5474	-20		-57	mA
				N7474	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			17	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	25		MHz
t_{setup}	Minimum input setup time	C_L = 15pF,	R_L = 400Ω		15	20	ns
t_{hold}	Minimum input hold time	C_L = 15pF,	R_L = 400Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	20	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

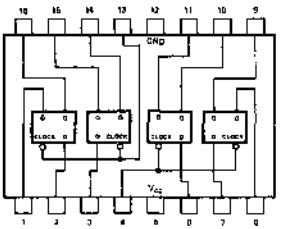
DESCRIPTION

The S5475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and $\bar{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

PIN CONFIGURATIONS

B PACKAGE



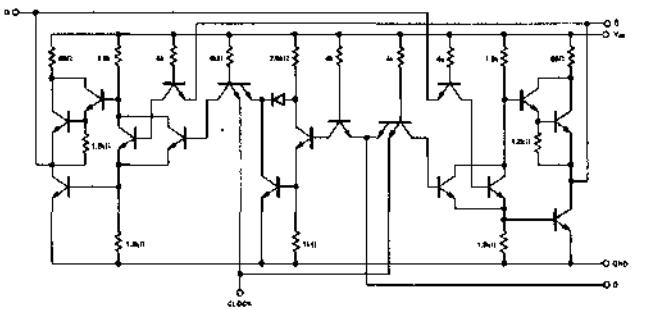
TRUTH TABLE

LOGIC

(Each Latch)		
t_n	t_{n+1}	
D	Q	$\bar{Q}$
1	1	0
0	0	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse
3. These voltages are with respect to network ground terminal.

SCHEMATIC (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): S5475 Circuits	4.5	5	5.5	V
N7475 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Outputs			10	
Operating Free-Air Temperature Range, T_A: S5475 Circuits	-55	25	125	°C
N7475 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,				-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX	V_{in} = 2.4V			160	μA
		V_{CC} = MAX	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	S5475	-20		-75	mA
		V_{out} = 0	N7475	-18		-75	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5475		32	46	mA
			N7475		32	53	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

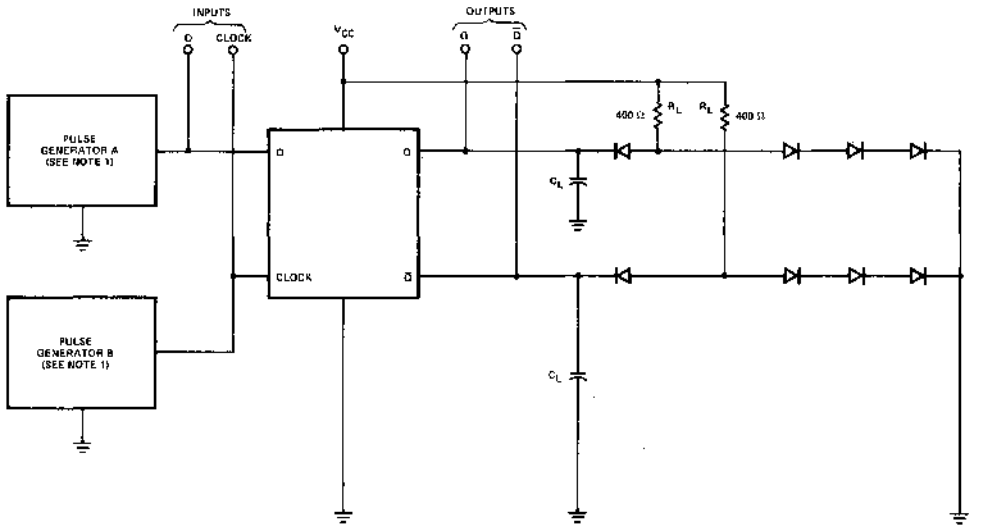
PARAMETER		TEST CONDITIONS NOTE A		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(D-\overline{Q})}$	Propagation delay time to logical 1 level from D input to $\overline{Q}$ output	C_L = 15pF,	R_L = 400Ω		24	40	ns
$t_{pd0(D-\overline{Q})}$	Propagation delay time to logical 0 level from D input to $\overline{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C-\overline{Q})}$	Propagation delay time to logical 1 level from clock input to $\overline{Q}$ output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-\overline{Q})}$	Propagation delay time to logical 0 level from clock input to $\overline{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.
¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

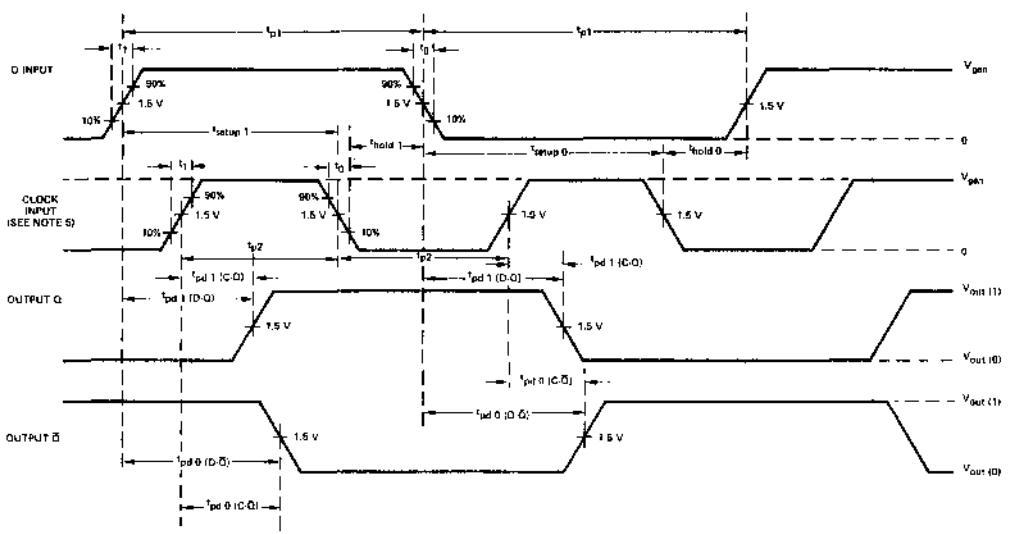
Note A AC Test circuit, voltage waveforms and switching times are given on page 2-76.

SWITCHING CHARACTERISTICS*

TEST CIRCUIT



VOLTAGE WAVEFORMS AND SWITCHING TIMES



NOTES:
1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.
5. When measuring $t_{pd1(D\text{-}Q)}$ and $t_{pd0(D\text{-}Q)}$ (or $t_{pd0(D\text{-}\bar{Q})}$ and $t_{pd1(D\ \bar{Q})}$ for the S5474/N7475), clock input must be held at logical 1.

†Complementary Q outputs are on the S5475/N7475 only.

signetics

DUAL J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

S5476 N7476

S5476–B,F,W • N7476–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5476B/N7476B J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

TRUTH TABLE

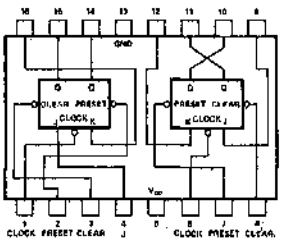
LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

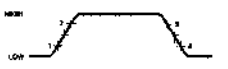
NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

PIN CONFIGURATIONS

B,F,W PACKAGE



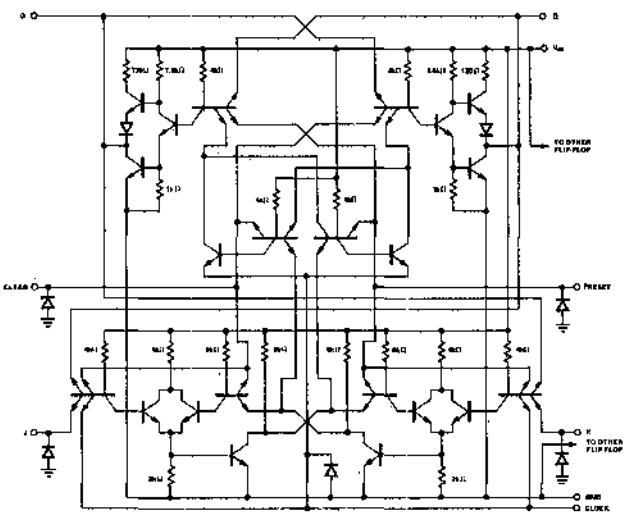
CLOCK WAVEFORM



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent from clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5476 Circuits	4.5	5	5.5	V
	N7476 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5476 Circuits	-55	25	125	°C
	N7476 Circuits	0	25	70	°C
Normalized Fanout from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5476 N7476	-20 -18		-57 -57	mA
I_{CC}	Supply current (each flip-flop)	V_{CC} = MAX,	V_{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

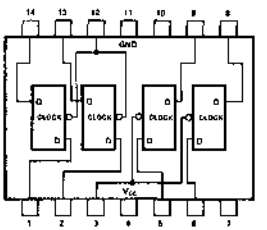
DESCRIPTION

The S5477Q/N7477Q is a monolithic, quadruple, bistable latch with Q outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

PIN CONFIGURATIONS

W PACKAGE



TRUTH TABLE

LOGIC

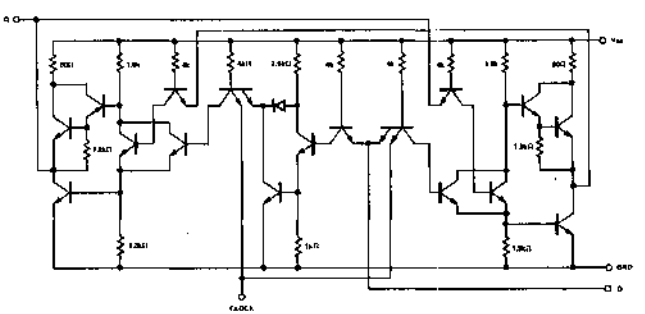
(Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S5477 Circuits	4.5	5	5.5	V
	N7477 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5477 Circuits	-55	25	125	°C
	N7477 Circuits	0	25	70	°C

SCHEMATIC (each latch)



ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,					−6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX, V_{in} = 2.4V,					160	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, V_{out} = 0		S5477	−20		−75	mA
				N7477	−18		−75	mA
I_{CC}	Supply current	V_{CC} = MAX,		S5477		32	46	mA
				N7477		32	53	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS NOTE A		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

NOTE A: AC Test circuit, voltage waveforms and switching times are given on page 2-76

signetics

GATED FULL ADDER

S5480
N7480

S5480—A,F,W • N7480—A,F

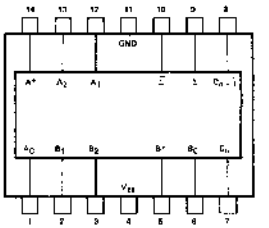
DIGITAL 54/74 TTL SERIES

DESCRIPTION

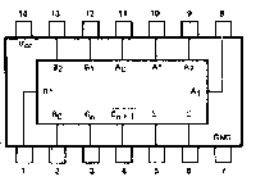
The S5480/N7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



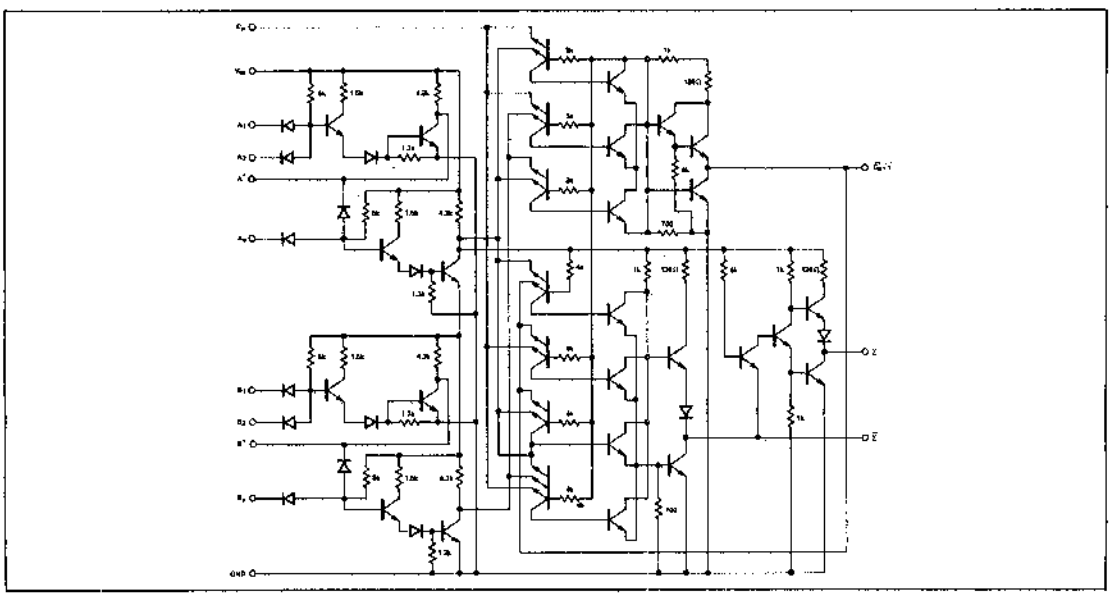
TRUTH TABLE (See Notes 1,2, and 3)

LOGIC

C_n	B	A	$C_{\overline{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES:
1. $A = \overline{A^* \cdot A_c}$, $B = \overline{B^* \cdot B_c}$ where $A^* = \overline{A_1 \cdot A_2}$, $B^* = \overline{B_1 \cdot B_2}$.
2. When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively, must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively, must be open or used to perform Dot-OR logic.
4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5480 Circuits	4.5	5	5.25	V
	N7480 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Outputs:	$\overline{C_n}$+1, N			5	
	Σ or $\overline{\Sigma}$, N			10	
	A* or B*, N			3	
Operating Free-Air Temperature Range, T_A:	S5480 Circuits	-55	25	125	°C
	N7480 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN			2.4	3.6		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN				0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A* or B*	V_{CC} = MAX,	V_{in} = 0.4V				-2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	V_{CC} = MAX,	V_{in} = 0.4V				-8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	V_{CC} = MAX, V_{CC} = MAX	V_{in} = 2.4V V_{in} = 5.5V				15 1	μA mA
$I_{in(1)}$	Logical 1 level input current at C_n	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				200 1	μA mA
I_{OS}	Short circuit output current at Σ or $\overline{\Sigma}$†	V_{CC} = MAX,		S5480 N7480	-20 -18		-57 -57	mA mA
I_{OS}	Short circuit output current at $\overline{C_{n+1}}$†	V_{CC} = MAX,		S5480 N7480	-20 -18		-70 -70	mA mA
I_{CC}	Supply current	V_{CC} = MAX,		S5480 N7480		21 21	31 35	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	C_L = 15pF,	R_L = 780Ω		13	17	ns
t_{pd0}			C_L = 15pF,	R_L = 780Ω		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	C_L = 15pF,	R_L = 780Ω		18	25	ns
t_{pd0}			C_L = 15pF,	R_L = 780Ω		38	55	ns
t_{pd1}	A_C	Σ	C_L = 15pF,	R_L = 400Ω		52	70	ns
t_{pd0}			C_L = 15pF,	R_L = 400Ω		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	C_L = 15pF,	R_L = 400Ω		38	55	ns
t_{pd0}			C_L = 15pF,	R_L = 400Ω		56	75	ns
t_{pd1}	A_1	A*	C_L = 15pF			48	65	ns
t_{pd0}			C_L = 15pF			17	25	ns
t_{pd1}	B_1	B*	C_L = 15pF			48	65	ns
t_{pd0}			C_L = 15pF			17	25	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

DESCRIPTION

The 54/7483 is a 4-Bit Binary Full Adder for adding two four bit binary numbers. A Carry Look Ahead circuit is included to provide minimum carry propagation delays.

Propagation delays of carry-in to carry-out is typically 12 nsec.

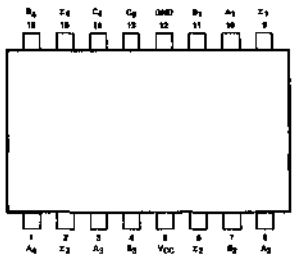
TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

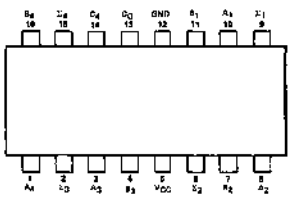
NOTES:
Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4 are then used to determine outputs Σ_3, Σ_4, and C_4.

PIN CONFIGURATIONS

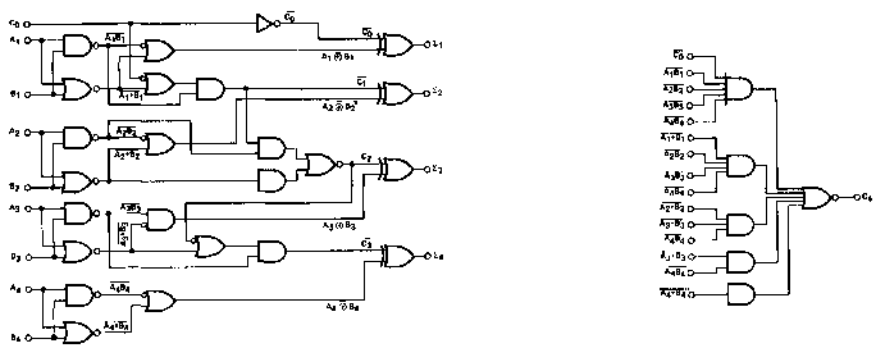
W PACKAGE



B,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	S5483 Circuits	4.5	5	5.5	V
	N7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:	C_4			5	
	Σ_1, Σ_2, Σ_3 or Σ_4			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN				0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current A_1, A_3, B_1, B_3, or C_0	V_{CC} = MAX, V_{in} = 2.4V				80	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current A_2, A_4, B_2, or B_4	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} @ MAX, V_{in} = 5.5V				1	mA
I_{OS}	Short-circuit output current at Σ_1, Σ_2, Σ_3, or Σ_4 †	V_{CC} = MAX	S5483	-20		-55	mA
			N7483	-18		-55	mA
I_{OS}	Short-circuit output current at C_4 †	V_{CC} = MAX	S5483	-20		-70	mA
			N7483	-18		-70	mA
I_{CC}	Supply current	V_{CC} = MAX,			58	79	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, unless otherwise noted N = 10

PARAMETER ‡		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	From C_0 to 1	C_L = 50pF,	R_L = 400Ω		23	34	ns
t_{pd0}	From C_0 to 1	C_L = 50pF,	R_L = 400Ω		20	34	ns
t_{pd1}	From C_0 to 2	C_L = 50pF,	R_L = 400Ω		24	35	ns
t_{pd0}	From C_0 to 2	C_L = 50pF,	R_L = 400 Ω		22	35	ns
t_{pd1}	From C_0 to 3	C_L = 50pF,	R_L = 400Ω		30	50	ns
t_{pd0}	From C_0 to 3	C_L = 50pF,	R_L = 400Ω		24	40	ns
t_{pd1}	From C_0 to 4	C_L = 50pF,	R_L = 400Ω		30	50	ns
t_{pd0}	From C_0 to 4	C_L = 50pF,	R_L = 400Ω		28	50	ns
t_{pd1}	From C_0 to C_4	C_L = 50pF,	R_L = 780Ω		12	20	ns
t_{pd0}	From C_0 to C_4	C_L = 50pF,	R_L = 780Ω		12	20	ns
t_{pd1}	From A_2 or B_2 to 2	C_L = 50pF,	R_L = 400Ω			40	ns
t_{pd0}	From A_2 or B_2 to 2	C_L = 50pF,	R_L = 400Ω			35	ns
t_{pd1}	From A_4 of B_4 to 4	C_L = 50pF,	R_L = 400Ω			40	ns
t_{pd0}	From A_4 of B_4 to 4	C_L = 50pF,	R_L = 400Ω			35	ns

‡ T_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

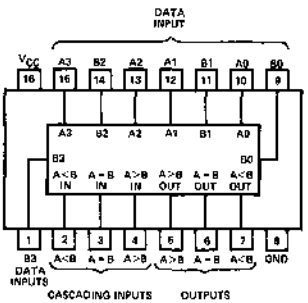
NOTE 1: These voltage values are with respect to network ground terminal.

DESCRIPTION

The S5485 and N7485 perform magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. When cascaded, the total time for comparison is the function of the word length; however, only a two-gate-level delay (12 ns) is added for each four-bit expansion.

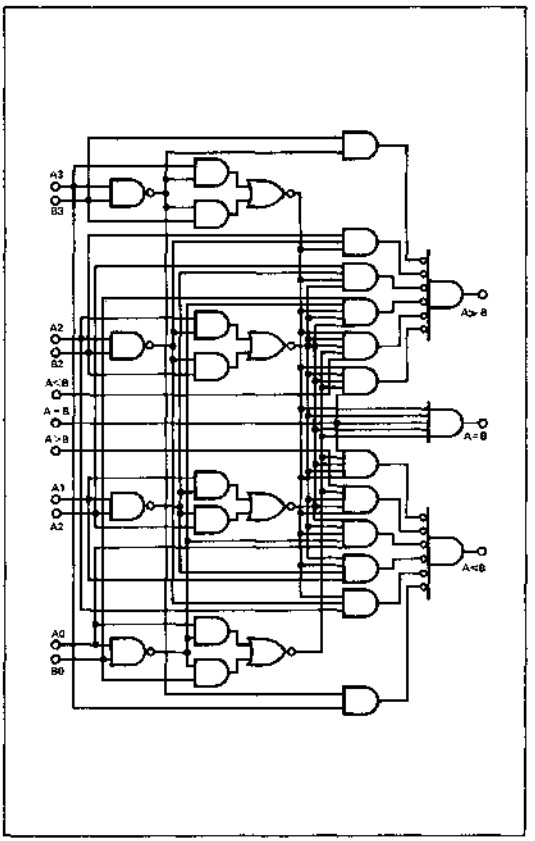
These circuits are completely compatible with most TTL and DTL families. Typical average power dissipation is 275 milliwatts. The S5485 is characterized for operation over the full military temperature range of −55°C to 125°C; The N7485 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION



Positive logic: See truth table

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = High level, L = Low level, X = Irrelevant.

RECOMMENDED OPERATING CONDITIONS

	S5485			N7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 2.4 V				40	μA
		all other inputs					120	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		all other inputs					−4.8	
I_{OS}	Short-circuit output current‡		V_{CC} = MAX, V_O = 0	S5485	−20		−55	mA
				N7485	−18		−55	
I_{CC}	Supply current		V_{CC} = MAX, See Note 1			55	88	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.
NOTE 1: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

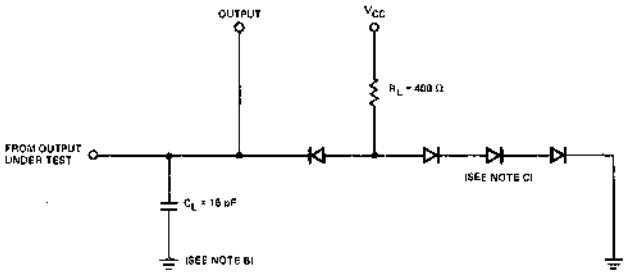
SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A > B, A < B	1	C_L = 15 pF, R_L = 400 Ω, See Figure 1		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			7	11	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

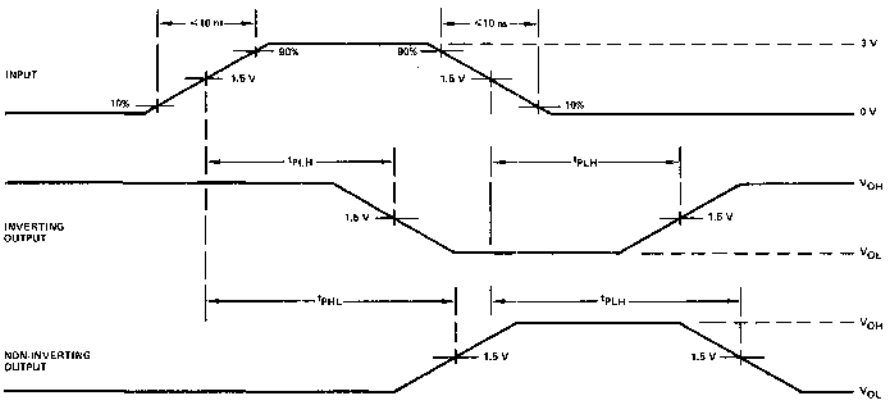
t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. Input pulses are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance
C. All diodes are 1N3064

FIGURE 1. PROPAGATION DELAY TIMES

signetics

QUAD 2-INPUT EXCLUSIVE OR GATE

S5486
N7486

S5486–A,F,W • N7486–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

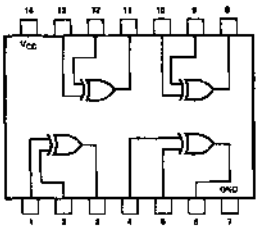
The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function $\overline{A}B + A\overline{B}$ at the output.

TRUTH TABLE

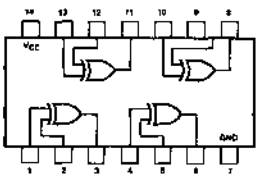
INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	S5486 Circuits	4.5	5	5.5	V
	N7486 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each output, N:	Logical 0			10	
	Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, $V_{in(1)}$ = 4.5V, $V_{in(0)}$ = 0	S5486	-20		-55	mA
			N7486	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V	S5486		30	43	mA
			N7486		30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	C_L = 15pF,	R_L = 400		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	C_L = 15pF,	R_L = 400		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (Other input high)	C_L = 15pF,	R_L = 400		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	C_L = 15pF,	R_L = 400		18	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

\+ Not more than one output should be shorted at a time.

DESCRIPTION

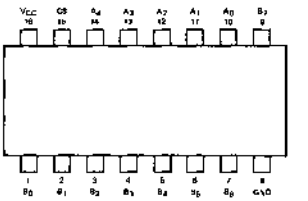
The 7488 is a TTL 256-Bit Read Only Memory organized as 32 word with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Select input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Select input is taken high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-OR operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

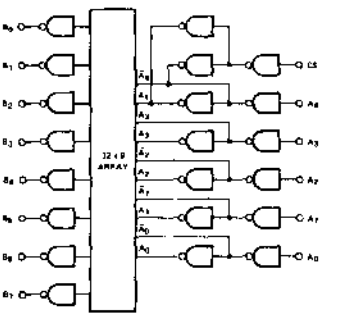
Customer may specify patterns for the 256-Bit Read Only Memory by completing the truth table/order blank.

PIN CONFIGURATIONS

B,W PACKAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
See 8223 or 8224 Data Sheet for Pin-for-Pin Replacement					

256-BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

	INPUTS						OUTPUTS							
WORD	A_4	A_3	A_2	A_1	A_0	ENABLE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1

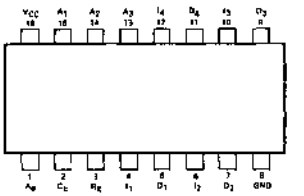
DESCRIPTION

The 7489 is a TTL 64-Bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 7489 is ideally suited for application in scratch pads and high speed buffer memories.

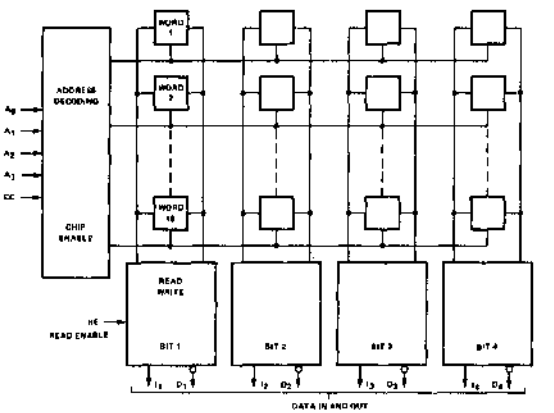
Words are selected through a 4-input binary decoder when the chip select input (CE) is at logic "0". Data is written into the memory when Read Enable (RE) is at logic "0" and read from the memory when RE is at logic "1".

PIN CONFIGURATION

B PACKAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

See 8225 Data Sheet for Pin-for-Pin Replacement

DESCRIPTION

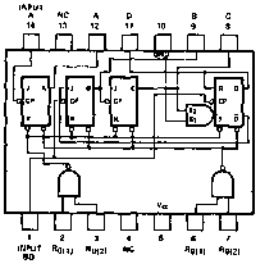
The S5490/N7490 is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical "0" or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional "0" reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

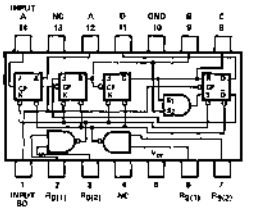
The 5490/7490 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 160mW.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



LOGIC TRUTH TABLES

BCD COUNT SEQUENCE (See Note 1)

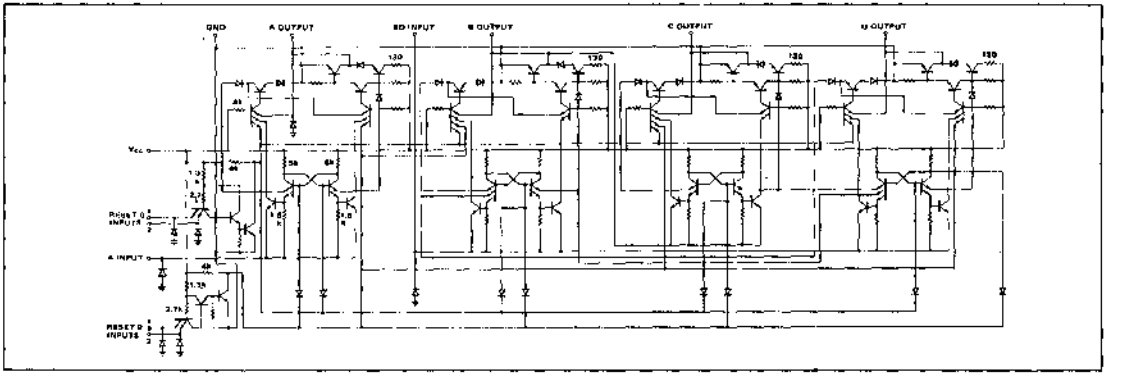
COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NOTES:
1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5490 Circuits	4.5	5	5.5	V
	N7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns
Operating Free-Air Temperature Range, T_A:	S5490 Circuits	−55	25	125	°C
	N7490 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input BD	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				160 1	μA mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	V_{CC} = MAX,	V_{in} = 0.4V				−6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0V	S5490 N7490	−20 −18		−57 −57	mA mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5490 N7490		32 32	46 53	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	C_L = 15pF,	R_L = 400Ω		60	100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DESCRIPTION

The S5491/N7491 is a monolithic serial-in, serial-out 8-bit shift register utilizing high-speed transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes the S5491/N7491 to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the S5470/N7470 flip-flop and the S5474/N7474 dual D-type flip-flop.

TRUTH TABLE

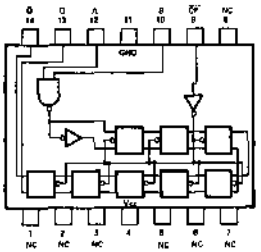
LOGIC

t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

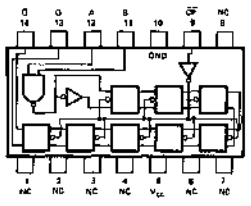
NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+8} = bit time after 8 clock pulse.

PIN CONFIGURATIONS

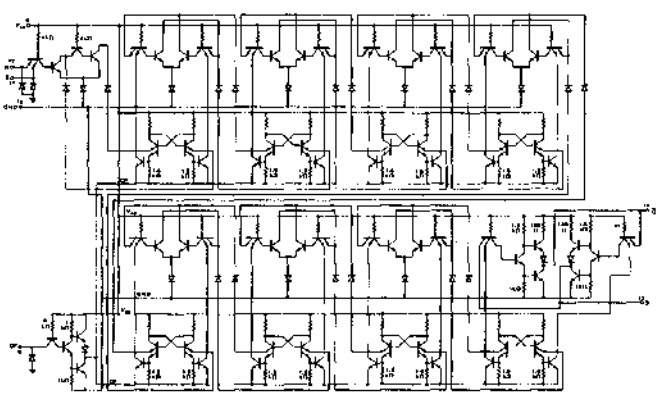
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5491 Circuits		4.5	5	5.5	V
N7491 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5491 Circuits	−55	25	125	°C
	N7491 Circuits	0	25	70	°C
Width of Clock Pulse, $t_{p(clock)}$		25			ns
Input Setup Time, t_{setup}		25			ns
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	S5491	−20		−57	mA
				N7491	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5491		35	50	mA
				N7491		35	58	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		27	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

S5492 N7492

S5492–A,F,W • N7492–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5492/N7492 is a high-speed monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flops outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

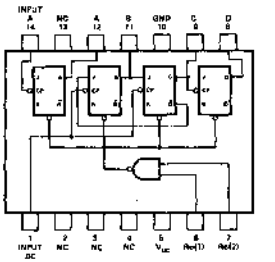
1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous division of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency division of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

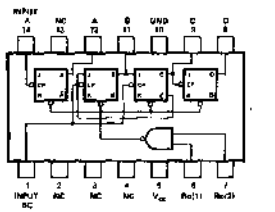
The S5492/N7492 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 155mW.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



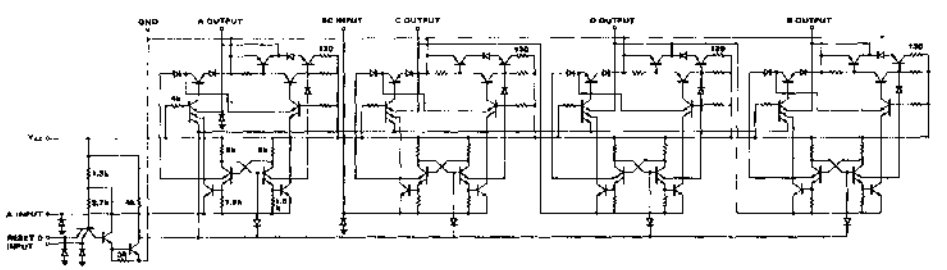
TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

COUNT	OUTPUT			
	D	C	B	A
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5492 Circuits		4.5	5	5.5	V
N7492 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5492 Circuits	−55	25	125	°C
	N7492 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input BC	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				160 1	μA mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	V_{CC} = MAX,	V_{in} = 0.4V				−6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	S5492 N7492	−20 −18		−57 −57	mA mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5492 N7492		31 31	44 51	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

signetics

4-BIT BINARY COUNTER

S5493
N7493

S5493—A,F,W • N7493—A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5493/N7493 is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

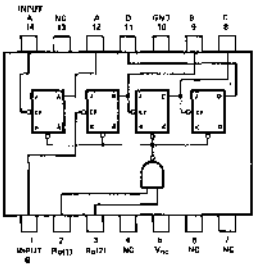
1. When used as a 4-bit ripple-through counter output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

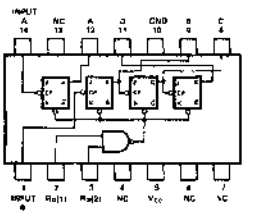
The S5493/N7493 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 32mW per flip-flop (128mW total).

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



TRUTH TABLE (See Notes 1 and 2)

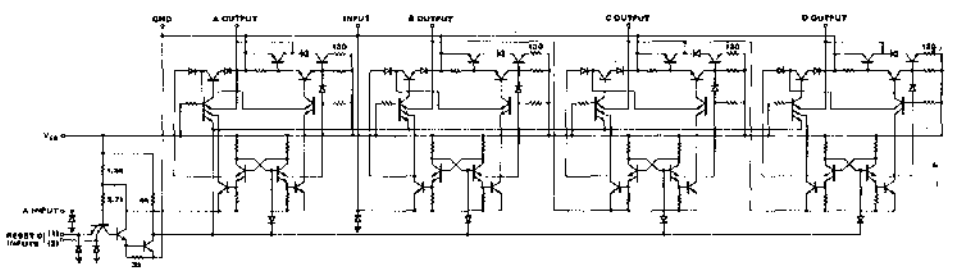
LOGIC

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

COUNT	OUTPUT			
	D	C	B	A
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5493 Circuits		4.5	5	5.5	V
N7493 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5493 Circuits	-55	25	125	°C
	N7493 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{out} = 0	S5493 N7493	-20 -18		-57 -57	mA mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5493 N7493		32 32	46 53	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		75	135	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

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4-BIT SHIFT REGISTER (PARALLEL-IN, SERIAL-OUT)

S5494—B,F,W • N7494—B,F

DIGITAL 54/74 TTL SERIES

S5494 N7494

DESCRIPTION

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

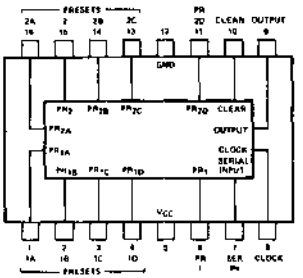
The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The output of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

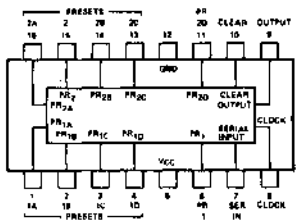
This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

PIN CONFIGURATIONS

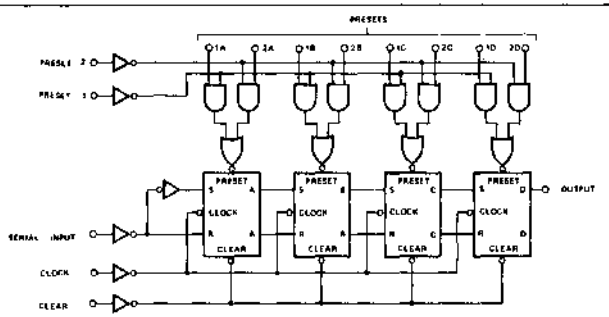
W PACKAGE



B,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC}	S5494 Circuits	4.5	5	5.5	V
	N7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output				10	
Width of Clock Pulse, $t_{p(clock)}$		35			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Serial Input Setup Time: $t_{setup(1)}$		35			ns
$t_{setup(0)}$		25			ns
Serial Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.6		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4V				160	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4V				−6.4	mA
I_{OS}	Short-circuit input current†	V_{CC} = MAX, V_{out} = 0	S5494	−20		−57	mA
			N7494	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	S5494		35	50	mA
			N7494		35	58	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15pF,	R_L = 400Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400Ω			40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

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4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER

S5495–A,F • N7495–A,F

DIGITAL 54/74 TTL SERIES

S5495 N7495

DESCRIPTION

The 54/7495 is a monolithic universal 4-Bit Shift Register designed with standard TTL techniques. The circuit layout consists of 4 R-S master-slave flip-flops, 4 AND-OR-INVERT gates, and 6 inverters configured to form a versatile register which will perform right-shift, left-shift, or parallel-in, parallel-out operations depending on the logical input level to the mode control.

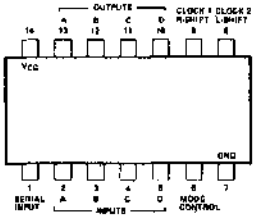
Right-shift operations are performed when a logical 0 level is applied to the mode control. Serial data is entered at the serial input D_S and shifted one position right on each clock 1 pulse. In this mode, clock 2 and parallel inputs D_A thru D_D are inhibited.

Parallel-in, parallel-out operations are performed when a logical 1 level is applied to the mode control. Parallel data is entered at parallel inputs D_A thru D_D and is transferred to the data outputs A_Q thru D_Q on each clock 2 pulse. In this mode, shift-left operations may be implemented by externally tying the output of each flip-flop to the parallel input of the previous flip-flop (D_Q to D_C and etc.), with serial data entry at input D_D.

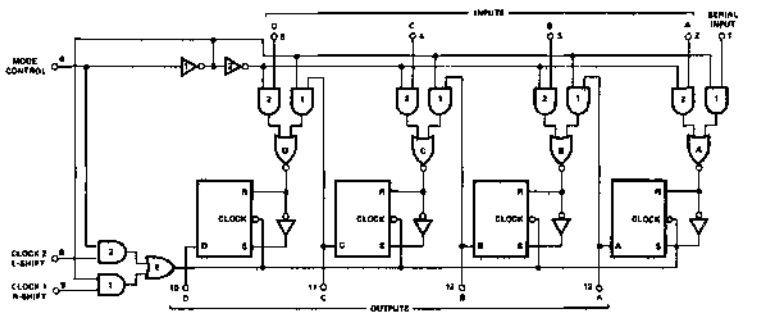
Information must be present at the R-S inputs prior to clocking and transfer of data occurs on the falling edge of the clock pulse.

PIN CONFIGURATIONS

A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	S5495 Circuits	4.5	5	5.5	V
	N7495 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output				10	
Width of Clock Pulse $t_{p(clock)}$	S5495 Circuits	20	10		ns
	N7495 Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup}		10	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold}		0	10		ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 1 inputs)		15			ns
Logical 1 level Setup Time Required at Mode Control (With Respect to Clock 2 input)		15			ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)		5			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 1 input)		5			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at mode control	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V				80 1	μA mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX	N7495	39	50	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	C_L = 15pF,	R_L = 400Ω	25	36		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	C_L = 15pF,	R_L = 400Ω		18	27	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	C_L = 15pF,	R_L = 400Ω		21	32	ns

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

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5-BIT SHIFT REGISTER

S5496-B,F,W • N7496-B,F

DIGITAL 54/74 TTL SERIES

S5496
N7496

DESCRIPTION

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

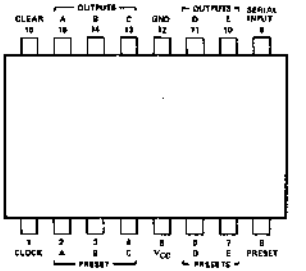
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

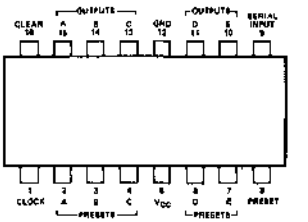
Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

PIN CONFIGURATIONS

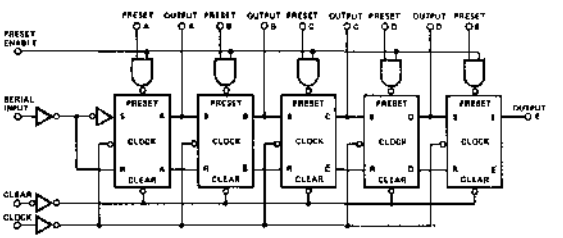
W PACKAGE



B,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC}	S5496 Circuits	4.5	5	5.5	V
	N7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output				10	
Width of Clock Pulse, $t_{p(clock)}$		35			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Serial Input Setup Time, t_{setup}		30			ns
Serial Input Hold Time, t_{hold}		0			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset (pin (8))	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset (pin (8))	V_{CC} = MAX, V_{in} = 2.4V				200	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset (pin (8))	V_{CC} = MAX, V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset (pin (8))	V_{CC} = MAX, V_{in} = 0.4V				−8	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX, V_{out} = 0	S5496	−20		−57	mA
			N7496	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	S5496		48	68	mA
			N7496		48	79	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15pF,	R_L = 400Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 15pF,	R_L = 400Ω		28	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400			55	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DESCRIPTION

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The S54100/N74100 features two independent quadruple latches in a single 24-pin dual in-line package. These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of -55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

ABSOLUTE MAXIMUM RATINGS (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3)	7V
Input Voltage, V_{in} (See Notes 3 and 4)	5.5V
Operating Free-Air Temperature Range:	
S54100 Circuits	-55°C to 125°C
N74100 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:

3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

TRUTH TABLE

LOGIC

(Each Latch)	
t_n D	t_{n+1} Q
1	1
0	0

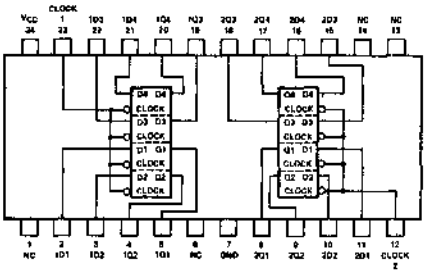
NOTES:

1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

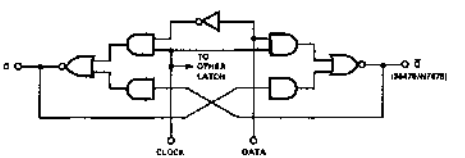
NC — No internal connection.

PIN CONFIGURATIONS

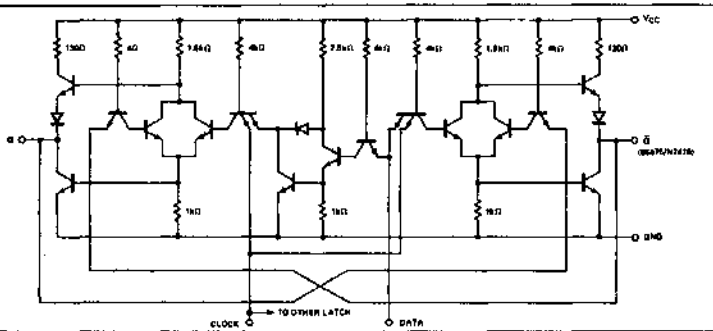
N,Q,F PACKAGE



LOGIC DIAGRAM (each latch)



SCHEMATIC DIAGRAM (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S54100	4.5	5	5.5	V
	N74100	4.75	5	5.25	V
Normalized Fan-Out from Output				10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	S54100, N74100			-12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX, V_{in} = 2.4V,	S54100, N74100			160	μA
						320	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_{out} = 0	S54100	-20		-57	mA
			N74100	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	S54100		64	92	mA
			N74100		64	106	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS NOTE A		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

NOTE A: AC Test circuit, voltage waveforms and switching times are given on p. 2-76.

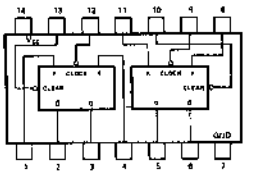
DESCRIPTION

The S54107A/N74107A J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:
See S5473/N7473 waveform.

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

PIN CONFIGURATIONS

A,F PACKAGE



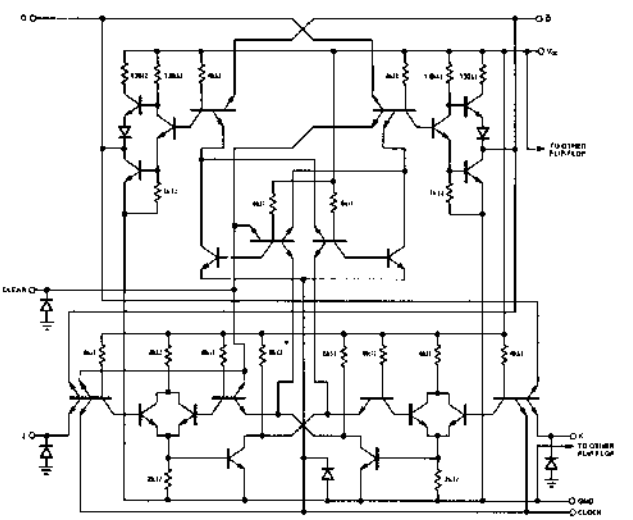
TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54107 Circuits	4.5	5	5.5	V
	N74107 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54107 Circuits	-55	25	125	°C
	N74107 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S54107	-20		-57	mA
				N74107	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DESCRIPTION

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

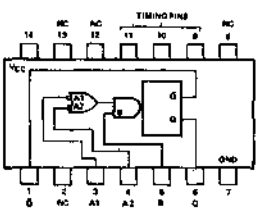
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T = 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

PIN CONFIGURATIONS

A, F, W PACKAGE



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

1 = $V_{in(1)} \geq 2V$ 0 = $V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin (9) to pin (14).
5. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.
7. t_n = time before input transition.
8. t_{n+1} = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:				V
N74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/µs
Input Pulse Width	50			ns
External Timing Resistance Between Pins (11) and (14) (Pin (9) open)	1.4			kΩ
External Timing Resistance: S54121			30	kΩ
N74121			40	kΩ
Timing Capacitance	0		1000	µF
Output Pulse Width			40	s
Duty Cycle: R_T = 2kΩ			67%	
R_T = 30kΩ (S54121) or			90%	
R_T = 40kΩ (N74121)				

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN				1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN			0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN				1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN			0.8	1.35		V
V_{out} (0)	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
V_{out} (1)	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400µA		2.4	3.3		V
I_{in} (0)	Logical 0 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 0.4V			-1	-1.6	mA
I_{in} (0)	Logical 0 level input current at B	V_{CC} = MAX,	V_{in} = 0.4V			-2	-3.2	mA
I_{in} (1)	Logical 1 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 2.4V			2	40	µA
		V_{CC} = MAX,	V_{in} = 5.5V			0.05	1	mA
I_{in} (1)	Logical 1 level input current at B	V_{CC} = MAX,	V_{in} = 2.4V			4	80	µA
		V_{CC} = MAX,	V_{in} = 5.5V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$†	V_{CC} = MAX		S54121	-20	-26	-55	mA
				N74121	-18	-25	-55	mA
I_{CC}	Power supply current in quiescent (unfired) state	V_{CC} = MAX				13	26	mA
I_{CC}	Power supply current in fired state	V_{CC} = MAX				23	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	C_L = 15pF,	C_T = 80pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output	C_L = 15pF,	C_T = 80pF	25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	C_L = 15pF,	C_T = 80pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output	C_L = 15pF,	C_T = 80pF	30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	C_L = 15pF, R_T = Open,	C_T = 80pF Pin (9) to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	C_L = 15pF, R_T = Open,	C_T = 0, Pin (9) to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 100pF, Pin (9) Open	600	700	800	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 1μF, Pin (9) Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	C_L = 15pF, R_T = Open,	C_T = 80pF, Pin (9) to V_{CC}		30	50	ns

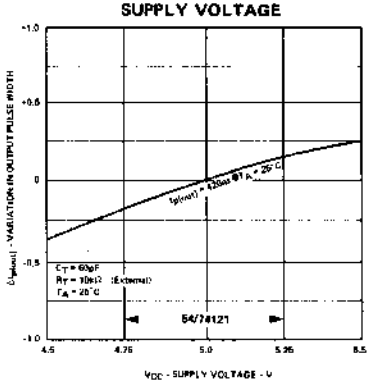
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

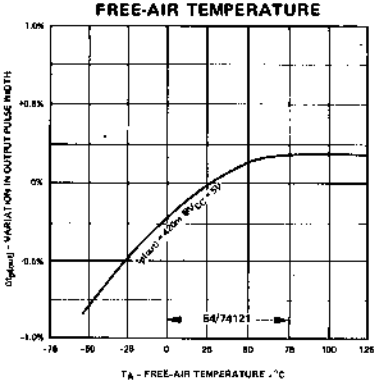
† Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

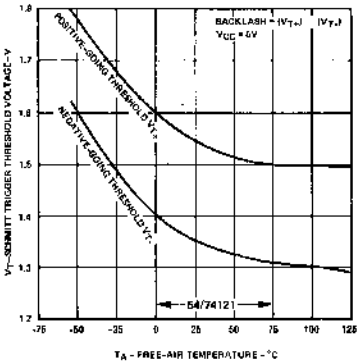


VARIATION IN OUTPUT PULSE WIDTH VERSUS FREE-AIR TEMPERATURE

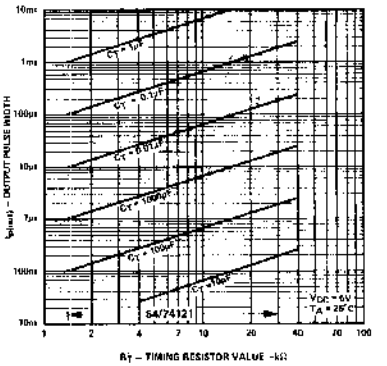


TYPICAL CHARACTERISTICS (Cont'd)

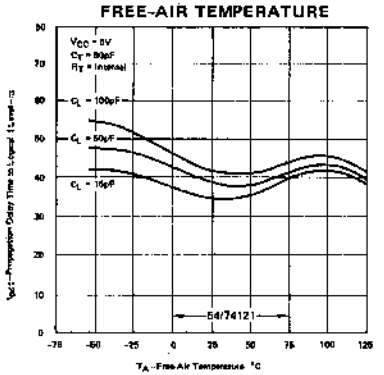
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS FREE-AIR TEMPERATURE



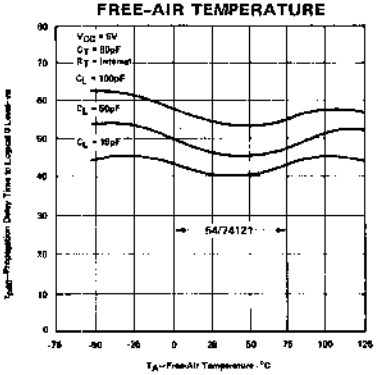
OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE



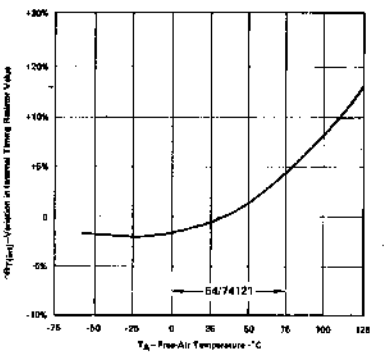
PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS FREE-AIR TEMPERATURE



signetics

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

N74122–A,F • S54123–B,F,W • N74123–B,F

DIGITAL 54/74 TTL SERIES

N74122 S54123 N74123

DESCRIPTION

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. N74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with N74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000pF$, the output pulse width (t_W) is defined as:

$$t_W = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

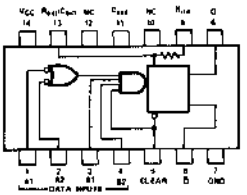
R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_W is in ns

For pulse widths when $C_{ext} \leq 1000pF$, see Figure B.

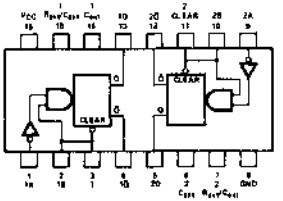
These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The N74122 and N74123 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

54/74123 B,F,W PACKAGE



74122 A,F PACKAGE



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE (See Note A)

N74122

INPUTS				OUTPUTS	
A_1	A_2	B_1	B_2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
	H	H	H	⎍	⎎

S54123,N74123

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

NOTES:

A. H = high level (steady-state), L = low level (steady-state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = No internal connection.

C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.

D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

RECOMMENDED OPERATING CONDITIONS

		S54123, N74122, N74123			UNIT
		MIN	NOM	MAX	
Supply Voltage V_{CC}		4.75	5	5.25	V
Normalized Fan-Out from each Output, N	High Logic Level			20	
	Low-Logic Level			10	
Input data setup time, t_{setup} (See Note 3)		40†			ns
Input data hold time, t_{hold} (See Note 4)		40†			ns
Width of Clear Pulse, $t_{w(clear)}$		40†			ns
External Timing Resistance		5		50	kΩ
External Capacitance		No Restriction			
Wiring Capacitance at R_{ext}/C_{ext} Terminal				50	pF
Operating Free-Air Temperature, T_A		0	25	70	°C

†These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

NOTES:
1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the N74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.
5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open. C_{ext} = 0.02μF, and R_{ext} = 25kΩ. R_{int} of S54122/N74122 is open.
7. I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open. C_{ext} = 0.02μF, and R_{ext} = 25kΩ. R_{int} of S54122/N74122 is open.

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

	PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = -800μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 16mA,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
		clear input					-3.2	
I_{OS}	Short-circuit output current†		V_{CC} = MAX,	See Note 5	-10		-40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7	N74122		23	28	mA
				N74123		46	66	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input				22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input	C_{ext} = 0, C_L = 15pF,	R_{ext} = 5kΩ, R_L = 400Ω,		30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				30	40	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000pF, C_L = 15pF,	R_{ext} = 10kΩ R_L = 400Ω	3.08	3.42	3.76	μs

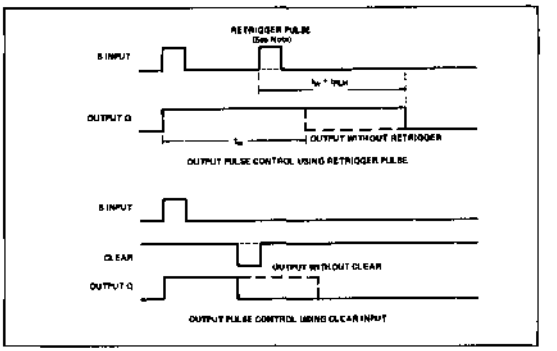
* For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DESCRIPTION

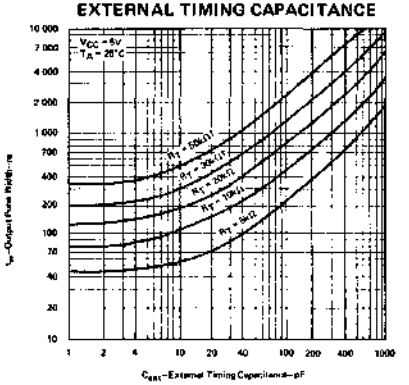
These monolithic TTL retriggerable monostable multivibrators feature dc triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A illustrates triggering the one-shot with the high-level-active (B) inputs.

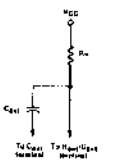
TYPICAL INPUT/OUTPUT PULSES (Figure A)



TYPICAL CHARACTERISTICS (Figure B)



† These values of resistance exceed the maximums recommended for use over the full temperature range of the S54122 and S54123.



NOTE:
When using electrolytic capacitor, insure that minimum rating is 20 volts so that 5% reverse voltage rating is 1.0 volt or greater.

DESCRIPTION

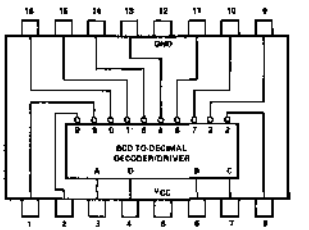
The N74141 is a BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the N74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The then high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

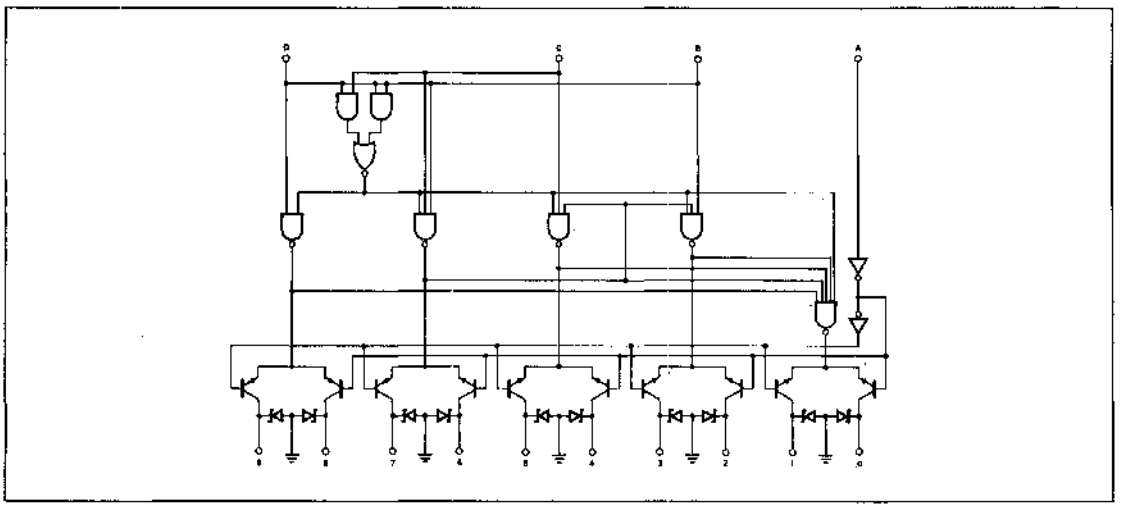
Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The N74141 is characterized for operation over the temperature range of 0°C to 70°C.

PIN CONFIGURATIONS

B PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level

*All other outputs are off

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1)	4.75	5	5.25	V
Output Voltage (See Notes 1 and 2)			65	V
Operating Free-Air Temperature Range	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, I_O = 7mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	V_{CC} = MAX, I_O = 0.5mA	65			V
$I_{O(off)}$	Off-state reverse current	V_{CC} = MAX, V_O = 55V			50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15	V_{CC} = MAX, V_O = 30V			5	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current into A	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{IL}	Low-level input current into B, C, or D				-3.2	mA
I_{CC}	Supply current	V_{CC} = MAX		11	16	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

** This typical value is at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

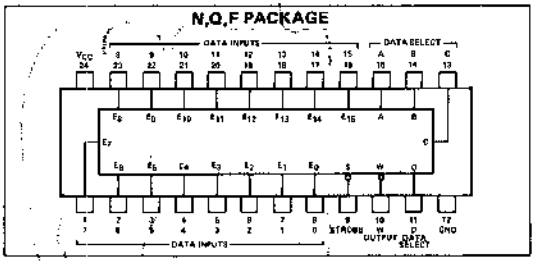
The 54/74150 is a one-of-sixteen data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

The S54150/N74150 is provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

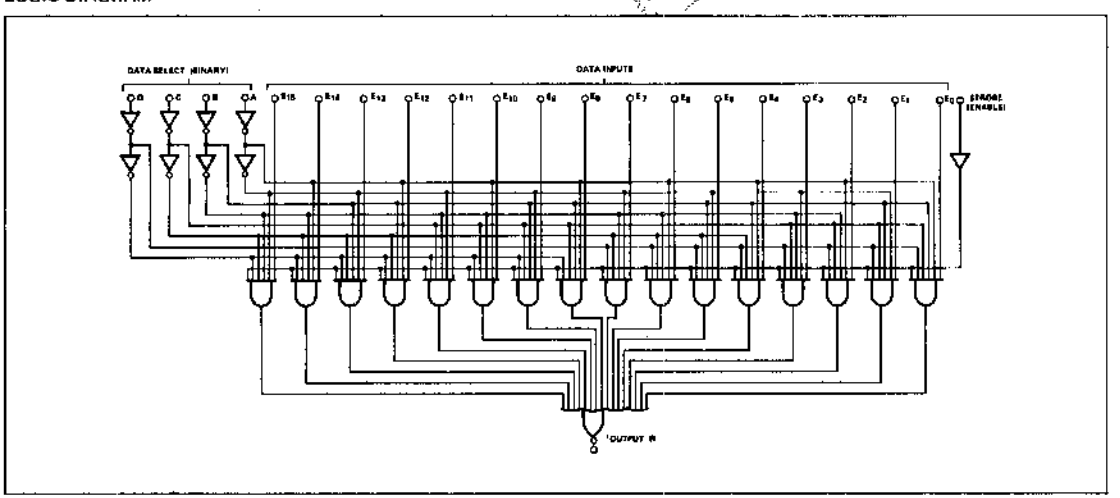
This data selector/multiplexer is fully compatible for use with other TTL or DTL circuit. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

S54150/N74150 — 200 milliwatts.

PIN CONFIGURATIONS



LOGIC DIAGRAM



TRUTH TABLE

INPUTS																				OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54150 Circuits	4.5	5	5.5	V
N74150 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Logical 0			10	
Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, V_{OUT} = 0	-20		-55	mA
			-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V		40	68	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	C_L = 15pF, R_L = 400Ω		20	30	ns
t_{pd1}	A,B,orC(4levels)	Y			36	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D_0 thru D_7	Y			16	24	ns
t_{pd1}	D_0 thru D_7	Y			19	29	ns
t_{pd0}	E_0 thru E_{15}	W			8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

S54151
N74151

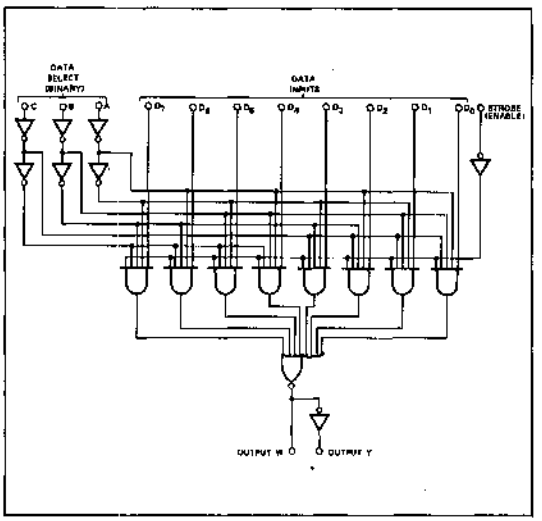
S54151–B,F,W • N74151–B,F

DIGITAL 54/74 TTL SERIES

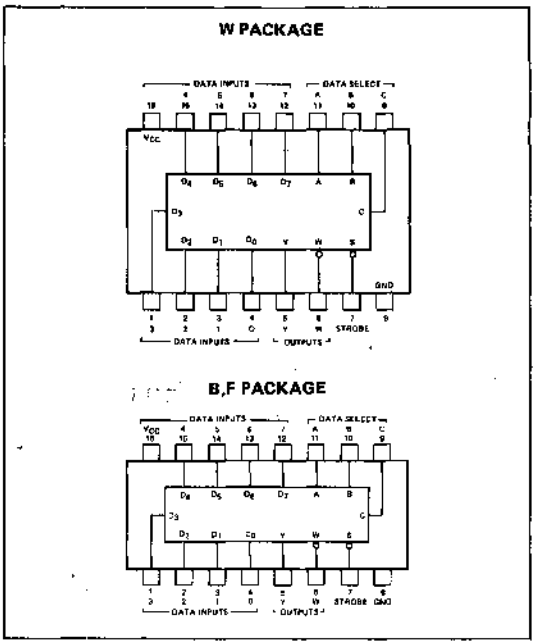
DESCRIPTION

The '54/74151 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line. Both true and complement outputs are available.

LOGIC DIAGRAM



PIN CONFIGURATIONS



TRUTH TABLE

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = irrelevant.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54151 Circuits	4.5	5	5.5	V
	N74151 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	Logical 0			10	
	Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = −800 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			−1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, V_{out} = 0	−20		−55	mA
			−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V		29	48	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	C_L = 15pF, R_L = 400Ω		20	30	ns
t_{pd1}	A,B,orC(4 levels)	Y			35	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D_0 thru D_7	Y			16	24	ns
t_{pd1}	D_0 thru D_7	Y			19	29	ns
t_{pd0}	E_0 thru E_{15}	W			8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

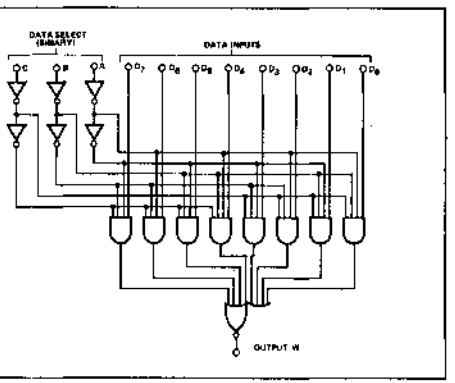
** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DESCRIPTION

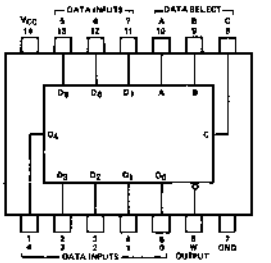
The S54152 is a one-of-eight data selector which performs parallel to serial data conversion. The S54152 is identical to the S54152 with the exclusion of the true output and strobe. It is available in the 14-pin flatpak only.

LOGIC DIAGRAM



PIN CONFIGURATIONS

W PACKAGE



TRUTH TABLE

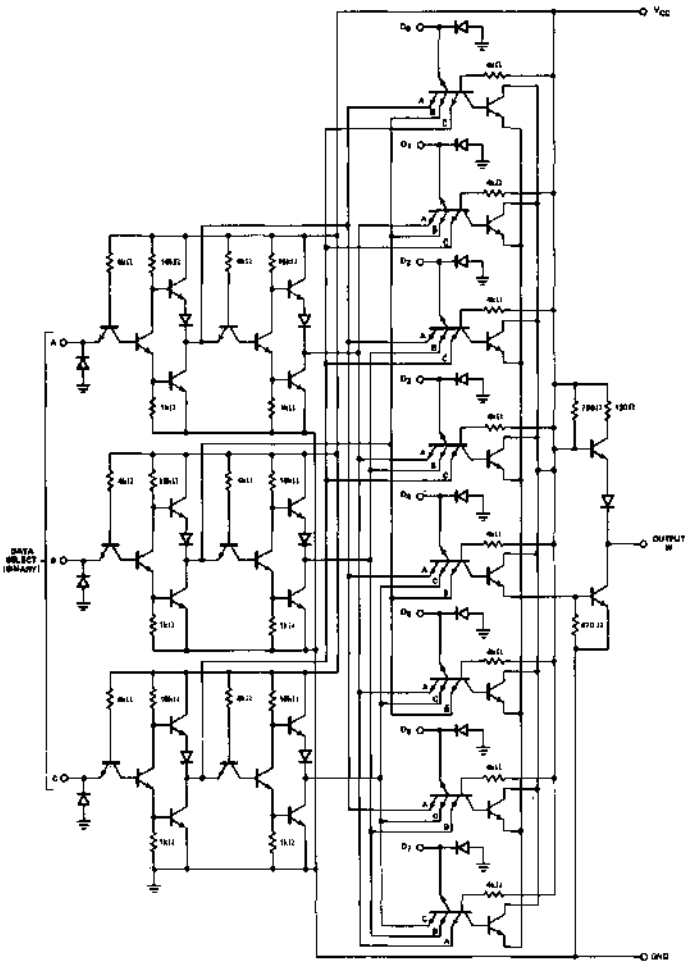
INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = Irrelevant.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54152 Circuits	4.5	5	5.5	V
	N74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	Logical 0			10	
	Logical 1			20	

SCHEMATIC DIAGRAM



Component values shown are nominal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	-20		-55	mA
		V_{out} = 0	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V		26	43	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	C_L = 15pF, R_L = 400Ω		20	30	ns
t_{pd1}	A,B,orC(4 levels)	Y			35	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D_0 thru D_7	Y			16	24	ns
t_{pd1}	D_0 thru D_7	Y			19	29	ns
t_{pd0}	E_0 thru E_{15}	W			8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

S54153–B,F,W • N74153–B,F

DIGITAL 54/74 TTL SERIES

S54153
N74153

DESCRIPTION

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

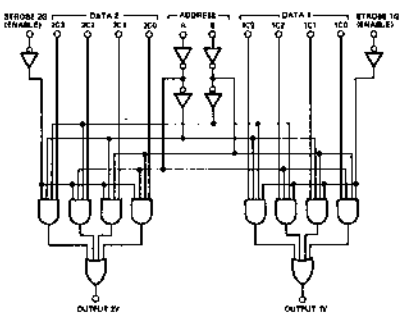
Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The S54153 is characterized for operation over the full military temperature range of -55°C to 125° C; the N74153 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

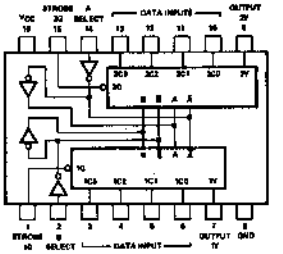
Address inputs A and B are common to both sections. H = high level, L = low level, X = irrelevant.

LOGIC DIAGRAM

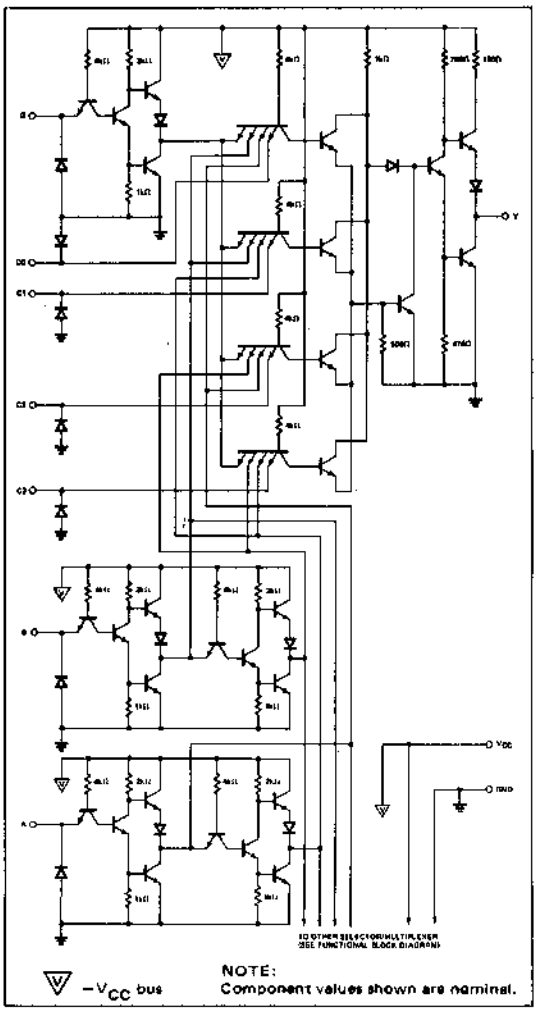


PIN CONFIGURATIONS

B,F,W PACKAGE



SCHEMATIC DIAGRAM



$-V_{CC}$ bus

NOTE:
Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	S54153			N74153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
High Logic Level			20			20	
Low Logic Level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA		0.2	0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S54153	-20		-55	mA
			N74153	-18		-57	
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	S54153		36	52	mA
			N74153		36	60	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y			12	18	ns
t_{PHL}	Data	Y			15	23	ns
t_{PLH}	Address	Y	C_L = 30pF, R_L = 400Ω		22	34	ns
t_{PHL}	Address	Y			22	34	ns
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}	Strobe	Y			15	23	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

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4-LINE TO 16 LINE DECODER/DEMULTIPLEXER

S54154–N,Q,F • N74154–N

DIGITAL 54/74 TTL SERIES

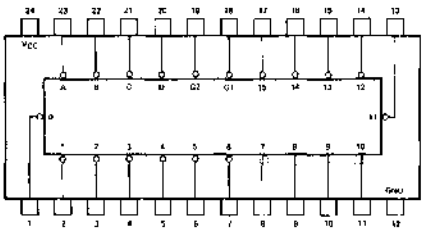
S54154
N74154

DESCRIPTION

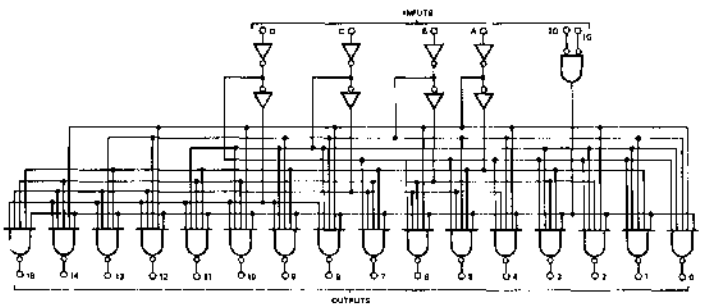
The 54/74154 decodes 4 binary-coded inputs to one of 16 mutually exclusive outputs when each of the two strobe inputs are low. The demultiplexing function is achieved by using the 4 input lines for output addressing and data from one strobe input while the other strobe input is held low.

PIN CONFIGURATIONS

N,Q,F PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High, L = Low, X = Irrelevant

RECOMMENDED OPERATING CONDITIONS

	S54154			N74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Low logic level			10			10	
High logic level			20			20	
Operating Free-Air Temperature Range	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V				40	A
		V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	S54154	-20		-55	mA
			N74154	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX	S54154		34	49	mA
			N74154		34	56	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15pF, R_L = 400Ω		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

S54155
S54156
N74155
N74156

S54155–B,F,W • S54156–B,F,W • N74155–B • N74156–B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired.

Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3- to 8-line decoder or 1- to 8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

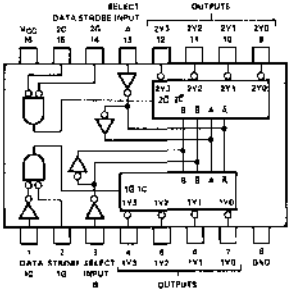
The S54155/N74155 circuits, with totem pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The S54156/N74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the S54155/N74155.

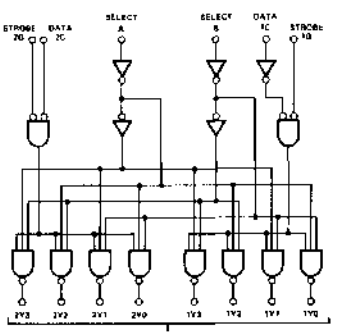
The S54155 and S54156 are characterized for operation over the full military temperature range of -55°C to 125°C the N74155 and N74156 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



TRUTH TABLES

TRUTH TABLES (H = High Level, L = Low Level, X = Irrelevant)

2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

RECOMMENDED OPERATING CONDITIONS

	S54155			N74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	−55	25	125	0	25	70	°C

	S54156			N74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			S54155,N74155 MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -800μA	V_{IH} = 2V,		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_{IL} = 0.8V,				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V				40	μA
		V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		S54155	-20		-55	mA
				N74155	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX		S54155		25	35	mA
				N74155		25	40	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			S54156,N74156 MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_I = 2V,				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_{IL} = 0.8V,				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V				40	μA
		V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{CC}	Supply current	V_{CC} = MAX		S54156		25	35	mA
				N74156		25	40	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	S54155 N74155 MIN	S54155 N74155 TYP	S54155 N74155 MAX	S54156 N74156 MIN	S54156 N74156 TYP	S54156 N74156 MAX	UNIT
t_{PLH}	A,B,2C, 1G,or2G	Y	2			13	20		15	23	ns
t_{PHL}	A,B,2C, 1G,or2G	Y	2	C_L = 15pF,		18	27		20	30	ns
t_{PLH}	A or B	Y	3	R_L = 400Ω		21	32		23	34	ns
t_{PHL}	A or B	Y	3			21	32		23	34	ns
t_{PLH}	1C	Y	3			16	24		18	27	ns
t_{PHL}	1C	Y	3			20	30		22	33	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

TYPICAL APPLICATION DATA

The S54155, N74155, S54156, or N74156 may be used as a dual 2-line to 4-line decoder or a 1-line to 4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

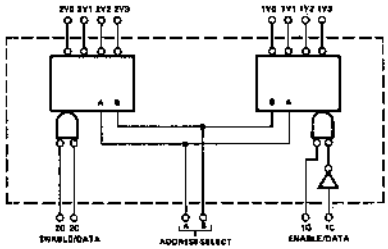
Any of these circuits may also be used as a 3-line to 8-line decoder or a 1-line to 8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.

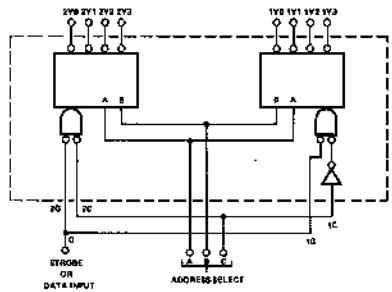
DUAL 2-LINE TO 4-LINE DECODER/1-TO 4-LINE DEMULTIPLEXER

S54155, N74155, S54156, N74156



3-LINE TO 8-LINE DECODER/1-TO 8-LINE DEMULTIPLEXER

S54155, N74155, S54156, N74156



signetics

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER

S54157
S54158
N74157
N74158

S54157–B,F,W • N74157–B,F • S54158–B,F,W • N74158–B,F

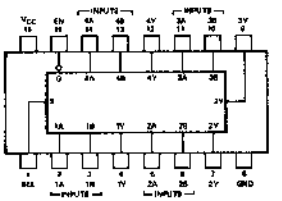
DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54157/N74157 and S54158/N74158 are identical with the exception of the S54158/N74158 being inverted. These devices are logical implementations of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The devices provide the ability, in one package, to select four bits of either data or control from two sources. By proper manipulation of the inputs, it can generate four functions of two variables with one variable common. Thus any number of random topic elements used to generate unusual truth tables can be replaced. All outputs are low when disabled (enable high). Both inputs and outputs are buffered.

PIN CONFIGURATION

B,F,W PACKAGE



S54/N74157

TRUTH TABLE

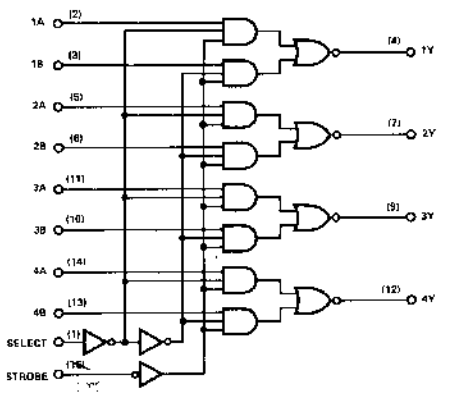
INPUTS			OUTPUT
STROBE	SELECT	A B	Y
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

S54/N74158

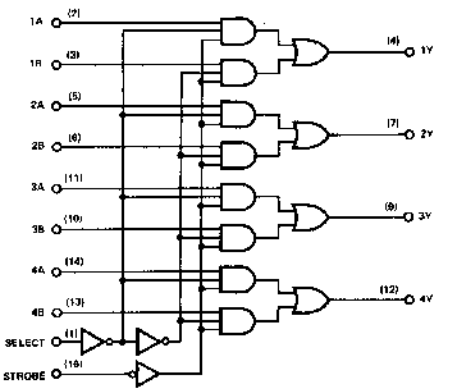
TRUTH TABLE

INPUTS			OUTPUT
STROBE	SELECT	A B	Y
H	X	X X	H
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

LOGIC DIAGRAM
S54/N74157



LOGIC DIAGRAM
S54/N74158



RECOMMENDED OPERATING CONDITIONS

	S54157/58			N74157/58			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
High Logic Level			20			20	
Low Logic Level			10			10	
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54157/58			N74157/58			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-55	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX			30	48		30	48	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Data	Output			9	14	ns
t_{PLH}	Data	Output	C_L = 15pF, R_L = 400		9	14	ns
t_{PHL}	Enable	Any Output			14	21	ns
t_{PLH}	Enable	Any Output			13	20	ns
t_{PHL}	Select	Any Output			18	27	ns
t_{PLH}	Select	Any Output			15	23	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

SYNCHRONOUS 4-BIT COUNTER

S54160 N74160
S54161 N74161
S54162 N74162
S54163 N74163

S54160–B,F,W • S54161–B,F,W • S54162–B,F,W • S54163–B,F,W
N74160–B,F • N74161–B,F • N74162–B,F • N74163–B,F

DIGITAL 54/74 TTL SERIES

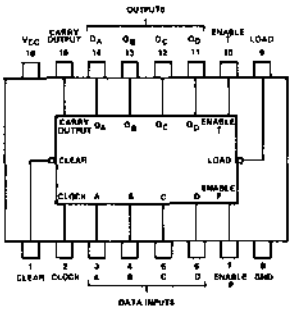
DESCRIPTION

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The S54160, S54162, N74160, and N74162 are decade counters and the S54161, S54163, N74161, and N74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs and power dissipation is typically 325 milliwatts.

PIN CONFIGURATION

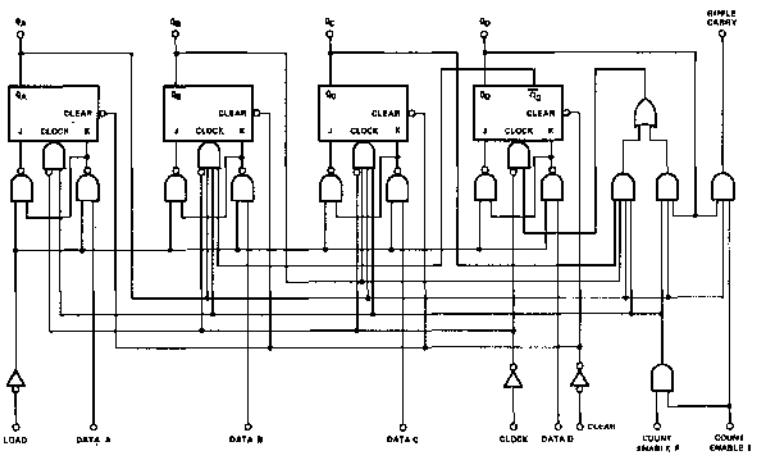
B,F,W PACKAGE



LOGIC DIAGRAM

S54160/N74160 SYNCHRONOUS DECADE COUNTERS

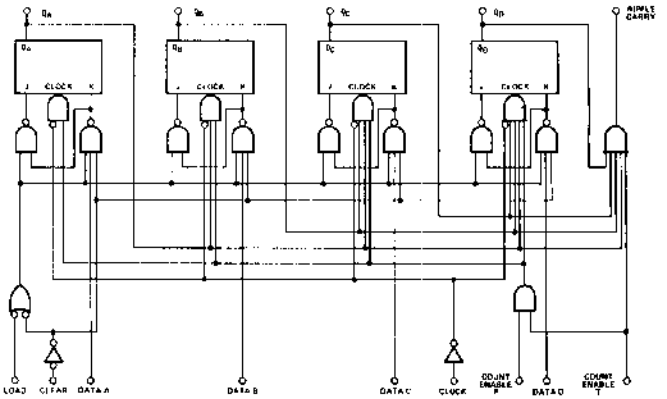
(S54162/N74162 synchronous decade counters are similar; however the clear is synchronous as shown for the S54163/N74163 binary counters).



LOGIC DIAGRAM (Cont'd)

S54163/N74163 SYNCHRONOUS BINARY COUNTERS

S54161/N74161 synchronous binary counters are similar; however the clear is asynchronous as shown for the S54160/N74160 decade counters).



RECOMMENDED OPERATING CONDITIONS

	S54160, S54161 S54162, S54163			N74160, N74161 N74162, N74163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock Pulse, $t_{w(clock)}$	25			25			ns
Width of Clear Pulse, $t_{w(clear)}$	20			20			ns
Setup Time, t_{setup}: Data Inputs, A,B,C,D	15			15			
Enable P	20			20			
Load	15			15			ns
Clear	20			20			
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise specified)

PARAMETER		TEST CONDITIONS*		S54160,S54161 S54162,S54163			N74160,N74161 N74162,N74163			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MAX,				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current: Clock or enable T	V_{CC} = MAX,	V_I = 2.4V			80			80	μA
	Other inputs					40			40	
I_{IL}	Low-level input current: Clock or enable T	V_{CC} = MAX,	V_I = 0.4V			-3.2			-3.2	mA
	Other inputs					-1.6			-1.6	
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CCL}	Supply current, all outputs high	V_{CC} = MAX,	See Note 3		59	85		59	94	mA
	Supply current, all outputs low	V_{CC} = MAX,	See Note 4		63	91		63	101	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

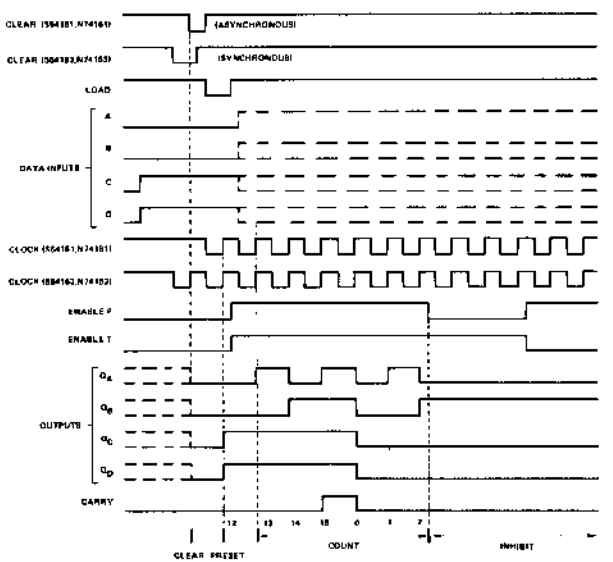
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T			8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			20	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

NOTES:
3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES FOR 54161, 74161, 54163, 74163 SYNCHRONOUS BINARY COUNTERS

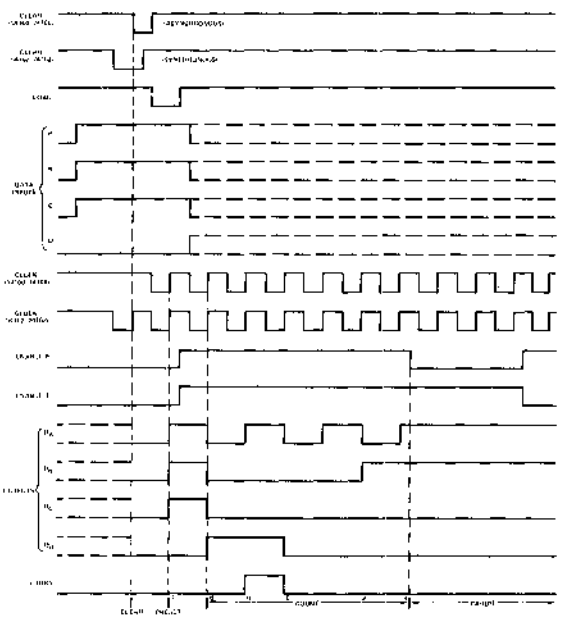
Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



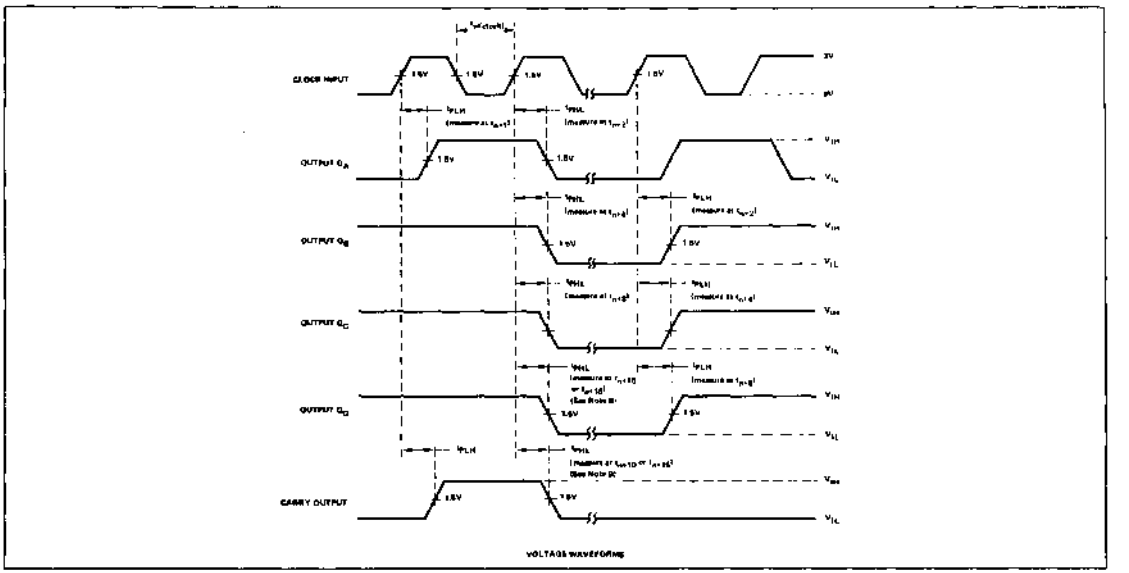
TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES FOR 54160, 54162, 74160, 74162 SYNCHRONOUS BINARY COUNTERS

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



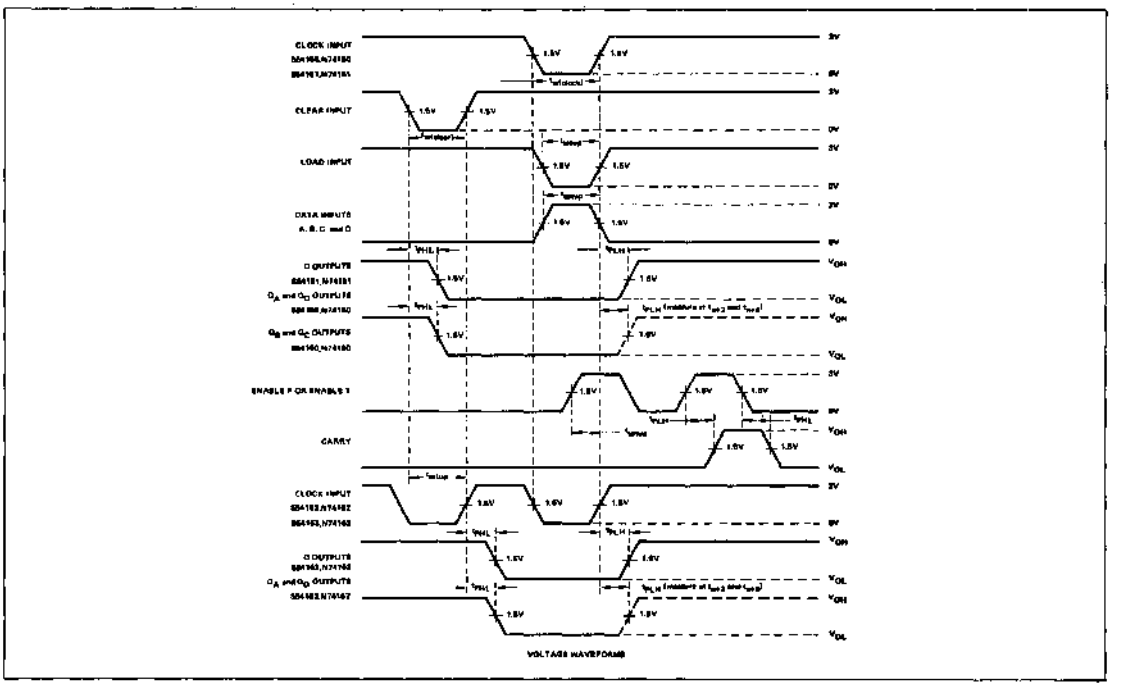
PARAMETER MEASUREMENT INFORMATION



NOTES:

A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ns; $t_f \leq 10$ns, PRR ≤ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the S54160, S54162, N74160, and N74162, and at t_{n+16} for the S54161, S54163, N74161, and N74163, where t_n is the bit time when all outputs are low.

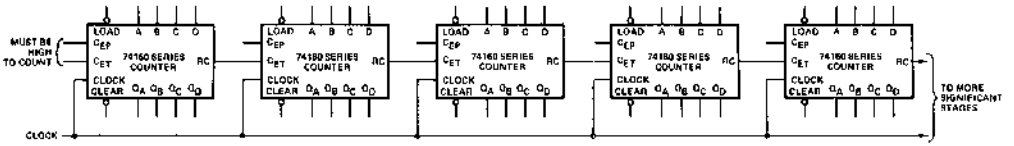


NOTES:

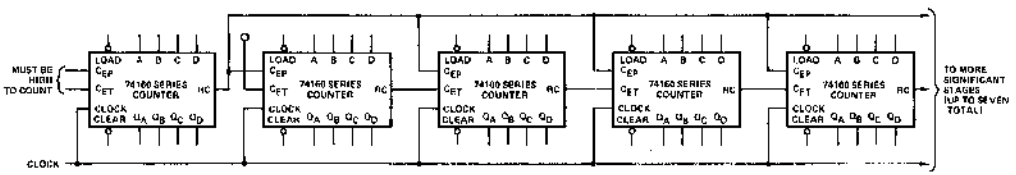
A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ns; $t_f \leq 10$ns; PRR ≤ 1 MHz, duty cycle $\leq$ 50%; $Z_{out} \approx 50\Omega$.

B. Enable P and enable T setup times are measured at $t_n = 0$.

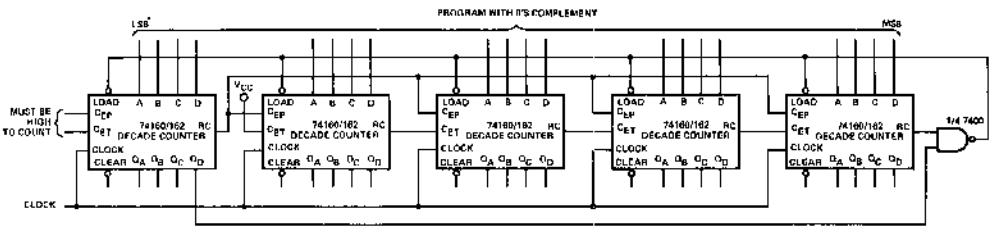
TYPICAL APPLICATIONS



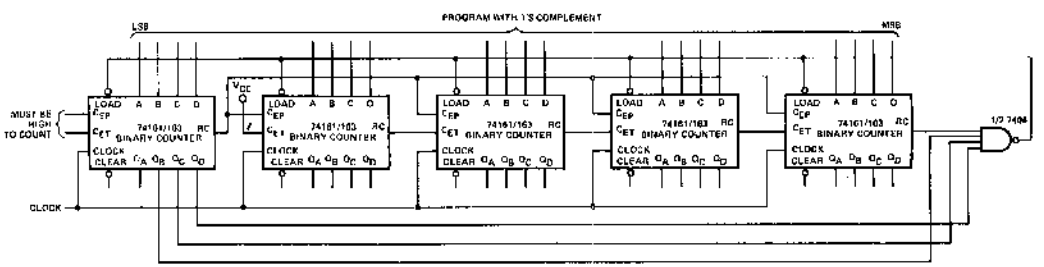
MULTISTAGE SYNCHRONOUS COUNTER EXPANSION



HIGH SPEED MULTISTAGE SYNCHRONOUS COUNTER EXPANSION



MULTISTAGE SYNCHRONOUS PROGRAMMABLE DECADE COUNTER



MULTISTAGE SYNCHRONOUS PROGRAMMABLE BINARY COUNTER

DESCRIPTION

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The S54164 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74164 is characterized for operation from 0°C to 70°C.

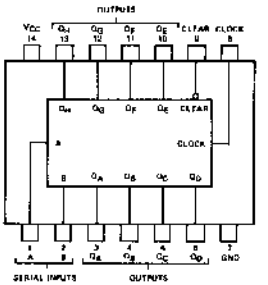
TRUTH TABLE

SERIAL INPUTS A AND B

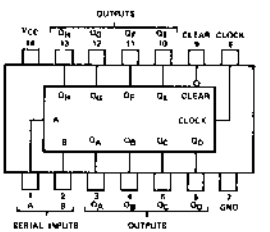
INPUTS $AT t_n$		OUTPUT $AT t_n+1$
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

PIN CONFIGURATIONS

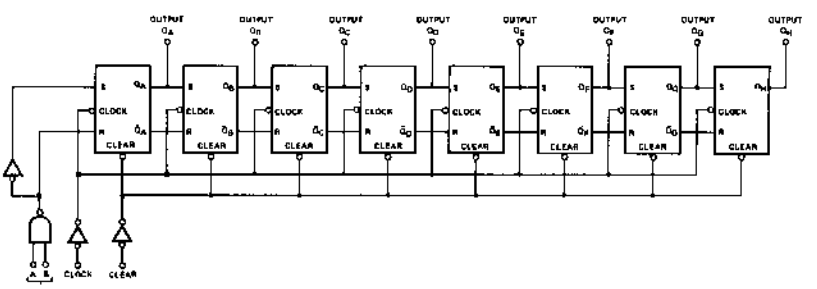
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54164			N74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			10			10	
Low logic level			5			5	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock or Clear Input Pulse, t_w	20			20			ns
Data Setup Time, t_{setup}	15			15			ns
Data Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		S54164 MIN	S54164 TYP**	S54164 MAX	N74164 MIN	N74164 TYP**	N74164 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 8mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		-10		-27.5	-9		-27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note	$V_{I(clock)}$ = 0.4V		30			30		mA
			$V_{I(clock)}$ = 2.4V		37	54		37	54	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 5

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	C_L = 15pF		24	36	ns
		C_L = 50pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input	C_L = 15pF	8	17	27	ns
		C_L = 50pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input	C_L = 15pF	10	21	32	ns
		C_L = 50pF	10	25	37	

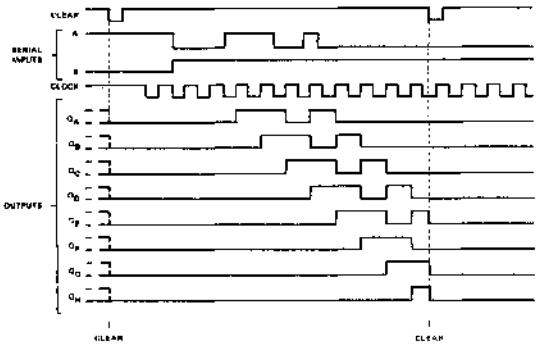
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

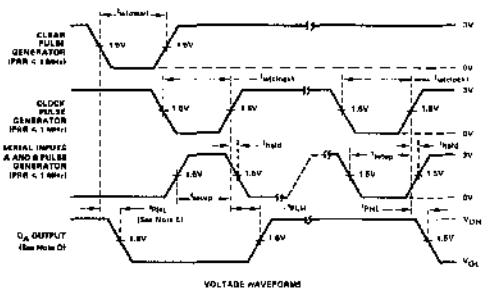
† Not more than two outputs should be shorted at a time.

NOTE: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V, applied to clear.

TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES



PARAMETER MEASUREMENT INFORMATION



NOTES:
A. The pulse generators have the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

DESCRIPTION

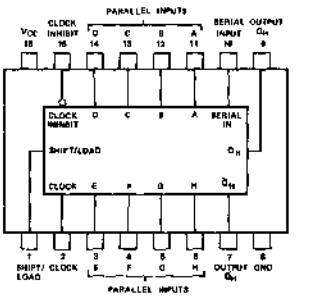
The S54165 and N74165 are 8-bit serial shift registers that shift data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

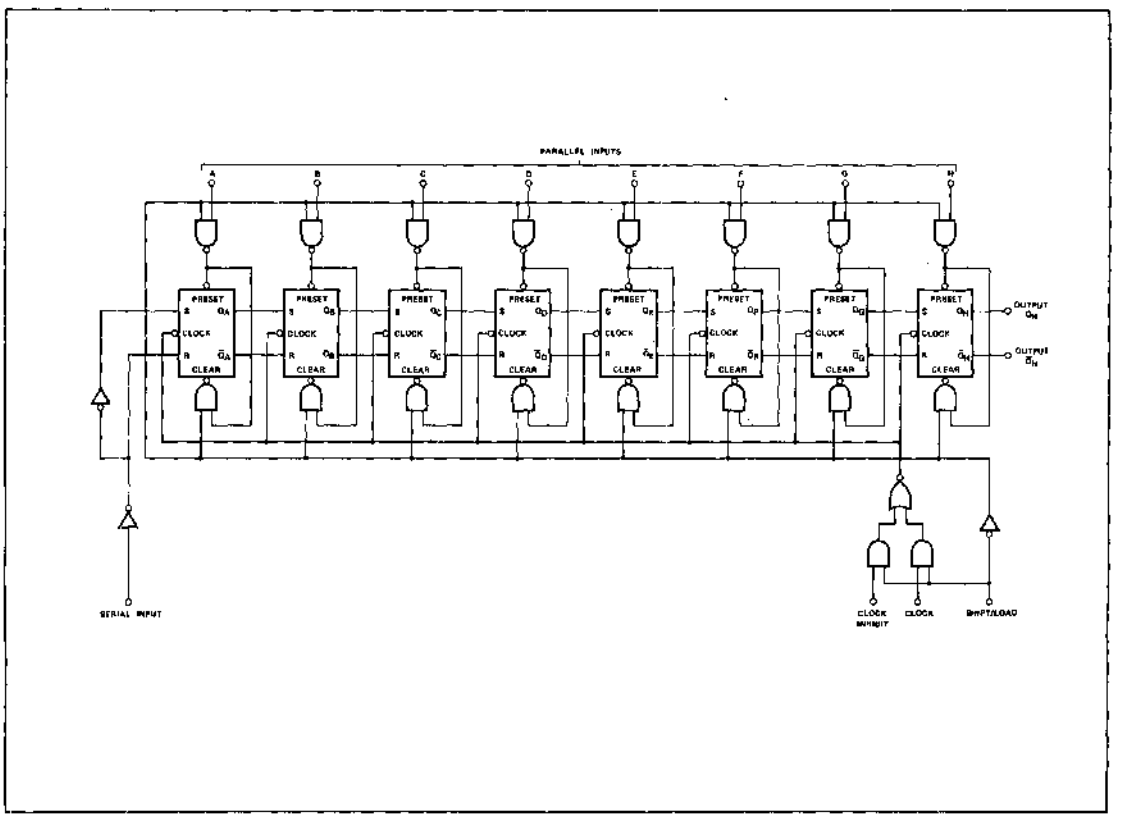
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The S54165 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74165 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54165			N74165			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		20	0		20	MHz
Width of Clock Input Pulse, $t_{w(clock)}$	25			25			ns
Width of Load Input Pulse, $t_{w(load)}$	15			15			ns
Clock-Enable Setup Time, t_{setup}	30			30			ns
Parallel Input Setup Time, t_{setup}	10			10			ns
Serial Input Setup Time, t_{setup}	20			20			ns
Shift Setup Time, t_{setup}	45			45			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS *	S54165			N74165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 µA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	Load input	V_{CC} = MAX, V_I = 2.4 V			80			80	µA
		Other inputs				40			40	
I_{IL}	Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current †		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note		42	63		42	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω,	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	27	ns
t_{PHL}					21	34	
t_{PLH}	H	Q_H			11	20	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

NOTE: With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

† Not more than one output should be shorted at a time.

f_{max} ≡ Maximum input count frequency

t_{PLH} ≡ Propagation delay time, low-to-high-level output

t_{PHL} ≡ Propagation delay time, high-to-low-level output

DESCRIPTION

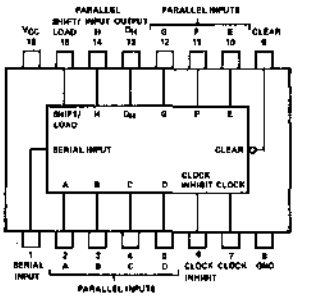
These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C. Series 74 devices are characterized for operation from 0°C to 70°C.

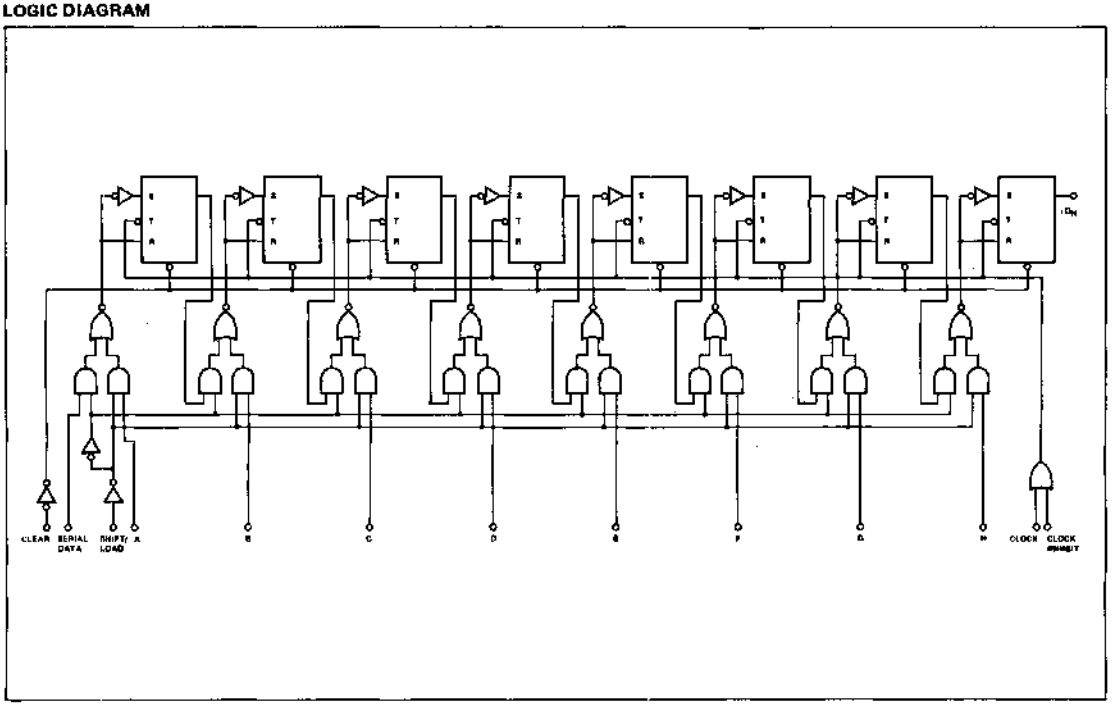
These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54166			N74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	S54166			N74166			UNIT
			MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800µA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54166, N74166	Serial Input	Clock	All other inputs

DESCRIPTION

The 54170 and 74170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates on a monolithic chip. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W is high, the data inputs are inhibited and their states can cause no change in the information stored in the internal latches. When the read enable output, G_R, is high, the data outputs are inhibited and remain high.

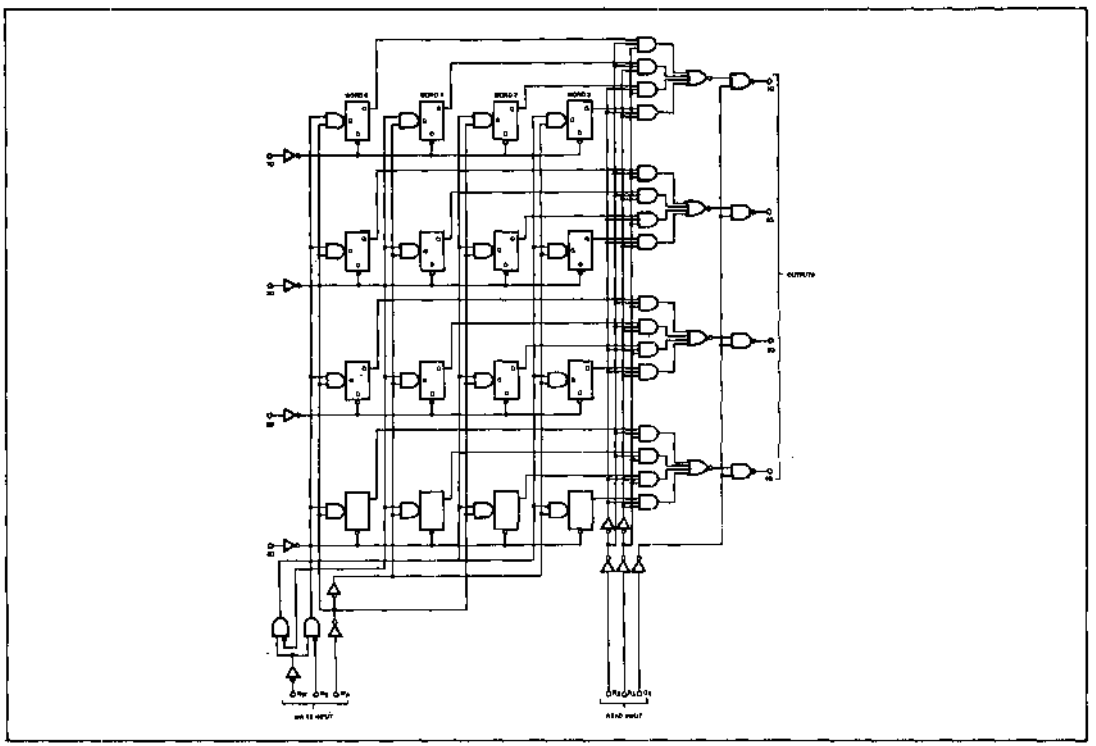
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a non-destructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

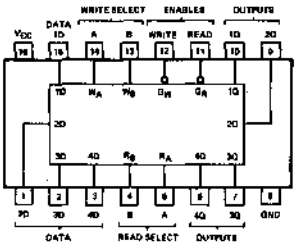
Power dissipation is typically 500 mW total or 5 mW per gate. The 54170 is characterized for operation over the full military temperature range of −55°C to 125°C; the 74170 is characterized for operation from 0°C to 70°C.

LOGIC DIAGRAM



PIN CONFIGURATION

B,F,W, PACKAGE



RECOMMENDED OPERATING CONDITIONS

		54170			74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (See Note 1)	data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	write select with respect to write enable, $t_{setup(W)}$	15			15			ns
	read select with respect to read enable, $t_{setup(R)}$	5			5			ns
Hold times, high- or low-level data (See Note 2)	data input with respect to write enable, $t_{hold(D)}$	0			0			ns
	write select with respect to write enable, $t_{hold(W)}$	5			5			ns
	read select with respect to read enable, $t_{hold(R)}$	5			5			ns
Latch time for new data, t_{latch} (See Note 3)		25			25			ns
Operating free-air temperature range, T_A		-55	25	125	0	25	70	°C

NOTES:
1. Setup time is the interval immediately preceding the negative-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the positive-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its continued recognition.
3. Latch time is the time required for the internal output of the latch to assume the state of new data. See Figure 1. This is important only when attempting to read from a location immediately after that location has received new data.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_O = 5.5 V			30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, see Note 6	54170		125‡	140	mA
			74170		125‡	160	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Typical power dissipation shown is an average for 50% duty cycle at V_{CC} = 5 V, T_A = 25°C.

NOTE 6:
Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		10	15	ns
t_{PHLq}	Propagation delay time, high-to-low-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		20	30	ns

LOGIC

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

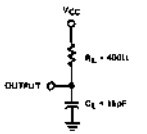
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q = D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q = D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q = D
X	X	H	Q_n	Q_n	Q_n	Q_n

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	1Q	2Q	3Q	4Q
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

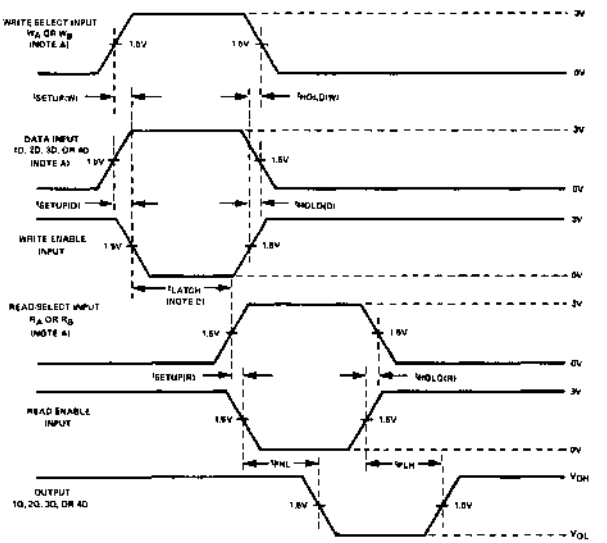
NOTES:
A. H = high level, L = low level, X = irrelevant
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_n = No change.
D. W0B1 = The first bit of word 0, etc.

SWITCHING CHARACTERISTICS



LOAD FOR OUTPUT UNDER TEST

VOLTAGE WAVEFORMS



NOTES:

A. High-level inputs are illustrated; however, low-level setup and hold times are the same.

B. Waveforms are supplied by generators with the following characteristics: PRR ≤ 1MHz, $Z_{OUT} \approx 50\Omega$, duty cycle ≤ 50%. $t_r \leq 10$ns, $t_f = 10$ns.

C. This applies only when reading from a location immediately after that location has received new data.

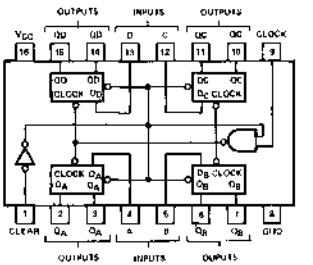
DESCRIPTION

These monolithic, positive-edge-triggered flip-flops utilize TTL circuits to implement the D-type flip-flop logic. Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 low logic-level loads and 20 high-logic-level loads is available from each of the outputs. This simplifies system design by allowing unused inputs to be tied to driven inputs. Maximum clock frequency is typically 25 megahertz, with a typical power dissipation of 38 milliwatts per flip-flop.

PIN CONFIGURATION

B,F,W PACKAGE

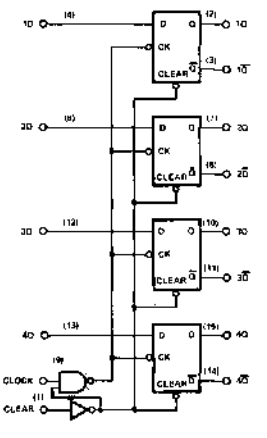


TRUTH TABLE

INPUT	OUTPUT
t_n	$t_n + 1$
D	Q
H	H
L	L

t_n = Bit time before clock pulse transition.
$t_n + 1$ = Bit time after clock pulse transition.

LOGIC DIAGRAM



PIN (16) = V_{CC}, PIN (8) = GND

RECOMMENDED OPERATING CONDITIONS

	54175			74175			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N — High Logic Level			20			20	
Low Logic Level			10			10	
Input clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (See Figure 1)	20			20			ns
Data setup time, t_{setup} (See Figure 1)	20			20			ns
Hold time t_{hold} (See Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C
Clear release setup, $t_{release}$ (See Figure 1)	25			25			ns

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		54175 MIN	54175 TYP‡	54175 MAX	74175 MIN	74175 TYP‡	74175 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX								
		Note 1			30	45		30	45	mA

§ Not more than one output should be shorted at a time.

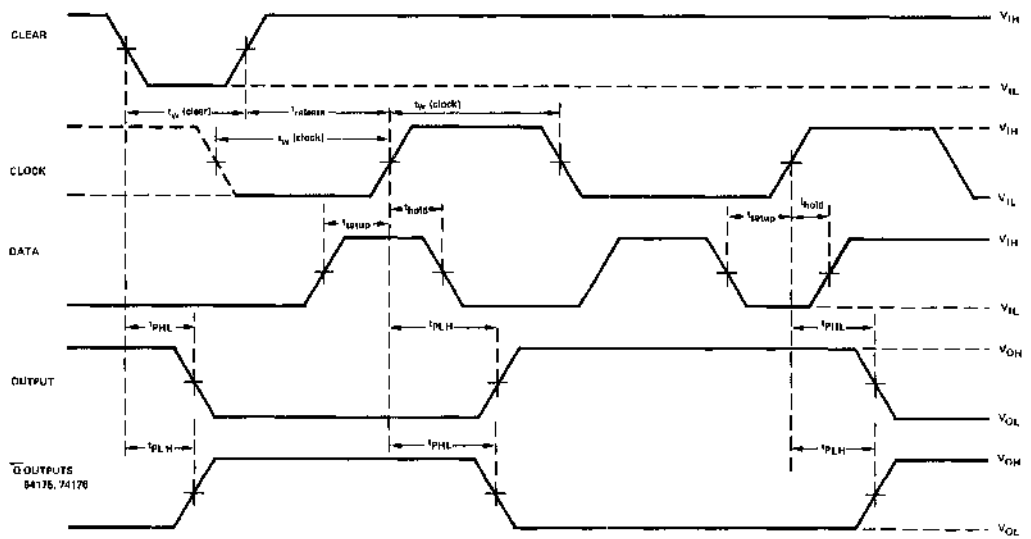
NOTE 1: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output Q from clear	C_L = 15 pF R_L = 400 Ω		23	35	ns
t_{PLH}	Propagation delay time low-to-high-level output Q from clear (54175, 74175)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns

SWITCHING TIMES

QUADRUPLE D-TYPE EDGE-TRIGGERED FLIP-FLOPS



NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω. Vary PRR to measure f_{max}.

FIGURE 1

signetics

8-BIT ODD/EVEN PARITY GENERATOR/CHECKER

S54180 N74180

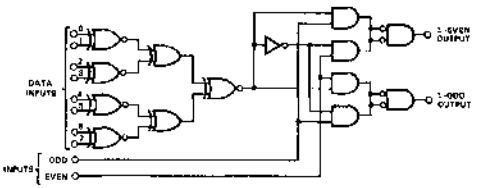
S54180–A,F,W • N74180–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

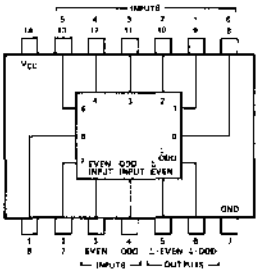
The 54/74180 8-Bit Odd/Even Parity Generator/Checker is a TTL monolithic array featuring gating logic arranged to generate or check odd or even parity.

LOGIC DIAGRAM

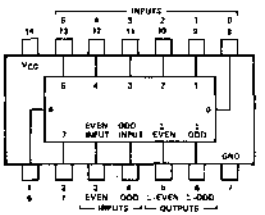


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = Irrelevant

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	S54180	4.5	5	5.5	V
	N74180	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	Logical 0			10	V
	Logical 1			20	V

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	V_{CC} = MAX, V_{in} = 2.4V				80	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	S54180	-20		-55	mA
			N74180	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX	S54180		34	49	mA
			N74180		34	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		25	38	ns
t_{pd1}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		25	38	ns
t_{pd1}	Even or Odd	Σ Even or Σ Odd	C_L = 15pF,	R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd	C_L = 15pF,	R_L = 400 Ω		7	10	ns

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

DESCRIPTION

The 54181 and 74181 are high-speed arithmetic logic units (ALU)/ function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the 54181/74181 for fast, simultaneous carry generation with a group carry propagate (P) and carry generate (G) for the 4 bits in the package. When used in conjunction with the 54182 or 74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the 54181/74181 is 24 nanoseconds for 4 bits. When expanding to 16-bit addition with the 54182/74182, only 13 nanoseconds, further delay is added so that the total addition time is 35 nanoseconds, or 2.2 nanoseconds per bit. One 54182/74182 is needed for every 16 bits (four 54181/74181 circuits).

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

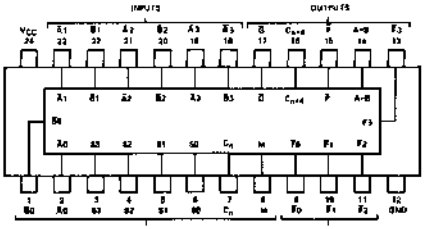
The 54181/74181 will accommodate active-high or active-low data if the pin-designations are reinterpreted as follows:

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR and OR functions.

The 54181/74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

PIN CONFIGURATION

N,F,Q PACKAGE



PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C_n}$	$\overline{C_{n+4}}$	X	Y
Active-low data	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1 which requires an end-around or forced carry to provide A—B.

The 54181/74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The 54181/74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

The 54181 is characterized for operation over the full military temperature range of −55°C to 125°C; the 74181 is characterized for operation from 0°C to 70°C.

TRUTH TABLE FOR COMPARATOR APPLICATION

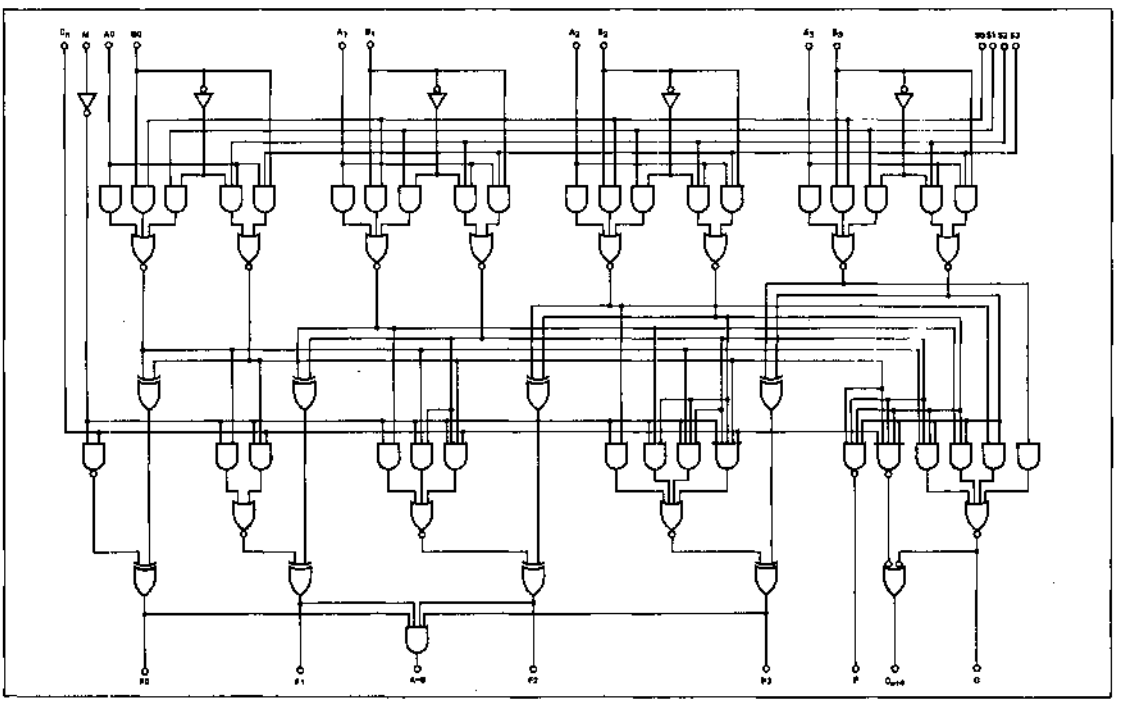
	Input C_n	Output C_{n+4}	Indicates
Active-high Data	H	H	A<B
	L	H	A<B
	H	L	A>B
	L	L	A>B
Active low Data	L	L	A<B
	H	L	A<B
	L	H	A>B
	H	H	A>B

FUNCTION TABLES

SELECTION $S_3 S_2 S_1 S_0$	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: $\overline{C_n}$ = 0	M = L; ARITHMETIC OPERATIONS: $\overline{C_n}$ = 1
		$\overline{C_n}$ = 1 = H	$\overline{C_n}$ = 0 = L
L L L L	$F = \overline{A}$	F = A	F = A PLUS 1
L L L H	$F = \overline{A+B}$	$F = A+\overline{B}$	$F = (A+\overline{B})$ PLUS 1
L L H L	$F = \overline{A}B$	$F = A+B$	$F = (A+\overline{B})$ PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L H L H	$F = \overline{B}$	$F = (A+B)$ PLUS $A\overline{B}$	$F = (A+B)$ PLUS $A\overline{B}$ PLUS 1
L H H L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H L L L	$F = \overline{A}+B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	$F = (A+\overline{B})$ PLUS AB	$F = (A+\overline{B})$ PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A	F = A PLUS A PLUS 1
H H L H	$F = A+\overline{B}$	$F = (A+B)$ PLUS A	$F = (A+\overline{B})$ PLUS A PLUS 1
H H H L	$F = A+B$	$F = (A+\overline{B})$ PLUS A	$F = (A+B)$ PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

SELECTION $S_3 S_2 S_1 S_0$	ACTIVE-LOW DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: C_n = 0	M = L; ARITHMETIC OPERATIONS: C_n = 1
		C_n = 0 = L	C_n = 1 = H
L L L L	$F = \overline{A}$	F = A MINUS 1	F = A
L L L H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L L H L	$F = \overline{A}+B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	$F = \overline{A+B}$	F = A PLUS $(A+\overline{B})$	F = A PLUS $(A+\overline{B})$ PLUS 1
L H L H	$F = \overline{B}$	F = AB PLUS $(A+\overline{B})$	F = AB PLUS $(A+\overline{B})$ PLUS 1
L H H L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = A+\overline{B}$	$F = A+\overline{B}$	$F = (A+\overline{B})$ PLUS 1
H L L L	$F = \overline{A}B$	F = A PLUS $(A+B)$	F = A PLUS $(A+B)$ PLUS 1
H L L H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	$F = A\overline{B}$ PLUS $(A+B)$	$F = A\overline{B}$ PLUS $(A+B)$ PLUS 1
H L H H	F = A + B	F = A + B	$F = (A+B)$ PLUS 1
H H L L	F = 0	F = A PLUS A	F = A PLUS A PLUS 1
H H L H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

LOGIC DIAGRAM



RECOMMENDED OPERATING CHARACTERISTICS

		S54181			N74181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			20	
	Low logic level			10			10	
Operating Free-Air Temperature Range, T_A		-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage any output except A=B	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_{OH}	High-level output current A=B only	V_{CC} = MIN V_{IL} = 0.8V,	V_{IN} = 2V V_{OH} = 5.5V				250	μA
I_{IH}	High-level input current (mode input)						40	μA
I_{IH}	High-level input current (any A or B input)						120	μA
I_{IH}	High-level input current (any S input)	V_{CC} = MAX,	V_I = 2.4V				160	μA
I_{IH}	High-level input current (carry input)						200	μA
I_{IH}	High-level input current (any input)	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (mode input)						-1.6	mA
I_{IL}	Low-level input current (any A or B input)						-4.8	mA
I_{IL}	Low-level input current (any S input)	V_{CC} = MAX,	V_I = 0.4V				-6.4	mA
I_{IL}	Low-level input current (carry input)						-8	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		S54181	-20		-55	mA
				N74181	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX		S54181		88	127	mA
				N74181		88	140	
I_{CC}	Supply current	V_{CC} = MAX		S54181		94	135	mA
				N74181		94	150	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (C_L = 15pF, R_L = 400Ω)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			12	18	ns
t_{PHL}					13	19	
t_{PLH}	C_n	Any F	M = 0V		13	19	ns
t_{PHL}			(SUM or DIFF mode)		12	18	
t_{PLH}	Any A or B	G	M = 0V, S0 = S3 = 4.5V,		13	19	ns
t_{PHL}			S1 = S2 = 0V (SUM mode)		13	19	
t_{PLH}	Any A or B	G	M = 0V, S0 = S3 = 0V,		17	25	ns
t_{PHL}			S1 = S2 = 4.5V (DIFF mode)		17	25	
t_{PLH}	Any A or B	P	M = 0V, S0 = S3 = 4.5V,		13	19	ns
t_{PHL}			S1 = S2 = 0V (SUM mode)		17	25	
t_{PLH}	Any A or B	P	M = 0V, S0 = S3 = 0V,		17	25	ns
t_{PHL}			S1 = S2 = 4.5V (DIFF mode)		17	25	
t_{PLH}	Any A or B	Any F	M = 0V, S0 = S3 = 4.5V,		28	42	ns
t_{PHL}			S1 = S2 = 0V (SUM mode)		21	32	
t_{PLH}	Any A or B	Any F	M = 0V, S0 = S3 = 0V,		32	48	ns
t_{PHL}			S1 = S2 = 4.5V (DIFF mode)		23	34	
t_{PLH}	Any A or B	Any F	M = 4.5V (logic mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	Any A or B	A = B	M = 0V, S0 = S3 = 0V,		35	50	ns
t_{PHL}			S1 = S2 = 4.5V (DIFF mode)		32	48	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

¶ t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation on delay time, high-to-low-level output

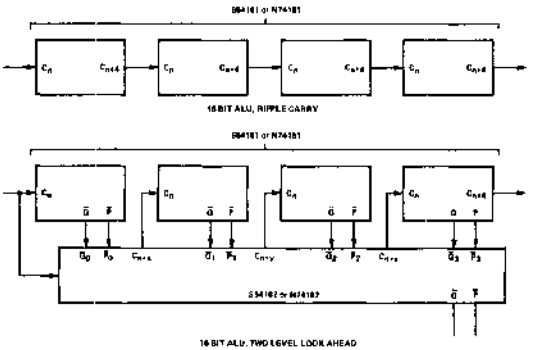
§ Not more than one output should be shorted at a time

TYPICAL APPLICATION DATA

Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

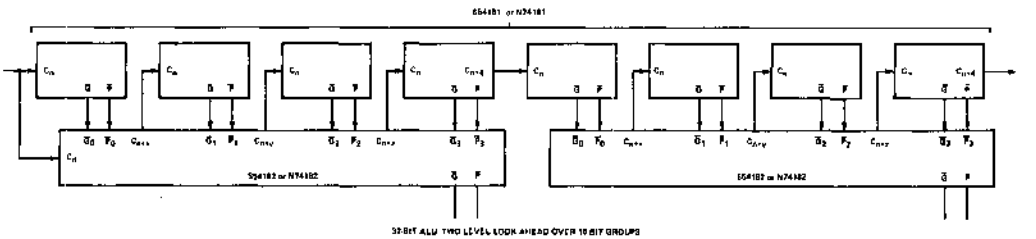
TYPICAL ADDITION TIMES

NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT	
			S54181/ N74181	S54182 N74182
4	24	6.0	1	
8	36	4.5	2	
12	48	4.0	3	
12	36	3.0	3	1
16	60	3.8	4	
16	36	2.2	4	1
32	120	3.8	8	
32	96	3.0	8	1
32	72	2.2	8	2
32	60	1.9	8	3
48	165	3.4	12	
48	148	3.1	12	1
48	132	2.7	12	2
48	108	2.2	12	3
48	60	1.25	12	4
64	220	3.5	16	
64	192	3.0	16	2
64	172	2.7	16	3
54	144	2.2	16	4
64	60	0.94	16	5

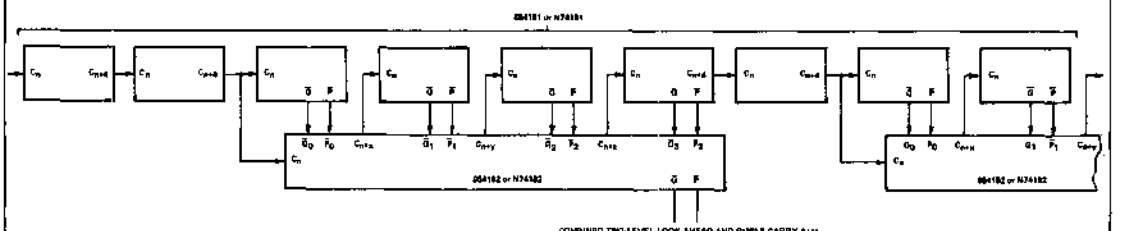


16-BIT ALU, RIPPLE CARRY

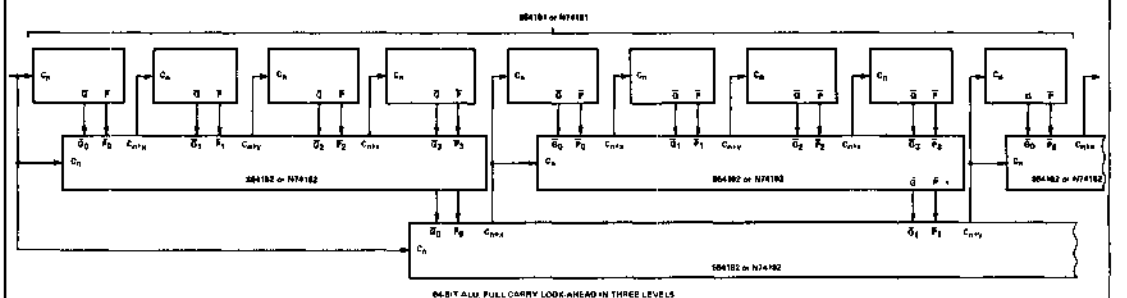
16-BIT ALU, TWO LEVEL LOOK AHEAD



32-BIT ALU TWO LEVEL LOOK AHEAD OVER 16-BIT GROUPS



COMBINED TWO-LEVEL LOOK AHEAD AND RIPPLE-CARRY ALU



64-BIT ALU, FULL CARRY LOOK-AHEAD IN THREE LEVELS

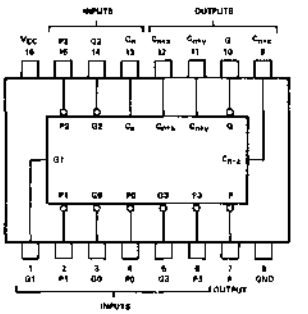
DESCRIPTION

The S54182, N74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanoseconds delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

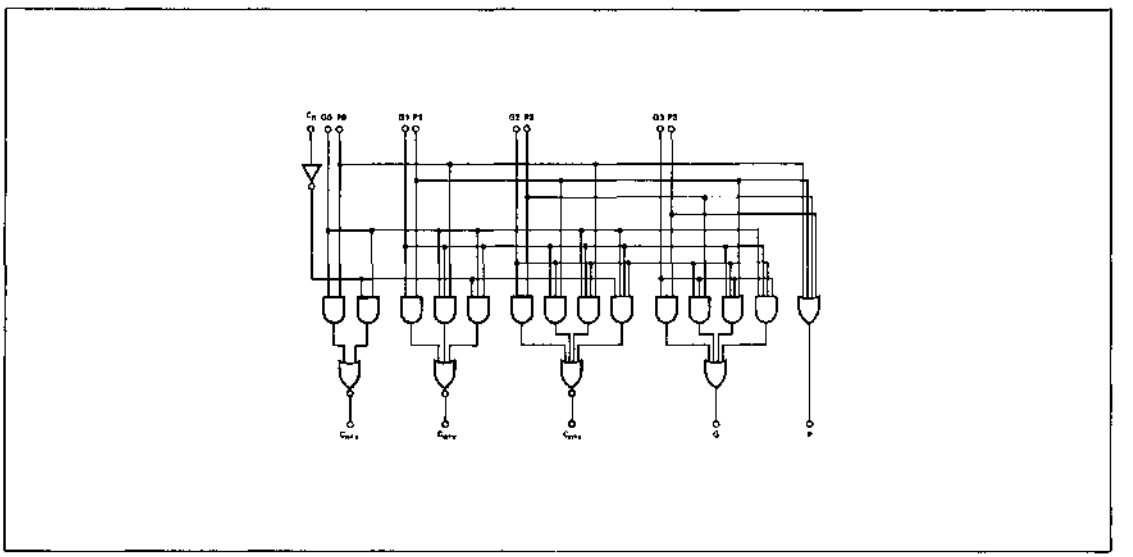
The S54182 or N74182, when used in conjunction with the S54181 or N74181 arithmetic logic unit (ALU), provides full high-speed carry look-ahead capability for up to n-bit words. Each S54182/N74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. Applications data for the S54181/N74181 illustrates cascading of S54182/N74182 circuits to perform multi-level look-ahead.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54182			N74182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (C_n input)						80	μA
I_{IH}	High-level input current (P3 input)						120	μA
I_{IH}	High-level input current (P2 input)						160	μA
I_{IH}	High-level input current (P0, P1, or G3 input)	V_{CC} = MAX,	V_I = 2.4V				200	μA
I_{IH}	High-level input current (G0 or G2 input)						360	μA
I_{IH}	High-level input current (G1 input)						400	μA
I_{IH}	High-level input current (any input)	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (C_n input)						−3.2	mA
I_{IL}	Low-level input current (P3 input)						−4.8	mA
I_{IL}	Low-level input current (P2 input)						−6.4	mA
I_{IL}	Low-level input current (P0, P1, or G3 input)	V_{CC} = MAX,	V_I = 0.4V				−8	mA
I_{IL}	Low-level input current (G0 or G2 input)						−14.4	mA
I_{IL}	Low-level input current (G1 input)						−16	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX		S54182		27		mA
				N74182		27		
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX		S54182		45	65	mA
				N74182		45	72	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 400Ω		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

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SYNCHRONOUS DECADE UP/DOWN COUNTER WITH PRESET INPUTS

S54192
N74192

S54192–B,F,W • N74192–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

This is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. The S54192 and N74192 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

These counters are fully programmable; that is, the outputs may be present to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

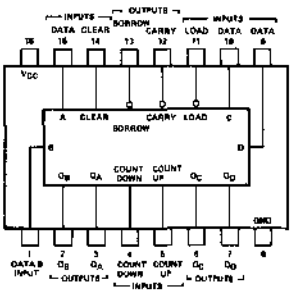
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

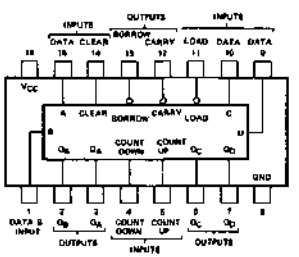
Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25MHz minimum.

PIN CONFIGURATIONS

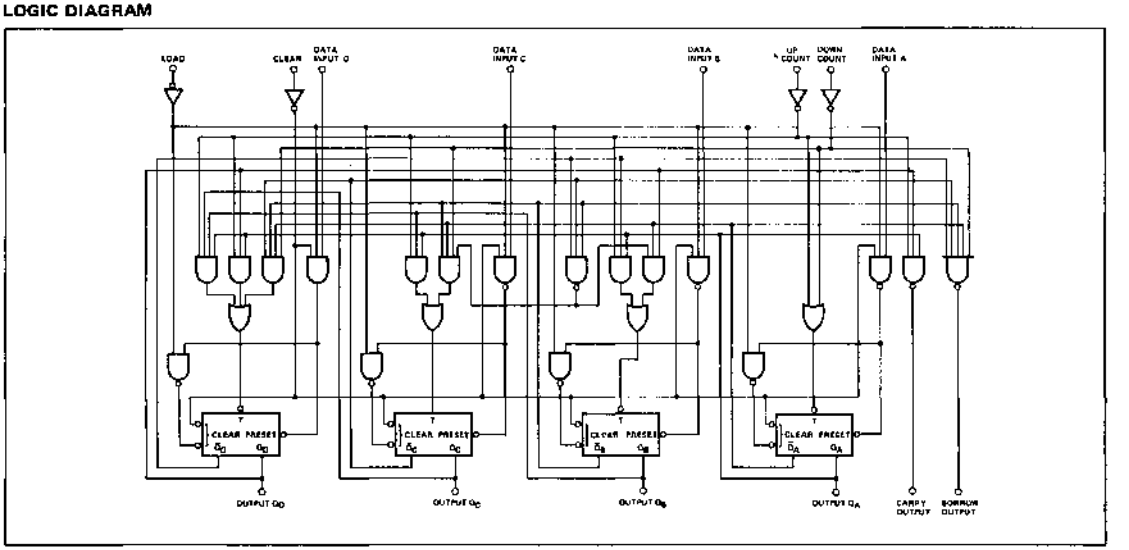
B, F PACKAGE



W PACKAGE

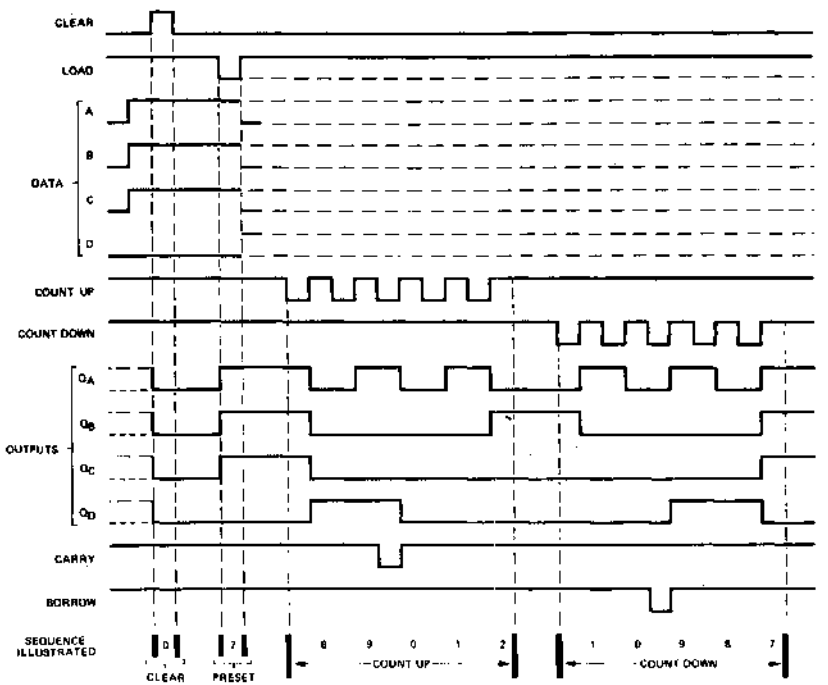


LOGIC DIAGRAM



DECADE COUNTER (typical clear, load, and count sequences)

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

RECOMMENDED OPERATING CONDITIONS

	S54192			N74192			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Input Count Frequency, f_{count}	0		25*	0		25*	MHz
Width of Any Input Pulse, t_w	20*			20*			ns
Data Setup Time, t_{setup} (See Note 2)	20*			20*			ns
Data Hold Time, t_{hold} (See Note 3)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
S54192						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	-20		-65	mA
I_{CC}	Supply current	V_{CC} = MAX		65	89	mA
N74192						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	-18		-65	mA
I_{CC}	Supply current	V_{CC} = MAX		65	102	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (See Note)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{setup}	Minimum input setup time			14	20	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from count-up input			17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from count-up input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level borrow output from count-down input			16	24	ns
t_{PHL}	Propagation delay time, high-to low-level borrow output from count-down input			18	24	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from either count input			25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either count input			31	47	ns
t_{PLH} LOAD				27		
t_{PLH} LOAD				29	40	
t_{PHL} CLEAR				22	25	

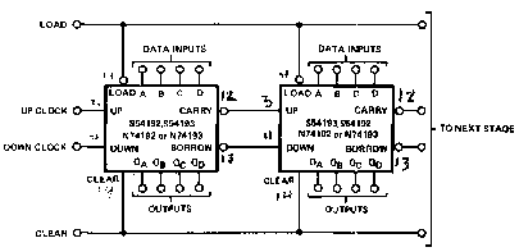
NOTE: Above Switching Table Applies to (S54192 & N74192)

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

CASCADING



Circuitry is provided internally for cascading these counters. The mode of cascading shown is ripple borrow/carry. No external components are required.

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SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH PRESET INPUTS

S54193 N74193

S54193–B,F,W • N74193–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54193 and N74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The oututs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

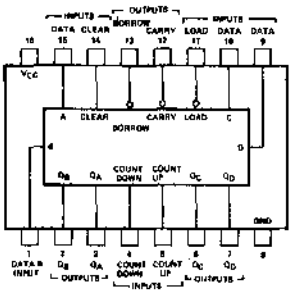
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

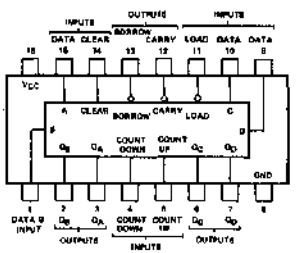
Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

PIN CONFIGURATIONS

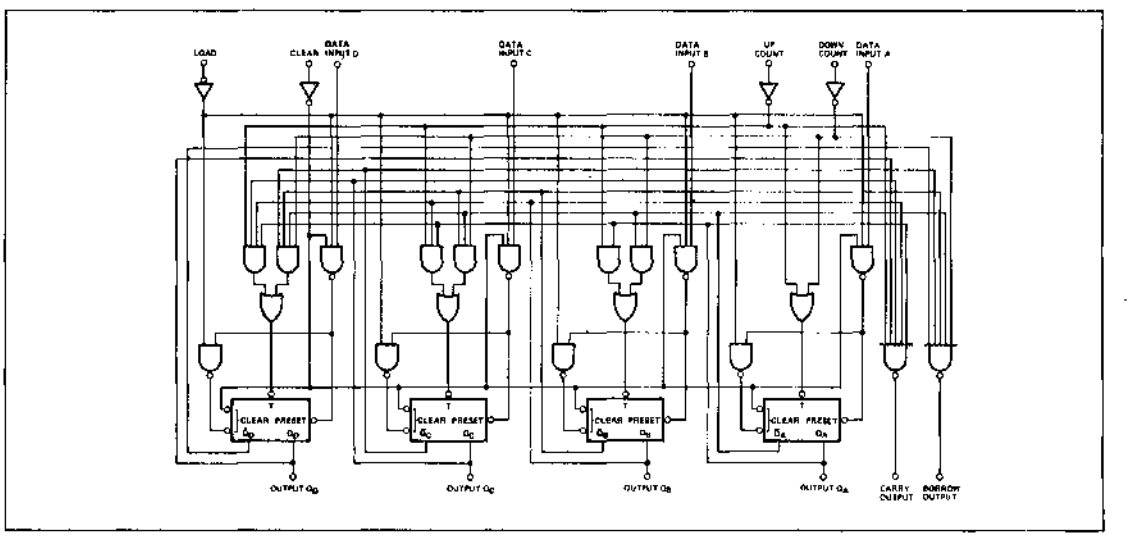
W PACKAGE



B,F PACKAGE

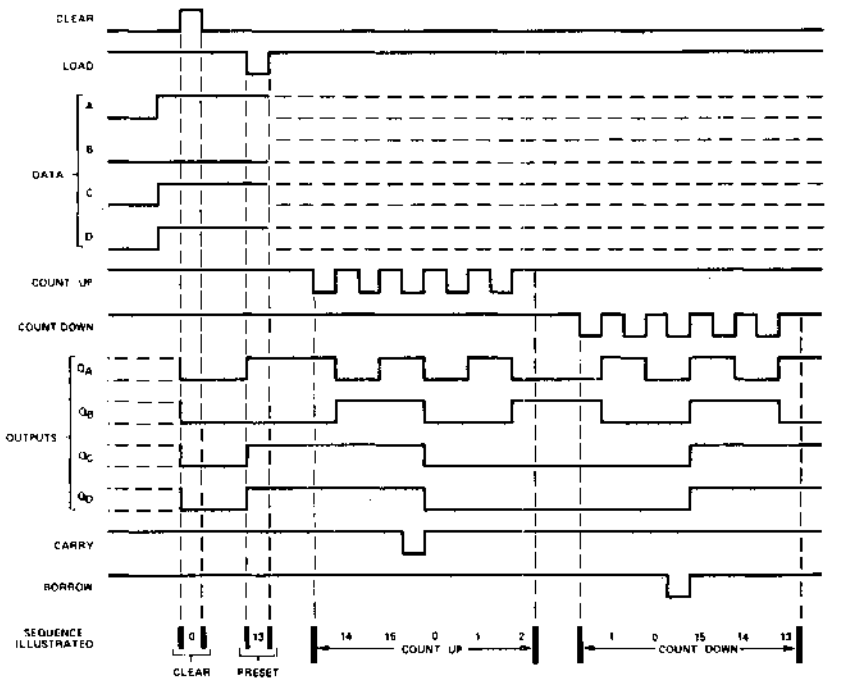


LOGIC DIAGRAM



BINARY COUNTER (typical clear, load, and count sequences)

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

RECOMMENDED OPERATING CONDITIONS

	S54193			N74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Input Count Frequency, f_{count}	0		25*	0		25*	MHz
Width of Any Input Pulse, t_w	20*			20*			ns
Data Setup Time, t_{setup} (See Note 1)	20*			20*			ns
Data Hold Time, t_{hold} (See Note 2)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:
1. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
S54193							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		−20		−65	mA
I_{CC}	Supply current	V_{CC} = MAX			65	89	mA
N74193							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX			65	102	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (See Note)

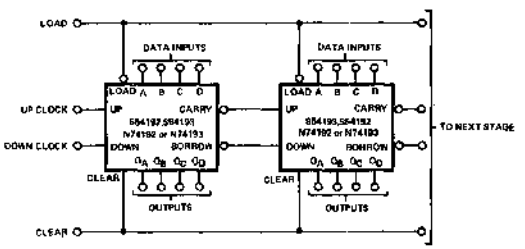
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{setup}	Minimum input setup time			14	20	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from count-up input			17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from count-up input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level borrow output from count-down input			16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level borrow output from count-down input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from either count input			25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either count input			31	47	ns
t_{PLH} LOAD				27	40	
t_{PLH} LOAD				29	40	
t_{PHL} CLEAR				22	25	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

CASCADING



Circuitry is provided internally for cascading these counters. The mode of cascading shown is ripple borrow/carry. No external components are required.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

S54194—B,F,W • N74194—B,F

DIGITAL 54/74 TTL SERIES

S54194
N74194

DESCRIPTION

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

	MODE CONTROL S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Hold)	L	L

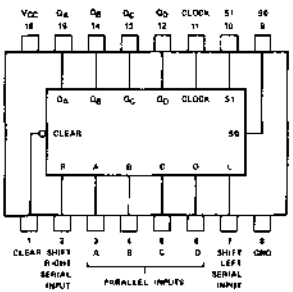
In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

These 4-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195mW.

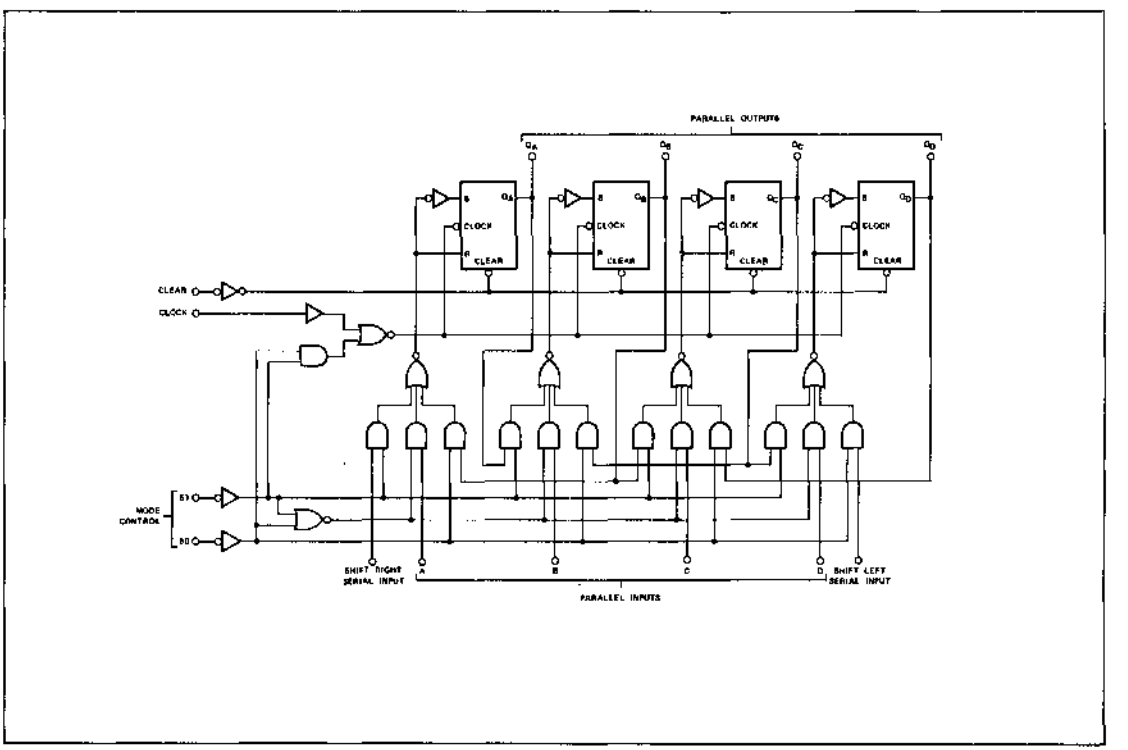
The S54194 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74194 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54194			N74194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Setup Time, t_{setup}: Mode control	30			30			ns
Serial and parallel data	20			20			ns
Clear inactive-state	25			25			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800µA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V				40	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		S54194	-20		-57	mA
				N74194	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			39	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF,	R_L = 400Ω	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

signetics

4-BIT PARALLEL-ACCESS SHIFT REGISTER

S54195-B,F,W • N74195-B, F

DIGITAL 54/74 TTL SERIES

S54195 N74195

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

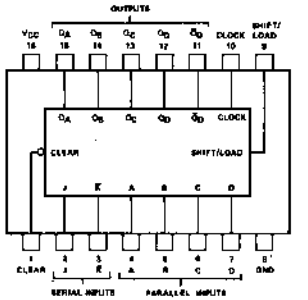
Parallel loading is accomplished by applying the 4 bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode are entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The S54195 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74195 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	K	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

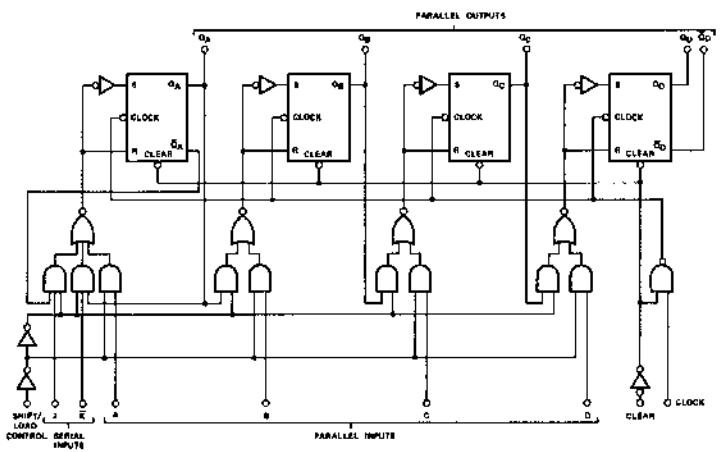
H = High Level, L = Low Level

NOTES A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

C. Q_{An} = state of Q_A at t_n

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54195			N74195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		30	0		30	MHz
Width of Clock Input Pulse, $t_{w(clock)}$	16			16			ns
Width of Clear Input Pulse, $t_{w(clear)}$	12			12			ns
Setup Time, t_{setup}: Shift/load	25			25			
Serial and parallel data	15			15			ns
Clear inactive-state	25			25			
Shift/Load Release Time, $t_{release}$			10			10	ns
Serial and Parallel Data Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		S54195	-20		-57	mA
				N74195	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note			39	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency			30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15pF,	R_L = 400Ω	6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

NOTE With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.

DESCRIPTION

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C. Series 74 devices are characterized for operation from 0°C to 70°C.

The bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

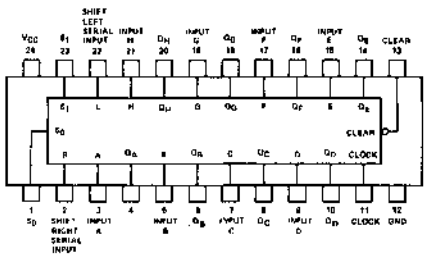
Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

Average power dissipation per gate is typically 4.15 mW.

PIN CONFIGURATIONS

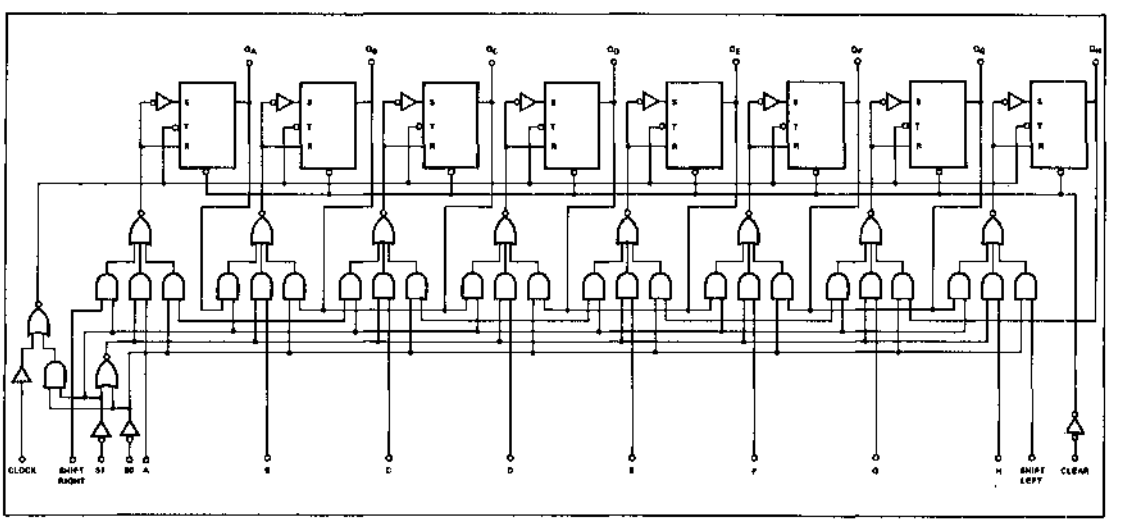
N,F,Q PACKAGE



TRUTH TABLE

OPERATION OF MODE CONTROL		
INPUTS		MODE
S_1	S_0	
L	L	INHIBIT CLOCK
H	L	SHIFT LEFT
L	H	SHIFT RIGHT
H	H	PARALLEL LOAD

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54198			N74198			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54198			N74198			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800µA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54198, N74198	Serial input, S_0, S_1	Clock	Clear, Inputs A thru H

DESCRIPTION

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

These synchronous 8-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

Parallel loading is accomplished by applying the 8 bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

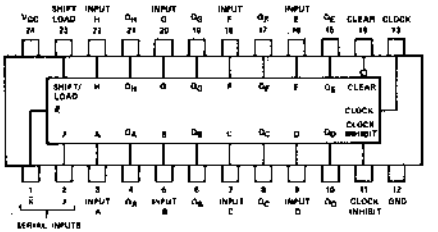
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-K inputs. See the J-K inputs truth table for states required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

PIN CONFIGURATIONS

N,F,Q PACKAGES



†Pin assignments for these circuits are the same for all packages.

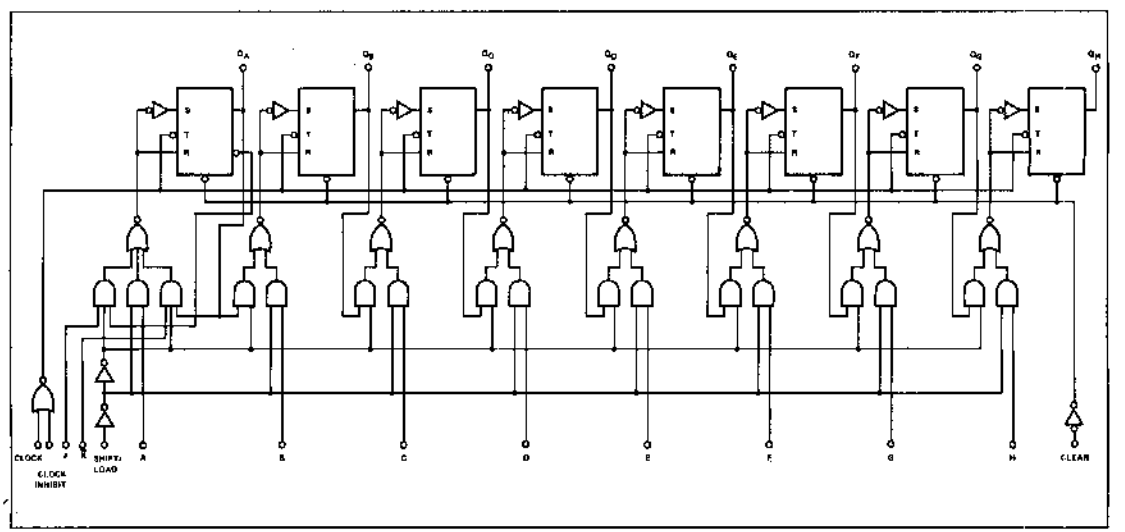
TRUTH TABLE

INPUTS at t_n		OUTPUT t_{n+1}
J	$\overline{K}$	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

H = high level, L = low level

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54199			N74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out From each output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		S54199			N74199			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

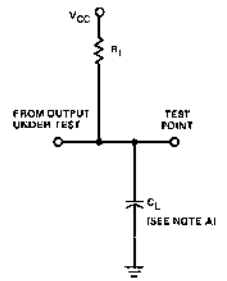
TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54199, N74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

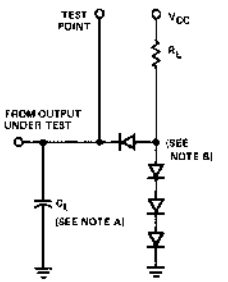
54/74 And 54/74H Typical A.C. Loads And Waveforms

PARAMETER MEASUREMENT INFORMATION

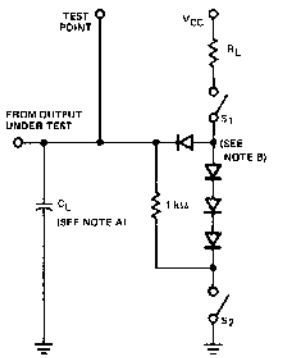
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



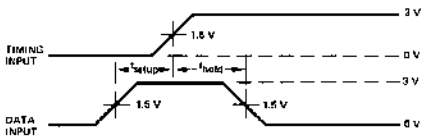
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



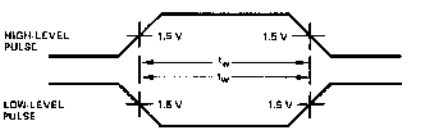
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

TYPICAL AC WAVEFORMS

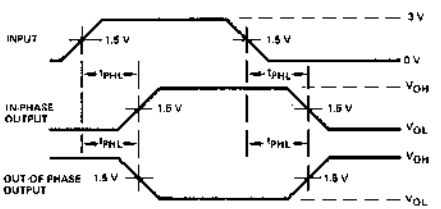
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



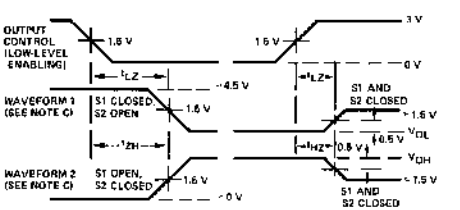
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS



NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR $\leq$ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

signetics

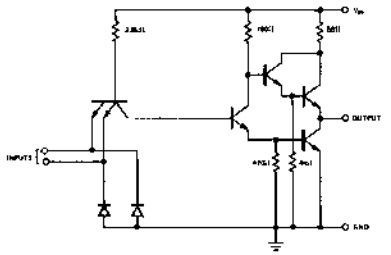
QUADRUPLE 2-INPUT POSITIVE NAND GATE

S54H00 N74H00

S54H00–A,F,W • N74H00–A,F

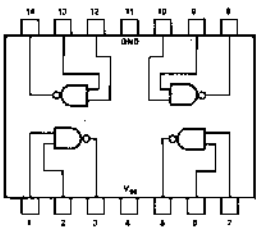
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

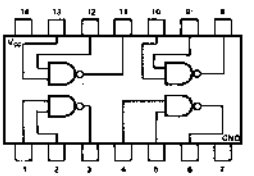


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H00 Circuits	4.5	5	5.5	V
	N74H00 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H00 Circuits	-55	25	125	°C
	N74H00 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		10	16.8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.2	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		5.9	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

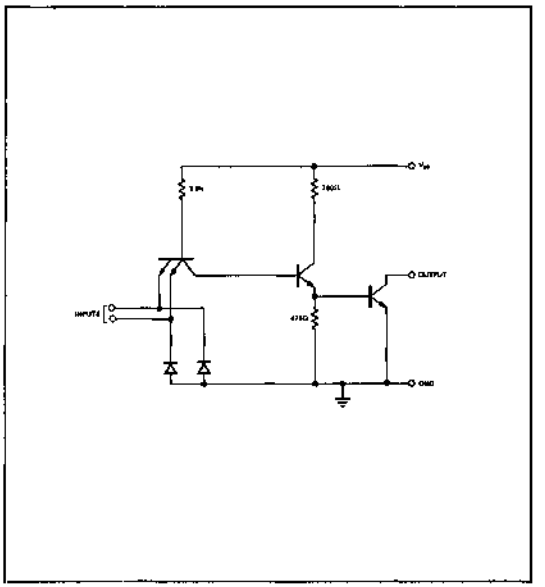
signetics QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S54H01 N74H01

S54H01–A,F,W • N74H01–A,F

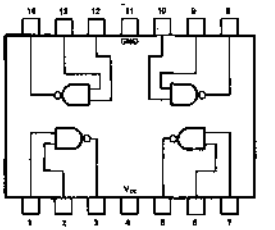
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

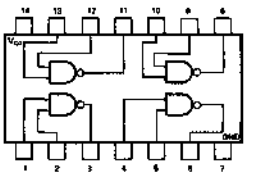


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H01 Circuits		4.5	5	5.5	V
N74H01 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H01 Circuits	-55	25	125	°C
	N74H01 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

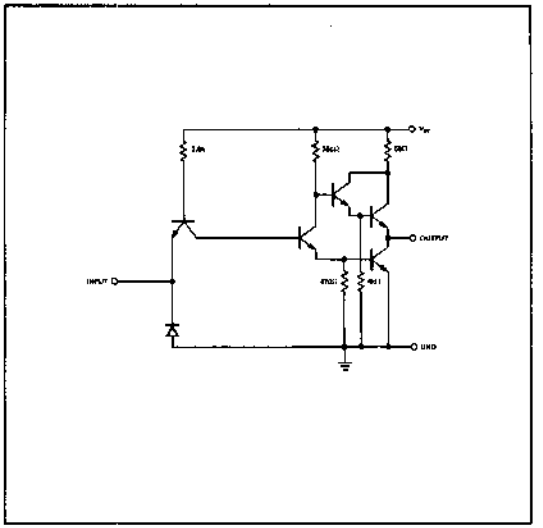
PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX	V_{in} = 0		6.8	10.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS†		MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.5	12.0	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		10.0	15.0	ns

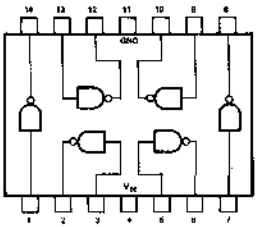
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Load resistor R_L is connected from V_{CC} to the output, and load capacitor C_L is connected from the output to ground.

SCHEMATIC (each inverter)

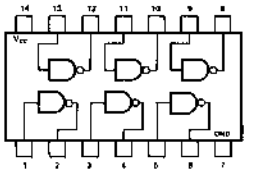


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H04 Circuits		4.5	5	5.5	V
N74H04 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H04 Circuits	-55	25	125	°C
	N74H04 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

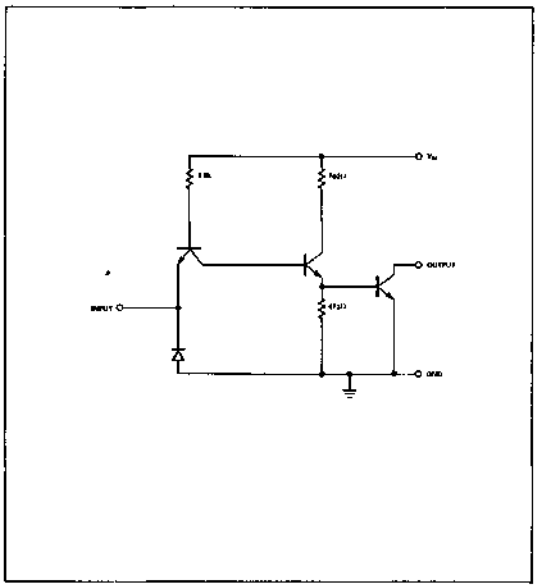
PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V,		40.0	58.0	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0,		16.0	26.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.5	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		9.0	13.0	ns

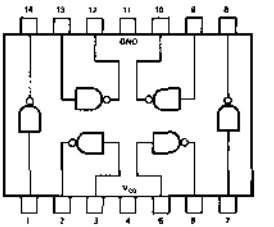
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

SCHEMATIC (each inverter)

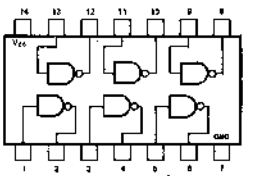


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGES



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H05 Circuits		4.5	5	5.5	V
N74H05 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H05 Circuits	-55	25	125	°C
	N74H05 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	µA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V			50	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		40.0	58.0	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		16.0	26.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

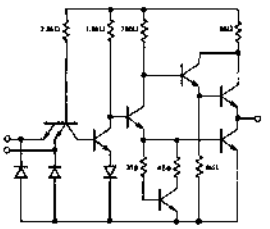
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 26pF,	R_L = 280Ω		10	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		13	18	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

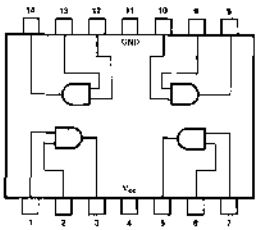
† Load resistor R_L is connected from V_{CC} to the output, and load capacitor C_L is connected from the output to ground.

SCHEMATIC (each gate)

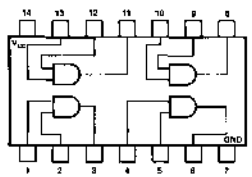


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:				
S54H08 Circuits	4.5	5	5.5	V
N74H08 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A:				
S54H08 Circuits	-55	25	125	°C
N74H08 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN,	$V_{out(1)} \geq$ .4V	2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 0 level at output	V_{CC} = MIN,	$V_{out(0)} \leq$ 2.4V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = 500μA	V_{in} = 2.0V	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 0.8V			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		40	64	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		24	40	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CI}	Input negative clamp voltage	V_{CC} = 5V I_{in} = -12.0mA T_A = 25°C			-1.5	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

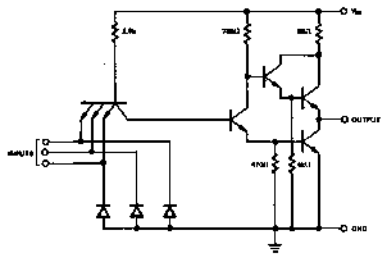
PARAMETER		TEST CONDITIONS	MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		7.5	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at: V_{CC} = 5V, T_A = 25°C.

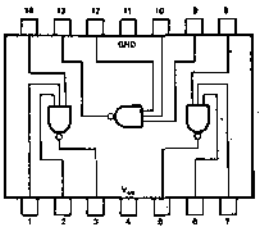
† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

SCHEMATIC (each gate)

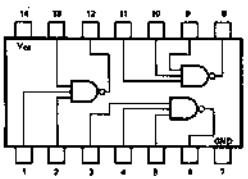


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H10 Circuits	4.5	5	5.5	V
	N74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H10 Circuits	-55	25	125	°C
	N74H10 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			– 2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		–40		–100	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		19.5	30	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		7.5	12.6	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

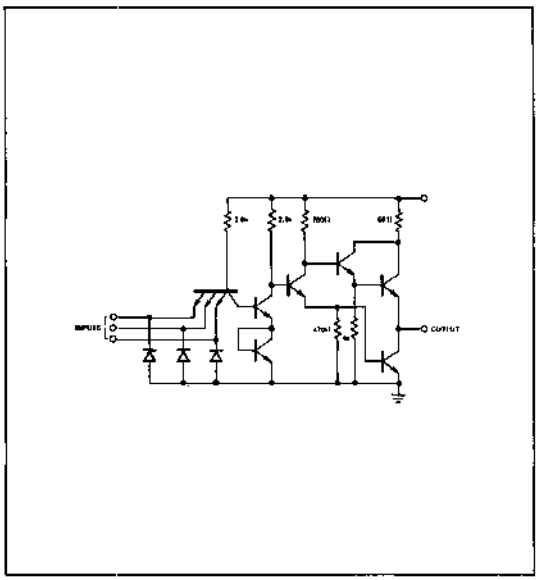
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.3	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		6.9	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

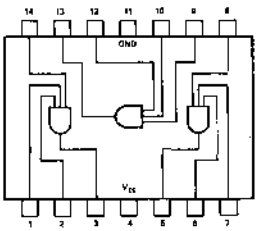
† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

SCHEMATIC (each gate)

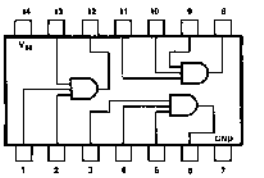


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H11 Circuits		4.5	5	5.5	V
N74H11 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H11 Circuits	-55	25	125	°C
	N74H11 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 0 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	$V_{in(1)}$ = 2V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	$V_{in(0)}$ = 0.8V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 4.5V	-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		30	48	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		18	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

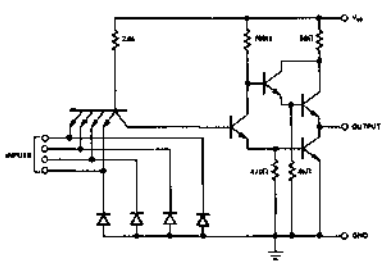
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		8.8	12	ns
t_{pd1}	Propagation delay time	C_L = 25pF, R_L = 280Ω		7.6	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

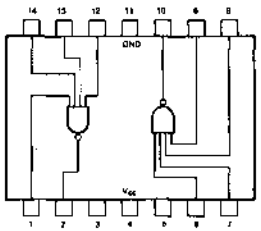
†Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

SCHEMATIC (each gate)

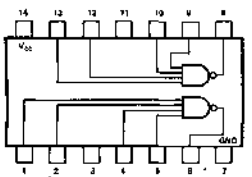


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}:	S54H20 Circuits	4.5	5	5.5	V
	N74H20 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H20 Circuits	−55	25	125	°C
	N74H20 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		5	8.4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

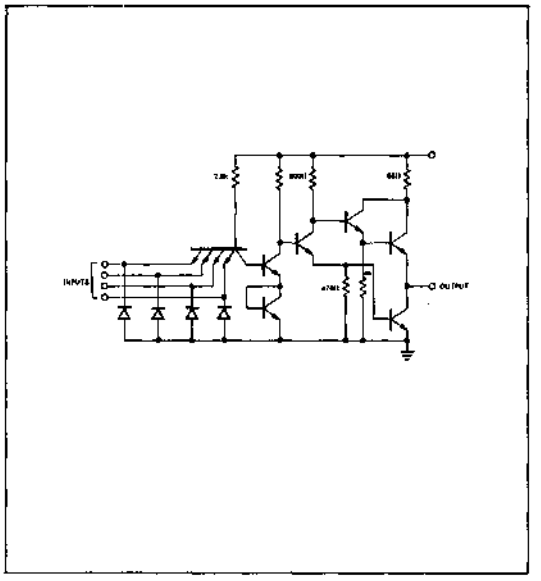
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		7	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		6	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

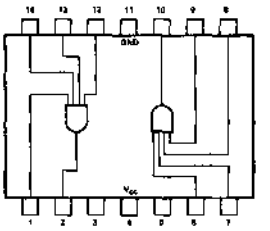
† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

SCHEMATIC (each gate)

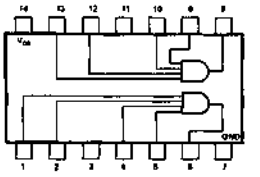


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H21 Circuits		4.5	5	5.5	V
N74H21 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H21 Circuits	-55	25	125	°C
	N74H21 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 0 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	$V_{in(1)}$ = 2V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	$V_{in(0)}$ = 0.8V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 4.5V	-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		20	32	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		12	20	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		7.6	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

signetics

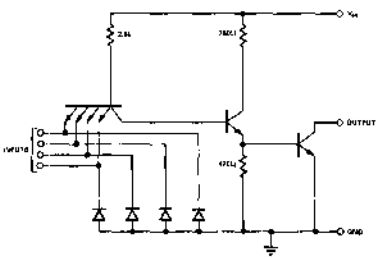
DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S54H22 N74H22

S54H22–A,F,W • N74H22–A,F

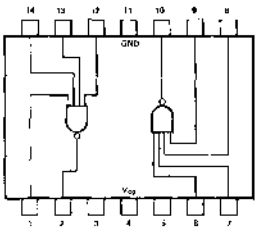
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

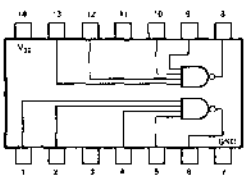


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H22 Circuits	4.5	5	5.5	V
N74H22 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range: S54H22 Circuits	-55	25	125	°C
N74H22 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

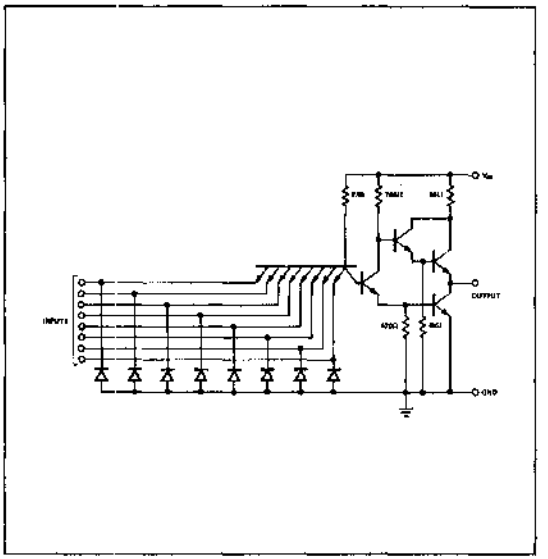
PARAMETER		TEST CONDITIONS*		MIN	TYP††	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		3.4	5.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS†		MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.5	12.0	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		10.0	15.0	ns

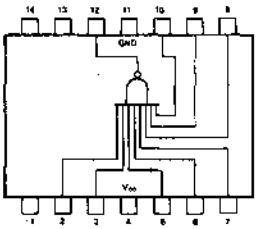
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

SCHEMATIC (each gate)

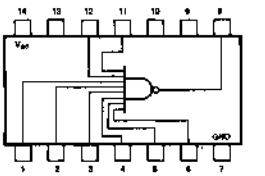


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H30 Circuits	4.5	5	5.5	V
	N74H30 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H30 Circuits	-55	25	125	°C
	N74H30 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		6.5	10	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		2.5	4.2	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

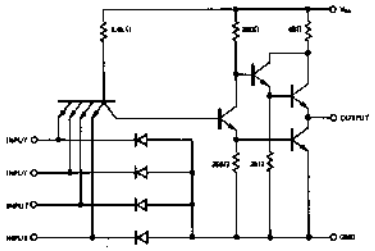
PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		8.9	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		6.8	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at: V_{CC} = 5V, T_A = 25°C.

† Duration of short circuit test should not exceed 1 second.

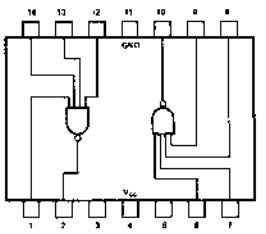
SCHEMATIC (each gate)



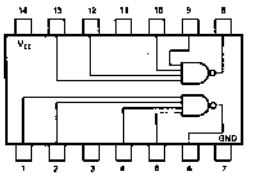
NOTES:
1. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H40 Circuits		4.5	5	5.5	V
N74H40 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				30	
Operating Free-Air Temperature Range, T_A:	S54H40 Circuits	−55	25	125	°C
	N74H40 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −1.5mA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 60mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−4	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			100	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX		−40		−125	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		25	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		10.4	16	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

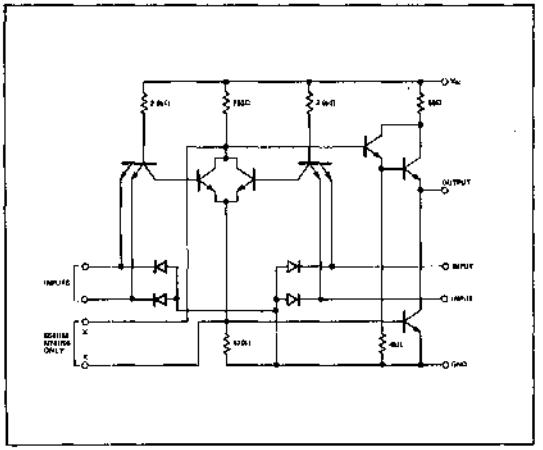
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 93Ω		6.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 93Ω		8.5	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

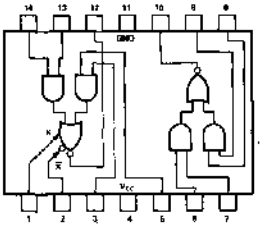
† All typical values are at V_{CC} = 5V, T_A = 25°C.

SCHEMATIC (each gate)



PIN CONFIGURATIONS

W PACKAGE



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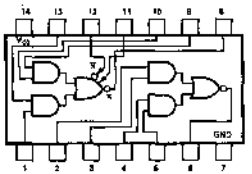


NOTES:
1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the S54H50 and N74H50 circuits only. Make no external connection to X and $\overline{X}$ pins of the S54H51 and N74H51.
5. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H50, S54H51 Circuits	4.5	5	5.5	V
N74H50, N74H51 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A: S54H50, S54H51 Circuits	-55	25	125	°C
N74H50, N74H51 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	Short circuit output current **	V_{CC} = MAX	-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX, V_{in} = 4.5V		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX, V_{in} = 0		8.2	12.8	mA

ELECTRICAL CHARACTERISTICS (S54H50 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V			-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA, I_1 = 700μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_1 = 320μA, I_2 = -320μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA, I_1 = 470μA, R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H50 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = 0°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V			-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA, I_1 = 1.1mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -600μA, I_1 = 570μA, I_2 = -570μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA, I_1 = 600μA, R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		6.8	11	ns

SWITCHING CHARACTERISTICS, (S54H50/N74H50 circuits only), V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		11		ns

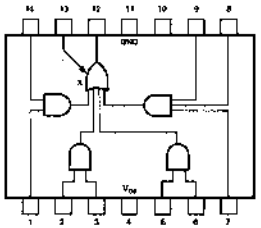
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

PIN CONFIGURATIONS

W PACKAGE



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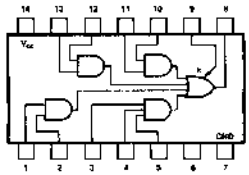
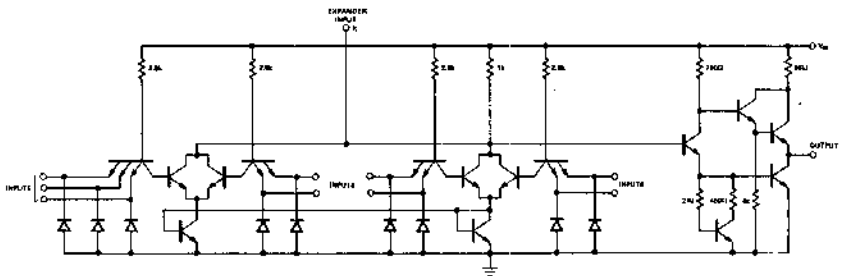


SCHEMATIC DIAGRAM



NOTE:
1. A total of six expander gates may be connected to the expander input.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H52 Circuits	4.5	5	5.5	V
	N74H52 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H52 Circuits	-55	25	125	°C
	N74H52 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 1 at output	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 0 at output	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, V_{in} = 2V, I_{load} = -500μA	2.4			V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 0.8V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 4.5V	-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		20	31	mA

ELECTRICAL CHARACTERISTICS (S54H52 circuits only) using expander input, V_{CC} = 4.5V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	V_X = 1V, T_A = -55°C	I_{load} = -500μA,	-2.7		-4.5	mA
$V_{out(1)}$	Logical 1 output voltage	V_X = 1V, T_A = -55°C	I_{load} = -500μA,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{inX} = -300μA, T_A = 125°C	I_{sink} = 20mA,			0.4	V

ELECTRICAL CHARACTERISTICS (N74H52 circuits only) using expander input, V_{CC} = 4.75V

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	V_X = 1V,	I_{load} = -500μA,	T_A = 0°C	-2.9		-5.35	mA
$V_{out(1)}$	Logical 1 output voltage	V_X = 1V,	I_{load} = -500μA,	T_A = 0°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{inX} = -300μA,	I_{sink} = 20mA,	T_A = 70°C			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pin is open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		9.2	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		10.6	15	ns

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15pF

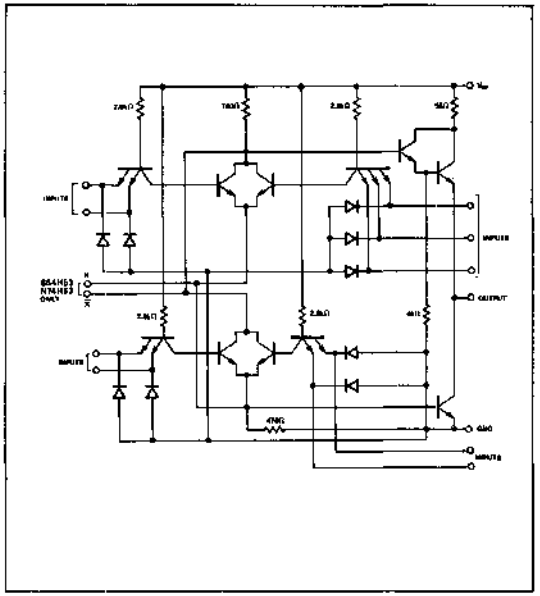
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		9.8		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		14.8		ns

* For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions for the applicable device type. Expander pin is open.

** Duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

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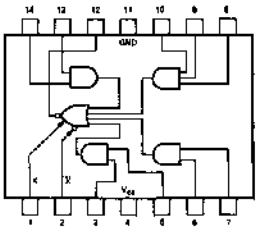

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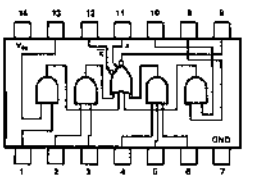


NOTES:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the S54H53 and N74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the S54H54 and N74H54.
5. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H53, S54H54 Circuits	4.5	5	5.5	V
	N74H53, N74H54 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H53, S54H54 Circuits	−55	25	125	°C
	N74H53, N74H54 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−2	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V				50 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		9.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		7.1	11	mA

ELECTRICAL CHARACTERISTICS (S54H53 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 700μA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -320μA	I_1 = 320μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA	I_1 = 470μA,	R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H53 circuits only) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 1.1mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -570μA	I_1 = 570μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 600μA,	R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		7	11	ns

SWITCHING CHARACTERISTICS, (S54H53/N74H53 circuits only) V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15 pF

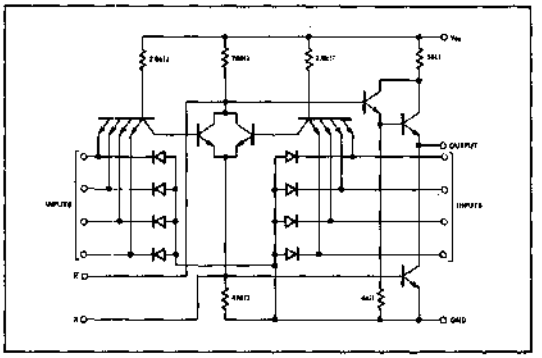
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		11.4		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

** Duration of short circuit test should not exceed 1 second.

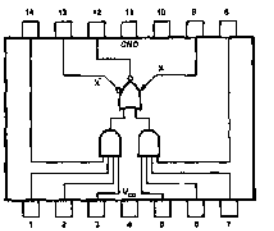
† All typical values are at V_{CC} = 5V, T_A = 25°C.

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

W PACKAGE



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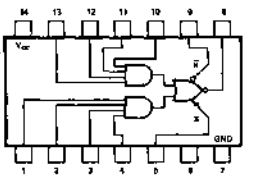


NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and X pins open.
4. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H55 Circuits		4.5	5	5.5	V
N74H55 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H55 Circuits	-55	25	125	°C
	N74H55 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		7.5	12	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4.5	6.4	mA

ELECTRICAL CHARACTERISTICS (S54H55 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 700μA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -320μA	I_1 = 320μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 470μA,	R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H55 circuits only) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 1.1mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA I_2 = -570μA	I_1 = 570μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 600μA,	R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.5	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		7	11	ns

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.7		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		11.4		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
** Duration of short circuit test should not exceed 1 second.
† All typical values are at V_{CC} = 5V, T_A = 25°C.

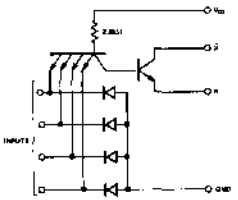
DUAL 4-INPUT EXPANDER (FOR USE WITH S54H50, S54H53, S54H55 CIRCUITS)

S54H60

S54H60—A,F,W

DIGITAL 54/74 TTL SERIES

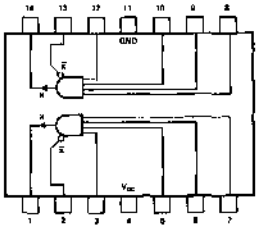
SCHEMATIC (each expander)



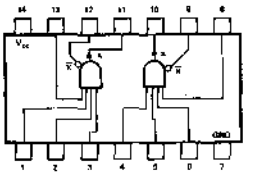
NOTES:
1. Connect to X input of S54H50, S54H53, or S54H55 circuit.
2. Connect to $\overline{X}$ input of S54H50, S54H53, or S54H55 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S54H50, S54H53, or S54H55 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = –55°C to 125°C)

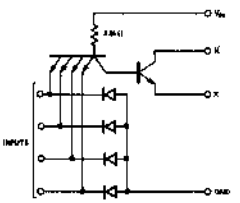
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.5V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, I_{on} = 5.85mA,	V_{in} = 2V, T_A = –55°	V_1 = 1V,			0.4	V
		V_{CC} = 5.5V I_{on} = 7.85mA,	V_{in} = 2V, T_A = 125°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 575Ω,	V_{in} = 0.8V, T_A = –55°C	V_1 = 4.5V,			320	μA
I_{on}	On-state output current	V_{CC}= 4.5V, T_A = –55°C	V_{in} = 2V,	V_1 = 1V,	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V	V_{in} = 0.4V				–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V, V_{CC} = 5.5V,	V_{in} = 2.4V V_{in} = 5.5V				50 1	μA mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 4.5V,			1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC}= 5.5V, V_1 = 0.85V	V_{in} = 0,			3	4.5	mA

† All typical values are at V_{CC} = 5V, T_A = 25°C.

OUTPUT CAPACITANCE V_{CC} and GND terminals open, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_X	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

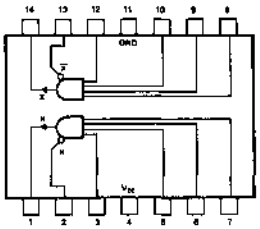
SCHEMATIC (each expander)



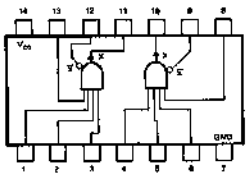
NOTES:
1. Connect to X input of N74H50, N74H53, or N74H55 circuit.
2. Connect to $\overline{X}$ input of N74H50, N74H53, or N74H55 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.75V to 5.25V
Maximum number of expanders that may be fanned-in to one N74H50, N74H53, or N74H55 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = 0°C to 70°C)

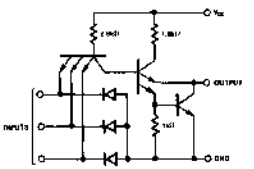
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.75V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.75V					0.8	V
V_{OS}	On-state output voltage	V_{CC} = 4.75V, I_{on} = 6.3mA,	V_{in} = 2V, T_A = 0°C	V_1 = 1V,			0.4	V
		V_{CC} = 5.25V, I_{on} = 7.4mA,	V_{in} = 2V, T_A = 70°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.75V, R = 576Ω	V_{in} = 0.8V, T_A = 0°C	V_1 = 4.6V,			570	µA
I_{on}	On-state output current	V_{CC} = 4.75V, T_A = 0°C	V_{in} = 2V,	V_1 = 1V,	–600			µA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 0.4V				–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 2.4V				50	µA
		V_{CC} = 5.25V,	V_{in} = 5.5V				1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.25V, V_1 = 0.85V	V_{in} = 4.5V,			1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.25V, V_1 = 0.85V	V_{in} = 0,			3	4.5	mA

OUTPUT CAPACITANCE V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

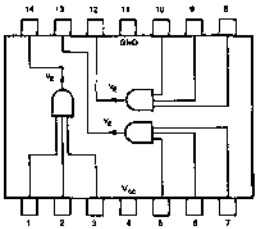
† All typical values are at V_{CC} = 5V, T_A = 25°C

SCHEMATIC (each expander)

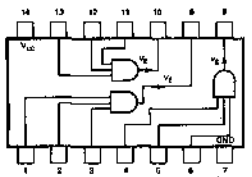


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:
1. Component values shown are nominal.
2. A total of six expander gates may be connected to the S54H52/N74H52 expander input.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H61 Circuits	4.5	5	5.5	V
	N74H61 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H61 Circuits	-55	25	125	°C
	N74H61 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = MIN				0.8	V
I_{off}	Off-state reverse current	V_{CC} = MIN, V_{off} = 2.2V,	$V_{in(0)}$ = 0.8V, T_A = MAX			50	μA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = MAX,	V_{in} = 4.5V		11	16	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = MAX,	V_{in} = 0		5	7	mA

ELECTRICAL CHARACTERISTICS S54H61 circuits only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.5V	2			V
V_{on}	On-state output voltage	V_{CC} = 4.5V, $V_{in(1)}$ = 2V, I_{on} = 4.5mA, T_A = −55°C			1	V

ELECTRICAL CHARACTERISTICS N74H61 circuits only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.75V	2			V
V_{on}	On-state output voltage	V_{CC} = 4.75V, $V_{in(1)}$ = 2V, I_{on} = 5.35mA, T_A = 0°C			1	V

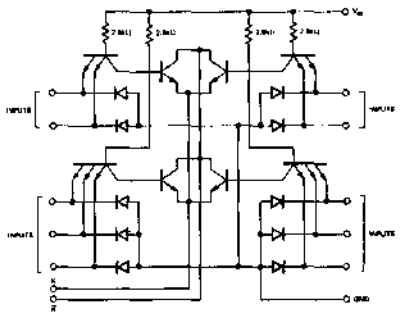
OUTPUT CAPACITANCE, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

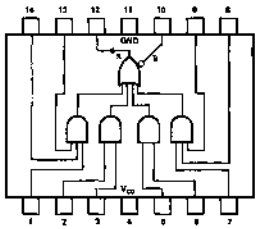
† All typical values are at V_{CC} = 5V, T_A = 25°C

SCHEMATIC (each gate)

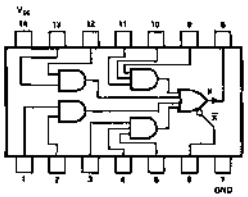


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:
1. Connect to X input of S54H50, S54H53, or S54H55 circuit
2. Connect to $\overline{X}$ input of S54H50, S54H53, or S54H55 circuit
3. Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S54H50, S54H53, or S54H55 circuit	1

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	V_{CC} = 4.5V,					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, I_{on} = 5.85mA,	V_{in} = 2V, T_A = –55°C	V_1 = 1V,			0.4	V
		V_{CC} = 5.5V, I_{on} = 7.85mA,	V_{in} = 2V, T_A = 125°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 575Ω,	V_{in} = 0.8V, T_A = –55°C	V_1 = 4.5V,			320	µA
I_{on}	On-state output current	V_{CC} = 4.5V, T_A = –55°C	V_{in} = 2V,	V_1 = 1V,	–470			µA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 2.4V			50	μA
		V_{CC} = 5.5V,	V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 4.5V,		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 0,		6	9	mA

OUTPUT CAPACITANCE, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capaitance of output transistor Q_1	f = 1 MHz		1.3		pF

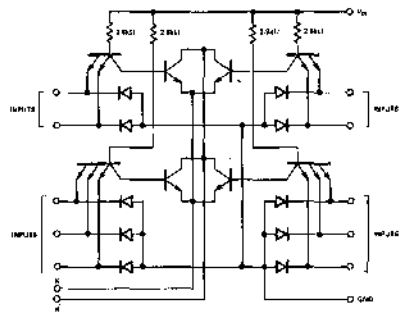
†All typical values are at V_{CC} = 5V, T_A = 25°C.

signetics 3-2-2-3-INPUT AND-OR EXPANDER (FOR USE WITH N74H50, N74H53, N74H55 CIRCUITS) N74H62

N74H62–A,F

DIGITAL 54/74 TTL SERIES

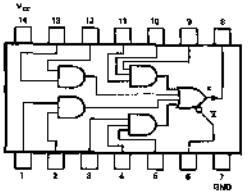
SCHEMATIC (each gate)



NOTES:
1. Connect to X input of N74H50, N74H53, or N74H55 circuit.
2. Connect to $\overline{X}$ input of N74H50, N74H53, or N74H55 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.75V to 5.25V
Maximum number of expanders that may be fanned-in to one N74H50, N74H53, or N74H55 circuit	1

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	V_{CC} = 4.75V			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	V_{CC} = 4.75V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.75V, I_{on} = 6.3mA,	V_{in} = 2V, T_A = 0°C	V_I = 1V,			0.4	V
		V_{CC} = 5.25V, I_{on} = 7.4mA,	V_{in} = 2V, T_A = 70°C	V_I = 0.8V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.75V, R = 575Ω,	V_{in} = 0.8V, T_A = 0°C	V_I = 4.5V,			570	μA
I_{on}	On-state output current	V_{CC} = 4.75V, T_A = 0°C	V_{in} = 2V,	V_I = 1V,	−600			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 2.4V			50	µA
		V_{CC} = 5.25V,	V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.25V, V_1 = 0.85V	V_{in} = 4.5V,		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.25V, V_1 = 0.85V	V_{in} = 0,		6	9	mA

OUTPUT CAPACITANCE V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

†All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND-OR gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

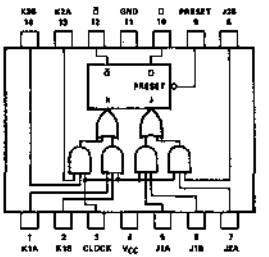
TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

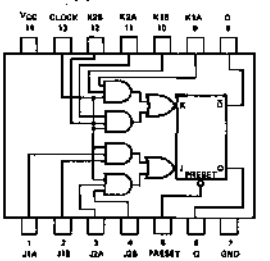
NOTES:
1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse.
4. t_n+1 = Bit time after clock pulse.

PIN CONFIGURATIONS

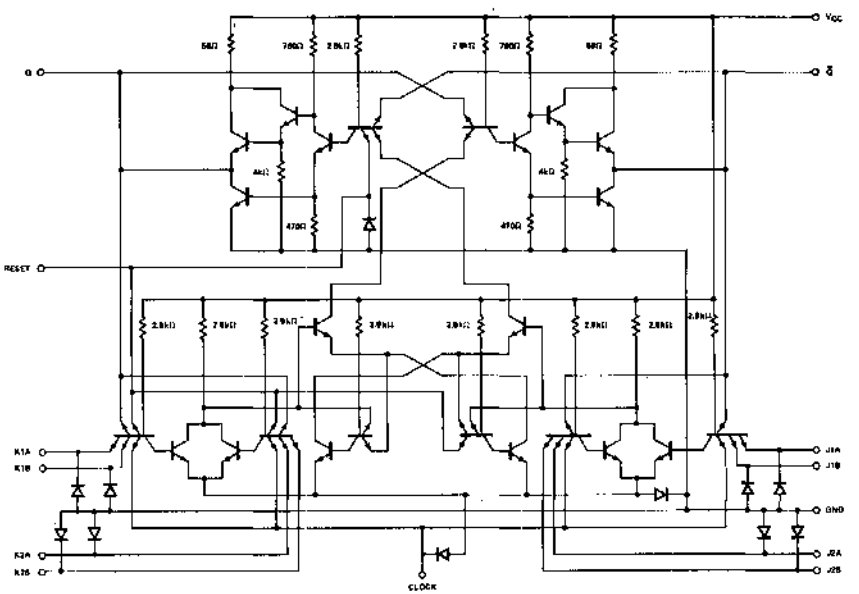
W PACKAGE



A,F PACKAGE



SCHEMATIC



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H71 Circuits	4.5	5	5.5	V
	N74H71 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H71 Circuits	-55	25	125	°C
	N74H71 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Input Setup Time, t_{setup} (See Above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(0)}$	Logical 0 level input current at preset	V_{CC} = MAX,	V_{in} = 0.4V			-6	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V			-4	mA
$I_{in(1)}$	Logical 1 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4V			150	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current **	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			19	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25 pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 25 pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 25 pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25 pF,	R_L = 280Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25 pF,	R_L = 280Ω	10	22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state

TRUTH TABLE

LOGIC

(Each Flip-Flop)

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

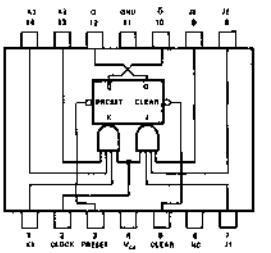
NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse
4. t_{n+1} = bit time after clock pulse.

POSITIVE LOGIC

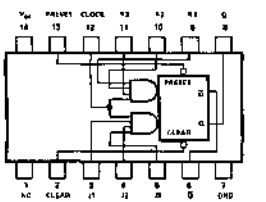
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

PIN CONFIGURATIONS

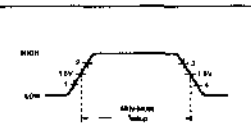
W PACKAGE



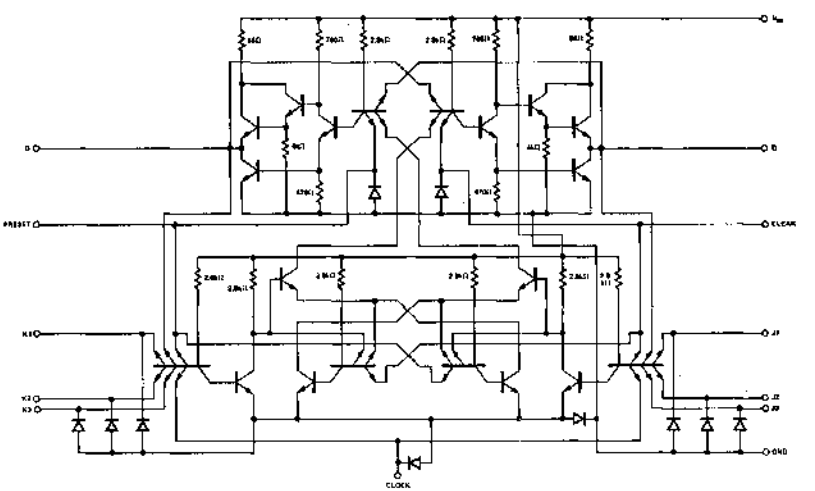
A,F PACKAGE



CLOCK WAVEFORM



SCHEMATIC DIAGRAM



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H72 Circuits	4.5	5	5.5	V
	N74H72 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H72 Circuits	−55	25	125	°C
	N74H72 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	V_{CC} = MAX,	V_{in} = 0.4V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 0.4V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			100 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,			16	25	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

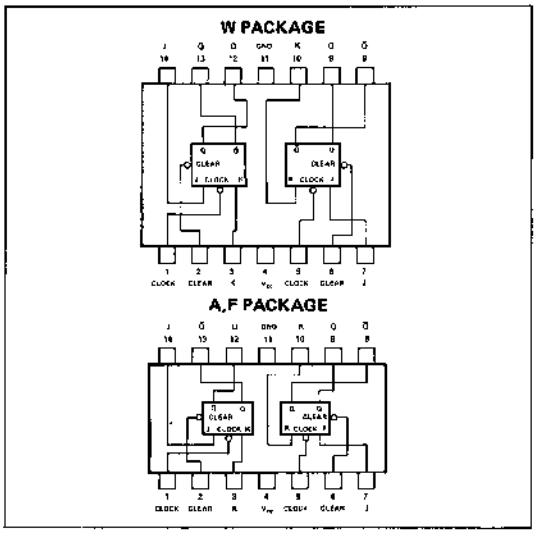
DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

PIN CONFIGURATIONS



TRUTH TABLE

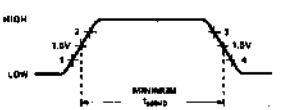
LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:

1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

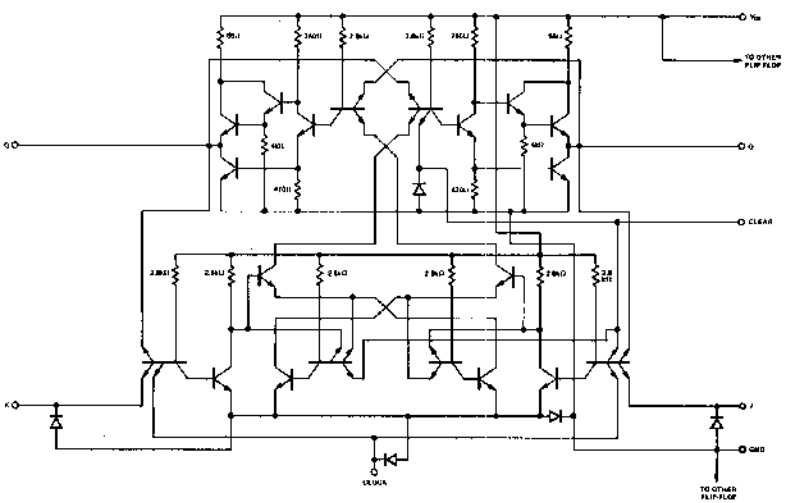
CLOCK WAVEFORM



POSITIVE LOGIC

Low input to clear sets Q to logical 0
Clear is independent of clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H73 Circuits	4.5	5	5.5	V
	N74H73 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H73 Circuits	-55	25	125	°C
	N74H73 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS**		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	V_{CC} = MAX,	V_{in} = 0.4V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear	V_{CC} = MAX,	V_{in} = 0.4V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			32	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

signetics

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

S54H74—A,F,W • N74H74—A,F

DIGITAL 54/74 TTL SERIES

S54H74
N74H74

DESCRIPTION

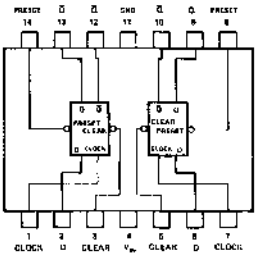
These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

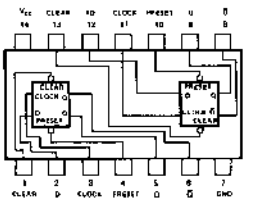
These circuits are fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. A full fan-out to 10 normalized Series 54H/74H loads is available from each of the outputs in the low-level condition. In the high-level state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 35 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

PIN CONFIGURATIONS

W PACKAGE



A, F PACKAGE



TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
L	L	H
H	H	L

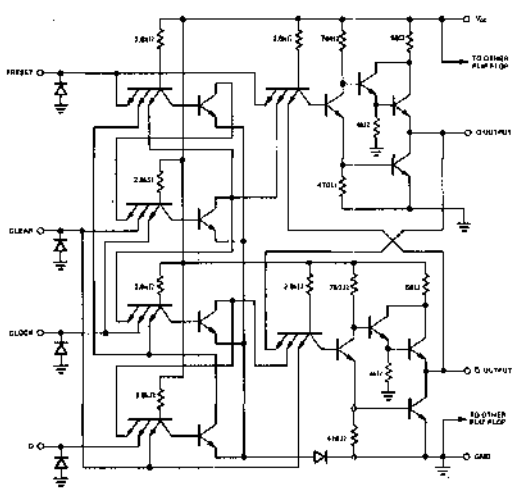
H = High Level, L = Low Level

NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

ASYNCHRONOUS INPUTS

Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	S54H74			N74H74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
Low Logic Level			10			10	
High Logic Level			20			20	
Clock Frequency, f_{clock}	0		35†	0		35	MHz
Width of Clock Pulse, $t_{w(clock)}$	15†			15†			ns
Width of Preset Pulse, $t_{w(preset)}$	25†			25†			ns
Width of Clear Pulse, $t_{w(clear)}$	25†			25†			ns
Input Setup Time, t_{setup} (See Note 3):							
High-level data	10†			10†			ns
Low-level data	15†			15†			ns
Input Hold Time, t_{hold} (See Note 4)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:

3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

† These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = -1mA	2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20mA		0.22	0.4	V
I_{IH}	High-level input current into D	V_{CC} = MAX,	V_I = 2.4V			50	µA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current into preset or clock	V_{CC} = MAX,	V_I = 2.4V			100	µA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current into clear	V_{CC} = MAX,	V_I = 2.4V			150	µA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current into preset or D	V_{CC} = MAX,	V_I = 0.4V			-2	mA
I_{IL}	Low-level input current into clear or clock	V_{CC} = MAX,	V_I = 0.4V			-4	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	S54H74		30	42	mA
			N74H74		30	50	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency			35	43		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs					20	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs	C_L = 25pF,	R_L = 280Ω			30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			4	8.5	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input			7	13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

DESCRIPTION

These dual J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

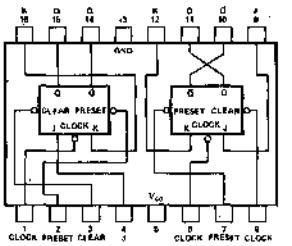
LOGIC

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

PIN CONFIGURATIONS

B PACKAGE

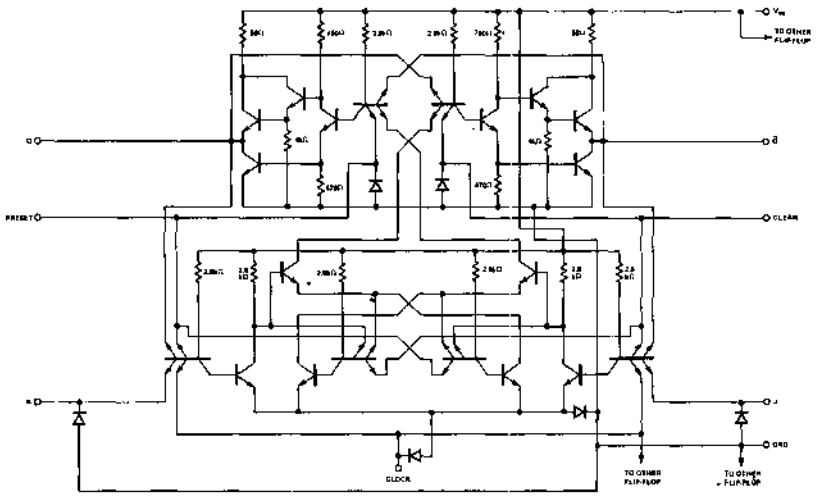


CLOCK WAVEFORM

POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H76 Circuits		4.5	5	5.5	V
N74H76 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H76 Circuits	−55	25	125	°C
	N74H76 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		$\geq t_{p(clock)}$			
Input Setup Time, t_{setup} (See above)					
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	V_{CC} = MAX,	V_{in} = 0.4V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear or preset	V_{CC} = MAX,	V_{in} = 0.4V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J,K, or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear or preset	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			100 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V		32	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

** Not more than one output should be shorted at a time.

DESCRIPTION

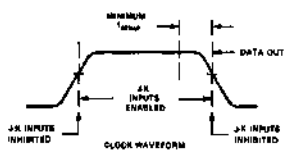
These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

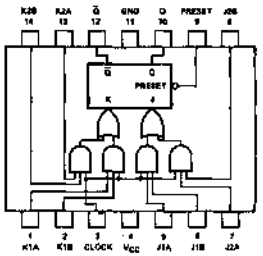
NOTES:
1. J=(J1A•J1B)+(J2A•J2B)
2. K=(K1A•K1B)+(K2A•K2B)
3. t_n=Bit time before clock pulse
4. t_{n+1}=Bit time after clock pulse

CLOCK WAVEFORM

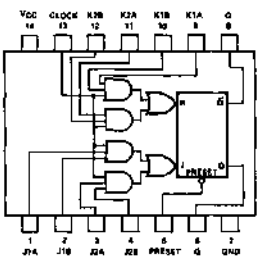


PIN CONFIGURATIONS

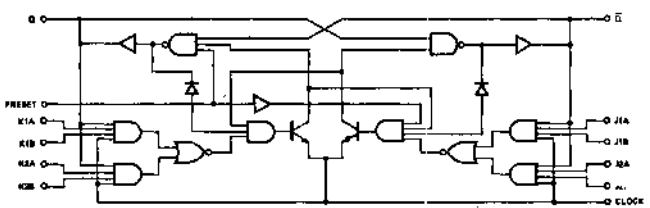
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H101 Circuits	4.5	5	5.5	V
	N74H101 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H101 Circuits	−55	25	125	°C
	N74H101 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Input Setup Time, t_{setup} (See Above):	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, or preset	V_{CC} = MAX,	V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4 V	0		−1	mA
		V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current**	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			20	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25 pF,	R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 25 pF,	R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock low)	C_L = 25 pF,	R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock high)	C_L = 25 pF,	R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

These monolithic J-K flip-flops are negative edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable-will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

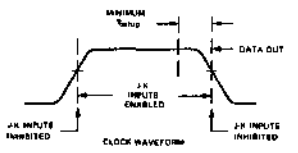
TRUTH TABLE

LOGIC

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

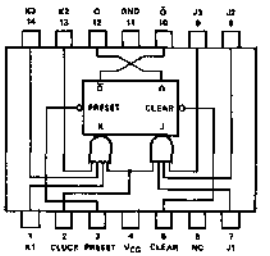
NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC—No Internal Connection.

CLOCK WAVEFORM

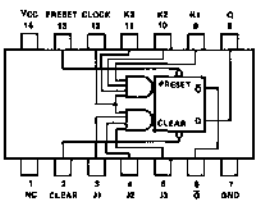


PIN CONFIGURATIONS

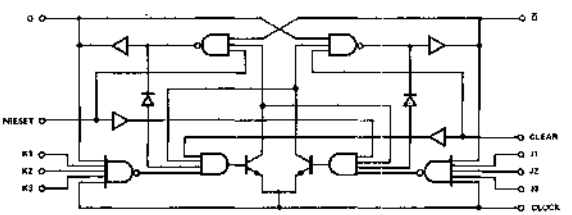
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H102 Circuits	4.5	5	5.5	V
	N74H102 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H102 Circuits	-55	25	125	°C
	N74H102 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		15			ns
Width of Clear Pulse, $t_{p(clear)}$		15			ns
Input Setup Time, t_{setup} (See Above):	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, preset, or clear	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current clock	V_{CC} = MAX,	V_{in} = 0.4V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			20	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

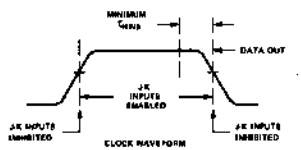
TRUTH TABLE

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES:

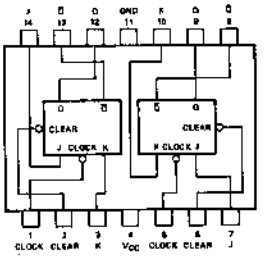
1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM

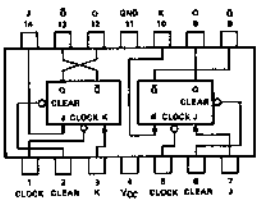


PIN CONFIGURATIONS

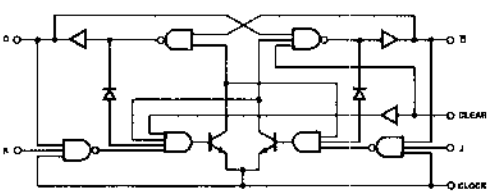
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H103 Circuits		4.5	5	5.5	V
N74H103 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H103 Circuits	-55	25	125	°C
	N74H103 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}: Logical 1		10			ns
Logical 0		13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clear	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current **	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	60		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output, (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

signetics DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H106
N74H106

S54H106–B,F,W • N54H106–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual monolithic J-K flip-flops are negative edge-triggered. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

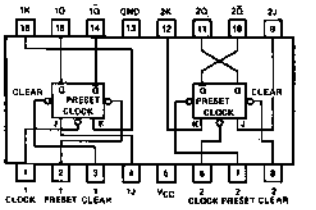
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

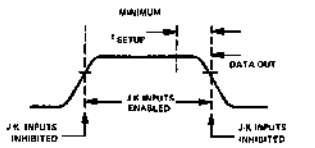
NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

PIN CONFIGURATION

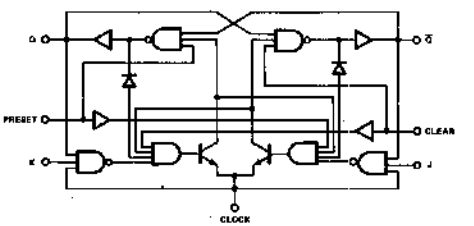
B,F,W PACKAGE



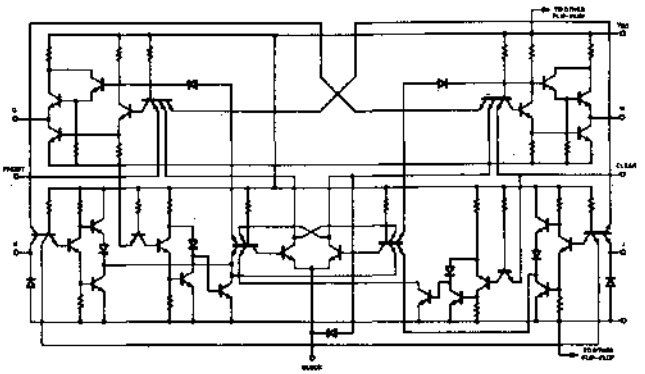
CLOCK WAVEFORM



BLOCK DIAGRAM (each flip-flop)



SCHEMATIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H106 Circuits		4.5	5	5.5	V
N74H106 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H106 Circuits	-55	25	125	°C
	N74H106 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See Above):	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = 500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, preset, or clear	V_{CC} = MAX,	V_{in} = 0.4 V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4 V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
	J or K	V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
	preset or clear	V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at	V_{CC} = MAX,	V_{in} = 2.4 V	0		-1	mA
	clock	V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25 pF,	R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	C_L = 25 pF,	R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	C_L = 25 pF,	R_L = 280 Ω		23	36	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	C_L = 25 pF,	R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	8	16	20	ns

signetics

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H108
N74H108

S54H108–A,F,W • N74H108–A,F

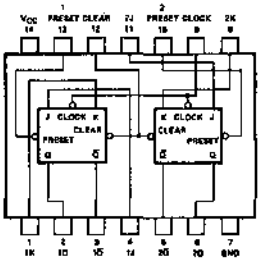
DIGITAL 54/74 TTL SERIES

DESCRIPTION

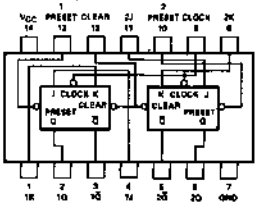
These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data is accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable performs according to the truth table as long as minimum set-up times are observed. Data input is transferred to the outputs on the negative edge of the clock pulse.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



TRUTH TABLE

LOGIC

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H108 Circuits		4.5	5	5.5	V
N74H108 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H108 Circuits	-55	25	125	°C
	N74H108 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		15			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}: Logical 1		10			ns
Logical 0		13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500µA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J,K, or preset	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V		-6	-9.6	mA
$I_{in(0)}$	Logical 0 level input current at clear	V_{CC} = MAX,	V_{in} = 0.4V		-2	-4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4V			100	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			200	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current *,**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DIGITAL 54/74 TTL SERIES

DESCRIPTION

Series 54S/74S Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54S/74S circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54L/74L TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the four speed-power ranges offered (Series 54/74, 54H/74H, 54L/74L, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54S circuits and over the temperature range of 0°C to 70°C for Series 74S circuits.

FEATURES

VERY-HIGH-SPEED, LOW-POWER OPERATION

- 3-ns typical gate propagation delay time
- 19-mW-per-gate power dissipation at 50% duty cycle--speed-power product = 57pJ
- 125-MHz typical J-K flip-flop maximum input clock frequency (d-c coupled)

EASE OF SYSTEM DESIGN

- fully compatible with Series 54/74, 54H/74H, and 54L/74L TTL (including MSI/LSI), and most DTL
- Schottky-diode-clamped inputs simplify system design
- terminated, controlled-impedance lines not normally required
- low output impedance: provides low AC noise susceptability drives highly capacitive loads

IMPROVED CIRCUIT PERFORMANCE

- switching times virtually insensitive to power supply and/or temperature variations
- power dissipation remains relatively low at operating frequencies up to 100 MHz
- high-fan-out: 20 54S/74S loads at the high logic level 10 54S/74S loads at the low logic level
- high DC noise margin—typically 1 volt

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Intermitter Voltage	5.5V
Output Voltage	7V
Operating Free-Air Temperature Range:	
Series 54S Circuits	−55°C to 125°C
Series 74S Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES:

1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

UNUSED INPUTS OF POSITIVE-AND/NAND GATES

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7V and 3.5V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

INPUT-CURRENT REQUIREMENTS

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 2mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 50μA maximum for each emitter. Currents into the input terminals are specified as positive values.

FAN-OUT CAPABILITY

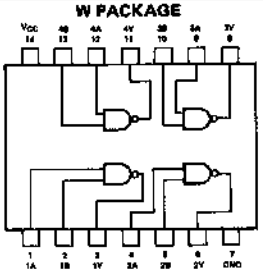
Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54H, 74H, 54S, or 74S loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard output is capable of sinking current from 10 Series 54H, 74H, 54S, or 74S loads (N_L = 10).

RECOMMENDED OPERATING CONDITIONS

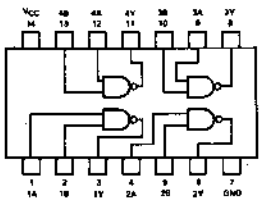
	SERIES 54S CIRCUITS			SERIES 74S CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

PIN CONFIGURATIONS

W PACKAGE

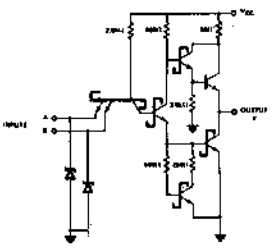


A,F PACKAGE



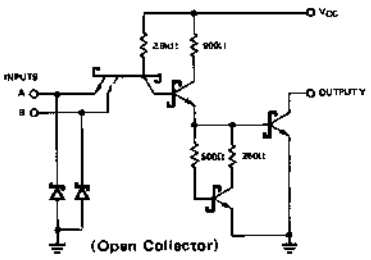
SCHEMATIC (each gate)

S54/N74S00



NOTE:
Component values shown are nominal.

S54/N74S03



RECOMMENDED OPERATING CONDITIONS

	S54S00			N74S00			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
		I_{OH} = −1mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				−2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	NOTE 1	2	3	4.5	ns
		C_L = 50pF,	R_L = 280Ω			4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω		2	3	5	ns
		C_L = 50pF,	R_L = 280Ω			5		

S54/N74S03

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_{IL} = 0.8V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	NOTE 1	2	5	7.5	ns
		C_L = 50pF,	R_L = 280Ω			7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω		2	4.5	7	ns
		C_L = 50pF,	R_L = 280Ω			7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

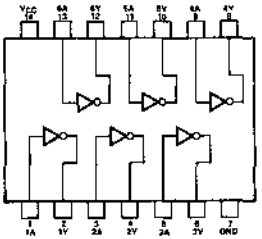
** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

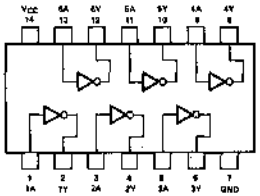
NOTE 1: Load circuit and waveforms are shown on page 2-293

PIN CONFIGURATIONS

W PACKAGE

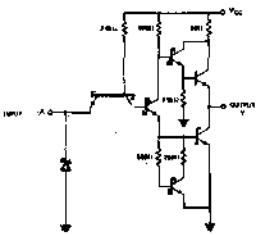


A,F PACKAGE



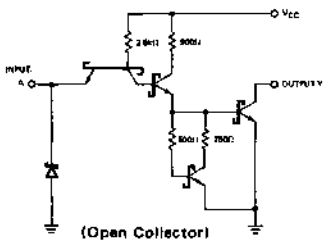
SCHEMATIC (each gate)

S54/N74S04



NOTE: Component values shown are nominal.

S54/N74S05



(Open Collector)

RECOMMENDED OPERATING CONDITIONS

		S54S04			N74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			20	
	Low logic level			10			10	
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
		I_{OH} = -1mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			-40		-100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	NOTE 1	2	3	4.5	ns
		C_L = 50 pF,	R_L = 280 Ω			4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω		2	3	5	ns
		C_L = 50 pF,	R_L = 280 Ω			5*		

S54/N74S05

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_{IL} = 0.8V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω,	NOTE 1	2	5	7.5	ns
		C_L = 50pF,	R_L = 280Ω			7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω		2	4.5	7	ns
		C_L = 50pF,	R_L = 280Ω			7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

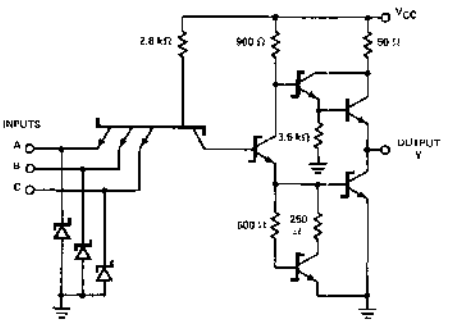
A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, t_1 = t_0 = 2.5ns, PRR = 1 MHz, duty cycle = 50%, and Z_{out} ≈ 50Ω.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

NOTE 1: Load circuit and waveforms are shown on page 2-293

SCHEMATIC DIAGRAM



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		S54S10			S74S10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8 V,	Series 54S	2.5	3.4		V
		I_{OH} = −1 mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V			5	9	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	NOTE 1	2	3	4.5	ns
		C_L = 50 pF, R_L = 280 Ω			4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω		2	3	5	ns
		C_L = 50 pF, R_L = 280 Ω			5		

NOTE 1: Load circuit and waveforms are shown on page 2-293

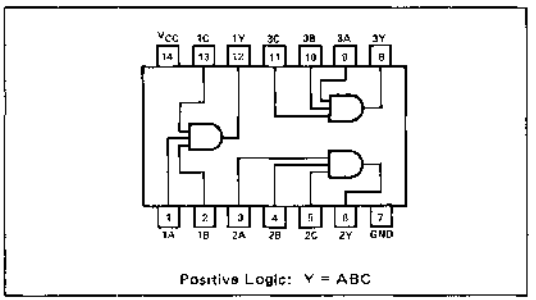
FEATURES

N74S11 ACTIVE PULL-UP

- TYPICAL PROPAGATION TIME — 5 ns at C_L = pF
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE — 32 mW PER GATE

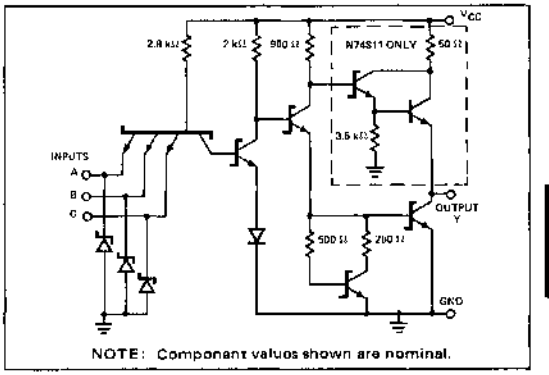
N74S15 OPEN-COLLECTOR

- TYPICAL PROPAGATION TIME — 6 ns at C_L = 15 pF
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE — 29 mW PER GATE



Positive Logic: Y = ABC

SCHEMATIC (each gate)



NOTE: Component values shown are nominal.

RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT

	N74S11	N74S15
Loads at a high logic level	20	
Loads at a low logic level	10	10

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	N74S11			N74S15			UNIT
			MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA	2.7	3.4					V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V						250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX	−40		−100				mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		4.5	8		3.5	6.5	mA
I_{CCL}	Supply current, low-level output (Average per gate)	V_{CC} = MAX, All inputs at 0 V		8	14		8	14	mA

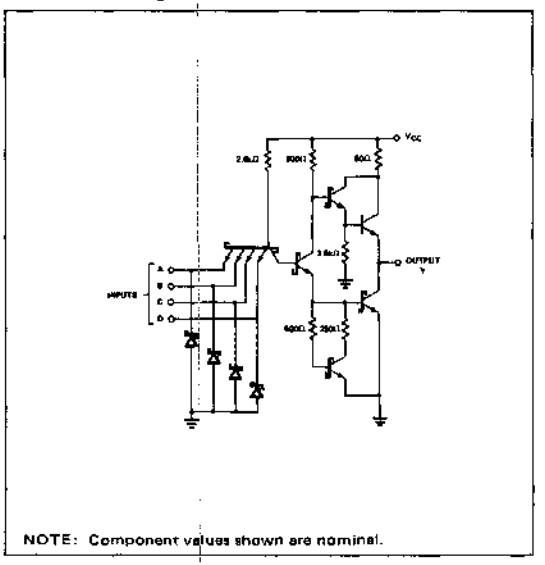
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS NOTE 1	N74S11			N74S15			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5.5	8.5	ns
		C_L = 50 pF, R_L = 280 Ω		6			8.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2.5	5	7.5	2.5	6	9	ns
		C_L = 50 pF, R_L = 280 Ω		7.5			8		

NOTE 1: Load circuits and waveforms are shown on page 2-293

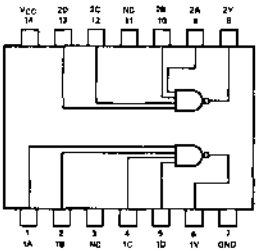
SCHEMATIC (each gate)



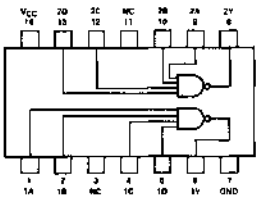
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S54S20			N74S20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
		I_{OH} = -1mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			-40		-100	mA
ICCH	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			2.5	4	mA
ICCL	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	NOTE 1	2	3	4.5	ns
		C_L = 50pF,	R_L = 280Ω			4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω		2	3	5	ns
		C_L = 50pF,	R_L = 280Ω			5		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: Load circuits and waveforms are shown on page 2-293

signetics

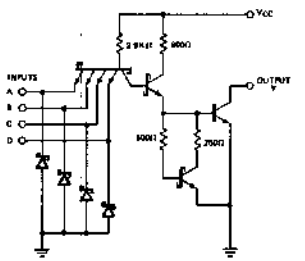
DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN-COLLECTOR OUTPUTS

S54S22 N74S22

S54S22–A,F,W • N74S22–A,F

DIGITAL 54/74 TTL SERIES

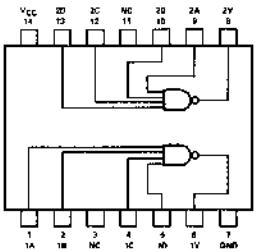
SCHEMATIC (each gate)



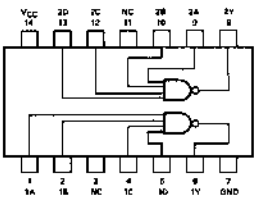
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S54S22			N74S22			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from any Output, N			10			10	
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_{IL} = 0.8V,			250	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V			50	µA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

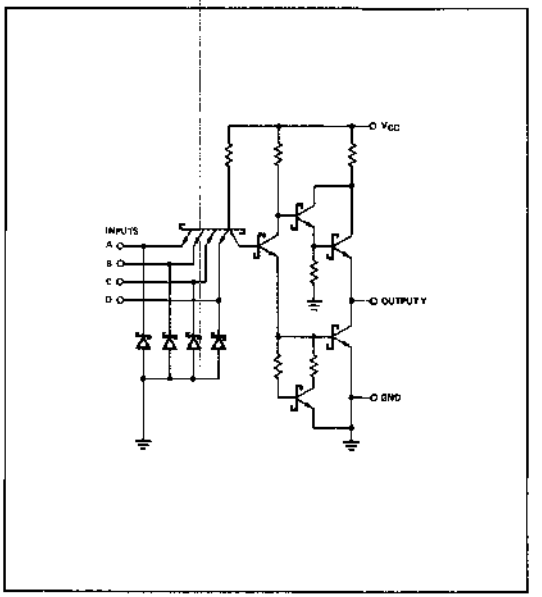
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	NOTE 1	2	5	7.5	ns
		C_L = 50pF,	R_L = 280Ω			7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω		2	4.5	7	ns
		C_L = 50pF,	R_L = 280Ω			7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

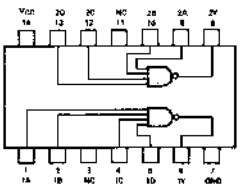
NOTE 1: Load circuit and waveforms are shown on page 2-293

SCHEMATIC (each gate)



PIN CONFIGURATIONS

A,F PACKAGE



NC – No internal connection

RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT

Loads at a high logic level	60
Load at a low logic level	30

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –3mA	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
				Series 74S	2.7	3.4		
		V_{CC} = MIN, R_O = 50Ω To GND	V_I = 0.5V,	S54S140 N74S140	2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 60mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				100	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				–4	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			–50		–225	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			5	9	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			12.5	22	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50pF,	R_L = 93Ω	NOTE 1	2	4	6.5	ns
		C_L = 150pF,	R_L = 93Ω			6		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 50pF,	R_L = 93Ω		2	4	6.5	ns
		C_L = 150pF,	R_L = 93Ω			6		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed 100 milliseconds.

NOTE 1: Load circuit and waveforms are shown on page 2-293

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4-2-3-2-INPUT AND-OR GATES

N74S64
N74S65

DIGITAL 54/74 TTL SERIES

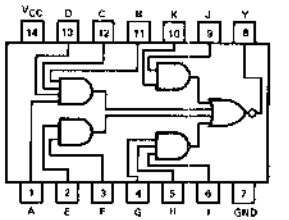
N74S64 ACTIVE PULL-UP

- TYPICAL PROPAGATION TIME — 3.5 ns at C_L = 15 pF
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE — 39 mW

N74S65 OPEN COLLECTOR

- TYPICAL PROPAGATION TIME — 5 ns at C_L = 15 pF
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE — 36 mW

PIN CONFIGURATIONS



Positive Logic: $\overline{ABCD + EF + GHI + JK}$

RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT

	N74S64	N74S65
Loads at a high logic level	20	
Loads at a low logic level	10	10

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	N74S64 MIN	N74S64 TYP**	N74S64 MAX	N74S65 MIN	N74S65 TYP**	N74S65 MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 0.8 V, I_{OH} = −1 mA (N74S64)	2.7	3.4					V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V						250	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V			50			50	µA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current ‡	V_{CC} = MAX	−40		−100				mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, See Note 1		7	12.5		6	11	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 2		8.5	16		8.5	16	mA

**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES: 1. I_{CCH} is measured with all inputs grounded, and the outputs open.

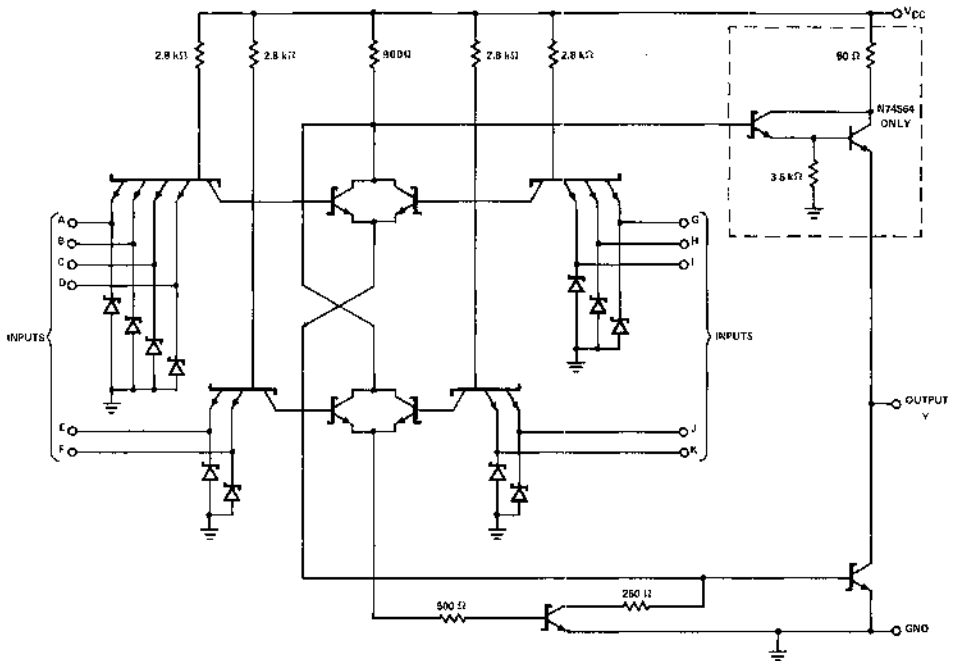
2. I_{CCL} is measured with all inputs of one gate at 5 V, the remaining inputs grounded, and the outputs open.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS NOTE 3	N74S64 MIN	N74S64 TYP	N74S64 MAX	N74S65 MIN	N74S65 TYP	N74S65 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5	7.5	ns
		C_L = 50 pF, R_L = 280 Ω		5			8		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5.5	3.5	ns
		C_L = 50 pF, R_L = 280 Ω		6.5			6.5		

NOTE 3: Load circuit and waveforms are shown on page 2-283

SCHEMATIC



NOTE: Component values shown are nominal.

DESCRIPTION

These monolithic dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very high speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

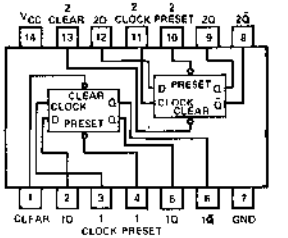
Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10-normalized series 54S/74S loads is available from each of the outputs at low logic level. At a high logic level, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 75 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The N74S74 is characterized for operation from 0°C to 70°C.

Typical Maximum Input Clock Frequency	90 MHz
Typical Power Dissipation	75 mW per Flip-Flop

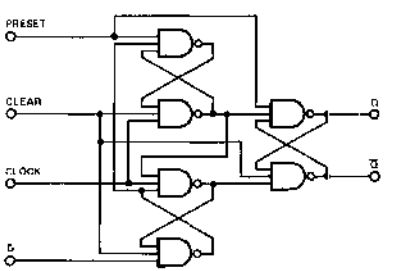
PIN CONFIGURATION



Positive Logic:

Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

FUNCTIONAL BLOCK DIAGRAM (EACH FLIP-FLOP)



TRUTH TABLE (Each Flip-Flop)

t_n	$t_n + 1$	
INPUT	OUTPUT	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = High level, L = Low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Clock frequency, f_{clock}			70		MHz
Width of clock pulse, t_w (clock)			7		ns
Width of preset pulse, t_w (preset)			7		ns
Width of clear pulse, t_w (clear)			7		ns
Input set-up time, t_{setup}	High level data		10		ns
	Low level data		12		
Input hold time, t_{hold}		0			ns
Operating free-air temperature, T_A		0		70	°C

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High level input voltage			2			V
V_{IL}	Low level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High level output voltage	V_{CC} = MIN,	V_{IH} = 2 V	2.7	3.4		V
		V_{IL} = 0.8,	I_{OL} = 20 mA				
V_{OL}	Low level output voltage	V_{CC} = MIN,	V_{IH} = 2 V			0.5	V
		V_{IL} = 0.8,	I_{OL} = 20 mA				
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High level input current	V_{CC} = MAX,	D input			50	μA
		V_I = 2.7 V	Clock or Preset			100	
			Clear			150	
I_{IL}	Low level input current	V_{CC} = MAX,	D input			−2	mA
		V_I = 0.5 V	Clock or Preset			−4	
			Clear			−6	
I_{OS}	Short circuit output current‡	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = MAX,	See Note 1		30		mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω NOTE 1		90		MHz
t_{PLH}	Propagation delay time, low-to-high level output, from clear or preset			5		ns
t_{PHL}	Propagation delay time, high-to-low level output, from clear or preset			8		ns
t_{PLH}	Propagation delay time, low-to-high level output, from clock			7		ns
t_{PHL}	Propagation delay time, high-to-low level output, from clock			7		ns

NOTE 1: Load circuit and test waveforms are shown on page 2-293

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DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54S112
N74S112

S54S112–B,F,W • N74S112–B

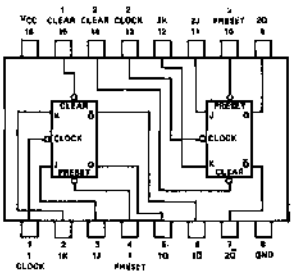
DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup and hold times are observed. Input data are transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

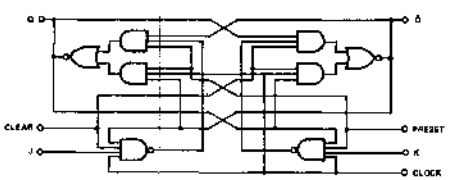
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

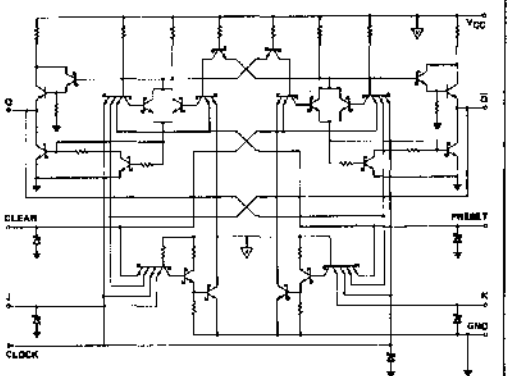
POSITIVE LOGIC

positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Clear and preset are independent of clock.

LOGIC DIAGRAM (each flip-flop)



SCHEMATIC (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

	S54S112			N74S112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		80	0		80	MHz
Width of Clock Pulse, $t_{w(clock)}$	6			6			ns
Width of Preset Pulse, $t_{w(preset)}$	8			8			ns
Width of Clear Pulse, $t_{w(clear)}$	8			8			ns
Input Setup Time, t_{setup} (See Note 1)	3			3			ns
Input Hold Time, t_{hold} (See Note 2)	0			0			ns
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −1mA	S54S112	2.5	3.4		V
				N74S112	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V		J or K input			50	µA
				Clock, preset, or clear			100	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V		J or K input			−1.6	mA
				Clock			−4	
				Preset or clear			−7	
I_{OS}	Short-circuit output current†	V_{CC} = MAX,			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3			30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset	C_L = 15pF, R_L = 280Ω	2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock	NOTE 4	2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

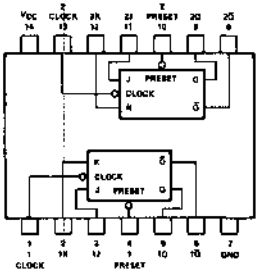
† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.
3. I_{CC} is measured with outputs open, clock grounded, and J-K preset and clear at 4.5V.
4. Load circuit and waveforms are shown on page 2-293

PIN CONFIGURATIONS

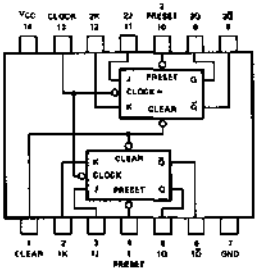
A, F, W PACKAGE



S54S113, N74S113

PIN CONFIGURATIONS

A, F, W PACKAGE



S54S114, N74S114

DESCRIPTION

The S54S113 and N74S113 offer individual J, K, preset, and clock inputs. The S54S114 and N74S114 offer common clock and common clear inputs and individual J, K, and preset inputs.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative-going edge of the clock pulse.

TRUTH TABLE

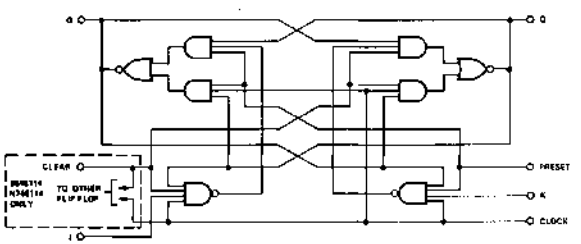
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

LOGIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

	S54S113, S54S114			N74S113, N74S114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		80	0		80	MHz
Width of Clock Pulse, $t_{w(clock)}$	6			6			ns
Width of Preset Pulse, $t_{w(preset)}$	8			8			ns
Width of Clear Pulse, $t_{w(clear)}$ S54S114, N74S114	8			8			ns
Input Setup Time, t_{setup}	3			3			ns
Input Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54S113 N74S113			S54S114 N74S114			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OL} = 20mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	J or K input			50			50	μA
			Clock			100			200	
			Preset			100			100	
			Clear						200	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	J or K input			−1.6			−1.6	mA
			Clock			−4			−8	
			Preset			−7			−7	
			Clear						−14	
I_{OS}	Short circuit output current†	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 1		30	50		30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 280Ω	NOTE 2	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset			2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset			2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock			2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock			2	5	7	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 64 through 69 of the Series 54H/74H section for test circuits.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5V.

2. Load circuit and waveforms are shown on page 2-293

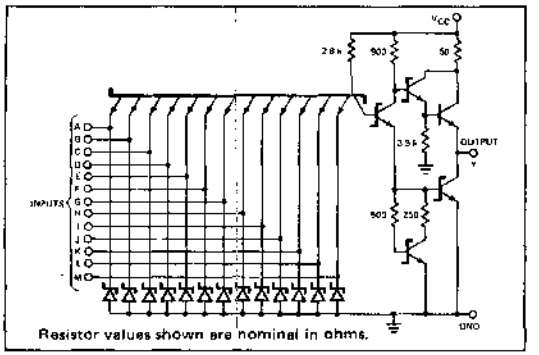
signetics

13-INPUT NAND GATE

S54S133
N74S133

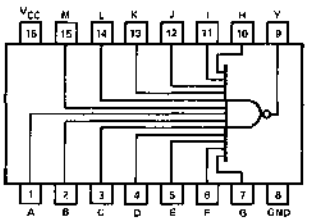
DIGITAL 54/74 TTL SERIES

SCHEMATIC



Resistor values shown are nominal in ohms.

PIN CONFIGURATION



Positive Logic: $Y = \overline{ABCDEFGHIJKLM}$

RECOMMENDED OPERATING CONDITIONS

		S54S133			N74S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −1 mA		S54S133	2.5	3.4		V
				N74S133	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, All inputs at 0 V				3	5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, All inputs at 5 V				5.5	10	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	See Note 1	2	4	6	ns
		C_L = 50 pF, R_L = 280 Ω			5.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω		2	4.5	7	ns
		C_L = 50 pF, R_L = 280 Ω			6.5		

NOTE 1: Load circuit and waveforms are shown on page 2-293

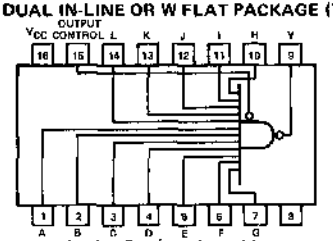
FUNCTION TABLE

INPUTS A B C D E F G H I J K L	OUTPUT CONTROL	OUTPUT Y
H H H H H H H H H H H H	L	L
ANY NUMBER OF INPUTS LOW	L	H
X X X X X X X X X X X X	H	Z

H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance (output off)

PIN CONFIGURATION

J OR N DUAL IN-LINE OR W FLAT PACKAGE (TOP VIEW)



Logic: See function table

RECOMMENDED OPERATING CONDITIONS

		S54S134 MIN	S54S134 NOM	S54S134 MAX	N74S134 MIN	N74S134 NOM	N74S134 MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			40			130	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54S134 MIN	S54S134 TYP**	S54S134 MAX	N74S134 MIN	N74S134 TYP**	N74S134 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −2 mA		2.4	3.4					V
		V_{CC} = Min, V_{IL} = 0.8 V, I_{OH} = −6.5 mA					2.4	3.2		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_O = 2.4 V				50			50	µA
		V_{CC} = MAX, V_O = 0.5 V				−50			−50	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50			50	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current, Output high	V_{CC} = MAX	All inputs at 0 V		7	13		7	13	mA
	Supply current, Output low		Output control at 0 V, Other inputs at 5 V		9	16		9	16	
	Supply current, Output off		All inputs at 5 V		14	25		14	25	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	See Note 1	2	4	6	ns
		C_L = 50 pF,	R_L = 280 Ω			5.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω		2	5	7.5	ns
		C_L = 50 pF,	R_L = 280 Ω			7		
t_{ZH}	Output enable time to high level	C_L = 50 pF,	R_L = 280 Ω			13	19.5	ns
t_{ZL}	Output enable time to low level					14	21	ns
t_{HZ}	Output disable time from high level	C_L = 5 pF				5.5	8.5	ns
t_{LZ}	Output disable time from low level					9	14	ns

NOTE 1: Load circuit and waveforms are shown on page 2-293

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8-INPUT DATA SELECTORS/MULTIPLEXERS

S54S151 S54S251 N74S151 N74S251

DIGITAL 54/74 TTL SERIES

DESCRIPTION

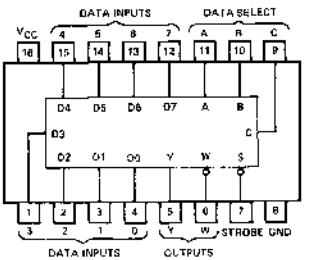
The S54S151, S54S251, N74S151, and N74S251 Schottky-clamped, high-performance, eight-input data selectors/multiplexers are designed for use in very high-speed data routing applications. These multiplexers select one of eight data sources when so directed by the binary address inputs. Both true and complementary data are presented when the strobe input goes low.

The S54S151 and N74S151 are functionally and mechanically interchangeable with the S54151 and N74151 respectively, and in most TTL systems can be utilized to upgrade the performance of existing designs as delay times are typically half that of the S54151 or N74151.

The S54S251 and N74S251 have three-state outputs which permit the outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output can neither drive nor load the bus. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

Typical power dissipation is 225 milliwatts for the S54S151 or N74S151 and 275 milliwatts for the S54S251 and N74S251, or approximately 14 and 17 milliwatts respectively per equivalent gate. The S54S151 and S54S251 are characterized for operation over the full military temperature range of −55°C to 125°C; the N74S151 and N74S251 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATION



Positive Logic: See function table.

FEATURES

- S54S151/N74S151 INTERCHANGEABLE WITH S54151/N74151 IN MOST SYSTEMS
- SCHOTTKY CLAMPED FOR SIGNIFICANT REDUCTION IN DELAY TIMES . . . 4.5 ns TYPICAL, DATA INPUT TO W OUTPUT
- HIGH-SPEED SELECTION FOR ONE OF EIGHT DATA SOURCES
- PERMITS MULTIPLEXING FROM N LINES TO ONE LINE
- S54S251 AND N74S251 HAVE TRI-STATE OUTPUTS
- FULLY COMPATIBLE WITH SERIES 54/74 AND OTHER TTL MSI CIRCUITS

RECOMMENDED OPERATING CONDITIONS

	S54S151			S54S251			N74S151			N74S251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Normalized fan-out from each output, N (at a low logic level)			10			10			10			10	
High-level output current, I_{OH}			−1			−2			−1			−6.5	mA
Operating free-air temperature, T_A	−55		125	−55		125	0		70	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54S151 N74S151			S54S251 N74S251			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	Series 54S	2.5	3.4		2.4	3.2		V
			Series 74S	2.7	3.4		2.4	3.2		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_O = 2.7 V							50	μA
		V_{CC} = MAX, V_O = 0.4 V							−50	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs at 4.5 V, All outputs open			45	70		55	85	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	S54S151, N74S151			S54S251, N74S251			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 280 Ω, See Note 1		12	18		12	18	ns
t_{PHL}					12	18		13	19.5	
t_{PLH}	A, B, or C (3 levels)	W			10	15		10	15	ns
t_{PHL}					9	13.5		9	13.5	
t_{PLH}	Any D	Y			8	12		8	12	ns
t_{PHL}					8	12		8	12	
t_{PLH}	Any D	W			4.5	7		4.5	7	ns
t_{PHL}					4.5	7		4.5	7	
t_{PLH}	Strobe	Y			11	16.5				ns
t_{PHL}					12	18				
t_{PLH}	Strobe	W			9	13				ns
t_{PHL}					8.5	12				
t_{ZH}	Strobe	Y	C_L = 50 pF, R_L = 280 Ω, See Note 1					13	19.5	ns
t_{ZL}								14	21	
t_{ZH}	Strobe	W						13	19.5	ns
t_{ZL}								14	21	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 280 Ω, See Note 1					5.5	8.5	ns
t_{LZ}								9	14	
t_{HZ}	Strobe	W						5.5	8.5	ns
t_{LZ}								9	14	

t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{ZH} = Output enable time to high level
t_{ZL} = Output enable time to low level
t_{HZ} = Output disable time from high level
t_{LZ} = Output disable time from low level
NOTE 1: See load circuits and waveforms on page 2-293

FUNCTION TABLE

INPUTS												OUTPUTS			
SELECT			STROBE	DATA								S54S151,	N74S151	S54S251,	N74S251
C	B	A	S	D0	D1	D2	D3	D4	D5	D6	D7	Y	W	Y	W
X	X	X	H	X	X	X	X	X	X	X	X	L	H	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	L	H	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L	H	L

H = high logic level, L = low logic level, Z = high impedance, X = irrelevant

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DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

S54S153
N74S153

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic Schottky-barrier-diode-clamped TTL circuits are high-performance multiplexers which are significantly faster than the S54153/N74153. As an example, the two-gate-level delay from the data inputs to the output is only 8.5 nanoseconds maximum compared to 18 or 23 nanoseconds maximum for the standard-speed part. Overall, the guaranteed delay times for the S54S153/N74S153 represent approximately a 100% improvement over standard TTL with only a 12% increase in maximum d-c power consumption. In many cases, the S54S153 or N74S153 can plug into existing systems designed for S54153 or N74153.

These data selectors/multiplexers are fully compatible for use with most standard, high-speed, and low-power TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54S/74S load, and full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normalized Series 54S/74S loads is provided at high logic levels to facilitate connection of unused inputs to used inputs. Typical power dissipation is 225 milliwatts.

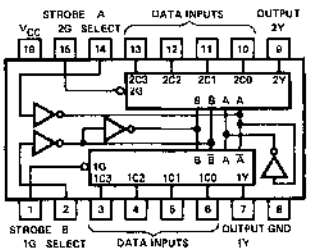
The S54S153 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S153 is characterized for operation from 0°C to 70°C.

FEATURES

- FULL SCHOTTKY-BARRIER-DIODE CLAMPING FOR VERY HIGH SPEEDS
- PERMITS MULTIPLEXING FROM N LINES TO 1 LINE
- SAME PIN ASSIGNMENTS AS S54153 AND N74153
- STROBE (ENABLE) LINE PROVIDED FOR CASCADING (N LINES TO n LINES)
- TYPICAL AVERAGE PROPAGATION DELAY TIMES:
  - DATA INPUT TO OUTPUT (2 GATE LEVELS) 6 ns
  - STROBE INPUT TO OUPUT (3 GATE LEVELS) 9.5 ns
  - SELECT INPUT TO OUTPUT (4 GATE LEVELS) 12 ns
- HIGH FAN-OUT LOW-IMPEDANCE TOTEM-POLE OUTPUTS
- FULLY COMPATIBLE WITH MOST TTL AND DTL CIRCUITS

PIN CONFIGURATION

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



LOGIC: SEE FUNCTION TABLE

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = High level, L = Low level, X = Irrelevant

RECOMMENDED OPERATING CONDITIONS

		S54S153			N74S153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IH} = 2 V,	Series 54S	2.5	3.4		V
		V_{IL} = 0.8 V,	I_{OH} = −1 mA	Series 74S	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2 V,				0.5	V
		V_{IL} = 0.8 V,	I_{OL} = 20 mA					
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CCL}	Supply current, low level output	V_{CC} = MAX,	See Note 1			45	70	mA

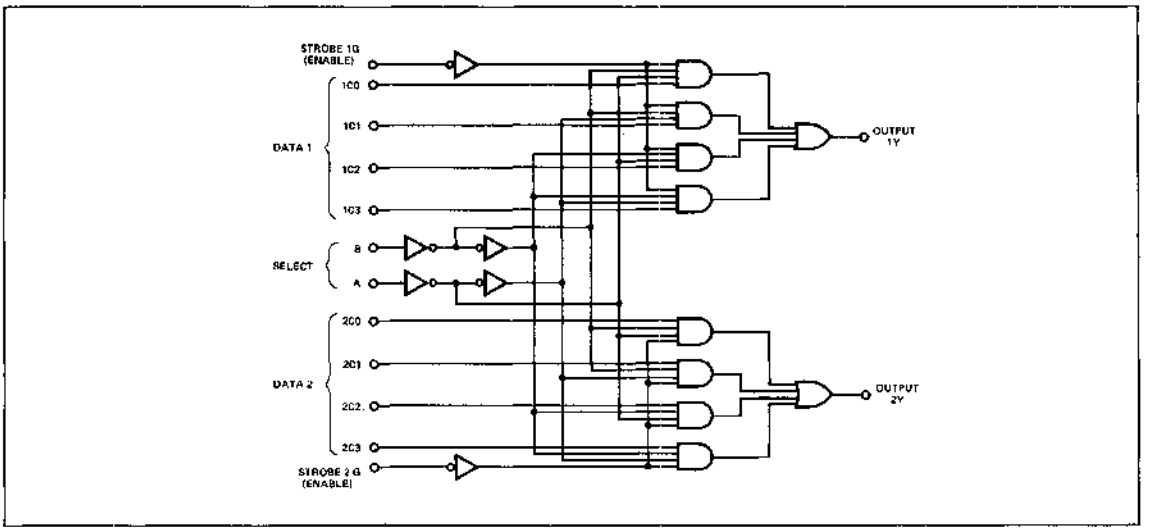
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.
NOTE: 1: I_{CCL} is measured with the outputs open and all inputs grounded.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 280 Ω, See Note 2		6	9	ns
t_{PHL}	Data	Y			6	9	ns
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}	Select	Y			12	18	ns
t_{PLH}	Strobe	Y			10	15	ns
t_{PHL}	Strobe	Y			9	13.5	ns

t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and test waveforms are shown on page 2-293

FUNCTIONAL BLOCK DIAGRAM



TEST TABLE FOR NOTE 2

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = Irrelevant A=IN-PHASE OUTPUT
B=OUT-OF-PHASE

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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

S54S157
S54S158
N74S157
N74S158

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The Schottky-clamped S54S157, S54S158, N74S157, and N74S158 are ultra-high-speed data selectors/multiplexers which can be employed in high-performance designs. These circuits select a 4-bit word from one of two sources and route it to the four outputs. The S54S157/N74S157 present true data whereas the S54S158/N74S158 present inverted data to minimize propagation delay time.

The S54S157/N74S157 can be used to replace the S54157/N74157 in existing designs to upgrade performance substantially.

The S54S157 and S54S158 are characterized for operation over the full military temperature range of −55°C to 125°C. The N74S157 and N74S158 are characterized for operation from 0°C to 70°C.

FEATURES

- **SCHOTTKY-CLAMPING REDUCES DELAY TIME TO 4 ns TYPICAL (S54S158, N74S158 DATA-TO-OUTPUT)**
- **S54S157, N74S157 CAN UPGRADE EXISTING SYSTEM PERFORMANCE AS THEY ARE PIN-FOR-PIN REPLACEMENTS FOR S54157, N74157**
- **S54S157, S54S158 OPERATE THROUGHOUT −55°C TO 125°C FREE-AIR TEMPERATURE RANGE**
- **FULLY COMPATIBLE WITH MOST TTL AND TTL MSI CIRCUITS**

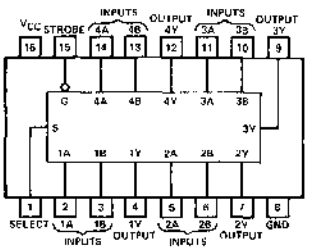
FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	S54S157 N74S157	S54S158 N74S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

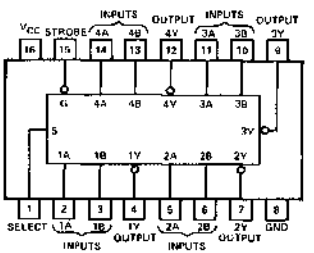
PIN CONFIGURATION

S54S157, N74S157



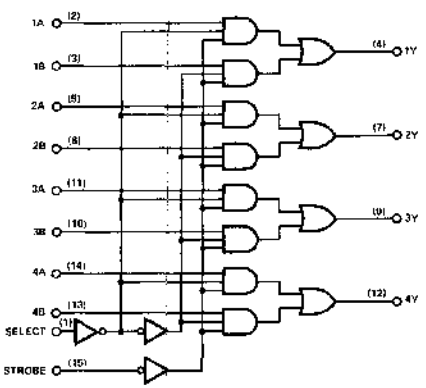
POSITIVE LOGIC:
Low logic level at S selects A inputs.
High logic level at S selects B inputs.

S54S158, N74S158

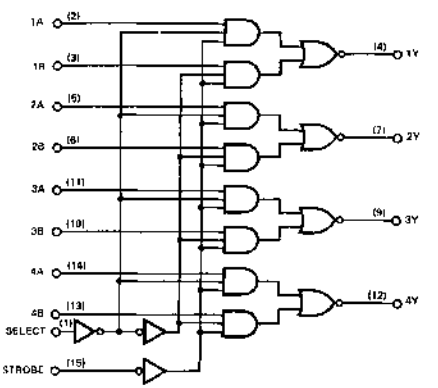


POSITIVE LOGIC:
Low logic level at S selects A inputs.
High logic level at S selects B inputs.

S54S157, N74S157



S54S158, N74S158



RECOMMENDED OPERATING CONDITIONS

		S54S157, S54S158			N74S157, N74S158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54S157 N74S157 MIN	TYP**	MAX	S54S158 N74S158 MIN	TYP**	MAX	UNIT
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.8			0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH} High-level input current	S or G input	V_{CC} = MAX, V_I = 2.7 V				100			100	µA
	A or B input					50			50	
I_{IL} Low-level input current	S or G input	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
	A or B input					−2			−2	
I_{OS} Short-circuit output current‡		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 1			50	78		39	61	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTE 1: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

SWITCHING CHARACTERISTICS , V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TEST CONDITIONS	S54S157, N74S157 MIN	TYP	MAX	S54S158, N74S158 MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 280 Ω, See Note 2		5	7.5		4	6	ns
t_{PHL}				4.5	6.5		4	6	
t_{PLH}	Strobe			8.5	12.5		6.5		ns
t_{PHL}				7.5	12		7		
t_{PLH}	Select			9.5	15		8	12	ns
t_{PHL}				9.5	15		8	12	

t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
NOTE 2: Load circuits and waveforms are shown on page 2-293

signetics

HEX QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

DIGITAL 54/74 TTL SERIES

S54S174
S54S175
N74S174
N74S175

DESCRIPTION

These high-performance monolithic, positive-edge-triggered flip-flops utilize Schottky TTL technology to implement D-type flip-flop logic. All have a direct clear input, and the S54S175 and N74S175 feature complementary outputs from each flip-flop. Pin assignments for these Schottky flip-flops are identical to the standard TTL versions meaning that these Schottky versions can be utilized to upgrade existing system performance in most cases.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FEATURES

- FULL SCHOTTKY CLAMPING TO ACHIEVE TYPICAL MAXIMUM TOGGLE RATES OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 COUNTERPARTS AND CAN BE USED TO UPGRADE EXISTING SYSTEMS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH OTHER TTL CIRCUITS
- S54S174 AND S54S175 OPERATE OVER FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- FOR USE IN HIGH-PERFORMANCE:
  - BUFFER/STORAGE REGISTERS
  - SHIFT REGISTERS
  - COUNTERS
  - PATTERN GENERATORS

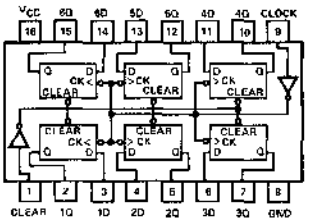
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established
† = S54S175 and N74S175 only

PIN CONFIGURATION

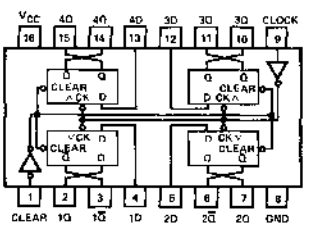
S54S174, N74S174



Positive Logic: See function table

PIN CONFIGURATION

S54S175, N74S175



Positive Logic: See function table

RECOMMENDED OPERATING CONDITIONS

		S54S174, S54S175			N74S174, N74S175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		75	0		75	MHz
Width of clock or clear pulse, t_w		12			12			ns
Setup time, t_{setup}	Data input	8			8			ns
	Clear inactive-state	15			15			
Data hold time, t_{hold}		2			2			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S		2.5	3.4		V
			Series 74S		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1	S54S174, N74S174			90		mA
			S54S175, N74S175			60		

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 1: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

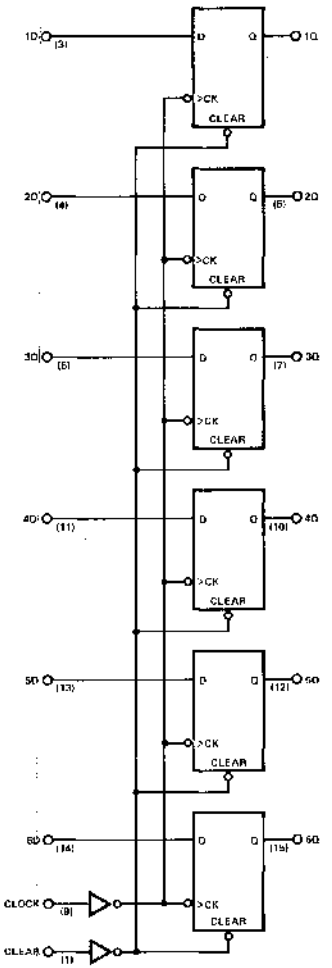
SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		MHz
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output from clear (S54S175,N74S175 only)			13		ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			13		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			9		ns
t_{PHL}	Propagation time, high-to-low-level output from clock			11		ns

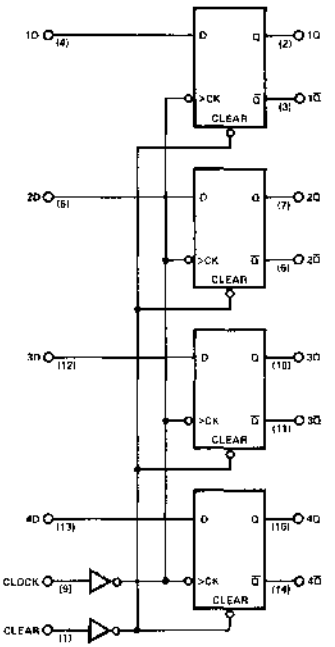
NOTE 2: See load circuit and waveforms shown on page 2-293

FUNCTIONAL BLOCK DIAGRAMS

S54S174, N74S174



S54S175, N74S175



Dynamic input activated by a transition from a high level to a low level.

DESCRIPTION

These Schottky-clamped high-speed arithmetic/logic units, functionally identical to the S54181 and N74181, perform 16 binary arithmetic operations on two 4-bit words with a full look-ahead carry scheme as propagate and generate terms are available at the P and G outputs. Typical performance is 19 nanoseconds add time for a 16-bit word when used with the S54S182 or N74S182 carry look-ahead.

Typical addition times are shown in Table III. The S54S181/N74S181 can replace the S54181/N74181 in most existing systems for significant performance upgrading as they are functionally and mechanically interchangeable.

The S54S181 and N74S181 will also perform the 16 possible functions on two Boolean variables without the use of external circuitry. The carry circuit is inhibited for logic functions.

The S54S181 and N74S181 will accommodate active-high or active-low data if the pin designations are interpreted as shown below:

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1 which requires an end-around or forced carry to provide A—B.

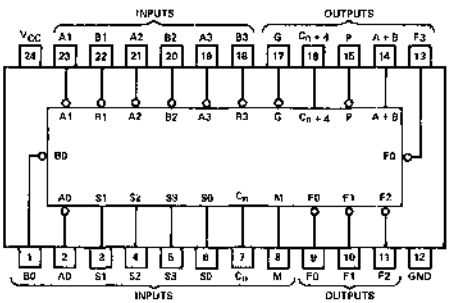
Mode of operation (arithmetic or logic) is controlled by the mode-control (M) input. Complete functions for active-high and active-low data are shown in Tables I and II.

Typical average power dissipation is 600 milliwatts, or approximately 8 milliwatts per equivalent gate. The S54S181 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S181 is characterized for operation from 0°C to 70°C.

For additional descriptive information and typical connection schemes, see the S54181/N74181 data sheet

PIN CONFIGURATION

J OR N DUAL IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



Logic: See function tables

FEATURES

- SIGNIFICANT IMPROVEMENT IN ADD TIMES OVER S54181/N74181
- TYPICAL ADD TIME FOR 16 BITS OF 19 ns USING S54S182, N74S182 LOOK-AHEAD
- S54S181 IS GUARANTEED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- FULLY COMPATIBLE WITH MOST TTL FUNCTIONS INCLUDING MSI

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table II)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

TABLE I

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L: ARITHMETIC OPERATIONS	
				LOGIC	C_n = 0 = H	C_n = 1 = L
S_3	S_2	S_1	S_0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) plus 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
L	L	H	H	F = 0	F = minus 1 (2's complement)	F = zero
L	H	L	L	$F = \overline{AB}$	$F = A$ plus $A\overline{B}$	$F = A$ plus $A\overline{B}$ plus 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ plus $A\overline{B}$	$F = (A + B)$ plus $A\overline{B}$ plus 1
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1	F = A minus B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ minus 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A plus AB	F = A plus AB plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	$F = (A + \overline{B})$ plus AB	$F = (A + \overline{B})$ plus AB plus 1
H	L	H	H	F = AB	F = AB minus 1	F = AB
H	H	L	L	F = 1	F = A plus A*	F = A plus A plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) plus A	F = (A + B) plus A plus 1
H	H	H	L	$F = A + B$	$F = (A + \overline{B})$ plus A	$F = (A + \overline{B})$ plus A plus 1
H	H	H	H	F = A	F = A minus 1	F = A

*Each bit is shifted to the next more significant position.

TABLE II

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L: ARITHMETIC OPERATIONS	
				LOGIC	C_n = 0 = L	C_n = 1 = H
S_3	S_2	S_1	S_0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	$F = \overline{A}$	F = A minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ minus 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = minus 1 (2's complement)	F = zero
L	H	L	L	$F = \overline{A + B}$	$F = A$ plus $(A + \overline{B})$	$F = A$ plus $(A + \overline{B})$ plus 1
L	H	L	H	$F = \overline{B}$	$F = AB$ plus $(A + \overline{B})$	$F = AB$ plus $(A + \overline{B})$ plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A minus B minus 1	F = A minus B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
H	L	L	L	$F = \overline{A}B$	F = A plus (A + B)	F = A plus (A + B) plus 1
H	L	L	H	$F = A \oplus B$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	$F = A\overline{B}$ plus (A + B)	$F = A\overline{B}$ plus (A + B) plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) plus 1
H	H	L	L	F = 0	F = A plus A*	F = A plus A plus 1
H	H	L	H	$F = A\overline{B}$	F = AB plus A	F = AB plus A plus 1
H	H	H	L	F = AB	$F = A\overline{B}$ plus A	$F = A\overline{B}$ plus A plus 1
H	H	H	H	F = A	F = A	F = A plus 1

*Each bit is shifted to the next more significant position.

RECOMMENDED OPERATING CONDITIONS

		S54S181			N74S181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	N54S181	2.5	3.4		V
				S74S181	2.7	3.4		
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	mode input	V_{CC} = MAX, V_I = 2.4 V				50	μA
		any A or B input					150	
		any S input					200	
		carry input					250	
I_{IL}	Low-level input current	mode input	V_{CC} = MAX, V_I = 0.4 V				−2	mA
		any A or B input					−6	
		any S input					−8	
		carry input					−10	
I_{OS}	Short-circuit output current, any output except A = B		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, T_A = 125°C See Note 1	N54S181 N pkg only			135	mA
			V_{CC} = MAX, See Note 1	N54S181		120	160	
				S74S181		120	220	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time.

NOTE 1: I_{CC} is measured for the following conditions:

a. S_0 through S_3, M, and A inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.

b. S_0 through S_3 and M are at 4.5 V, all other inputs are grounded, and all outputs are open.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10 $(C_L$ = 15 pF, R_L = 280 Ω see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			7	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		12.5	18.5	ns
t_{PHL}					12.5	18.5	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		15.5	23	ns
t_{PHL}					15.5	23	
t_{PLH}	C_n	Any F	M = 0 V (SUM or DIFF mode)		7	12	ns
t_{PHL}					7	12	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM Mode)		8	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		7.5	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	Any A or B	Any F	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		11	16.5	ns
t_{PHL}					11	16.5	
t_{PLH}	Any A or B	Any F	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any A or B	Any F	M = 4.5 V (logic mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		15	23	ns
t_{PHL}					20	30	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and waveforms are shown on p. 2-293.

Typical addition times for various configurations are given in the table below. Subtraction times are typically 3 nanoseconds longer than sum mode times. For typical look-ahead configurations, see the 54S181/N74S181 data sheet in this catalog.

TABLE III
TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES USING S54S181 AND S54S182	ADDITION TIMES USING S54S181 AND S54S182	ADDITION TIMES USING S54181 AND S54182	PACKAGE COUNT ARITHMETIC/ LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	11 ns	11 ns	24 ns	1		NONE
5 to 8	18 ns	18 ns	36 ns	2		RIPPLE
9 to 16	19 ns	24 ns	36 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	26 ns	45 ns	60 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

signetics

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

S54S194
N74S194

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These high-performance bidirectional shift registers are functionally and mechanically identical to the N54194 and S74194, however, with a typical shift frequency of 110 megahertz the Schottky-clamped versions can be used in very high-speed systems, or can be substituted for the N54194/S74194 to upgrade the performance of most existing systems. The universal shift register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Hold (recirculate) data	L	L

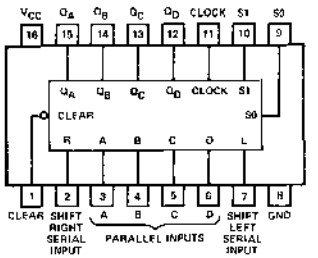
In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Data is recirculated when both mode control inputs are low. For added flexibility the mode controls can be changed independently of the clock.

These four-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54S/74S load, and input clamping diodes minimize switching transients to simplify system design. With the equivalent of 46 gates on the monolithic chip, typical power dissipation is less than 10 milliwatts per equivalent gate.

The N54S194 is characterized for operation over the full military temperature range of −55°C to 125°C; the S74S194 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

J OR N DUAL IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



Positive Logic: See description

FEATURES

- SCHOTTKY-CLAMPED TO ACHIEVE TYPICAL MAXIMUM SHIFT FREQUENCY OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO N54194, S74194 AND CAN BE USED TO UPGRADE EXISTING SYSTEMS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH MOST OTHER TTL AND DTL CIRCUITS
- N54S194 OPERATES OVER FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- FOR USE IN HIGH-PERFORMANCE:
  ACCUMULATORS/PROCESSORS,
  SERIAL-TO-PARALLEL AND
  PARALLEL-TO-SERIAL CONVERTERS

RECOMMENDED OPERATING CONDITIONS

		N54S194,			S74S194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		75	0		75	MHz
Width of clock or clear pulse, t_w		12			12			ns
Setup time, t_{setup} (NOTE 2)	Mode control	12			12			ns
	Serial and parallel data	10			10			
	Clear inactive-state	15			15			
Hold time at any input, t_{hold}		2			2			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		N54S194	2.5	3.4		V
				S74S194	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1		N54S194		90		mA
				S74S194		90		

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

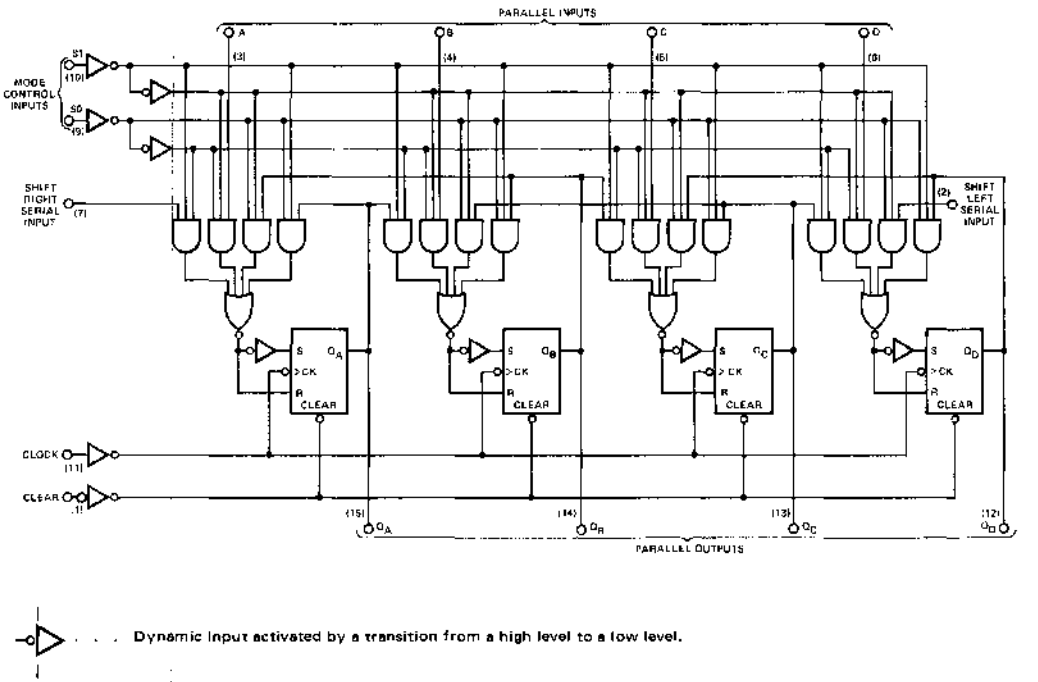
NOTE 1: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5 V, applied to clock.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			11		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		4	9		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		4	10		ns

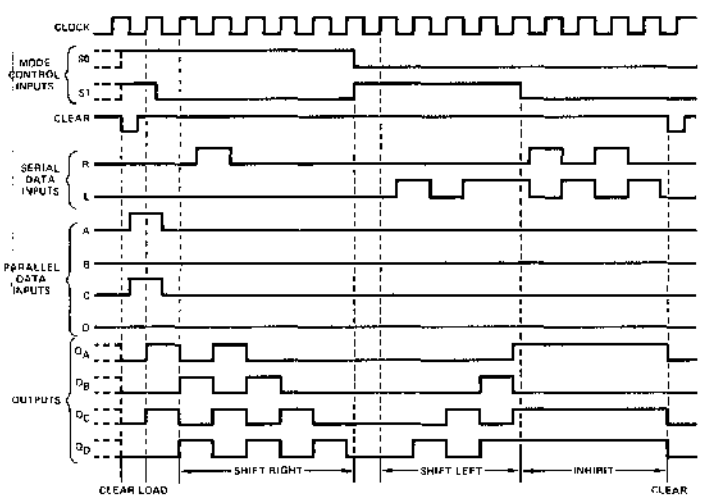
NOTE 2: Waveforms and load circuits on page 2-293 with the following additions: $t_{w\ (clock)} \geq 12$ns, $t_{w\ (clear)} \geq 12$ns.

FUNCTIONAL BLOCK DIAGRAM



. . . . Dynamic input activated by a transition from a high level to a low level.

TYPICAL CLEAR, LOAD, RIGH-SHIFT, INHIBIT, AND CLEAR SEQUENCES



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4-BIT PARALLEL-ACCESS SHIFT REGISTERS

S54S195
N74S195

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These high-performance 4-bit registers feature a 110-megahertz typical maximum shift-frequency which makes them particularly attractive for very high-speed data processing systems. As the pin assignments are the same as the S54195 and N74195, existing systems can in most cases be upgraded merely by utilizing the Schottky-clamped versions. The registers have two modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_D)

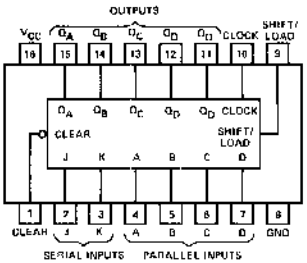
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

These shift registers are fully compatible with other TTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54S/74S load, including the clock input. The S54S195 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S195 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

J OR N DUAL-IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



Positive Logic: See function table

FEATURES

- SCHOTTKY-CLAMPED TO ACHIEVE TYPICAL MAXIMUM SHIFT FREQUENCY OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO N54195, S74195 AND CAN BE USED TO UPGRADE EXISTING DESIGNS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH OTHER TTL CIRCUITS
- N54S195 OPERATES OVER FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- USE IN HIGH-PERFORMANCE:
  ACCUMULATORS/PROCESSORS
  SERIAL-TO-PARALLEL,
  PARALLEL-TO-SERIAL CONVERTERS

FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	A	B	C	D	A	B	C	D	$\overline{D}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{B0}	Q_{C0}	$\overline{Q}_{C0}$
H	H	↑	L	L	X	X	X	X	L	Q_{A0}	Q_{B0}	Q_{C0}	$\overline{Q}_{C0}$
H	H	↑	H	H	X	X	X	X	H	Q_{A0}	Q_{B0}	Q_{C0}	$\overline{Q}_{C0}$
H	H	↑	H	L	X	X	X	X	Q_{A0}	Q_{A0}	Q_{B0}	Q_{B0}	$\overline{Q}_{C0}$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level
A, B, C, D, = The level of steady state input at A, B, C, or D respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D respectively before the indicated steady state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

		S54S195			N74S195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		75	0		75	MHz
Width of clock input pulse, $t_{w(clock)}$		12			12			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup}	Shift/load	12			12			ns
	Serial and parallel data	10			10			
	Clear inactive-state	15			15			
Shift/load release time, $t_{release}$				7			7	ns
Serial and parallel data hold time, t_{hold}		2			2			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		S54S195	2.5	3.4		V
				N74S195	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1		S54S195		75	99	mA
				N74S195		75	109	

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			11		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			9		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			10		ns

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

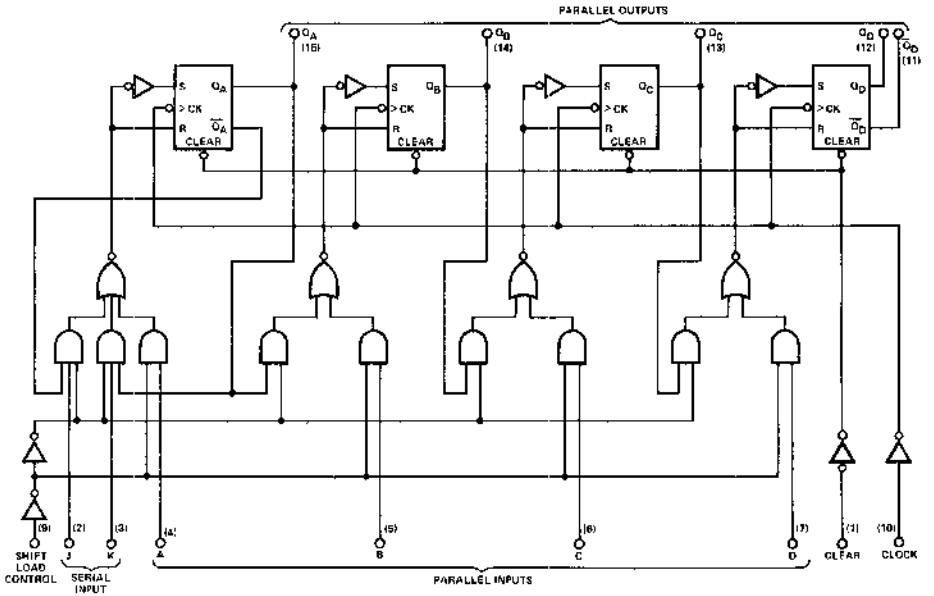
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

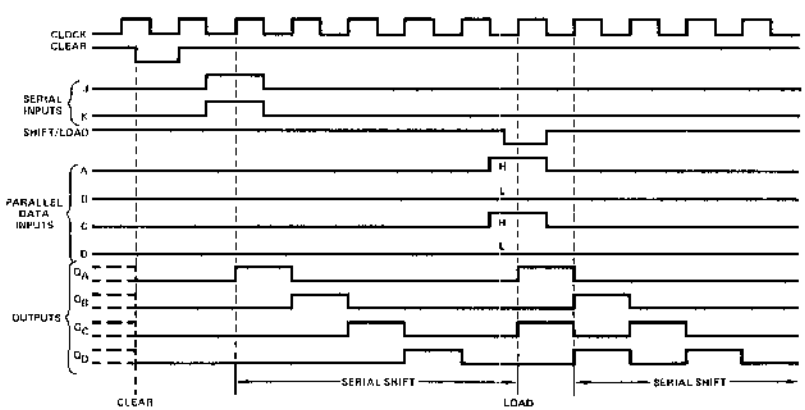
NOTES: 1. With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

2. Load circuit and waveforms are shown on page 2-293 with the following additions: $t_{w(clock)} \geq 12$ns, $t_{w(clear)} \geq 12$ns.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



signetics

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

DIGITAL 54/74 TTL SERIES

S54S257
S54S258
N74S257
N74S258

DESCRIPTION

These Schottky-clamped high-performance multiplexers feature three-state outputs which can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

The typical propagation delay times from data input to output average only 4.8 nanoseconds for the S54S257, N74S157 and only 4 nanoseconds for the S54S258, N74S258. Also, to minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

FEATURES

- **TRI-STATE OUTPUTS INTERFACE DIRECTLY WITH SYSTEM BUS**
- **SCHOTTKY-CLAMPED FOR SIGNIFICANT IMPROVEMENT IN A-C PERFORMANCE**
- **FULLY COMPATIBLE WITH MOST TTL FUNCTIONS INCLUDING MSI**
- **SAME PIN ASSIGNMENTS AS S54S157, N74S157 AND S54S158, N74S158**
- **PROVIDES BUS INTERFACE FROM MULTIPLE SOURCES IN HIGH-PERFORMANCE SYSTEMS**
- **N54S257 AND N54S258 ARE GUARANTEED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C**

FUNCTION TABLE

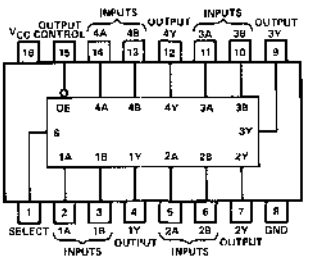
INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	N54S257 S74S257	N54S258 S74S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level, L = Low level, X = Irrelevant, Z = High impedance (off)

PIN CONFIGURATION

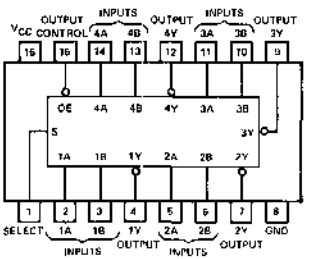
J OR N DUAL IN-LINE OR W FLAT PACKAGE
(TOP VIEW)

S54S257, N74S257



Positive Logic: See function table

S54S258, N74S258



Positive Logic: See function table

RECOMMENDED OPERATING CONDITIONS

		S54S257, S54S258			N74S257, N74S258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			40			130	
	Low logic level			10			10	
High-level output current, I_{OH}				2			6.5	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS*	S54S257, S54S258			N74S257, N74S258			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, Series 54S	2.5	3.4		2.5	3.4		V
			V_{IL} = 0.8 V, I_{OH} = MAX, Series 74S	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
$I_{O(off)}$	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 2.4 V			50			50	μA
			V_{CC} = MAX, V_O = 0.4 V			−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	S input	V_{CC} = MAX, V_I = 2.7 V			100			100	μA
		Any other				50			50	
I_{IL}	Low-level input current	S input	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
		Any other				−2			−2	
I_{OS}	Short circuit output current‡		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	All outputs high	V_{CC} = MAX, See Note 1		44	68		36	56	mA
		All outputs low			60	93		52	81	
		All outputs off			64	99		56	87	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
NOTE 1: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

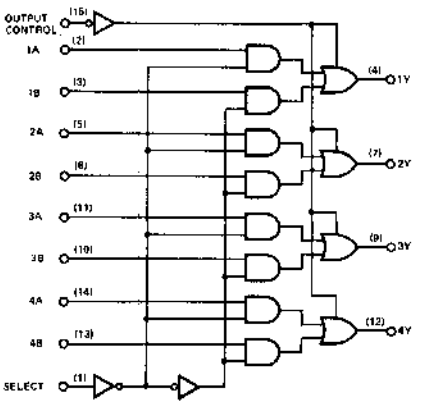
SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	S54S257, N74S257			S54S258, N74S258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	Any	C_L = 15 pF, R_L = 280 Ω, See Note 4		5	7.5		4	6	ns
t_{PHL}					4.5	6.5		4	6	
t_{PLH}	Select	Any			8.5			8	12	ns
t_{PHL}					8.5			7.5	12	
t_{ZH}	Output Control	Any			13	19.5		13	19.5	ns
t_{ZL}					14	21		14	21	
t_{HZ}	Output	Any	C_L = 5 pF See Note 2		5.5	8.5		5.5	8.5	ns
t_{LZ}	Control				9	14		9	14	

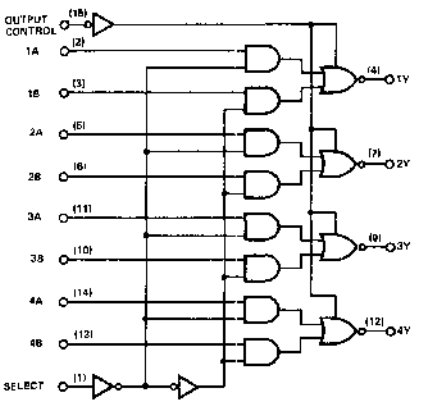
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 2: Load circuit and waveforms are shown on page 2-293

FUNCTIONAL BLOCK DIAGRAMS

S54S257, N74S257



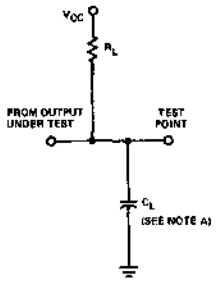
S54S258, N74S258



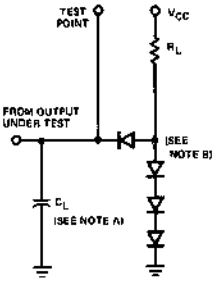
54/74S Typical A.C. Loads And Waveforms

PARAMETER MEASUREMENT INFORMATION

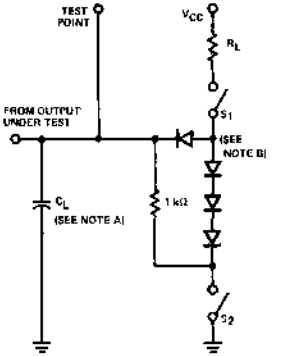
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



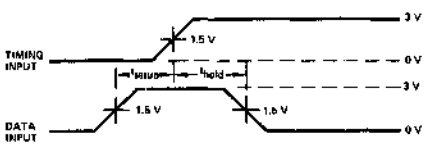
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



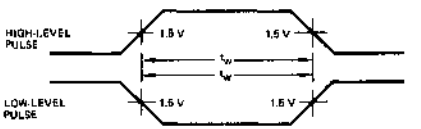
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

TYPICAL AC WAVEFORMS

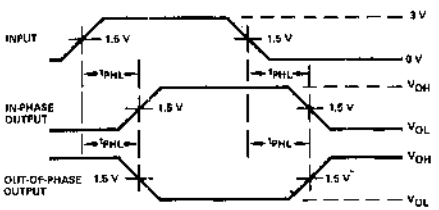
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



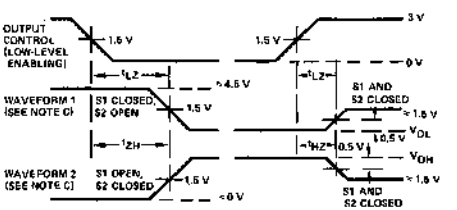
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS



NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

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signetics

MSI/TTL
8000 PRODUCT
SPECIFICATIONS

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MSI Functional Index

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INTRODUCTION

The 8200 Series MSI, 82S Schottky MSI and 8T interface circuits are described in this section. These devices are directly compatible with other TTL circuits such as the bipolar memories covered in Section 4 and the 54/74 series described in Section 2.

Other 8000 Series circuits such as gates, binaries and several interface elements are described in Volume 1 of the 8000 Series that may be obtained from your nearest Signetics representative.

The electrical specifications given for the IC's in this section are designed to serve as an exact guide for procurement documents. Detailed test conditions and test limits are given for each integrated circuit. Whenever possible, worst case limits for the electrical parameters have been provided.

Ordering information for the circuits described in this section can be found below. For the designers convenience, package outlines for each device are given on pages 3–8 through 3–15. This information should be reveiwed in conjunction with detailed package descriptions given in Section 8 where physical dimensions as well as thermal impedance data are given.

Reliability information that details production screens, acceptance tests and qualification tests is given in Section 8 as well. The users attention is also directed to the optional high reliability programs described in Section 8. These are the Signetics SUPR DIP Program for plastic packages and the Signetics SURE 883 program.

Application ideas are provided with the product electrical specifications. Additional applications information may be obtained from the nearest Signetics representative or local Signetics field applications engineer. The user may also find the general systems design considerations helpful which are given on pages 3–2 through 3–7.

ORDERING INFORMATION

Unless otherwise specified all devices are available in the "S" and "N" temperature ranges:

"S" = −55°C to +125°C
"N" = 0°C to + 75°C

The package type designators below, in conjunction with detailed package information given in section 8, may be used for procurement purposes.

PART IDENTIFICATION
Y8XXXZ

Y	= Temperature Range
"S"	= −55°C to +125°C (Military)
"N"	= 0°C to + 75°C (Commercial)

NOTE: 82XX = Standard MSI
82SXX = Schottky MSI
8TXX = Interface Circuit

Z	= Package Type Designator
V	= 8-pin Dual-in-line Plastic Package
A	= 14-pin Dual-in-line Plastic Package
B	= 16-pin Dual-in-line Plastic Package
N	= 24-pin Dual-in-line Plastic Package
F	= 14, 16, 24-pin Dual-in-line Ceramic Package (Cerdip)
W	= 14, 16-pin Ceramic Flat Package (Cerpac)
I	= 14, 16, 24-pin Ceramic Dual-in-line Package
Q	= 14, 16, 24-pin Ceramic Flat Package

ABSOLUTE MAXIMUM RATINGS

Over Operating Free-Air Temperature Range (unless otherwise noted)

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages in accordance with Table 1. These ratings apply to both 82XX and 8TXX MSI devices unless otherwise specified.

TABLE 1

Input Voltage	+5.5V
Output Voltage	+7.0V
V_{CC} (Note 2)	+7.0V
Storage Temperature Range	
A,B, N packages	−65°C to +175°C
F,I,Q,W packages	−65°C to +200°C

NOTES:
1. All devices must be derated at elevated temperatures based on maximum allowable junction temperature. (See maximum storage temperature above and the thermal resistance of the package, given in section 8).
2. Operating V_{CC} for the 8200 Series is specified at +5V ± 5%. None of the Signetics MSI elements will be damaged by supply voltages of 7 volts or less; however, in some of the more complex functions, power dissipation at such voltages could become excessive. It is recommended therefore, that such overvoltages be limited to a maximum of 1 second duration.

SYSTEMS DESIGN CONSIDERATIONS

DC Fan-Out and Noise Margin

Because of the growing complexity of new MSI and memory products, loading and noise margin tables are not included in this section. The numbers are easily generated for individual cases as shown below. The lower of the two numbers is the DC fan-out.

$$\text{DC FAN OUT ("0" Output Condition)} = \frac{\text{"0" maximum output current of driving element}}{\text{"0" maximum input current requirement of driven element}}$$

$$\text{DC FAN OUT ("1" Output Condition)} = \frac{\text{"1" maximum output current of driving element}}{\text{"1" maximum input current requirement of driven element}}$$

DC Noise Margin ("0" state) is obtained by subtracting the maximum "0" level output voltage for the driving gate from the minimum "0" threshold for the driven gate.

DC Noise Margin ("1" state) is obtained by subtracting the maximum "1" level input threshold of the driven gate from the minimum "1" output voltage level of the driving gate.

OUTPUT STRUCTURES

Certain guidelines should be observed to ensure optimum system performance. Systems incorporating TTL elements such as gates, binaries and MSI circuits have inherent V_{CC} and GROUND transients attributable to the current spike produced by "totem pole" output structures.

Figure 1 shows totem pole structures commonly used in MSI designs as output buffers to increase fan-out and provide adequate switching speeds.

COMMON TOTEM POLE OUTPUT STRUCTURES

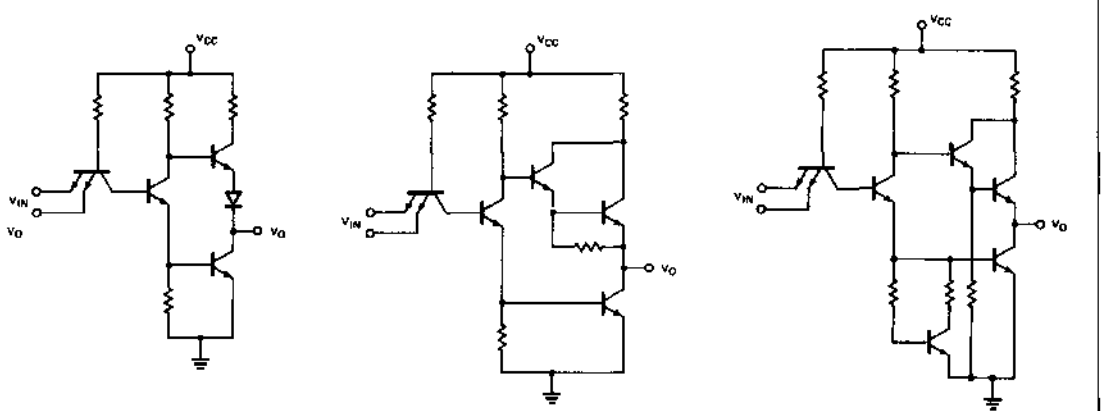


FIGURE 1

DECOUPLING MSI

The current spike produced by the totem pole output structure during switching transitions can cause MSI subsystems to malfunction if V_{CC} is not adequately decoupled to GROUND. With the large number of SSI and MSI devices available it is almost impossible to establish a general rule for decoupling. When in doubt, a capacitor of 2000pF or more, for each totem pole structure should be connected from V_{CC} to GROUND. The non-inductive capacitor (ceramic disc, tantalum slug, etc.) should be mounted with leads as short as possible and should be placed in close proximity to the MSI package to minimize lead length inductance. A properly designed printed circuit board should have the total required capacitance evenly distributed throughout the board. Example: A printed circuit board contains 25 packages averaging four totem pole structures per package. The total capacitance required is 25 packages x 4 totem pole structures x 2000pF or 0.2μF ceramic disc capacitors evenly distributed, satisfy the V_{CC} to GROUND decoupling requirements.

POWER SUPPLY AND GROUND DISTRIBUTION SYSTEMS

High-frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include a large ground plane to minimize DC offsets and to provide an extremely low impedance path to reduce transient voltage signals on the printed circuit board. The power supply should be +5V ±5% with R-F (1GHz) bypassing. Catastrophic damage can occur if V_{CC} is not properly regulated.

Power distributed from the main supply must, by necessity, come through a path which displays finite resistance (R_{PS}), inductance (L_{PS}) and capacitance (C_{PS}), as illustrated in Figure 2. The resistive component of the power lines is small, producing very little DC voltage drop at the V_{CC} and GROUND inputs to the printed circuit board. However, the inductance in the power lines can cause the noise generated by current spiking to be transmitted throughout the system on the V_{CC} and GROUND lines. If the printed circuit boards are adequately decoupled, the power line noise will be reduced significantly. In order to repel power line noise transmitted to a printed circuit board, ferrite beads may be placed on the incoming V_{CC} and GROUND lines as shown in Figure 3. A 10μf tantalum capacitor, per 25 packages, connected from V_{CC} to GROUND should be placed on the printed circuit board in the position shown. In conjunction with the distributed ceramic disc capacitors, this approach will prevent most system malfunctions attributable to internally generated noise.

POWER CHARACTERISTIC IMPEDANCE

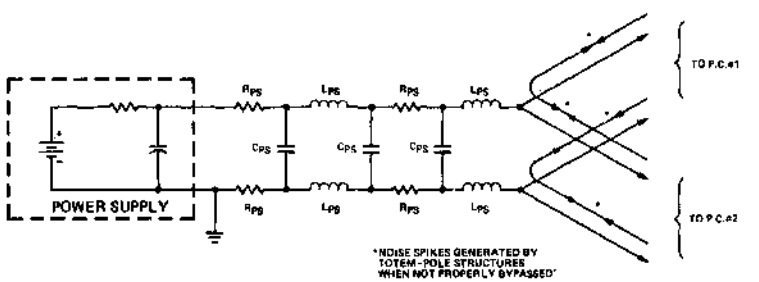


FIGURE 2

FERRITE BEAD
ISOLATION OF GENERATED NOISE

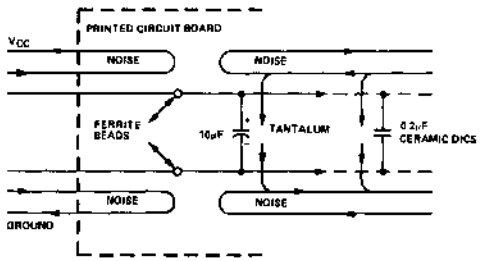


FIGURE 3

ISOLATION DIODES

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

DISPOSITION OF UNUSED INPUTS

Electrically open inputs degrade AC noise immunity as well as the switching speed of an MSI circuit. To optimize performance, each input must be connected to a low impedance source. Depending on their logical activating level, unused inputs should be tied to V_{CC}, GROUND or a driving source. When paralleling an unused input with a driven input of the same multiple emitter transistor (MET), care should be taken to remain within the "1" level fan-out specifications for the driving source. The AND or NAND structures do not affect the "0" level fan-out of the driving source. When an unused input of an OR or NOR structure is commoned with a driven input, both the "1" and "0" level fan-out of the driving source are affected.

If fan-out of the driving source will be exceeded or if there is no convenient connection to an appropriate driven input, a second method of avoiding open inputs is useful. Inputs which activate on "0" (AND and NAND) may be tied directly to V_{CC} or tied to V_{CC} through a current limiting resistor of 1 KΩ or more.

The current limiting resistor is required if power supply transients can exceed 5.5V for longer than 1μsec; since the power dissipated in the emitter junction under these conditions can destroy the junction.

More than one unused input can be tied to V_{CC} through a single resistor.

INPUT CLAMP DIODES

MSI circuits contain input clamp diodes as shown in Figure 4. At the input, these diodes limit negative excursions which exceed −1V by providing a low impedance current source from GROUND through the forward biased diode clamp. The clamps are designed to minimize ringing which may result from interconnect wires in excess of six inches in length.

INPUT CLAMP DIODES

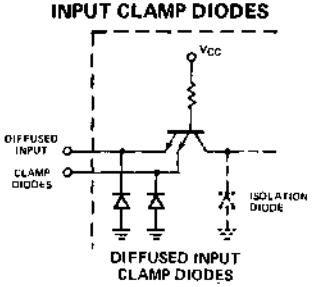


FIGURE 4

SIGNAL PROCESSING

The rise and fall times of all incoming data signals should be less than 200ns. The amplitude of incoming data signals should be 2.4V or greater. Figure 5 shows the transfer characteristic of the classic TTL gate. In the input threshold region, from point one to point two, the gate has approximately 25dB of gain. In this region, any discontinuity of the input waveform will be amplified more than 10 times at the output of the gate.

TTL TRANSFER CHARACTERISTIC

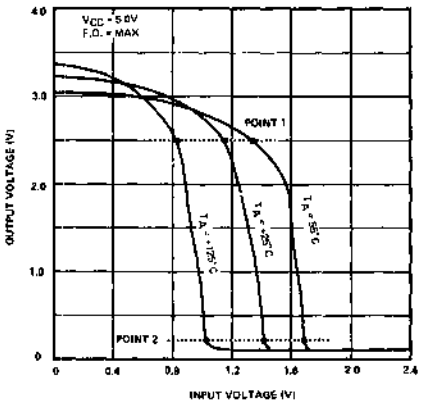


FIGURE 5

Should the input voltage remain in the threshold region (approximately 200mV wide) for more than 15ns, a typical TTL gate tends to oscillate as shown in Figure 6. The equivalent circuit in Figure 7 illustrates the potential oscillatory feed-back paths. The primary contributor to oscillation is the changing power supply voltage with the chip, caused by the current spiking which occurs during switching transitions. Since output voltage is directly proportional to V_{CC} and threshold voltage tends also to drop with lower supply voltage, the net effect is a positive feedback loop from output to input.

TYPICAL TTL GATE OSCILLATION WITH SLOW INPUT TRANSITIONS

FIGURE 6

POTENTIAL OSCILLATORY FEEDBACK PATHS

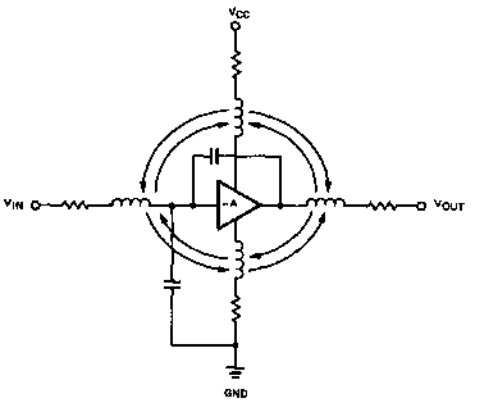


FIGURE 7

WIRED-AND APPLICATIONS OF OPEN-COLLECTOR MSI

Open-collector MSI, when supplied with a proper load resistor (R_L) can be paralleled with other similar MSI or open collector TTL gates to perform the WIRED-AND function, and simultaneously, will drive several TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. The user may choose a load resistor that must be between the following limits: A maximum resistor value must be determined which will ensure that sufficient load current to the TTL loads to be driven, as well as leakage current to the paralleled outputs, is available during the logical "1" state at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical "0" level even if one of the paralleled outputs is sinking all the current.

LOGICAL "1" (off level) CALCULATIONS FOR R_L MAX

The maximum value of load resistance (R_L MAX) is determined by the maximum voltage drop across R_L caused by the total leakage current which will still ensure a minimum logical "1" at the common collector node. As shown in Figure 8:

Total leakage current $I(1)_{total} = n\,I(1)_{off} + m\,I(1)_{in}$
n = Number of commoned collectors (driving gates)
m = Number of fan-outs (driven gates)

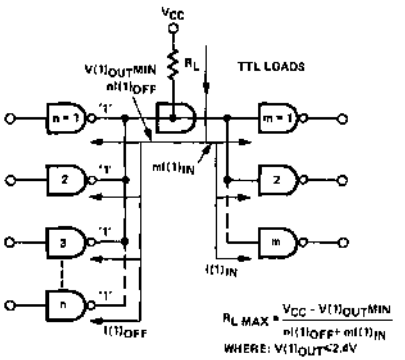


FIGURE 8

LOGICAL "0" (on level) CALCULATIONS FOR R_L MIN

The minimum value of load resistance (R_L MIN) is determined from the worst case maximum logical "0" state in which only one element is sinking current. This condition is illustrated in Figure 9:

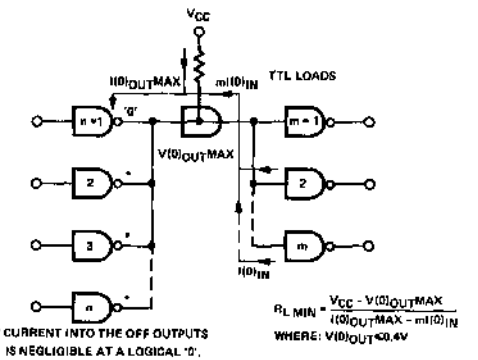


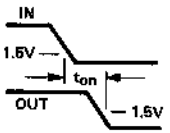
FIGURE 9

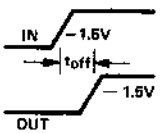
PROPAGATION DELAY

Propagation delay for the 8000 Series elements is specified in terms of t_{on} and t_{off} switching times which provides a figure of merit by which comparison can be made with similar products. The guaranteed delay times given in the electrical characteristics section take into consideration the logical "1" and logical "0" input current and load capacitance as shown in the AC test figures. Inverting and non-inverting paths are measured as shown in Figure 10.

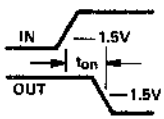
PROPAGATION DELAY WAVEFORMS

NON-INVERTING PATHS





INVERTING PATHS



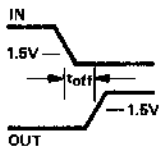
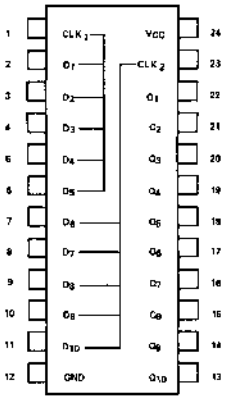


FIGURE 10

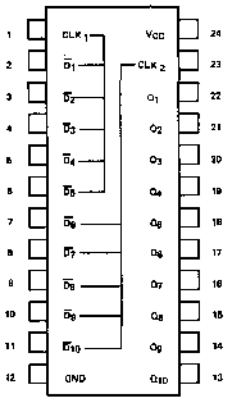
PIN CONFIGURATIONS

8200



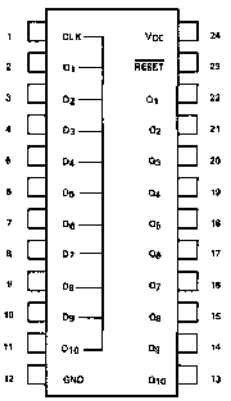
N,F,Q PACKAGES

8201



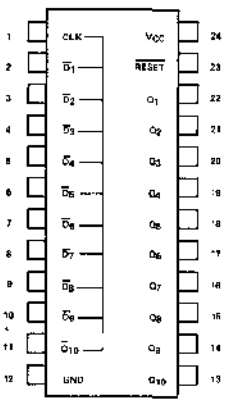
N,F,Q PACKAGES

8202



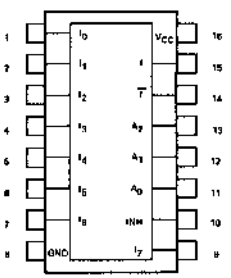
N,F,Q PACKAGES

8203



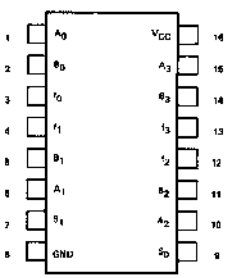
N,F,Q PACKAGES

8230/31/32



B,F,W PACKAGES

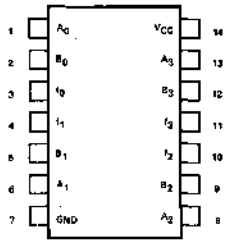
8233/34/35



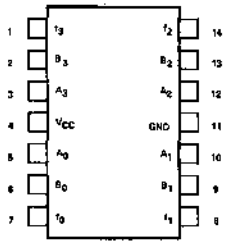
B,F,W PACKAGES

PIN CONFIGURATIONS (Cont'd)

8241/42

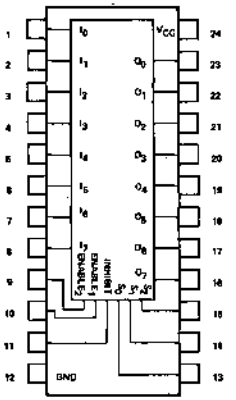


A,F PACKAGES



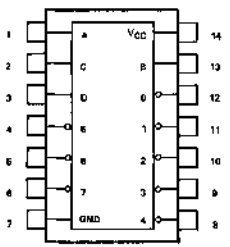
W PACKAGE

8243

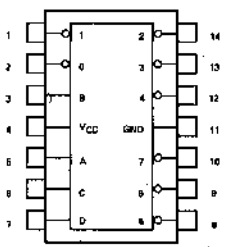


N,F,Q PACKAGES

8250

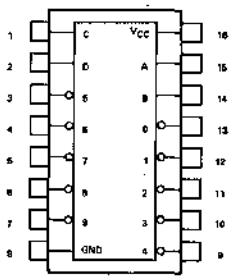


A,F PACKAGES



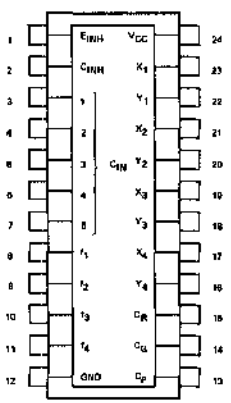
W PACKAGE

8251/52



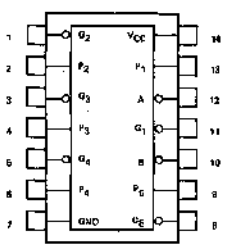
B,F,W PACKAGES

8260

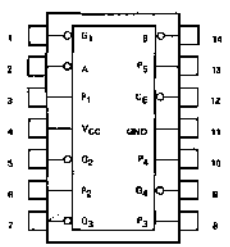


N,F,Q PACKAGES

8261



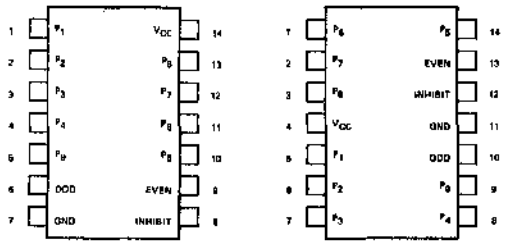
A,F PACKAGES



W PACKAGE

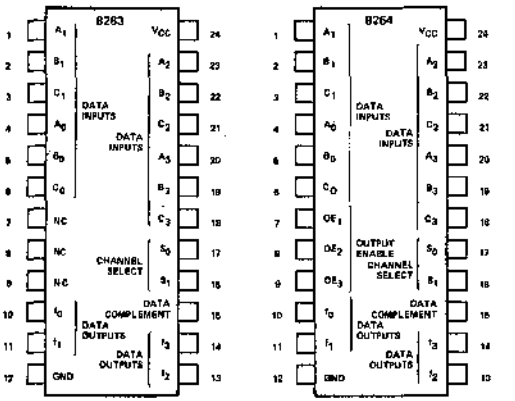
PIN CONFIGURATIONS (Cont'd)

8262



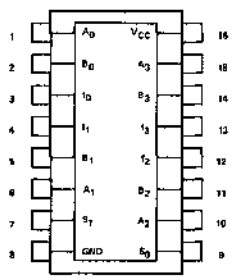
A,F PACKAGES W PACKAGE

8263/64



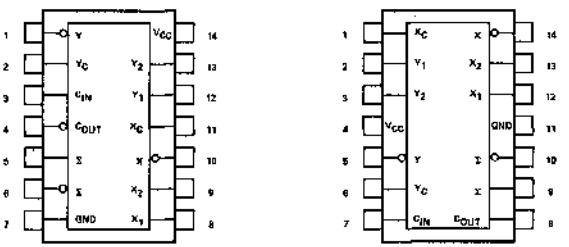
N,F,Q PACKAGES

8266/67



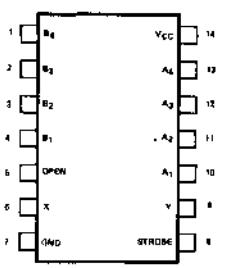
B,F,W PACKAGES

8268



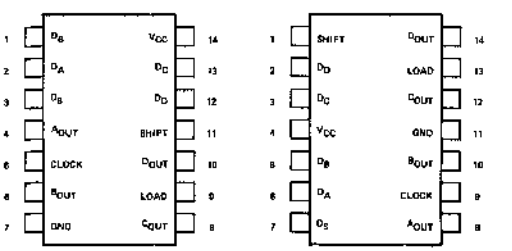
A,F PACKAGES W PACKAGE

8269



A,F,W PACKAGES

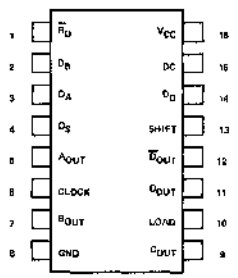
8270



A,F PACKAGES W PACKAGE

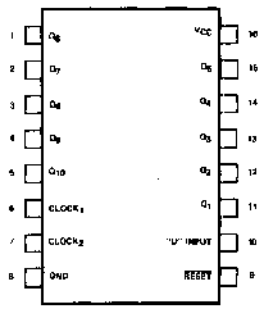
PIN CONFIGURATIONS (Cont'd)

8271



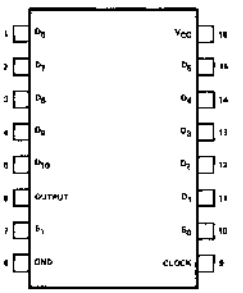
B,F,W PACKAGES

8273



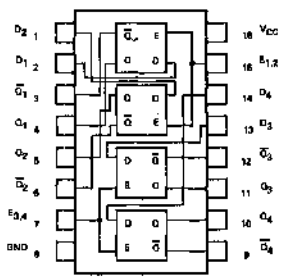
B,F,W PACKAGES

8274



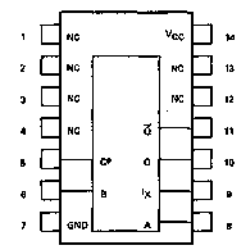
B,F,W PACKAGES

8275



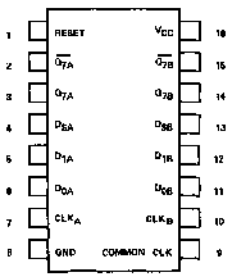
B,F,W PACKAGES

8276



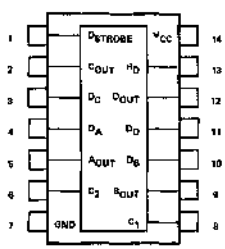
A,F PACKAGES

8277

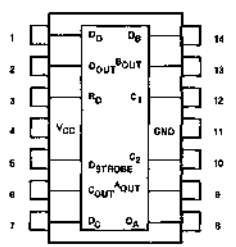


B,F PACKAGES

8280/81

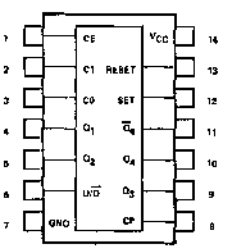


A,F PACKAGES

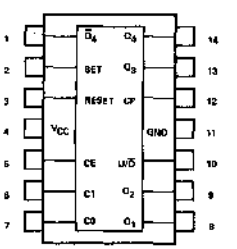


W PACKAGE

8284/85



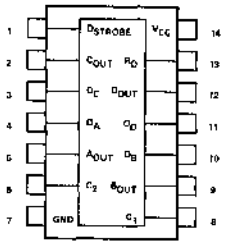
A,F PACKAGES



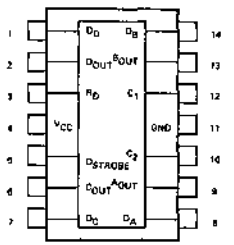
W PACKAGE

PIN CONFIGURATIONS (Cont'd)

8288

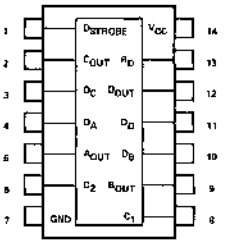


A,F PACKAGES

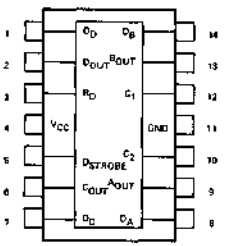


W PACKAGE

8290/91

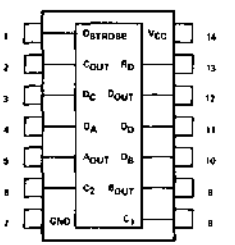


A,F PACKAGES

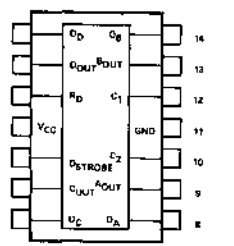


W PACKAGE

8292/93



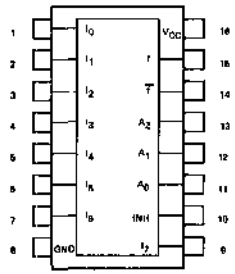
A,F PACKAGES



W PACKAGE

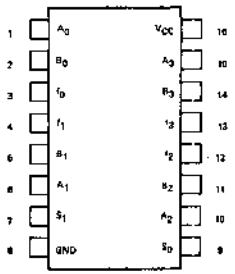
PIN CONFIGURATIONS (Cont'd)

82S30/31/32



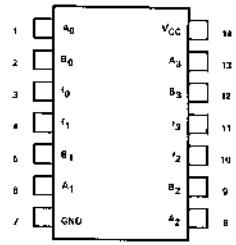
B,F PACKAGES

82S33/34



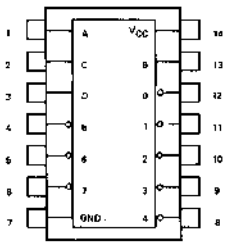
B,F PACKAGES

82S41/42



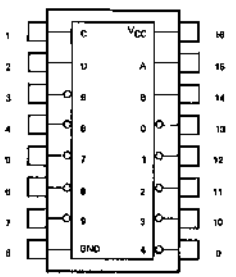
A,F PACKAGES

82S50



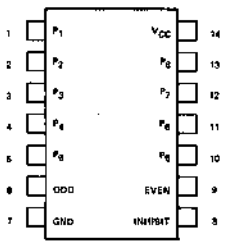
A,F PACKAGES

82S52



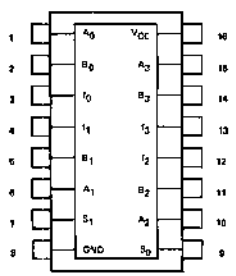
B,F PACKAGES

82S62



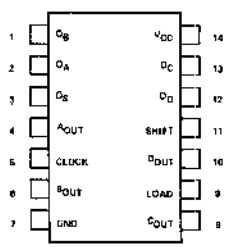
A,F PACKAGES

82S66/67



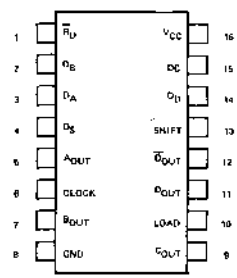
B,I PACKAGES

82S70



A,F PACKAGES

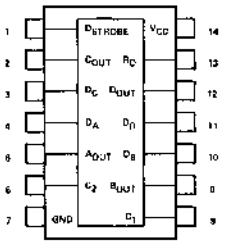
82S71



B,F PACKAGES

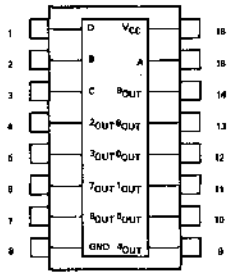
PIN CONFIGURATIONS (Cont'd)

82S90/91



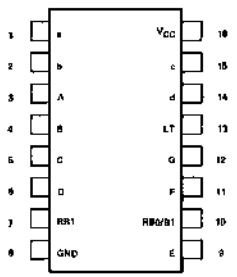
A,F PACKAGES

8T01



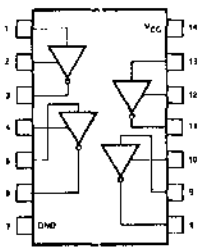
B,F PACKAGES

8T04/05/06

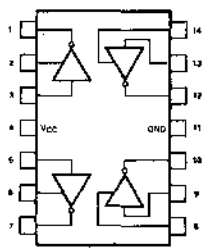


B,F,W PACKAGES

8T09

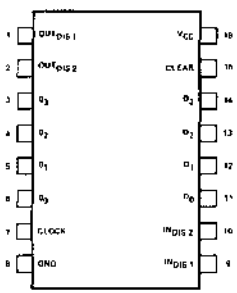


A,F PACKAGES



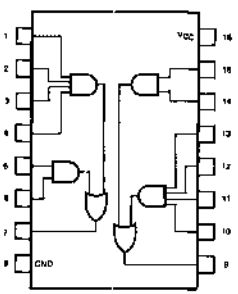
W PACKAGE

8T10



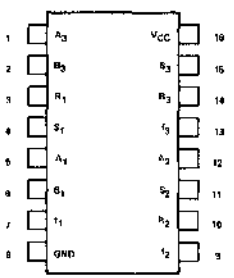
B,F,W PACKAGE

8T13



B,F,W PACKAGES

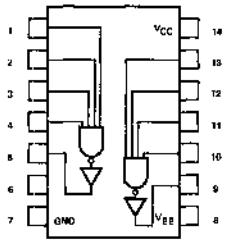
8T14



B,F,W PACKAGES

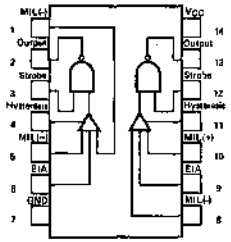
PIN CONFIGURATION (Cont'd)

8T15



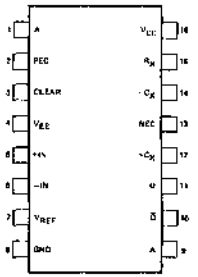
A,F PACKAGES

8T16



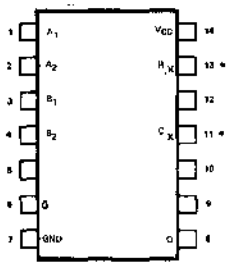
A,F PACKAGES

8T20



B,F PACKAGES

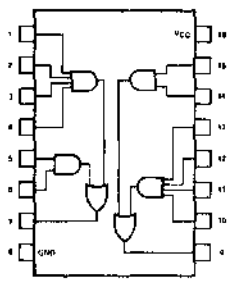
8T22



*Pins for External Timing Components

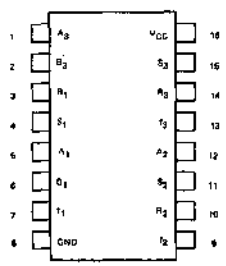
A,F PACKAGES

8T23



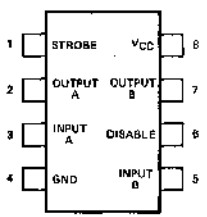
B,W PACKAGES

8T24



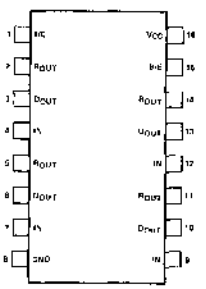
B,W PACKAGES

8T25



V PACKAGE

8T26



B,F PACKAGES

DESCRIPTION

The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel-in parallel-out register applications. They are also suitable for general purpose applications as parallel-in serial-out, serial-in parallel-out registers.

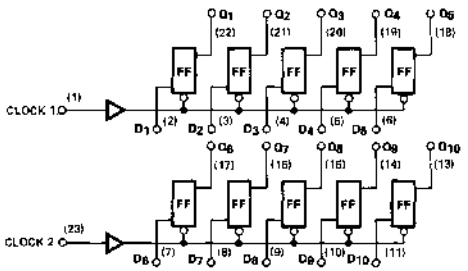
The flip-flops are arranged as dual 5 arrays, (8200 & 8201) and single 10 arrays with reset, (8202 & 8203). The true output of each bit is made available to the user.

The 8200 and 8202 feature true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock.

The 8201 and 8203 feature complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative going transition of the clock. This complementing input feature ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

LOGIC DIAGRAMS AND TRUTH TABLES

DUAL 5-BIT BUFFER REGISTER

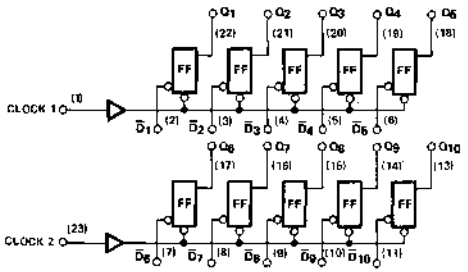


D_n	Q_{n+1}
1	1
0	0

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8200

DUAL 5-BIT BUFFER REGISTER–INVERTED INPUTS

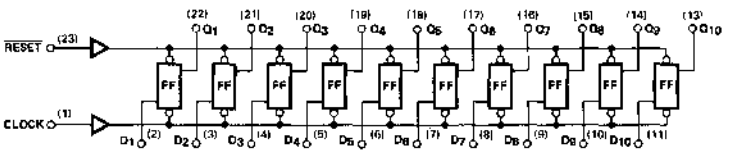


$\overline{D}_n$	Q_{n+1}
1	0
0	1

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8201

10-BIT BUFFER REGISTER



D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

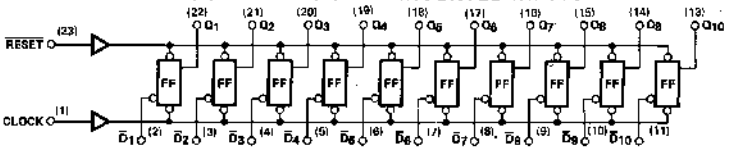
$\overline{RESET}$ = 0 ⇒ Q = 0
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8202

LOGIC DIAGRAMS AND TRUTH TABLES (Cont'd)

10-BIT BUFFER REGISTER—INVERTED INPUTS



D_n	$\overline{RESET}$	Q_{n+1}
0	1	1
1	1	0

$\overline{RESET}$ = 0 ⇒ Q = 0
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8203

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n 8200 8202	$\overline{D_n}$ 8201 8203	CLOCK	$\overline{RESET}$ 8202 8203	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	0.8V	Pulse		−800μA	6
"0" Output Voltage			0.4	V	0.8V	2.0V	Pulse		9.6mA	7
"0" Input Current										
D_n (8200, 8202)	−0.1		−1.6	mA	0.4V					
$\overline{D_n}$ (8201, 8203)	−0.1		−1.6	mA		0.4V				
Clock	−0.1		−1.6	mA			0.4V			
$\overline{Reset}$ (8202, 8203)	−0.1		−1.6	mA				0.4V		
"1" Input Current										
D_n (8200, 8202)			40	μA	4.5V					
$\overline{D_n}$ (8201, 8203)			40	μA		4.5V				
Clock			40	μA			4.5V			
Reset (8202, 8203)			40	μA				4.5V		
Input Voltage Rating (All inputs)	5.5			V	10mA	10mA	10mA	10mA		
Power/Current Consumption		409/77.7	580/110	mW/mA	0V	0V	0V			11,13

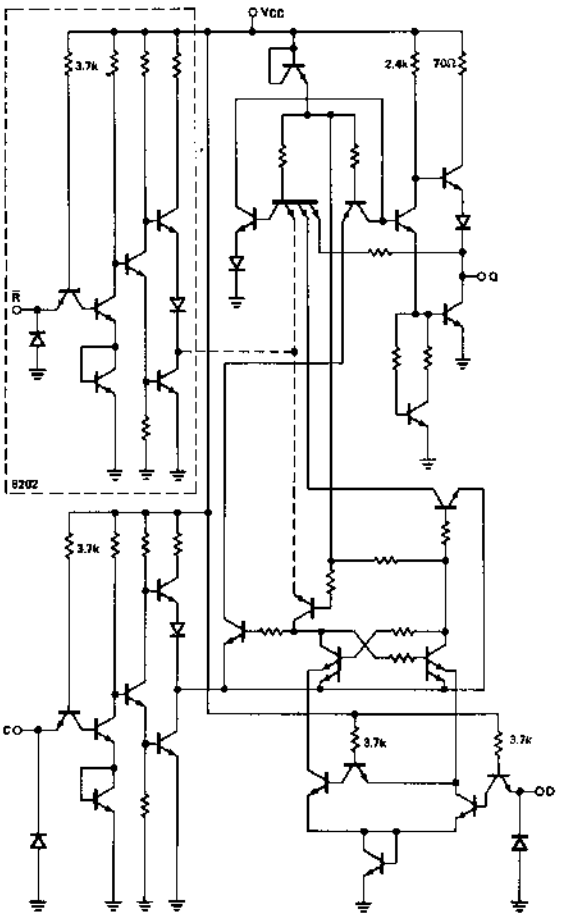
T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Propagation Delay						
t_{on} Clock to Q		30	45	ns		8
t_{off} Clock to Q		25	40	ns		8
t_{on} Reset to Q		30	45	ns		8
Set Up Time		6	15	ns		10
Hold Time		0	5	ns		12
Minimum Clock Pulse Width		12	17	ns		
Transfer Rate	15	35		MHz		8
Output Short Circuit Current	−20		−70	mA		9, 13

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to V_{CC}.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. Set Up Time defined as data presence before clock.
11. Outputs are in the low state for this test.
12. Hold time defined as data presence after clock.
13. V_{CC} = 5.25 volts.

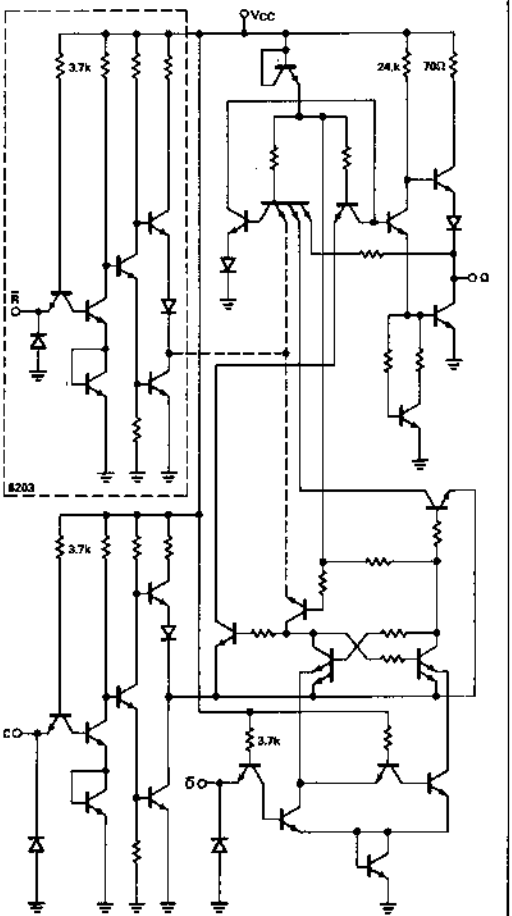
SCHEMATIC DIAGRAMS

DUAL 5-BIT BUFFER REGISTER 8200
SINGLE 10-BIT BUFFER REGISTER 8202



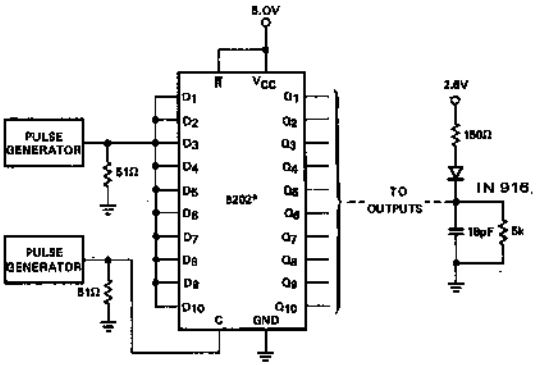
DUAL 5-BIT BUFFER REGISTER
INVERTED INPUTS 8201

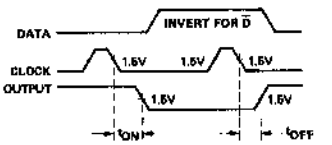
SINGLE 10-BIT BUFFER REGISTER
INVERTED INPUTS 8203



AC TEST FIGURES AND WAVEFORMS

t_{pd} FROM CLOCK TO Q

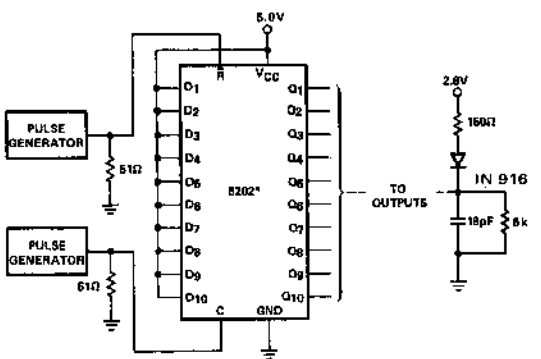


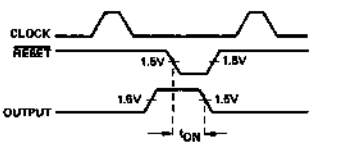


INPUT PULSE:
Data = P.R.R. = 7.5 MHz
Clock = P.R.R. = 15 MHz
PW = 17 ns (at 50% point)
$t_r = t_f = 5$ ns Max.
Amplitude = 2.6V.

*Refer to the Pin-Outs for the 8200/01/03 AC Testing.

t_{on} FROM $\overline{\text{RESET}}$ TO Q



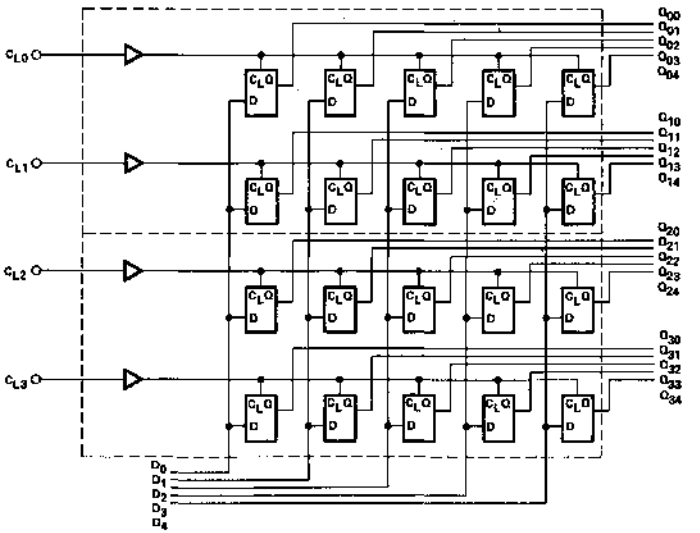


INPUT PULSE:
Amplitude = 2.8V
Clock: P.R.R. = 5 MHz
$\overline{\text{Reset}}$: P.R.R. = 5 MHz
PW = 30 ns (at 50% point)
$t_r = t_f = 5$ ns

*Refer to the Pin-Outs for the 8200/01/02/03 AC Testing.

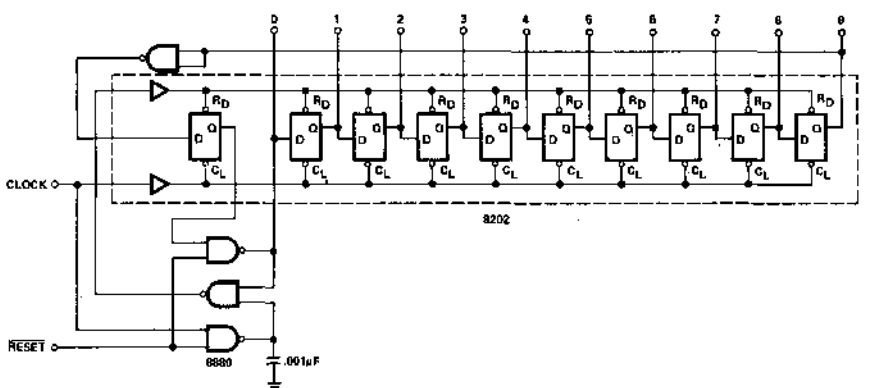
TYPICAL APPLICATIONS

20 BIT (4 WORDS X 5 BITS EACH) MEMORY CELL



Total Package Count = 2-8200's

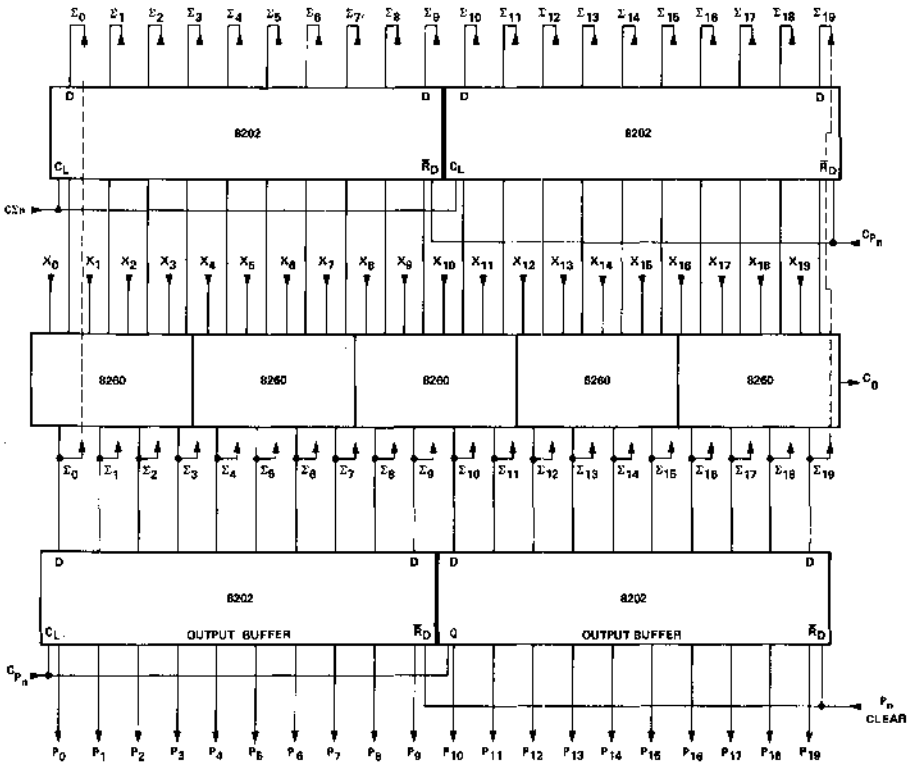
ONE OUT OF TEN – COUNTER/DISPLAY (SELF-CORRECTING)



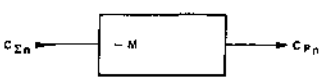
Total Package Count = 1-8202; 1-8880

TYPICAL APPLICATIONS (Cont'd)

MULTIPLICATION AT 10MHz OF A 20-BIT BINARY WORD



$P_O = (X_n)M$ WHERE $X_n \equiv$ MULTIPLICAND
$M \equiv$ MULTIPLIER
TOTAL PACKAGE COUNT = 9 PACKAGES (4-8202'S AND 5-8260'S)



signetics

8-INPUT DIGITAL MULTIPLEXER

B,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

8230
8231
8232

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 8230 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, the f output is unconditionally low and the $\bar{f}$ output is unconditionally high. The 8230 is a functional and pin-for-pin replacement for the 9312.

The 8231 is a variation of the 8230 that provides open collector output $\bar{f}$ for expansion of input terms. The 8232 is similar to the 8230 except in the effect of the INHIBIT input on the $\bar{f}$ output. With the INHIBIT low, the selected input appears at the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, both the f and the $\bar{f}$ output are unconditionally low.

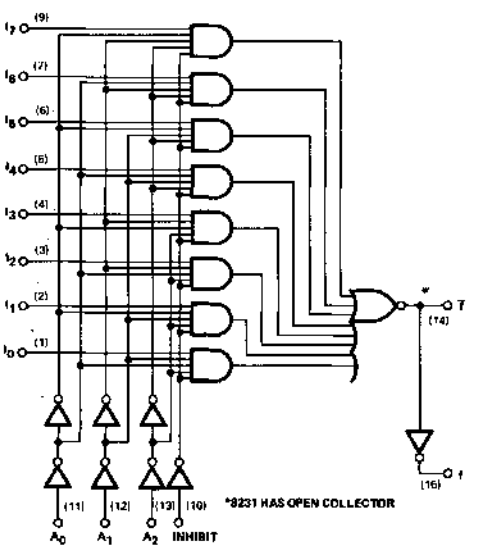
TRUTH TABLE

ADDRESS			DATA INPUTS									OUTPUT		
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	f	8230 8231 $\bar{f}$	8232 $\bar{f}$
0	0	0	x	x	x	x	x	x	x	1	0	1	0	0
0	0	1	x	x	x	x	x	x	1	x	0	1	0	0
0	1	0	x	x	x	x	x	1	x	x	0	1	0	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0	0
1	0	0	x	x	x	1	x	x	x	x	0	1	0	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1	1
0	0	1	x	x	x	x	x	x	0	x	0	0	1	1
0	1	0	x	x	x	x	x	0	x	x	0	0	1	1
0	1	1	x	x	x	x	0	x	x	x	0	0	1	1
1	0	0	x	x	x	0	x	x	x	x	0	0	1	1
1	0	1	x	x	0	x	x	x	x	x	0	0	1	1
1	1	0	x	0	x	x	x	x	x	x	0	0	1	1
1	1	1	0	x	x	x	x	x	x	x	0	0	1	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1	0

x = don't care

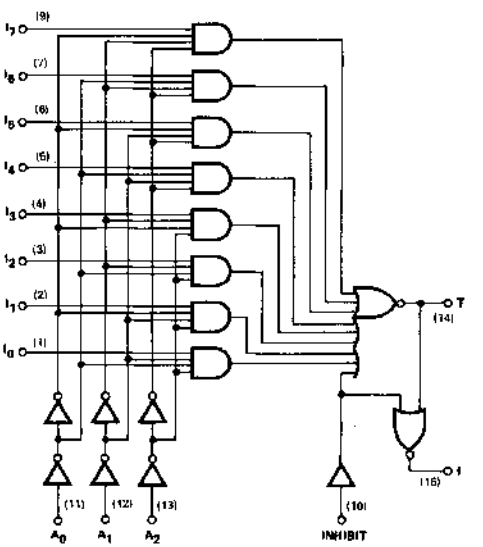
LOGIC DIAGRAMS

8230 AND 8231



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8232



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	A_1	A_2	A_3	INH	DATA INPUT In	OUTPUTS	
"1" Output Voltage, Output f	2.6	3.5		V	*	*	*	0.8V	2.0V	-800μA	6, 9
Output $\overline{f}$ (8230, 8232)	2.6	3.5		V	*	*	*	2.0V	*	-800μA	6, 9
"1" Output Leakage Current, Output $\overline{f}$ (8231)			150	μA	0.8V	2.0V	2.0V	2.0V	0.6V		11
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V	0.8V	0.8V	16mA	7, 9
"1" Input Current											
Inputs An, I_n			40	μA	4.5V	4.5V	4.5V		4.5V		
Input INH, 8230 & 8231			80	μA				4.5V			
Input INH, 8232			80	μA				4.5V			
"0" Input Current											
A_n, I_n, INH (8230 & 8231)	-0.1		-1.6	mA	0.4V	0.4V	0.4V		0.4V		
INH, (8232)	-0.1		-3.2	mA				0.4V			

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	A	A	A	INH	DATA INPUT In	OUTPUTS f $\overline{f}$	
Propagation Delay											
A_n to $\overline{f}$ (8230, 8232)		19	30	ns							8
A_n to $\overline{f}$ (8231)		17	30	ns							8
I_n to $\overline{f}$ (8230, 8232)		11	20	ns							8
$\overline{f}$ to f		10	15	ns							8
I_n to $\overline{f}$ (8231)		13	24	ns							8
INH to $\overline{f}$ (8230, 8231)		18	30	ns							8
INH to f or $\overline{f}$ (8232)		11	20	ns							8
Power Consumption/Supply Current											
8230, 8231		184/ 35	260/ 47.7	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		10
8232		173/ 33	262/ 50.0	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		10
Output Short Circuit Current											
Output f	-20		-70	mA	0V	0V	0V	0V	4.5V	0V	10, 12
Output $\overline{f}$ (8230, 8232)	-20		-70	mA	0V	0V	0V	0V	0V	0V	10, 12
Input Voltage Rating	5.5			V	10mA	10mA	10mA	10mA	10mA		

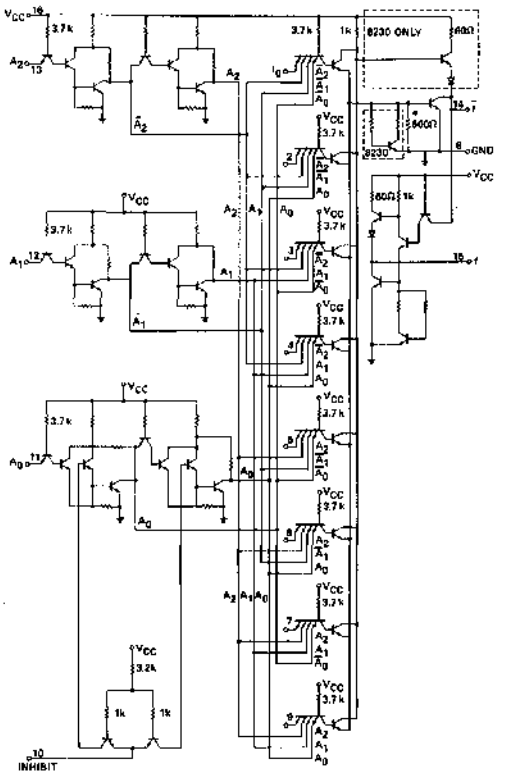
*See Truth Table for Logical Conditions

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
10. All 1_n data inputs are at 0V. $V_{CC} = 5.25V$.
11. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
12. Not more than one output should be shorted at a time.

SCHEMATIC DIAGRAMS

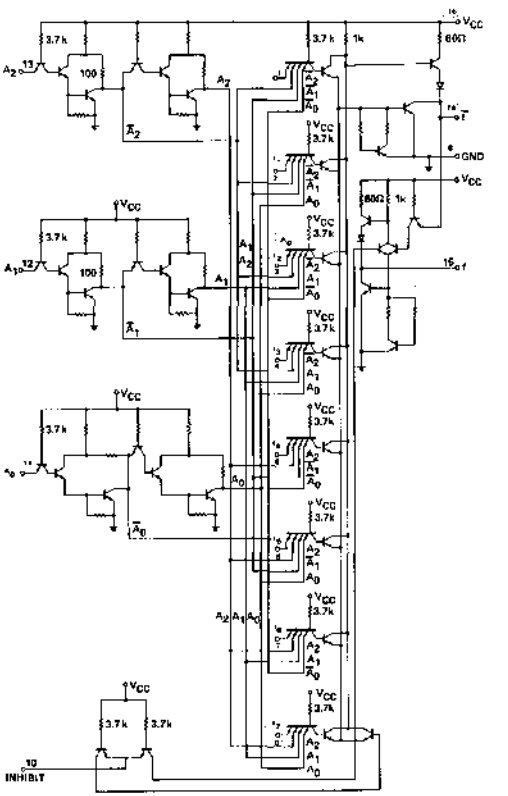
8230 AND 8231



*500 Resistor on 8231 only.

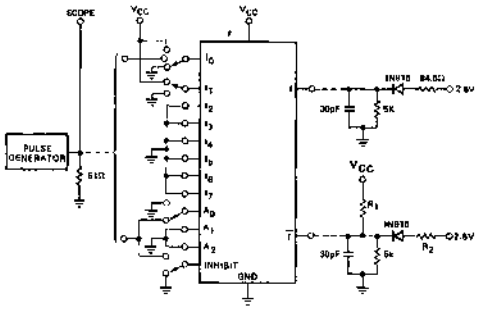
Note: All inputs have diode clamping. All outputs have isolation diodes.

8232



Note: All inputs have diode clamping. All outputs have isolation diodes.

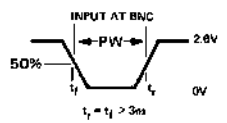
AC TEST FIGURE AND WAVEFORMS

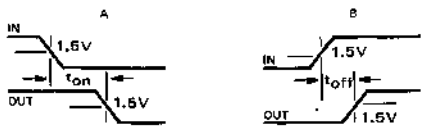


	8320/32	8231
R_1	∞	360Ω
R_2	84.5Ω	440Ω

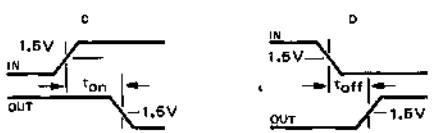
NOTES:
1. 5K, 30pF load includes test jigs and scope impedance.
2. Scope terminals to be ⩽ 1½" from package pins.
3. See truth table for logical conditions.

NON-INVERTING PATHS





INVERTING PATHS



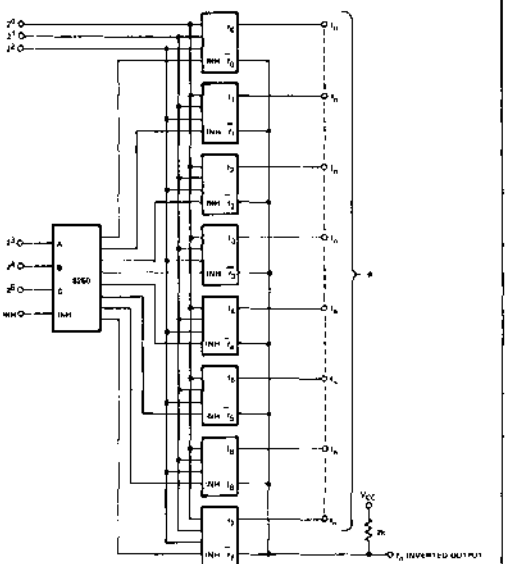
AC TEST CONDITIONS

STEP NO.	TYPE/S	DELAY FROM-TO	INPUTS I_0	INPUTS I_1	INPUTS A_0	INPUTS INH	WAVE-FORM TYPE
1	ALL	A_0 to $\overline{f}$	0 V	V_{CC}	P.G.	0 V	C, D
2	ALL	I_0 to $\overline{f}$	P. G.	0 V	0 V	0 V	C, D
3	ALL	$\overline{f}$ to f*	P. G.	0 V	0 V	0 V	C, D
4	8230 8231	INH to $\overline{f}$	V_{CC}	0 V	0 V	P. G.	A, B
5	8232	INH to $\overline{f}$	0 V	0 V	0 V	P. G.	C, D
6	8232	INH to f	V_{CC}	0 V	0 V	P. G.	C, D

NOTE: 1. P. G. = Pulse Generator
*Both f and $\overline{f}$ are simultaneously loaded.

TYPICAL APPLICATIONS

EXPANSION OF 8231 TO MULTIPLEXER 64 LINES



*$f_n = f_0 + f_1 + f_2 \ldots . f_7$
True Output
All Outputs may be tied together to drive 8x16mA (eight 1.6mA F.O.) or each Output may drive separately ten 1.6mA F.O.

Note:
Each 8231 has 8 data inputs which are not shown.

signetics

2-INPUT 4-BIT DIGITAL MULTIPLEXER

B,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

8233 8234 8235

DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features *non-inverting* data paths; and, the 8234 features *inverting* data paths.

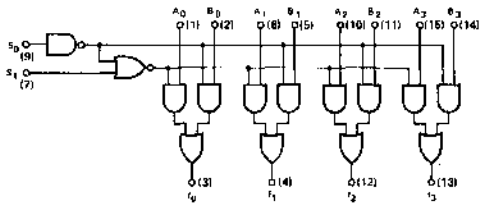
The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform CONDITIONAL COMPLEMENTING (TRUE/COMPLEMENT). When the two inputs for each bit position (Ai, Bi) are connected together, the f output will provide either the *True* or *Complement* of the input data. This capability is especially useful for transferring data into parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

LOGIC DIAGRAM AND TRUTH TABLES

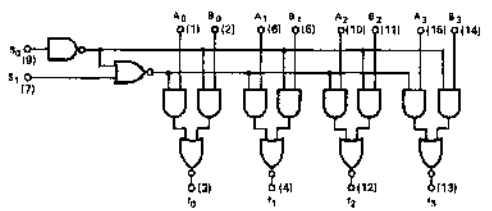
8233 (ACTIVE PULL-UP)



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

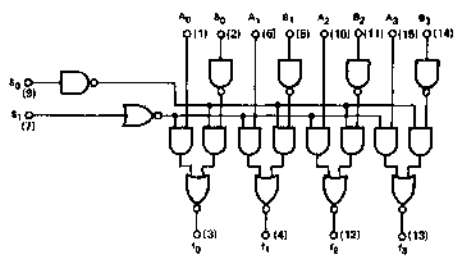
8234 (OPEN COLLECTOR)



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8235 (OPEN COLLECTOR)



S_0	S_1	f_n
0	0	$\overline{A_n}B_n$
0	1	B_n
1	0	$\overline{A_n}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					INPUTS					
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (8233)	2.6	3.5		V	2.0V	2.0V	0.8V	0.8V	-800μA	6
"0" Output Voltage (8233)			0.4	V	0.8V	2.0V	2.0V	0.8V	16mA	7
"0" Output Voltage (8234)			0.4	V	0V	2.0V	0.8V	0.8V	16mA	7
"0" Output Voltage (8235)			0.4	V	2.0V	2.0V	2.0V	0.8V	16mA	7
"1" Output Leakage Current										
(8234)			100	μA	2.0V	2.0V	2.0V	2.0V	5.0V	8
"1" Output Leakage Current										
(8235)			100	μA	2.0V	2.0V	2.0V	2.0V	5.0V	8
"0" Input Current										
A_n	-0.1		-1.6	mA	0.4V	4.5V		0V		
B_n	-0.1		-1.6	mA	4.5V	0.4V	0V	0V		
S_0	-0.1		-1.6	mA			0.4V			
S_1	-0.1		-1.6	mA				0.4V		
"1" Input Current										
A_n			40	μA	4.5V	0V				
B_n			40	μA	0V	4.5V				
S_0			40	μA			4.5V			
S_1			40	μA				4.5V		
Input Voltage Rating										
A_n	5.5			V	10mA	0V				
B_n	5.5			V	0V	10mA				
S_0	5.5			V			10mA			
S_1	5.5			V				10mA		
Output Short Circuit Current										
(8233)	-20		-70	mA	5V	5V	0V	0V	0V	10, 11
Input Clamp Voltage										
A_n			-1.5	V	-12mA					
B_n			-1.5	V		-12mA				
S_0			-1.5	V			-12mA			
S_1			-1.5	V				-12mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$

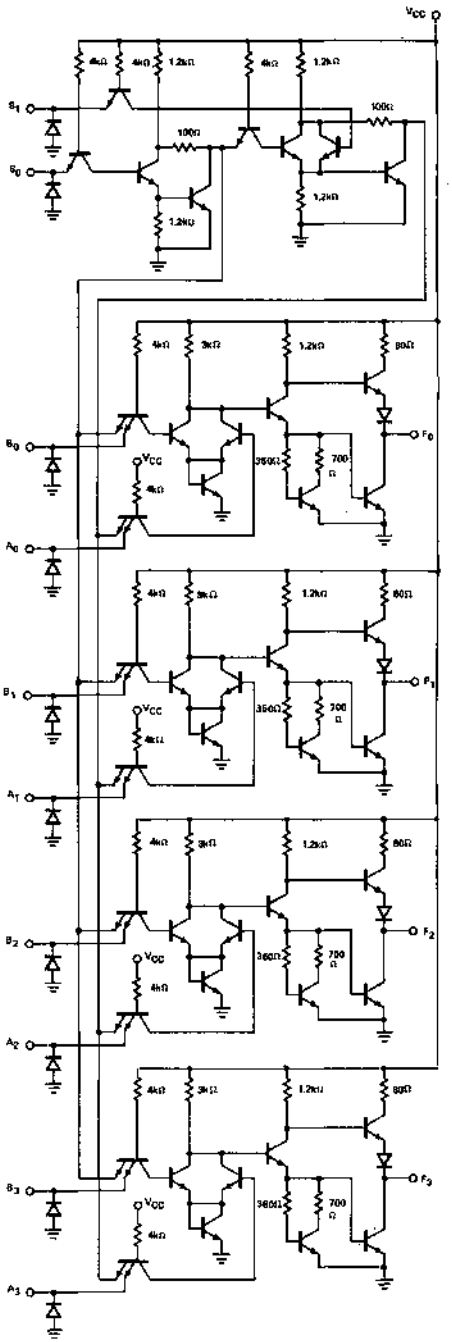
CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					INPUTS					
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1		
Power/Current Consumption:										
8233		200/38	252/48	mW/mA		0V		0V		10
8234		160/31	210/40	mW/mA		0V		0V		10
8235		230/44	310/69	mW/mA		4.5V		4.5V		10
8233 Turn-On Times, t_{on}										
A_n, B_n to f_n		16	25	ns						9
S_0 to f_n		27	38	ns						9
S_1 to f_n		27	38	ns						9
8233 Turn-Off Times, t_{off}										
A_n, B_n to f_n		16	25	ns						9
S_0 to f_n		27	38	ns						9
S_1 to f_n		27	38	ns						9
8234 Turn-On Times, t_{on}										
A_n, B_n to f_n		16	25	ns						9
S_0 to f_n		27	38	ns						9
S_1 to f_n		27	38	ns						9
8234 Turn-Off Times, t_{off}										
A_n, B_n to f_n		16	25	ns						9
S_0 to f_n		27	38	ns						9
S_1 to f_n		27	38	ns						9
8235 Turn-On Times, t_{on}										
A_n to f_n		16	25	ns						9
B_n to f_n		24	35	ns						9
S_0 to f_n		27	38	ns						9
S_1 to f_n		27	38	ns						9
8235 Turn-Off Times, t_{off}										
A_n to f_n		16	25	ns						9
B_n to f_n		24	35	ns						9
S_0 to f_n		27	38	ns						9
S_1 to f_n		27	38	ns						9

NOTES:

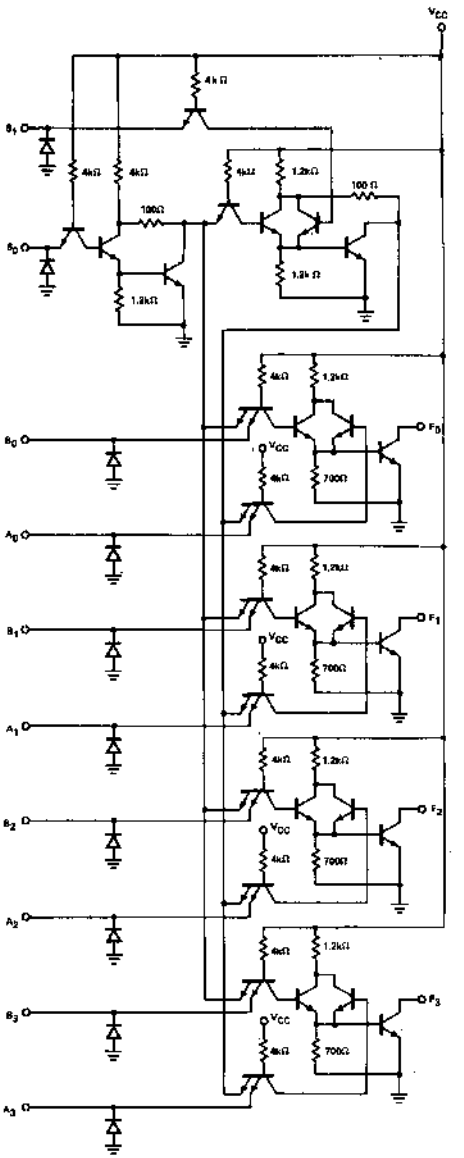
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
9. Reference AC Test Circuit, Waveforms and Test Tables.
10. $V_{CC} = 5.25V$.
11. Not more than one output should be shorted at a time.

SCHEMATIC DIAGRAMS

8233 (ACTIVE PULL-UP)

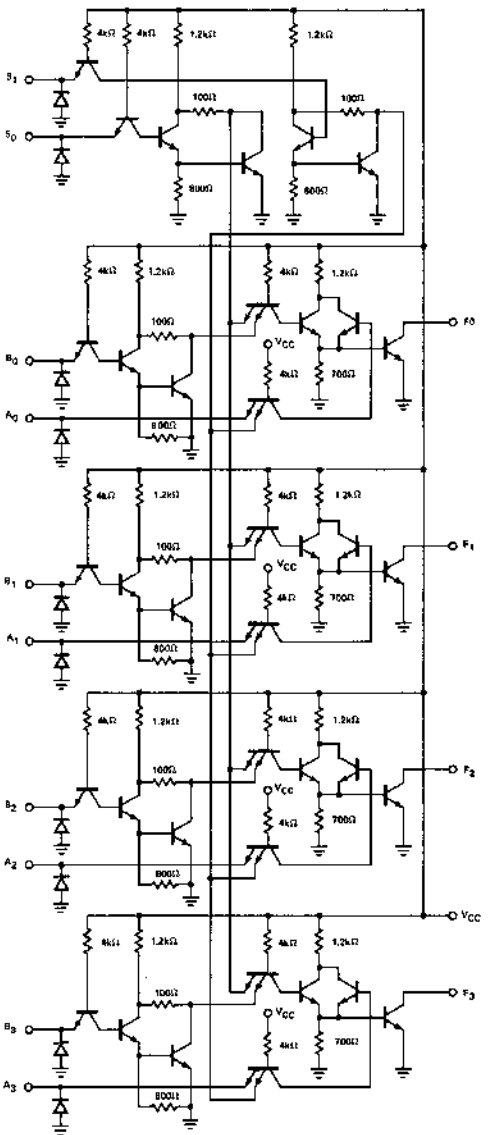


8234 (OPEN COLLECTOR)



SCHEMATIC DIAGRAMS (Cont'd)

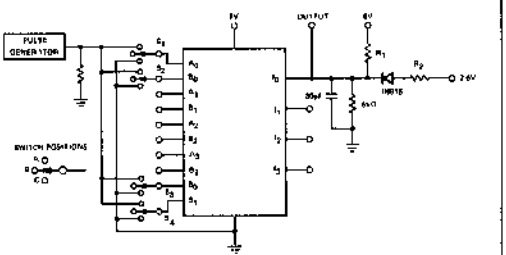
8235



PROPAGATION DELAY TEST TABLE

PRODUCT	PATH	PARAMETER	S_1	S_2	S_3	S_4
ALL	A_0 to f_0	$\frac{t_{on}}{t_{off}}$	a	b	b	c
8233 8234	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	c	a	c	b
8233 8234	S_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	b	a	b
8233 8234	S_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	a	c
8235	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	c	a	c	b
8235	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	a	b
8235	S_1 to f_0	$\frac{t_{on}}{t_{off}}$	b	b	c	a
8233 8234	S_1 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	b	a

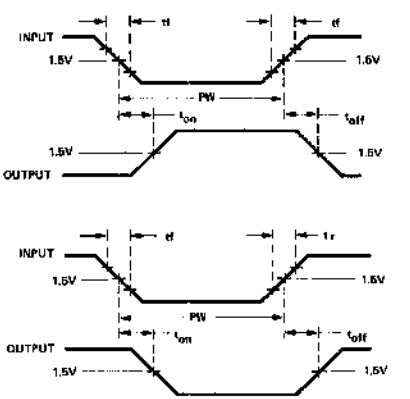
AC TEST FIGURE AND WAVEFORMS



	R_1	R_2
8233	∞	84.5Ω
8234 8235	360Ω	440Ω

INPUT PULSE:
Amplitude = 2.6V
PW = 200ns
PRR = 1 MHz
$t_r = t_f$ = 5ns

PULSE REQUIREMENTS



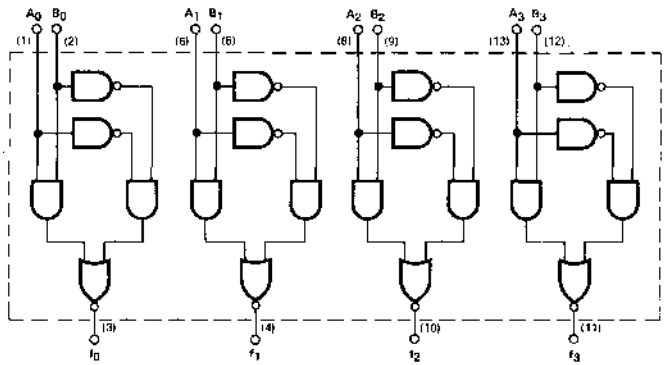
DESCRIPTION

The 8241 contains four independent gating structures to perform the Exclusive-OR function on two input variables. The output of the 8241 employs the totem-pole structure characteristic of TTL devices.

The 8242 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 8242 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

LOGIC DIAGRAMS AND TRUTH TABLES

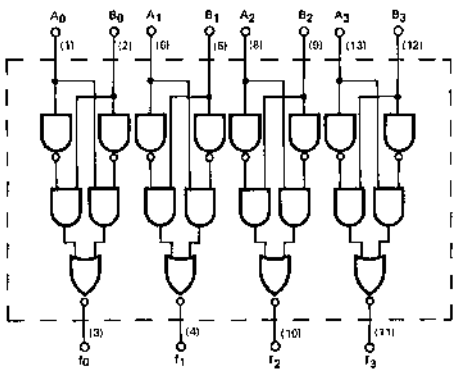
8241 QUAD EXCLUSIVE – OR



A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

8242 4-BIT DIGITAL COMPARATOR (OPEN COLLECTOR)



A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage) (8241)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUTS	
Output "1" Voltage	2.6	3.5		V	2.0	0.8	−800μA	7
Output "0" Voltage			0.4	V	2.0	2.0	16mA	8
Input "1" Current			80	μA	4.5	4.5V		11
Input "0" Current	-0.1		-3.2	mA	0.4	0.4		12
Power/Current Consumption		225/42.4	300/57.1	mW/mA				13
Output Short Circuit Current	-20		-70	mA			0V	6, 13
Input Voltage Rating								
A Input	5.5			V	10mA	0V		
B Input	5.5			V	0V	10mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$ (8241)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUTS	
Propagation Delay t_{on}		17	23	ns				9
Propagation Delay t_{off}		11	17	ns				9

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage) (8242)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUT	
Output "1" Leakage Current			25	μA	2.0	2.0		10
Output "0" Voltage			0.4	V	2.0	0.8	25mA	8
Input "1" Current			80	μA	4.5	4.5V		11
Inpute "0" Current	-0.1		-3.2	mA	0.4	0.4		12
Power/Current Consumption		170/32	260/47.5	mW/mA	0.4	0.4		13
Input Voltage Rating								
A Input	5.5			V	10mA	0V		
B Input	5.5			V	0V	10mA		10

$T_A = 25°C$ and $V_{CC} = 5.0V$ (8242)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			INPUTS
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUTS	
Inverting Path t_{on}		12	20	ns				
Inverting Path t_{off}		14	23	ns				
Non-Inverting Path t_{on}		14	21	ns				9
Non-Inverting Path t_{off}		20	28	ns				

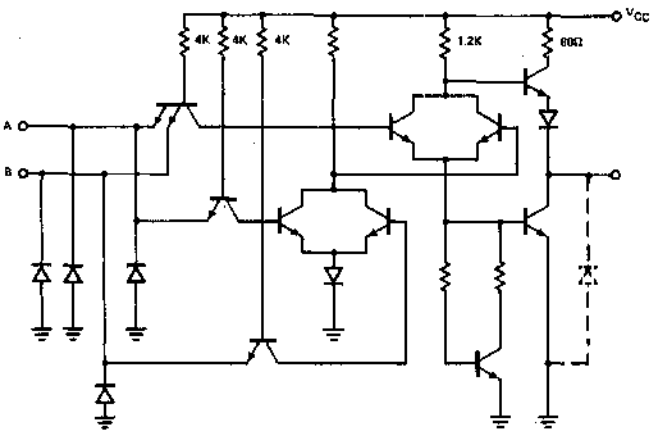
Propagation Delay

NOTES:

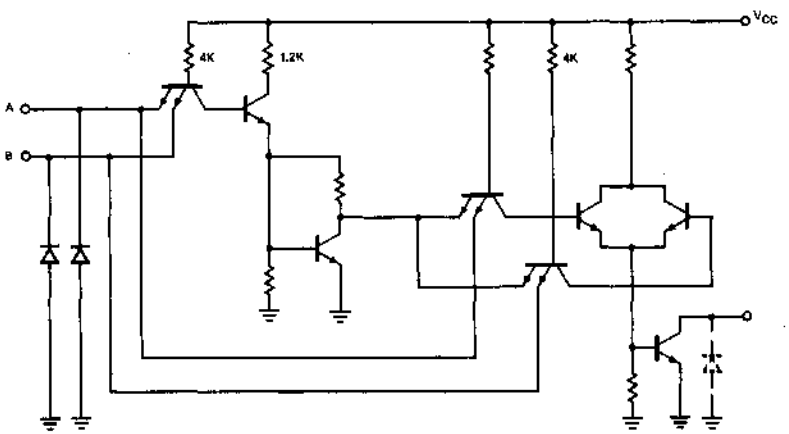
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current-limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Not more than one output should be shorted at a time.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure and waveforms.
10. Connect an external 1K ±1% resistor from V_{CC} to the output terminal for this test.
11. A and B are tested separately. When A is 4.5V, B is 0V, and vice versa.
12. A and B are tested separately. When A is 0.4V, B is 5.25V, and vice versa.
13. V_{CC} = 5.25V.

SCHEMATIC DIAGRAMS

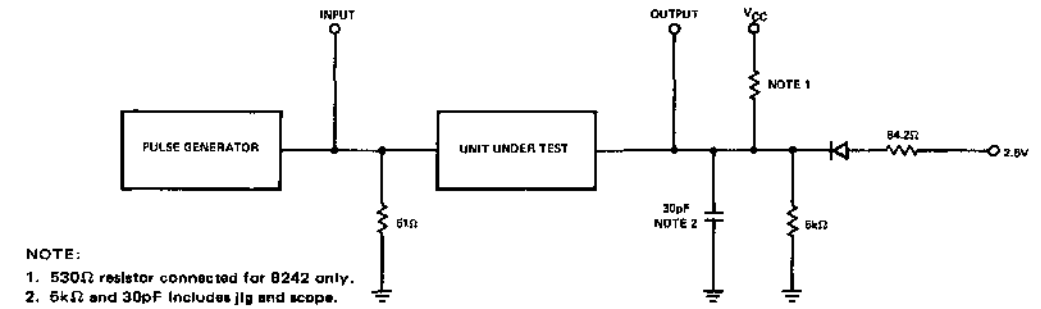
8241



8242 (OPEN COLLECTOR)



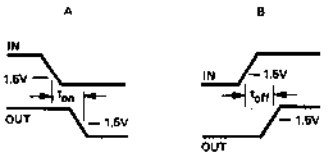
AC TEST FIGURE AND WAVEFORMS



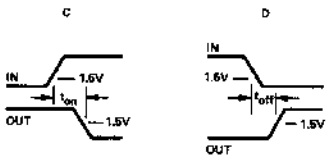
NOTE:
1. 530Ω resistor connected for 8242 only.
2. 5kΩ and 30pF includes jig and scope.

PROPAGATION DELAY WAVEFORMS

NON-INVERTING PATHS

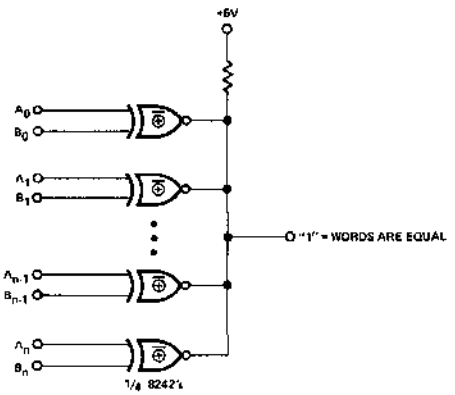


INVERTING PATHS

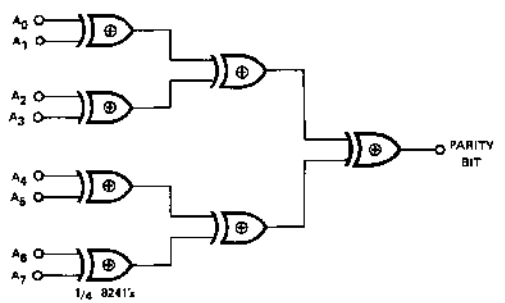


TYPICAL APPLICATIONS

EQUALITY GATE USED FOR COMPARISON



PARITY GENERATOR/TESTER



DESCRIPTION

The 8243 8-Bit Position Scaler is an MSI array of approximately 70 gate complexity. The primary function of the 8243 is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

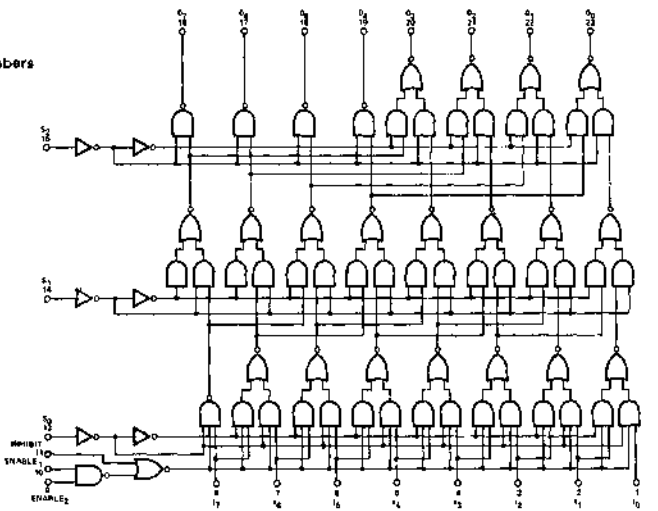
The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0, I_1 to O_1, I_2 to O_2, etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_{n-1}). See truth table for other shift codes.

The 8243's advantages over shift registers are the speed of operation and lower complexity of external logic required to effect a scale function. The speed of the 8243 Scaler is a function of gate propogation delays—the speed of equivalent shift registers is the time for clock periods plus the propagation delay to effect a scale function.

The 8243 is provided with open collector outputs to provide expansion to larger scaling functions. Data input logic zero loading is reduced to less than −100μA when the unit is disabled.

LOGIC DIAGRAM AND TRUTH TABLE

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers



NOTE: All inputs have diode clamps.

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$
0	1	1	0	0	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1
0	1	0	1	0	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1
0	1	1	1	0	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1
0	1	0	0	1	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1
0	1	1	0	1	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1	1
0	1	0	1	1	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1	1	1
0	1	1	1	1	$\overline{I}_7$	1	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	1	1	1	1	1	1	1	1

X Indicates either logic "1" or logic "0" may be present.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	I_n	S_0	S_1	S_2	ENABLE 1&2	INHIBIT	OUTPUTS	
"1" Output Leakage Current			150	μA	0.8V	*	*	*	2.0V	0.8V		7
"0" Output Voltage			0.4	V	2.0V	*	*	*	2.0V	0.8V	12.8mA	7
"0" Input Current												
Data In (Disabled)			-100	μA	0.4V				0.8V	2.0V		
Data In (Enabled)	-0.1		-1.6	mA	0.4V	0.8V			2.0V	0.8V		
Select S_n	-0.1		-1.6	mA		0.4V	0.4V	0.4V				
Inhibit	-0.1		-1.6	mA					0.4V	0.4V		
Enable 1 & 2	-0.1		-1.6	mA					0.4V	4.5V		11
"1" Input Current												
Data In			80	μA	4.5V	2.0V				2.0V		
Select S_n			40	μA		4.5V	4.5V	4.5V				
Inhibit			40	μA					2.0V	4.5V		
Enable 1 & 2			40	μA					4.5V			12

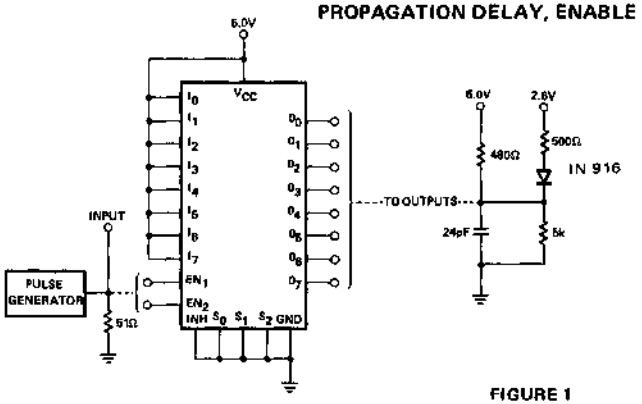
$T_A = 25°C$ and $V_{CC} = 5.0V$

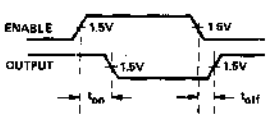
CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	I_n	S_0	S_1	S_2	ENABLE 1&2	INHIBIT	OUTPUTS	
Propagation Delay												
Data In		20	32	ns								9, 10
Select S_n		30	40	ns								
Inhibit		25	35	ns								
Enable 1 & 2		30	45	ns								
Power/Current		315/	500/	mW/								13
Consumption		60	75.2	mA								
Input Voltage Rating	5.5				10mA	10mA	10mA	10mA	10mA	10mA		

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
8. Manufacturer reserves the right to make design and process changes and improvements.
9. Refer to AC Test figures.
10. I_n "0" threshold 0.7 volts for S8243.
11. Input under test at 0.4V, other Enable Input tied to V_{CC}.
12. Input under test at 4.5V, other Enable Input, 0 volts.
13. $V_{CC} = 5.25V$.

AC TEST FIGURES AND WAVEFORMS

PROPAGATION DELAY, ENABLE TO OUTPUT





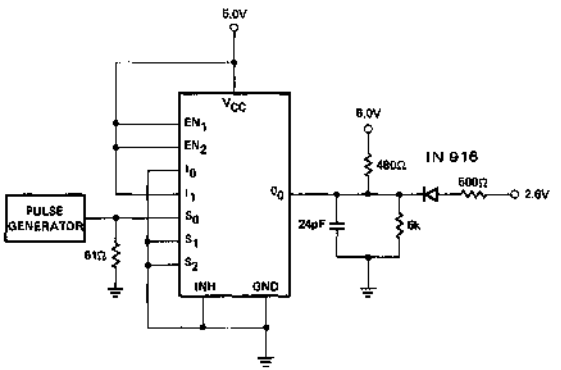
INPUT PULSE:
Amplitude = 2.8V
PW = 100ns @ 50% Points
PRR = 5MHz
tr = tf = 6ns (10% to 90% Points)

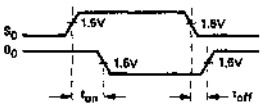
NOTE:
$Enable_1$ with $Enable_2$ at V_{CC} or
$Enable_2$ with $Enable_1$ at V_{CC}.

FIGURE 1

AC TEST FIGURES AND WAVEFORMS (Cont'd)

PROPAGATION DELAY, DATA INPUT TO DATA OUTPUT

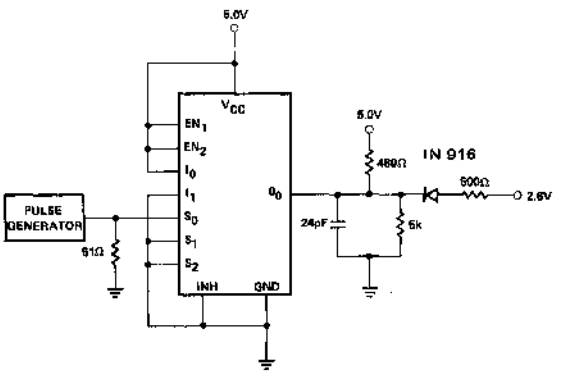


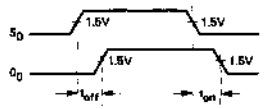


INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% Points
PRR = 6MHz
tr = tf = 5ns (10% to 90% Points)

FIGURE 2

PROPAGATION DELAY, DATA SELECT TO OUTPUT

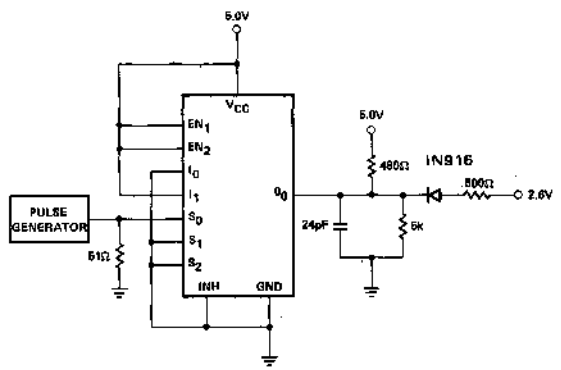


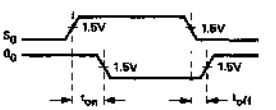


INPUT PULSE:
Amplitude = 2.6V
PRR = 6MHz
PW = 100ns @ 50% Points
tr = tf = 5ns (10% to 90% Points)

FIGURE 3

PROPAGATION DELAY, DATA SELECT TO OUTPUT



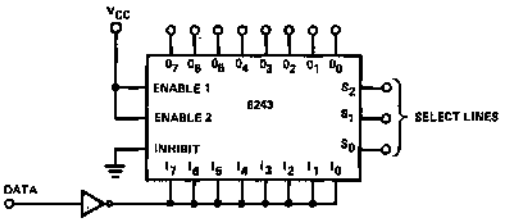


INPUT PULSE:
Amplitude = 2.6V
PRR = 6MHz
PW = 100ns @ 50% Points
tr = tf = 5ns (10% to 90% Points)

FIGURE 4

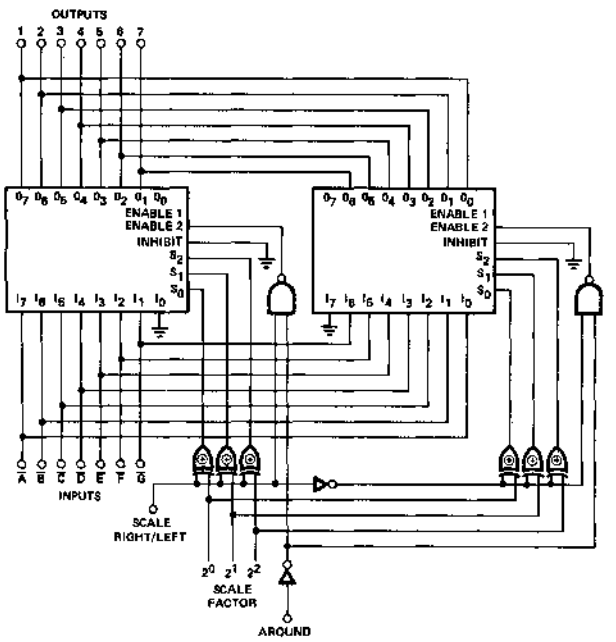
TYPICAL APPLICATIONS

ONE TO EIGHT LINE DEMULTIPLEXER



SCALE SELECT	3 BIT BINARY CODE			OUTPUTS							
	S_2	S_1	S_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	0	Data	Data	Data	Data	Data	Data	Data	Data
1	0	0	1	Data	Data	Data	Data	Data	Data	Data	1
2	0	1	0	Data	Data	Data	Data	Data	Data	1	1
3	0	1	1	Data	Data	Data	Data	Data	1	1	1
4	1	0	0	Data	Data	Data	Data	1	1	1	1
5	1	0	1	Data	Data	Data	1	1	1	1	1
6	1	1	0	Data	Data	1	1	1	1	1	1
7	1	1	1	Data	1	1	1	1	1	1	1

BI-DIRECTIONAL 8-POSITION SHIFTER



SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE RIGHT
1	1	A	B	C	D	E	F	
2	1	1	A	B	C	D	E	
3	1	1	1	A	B	C	D	
4	1	1	1	1	A	B	C	
5	1	1	1	1	1	A	B	SCALE = 0
6	1	1	1	1	1	1	A	AROUND = 0
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE LEFT
1	B	C	D	E	F	G	1	
2	C	D	E	F	G	1	1	
3	D	E	F	G	1	1	1	
4	E	F	G	1	1	1	1	
5	F	G	1	1	1	1	1	SCALE = 1
6	G	1	1	1	1	1	1	AROUND = 0
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE RIGHT & AROUND
1	G	A	B	C	D	E	F	
2	F	G	A	B	C	D	E	
3	E	F	G	A	B	C	D	
4	D	E	F	G	A	B	C	
5	C	D	E	F	G	A	B	SCALE = 0
6	B	C	D	E	F	G	A	AROUND = 1
7	A	B	C	D	E	F	G	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE LEFT & AROUND
1	B	C	D	E	F	G	A	
2	C	D	E	F	G	A	B	
3	D	E	F	G	A	B	C	
4	E	F	G	A	B	C	D	
5	F	G	A	B	C	D	E	SCALE = 1
6	G	A	B	C	D	E	F	AROUND = 1
7	A	B	C	D	E	F	G	

signetics

BINARY-TO-OCTAL DECODER
BCD-TO-DECIMAL DECODER

A,F,W PACKAGES FOR 8250
B,F,W PACKAGES FOR 8251

DIGITAL 8000 SERIES TTL/MSI

8250
8251
8252

DESCRIPTION

The 8250, 8251 and 8252 are gate arrays for decoding and logic conversion applications.

The 8250 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

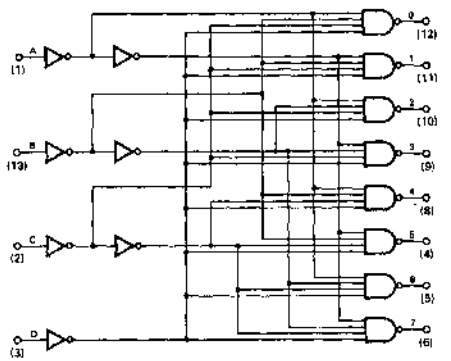
The 8251 and 8252 convert a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

The 8252 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs.

The selected output is a logic "0"

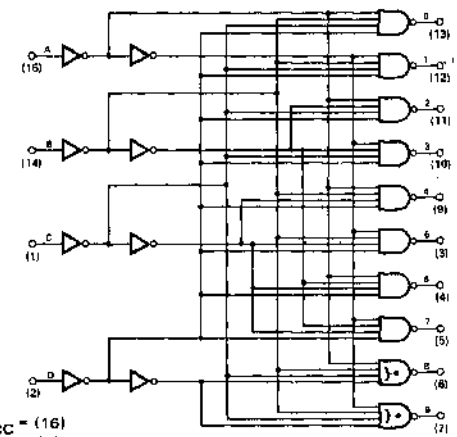
LOGIC DIAGRAMS

8250



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

8251/8252



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers for 16 Pin Dual-In-Line Package

*Connections made on 8252 only

TRUTH TABLE

INPUT STATE				OUTPUT STATES											
				8250								8251		8252	
A	B	C	D	0	1	2	3	4	5	6	7	8	9	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS						
"1" Output Voltage	2.6	3.5		V					-800μA	6, 10
"0" Output Voltage			0.4	V					16mA	7, 10
"1" Input Current										
A, B, C, D			40	μA	4.5V	4.5V	4.5V	4.5V		
"0" Input Current										
A, B, C (8250, 8251)	-0.1		-1.2	mA	0.4V	0.4V	0.4V			
A, B, C, D (8252)	-0.1		-1.6	mA	0.4V	0.4V	0.4V	0.4V		
D (8251 Only)	-0.1		-1.2	mA				0.4V		
D (8250 Only)	-0.1		-1.0	mA				0.4V		

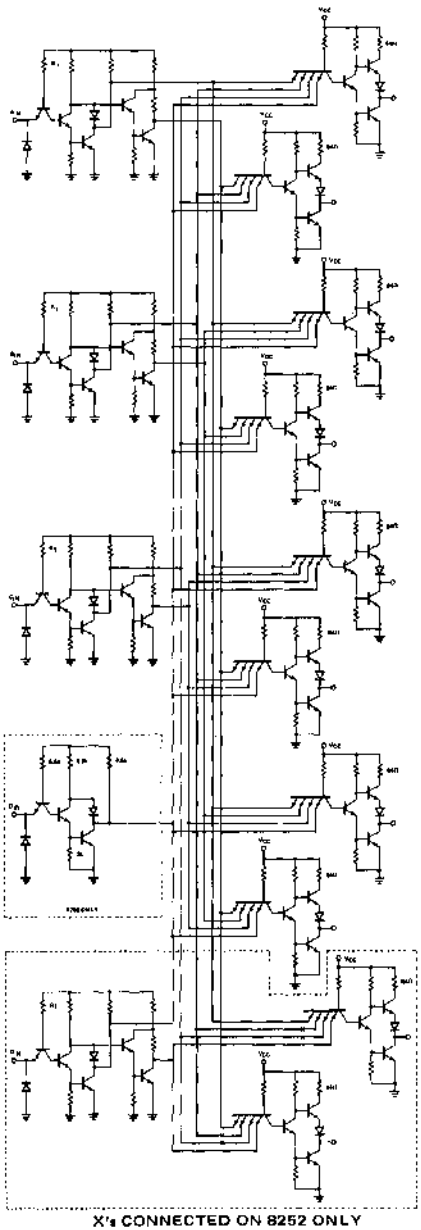
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS						
Turn-on Delay t_{on}		20	35	ns						8
Turn-off Delay t_{off}		20	35	ns						8
Power/Current Consumption										
(8251 Only)			135/25.7	mW/mA	5.25V	5.25V	5.25V	0V		11
(8250 Only)			125/23.8	mW/mA	5.25V	5.25V	5.25V	0V		11
Input Voltage Rating	5.5			V	10mA	10mA	10mA	10mA		
Output Short Circuit Current										
Outputs 1 thru 9	-10		-55	mA	0V	0V	0V	0V	0V	9, 11
Output 0	-10		-55	mA	5.0V	0V	0V	0V	0V	9, 11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0"
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures and waveforms.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Inputs for "1" and "0" output voltage test is per TRUTH table with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. Not more than one output should be shorted at a time.
12. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS

TURN-ON DELAY (t_{on})

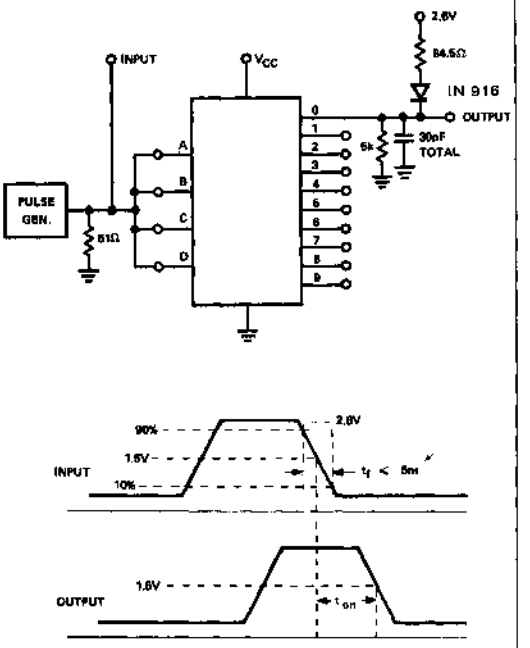


FIGURE 1

TURN-OFF DELAY (t_{off})

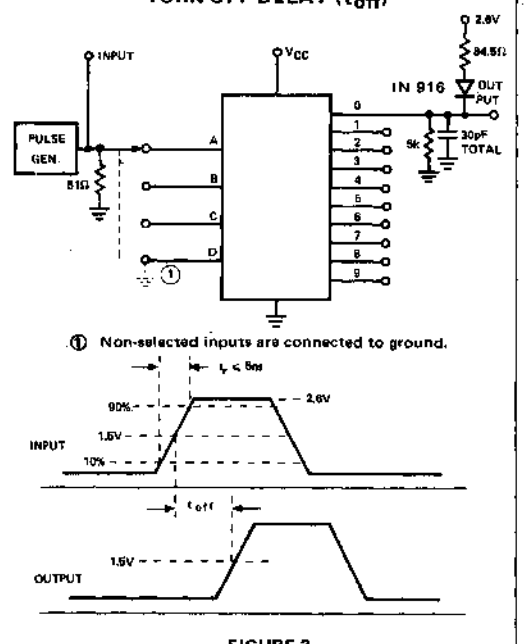
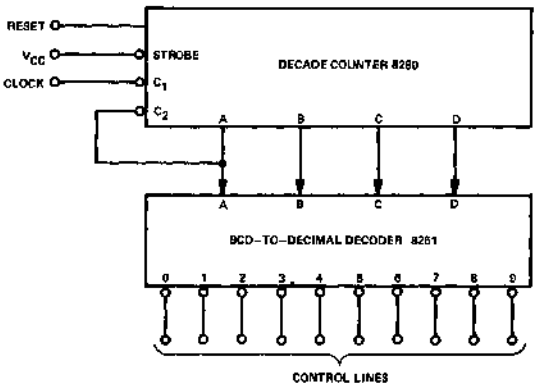


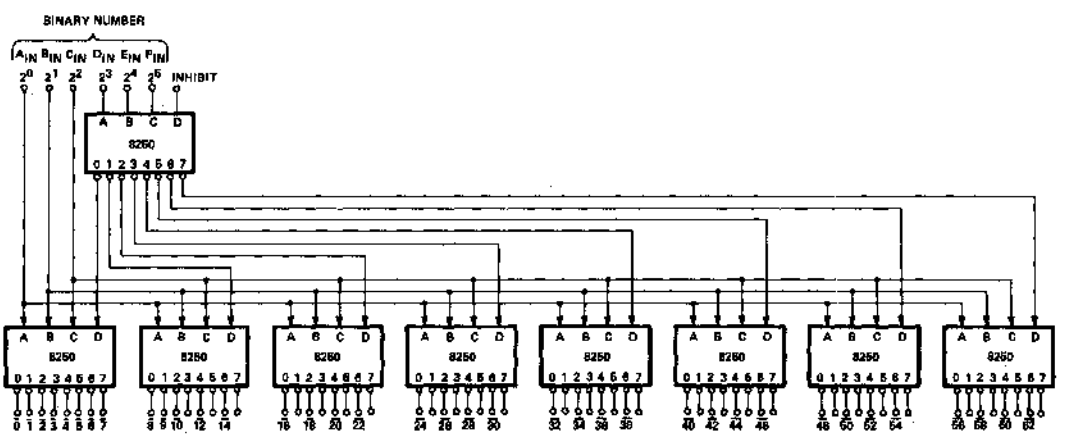
FIGURE 2

TYPICAL APPLICATIONS

ONE-OF-10 DECODER



ONE-OF-64 DECODER



DESCRIPTION

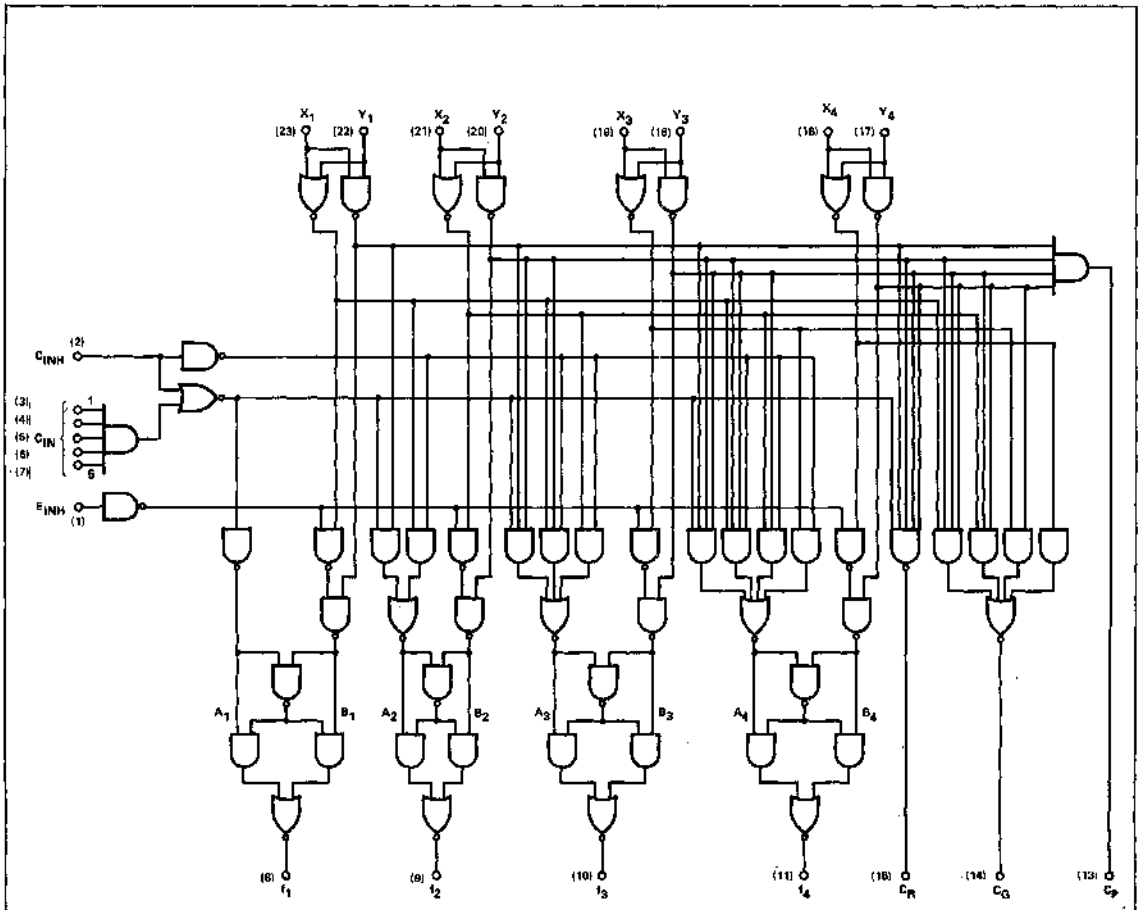
The 8260 Arithmetic Logic Element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

As a four-bit adder, the 8260 permits high speed parallel addition of four sets of data and features both simultaneous addition on a character to character and on a bit to bit basis within the package.

When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

The carry-outs available are: Internally Generated (C_G); Propagated (C_p); and Ripple (C_R). This gives the 8260 complete flexibility when used in Ripple Carry or Anticipated Carry Adder Systems.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (12)
( ) = Denotes Pin Numbers
A and B refer to Functional Block Diagram on page 54.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					OUTPUT TERMINALS				NOTES
					INPUT TERMINALS									
	MIN.	TYP.	MAX.	UNITS	X_n	Y_n	C_{IN}	C_{INH}	E_{INH}	C_p	C_G	C_R	f_n	
"1" Output Voltage	2.6	3.5		V	2.0	2.0	2.0	2.0	2.0		-800 µA	-800 µA	-800 µA	1
"0" Output Voltage														
f_n, C_G and C_R			0.4	V	0.8	0.8	0.8	0.8	0.8		9.6	9.6	9.6	2
C_p			0.4	V	2.0	2.0	2.0	2.0	2.0	16 mA	mA	mA	mA	2
"0" Input Current														
X_n and C_{INH}	-0.1		-3.2	mA	0.4	5.25		0.4						
Y_n	-0.1		-3.2	mA	5.25	0.4								
E_{INH} & C_{IN1} through C_{IN5}	-0.1		-1.6	mA			0.4		0.4					3
"1" Input Current														
X_n and C_{INH}			80	µA	4.5	0V		4.5						
Y_n			80	µA	0V	4.5								
E_{INH} & C_{IN1} through C_{IN5}			40	µA			4.5		4.5					4
Input Voltage Rating														
X_n and C_{INH}	5.5			V	10mA	0V		10mA						
Y_n	5.5			V	0V	10mA								
E_{INH} & C_{IN1} through C_{IN5}	5.5			V			10mA		10mA					4
Power/Current Consumption			400/ 76.2	600/ 114.1	mW/ mA									11

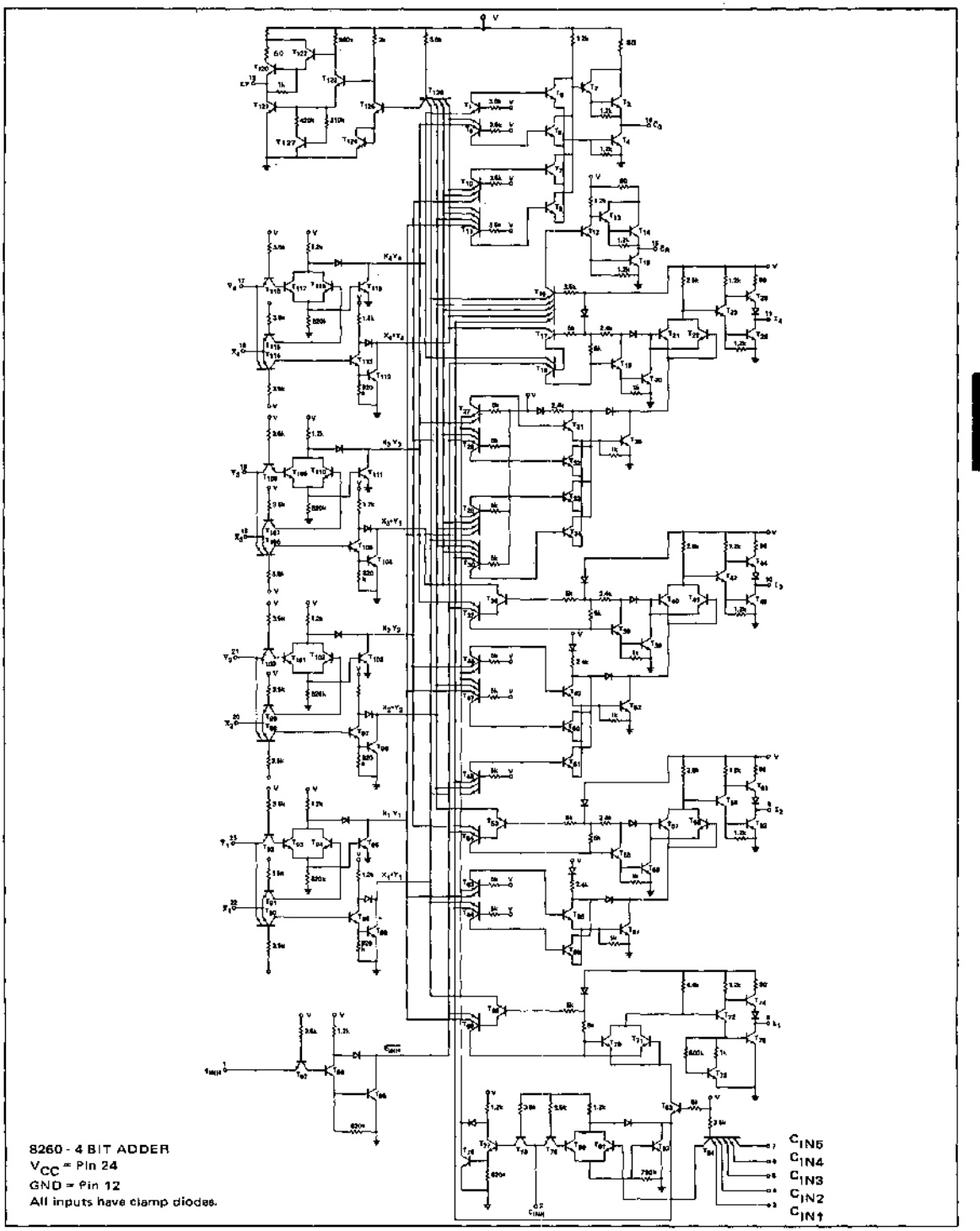
$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					OUTPUT TERMINALS				NOTES
					INPUT TERMINALS									
	MIN.	TYP.	MAX.	UNITS	X_n	Y_n	C_{IN}	C_{INH}	E_{INH}	C_p	C_G	C_R	f_n	
Propagation Delay														
X_n, Y_n and C_{IN} to C_R		14	20	ns										12
X_n and Y_n to Cp and C_G		14	20	ns										12
X_n and Y_n to f_n		24	33	ns										12
C_{IN} to f_n		14	22	ns										12
Output Short Circuit Current														
f_n, C_G and C_R	-20		-70	mA	5.0	5.0	5.0	5.0	5.0		0V	0V	0V	10, 11
Cp	-30		-90	mA	0V					0V				10, 11

NOTES:

1. Output source current is supplied through a resistor to ground.
2. Output sink current is supplied through a resistor to V_{CC}.
3. When testing for separate C_{IN} inputs, tie the remaining C_{IN} inputs to V_{CC}.
4. When testing for separate C_{IN} inputs, tie the remaining C_{IN} inputs to ground.
5. Keep unused inputs tied to V_{CC} unless otherwise specified.
6. All voltage measurements are referenced to the ground terminal.
7. Positive current flow is defined as into the terminal referenced.
8. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
9. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
10. Not more than one output should be shorted at a time.
11. $V_{CC} = 5.25V$.
12. Refer to AC test figure and waveforms.

SCHEMATIC DIAGRAM

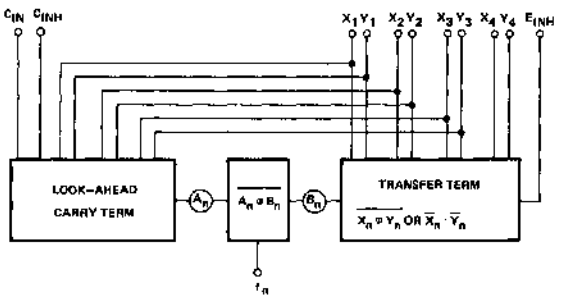


MODE OF OPERATION

INPUTS	Least Significant C_{IN} Inputs to be *	CONTROLS C_{INH}	CONTROLS E_{INH}	f	
X_n, Y_n	0	0	0	Σ_n	Add
	0	0	1	- -	Not Used
	0	1	0	$X_nY_n + \overline{X}_n\overline{Y}_n$	Coincidence
	0	1	1	X_nY_n	AND
$\overline{X}_n$, $\overline{Y}_n$	1	0	0	$\overline{\Sigma}_n$	Add
	1	0	1	- - -	Not Used
	1	1	0	$\overline{X}_n\overline{Y}_n + X_nY_n$	Coincidence
	1	1	1	$\overline{X}_n\overline{Y}_n$	AND

*Least significant of a "Multiple Package" adder system.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

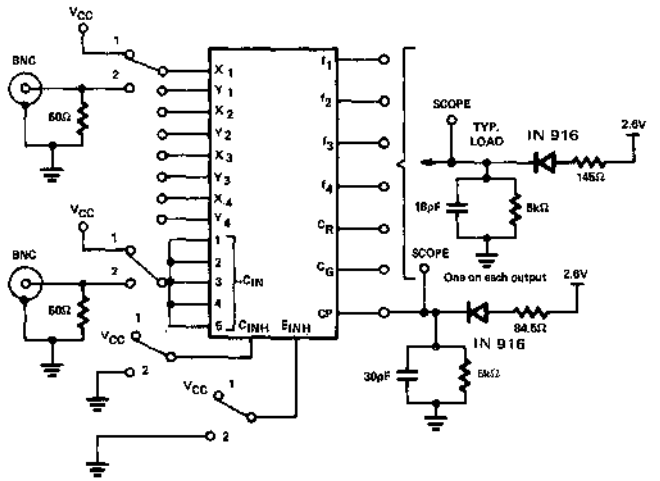
$C_{INH} = 1 \longrightarrow A_n = 1$
$C_{INH} = 0 \longrightarrow A_n =$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

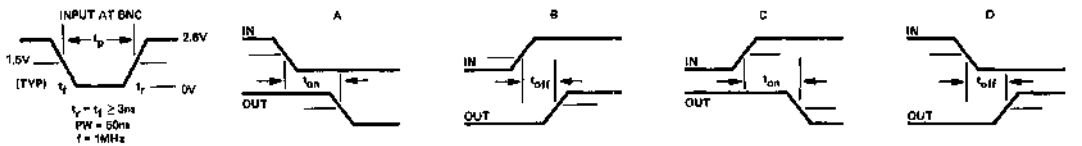
A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

AC TEST FIGURE AND WAVEFORMS



NOTE: Scope terminals to be ≤ ¼" from Package Pins.



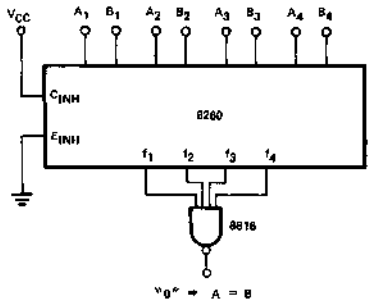
STEP NO.	DELAY FROM TO	DRIVEN INPUTS	SWITCH POSITION: OTHER INPUTS											WAVEFORM TYPE
			X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	C_{IN}	E_{INH}	C_{INH}	
1	X_n to C_R or X_n to C_P	2	2	1	2	1	2	1	2	1	2	2	2	A, B C, D
2	Y_n to C_R or Y_n to C_P	2	1	2	1	2	1	2	1	2	2	2	2	A, B C, D
3	X_n, Y_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	A, B
4	C_{IN} to C_R	2	2	2	2	2	2	2	2	2	2	2	2	A, B
5	C_{IN} to f_n	2	1	2	1	2	1	2	1	2	2	2	2	C, D

TYPICAL APPLICATIONS

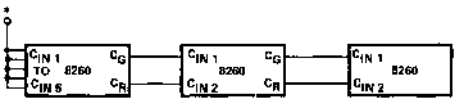
The 8260 contains the control logic necessary to allow operation as a general purpose arithmetic logic device. Below, the internal carries are inhibited to effect Exclusive-NOR or coincidence operation. The 8260 may also be operated as four independent AND gates to implement masking and similar requirements of micro-programming.

The Ripple Adder System is the simplest but also the slowest application of the 8260. The typical total addition time (input to sum output for 12-bit ripple adder is 42ns).

FOUR-BIT COMPARATOR



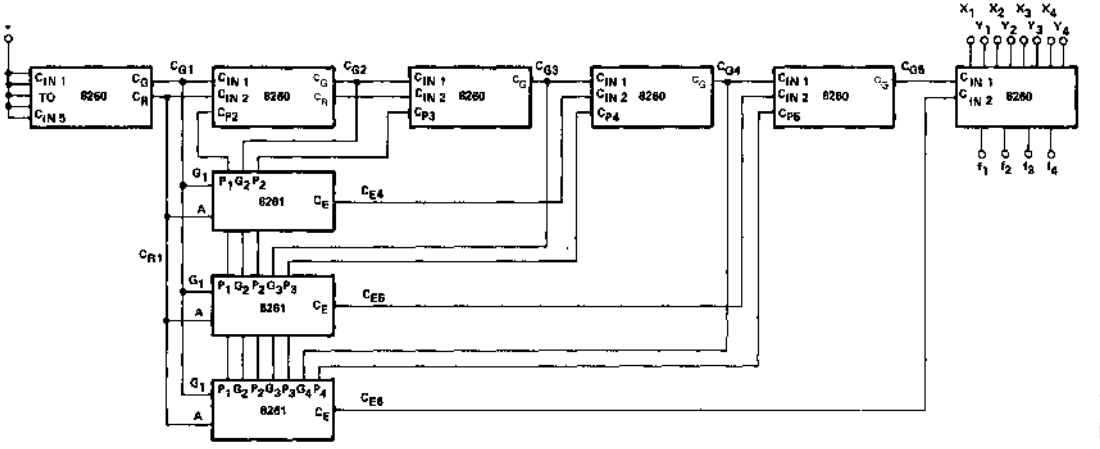
RIPPLE ADDER SYSTEM



*Tied to V_{CC} if Not-True Inputs Are Used, Otherwise to Ground.

The Fast Adder System provides complete carry look-ahead addition for words to 24 bits in length and is the fastest application of the 8260 units. The typical total addition time for a 24 bit fast adder is 42ns.

24-BIT FAST ADDER SYSTEM

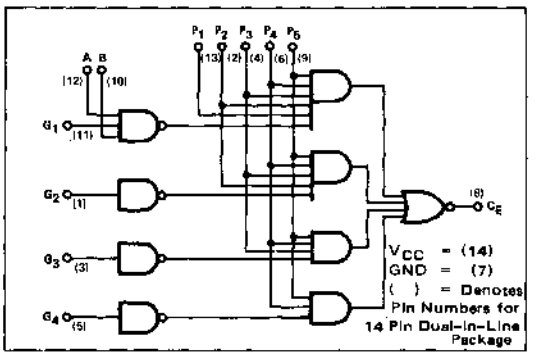


*Tied to V_{CC} if Not-True Inputs Are Used, Otherwise to Ground.

DESCRIPTION

The 8261 Fast Carry Extender is a monolithic gate array designed specifically to be used in conjunction with the 8260 Arithmetic Logic element. A 8260/8261 combination facilitates the implementation of the look-ahead technique in adder systems, thus considerably improving propagation times. The circuit structure of this array is of the familiar TTL type.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					DRIVEN INPUTS		OTHER INPUTS			
	MIN.	TYP.	MAX.	UNITS	G,A,B	P	G,A,B	P		
"1" Output Voltage	2.6	3.5		V	2.0V				-800μA	6
"0" Output Voltage			0.4	V	0.8V		4.75V	4.75V	9.6mA	7
"1" Input Current										
G Input			40	μA	4.5V		A = 0V			
A and B Inputs			40	μA	4.5V		G_1 = 0V			
P_1 Input			40	μA		4.5V		0V		
P_2 Input			80	μA		4.5V		0V		
P_3 Input			120	μA		4.5V		0V		
P_4 and P_5 Inputs			160	μA		4.5V		0V		
"0" Input Current										
G, A and B			-1.6	mA	0.4V			5.25V		
P_1 Input			-1.6	mA		0.4V	0V	5.25V		
P_2 Input			-3.2	mA		0.4V	0V	5.25V		
P_3 Input			-4.8	mA		0.4V	0V	5.25V		
P_4 and P_5 Inputs			-6.4	mA		0.4V	0V	5.25V		
Power/Current Consumption		115/22	158/30	mW/mA			5.25V	0V		10
Input Voltage Rating	5.5			V	10mA	10mA	0V	0V		

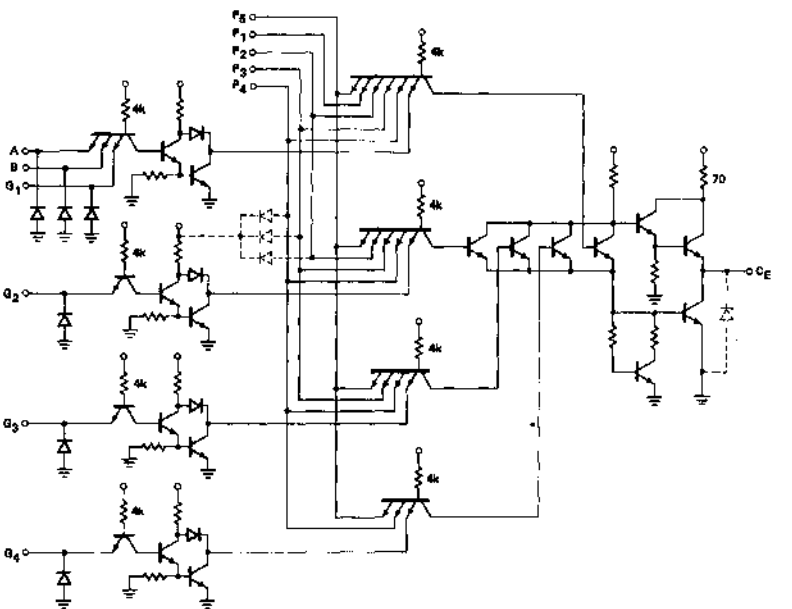
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					DRIVEN INPUTS		OTHER INPUTS			
	MIN.	TYP.	MAX.	UNITS	G,A,B	P	G,A,B	P		
Turn-on Delay, t_{on}										
G to C_E		16	25	ns						8
P to C_E		13	25	ns						8
Turn-off Delay, t_{off}										
G to C_E		16	23	ns						8
P to C_E		9	15	ns						8
Output Short Circuit Current	-20		-70	mA	5.0V	0V			0V	10

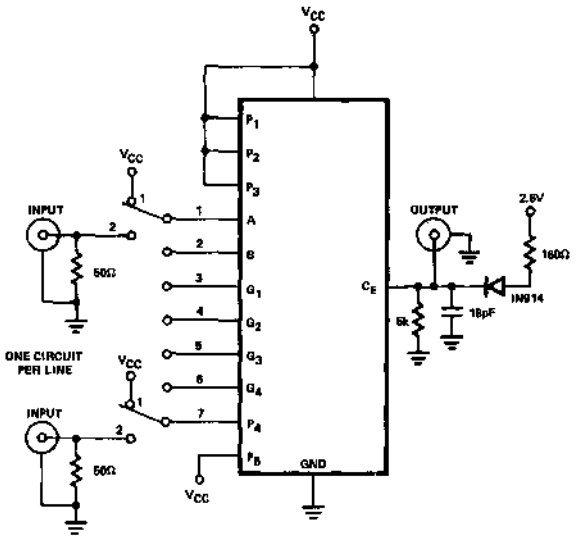
NOTES:

1. All voltage and current measurements are referenced to the ground terminal. Input terminals not specifically referenced are tied to V_{CC}.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Input "0" thresholds for P_1 through P_5 inputs are guaranteed to be 0.7 volts.
10. V_{CC} = 5.25V.

SCHEMATIC DIAGRAM

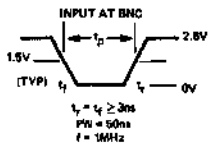


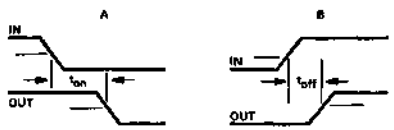
AC TEST FIGURE AND WAVEFORMS

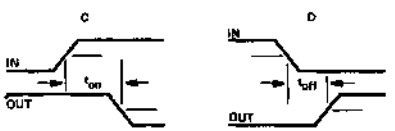


TEST TABLE

PIN DESIGNATION	INPUT A	B	G_1	G_2	G_3	G_4	P_4	WAVEFORM
1	PULSE	1	1	1	1	1	1	A,B
2	1	PULSE	1	1	1	1	1	
3	1	1	PULSE	1	1	1	1	
4	1	1	1	PULSE	1	1	1	
5	1	1	1	1	PULSE	1	1	
6	1	1	1	1	1	PULSE	1	
7	2	2	2	2	2	2	PULSE	C,D



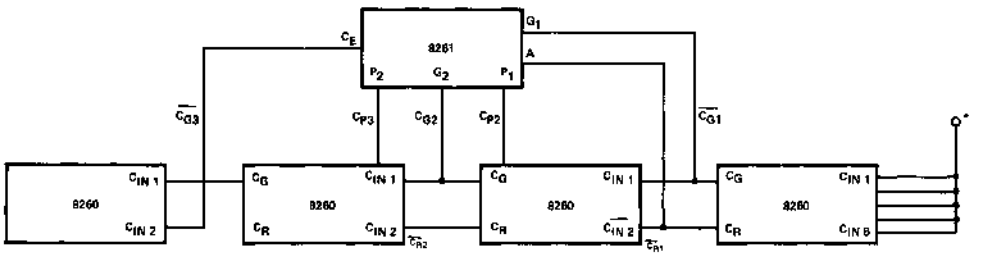




NOTES:

A. Position 1 on all switches provides a logical "1". Position 2 on all switches provides a logical "0" when input signal is not present.
B. All measurements are made at 1.5 volts level.

TYPICAL APPLICATION



16 BIT, T_A = 42ns, typical Fast Adder System (5 packages)
*Tied to V_{CC} if not-true inputs are used, otherwise to ground. Unused 8261 pins should be tied to V_{CC}.

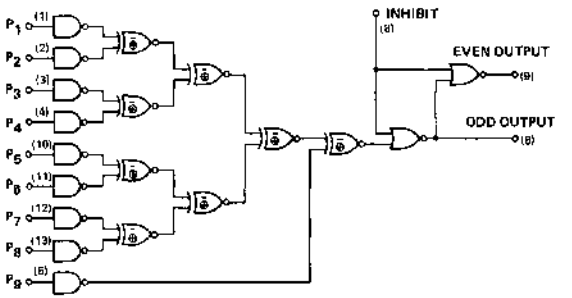
DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for
14-Pin Dual-in-Line Package

LOGIC EQUATIONS:

Odd =

$$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

Even =

$$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$$

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT UNDER TEST			
"1" Output Voltage								
Even	2.6	3.5		V	0V	.8V	-800μA	6
Odd	2.6	3.5		V	2.0V	.8V	-800μA	6
"0" Output Voltage								
Even			0.40	V	2.0V	.8V	16mA	7
Odd			0.40	V	0V	.8V	16mA	7
"0" Input Current								
Data Inputs	-0.1		-1.6	mA	0.4V			
Inhibit	-0.1		-3.2	mA		0.4V		
"1" Input Current								
Data Inputs			80	μA	4.5V			
Inhibit			160	μA		4.5V		
Input Voltage Rating								
Data Inputs	5.5			V	10mA			
Inhibit	5.5			V		10mA		
Power/Current Consumption		300/57	370/70	mW/mA				9
Output Short Circuit Current								
Even	-20		-70	mA	0V	0V	0V	9, 10
Odd	-20		-70	mA	4.5V	0V	0V	9, 10

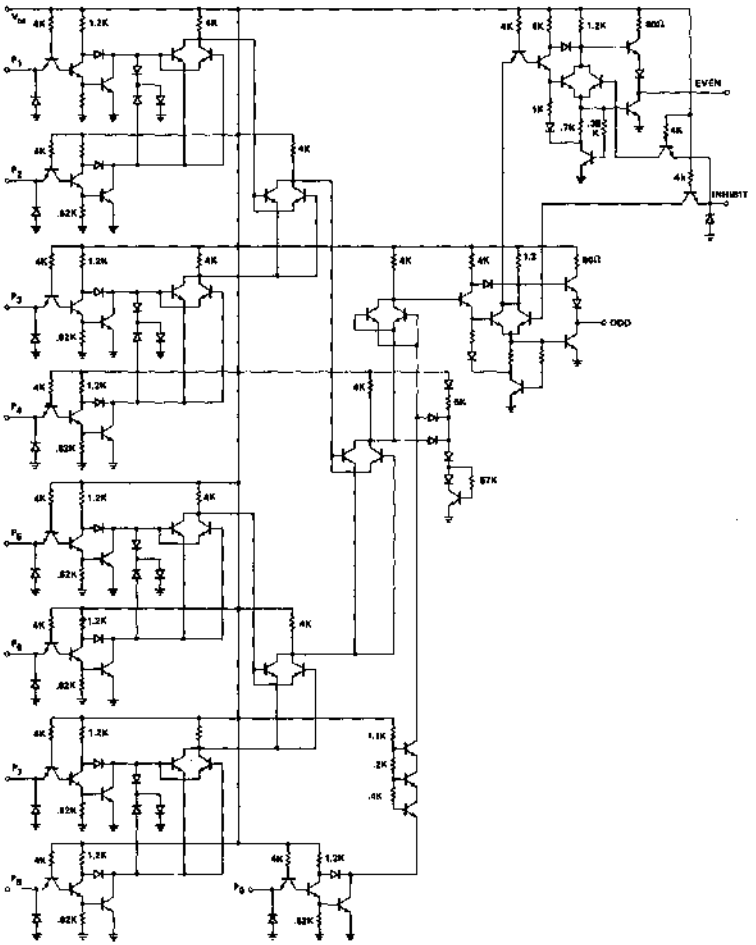
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN.	TYP.	MAX.	UNITS	UNDER TEST			
Turn-On Times								
$P_1 - P_8$ to Even		35	50	ns	Pulse			8
$P_1 - P_8$ to Odd		30	45	ns	Pulse			8
P_9 to Even		20	35	ns	Pulse			8
P_9 to Odd		15	30	ns	Pulse			8
Inhibit to Even		8	15	ns		Pulse		8
Inhibit to Odd		8	15	ns		Pulse		8
Turn-Off Times								
$P_1 - P_8$ to Even		38	55	ns	Pulse			8
$P_1 - P_8$ to Odd		32	45	ns	Pulse			8
P_9 to Even		23	40	ns	Pulse			8
P_9 to Odd		20	35	ns	Pulse			8
Inhibit to Even		10	18	ns		Pulse		8
Inhibit to Odd		10	18	ns		Pulse		8

NOTES:

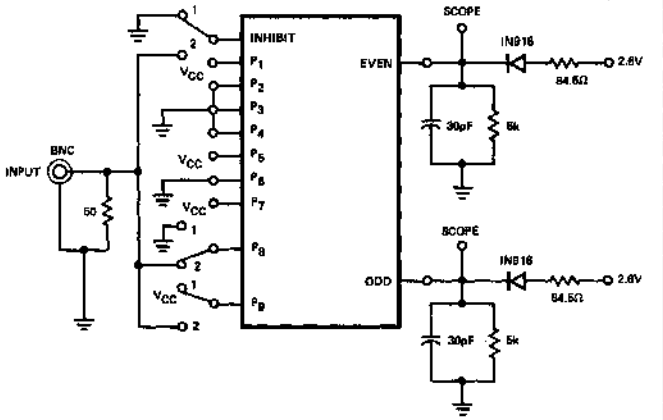
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. $V_{CC} = 5.25$ volts.
10. Not more than one output should be shorted at a time.

SCHEMATIC DIAGRAM

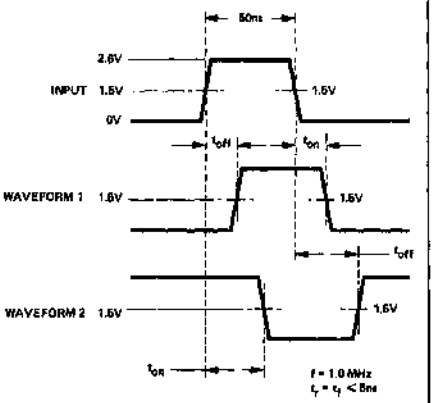


AC TEST FIGURE AND WAVEFORMS

8262 PARITY GENERATOR-CHECKER



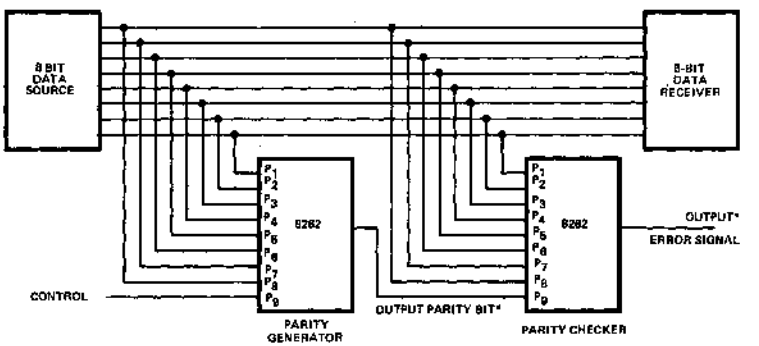
PULSE REQUIREMENTS



TRUTH TABLE

MEASURE DELAY FROM	SWITCH POSITION			WAVEFORM	
	INH	P_8	P_9	EVEN	ODD
P_8 to ODD	1	2	↑		1
P_9 to ODD	↑	↑	2		2
P_8 to EVEN	↑	2	↑	2	
P_9 to EVEN	↑	↑	2	1	
INH to EVEN	2	↑	1	2	

TYPICAL APPLICATIONS



*Output can be conditioned for odd or even parity.

An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.

An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.
The 8263 employs active output structures to effect minimum delays; the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

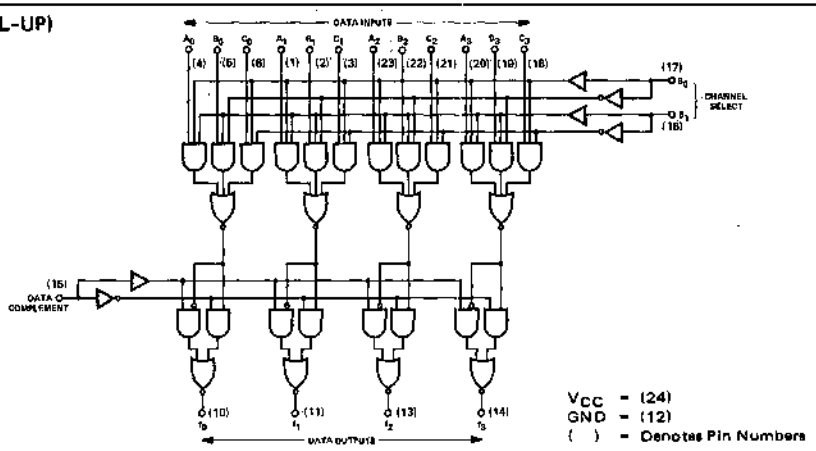
TRUTH TABLE

Data Input A_n B_n C_n	Channel Select S_0 S_1	Data Complement	Output Enable (8264)	Data Outputs
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	$\overline{A_n}$
x B_n x	0 1	1	1	$\overline{B_n}$
x x C_n	1 0	1	1	$\overline{C_n}$
x x x	0 0	1	1	1
x x x	x x	x	0	Z

X = Either State

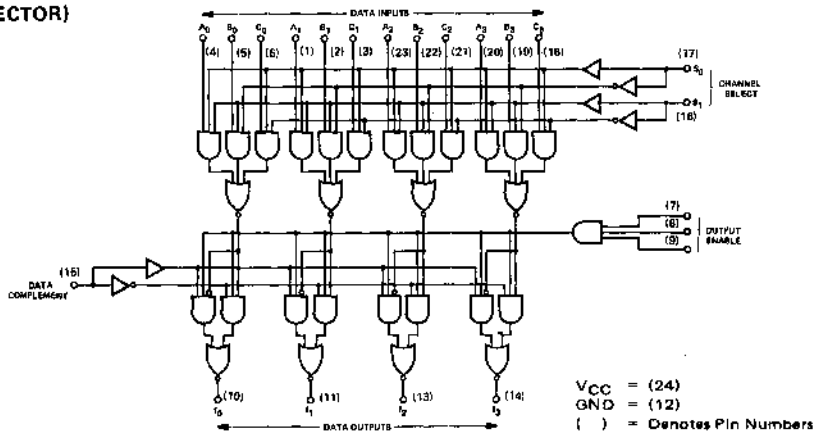
LOGIC DIAGRAMS

8263 (ACTIVE PULL-UP)



V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8264 (OPEN COLLECTOR)



V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	C_n	S_0	S_1	DATA COMP	OUTPUT ENABLE	OUTPUTS	
"1" Output Voltage (8263)	2.6	3.5		V	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V		-800μA	6
"1" Output Leakage Current (8264)			200	μA	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V	2.0V		8
"0" Output Voltage (8263)			0.4	V	0.8V	0.8V	0.8V	2.0V	2.0V	0.8V		9.6mA	7
"0" Output Voltage (8264)			0.4	V	0.8V							16.0mA	7
"0" Input Current													
A_n	-0.1		-1.6	mA	0.4V								
B_n	-0.1		-1.6	mA		0.4V		0.4V					
C_n	-0.1		-1.6	mA			0.4V		0.4V				
OE, DC	-0.1		-1.6	mA						0.4V	0.4V		
S_0, S_1	-0.1		-3.2	mA				0.4V	0.4V				
"1" Input Current													
A_n			40	μA	4.5V			0V	0V				
B_n			40	μA		4.5V			0V				
C_n			40	μA			4.5V	0V					
OE, DC			40	μA						4.5V	4.5V		
S_0, S_1			80	μA				4.5V	4.5V				

$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	C_n	S_0	S_1	DATA COMP	OUTPUT ENABLE	OUTPUTS	
Propagation Delay (8263)													
A_n to f_n		17	26	ns									10
S_0, S_1 to f_n		25	36	ns									10
DC to f_n		17	26	ns									10
Propagation Delay (8264)													
A_n to f_n		25	36	ns									10
S_0, S_1 to f_n		25	36	ns									10
DC to f_n		20	30	ns									10
OE to f_n		20	30	ns									10
Input Voltage Rating													
A_n	5.5			V	10mA			0V	0V				
B_n	5.5			V		10mA			0V				
C_n	5.5			V			10mA	0V					
S_0	5.5			V				10mA					
S_1	5.5			V					10mA				
DC	5.5			V						10mA			
OE	5.5			V							10mA		
Output Short Circuit Current (8263)	-20		-70	mA								0V	9, 11
Power/Current Consumption													9
(8263)		378/ 72	420/ 80	mW/ mA				0V					
(8264)		400/ 76	475/ 90.4	mW/ mA				0V					

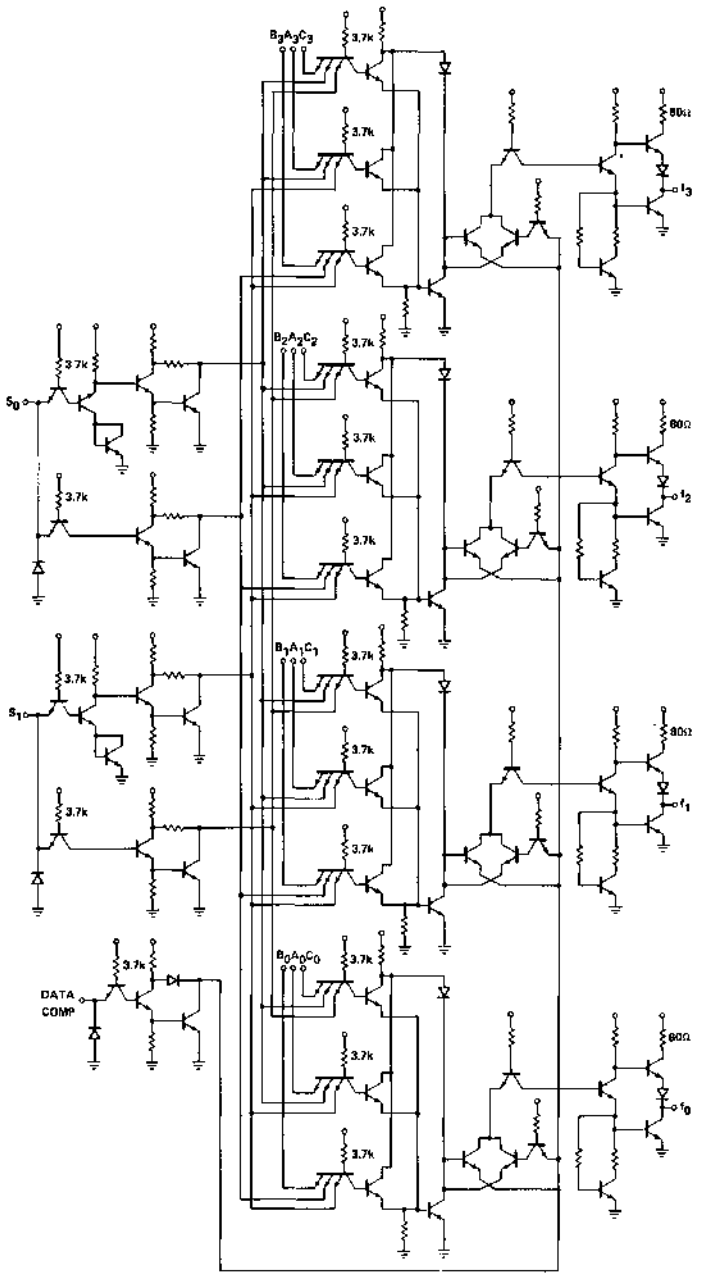
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
9. V_{CC} = 5.25V.
10. Refer to AC test figure.
11. Not more than one output should be shorted at a time.

7.

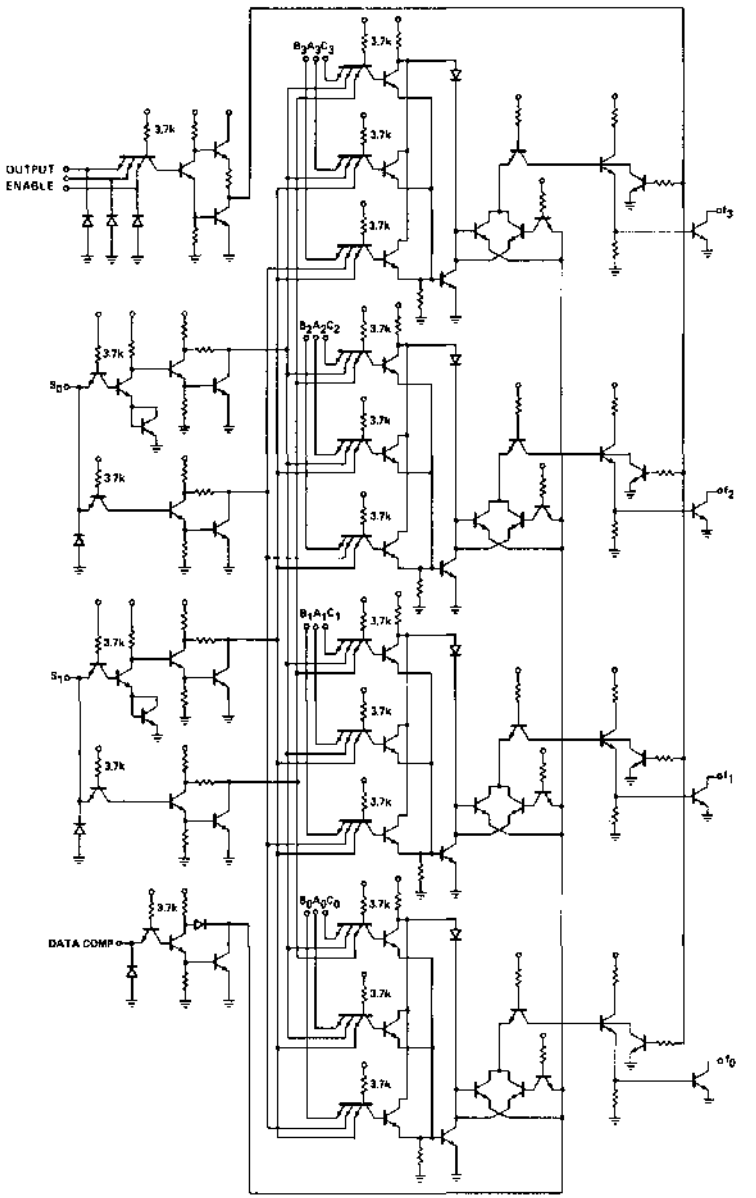
SCHEMATIC DIAGRAMS

8263



SCHEMATIC DIAGRAMS (Cont'd)

8264



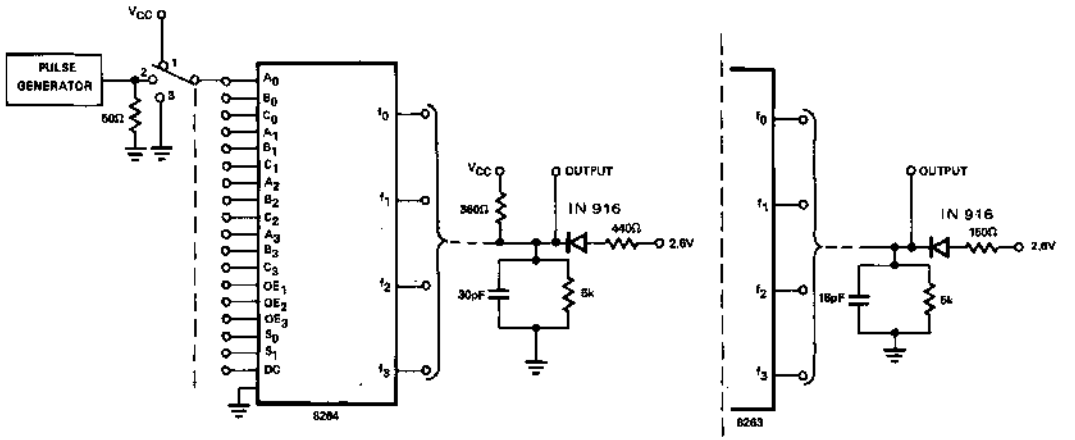
AC TESTING

Step No.	Delay From-To	Switching Positions																		Waveform Types
		Driven Inputs	Other Inputs																	
			A_0	B_0	C_0	A_1	B_1	C_1	A_2	B_2	C_2	A_3	B_3	C_3	OE	OE	OE	S_0	S_1	DC	
1	A_n to f_n	2	2	1	1	2	1	1	2	1	1	2	1	1	1	1	1	1	1	1	C, D
2	S_0 to f_n	2	3	1	1	3	1	1	3	1	1	3	1	1	1	1	1	2	1	1	A, B
3	S_0 to f_n	2	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	1	C, D
4	S_1 to f_n	2	1	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	C, D
5	DC to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	C, D
6	OE_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	*	*	*	1	1	1	C, D

NOTE: Step number 6 is for 8284 only.

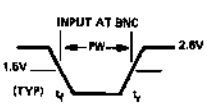
* Test one input at a time - others remain at "1".

AC TEST FIGURE AND WAVEFORMS

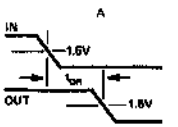


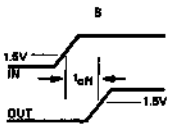
NOTE:
1. Scope terminals to be < 1½" from package pins.
2. Position 1 on switch provides a logical "1". Position 2 on switch provides pulse. Position 3 on switch provides a logical "0".
3. All measurements are made at 1.5V level.
4. See truth table for logical conditions.

NON-INVERTING PATHS

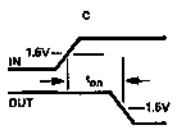


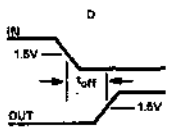
$t_r = t_f \leq 3ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz





INVERTING PATHS





TYPICAL APPLICATIONS

An approach to expanding the 8264 (bare collector output) is shown in Figure 1. The idea is to use common collectors with external pull-up resistors (one resistor for each of the four outputs) and make use of the output enable code.

As can be seen, the channel select lines are tied common, while a different enable code would be used to select a particular 8264. All non-selected 8264's have their outputs in the logic "1" condition, thus allowing the selected multiplexer to predominate.

Figure 2 illustrates a typical example using the 8263 (totem pole output) along with the 8281 (4-bit binary counter) and the 8270/71 (4-bit shift register), to implement a variable modulus counter. The 8270's act as a 3-register memory. The outputs of the 8270's are fed to the corresponding inputs of the 8263. Now there are three different presettable 4-bit words that can be chosen by the 8264. By alternating the channel select codes, the 8281 counter is preset with one of three words and produces an output whose repetition rate is dependent on the inputs from the multiplexer.

EXPANDING THE 8264

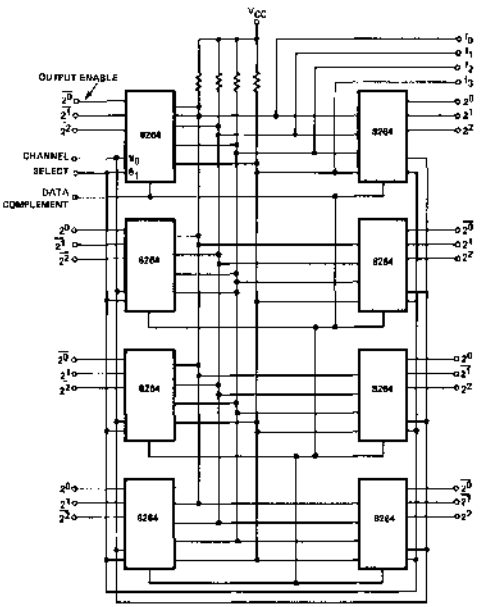


FIGURE 1

VARIABLE MODULUS COUNTER

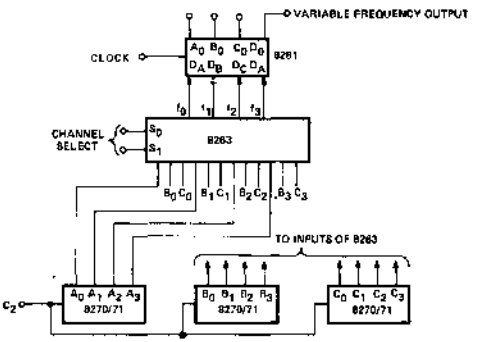


FIGURE 2

DESCRIPTION

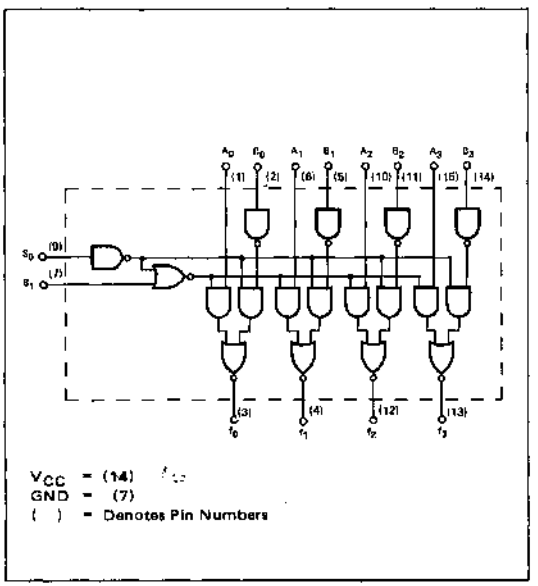
The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3), B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

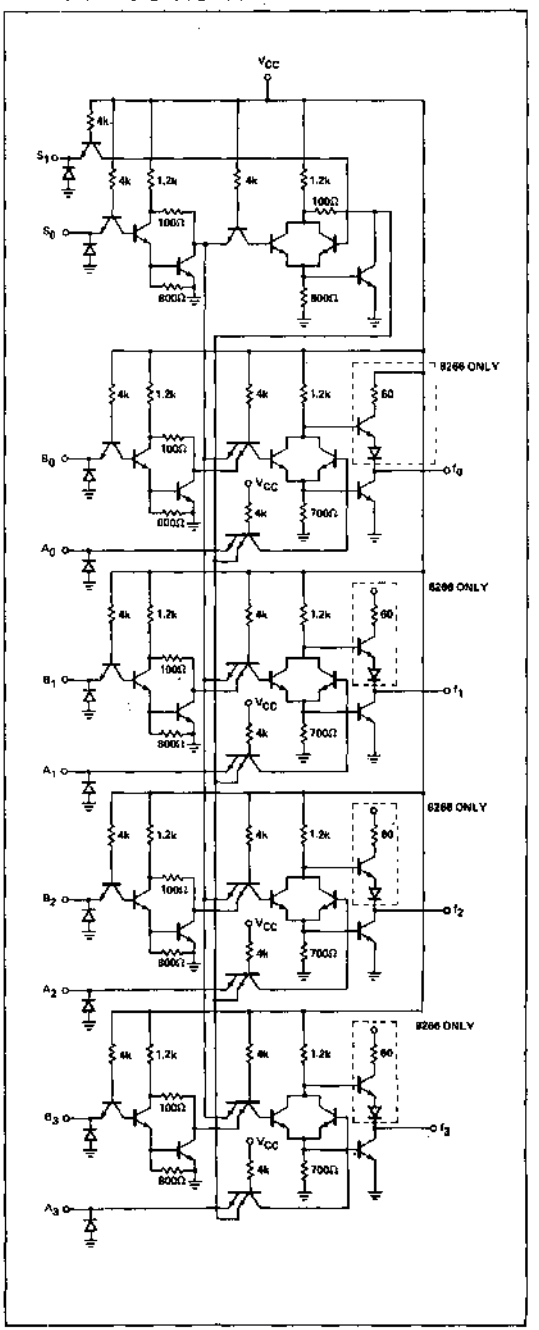
LOGIC DIAGRAM



TRUTH TABLE

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

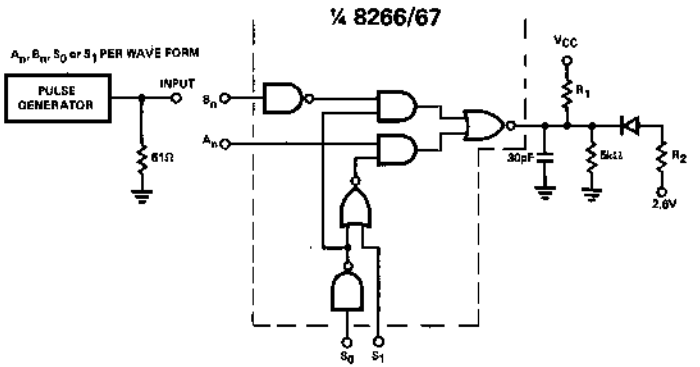
CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
"1" Output Voltage (8266)	2.6	3.5		V	0.8V	2.0V	0.8V	0.8V	-800μA	7
"0" Output Voltage			0.40	V	2.0V	2.0V	2.0V	0.8V	16mA	8
"1" Output Leakage Current (8267)			25	μA	0.6V	2.0V	2.0V	0.8V		10
"0" Input Current										
A_n, B_n	-0.1		-1.6	mA	0.4V	0.4V	0V	0V		
S_0, S_1	-0.1		-1.6	mA			0.4V	0.4V		
"1" Input Current										
A_n, B_n			40	μA	4.5V	4.5V		2.0V		
S_0, S_1			40	μA			4.5V	4.5V		
Input Voltage Rating										
S_0, A_n, B_n	5.5			V	10mA	10mA	10mA	2.0V		
S_1	5.5			V			2.0V	10mA		
Output Short Circuit Current (8266)	-20		-70	mA					0V	11, 12

T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
Propagation Delay (8266)										
S_0 to f_n (short path)		18	28	ns						9
S_0 to f_n (long path)		20	30	ns						9
A_n to f_n		13	20	ns						9
B_n, S_1 to f_n		14	25	ns						9
Propagation Delay (8267)										
S_0 to f_n		27	36	ns						9
A_n to f_n		15	20	ns						9
B_n, S_1 to f_n		21	28	ns						9
S_0 to f_n (short path)		18	28	ns						9
Power/Current Consumption		200/ 38.1	275/ 52.4	mW/ mA	4.5V	0V	4.5V	0V		12

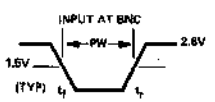
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. Connect an external 1k ± 1% resistor from V_{CC} to the output for this test.
11. Not more than one output should be shorted at a time.
12. V_{CC} = 5.25 volts.

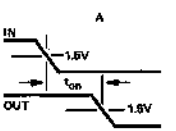
AC TEST FIGURE AND WAVEFORMS

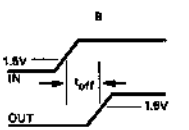


	8266	8267
R_1	∞	330Ω
R_2	84.5Ω	470Ω

NON-INVERTING PATHS

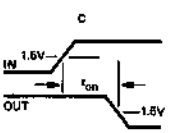


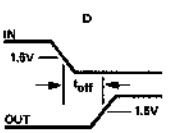




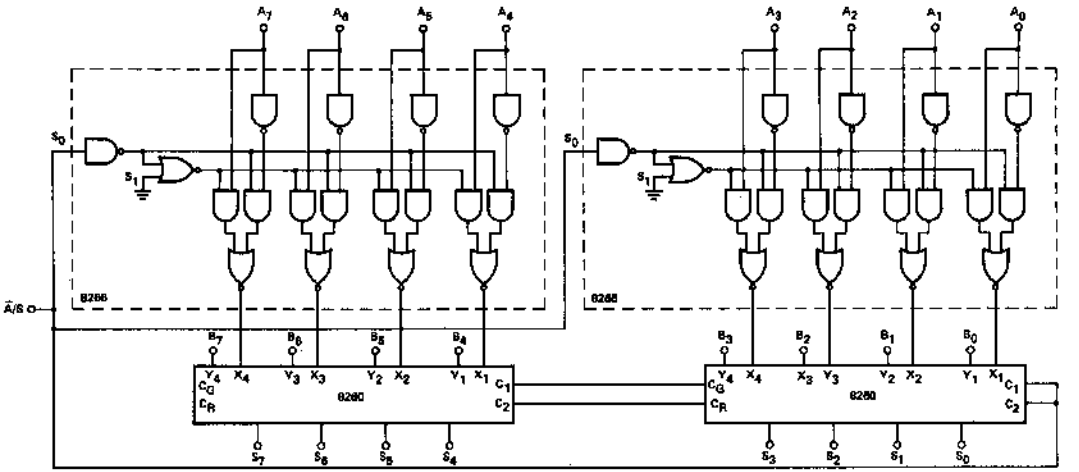
$t_r = t_f \leq 6ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz

INVERTING PATHS





TYPICAL APPLICATIONS



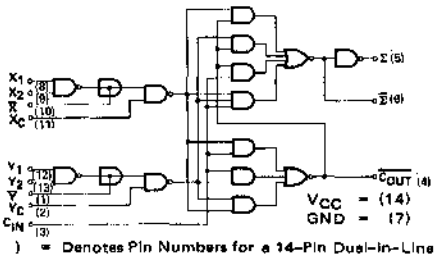
The 8266 can be used in conjunction with the 8260 (Look-Ahead Carry Adder) to form an adder-subtractor.

DESCRIPTION

The 8268 is a single-bit full adder with gated true and complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and an inverted carry output. By taking advantage of the unique true or inverted inputs and true or inverted outputs, parallel addition speed is greatly enhanced (by eliminating unnecessary inversions).

The device is designed for medium speed parallel and serial adder systems.

LOGIC DIAGRAM



( ) = Denotes Pin Numbers for a 14-Pin Dual-In-Line Package

TRUTH TABLE (See Notes 1, 2 and 3)

C_{IN}	Y	X	$\overline{C_{OUT}}$	Σ	$\overline{\Sigma}$
0	0	0	1	0	1
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	1	0

NOTES:
1. $X = \overline{\overline{X} \cdot X_c}$; $Y = \overline{\overline{Y} \cdot Y_c}$ where $\overline{X} = \overline{X_1 \cdot Y_2}$; $\overline{Y} = \overline{Y_1 \cdot Y_2}$
2. When $\overline{X}$ or $\overline{Y}$ are used as inputs, X_1 and X_2 or Y_1 and Y_2 respectively must be tied to GND.
3. When X_1 and X_2 or Y_1 and Y_2 are used as inputs, $\overline{X}$ or $\overline{Y}$ respectively must be left open or used to perform the WIRED-AND function.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

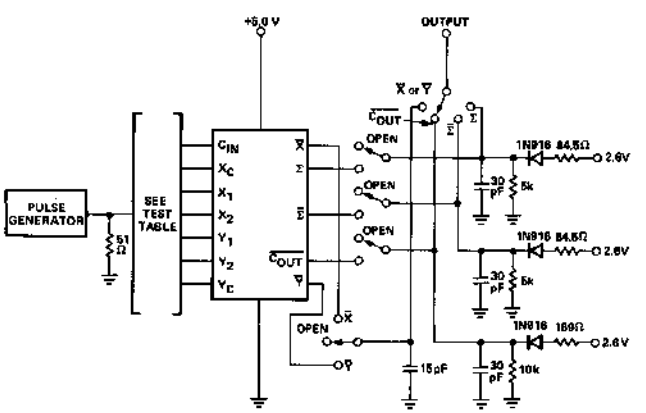
CHARACTERISTICS	LIMITS				TEST CONDITIONS										NOTES
	MIN.	TYP.	MAX.	UNITS	X_1	X_2	X	X_c	Y_1	Y_2	Y	Y_c	C_{IN}	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	0.8V	2.0V	2.0V	0.8V	0.8V	0.8V	2.0V	0.8V	-600μA	6
"0" Output Voltage			0.4	V	0.8V	0.8V	2.0V	2.0V	0.8V	0.8V	2.0V	2.0V	0.8V	16mA	7
"0" Input Current															
X_1	-0.1		-1.6	mA	0.4V	4.5V									
X_2	-0.1		-1.6	mA	4.5V	0.4V									
X	-0.1		-2.6	mA	0.0V	0.0V	0.4V	4.5V							
X_c	-0.1		-1.6	mA	0.0V	0.0V		0.4V							
Y_1	-0.1		-1.6	mA					0.4V	4.5V					
Y_2	-0.1		-1.6	mA					4.5V	0.4V					
Y	-0.1		-2.6	mA					0.0V	0.0V	0.4V	4.5V			
Y_c	-0.1		-1.6	mA					0.0V	0.0V		0.4V			
C_{IN}	-0.1		-8.0	mA									0.4V		
"1" Input Current															
X_1			40	μA	4.5V										
X_2			40	μA	0.0V										
X_c			40	μA			0.0V	4.5V							
Y_1			40	μA					4.5V	4.5V					
Y_2			40	μA					0.0V	0.4V					
Y_c			40	μA							0.0V	4.5V			
C_{IN}			160	μA	0.0V	0.0V			0.0V	0.0V			4.5V		
Input Voltage Rating															12
X_1	5.5			V	10mA	0.0V									
X_2	5.5			V	0.0V	10mA									
X_c	5.5			V			0.0V	10mA							
Y_1	5.5			V					10mA	0.0V					
Y_2	5.5			V					0.0V	10mA					
Y_c	5.5			V							0.0V	10mA			
C_{IN}	5.5			V									10mA		

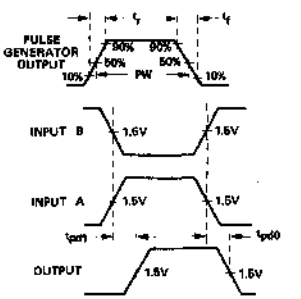
$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS										NOTES
	MIN.	TYP.	MAX.	UNITS	X_1	X_2	X	X_c	Y_1	Y_2	Y	Y_c	C_{IN}	OUTPUTS	
Power/Current Consumption		152/ 29	185/ 35	mW/ mA											11
Output Short Circuit Current (Σ)	-18		-57	mA	0.0V	0.0V			0.0V	0.0V	0.0V		2.0V	0.0V	10, 11
Output Short Circuit Current ($\overline{\Sigma}$)	-18		-57	mA	0.0V	0.0V			0.0V	0.0V			0.0V	0.0V	10, 11
Output Short Circuit Current ($\overline{C}_{out}$)	-18		-70	mA	0.0V	0.0V			0.0V	0.0V			0.0V	0.0V	10, 11
t_{pd} 1 C_{in} to $\overline{C}_{out}$		8	13	ns											8
t_{pd} 0 C_{in} to $\overline{C}_{out}$		8	13	ns											8
t_{pd} 1 Y_c to $\overline{C}_{out}$		20	25	ns											8
t_{pd} 0 Y_c to $\overline{C}_{out}$		20	25	ns											8
t_{pd} 1 X_c to Σ		35	45	ns											8
t_{pd} 0 X_c to Σ		35	45	ns											8
t_{pd} 1 Y_c to $\overline{\Sigma}$		25	35	ns											8
t_{pd} 0 Y_c to $\overline{\Sigma}$		25	35	ns											8
t_{pd} X_1, X_2 to $\overline{X}$		30	40	ns											8, 9
t_{pd} 0 X_1, X_2, to $\overline{X}$		15	20	ns											8, 9
t_{pd} 1 Y_1, Y_2, to $\overline{Y}$		30	40	ns											8, 9
t_{pd} 0 Y_1, Y_2, to $\overline{Y}$		15	20	ns											8, 9

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}
8. Refer to AC Test Figure.
9. This test is a measure of the required worst-case data set-up time.
10. Not more than one output should be shorted at a time.
11. V_{CC}=5.25 volts.
12. The total time required to perform the ADD function may be determined by summing the delays from X_1, X_2 to $\overline{X}$ or Y, Y_2 to $\overline{Y}$ with the delay from X_C or Y_C to Σ or $\overline{\Sigma}$.

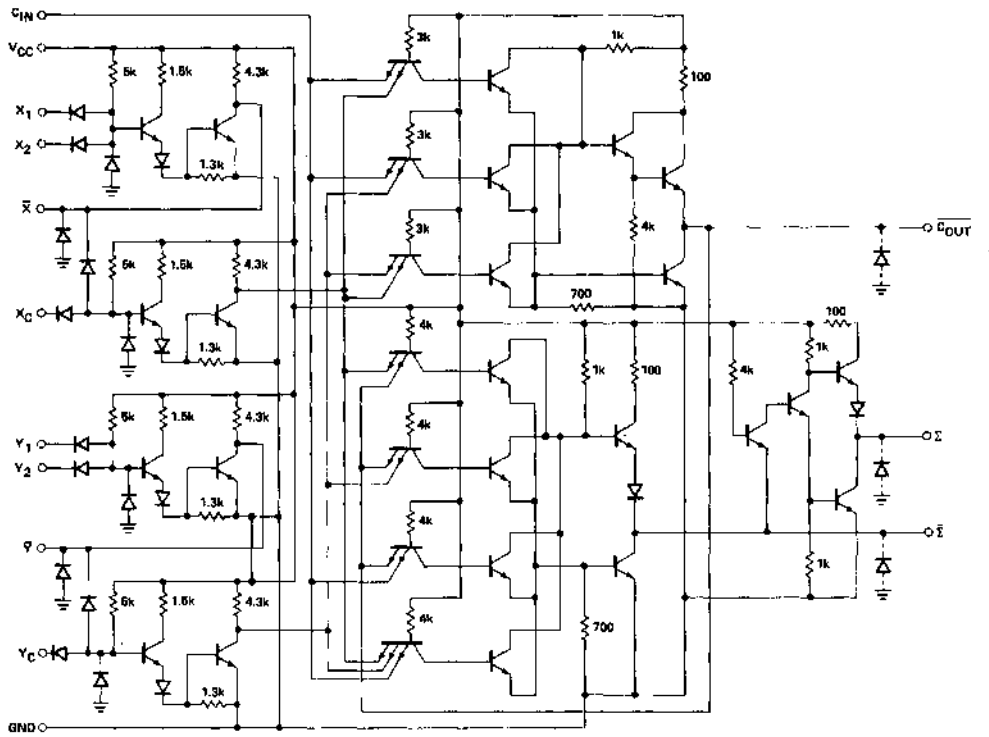
AC TEST FIGURE AND WAVE FORMS





NOTES:
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 2.6V, tr = tf ≤ 15ns, PW = 0.5ns, PRR = 1MHz.
5. Inputs and outputs not otherwise specified are open.
6. Capacitance shown include probe and jig capacitance.
7. All resistances are in ohms.

SCHEMATIC DIAGRAM

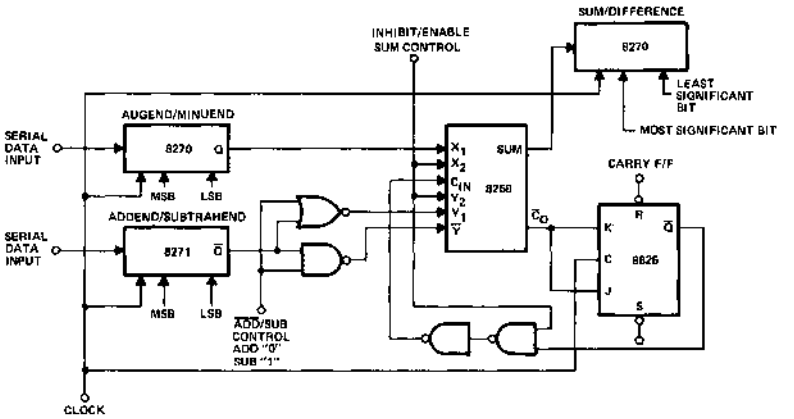


TEST TABLE (See Note 5)

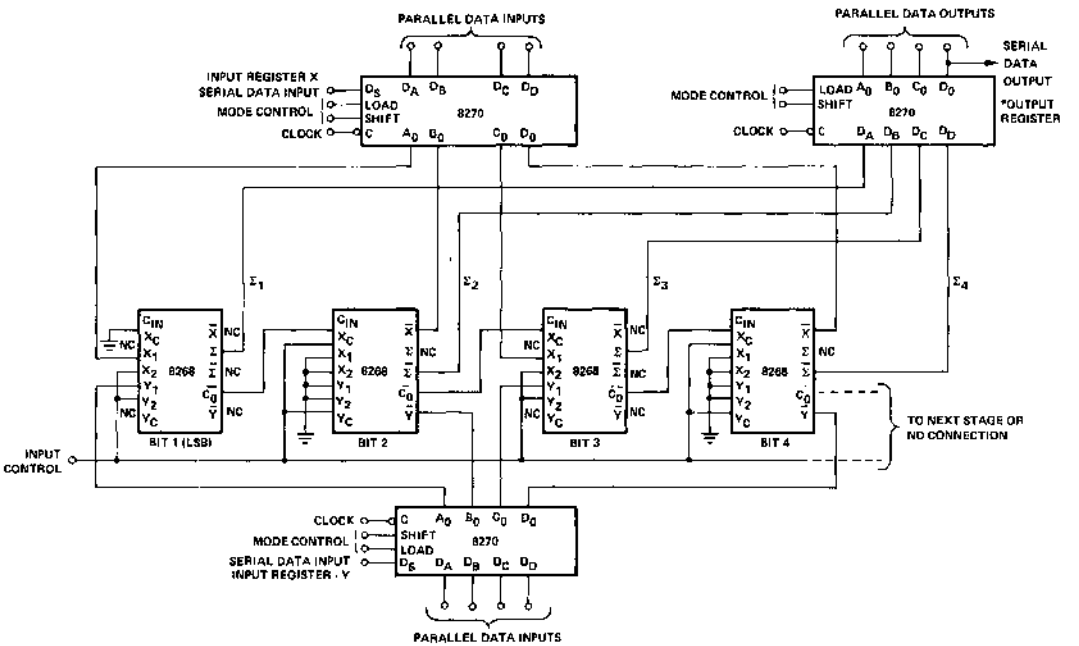
TEST NO.	OUTPUTS UNDER TEST	APPLY INPUT A TO	APPLY INPUT B TO	APPLY +2.6V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
2	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
3	$\overline{C}_{out}$	Y_C	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
4	$\overline{C}_{out}$	Y_C	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
5	Σ	X_C	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
6	Σ	X_C	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
7	Σ	Y_C	None	C_{in}	Y_1	Σ
8	$\overline{\Sigma}$	Y_C	None	C_{in}	Y_1	$\overline{\Sigma}$
9	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
10	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
11	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)
12	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)

TYPICAL APPLICATIONS

4-BIT SERIAL ADD/SUBTRACTOR



N-BIT PARALLEL ADDER



NOTES:
To expand storage register for serial/parallel operation, connect D_Q to D_S of next stage and common the mode control lines and the clock line of the first stage to their respective second stage equivalents.

*NOTE:
To expand output register for parallel outputs common clock, shift and load lines with their respective counterparts. For serial data output, also connect D_Q of first register to D_S of next register.

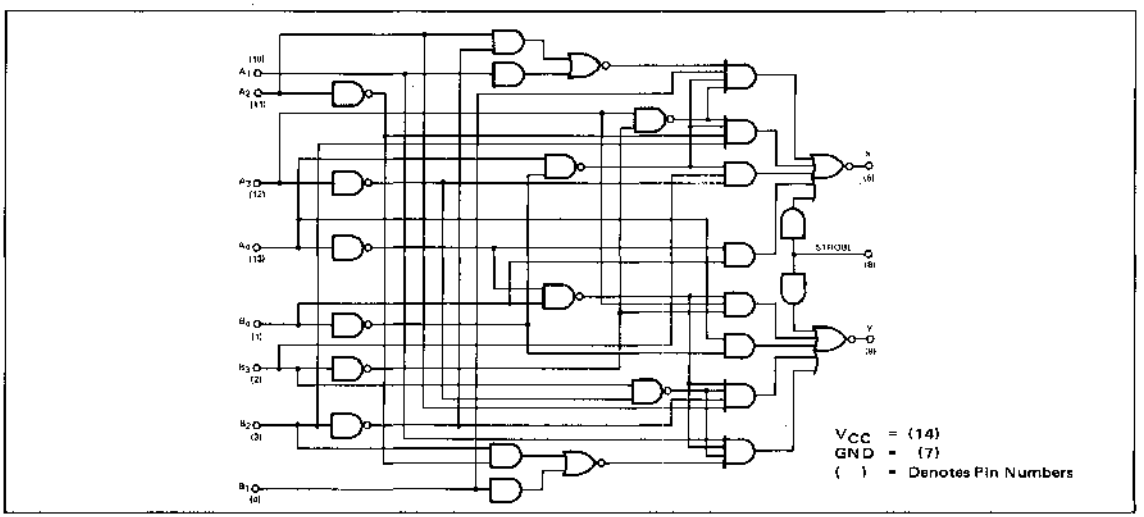
DESCRIPTION

The 8269, a 4 BIT COMPARATOR, is an array of gates designed to perform the numerical comparison of two four-bit binary numbers. The outputs indicate whether the two numbers are equal in value, or which number is the greater. The 8269 is a functional and pin-for-pin replacement for the DM8200.

TRUTH TABLE

INPUT				OUTPUT	
A_n		B_n	STROBE	X	Y
A	>	B	0	1	0
A	<	B	0	0	1
A	=	B	0	1	1
A	=	B	1	0	0

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"1" Output Voltage	2.6	3.5		V	I_{out} =-800µA	6
"0" Output Voltage		0.2	0.4	V	I_{out} = 16mA	7
"1" Input Current			80	µA	V_{in} = 4.5V	
"0" Input Current	-0.1		-3.2	mA	V_{in} = 0.4V	
Power Consumption			278/53	mW/mA	V_{CC} = 5.25V	
Short Circuit Output Current	- 18		-55	mA	V_{out} = 0V, V_{CC} = 5.25V	8
Input Voltage Rating	5.5			V	I_{in} = 10mA	

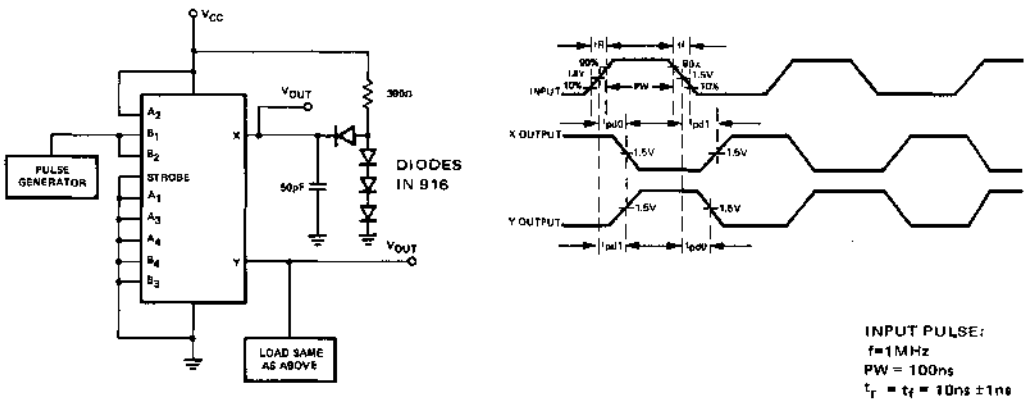
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Propagation Delay					
tpd1 (Data Input to Output)			40	ns	Test Figure 1
tpd0 (Data Input to Output)			30	ns	Test Figure 1
tpd1 (Strobe to Output)			27	ns	Test Figure 2
tpd0 (Strobe to Output)			18	ns	Test Figure 2

NOTES:

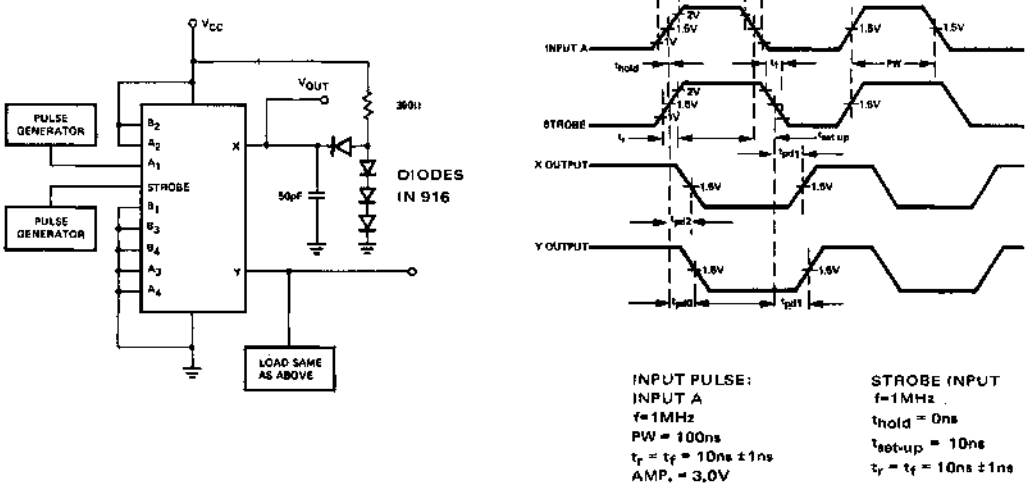
1. All voltage and capacitance measurements are referenced to the ground terminal.
   Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1","DOWN" Level = "0"
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Not more than one output should be shorted at a time.

AC TEST FIGURE AND WAVEFORMS



INPUT PULSE:
f=1MHz
PW = 100ns
$t_r = t_f$ = 10ns ±1ns
AMP. = 3.0V

FIGURE 1



INPUT PULSE:
INPUT A
f=1MHz
PW = 100ns
$t_r = t_f$ = 10ns ±1ns
AMP. = 3.0V

STROBE INPUT
f=1MHz
t_{hold} = 0ns
$t_{set\text{-}up}$ = 10ns
$t_r = t_f$ = 10ns ±1ns

FIGURE 2

DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.

The truth table for the control modes is shown below.

For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

The 8271 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

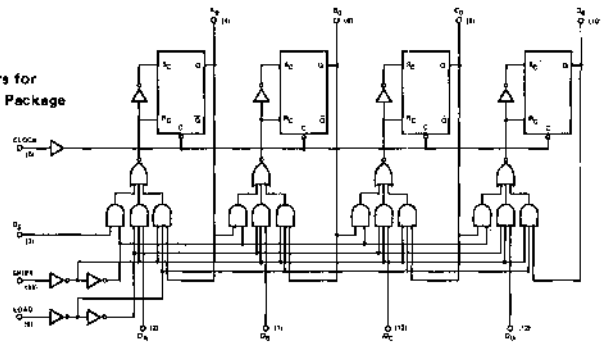
TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

LOGIC DIAGRAM

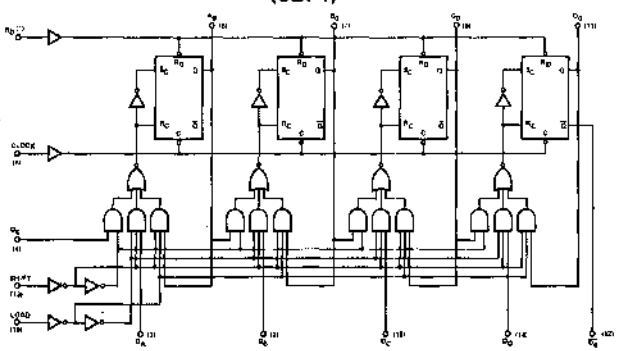
(8270)

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 pin Dual-In-Line Package



(8271)

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	LOAD	SHIFT	DATA INPUT	CLOCK	RESET 8271	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	0.8V	2.0V	Pulse	2.0V	-800μA	6
"0" Output Voltage			0.4	V	2.0V	0.8V	0.8V	Pulse	2.0V	11.2mA	7
"0" Input Current											
Load	-0.1		-1.2	mA	0.4V						
Shift	-0.1		-1.2	mA		0.4V	0.4V				
Data Input	-0.1		-1.2	mA			0.4V				
Clock	-0.1		-1.2	mA				0.4V			
Reset (8271 only)	-0.1		-1.2	mA					0V		
"1" Input Current											
Load			40	μA	4.5V						
Shift			40	μA		4.5V					
Data Input			40	μA			4.5V				
Clock			40	μA				4.5V			
Reset (8271 only)			40	μA					4.5V		
Input Voltage Rating											
(All Inputs)	5.5			V	10mA	10mA	10mA	10mA	10mA		

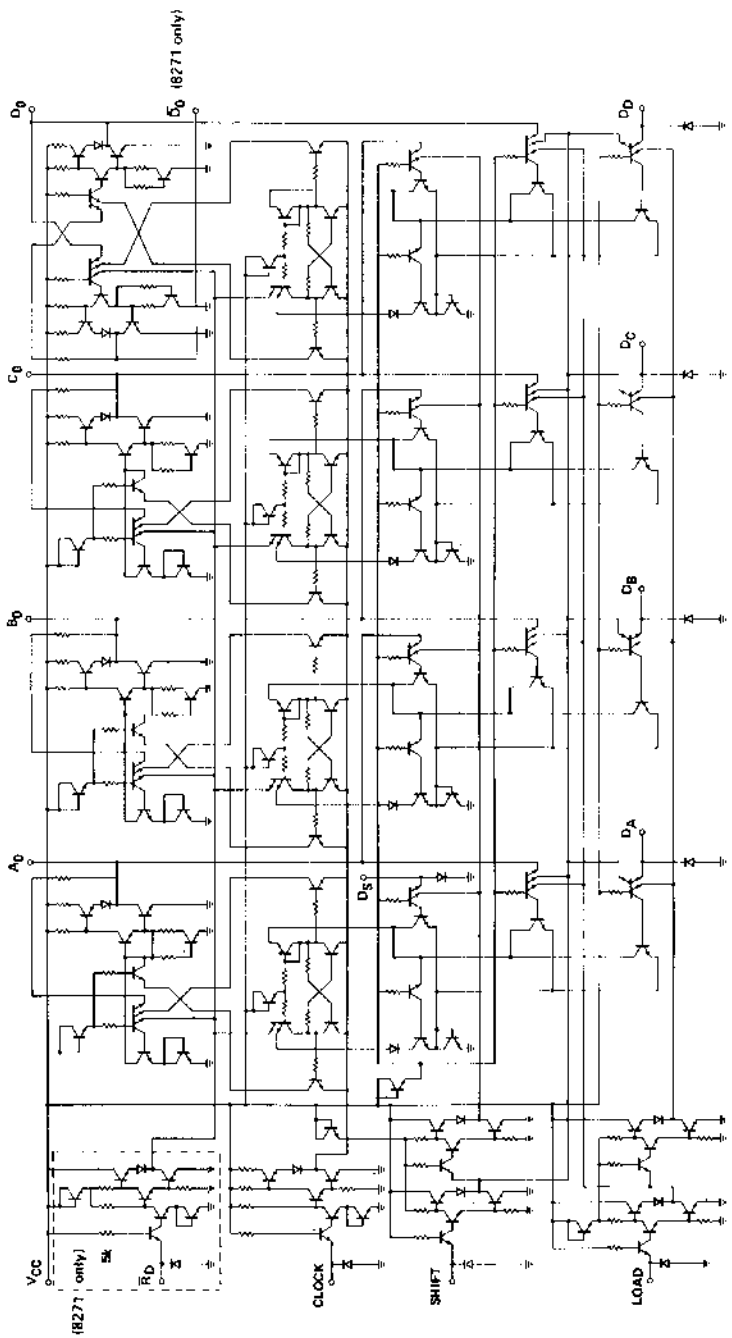
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	LOAD	SHIFT	DATA INPUT	CLOCK	RESET 8271	OUTPUTS	
Power/Current Consumption											
8270 Only		168/32	247/47	mW/mA							9
8271 Only		271/52	344/65	mW/mA							9
Turn-On Delay t_{on}											
All Binaries		25	40	ns							8
Turn-Off Delay t_{off}											
All Binaries		25	40	ns							8
Clock "1" Interval	20			ns				2.0V			
Transfer Rate	15	22		MHz							
Shift Load Set-Up Time		20	30	ns							
Data Set-Up Time		7	15	ns							

NOTES:

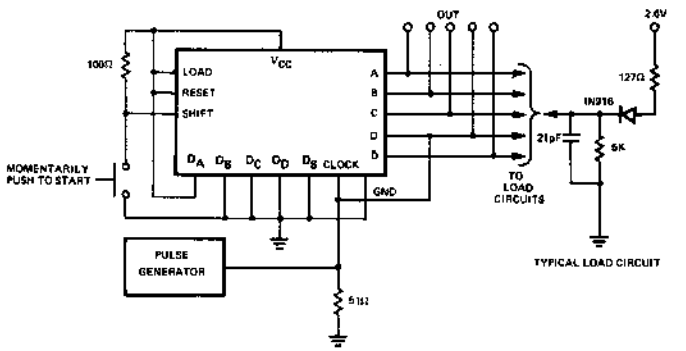
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Rating should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM



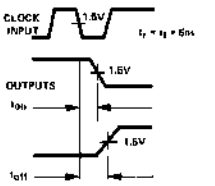
AC TEST FIGURES AND WAVEFORMS

TURN ON/OFF AND TRANSFER RATE



NOTES:

1. t_{on}/ t_{off}



2. Transfer rate & min clock "1" level: check that binary outputs are changing.

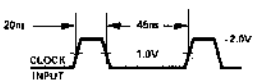
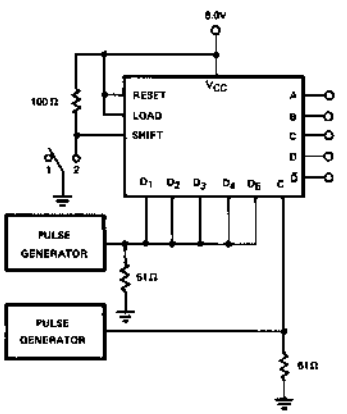
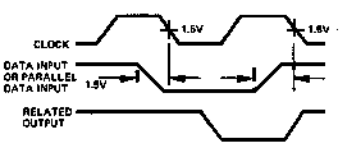


FIGURE 1

DATA SET-UP TIME



Load see Figure 1 above.



NOTES:

1. Switch in position 1 to test serial data input.
2. Switch in position 2 to test parallel data input.

Adjust data input or parallel input delays to test condition and verify output operation.

FIGURE 2

AC TEST FIGURES AND WAVEFORMS (Cont'd)

SHIFT/LOAD SET-UP TIME

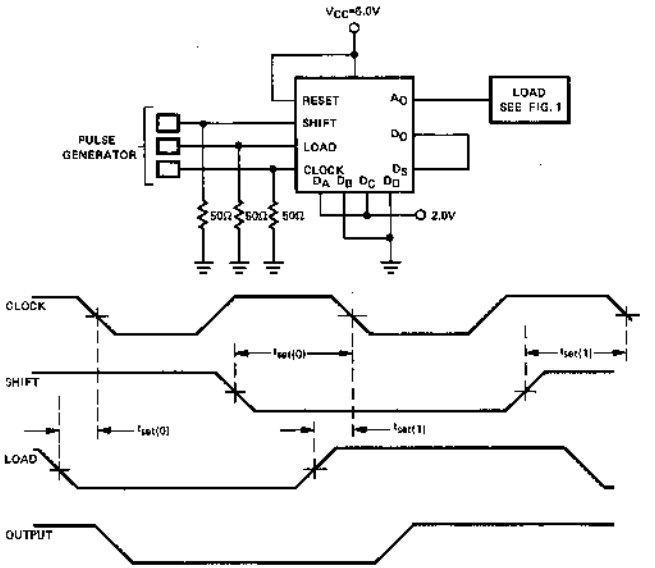
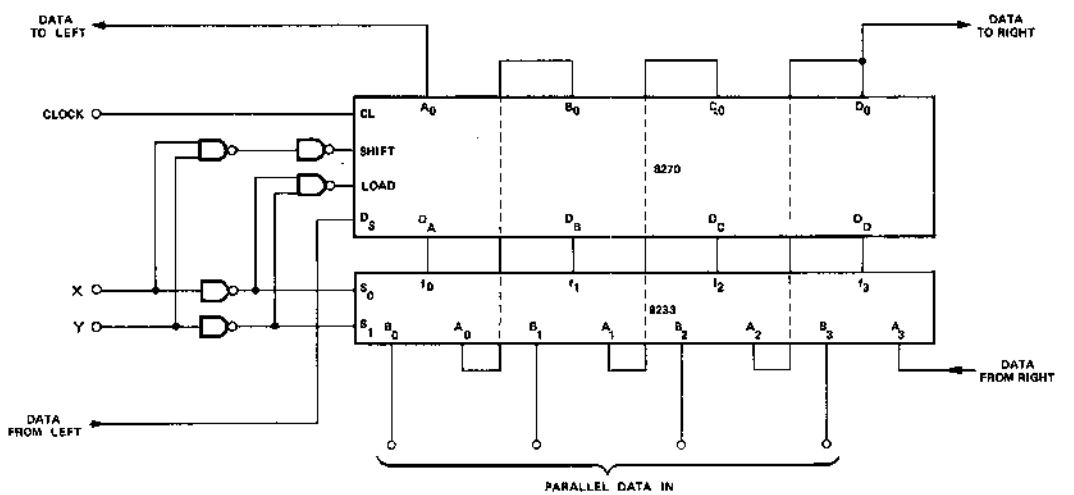


FIGURE 3

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1 MHz, V_{AC} = mV rms.
3. All diodes are 1N916.

TYPICAL APPLICATIONS

SHIFT-RIGHT/SHIFT-LEFT/PARALLEL ENTRY SHIFT REGISTER



X	Y	Function
0	0	Hold
0	1	Shift Left
1	0	Parallel Load
1	1	Shift Right

Package Count: 1-8270
1-8233
½ -8H90
¼ -8H80

signetics

10-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

8273

B,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

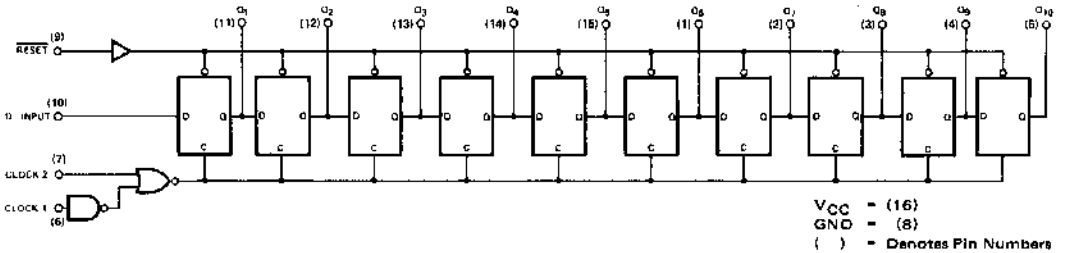
The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

TRUTH TABLE

INPUT	$\overline{\text{RESET}}$	CLOCK 1	CLOCK 2	$Q_n + 1$
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

NOTE: The unused clock input performs the INHIBIT function.
$\overline{\text{RESET}}$ = 0 ⇒ Q = 0

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	"D" INPUT	CLOCK 1	CLOCK 2	RESET		
"1" Output Voltage	2.6	3.4		V	2.0V	Pulse	0.8V		-500μA	6
"0" Output Voltage		0.2	0.4	V	0.8V	Pulse	0.8V		9.6mA	7
"0" Input Current										
"D" Input	-0.1		-1.6	mA	0.4V					
Clock 1	-0.1		-1.6	mA		0.4V				
Clock 2	-0.1		-1.6	mA			0.4V			
Reset	-0.1		-1.6	mA				0.4V		
"1" Input Current										
"D" Input			40	μA	4.5V					
Clock 1			40	μA		4.5V				
Clock 2			40	μA			4.5V			
Reset			40	μA				4.5V		
Input Voltage Reting (All Inputs)	5.5			V	10mA	10mA	10mA	10mA		

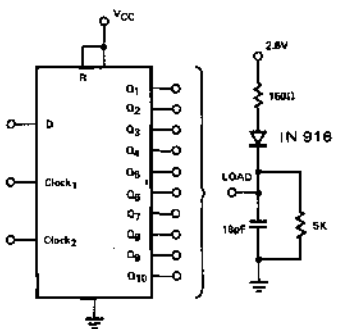
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	"D" INPUT	CLOCK 1	CLOCK 2	RESET		
Max. Data Transfer Rate	25	36		MHz						
Turn-On Delay t_{on}										
Clock 1 to Output		32	40	ns			0.0V	4.5V		10
Clock 2 to Output		28	40	ns				4.5V		10
Reset to Output		35	60	ns		4.5V				10
Turn-Off Delay t_{off}										
Clock 1 to Output		25	40	ns			0.0V			10
Clock 2 to Output		19	40	ns		4.5V				10
Clock Pulse Width										
Clock 1		16	25	ns			0.0V			10
Clock 2		12	20	ns		4.5V				10
Set-Up Time (t_{set-up})										
Clock 1			15	ns			0.0V			10
Clock 2			10	ns		4.5V				10
Hold Time (t_{hold})										
Clock 1			15	ns			0.0V			10
Clock 2			10	ns		4.5V				10
Power Consumption/Supply Current		341/ 65	540/ 103	mW						8
Short Circuit Output Current	-20		-70	mA						8,9
Input Voltage Rating										
(All Inputs)	5.5			V	10mA	10mA	10mA	10mA		

NOTES:

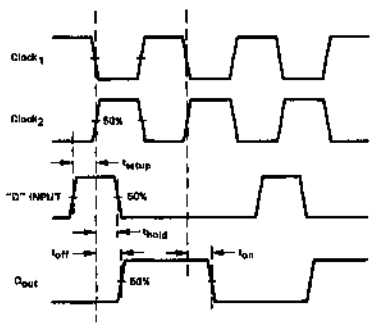
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. $V_{CC} = 5.25V$.
9. Not more than one output should be shorted at one time.
10. See AC Test Figure.

AC TEST FIGURE AND WAVEFORMS



NOTES:

1. Unused clock 2 input must be grounded.
2. Input pulse characteristics
   CLOCK
   Amplitude = 3.0V
   $t_r = t_f \leq 6ns$.



signetics

10-BIT PARALLEL-IN, SERIAL-OUT SHIFT REGISTER

8274

B,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

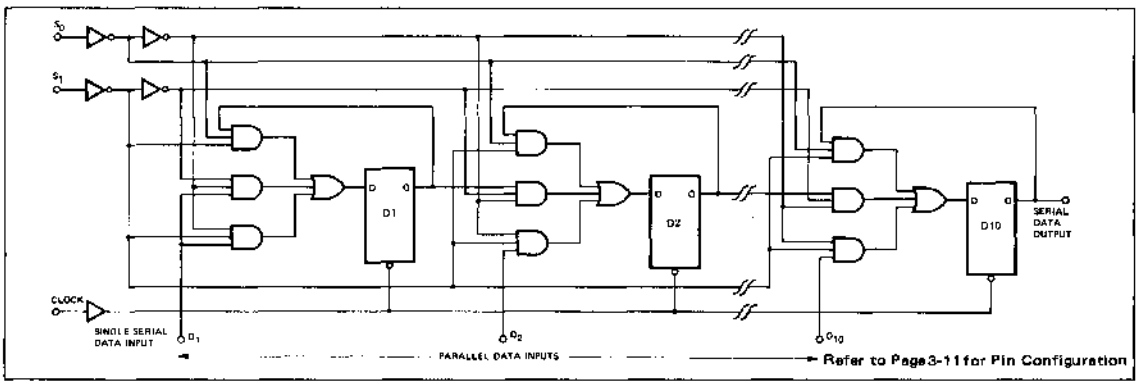
DESCRIPTION

The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in, serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D_1 input can also be used for serial entry. Two control inputs, S_0 and S_1, determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse. Guaranteed input clock frequency is 25MHz. With the exception of the Hold Mode, the control inputs may be changed when the clock is in either the high or low state without causing false triggering. The Hold Mode can be entered only when the clock is low. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmission, Pseudo-Random Code generation and Modulo-N Frequency Division.

TRUTH TABLE

S_0	S_1	OPERATING MODE
0	0	Hold
0	1	Clear
1	0	Load
1	1	Shift

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

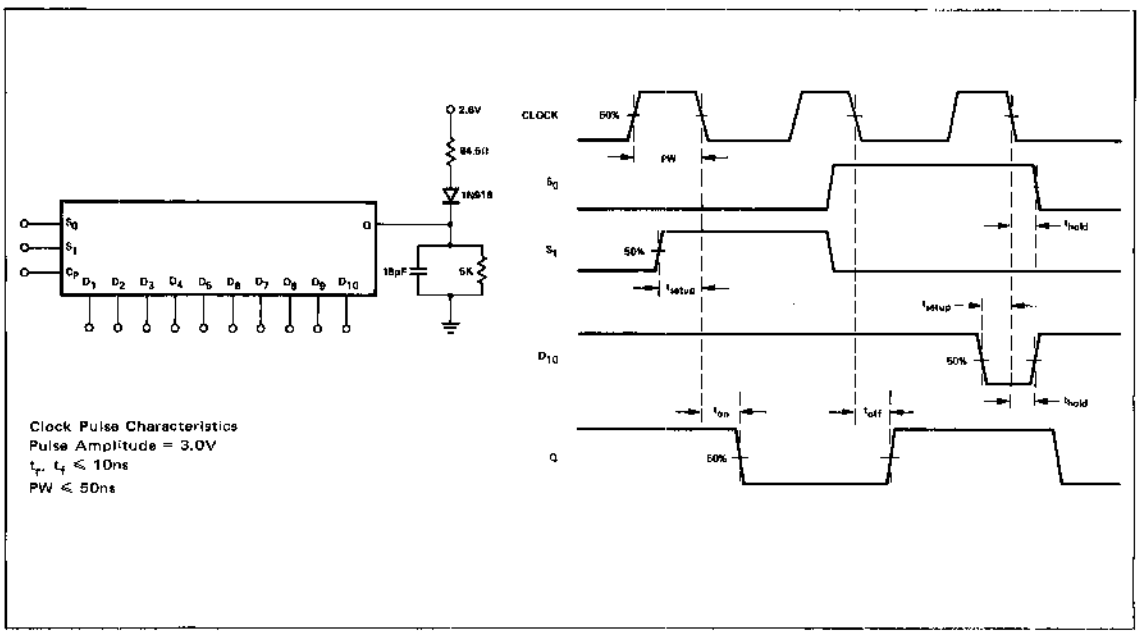
CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	S_0	S_1	CLOCK	OUTPUTS	
"1" Output Voltage	2.6	3.4		V	2.0V	2.0V	2.0V	Pulse	-800μA	6
"0" Output Voltage		0.2	0.4	V	0.8V	2.0V	2.0V	Pulse	16mA	7
"0" Input Current										
D_n	-0.2		-1.2	mA	0.4V					
S_0 and S_1	-0.2		-1.2	mA		0.4V	0.4V			
Clock	-0.2		-1.6	mA				0.4V		
"1" Input Current										
D_n			40	μA	4.5V					
S_0 and S_1			40	μA		4.5V	4.5V			
Clock			40	μA				4.5V		

$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	S_0	S_1	CLOCK	OUTPUT	
Data Transfer Rate	25MHz	30		MHz						10
Turn-On Delay (Clock to Output)		27	40	ns						10
Turn-Off Delay (Clock to Output)		21	40	ns						10
Clock Pulse Width		15	20	ns						10
Set-Up Time (t_{setup})										10
D_n		16	10	ns						
S_0, S_1		16	25	ns						
Hold Time (t_{hold})										
D_n		2	15	ns						
S_0, S_1		16	25	ns						
Power Consumption/Supply Current		380/72	567/108	mW	4.5V	4.5V	4.5V	0V		8
Short Circuit Output Current	-20		-70	mA	2.0V	2.0V	2.0V	Pulse	0.0V	8,9
Input Voltage Rating	5.5			V	10mA					

NOTES:
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. $V_{CC} = 5.25V$.
9. Not more than one output should be shorted at one time.
10. See AC Test Figure.

AC TEST FIGURE AND WAVEFORMS

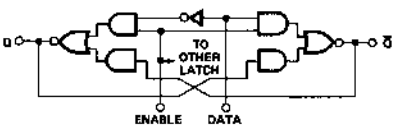


Clock Pulse Characteristics
Pulse Amplitude = 3.0V
t_r, $t_f \leq 10ns$
$PW \leq 50ns$

DESCRIPTION

The 8275 is a QUAD LATCH circuit designed to provide temporary storage of four bits of information. A common application is as a holding register between a counter and a display driver (such as the 8280 and 8T01.) Separate enable lines to latches 1-2 and 3-4 allow individual control of each pair of latches. Initially, data is transferred on the rising edge of the enable pulse. While the enable is high, output Q follows the data input. When the enable falls, the input data present at fall time is retained at the Q output. Both Q and $\overline{Q}$ are accessible.

LOGIC DIAGRAM AND TRUTH TABLE



Refer to Page 3-11 for Pin Configuration

(Each Latch)			
ENABLE	DATA	Q	$\overline{Q}$
1	1	1	0
1	0	0	1
0	1	*	*
0	0	*	*

*No Change.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT	ENABLE INPUT	OUTPUTS	
"1" Output Voltage (Q, $\overline{Q}$)	2.6	3.5		V			-800μA	6, 11
"0" Output Voltage (Q, $\overline{Q}$)			0.4	V			16mA	7, 11
"0" Input Current (Data)	-0.1		-3.2	mA	0.4V	5.25V		
"0" Input Current (Enable)	-0.1		-6.4	mA	5.25V	0.4V		
"1" Input Current (Data)			80	μA	4.5V	0.0V		
"1" Input Current (Enable)			160	μA	0.0V	4.5V		

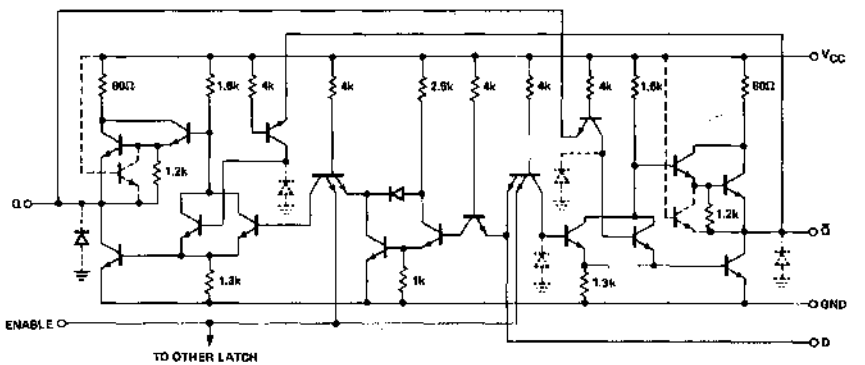
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT	ENABLE INPUT	OUTPUTS	
t_{setup} (1) at D input		12	20	ns				8, 12
t_{setup} (0) at D input		14	20	ns				8, 12
t_{hold} (1) at D input	0	15		ns				8, 13
t_{hold} (0) at D input	0	6		ns				8, 13
t_{pd} (1) D to Q		16	30	ns				8
t_{pd} (0) D to Q		14	25	ns				8
t_{pd} (1) D to $\overline{Q}$		24	40	ns				8
t_{pd} (0) D to $\overline{Q}$		7	15	ns				8
t_{pd} (1) E to Q		16	30	ns				8
t_{pd} (0) E to Q		12	20	ns				8
t_{pd} (1) E to $\overline{Q}$		16	30	ns				8
t_{pd} (0) E to $\overline{Q}$		12	20	ns				8
Power Consumption/Supply Current		205/39	265/50	mW/mA				11
Input Voltage Rating (Data)	5.5			V	10mA	0.0V		
Input Voltage Rating (Enable)	5.5			V	0.0V	10mA		
Output Short Circuit Current	-20		-70	mA	0.0V		0.0V	9

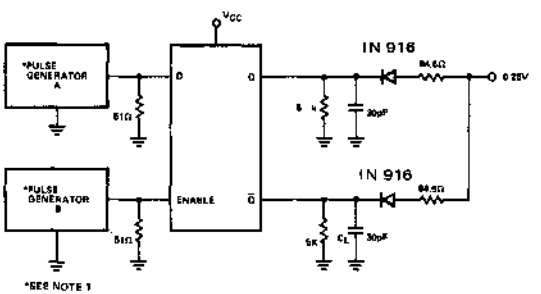
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. Inputs for output voltage test is per TRUTH TABLE with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. V_{CC} = 5.25 volts.
12. t_{setup} is defined as the time prior to the fall of the clock.
13. t_{hold} is defined as the time after the fall of the clock.

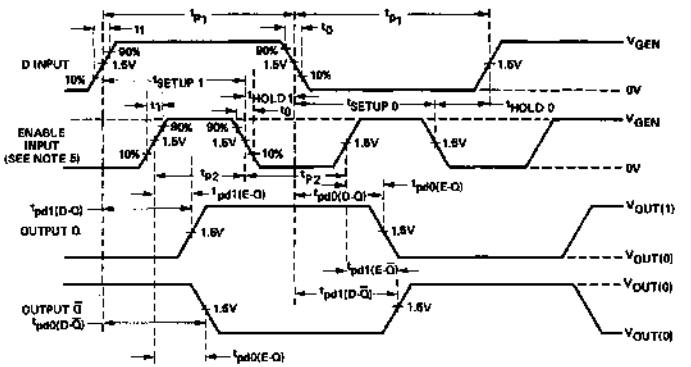
SCHEMATIC DIAGRAM



AC TEST FIGURE



AC TEST WAVEFORMS

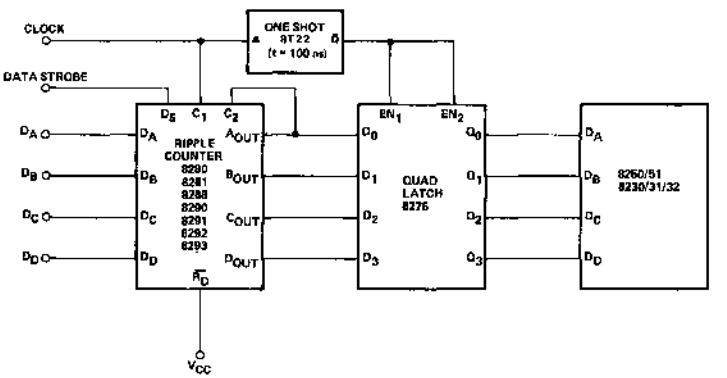


NOTES:

1. The pulse generators have the following characteristics: V_{gen} = 3V, $t_1 = t_0 \leq 10$ns, and $Z_{out} \approx 50\Omega$. For pulse generator A, t_{p1} = 1µs and PRR = 500kHz. For pulse generator B, tp2 = 500ns and Prr = 1MHz. Positions of D-input and enable input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. When measuring $t_{pd}1$ (D-Q), $t_{pd}0$ (D-Q), $t_{pd}0$ (D-$\overline{Q}$), and $t_{pd}1$(D-$\overline{Q}$), enable input must be held at logical 1.

TYPICAL APPLICATION

OUTPUT STROBING OF RIPPLE COUNTER TO ACHIEVE SYNCHRONOUS OUTPUT CHANGES



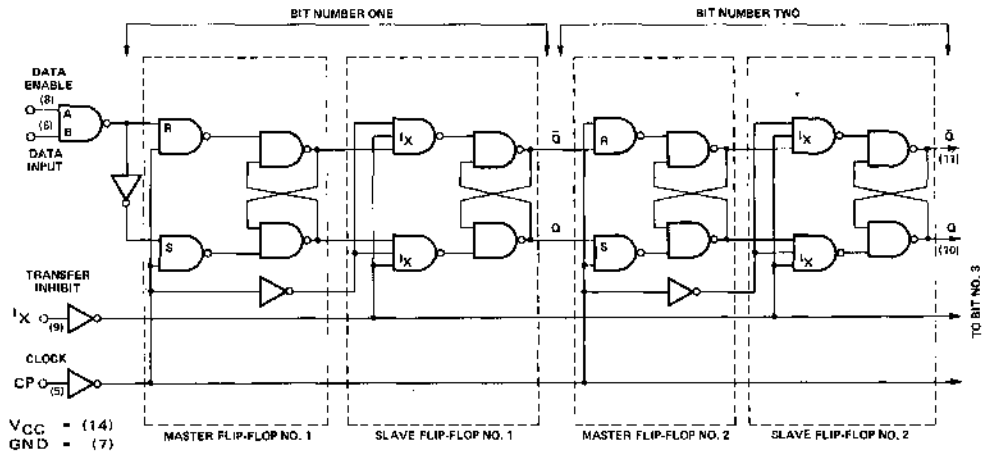
DESCRIPTION

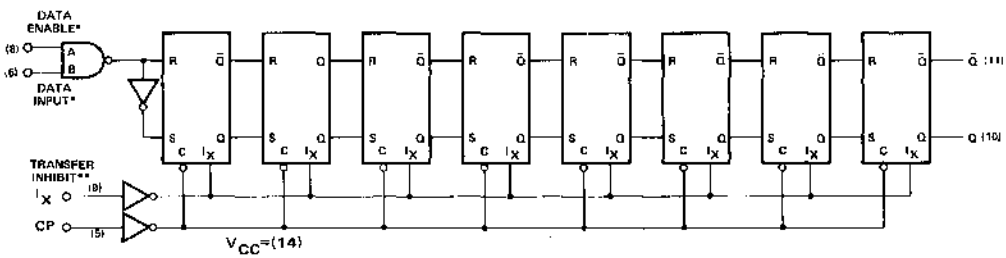
The 8276 is a serial-in, serial-out 8-Bit Shift Register composed of eight R-S master slave flip-flops. This shift register has input gating and an internal clock driver. In addition, a data transfer inhibit input is provided.

Data Input and Data Enable are gated through inputs A and B. An internal inverter provides the complimentary inputs to the first bit of the shift register. All inputs are fully buffered. Complementary Q and $\overline{Q}$ outputs are provided.

The internal clock driver/inverter causes the 8276 to shift data to the output on the positive edge of the input clock pulse, making the shift register compatible with the 8825 J-K Binary and the 8828 Dual D type Binary. The register is inhibited from shifting data when the Transfer Inhibit line is high. The inhibit function is achieved by preventing data transfer from master to slave sections of the register elements when the inhibit line is used.

LOGIC DIAGRAMS AND TRUTH TABLES





t_n		t_{n+8}
A (Data Enable)	B (Data Input)	Q
0	0	0
0	1	0
1	0	0
1	1	1

*NOTE: These functions are interchangeable.

**NOTE: Transfer Inhibit prevents transfer of data from master to slave.

NOTES:

t_n = Bit time before clock pulse.

t_{n+8} = Bit time after 8 clock pulses.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUTS	CLOCK	TRANS. INHIBIT	OUTPUTS	
"1" Output Voltage Q	2.6			V	2.0V		0.8V	-800μA	6, 10
"1" Output Voltage $\overline{Q}$	2.6			V	0.8V		0.8V	-800μA	6, 10
"0" Output Voltage Q			0.4	V	0.8V		0.8V	16mA	7, 10
"0" Output Voltage $\overline{Q}$			0.4	V	2.0V		0.8V	16mA	7, 10
"0" Input Current									
Data Input	-0.1		-1.6	mA	0.4V				
Clock Input	-0.1		-1.6	mA		0.4V			
Inhibit Input	-0.1		-1.6	mA			0.4V		
"1" Input Current									
Data Inputs			40	μA	4.5V				
Clock Input			40	μA		4.5V			
Inhibit Input			40	μA			4.5V		
Input Voltage Rating	5.5			V	10mA	10mA	10mA		

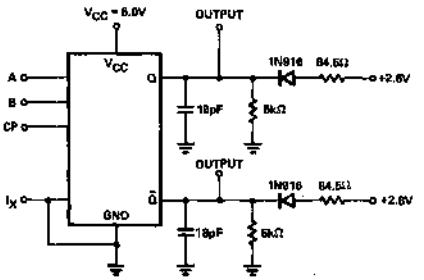
$T_A = 25°C$ and $V_{CC} = 5.0V$

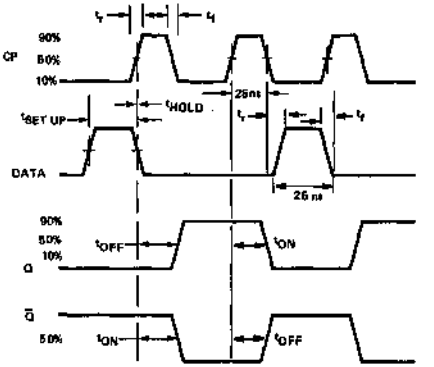
CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUTS	CLOCK	TRANS. INHIBIT	OUTPUTS	
Power/Current Consumption		205/39	340/65	mW/mA					11
Transfer Rate	15	20		MHz					
Turn-on Delay									
(Clock to Output)		22	33	ns					8
Turn-off Delay									
(Clock to Output)		22	33	ns					8
Clock Pulse Width	25			ns					
Set Up Time (Logical)									
"0" at A or B Input	25			ns					8
Set Up Time (Logical)									
"1" at A or B Input	25			ns					8
Output Short Circuit Current	-18		-55	mA				0V	9,11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at one time.
10. Clock input is driven by a 1kHz square wave for at least 8 cycles prior to measurements.
11. $V_{CC} = 5.25V$.

AC TEST FIGURE AND WAVEFORMS



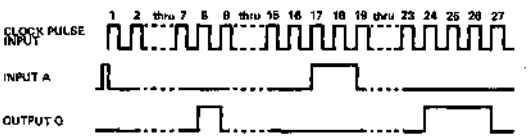


NOTES:
1. Unused input connected to 2.6V
2. Input pulse characteristics:
3. Setup time = 25ns
   Hold time = 0ns

CLOCK:
Amplitude = 3.0V
$t_r = t_f$ = 5ns max
PRR = 15 MHz, Pulse width = 25ns at 50% points

INPUT:
Amplitude = 3.0V
$t_r = t_f$ = 5ns max
PRR = 7.5 MHz
Pulse width = 25ns at 50% points

TYPICAL INPUT/OUTPUT WAVEFORMS



NOTE: Input B is connected to 2.6V. Transfer Inhibit Connected to 0V

Signetics

DUAL 8-BIT SHIFT REGISTER | 8277

PRODUCT AVAILABLE IN 0°C TO +75°C TEMP RANGE ONLY.

B,F PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

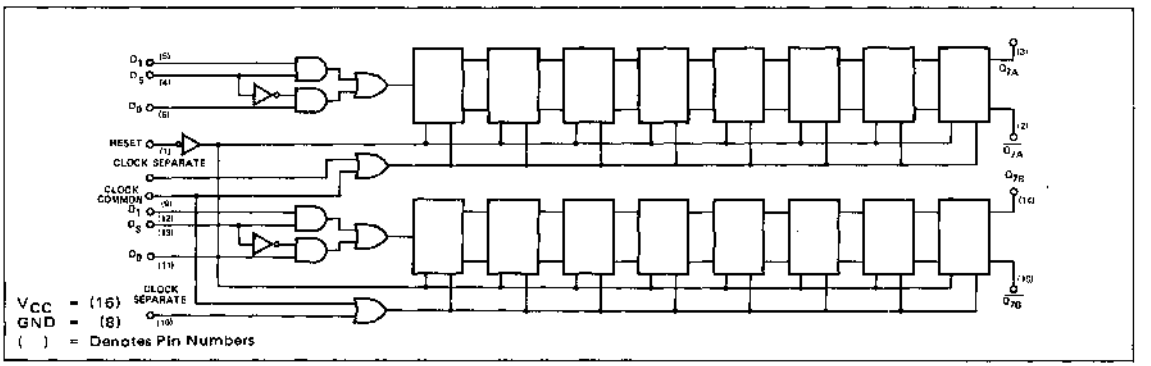
The 8277 is a dual 8-Bit Shift Register which provides the designer with sixteen (16) bits of serial storage operating at a typical shift rate of 20MHz. Features of the 8277 are:

1. TRUE and COMPLEMENT outputs are provided on each register's eighth bit.
2. Positive edge triggering on clock input.
3. SEPARATE CLOCK lines (pins 7 and 10) for each 8-bit register are provided as well as a COMMON CLOCK line (pin 9) for all sixteen storage bits.
4. Common RESET (pin 1).
5. AND-OR gating to the input of each 8-bit register is provided to accomplish the multiplex function.
6. Direct replacement for 9328.

TRUTH TABLE

D_S	D_0	D_1	Reset	Function
0	0	x	1	Shift in "0"
0	1	x	1	Shift in "1"
1	x	0	1	Shift in "0"
1	x	1	1	Shift in "1"
x	x	x	0	Reset "Q" to "0"

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

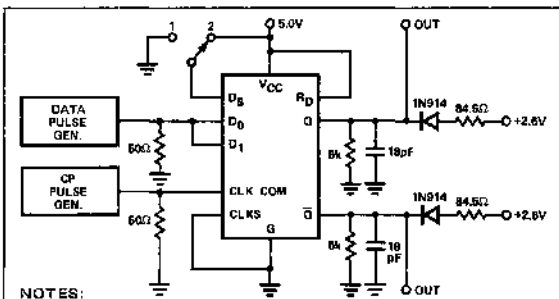
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA D_1, D_0	DATA SELECT	CLK COMMON	CLK SEP	RESET	OUTPUTS	
"1" Output Voltage (Q)	2.6	3.5		V	2.0V	2.0V	Pulse	0.8V	2.0V	-800µA	6
"1" Output Voltage (Q)	2.6	3.5		V	0.8V	2.0V	0.8V	Pulse		-800µA	6
"0" Output Voltage (Q)			0.4	V	0.8V	0.8V	Pulse	0.8V		16mA	7
"0" Output Voltage (Q)			0.4	V	2.0V	0.8V	Pulse	0.8V		16mA	7
"0" Input Current											
Data, Reset	-0.1		-1.6	mA	0.4V				0.4V		
Data Select	-0.1		-3.2	mA		0.4V					
Clock Separate	-0.1		-1.6					0.4V			
Clock Common	-0.1		-3.2	mA			0.4V				
"1" Input Current											
Data, Reset, Clock Separate			40	µA	4.5V			4.5V	4.5V		
Data Select			80	µA		4.5V					
Clock Common			80	µA			4.5V				
Power/Current Consumption			540/ 103	mW/mA							8
Input Voltage Rating											
All Inputs	5.5			V	10mA	10mA	10mA	10mA	10mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$

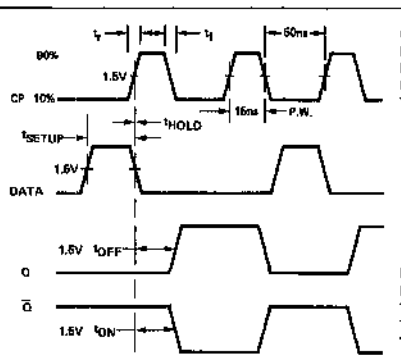
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA D_1, D_0	DATA SELECT	CLK COMMON	CLK SEP	RESET	OUTPUTS	
Turn-on Delay											
Clock To Output		25	40	ns							10
Reset To Output		25	40	ns							10
Turn-off Delay											
Clock To Output		25	40	ns							10
Reset To Output		25	40	ns							10
Clock Pulse Width	15			ns							10
Shift Rate	15	20		MHz							10
Data Set-up Time		20	30	ns							10
Data Hold Time			5	ns							10

NOTES:
1. All voltage measurments are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive Logic Definitions: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. $V_{CC} = 5.25V$
9. Clock input is driven by a 1kHz square wave for at least 8 cycles prior to measurement.
10. Refer to AC Test Figure.

AC TEST FIGURE AND WAVEFORMS



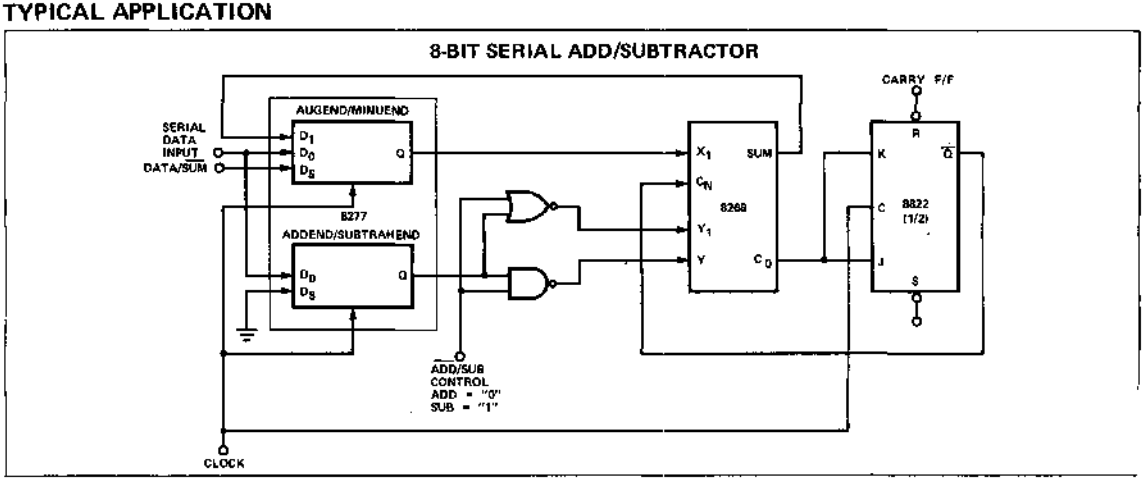
NOTES:
1. Each register is tested separately.
2. All T delay measurements taken at 1.6V level.
3. Tie all unused inputs to 2.6V.
4. 18 pF on outputs includes probe and jig capacitance.



CLOCK PULSE:
P.A. = 3.0V
P.R.R. = 15 MHz
P.W. = 15 ns
$T_r = T_f = 5ns$

DATA PULSE:
P.A. = 3.0V
P.R.R. = 7.5 MHz
P.W. = 25 ns
$T_r = T_f = 5$ ns
$T_{SETUP} = 25$ ns
$T_{HOLD} = 0$ ns.

TYPICAL APPLICATION



signetics

BCD DECADE COUNTER/STORAGE ELEMENT
4-BIT BINARY COUNTER/STORAGE ELEMENT

8280
8281

A,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit subsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

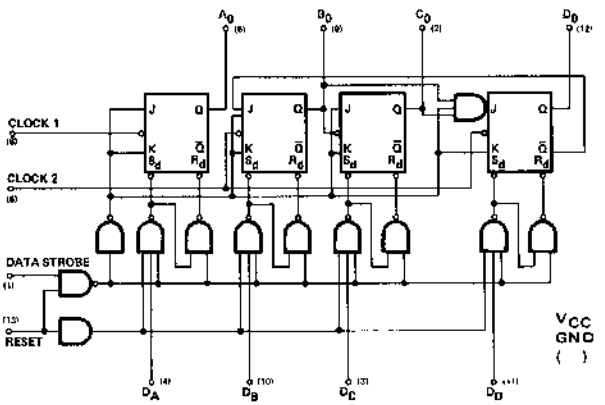
The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

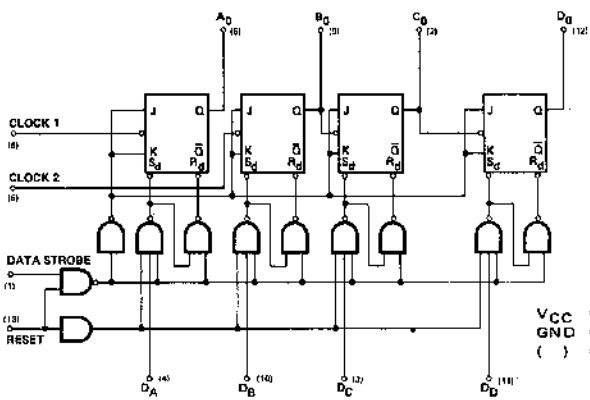
The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

LOGIC DIAGRAMS

8280



8281



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage (All Outputs)	2.6	3.5		V	0.8V	2.0V	2.0V		Output A	-800μA	7
"0" Output Voltage (All Outputs)			0.4	V	0.8V	0.8V	0.8V		Output A	16mA	8
"0" Input Current											
$\overline{\text{Strobe}}$	-0.1		-1.6	mA	0.4V						
Data Inputs	-0.1		-1.2	mA		0.4V					
$\overline{\text{Reset}}$	-0.1		-3.2	mA			0.4V				
Clock 1	-0.1		-3.2	mA				0.4V			
Clock 2 (8280)	-0.1		-3.2	mA					0.4V		
Clock 2 (8281)	-0.1		-1.6	mA					0.4V		
"1" Input Current											
$\overline{\text{Strobe}}$			40	μA	4.5V						
Data Inputs			40	μA		4.5V					
$\overline{\text{Reset}}$			80	μA			4.5V				
Clock 1			80	μA				4.5V			
Clock 2 (8280)			80	μA					4.5V		
Clock 2 (8281)			40	μA					4.5V		
Power/Current Consumption		184/35	236/45	mW/mA			0V	0V	0V		12
Input Voltage Rating all Inputs	5.5			V	10mA	10mA	10mA	10mA	10mA		10
Output Short Circuit Current	-10		-60	mA	0V					0V	9, 12

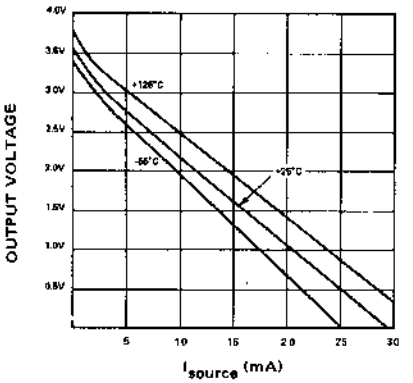
T_A = 25° C and V_{CC} = 5.0V

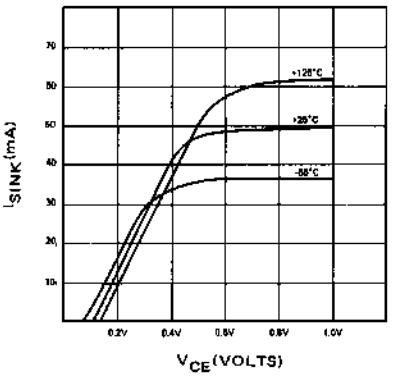
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Clock Mode t_{on} Delay											
Bit A, B, C, D		15	25	ns							11
Clock Mode t_{off} Delay											
Bit A, B, C, D		15	25	ns							11
Data/Strobe t_{on} Delay											
Bit A, B, C, D		25	35	ns							11
Data/Strobe t_{off} Delay											
Bit A, B, C, D		30	40	ns							11
Toggle Rate	20	25		MHz							11
$\overline{\text{Strobe}}$ Pulse Width		20	35	ns					A_{OUT}		11
$\overline{\text{Reset}}$ Pulse Width		20	35	ns					A_{OUT}		11
$\overline{\text{Strobe}}$ Release Time		30	40	ns					A_{OUT}		11
$\overline{\text{Reset}}$ Release Time		50	75	ns					A_{OUT}		11

NOTES:

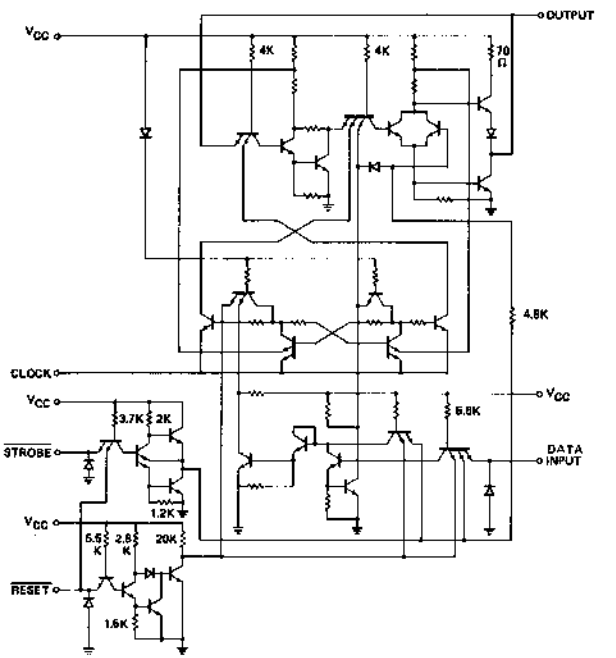
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Not more than one output should be shorted at a time.
10. Each input is tested separately.
11. Refer to AC Test Figures.
12. V_{CC} = 5.25V.

TYPICAL OUTPUT CHARACTERISTICS

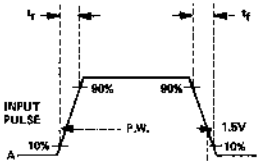




SCHEMATIC DIAGRAM

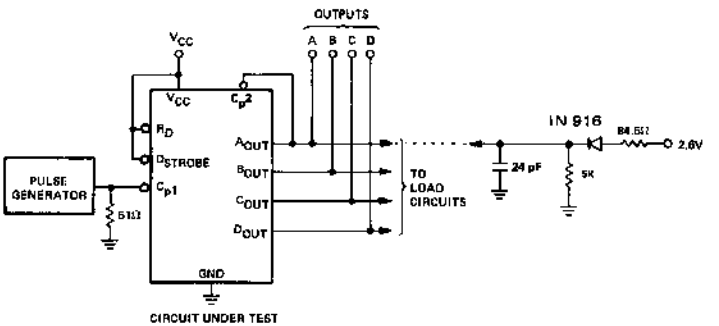


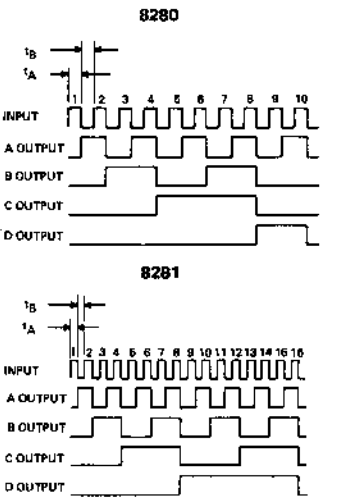
AC TEST FIGURES AND WAVEFORMS



NOTE: Input pulse notations apply unless otherwise specified.

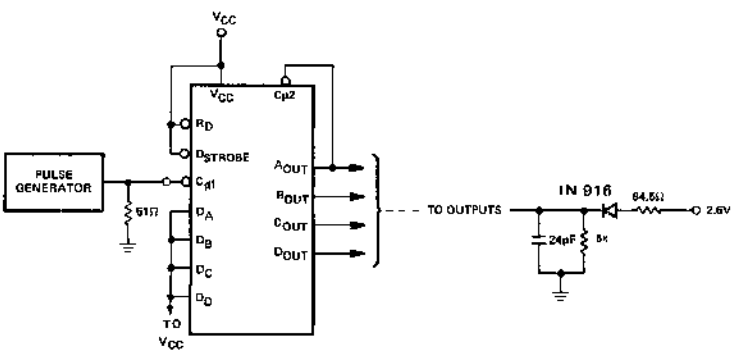
TOGGLE RATE

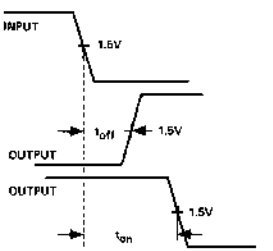




INPUT PULSE:
Amplitude = 2.6V
t_A = 25ns, t_B = 25ns,
$t_r = t_f$ = 5ns max.

CLOCK MODE t_{on}/t_{off} DELAY



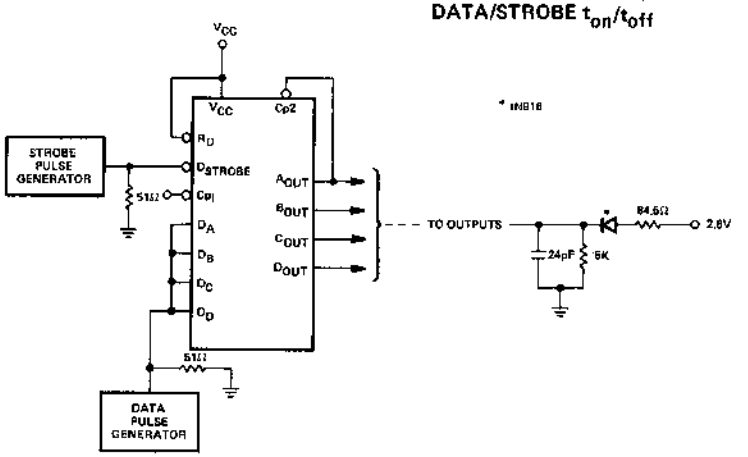


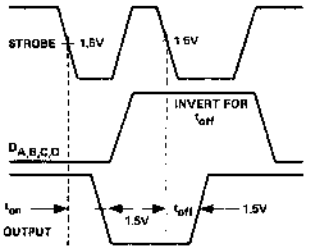
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with a load circuit as shown.

INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns
$t_r = t_f$ = 5ns.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

DATA/STROBE t_{on}/t_{off}

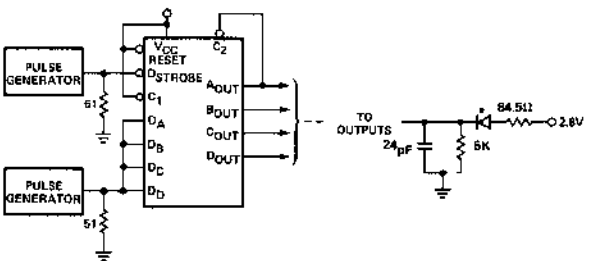


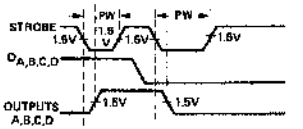


Strobe, P.A. = 2.6V
P.W. = 300ns
PRR = 1 MHz
t_r = t_f = 5ns
Data, P.A. = 2.6V
P.W. = 600ns
PRR = 500 KHz
t_r = t_f = 5ns.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.

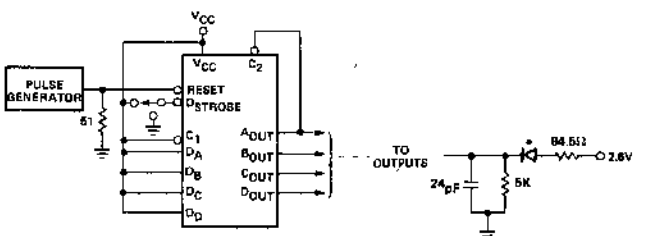
MINIMUM STROBE PULSE WIDTH

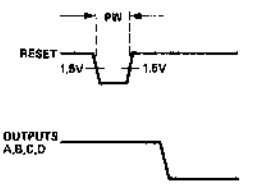




INPUT PULSE:
Amplitude = 2.6V
t_r = t_f = 5ns.

MINIMUM RESET PULSE WIDTH

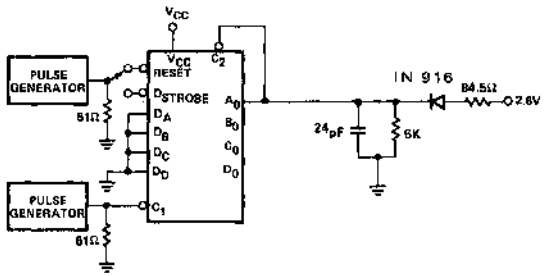


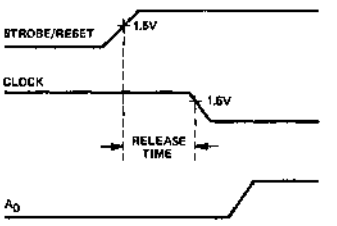


INPUT PULSE:
Amplitude = 2.6V
t_r = t_f = 5ns max.
Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBE/RESET RELEASE TIME



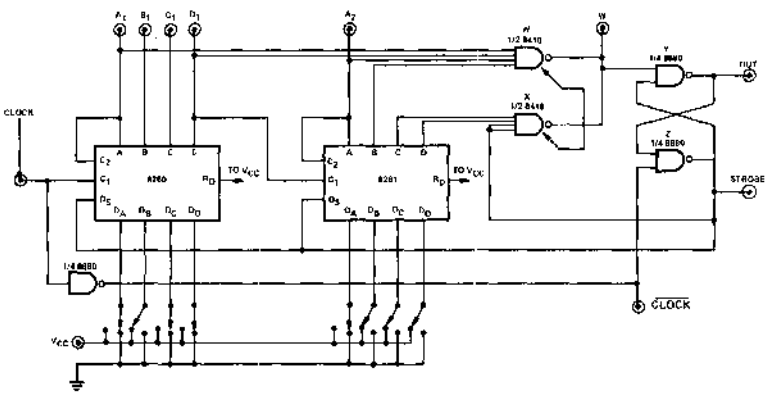


NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.

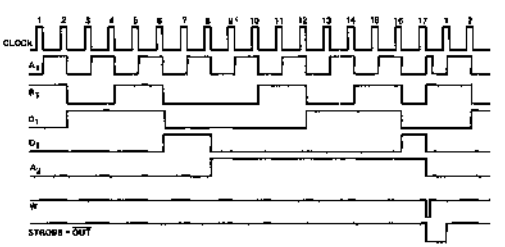
Clock, Strobe/Reset:
Ampl = 2.6V
tr = tf = 5 ns max.
PRR = 1 MHz 50% Duty Cycle.

TYPICAL APPLICATIONS

VARIABLE MODULUS COUNTER



TIMING DIAGRAM



signetics

BINARY HEXADECIMAL AND BCD DECADE, SYNCHRONOUS UP/DOWN COUNTERS

8284
8285

A,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The Up/Down Counter is a monolithic MSI circuit containing gates and binaries interconnected to provide a bi-directional divide-by-ten (decade) or divide-by-sixteen (hexadecimal) result as a function of the clock input.

The output code of the decade up/down counter is the commonly used BCD (8421) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9.

The hexadecimal up/down counter provides the output sequence 0 through 15 which is presented in a weighted binary code (8421).

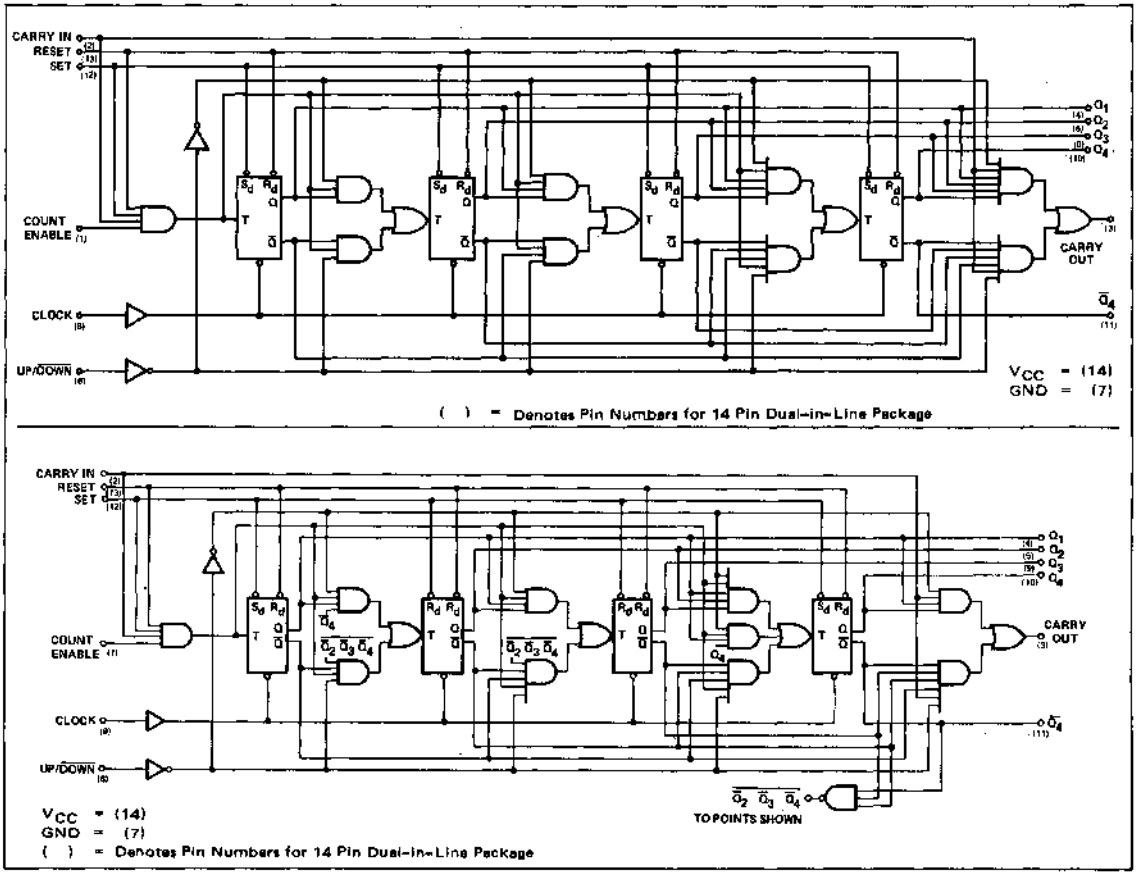
Set and Reset on the binary elements provide asynchronous entry with respect to the clock line, causing a count of "0" or "15" (8284) or of "0" or "9" (8285), and also inhibit propagation of count enable data.

Entry and propagation of data is performed in a synchronous manner with the clock line, which is active on its negative going excursion. The input from a previous stage or other source is channeled through "Carry In" and its propagation can be inhibited by the "Count Enable" line. "Carry In" and "Count Enable" input duality gives added flexibility in multiple package cascading applications.

Direction of the counter is steered from a single line (Up/$\overline{\text{Down}}$), where a "0" level will cause a "down" count and a "1" level will accomplish an "up" count.

In addition to all Q outputs of the four binaries the $\overline{Q}$ output of the most significant binary (Q4) and the Carry Out term are available.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	SET	RESET	UP/DOWN	COUNT ENABLE	CLOCK	CARRY IN	OUTPUTS	
"1" Output Voltage												
Q_1, Q_4, Carry Out	2.6			V	0.8V	2.0V	2.0V			2.0V	-800μA	5
Q_2, Q_3, (8284)												
Q_2, Q_3 (8285)	2.6			V	Pulse		0.8V				-800μA	5, 9
$\overline{Q}_4$	2.6			V	2.0V	0.8V					-800μA	5
"0" Output Voltage												
Q_1,Q_2,Q_3,Q_4 and Carry Out			0.4	V	2.0V	0.8V				0.8V	9.6mA	6
$\overline{Q}_4$			0.4	V	0.8V	2.0V					9.6mA	6
"1" Input Current												
Carry In			120	μA	Pulse		5.0V			4.5V		
Set			200	μA	4.5V	Pulse						
Reset			40	μA	Pulse	4.5V						
Count Enable			40	μA				4.5V				
Clock and Up/Down			40	μA			4.5V		4.5V			
"0" Input Current												
Carry In	-0.1		-3.2	mA	Pulse		0V			0.4V		
Set	-0.1		-6.4	mA	0.4V							
Reset	-0.1		-1.6	mA		0.4V						
Count Enable	-0.1		-1.6	mA				0.4V				
Clock	-0.1		-1.6	mA					0.4V			
Up/Down	-0.1		-1.6	mA			0.4V					
Input Voltage Rating												
Carry In	5.5			V		0V	5.0V	0V		10mA		
Reset	5.5			V		10mA		0V		0V		
Set	5.5			V	10mA			0V		0V		
Count Enable	5.5			V	0V			10mA		0V		
Up/Down	5.5			V			10mA					
Output Short Circuit Current	-20		-70	mA							0V	8, 10

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	SET	RESET	UP/DOWN	COUNT ENABLE	CLOCK	CARRY IN	OUTPUTS	
Power/Current Consumption		315/ 80	420/ 80	mW/ mA								10
Propagation Delay												
t_{on} Clock to Q_4 & $\overline{Q}_4$		32	45	ns								7
t_{on} Clock to Q_1, Q_2, Q_3		28	40	ns								7
t_{off} Clock to Q_n, $\overline{Q}_n$		25	35	ns								7
t_{on} Reset to Q_n		24	35	ns								7
t_{off} Set to Q_n		15	25	ns								7
t_{on} Reset to $\overline{Q}_n$		32	45	ns								7
t_{on} Carry In to Carry Out		15	25	ns								7
t_{off} Carry In to Carry Out		20	30	ns								7
Clock Min. "1" Interval	20	15		ns								7
Count Rate	20	30		MHz								
Carry In, Count Enable, & Up/Down Set-Up Time		15	25	ns								
Carry In, Count Enable & Up/Down Hold Time		0	2	ns								
Set/Reset Pulse Width		20	25	ns								

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to V_{CC}.
7. Refer to AC Test Figure.
8. Not more than one output should be shorted at a time.
9. Connect Q_4 to count enable, set the counter (1001), and count down. The counter will halt at BCD-7 (0111).
10. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

MODE OF OPERATION

8284 Binary Synchronous Up/Down Counter
8285 BCD Synchronous Up/Down Counter

	SET	RESET	CARRY IN	COUNT ENABLE	UP/$\overline{\text{DOWN}}$	FUNCTION
A. Asynchronous						
	1	0	X	X	X	"0" (0 0 0 0)
8284 Only	0	1	X	X	X	"15" (1 1 1 1)
8285 Only	0	1	X	X	X	"9" (1 0 0 1)
B. Synchronous						
	1	1	0	X	X	Hold *
	1	1	X	0	X	Hold *
	1	1	1	1	0	"Down" Count *
	1	1	1	1	1	"Up" Count *

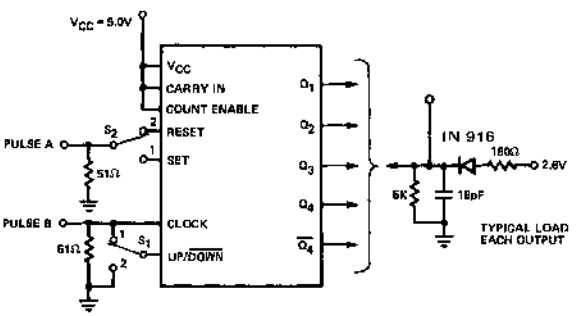
*Function is synchronous with NEGATIVE going transition of the Clock pin.
X = don't care.

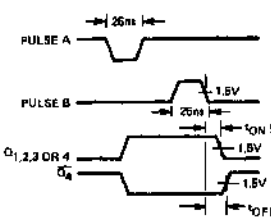
CARRY OUT

Carry Out_{8284} = Carry In $(Q_1Q_2Q_3Q_4$ UP + $\bar{Q}_1\bar{Q}_2\bar{Q}_3\bar{Q}_4$ $\overline{\text{DOWN}}$

Carry Out_{8285} = Carry In $(Q_1Q_4$ UP + $\bar{Q}_1\bar{Q}_2\bar{Q}_3\bar{Q}_4$ $\overline{\text{DOWN}}$

CLOCK MODE (t_{on} AND t_{off})

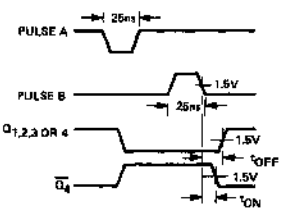




Reset Tied To V_{CC}
S_1' Position 1
S_2' Position 1

PULSE A

Pulse Amplitude = 2.6V
Pulse $Width_{(0)}$ = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10% to 90% Points



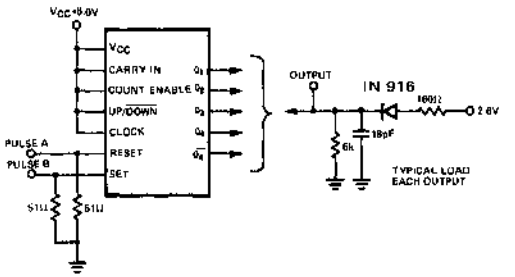
Set Tied To V_{CC}
S_1' Position 2
S_2' Position 2

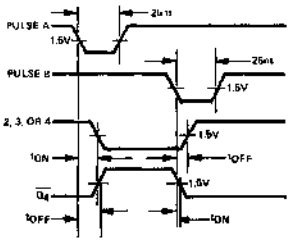
PULSE B

Pulse Amplitude = 2.6V
Pulse Width = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10% to 90% Points

AC TEST FIGURES AND WAVEFORMS (Cont'd)

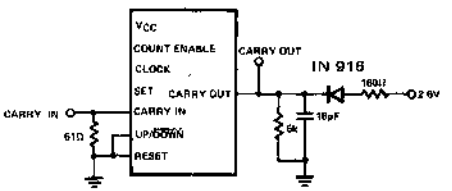
SET/RESET MODE (t_{on} and t_{off})

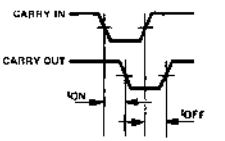




Pulse A and B
Pulse amplitude = 2.6V
Pulse width (0) =25ns
Frequency = 5MHz
$t_r = t_f$ =5ns at 10% to 90% points

CARRY IN/CARRY OUT (t_{on} and t_{off})

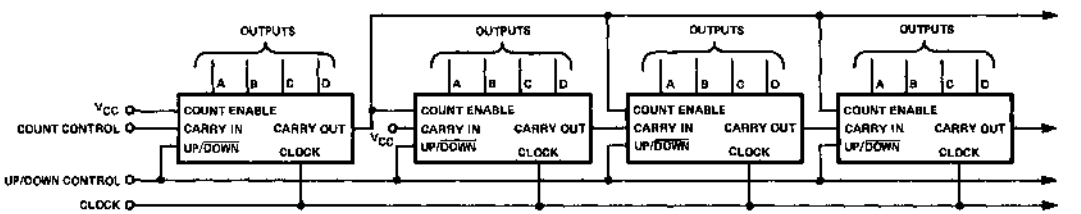




Carry in pulse
Pulse amplitude = 2.6V
Pulse width (0) = 50ns
Frequency =10MHz
$t_r = t_f$ =5ns at 10% to 90% points

TYPICAL APPLICATIONS

SYNCHRONOUS EXPANSION UP/DOWN COUNTERS



DESCRIPTION

The 8288 Divide by Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

The 8288 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, the 8288 is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

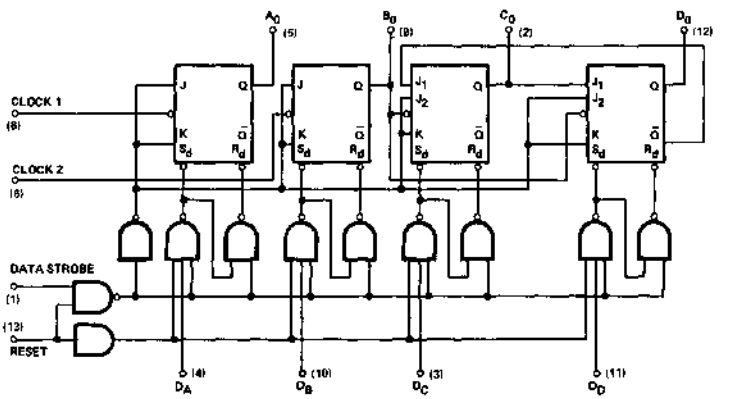
The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset functions are asynchronous with respect to the clock.

TRUTH TABLE*

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

*Connected for Divide-by-Twelve operation (output A connected to CP2)

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7) A,F PACKAGES
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V		Output A	-800μA	6, 7
"0" Output Voltage			0.4V	V	0.8V	0.8V	0.8V		Output A	16mA	6, 8
"0" Input Current											
Data Strobe	-0.1		-1.6	mA	0.4V		5.25V				
Data Inputs	-0.1		-1.2	mA		0.4V					
Reset	-0.1		-3.2	mA	5.25V		0.4V				
Clock 1	-0.1		-3.2	mA				0.4V			
Clock 2	-0.1		-1.6	mA					0.4V		
"1" Input Current											
Data Strobe			40	μA	4.5V		0V				
Data Input			40	μA		4.5V					
Reset			80	μA			4.5V				
Clock 1			80	μA				4.5V			
Clock 2			80	μA					4.5V		
Power/Current Consumption		184/35	236/45	mW/mA			0V	0V	0V		11
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				
Output Short Circuit Current	-10		-60	mA	0V					0V	10, 11

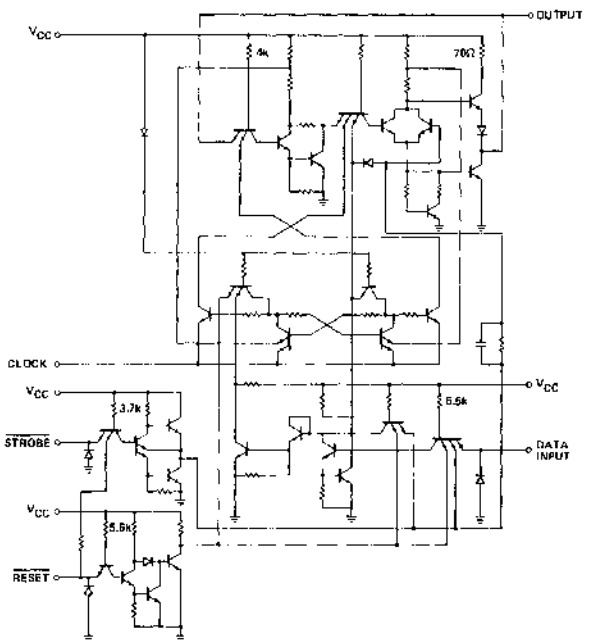
T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Clock Mode t_{on} Delay											
Bit A, B, C, D		15	25	ns							9
Clock Mode t_{off} Delay											
Bit A, B, C, D		15	25	ns							9
Data/Strobe t_{on} Delay											
Bit A, B, C, D		20	35	ns							9
Data/Strobe t_{off} Delay											
Bit A, B, C, D		25	40	ns							9
Toggle Rate	20	25		MHz							9
Strobe Hold Time		25	35	ns		0.8V	2.0V	2.0V	Output A		
Reset Hold Time		20	35	ns	2.0V	0.8V		2.0V	Output A		
Strobe Release Time		30	40								
Reset Release Time		50	75	ns							

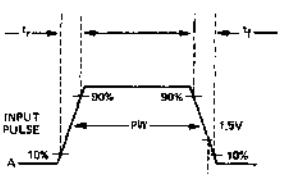
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Not more than one output should be shorted at a time.
11. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM

8288 BASIC BINARY



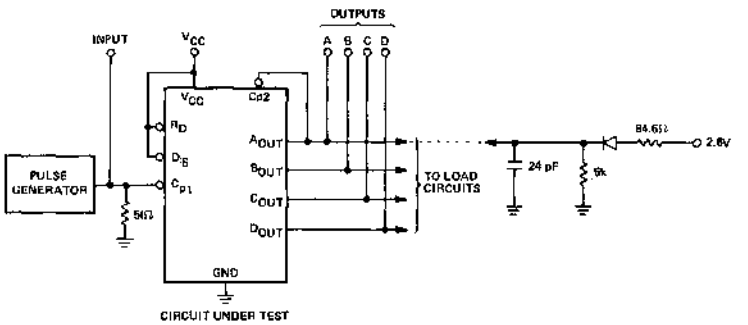
AC TEST FIGURES AND WAVEFORMS

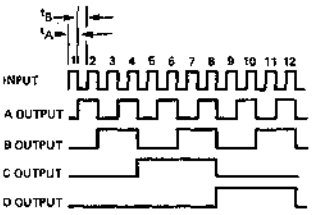


NOTE: Input pulse notations apply unless otherwise specified.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

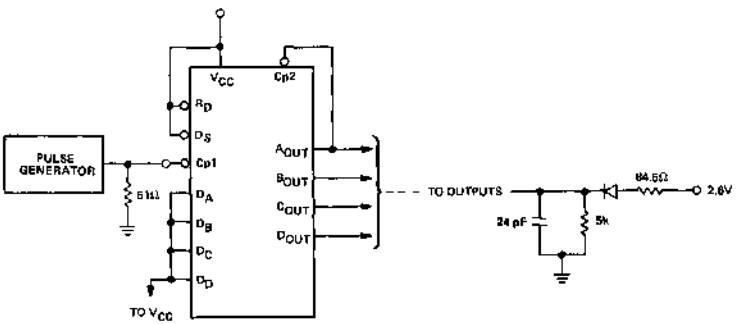
TOGGLE RATE

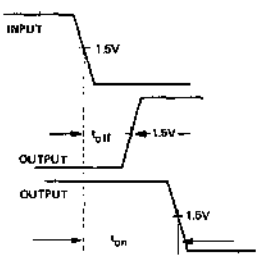




INPUT PULSE:
Amplitude = 3.4V
t_A = 100ns
t_r = 20ns
t_B = 300ns

CLOCK MODE t_{on}/t_{off} DELAY



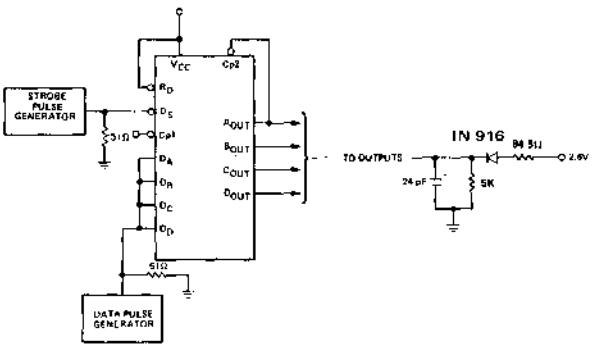


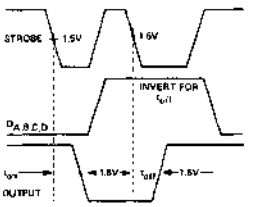
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns
$t_r = t_f$ = 5ns

AC TEST FIGURES AND WAVEFORMS (Cont'd)

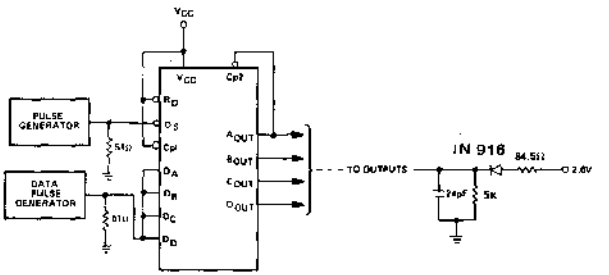
DATA/STROBE t_{on} t_{off}

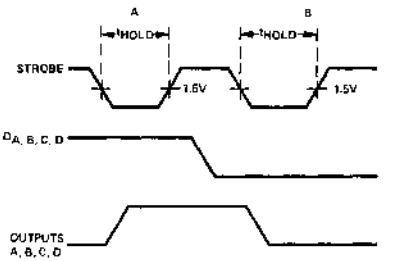




INPUT PULSE
AMPLITUDE=2.6V
t_r=t_f=5ns

STROBE HOLD TIME

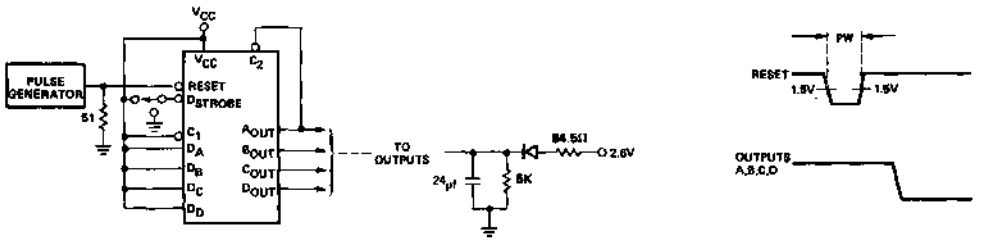




INPUT PULSE
AMPLITUDE=2.6V
t_r=t_f=5ns

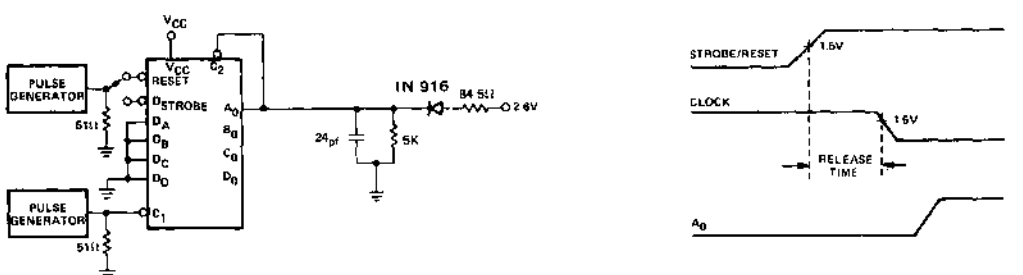
AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM RESET PULSE WIDTH



INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.
Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME



Clock, Strobe/Reset Amplitude = 2.6V
$t_r = t_f$ = 5ns max. PRR = 1MHz 50% Duty Cycle.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.

signetics

PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER

8290
8291

A,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8290 Decade Counter and 8291 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8291 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

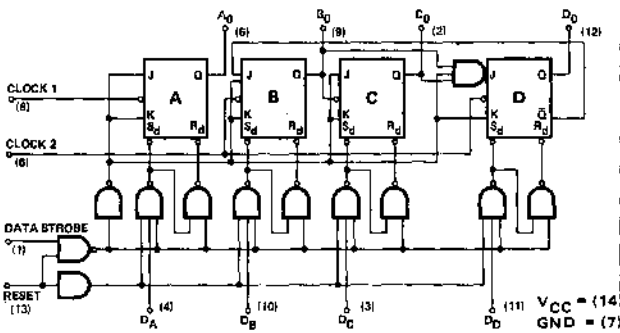
The counting operation is performed on the falling (negative going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

LOGIC DIAGRAMS AND TRUTH TABLES

8290

Bi-Quinary (5-2)				
Input	B_0	C_0	D_0	A_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	1

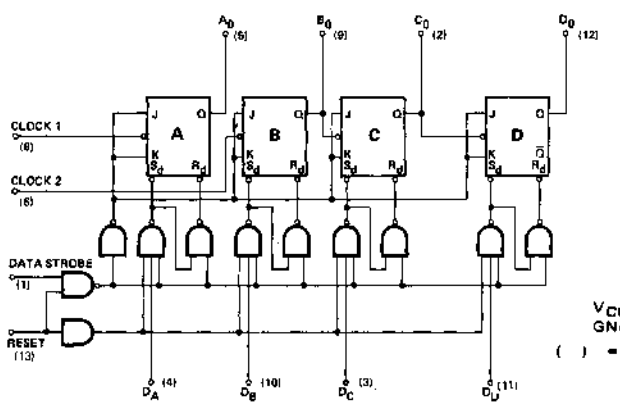


Decade (BCD)				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

8291

Binary				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V			-200μA	6, 7
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V			9.6mA	6, 8
"0" Input Current											
Data Strobe	-0.1		-1.6	mA	0.4		5.25V				
Data Inputs	-0.1		-1.2	mA		0.4					
Reset	-0.1		-2.8	mA	5.25V		0.4				
Clock 1	-0.1		-4.8	mA	5.25V			0.4			
Clock 2 (8290)	-0.1		-4.8	mA	5.25V				0.4		
Clock 2 (8291)	-0.1		-2.4	mA	5.25V				0.4		
"1" Input Current											
Data Strobe			40	μA	4.5V		0.0V				
Data Inputs			40	μA		4.5V					
Reset			80	μA	0.0V		4.5V				
Clock 1			80	μA	0.0V			4.5V			
Clock 2 (8290)			120	μA	0.0V				4.5V		
Clock 2 (8291)			80	μA	0.0V				4.5V		
Output Short Circuit Current A	-20		-70	mA						0.0V	10, 12
B, C, D	-10		-60	mA	0.0V					0.0V	10, 12
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Clock 1 & 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				

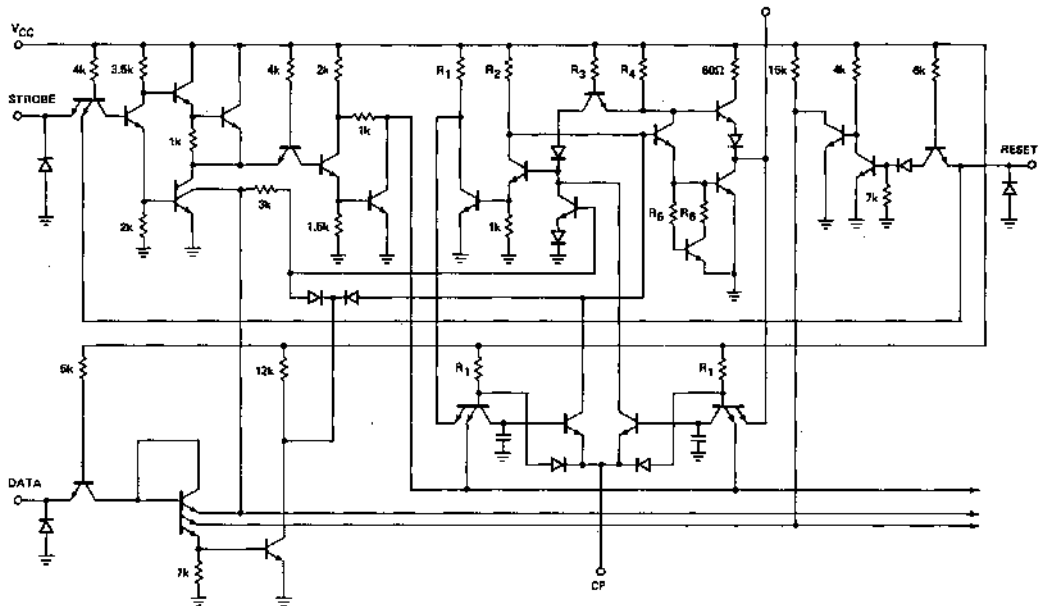
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Power Consumption/		190/	256/	mW/			0.0V	0.0V	0.0V		12
Supply Current		36.5	48.5	mA							
Strobe Pulse Width		15		ns					A_{OUT}		9
Reset Pulse Width		25		ns					A_{OUT}		9
Strobe/Reset Release Time		20		ns					A_{OUT}		9
Clock Mode t_{on} Delay											
Bit A		12	25	ns							9
Bits B, C, D		15	30	ns							9
Clock Mode t_{off} Delay											
Bit A		12	23	ns							9
Bits B, C, D		15	25	ns							9
Strobed Data t_{on} Delay											
(All Bits)		31	42	ns							9
Strobed Data t_{off} Delay											
(All Bits)		33	42	ns							9
Toggle Rate	40	60		MHz							9
Clock Mode Switching Test			75	ns							9, 11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Not more than one output should be shorted at a time.
11. This test guarantees the device will reliably trigger on a pulse with 75ns fall-time.
12. $V_{CC} = 5.25V$.

SCHEMATIC DIAGRAM

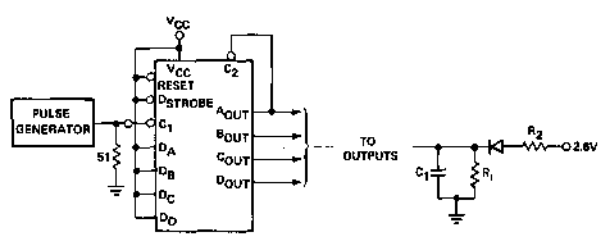


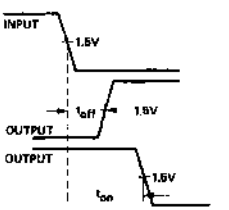
RESISTOR VALUES

	BIT A	BIT B,C,D
R_1	2.5k	5k
R_2	3.2k	5.5k
R_3	2k	5k
R_4	800Ω	3.5k
R_5	45Ω	355Ω
R_6	200Ω	1.15k

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY



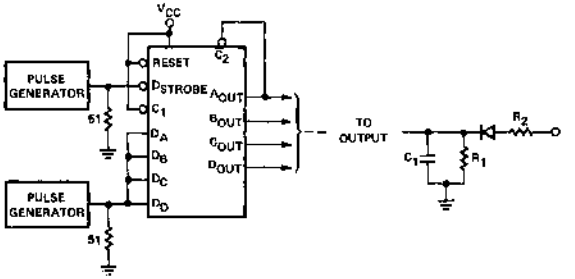


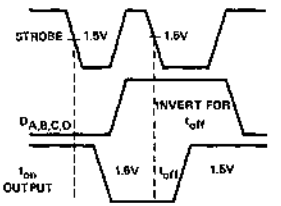
Note:
t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

INPUT PULSE:
Amplitude = 2.6V
PW = 30ns, 50% to 50%
$t_r = t_f = 5ns$
PRR = 1MHz

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBED DATA t_{on}/t_{off} DELAY

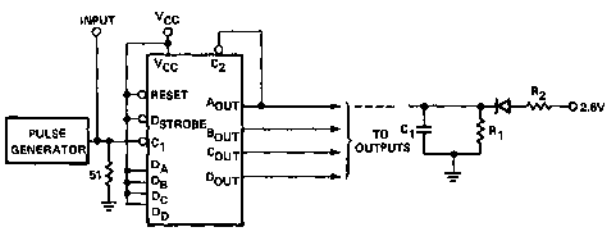




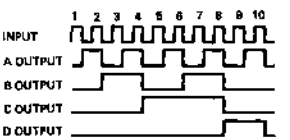
STROBE, PA = 2.6V
PW = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f = 5ns$

DATA, PA = 2.6V
PW = 500ns, 50% to 50%
PRR = 500kHz
$t_r = t_f = 5ns$

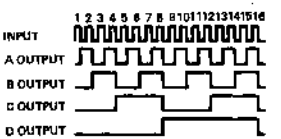
CLOCK MODE SWITCHING TEST



8290



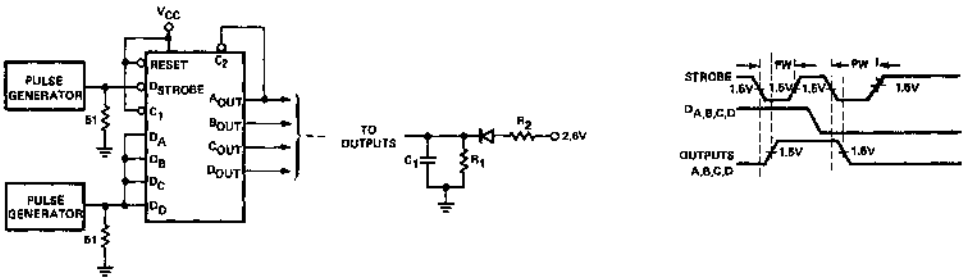
8291



INPUT PULSE:
Amplitude = 3.4V
PW = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns, t_f = 78ns

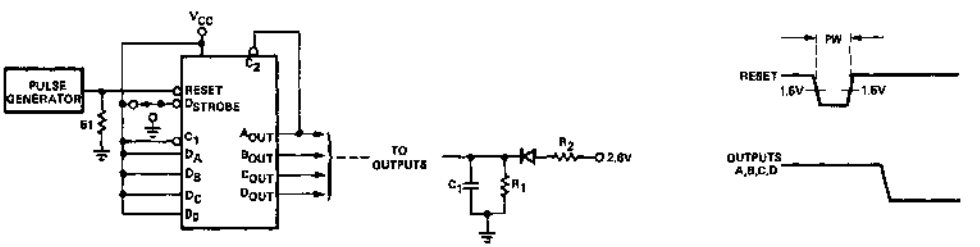
AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM STROBE PULSE WIDTH



INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f = 6ns$

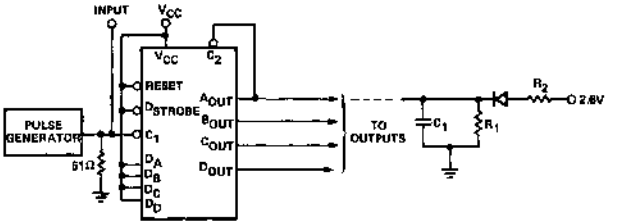
MINIMUM RESET PULSE WIDTH

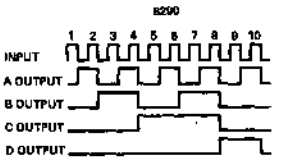


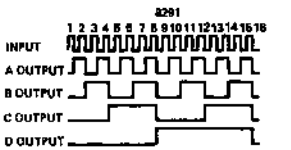
INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f = 6ns$.
Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

TOGGLE RATE

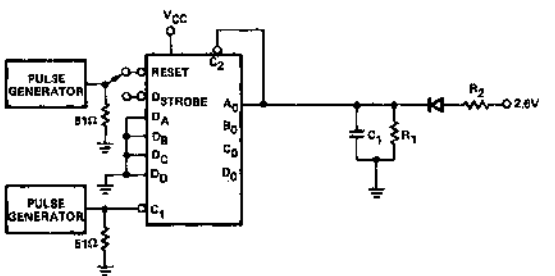


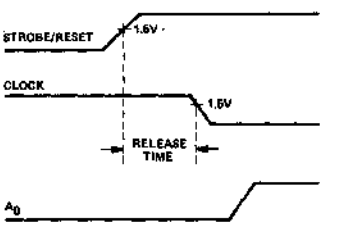




INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 6ns max.
PRR = 40MHz, 50% duty cycle.

STROBE/RESET RELEASE TIME





NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.
4. R1 = 20k, R2 = 146Ω, C1 = 30pF.

signetics

PRESETTABLE LOW POWER DECADE/BINARY COUNTER

8292
8293

A,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8293 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.
The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

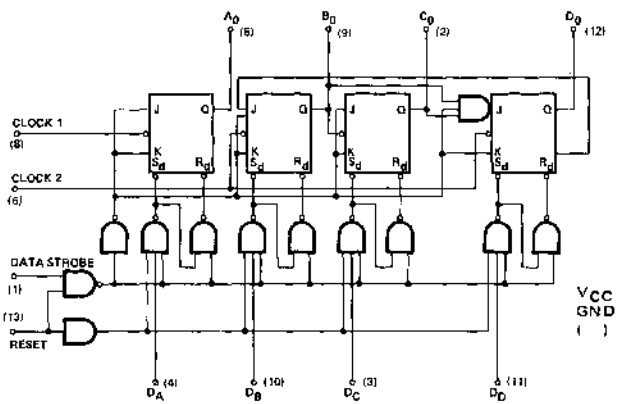
Triggering requirements are compatible with any of the 8000 Series elements.

LOGIC DIAGRAMS AND TRUTH TABLES

8292

Bi-Quinary (5-2)

Input	B_0	C_0	D_0	A_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	1



Decade (BCD)

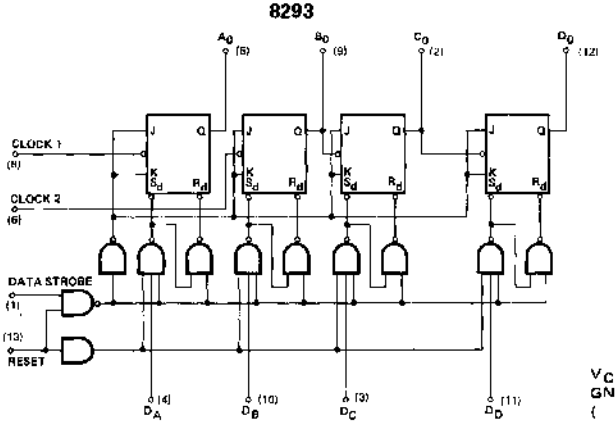
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

8293

Binary

Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.6		V	0.8V	2.0V	2.0V		A_{OUT}	−100μA	6,8
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V		A_{OUT}	3.2mA	6,9
"0" Input Current											
Data Strobe	-0.1		-0.4	mA	0.4V		5.25V				
Data Inputs	-0.1		-0.4	mA		0.4V					
Reset	-0.1		-0.6	mA	5.25V		0.4V				
Clock 1	-0.1		-0.6	mA	5.25V			0.4V			
Clock 2 (8292)	-0.1		-1.2	mA	5.25V				0.4V		
Clock 2 (8293)	-0.1		-0.6	mA	5.25V				0.4V		
"1" Input Current											
Data Strobe			20	μA	4.5V		0.0V				
Data Inputs			20	μA		4.5V					
Reset			40	μA	0.0V		4.5V				
Clock 1			40	μA	0.0V			4.5V			
Clock 2 (8292)			80	μA	0.0V				4.5V		
Clock 2 (8293)			40	μA	0.0V				4.5V		
Output Short Circuit Current	-5		-45	mA	0.0V					0.0V	7, 13
Input Voltage Rating											
Data Strobe					10mA						
Clock 1 and 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				

$T_A = 25°C$ and $V_{CC} = 5.0V$

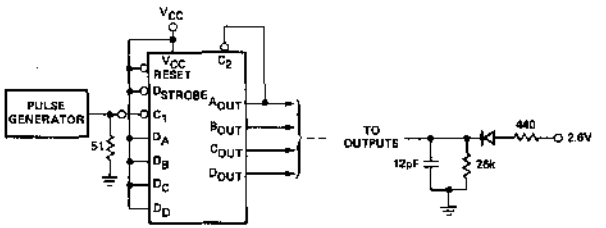
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Power/Current Consumption		52.5/ 10	69/ 13.1	mW/ mA			0.0V	0.0V	0.0V		13
Clock Mode t_{on} Delay (All Bits)		37	55	ns							10
Clock Mode t_{off} Delay (All Bits)		32	55	ns							10
Strobed Data t_{on} Delay (All Bits)		80	100	ns							10
Strobed Data t_{off} Delay (All Bits)		80	100	ns							10
Clock Mode Switching Test			75	ns							12
Strobe Pulse Width		60	75	ns		0.8V	2.0V	2.0V	A_{OUT}		
Reset Pulse Width		45	60	ns		2.0V	2.0V	2.0V	A_{OUT}		
Strobe/Reset Release Time		80		ns					A_{OUT}		
Toggle Rate	5	10		MHz							

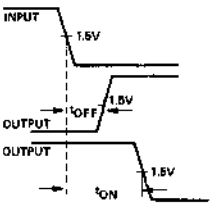
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Not more than one output should be shorted at a time.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Refer to AC Test Figure.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. This test guarantees the device will reliably trigger on a pulse with a 75ns fall-time or less.
13. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY

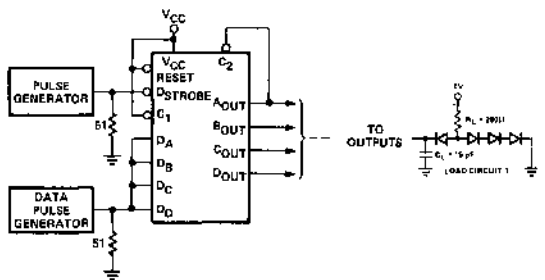


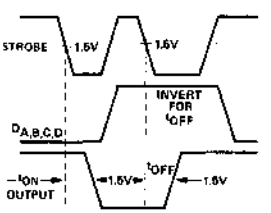


INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns, 50% to 50%
$t_r = t_f = 5ns$
PRR = 1MHz

NOTE:
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

STROBED DATA t_{on}/t_{off} DELAY



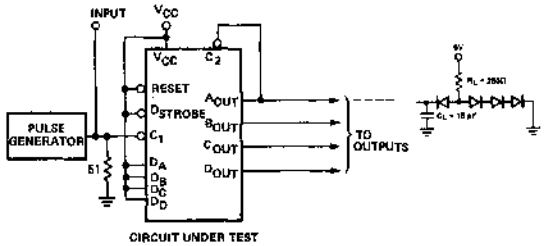


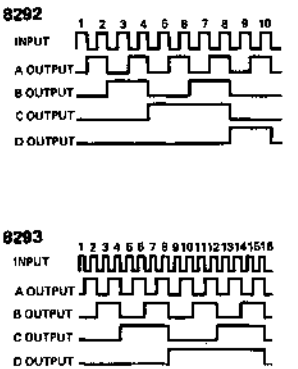
Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f = 5ns$

Data,
P.A. = 2.6V
P.W. = 600ns, 50% to 50%
PRR = 500KHz
$t_r = t_f = 5ns$

AC TEST FIGURES AND WAVEFORMS (Cont'd)

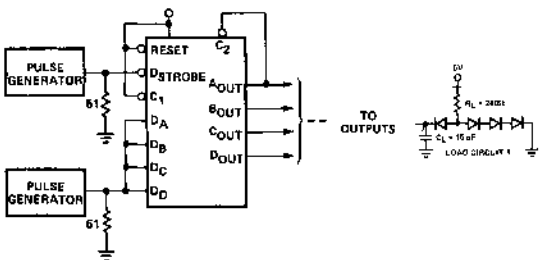
CLOCK MODE SWITCHING TEST

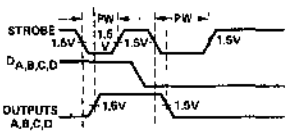




INPUT PULSE:
Amplitude = 3.4V
P.W. = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns
t_f = 75ns

MINIMUM STROBE PULSE WIDTH

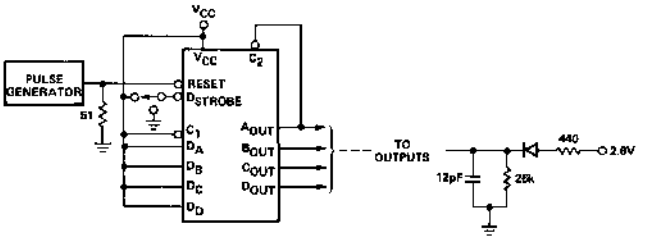


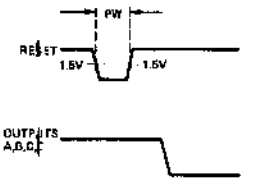


INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 6ns max.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

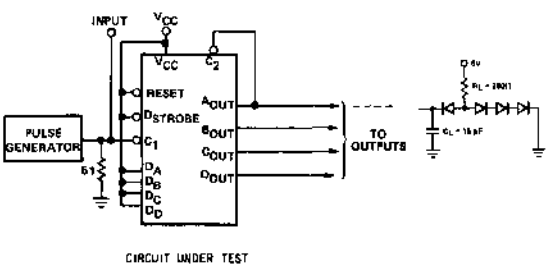
MINIMUM RESET PULSE WIDTH

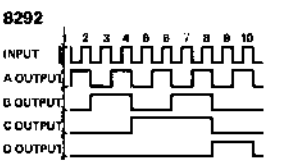


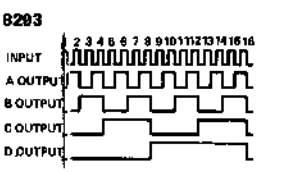


INPUT PULSE:
Amplitude 2.6V
$t_r = t_f$ = 5ns max.
NOTE: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

TOGGLE RATE



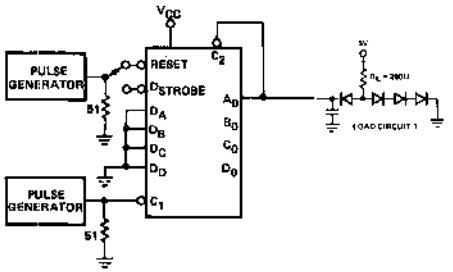


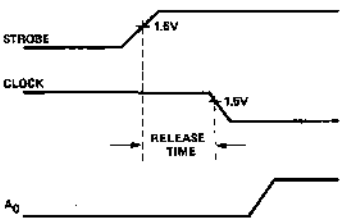


INPUT PULSE:
Amplitude = 2.6V
PRR = 6MHz, 50% duty cycle
$t_r = t_f$ = 6ns max.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBE/RESET RELEASE TIME





CLOCK, STROBE/RESET:
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f$ = 6ns max.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.

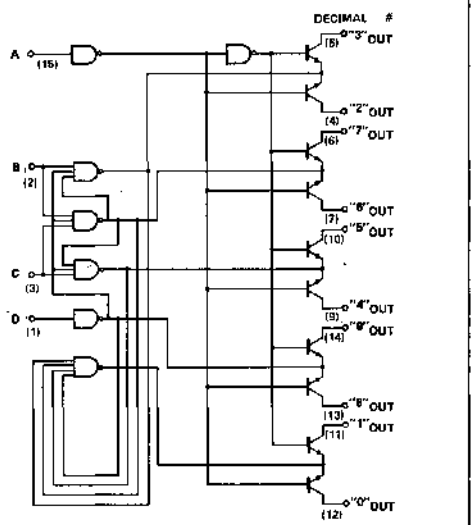
DESCRIPTION

The 8T01 Nixie* Decoder/Driver is a one-out-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes.

It may also be utilized in driving relays or other high voltage interface circuitry. The element is designed using TTL techniques and is therefore completely compatible with DTL and TTL elements.

The specially designed output drivers provide the necessary stable output state. There are no input codes where all outputs are "off" or where more than one output can be turned "on."

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	8
1	0	1	1	9
1	1	0	0	8
1	1	0	1	9
1	1	1	0	8
1	1	1	1	9

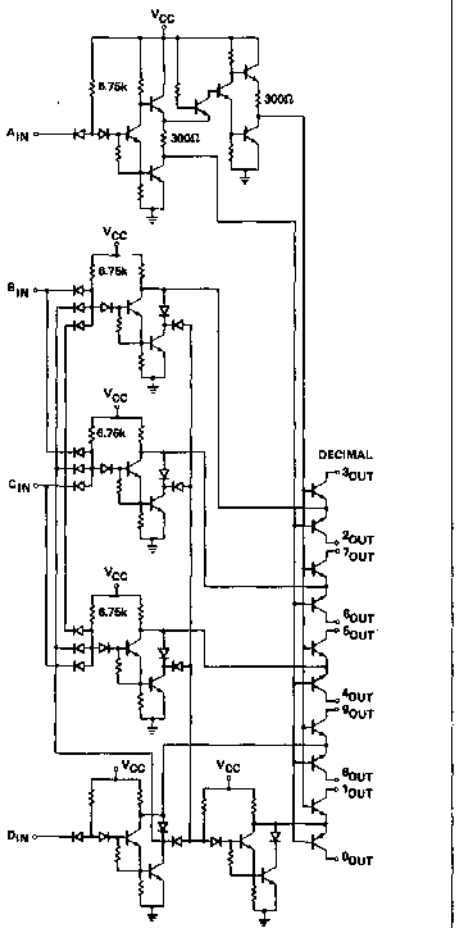
ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	
	MIN.	TYP.	MAX.	UNITS	INPUTS	OUTPUTS
"1" Output Voltage	6.8			V	0.8V	1.0mA
"0" Output Voltage			2.75	V	2.2V	5.0mA
"1" Input Current			40	µA	4.5V	
"0" Input Current (A and D)			-0.9	mA	0.4V	
"0" Input Current (B and C)			-1.8	mA	0.4V	
Power/Current Consumption (V_{CC} = 5.25V)		63/12	147/28	mW/mA		

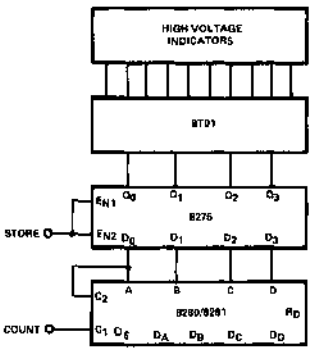
NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with Pin 8 tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. S8T01B operating temperature range is -20°C to +85°C.

SCHEMATIC DIAGRAM



TYPICAL APPLICATIONS



8T01 is used to decode output of 8280 or 8281 counter and drive NIXIE* indicator tubes.
An 8275 Quad-Latch is used as an intermediate storage register.

*A trademark of the Burroughs Corporation.

DESCRIPTION

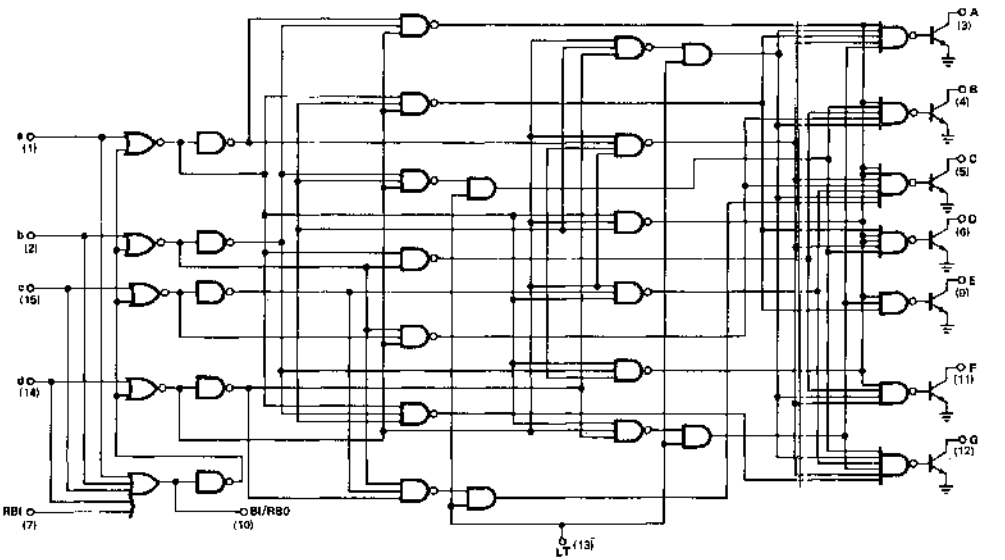
The 8T04 consists of the necessary logic to decode a 4-bit BCD code to seven segment (0 through 9) readout, as well as some selected signs and letters.

Incorporated in this device is a blanking circuit which turns all segments off when activated. The blanking circuit allows suppression of all numerically insignificant zeros, thereby presenting an easily read display.

Also included is the necessary circuitry to implement suppression of leading and/or trailing zeros. A Lamp Test control is provided to turn all segments on. The Lamp Test allows the viewer to check the validity of the display lamps.

High performance bare collector output transistors are used in the 8T04 for directly driving incandescent lamps or common anode LED displays.

LOGIC DIAGRAM



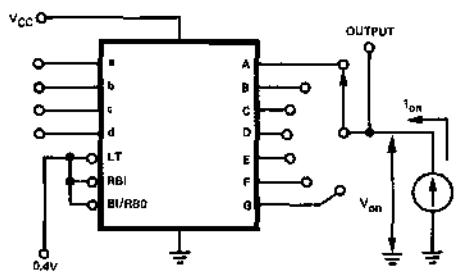
V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	LT	RBI	RBO BI	DRIVEN INPUTS	OUTPUTS	
"1" Output Voltage RBO	3.1			V			-160μA			7, 9
"0" Output Voltage										
RBO			0.4	V		0.8V	4.8mA	0.8V		8, 9
A-G			0.50	V	0.4V	0.4V	0.4V		40mA	8, 9
"1" Output Leakage Current (A-G)			100	μA		0.8V			6.0V	9, 10
"1" Input Current										
RBI			40	μA		4.5V				
LT			160	μA	4.5V					
All Other Inputs			80	μA		4.5V	4.5V	4.5V		
"0" Input Current										
RBI	-.1		-1.2	mA		0.4V				
BI	-.1		-2.2	mA			0.4V			
LT	-.1		-10	mA	0.4V					
All Other Inputs	-.1		-1.6	mA	0.4V			0.4V		
Input Voltage Rating	5.5			V			10mA			11
Power/Current Consumption:										
"S" Temperature Range			394/75	mW/mA						11
"N" Temperature Range			446/85	mW/mA						11

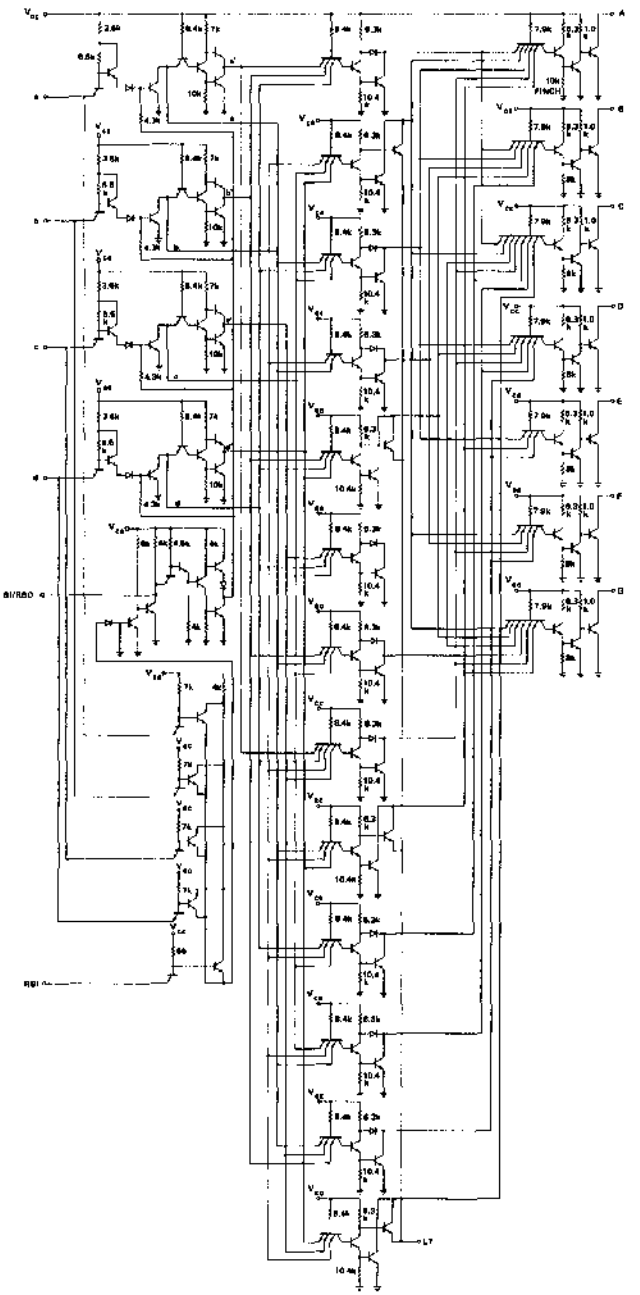
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. See truth table: "1" Threshold = 2.0V for a,b,c,d.
   "0" Threshold = 0.8V for a,b,c,d.
10. Connect an external 1k ±1% resistor to the output for this test.
11. V_{CC} = 5.25V.

TEST FIGURE FOR "0" OUTPUT VOLTAGE



Each output is tested separately in the ON state.

SCHEMATIC DIAGRAM



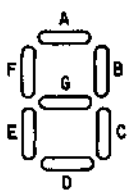
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		NOTE	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	0	0	0	0	0	0	0	8
X	X	X	X	1	X	0 (Note 1 & 2)	1	1	1	1	1	1	1	BLK
0	0	0	0	1	0	0 (Note 2)	1	1	1	1	1	1	1	BLK
0	0	0	0	1	1	1	0	0	0	0	0	0	1	0
0	0	0	1	1	X	1	1	0	0	1	1	1	1	1
0	0	1	0	1	X	1	0	0	1	0	0	1	0	2
0	0	1	1	1	X	1	0	0	0	0	1	1	0	3
0	1	0	0	1	X	1	1	0	0	1	1	0	0	4
0	1	0	1	1	X	1	0	1	0	0	1	0	0	5
0	1	1	0	1	X	1	1	1	0	0	0	0	0	6
0	1	1	1	1	X	1	0	0	0	1	1	1	1	7
1	0	0	0	1	X	1	0	0	0	0	0	0	0	8
1	0	0	1	1	X	1	0	0	0	1	1	0	0	9
1	0	1	0	1	X	1	1	1	1	1	1	1	0	-
1	0	1	1	1	X	1	1	1	1	1	1	1	1	BLK
1	1	0	0	1	X	1	0	0	0	1	0	0	0	°
1	1	0	1	1	X	1	1	1	0	1	1	1	1	'
1	1	1	0	1	X	1	1	1	1	0	0	0	1	L
1	1	1	1	1	X	1	1	1	1	1	1	1	1	BLK

*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.



DESCRIPTION

The 8T05 consists of the necessary logic to decode a 4-Bit BCD code to seven segment (0 through 9) readout as well as some selected signs and letters.

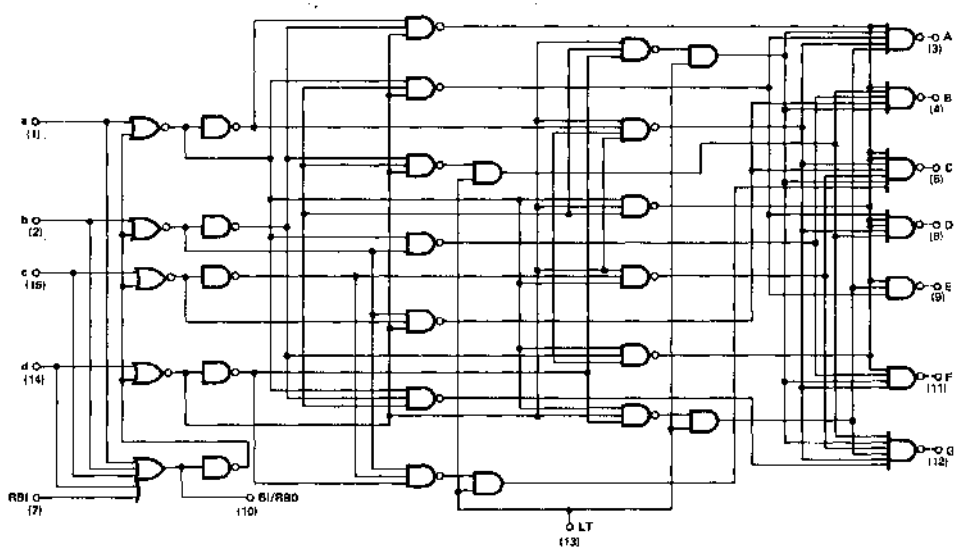
A Ripple Blanking input is provided to implement suppression of leading and/or trailing zeros. The suppression of all numerically insignificant zeros provides an easily read display.

Incorporated in the Ripple Blanking output (BI/RBO) is the facility to ground all the outputs. Blanking of the outputs allows for intensity modulation.

A Lamp Test input is provided which, when grounded forces all segment outputs high. This allows the viewer to check the validity of the display presentation by testing the integrity of the lamps.

The 8T05 has resistor pullups on the outputs to provide source current sufficient to drive interfacing elements. This allows the unit to drive high voltage transistors for neon displays. The 8T05 can also be used to drive common cathode LED displays at moderate light intensity levels.

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

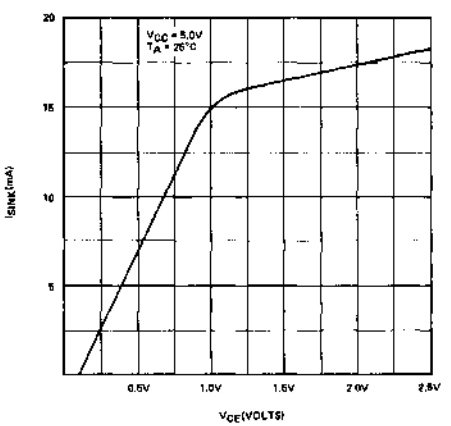
CHARACTERISTICS	LIMITS				LT	TEST CONDITIONS			OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS		RBI	RBO BI	DRIVEN INPUTS		
A-G "1" Output Voltage	3.9			V	0.4V				-500μA	7, 9
A-G Output Source Current	-2.3			mA	0.4V				1.0V	
A-G "0" Output Voltage			0.3	V	4.5V	0.4V	0.4V		+500μA	8, 9
RBO "1" Output Voltage	3.1			V			-160μA			7, 9
RBO "0" Output Voltage			0.4	V		0.8V	4.8mA	0.8V		8, 9
"1" Input Current										
RBI			40	μA		4.5V				
LT			160	μA	4.5V					
All other Inputs			80	μA		4.5V	4.5V	4.5V		
"0" Input Current										
RBI	-.1		-1.2	mA		0.4V				
BI	-.1		-2.2	mA			0.4V			
LT	-.1		-1.0	mA	0.4V					
All Other Inputs	-.1		-1.6	mA				0.4V		
Input Voltage Rating	5.5			V				10mA		
Power/Current Consumption:										
"S" Temperature Range			394/75	mW/mA						10
"N" Temperature Range			110/85	mW/mA						10

NOTES:

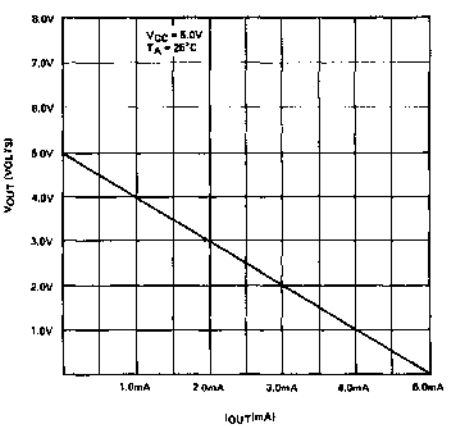
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. See truth table: "1" Threshold = 2.0V for a,b,c,d. "0" Threshold = 0.8V for a,b,c,d.
10. V_{CC} = 5.25V.

TYPICAL CHARACTERISTIC CURVES

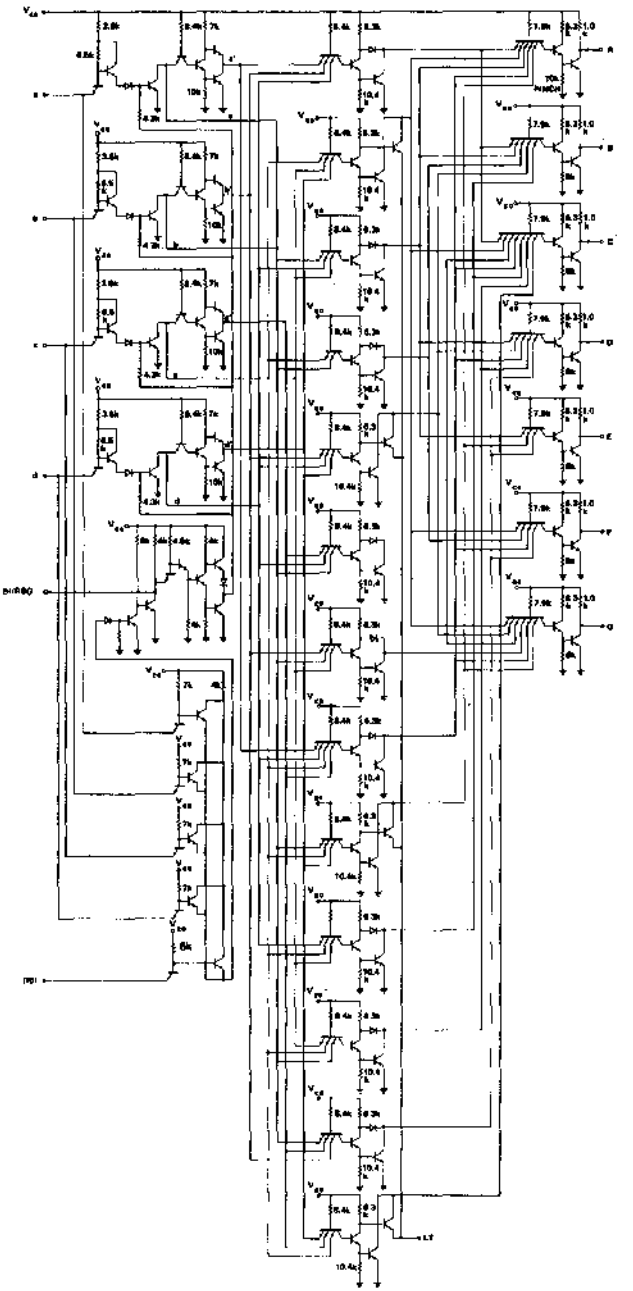
TYPICAL CURRENT SINK CAPABILITY VERSUS V_{CE}(SAT) (OUTPUTS A-G)



TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUTS A-G)



SCHEMATIC DIAGRAM



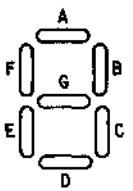
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 (Note 1 & 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 (Note 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	-
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	R
1	1	0	1	1	X	1	0	0	1	0	0	0	0	r
1	1	1	0	1	X	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

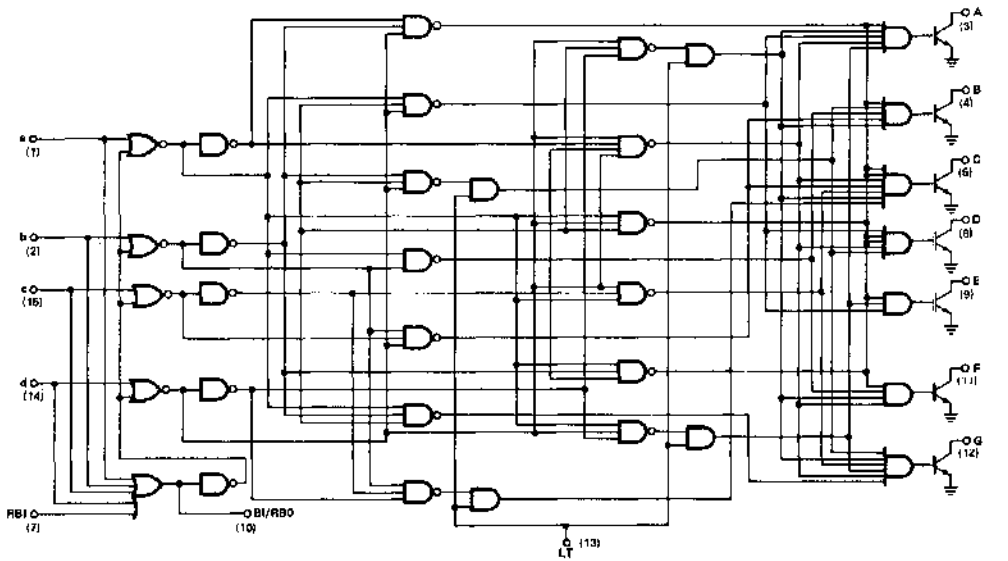
NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a, b, c, d, RBI terminals are low, or damage may occur to the unit.



DESCRIPTION

The 8T06 is a monolithic MSI circuit consisting of the necessary logic to decode a 4-bit BCD code to drive 7-segment indicators directly. Open-collector outputs are used for high current source applications, such as driving common cathode LED displays and discrete active components. The 8T06 seven segment decoder/driver accepts a 4-bit binary code and decodes all possible inputs as decimals 0-9 or selected signs and letters. Auxiliary inputs are provided for maximum versatility. The ripple blanking inputs (RBI) and the ripple blanking output (RBO) may be used for automatic leading and/or trailing-edge zero suppression. The RBO output also acts as an overriding blanking input (BI) which may be used for intensity modulation or strobing of the display. A lamp test (LT) input is provided to check the integrity of the display by activating all outputs independent of the input code.

LOGIC DIAGRAM



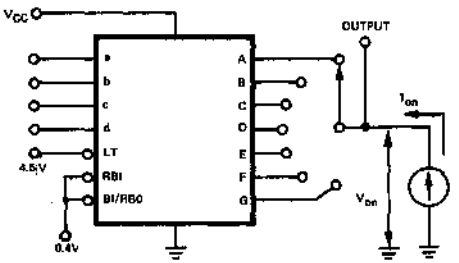
V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	LT	RBI	RBO BI	DRIVEN INPUTS	OUTPUTS	
"1" Output Voltage										
RBO	3.1			V			-160μA			7, 9
"0" Output Voltage										
(A-G)			0.5	V	4.5V	0.4V	0.4V		40mA	8, 9
RBO			0.4	V		0.8V	4.8mA	0.8V		8, 9
"1" Output Leakage Current										
(A-G)			100	μA	0.4V				6.0V	9, 10
"1" Input Current										
RBI			40	μA		4.5V				
LT			160	μA	4.5V					
All Other Inputs			80	μA		4.5V	4.5V	4.5V		
"0" Input Current										
RBI	-.1		-1.2	mA		0.4V				
BI	-.1		-2.2	mA			0.4V			
LT	-.1		-10	mA	0.4V					
All Other Inputs	-.1		-1.6	mA	0.4V	0.4V	0.4V	0.4V		
Input Voltage Rating	5.5			V		10mA		10mA		
Power/Current Consumption:										
"S" Temperature Range			394/75	mW/mA						11
"N" Temperature Range			446/85	mW/mA						11

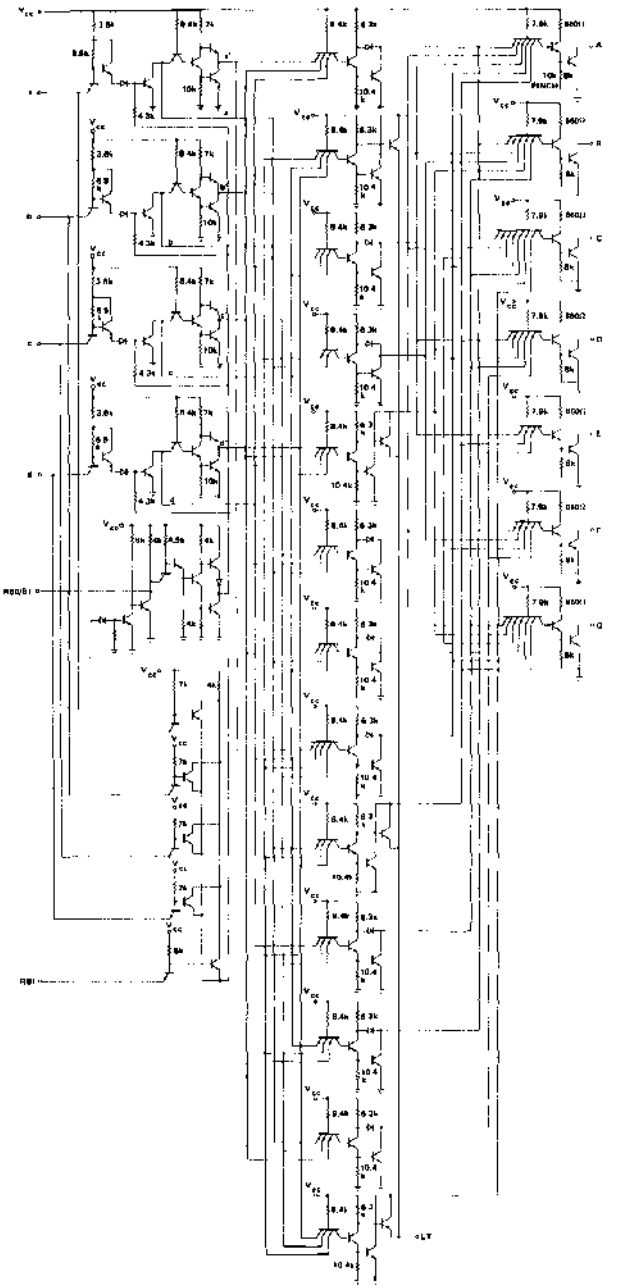
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definitions: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. See truth table: "1" Threshold = 2.0V for a,b,c,d. "0" Threshold = 0.8V for a,b,c,d.
10. Connect an external 1k ±1% resistor to the output for this test.
11. V_{CC} = 5.25V.

TEST FIGURE FOR "0" OUTPUT VOLTAGE



Each output is tested separately in the ON state.

SCHEMATIC DIAGRAM



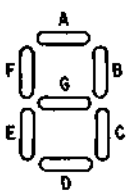
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 (Note 1 & 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 (Note 2)	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	-
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	R
1	1	0	1	1	X	1	0	0	1	0	0	0	0	r
1	1	1	0	1	X	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a, b, c, d, RBI terminals are low, or damage may occur to the unit.

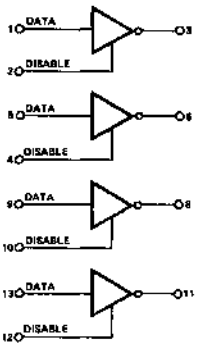


DESCRIPTION

The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The tri-state outputs present a high impedance to the bus when disabled, (control input "1") and active drive when enabled (control input "0"). This eliminates the resistor pull-up requirement while providing performance superior to open collector schemes. Each output can sink 40mA and drive 300pF loading with guaranteed propagation delay less than 22 nanoseconds.

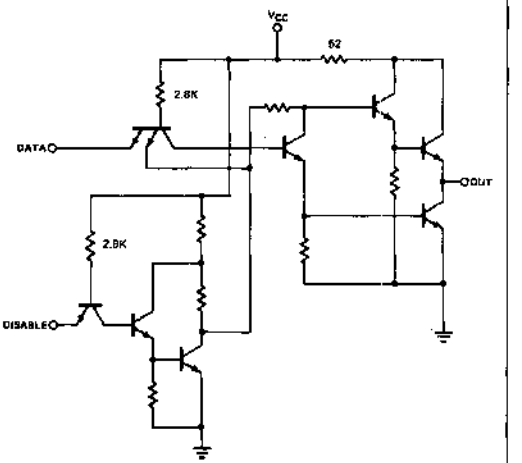
LOGIC DIAGRAM AND TRUTH TABLE



Data	Disable	Output
0	0	1
1	0	0
0	1	Hi- Z
1	1	Hi- Z

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA	DISABLE	OUTPUTS	
"1" Output Voltage	2.4	3.0		V	0.8V	0.8V	-5.2mA	7
"0" Output Voltage		0.2	0.4	V	2.0V	0.8V	40mA	8
Output Leakage Current	-40		+40	μA		2.0V	0.4V or 2.4V	3
"1" Input Current			40	μA		4.5V		
"0" Input Current			-2.0	mA	0.4V	0.4V		
Input Voltage Rating	5.5			V	10mA	10mA		
Power/Current Consumption		236/45	340/65	mW/mA				11
Output Short Circuit Current	-40		-120	mA	0V	0V	0V	10, 11

T_A = 25° C and V_{CC} = 5.0V

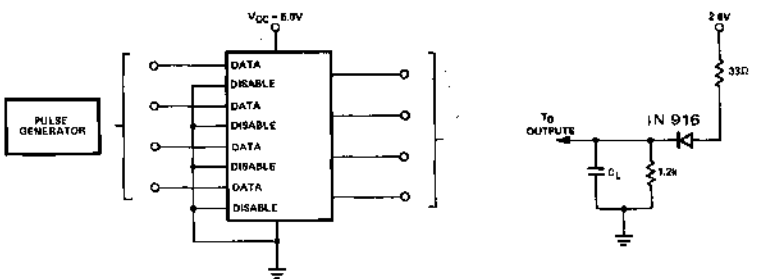
CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA	DISABLE	OUTPUTS	
Propagation Delay								
Data to Output								
t_{on}, t_{off}			10	ns			30pF load	9
			20	ns			300pF load	9
Disable to Output								
High Z to 0, 0 to High Z			14	ns			30pF load	9
			22	ns			300pF load	9
High Z to 1, 1 to High Z			14	ns			30pF load	9
			22	ns			300pF load	9

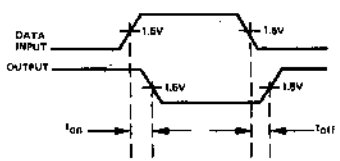
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Not more than one output should be shorted at a time.
11. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

PROPAGATION DELAY (DATA TO OUTPUT)



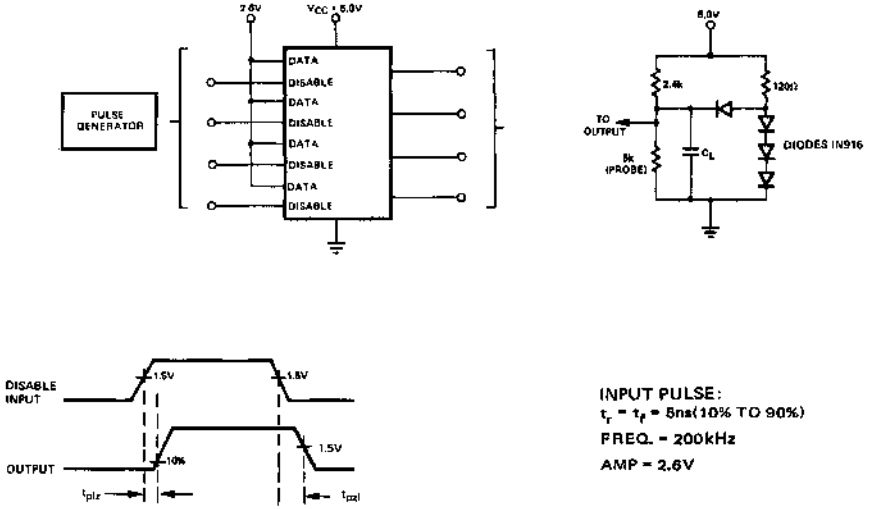


INPUT PULSE:
t_r = t_f = 5ns (10% TO 90%)
FREQ. = 1MHz (50% DUTY CYCLE)
AMP. = 2.6V

FIGURE 1.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

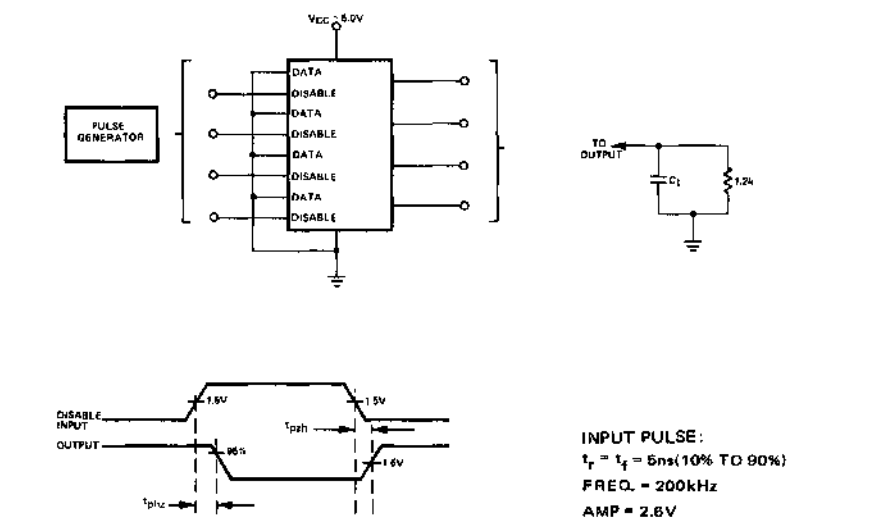
PROPAGATION DELAY
("0" TO HIGH Z, t_{pLz}; HIGH Z TO 0, t_{pzL})



INPUT PULSE:
$t_r = t_f$ = 5ns(10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 2.

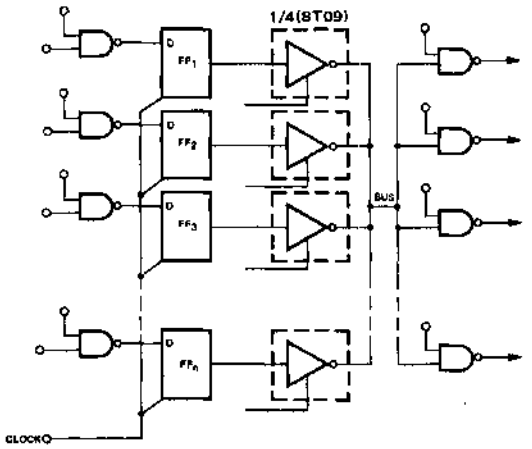
PROPAGATION DELAY
("1" TO HIGH Z, t_{pHz}; HIGH Z to "1", t_{pzH})



INPUT PULSE:
$t_r = t_f$ = 5ns(10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 3.

TYPICAL APPLICATION



The above figure illustrates usage of the 8T09 in data processing logic. For example, FF_1 thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".

DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A common clear input resets all flip-flops upon application of a logic "1" level.

Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

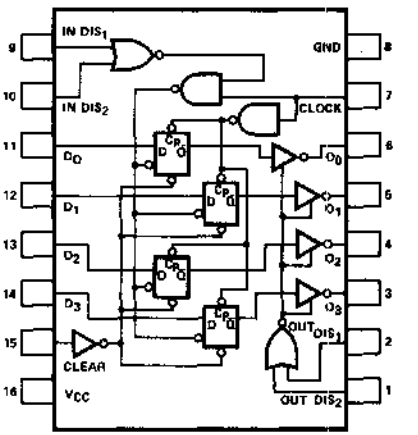
TRUTH TABLE

D_n	IN_{DIS}	OUT_{DIS}	0_{n+1}
0	0	0	0
1	0	0	1
X	1	0	0_n
X	X	1	High Z

0_n refers to the output state before a clock pulse.

0_n + 1 refers to the output state after a clock pulse.

LOGIC DIAGRAM



V_{CC}=16
GND=8

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	IN DIS 1	IN DIS 2	OUT DIS 1	OUT DIS 2	CLEAR	CLOCK	OUTPUT	
"1" Output Voltage	2.4	3.0		V	2.0V	0.8V	0.8V	0.8V	0.8V	0.8V	Pulse	-5.2mA	6
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	Pulse	32mA	7
Output Leakage Current (High Impedance State)	-40		+40	μA		0.8	0.8V	+2.0V	+2.0V	0.8V	Pulse	+0.4V/ +2.4V	
"1" Input Current													
D_n Inputs			40	μA	4.5V	0.4V	0.4V	0.4V	0.4V	0.4V			
All Other Inputs			50	μA		4.5V	4.5V	4.5V	4.5V	4.5V	4.5V		
"0" Input Current													
D_n Inputs	-.100		-3.2	mA	0.4V								
All Other Inputs	-.100		-2.0	mA		0.4V	0.4V	0.4V	0.4V	0.4V	0.4V		
Input Voltage Rating	+5.5V				10mA	10mA	10mA	10mA	10mA	10mA	10mA		

T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	IN DIS 1	IN DIS 2	OUT DIS 1	OUT DIS 2	CLEAR	CLOCK	OUTPUT	
Propagation Delay (t_{on}, t_{off})													
Clock to Output													
C_L = 30pf		18	25	ns									12
C_L = 300pf		24	35	ns									12
Disable to Output													
High Z to Logic 0, t_{pZL} State (C_L = 300pf)		20	30	ns									10, 12
Logic 0 to High Z, t_{pLZ} High Z (C_L = 300pf)		20	30	ns									11, 12
Clear to Output													
C_L = 30pf		15	22	ns									12
C_L = 300pf		21	30	ns									12
Set Up Time, t_{setup}													
Data	+5	-1		ns									12
Input Disable		-6	0	ns									12
Hold Time, t_{hold}													
Data		-1	+5	ns									12
Reset Pulse Width	15			ns									12
Clock Frequency	35	50		MHz									12
Clock Pulse Width													
Positive		8	12	ns									12
Negative		8	12	ns									12
Power/Current Consumption			619/ 118	mW/mA	0.4V	0.4V	0.4V	4.5V	0.4V	0.4V	4.5V		8
Output Short Circuit Current	-40		-120	mA	4.5V	0.4V	0.4V	0.4V	0.4V	0.4V		0.0V	8, 9

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. V_{CC} = 5.25V.
9. Not more than one output should be shorted at a time.
10. Measured to 1.5V level of output waveform.
11. Measured to 10% level of output waveform.
12. Refer to AC Test Circuits.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY t_{on}, t_{off} (CLOCK TO OUTPUT)

DATA SETUP TIME, t_{setup}

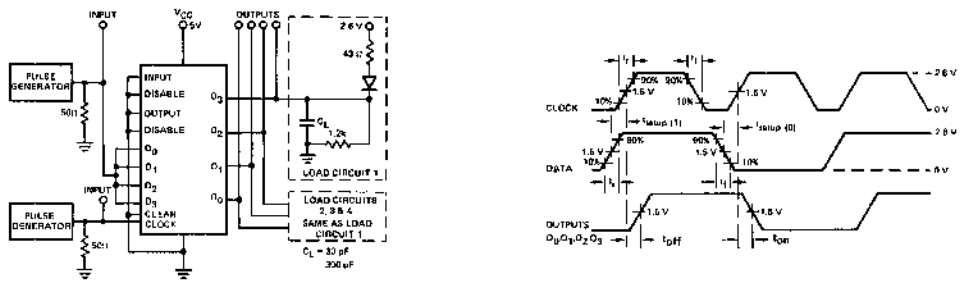


FIGURE 1

AC TEST CIRCUITS AND WAVEFORMS (Cont'd)

PROPAGATION DELAY (CLEAR TO OUTPUT)

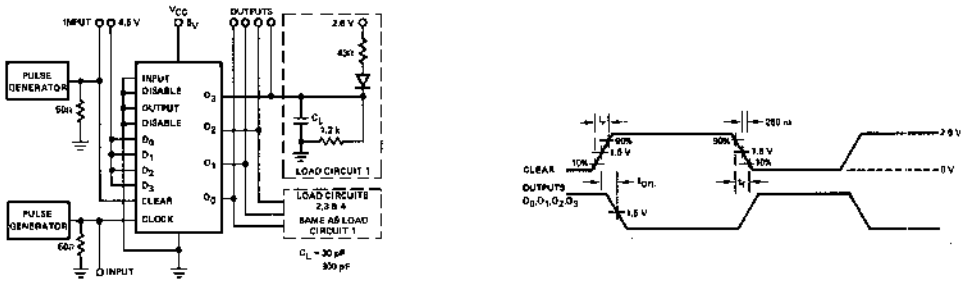


FIGURE 2

PROPAGATION DELAY (DATA HOLD TIME)

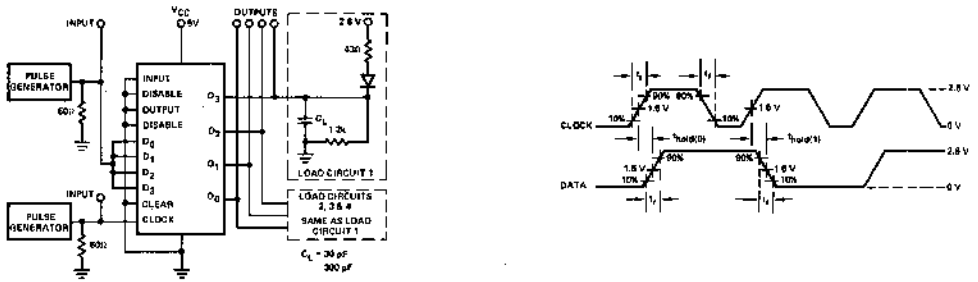


FIGURE 3

PROPAGATION DELAY (DISABLE TO OUTPUT)

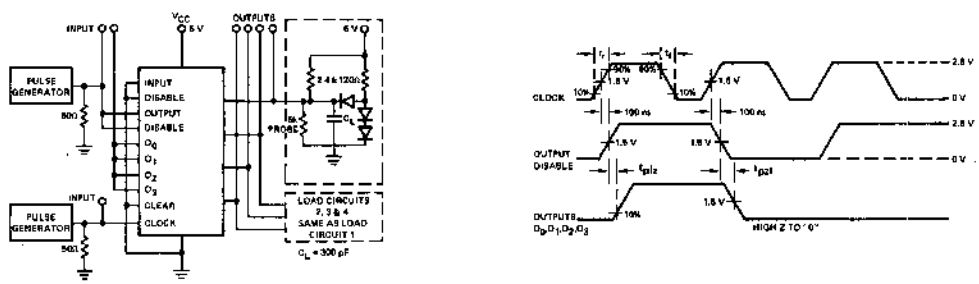
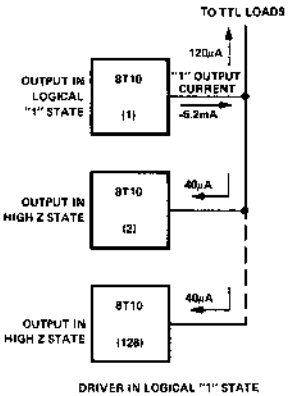
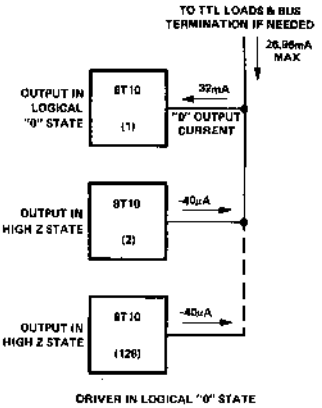


FIGURE 4

TYPICAL APPLICATIONS

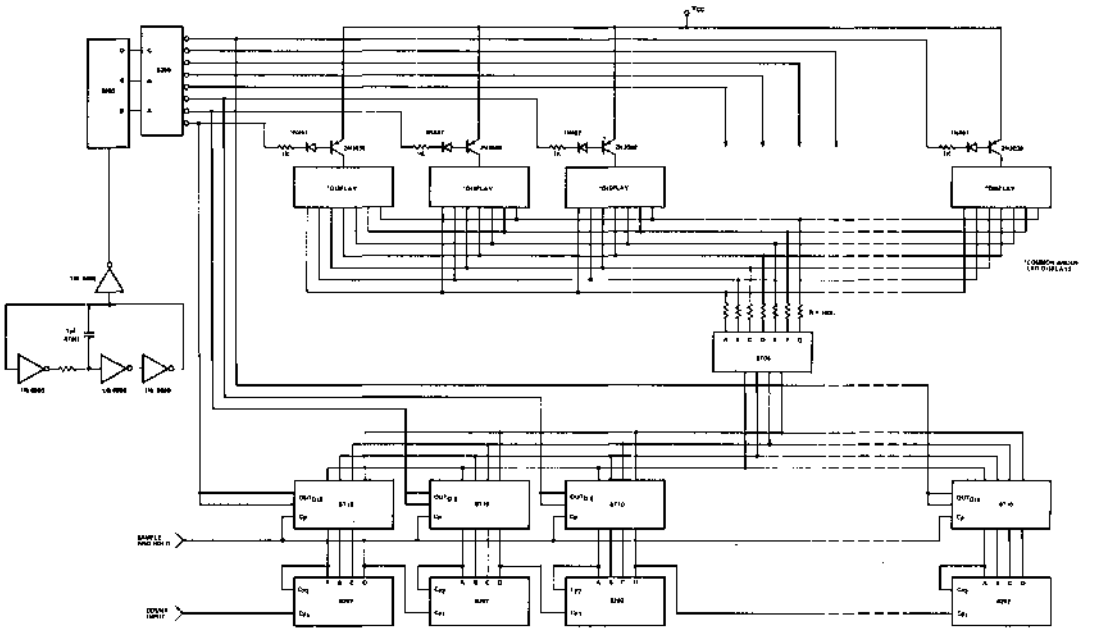


DRIVER IN LOGICAL "1" STATE



DRIVER IN LOGICAL "0" STATE

MULTIPLEXING EIGHT LED DISPLAYS



DESCRIPTION

The 8T13 is a monolithic Dual Line Driver designed to drive 50 ohm or 75 ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ωto 500Ω.

Key Design Benefits:

a. High-Power Drive Capability:
Specified at -75mA source current rating at 2.4 volts.

b. Party-Line Operation:
Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.

c. Input gating structure allows employment of the "OR" as well as the "AND" function.

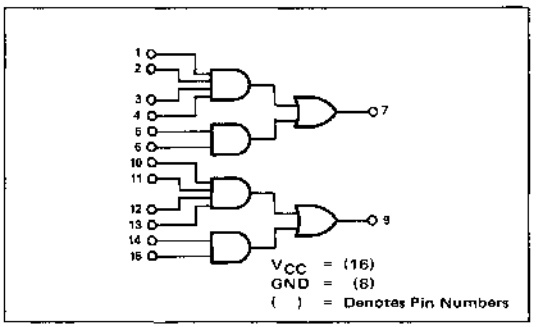
d. High Speed: $t_{on} = t_{off} = 20ns$ (max).

e. Input Clamp Diodes: Protects inputs from line ringing.

f. Single 5 Volt power supply.

g. Short Circuit Protection:
Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source when operating under conditions of zero load resistance.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

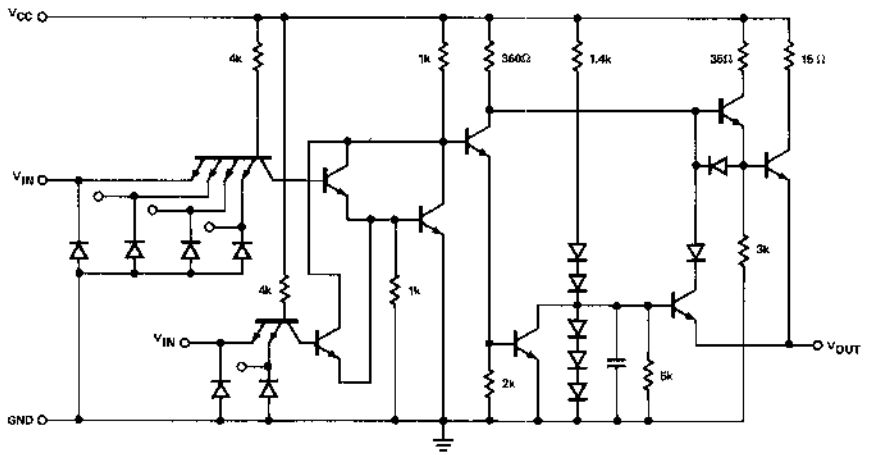
CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE #1		INPUTS OF #2 AND GATE	OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	INPUT UNDER TEST	OTHER INPUTS			
"1" Output Voltage	2.4			V	2.0V	2.0V	0.8V	-75mA	6
"1" Output Leakage Current			80	μA	0V	0V	0V	3.0V	7
"0" Output Leakage Current			-800	μA	0.8V	4.5V	0V	0.4V	
"0" Input Current	-0.1		-1.6	mA	0.4V	4.5V			
"1" Input Current			40	μA	4.5V	0V			

$T_A = 25°C$ and $V_{CC} = 5.0V$

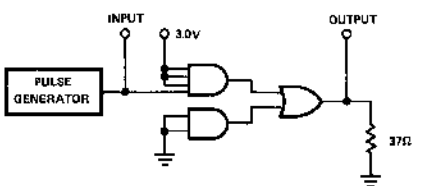
CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	INPUT UNDER TEST	OTHER INPUTS			
Turn-On Delay, t_{on}			20	ns					8, 11
		32		ns					9, 11
Turn-Off Delay, t_{off}			20	ns					8, 11
		22		ns					9, 11
Power/Current Consumption:									
Output at "0"			315/60	mW/mA	0.8V	0.8V	0.8V		10, 13
Output at "1"			150/28	mW/mA	2.0V	2.0V	2.0V		10, 13
Input Voltage Rating	5.5			V	10mA	0V	0V		
"1" Output Current	-100		-250	mA	4.5V	4.5V	0V	2.0V	12
Output Short Circuit Current			-30	mA	4.5V	4.5V	0V	0V	12
Input Clamp Voltage			-1.5	V	-12mA				

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. With forced output voltage of 3 volts no more than 500 μA will enter the driver when output is in "0" state. V_{CC} = 0V.
8. R_L = 37Ω to ground.
9. Load is 37Ω in parallel with 1000pF.
10. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition.
11. Reference AC Test Figure and Pulse Requirements.
12. Reference "Typical Output Current vs Output Voltage Curve."
13. V_{CC} = 5.25 volts, Power Consumption specified for both drivers in package.

SCHEMATIC DIAGRAM

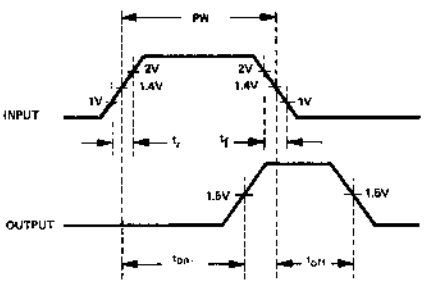


AC TEST FIGURE AND WAVEFORMS

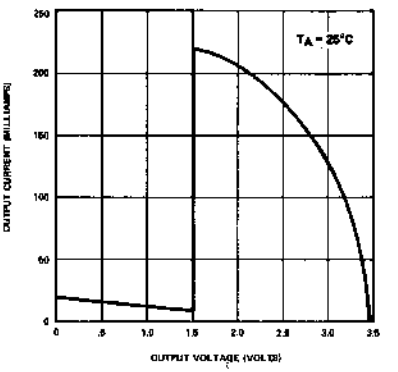


INPUT PULSE:
Amplitude = 3.0V
PW = 40ns (50% Duty Cycle)
t_r = t_f ≤5ns (10% and 90% measurement points)

PULSE REQUIREMENTS



TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE CURVE



TYPICAL APPLICATIONS

A typical application for the 8T13 is shown in Figure 1. If only one line driver is to be used for each transmission line, the line may be terminated with 50 ohms on the receiving end only. See Figure 2.

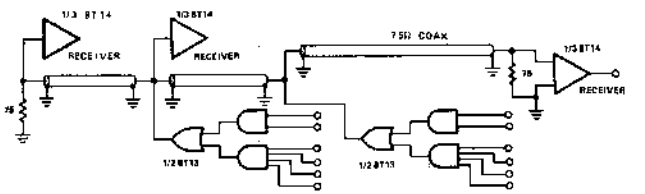


FIGURE 1

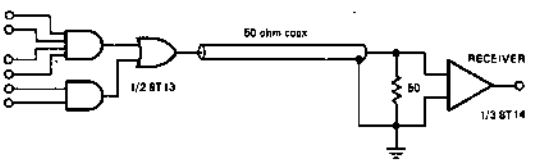


FIGURE 2

signetics

TRIPLE LINE RECEIVER WITH HYSTERESIS

8T14

B,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T14 is a Triple Line Receiver designed for applications requiring digital information to be transmitted over long lengths of coaxial cable, strip line, or twisted pair transmission lines. The Receiver's high impedance input structure (≈30kΩ) presents a minimal load to the driver circuit and allows the transmission line to be terminated in its characteristic impedance to minimize line reflections.

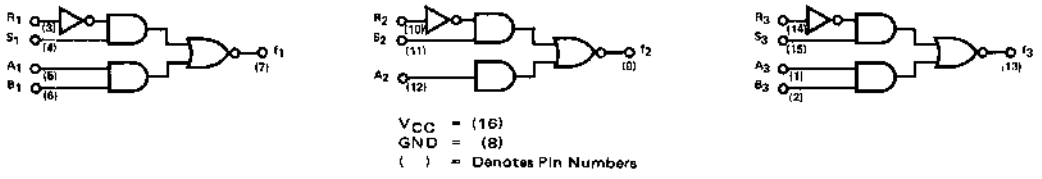
The built-in hysteresis characteristic of the 8T14 also makes it ideal for such applications as Schmitt triggers, one-shots and oscillators.

FEATURES

- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $t_{on} = t_{off} = 20ns$ (Typical)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5 VOLT LOGIC SUPPLY

*Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.5 volts typically and 0.3 volts minimum over the operating temperature range.

LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
"1" Output Voltage	2.8	3.5		V	2.0V	4.5V	0V	0V	-800μA	6, 11
	2.6	3.5		V	0V	0.8V	0V	0V	-800μA	6, 11
"0" Output Voltage			0.4	V	0.8V	2.0V	0V	0V	16mA	7, 10
			0.4	V	0V	0V	2.0V	2.0V	16mA	7, 10
"0" Input Current:										
S_n	-0.1		-1.6	mA	0V	0.4V				
A_n	-0.1		-1.6	mA	0V		0.4V			
B_n	-0.1		-1.6	mA				0.4V		
"1" Input Current										
R_n			0.17	mA	3.8V					
S_n			40	μA	3.8V	4.5V				8, 9
A_n			40	μA			4.5V	0V		
B_n			40	μA			0V	4.5V		
Hysteresis	0.30	0.50		V		4.5V	0V	0V		8, 9

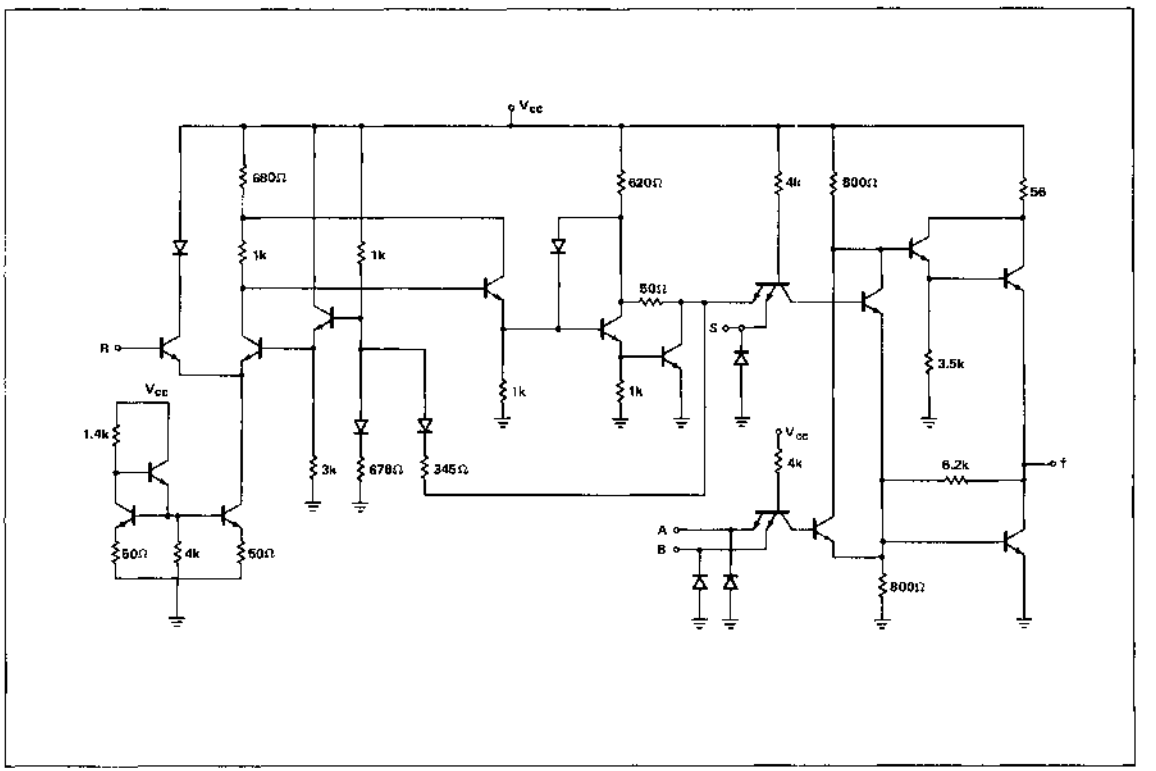
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-On Delay, t_{on}		20	30	ns						
Turn-Off Delay, t_{off}		20	30	ns						12
Power/Current Consumption		315/60	380/72	mW/mA						
Input Voltage Rating										
S	5.5			V	3.8V	10mA	0V	0V		
A	5.5			V	0V	0V	10mA	0V		
B	5.5			V	0V	0V	0V	10mA		
Output Short Circuit Current	-50		-100	mA	3.8V	0V	0V	0V	0V	12, 13
Input Clamp Voltage:										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

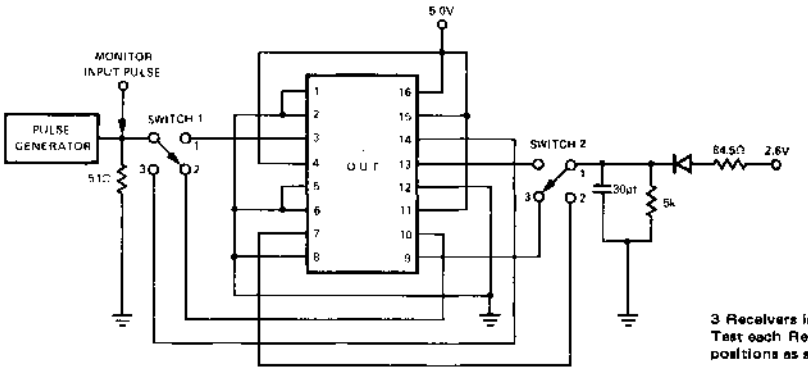
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referanced.

3. Positive current flow is defined as into the terminal referenced.
4. Positive Logic Definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Hysteresis is defined as voltage difference between R input level at which output begins to go from "0" to "1" state and level at which output begins to go from "1" to "0". Refer to Hysteresis Test Circuit.
9. $V_{CC} = 5.0V$.
10. Previous condition is a "1" output state.
11. Previous condition is a "0" output state.
12. $V_{CC} = 5.25$ volts.
13. Not more than one output should be shorted at a time.
14. Refer to AC Test Circuit and waveforms.

SCHEMATIC DIAGRAM

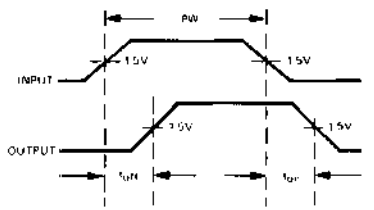


AC TEST CIRCUIT AND WAVEFORMS



3 Receivers in the package.
Test each Receiver using switch positions as shown in Table I.

TABLE I		
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3



Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

HYSTERESIS TEST CIRCUIT

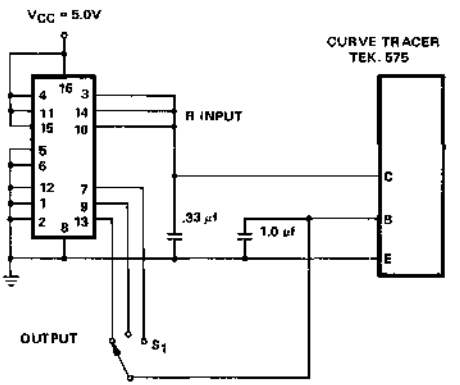


FIGURE 1

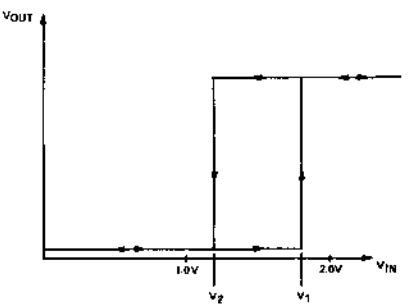
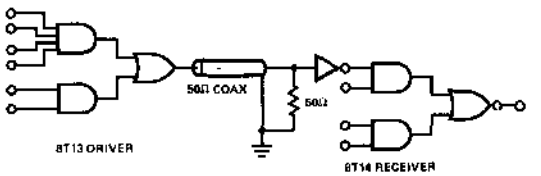


FIGURE 2

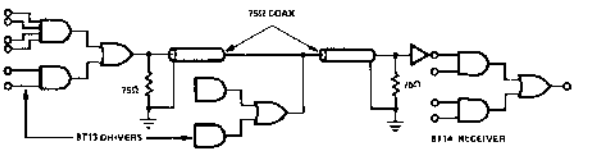
Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.
1. V_1 and V_2 must be between 0.8V minimum and 2.0V max.
2. Hysteresis = $V_1 - V_2 \geq 0.3V$.

TYPICAL APPLICATIONS

COAXIAL TRANSMISSION SYSTEM

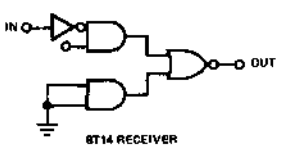


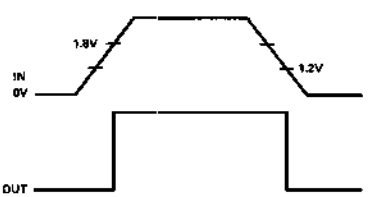
PARTY-LINE APPLICATION



If more than one driver/receiver is to be used for each transmission line, the line should be terminated at both ends as shown in Fig. 2.

SCHMITT TRIGGER APPLICATION





signetics

DUAL COMMUNICATIONS EIA/MIL LINE DRIVER

8T15

A,F PACKAGES PRODUCT AVAILABLE IN 0°C TO +75°C TEMPERATURE RANGE ONLY

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T15 Dual Communications Line Driver provides line driving capability for data transmission between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24.

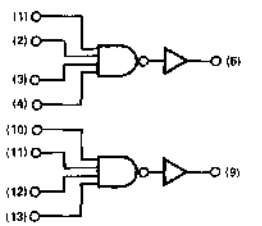
This dual 4-input NAND driver will accept standard TTL logic level inputs and will drive interface lines with nominal data levels of +6V and -6V. Output slew rate may be adjusted by attaching an external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as ±25V.

ABSOLUTE MAXIMUM RATINGS *

Input Voltage	+5.5V
Output Voltage	±25V
V_{CC}	+15V
V_{EE}	−15V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C

*Limiting values above which serviceability may be impaired.

LOGIC DIAGRAM



V_{EE} = (8)
V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS DRIVEN	INPUTS OTHER	OUTPUTS	
"1" Output Voltage	+5.0	+6.0	+7.0	V	0.8V		-4.0mA	
"0" Output Voltage	-5.0	-6.0	-7.0	V	2.0V		4.0mA	
"0" Input Current	-0.1	-0.8	-1.6	mA	0.4V			
"1" Input Current			40	μA	4.5V	0.0V		

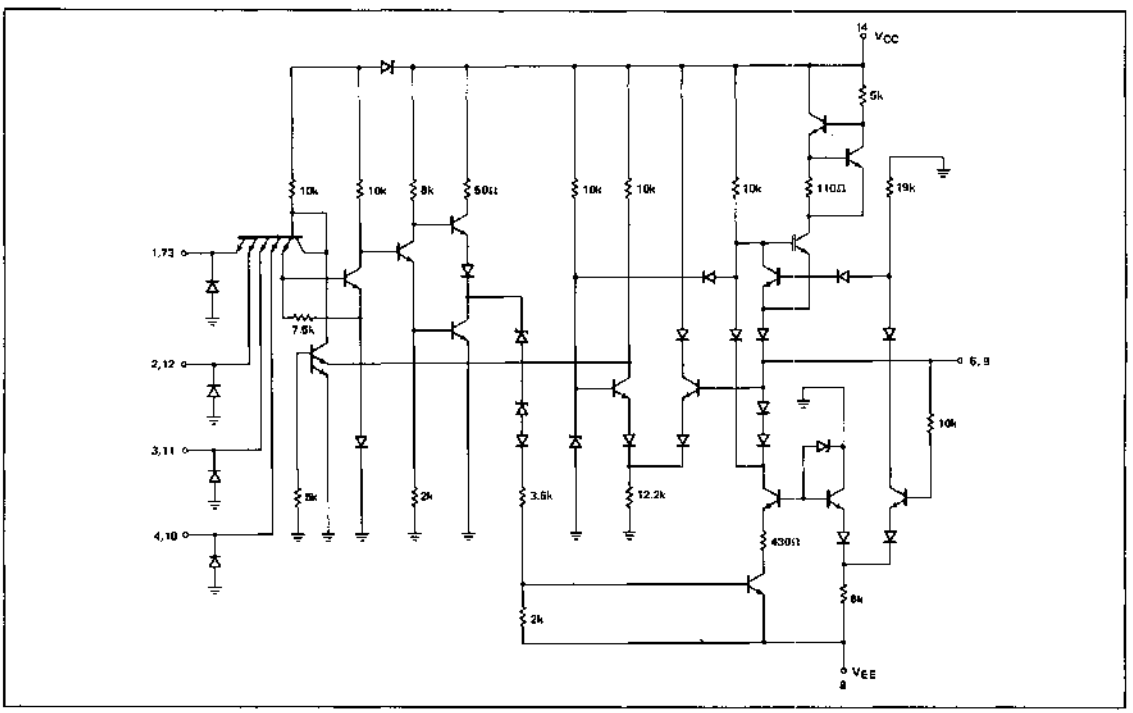
$T_A = 25^oC$, $V_{CC} = +12.0V$, $V_{EE} = -12.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS DRIVEN	INPUTS OTHER	OUTPUTS	
Output Rise Time			4	µs			Load A	7, 8
Output Fall Time			4	µs			Load B	7, 8
Output Rise Time	200			ns			Load C	7, 8
Output Fall Time	200			ns			Load D	7, 8
Power Consumption (per driver)			275	mW				10
Current from Positive Supply			16	mA				10
Current from Negative Supply			28	mA				10
Input Voltage Rating	5.5			V	10mA	0.0V		
Output Short Circuit Current			-25	mA	0.0V		-25V	9, 10
			+25	mA			+25V	9, 10
Output Impedance								
(Power on)		95		ohms	0.0V		-3.5±1mA	
(Power on)		95		ohms	2.0V		+3.5±1mA	
(Power off)	300	2.5M		ohms			±2V	
Input Clamp Voltage			-1.5	V	-12.0mA			

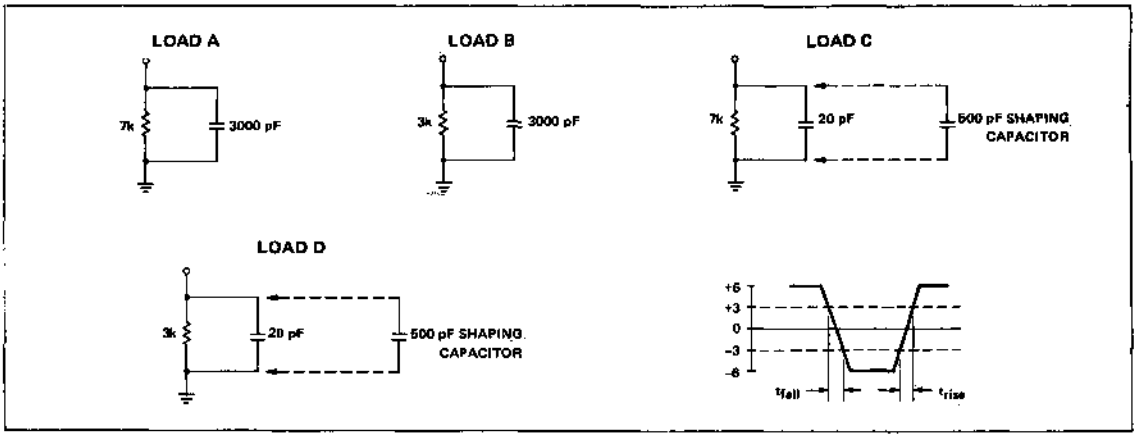
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Refer to AC Test Circuits and waveforms.
8. Rise and fall times are measured between the +3V and -3V points on the output waveform.
9. Test each driver separately.
10. $V_{CC} = +12.6V$, $V_{EE} = -12.6V$

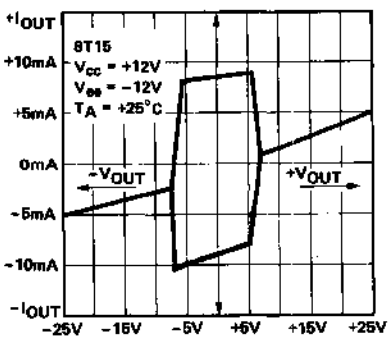
SCHEMATIC DIAGRAM



AC TEST FIGURES & WAVEFORMS



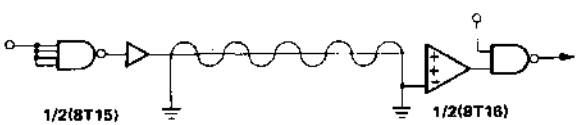
TYPICAL OUTPUT CHARACTERISTIC CURVE



TYPICAL APPLICATIONS

HIGH DIFFERENTIAL NOISE IMMUNITY (EIA + INPUT)

HIGH COMMON MODE NOISE IMMUNITY (MIL + INPUT)



signetics DUAL COMMUNICATIONS EIA/MIL LINE RECEIVER WITH HYSTERESIS | 8T16

A,F PACKAGES PRODUCT AVAILABLE IN 0° TO +75°C TEMP. RANGE ONLY.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T16 Dual Communications Line Receiver provides receiving capability for data lines between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL-STD-188B and CCITT V24 and operates from a single 5 volt power supply.

The receivers accept single (EIA) or double ended (MIL) inputs and are provided with an output strobing control. Both EIA and MIL input standards are accommodated.

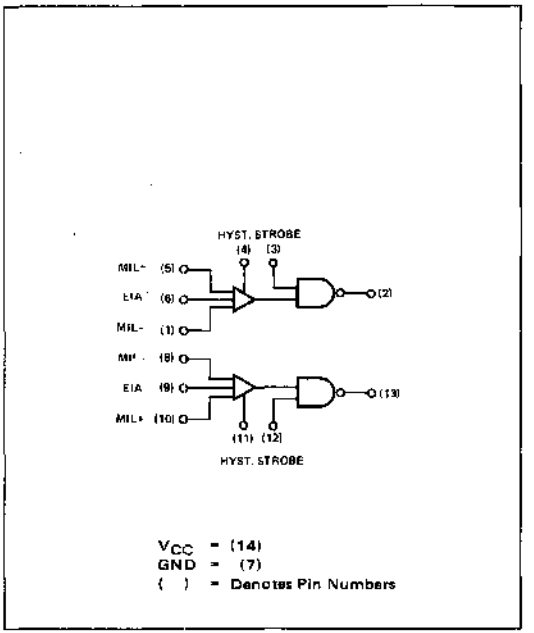
When using the EIA input terminal (with the Hysteresis terminal open), input voltage threshold levels are typically +2V and -2V with a guaranteed minimum Hysteresis of 2.4V. By grounding the "Hysteresis" terminal, the EIA input voltage threshold levels may be shifted to typically +1.0V and +2.1V with a minimum guaranteed Hysteresis of 0.75V. (Note that when using the EIA inputs, the MIL inputs—both positive and negative—must be grounded).

The MIL input voltage threshold levels are typically +0.6V and −0.6V with a minimum guaranteed Hysteresis of 0.7V. A MIL negative terminal is provided on each receiver per specification MIL-STD-188B to provide for common mode noise rejection.

Each receiver includes a strobe input so that:

a. A "1" on the strobe input allows data transfer.
b. A "0" on the strobe input holds the output high.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ABSOLUTE MAXIMUM RATINGS*

Input Voltage (EIA and MIL)	±25V
V_{CC}	+7.0V
Storage Temperature	-65°C to +175°C
Operating Temperature	0°C to +75°C

*Limiting values above which serviceability may be impaired.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					OUTPUTS	NOTES
					INPUTS						
	MIN.	TYP.	MAX.	UNITS	EIA	MIL(+)	MIL(-)	HYS	STROBE		
"1" Output Voltage (EIA) ("Hysteresis" Open)	2.6	3.5		V	-3.0V	0V	0V		2.0V	-800μA	8, 12
"1" Output Voltage (EIA) ("Hysteresis" grounded)	2.6	3.5		V	+0.3V	0V	0V	0V	2.0V	-800μA	8, 10
"1" Output Voltage (MIL)	2.6	3.5		V		-0.1mA	0V		2.0V	-800μA	8, 11
	2.6	3.5		V		-0.9V	0V		2.0V	-800μA	8, 11
"1" Output Voltage (Strobe)	2.6	3.5		V	+3.0V	0V	0V		0.8V	-800μA	8
"0" Output Voltage (EIA) ("Hysteresis" Open)			0.4	V	+3.0V	0V	0V		2.0V	9.6mA	9, 12
"0" Output Voltage (EIA) ("Hysteresis" grounded)			0.4	V	+3.0V	0V	0V	0V	2.0V	9.6mA	9, 12
"0" Output Voltage (MIL)			0.4	V		+0.1mA	0V		2.0V	9.6mA	9, 13
			0.4	V		+0.9V	0V		2.0V	9.6mA	9, 13

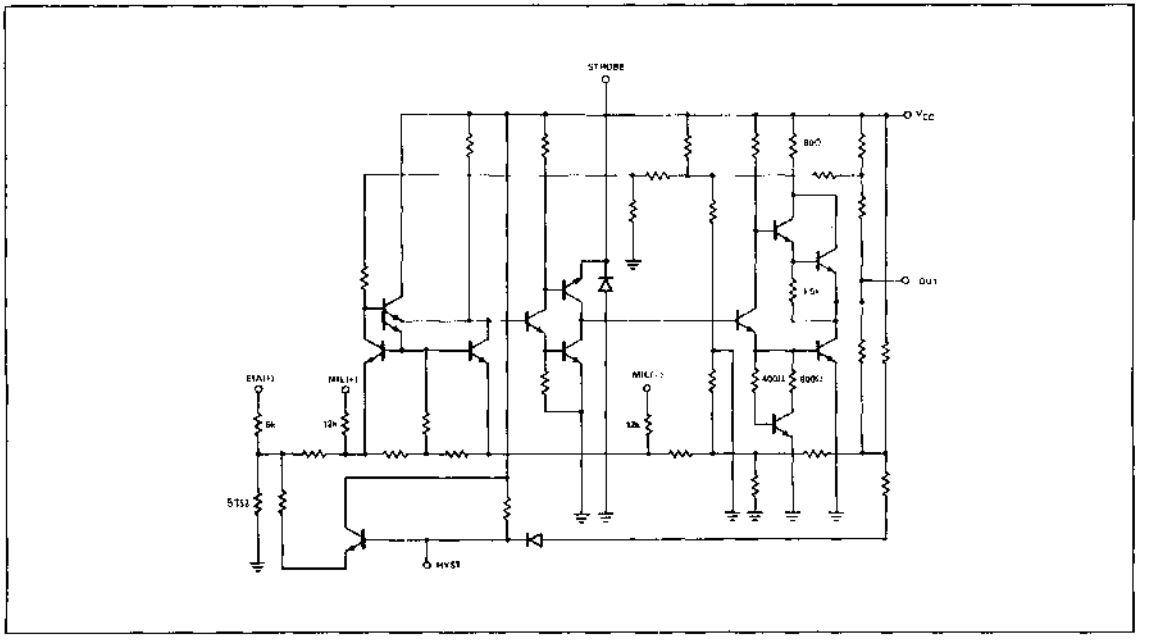
T_A = 25° C and V_{CC} = 5.0V (Cont'd)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					OUTPUTS	NOTES
					INPUTS						
	MIN.	TYP.	MAX.	UNITS	EIA	MIL(+)	MIL(-)	HYS	STROBE		
"1" Output Voltage (EIA) ("Hysteresis" open)	2.8	3.5		V	+1.2V	0V	0V		2.0V	-800μA	8, 12
"1" Output Voltage (MIL)	2.8	3.5		V		+0.35V	0V		2.0V	-800μA	8, 13
"0" Output Voltage (EIA) ("Hysteresis" open)		0.2	0.4	V	-1.2V	0V	0V		2.0V	9.6mA	9, 10
"0" Output Voltage (MIL)		0.2	0.4	V		-0.35V	0V		2.0V	9.6mA	9, 11
Input Resistance (EIA)	3	5	7	kΩ	±25V	0.0V	0.0V				
Input Resistance (MIL)	7.5	11.4		kΩ	0.0V	±25V	0.0V				
Power Consumption (per receiver)		44	75	mW	3.0V	0V	0V				17
Output Short Circuit Current	-10		-70	mA	-3.0V	0.0V	0.0V		5.00V	0.0V	16, 17
Propagation Delay		100	150	ns					5.00V		14
Signal Switching Acceptance	20			kHz					5.00V		15

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. This test guarantees operation free of latch-up over the specified input voltage range.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Previous EIA input: +3V (See hysteresis curve).
11. Previous MIL input: +0.9V (See hysteresis curve)
12. Previous EIA input: -3V (See hysteresis curve).
13. Previous MIL input: -0.9V (See hysteresis curve).
14. Reference AC Test Figure.
15. This test guarantees transfer of signals of up to 20kHz. Connect 1000pF between the output terminal and ground.
16. Each receiver to be tested separately.
17. V_{CC} = 5.25V.

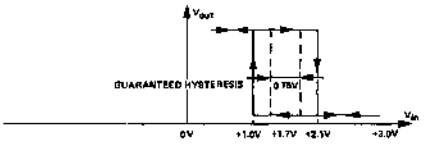
SCHEMATIC DIAGRAM



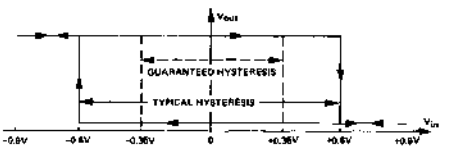
HYSTERESIS CURVES

EIA – "HYSTERESIS" OPEN

EIA – "HYSTERESIS" GROUNDED

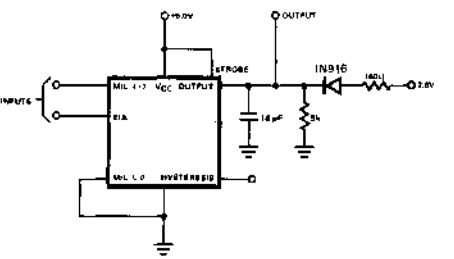


MIL – HYSTERESIS

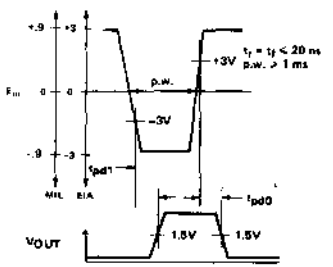


*V_{in} IS REFERENCED TO THE MIL (-) INPUT TERMINAL

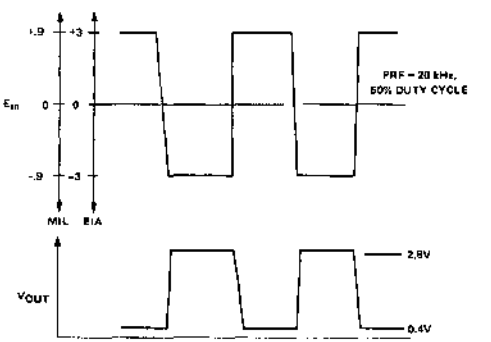
AC TEST FIGURE AND WAVEFORMS



PROPAGATION DELAY

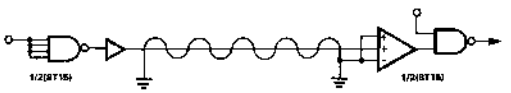


SIGNAL SWITCHING ACCEPTANCE

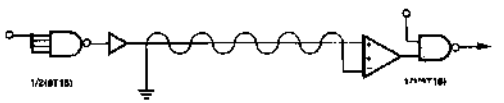


TYPICAL APPLICATIONS

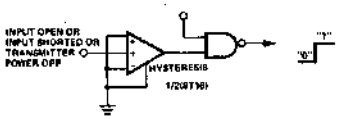
HIGH DIFFERENTIAL NOISE IMMUNITY (EIA + INPUT)



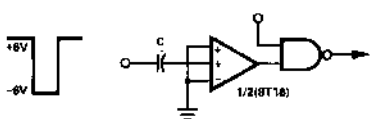
HIGH COMMON MODE NOISE IMMUNITY (MIL + INPUT)



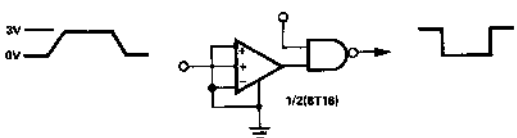
EIA FAIL-SAFE OPERATION



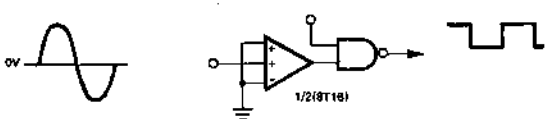
AC COUPLED OPERATIONS



SCHMITT TRIGGER



SINE TO SQUARE WAVE CONVERTER



DESCRIPTION

The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is between ±4mV with respect to the input reference level which may range from -3.2V to +4.2V. For input frequencies up to 8MHz, the device may be conditioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t_W) is defined by the relationship $t_W = C_X R_X \text{Log}_e 2$. Pulse width stability is internally compensated and virtually independent of temperature and V_{CC} variations, thus only limited by the accuracy of external timing components.

An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

ABSOLUTE MAX RATINGS

Input Voltage

V_{CC}: +7V

V_{EE}: −7V

MAX DIFF. INPUT VOLTAGE ± 5V

APPLICATIONS

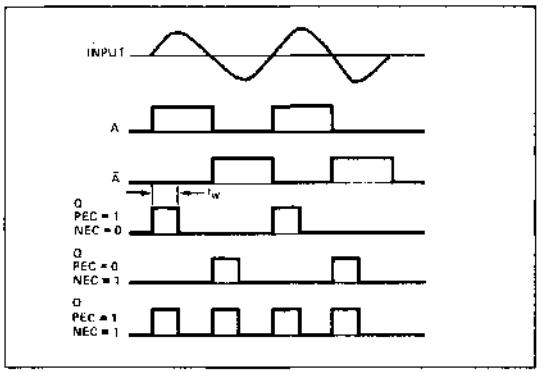
DISC, TAPE AND DRUM READERS

DIGITAL COMMUNICATIONS RECEIVERS

SIGNAL CONDITIONERS

TRANSITION DETECTORS

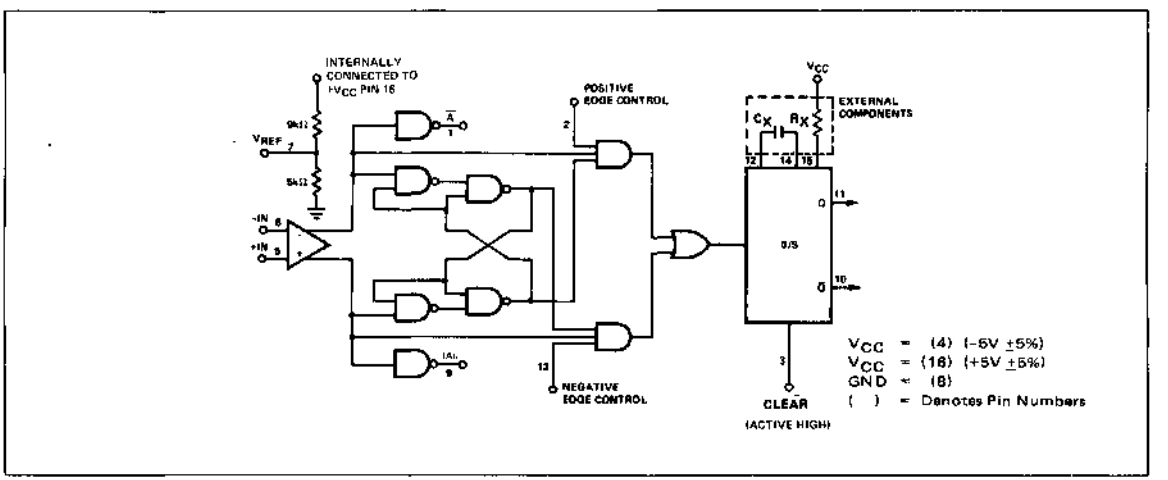
INPUT/OUTPUT WAVEFORMS



FEATURES

- DIFFERENTIAL INPUT THRESHOLD = ±4mV
- PULSE POSITION ERROR = TYPICALLY <3ns
- MAX. INPUT FREQUENCY = 8 MHz
- TRIGGERS ON POSITIVE AND/OR NEGATIVE TRANSITIONS

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Temperature Range and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"1" Output Voltage (All Outputs)	2.6			V	I_{out} = -800uA	7
"0" Output Voltage (All Outputs)			0.4	V	I_{out} = +16mA	8
DIFFERENTIAL INPUTS						
Input Threshold Voltage (V_T)			±4	mV		10
Input Bias Current			125	uA	Figure 5	
Input Offset Current		2		uA		
Common Mode Input Volt. Range	-3.2		+4.2	V		12
DIGITAL INPUTS						
"1" Input Current			40	uA	V_{in} = 4.5V	
"0" Input Current						
PEC, NEC	-0.1		-2.4	mA	V_{in} = 0.4V	
Clear	-0.1		-1.6	mA	V_{in} = 0.4V	
Input Voltage Rating (Logic Inputs)	5.5			V	I_{in} = 10mA	
Reference Voltage (V_{REF})	0.8	1.4	2.0	V	Pin 7 tied to Pin 6	
Output Pulse Width, Fig. 1	10		40	ns	Rx = 10K, Cx = Open	11
Output Pulse Width, Fig. 3	600		800	ns	Rx = 10K, Cx = 100pf	11
Power Supply Current						
I_{CC}		37	55	mA	Vcc = +5.25V	
I_{EE}		-12	-20	mA	Vcc = -5.25V	
Short Circuit Current (I_{SO})	-20		-70	mA		9

$T_A = 25°C$, V_{CC} = +5.00V, V_{EE} = -5.00V

CHARACTERISTICS		LIMITS			TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Output Frequency	16			MHz	Fig. 1, f_{in} = 8 MHz	11
Propagation Delay (ton, toff)						
Input to Q, $\overline{Q}$		30	50	ns	Fig. 2	11
Input to A, $\overline{A}$		30	50	ns	Fig. 4	11
Clear to Q, $\overline{Q}$		20	30	ns		

NOTE:

1. All Voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward based.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is applied through a resistor to ground.
8. Output sink current is supplied through a resistor to Vcc.
9. Not more than one output should be shorted at a time.
10. The differential input threshold voltage (V_T) is defined as the maximum DC voltage deviation from the reference level necessary to trigger the one-shot.
11. Refer to AC test circuits.
12. Common mode voltages that are confined within the dynamic range as specified will not cause false triggering of the one-shot.

AC TEST CIRCUITS

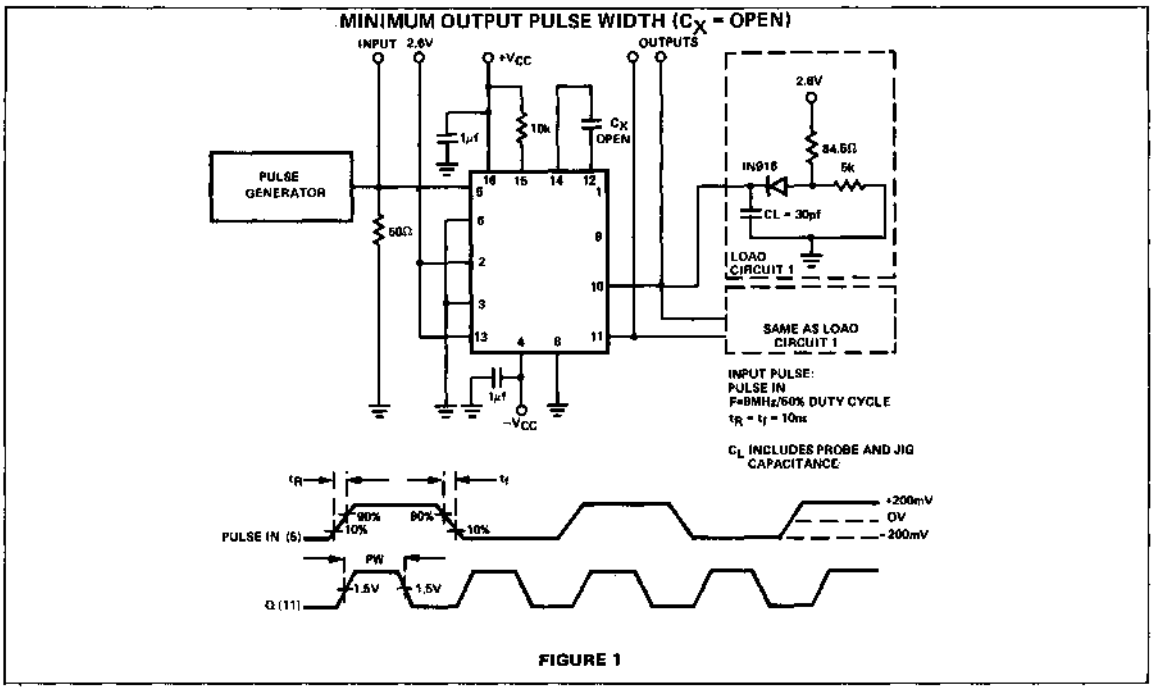


FIGURE 1

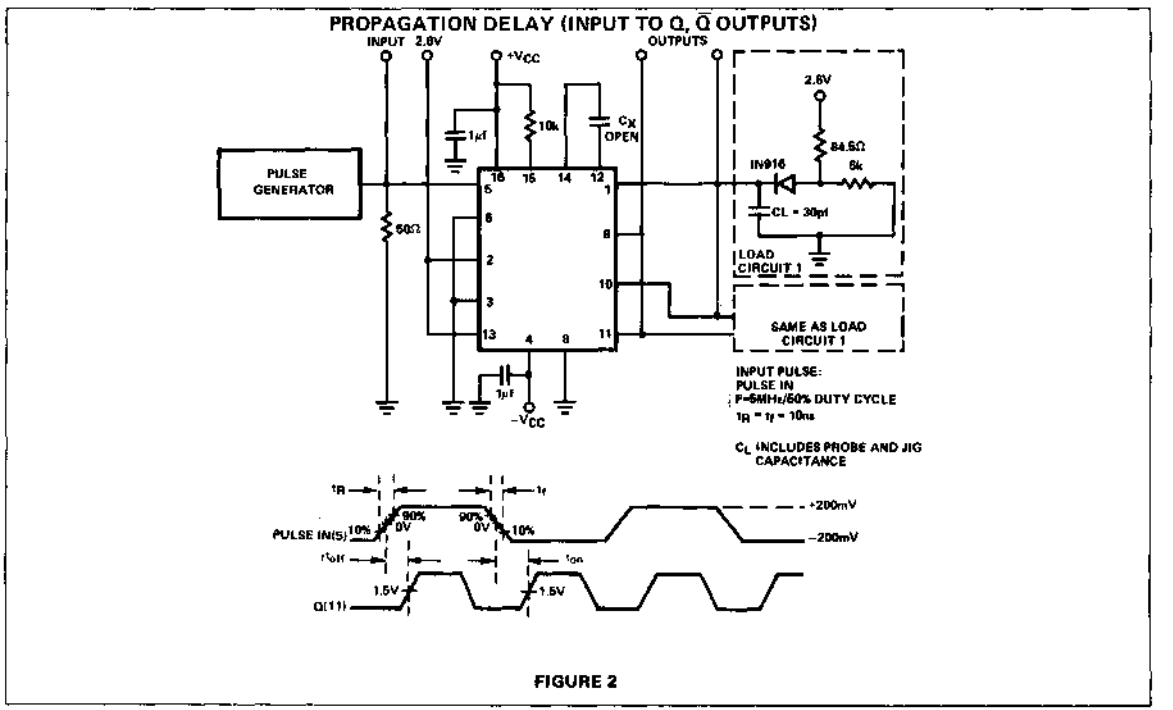


FIGURE 2

AC TEST CIRCUITS (Cont'd)

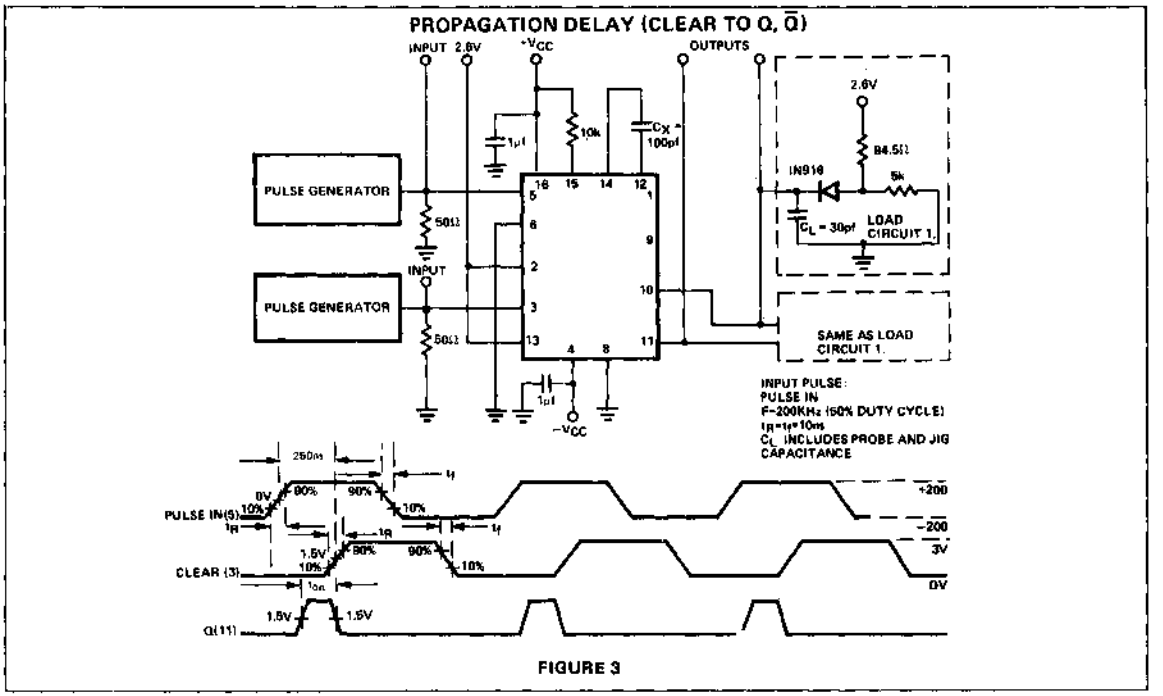


FIGURE 3

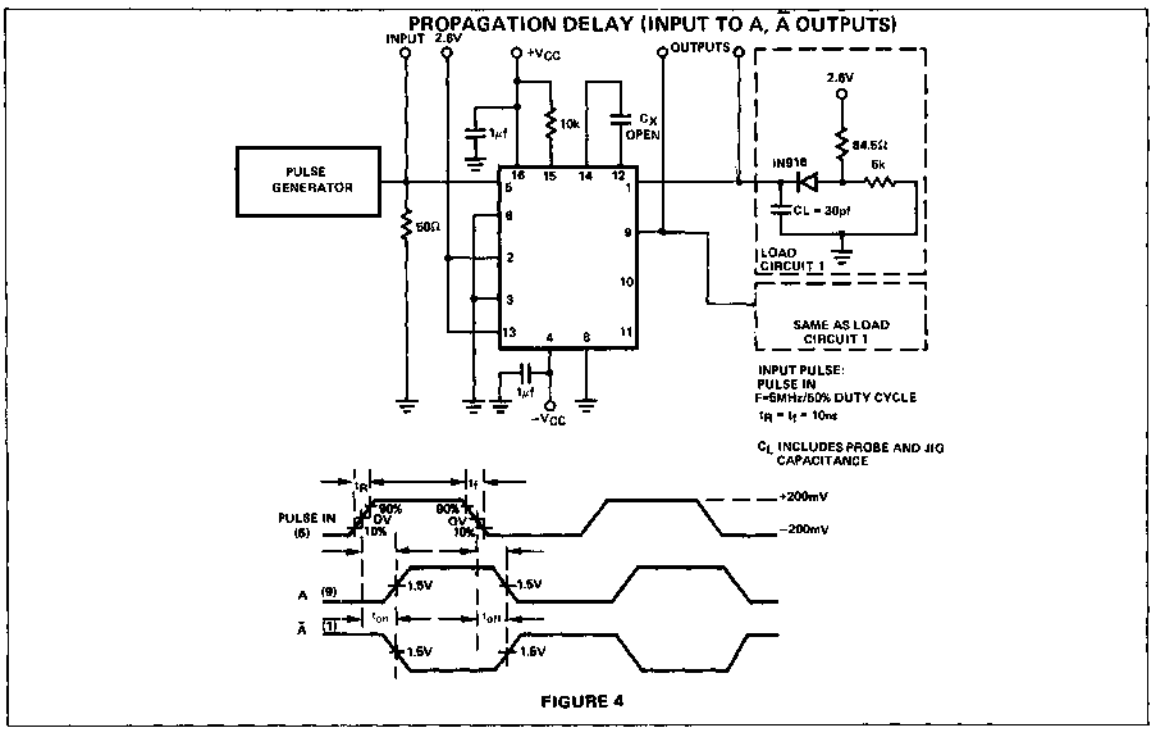


FIGURE 4

INPUT BIAS CURRENT TEST CIRCUIT

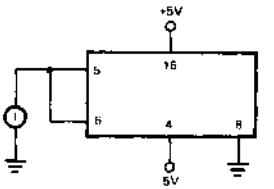


FIGURE 5

PRODUCT AVAILABLE IN 0°C TO +75°C TEMP. RANGE ONLY.

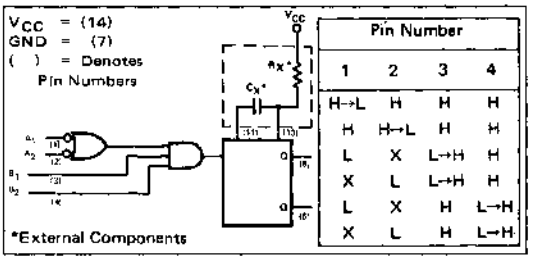
DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The Signetics N8T22A is a direct pin-for-pin replacement for the 9601 retriggerable one-shot. Triggering can be performed on either the leading or falling edge of the input signal through selection of the proper input terminal.

The inputs are level-sensitive making triggering independent of signal transition times. Output pulse width is determined by external timing components (R_X and C_X) with each trigger pulse initiating a complete new timing cycle.

LOGIC DIAGRAM



Pin Number			
1	2	3	4
H→L	H	H	H
H	H→L	H	H
L	X	L→H	H
X	L	L→H	H
L	X	H	L→H
X	L	H	L→H

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
"1" Output Voltage	2.4	3.4		V	I_{out} = -960μA
"0" Output Voltage		0.2	0.45	V	I_{out} = 12.8mA
Input HIGH Voltage	1.9			V	
Input LOW Voltage			0.9	V	
"0" Input Current			1.6	mA	V_{in} = 0.45V
"1" Input Current			60	μA	V_{in} = 4.5V
Timing Resistor	5.0		50	kΩ	
C_{Stray} - Maximum allowable wiring capacitance			50	pF	P13 to Ground

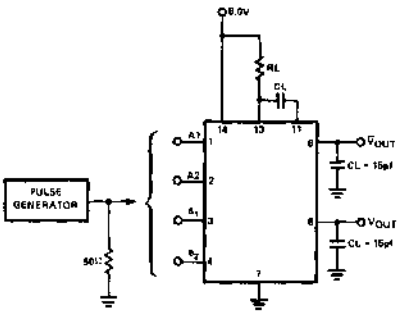
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Propagation Delay					
Negative Trigger Input		25	40	ns	R_X = 5.0kΩ, C_X = 0
to True Output (t_{pd}+)					C_L = 15pf
Negative Trigger Input		25	40	ns	R_X = 5.0kΩ, C_X = 0
to False Output (t_{pd}-)					C_L = 15pF
Min. True Output Pulse Width		45	65	ns	R_X = 5.0kΩ, C_X = 0
					C_L = 15pF
Pulse Width Variation	3.08	3.42	3.76	μs	R_X = 10kΩ, C_X = 1000pF
Short Circuit Current	-10		-40	mA	V_{out} = 0V
Power Supply Current			25	mA	V_{CC} = 5.25V

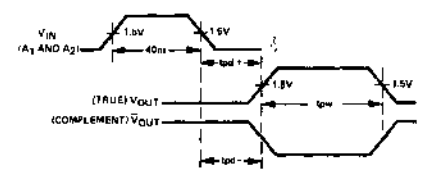
NOTES:
1. Positive current is defined as into the pin referenced.
2. Unless otherwise noted, 10kΩ resistor placed between Pin 13 and V_{CC} (R_X).

AC TEST FIGURE AND WAVEFORMS

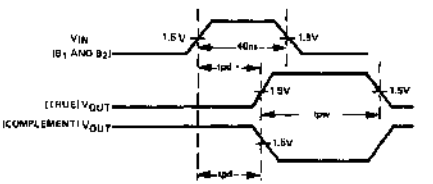
TRIGGER INPUT/OUTPUT AND PULSE WIDTH



NOTES:
1. Pulse Generator has the following characteristics: $t_r = t_f$ = 10ns (10% to 90%), AMP. = 3V.
2. C_L includes probe and jig capacitance.
3. For tpd+, tpd- and tpw (min.) RX = 5kΩ ± 1%, CX = OPEN, PRR = 1MHz.
4. For Δtpw: RX = 10kΩ ± 1%, C_X = 1000pF ± 1%, PRR = 200kHz.



WAVEFORM A.



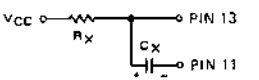
WAVEFORM B.

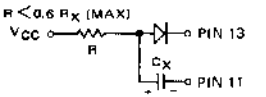
OPERATION RULES

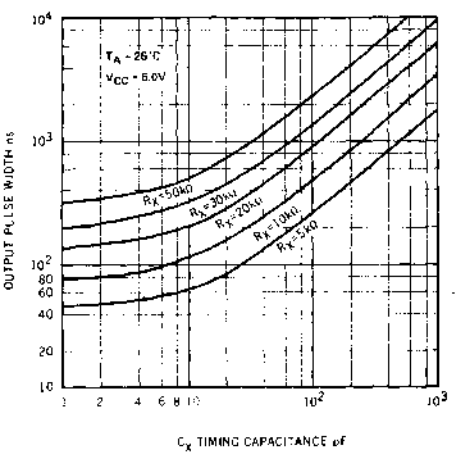
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ (0 to 75°).
3. C_X may vary from 0 to any necessary value available. If however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. If electrolytic capacitors are to be used, the following configurations are recommended:

   A. For use with low leakage electrolytic capacitors.
   The normal RC configuration can be used predicably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and Rule 3 above is satisfied.

   B. Use with high inverse leakage current electrolytic capacitors.
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.







$t \approx 0.3\ RC_X$

The output pulse with (t) is defined as follows

$$t = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right]$$

Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF.

TYPICAL OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF IS SHOWN IN THE OPPOSITE GRAPH.

DESCRIPTION

The 8T23 is a Dual Line Driver designed to meet all of the requirements of the IBM System/360, System/370 I/O interface specifications (IBM Specification GA 22-6974-0).

The low impedance emitter follower output will drive terminated lines such as coaxial cable or twisted pair. The output is protected against accidental shorting by an internal clamping network which turns on once the output voltage drops below approximately 1.5 volts. The uncommited emitter output structure allows Dot-OR logic to be performed as in "Party-Line" operations.

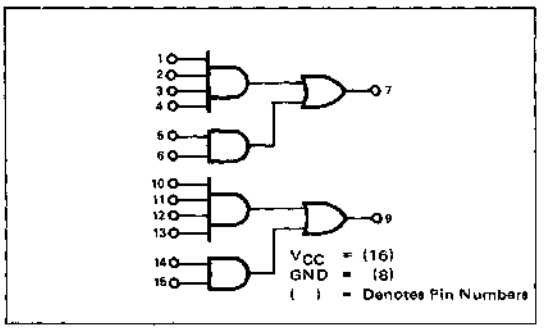
Multiple emitter inputs allow the 8T23 to interface with standard TTL or DTL systems and the circuit operates from a single +5 volt power supply.

Additional logic incorporated in the 8T23 Dual Line Driver can be used during the power-up and power-down sequence to ensure that no spurious noise is generated on the line.

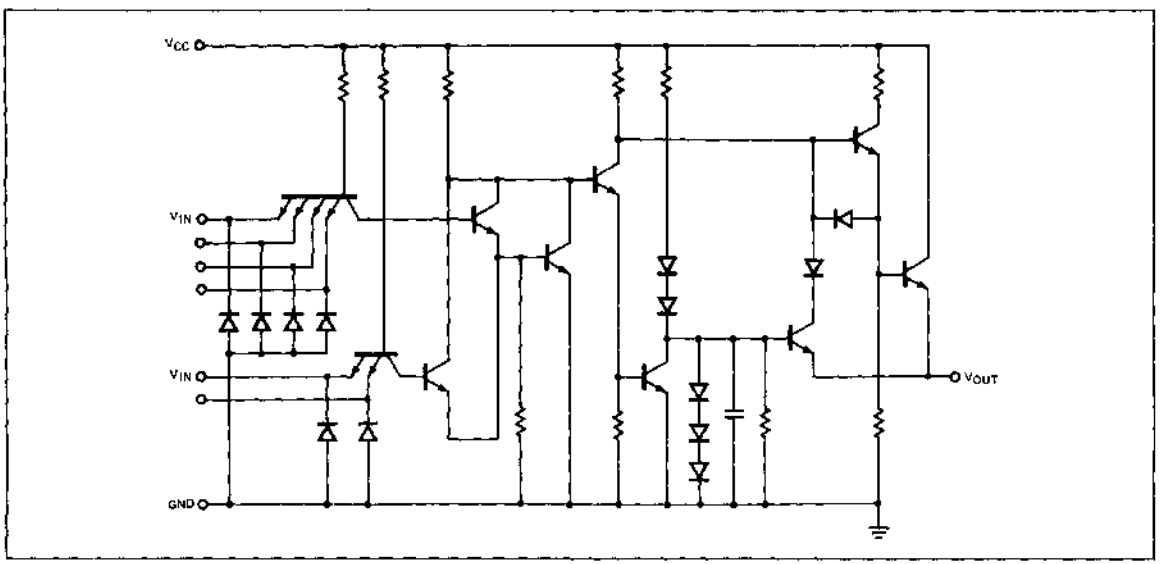
FEATURES

- I_{OUT} = 59.3mA AT 3.11 VOLTS
- UNCOMMITTED EMITTER OUTPUT STRUCTURE FOR PARTY-LINE OPERATION
- SHORT-CIRCUIT PROTECTION
- SINGLE 5 VOLT POWER SUPPLY
- AND-OR LOGIC CONFIGURATION

LOGIC DIAGRAM WITH PIN LAYOUT



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C TO +75°C)

CHARACTERISITCS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE #1		INPUTS		
	MIN	TYP	MAX	UNITS	INPUT UNDER TEST	OTHER INPUT	OF #2 AND GATE	OUTPUT	
"0" Output Voltage			+0.15	V	0.8V	4.5V	0V	-240μA	7
"1" Output Leakage Current			40	μA	0V	0V	0V	3.0V	1, 13
"0" Input Current	-0.1		-1.6	mA	0.4V	4.5V			
"1" Input Current			40	μA	4.5V	0V			

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

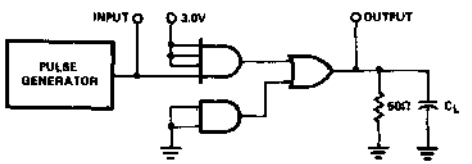
CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE #1		INPUTS		
	MIN	TYP	MAX	UNITS	INPUT UNDER TEST	OTHER INPUT	OF #2 AND GATE	OUTPUT	
"1" Output Voltage	3.11			V	2.0V	2.0V	0.8V	-59.3mA	
Turn-On Delay, t_{on}		12 15	20 25	nS nS					8, 11 9, 11
Turn-Off Delay, t_{off}		12 20	20 35	nS nS					8, 11 9, 11
Power/Current Consumption									
Output at "0"			315/ 60	mW/ mA	0.8V	0.8V	0.8V		10, 14
Output at "1"			150/ 28	mW/ mA	2.0V	2.0V	2.0V		10, 14
Input Voltage Rating	5.5			V	10mA	0V	0V		
"1" Output Current	-100		-250	mA	4.5V	4.5V	0V	2.0V	12, 14
Input Clamp Voltage			-1.5	V	-12mA				

NOTES:

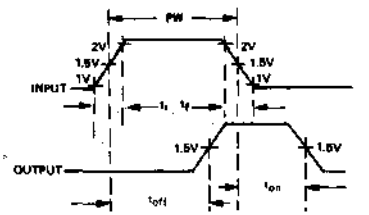
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. With forced output current of 240μA the output voltage must not exceed 0.15V.
8. RL = 50Ω to ground.
9. Load is 50Ω in parallel with 100pF.
10. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition for both drivers.
11. Reference AC Test Circuit and Pulse Requirements.
12. Reference "Typical Output Current vs. Output Voltage Curve".
13. V_{CC} = 0.00V.
14. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS

AC TEST CIRCUIT

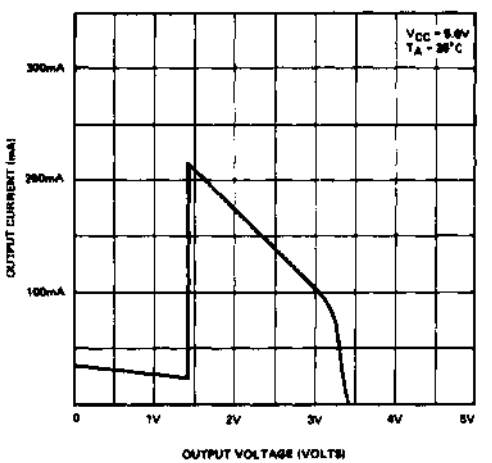


PULSE REQUIREMENTS

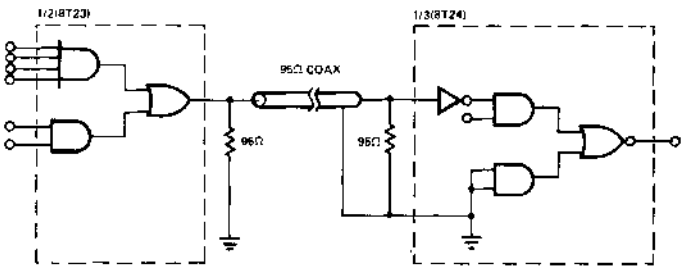


INPUT PULSE:
AMPLITUDE = 3.0V
PW = 90ns (50% DUTY CYCLE)
$t_r = t_f \leq 5ns$ (10% AND 90% MEASUREMENT POINTS)

TYPICAL OUTPUT CHARACTERISTICS



TYPICAL APPLICATIONS



signetics

TRIPLE LINE RECEIVER WITH HYSTERESIS

8T24

B,W PACKAGES 0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System/360, System/370 I/O Interface Specification (IBM Specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of -0.15V with power on or off.

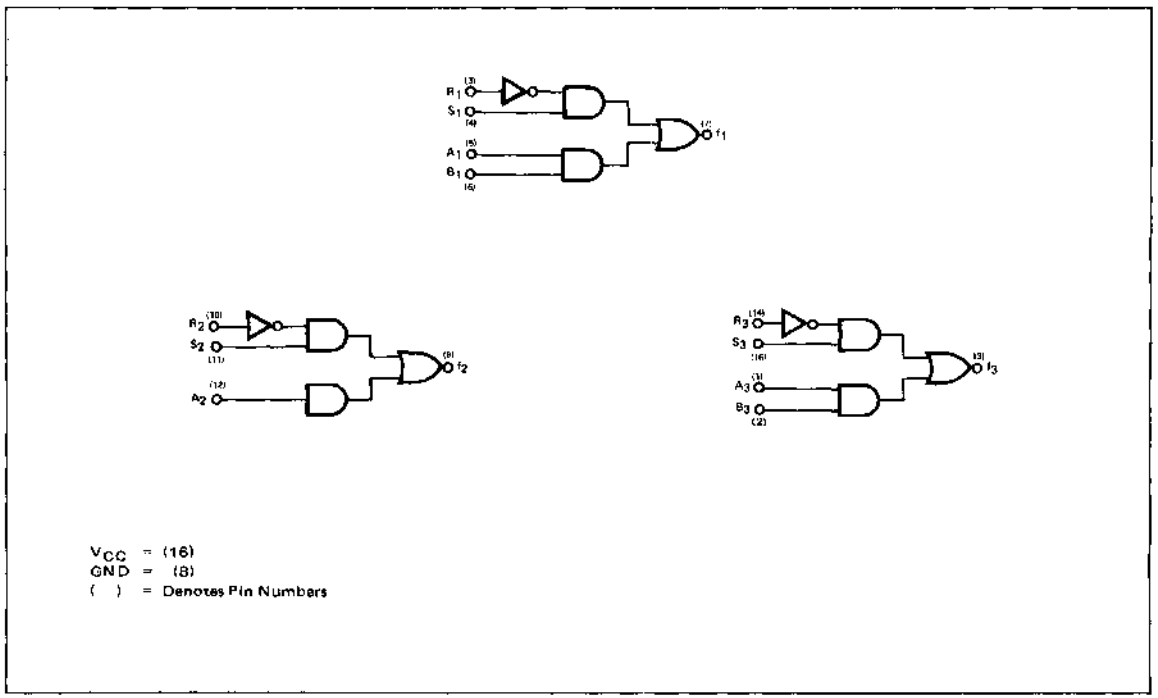
The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

FEATURES

- BUILT–IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $T_{ON} = T_{OFF} = 20ns$ (TYPICAL)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5V POWER SUPPLY

* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

LOGIC DIAGRAM WITH PIN LAYOUT



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±5%, T_A= 0°C TO +75°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
"1" Output Voltage	2.6	3.4		V	1.70V	4.5V	0V	0V	-800μA	7
	2.6	3.4		V	0V	0.7V	0V	0V	-800μA	7
"0" Output Voltage		0.2	0.4	V	0.70V	1.7V	0V	0V	16mA	8
		0.2	0.4	V	0V	0V	1.7V	1.7V	16mA	8
"0" Input Current										
S_n	-0.1		-1.6	mA	0V	0.4V				
A_n	-0.1		-1.6	mA	0V		0.4V			
B_n	-0.1		-1.6	mA				0.4V		
"1" Input Current										
R_n			0.17	mA	3.11V					
R_n			5.0	mA	7.0V					
R_n			5.0	mA	6.0V					9
S_n			40	μA	3.11V	4.5V				
A_n			40	μA			4.5V	0V		
B_n			40	μA			0V	4.5V		

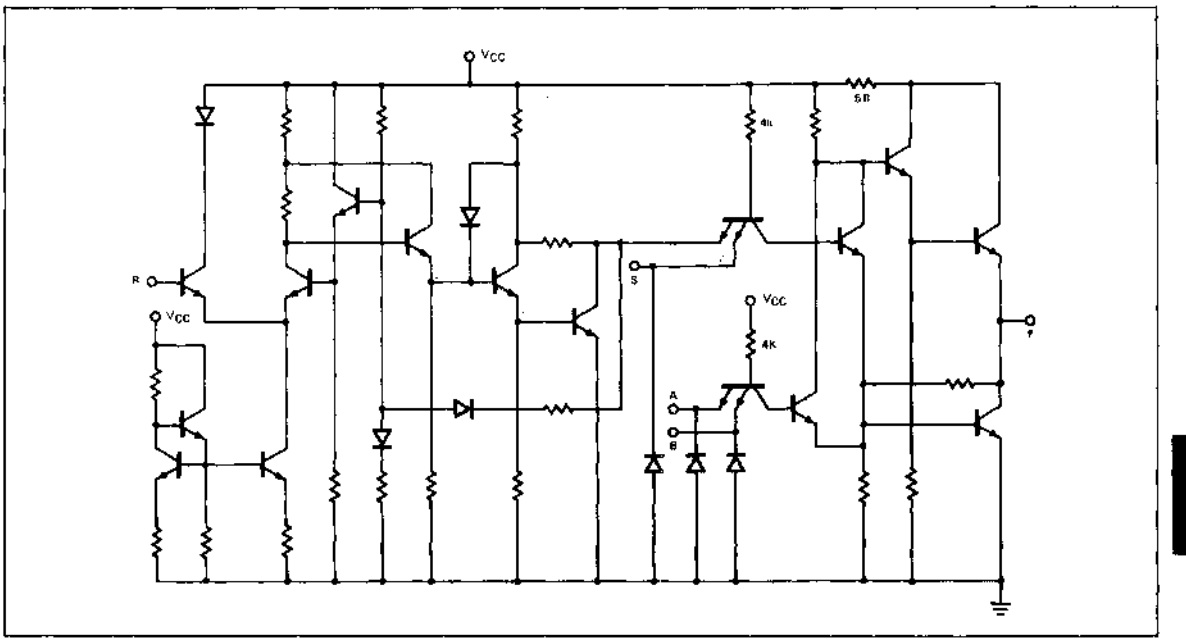
ELECTRICAL CHARACTERISTICS (AT V_{CC}= 5.0v AND T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-On Delay, t_{on}		20	30	nS						13
Turn-Off Delay, t_{off}		20	30	nS						13
Hysteresis	0.2	0.4		V		4.5V	0V	0V		11, 12
Power/Current		315	380	mW						
Consumption		60	72	mA						14
Input Voltage Rating										
S	5.5			V	3.11V	10mA	0V	0V		
A	5.5			V	0V	0V	10mA	0V		
B	5.5			V	0V	0V	0V	10mA		
Output Short Circuit Current	-50		-100	mA	3.11V	0V	0V	0V		10, 14
Input Voltage Rating										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

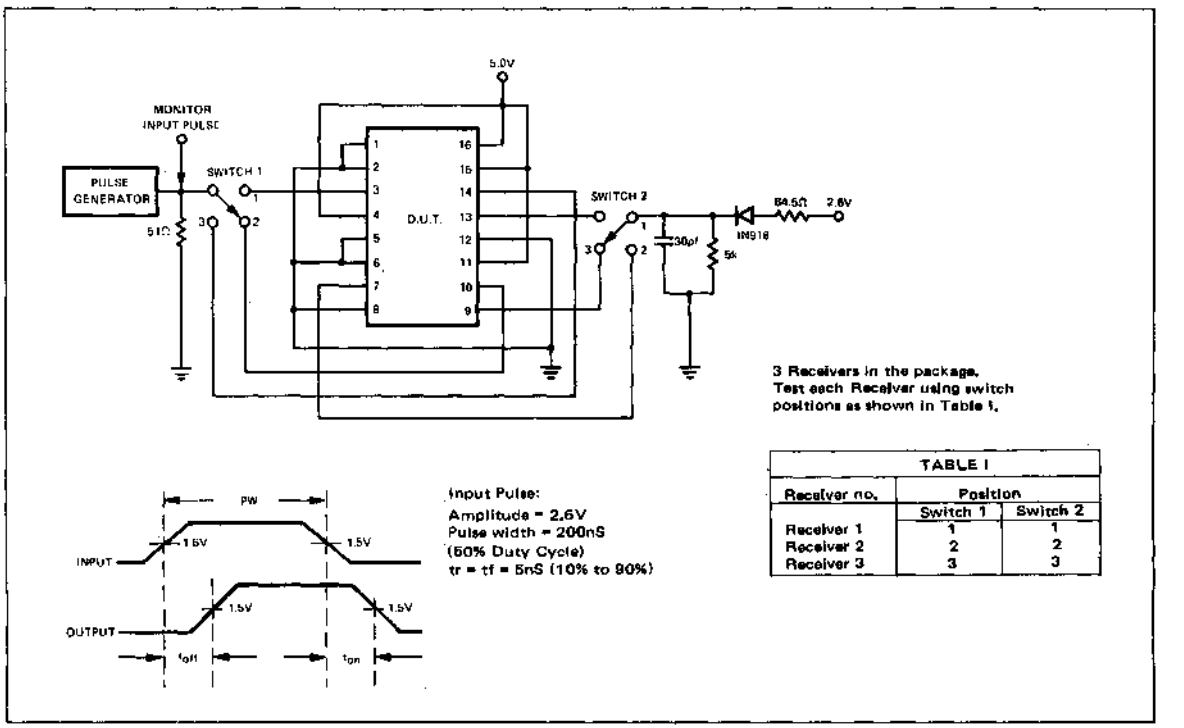
NOTES:

1. All voltage measurments are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is applied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. V_{CC} = 0.00V
10. Not more than one output should be shorted at a time.
11. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "0" to "1" state and the level at which the output begins to go from "1" to "0".
12. See Hysteresis test circuit.
13. Refer to AC test circuits.
14. V_{CC} = 5.25V.

CIRCUIT SCHEMATIC



AC TEST CIRCUIT AND WAVEFORMS



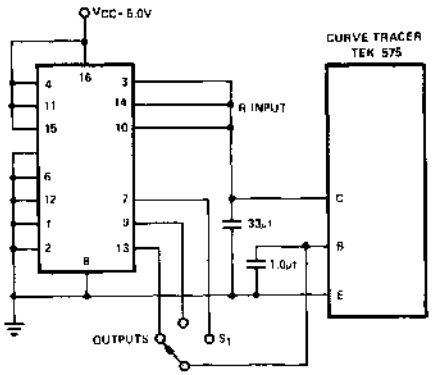
3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

TABLE I

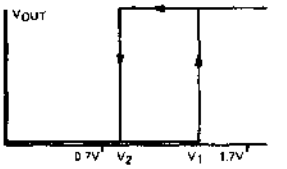
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

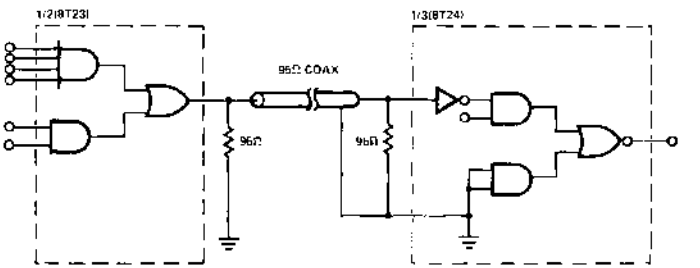


Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.7V minimum and 1.7 maximum.
2. Hysteresis = $V_1 - V_2$



TYPICAL APPLICATION



signetics

DUAL SENSE AMPLIFIER | 8T25

V PACKAGE N8T25 0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T25 is a Dual MOS-to-TTL Sense Amplifier designed to accept low level MOS signals from the output of Random Access Memories and store the information in a latch in response to an external Strobe signal. A tristate buffer presents the data to the output using conventional TTL logic levels. The 8T25 operates from a single +5 volt supply.

CIRCUIT OPERATION

A logic "1" level on the Disable line will effectively disconnect the outputs of the Sense Amplifier from a common bus by turning both totem-pole transistors off. When the Disable line returns to a logic "0" level, the outputs will be preset to a logic "1" state. A low-going Strobe pulse will then transfer the data at Inputs A and B to their respective outputs non-inverted.

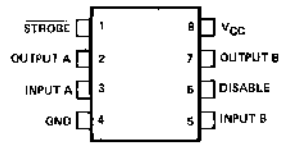
Due to the internal latch, output data will remain stable regardless of any change in input levels until a Disable signal again forces both outputs to the high impedance state.

The data inputs are current sensitive with a threshold of 300μA, although the driving source voltage must be greater than 1.6 volts in the high level.

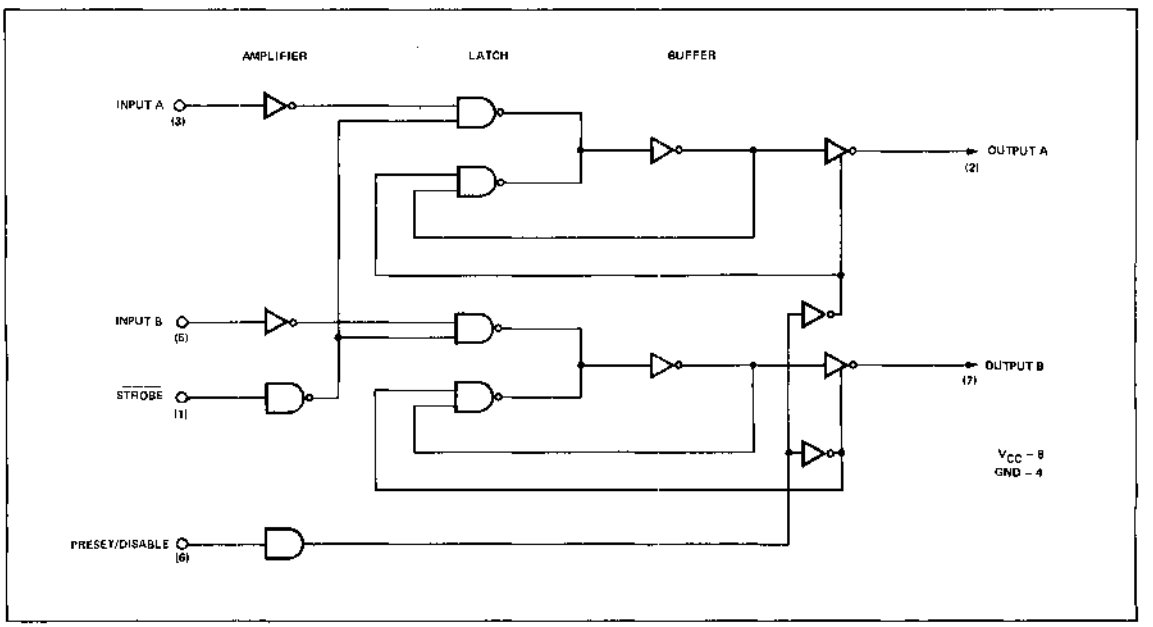
FEATURES

- MOS-TO-TTL CONVERTER
- INTERNAL LATCH
- TRISTATE OUTPUTS
- SINGLE +5V SUPPLY

PIN CONFIGURATION



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 0°C TO 75°C, V_{CC} = 5V ± 5%)

PARAMETER	LIMITS				INPUTS					
	MIN.	TYP.	MAX.	UNITS	A	B	DISABLE	STROBE	OUTPUTS	NOTES
"1" Output Voltage	2.8	3.5		V	400μA	400μA	0.8V	0.8V	-1.5mA	7
"0" Output Voltage			0.40	V	200μA	200μA	0.8V	0.8V	16mA	8
Output "1" Leakage Current										
Output "A"			100	μA	200μA	1.5mA	2.0V	0.8V	3.9V	
Output "B"			100	μA	1.5mA	200μA	2.0V	0.8V	3.9V	
Output "0" Leakage Current			100	μA	1.5mA	1.5mA	2.0V	0.8V	0V	
Input Clamp Voltage			-1.5	V			-12mA	-12mA		
Power/Current Consumption			210/40	mW/mA	400μA	400μA	4.5V	0V		11
"0" Input Current (Strobe, Disable)	-0.1		-1.6	mA			0V	0V		
"1" Input Current (Strobe, Disable)			40	μA			4.5V	4.5V		
Input Voltage Rating (Strobe, Disable)			5.5	V			1.0mA	1.0mA		
Output Short Circuit Current	-20		-70	mA				2.0V	0V	10, 11

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. V_{CC}=5.25V.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

PARAMETER	LIMITS				INPUTS					
	MIN.	TYP.	MAX.	UNITS	A	B	DISABLE	STROBE	OUTPUTS	NOTES
Propagation Delay Strobe to Output (t_{ds})		15	25	ns						Fig. 1
Disable to "0" Output (t_{PZL})		15	25	ns						Fig. 2
"0" Output to Disable (t_{PLZ})		8	15	ns						Fig. 2
Disable to "1" Output (t_{PZH})		15	25	ns						Fig. 3
"1" Output to Disable (t_{PHZ})		9	20	ns						Fig. 3

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (STROBE TO OUTPUT)

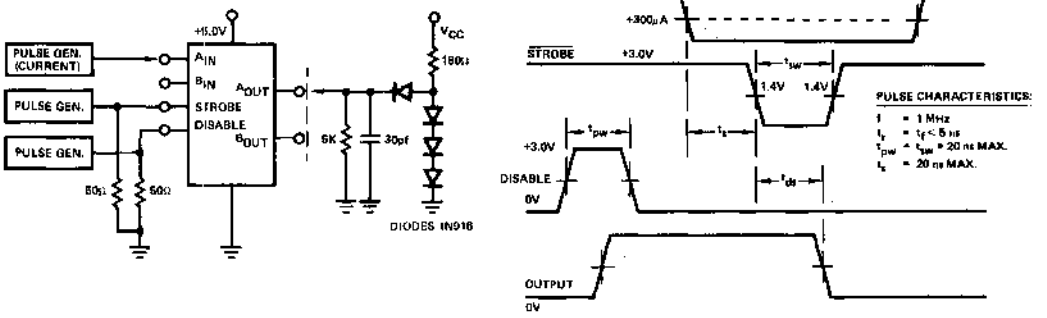
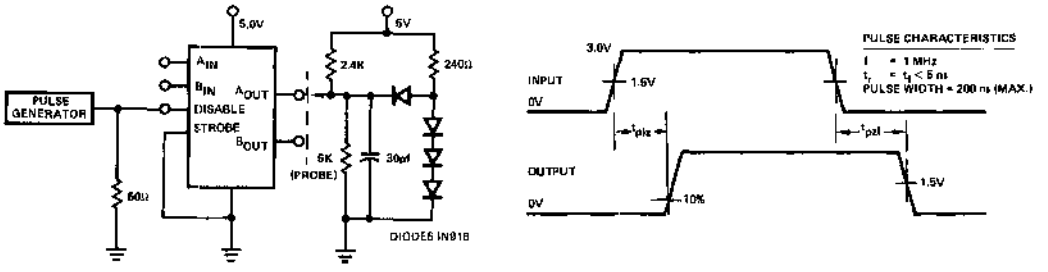


Fig. 1

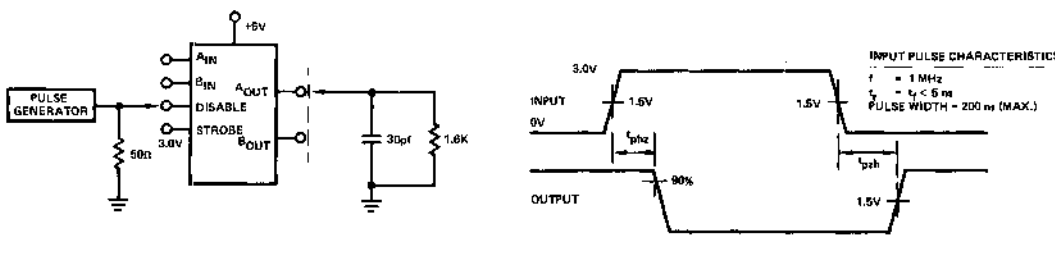
PROPAGATION DELAY (DISABLE TO OUTPUT)



NOTE: t_{plz} = "0" OUTPUT TO HIGH–Z
t_{pzl} = HIGH–Z TO "0" OUTPUT

Fig. 2

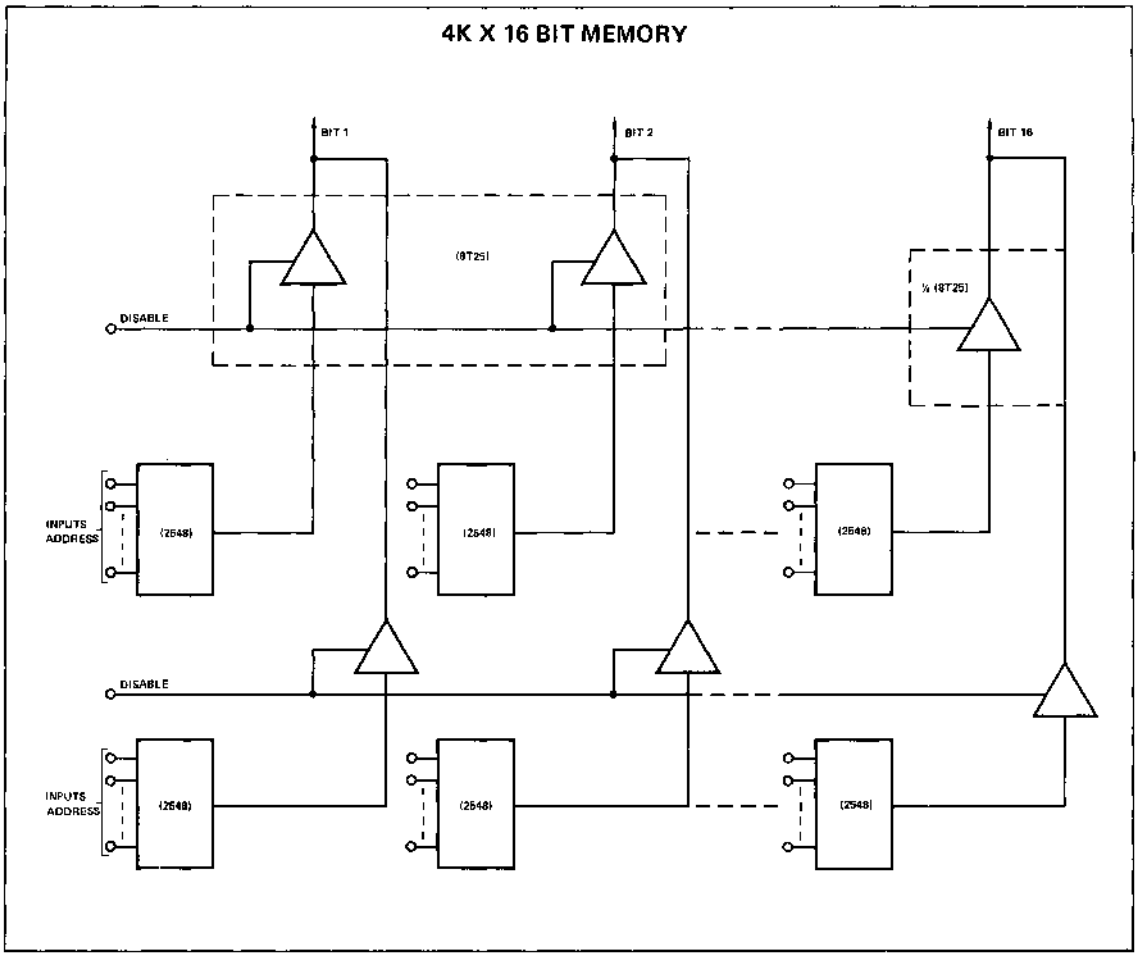
PROPAGATION DELAY (DISABLE TO OUTPUT)



NOTE: t_{phz} = "1" OUTPUT TO HIGH–Z
t_{pzl} = HIGH–Z TO "0" OUTPUT

Fig. 3

TYPICAL APPLICATION



DESCRIPTION

The 8T26 Bus Driver/Receiver contains four pair of inverting logic gates along with two buffered common enable lines.

Both the Driver and Receiver gates have tri-state outputs and PNP inputs. Tri-state outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

A logic "1" on the Data Enable (D/E) input allows input data to be transferred to the outputs of the Drivers while a logic "0" will force the outputs to a high impedance state and will also disable the PNP resulting in negligible input load current. The Driver gate will sink 40mA of current with a maximum V_{CE} of 0.5V.

The Receiver gates are enabled by a logic "0" on the Receiver Enable (R/E) pin and provide 16mA current sink capability. A logic "1" forces the Receiver outputs to a high impedance state and disables the PNP inputs.

FEATURES

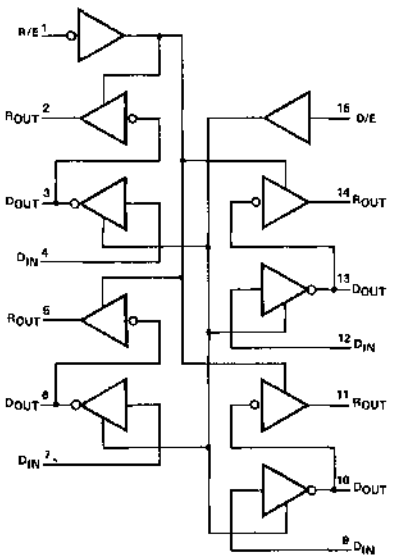
- SCHOTTKY-CLAMPED TTL
- PROPAGATION DELAY = 17ns (MAX.)
- TRI-STATE OUTPUTS
- PNP INPUTS
- 40mA CURRENT SINK CAPABILITY
- SBD* INPUT CLAMPS

*SCHOTTKY-BARRIER-DIODE

APPLICATIONS

- HALF-DUPLEX DATA TRANSMISSION
- ROUTING DATA IN BUS-ORIENTED SYSTEMS
- HIGH CURRENT DRIVERS
- MOS-TO-TTL INTERFACE

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_A = -0°C TO +75°C)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION	NOTES
Input "0" current (All inputs)			-200	μA	V_{in} = 0.4	
Input "1" current D_{in}, D_E, R_E			25	μA	V_{in} = 5.25	
Input (0) Threshold Voltage	0.85			volts		
Input (1) Threshold Voltage			2	volts		
D_{Out} (1) Voltage Pins 3,6,10,13	2.6	3.1		volts	I_{out} = -10mA	7
R_{Out} (1) Voltage Pins 2,5,11,14	2.6	3.1		volts	I_{out} = -2.0mA	7
D_{Out} (0) Voltage Pins 3,6,10,13			0.50	volts	I_{out} = 40mA	8
R_{Out}(0) Voltage Pins 2,5,11,14			0.50	volts	I_{out} = 16mA	8
Output (1) off leakage current			100	μA	V_{out} = 2.6V	
Input clamp voltage			-1.0	volts	I_{in} = -5mA	
D_{Out} short circuit current — Pins 3,6,10,13	-50		-150	mA	V_o = 0 volts	11, 12
R_{Out} short circuit current — Pins 2,5,11,14	-30		-75	mA	V_o = 0 volts	11, 12
Power/Current Consumption			457/87	mW/mA	V_{cc} = 5.25	11

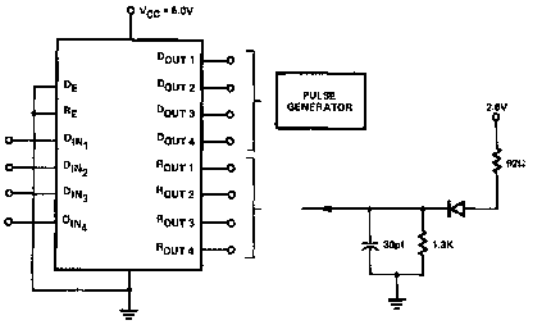
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.00V, T_A = 25°C)

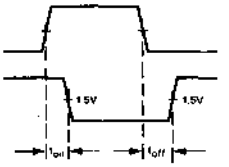
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION	NOTES
Propagation Delay						
D_{Out} to R_{Out} (t_{on})		6	10	nsec		9
D_{Out} to R_{Out} (t_{off})		13	18	nsec		9
D_{In} to D_{Out} (t_{on})		16	20	nsec		9
D_{In} to D_{Out} (t_{off})		16	20	nsec		9
Data Enable to Data Output						
High Z to 0 (t_{pZL})		29	38	nsec		9
0 to High Z (t_{pLZ})		35	43	nsec		9
Receiver Enable to Receiver Output						
High Z to 0 (t_{pZL})		20	30	nsec		9
0 to High Z (t_{pLZ})		10	17	nsec		9

NOTES:
1. All voltage measurements are referenced to the ground terminal.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Circuits.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. V_{CC} = 5.25 volts.
12. Do not ground more than one output at a time.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (D_{OUT} TO R_{OUT})

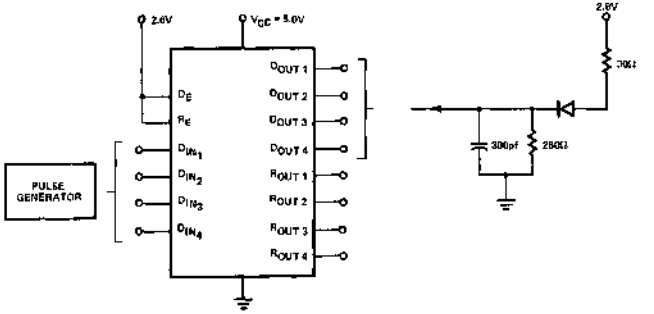


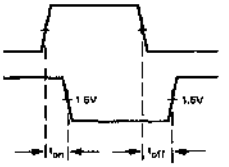


INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (D_{IN} TO D_{OUT})

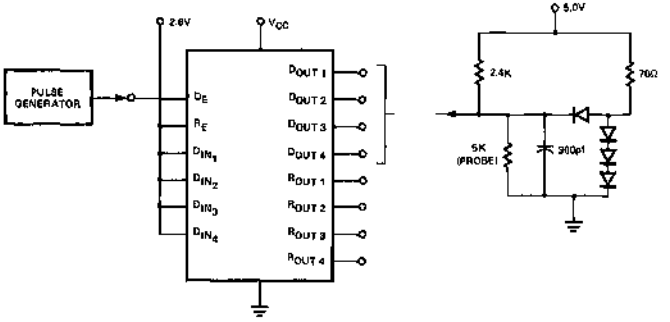


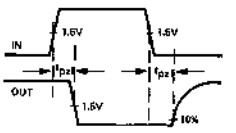


INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% Duty Cycle)
Amplitude = 2.6V

PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)

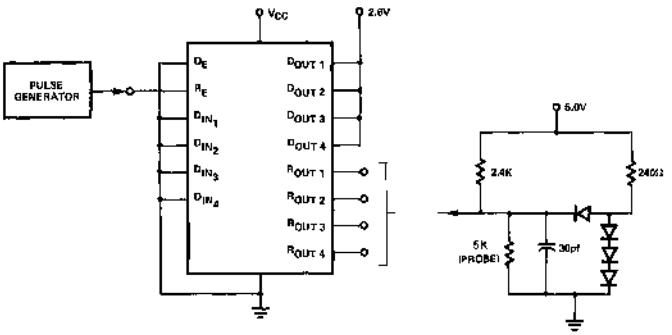


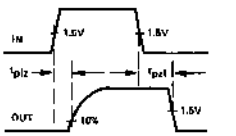


INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% Duty Cycle)
Amplitude = 2.6V

PROPAGATION DELAY (RECEIVE ENABLE TO RECEIVE OUTPUT)

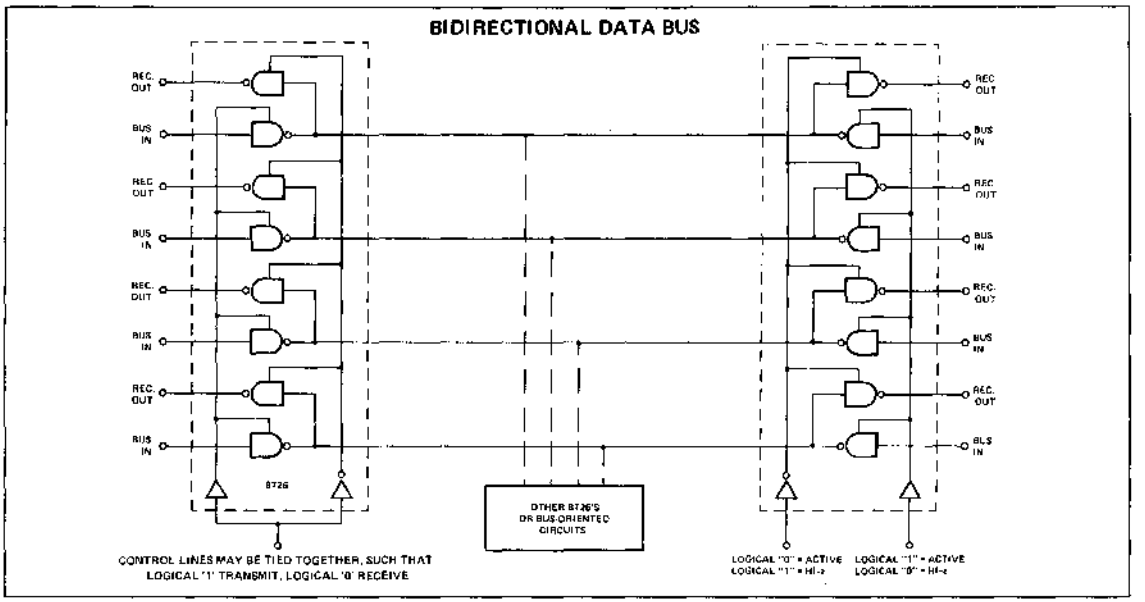




INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% Duty Cycle)
Amplitude = 2.6V

TYPICAL APPLICATIONS



DESCRIPTION

Series 82S Schottky TTL circuits are implemented with Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

The Schottky-clamped transistors are formed by using Schottky-barrier-diodes in parallel with the base-collector junctions. This is realized physically be depositing metal over the base and N region of the collector forming a metal-silicon diode. The effect of this diode, which has a lower forward voltage than the collector-base function is to hold the transistor out of saturation by diverting most of the excess base current. The reduction in stored-charge plus the use of smaller geometries results in a major improvement of switching characteristics.

By eliminating gold-doping normally employed in conventional TTL processing to reduce storage time, PNP transistors can be used to advantage by the circuit designers.

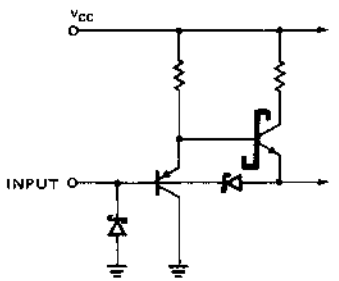
In 82S MSI, PNP transistors are used to reduce input loading as illustrated in Fig. 1. Maximum low level input current is specified at 400 μA which allows the systems designer to upgrade existing designs without encountering fanout limitations.

FEATURES

- 3ns TYPICAL GATE PROPAGATION DELAY
- 20mW PER-GATE TYPICAL POWER DISSIPATION
- LOW LEVEL INPUT CURRENT (PER UNIT LOAD = 0.4mA MAX.

EASE OF SYSTEM DESIGN

- FULLY COMPATIBLE WITH SERIES 8000, 54/74 TTL, AND MOST DTL
- SCHOTTKY-DIODE-CLAMPED INPUTS SIMPLIFY SYSTEM DESIGN
- TERMINATED, CONTROLLED-IMPEDANCE LINES NOT NORMALLY REQUIRED
- LOW OUTPUT IMPEDANCE: PROVIDES LOW AC NOISE SUSCEPTABILITY AND DRIVES HIGHLY CAPACITIVE LOADS



LOW CURRENT PNP INPUT STRUCTURE

Figure 1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted)

SUPPLY VOLTAGE V_{CC}	+7V
INPUT VOLTAGE	+6V
OUTPUT VOLTAGE	+7V
OPERATING FREE-AIR TEMPERATURE RANGE	0°C to 75°C

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 82S30 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, the f output is unconditionally low and the $\bar{f}$ output is unconditionally high.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- DIRECT OUTPUT INHIBIT
- 82S80 REPLACES 9312 FOR HIGHER SPEED

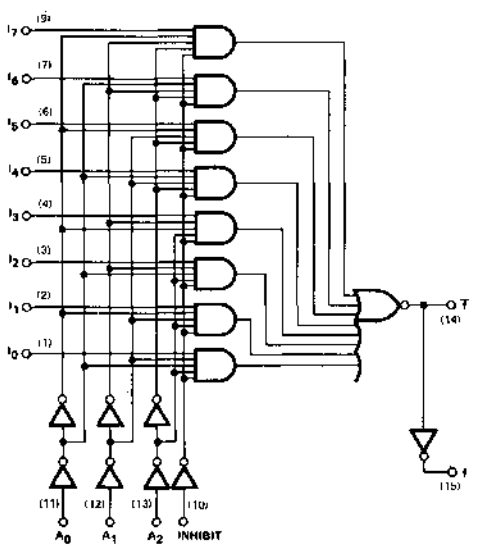
TRUTH TABLE

ADDRESS			DATA INPUT									OUTPUT	
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	f	$\bar{f}$
0	0	0	x	x	x	x	x	x	x	1	0	1	0
0	0	1	x	x	x	x	x	x	1	x	0	1	0
0	1	0	x	x	x	x	x	1	x	x	0	1	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0
1	0	0	x	x	x	1	x	x	x	x	0	1	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1
0	0	1	x	x	x	x	x	x	0	x	0	0	1
0	1	0	x	x	x	x	x	0	x	x	0	0	1
0	1	1	x	x	x	x	0	x	x	x	0	0	1
1	0	0	x	x	x	0	x	x	x	x	0	0	1
1	0	1	x	x	0	x	x	x	x	x	0	0	1
1	1	0	x	0	x	x	x	x	x	x	0	0	1
1	1	1	0	x	x	x	x	x	x	x	0	0	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1

x = don't care

LOGIC DIAGRAM

82S30



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	A_1	A_2	A_3	INH	DATA INPUT I_n	OUTPUTS	
"1" Output Voltage	2.7			V	*	*	*	*	*	−1.0mA	6
"0" Output Voltage			0.5	V	*	*	*	*	*	20mA	7
"1" Input Current											
Inputs An, In, Inh			10	µA	4.5V	4.5V	4.5V	4.5V	4.5V		
"0" Input Current											
A_n, I_n, INH			−400	µA	0.5V	0.5V	0.5V	0.5V	0.5V		

T_A = 25°C and V_{CC} = 5.0V

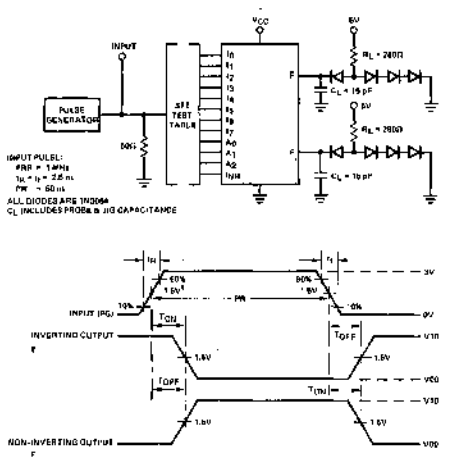
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	A	A	A	INH	DATA INPUT I_n	OUTPUTS f $\overline{f}$	
Propagation Delay											
A_n to f			20	ns							8
A_n to $\overline{f}$			17	ns							8
I_n to $\overline{f}$			12	ns							8
INH to $\overline{f}$			16	ns							8
Power Consumption/Supply Current			325/62	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		9, 11
Output Short Circuit Current											
Output f	−40		−100	mA	0V	0V	0V	0V	4.5V	0V	
Output $\overline{f}$	−40		−100	mA	0V	0V	0V	0V	0V	0V	
Input Clamp Voltage	−1.2			V	−18 mA	−18 mA	−18 mA	−18 mA			

*See Truth Table for Logical Conditions

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. V_{CC} = 5.25V
10. By DC tests per the truth table, all inputs have guaranteed thresholds at 0.8V for logical "0" and 2.0V for logical "1".
11. All I_n data inputs are at 0V, V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



TEST TABLE

TEST NO.	INPUTS A_0	A_1	A_2	INH	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	OUTPUTS $\overline{F}$	F
1	PG	0	0	0	D	1	0	0	0	0	0	0	T	T
2	0	PG	0	0	0	D	1	0	0	0	0	0	T	
3	0	0	PG	0	0	0	0	D	1	0	0	0	T	
4	0	1	1	PG	0	0	0	0	0	1	0	0	T	
5	1	1	1	0	0	0	0	0	0	0	PG	T		

"1" = 2.7V "0" = GROUND

NOTE:
1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTHS FROM PACKAGE PINS.

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 82S31 is a variation of the 82S30 that provides open collector output $\overline{f}$ for expansion of input terms. The 82S32 is similar to the 82S30 except in the effect of the INHIBIT input on the $\overline{f}$ output. With the INHIBIT low, the selected input appears at the f output and, in complement, on the $\overline{f}$ output. With the INHIBIT input high, both the f and the $\overline{f}$ output are unconditionally low.

ELECTRICAL CHARACTERISTICS

Propagation Delay (Typ)

	82S32	82S31
A_n to $\overline{f}$	12ns	14ns
I_n to $\overline{f}$	7ns	9ns

Input Load Current (Max)

I_{In}"0"	400μA
I_{In}"1"	10μA

Output Current

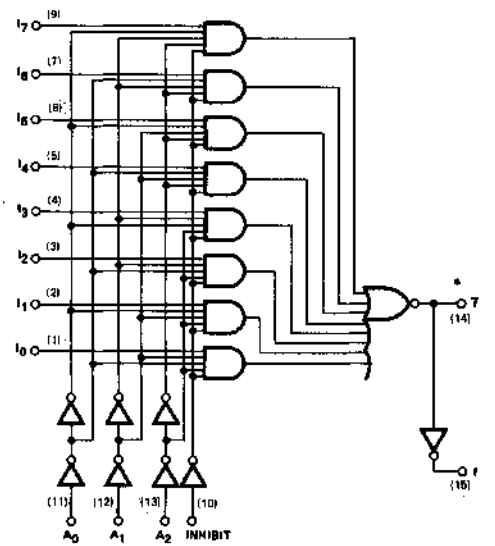
I_{out}"0"	20mA @ 0.5V
I_{out}"1"	1mA @ 2.7V for 82S31 f output only

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUT (82S31)
- DIRECT OUTPUT INHIBIT (82S32)

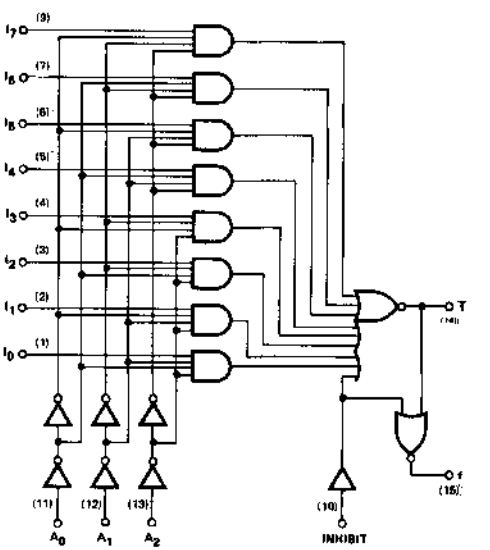
LOGIC DIAGRAMS

82S31



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers
* ($\overline{f}$ Output Has Open Collector)

82S32



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

Signetics

2-INPUT 4-BIT DIGITAL MULTIPLEXER

82S33
82S34

B,F PACKAGES

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 82S33 features non-inverting data paths; and, the 82S34 features inverting data paths.

The 82S34 has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as forty four-bit words can be multiplexed by using twenty 82S34's in the WIRED-AND mode.

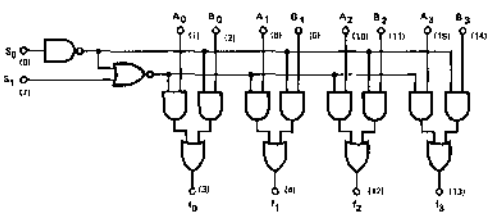
The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S34)
- INHIBIT STATE

LOGIC DIAGRAM

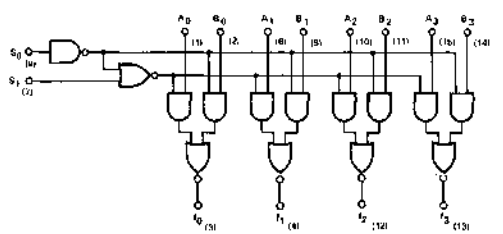
82S33



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

82S34 (OPEN COLLECTOR)



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

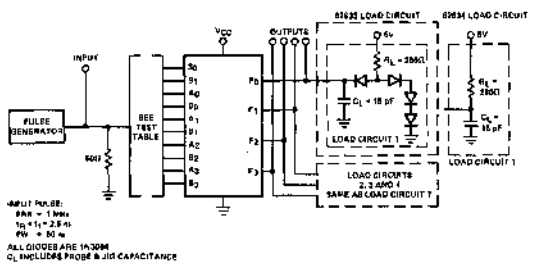
CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUTS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (82S33)	2.7			V	2.0V	2.0V	0.8V	0.8V	−1mA	6
"0" Output Voltage (82S33)			0.5	V	0.8V	2.0V	2.0V	0.8V	20mA	7
"0" Output Voltage (82S34)			0.5	V	0V	2.0V	0.8V	0.8V	20mA	7
"1" Output Leakage Current (82S34)			250	μA	2.0V	2.0V	2.0V	2.0V	5.5V	9
"0" Input Current (ALL)			400	μA	0.5V	0.5V	0.5V	0.5V		
"1" Input Current (ALL)			−10	μA	4.5V	4.5V	4.5V	4.5V		
Output Short Circuit Current (82S33)	−40		−100	mA	5V	5V	0V	0V	0V	10, 11
Input Clamp Voltage (ALL)			−1.2V	V	−18mA	−18mA	−18mA	−18mA		

T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUTS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
Power/Current Consumption:										
82S33			305/58	mW/mA		0V		0V		10
82S34			265/50	mW/mA		0V		0V		10
82S33/34 Turn-On/Turn-Off Times										
A_n, B_n to f_n			12	ns						8,1
S_0 to f_n			20	ns						8,1
S_1 to f_n			18	ns						8,1

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures and Test Table.
9. Connect an external 1K ± 1% resistor to V_{CC} for this test.
10. V_{CC} = 5.25V.
11. Not more than one output should be shorted at a time.

AC TEST FIGURES AND WAVEFORMS



TEST TABLE

TEST NO.	INPUTS S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	OUTPUTS F_0	F_1	F_2	F_3
1	PG	0	1	0	1	0	1	0	1	0	T			
2	PG	0	1	0	1	0	1	0	1	0	T	T	T	T
3	PG	0	0	1	0	1	0	1	0	1		T		
4	1	PG	1	0	1	0	1	0	1	0			T	
5	0	0	0	PG	0	0	0	0	0	0	T			
6	0	1	0	0	0	PG	0	0	0	0		T		
7	1	0	0	0	0	0	PG	0	0	0			T	
8	1	0	0	0	0	0	0	PG	0					T

"1" = 2.7V "0" = GROUND

NOTE:
1. A.C. TEST JIG'S MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIG'S MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

DESCRIPTION

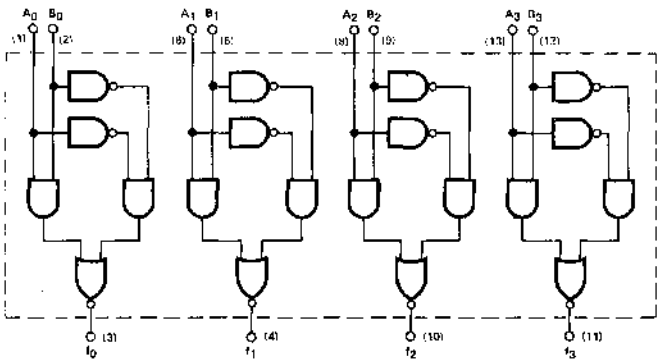
The 82S41 contains four independent gating structures to perform the Exclusive-OR function on two input variables. The output of the 82S41 employs the totem-pole structure characteristic of TTL devices.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS

LOGIC DIAGRAMS

82S41 QUAD EXCLUSIVE–OR



A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14-pin dual in-line package

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
					INPUTS		OUTPUTS	
	MIN.	TYP	MAX	UNITS	A	B		
Output "1" Voltage	2.7			V	2.0V	0.8V	−1mA	7
Output "0" Voltage			0.5	V	2.0V	2.0V	20mA	8
Input "1" Current			10	μA	4.5V	4.5V		11
Input "0" Current			−800	μA	0.5V	0.5V		12
Power/Current Consumption			290/55	mW/mA				13
Output Short Circuit Current	−40		−100	mA		18mA	0V	13,10
Input Clamp Voltage	−1.2			V	−18mA			

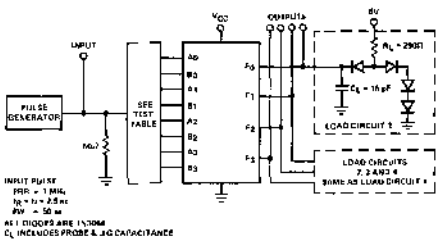
$T_A = 25^oC$ and $V_{CC} = 5.0V$

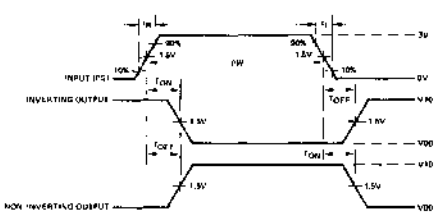
CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
					INPUTS		OUTPUTS	
	MIN	TYP	MAX	UNITS	A	B		
Turn-On/Turn-Off Times			10	ns				9

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. Not more than one output should be shorted at a time.
11. A and B are tested separately. When A is 4.5V, B is 0V, and vice versa.
12. A and B are tested separately. When A is 0.4V, B is 5.25V, and vice versa.
13. $V_{CC} = 5.25V$.

AC TEST FIGURE AND WAVEFORMS





TEST TABLE												
TEST	INPUTS								OUTPUTS			
NO.	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	0	0	0	PG	0	0	0	0		T		
2	0	PG	0	0	0	0	0	0	T			
3	0	0	0	PG	0	0	0	0		T		
4	0	0	0	0	0	PG	0	0			T	
5	0	0	0	0	0	0	PG	0				T
6	PG	0	0	0	0	0	0	0	T			
7	0	0	0	0	0	0	PG	0				T

"1" = 2.7V "0" = GROUND

NOTE.

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

82S42 | 4-BIT QUAD EXCLUSIVE-NOR

signetics

A,F PACKAGES

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S42 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 82S42 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

FEATURES

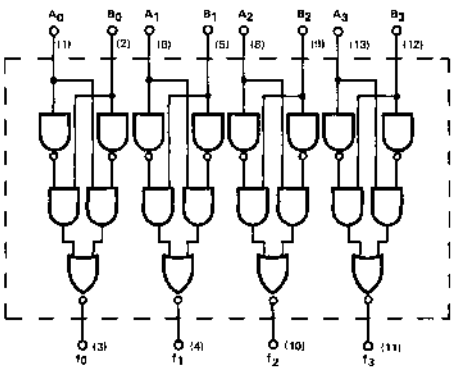
- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS

ELECTRICAL CHARACTERISTICS

Propagation Delay (Typ)	
A_n, B_n to f_n	9ns (82S42)
Input Load Current (Max)	
I_{In}"0"	800μA
I_{In}"1"	20μA
Output Current (Min)	
I_{out}"0"	30mA @ 0.5V (82S42)

LOGIC DIAGRAM

82S42 QUAD EXCLUSIVE–NOR



A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

signetics

BINARY-TO-OCTAL DECODER
BCD-TO-DECIMAL DECODER

82S50
82S52

A,F PACKAGES 82S50
B,F PACKAGES 82S52

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S50 and 82S52 are gate arrays for decoding and logic conversion applications.

The 82S50 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

The 82S52 converts a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

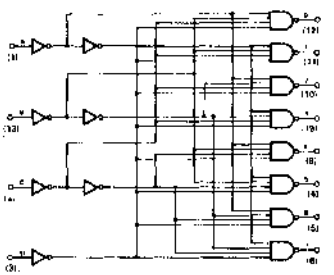
The 82S52 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs. The selected output is a logic "0".

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- INHIBIT INPUT FORCES ALL OUTPUTS HIGH (82S50)
- 82S52 REPLACES 9301 FOR HIGHER SPEED

LOGIC DIAGRAMS

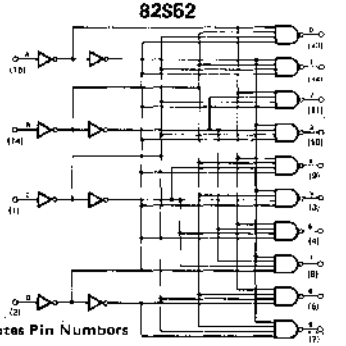
82S50



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

*NOTE: PIN-OUT FOR DUAL IN-LINE PACKAGE ONLY

82S52



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

TRUTH TABLE

INPUT STATE				OUTPUT STATES									
				82S50								82S52	
A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS						
"1" Output Voltage	2.7			V					−1mA	6, 10
"0" Output Voltage			0.5	V					20mA	7,10
"1" Input Current			10	μA	4.5V	4.5V	4.5V	4.5V		
"0" Input Current (ALL)			−400μA	mA	0.5V	0.5V	0.5V	0.5V		

$T_A = 25^oC$ and $V_{CC} = 5.0V$

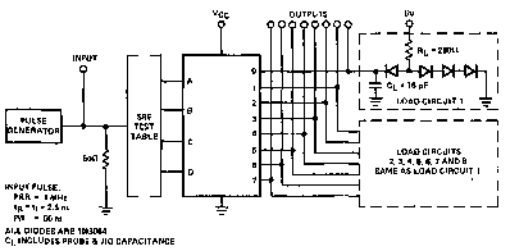
CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS						
Turn-on Delay t_{on}			16	ns						8
Turn-off Delay t_{off}			16	ns						8
Power/Current Consumption										
(82S50 Only)			380/72	mW/mA	5.25V	5.25V	5.25V	0V		11
(82S52 Only)			450/85	mW/mA						11
Input Clamp Voltage			−1.2	V	−18mA	−18mA	−18mA	−18mA		
Output Short Circuit Current (ALL)	−40		−100	mA	4.0V	4.0V	4.0V	4.0V	0V	9,11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. Inputs for "1" and "0" output voltage test is per TRUTH table with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. $V_{CC} = 5.25V$.

AC TEST FIGURE AND WAVEFORMS

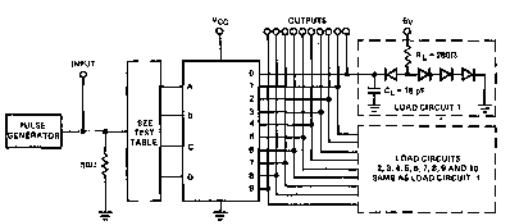
82S50



TEST TABLE													
TEST NO.	INPUTS A	B	C	D	OUTPUTS 0	1	2	3	4	5	6	7
1	1	1	PG	0								T
2	1	1	PG	0				T				T
3	PG	1	0	0			T	T				
4	0	PG	1	0					T		T	
5	0	0	0	PG	T					T		
6	1	0	PG	0		T					T	

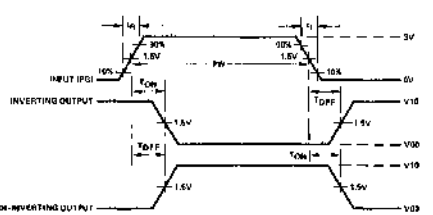
"1" = 2.7V "0" = GROUND

82S52



TEST TABLE													
TEST NO.	INPUTS A	B	C	D	OUTPUTS 0	1	2	3	4	5	6	7	8	9
1	0	0	PG	0				T						
2	PG	1	0	0			T	T						
3	0	0	0	PG	T							T		
4	1	0	PG	0		T			T					
5	1	PG	0	1										T
6	PG	1	1	0										

"1" = 2.7V "0" = GROUND



NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

signetics

9-BIT PARITY GENERATOR AND CHECKER | 82S62

A,F PACKAGES

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S62 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 82S62. (A logic 1 on the INHIBIT input forces both outputs to a logic 0.)

When used as a Parity Generator, the 82S62 supplies a parity bit which is transmitted together with the data word.

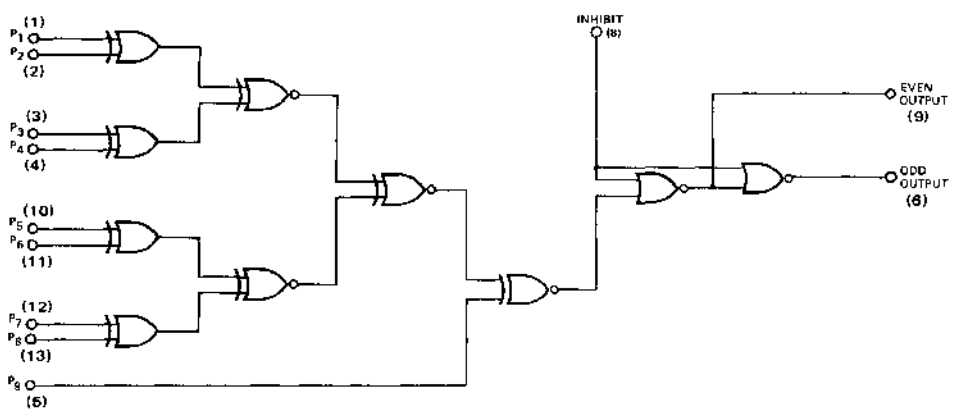
At the receiving end, the 82S62 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- EVEN/ODD PARITY OUTPUTS
- INHIBIT INPUT
- PNP INPUTS

LOGIC DIAGRAM

82S62



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

LOGIC EQUATIONS:

ODD OUTPUT = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

EVEN OUTPUT = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

NOTE: Pin-Outs shown for Dual In-Line package only

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN	TYP	MAX	UNITS	DATA INPUT UNDER TEST			
"1" Output Voltage								
Even	2.7			V	0V	.8V	−1mA	6
Odd	2.7			V	2.0V	.8V	−1mA	6
"0" Output Voltage								
Even			0.50	V	2.0V	.8V	20mA	7
Odd			0.50	V	0V	.8V	20mA	7
"0" Input Current								
Data Inputs P_1–P_8			−800	μA	0.5V			
Data Input P_9			−1.2	mA	0.5V			
Inhibit			−800	μA		0.5V		
"1" Input Current								
Data Inputs			10	μA	4.5V			
Inhibit			10	μA		4.5V		
Power/Current Consumption			365/67	mW/mA				11
Output Short Circuit Current								
Even	−40		−100	mA	0V	0V	0V	11,12
Odd	−40		−100	mA	4.0V	0V	0V	11,12

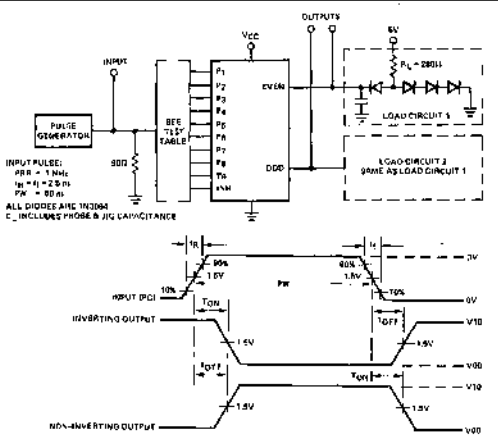
$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN	TYP	MAX	UNITS	UNDER TEST			
Turn-on/Turn-off Times								
P_1 – P_8 to Even			23	ns	Pulse			8
P_1 – P_8 to Odd			28	ns	Pulse			8
P_9 to Even			12	ns	Pulse			8
P_9 to Odd			18	ns	Pulse			8
Inhibit to Even			9	ns		Pulse		8
Inhibit to Odd			9	ns		Pulse		8

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. V_{CC} = 5.25V.
12. Not more than one output should be shorted at a time.

AC TEST FIGURE AND WAVEFORMS



TEST TABLE

TEST NO.	INPUTS P1	P2	P3	P4	P5	P6	P7	P8	P9	INH	OUTPUTS EVEN	ODD
1	PG	0	0	0	0	0	0	0	0	0		T
2	PG	0	0	0	0	0	0	0	0	0	T	T
3	0	0	PG	0	0	0	0	0	0	0	T	T
4	0	0	0	PG	0	0	0	0	0	0	T	T
5	0	0	0	0	PG	0	0	0	0	0	T	T
6	0	0	0	0	0	PG	0	0	0	0	T	T
7	0	0	0	0	0	0	0	0	0	PG	T	T

"1" = 2.7V "0" = GROUND

NOTE

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.

signetics

2-INPUT, 4-BIT DIGITAL MULTIPLEXER

82S66
82S67

B,I PACKAGES

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S66/82S67 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing Schottky TTL circuit structures. The 82S67 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3), B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

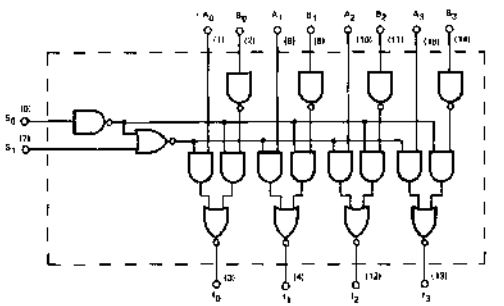
For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with adder elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S67)
- INHIBIT STATE

LOGIC DIAGRAM AND TRUTH TABLE

82S66/82S67



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
"1" Output Voltage (82S66)	2.7	3.5		V	0.8V	2.0V	0.8V	0.8V	−1mA	7
"0" Output Voltage			0.5	V	2.0V	2.0V	2.0V	0.8V	20mA	8
"1" Output Leakage Current (82S67)			250	μA	0.8V	2.0V	2.0V	0.8V	5.5V	
"0" Input Current										
A_n, B_n			−400	μA	0.5V	0.5V	0V	0V		
S_0, S_1			−400	μA			0.5V	0.5V		
"1" Input Current										
A_n, B_n			10	μA	4.5V	4.5V		2.0V		
S_0, S_1			10	μA			4.5V	4.5V		
Output Short Circuit Current (82S66)	−40		−100	mA						12

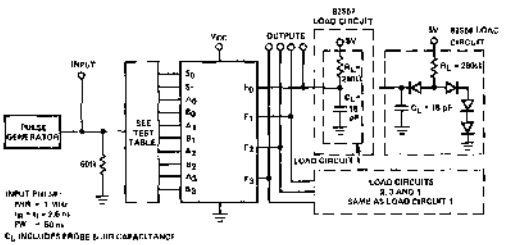
$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
Turn-on/Turn-off Times (82S66)										
S_1 to f_n			15	ns						9
S_0 to f_n			18	ns						9
A_n to f_n			10	ns						9
B_n to f_n			12	ns						9
Propagation Delay (82S67)										
S_1 to f_n			18	ns						9
S_0 to f_n			20							
A_n to f_n			12	ns						9
B_n to f_n			15	ns						9
Power/Current Consumption			385/69	mW/mA	4.5V	0V	4.5V	0V		12

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. V_{CC} = 5.25 V.

AC TEST FIGURE AND WAVEFORMS



TEST TABLE														
TEST NO.	INPUTS										OUTPUTS			
	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	1	PG	1	1	1	1	1	1	1	1	T			
2	1	PG	1	1	1	1	1	1	1	1	T	T	T	T
3	PG	0	1	1	1	1	1	1	1	1	T			T
4	0	0	0	0	0	PG	0	0	0	0		T		
5	0	0	0	0	0	0	0	PG	0	0			T	
6	1	0	PG	1	0	1	0	1	0	1	T			
7	1	0	0	1	0	1	0	1	PG	1				T

"1" = 2.7V "0" = OUTPUT

NOTE:
1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 3/8 INCH LEAD LENGTH FROM PACKAGE PINS.

DESCRIPTION

The 82S70 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.

The 82S71 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 82S70 element.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- SYNCHRONOUS LOAD
- SHIFT RIGHT/LEFT CAPABILITY
- HOLD MODE

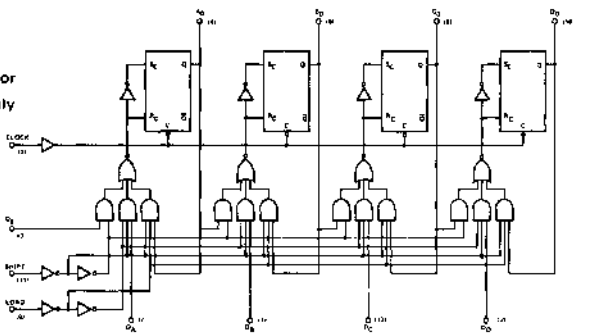
ELECTRICAL CHARACTERISTICS

Transfer Rate	60 MHz (Typ)
Input Load Current (Max)	
I_{in}"0"	400μA
I_{in}"1"	25μA
Output Current	
I_{out}"0"	20mA @ 0.5V
I_{out}"1"	1mA @ 2.7V

LOGIC DIAGRAM

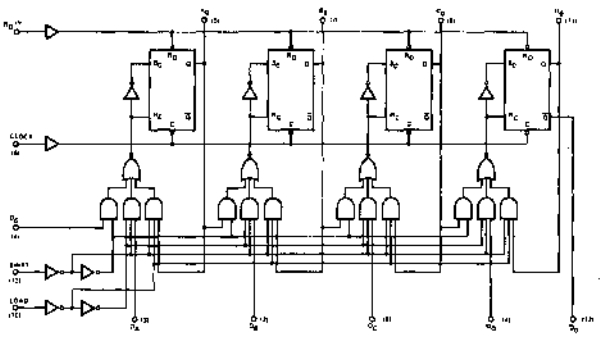
82S70

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14-pin dual in-line package only



82S71

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers



DESCRIPTION

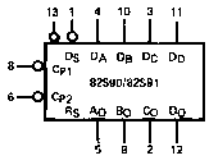
The 82S90 Decade Counter and 82S91 Binary Counter are very high speed versions of the popular 8290 Decade and 8291 Binary Counters. They are multifunctional MSI building blocks capable of being used in counting frequency synthesis, digital integration where high speed is essential.

FEATURES

- **100 MHz TYPICAL COUNT FREQUENCY**
- **HIGH IMPEDANCE PNP INPUTS**
- **VARIABLE MODULUS, ÷2, 4, 5, 8, 10, and 16**
- **STROBED PARALLEL ENTRY**
- **PIN REPLACEABLE for the 8290/8291, 74196/74197**

LOGIC SYMBOL

A, F PACKAGES



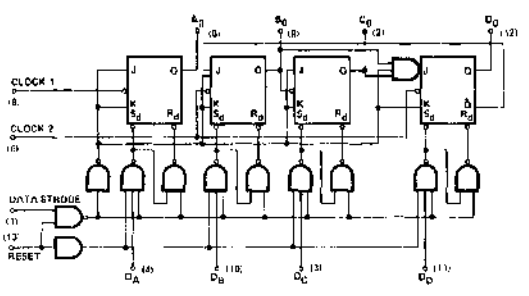
VCC = PIN 14
GND = PIN 7

PIN DESIGNATIONS

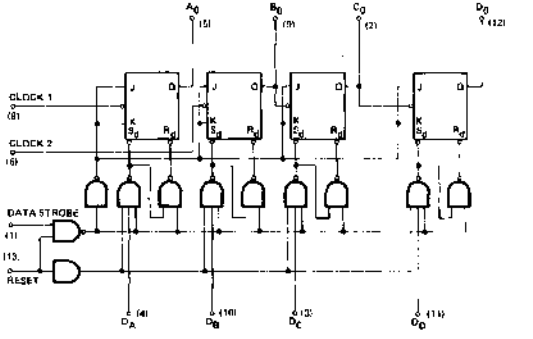
CP_1	Clock input to counter first stage (active low going edge)
CP_2	Clock input to counter last three stages (active low going edge)
DS	Data Strobe Input for enabling data entry
RS	Reset Input for resetting all stages and outputs to zero
D_A, D_B, D_C, D_D	Data Inputs
A_O, B_O, C_O, D_O	Data Outputs

LOGIC DIAGRAMS

82S90



82S91



D.C. ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V			−1mA	6, 8
"0" Output Voltage			0.5	V	0.8V	0.8V	0.8V			20mA	6, 9
"0" Input Current											
Data Strobe			-0.4	mA			5.25V				
Data Inputs			-0.4	mA							
Reset			-0.4	mA	5.25V						
Clock 1			-6.0	mA	5.25V						
Clock 2 (8290)			-6.0	mA	5.25V						
Clock 2 (8291)			-3.0	mA	5.25V						
"1" Input Current											
Data Strobe			10	μA	4.5V		0.0V				
Data Inputs			10	μA		4.5V					
Reset			10	μA	0.0V		4.5V				
Clock 1			100	μA	0.0V			4.5V			
Clock 2 (8290)			100	μA	0.0V				4.5V		
Clock 2 (8291)			50	μA	0.0V				4.5V		
Output Short Circuit Current	-40		-100	mA	0.0V	4.5V				0.0V	11, 12
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Clock 1 & 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				
Power Consumption/		308	461	mW/			0.0V	0.0V	0.0V		12
Supply Current		62	88	mA							

A.C. ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V

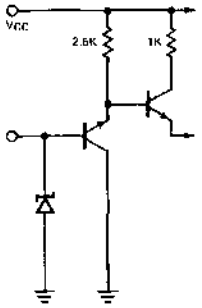
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Strobe Pulse Width		5		ns					A_{OUT}		9
Reset Pulse Width		7		ns					A_{OUT}		9
Strobe/Reset Release Time		10		ns					A_{OUT}		9
Clock Mode t_{on} Delay											
Bit A		9	12	ns							9
Bits B, C, D		10	13	ns							9
Clock Mode t_{off} Delay											
Bit A		5	8	ns							9
Bits B, C, D		6	10	ns							9
Strobed Data t_{on} Delay											
(All Bits)		15	22	ns							9
Strobed Data t_{off} Delay											
(All Bits)		13	20	ns							9
Toggle Rate	85	100		MHz							9

NOTES:

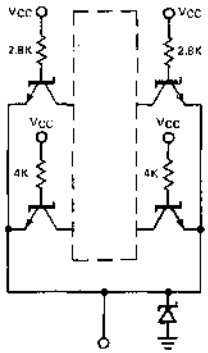
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. Not more than one output should be shorted at a time.
12. V_{CC} = 5.25V.

INPUT AND OUTPUT STRUCTURES

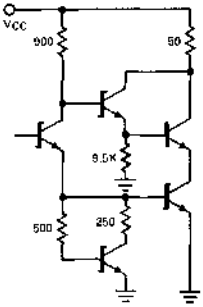
DATA, STROBE and RESET INPUTS



CLOCK INPUTS

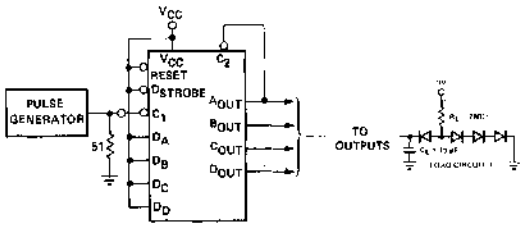


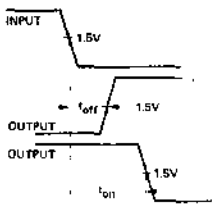
OUTPUTS



AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY

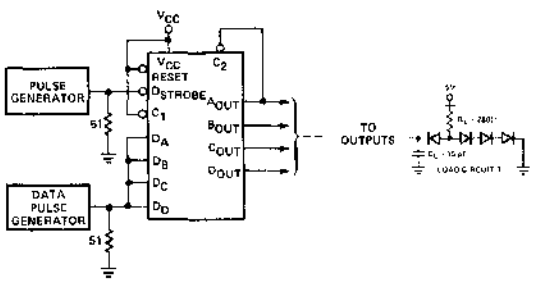


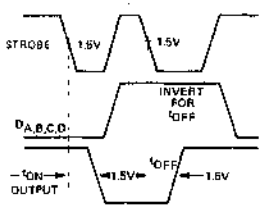


Note:
t_{on} and t_{off} are measured from the clock input of each binary to the Q

INPUT PULSE:
Amplitude = 2.6V
PW = 30ns, 50% to 50%
$t_r = t_f$ = 5ns

STROBED DATA t_{on}/t_{off} DELAY



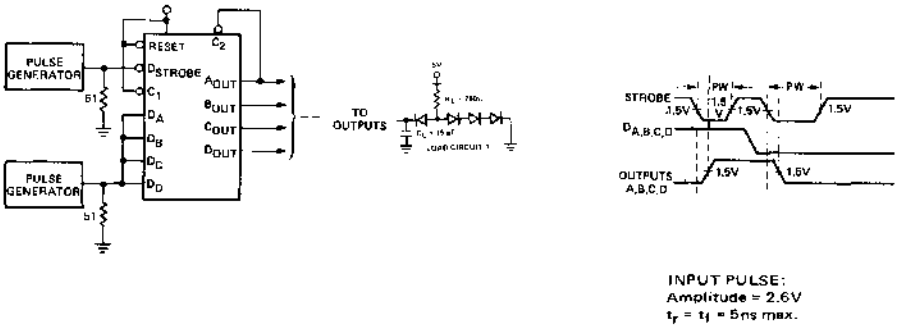


Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f$ = 5ns

Data,
P.A. = 2.6V
P.W. = 500ns, 50% to 50%
PRR = 500KHz
$t_r = t_f$ = 5ns

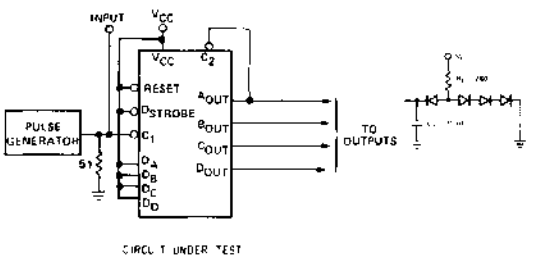
AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM STROBE PULSE WIDTH



INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

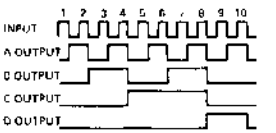
TOGGLE RATE



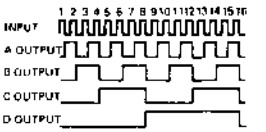
CIRCUIT UNDER TEST

INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz, 50% duty cycle
$t_r = t_f$ = 5ns max

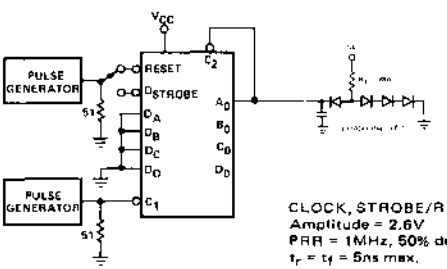
82S90



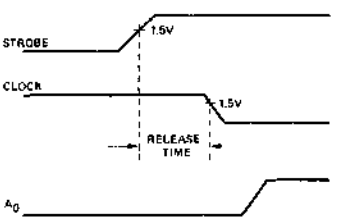
82S91



STROBE/RESET RELEASE TIME



CLOCK, STROBE/RESET:
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.



NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.

FUNCTIONAL DESCRIPTION

1. 82S90 Decade Counter

The 82S90 can be used in three basic count modes as follows:

a. BCD Counter. The CP2 input must be connected to the A_O output and CP1 receives the count input. The count sequence obtained is BCD in accordance with the truth table.

b. Bi-Quinary Counter. If a symmetrical output is required for divide by 10 operation, the D_O output must be connected to the CP1 input and the count input applied to CP2. A symmetrical square wave is then obtained at A_O of one-tenth the input frequency present at CP2 in accordance with the truth table.

c. Separate Divide by Two and Five Counters. Because the inherent structure of the counter is that of two separate divide by two and divide by five sections, no other connections are required for this mode of operation. An input presented to CP1 will appear at A_O output at half the input frequency. An input presented to CP2 will appear at outputs B_O, C_O and D_O as a binary divide by five count (i.e., from 0 = 000 to 4 = 100). Operation of the D_S and R_S inputs remain common to all four flip flops as with any other count mode.

TRUTH TABLES

Decade (BCD)				
Input	A_O	B_O	C_O	D_O
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

Bi-Quinary (5-2)				
Input	A_O	B_O	C_O	D_O
0	0	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	1	1	0
4	0	0	0	1
5	1	0	0	0
6	1	1	0	0
7	1	0	1	0
8	1	1	1	0
9	1	0	0	1

2. 82S91 Binary Counter

The 82S90 can be used in two basic count modes as follows:

a. Binary Counter—For this mode of operation A_O output must be connected to CP2 input and the count input connected to CP1. Subdivisions of the count input frequency then appear at A_O = ÷2, B_O = ÷4, C_O = ÷8, D_O = ÷16 as shown in the truth table.

b. Separate Divide by Two and Divide by Eight Counters—In similar manner to the 82S90 the 82S91 inherent structure allows separate use of the first and last three stages. In the first stage the input count frequency presented to CP2 appears at outputs B_O = ÷2, C_O = ÷4 and D_O = ÷8 simultaneously. Operation of the D_S and R_S inputs remains common to all stages.

TRUTH TABLE

Binary				
Input	A_O	B_O	C_O	D_O
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

3. Operation of the D_S Data Strobe and R_S Reset Inputs:

a. Data Strobe D_S Input—When D_S = 0 the four stages of the 82S90/91 can be used as four separate latches with the outputs A_O - D_O following the data presented to the inputs D_A - D_D regardless of clock inputs.

With D_S = 1 the four stages remain unchanged until the next clock inputs, which activate counting in accordance with the various modes described previously. The Reset R_S inputs when low overrides D_S as described below.

b. Reset R_S Input—With R_S = 0 the clock inputs CP1/CP2 and D_S input are overridden, all stages of the 82S90/91 are cleared and zeros appear at the counter outputs A_O - D_O. When R_S = 1, operation is controlled by D_S or CP1/CP2 clock inputs as described.

signetics

4-BIT BCD ARITHMETIC UNIT
4-BIT BCD ADDER

82S82
82S83

PRELIMINARY INFORMATION

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S82 Binary Coded Decimal (BCD) Arithmetic unit and the 82S83 Binary Coded Decimal (BCD) Adder are Schottky MSI circuits that have been designed for easy systems usage. Each unit provides a single IC solution to perform BCD Arithmetic that previously had to be implemented with several Binary Adders, Exclusive OR's, ROM's and Gates

High Speed operation is achieved with Schottky TTL technology and use of PNP high impedance inputs results in reduced input loading compared with conventional TTL.

82S82 BCD Arithmetic Unit
FEATURES

- Adds and Subtracts BCD Numbers
- Converts Binary to BCD
- Comparison Output (Open Collector)
- Internal Look-Ahead Carry/Borrow
- Fast Look-Ahead Carry/Borrow Outputs
- Ripple Carry/Borrow Output
- Easy Array Expansion

82S83 BCD Adder
FEATURES

- Adds BCD Numbers
- Converts Binary to BCD
- Internal Look-Ahead Carry
- Ripple Carry Output
- Easy Array Expansion

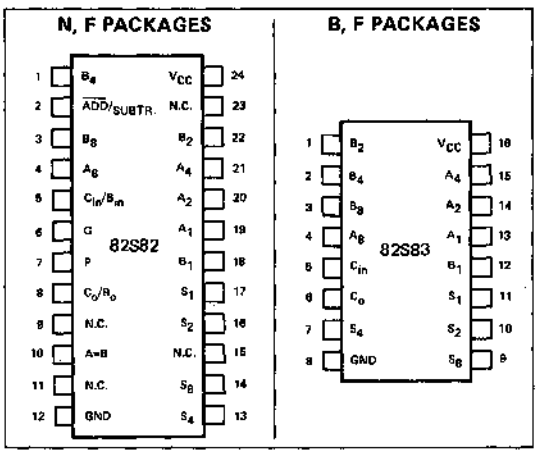
ELECTRICAL CHARACTERISTICS

Propagation Delay (Typ.)	82S82	82S83
A_n to S_n	29ns	29ns
B_n to S_n	32ns	29ns
A_n to C_o/B_o	22ns	22ns
B_n to C_o/B_o	29ns	22ns
A_n to G or P	20ns	-
B_n to G or P	23ns	-
Input "0" Current (Max.)	**82S82**	**82S83**
A_n, C_{in}, B_4, B_8	0.4mA	0.4mA
B_1 B_2	0.8mA	0.4mA
$\overline{Add}$/Subtract	0.8mA	-
Input "1" Current (Max.)		
(All Inputs)	40μA	
"0" Output Current	16mA	@ 0.5V
"1" Output Current (Except A=B Output)	800μA	@ 2.7V

82S82 BCD ARITHMETIC UNIT

Pin Designation	Pin Nos.	Function
A_8, A_4, A_2, A_1	4, 21, 20, 19	BCD Inputs Word A Weighted (8-4-2-1)
B_8, B_4, B_2, B_1	3, 1, 22, 18	BCD Inputs Word B Weighted (8-4-2-1)
S_8, S_4, S_2, S_1	14, 13, 16, 17	BCD Sum Outputs Weighted (8-4-2-1)
$\overline{Add}$/Subtract	2	Add=Logic "0" Subtract=Logic "1"
C_{in}/B_{in}	5	Carry/Borrow Input
C_0/B_0	8	Carry/Borrow Output
G	6	Carry Generate Output (Active Low)
P	7	Carry Propagate Output (Active Low)
A = B	10	Compare Output (Open Collector)
V_{CC}	24	Supply Voltage
GND	12	Ground

PIN CONFIGURATIONS (Top View)



82S83 BCD ADDER

Pin Designation	Pin Nos.	Function
A_8, A_4, A_2, A_1	4, 15, 14, 13	BCD Inputs Word A Weighted (8-4-2-1)
B_8, B_4, B_2 B_1	3, 2, 1, 12	BCD Inputs Word B Weighted (8-4-2-1)
S_8, S_4, S_2, S_1	9, 7, 10, 11	BCD Sum Outputs Weighted (8-4-2-1)
C_{in}	5	Carry Input
C_0	6	Carry Output
V_{CC}	16	Supply Voltage
GND	8	Ground

SECTIONS
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SECTIONS

signetics

BIPOLAR
MEMORY PRODUCT
SPECIFICATIONS

4

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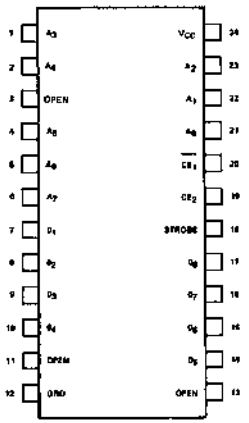
SECTIONS

Bipolar Memory Functional Index

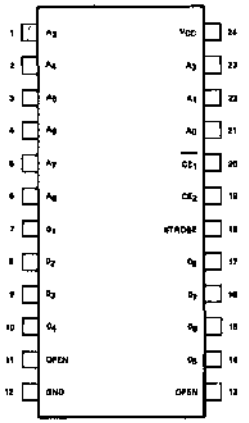
PIN CONFIGURATIONS

8204



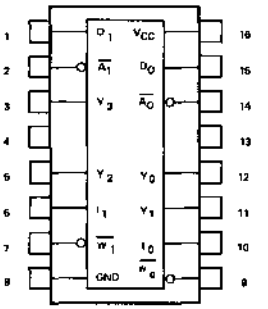
I PACKAGE

8205



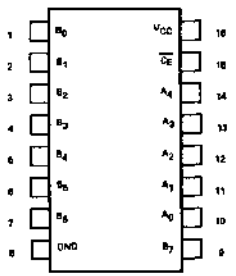
I PACKAGE

8220



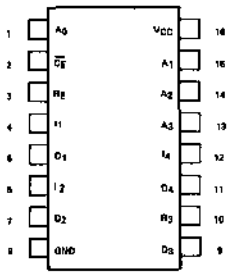
B, F PACKAGES

8223/24
82S23
82S123



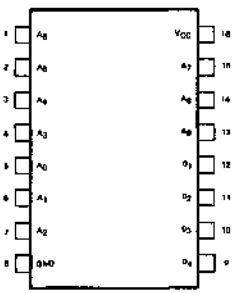
B, F PACKAGES

8226



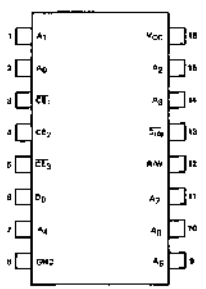
B, F PACKAGES

8228



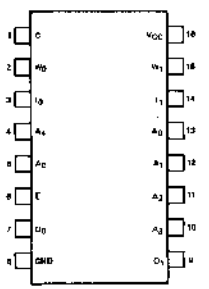
I PACKAGE

82S06/07/16/17



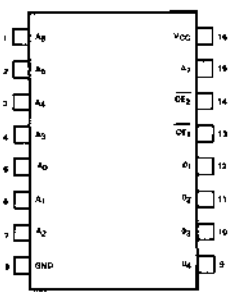
I PACKAGE

82S21



L PACKAGE

82S26/29



I PACKAGE

signetics

2048 BIT BIPOLAR ROM (256x8 ROM)
4096 BIT BIPOLAR ROM (512x8 ROM)

8204
8205

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8205 and 8204 are high performance bipolar ROM's incorporating the storage output or memory data register into the chip. Data is addressed by applying address information to the address lines. After valid data appears at the output of the memory array, (typically 35ns after the address is applied) and if the circuit is enabled, the strobe pulse will enter data into the 8 bit output latch register. A D-type latch (L) is used to enable the tri-state output drivers. If the circuit enable signals are valid, the strobe will set the latch. This turns on the output stage. The latch will remain set and keep the output enabled until the chip is disabled and the next strobe pulse occurs. If the strobe line is held high, the ROM will function in a conventional mode. The output will be controlled solely by the chip enable and the output latches will be bypassed.

See page 4-34 for ASCII (ADDRESS) to EBCDIC (DATA) and EBCDIC (ADDRESS) to ASCII (DATA) and 4-35/ for 4-53 for ORDERING BLANKS.

APPLICATIONS

- MICROPROGRAMMING
- HARDWIRE ALGORITHMS
- CHARACTER GENERATION
- CONTROL STORE

FEATURES

BUFFERED ADDRESS LINES

ON THE CHIP DECODING

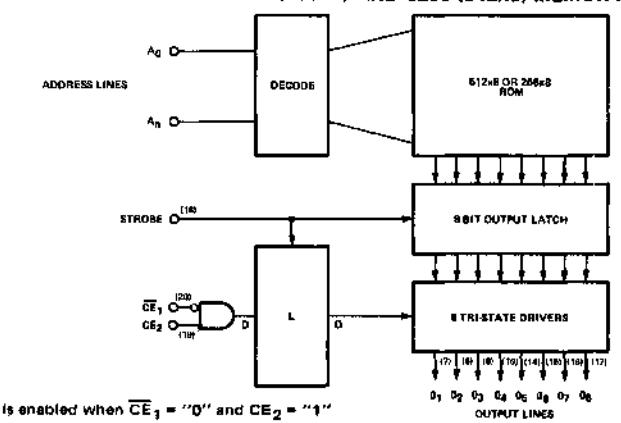
ON THE CHIP STORAGE LATCHES

TRI-STATE OUTPUT

PROTECTED INPUTS

BLOCK DIAGRAM

8204 (256x8) AND 8205 (512x8) MEMORY ORGANIZATION



Chip is enabled when $\overline{CE}_1$ = "0" and CE_2 = "1"

Address Pins	8204	8205
A_0	(21)	(20)
A_1	(22)	(21)
A_2	(23)	(23)
A_3	(1)	(1)
A_4	(2)	(2)
A_5	(4)	(3)
A_6	(6)	(4)
A_7	(8)	(5)
A_8	–	(6)

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Input "0" Current			-100	μA	V_{in} = 0.5V	
Input "1" Current			25	μA	V_{in} = 5.25V	
Input (0) Threshold Voltage			.85	V		
Input (1) Threshold Voltage	2			V		
Input Clamp Voltage	-1.0			V	I_{in} = -5.0mA	
Output (0) Current		0.2	0.5	V	I_{out} = 9.6 mA	
Output (1) Current	2.7	3.3		V	I_{out} = -2.0mA	
Output (1) Short Circuit Current	-20	-35	-70	mA	V_{out} = 0V, V_{CC} = 5.0V	2
Input Capacitance		5		pF	V_{IH} = 2.0V, V_{CC} = 5.0V	
Output Capacitance		8		pF	V_{out} = 2.0V; V_{CC} = 5.0V	5
Power Supply Current		135	170	mA	V_{CC} = 5.0V	
Output (1) off Leakage Current (Chip Disabled)			100	μA	V_{in} = 2.7V	
Output (0) off Leakage Current (Chip Disabled)			-100	μA	V_{in} = 0.5V	

T_A = 25°C and V_{CC} = 5.0V

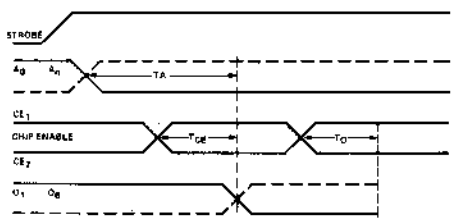
CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Address Access Time T_A		35	60	ns	Read Mode I or Read Mode II	6
Address Hold Time T_{ADS}	0	-10		ns	Read Mode 2 Only	6
Chip Enable Access Time T_{CE}		20	45	ns	Read Mode I or Read Mode II	6
Chip Enable Hold Time T_{CDS}	12	5		ns	Read Mode II Only	6
Output Disable Time T_O		20	45	ns	Read Mode I or Read Mode II	6
Strobe Pulse Width T_{SW}	33	20		ns	Read Mode II Only	6
Strobe Set-Up Time T_S		30	60	ns	Read Mode II Only	6
Output Disable Time T_R		18	32	ns	Read Mode I Only	6

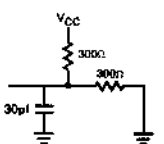
NOTES:

1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 5.5V.
   Input currents must not exceed ±30 mA.
   Output currents must not exceed ±100 mA.
   Storage temperature must be between −60°C to +150°C.
5. Chip disabled.
6. Rise and fall times for tests must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

MEMORY TIMING

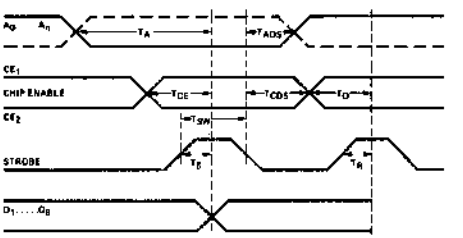
READ MODE I (OUTPUT LATCHES NOT USED)



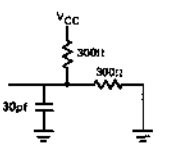


If the strobe is high, the device functions in a manner identical to conventional bipolar ROM's. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_O is the time required to disable the output and switch it to an 'off' or high impedance state after it has been enabled.

READ MODE II (OUTPUT LATCHES USED)



NOTE: Outputs are undefined during the strobe setup time, T_S



In Read Mode II, the address is applied to the memory element T_A ns before output details desired. Applying the chip enable does not directly enable the outputs. When the strobe is applied T_S nanoseconds before the output, data from the memory array is copied into the output latches and the chip enable signal is copied into the delay latch L. The latch L in turn enables the output. After the strobe reaches the strobe level, both the chip enable and address lines may be altered but the output data stored in the latches will remain unchanged and the output of the circuit will remain enabled. The output will stay enabled until another strobe copies a Not chip enable signal into the latch L. The switching of the output to the "off" or high impedance state occurs T_R nanoseconds after the strobe.

signetics

8-BIT CONTENT ADDRESSABLE MEMORY (4x2 CAM) 8220

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8220 CAM Element is a high speed monolithic array, incorporating the necessary addressing logic and eight identical memory cells organized as four words, each being two bits long. In reference to data-in/data-stored, the 8220 can be conditioned to perform the following functions: associate, write-in only, and read-out only.

When addressed into the "ASSOCIATE" mode, this element offers the novel capability of data association, where each cell (M_{ij}) will respond with a "Match" or "Mismatch" answer (Y_n) to each bit presented to the data inputs (I_j), depending on presence or absence of an alike bit stored within the cell.

Write-in can be simultaneously done to all bits, or one bit at a time. Read-out of stored information is performed on one word at a time. Cell-selection for read and write is performed by proper addressing of Y_n and A_n lines.

The element's output structures (Y_n and D_j) are of the "bare collector" variety and can be mutually connected, thus allowing direct expansion when multiple packages are employed. Expansion of the CAM may be implemented in both directions, i.e., in the word length and in the number of words.

The CAM circuit structure is the familiar TTL type (DCL Family) and fully compatible with TTL and DTL input/output structures.

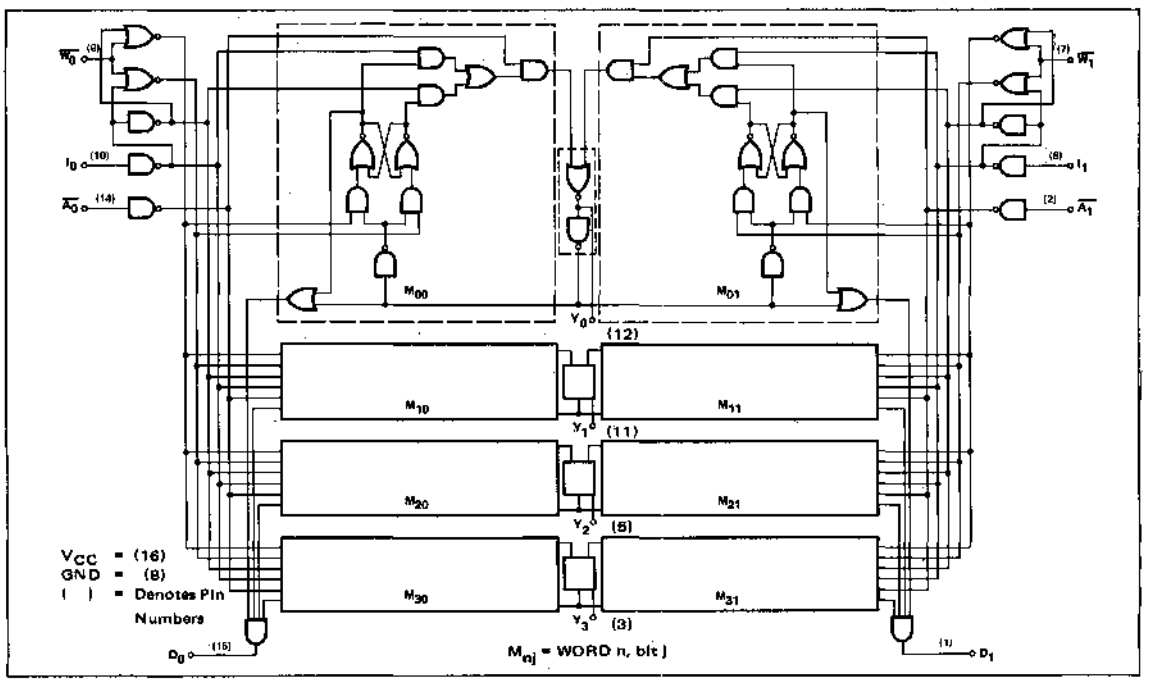
FEATURES

- WRITE ENABLE CONTROL LINES
- ASSOCIATE CONTROL LINES
- ADDRESS SELECT CONTROL LINES
- ASSOCIATES IN 20nsec TYP.
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

DATA-TO-MEMORY COMPARISON
PATTERN RECOGNITION
HIGH SPEED INFORMATION RETRIEVAL
CACHE MEMORY
AUTO CORRELATION
VIRTUAL MEMORY
LEARNING MEMORY

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS				$\overline{Wj}$	$\overline{Aj}$	I_j	Yl	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
"0" Output Voltage											
Yn			0.4	V	2.0V	0.8V	2.0V	30mA			8, 9
			0.6	V	2.0V	0.8V	2.0V	60mA			
Dj			0.4	V	2.0V	2.0V			0.8V	20mA	8, 9
			0.6	V	2.0V	2.0V			0.8V	40mA	
"1" Output Leakage Current											
Yn			125	μA		2.0V					10
Dj			100	μA				0V	0V		10
"1" Input Current											
Ij and $\overline{A_j}$			40	μA		4.5V	4.5V				
$\overline{W_j}$			80	μA	4.5V						
"0" Input Current											
Ij, Yn and $\overline{Aj}$	-0.1		-1.2	mA		0.4V	0.4V	0.4V			
$\overline{W_j}$			-2.4	mA							

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				Wj	Aj	Tj	Yl	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
Delay Time											
Associate ($\overline{Aj}$ to Yn)		20	30	ns							8, 11
Associate (Ij to Yn)		35	45	ns							8, 11
Read-Out (Yn to Dj)		30	40	ns							8, 11
Write-In to Read-Out ($\overline{Wj}$ to Dj)		45	60	ns							
Write Pulse Width		20	35	ns							
Power Consumption			590/ 118	mW/mA							

NOTES:

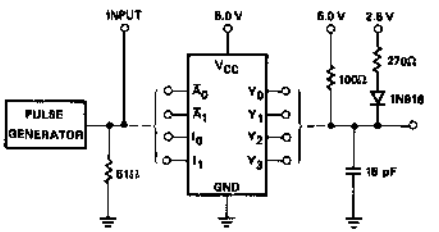
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Prior to this test write in a "0" in all or desired Memory cells as follows: Wj = Ij = 0V, Aj = V_{CC}.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Connect an external 1K ohm ± 1% resistor from V_{CC} to the output terminal for this test.
11. See AC test Figures on the following pages.

MODE OF OPERATION

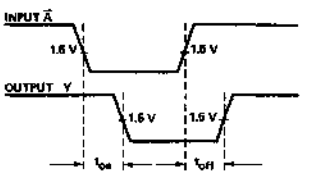
FUNCTION	$\overline{W_0}\ \overline{W_1}\ \overline{A_0}\ \overline{A_1}\ I_0\ I_1$	REMARKS (Ref. Definitions & Glossary)	FUNCTION	$\overline{W_0}\ \overline{W_1}\ \overline{A_0}\ \overline{A_1}\ I_0\ I_1$	REMARKS (Ref. Definitions & Glossary)
HOLD	1 1 1 1 x x	NO OPERATION	HOLD	1 1 1 1 x x	NO OPERATION
ASSOCIATE	1 1 1 0 x x	Question: $I_1=M_{i1}$? YES — Y_i=1, Y_k=0; NO — $Y_i=Y_k$=0	WRITE-IN	1 0 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_1 into M_{i1}
				0 1 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_0 into M_{i0}
	1 1 0 1 x x	Question: $I_0=M_{i0}$? YES — Y_i=1, Y_k=0; NO — $Y_i=Y_k$=0		0 0 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_1 and I_0 into M_{i1} and M_{i0}
	1 1 0 0 x x	Question: $I_1=M_{i1}$ and $I_0=M_{i0}$? YES — Y_i=1, Y_k=0; NO — $Y_i=Y_k$=0	READ-OUT	1 1 1 1 x x	Forced Y_i=1, Y_k=0: D_0= 1 - IF M_{i0}=1, 0 - IF M_{i0}=0
				1 1 1 1 x x	Forced Y_i=1, Y_k=0: D_1= 1 - IF M_{i1}=1, 0 - IF M_{i1}=0
				1 1 1 1 x x	Forced Y_i=0, Y_k=0: $D_0=D_1$ = 1

AC TEST FIGURES AND WAVEFORMS

ASSOCIATE DELAY AND INPUT DELAY

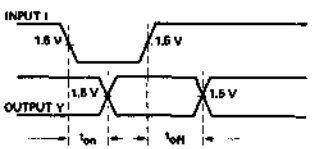


ASSOCIATE DELAY



NOTES:
1. When checking $\overline{A_0}$ let $\overline{A_1}$ = "1" and when checking $\overline{A_1}$ let $\overline{A_0}$ = "1".
2. $\overline{W_0}$ = $\overline{W_1}$ = "1".

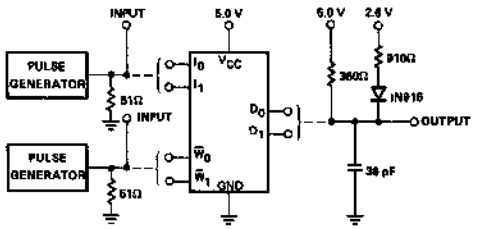
INPUT DELAY

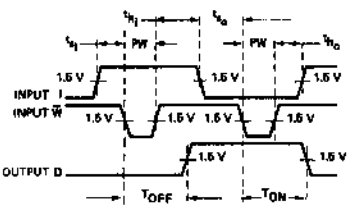


NOTES:
1. When checking I_1, $\overline{A_1}$ = "0" and $\overline{A_0}$ = "1" and when checking I_0, $\overline{A_0}$ = "0" and $\overline{A_1}$ = "1"
2. $\overline{W_0}$ = $\overline{W_1}$ = "1".

AC TEST FIGURES AND WAVEFORMS (Cont'd)

WRITE DELAY

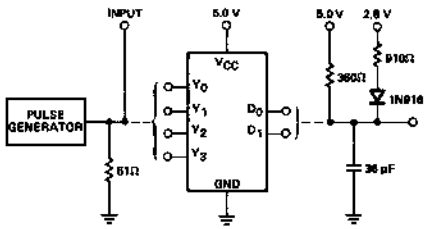


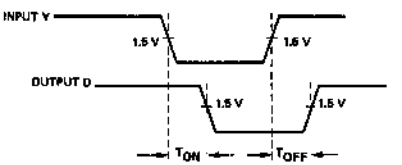


t_{si} = "1" set-up time.
t_{so} = "0" set-up time.
t_{hi} = "1" hold time.
t_{ho} = "0" hold time.
PW = Pulse width

NOTES:
1. $A_0 = A_1 = "1"$.
2. Let all non-selected Y's = "0".
3. W's pulse width is 40ns @50% points.

READ DELAY





NOTES:
1. A tested bit must store a "0".
2. $\overline{W}_0 = \overline{W}_1 = "1"$.
3. $\overline{A}_0 = \overline{A}_1 = "1"$.
4. All non-tested Y's = "0".

GENERAL NOTES FOR AC TESTING:
1. Use 5k Probes for all AC tests TEK 169 or equivalent.
2. The Pulse Generator signal should consist of the following
   Frequency: 10 MHz ±5 MHz
   Amplitude: 0V to 3V
   Rise & Fall Times: 5 ns ±2ns
3. i = bit number (i = 0, 1). j = word number (j = 0, 1, 2, 3).

INPUT/OUTPUT DEFINITIONS

I_j – Data Inputs
Data entering these terminals are either compared with stored information at the cell(s) in the "associate" mode or stored in the cell(s) in the "write-in" mode.

$\overline{A}_j$ – Associate Controls
A logical "0" at this pin enables Data-Cell association to result into a defined logical level at the Y_n lines (e.g. Y_n = "1" = Match, Y_n = "0" Mismatch). A logical "1" at this pin forces all Y_n to a "1".

$\overline{W}_j$ – Write Enable
A logical "0" at this control pin opens the gates of the selected word, allowing data-in to be stored. A logical "1" locks the gates such that data-in can no longer disturb the cell(s).

Y_n – "Associate" Output and Address Selection Control
During "Associate" mode these "bare collector" lines provide output results of match or mismatch between input and stored data (logical "1" = Match, logical "0" = Mismatch).

In the read and write modes these terminals act as input controls and word-select lines Y lines (Y_1) associated with words desired to accept writing of data or read-out are to be kept in the logical "1" state and the remaining Y lines (Y_k) to be forced to a logical "0" state. (Note that A = 1 forces all Y_n = 1).

D_j – Data Output
These are "bare collector" output lines indicating the state of one or more selected cells. Cell-Selection is accomplished as defined under "Y_n" above.

GLOSSARY OF TERMS – SUBSCRIPTS

A. n = Word number = 0, 1, 2 and 3
   j = Bit number = 0 or 1
   l = Input/Output number(s) associated with cell(s) upon which a "Write-In", "Read-out" or other function is being performed.
   k = Input/Output number(s) other than "l" above.
   M = Designation of Memory Cell (word) = eight identical cells in each package.

B. Examples
   1. I_j for bit "1" equals I_1.
   2. $M_{nj} = M_{10}$ = word "1" bit "0".
   3. $Y_l = 0$, $Y_k = 1$: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3} = 0$ and $Y_{0,2} = 1$.

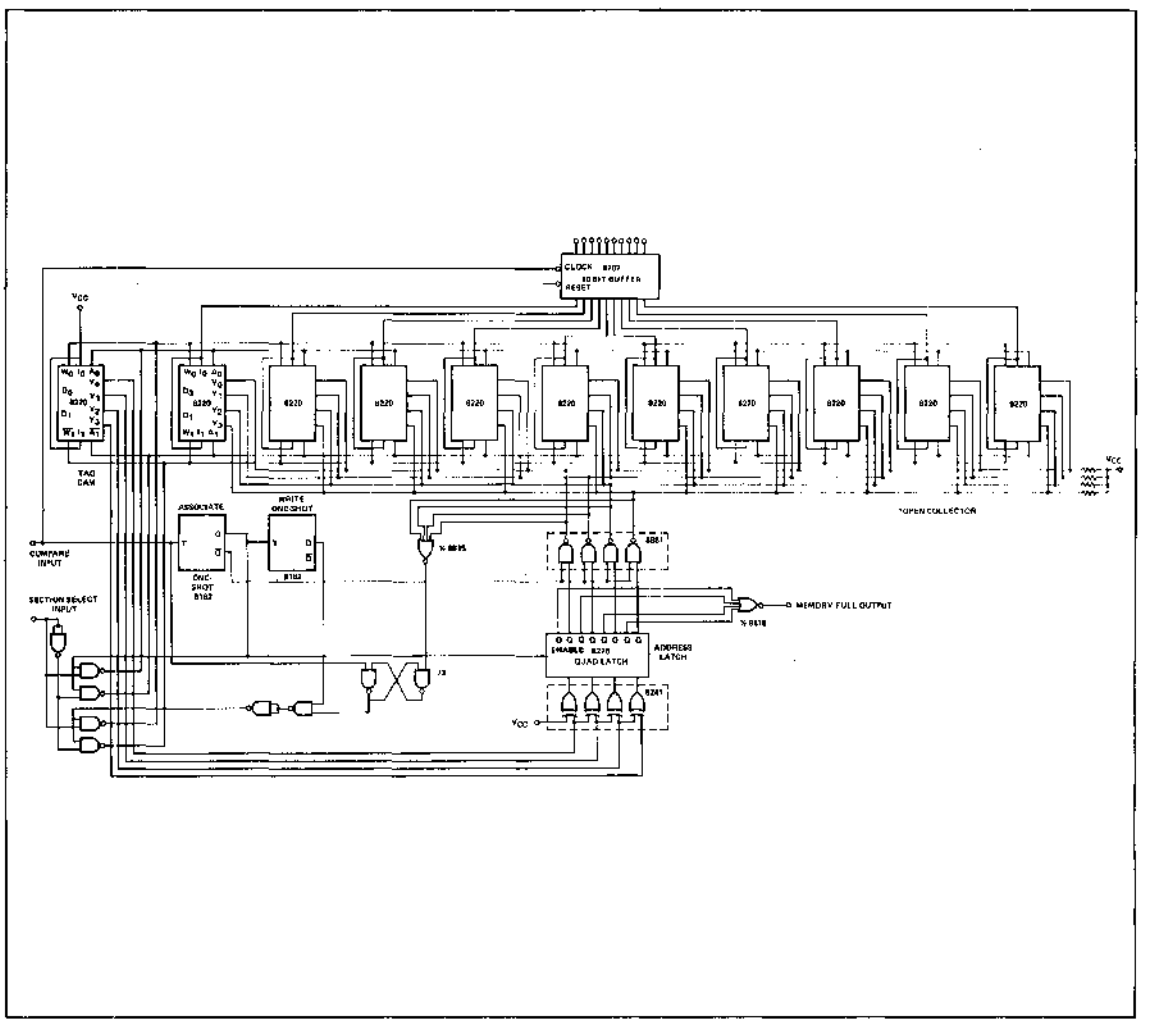
APPLICATION: LEARNING MEMORY

This system is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being 8 ten bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in the number of words and in word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word, with which the memory was presented, is already contained in storage, no need for "learning" i.e. data acquisition, exists. This fact is indicated by a match from one of the Y_n lines ($Y_i = 1$) and thus no write command is initiated.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

By monitoring the Y_n lines of the tag CAM, a convenient way of decoding an available address exists. Here exclusive OR circuitry is used which ensures that memory locations are filled successively when the need for "learning" exists. The quad latch is enabled before the write command is available to the CAM array. Thus the Y lines of unavailable memory locations are forced low ($Y_k = 0$).



DESCRIPTION

The 8223 is a TTL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which permits wired AND operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum. The 8223 may be programmed to any desired pattern by the user. (See fusing procedure.) This feature is ideal for prototype hardware and systems requiring propriety codes.

A Truth Table/Order Blank is included on page 4-43 for ordering custom patterns.

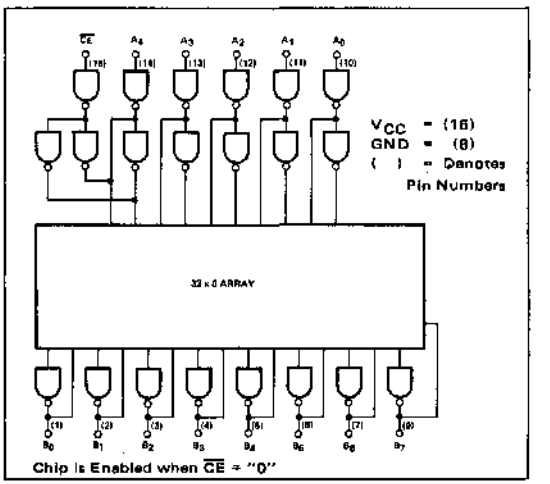
FEATURES

- **BUFFERED ADDRESS LINES**
- **ON THE CHIP DECODING**
- **CHIP ENABLE CONTROL LINE**
- **OPEN COLLECTOR OUTPUTS**
- **DIODE PROTECTED INPUTS**
- **NO SEPARATE FUSING PINS**
- **BOARD LEVEL PROGRAMMABLE**

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (S8223 $-55°C \leq T_A \leq +125°C$ N8223 $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
"1" Output Leakage Current (N8223-)			100	μA			2.0V		13
(S8223-)			250	μA					
"0" Output Voltage (N8223-) (S8223-)			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
(N8223-)			0.5	V	0.8V	2.0V	0.8V	16mA	6,10
"1" Input Current									
An, Address			40	μA		4.5V			
$\overline{\text{Chip Enable}}$ Input			80	μA			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1		-1.6	mA	0.4V		0.4V		

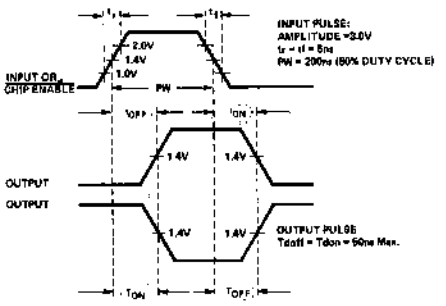
T_A = 25° C and V_{CC} = 5.0V

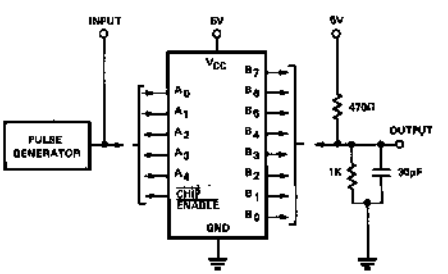
CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
Propagation Delay									
An to Bn		35	50	ns				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to B_n		35	50	ns		4.5V		DC F.O.=12	7,12
Power Consumption		310/62	400/77	mW/mA		4.5V	4.5V		14
Input Latch Voltage	5.5			V			10mA		11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1" "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
14. V_{CC} = 5.25V.

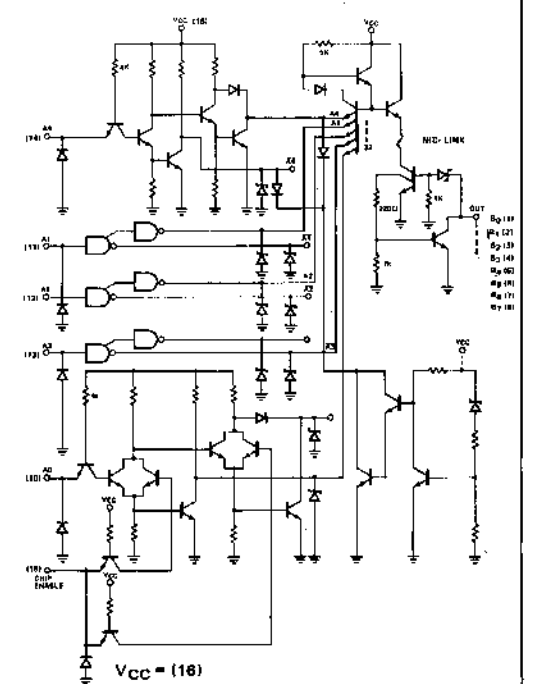
AC TEST FIGURE AND WAVEFORMS





Ground Pin 15 When Testing Address-Output Delays

SCHEMATIC DIAGRAM



V_{CC} = (16)
GND = (8)
(8) denotes pin number ( )

8223 PROGRAMMING PROCEDURE

The 8223 may be programmed by using Curtis Electro Devices, Spectrum Dynamics or Data I/O Programmers.

The 8223 Standard part is shipped with all outputs at logical "0". To write a logical "1" proceed as follows:

Programming Procedure A

Simple Programming Procedure using "bench" Equipment

1. Start with pin 8 grounded and V_{CC} removed from pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground (i.e., 0.4V maximum) for a "0", and +5.0V (i.e., +2.8V minimum) for a "1" at the address input lines.
5. Apply +12.5V ± 0.5V to the output to be programmed through a 390 ohm ± 10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 50 msec to 1sec (max.) with a V_{CC} rise time of 50μsec or less. If 1.0 second is exceeded, the duty cycle should be limited to a maximum of 25%. The V_{CC} overshoot should be limited to 1.0V maximum. If necessary, a clamping circuit should be used. The V_{CC} current requirement is 40 mA maximum at +12.5V. Several fuses can be programmed in sequence until 1.0 sec of high V_{CC} time is accumulated before imposing the duty cycle restriction.

   NOTE: Normal practice in test fixture layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A capacitor of 10 microfarads minimum, connected from the +12.5V to ground, should be located close to the unit being programmed.
7. Remove the programming voltage from pin 16.
8. Open the output.
9. Proceed to the next output and repeat, or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 8223.

Fast Programming Procedure — Programming Procedure B

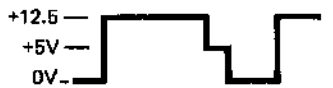
1. Remove V_{CC} (open or ground pin 16).
2. Remove any load from the output.
3. Ground $\overline{CE}$ (pin 15).
4. Address the word to be programmed by applying 5 volts of a "1" and ground for a "0" to the address lines. (Solid TTL logic levels are ok, but we suggest buffer drivers or Utilogic OR/NOR gates for the addressing).
5. Apply +12.5V ± 0.5V to the output to be programmed through a 390 ohm ± 10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 25-50mS. The V_{CC} rise time must be 50μsec or less. Limit the V_{CC} overshoot to 1.0 volts max.
7. Reduce V_{CC} to ground (< 0.5V) and remove the load from the output.
8. Immediately repeat steps 5 and 6 for other outputs of the same word, or repeat 4 through 6 for a different word. Continue programming for a max of 1 second. Then remove power for 4 seconds and continue until the entire bit pattern is programmed.

After programming the 8223, the unit should be checked to insure the code is correct. If additional fuses must be opened, they may be programmed during verification.

Fast Programming Procedure — Programming Procedure C
Steps 1 through 5 are the same as in Procedure B.

6. Apply a 5mS pulse to V_{CC} (pin 16). Limit the V_{CC} overshoot.
7. Reduce V_{CC} to 5 volts for 10-15uS and verify the fuse opened (output is now a "1". If the bit programmed go on to the next bit to be programmed. If the bit did not program, then reduce V_{CC} to ground (or open) for 1-5uS and repeat step 6 and 7 until the fuse programs (1 second total time max).
8. Continue programming at this rate for 1 second. Remove all power from the device for 4 seconds then continue programming procedure.

V_{CC} Waveform

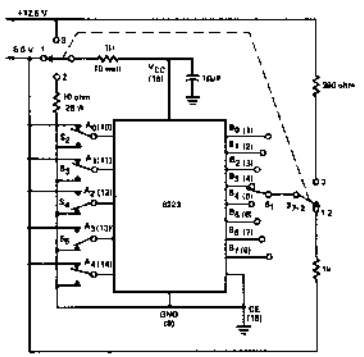


BOARD LEVEL PROGRAMMING PROCEDURE FOR THE 8223

The chip select controls which 8223 is being programmed when several PROMS are collector OR'd. To program in this manner, the only changes required are:

1. The 390 ohm resistor is reduced to $\frac{200 \text{ ohm}}{N}$ where N is the number of outputs tied together ($2 \leq N \leq 12$).
2. Reduce max fuse pulse width from 1 second max to 0.92 sec max.

MANUAL PROGRAMMER DIAGRAM



S_1 = Single pole 9 position switch
S_2 through S_6 = single pole 2 position switch
S_7 = Two pole 3 position switch with ground connected to the middle position of the section connected to V_{CC}, pin 16 to go from 5 volts to 12.5V the switch will momentarily ground V_{CC} and positions 1 and 2 of the other section connected to 5.0V to provide the needed 5 volts to the output for verification.

NOTE:
1. The 10μf capacitor across pin 16 to ground is required to eliminate noise from V_{CC}.
2. During programming switch S_7 must be in position 2 long enough for the 1.0μf capacitor to discharge to less than 0.5 volts.

DESCRIPTION

The 8224 is a TTL 256 Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Enable input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Enable input is taken high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-AND operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

The 8224-CB180 has been programmed to convert the seven bit ASC II alphabet code to the 8 bit EBCDIC Alphabet code. The conversion includes the letters A through Z. With the addition of gating circuitry, the 8224-CB180 will convert both upper case and lower case letters.

Customer specified patterns are also available as custom products. Refer to page 4-43 for Truth Table/Order Blank.

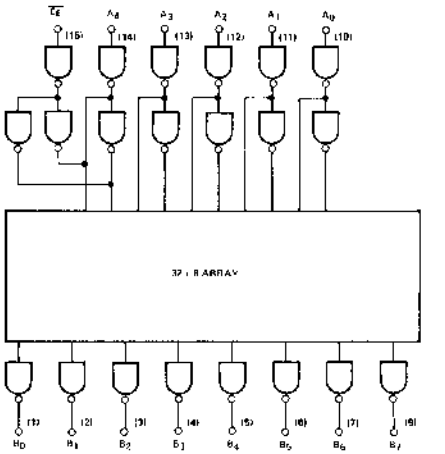
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- CHIP ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATOR
CONTROL STORE

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS ($S8224 - 55°C \leq T_A \leq 125°C$, $N8224\ 0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS			TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	MAX.	UNITS	V_{CC}	A_n "0"	A_n "1"	$\overline{\text{CHIP ENABLE}}$		
"1" Output Leakage Current		100	µA	5.00			2.0V		13
"0" Output Voltage		0.4	V	4.75	0.8V	2.0V	0.8V	9.6mA	6,10
		0.4	V	5.00	0.8V	2.0V	0.8V	9.6mA	6,10
		0.4	V	4.75	0.8V	2.0V	0.8V	9.6mA	6,10
"1" Input Current									
An, Address		40	µA	5.25		4.5V	4.5V		
$\overline{\text{Chip Enable}}$ Input		80	µA	5.25			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1	-1.6	mA	5.25	0.4V		0.4V		

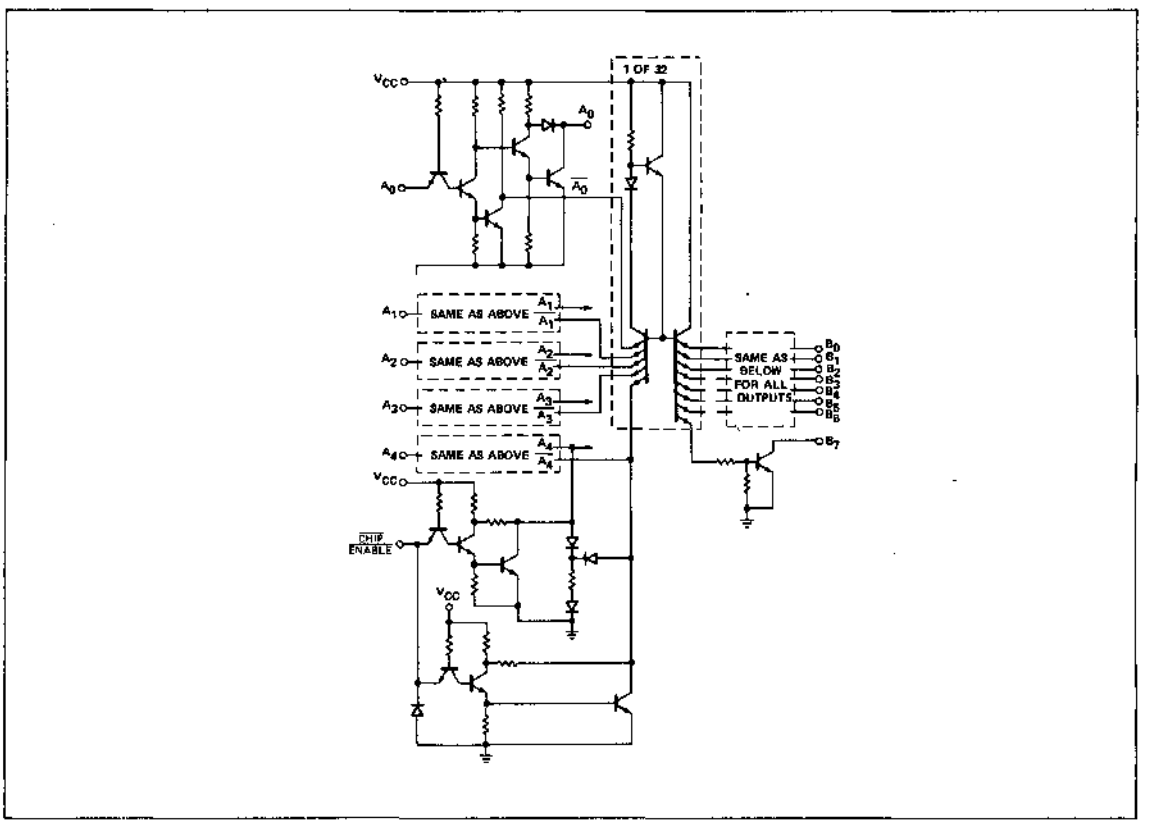
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS			TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	MAX.	UNITS	V_{CC}	A_n "0"	A_n "1"	$\overline{\text{CHIP ENABLE}}$		
Propagation Delay									
An to Bn		50	ns	5.00				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to Bn		50	ns	5.00		4.5V		DC F.O.=12	7,12
Power Consumption		400	mW	5.25		4.5V	4.5V		
Input Latch Voltage	5.5		V	5.00	10mA		10mA		11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.

SCHEMATIC DIAGRAM



CODE CONVERSION ASCII TO EBCDIC (UPPER & LOWER CASE LETTERS ONLY) 8224–CB180

ASC II CODE							CHARACTER	EBCDIC CODE
B_7	B_6	B_5	B_4	B_3	B_2	B_1		0 1 2 3 4 5 6 7
0	0	0	X	X	X	X	–	Not Decoded
0	0	1	X	X	X	X	–	Not Decoded
0	1	0	X	X	X	X	–	Not Decoded
0	1	1	X	X	X	X	–	Not Decoded
1	0	0	0	0	0	0	–	Not Decoded
1	0	0	0	0	0	1	A	1 1 0 0 0 0 0 1
1	0	0	0	0	1	0	B	1 1 0 0 0 0 1 0
1	0	0	0	0	1	1	C	1 1 0 0 0 0 1 1
1	0	0	0	1	0	0	D	1 1 0 0 0 1 0 0
1	0	0	0	1	0	1	E	1 1 0 0 0 1 0 1
1	0	0	0	1	1	0	F	1 1 0 0 0 1 1 0
1	0	0	0	1	1	1	G	1 1 0 0 0 1 1 1
1	0	0	1	0	0	0	H	1 1 0 0 1 0 0 0
1	0	0	1	0	0	1	I	1 1 0 0 1 0 0 1
1	0	0	1	0	1	0	J	1 1 0 1 0 0 0 1
1	0	0	1	0	1	1	K	1 1 0 1 0 0 1 0
1	0	0	1	1	0	0	L	1 1 0 1 0 0 1 1
1	0	0	1	1	0	1	M	1 1 0 1 0 1 0 0
1	0	0	1	1	1	0	N	1 1 0 1 0 1 0 1
1	0	0	1	1	1	1	O	1 1 0 1 0 1 1 0
1	0	1	0	0	0	0	P	1 1 0 1 0 1 1 1
1	0	1	0	0	0	1	Q	1 1 0 1 1 0 0 0
1	0	1	0	0	1	0	R	1 1 0 1 1 0 0 1
1	0	1	0	0	1	1	S	1 1 1 0 0 0 1 0
1	0	1	0	1	0	0	T	1 1 1 0 0 0 1 1
1	0	1	0	1	0	1	U	1 1 1 0 0 1 0 0
1	0	1	0	1	1	0	V	1 1 1 0 0 1 0 1
1	0	1	0	1	1	1	W	1 1 1 0 0 1 1 0
1	0	1	1	0	0	0	X	1 1 1 0 0 1 1 1
1	0	1	1	0	0	1	Y	1 1 1 0 1 0 0 0
1	0	1	1	0	1	0	Z	1 1 1 0 1 0 0 1
1	0	1	1	0	1	1	–	1 Not Decoded
1	0	1	1	1	0	0	–	1 Not Decoded
1	0	1	1	1	0	1	–	1 Not Decoded
1	0	1	1	1	1	0	–	1 Not Decoded
1	0	1	1	1	1	1	–	1 Not Decoded
1	1	0	0	0	0	0	–	1 Not Decoded
1	1	0	0	0	0	1	a	1 0 0 0 0 0 0 1
1	1	0	0	0	1	0	b	1 0 0 0 0 0 1 0
1	1	0	0	0	1	1	c	1 0 0 0 0 0 1 1
1	1	0	0	1	0	0	d	1 0 0 0 0 1 0 0
1	1	0	0	1	0	1	e	1 0 0 0 0 1 0 1
1	1	0	0	1	1	0	f	1 0 0 0 0 1 1 0
1	1	0	0	1	1	1	g	1 0 0 0 0 1 1 1
1	1	0	1	0	0	0	h	1 0 0 0 1 0 0 0
1	1	0	1	0	0	1	i	1 0 0 0 1 0 0 1
1	1	0	1	0	1	0	j	1 0 0 1 0 0 0 1
1	1	0	1	0	1	1	k	1 0 0 1 0 0 1 0
1	1	0	1	1	0	0	l	1 0 0 1 0 0 1 1
1	1	0	1	1	0	1	m	1 0 0 1 0 1 0 0
1	1	0	1	1	1	0	n	1 0 0 1 0 1 0 1
1	1	0	1	1	1	1	o	1 0 0 1 0 1 1 0
1	1	1	0	0	0	0	p	1 0 0 1 0 1 1 1
1	1	1	0	0	0	1	q	1 0 0 1 1 0 0 0
1	1	1	0	0	1	0	r	1 0 0 1 1 0 0 1
1	1	1	0	0	1	1	s	1 0 1 0 0 0 1 0
1	1	1	0	1	0	0	t	1 0 1 0 0 0 1 1
1	1	1	0	1	0	1	u	1 0 1 0 0 1 0 0
1	1	1	0	1	1	0	v	1 0 1 0 0 1 0 1
1	1	1	0	1	1	1	w	1 0 1 0 0 1 1 0
1	1	1	1	0	0	0	x	1 0 1 0 0 1 1 1
1	1	1	1	0	0	1	y	1 0 1 0 1 0 0 0
1	1	1	1	0	1	0	z	1 0 1 0 1 0 0 1
1	1	1	1	0	1	1	–	Not Decoded
1	1	1	1	1	0	0	–	Not Decoded
1	1	1	1	1	0	1	–	Not Decoded
1	1	1	1	1	1	0	–	Not Decoded
1	1	1	1	1	1	1	–	Not Decoded

TRUTH TABLES FOR 8224–CB180

INPUT PINS						OUTPUT PINS							
15	14	13	12	11	10	9	7	6	5	4	3	2	1
$\overline{CE}$	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	0	1	0	0	0	1	1
0	0	0	1	1	0	0	1	1	0	0	0	1	1
0	0	0	1	1	1	1	1	1	0	0	0	1	1
0	0	1	0	0	0	0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1	0	0	1	1
0	0	1	0	1	0	1	0	0	0	1	0	1	1
0	0	1	0	1	1	0	1	0	0	1	0	1	1
0	0	1	1	0	0	1	1	0	0	1	0	1	1
0	0	1	1	0	1	0	0	1	0	1	0	1	1
0	0	1	1	1	0	1	0	1	0	1	0	1	1
0	0	1	1	1	1	0	1	1	0	1	0	1	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	1	0	0	0	1	1	0	1	1
0	1	0	0	1	0	1	0	0	1	1	0	1	1
0	1	0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	1	0	0	1	1	0	0	0	1	1	1
0	1	0	1	0	1	0	0	0	1	0	1	1	1
0	1	0	1	1	0	1	0	0	1	0	1	1	1
0	1	0	1	1	1	0	1	1	0	0	1	1	1
0	1	1	0	0	0	1	1	1	0	0	1	1	1
0	1	1	0	0	1	0	0	0	1	0	1	1	1
0	1	1	0	1	0	1	0	0	1	0	1	1	1
0	1	1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	1	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0	0	0	0
1	x	x	x	x	x	1	1	1	1	1	1	1	1

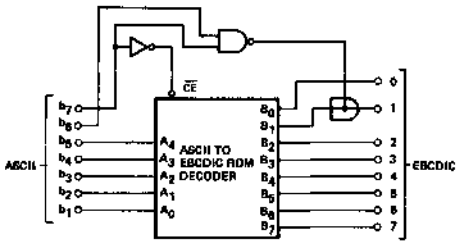
TYPICAL APPLICATIONS

To select the ROM only when addressed by an upper or lower case alphabet character, the following truth table applies:

	Upper Case		Lower Case	
ASCII	0	0	1	1
ASCII	0	1	0	1
CHIP ENABLE = B_7	1	1	0	0
EBCDIC #1 OUTPUT = $\overline{B_6 \cdot B_7}$	1	1	1	0

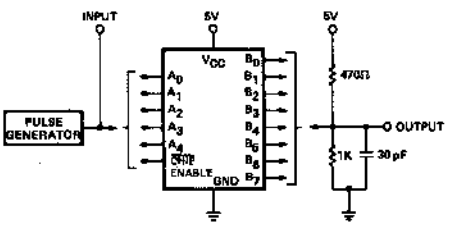
Thus, the ASCII to EBCDIC ROM standard product plus gating as shown performs the complete conversion.

TYPICAL APPLICATIONS (Cont'd)

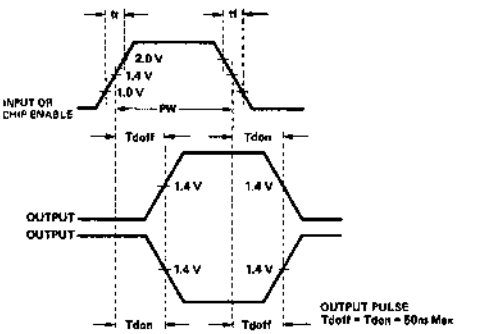


GROUND PIN 15 WHEN TESTING ADDRESS-OUTPUT DELAYS

AC TEST FIGURE AND WAVEFORMS



INPUT PULSE:
Amplitude = 3.0V
tr = tf = 5ns
PW = 200ns (50% DUTY CYCLE)



signetics

64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM)

8225

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8225 is a TTL 64-bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 8225 is ideally suited for application in scratch pads and high-speed buffer memories.

Words are selected through a 4-input binary decoder when the chip enable input ($\overline{CE}$) is at logic "0". Data is written into the memory when Read Enable (RE) is at logic "0" and read from the memory when RE is at logic "1".

The outputs of the 8225 are logical "1" during write operation, therefore, inputs and outputs can be commoned in busses to reduce the number of I/O leads. Output collectors are uncommitted.

FEATURES

- CHIP ENABLE LINE FOR EXPANSION
- OPEN COLLECTOR OUTPUTS FOR EXPANSION
- ON THE CHIP DECODING
- ALL OUTPUTS "1" DURING WRITING
- DIODE PROTECTED INPUTS

APPLICATIONS

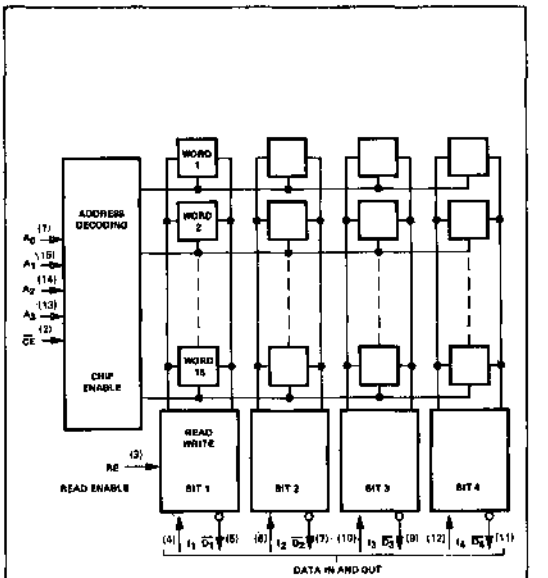
SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS (First in-first out)
CONTROL STORE

TRUTH TABLE

RE	$\overline{CE}$ (Chip Enable)	MODE	OUTPUTS
0	0	Write	"1"
1	0	Read	Information
X	1	Chip Disable	"1"

X = Either State

BLOCK DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL IN OR DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

Chip is enabled when $\overline{CE}$ = "0"

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A\ 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

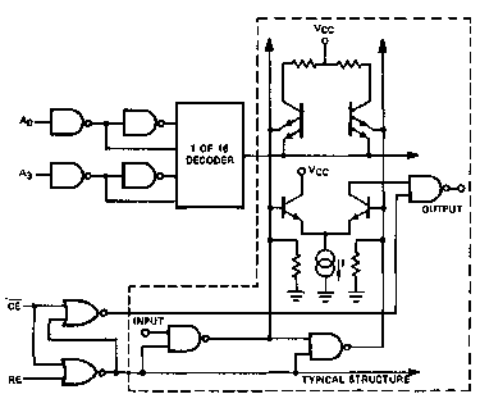
CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
"0" Output Voltage			.4	V	.8V	Pulse			16mA	8, 11, 12
"1" Output Leakage Current			100	μA	.8V	Pulse		.8V	5.25V	11, 12
"0" Input Current	-.1		-1.6	mA	.4V	.4V	.4V	.4V		16
"1" Input Current										
Chip Enable			80	μA	4.5V					
Write, Address, Data			40	μA	4.5V	4.5V	4.5V	4.5V		16

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
Minimum Write Pulse Width (W_{PW})		18	30	ns						
Input Setup Time (I_{SU})		18	20	ns						
Input Hold Time (I_{HO})		0	5	ns						
Address Setup Time (A_{SU})			5	ns						
Address Hold Time (A_{HO})			5	ns						
Access Time (T_A)	20	35	50	ns						17
Data Pulse Width (D_{PW})	20			ns						
Write Recovery Time (T_{WR})	10	25	40	ns						
Write Access Time (T_{WA})		25	40	ns						
Chip Enable Recovery Time (T_{CR})		20	30	ns						
Chip Enable Access Time (T_{CA})		20	30	ns						
Input Clamp Voltage			-1.5	V	-12mA	-12mA	-12mA	-12mA		16
Input Latch Voltage – except Data			5.5	V	10mA	10mA	10mA			16
Data			5.5	V	5V	5V		10mA		16
Power Consumption		400	552	mW	0V	5V	0V	0V		14

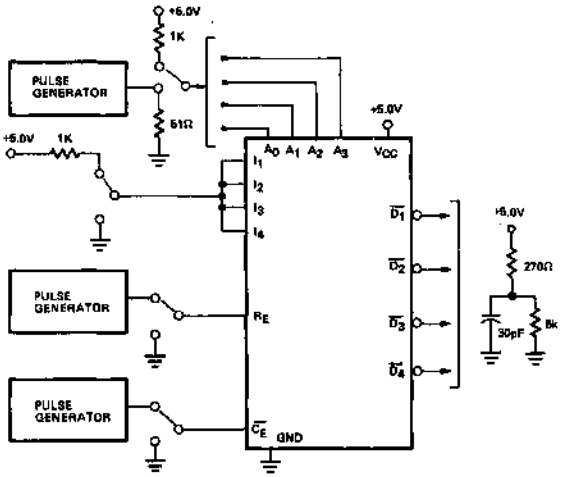
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Capacitance is measured on Boonton Electronic Corporation Model 75A-53 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25m V_{rms}.
7. All pins not specifically referenced are tied to ground for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{CC}.
9. One DC fan-out is defined as 0.8mA.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
12. For any given binary code on the Address inputs the Write input must be momentarily brought to a logical "0" level.
13. See AC test circuits on following pages.
14. All sense outputs in "0" state.
15. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
16. Test each input one at a time.
17. Address Pulse Width (A_{PW}) is 40ns for this test.

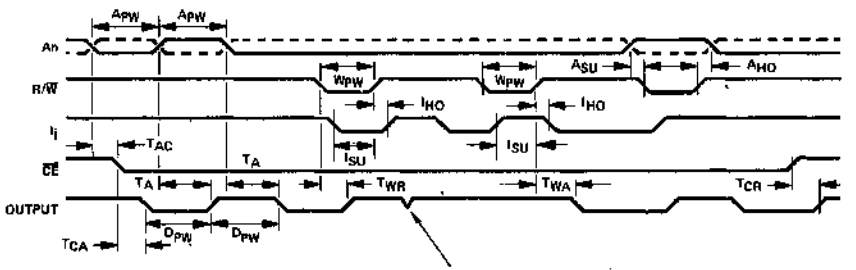
FUNCTIONAL DIAGRAM



ONE LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

AC TEST FIGURES AND WAVEFORMS





NOTE: NEGATIVE TRANSITION DOES NOT GO BELOW 2.6 VOLTS AND GENERALLY IS NOT MEASURABLE.

DESCRIPTION

The 8228 is a 4096 Bit Bipolar Read Only Memory organized as 1024 words by 4 bits per word. Available in a 16 pin dual in-line package, the 8228 can provide very high bit packing density by replacing four standard 256X4 ROMS.

The 8228 is fully TTL compatible and includes on-the-chip decoding. Typical access time is 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N8228I - CD162, while custom circuits are identified as N8228I - CXXX. A truth table/order blank is included on page 4-46 for ordering custom patterns.

See page 4-35 for CD162 Pattern and USASCII Row Character Generator.

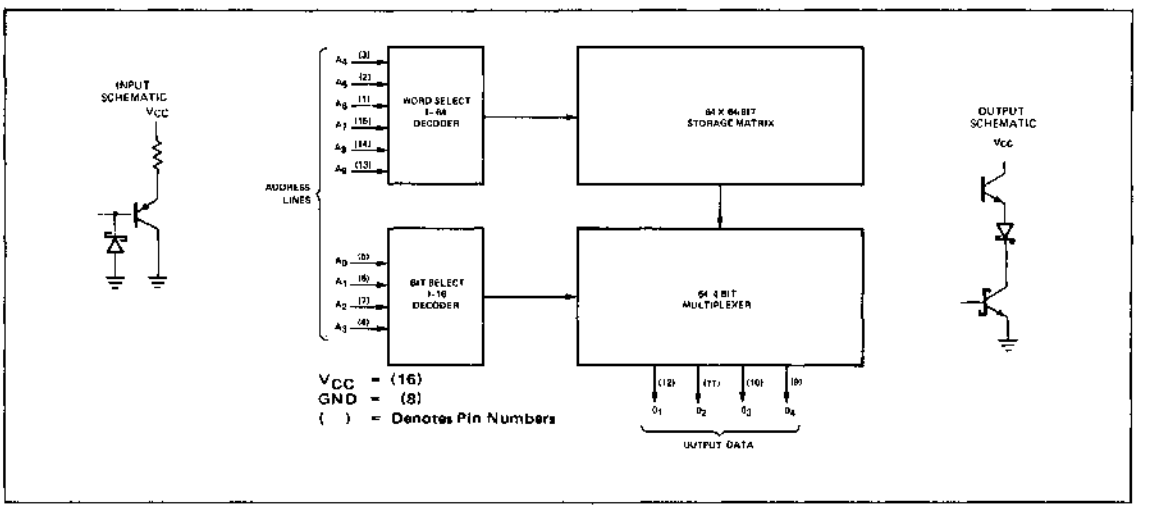
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TOTEM POLE OUTPUTS
- DIODE PROTECTED INPUTS
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)

APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATION
CONTROL STORE

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			0.5	V	I_{out} = 11.2 mA	
"1" Output Voltage	2.7			V	I_{out} = -1.0 mA	
"0" Input Current		-10	-200	μA	V_{in} = 0.5V	
"1" Input Current		1	25	μA	V_{in} = 5.25V	
Input Threshold Voltage						
"0" Level			.85	V		
"1" Level	2.0			V		

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Input Clamp Voltage	-1.0			V	I_{in} = 5.0mA	
Power Consumption		140	170	mA	O_1 to O_3 = "0"	
Output Short Circuit Current	-20		-70	mA		

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V)

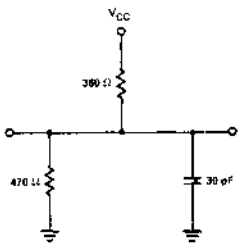
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Access Time—Address to Output		50	75	ns		5

NOTES:

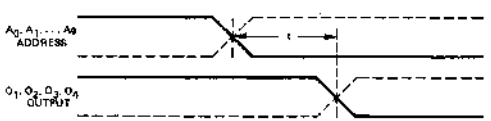
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 5.5V
   Input currents must not exceed ±30mA
   Output currents must not exceed ±100mA
   Storage temperature must be between -60°C to +150°C
5. Rise and fall time for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

AC TEST FIGURE AND WAVEFORM

TEST LOAD



READ CYCLE



DESCRIPTION

The 82S06 and 82S07 are ideal devices for use in Control Stores, small buffers, scratch pads, "cache" type buffer stores, memory maps, etc. The typical read time (the time between applying an address and obtaining valid output data) is 45ns. The typical write time (the time between applying one address and storing data) is 20ns. The circuit has 3 chip enable inputs which greatly simplifies the circuit configuration when used in large memories. The 82S06 and 82S07 also feature very low input loadings, 25 microamperes for a "1" state and -100 microamperes for "0".

The memories are TTL compatible and operate from single 5 volt supply.

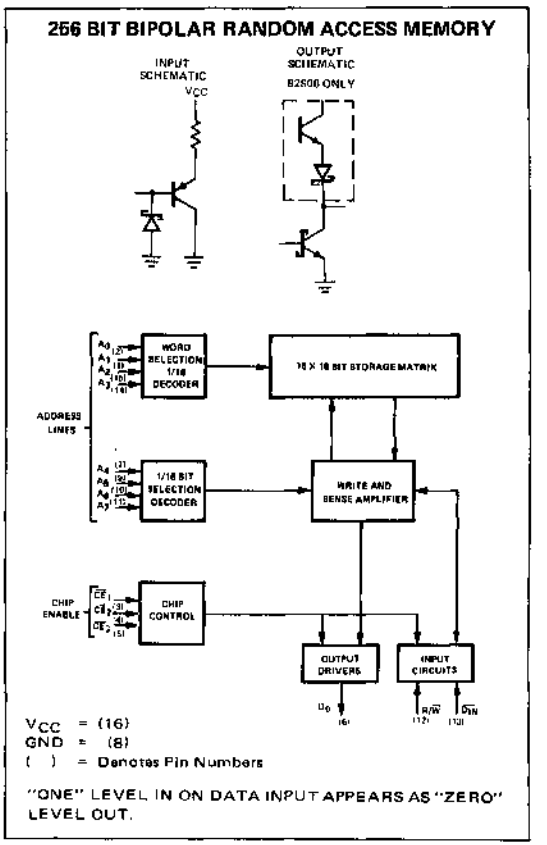
APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK

FEATURES

- **256 X 1 ORGANIZATION**
- **30 NANOSECOND ACCESS TIME TYPICAL**
- **LOW 1.5 mw/BIT POWER DISSIPATION TYPICAL**
- **LOW 100 µA INPUT LOADING**
- **TRI-STATE (82S06) OR OPEN COLLECTOR (82S07) OUTPUT**
- **ON CHIP DECODING**

BLOCK DIAGRAM



PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = 0 to 75°C, V_{CC} = 5.0V ±5) Note 1, 2, 3

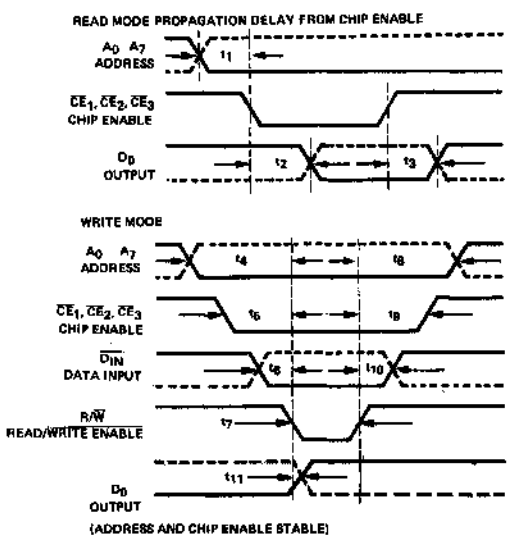
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Input Current		-10	-100	µA	V_{in} = 0.5V	
"1" Input Current		<1.0	25	µA	V_{in} = 5.25V	
"0" Output Voltage		.35	.5	V	I_{out} = 16mA	
Output Leakage Current (82S07)		<1.0	100	µA	$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ = "1", V_{out} = 2.7V	
Output "off" Current (82S06)		<1.0	±100	µA	$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ = "1", 0.5 ≤ V_{out} ≤ 2.7V	
"1" Output Voltage (82S06)	2.6			V	$\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3$ = "0" I_{out} = -3.2mA	
"0" Input Threshold			.85	V		
"1" Input Threshold	2.0			V		
Power Consumption		110/550	130/683	mA/mW		
Input Clamp Voltage	-1.5	-.8		V	I_{in} = -12mA	
Input Capacitance		5		pF		
Output Capacitance		8		pF		

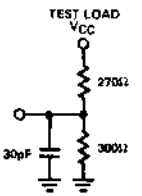
OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

CHARACTERISTICS		LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTES
Access Time—Address to Output			45	65	ns		4,5
Address Set-Up Time (read)	t_1		10		ns		
Propagation Delay							4,5
Chip Enable to Output Enable	t_2		25	40	ns		
Propagation Delay							4,5
Chip Enable to Output Disable	t_3		25	40	ns		
Address to Write Enable							4,5
Set-Up Time	t_4	25	5		ns		
Chip Enable to Write Enable							4,5
Set-Up Time	t_5	10	0		ns		
Data Input to Write Enable							4,5
Set-Up Time	t_6	10	0		ns		
Write Enable Pulse Width	t_7	30	15		ns		4,5
Address Hold Time	t_8	10	0		ns		4,5
Chip Enable Hold Time	t_9	10	0		ns		4,5
Data Input Hold Time	t_{10}	10	0		ns		4,5
Write Enable Propagation Delay	t_{11}		30	40	ns		4,5
Output Short Circuit Current (82S06)		−20		−100	mA	V_{out} = 0V	4,5

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltages must not exceed 6.0V, Input currents must not exceed ±30mA, Output currents must not exceed ±100mA, Storage temperature must be between -60°C to +150°C.
4. Refer to Timing Diagram for definition of terms and test load.
5. Rise and fall times for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5 volts.

TIMING DIAGRAM





t_1 = set up time for an address input to chip enable for valid data at output
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output

DESCRIPTION

The 82S16 and 82S17 are ideal devices for use in Control Stores, small buffers, scratch pads, "cache" type buffer stores, memory maps, etc. The typical read time (the time between applying an address and obtaining valid output data) is 30ns. The typical write time (the time between applying one address and storing data) is 20ns. The circuit has 3 chip enable inputs which greatly simplifies the circuit configuration when used in large memories. The 82S16 and 82S17 also feature very low input loadings, 25 microamperes for a "1" state and -100 microamperes for "0".

The memories are TTL compatible and operate from single 5 volt supply.

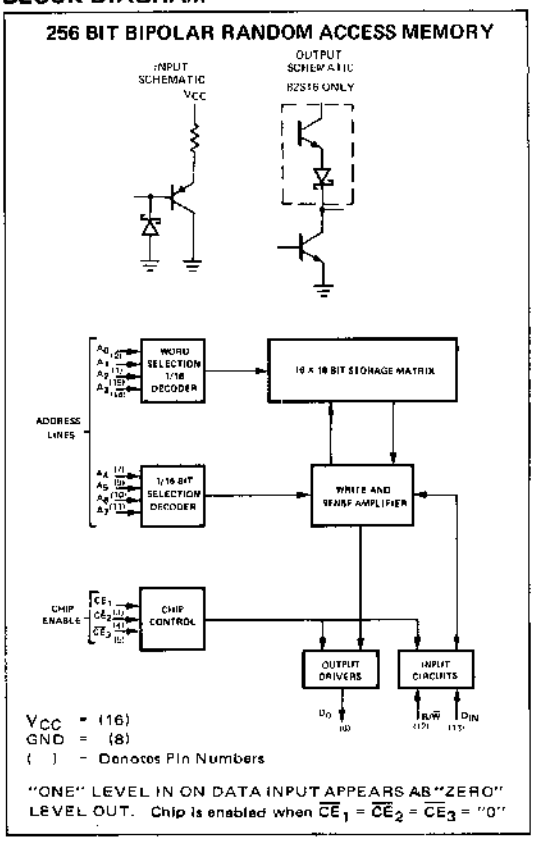
APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK

FEATURES

- **256 X 1 ORGANIZATION**
- **30 NANOSECOND ACCESS TIME TYPICAL**
- **LOW 1.5 mw/BIT POWER DISSIPATION TYPICAL**
- **LOW 100 µA INPUT LOADING**
- **TRI-STATE (82S16) OR OPEN COLLECTOR (82S17) OUTPUT**
- **ON CHIP DECODING**

BLOCK DIAGRAM



OBJECTIVE ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$) Note 1, 2, 3

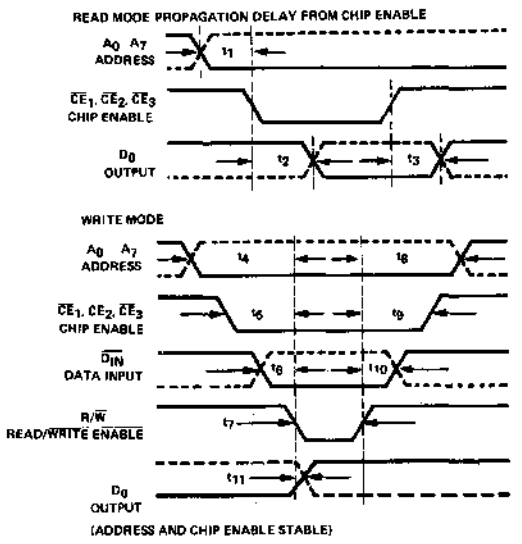
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Input Current		-10	-100	µA	V_{in} = 0.5V	
"1" Input Current		<1.0	25	µA	V_{in} = 5.25V	
"0" Output Voltage		.35	.45	V	I_{out} = 16mA	
Output Leakage Current (82S17)		<1.0	40	µA	$\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ = "1", V_{out} = 2.7V	
Output "off" Current (82S16)		<1.0	40	µA	$\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ = "1", $0.5 \leq V_{out} \leq 2.7V$	
"1" Output Voltage (82S16)	2.6			V	$\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3$ = "0" I_{out} = -3.2mA	
"0" Input Threshold			.85	V		
"1" Input Threshold	2.0			V		
Power Consumption		110/550	130/683	mA/mW		
Input Clamp Voltage	-1.5	-.8		V	I_{in} = -12mA	
Input Capacitance		5		pF		
Output Capacitance		8		pF		

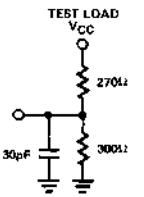
OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

CHARACTERISTICS		LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTES
Access Time—Address to Output			30	50	ns		4,5
Address Set-Up Time (read)	t_1		10	20	ns		4,5
Propagation Delay Chip Enable to Output Enable	t_2		20	30	ns		4,5
Propagation Delay Chip Enable to Output Disable	t_3		20	30	ns		4,5
Address to Write Enable Set-Up Time	t_4	20	5		ns		4,5
Chip Enable to Write Enable Set-Up Time	t_5	5	0		ns		4,5
Data Input to Write Enable Set-Up Time	t_6	5	0		ns		4,5
Write Enable Pulse Width	t_7	25	15		ns		4,5
Address Hold Time	t_8	5	0		ns		4,5
Chip Enable Hold Time	t_9	5	0		ns		4,5
Data Input Hold Time	t_{10}	5	0		ns		4,5
Write Enable Propagation Delay	t_{11}		30	40	ns		4,5
Output Short Circuit Current (82S16)		−20		-70	mA	V_{out} = 0V	4,5

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltages must not exceed 6.0V, Input currents must not exceed ±30mA, Output currents must not exceed ±100mA, Storage temperature must be between -60°C to +150°C.
4. Refer to Timing Diagram for definition of terms and test load.
5. Rise and fall times for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5 volts.

TIMING DIAGRAM





t_1 = set up time for an address input to chip enable for valid data at output
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output

signetics

64-BIT BIPOLAR HIGH SPEED WRITE-WHILE-READ RAM (32x2 RAM)

82S21

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

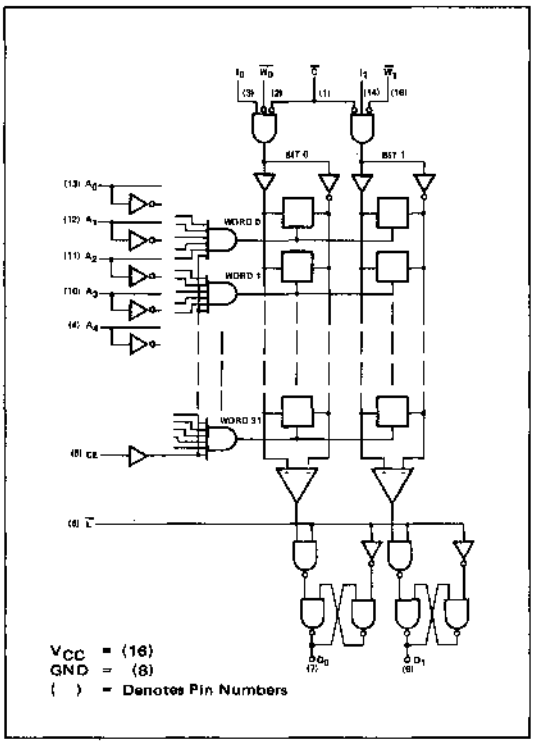
FEATURES

- BUFFERED ADDRESS LINES
- ON CHIP LATCHES
- ON CHIP DECODING
- BIT MASKING CONTROL LINES
- ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS WITH 40mA CAPABILITY
- PROTECTED INPUTS
- VERY HIGH SPEEDS (25ns TYP)

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

LOGIC DIAGRAM



TRUTH TABLE

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			.45	V	V_{out} = 40mA	
"1" Output Leakage Current			40	μA	V_{out} = 5.5V	
"0" Input Current (All Inputs)			−1.6	mA	V_{in} = 0.5V	
"1" Input Current (All Inputs			25	μA	V_{in} = 2.4V	
			100	μA	V_{in} = 5.5V	
Input "0" Threshold Voltage			0.85	V		
Input "1" Threshold Voltage	2.0			V		
Power Consumption			130/683	mA/mW		

ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5.0V)

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Read Access Time Address to Output	t_1		25	50	ns		
Address Set-Up Time	t_2		8	15	ns		
Data Set-Up Time	t_3		15	20	ns		
Address to Address Hold Time	t_4		0	0	ns		
Control or Write Pulse Width	t_5	20	15		ns		
Write Access Time	t_6		20	25	ns		
Address to Latch Set-Up Time	t_7		25	50	ns		
Latch Address to Address Hold Time	t_8		7	10	ns		
Delatch Access Time	t_9		15	25	ns		
Data Hold Time Earliest	t_{10}		0	5	ns		

NOTES:

1. Positive current is defined as into the Terminal.
2. No more than one output should be grounded at the same time.
3. Applied voltages must not exceed 5.5V.
   Input current must not exceed ±12 mA.
   Output current must not exceed ±100 mA.
   Storage temperature must be within the −60°C to +150°C range.
4. Manufacturer reserves the right to make design and process changes and improvements.

AC WAVEFORMS

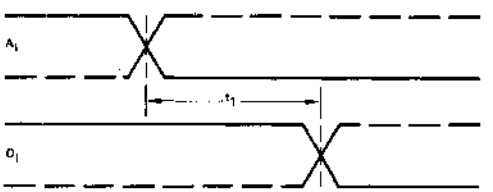


Fig. 1 Read Access Time

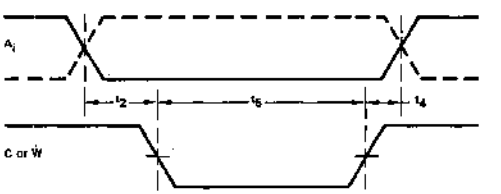


Fig. 2 Address Setup and Hold Time

AC WAVEFORMS

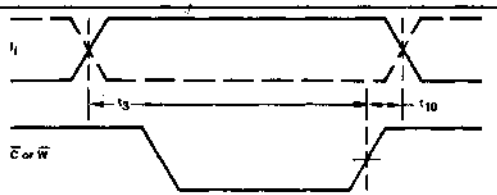


Fig. 3 Data Setup and Hold Time

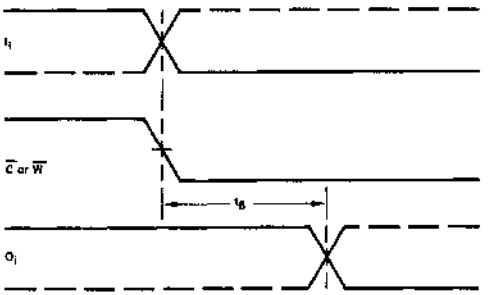


Fig. 4 Write Access Time

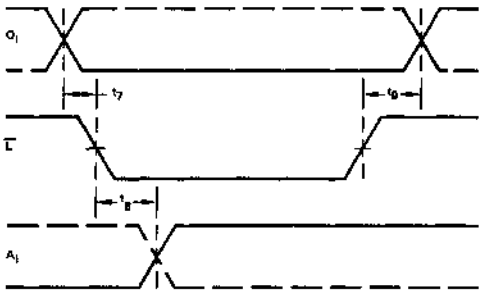
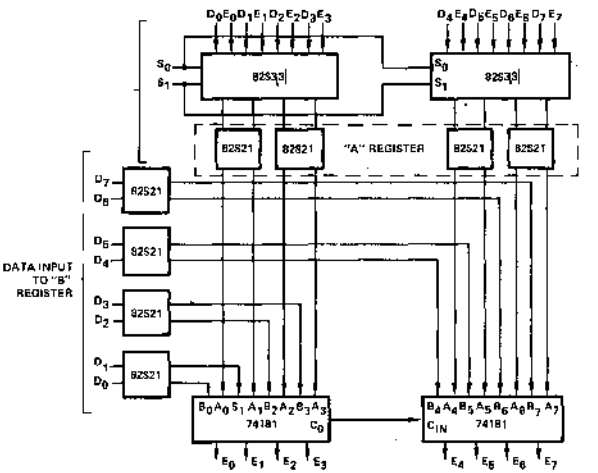


Fig. 5 Latch Times

TYPICAL APPLICATION



BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 x 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B — A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

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256-BIT BIPOLAR PROGRAMMABLE ROM (32×8 PROM)
(82S23 OPEN COLLECTOR)(82S123 TRI-STATE)

82S23
82S123

OBJECTIVE SPECIFICATION

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S23 (open Collector Outputs) and the 82S123 (Tristate Outputs) are Bipolar 256 Bit Read Only Memories organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. A chip enable line is provided and the outputs are bare collector or Tristate to allow for memory expansion capability.

The 82S23 and 82S123 are fully TTL compatible and include on-the-chip decoding. Typical access time is 25 nS.

The standard 82S23 and 82S123 are supplied with all outputs at a logical "0." If a programmed unit is required the Truth Table/Order Blank on page 4-43 of the TTL MSI/Memory Handbook may be used.

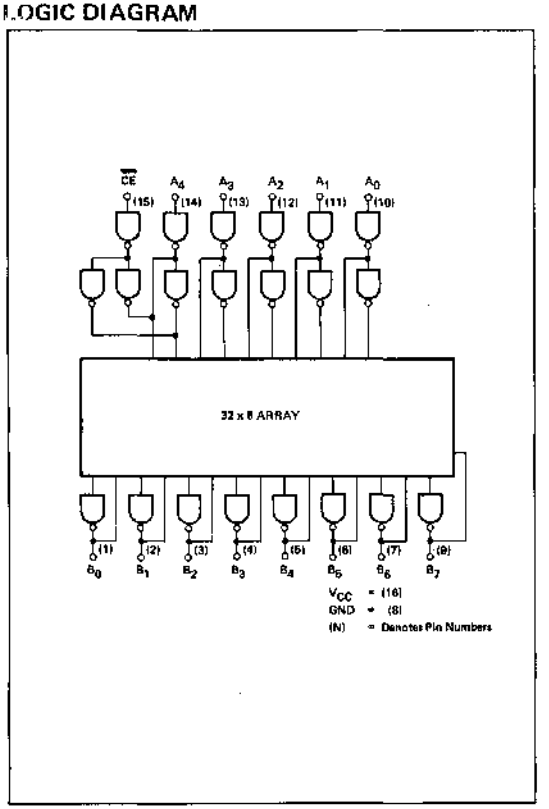
FEATURES

- PNP INPUTS
- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- A CHIP ENABLE LINE
- OPEN COLLECTOR OR TRISTATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- BOARD PROGRAMMABLE

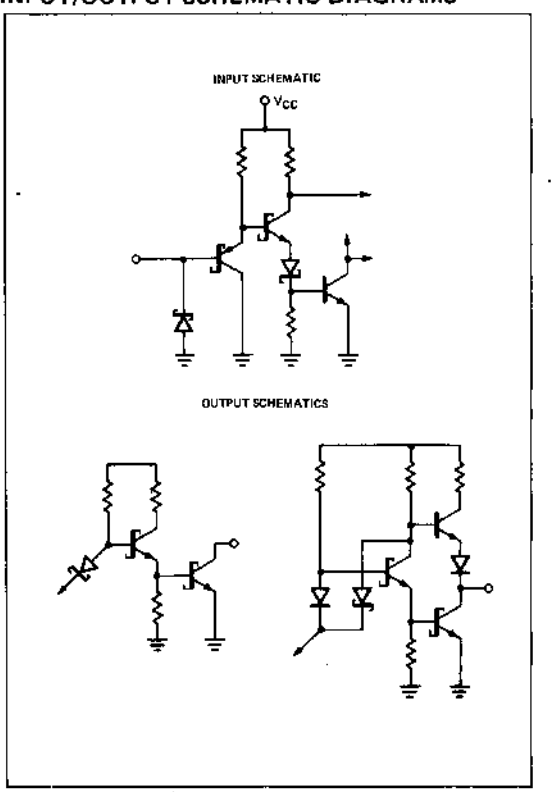
APPLICATIONS

- PROTOTYPING
- VOLUME PRODUCTION
- MICROPROGRAMMING
- HARDWIRED ALGORITHMS
- CONTROL STORE

LOGIC DIAGRAM



INPUT/OUTPUT SCHEMATIC DIAGRAMS



OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage				V	I_{out} = 20mA	
"1" Output Leakage			40	μA	CE = "1" V_{out} = 2.6V	
82S23			100	μA	CE = "0" V_{out}=2.6V After Fusing	
82S123	-40		+40	μA	V_{out} = 0.5V/V_{out} = 2.4V, CE = "1"	
"1" Output Current 82S123	- 2.0			mA	V_{out} = 2.4V, CE = "0"	After Fusing
"0" Input Current			250	μA	V_{in} = 0.5V	
"1" Input Current			50	μA	V_{in} = 2.7V	
Input Threshold Voltage						
"0" Level	.80			V		
"1" Level			2.0	V		
Propagation Delay						
Address to Output		25	40	ns		
Enable to Output		15	35	ns		
Input Clamp Voltage	-1.0			V	I_{in} = 5.0mA	
Power Consumption					V_{cc} = 5.00V	
82S23		80/400	100/500	mA/mW		
82S123		80/400	100/500	mA/mW		

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1" "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8 mA.
8. One AC fan-out is defined as 50 pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed conditions, see AC testing.
13. Connect an external 1K resistor from V_{CC} to the output terminal for this test.
14. V_{CC} = 5.25V.

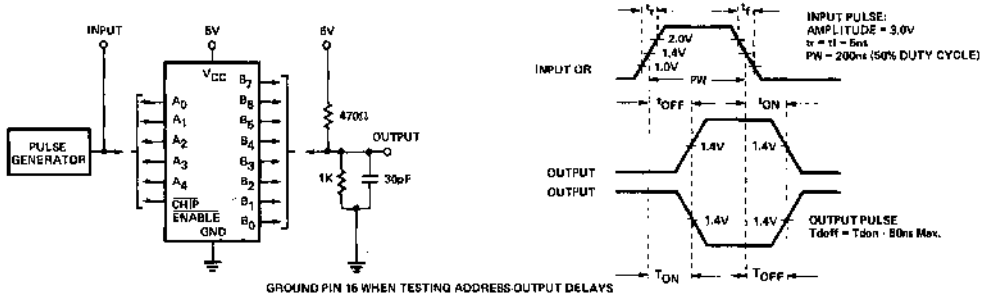
OBJECTIVE FUSING PROCEDURE

The 82S23/82S123 standard part is shipped with all outputs at Logical "0". To write a Logical "1" proceed as follows:
1. GND Pin 8 and apply 5V to V_{CC}, Pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground for a "0" and 5.0 ±0.25V for a "1" at the address input lines.
5. Raise V_{CC} to 10.0V ±0.5V.
6. Apply 65 ±3 mA to the output to be programmed to logic "1". (The voltage will be between 12 to 18V until fused, and must be clamped at 20.0V max.)
7. Release fusing current.
8. Reduce V_{CC} to 5.0V.
9. Proceed to the next output and repeat, or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 82S23/82S123.

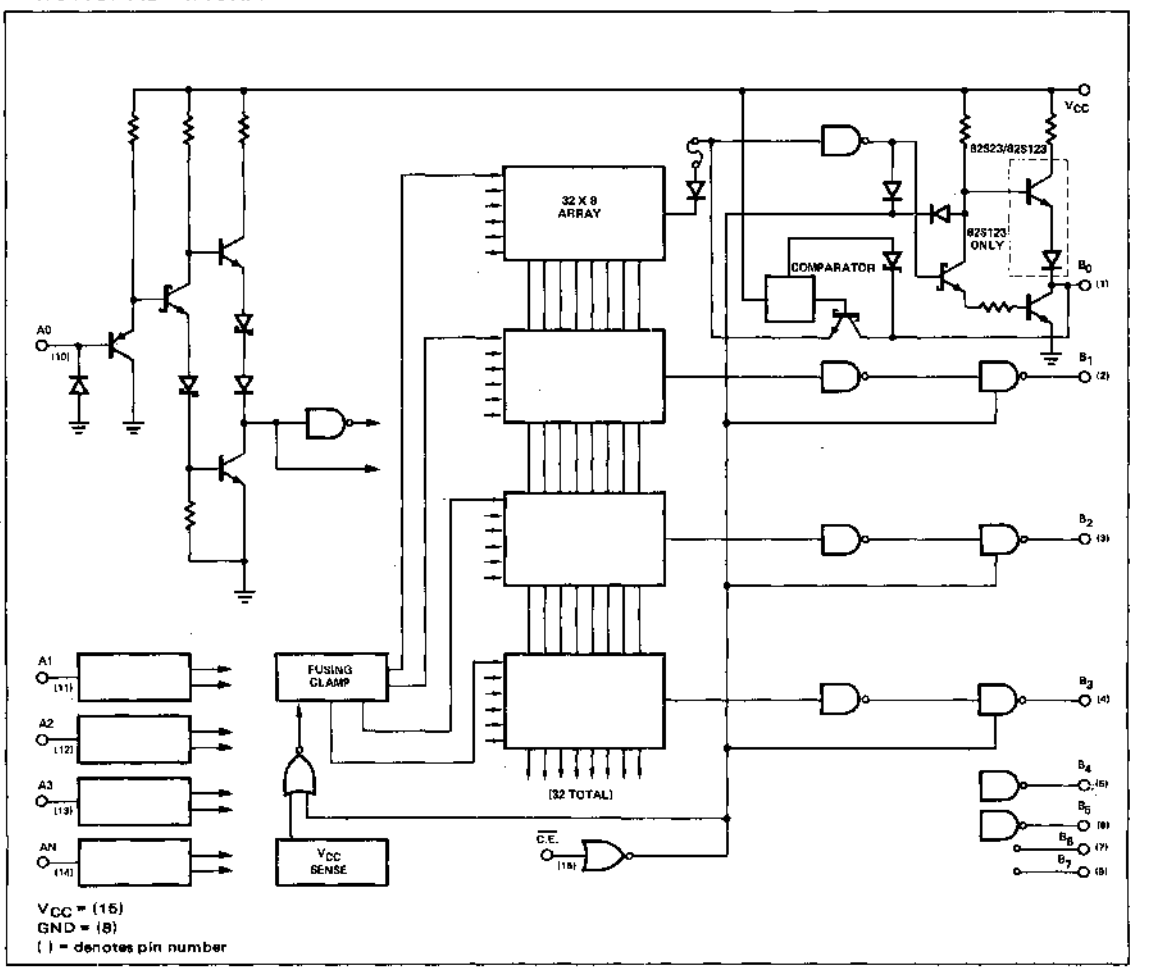
NOTE:

After 1.0 SEC of programming, a 25% duty cycle on power must be imposed to avoid over heating.

AC TEST FIGURE AND WAVEFORMS



FUNCTIONAL DIAGRAM



signetics

1024 BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

82S26
82S29

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S26 (open Collector Outputs) and the 82S29 (tri State Outputs) are Bipolar 1024 Bit Read Only Memories organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. Two chip enable lines are provided and the outputs are bussable to allow for memory expansion capability.

The 82S26 and 82S29 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35ns.

The standard 82S26 and 82S29 are supplied with all outputs at a logical "0". If a programmed unit is required the Truth Table/Order Blank on page 4-44/45 can be used.

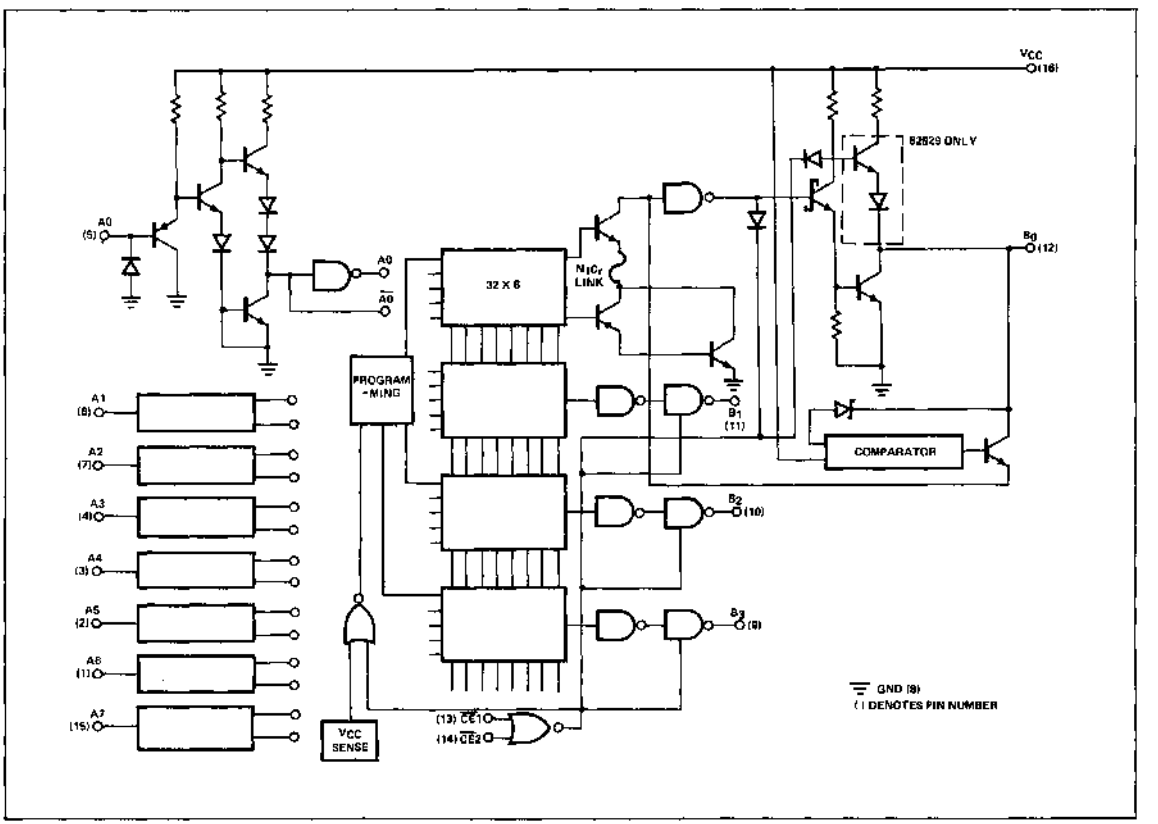
APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CONTROL STORE

FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TWO CHIP ENABLE LINES
- OPEN COLLECTOR OR TRI STATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- BOARD LEVEL PROGRAMMABLE

LOGIC DIAGRAM



PROGRAMMING PROCEDURE

82S26 AND 82S29 PROGRAMMING PROCEDURE

1. Connect pin 8 (Grnd) to ground.
2. Disable the device by bringing $\overline{CE}_1$ and/or $\overline{CE}_2$ to a logical "1" (greater than 2.6 volts). A Signetics SP380A or equivalent may be used. If only one $\overline{CE}$ pin is used for the control of programming the other $\overline{CE}$ pin should be at logical "0" (0.4 volts or less).
3. Raise V_{CC} (pin 16) to 12.5 ± 0.5 volts. A 10μF in parallel with a 200pF high frequency capacitor should be connected between pins 16 and 8, as near the device as possible, to minimize noise on the V_{CC} line.
4. Address the word to be programmed, using standard TTL logic levels, and apply 85 ± 5mA into the output to be programmed to a logical "1". The output must be limited to 22 volts ±5% and only one output at a time should be programmed.
5. Wait until the current generator has reached the 22 volt clamp. (The current generator will be supplying about 50mA min.) Then drop both $\overline{CE}_1$ and $\overline{CE}_2$ to a logical "0" for 2msec. (If one $\overline{CE}$ was already at logical "0" it remains at logical "0".)

   This programming pulse can be longer but a duty cycle of 20% at high V_{CC} must be imposed after 1 second of programming.
6. Return $\overline{CE}_1$ and/or $\overline{CE}_2$ to a logical "1" and wait 10 microseconds (or longer).
7. Repeat steps 5, 6, and 7 until the entire word has been programmed.

   At this point the V_{CC} can be dropped to 5.0 volts and the chip enabled so that the outputs can be tested to verify that all bits programmed; or programming can be continued until the entire device has been programmed.

TO PROGRAM THE ENTIRE DEVICE PRIOR TO VERIFICATION, PROCEED AS FOLLOWS:

8. Address the next word to be programmed and repeat steps 4, 5, 6, and 7 until the entire chip has been programmed. Drop V_{CC} to 0 volts.
9. If less than ½ second has elapsed during this, then apply 5.0 volts V_{CC}, enable the device and check each output to insure all bits have programmed. If more than ½ second has elapsed wait for 4 seconds before the verifying cycle.
   NOTE: Do not apply the high V_{CC} (12.5 volts) for greater than 1.0 seconds continuously. At that point use a 20% duty cycle.

TO VERIFY THE BITS ARE PROGRAMMED AFTER EACH WORD, PROCEED AS FOLLOWS:

10. Disconnect the current generator from the output and connect 5.0 volts to V_{CC} and a 390 ohm pull-up resistor from each output to the 5.0 volts supply. Connect $\overline{CE}_1$ and $\overline{CE}_2$ to logical "0". Verify that all bits have programmed using a comparitor such as the N8242A.
    NOTE: Do not apply the high V_{CC} (12.5 volts) for greater than 1.0 seconds continuously. At that point use a 20% duty cycle.

OPERATION OF THE 82S26/82S29 PROGRAMMER

INTRODUCTION

Figure 1 shows the complete programmer schematic. The memory to be programmed is inserted, and by means of seven single-pole, double-throw (SPDT) switches, the binary address is selected. Notice that these switches may easily be replaced by thumbwheel switches. The memory outputs are programmed, one at a time, by means of four double-pole, double-throw (DPDT) switches. This arrangement has the advantage that the switches are normally in the verify mode, indicating the state of the output (logic "0" when not programmed). By switching to the programming position, the outputs may be altered to a logic "1" which will turn on the light emmiting diode (LED) indicator. Upon return to the verify position the LED indicator will stay lit for a programmed bit position.

Once the switch is in the programming position, it may remain there as long as the operator wishes. The total programming cycle is set up to last only for 5ms and is controlled by one-shots as shown in the timing diagram, Fig. 2. The programmer timing follows the recommendation of the Signetics revised programming procedure and is easily adaptible to automatic programming and duplicating equipment.

CIRCUIT DESCRIPTION

Activating one of the four programming switches triggers one-shot No. 1 for 5 milliseconds. This activates gate No. 1 of the peripheral driver (75451) and, by releasing zener diode No. 1, V_{CC} is raised to 12.5V for 5 milliseconds while the 82S26 or 82S29 chip is disabled. (It should be mentioned that use of the 74121 eliminates contact bounce problems since it is non-retriggerable.)

After a time delay of 1 millisecond generated by one-shot No. 2, one-shot No. 3 is turned on. This turns off the output transistor of gate No. 2 of the 75451, enabling the programming current source. The constant current generator consists of LM309 No. 3 that is clamped to 22V by zener diode No. 2. The programming current is determined by the 59 ohm resistor and maintained at a constant 85mA.

An additional time delay of 1 millisecond, established by one-shot No. 4, guarantees that even slow current sources have reached the required current before the chip is enabled for 2ms to open the NiCr link. One-shot No. 5 establishes the chip enable ($\overline{CE}$) signal and thus the programming time.

Figure 2 shows that V_{CC} for the memory is held at 12.5V for an additional 1 millisecond before the output of one-shot No. 1 allows the supply to return to 5V.

The two time delays of 1 millisecond generated by one-shots No. 2 and No. 4 can be shortened to the microsecond range for automatic programming equipment if fast switching and a fast current source, as the one discussed above, are chosen. Should it be desired to make the programmer self-contained, a power supply suggestion is also shown in Figure 2.

PROGRAMMER

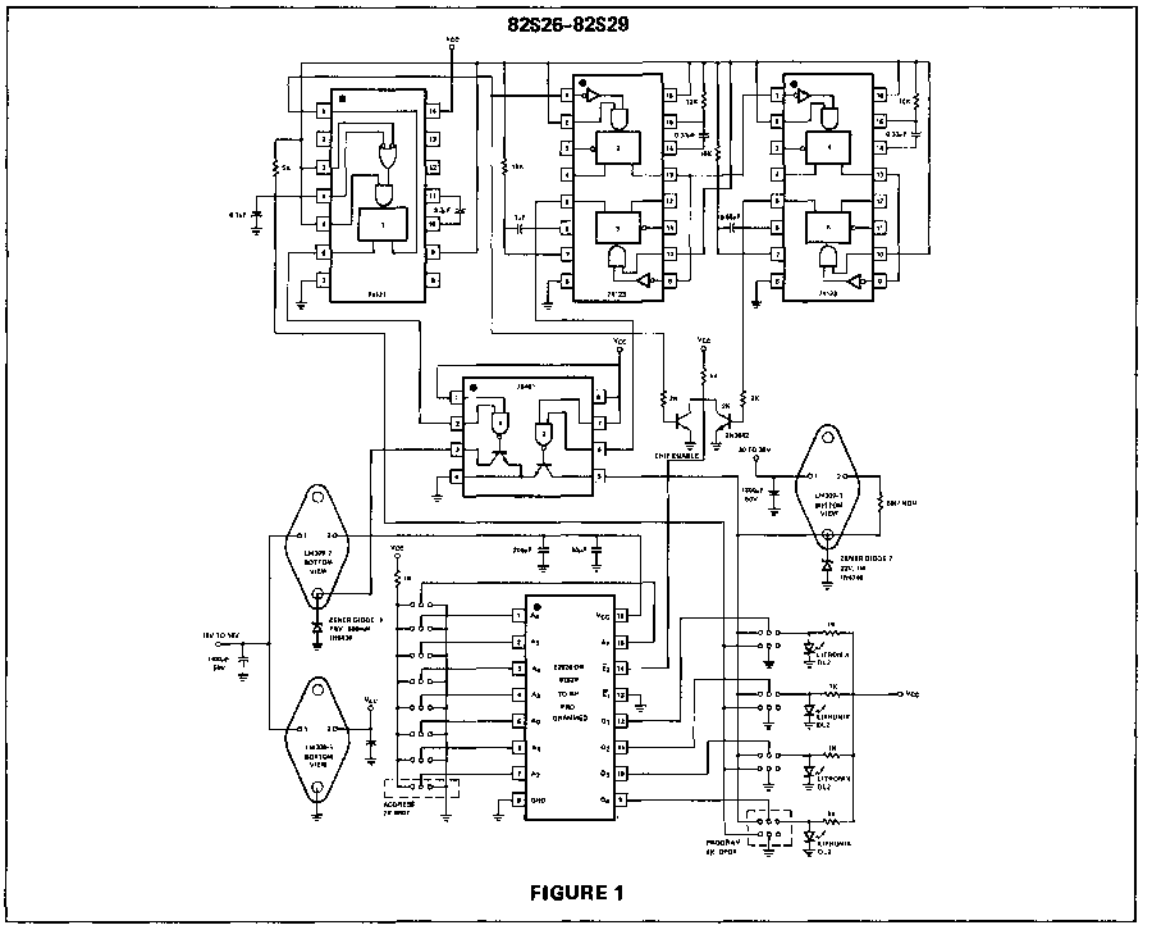


FIGURE 1

POWER SUPPLY AND WAVEFORMS

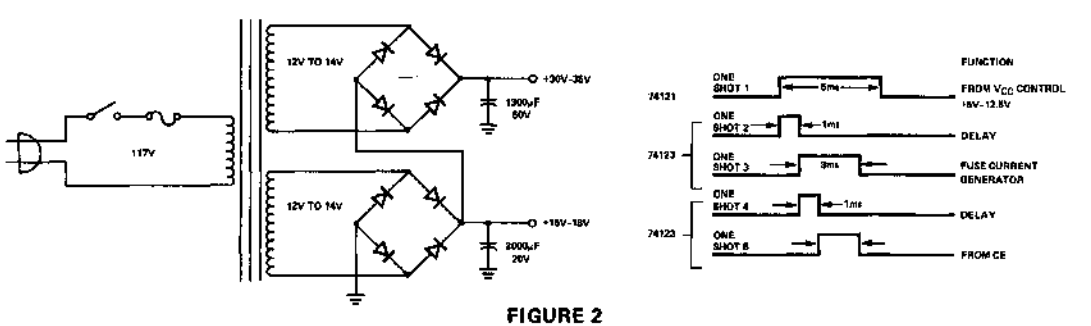


FIGURE 2

OBJECTIVE ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25$)

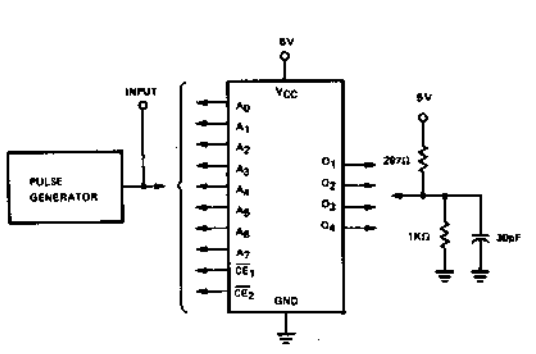
CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
"0" Output Voltage			0.5	V	I_{out} = 16mA
"1" Output Leakage (82S26)			40	μA	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{out} = 2.6V
(82S29)			100	μA	$\overline{CE_1}$ = $\overline{CE_2}$ = "0", V_{out} = 2.6V
(82S29)	-40		+40	μA	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{out} = 0.5 to 2.4V
"1" Output Current (82S29)	-2.0			mA	$\overline{CE_1}$ = $\overline{CE_2}$ = "0", V_{out} = 2.4V
"0" Input Current			-250	μA	V_{in} = 0.5V
"1" Input Current			50	μA	V_{in} = 2.7V
Input Threshold Voltage					
"0" Level	.85			V	
"1" Level			2.0	V	
Power Consumption 82S26		105/525	130/685	mA/mW	
82S29		115/575	145/760	mA/mW	

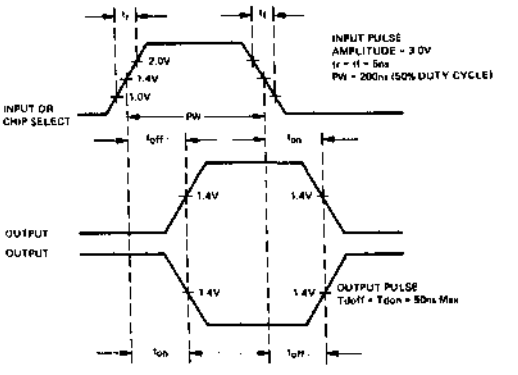
(T_A = 25°C and V_{CC} = 5.0V)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Input Clamp Voltage	-1.0			V	I_{in} = 5.0mA
Propagation Delay					
Address to Output			60	ns	
$\overline{\text{Chip Enable}}$ to Output			50	ns	

1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltage must not exceed 6.0V except while programming.
   Input currents must not exceed ±30 mA.
   Output currents must not exceed ±60mA except while programming.
4. Specifications are tentative. Final specifications will be available by May 1972.

AC TEST FIGURE AND WAVEFORM





Pins 13 and 14 when testing address-Output delays

CUSTOMER ORDERING INFORMATION

N8205Y - CB175	ASCII-TO-EBCDIC, EBCDIC-TO-ASCII
N8204Y - CB504	ASCII-TO-EBCDIC CODE CONVERTER
N8204Y - CB505	EBCDIC-TO-ASCII CODE CONVERTER

ASCII (ADDRESS) TO EBCDIC (DATA)

8205 — CB175 FIRST HALF
8204 — CB504

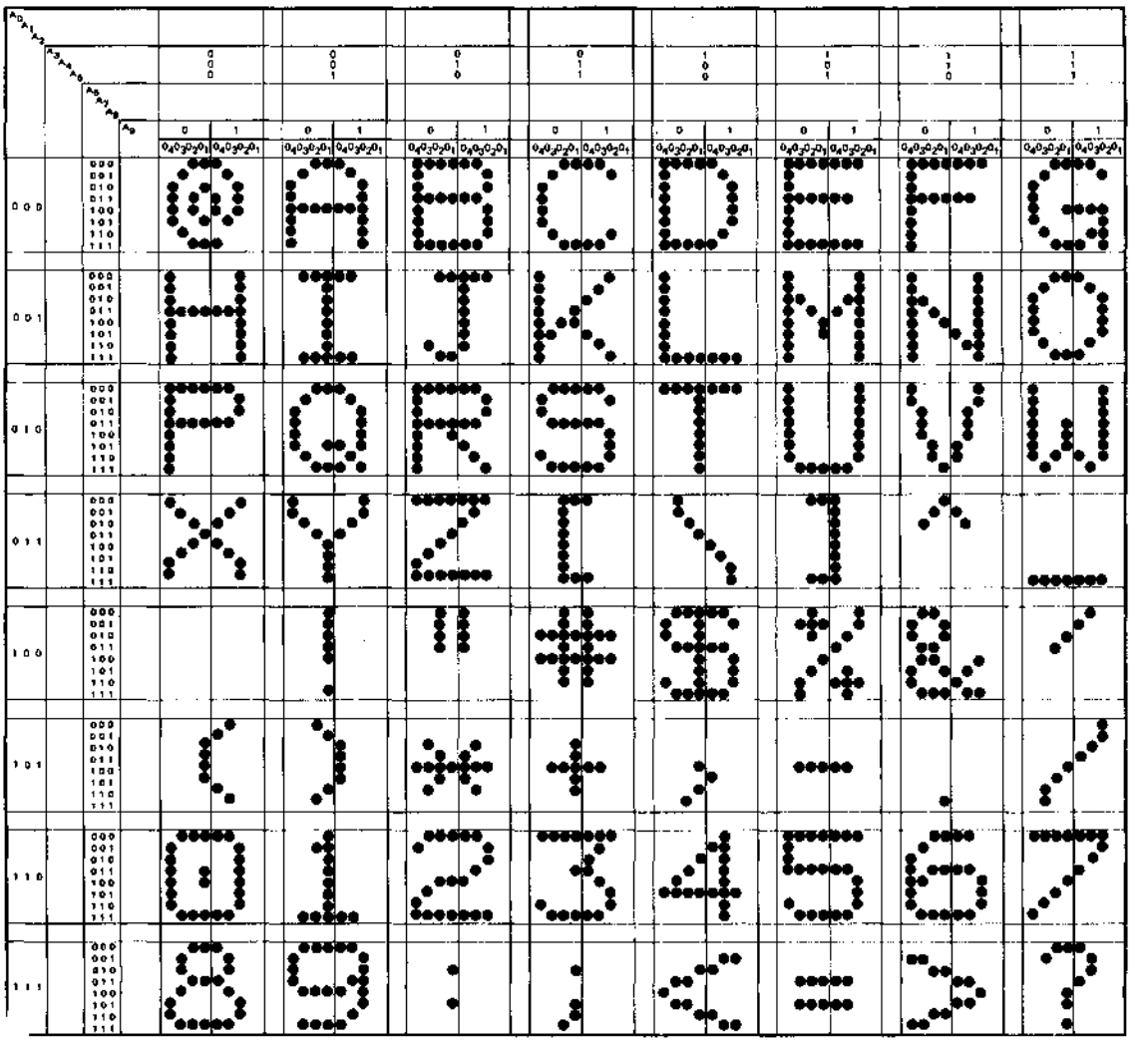
0 00000000	1 00000001	2 00000010	3 00000011	128 00100000	129 00100001	130 00100010	131 00100011
4 00110111	5 00101101	6 00101110	7 00101111	132 00100100	133 00010101	134 00000110	135 00010111
8 00010110	9 00000101	10 00100101	11 00001011	136 00101000	137 00101001	138 00101010	139 00101011
12 00001100	13 00001101	14 00001110	15 00001111	140 00101100	141 00001001	142 00001010	143 00011011
16 00010000	17 00010001	18 00010010	19 00010011	144 00110000	145 00111001	146 00011010	147 00110011
20 00111100	21 00111101	22 00110010	23 00100110	148 00110100	149 00110101	150 00110110	151 00001000
24 00011000	25 00011001	26 00111111	27 00100111	152 00111000	153 00111001	154 00111010	155 00111011
28 00011100	29 00011101	30 00011110	31 00011111	156 00000100	157 00010100	158 00111100	159 11100001
32 01000000	33 01001111	34 01111111	35 01111011	160 01000001	161 01000010	162 01000011	163 01000100
36 01011011	37 01101100	38 01010000	39 01111101	164 01000101	165 01000110	166 01000111	167 01001000
40 01001101	41 01011101	42 01011100	43 01001110	168 01001001	169 01010001	170 01010010	171 01010011
44 01101011	45 01100000	46 01001011	47 01100001	172 01010100	173 01010101	174 01010110	175 01010111
48 11110000	49 11110001	50 11110010	51 11110011	176 01011000	177 01011001	178 01100010	179 01100011
52 11110100	53 11110101	54 11110110	55 11110111	180 01100100	181 01100101	182 01100110	183 01100111
56 11111000	57 11111001	58 01111010	59 01011110	184 01101000	185 01101001	186 01110000	187 01110001
60 01001100	61 01111110	62 01101110	63 01101111	188 01110010	189 01110011	190 01110100	191 01110101
64 01111100	65 11000001	66 11000010	67 11000011	192 01110110	193 01110111	194 01111000	195 10000000
68 11000100	69 11000101	70 11000110	71 11000111	196 10001010	197 10001011	198 10001100	199 10001101
72 11001000	73 11001001	74 11010001	75 11010010	200 10001110	201 10001111	202 10010000	203 10011010
76 11010011	77 11010100	78 11010101	79 11010110	204 10011011	205 10011100	206 10011101	207 10011110
80 11010111	81 11011000	82 11011001	83 11100010	208 10011111	209 10100000	210 10101010	211 10101011
84 11100011	85 11100100	86 11100101	87 11100110	212 10101100	213 10101101	214 10101110	215 10101111
88 11100111	89 11101000	90 11101001	91 01001010	216 10110000	217 10110001	218 10110010	219 10110011
92 11100000	93 01011010	94 01011111	95 01101101	220 10110100	221 10110101	222 10110110	223 10110111
96 01111001	97 10000001	98 10000010	99 10000011	224 10111000	225 10111001	226 10111010	227 10111011
100 10000100	101 10000101	102 10000110	103 10000111	228 10111100	229 10111101	230 10111110	231 10111111
104 10001000	105 10001001	106 10010001	107 10010010	232 11001010	233 11001011	234 11001100	235 11001101
108 10010011	109 10010100	110 10010101	111 10010110	236 11001110	237 11001111	238 11011010	239 11011011
112 10010111	113 10011000	114 10011001	115 10100010	240 11011100	241 11011101	242 11011110	243 11011111
116 10100011	117 10100100	118 10100101	119 10100110	244 11101010	245 11101011	246 11101100	247 11101101
120 10100111	121 10101000	122 10101001	123 11000000	248 11101110	249 11101111	250 11111010	251 11111011
124 01101010	125 11010000	126 10100001	127 00000111	252 11111100	253 11111101	254 11111110	255 11111111

EBCDIC (ADDRESS) TO ASCII (DATA)

8205 — CB175 SECOND HALF
8204 — CB505

256 00000000	257 00000001	258 00000010	259 00000011	384 11000011	385 01100001	386 01100010	387 01100011
260 10011100	261 00001001	262 10000110	263 01111111	388 01100100	389 01100101	390 01100110	391 01100111
264 10010111	265 10001101	266 10001110	267 00001011	392 01101000	393 01101001	394 11000100	395 11000101
268 00001100	269 00001101	270 00001110	271 00001111	396 11000110	397 11000111	398 11001000	399 11001001
272 00010000	273 00010001	274 00010010	275 00010011	400 11001010	401 11001011	402 01101011	403 01101100
276 10011101	277 10000101	278 00001000	279 10000111	404 01101101	405 01101110	406 01101111	407 01110000
280 00011000	281 00011001	282 10010010	283 10001111	408 01110001	409 01110010	410 11001011	411 11001100
284 00011100	285 00011101	286 00011110	287 00011111	412 11001101	413 11001110	414 11001111	415 11010000
288 10000000	289 10000001	290 10000010	291 10000011	416 11010001	417 01111110	418 01110011	419 01110100
292 10000100	293 00001010	294 00010111	295 00011011	420 01110101	421 01110110	422 01110111	423 01111000
296 10001000	297 10001001	298 10001010	299 10001011	424 01111001	426 01111010	426 11010010	427 11010011
300 10001100	301 00000101	302 00000110	303 00000111	428 11010100	429 11010101	430 11010110	431 11010111
304 10010000	305 10010001	306 00010110	307 10010011	432 11011000	433 11011001	434 11011010	435 11011011
308 10010100	309 10010101	310 10010110	311 00000100	436 11011100	437 11011101	438 11011110	439 11011111
312 10011000	313 10011001	314 10011010	315 10011011	440 11100000	441 11100001	442 11100010	443 11100011
316 00010100	317 00010101	318 10011110	319 00011010	444 11100100	445 11100101	446 11100110	447 11100111
320 00100000	321 10100000	322 10100001	323 10100010	448 01111011	449 01000001	450 01000010	451 01000011
324 10100011	325 10100100	326 10100101	327 10100110	452 01000100	453 01000101	454 01000110	455 01000111
328 10100111	329 10101000	330 01011011	331 00101110	456 01001000	457 01001001	458 11101000	459 1110100
332 00111100	333 00101000	334 00101011	335 00100001	460 11101010	461 11101011	462 11101100	463 111011
336 00100110	337 10101001	338 10101010	339 10101011	464 01111101	465 01001010	466 01001011	467 0100
340 10101100	341 10101101	342 10101110	343 10101111	468 01001101	469 01001110	470 01001111	471 0101
344 10110000	345 10110001	346 01011101	347 00100100	472 01010001	473 01010010	474 11101110	475 111
348 00101010	349 00101001	350 00111011	351 01011110	476 11110000	477 11110001	478 11110010	479 111
352 00101101	353 00101111	354 10110010	355 10110011	480 01011100	481 10011111	482 01010011	483 01(
356 10110100	357 10110101	358 10110110	359 10110111	484 01010101	485 01010110	486 01010111	487 01(
360 10111000	361 10111001	362 01111100	363 00101100	488 01011001	489 01011010	490 11110100	491 11
364 00100101	365 01011111	366 00111110	367 00111111	492 11110110	493 11110111	494 11111000	495 11
368 10111010	369 10111011	370 10111100	371 10111101	496 00110000	497 00110001	498 00110010	499 00
372 10111110	373 10111111	374 11000000	375 11000001	500 00110100	501 00110101	502 00110110	503 0(
376 11000010	377 01100000	378 00111010	379 00100011	504 00111000	505 00111001	506 11111010	507 11
380 01000000	381 00100111	382 00111101	383 00100010	508 11111100	509 11111101	510 11111110	511 11

N8228I - CD162 PATTERN
USASC II ROW CHARACTER GENERATOR



PUNCHED CARD PROGRAM INPUT FOR 8204 & 8205

The customer may specify the content of the ROM either by filling out the accompanying form or by using punched cards. He should note that:

1. "Zero" levels on data out lines are defined as low.
2. Address bit A_0 is the least significant address bit. (See 8204 and 8205 data sheet)

Punched Card Data Input - Data to program the 8205 and the 8204 can be supplied in punched card-format. The format for the data is shown in Figure 1. Each data word is preceded by an address word which identifies its position in memory. Figure 2 shows the deck format for the 8204 256 x 8 bit ROM. For the 8204 the first card in the deck contains the part number and it is immediately followed by up to 40 alphanumeric characters of customer supplied information used to identify the part. The 64 customer data cards follow immediately. Figure 3 shows the deck format for the 8205 512 x 8 ROM. For the 8205 the first card in the deck contains the part number and it is immediately followed by up to 40 alphanumeric characters of customer supplied information used to identify the part. 128 data cards follow immediately. The left-most digit in the data word corresponds to output O_8 and the right-most digit to output O_1.

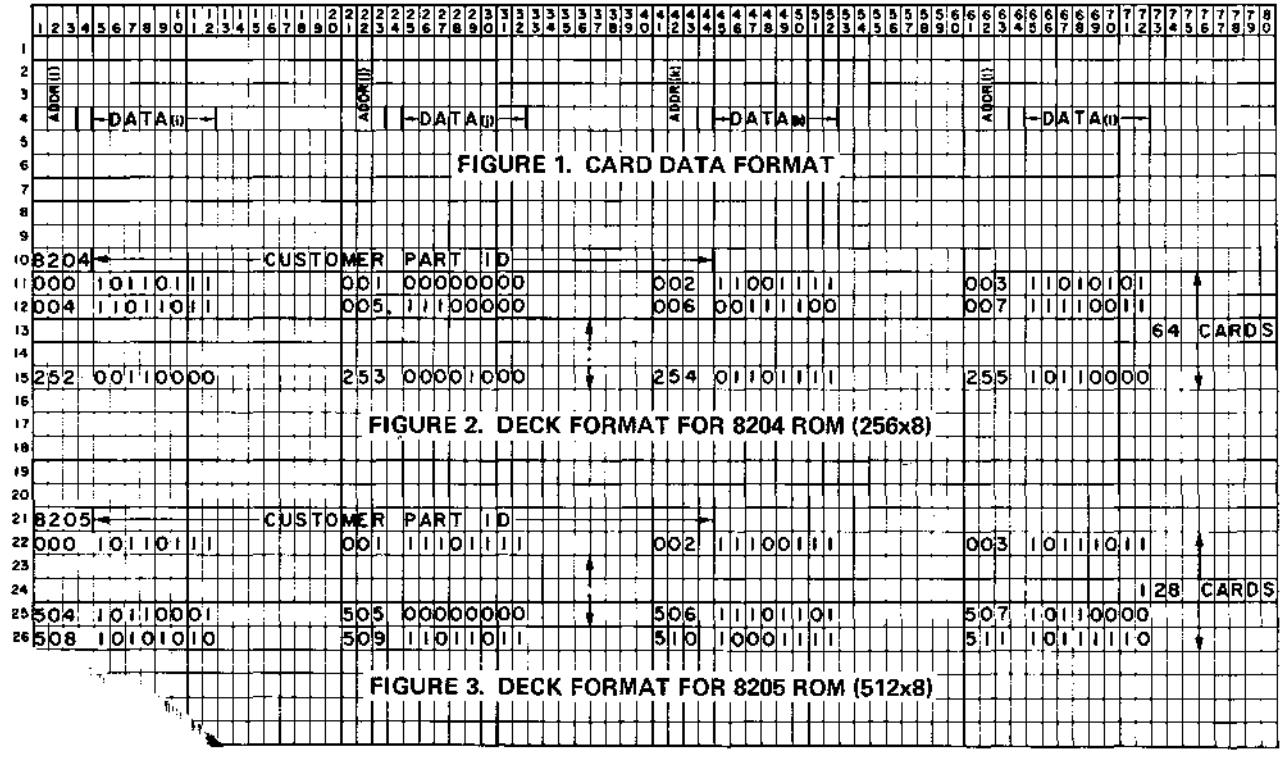


FIGURE 1. CARD DATA FORMAT

FIGURE 2. DECK FORMAT FOR 8204 ROM (256x8)

FIGURE 3. DECK FORMAT FOR 8205 ROM (512x8)

program can be transmitted directly to Signetics. Data
program the ROM requires 128 80-column IBM punched cards per 4096 bit device and 64 punched cards per 256 bit device.

Input Deck Format

For each 4096 bit ROM, the customer should prepare an input card deck as shown in Figure 1. The first two cards should be punched as shown and placed at the start of the deck. The third card should contain "8228" in the first four columns. In the next 40 positions, the customer should fill in his own part identification. These first three cards are then followed by 128 data cards. Immediately following are two cards to terminate the computer run. These should be punched by the customer.

Data Cards

Figure 2 shows the layout used in the data cards. Each data card specifies eight addresses and the four bits of data associated with these addresses. Address (i) tells the computer what position to assign Data (i) to etc. Immediately under this, a typical layout for the first two and the last data cards is shown.

INPUT CARD

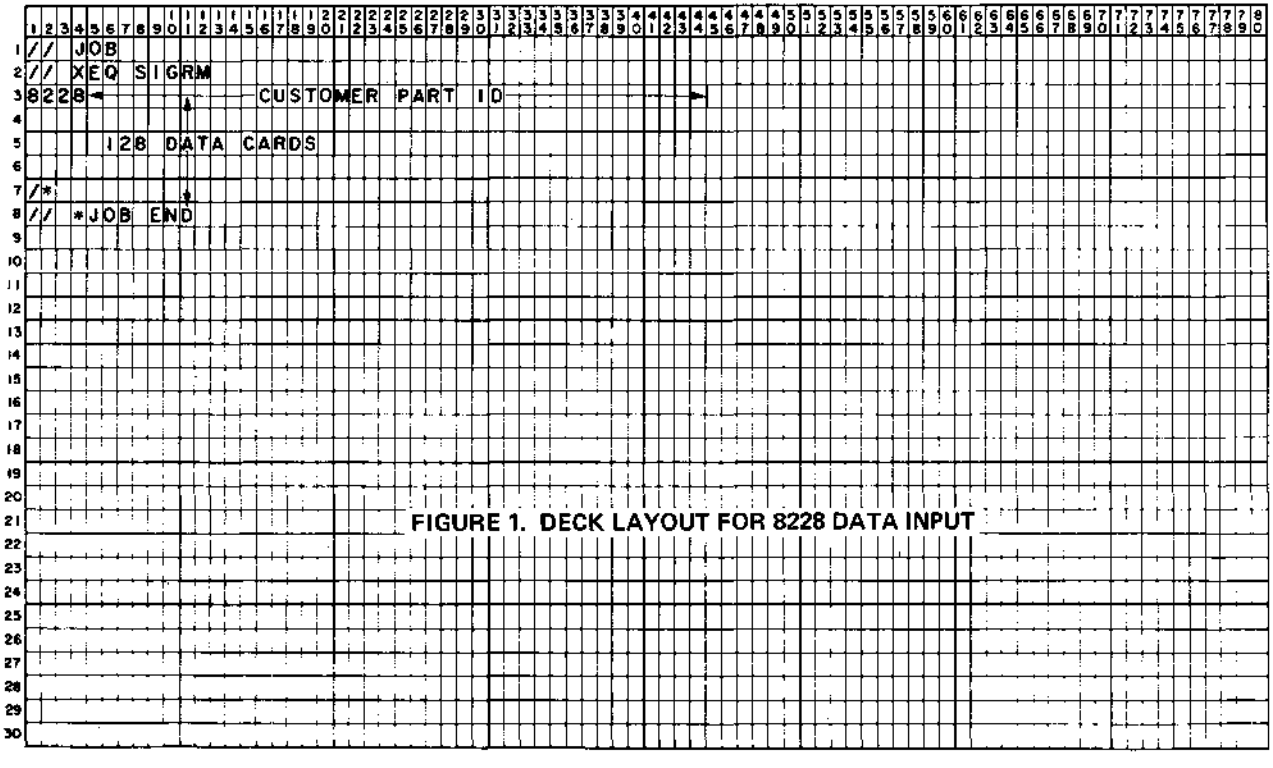


FIGURE 1. DECK LAYOUT FOR 8228 DATA INPUT

DATA CARDS

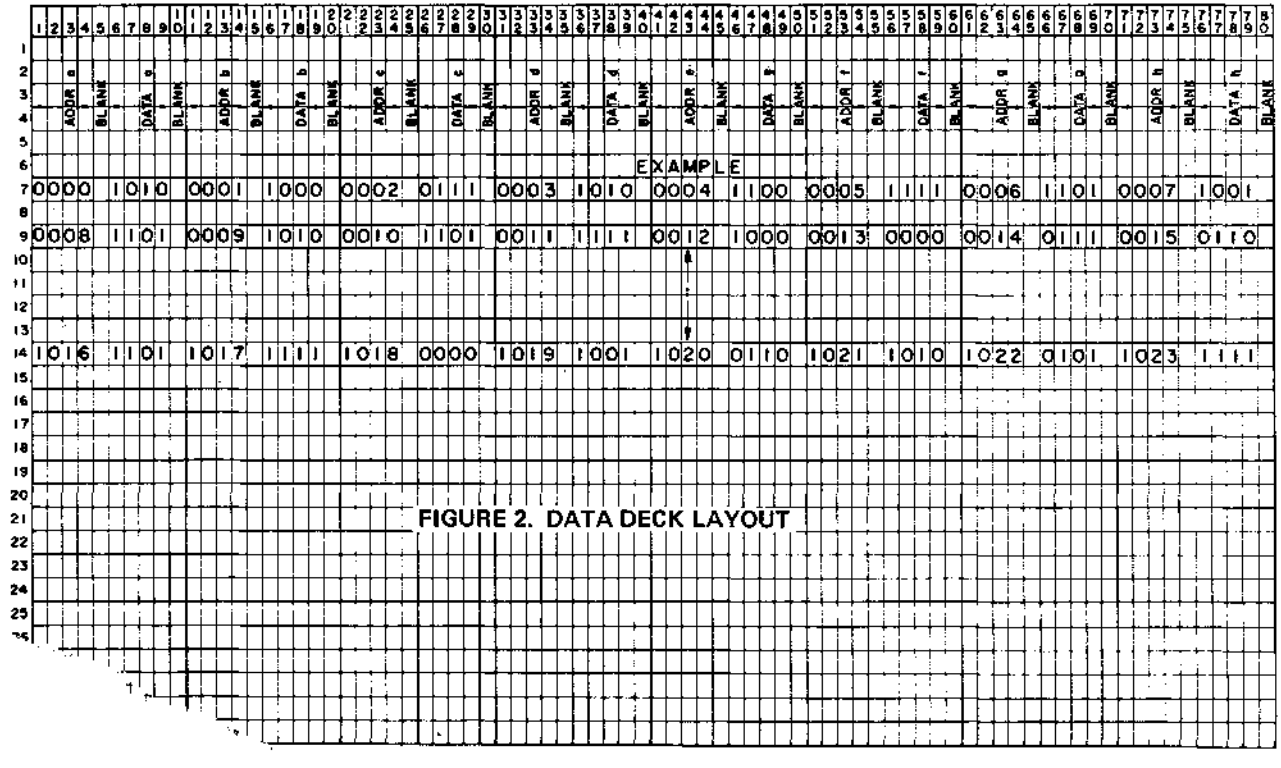


FIGURE 2. DATA DECK LAYOUT

(8204,8205)

READ ONLY MEMORY TRUTH TABLE/ORDERING BLANK

THIS PORTION TO BE COMPLETED BY SIGNETICS

YOUR NAME: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

Note: For 256 x 8 Use This Page Only

Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0									64									128									192								
1									65									129									193								
2									66									130									194								
3									67									131									195								
4									68									132									196								
5									69									133									197								
6									70									134									198								
7									71									135									199								
8									72									136									200								
9									73									137									201								
10									74									138									202								
11									75									139									203								
12									76									140									204								
13									77									141									205								
14									78									142									206								
15									79									143									207								
16									80									144									208								
17									81									145									209								
18									82									146									210								
19									83									147									211								
20									84									148									212								
21									85									149									213								
22									86									150									214								
23									87									151									215								
24									88									152									216								

25	89	153	217
26	90	154	218
27	91	155	219
28	92	156	220
29	93	157	221
30	94	158	222
31	95	159	223
32	96	160	224
33	97	161	225
34	98	162	226
35	99	163	227
36	100	164	228
37	101	165	229
38	102	166	230
39	103	167	231
40	104	168	232
41	105	169	233
42	106	170	234
43	107	171	235
44	108	172	236
45	109	173	237
46	110	174	238
47	111	175	239
48	112	176	240
49	113	177	241
50	114	178	242
51	115	179	243
52	116	180	244
53	117	181	245
54	118	182	246
55	119	183	247
56	120	184	248
57	121	185	249
58	122	186	250
59	123	187	251
	124	188	252
	125	189	253
	126	190	254
		191	255

(8204,8205)

2048/4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDERING BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Note: For 256 x 8 Use Previous Page Only

Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
256									320									384									448								
257									321									385									449								
258									322									386									450								
259									323									387									451								
260									324									388									452								
261									325									389									453								
262									326									390									454								
263									327									391									455								
264									328									392									456								
265									329									393									457								
266									330									394									458								
267									331									395									459								
268									332									396									460								
269									333									397									461								
270									334									398									462								
271									335									399									463								
272									336									400									464								
273									337									401									465								
274									338									402									466								
275									339									403									467								
276									340									404									468								
277									341									405									469								
278									342									406									470								
279									343									407									471								
280									344									408									472								

281									345									409									473								
282									346									410									474								
283									347									411									475								
284									348									412									476								
285									349									413									477								
286									350									414									478								
287									351									415									479								
288									352									416									480								
289									353									417									481								
290									354									418									482								
291									355									419									483								
292									356									420									484								
293									357									421									485								
294									358									422									486								
295									359									423									487								
296									360									424									488								
297									361									425									489								
298									362									426									490								
299									363									427									491								
300									364									428									492								
301									365									429									493								
302									366									430									494								
303									367									431									495								
304									368									432									496								
305									369									433									497								
306									370									434									498								
307									371									435									499								
308									372									436									500								
309									373									437									501								
310									374									438									502								
311									375									439									503								
312									376									440									504								
313									377									441									505								
314									378									442									506								
315									379									443									507								
316									380									444									508								
317									381									445									509								
318									382									446									510								
319									383									447									511								

(8223,8224) (82S23, 82S123)

CB (XXX) 256 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

WORD	INPUTS						OUTPUTS							
	A_4	A_3	A_2	A_1	A_0	ENABLE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
0					64					128					192				
1					65					129					193				
2					66					130					194				
3					67					131					195				
4					68					132					196				
5					69					133					197				
6					70					134					198				
7					71					135					199				
8					72					136					200				
9					73					137					201				
10					74					138					202				
11					75					139					203				
12					76					140					204				
13					77					141					205				
14					78					142					206				
15					79					143					207				
16					80					144					208				
17					81					145					209				
18					82					146					210				
19					83					147					211				
20					84					148					212				
21					85					149					213				
22					86					150					214				
23					87					151					215				
24					88					152					216				
25					89					153					217				

26					90					154					218					
27					91					155					219					
28					92					156					220					
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30					94					158					222					
31					95					159					223					
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34					98					162					226					
35					99					163					227					
36					100					164					228					
37					101					165					229					
38					102					166					230					
39					103					167					231					
40					104					168					232					
41					105					169					233					
42					106					170					234					
43					107					171					235					
44					108					172					236					
45					109					173					237					
46					110					174					238					
47					111					175					239					
48					112					176					240					
49					113					177					241					
50					114					178					242					
51					115					179					243					
52					116					180					244					
53					117					181					245					
54					118					182					246					
55					119					183					247					
56					120					184					248					
57					121					185					249					
58					122					186					250					
59					123					187					251					
60					124					188					252					
61					125					189					253					
62					126					190					254					
63					127					191					255					

8228

4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

	OUTPUT					OUTPUT					OUTPUT					OUTPUT			
Word	O_4	O_3	O_2	O_1	Word	O_4	O_3	O_2	O_1	Word	O_4	O_3	O_2	O_1	Word	O_4	O_3	O_2	O_1
0					70					140					210				
1					71					141					211				
2					72					142					212				
3					73					143					213				
4					74					144					214				
5					75					145					215				
6					76					146					216				
7					77					147					217				
8					78					148					218				
9					79					149					219				
10					80					150					220				
11					81					151					221				
12					82					152					222				
13					83					153					223				
14					84					154					224				
15					85					155					225				
16					86					156					226				
17					87					157					227				
18					88					158					228				
19					89					159					229				
20					90					160					230				
21					91					161					231				
22					92					162					232				
23					93					163					233				
24					94					164					234				
25					95					165					235				
26					96					166					236				
27					97					167					237				
28					98					168					238				

29	99	169	239
30	100	170	240
31	101	171	241
32	102	172	242
33	103	173	243
34	104	174	244
35	105	175	245
36	106	176	246
37	107	177	247
38	108	178	248
39	109	179	249
40	110	180	250
41	111	181	251
42	112	182	252
43	113	183	253
44	114	184	254
45	115	185	255
46	116	186	256
47	117	187	257
48	118	188	258
49	119	189	259
50	120	190	260
51	121	191	261
52	122	192	262
53	123	193	263
54	124	194	264
55	125	195	265
56	126	196	266
57	127	197	267
58	128	198	268
59	129	199	269
60	130	200	270
61	131	201	271
62	132	202	272
63	133	203	273
64	134	204	274
65	135	205	275
66	136	206	276
67	137	207	277
68	138	208	278
69	139	209	279

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Word	OUTPUT O_4	O_3	O_2	O_1	Word	OUTPUT O_4	O_3	O_2	O_1	Word	OUTPUT O_4	O_3	O_2	O_1	Word	OUTPUT O_4	O_3	O_2	O_1
280					350					420					490				
281					351					421					491				
282					352					422					492				
283					353					423					493				
284					354					424					494				
285					355					425					495				
286					356					426					496				
287					357					427					497				
288					358					428					498				
289					359					429					499				
290					360					430					500				
291					361					431					501				
292					362					432					502				
293					363					433					503				
294					364					434					504				
295					365					435					505				
296					366					436					506				
297					367					437					507				
298					368					438					508				
299					369					439					509				
300					370					440					510				
301					371					441					511				
302					372					442					512				
303					373					443					513				
304					374					444					514				
305					375					445					515				
306					376					446					516				
307					377					447					517				
308					378					448					518				

309					379					449					519				
310					380					450					520				
311					381					451					521				
312					382					452					522				
313					383					453					523				
314					384					454					524				
315					385					455					525				
316					386					456					526				
317					387					457					527				
318					388					458					528				
319					389					459					529				
320					390					460					530				
321					391					461					531				
322					392					462					532				
323					393					463					533				
324					394					464					534				
325					395					465					535				
326					396					466					536				
327					397					467					537				
328					398					468					538				
329					399					469					539				
330					400					470					540				
331					401					471					541				
332					402					472					542				
333					403					473					543				
334					404					474					544				
335					405					475					545				
336					406					476					546				
337					407					477					547				
338					408					478					548				
339					409					479					549				
340					410					480					550				
341					411					481					551				
342					412					482					552				
343					413					483					553				
344					414					484					554				
345					415					485					555				
346					416					486					556				
347					417					487					557				
348					418					488					558				
349					419					489					559				

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

	OUTPUT					OUTPUT					OUTPUT					OUTPUT			
Word	O_4	O_3	O_2	O_1	Word	O_4	O_3	O_2	O_1	Word	O_4	O_3	O_2	O_1	Word	O_4	O_3	O_2	O_1
560					630					700					770				
561					631					701					771				
562					632					702					772				
563					633					703					773				
564					634					704					774				
565					635					705					775				
566					636					706					776				
567					637					707					777				
568					638					708					778				
569					639					709					779				
570					640					710					780				
571					641					711					781				
572					642					712					782				
573					643					713					783				
574					644					714					784				
575					645					715					785				
576					646					716					786				
577					647					717					787				
578					648					718					788				
579					649					719					789				
580					650					720					790				
581					651					721					791				
582					652					722					792				
583					653					723					793				
584					654					724					794				
585					655					725					795				
586					656					726					796				
587					657					727					797				
588					658					728					798				

589					659					729					799				
590					660					730					800				
591					661					731					801				
592					662					732					802				
593					663					733					803				
594					664					734					804				
595					665					735					805				
596					666					736					806				
597					667					737					807				
598					668					738					808				
599					669					739					809				
600					670					740					810				
601					671					741					811				
602					672					742					812				
603					673					743					813				
604					674					744					814				
605					675					745					815				
606					676					746					816				
607					677					747					817				
608					678					748					818				
609					679					749					819				
610					680					750					820				
611					681					751					821				
612					682					752					822				
613					683					753					823				
614					684					754					824				
615					685					755					825				
616					686					756					826				
617					687					757					827				
618					688					758					828				
619					689					759					829				
620					690					760					830				
621					691					761					831				
622					692					762					832				
623					693					763					833				
624					694					764					834				
625					695					765					835				
626					696					766					836				
627					697					767					837				
628					698					768					838				
629					699					769					839				

CUSTOMER: _____	THIS PORTION TO BE COMPLETED BY SIGNETICS
P.O. NO.: _____	PART NO.: _____
YOUR PART NO.: _____	S.D. NO.: _____
DATE: _____	DATE RECEIVED: _____

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
840					910					980									
841					911					981									
842					912					982									
843					913					983									
844					914					984									
845					915					985									
846					916					986									
847					917					987									
848					918					988									
849					919					989									
850					920					990									
851					921					991									
852					922					992									
853					923					993									
854					924					994									
855					925					995									
856					926					996									
857					927					997									
858					928					998									
859					929					999									
860					930					1000									
861					931					1001									
862					932					1002									
863					933					1003									
864					934					1004									
865					935					1005									
866					936					1006									
867					937					1007									
868					938					1008									

869	939	1009
870	940	1010
871	941	1011
872	942	1012
873	943	1013
874	944	1014
875	945	1015
876	946	1016
877	947	1017
878	948	1018
879	949	1019
880	950	1020
881	951	1021
882	952	1022
883	953	1023
884	954	
885	955	
886	956	
887	957	
888	958	
889	959	
890	960	
891	961	
892	962	
893	963	
894	964	
895	965	
896	966	
897	967	
898	968	
899	969	
900	970	
901	971	
902	972	
903	973	
904	974	
905	975	
906	976	
907	977	
908	978	
909	979	

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signetics

ECL 1000/10,000
PRODUCT
SPECIFICATIONS

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ECL Functional Index

PART NO.	REPLACES
N1004A	MC1004P
N1005A	MC1005P
N1006A	MC1006P
N1010A	MC1010P
N1011A	MC1011P
N1012A	MC1012P
N1013A	MC1013P
N1014A	MC1014P

PART NO.	REPLACES
N1015A	MC1015P
N1016A	MC1016P
N1017A	MC1017P
N1024A	MC1024P
N1025A	MC1025P
N1027A	MC1027P
N1033A	MC1033P
N1039B	MC1039P

DESCRIPTION

The ECL II series of monolithic integrated logic circuits presents the system designer with an integrated circuit family designed to permit system implementation with a relatively small number of individual types. This approach offers cost savings, reduced power supply requirements, small physical size and high reliability.

ECL II circuits feature very fast propagation times relative to rise and fall times. This and the constant current feature impose fewer restrictions on system design, layout and fabrication than other high-speed families.

FEATURES

- FULL REPLACEMENTS FOR MOTOROLA MECL II PARTS
- EXCELLENT NOISE IMMUNITY
- SIMULTANEOUS OR/NOR OUTPUTS
- HIGH FAN-IN AND FAN-OUT
- INTERNAL TEMPERATURE COMPENSATION

APPLICATIONS

- HIGH SPEED DATA PROCESSORS
- DATA CONCENTRATORS
- CHARACTER RECOGNITION EQUIPMENT
- INSTRUMENTATION

REFER TO SECTION 8 FOR ECL II PACKAGE DESCRIPTIONS

(V_{CC} = 0, V_{EE} = -5.2V, T_A = 25°C)

FUNCTION	PART NO. (0 to +75°C)	DC OUTPUT LOADING FACTOR	PROPAGATION DELAY nsec typ.	TOTAL POWER DISSIPATION mW typ.
Dual 4 Input Gate, 2 OR Outputs w/Pulldowns 2 NOR Outputs w/Pulldowns	N1004A	25	4.0	95
Dual 4 Input Gate, 2 OR Outputs w/Pulldowns 2 NOR Outputs w/o Pulldowns	N1005A	25	4.0	65
Dual 4 Input Gate, 2 OR Outputs w/o Pulldowns 2 NOR Outputs w/o Pulldowns	N1006A	25	4.0	45
Quad 2 Input Gate, 4 NOR Outputs w/Pulldowns	N1010A	25	4.5	115
Quad 2 Input Gate, 2 NOR Outputs w/Pulldowns 2 NOR Outputs w/o Pulldowns	N1011A	25	4.5	95
Quad 2 Input Gate, 4 NOR Outputs w/o Pulldowns	N1012A	25	4.5	65
AC Coupled J-K Flip-Flop (85MHz Typ.)	N1013A	25	6.0	125
Dual R-S Flip-Flop (Positive Clock)	N1014A	25	6.0	140
Dual R-S Flip-Flop (Negative Clock)	N1015A	25	6.0	140
Dual R-S Flip-Flop (Single Rail)	N1016A	25	6.0	140
Level Translator (Saturated Logic to ECL)	N1017A	25 (ECL)	15	105
Dual 2 Input Expandable Gate	N1024A	25	4.0	95
Dual 4 and 5 Input Expander	N1025A	–	–	–
AC Coupled J-K Flip-Flop (120 MHz Typ.)	N1027A	25	4.0	250
Dual R-S Flip-Flop (Single Rail, Negative Clock)	N1033A	25	6.0	140
Quad Level Translator (ECL to Saturated Logic)	N1039B	7 (DTL)	12	200

DEFINITIONS

I_{in} — Current drawn by the input of the test unit when a maximum logic "1" ($V_{IH\ max}$) is applied at that input

I_{out} — Output current

I_R — Reverse current drawn from a transistor input of the test unit when V_{EE} is applied at that input

V_{BB} — Bias reference supply voltage (-1.175 V nominal at 25°C)

V_{BE} — Base-to-emitter voltage drop of a transistor

V_{CB} — Collector-to-base voltage drop of a transistor

V_{CC} — Most positive power supply voltage for a circuit

V_{EE} — Most negative power supply voltage for a circuit

V_{in} — Input voltage

$V_{IH\ max}$ — Maximum input logic "1" level voltage

$V_{IH\ min}$ — Minimum input logic "1" level (threshold) voltage

$V_{IL\ max}$ — Maximum input logic "0" level (threshold) voltage

$V_{IL\ min}$ — Minimum input logic "0" level voltage

$V_{OH\ max}$ — Maximum output "1" or high-level voltage

$V_{OH\ min}$ — Minimum output "1" high-level voltage

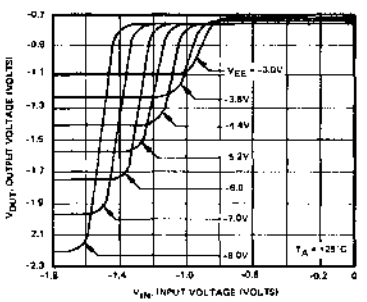
$V_{OL\ max}$ — Maximum output "0" or low-level voltage

$V_{OL\ min}$ — Minimum output "0" or low-level voltage

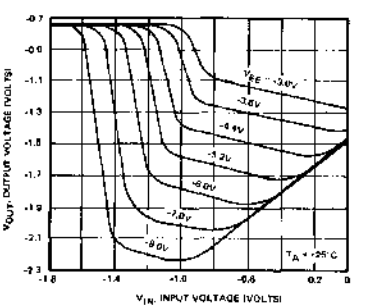
V_{out} — Output voltage

TYPICAL CHARACTERISTIC CURVES

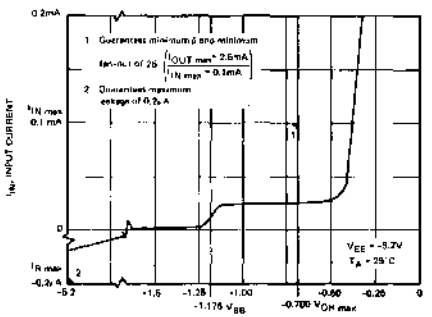
TYPICAL "OR" TRANSFER CHARACTERISTICS



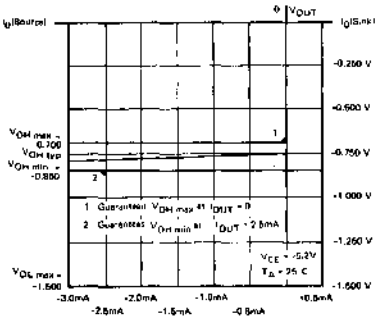
TYPICAL "NOR" TRANSFER CHARACTERISTICS



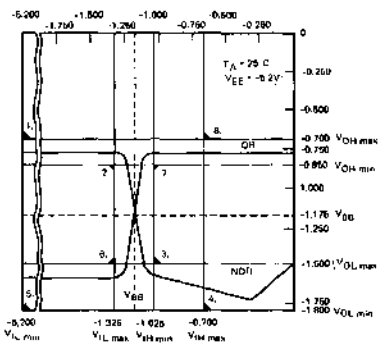
TYPICAL INPUT VOLTAGE VERSUS INPUT CURRENT



TYPICAL OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



ECL II TRANSFER CHARACTERISTICS AND SPECIFICATION POINTS



ECL II WORST-CASE LEVELS

VOLTAGE LEVEL	AMBIENT TEMPERATURE				
	125°C	75°C	25°C	0°C	-55°C
V_{IH} max	-0.630	-0.615	-0.700	-0.740	-0.825
V_{OH} max	-0.630	-0.615	-0.700	-0.735	-0.825
V_{OH} min	-0.700	-0.775	-0.850	-0.895	-0.990
V_{IH} min	-0.875	-0.950	-1.025	-1.070	-1.165
V_{IL} max	-1.205	-1.260	-1.325	-1.350	-1.405
V_{OL} max	-1.380	-1.435	-1.500	-1.525	-1.580
V_{OL} min	-1.720	-1.760	-1.800	-1.830	-1.890
V_{IL} min	<V_{EE}	<V_{EE}	<V_{EE}	<V_{EE}	<V_{EE}

$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ = 0.015 max

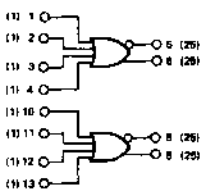
$\frac{\Delta(V_{IH\ min}, V_{IL\ max})}{\Delta V_{EE}}$ = 0.110 min, 0.115 nom, 0.120 max

$\frac{\Delta(V_{OL\ max}, V_{OL\ min})}{\Delta V_{EE}}$ = 0.210 min, 0.320 nom, 0.250 max

LOGIC DIAGRAMS

The logic diagrams shown describe the circuits of the ECL II line and permit quick selection of those circuits required to implement a particular logic system. Logic equations, truth tables, typical propagation delay time (t_{pd}), and typical power dissipation per package (P_D) are provided to show line compatibility. Package pin numbers and dc loading factors are specified on each logic diagram. Numbers at the ends of the terminals are package pin numbers. Numbers in parenthesis indicate dc loading factors at each terminal. ECL II circuits contain internal bias networks, insuring that the transition point is always in the center of the transfer characteristic curves over the temperature range.

DUAL 4-INPUT GATE



$5 = \overline{1 + 2 + 3 + 4}$

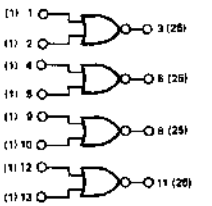
$6 = 1 + 2 + 3 + 4$

t_{pd} = 4.0ns

P_D = 1004 -95mW, 1005 -65mW, 1006 -45mW

1004, 1005, 1006

QUAD 2-INPUT GATE



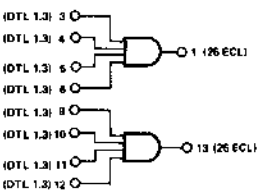
$3 = \overline{1 + 2}$

t_{pd} = 4.5ns

P_D = 1010 -115mW, 1011 - 95mW, 1012 - 65mW

1010, 1011, 1012

LEVEL TRANSLATOR



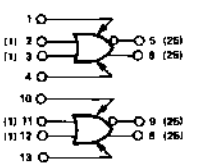
$1 = 3 \bullet 4 \bullet 5 \bullet 6$

t_{pd} = 15ns

P_D = 105mW

1017

DUAL 2-INPUT EXPANDABLE GATE



$5 = \overline{2 + 3}$

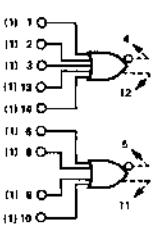
$6 = 2 + 3$

t_{pd} = 4.0ns

P_D = 95mW

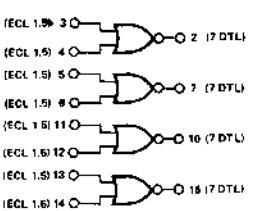
1024

DUAL 4-5 INPUT EXPANDER



1025

QUAD LEVEL TRANSLATOR



$2 = \overline{3 + 4}$

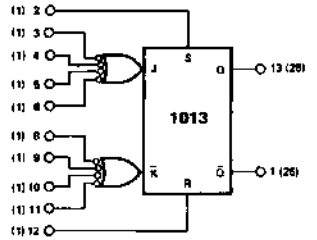
or $2 = \overline{3} \cdot \overline{4}$

t_{pd} = 12ns

P_D = 200mW

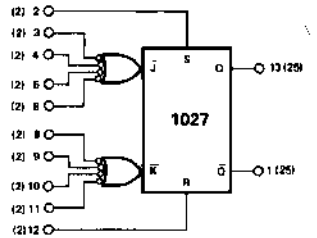
1039

AC COUPLED J-K FLIP-FLOP (85 MHz TYP)



t_{pd} = 6.0ns
P_D = 126mW

AC COUPLED J-K FLIP-FLOP (120 MHz TYP)



t_{pd} = 4.0ns
P_D = 250mW

CLOCKED J-K OPERATION

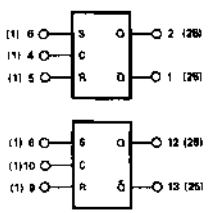
$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
ϕ	ϕ	0	Q^n
0	0	1	Q^n
0	1	1	1
1	0	1	0
1	1	1	Q^n

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} -0.6V) Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

R-S OPERATION

R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	ND

DUAL CLOCKED R-S FLIP-FLOP



t_{pd} = 6.0ns
P_D = 140mW

1014 1015

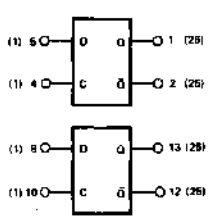
1014

C	R	S	Q^{n+1}
1	0	0	Q^n
1	0	1	1
1	1	0	0
1	1	1	ND
0	ϕ	ϕ	Q^n

1015

C	R	S	Q^{n+1}
0	0	0	Q^n
0	0	1	1
0	1	0	0
0	1	1	ND
1	ϕ	ϕ	Q^n

DUAL CLOCKED SINGLE RAIL R-S FLIP-FLOP



t_{pd} = 6.0ns
P_D = 140mW

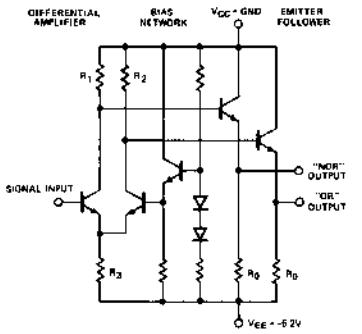
1016 1033

1016

C	D	Q^{n+1}
0	0	Q^n
0	1	Q^n
1	0	0
1	1	1

1033

C	D	Q^{n+1}
1	0	Q^n
1	1	Q^n
0	0	0
0	1	1



LOGICAL "1" = -0.75 V(V_H)

LOGICAL "0" = -1.60 V(V_L)

FOR LOGICAL "1" INPUT, "NOR" OUTPUT = - .60V
"OR" OUTPUT = -1.75V
FOR LOGICAL "0" INPUT, "NOR" OUTPUT = -1.75V
"OR" OUTPUT = - .60V

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC}=0)	V_{EE}	-10	V_{DC}
Input Voltage (V_{CC}=0)	V_{IN}	0 to V_{EE}	V_{DC}
Output Source Current	I_O	0 to +25	mAdc
Storage Temperature Range	T_{stg}	-55 to -125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
AC Fan-In (Expandable Gates)	m	20	-
AC Fan-Out* (Gates and Flip-Flops)	n	15	-

*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

CIRCUIT DESCRIPTION

The ECL II line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic.

The typical ECL II circuit comprises a differential-amplifier input with internal bias reference and with emitter-follower output to restore dc levels. High fan-out operation is possible because of high input impedance of the differential amplifier and low output impedance of the emitter followers. Power supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during transition time. Basic gate design provides for simultaneous output of both the function and its complement.

As shown in the schematic above, it is recommended that -5.2V be applied at V_{EE} with V_{CC} = Gnd.

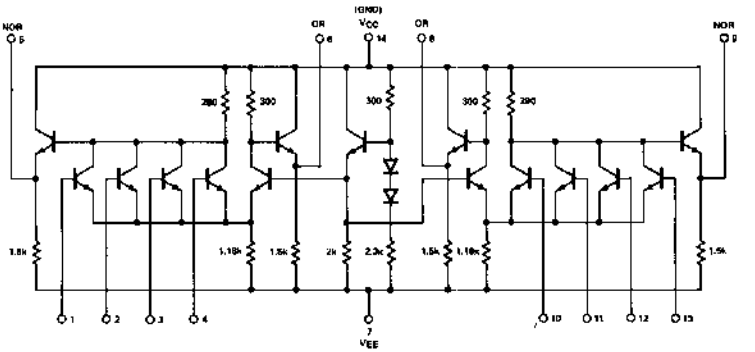
The nominal output logic swing of 0.85V varies from a low state of V_L = -1.60V to a high state of V_H = -0.75V.

An internal voltage of -1.175V is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_3 is supplied by the internally biased transistor. A drop of 0.85V occurs across R_2. The OR output then is -1.60V, one V_{BE} drop below 0.85V. Since no current flows in the "signal input transistor, the NOR output is a V_{BE} drop below ground, -0.75V. When a logical "1" level is applied to the "signal input", the current through R2 is switched to the "signal input" transistor and a drop of 0.85V occurs across R_1. The OR output then goes to -0.75V, and the NOR output goes to -1.60V.

NOTE: Unused inputs should be connected to V_{EE}.

The voltage applied to the bias input is obtained from an internal regulated, temperature-compensated bias network. The temperature characteristics of the bias network compensate for variations in circuit operating point over the temperature range or supply voltage changes, and insure that the threshold point is in the center of the transfer characteristic curves.

DUAL 4-INPUT GATES



1004 Shown

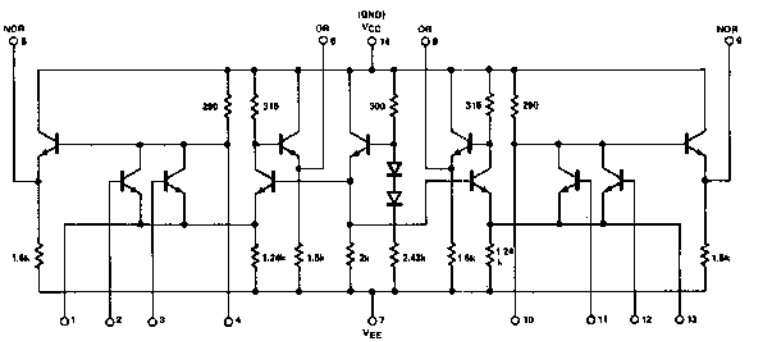
1005
Omit NOR output pulldown resistors

1006
Omit all output pulldown resistors

Resistor values are nominal

1004 THRU 1006

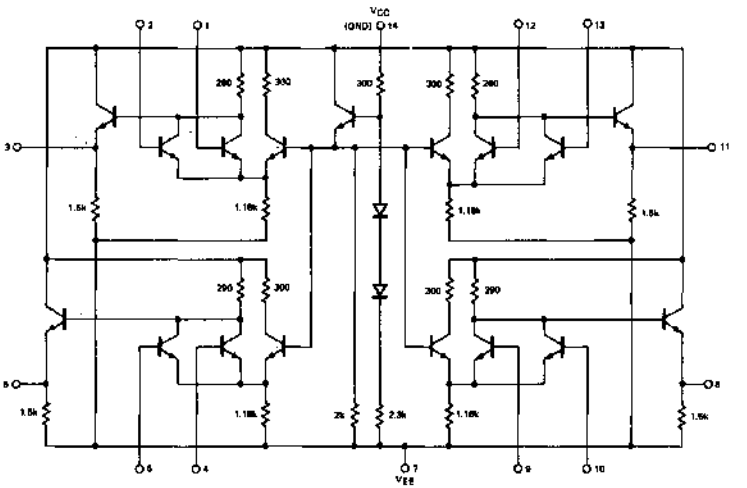
DUAL 2-INPUT EXPANDABLE GATE



Resistor values are nominal

1024

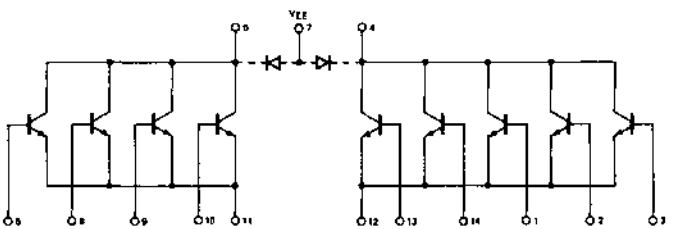
QUAD 2-INPUT GATES



1010 Shown
1011
Omit pulldown resistors
on pins 3 and 6
1012
Omit all output
pulldown resistors
Resistor values are nominal

1010 THRU 1012

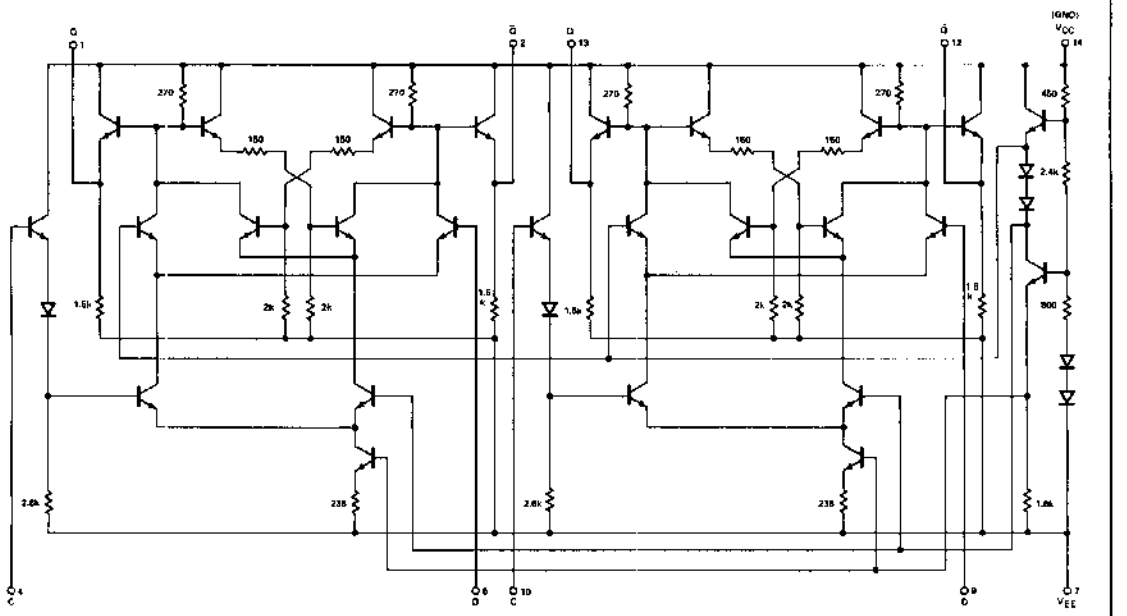
DUAL 4-5 INPUT EXPANDER



Resistor values are nominal

1026

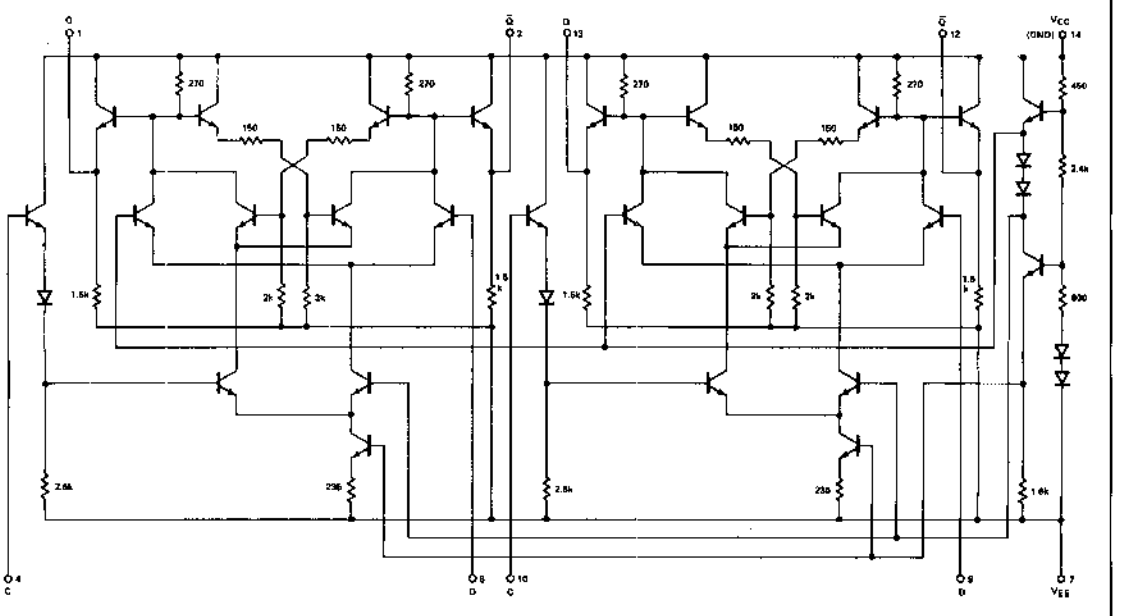
DUAL R-S FLIP-FLOP WITH SINGLE RAIL INPUT AND POSITIVE CLOCK



Resistor values are nominal

1016

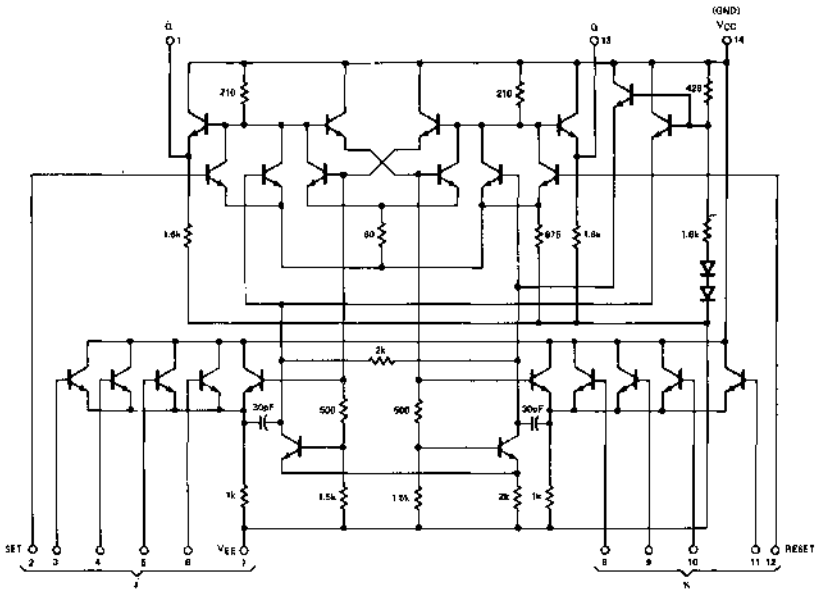
DUAL R-S FLIP-FLOP WITH SINGLE RAIL INPUT AND NEGATIVE CLOCK



Resistor values are nominal

1033

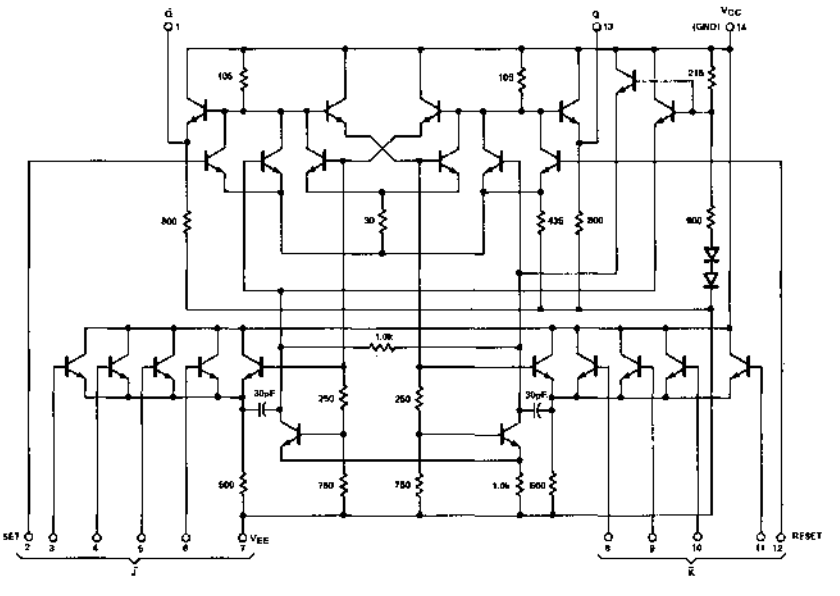
85-MHz AC-COUPLED $\overline{J}$-$\overline{K}$ FLIP-FLOP



Resistor values are nominal

1013

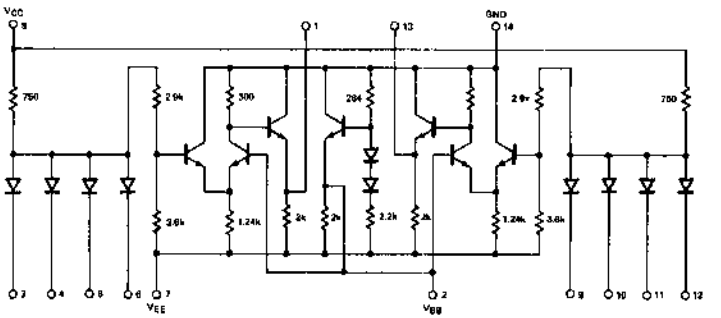
120-MHz AC-COUPLED $\overline{J}$-$\overline{K}$ FLIP FLOP



Resistor values are nominal

1027

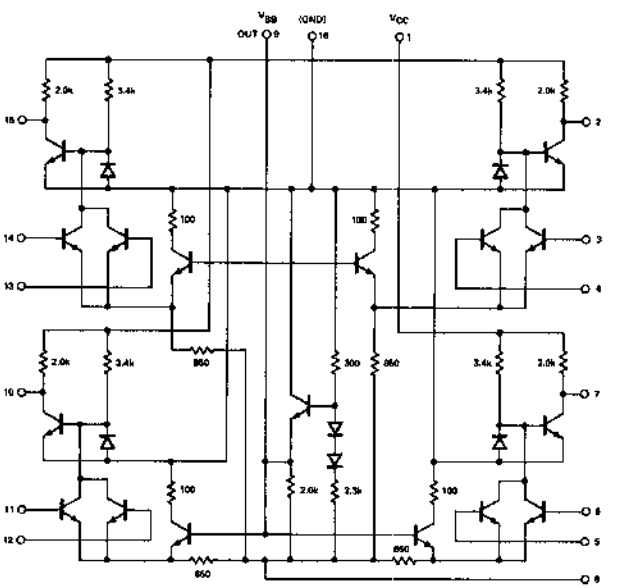
SATURATED LOGIC-TO-ECL DUAL TRANSLATOR



Resistor values are nominal

1017

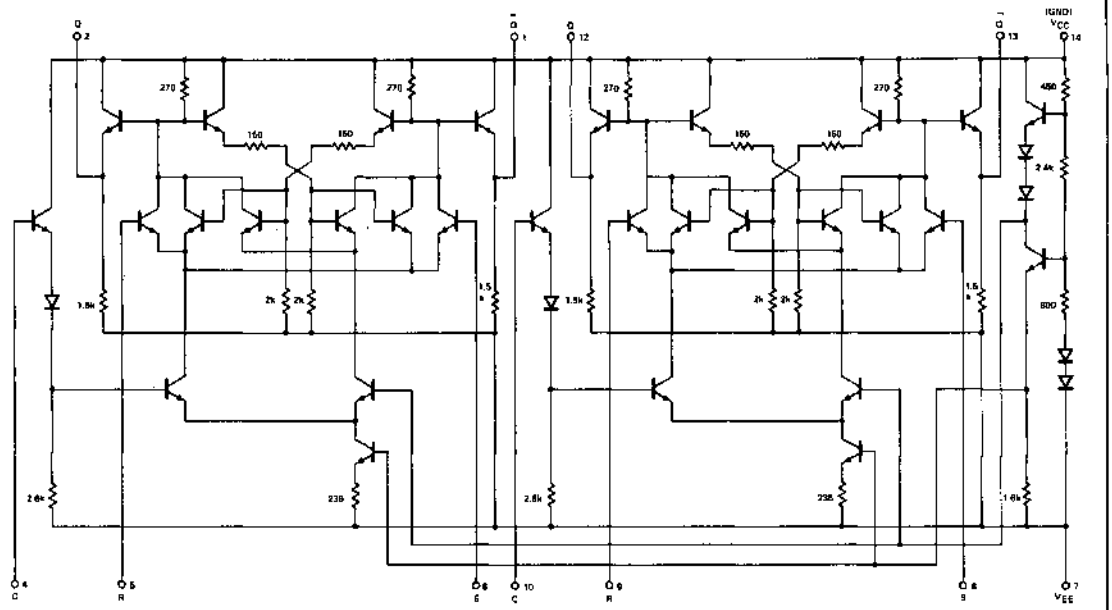
ECL-TO-SATURATED LOGIC QUAD TRANSLATOR



Resistor values are nominal

1039

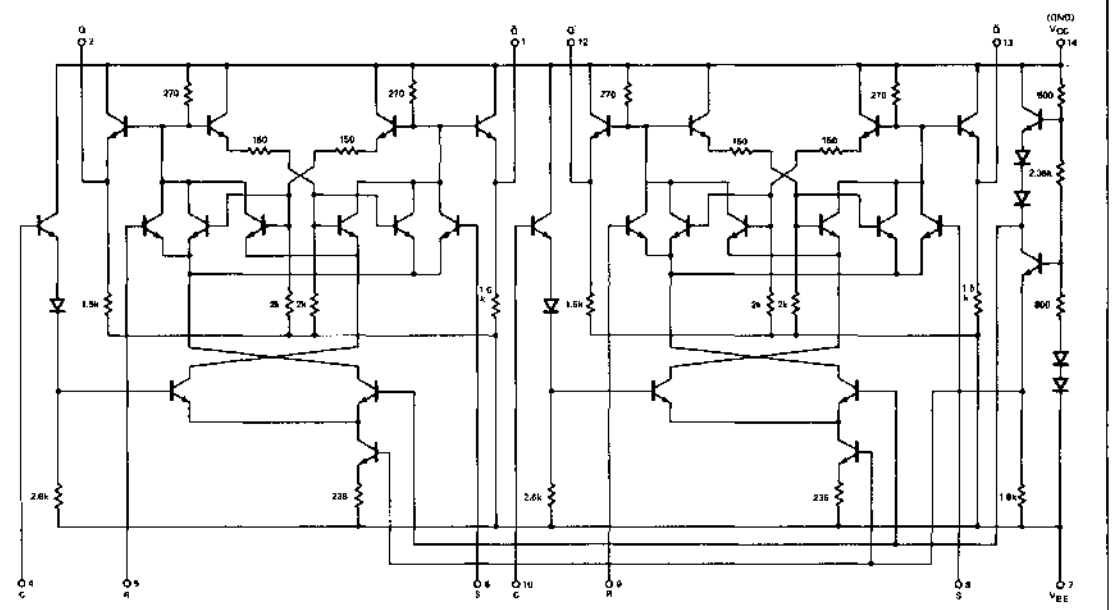
DUAL R-S FLIP-FLOP WITH POSITIVE CLOCK



Resistor values are nominal

1014

DUAL R-S FLIP-FLOP WITH NEGATIVE CLOCK



Resistor values are nominal

1015

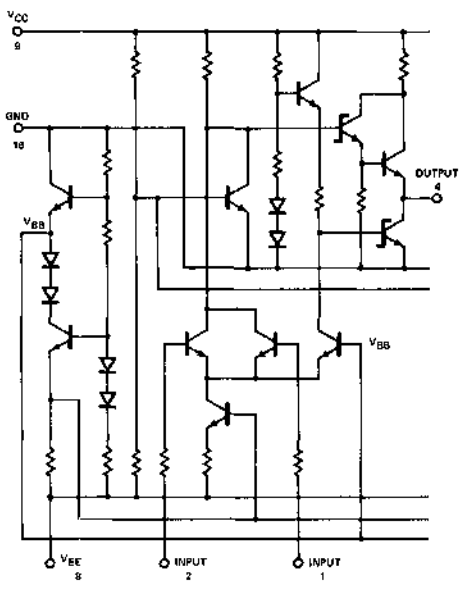
DESCRIPTION

Four level translators for converting ECL signal levels to TTL or DTL logic levels. The 1068 incorporates familiar Schottky "totem pole" outputs to provide high speed operation.

FEATURES

- FAST PROPAGATION DELAY = 5.0 ns TYP
- POWER DISSIPATION = 360 mW/PACKAGE TYP
- SCHOTTKY TTL TOTEM POLE OUTPUTS
- RECOMMENDED POWER SUPPLIES:
  V_{CC} = +5.0 V DC ±5%
  V_{EE} = −5.2 V DC ±5%
- FOUR TRANSLATORS PER PACKAGE

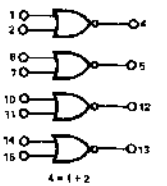
CIRCUIT SCHEMATIC



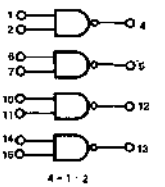
(ONE OF FOUR TRANSLATOR CIRCUITS SHOWN)

LOGIC DIAGRAM AND PIN CONFIGURATION

POSITIVE LOGIC



NEGATIVE LOGIC



Gnd = 16
V_{CC} (+5.0 Vdc) = 9
V_{EE} (−5.2 Vdc) = 8

DC Input Loading Factor = 2.5 (ECL)
DC Output Loading Factor = 10 (TTL)

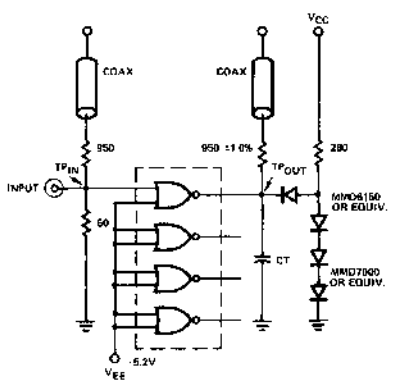
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one translator. The other translators are tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES						
	Volts					mAdc	
	V_{IL} min to V_{IL} max	V_{IH} min to V_{IH} max	V_{IH} max	V_{CC}	V_{EE}	I_{OL}	I_{OH}
0°C	−5.2 to −1.375	−1.045 to −0.740	–	+5.0	−5.2	2	−2.0
1068 +25°C	−5.2 to −1.350	−1.000 to −0.700	−0.700	+5.0	−5.2	20	−2.0
+75°C	−5.2 to −1.285	−0.926 to −0.625	–	+5.0	−5.2	20	−2.0

Characteristic	Symbol	Pin Under Test	N1068 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL} min to V_{IL} max	V_{IH} min to V_{IH} max	V_{IH} max	V_{CC}	V_{EE}	I_{OL}	I_{OH}	Gnd
Positive Supply Drain Current	I_{CCH}	9	–	–	–	60	–	–	mAdc		–	1,2,6,7,10,14,15	9	8	–	–	16
	I_{CCL}	9	–	–	–	45	–	–	mAdc	–	–	–	9	1,2,5,7,8,10,11,14,15	–	–	16
Negative Supply Drain Current	I_E	8	–	–	–	60	–	–	mAdc	–	–	–	–	1,2,6,7,8,10,11,14,15	–	–	16
Input Current	I_{in}	1	–	–	–	250	–	–	µAdc	–	1	–	9	2,6,7,8,10,11,14,15	–	–	16
		2	–	–	–	250	–	–	µAdc	–	2	–	9	1,6,7,8,10,11,14,15	–		16
Input Leakage Current	I_R	1	–	–	–	0.5	–	1.0	µAdc	–	–		9	1,8	–	–	16
		2	–	–	–	0.5	–	1.0	µAdc	–	–	–	9	2,8	–	–	16
Output Voltage High	V_{OH}	4	2.4	–	2.4	–	2.4	–	Vdc	2	–	–	9	8	–	3	16
		4	2.4	–	2.4	–	2.4	–	Vdc	1	–		9	8	–	3	16
Output Voltage Low	V_{OL}	4	–	0.5	–	0.5	–	0.5	Vdc	–	1	–	9	2,6,7,8,10,11,14,15	3	–	16
		4	–	0.5	–	0.5	–	0.5	Vdc	–	2	–	9	1,6,7,8,10,11,14,15	3		16
Output Short Circuit Current	I_{SC}	4	−30	−90	−30	−90	−30	−90	mAdc		–	–	9	1,2,6,7,8,10,11,14,15	–	–	3,16
			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out						
Switching Times	t_{1-4+}	4			5.0				ns	1	4	–	9	2,6,7,8,10,11,14,15	–		16
	t_{1+4-}		–	–		–	–	–		1		–		2,6,7,8,10,11,14,15	–	–	
	t_{2-4+}		–	–		–	–	–		2		–		1,6,7,8,10,11,14,15	–	–	
	t_{2+4-}		–	–		–	–	–		2		–		1,6,7,8,10,11,14,15		–	

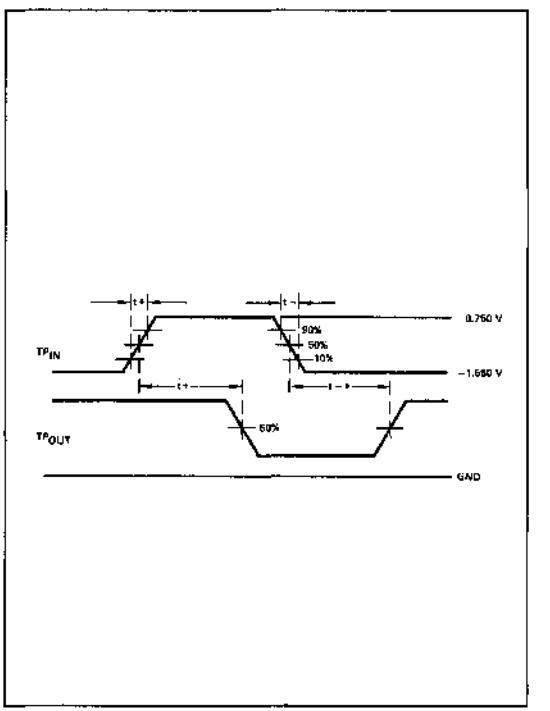
SWITCHING TIME TEST CIRCUIT



INPUT PULSE

t^+, t^- = 2.0 ± 0.2ns

WAVEFORM@ 25°C



The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

ECL 1,000/10,000 SERIES PRODUCT INFORMATION

10,000 SERIES ADVANTAGES

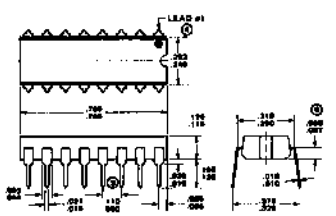
- Best system cost — Performance available in a standard integrated circuit family.
- Factor of 2-or-more — higher system performance than Schottky TTL.
- Complete family of SSI, interface elements, and high performance MSI, with memories coming soon.
- ECL 10,000 Series includes MECL 10,000 equivalents and Signetics-originated 10,000 Series designs.
- Offers designers the logic power of ECL — Open emitter logic, simultaneous complementary outputs, transmission line capability.
- Offers designers system-optimized circuit characteristics — Excellent speed power product, excellent propagation delay/rise time ratio, excellent noise immunity/noise generation ratio, transmission line capability, differential interface capability, and high immunity from power supply variations (±5% recommended, ±10% results in minimal change in system characteristics).
- Compatible with transmission line environment, two-sided printed circuit boards, standard fan cooling techniques. Less support hardware required than Schottky TTL for many system designs.
- Low noise generation capability — Complementary balanced-load outputs, optimized propagation delay/rise time ratio, minimum "1"/"0" power imbalance.
- Directly compatible with MECL III family. Also compatible with ECL II/MECL II family with some reduction in noise immunity at the interface.
- These products contain a temperature compensated internal bias which ensures that the threshold point tracks with the center of the transition region over temperature.

10,000 SERIES TECHNOLOGY

- Signetics thin-epitaxial high performance, high volume production process.
- Advanced circuit design techniques used:
  - Internal Emitter-Dot 'OR' Logic
  - Internal Collector-Dot 'AND' Logic
  - Internal Stacked Series Gating
  - Single Stage Delay Exclusive OR Gates

PACKAGE INFORMATION

B PACKAGE



NOTES:

1. Lead Material: Nickel, tin plated
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash

PACKAGE TYPES

- SSI, MSI and memories will be available in cerdip packages. Signetics new designation F specifies cerdip packages or any number of leads. (Previously E specified 16 lead cerdip).
- Presently SSI, and later some MSI and memories will be available in Signetics' double-encapsulated silicone dip with nickel lead frame. This provides minimum thermal resistance and hence maximum thermal compatibility with cerdip packages.

MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage (V_{CC} = 0)	Note 1	V_{EE}	-8	Vdc
Input Voltage (V_{CC} = 0)	Note 1	V_{IN}	0 to V_{EE}	Vdc
Output Source Current	Note 1	I_o		
Continuous			50	mAdc
Surge			100	mAdc
Storage Temperature Range	Note 1	T_{stg}	-55 to +125	°C
Operating Junction Temperature	Note 1	T_J	125	°C
Operating Temperature Range	Note 2	T_A	-30 to +85	°C
DC Fan-Out (Gates and Flip-Flops)	Notes 2,3	—	70	—
Power Supply Regulation Required	Note 2	—	±10%	—

NOTES:

1. Ratings above which device life may be impaired.
2. Recommended maximum rating above which performance may be degraded.
3. AC fan-out is defined by desired system performance.

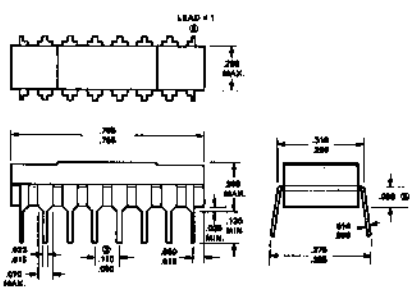
ORDERING INFORMATION

101XX F — Specifies a 10,000 Series product in Cerdip Dual-in-Line package, operating temperature range -30°C to +85°C (intermediate Range). (F is Signetics' new designation for Cerdip).

101XX B — Specifies a 10,000 Series product in 16 pin Silicone Dual-in-Line package, operating temperature range -30°C to +85°C (intermediate Range).

Availability of a device in a particular package is indicated on the appropriate product Data Sheet.

F PACKAGE

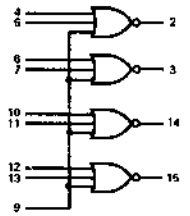


NOTES:

1. Lead Material: Alloy 42 or equivalent, tin plated
2. Body Material: Ceramic with glass seal
3. Tolerances non-cumulative
4. Signetics symbol denotes lead No. 1
5. Lead spacing shall be measured within this zone

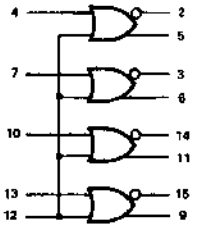
LOGIC DIAGRAMS: BASIC GATES

10100
QUAD 3-INPUT NOR



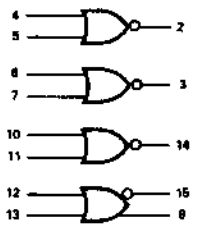
t_{pd} = 2.0 ns TYP.

10101
QUAD OR/NOR



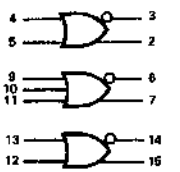
t_{pd} = 2.0 ns TYP.

10102
QUAD 2-INPUT NOR



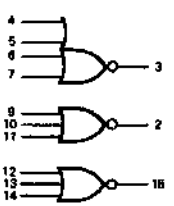
t_{pd} = 2.0 ns TYP.

10105
TRIPLE 2, 3, 2-INPUT OR/NOR



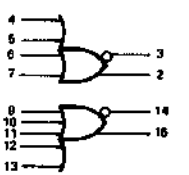
t_{pd} = 2.0 ns TYP.

10106
TRIPLE 4, 3, 3-INPUT NOR



t_{pd} = 2.0 ns TYP.

10109
DUAL 4, 5-INPUT OR/NOR



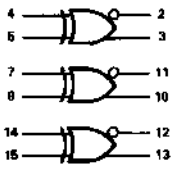
t_{pd} = 2.0 ns TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = "1"

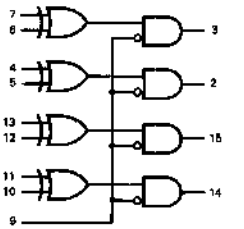
LOGIC DIAGRAMS: COMPLEX GATES

10107
TRIPLE EXCLUSIVE OR/NOR



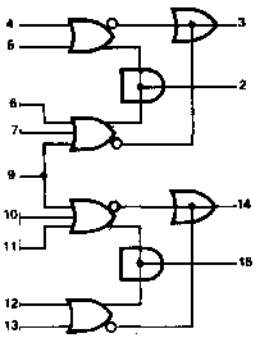
t_{pd} = 2.0, 2.8 ns TYP.

10113
QUAD EXCLUSIVE OR (WITH ENABLE)



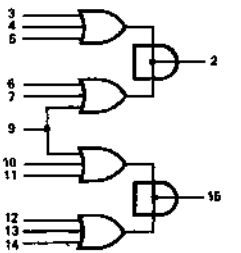
t_{pd} = 2.5 ns TYP.

10117
DUAL 2-WIDE 2, 3-INPUT OA/OAI GATE



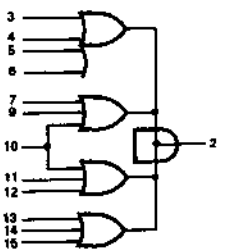
t_{pd} = 2.3 ns TYP.

10118
DUAL 2-WIDE 3-INPUT OR-AND



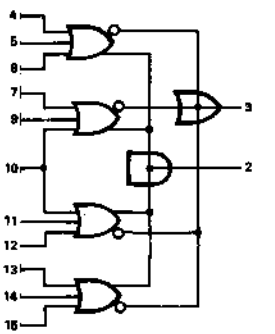
t_{pd} = 2.3 ns TYP.

10119
4-WIDE 4, 3, 3, 3-INPUT OR-AND



t_{pd} = 2.3 ns TYP.

10121
4-WIDE 3, 3, 3, 3-INPUT OA/OAI



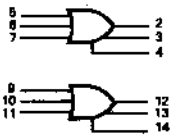
t_{pd} = 2.3 ns TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

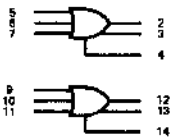
LOGIC DIAGRAMS: MULTIPLE OUTPUT GATES

10110
DUAL 3-INPUT 3-OUTPUT OR



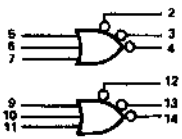
t_{pd} = 2.4 ns TYP. (ALL OUTPUTS LOADED)

10210
DUAL 3-INPUT 3-OUTPUT OR



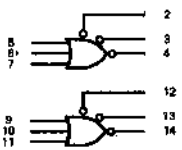
t_{pd} = 1.7 ns TYP. (ALL OUTPUTS LOADED)

10111
DUAL 3-INPUT 3-OUTPUT NOR



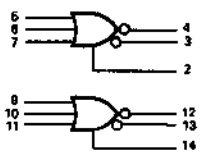
t_{pd} = 2.4 ns TYP. (ALL OUTPUTS LOADED)

10211
DUAL 3-INPUT 3-OUTPUT NOR



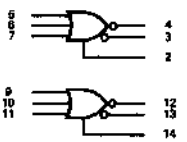
t_{pd} = 1.7 ns TYP. (ALL OUTPUTS LOADED)

10112
DUAL 3-INPUT 2-NOR/1-OR



t_{pd} = 2.4 ns TYP. (ALL OUTPUTS LOADED)

10212
DUAL 3-INPUT 2-NOR/1-OR



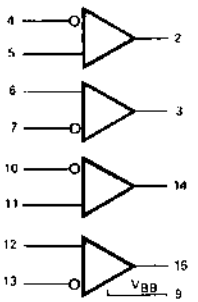
t_{pd} = 1.7 ns TYP. (ALL OUTPUTS LOADED)

NOTES: V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

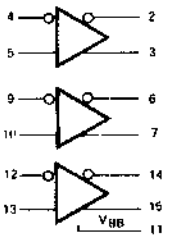
LOGIC DIAGRAMS: INTERFACE CIRCUITS

10115
QUAD DIFFERENTIAL LINE RECEIVER



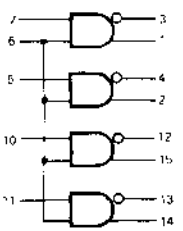
t_{pd} = 2.0 ns TYP.
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10116
TRIPLE DIFFERENTIAL LINE RECEIVER (OR/NOR)



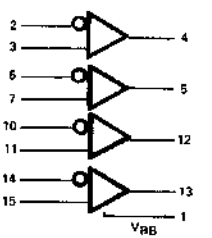
t_{pd} = 2.0 ns TYP.
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10124
QUAD TTL TO-ECL TRANSLATOR



t_{pd} = 5.0 ns TYP.
V_{CC} = 9 GND = 16 V_{EE} = 8

10125
QUAD ECL TO TTL TRANSLATOR (TOTEM-POLE OUTPUTS)

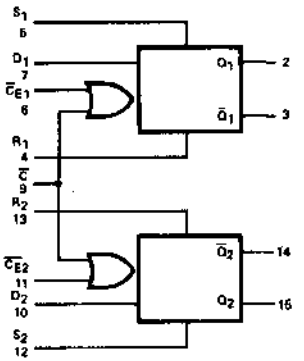


t_{pd} = 5.0 ns TYP.
V_{CC} = 9 GND = 16 V_{EE} = 8

NOTE: POSITIVE LOGIC: HIGH LEVEL = "1"

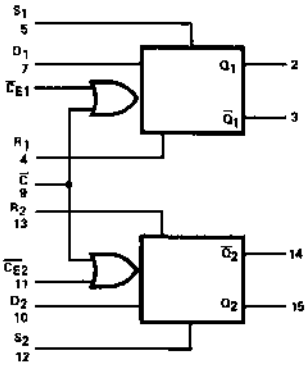
LOGIC DIAGRAMS: DUAL LATCHES AND FLIP-FLOPS

10130
DUAL D-TYPE LATCH



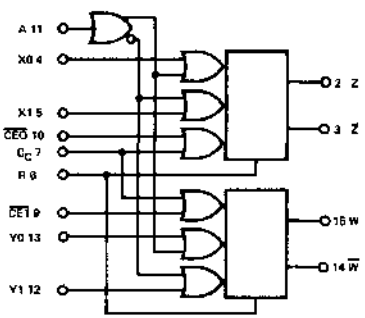
t_{pd} (DATA) = 2.5 ns TYP.
t_{pd} (CLOCK) = 3.0 ns TYP.

10131
DUAL TYPE D MASTER-SLAVE FLIP FLOP



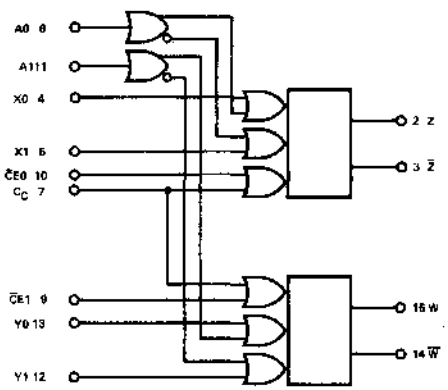
f = 170 MHz TYP.

10132
DUAL MULTIPLEXER-LATCH (WITH RESET)



t_{pd} (DATA) = 2.5 ns TYP.
t_{pd} (CLOCK) = 4.0 ns TYP.

10134
DUAL MULTIPLEXER-LATCH



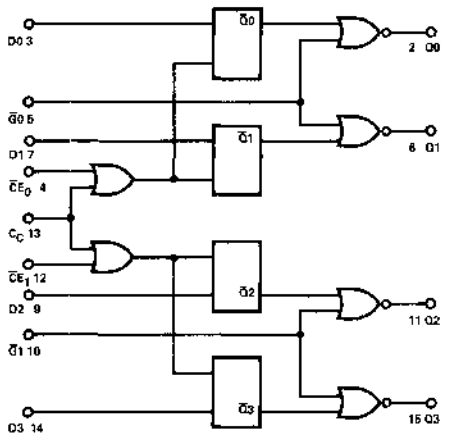
t_{pd} (DATA) = 2.5 ns TYP.
t_{pd} (CLOCK) = 4.0 ns TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

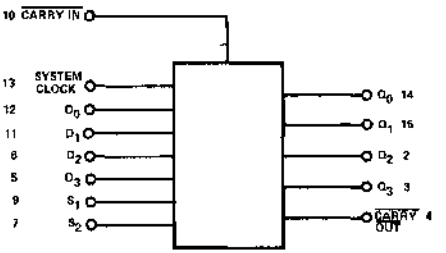
LOGIC DIAGRAMS: MSI: QUAD LATCH, COUNTERS, SHIFT REGISTER

10133
QUAD LATCH
(WITH OUTPUT GATING)

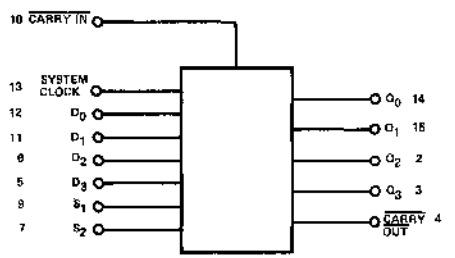


t_{pd} = 4.0 ns TYP.

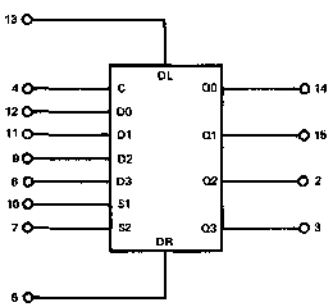
10136
UNIVERSAL HEXADECIMAL COUNTER



10137
UNIVERSAL DECADE COUNTER



10141
FOUR-BIT SHIFT REGISTER



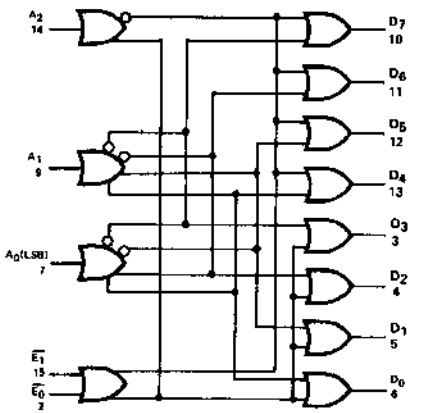
f_{TOG} = 200 MHz TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = "1"

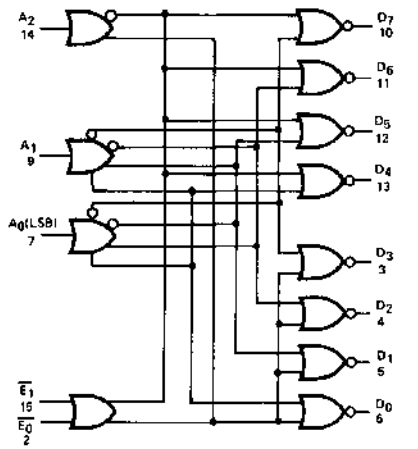
LOGIC DIAGRAMS: MSI DECODERS

10161
1 OF 8 DEMULTIPLEXER/DECODER
(SELECTED OUTPUT IS LOW)



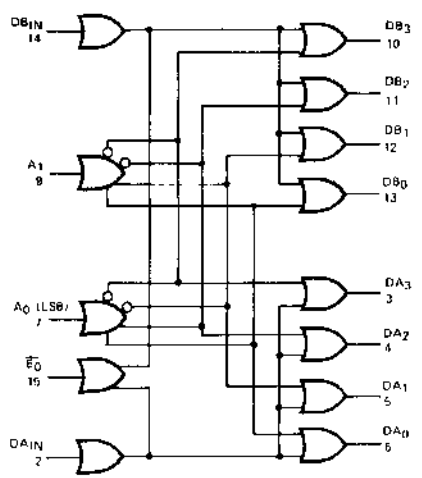
t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

10162
1 OF 8 DEMULTIPLEXER/DECODER
(SELECTED OUTPUT IS HIGH)



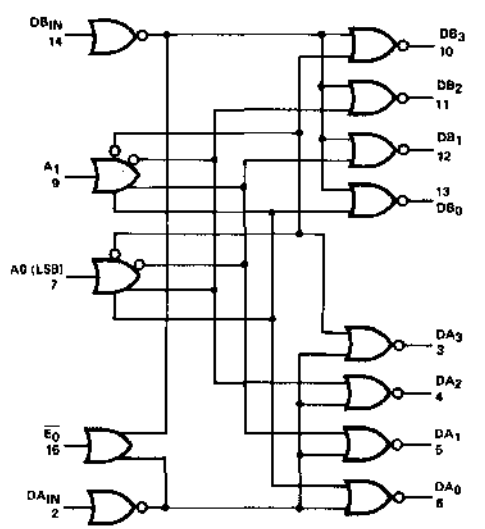
t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

10171
DUAL 1 OF 4 DEMULTIPLEXER/DECODER
(SELECTED OUTPUTS LOW)



t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

10172
DUAL 1 OF 4 DEMULTIPLEXER/DECODER
(SELECTED OUTPUTS HIGH)



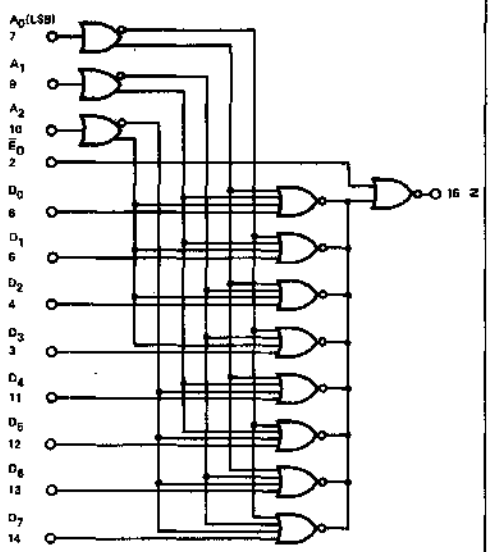
t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

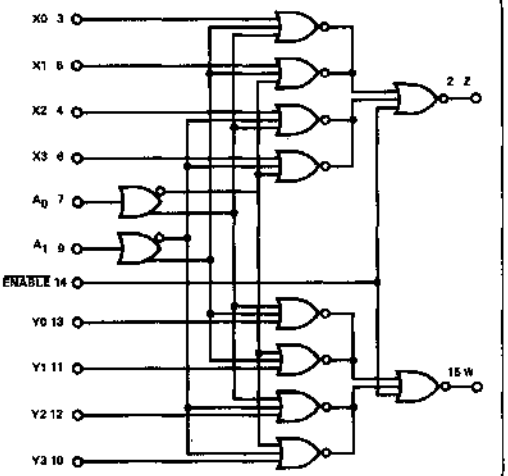
LOGIC DIAGRAMS: MSI: MULTIPLEXERS, QUAD MULTIPLEXER-LATCH

10164
8 TO 1 MULTIPLEXER



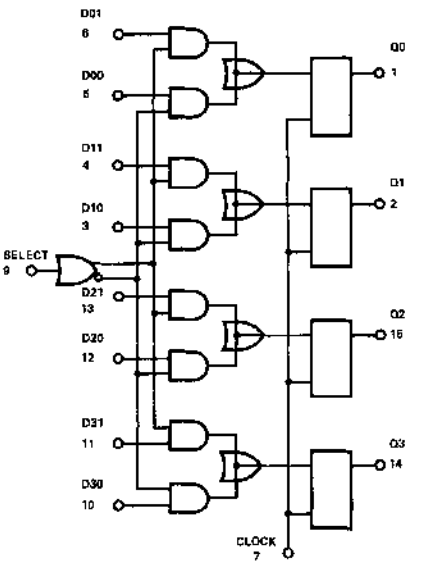
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10174
DUAL 4 TO 1 MULTIPLEXER



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10173
QUAD MULTIPLEXER-LATCH



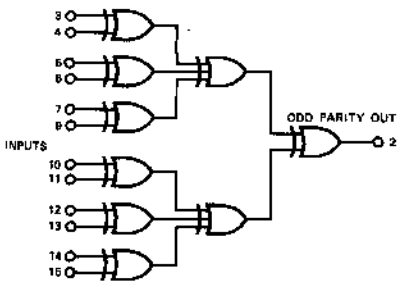
V_{CC1} = V_{CC2} = 16, V_{EE} = 8

NOTE: POSITIVE LOGIC: HIGH LEVEL = '1'

LOGIC DIAGRAMS: MSI: PARITY AND ALU FUNCTIONS

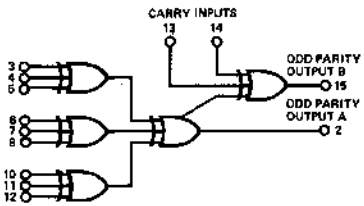
TO BE ANNOUNCED

10160
12-BIT PARITY CIRCUIT



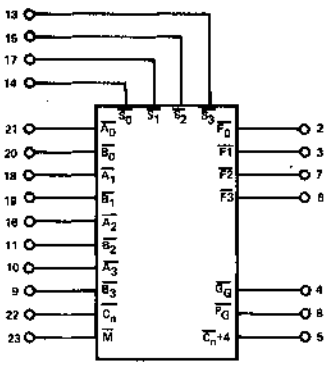
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10170
9 + 2 PARITY CIRCUIT



t_{pd} (OUTPUT A) = 4.0 ns TYP.
t_{pd} (OUTPUT B) = 6.0 ns TYP.
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10181
4-BIT ARITHMETIC UNIT (16 ARITHMETIC FUNCTIONS AND 16 LOGICAL OPERATIONS)



t_{pd} = 7.0nS ($\overline{A}$ TO $\overline{F}$)
t_{pd} = 5.0 ns ($\overline{A}$ TO $\overline{Cn+4}$)
V_{CC1} = 1, V_{CC2} = 24, V_{EE} = 12

NOTE: POSITIVE LOGIC: HIGH LEVEL = '1'

signetics

QUAD 3-INPUT NOR GATE | 10100

10100B,F: −30 to +85°C

ADVANCED INFORMATION

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10100 is a high speed Quad 3-Input NOR Gate. All inputs are terminated with a 50K ohm resistor to V_{EE} which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10100 is optimized for high performance logic applications. This gate meets the ECL 10,000 Series standard voltage current and rise and fall time specifications.

FEATURES

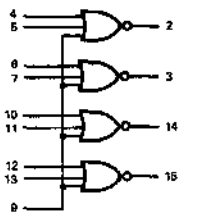
- FAST PROPAGATION DELAY = 2.0ns TYPICAL
- LOW POWER DISSIPATION = 100mW/PACKAGE – (NO LOAD)
- HIGH FANOUT CAPABILITY
  - CAN DRIVE FOUR 50 OHM LINES
  - DC OUTPUT LOADING FACTOR OF 90X4
- HIGH Z INPUTS – DC LOADING FACTOR OF 1
- INTERNAL 50K OHM PULLDOWN RESISTORS
- OUTPUT RISE AND FALL TIMES
  - 3.5ns TYPICAL (10% TO 90%)
  - 2.0ns TYPICAL (20% TO 80%)
- SEPARATE OUTPUT EMITTER FOLLOWER V_{CC} PIN – NEGLIGIBLE COUPLING
- HIGH NOISE IMMUNITY/NOISE GENERATION RATIO
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = 5.2V ± 5% RECOMMENDED
- MINIMUM CHANGE IN SYSTEM CHARACTERISTICS OCCURS WITHIN ± 10% V_{EE}
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

ELECTRICAL CHARACTERISTICS

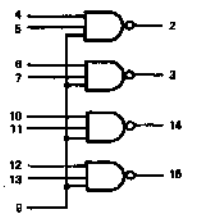
Conditions:	T_A = 25°C, V_{EE} = −5.2V ± 1%
1. I_E	= 20mA dc typical = 26mA dc max.
2. I_{inH}	= 265μA dc max. = 550μA dc max. (Pin 9)
Conditions:	T_A = 25°C, V_{CC} = +2.0V ± 1%, V_{EE} = −3.2V ± 1%, 50 ohm loads
3. t_{pd}	= 2.0ns typical (t+−, t−+)
4. t_r, t_f	= 2.0ns typical (20% to 80%)

LOGIC DIAGRAM

10100



Positive Logic: High Level = '1'



Negative Logic: Low Level = '1'

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

TEMPERATURE RANGE

- −30 to +85° C Operating Ambient

RECOMMENDED OPERATING VOLTAGE

- V_{CC1} = V_{CC2} = GND, V_{EE} = 5.2V ± 5%

PACKAGE TYPES

- B: 16 pin Silicone Dip
- F: 16 pin Cerdip

signetics

QUAD 2-INPUT OR/NOR GATE (COMPLEMENTARY OUTPUTS) 10101

10101F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10101 is a high speed 2-input OR/NOR quad gate with complementary outputs. The 10101 is particularly useful as a quad differential line driver.

Each gate has one input connected to pin 12. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10101 is optimized for high performance logic applications. This gate meets the ECL 10,000 Series standard voltage, current and rise and fall time specifications.

FEATURES

- FAST PROPAGATION DELAY = 20 ns TYP
- COMPLEMENTARY OR/NOR OUTPUTS — EXCELLENT FOR DRIVING TWISTED PAIRS
- COMMON INPUT FOR GATING
- LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY — CAN DRIVE 50 ohm LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

TEMPERATURE RANGE

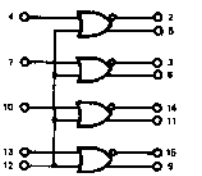
- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16 Pin CERDIP

LOGIC DIAGRAM

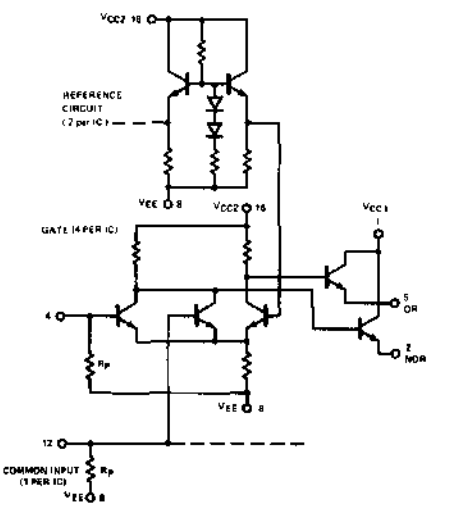
10101



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

CIRCUIT SCHEMATIC

10101



All R_P = 50 kΩ

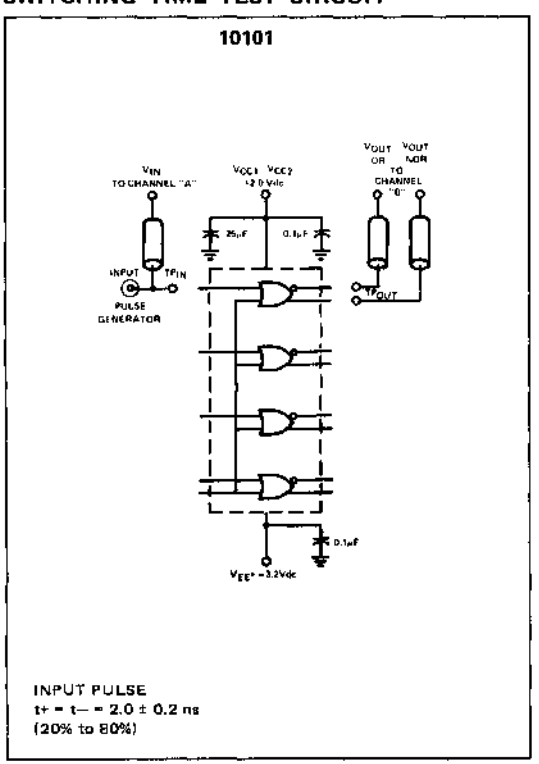
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.880	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10101 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	29	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
		12	–	–	–	–	550	–	–	μAdc	12	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
		12	–	–	0.5	–	–	–	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	5	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	12	–	–	–	8	1,16
		5	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4	–	–	–		
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	12	–	–		
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	4	–	–		
Logic "0" Output Voltage	V_{OL}	5	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	12	–	–		
		5	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	4	–	–		
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	12	–	–	–		
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	5	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	12	–	8	1,16
		5	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	4	–		
		2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	12		
		2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	4		
Logic "0" Threshold Voltage	V_{OLA}	5	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	12	8	1,16
		5	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	4		
		2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	12	–		
		2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	4	–		
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2+}	2									–	–		2		
	t_{4+5+}	5									–	–		5		
	t_{4-5-}	5									–	–		5		
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–		2		
	t_{5+}	5									–	–		5		
Fall Time (20% to 80%)	t_{2-}	2									–	–		2		
	t_{5-}	5									–	–		5		

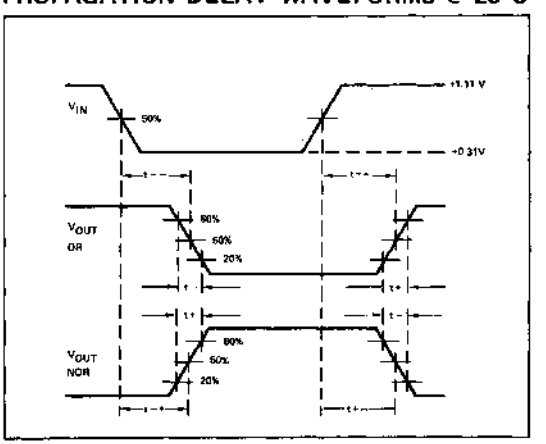
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

QUAD 2-INPUT NOR GATE | 10102

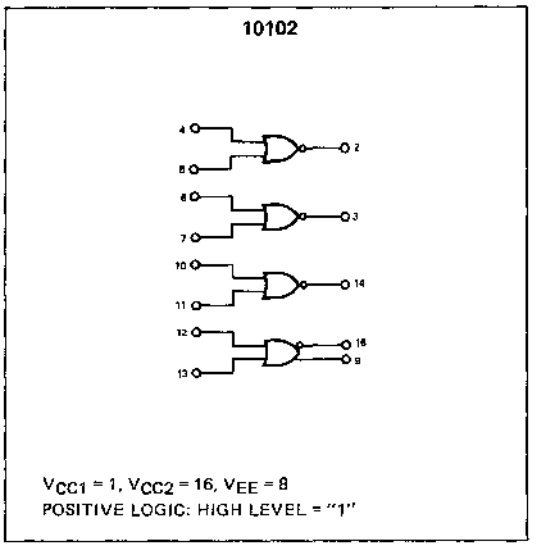
10102B,F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

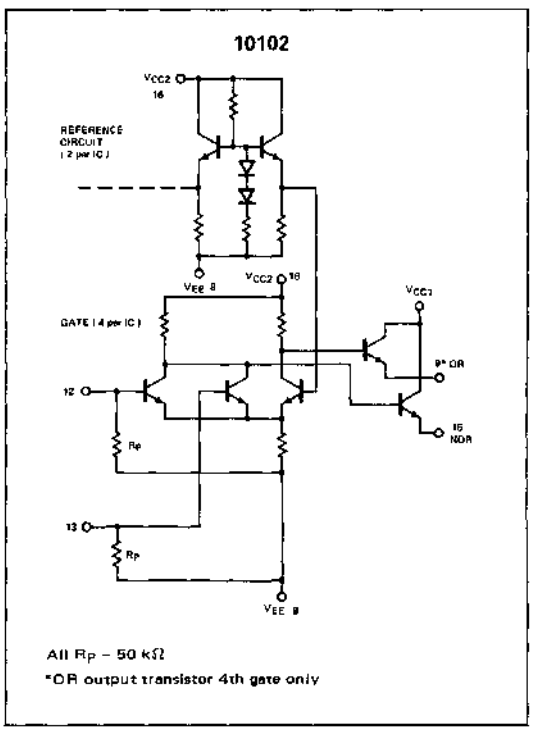
The 10102 is a high speed quad 2-input NOR gate. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10102 is optimized for high performance logic applications. This gate meets the ECL 10,000 Series standard voltage current and rise and fall time specifications.

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

CIRCUIT SCHEMATIC



All Rp – 50 kΩ
*OR output transistor 4th gate only

FEATURES

- **FAST PROPAGATION DELAY = 2.0 ns TYP**
- **LOW POWER DISSIPATION = 100 mW/PACKAGE (NO LOAD)**
- **HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES**
- **HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED**
- **OPEN EMITTER LOGIC AND BUSSING CAPABILITY**

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

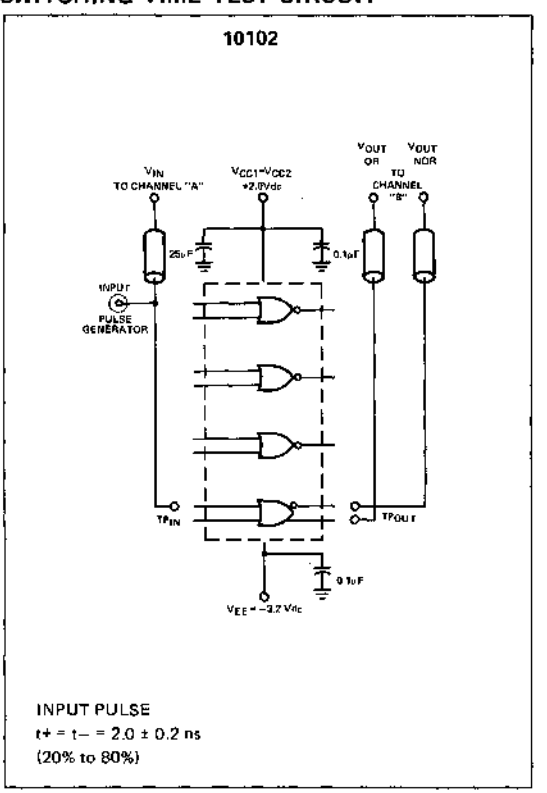
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10102 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC1} and Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	–	265	–	–	µAdc	12	–	–	–	8	1,16
	I_{inL}	12	–	–	0.5	–	–	–	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	12	–	–	–	8	1,16
		9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		13	–	–	–		
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		–	12	–	–		
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		–	13		–		
Logic "0" Output Voltage	V_{OL}	9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	12	–	–	8	1,16
		9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		–	13	"	"		
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		12	–	–	–		
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		13	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	9	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	12	–	8	1,16
		9	−1.080		−0.980	–	–	−0.910	–		–	–	13	–		
		15	−1.080	–	−0.980	–	–	−0.910	–		–	–	–	12		
		15	−1.080	–	−0.980	–	–	−0.910	–		–	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	9	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	12	8	1,16
		9	–	−1.655	–	–	−1.630	–	−1.595		–	–	–	13		
		15	–	−1.655	–	–	−1.630	–	−1.595		–	–	12	–		
		15	–	−1.655	–	–	−1.630	–	−1.595		–	–	13	–		
Switching Times* (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{12+\ 15-}$	15	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	15	8	1,16
	$t_{12-\ 15+}$	15									–	–		15		
	$t_{12+\ 9+}$	9									–	–		9		
	$t_{12-\ 9-}$	9												9		
Rise Time (20% to 80%)	t_{15+}	15	1.1	3.6	1.1		3.3	1.1	3.7		–	–		15		
	t_{9-}	9									–	–		9		
Fall Time (20% to 90%)	t_{15-}	15									–	–		15		
	t_{9-}	9									–	–		9		

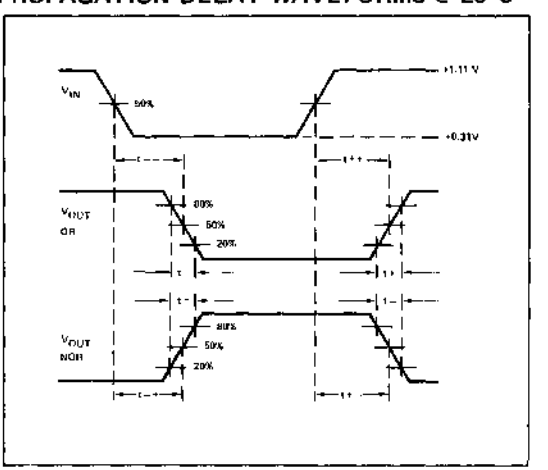
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

TRIPLE 2-3-2 OR/NOR GATE | 10105

10105B,F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10105 package contains one 3 input OR/NOR gate, and two 2 input OR/NOR gates. The 10105 is optimized for high performance logic applications. Each gate has an excellent speed power product of 50 picojoules. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment. This gate meets the ECL 10,000 Series standard voltage, current, and rise and fall time specifications.

Complementary outputs make the 10105 particularly useful for differential line driving.

FEATURES

- **FAST PROPAGATION DELAY = 2.0 ns TYP**
- **POWER DISSIPATION = 75 mW/PACKAGE TYP (NO LOAD)**
- **VERY HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES**
- **HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED**
- **COMPLEMENTARY OR/NOR OUTPUTS**
- **OPEN EMITTER LOGIC AND BUSSING CAPABILITY**

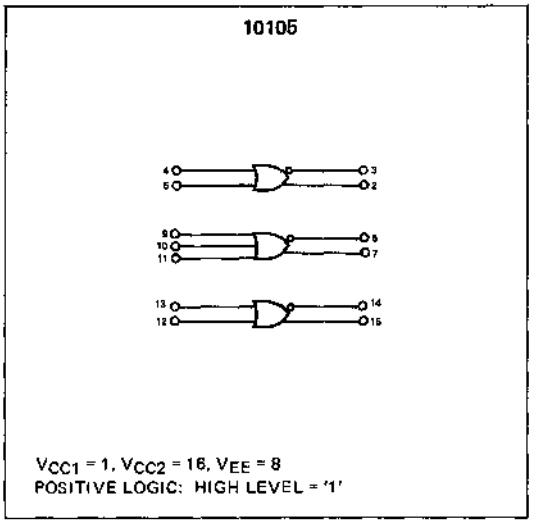
TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

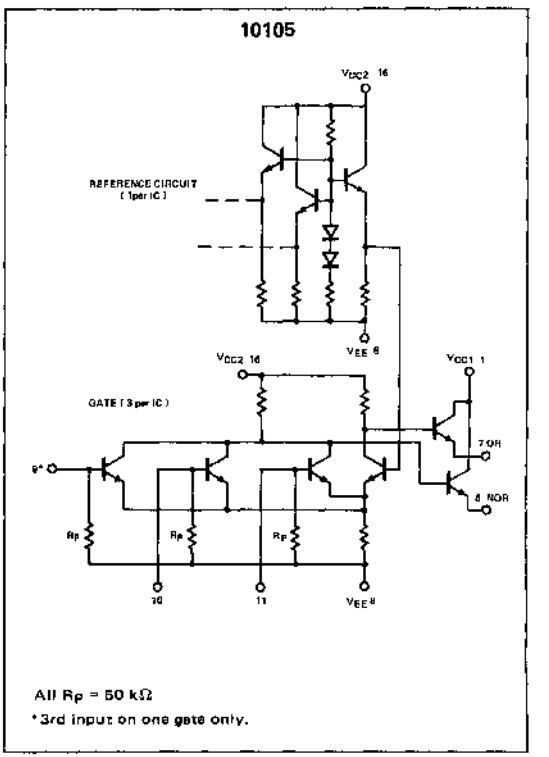
B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

CIRCUIT SCHEMATIC



All R_P = 50 kΩ
*3rd input on one gate only.

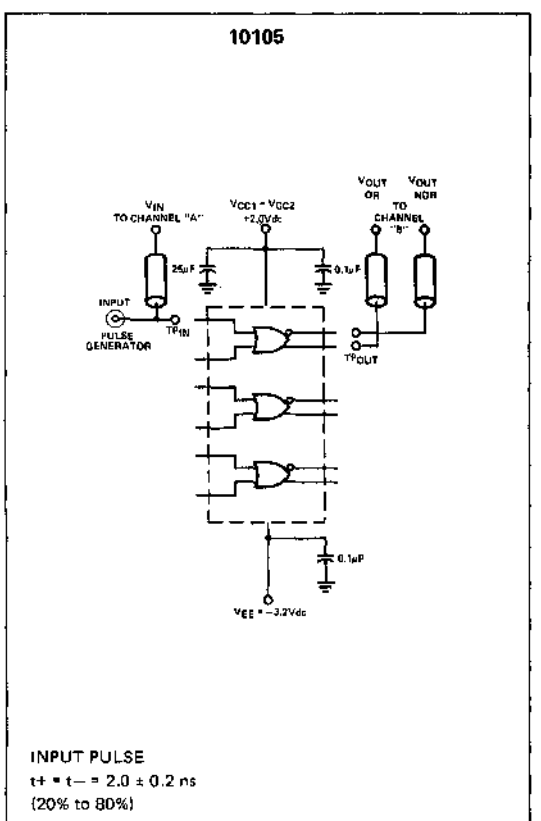
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10105 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	16	21	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	266	–		µAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	−1.060	−0.890	−0.980	–	−0.810	−0.890	−0.700	Vdc	–	4	–	–	8	1,16
		2	−1.060	−0.890	−0.980	–	−0.810	−0.890	−0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	–	–	–	8	1,16
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	4	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	4	8	1,16
		2	−1.060	–	−0.980	–	–	−0.910	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655		–	−1.630		−1.595	Vdc	–	–	4		8	*1,16
		2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	4	8	1,16
Switching Times* (50-ohm load)													Pulse In	Pulse Out	−5.2 V	+2.0 V
Propagation Delay	$t_{4+\ 3-}$	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	$t_{4-\ 3+}$	3									–	–		3		
	$t_{4+\ 2+}$	2									–	–		6		
	$t_{4-\ 2-}$	2												6		
Rise Time (20% to 80%)	t_{3+}	3	1.1	3.6	1.1		3.3	1.1	3.7		–	–		3		
	t_{2+}	2									–	–		6		
Fall Time (20% to 80%)	t_{3-}	3									–	–		3		
	t_{2-}	2									–	–		6		

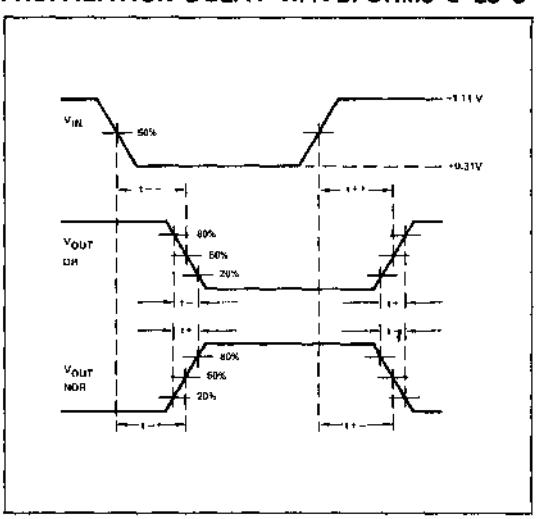
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DESCRIPTION

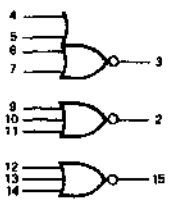
The 10106 package contains one 4 input NOR gate and two 3 input NOR gates. The 10106 is optimized for high performance logic applications. The gate has an excellent speed power product of 50 picojoules. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment. This gate meets the ECL 10,000 Series standard voltage, current and rise and fall time specifications.

FEATURES

- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 75 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY — CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

LOGIC DIAGRAM

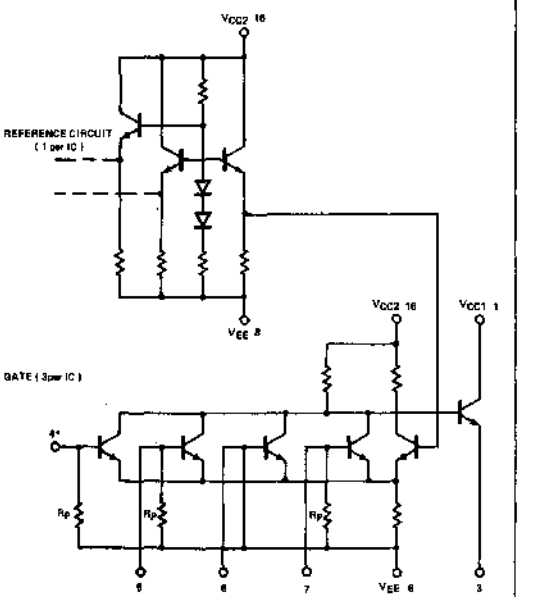
10106



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

CIRCUIT SCHEMATIC

10106



All Rp = 50 kΩ.
*4th input on one gate only.

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

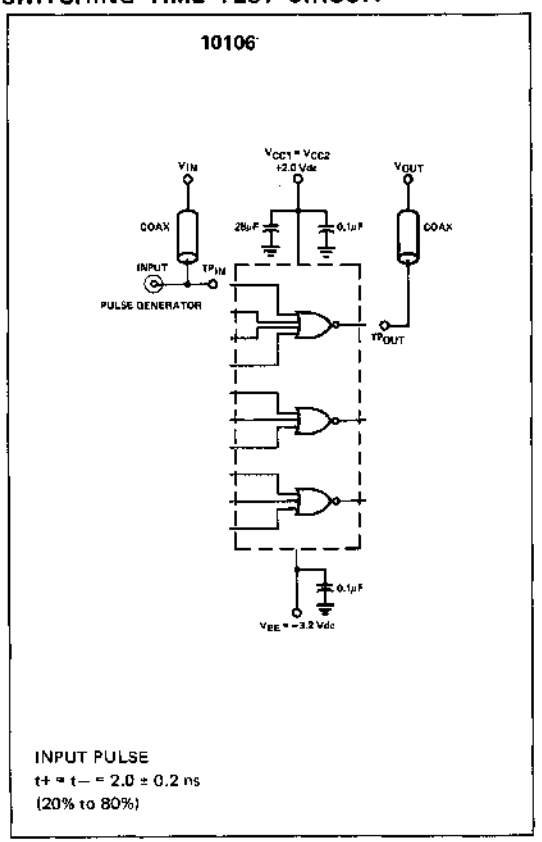
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

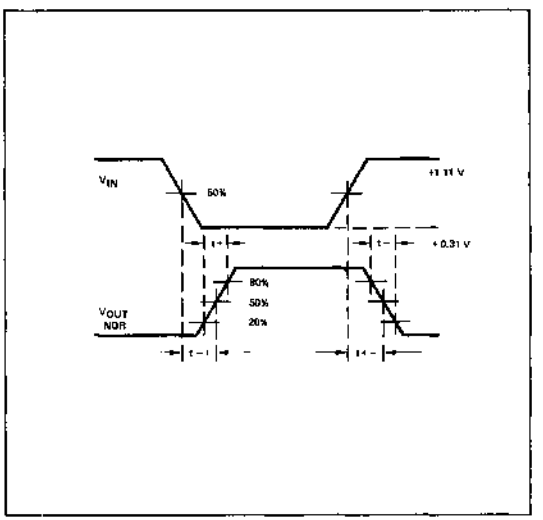
Characteristic	Symbol	Pin Under Test	10106 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8	–	–	–	16	21	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	µAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	4	–	–	8	1,16
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		–	9	–	–	–	–
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	–		–	8	1,16
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		9	–	–	–	–	–
Logic "1" Threshold Voltage	V_{OHA}	3	−1.080	–	−0.960	–	–	−0.910	–	Vdc	–	–	–	4	8	1,16
		2	−1.080	–	−0.980	–	–	−0.910	–	–	–	–	–	9	–	–
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.658	–	–	−1.630	–	−1.595	Vdc	–	–	4	–	8	1,16
		2	–	−1.665	–	–	−1.630	–	−1.595			–	9	–	–	–
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{+} 3−	3	1.0	3.1	1.0	2.0	2.9	1.0	3.2	ns			4	3	8	1,16
	t_{-} 3+	1	1.0	3.1	1.0	↓	2.9	1.0	3.3		–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t_{3+}	↓	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	↓	↓	↓
Fall Time (20% to 80%)	t_{3-}	↓	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	↓	↓	↓

*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

TRIPLE EXCLUSIVE OR/NOR GATE | 10107

10107B,F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

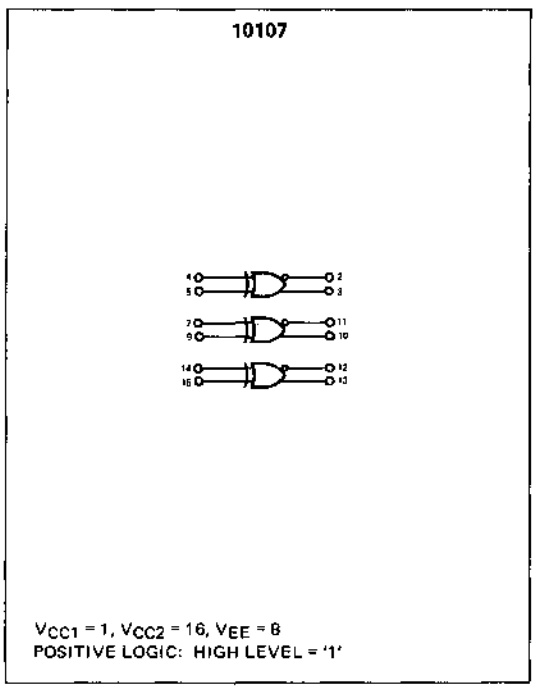
DESCRIPTION

The 10107 is a triple high speed 2-input Exclusive OR/Exclusive NOR gate. The 10107 is optimized for high speed comparator and parity functions, and has an excellent speed power product for this function. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout are ideal for a transmission line environment. The 10107 contains a temperature tracking internal bias which insures that the threshold point remains in the center of the transition region over temperature. The 10107 has complementary outputs.

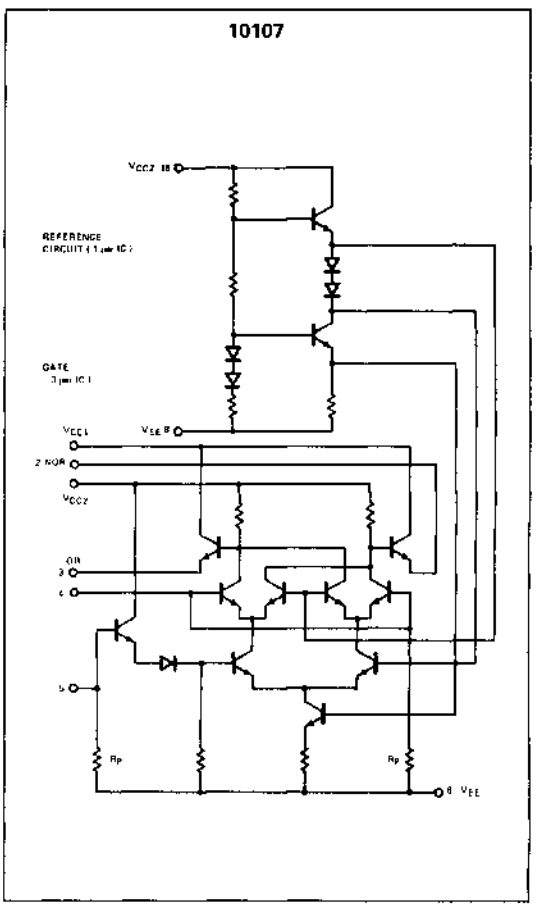
FEATURES

- FAST PROPAGATION DELAY
  - 2.0 ns TYP (INPUTS 4, 9, 14)
  - 2.8 ns TYP (INPUTS 5, 7, 15)
- LOW POWER DISSIPATION = 115 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY
  - CAN DRIVE SIX 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- COMPLEMENTARY OR/NOR OUTPUTS
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

LOGIC DIAGRAM



CIRCUIT SCHEMATIC



TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS

(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

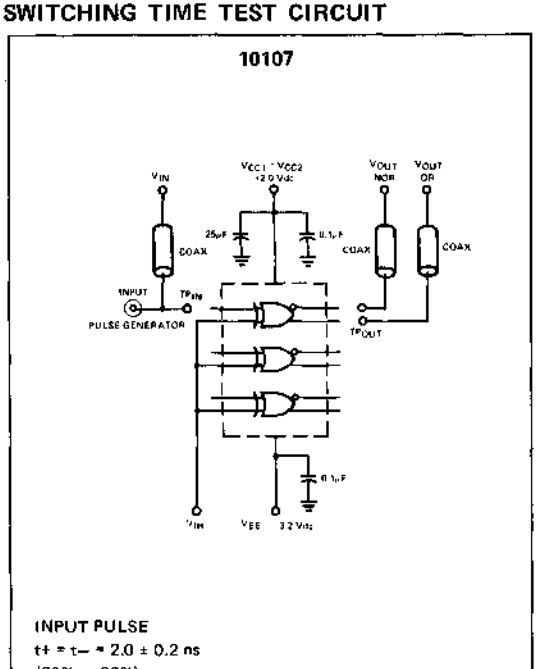
Characteristic	Symbol	Pin Under Test	10107 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	All Inputs	–	–	–	8	1,16
	I_{inH}	4,9,14	–	–	–	265	–		µAdc	*	–	–	–	8	1,16
		5,7,15	–	–	–	220	–	–	µAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	4,5	–	–	–	8	1,16
		2	1.060	−0.890	−0.960	−0.810	−0.890	−0.700		–	4,5	–	–		
		3	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700		4	5	–	–		
		3	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700		5	4	–	–		
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	4	5	–	–	8	1,16
		2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615		5	4	–	–		
		3	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615		4,5	–	–	–		
		3	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615		–	4,5	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980		−0.910	–	Vdc	5	–	4	–	8	1,16
		2	−1.080	–	−0.980	–	−0.910	–		–	–	–	4		
		3	−1.080	–	−0.980	–	−0.910	–		–	–	4	–		
		3	−1.080	–	−0.980	–	−0.910	–		–	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	−1.630	–	−1.595	Vdc	–	–	4	–	8	1,16
		2	–	−1.655	–	−1.630	–	−1.595		–	–	5			
		3	–	−1.655	–	−1.630	–	−1.595		5	–	4	–		
		3	–	−1.655	–	−1.630	–	−1.595		–	–	–	4		
Switching Times† (50-ohm load)					Min	Typ	Max		Unit	+1.1 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t++	Inputs	1.0	3.8	1.1	2.0	3.7	1.1	4.0	ns	9,7,15	–	Input	Corresponding	8	1,16
	t+−	4,9,or 14										–	4,9, or	Ex-OR/Ex-NOR		
	t−+	to either										–	14	Outputs		
	t−−	Output										–				
	t++	Inputs				2.8					4,9,14	–	Input	Corresponding		
	t+−	5,7, or 15										–	5,7, or	Ex-OR/Ex-NOR		
	t−+	to either										–	15	Outputs		
	t−−	Output										–				
Rise Time (20% to 80%)	t+	**	1.1	3.5		2.5	3.5		3.8		4,9,14	–	Any Input	Corresponding Ex-OR/Ex-NOR Outputs		
Fall Time (20% to 80%)	t−	**	1.1	3.5		2.5	3.5		3.8		4,9,14	–	Any Input			

*Individually test each input applying V_{IH} or V_{IL} to input under test.

**Any Output

†Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT

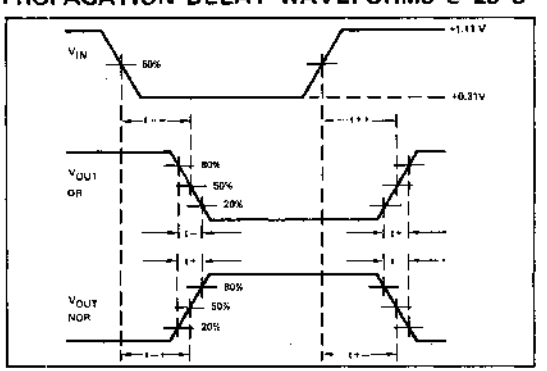


INPUT PULSE

t+ = t− = 2.0 ± 0.2 ns

(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

DUAL 4-5 INPUT OR/NOR GATE | 10109

10109B,F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

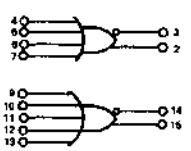
The 10109 is a high speed 4-input OR/NOR and 5-input OR/NOR dual gate. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10109 is optimized for high performance logic applications. The 10109 has complementary outputs.

FEATURES

- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 50 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- COMPLEMENTARY OR/NOR OUTPUTS
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

LOGIC DIAGRAM

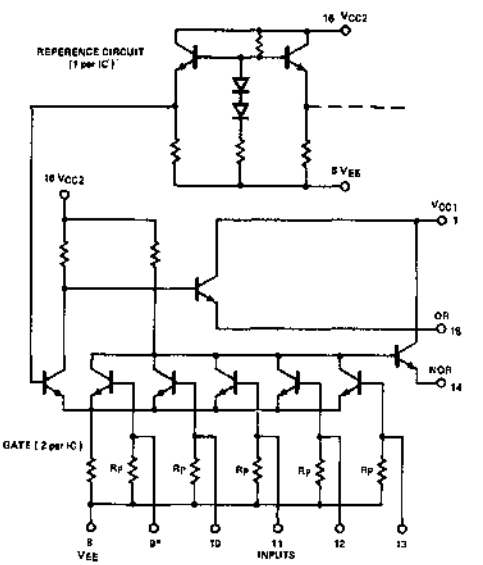
10109



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

CIRCUIT SCHEMATIC

10109



All RP = 50 kΩ.
*5th input on one gate only.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

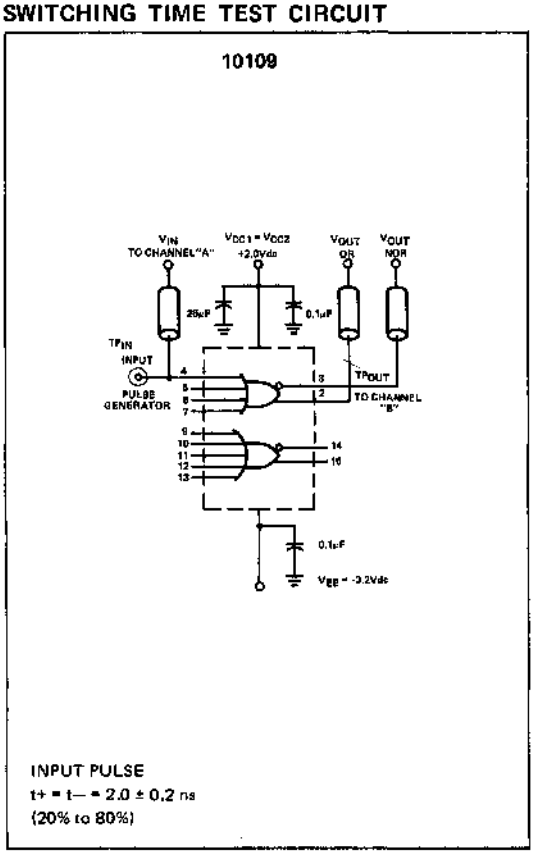
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10109 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8		–	–	10	14	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
High Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4	–	–	–	8	1,16
		3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	4	–	–	8	1,16
Low Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	4	–	–	8	1,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	–	–	–	8	1,16
High Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	4	–	8	1,16
		3	−1.060	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	4	8	1,16
		3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	4	–	8	1,16
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−5.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2+}	2									–	–		2		
	t_{4+3-}	3									–	–		3		
	t_{4-3+}	3									–	–		3		
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.8	1.1		3.3	1.1	3.7		–	–		2		
	t_{3-}	3									–	–		3		
Fall Time (20% to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		

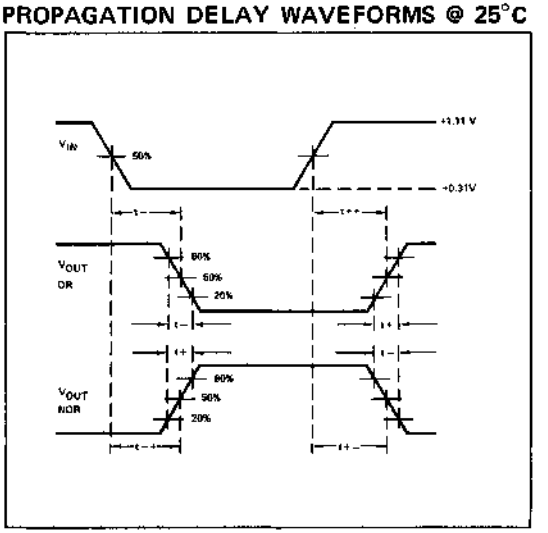
* Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

DUAL 3-INPUT 3-OUTPUT OR GATE | 10110

10110B,F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10110 is a dual high speed 3-input 3-output OR gate. The 10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three paraltel lines from a single point makes the 10110 particularly useful in clock distribution applications where minimum clock skew is desired.

FEATURES

- FAST PROPAGATION DELAY = 2.4 ns TYP (ALL OUTPUTS LOADED)
- POWER DISSIPATION = 150 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY — CAN DRIVE SIX 50 Ω LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

TEMPERATURE RANGE

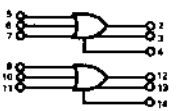
- −30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

LOGIC DIAGRAM

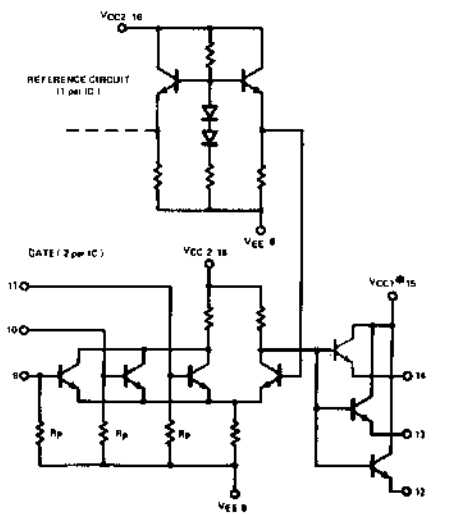
10110



V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

CIRCUIT SCHEMATIC

10110



All Rp = 50 kΩ.
*V_{CC1} for other gate is pin 7.

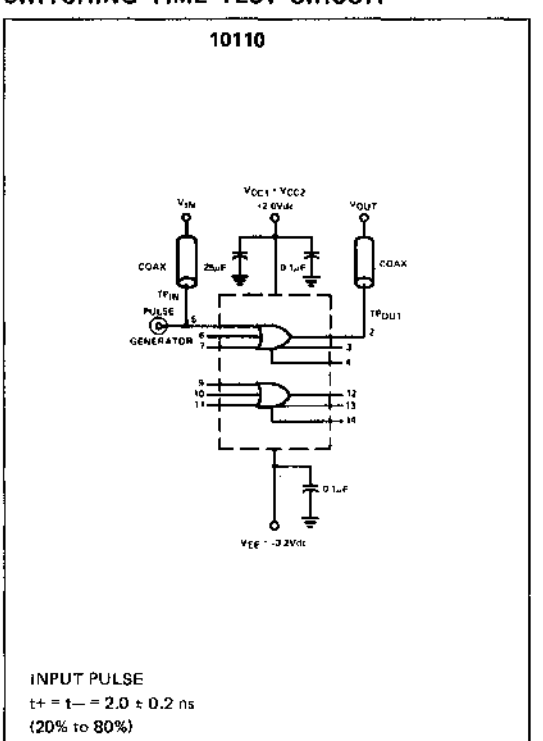
ELECTRICAL CHARACTERISTICS
(At Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10110 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	425	–	–	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	–	–	–	8	1,15,16
		3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	6	–	–	–	8	1,15,16
		4	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc	–	5	–	–	8	1,15,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	6	–	–	8	1,15,16
		4	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	7	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times ** (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t5+ 2+	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t5− 2−	2										–		2		
	t6+ 3+	3									–	–		3		
	t6− 3−	3									–			3		
	t6+ 4+	4									–	–		4		
	t6− 4−	4									–			4		
Rise Time (20% to 80%)	t2+	2	1.0		1.1	2.2		1.2			–	–		2		
	t3+	3									–	–		3		
	t4+	4									–	–		4		
Fall Time (20% to 80%)	t2−	2									–	–		2		
	t3−	3									–	–		3		
	t4−	4									–	–		4		

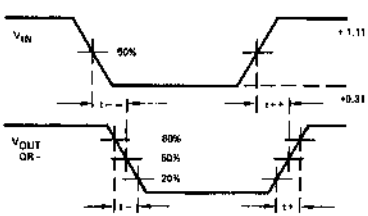
*Individually test each input using the pin connections shown.
**Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DESCRIPTION

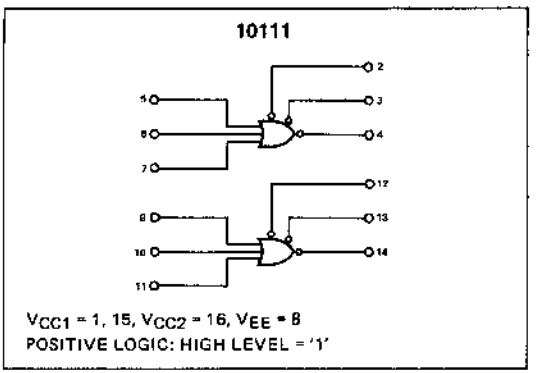
The 10111 is a dual high speed 3-input 3-output NOR gate. The 10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the 10111 particularly useful in clock distribution applications where minimum clock skew is desired.

FEATURES

- FAST PROPAGATION DELAY = 2.4 ns TYP (ALL OUTPUTS LOADED)
- POWER DISSIPATION = 150 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY – CAN DRIVE SIX 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

LOGIC DIAGRAM



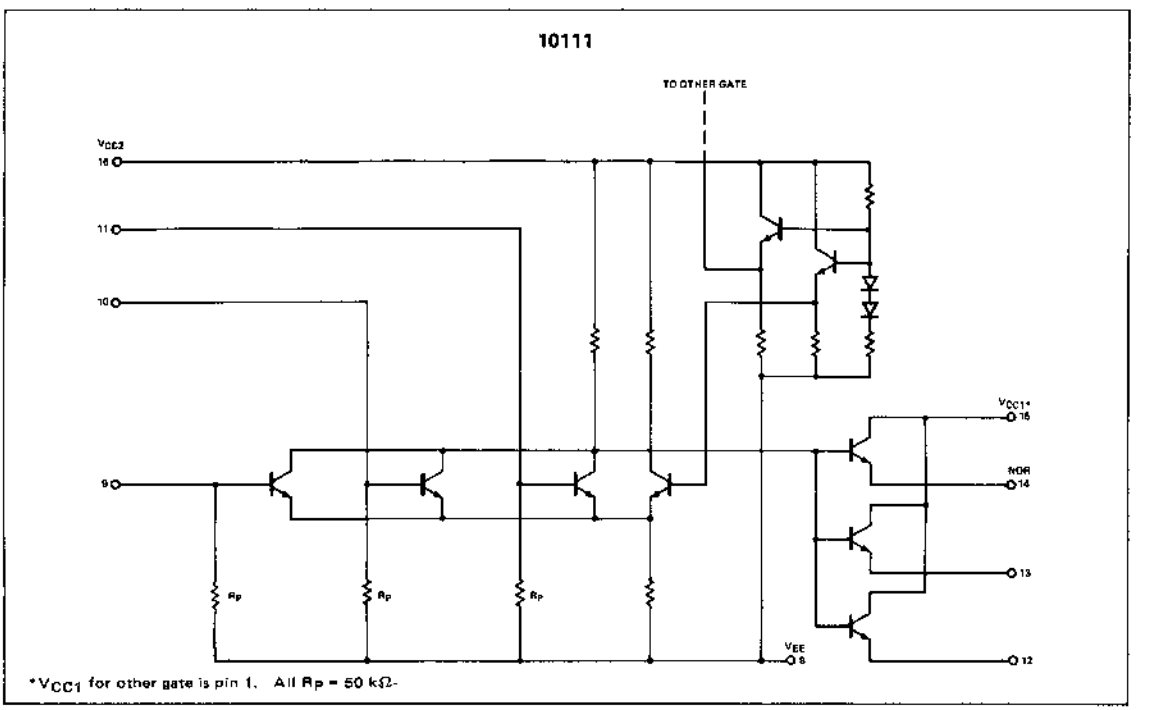
TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

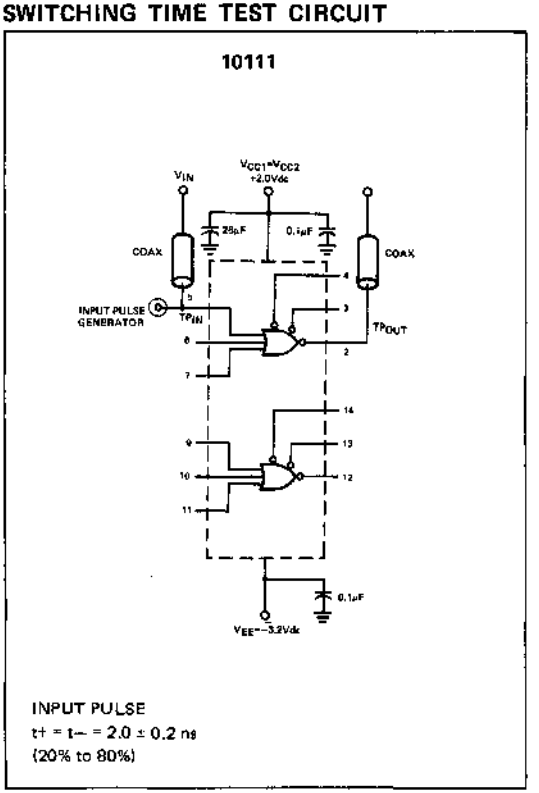
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10111 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1,15,16
	I_{inH}	5,6,7	–	–	–	–	435	–	–	μAdc	*	*	*	*	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	*	*	*	*	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	6	–	–	8	1,15,16
		3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	6	–	–	8	1,15,16
		4	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	7	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5	–	–	–	8	1,15,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	6	–	–	–	8	1,15,16
		4	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.060	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	−1.060	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	−1.060	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times ** (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{5+\ 2-}$	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	$t_{6-\ 2+}$	2									–	–		2		
	$t_{6+\ 3-}$	3									–	–		3		
	$t_{5-\ 3+}$	3									–	–		3		
	$t_{6-\ 4+}$	4									–	–		4		
	$t_{6+\ 4-}$	4									–	–		4		
Rise Time (20% to 80%)	t_{2+}	2	1.0		1.1	2.2	3.5	1.2	3.8		–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20% to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

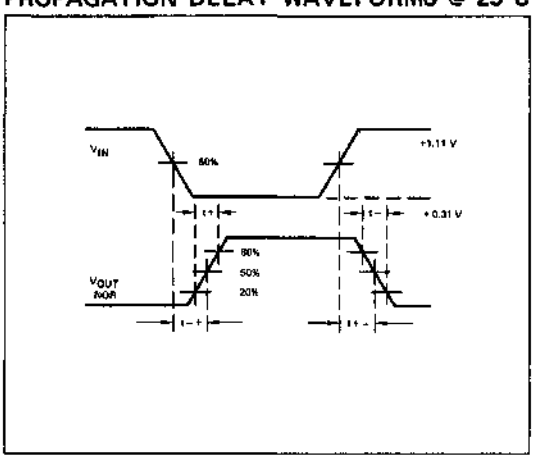
*Individually test each input using the pin connections shown.
**Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t+ = t- = 2.0 \pm 0.2$ ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

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DUAL 3-INPUT 1 OR/2 NOR OUTPUT GATE 10112

10112B,F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

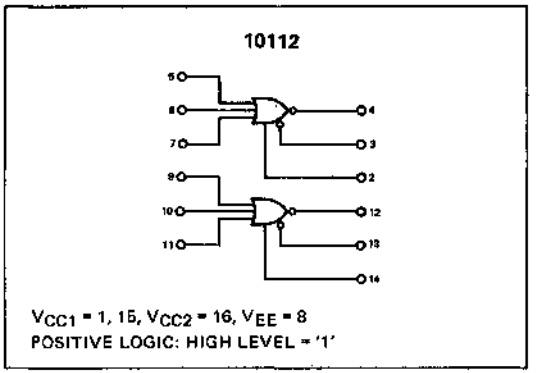
The 10112 is a dual high speed 3-input 1 OR/2 NOR output gate. The 10112 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the 10112 particularly useful in clock distribution applications where minimum clock skew is desired. The 10112 is suitable for use in memory chip select decoding. The 10112 is particularly useful as a clock amplifier on a board using clock signals of both polarities.

FEATURES

- FAST PROPAGATION DELAY = 2.4 ns TYP (ALL OUTPUTS LOADED)
- POWER DISSIPATION = 150 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY — CAN DRIVE SIX 50 Ω LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

LOGIC DIAGRAM



V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

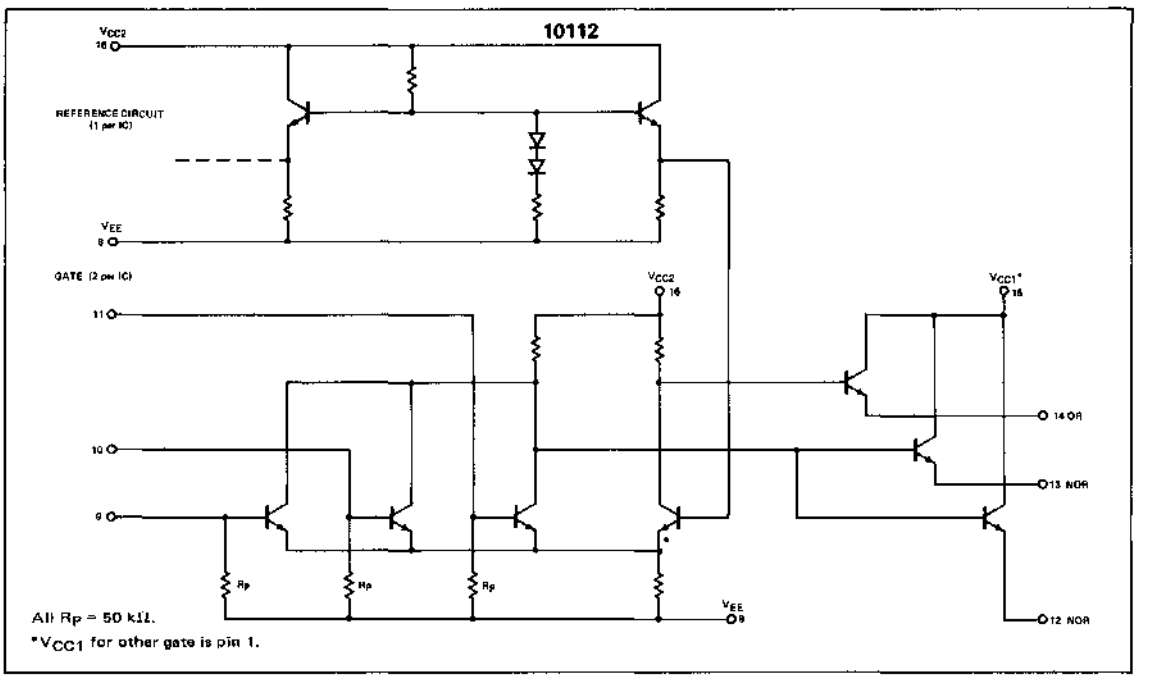
TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

CIRCUIT SCHEMATIC

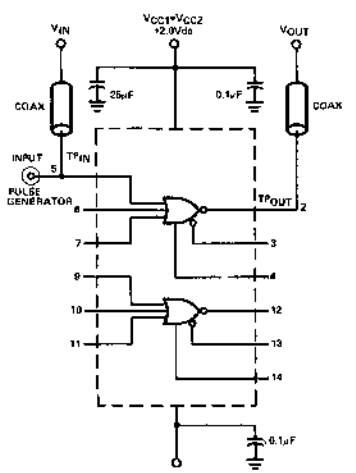


ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST CONDITIONS — TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$
−30°C	−0.890	−1.890	−1.205	−1.500
+25°C	−0.810	−1.850	−1.105	−1.475
+85°C	−0.700	−1.825	−1.035	−1.440

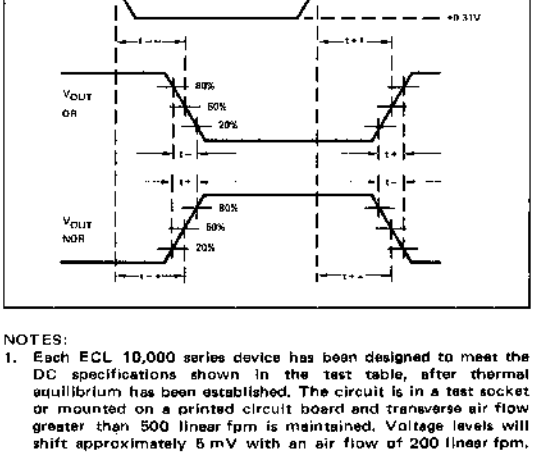
Characteristic	Symbol	Pin Under Test	10112 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	NOTES
Power Supply Drain Current	I_E	8	–	–	–	–	38		–	mAdc					5
Input Current	I_{inH}	5	–	–	–	–	420	–	–	µAdc	5	–	–	–	5
	I_{inL}	5	–	–	0.5	–	–	–	–	µAdc	–	5	–	–	5
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	–	–	–	5
		3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	6	–	–	5
		4	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	7	–	–	5
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	5	–	–	5
		3	1.890	1.675	−1.850		−1.650	−1.825	−1.615	Vdc	6	–	–	–	5
		4	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	5
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.810	–	Vdc	–	–	5	–	5
		3	−1.080	–	−0.980	–	–	−0.810	–	Vdc	–	–	–	6	5
		4	−1.080	–	−0.980	–	–	−0.810	–	Vdc	–	–	–	7	5
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.650	–	−1.595	Vdc	–	–	–	5	5
		3	–	−1.655	–	–	−1.650	–	−1.595	Vdc	–	–	6	–	5
		4		1.655			−1.650	–	−1.595	Vdc	–	–	7	–	5
Switching Times (50-ohm load)													Pulse In	Pulse Out	
Propagation Delay	$t_{5+\ 2+}$	2	–	–	1.4	2.4	3.5	–	–	ns			5	2	2,6
	$t_{5-\ 2-}$	2	–	–				–	–		–	–		2	
	$t_{5+\ 3-}$	3	–	–				–	–		–	–		3	
	$t_{5-\ 3+}$	3	–	–				–	–		–	–		3	
	$t_{5+\ 4-}$	4	–	–				–	–		–	–		4	
	$t_{5-\ 4+}$	4	–	–				–	–		–	–		4	
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.1	2.2	3.5	–	–		–	–		2	
	t_{3+}	3	–	–				–	–		–	–		3	
	t_{4+}	4	–	–				–	–		–	–		4	
Fall Time (20% to 80%)	t_{2-}	2	–	–				–	–		–	–		2	
	t_{3-}	3	–	–				–	–		–	–		3	
	t_{4-}	4	–	–				–	–		–	–		4	

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. Pin 1 = Pin 15 = Pin 16 = V_{CC} = 0 V, Pin 8 = V_{EE} = −5.2 V.
6. Pin 1 = Pin 15 = Pin 16 = V_{CC} = +2.0 V, Pin 8 = V_{EE} = −3.2 V.

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QUAD EXCLUSIVE OR (WITH ENABLE) 10113

10113B, F: –30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10113 is a four gate array designed to provide the positive logic Exclusive OR function in high performance applications. This device contains a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over temperature. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

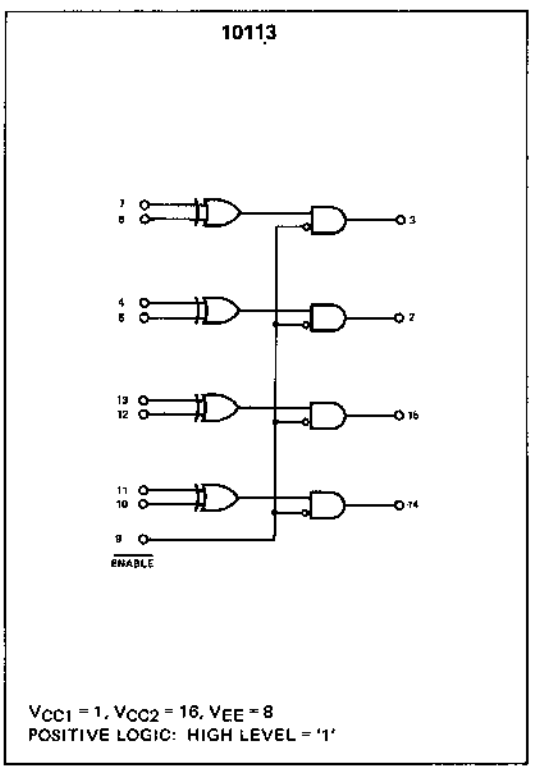
Open emitter outputs are provided to enable bussing of multiple outputs together. If the four outputs of the 10113 are wire-ORed together the device performs a 4-bit compare function (outputs low for compare).

The outputs are all gated by the enable input. If this $\overline{\text{enable}}$ input is high all outputs will be forced low.

FEATURES

- PERFORMS 4-BIT COMPARE FUNCTION (IF OUTPUTS ARE WIRE- ORed TOGETHER)
- HIGH FUNCTIONAL DENSITY – FOUR EXCLUSIVE OR GATES/PACKAGE
- FAST PROPAGATION DELAY FOR EXCLUSIVE OR: 2.5 ns TYP
- LOW POWER DISSIPATION: 165 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE FOUR 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- OUTPUT ENABLE GATING MAKES POWERFUL LOGIC FUNCTION

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

APPLICATIONS

- QUAD EXCLUSIVE-OR
  (For parity, error correcting, and other logic functions).
- FOUR-BIT COMPARATOR
  (For logic, test equipment, error detection applications).
- GATED FOUR-BIT COMPARATOR
  (Enable input permits wire-ORing multiples of four bits)

TRUTH TABLE

$\overline{E9}$	IN 7	IN 6	OUT 3
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	ϕ	ϕ	L

ϕ = Don't Care.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPES

- B: 16-Pin Silicone DIP
- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS

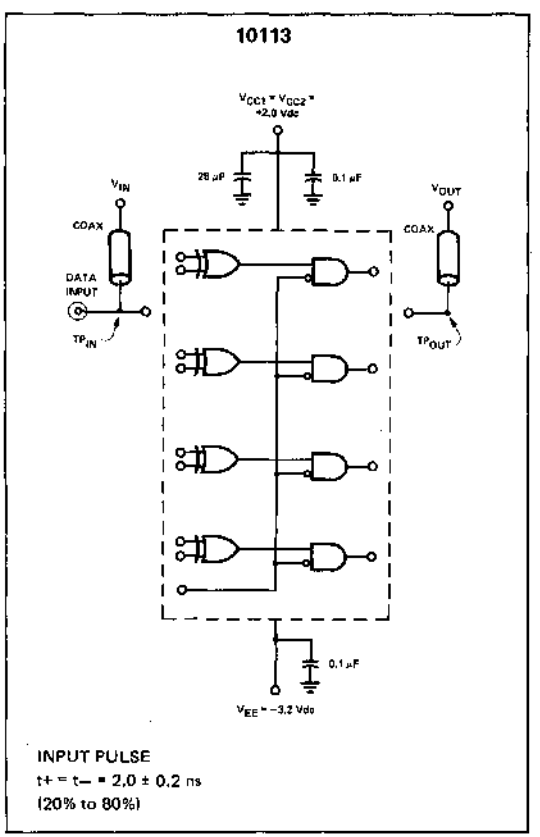
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10113 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	40		–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,7	–	–	–	265	–	–	µAdc	6,7	–	–	–	8	1,16
		9	–	–	–	720	–	–	µAdc	9	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	−1.050	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	6	–	–	–	8	1,16
		3	−1.050	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−1.850	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	–	–	–	–	8	1,16
		3	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	6,7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	−1.080	–	−0.980	–	−0.810	–	Vdc	–	–	6	–	8	1,16
		3	−1.080	–	−0.980	–	−0.810	–	Vdc	–	–	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	−1.630	–	−1.595	Vdc	7		6		8	1,16
		3	–	−1.655	–	−1.630	–	−1.595	Vdc	–	–	–	6	8	1,16
Switching Times** (50 Ω load)					Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t+	3				2.5			ns	–	–	6	3	8	1,16
	t+									/					
	t−									7	–	–	–		
	t−									–	–	–	–		
	t+	2,3,14,15				2.7				4,7,11,13	–	9	2,3,14,15		
	t−					2.7				–	–	–	–		
Rise Time (20% to 80%)	t+					2.5				–	–	Any Input	–		
Fall Time (20% to 80%)	t−					2.5				–	–	Any Input	–		

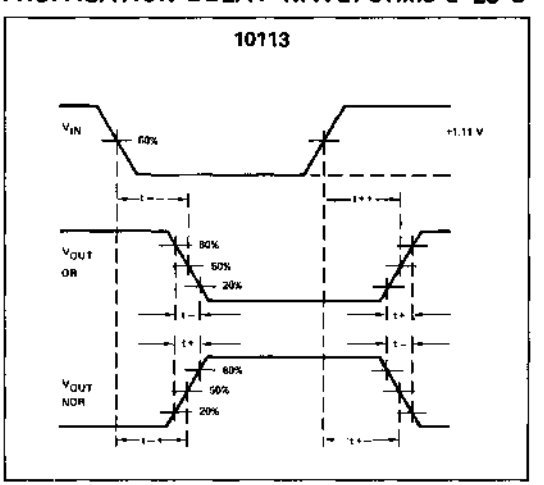
* Individually test each input applying V_{IH} or V_{IL} to input under test.
** Any Output
* Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2,0 ± 0,2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a linear printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coax(s) cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics QUAD DIFFERENTIAL LINE RECEIVER 10115

10115B,F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the 10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

FEATURES

- GOOD COMMON MODE NOISE REJECTION
- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH SYSTEM DENSITY – FOUR RECEIVERS PER PACKAGE
- VERY HIGH INPUT Z – NO 50 K PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- V_{BB} VOLTAGE AVAILABLE ON PIN 9

TEMPERATURE RANGE

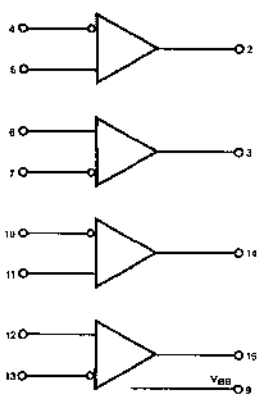
- –30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

LOGIC DIAGRAM

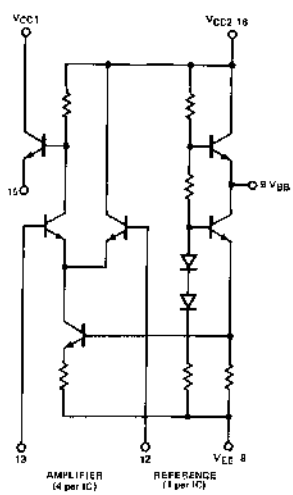
10115



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

CIRCUIT SCHEMATIC

10115



ELECTRICAL CHARACTERISTICS

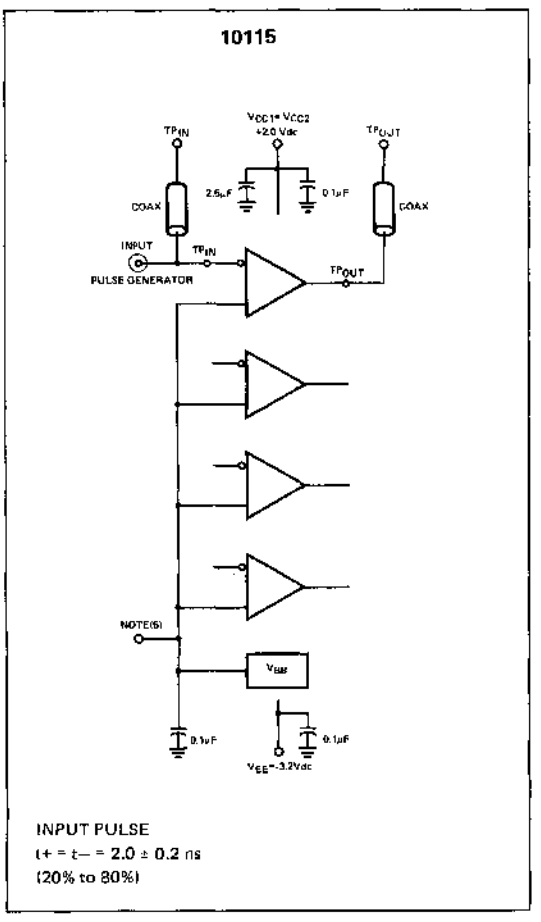
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	From	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	Pin	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	9	−5.2

Characteristic	Symbol	Pin Under Test	10115 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	26	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	9	1,16
Input Current	I_{inH}	4	–	–	–	95	–	–	µAdc	4	7,10,13	–	–	5,6,11,12	9	1,16
	I_{CBO}	4	–	–	–	1.0	–	–	µAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	7,10,13	4	–	–	5,6,11,12	9	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	4	7,10,13	–	–	5,6,11,12	9	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	−0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	9	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	−1.630	–	−1.595	Vdc	–	7,10,13	4	–	5,6,11,12	9	1,16
Reference Voltage	V_{BB}	9	−1.420	−1.280	−1.360	−1.230	−1.295	−1.160	Vdc	–	–	–	–	5,6,11,12	9	1,16
Switching Times * (50-ohm load)										Pulse In		Pulse Out			−3.2 V	+2.0 V
Propagation Delay	t_{d-} 2+	2	1.0	3.1	1.0	2.9	1.0	3.3	ns	4		2		5,6,11,12	8	1,16
	t_{d+} 2−	2	1.0	2.9	1.0	2.9	1.0	3.3								
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	3.3	1.1	3.7								
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.3	1.1	3.3	1.1	3.7								

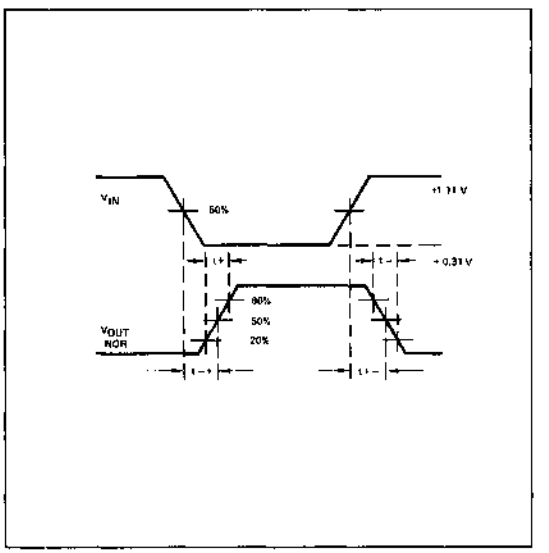
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
(+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 9) during testing.

signetics

TRIPLE DIFFERENTIAL OR/NOR LINE RECEIVER | 10116

10116B,F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the 10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complemented outputs of the input logic function.

FEATURES

- GOOD COMMON MODE NOISE REJECTION
- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 83 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- VERY HIGH INPUT Z – NO 50 K PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- COMPLEMENTARY OUTPUTS
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- V_{BB} VOLTAGE AVAILABLE ON PIN 11

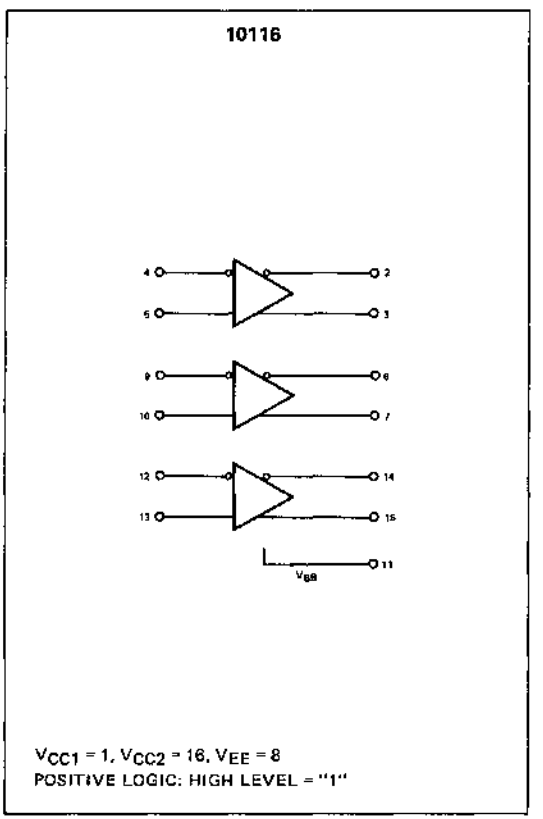
TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

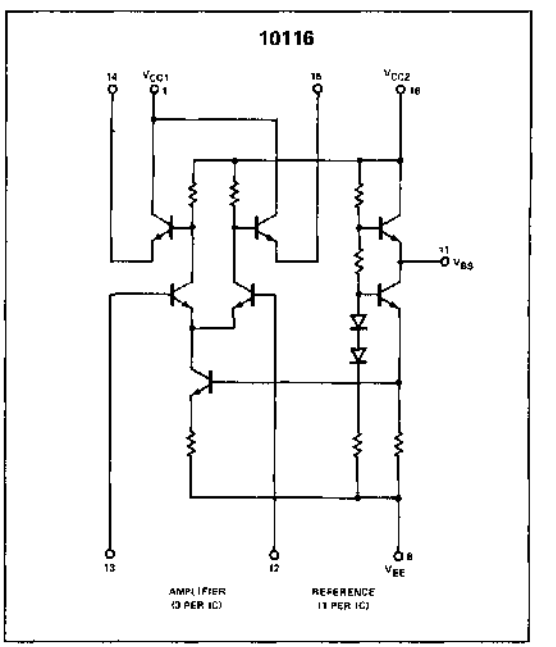
PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

LOGIC DIAGRAM



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

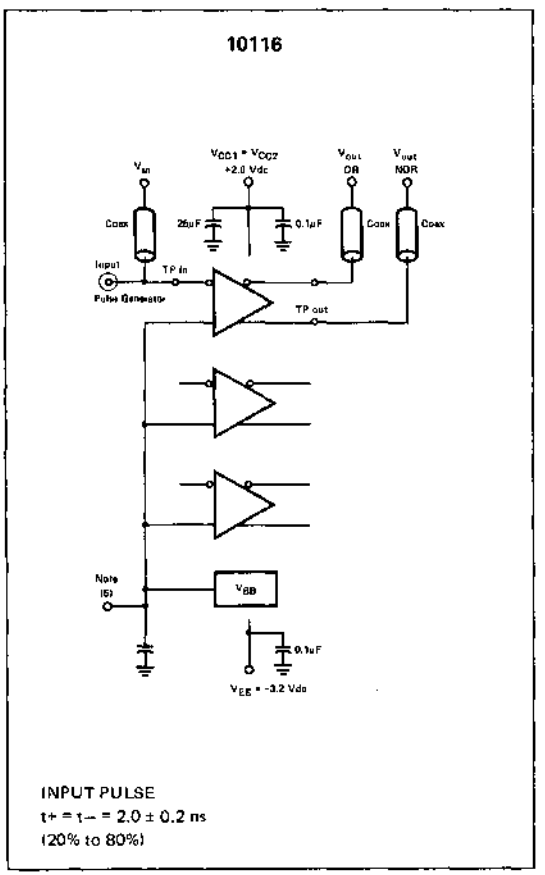
(At Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	From	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	Pin	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	11	−5.2

Characteristic	Symbol	Pin Under Test	10116 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	16	20	–	–	mAdc	–	4,9,12	–	–	5,10,13	8	1,16
	I_{inH}	4	–	–	–	–	95	–	–	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	−1.060	−0.890	−0.980	–	−0.810	−0.890	−0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	−1.060	−0.890	−0.980	–	−0.810	−0.890	−0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	−1.690	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc	4	9,12		–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	−1.060	–	−0.980	–	–	−0.810	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	−1.060	–	−0.980	–	–	−0.810	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	−1.665	–	–	−1.630	–	−1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	−1.665	–	–	−1.630	–	−1.595	Vdc	9,12	–	4		5,10,13	8	1,16
Reference Voltage	V_{BB}	11	−1.420	−1.280	−1.350	–	−1.230	−1.295	−1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out		−3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.8	1.0	3.0	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓		–	–		2			
	t_{4+3-}	3									–	–		3			
	t_{4-3+}	3									–	–		3			
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7		–	–		2			
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓		–	–	↓	3	↓	↓	↓
Fall Time (20% to 80%)	t_{2-}	2									–	–		2			
	t_{3-}	3									–	–		3			

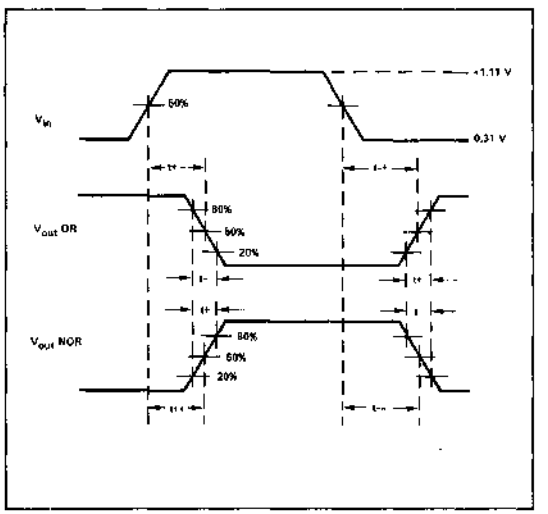
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t_{+} = t_{-} = 2.0 \pm 0.2$ ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 11) during testing.

signetics

DUAL 2-WIDE 2,3-INPUT OR-AND/OR-AND-INVERT GATE

10117

10117B,F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

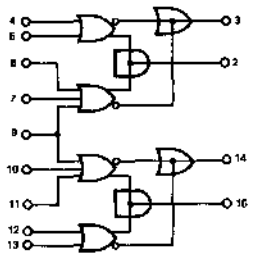
The 10117 package contains two 2 input/3 input OR-AND/OR-AND INVERT complex gates. Pin 9 is common to both gates. This function is particularly useful in data control, multiplexing and distribution. The 10117 is optimized for high performance applications and has an excellent speed power product. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment.

FEATURES

- FAST PROPAGATION DELAY FOR TWO LOGIC LEVELS = 2.3 ns TYP
- POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY
- OUTPUTS MAY BE CROSS COUPLED BACK TO INPUTS TO MAKE A LATCH FUNCTION

LOGIC DIAGRAM

10117



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

TEMPERATURE RANGE

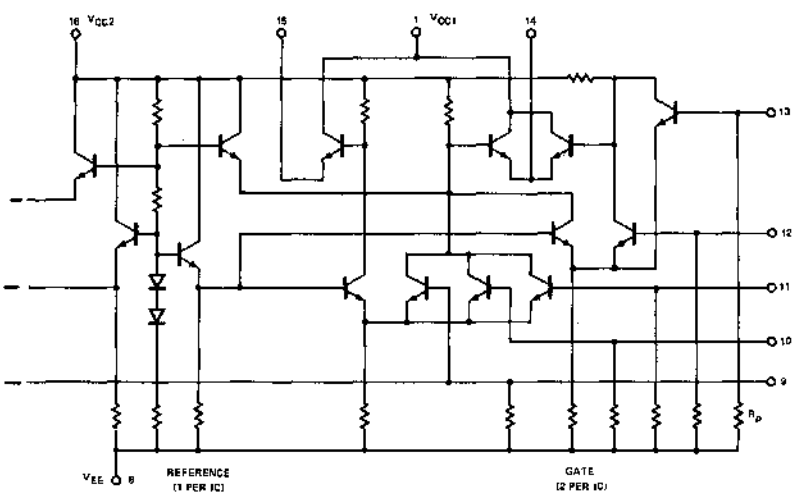
- –30 to +85

PACKAGE TYPE

B: 16 Pin Silicone DIP
F: 16 Pin CERDIP

CIRCUIT SCHEMATIC

10117



All Rp = 50 kΩ.

ELECTRICAL CHARACTERISTICS

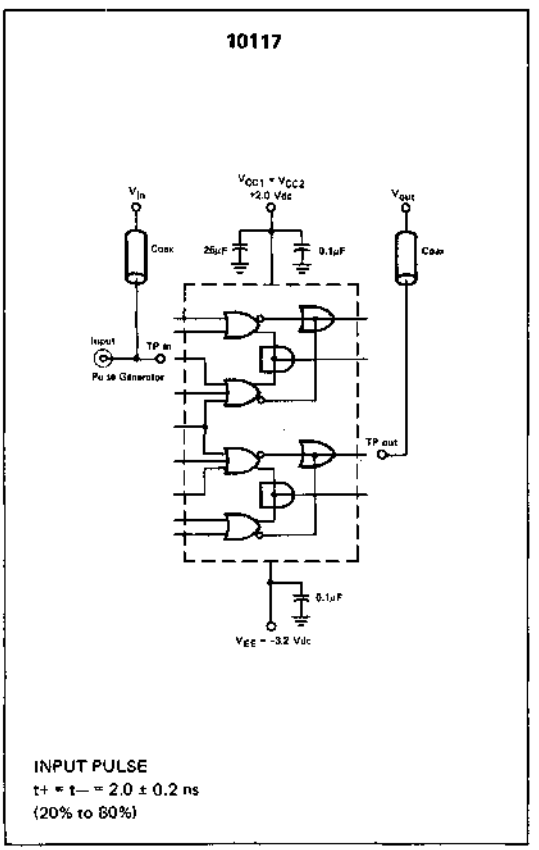
(at Listed Voltage and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10117 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	"	–	μAdc	4	–	–	–	8	1,16
		9	–	–	–	–	370	–	–	μAdc	9	–	–	–	8	1,16
	I_{inL}	4	"	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
		9	–	–	0.5	–	–	–	–	μAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4,9	–	–	–	8	1,16
		3	−1.060	−0.780	0.960	–	−0.700	−0.890	−0.690	Vdc	–	4,9	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−2.000	−1.675	−1.990	–	−1.650	−1.920	−1.615	Vdc	–	4,9	–	–	8	1,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4,9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.060	–	−0.960	–	–	−0.910	–	Vdc	9	–	4	–	8	1,16
		3	−1.080	–	−0.980	–	–	−0.810	–	Vdc	9	–	–	4	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	"	"	−1.630	–	−1.595	Vdc	9	–	–	4	8	1,16
		3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	9	–	4	–	8	1,16
Switching Times * (50-ohm load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.4	3.8	1.4	2.3	3.4	1.4	3.8	ns	9	–	4	2	8	1,16
	t_{4-2-}	2										–		2		
	t_{4+3-}	3										–		3		
	t_{4-3+}	3										–		3		
Rise Time (20% to 80%)	t_{2+}	2	0.9	4.1	1.1	2.2	4.0	1.1	4.6			–		2		
	t_{3+}	3										–		3		
Fall Time (20% to 80%)	t_{2-}	2										–		2		
	t_{3-}	3										–		3		

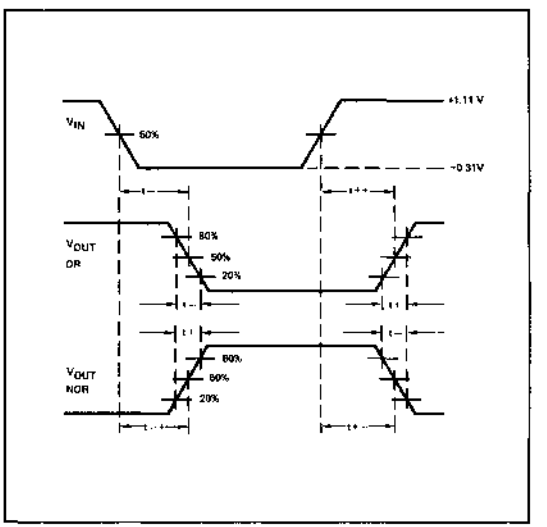
* Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

DUAL 2-WIDE 3,3-INPUT OR-AND GATE | 10118

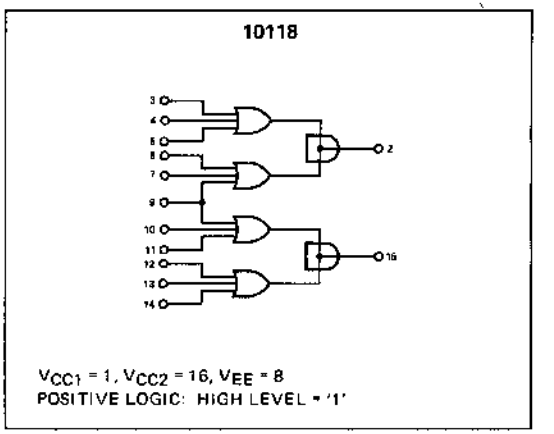
10118B, F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10118 package contains two 3,3-input OR-AND Complex gates. Pin 9 is common to both gates. This function is particularly useful in data control, multiplexing and data distribution. The 10118 is optimized for high performance applications and has an excellent speed power product. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment. This gate meets the ECL 10,000 Series current and rise and fall time specifications.

LOGIC DIAGRAM



FEATURES

- **FAST PROPAGATION DELAY FOR 2 LOGIC LEVELS = 2.3 ns TYP**
- **LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)**
- **HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINE**
- **HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{CC} = –5.2 V ±5% RECOMMENDED**
- **OPEN EMITTER LOGIC AND BUSSING CAPABILITY**

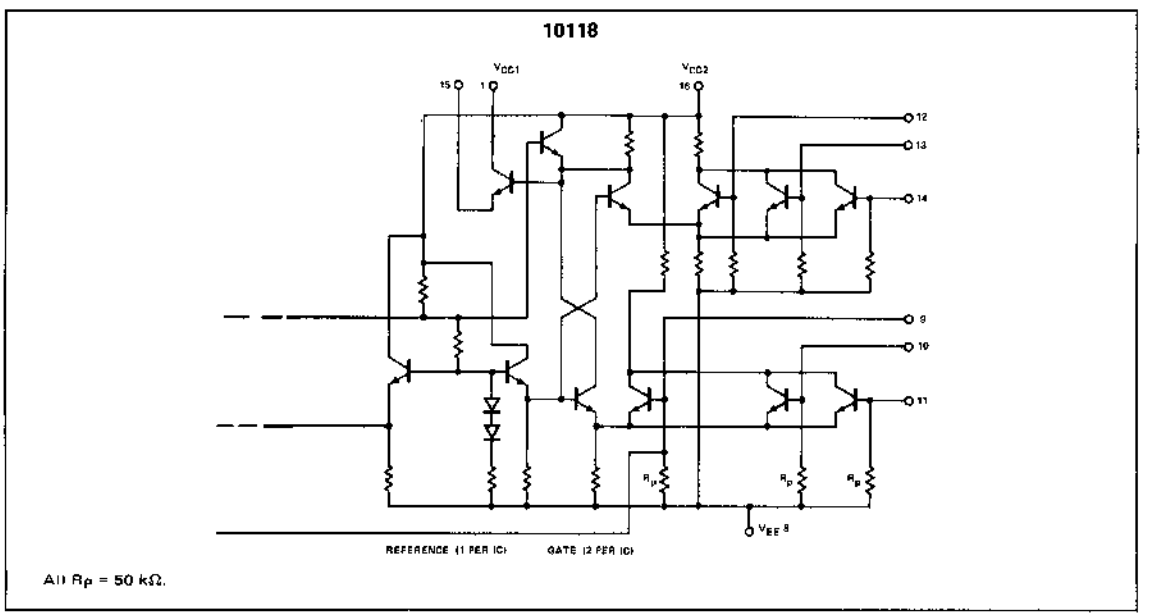
TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

CIRCUIT SCHEMATIC



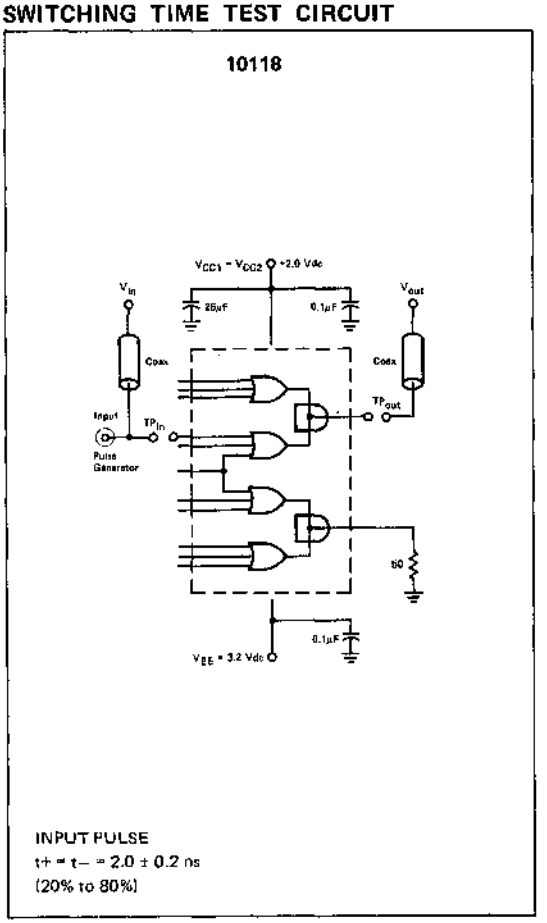
ELECTRICAL CHARACTERISTICS (at Listed Voltages and Ambient Temperatures).

Ø Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.036	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10118 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} Gnd
Power Supply Drainm Current	I_E	8	–	–	–	20	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6	–	–	–	–	265	–	–	µAdc	6	–	–	–	8	1,16
		7	–	–	–	–	265	–	–		7	–	–	–		
		9	–	–	–	–	370	–	–		9	–	–	–		
	I_{inL}	6	–	–	0.5	–	–	–	–	µAdc	–	6	–	–	8	1,16
		7	–	–		–	–	–	–		–	7	–	–		
		9	–	–		–	–	–	–		–	9	–	–		
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.880	−0.700	Vdc	3,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−2.000	−1.675	−1.990	–	−1.650	−1.920	−1.615	Vdc	–	3,9	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.060	–	−0.960	–	–	−0.910	–	Vdc	9	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	9	–	–	3	8	1,16
Switching Times* (50-ohm load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{\emptyset+\ 2+}$	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	3	–	6	2	8	1,16
	$t_{\emptyset-\ 2-}$		1.4	3.9	1.4	2.3	3.4	1.4	3.8			–				
Rise Time (20% to 80%)	t_+		0.8	4.1	1.5	2.6	4.0	1.5	4.6			–				
Fall Time (20% to 80%)	t_-		0.8	4.1	1.5	2.6	4.0	1.5	4.6			–				

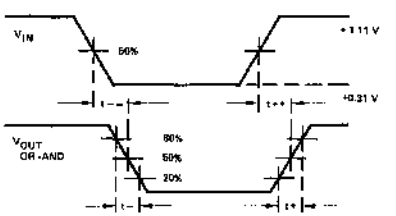
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t_+ = t_- = 2.0 \pm 0.2$ ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

4-WIDE 4,3,3,3-INPUT OR-AND GATE DUAL | 10119

10119B,F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

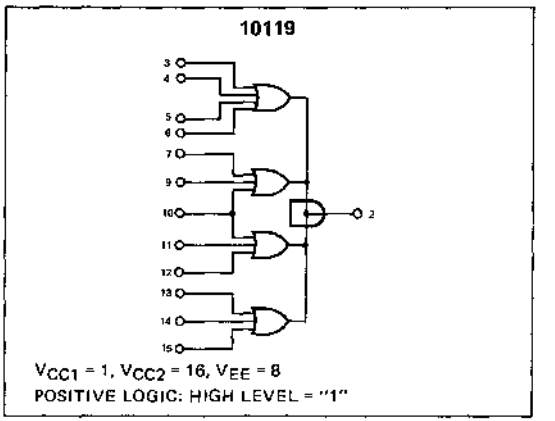
DESCRIPTION

The 10119 is a 4 wide 4-3-3-3 input OR-AND gate. Pin 10 is common to two of the input gates. This function is particularly useful in data control and multiplexing. The 10119 is optimized for high performance applications and has an excellent speed power product. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment.

FEATURES

- FAST PROPAGATION DELAY FOR 2 LOGIC LEVELS = 2.3 ns TYP
- LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINE
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

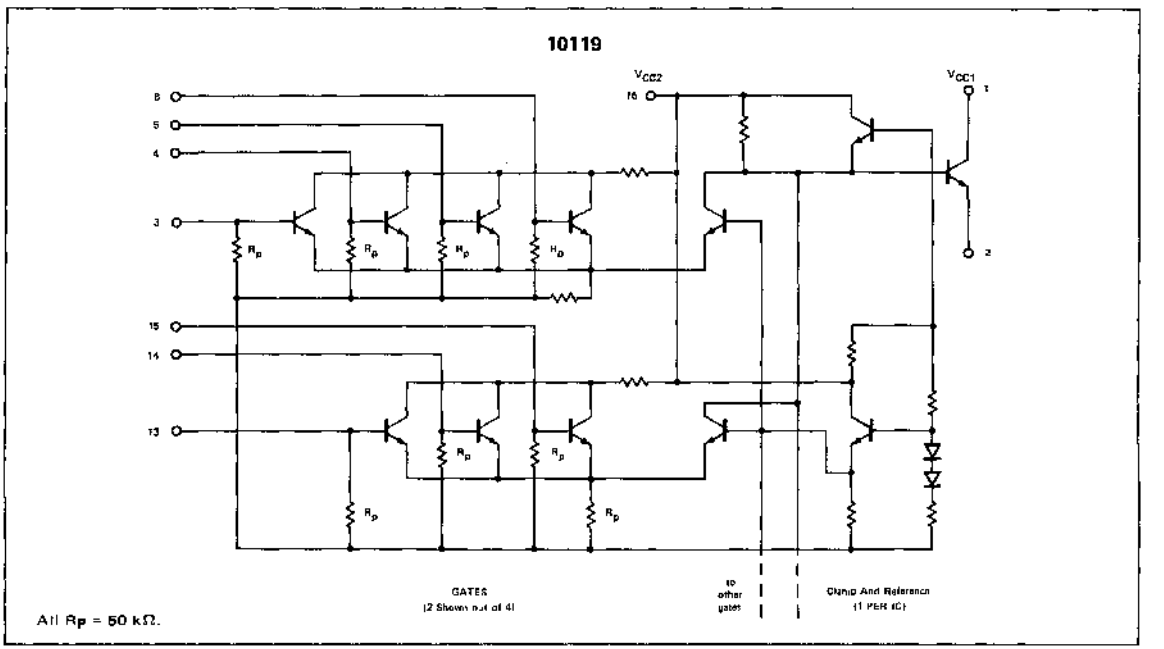
TEMPERATURE RANGE

−30 to +85

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

CIRCUIT SCHEMATIC



All Rp = 50 kΩ.

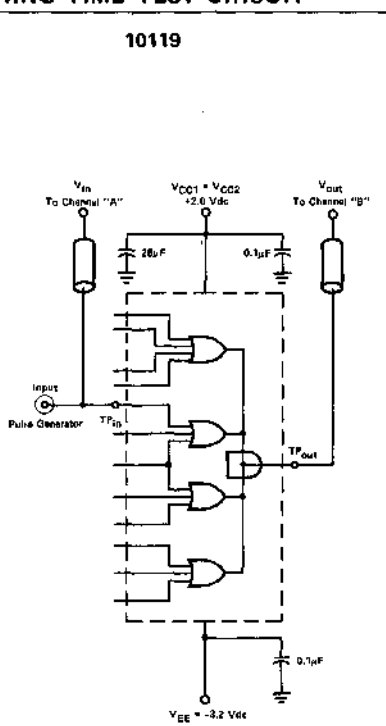
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.705	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10119 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1,16
		9	–	–	–	–	265	–	–		9	–	–			
		10	–	–	–	–	370	–	–		10	–	–	–		
	I_{inL}	7	–	–	0.5	–	–	–	–	μAdc	–	7	–	–	8	1,16
		9	–	–		–	–	–	–		–	9	–			
		10	–	–	–	–	–	–	–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	2	−1.080	−0.890	−0.960	–	−0.810	−0.830	−0.700	Vdc	3,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−2.000	−1.675	−1.900	–	−1.650	−1.920	−1.615	Vdc	–	3,10,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	10,15	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	10,15			3	8	1,16
Switching Times * (50-ohm load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t3+ 2+	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	10,13	–	3	2	8	1,16
	t3− 2−		1.4	3.9	1.4	2.3	3.4	1.4	3.8		10,13	–				
Rise Time (20% to 80%)	t+		0.8	4.1	1.5	2.5	4.0	1.5	4.6		–	–				
Fall Time (20% to 80%)	t−		0.8	4.1	1.5	2.5	4.0	1.5	4.6		–	–				

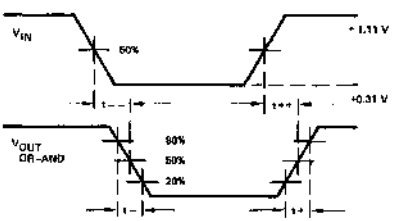
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

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4-WIDE 3,3,3,3-INPUT OR-AND/OR-AND-INVERT GATE

10121

10121B,F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10121 is a 4 wide 3-3-3-input OR-AND/OR-AND-INVERT gate. Pin 10 is common to two of the input gates. This function is particularly useful in data control and multiplexing. The 10121 is optimized for high performance applications and has an excellent speed power product. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment.

FEATURES

- FAST PROPAGATION DELAY FOR 2 LOGIC LEVELS = 2.3 ns TYP
- LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY
  – CAN DRIVE TWO 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

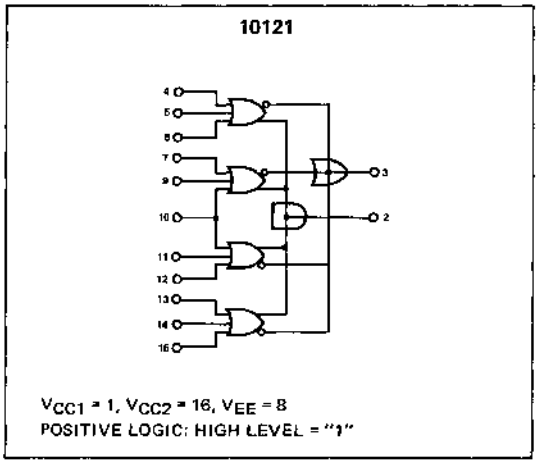
EQUATIONS (Positive Logic)

$$2 = (4+5+6) \cdot (7+9+10) \cdot (10+11+12) \cdot (13+14+15)$$

$$3 = \overline{(4+5+6)} + \overline{(7+9+10)} + \overline{(10+11+12)} + \overline{(13+14+15)}$$

$$= \overline{(4+5+6) \cdot (7+9+10) \cdot (10+11+12) \cdot (13+14+15)}$$

LOGIC DIAGRAM



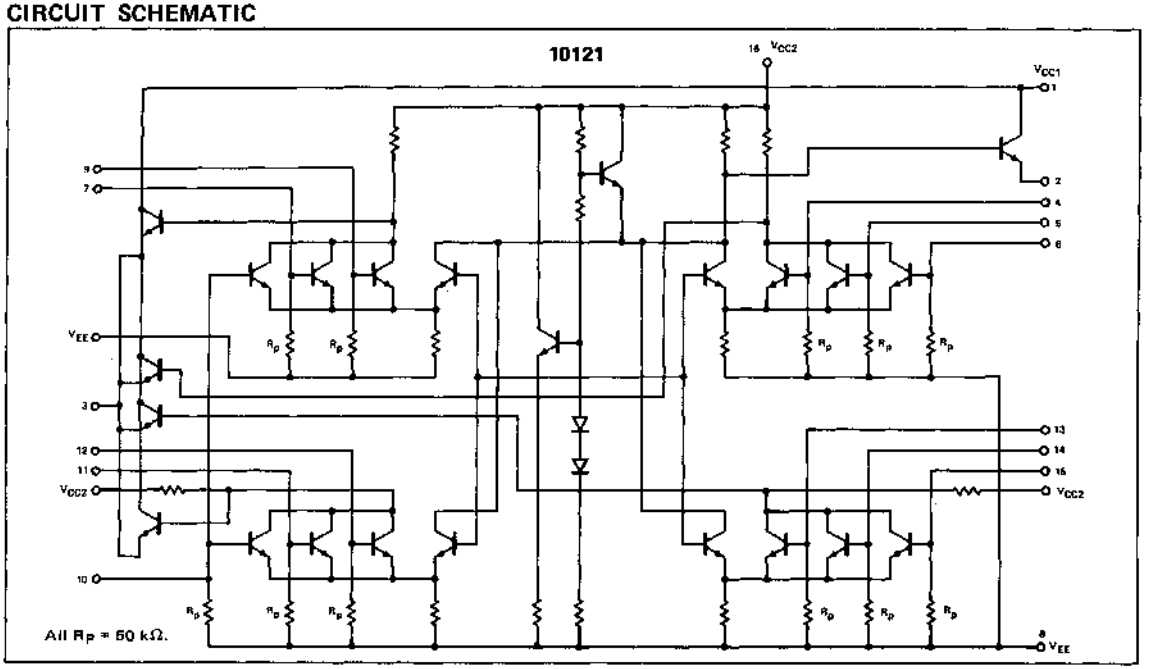
TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

CIRCUIT SCHEMATIC



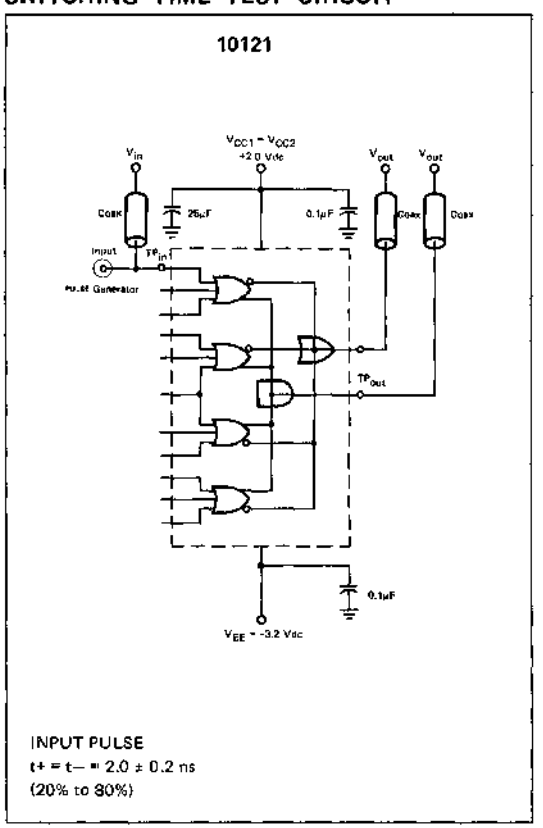
ELECTRICAL CHARACTERISTICS
(at Listed Voltage and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10121 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	7	–	–	–	–	265	–	–	μAdc	7	–		–	8	1,16
		9	–	–	–	–	265	–	–		9	–	–	–		
		10	–	–	–	–	370	–	–		10	–	–	–		
	I_{inL}	7	–	–	0.5	–	–	–	–	μAdc	–	7	–	–	8	1,16
		9	–	–		–	–	–	–		–	9	–	–		
		10	–	–		–	–	–	–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	3	−1.060	−0.780	−0.960	–	−0.700	−0.890	−0.680	Vdc	–	–	–	–	8	1,16
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4,10,15	–	–	–	8	1,16
		2	−2.000	−1.675	−1.990	–	−1.650	−1.920	−1.615	Vdc	–	4,10,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	1.060	–	−0.980	–	–	−0.910	–	Vdc	10,15	–	–	4	8	1,16
		2	−1.060	–	−0.980	–	–	−0.910	–	Vdc	10,15	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	10,15	–	4	–	8	1,16
		2		−1.655	–	–	−1.630	–	−1.595	Vdc	10,15	–	–	4	8	1,16
Switching Times * (50-ohm load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{4-3-}	3	1.4	3.9	1.4	2.3	3.4	1.4	3.6	ns	10,13	–	4	3	8	1,16
	t_{4-3+}	3										–		3		
	t_{4-2+}	2										–		2		
	t_{4-2-}	2										–		2		
Rise Time (20% to 80%)	t_{3+}	3	0.8	4.1	1.1	2.5	4.0	1.0	4.8			–		3		
	t_{2+}	2										–		2		
Fall Time (20% to 80%)	t_{3-}	3										–		3		
	t_{2-}	2										–		2		

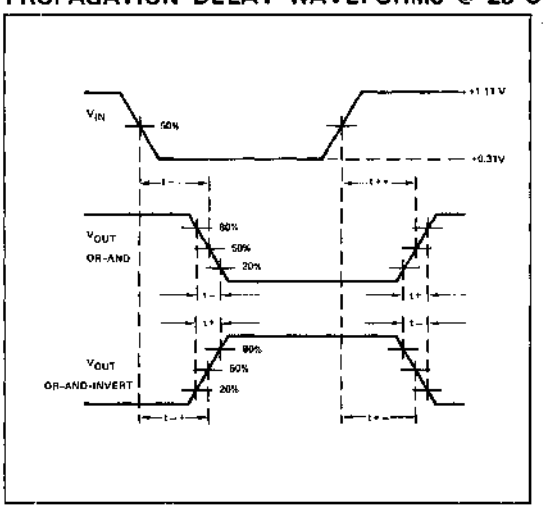
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

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QUAD DIFFERENTIAL LINE DRIVER
QUAD TTL TO ECL TRANSLATOR

10124

10124 B,F: -30 to 85°C

ADVANCED INFORMATION

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10124 is a Quad Differential Line Driver or TTL to ECL translator. The 10124 inputs are compatible with standard and Schottky TTL levels. The outputs are standard ECL 10,000 levels. Complementary open emitter outputs provide for inverting, non-inverting or differential applications. A common strobe input when at a TTL logical "0" forces all true outputs to an ECL logical "0" and all inverting outputs to an ECL logical "1".

FEATURES

- FAST PROPAGATION DELAY = 5.0 ns TYP.
- POWER DISSIPATION = 340mW/PACKAGE TYP.
- VERY HIGH FANOUT CAPABILITY
  - CAN DRIVE EIGHT 50Ω LINES
  - DC OUTPUT LOADING FACTOR OF 90X8
- COMPLEMENTARY OUTPUTS
- STANDARD ECL 10,000 SERIES OUTPUT LEVELS
- OPEN EMITTER OUTPUTS FOR BUSSING AND LOGIC CAPABILITY
- TTL COMPATIBLE INPUT STROBE
- INPUT-CLAMP DIODES
- FOUR TRANSLATORS PER PACKAGE

TEMPERATURE RANGE

- -30 to +85°C Operating Ambient

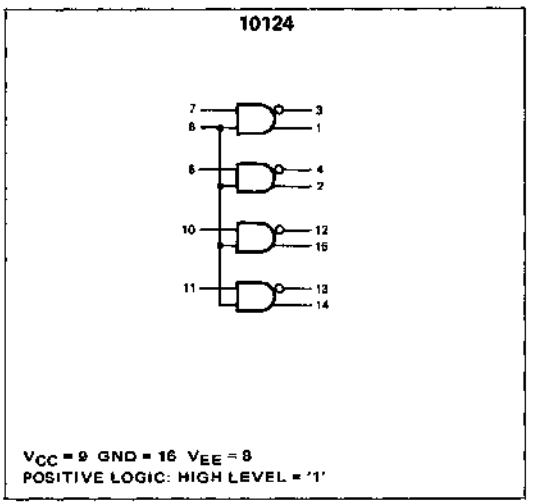
RECOMMENDED OPERATING VOLTAGE

- V_{CC} = +5.0V±5%, V_{EE} = -5.2V±5%

PACKAGE TYPES

- B: 16 Pin Silicone Dip
- F: 16 Pin Cerdip

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: T_A = 25°C, V_{CC} = +5.0V±1%, V_{EE} = -5.2V±1%

1. I_{EE} = 66mA max.
   I_{CCH} = 14.5mA max.
   I_{CCL} = 24mA max.

2. I_{inL} = -3.2mA max. (pins 5, 7, 10, 11)
   I_{inL} = -12.8mA max. (pin 6)
   I_{inH} = 265μA max. (pin 6)

3. V_{in} = -1.2V min. (I_{in} = -18mA)

   Conditions: T_A = 25°C, V_{CC} = +5.0V±1%
   V_{EE} = -5.2V±1%, R_L = 50Ω to -2.0V
   V_{in} = +2.0V min. or
   V_{in} = +0.8V max.

4. V_{OH} = -.81V max.
   = -.96V min.

5. V_{OL} = -1.65V max.
   = -1.85V min.

6. t_{pd} = 5.0 ns typ.
   = 8.0 ns max.

7. t_r, t_f = 2.5 ns typ. (20 to 80%)

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QUAD DIFFERENTIAL LINE RECEIVER
QUAD ECL TO TTL TRANSLATOR

10125

10125, B, F: -30 to +85°C

ADVANCED INFORMATION

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10125 is a quad differential translator. It can be used as a quad differential line receiver in a TTL system and also as a quad ECL to TTL translator. The 10125 incorporates differential inputs and Schottky-clamped TTL totem pole outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver.

FEATURES

- FAST PROPAGATION DELAY = 5.0ns TYP.
- POWER DISSIPATION = 360mW/PACKAGE TYPICAL
- DIFFERENTIAL INPUTS, ECL COMPATIBLE
- ECL 10,000 LEVEL V_{BB} AVAILABLE
- INVERTING OR NON-INVERTING FUNCTION
- SCHOTTKY TTL TOTEM POLE OUTPUTS
- RECOMMENDED POWER SUPPLIES:
  V_{CC} = +5.0V DC ±5%
  V_{EE} = -5.2V DC ±5%
- FOUR TRANSLATORS PER PACKAGE
- OUTPUT LEVELS SPECIFIED FOR INPUT VOLTAGE RANGE +0.2V to -2.2V

ELECTRICAL CHARACTERISTICS

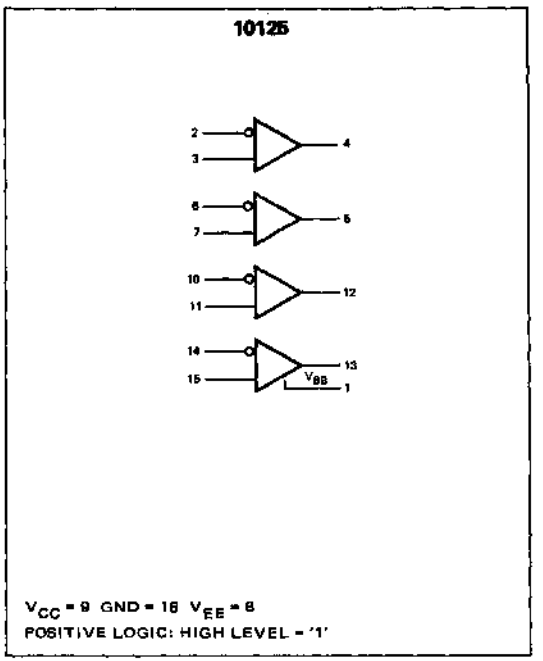
Conditions: T_A = 25°C, V_{EE} = -5.2V ±1%
V_{CC} = +5.0V ±1%

1. I_{EE} = 40mA max.
   I_{CCH} = 54mA max.
   I_{CCL} = 45mA max.
2. I_{inH} = 110μA max.
3. V_{BB} = -1.35V min.
   = -1.23V max.
4. t_{pd} = 5.0ns typ. (C_L = 15pF, R_L = 280Ω)
   = 7.0ns typ. (C_L = 50pF, R_L = 280Ω)

Conditions: T_A = 25°C, V_{EE} = -5.2V ±1%
V_{CC} = +5.0V ±5% ΔV_{in} = 200mV

5. V_{OL} = 0.5 max. (I_{OL} = 20mA)
6. V_{OH} = +2.7V min. (I_{OL} = -1mA)

LOGIC DIAGRAM



APPLICATIONS

- QUAD DIFFERENTIAL LINE RECEIVER
- QUAD ECL TO TTL TRANSLATOR
- QUAD MOS TO TTL SENSE AMP
- QUAD LEVEL DETECTOR

TEMPERATURE RANGE

- -30 to +85°C Operating Ambient

RECOMMENDED OPERATING VOLTAGE

- V_{CC} = +5.0V ±5%, V_{EE} = -5.2V ±5%

PACKAGE TYPE

- B: 16-Pin Silicone DIP
- F: 16-Pin CERDIP

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DUAL D-TYPE LATCH 10130

10130F: –30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10130 is a clocked dual D-type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

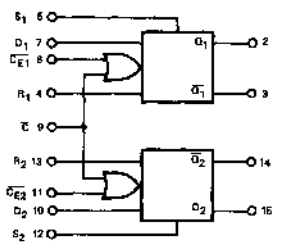
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

The asynchronous set (S) and reset (R) inputs are effective only with the clock input high.

The 10130 is pin compatible with the 10131 dual master/slave type D flip-flop.

LOGIC DIAGRAM

10130



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

FEATURES

- FAST PROPAGATION DELAY = 2.5 ns TYP (DATA)
  = 2.8 ns TYP (SET, RESET)
  = 3.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 140 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- PIN COMPATIBLE WITH 10131

APPLICATIONS

- HIGH SPEED REGISTERS
- CONTROL LATCHES
- STATUS LATCHES

TRUTH TABLE

D	C	S	R	Q_{n+1}
L	L	ϕ	ϕ	I
A	I	ϕ	ϕ	H
ϕ	H	L	L	Q_n
ϕ	H	H	L	H
ϕ	H	L	H	L
ϕ	H	H	H	N.D.

$C = \overline{CE} + \overline{C}$
ϕ = Don't care
N.D. = Not defined

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.600	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

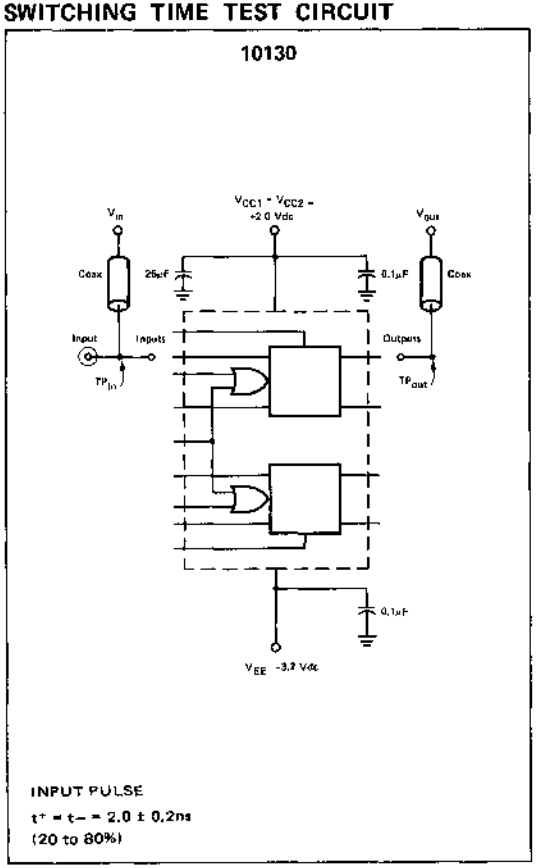
Characteristic	Symbol	Pin Under Test	10130 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	35	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	–	–	–	220	–	–	µAdc	8	–	–	–	8	1,16
		9	–	–	–	–	265	–	–		4,8	–	–	–		
		4,5,7	–	–	–	–	265	–	–		5,9	–	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	7	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	7	–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	7	–	–	9	8	1,16
Switching Times (50 Ω load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{7-2-}	2	–	–	1.5	2.5	4.3	–	–	ns	–	–	7	2	8	1,16
	t_{7+2+}		–	–	1.5	2.5	4.3	–	–		–	–	7			
	t_{5+2+}		–	–	1.5	2.8	4.3	–	–		6	–	5			
	t_{4+2-}		–		1.2	2.8	4.3				6		4			
Rise Time (20% to 80%)	t_{2+}		–	–	1.1	2.5	4.6	–	–		–	–	7			
Fall Time (20% to 80%)	t_{2-}		–	–	1.1	2.5	4.6	–	–		–	–	7			
Setup Time	t_{setup}†	2	–	–	–	–	2.5	–	–	ns	–	–	6,7	2	8	1,16
Hold Time	t_{hold}††	2	–	–	1.5	–	–	–	–	ns	–	–	6,7	2	8	1,16

*All other inputs are tested in the same manner.

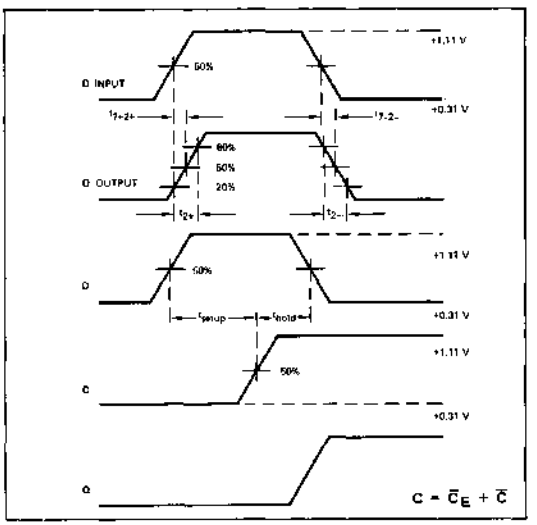
† t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

†† t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C

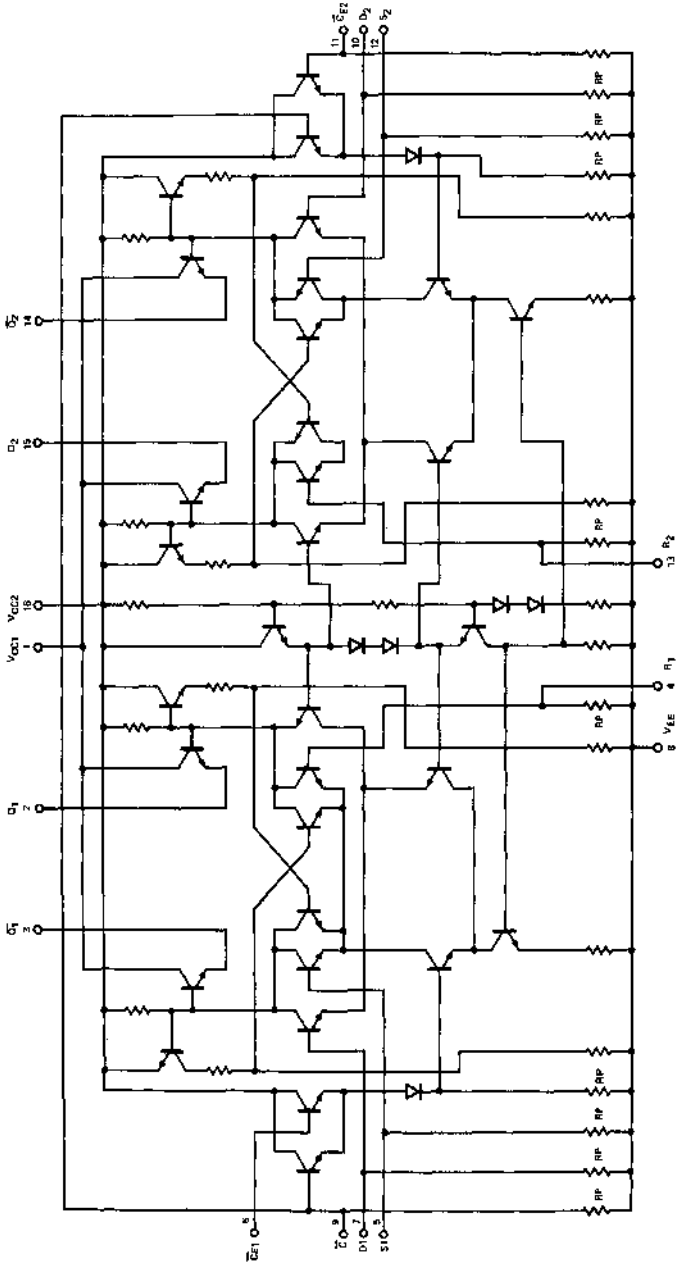


NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

CIRCUIT SCHEMATIC

10130



$C = \overline{C}_E + \overline{C}$. All Rp = 50 kΩ.

signetics

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP 10131

10131F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

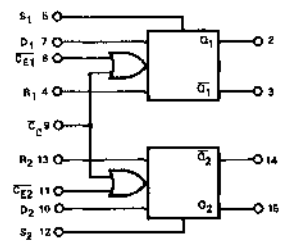
The 10131 is a dual master-slave type D flip-flop. Asynchronous set (S) and reset (R) override clock ($\overline{C}$) and clock enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the clock enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master-slave construction. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

The 10131 is pin compatible with the 10130 dual D-type latch.

LOGIC DIAGRAM

10131



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

FEATURES

- f_{TOG} = 125 MHz MIN
  = 160 MHz TYP
- FAST PROPAGATION DELAY
  = 2.8 ns TYP (SET, RESET)
  = 3.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 235 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY
  – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- PIN COMPATIBLE WITH 10130

APPLICATIONS

- CONTROL LOGIC
- STATUS LOGIC
- COUNTERS
- SHIFT REGISTER
- PRESCALERS

TRUTH TABLE

D	C*	S	R	Q_{n+1}
ϕ	L	L	L	Q_n
L	H	L	L	L
H	H	L	L	H
ϕ	*ϕ	H	L	H
ϕ	ϕ	L	H	L
ϕ	ϕ	H	H	N.D.

*An H represents a transition from L to H between t = n and t = n + 1

$C = C_C + \overline{CE}$

N.D. = Not defined

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES, Vee ± 1% V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10131 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	45	55	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	330	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	–	330	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	245	–	–		7	–	–	–		
		9	–	–	–	–	265	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	μAdc	–	+	–	–	8	1,16
		6,7,9	–	–	0.5	–	–	–	–	μAdc	–	+	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	–	–	–	8	1,16
		2†	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5	–	–	–	8	1,16
		3†	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	5	–	8	1,16
		2†	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	7	9	6	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	5	–	8	1,16
		3†	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	7	8	1,16
Switching Times Clock Input**											+1.11 Vdc		Pulse In	Pulse Out	−3.2 Vdc	+2.0 Vdc
Propagation Delay	$t_{9+\ 2-}$	2	1.4	4.6	1.5	3.0	4.5	1.8	5.0	ns	–	–	9	2	8	1,16
	$t_{9+\ 2+}$	2									7	–	9	2		
	$t_{8+\ 2+}$	2									7	–	8	2		
	$t_{8+\ 2-}$	2									–	–	8	2		
Rise Time (20% to 80%)	t_{2+}	2	0.8		1.1	2.5		1.1	4.8		7	–	9	2		
Fall Time (20% to 80%)	t_{2-}	2	0.8		1.1	2.5		1.1	4.9		–	–	9	2		
Set Input																
Propagation Delay	$t_{8+\ 2+}$	2	1.1	4.4	1.2	2.8	4.3	1.2	4.8	ns	–	–	8	2	8	1,16
	$t_{12+\ 15+}$	15									–	–	12	15		
	$t_{8+\ 3-}$	3									–	–	8	3		
	$t_{12+\ 14-}$	14									–	–	12	14		
Reset Input																
Propagation Delay	$t_{4+\ 2-}$	2	1.1	4.4	1.2	2.8	4.3	1.2	4.8	ns	–	–	4	2	8	1,16
	$t_{13+\ 15-}$	15									–	–	13	15		
	$t_{4+\ 3+}$	3									–	–	4	3		
	$t_{13+\ 14+}$	14									–	–	13	14		
Setup Time	t_{setup}	7	–	–	–	1.5	2.5	–	–	ns	–	–	6,7	2	8	1,16
Hold Time	t_{hold}	7	–	–	1.5	−0.5	–	–	–	ns	–	–	6,7	2	8	1,16
Toggle Frequency (Max)	f_{Tog}	2	125	–	125	160	–	125	–	MHz	–	–	8	2	8	1,16

*Individually test each input; apply V_{IL} min to pin under test.

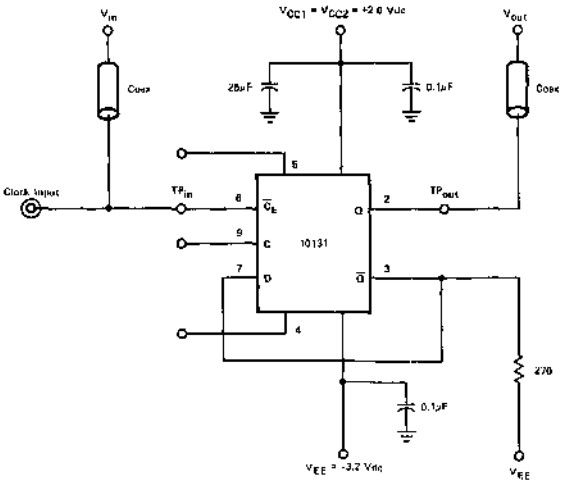
**Pin 3 is tied to pin 7 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) 

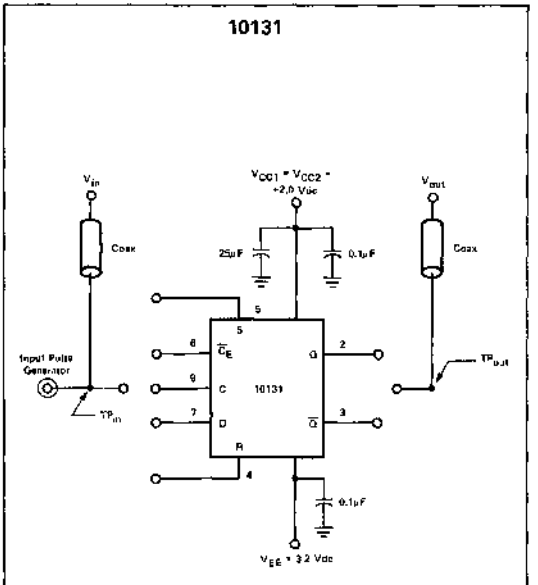
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

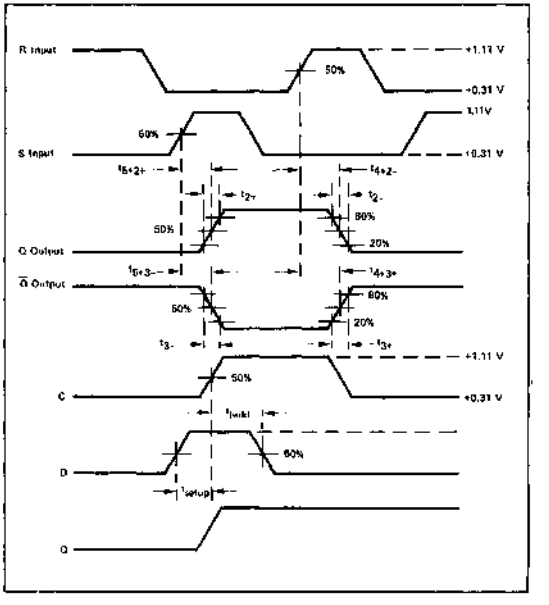
TOGGLE FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



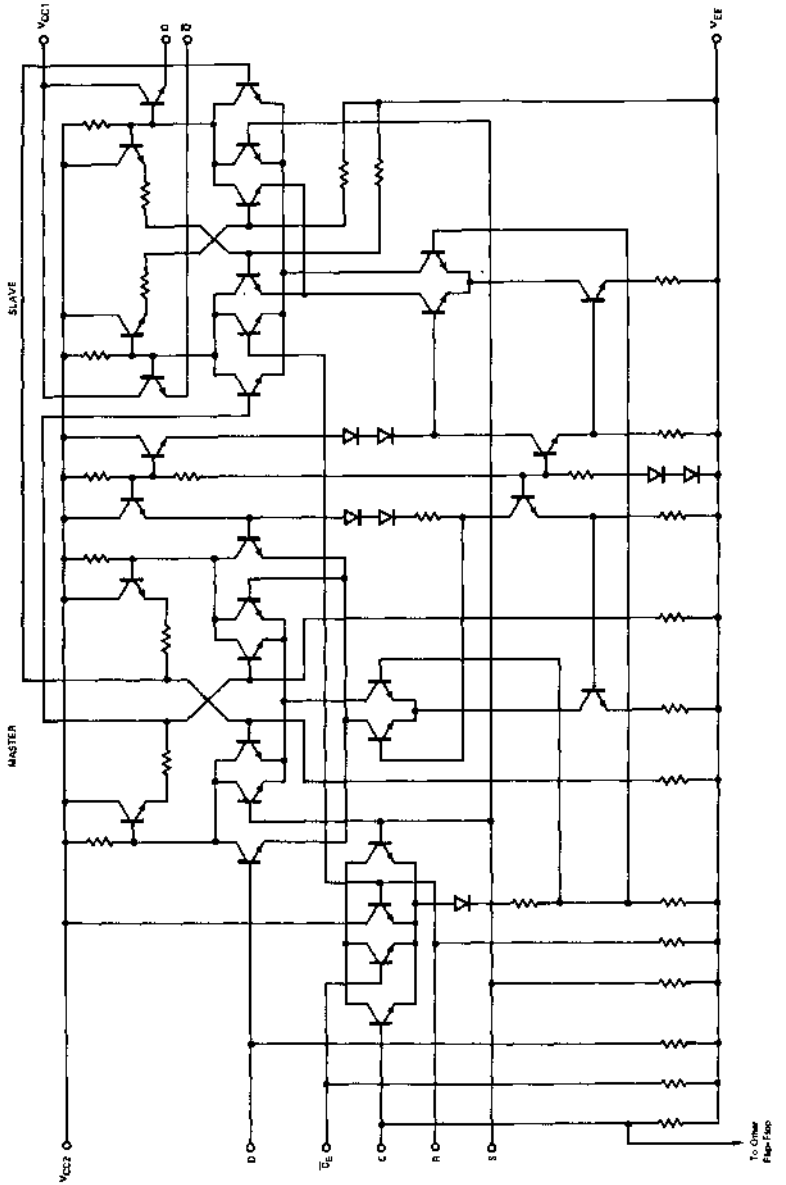
NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

CIRCUIT SCHEMATIC

10131
(1/2 OF CIRCUIT SHOWN)



signetics

DUAL MULTIPLEXER LATCH (WITH RESET) 10132

10132F: −30 TO +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

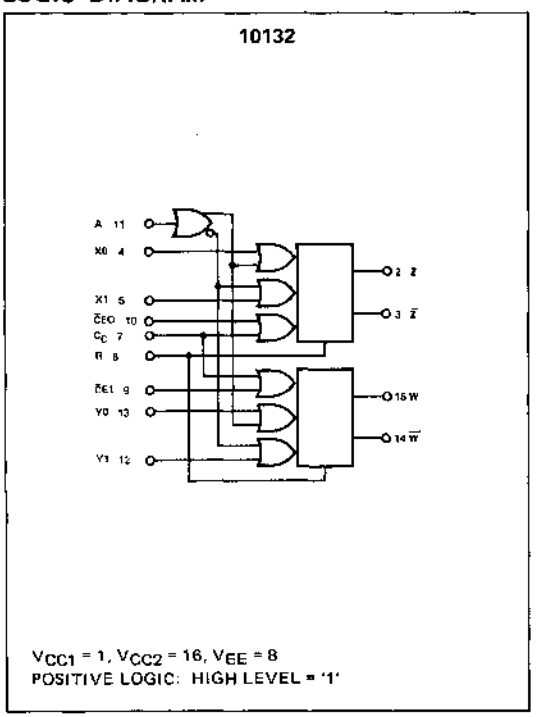
The 10132 is a dual clocked D-type latch with 2 to 1 data multiplexing. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this state, the enable inputs perform the function of enabling the common clock, (C_C).

Any change at the selected D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data or select inputs will not affect the output information.

The asynchronous reset input (R) overrides the clock inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

LOGIC DIAGRAM



FEATURES

- HIGH SPEED COMBINED MULTIPLEXER – LATCH IMPROVES SYSTEM PERFORMANCE.
- MULTIPLEXED INPUTS TO REDUCE PACKAGE COUNT
- FAST PROPAGATION DELAY = 2.5 ns TYP (DATA)
  = 3.7 ns TYP (SELECT)
  = 3.0 ns TYP (RESET)
  = 4.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 200 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

APPLICATIONS

- COMBINED MULTIPLEXER – REGISTER FOR:
  - high speed central processors
  - high speed peripherals
  - high speed minicomputers
  - high speed accumulators
  - communication systems

TRUTH TABLE

R	X_{in}	C_C	$\overline{CE}$	Z_{n+1}
L	L	L	L	L
L	L	L	H	Z_n
L	L	H	L	Z_n
L	L	H	H	Z_n
L	H	L	L	H
L	H	L	H	Z_n
L	H	H	L	Z_n
L	H	H	H	Z_n
H	φ	H	φ	L

φ = Don't Care.

$X_{in} = \overline{A} \cdot X0 + A \cdot X1$

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

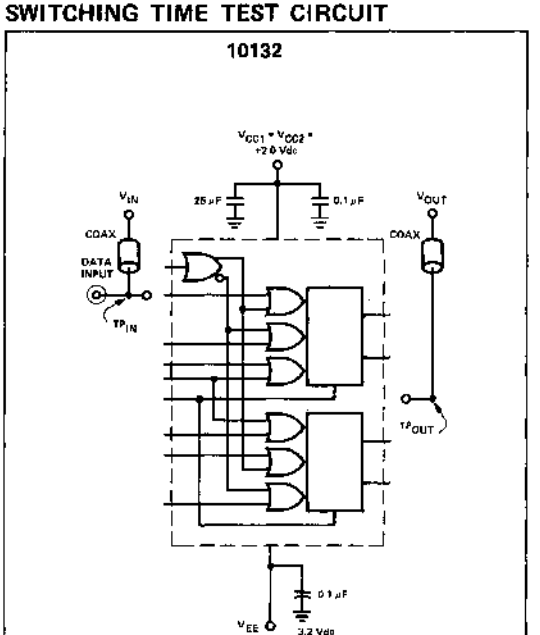
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

● Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	0.890	−1.890	−1.205	−1.600	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic		Symbol	Pin Under Test	10132 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Current		I_E	8	–	–	–	–	50	–	–	mAdc	7,11	–	–	–	8	1,16
Input Current		$I_{in\ H}$	4	–	–	–	–	290	–	–	μAdc	4	–	–	–	8	1,16
			5	–	–	–	–	290	–	–		5,11	–	–	–		
			6	–	–	–	–	390	–	–		6,7	–	–	–		
			7	–	–	–	–	290	–	–		7	–	–	–		
			10	–	–	–	–	220	–	–		10	–	–	–		
			11	–	–	–	–	220	–	–		11	–	–	–		
		$I_{in\ L}$	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage		V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4	7,9,10	–	–	8	1,16
			3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "0" Output Voltage		V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	7,9,11	–	–	8	1,16
			3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "1" Threshold Voltage		V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	7,9,10	4	–	8	1,16
			2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	11	7,8,10	5	–	8	1,16
Logic "0" Threshold Voltage		V_{OLA}	3	–	−1.655			−1.630	–	−1.595	Vdc		7,9,10	4	–	8	1,16
			3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	11	7,9,10	5	–	8	1,16
Switching Times (50-ohm load) (See Figure 1)												+1.11 V	+0.31 V	Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	Data	t_{4+2+}	2		–	–	2.5	–	–		ns	–	7,9,10	4	2	8	1,16
	Reset	t_{612-}		–	–	–	3.0	–	–	–		7	–	6			
	Clock	t_{7-2+}		–	–	–	4.0	–	–	–		4	–	7			
	Select	t_{11+2-}		–	–	–	3.7	–	–	–		5	7	11			
Setup Time	Data	t_{setup}	2	–	–	–	1.5	–	–	–	ns	–	11	4,10	2	8	1,16
	Select	t_{setup}	2	–	–	–	2.5	–	–	–	ns	5	7	10,11	2	8	1,16
Hold Time	Data	t_{hold}	2	–	–	–	0.0	–	–	–	ns	–	11	4,10	2	8	1,16
	Select	t_{hold}	2	–	–	–	−0.5	–	–	–	ns	5	7	10,11	2	8	1,16
Rise Time (20% to 80%)		t_{2+}	2	–	–	–	2.0	–	–	–	ns	–	7,9,10	4	2	8	1,16
Fall Time (20% to 80%)		t_{2-}	2	–	–	–	2.0	–	–	–	ns	–	7,9,10	4	2	8	1,16

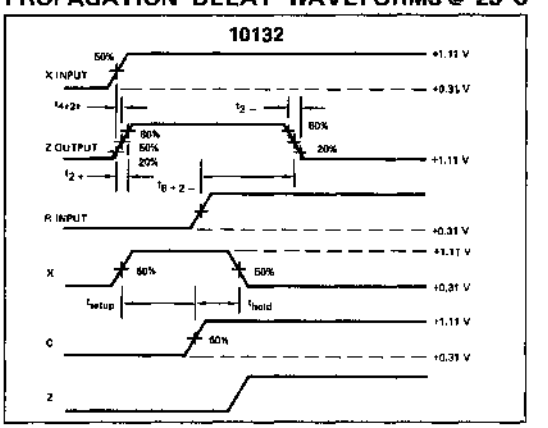
*All other inputs tested in the same manner.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

QUAD D-TYPE LATCH (WITH GATED OUTPUTS) 10133

10133F: −30 to +85°C, CERDIP

ADVANCED INFORMATION

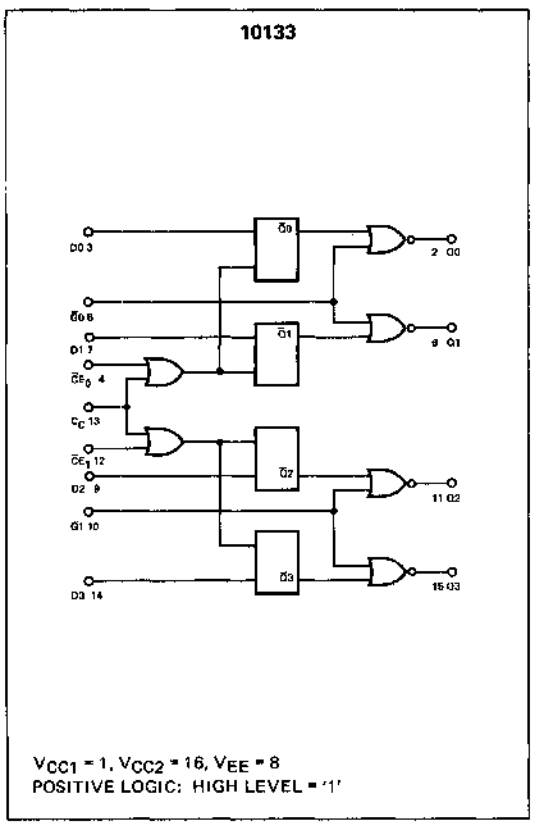
DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10133 is a high speed, low power, ECL quad latch consisting of four bistable latch circuits with D-type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is high, the outputs will follow the D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated low when the output enable is high. All four latches may be clocked at one time with the common clock, or each half may be clocked separately with its clock.

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

FEATURES

- FAST PROPAGATION DELAY
  - = 4.0 ns TYP CLOCK OR DATA TO OUTPUT
  - = 2.0 ns TYP ENABLE TO OUTPUT
  - = 0.7 ns TYP SETUP AND HOLD TIMES
- GATED OUTPUTS FOR BUS-ORIENTED APPLICATIONS
- HIGH DENSITY – FOUR LATCHES PLUS GATING
- LOW POWER DISSIPATION = 290 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE FOUR 50 Ω LINES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

APPLICATIONS

- TEMPORARY STORAGE ELEMENT IN:
  - high speed central processors
  - high speed peripherals and memories
  - high speed digital communications
  - instrumentation
  - test equipment
- BUS-ORIENTED STORAGE REGISTER FOR:
  - mini-computers
  - array processors

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

$C = \overline{C_C} + C_E$

ϕ = Don't Care

NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
2. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

ELECTRICAL CHARACTERISTICS

(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10133 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8				–	75	–	–	mAdc	–	13		–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	245	–	–	µAdc	3	–	–	–	8	1,16
		4					220				4					
		5	–	–	–	–	360	–	–		5	–	–	–		
	I_{inL}	3			0.5					µAdc		3			8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	3,4	–	–	–	8	1,16
		2									3,13					
		2									4	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	13			–	8	1,16
		2									3,5	–	–	–		
		2									13		–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080		−0.980	–	−0.910			Vdc	3,4			6	8	1,16
		2		–		–		–			4		3	–		
		2		–		–					3,4	–	–			
		2,1		–		–					3		–			
		2,11					–				–	–	–			
		2,1		–		–	–				–	–	–	4		
		2		–		–	–				3	–	4	–		
		2					–				3	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	3,4		5	–	8	1,16
		2	–								4			3		
		2	–			–		–			4	–	–			
		2,1	–			–					–	–	–			
		2,11	–					–			3	–	–			
		2,1	–			–					3			13		
Switching Times (Figure 1) (50 Ω load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–			4.0				ns	4		3	2	8	1,16
	t_{4+2+}	2	–	–	–	4.0	–	–	–		3	–	4	7		
	t_{5-2-}	2	–	–		2.0	–	–	–		–	–	5	2		
	t_{setup}*	3	–		–	0.7	–	–			–	–	3	2		
	t_{hold}**	3		–	–	0.7	–	–	–		–		3	2		
Rise Time (20% to 80%)	t_{2+}	2	–	–		2.0	–	–	–		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	–			2.0	–	–	–		4	–	3	2		

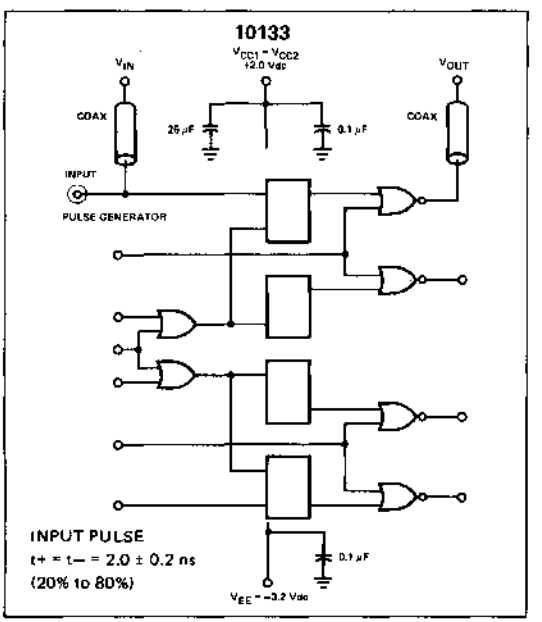
†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

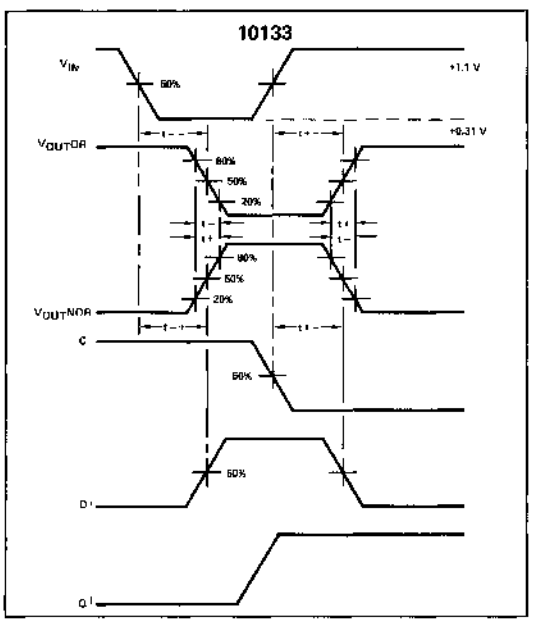
*t_{setup} is minimum time before the negative transition of the clock pulse (C) that information must be present at the data input (D).

**t_{hold} is the minimum time after the negative transition of the clock pulse (C) that information must remain unchanged at the data input (D).

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



signetics

DUAL MULTIPLEXER - LATCH (WITH INDEPENDANT SELECTS) 10134

10134F: −30 to +85°C CERDIP

DIGITAL 10,000 SERIES ECL

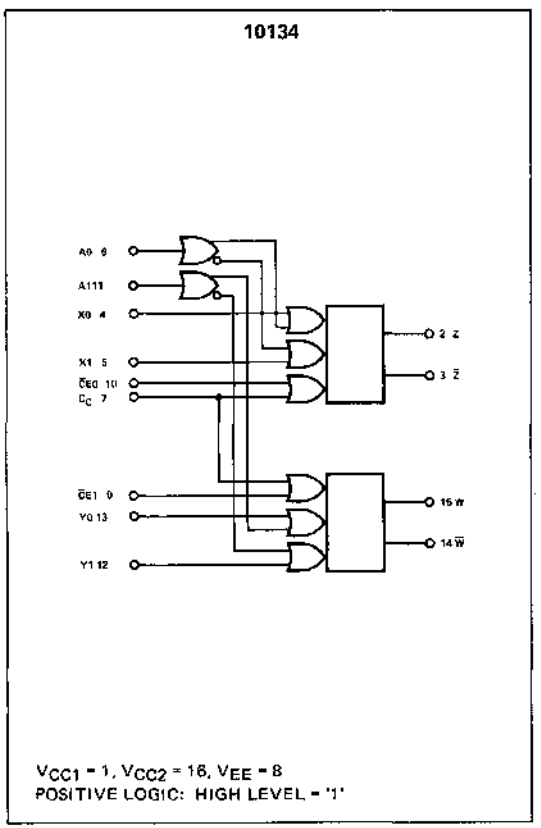
DESCRIPTION

The 10134 is a dual clocked D-type latch with 2 to 1 data multiplexing. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this state, the enable inputs perform the function of enabling the common clock (C_C).

Any change at the selected D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data or select inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

LOGIC DIAGRAM



FEATURES

- HIGH SPEED COMBINED MULTIPLEXER — LATCH IMPROVES SYSTEM PERFORMANCE.
- MULTIPLEXED INPUTS TO REDUCE PACKAGE COUNT
- FAST PROPAGATION DELAY = 2.5 ns TYP (DATA)
  = 3.5 ns TYP (SELECT)
  = 4.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 225 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY — CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

APPLICATIONS

- COMBINED MULTIPLEXER — REGISTER FOR:
  - high speed central processors
  - high speed peripherals
  - high speed minicomputers
  - high speed accumulators
  - communication systems

TRUTH TABLE

C	A0	X0	X1	Z_{n+1}
L	L	L	φ	L
L	L	H	φ	H
L	H	φ	L	L
L	H	φ	H	H
H	φ	φ	φ	Z_n

φ = Don't Care
$C = \overline{CE} + C_C$
$X_{in} = \overline{A0} \cdot X0 + A0 \cdot X1$

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS

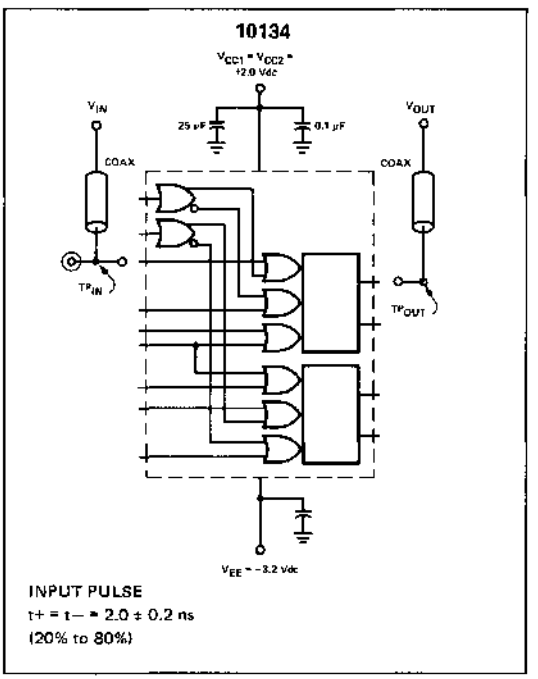
(At Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.600	−5.2
+25°C	0.810	1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.625	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10134 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Limit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	8,7,11	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	290	–	–	µAdc	4	–	–	–	8	1,16
		5			–	290	–	–		5,6					
		6	–	–	–	220	–	–		6	–		–		
		7	–	–	–	290	–	–		7	–	–	–		
		10	–	–	–	220	–	–		10	–	–	–		
	$I_{in\ L}$	4*	–	–	0.50	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	4	6,7,10	–		8	1,16
		2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	5,6	7,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	–	4,6,7,10	–	–	8	1,16
		2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	6	5,7,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	−0.910	–	Vdc	–	6,7,10	4	–	8	1,16
		2	−1.080	–	−0.980	–	−0.910	–	Vdc	5	7,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	−1.630	–	−1.595	Vdc	–	6,7,10	–	4	8	1,16
		2	–	1.655	–	−1.630	–	1.595	Vdc	5	7,10		5	8	1,16
Switching Times (50-ohm load) (See Figure 1)					Typ	Max				+1.11 V	+0.31 V	Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	–	–	2.5	–	–	–	ns	–	6,7,10	4	2	8	1,16
Clock	t_{10-2+}		–	–	4.0	–	–	–		4	7	10			
Select	t_{5e2+}		–	–	3.5	–	–	–		5	7,10	5			
Setup Time Data	t_{setup}	2	–	–	1.5	–	–	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{setup}	2	–	–	2.5	–	–	–	ns	5	7,11	6,10	2	8	1,16
Hold Time Data	t_{hold}	2	–	–	0.0	–	–	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{hold}	2	–	–	−0.5	–	–	–	ns	5	7,11	6,10	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	2.0	–	–	–	ns	–	6,7,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–		2.0	–	–		ns	–	6,7,10	4	2	8	1,16

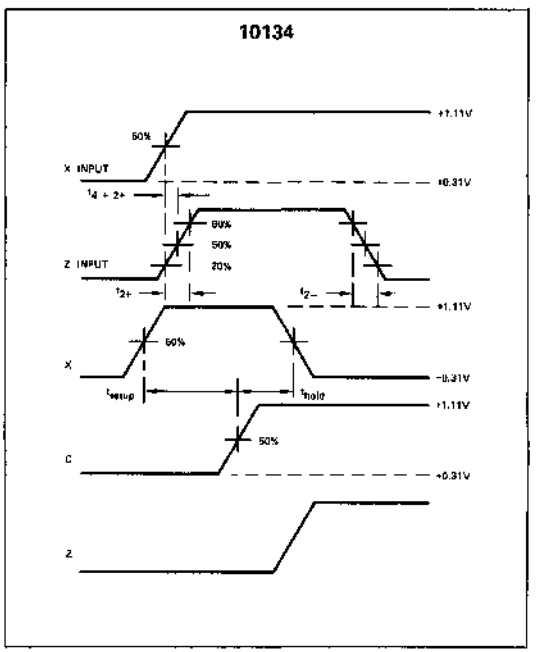
*All other inputs tested in the same manner

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

UNIVERSAL HEXADECIMAL COUNTER
UNIVERSAL DECIMAL COUNTER

10136
10137

ADVANCE INFORMATION
TO BE ANNOUNCED

10136F, 10137F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10136 and 10137 are high speed synchronous counters that can count up, count down, preset, or stop count at rates exceeding 100 MHz.

The 10136 is a 16-state (Hexadecimal) counter and the 10137 is a 10-state (Decade) counter.

The flexibility of these devices allows the designer to use one basic counter design for all applications. The synchronous count feature makes these MSI parts suitable for either computers or instrumentation.

The carry input enables the counter, and prevents it from changing state when the clock goes high. The inputs S1 and S2 control the state of the counter: stop count, increment (count up), decrement (count down), and preset (program) count. The other inputs are clock, and the four D inputs for presetting the counter.

The outputs include four Q's and a carry out which goes low on the terminal count. When an output is not needed, it can be left open to conserve system power.

The counter changes state only on the positive-going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The next state of the counter is determined by the configuration of the inputs only during the positive transition of the clock.

APPLICATIONS

Either the binary counter (10136) or the decade counter (10137) can be useful in high speed central processors and peripheral controllers, mini-computers, high speed digital communication equipment, and instrumentation.

When used as a prescaler, it is possible to extend the input frequency of the 10136, 37 to over 200 MHz with the 10231.

FUNCTION SELECT TABLE

S1	S2	OPERATING MODE
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

TEMPERATURE RANGE

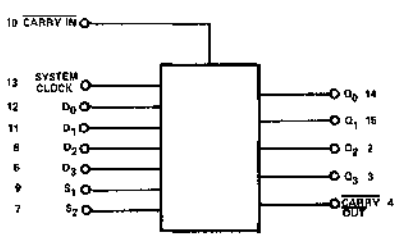
- −30 to +85°C Operating Ambient

PACKAGE TYPE

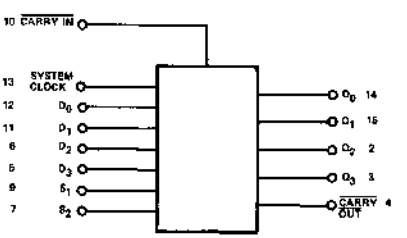
- F: 16-Pin CERDIP

BLOCK DIAGRAMS

10136



10137



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

signetics

FOUR-BIT UNIVERSAL SHIFT REGISTER | 10141

ADVANCE INFORMATION
TO BE ANNOUNCED

10141F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

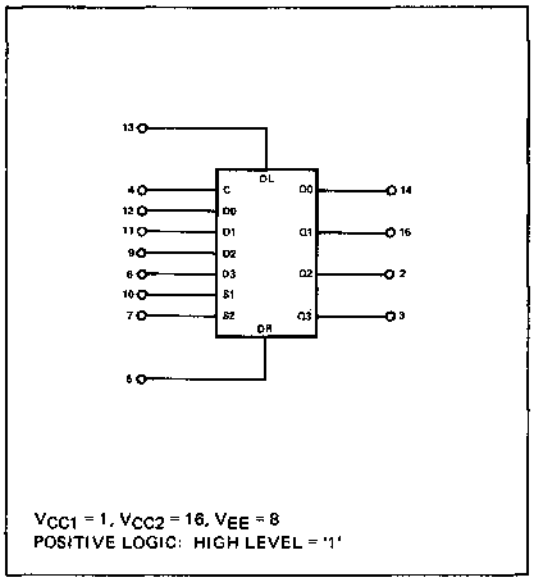
DESCRIPTION

The 10141 is a four bit universal shift register. The register performs shift left or right, serial/parallel in and serial/parallel out with no external gating. This device is useful for counting, temporary storage, and shifting in high speed digital communication systems, instrumentation, peripheral controllers and computers.

Inputs S1 and S2 control the four possible operations of the register without interfering with the clock. The flip-flops shift information on the positive edge of the clock. The four operations are: stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs: four for parallel data entry, one for shifting in from the left (DL), and one for shifting in from the right (DR). When the register is used for serial output only, the unused emitter-follower outputs can be left open.

The 10141 is capable of 200 MHz shift rate operation (typical).

BLOCK DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

TRUTH TABLE

PULSE	INPUTS								OUTPUTS*			
	S1	S2	D3	D2	D1	D0	DR	DL	Q3	Q2	Q1	Q0
0	L	L	L	H	H	L	X	X	—	—	—	—
1	L	L	L	H	H	L	X	X	L	H	H	L
2	L	L	H	L	L	H	X	X	H	L	L	H
3	L	L	H	H	L	L	X	X	H	H	L	L
4	L	H	X	X	X	X	L	X	L	H	H	L
5	L	H	X	X	X	X	H	X	H	L	H	H
6	L	H	X	X	X	X	L	X	L	H	L	H
7	L	H	X	X	X	X	L	X	L	L	H	L
8	H	L	X	X	X	X	X	L	L	H	L	L
9	H	L	X	X	X	X	X	H	H	L	L	H
10	H	L	X	X	X	X	X	H	L	L	H	H
11	H	L	X	X	X	X	X	L	L	H	H	L
12	H	L	X	X	X	X	X	L	H	H	L	L
13	H	H	X	X	X	X	X	X	H	H	L	L
14	H	H	X	X	X	X	X	X	H	H	L	L

*Outputs as exist after pulse appears at "C" input with input conditions as shown.

(Pulse = Positive transition of clock input)
X = Don't Care

FUNCTION TABLE

FUNCTION TABLE		
SELECT		
S1	S2	OPERATING MODE
L	L	Parallel Entry
L	H	Shift Right
H	L	Shift Left
H	H	Stop Shift

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

signetics

12-BIT PARITY CHECKER-GENERATOR CIRCUIT | 10160

ADVANCE INFORMATION
TO BE ANNOUNCED

10160 F: −30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10160 is a high performance parity circuit constructed with nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation.

Input pulldown resistors ensure that the unconnected inputs are pulled to low logic level allowing parity detection and generation for less than 12 bits.

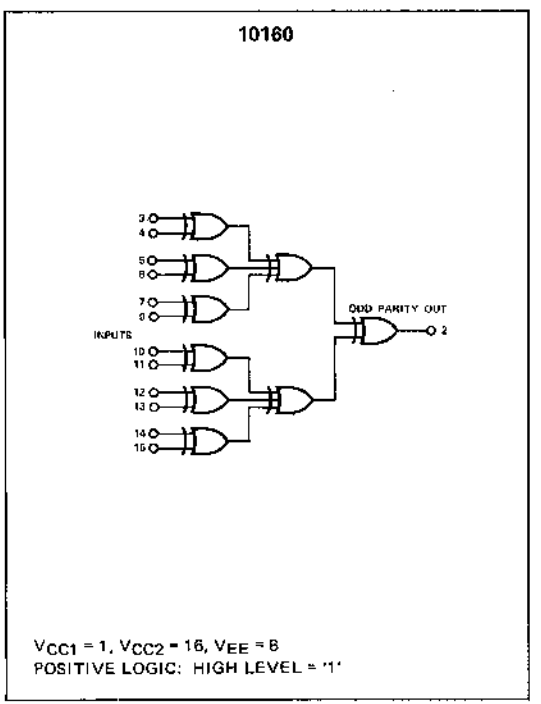
The Output goes high with ODD parity on input pins 3 through 15. (That is, if there are 1,3,5,7,9 or 11 '1's on these inputs).

Expansion for word lengths greater than 12 bits can be achieved by connecting to the carry inputs of the 10170 Parity Circuit or by using 10107 or 10113 EXCLUSIVE-OR gates.

FEATURES

- HIGH FUNCTIONAL DENSITY ON ONE CHIP REDUCES PACKAGE COUNT AND SAVES SYSTEM POWER
- FAST PROPAGATION DELAY = 4.0 ns TYP
- LOW POWER DISSIPATION = 325 mW/PACKAGE TYPE (NO LOAD)
- HIGH FANOUT CAPABILITY — CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- CONTROLLED OUTPUT RISE AND FALL TIMES —2.0 ns TYP (20% TO 80%)(ALL OUTPUTS LOADED)
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

ELECTRICAL CHARACTERISTICS

Conditions: T_A = 25°C, V_{EE} = −5.2 V ±1%

1. I_E = 62 mA dc typ.
   = 78 mA dc max.
2. I_{inH} = 265 μA dc max. (pin 3 etc.)
   = 220 μA dc max. (pin 4 etc.)

Conditions: T_A = 25°C, V_{CC} = +2.0 V ±1%, V_{EE} = −3.2 V ±1%, 50 Ω loads

3. t_{pd} = 4.0 ns typ.
4. t_r, t_f = 2.0 ns typ. (20% to 80%)

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

signetics

1 OF 8 DEMULTIPLEXER/DECODER (SELECTED OUTPUT IS LOW) 10161

10161F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

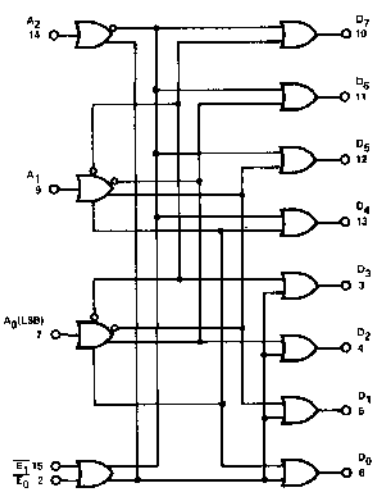
DESCRIPTION

The 10161 is a binary coded 3 line to 8 line decoder. Outputs are normally high with the selected output going low. Two enable inputs make it ideally suited for demultiplexer applications. One of the two enable inputs can be used as the data enable input. Either enable input when high, forces all outputs high.

The 10161 is a true parallel decoder using internal emitter dotting techniques. Hence it eliminates unequal delay times found in other decoders. The 10161 is a low power, high speed device with high Z input pulldown resistors and open emitter outputs.

LOGIC DIAGRAM

10161



(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- FAST PROPAGATION DELAY
  = 4.0 ns TYP ADDRESS TO OUTPUT
  = 4.5 ns TYP ENABLE TO OUTPUT
- LOW POWER DISSIPATION = 295 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE EIGHT 50 Ω LINES
- TRUE PARALLEL DECODER – ELIMINATES UNEQUAL DELAY TIMES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- OPEN EMITTER OUTPUTS
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

APPLICATIONS

- 1 of 8 Decoder
- 1 line to 8 line Demultiplexer

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	E0	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	φ	φ	φ	H	H	H	H	H	H	H	H
L	H	φ	φ	φ	H	H	H	H	H	H	H	H
H	H	φ	φ	φ	H	H	H	H	H	H	H	H

φ = Don't Care.

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

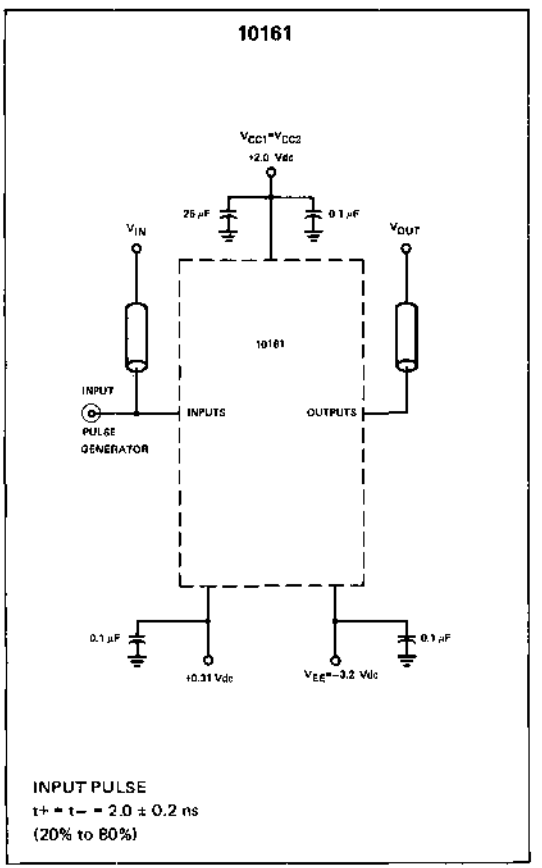
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10161 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8	–	–	–	57	72	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	265	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	2	–			8	1,16
		13	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	14		–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	−1.060	–	−0.960	–	–	−0.810	–	Vdc	–	–	2	–	8	1,16
		13	−1.060	–	−0.960	–	–	−0.810	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	14	–	8	1,16
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t14+ 13−	13	–	–	–	4.0	–	–	–	ns	–	–	14	13	8	1,16
	t14− 13+	13	–	–	–	4.0	–	–	–		–	–				
Rise Time (20% to 80%)	t13+	13	–	–	–	2.0	–	–	–		–	–				
Fall Time (20% to 80%)	t13−	13	–	–	–	2.0	–	–	–		–	–				

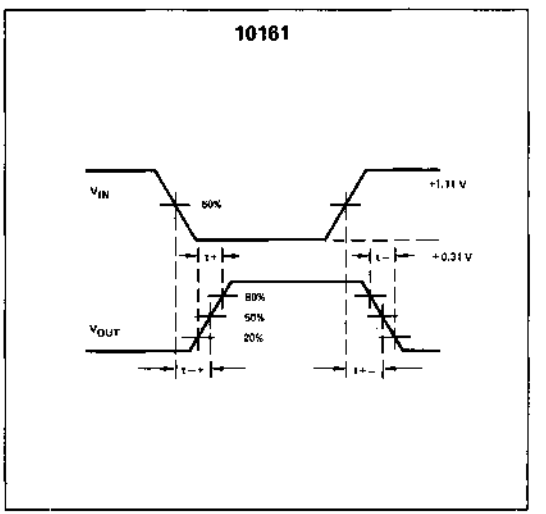
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

1 OF 8 DEMULTIPLEXER/DECODER (SELECTED OUTPUT IS HIGH) 10162

10162F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

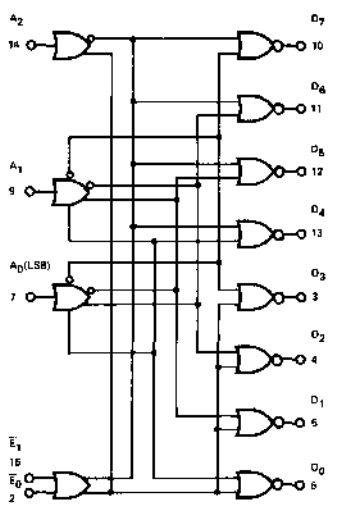
DESCRIPTION

The 10162 is a binary coded 3 line to 8 line decoder. Outputs are normally low with the selected output going high. Two enable inputs make it ideally suited for demultiplexer applications. One of the two enable inputs can be used as the data enable input. Either enable input when high, forces all outputs low.

The 10162 is a true parallel decoder using internal emitter dotting techniques. Hence it eliminates unequal delay times found in other decoders. The 10162 is a low power, high speed device with high Z input pulldown resistors and open emitter outputs.

LOGIC DIAGRAM

10162



(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- FAST PROPAGATION DELAY
  = 4.0 ns TYP ADDRESS TO OUTPUT
  = 4.5 ns TYP ENABLE TO OUTPUT
- LOW POWER DISSIPATION = 295 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE EIGHT 50 Ω LINES
- TRUE PARALLEL DECODER – ELIMINATES UNEQUAL DELAY TIMES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- OPEN EMITTER OUTPUTS
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

APPLICATIONS

- 1 of 8 Decoder
- 1 line to 8 line Demultiplexer

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E1}$	$\overline{E0}$	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	L	φ	φ	φ	L	L	L	L	L	L	L	L
L	H	φ	φ	φ	L	L	L	L	L	L	L	L
H	H	φ	φ	φ	L	L	L	L	L	L	L	L

φ = Don't Care.

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

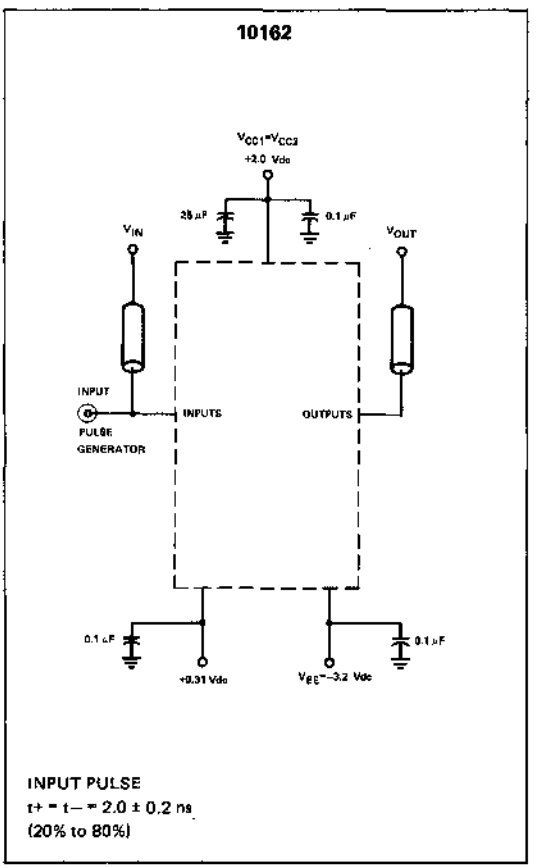
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10162 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	$\|V_{CC}\|$ Gnd
Power Supply Drain Current	I_E	8	–	–	–	57	72	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	266	–	–	µAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	2	–	–	–	8	1,16
		13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	−1.060	–	−0.960	–	–	−0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13		−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	2	–	8	1,16
		13	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	15	–	8	1,16
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t14− 13−	13	–	–	–	4.0	–	–	–	ns	–	–	14	13	8	1,16
	t14− 13−	13	–	–	–	4.0	–	–	–	ns	–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t+	13	–	–	–	2.0	–	–	–	ns	–	–				
Fall Time (20% to 80%)	t−	13	–	–	–	2.0	–	–	–	ns	–	–				

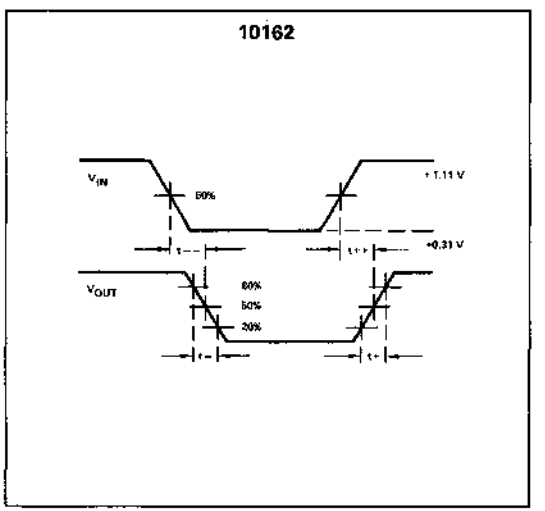
*Unused outputs connected to 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

8 LINE TO 1 LINE MULTIPLEXER (WITH ENABLE) 10164

10164F: –30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

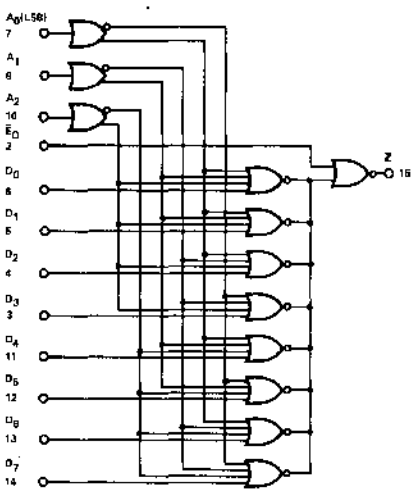
The 10164 is a high speed, low power 8 to 1 multiplexer/data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion. The 10164 has high Z input pulldown resistors and open emitter outputs.

FEATURES

- FAST PROPAGATION DELAY
  - = 3.5 ns TYP DATA TO OUTPUT
  - = 5.0 ns TYP ADDRESS TO OUTPUT
  - = 2.0 ns TYP ENABLE TO OUTPUT
- OUTPUT ENABLE TO PERMIT OUTPUT BUSSING
- LOW POWER DISSIPATION = 290 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE A 50 Ω LINE
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

LOGIC DIAGRAM

10164



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

APPLICATIONS

- 8 to 1 Multiplexer
- 8 to 1 Data Selector
- Parallel to Serial Conversion
- Barrel Shift Logic

TRUTH TABLE

ENABLE	ADDRESS INPUTS			Z
	A2	A1	A0	
L	L	L	L	D0
L	L	L	H	D1
L	L	H	L	D2
L	L	H	H	D3
L	H	L	L	D4
L	H	L	H	D5
L	H	H	L	D6
L	H	H	H	D7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

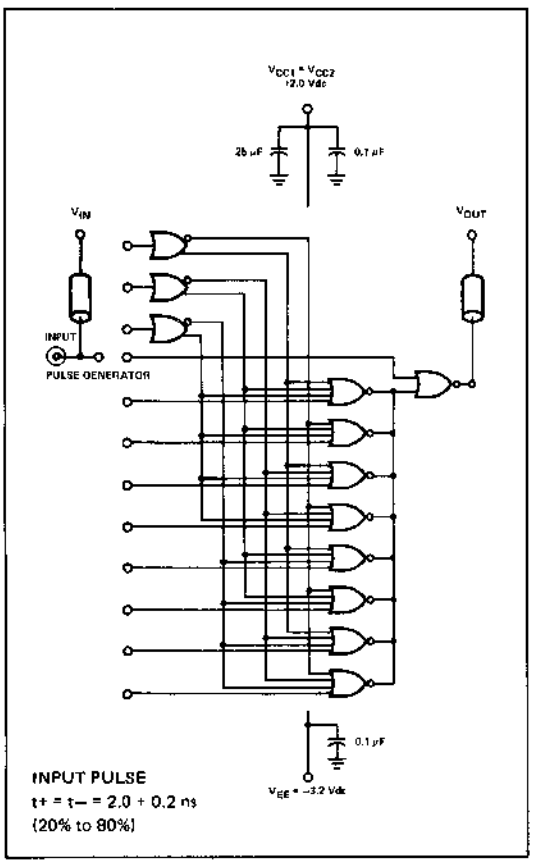
ELECTRICAL CHARACTERISTICS

(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

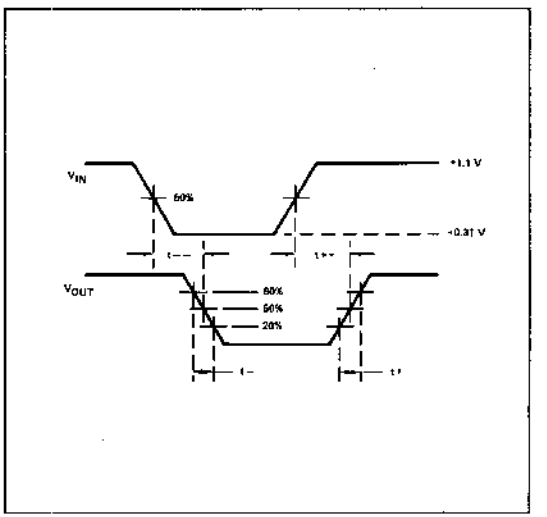
Characteristic	Symbol	Pin Under Test	10164 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	V_{CC1} and V_{CC2}
Power Supply Drain Current	I_E	8	–	–	–	55	75	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	220	–	–	µAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc		4		–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	−1.050	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	1.890	1.675	1.860		−1.650	1.825	1.615	Vdc	9			–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	−1.080	–	−0.960	–	–	−0.910	–	Vdc	4,9	–	–	2	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	−1.655	–		1.630		1.595	Vdc	9			2	8	1,16
Switching Times* (50 Ωload)											+1.11 V		Pulse In	Pulse Out	−5.2 V	+2.0 V
Propagation Delay	t_{4+} t_{5+}	15	–	–	–	3.5	–	–	–	ns	9	–	4	15	8	1,16
	t_{4-} t_{5-}	15	–	–	–	3.5	–	–	–		9	–	4			
	t_{7+} t_{5+}	15	–	–	–	5.0	–	–	–		5	–	7			
	t_{7-} t_{5-}	15	–	–	–	5.0	–	–	–		5	–	7			
	t_{2+} t_{5+}	15		–	–	2.0	–	–	–		7,5		2			
	t_{2-} t_{6+}	15	–	–	–	2.0	–	–	–		7,5	–	2			
Rise Time (20% to 80%)	t_+	15	–	–	–	2.0	–	–	–		9	–	4			
Fall Time (20% to 80%)	t_-	15	–	–	–	2.0	–	–	–		9		4			

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t_+ = t_- = 2.0 + 0.2$ ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope channel input.
3. Test procedures are shown for only one input or for one set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

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9-BIT PARITY CIRCUIT (WITH 2 CARRY INPUTS) 10170

ADVANCE INFORMATION

10170F: –30 TO +85°C, CERDIP

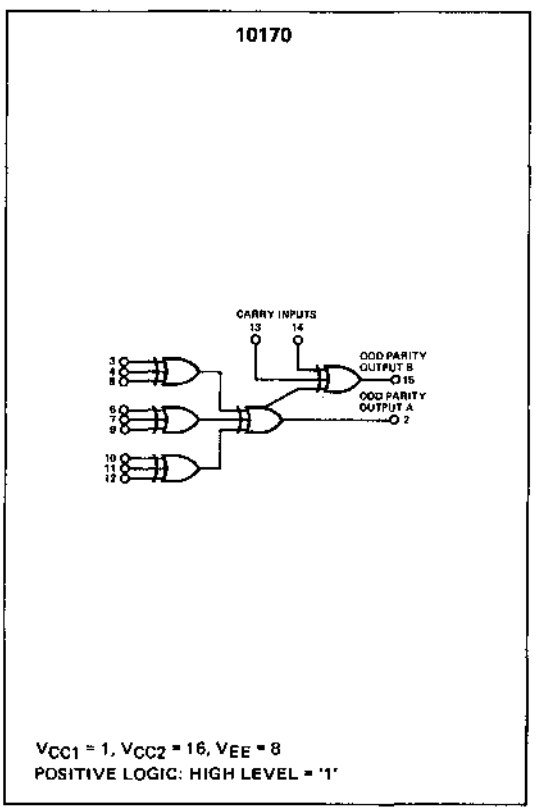
DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10170 is a high performance parity circuit constructed with triple EXCLUSIVE-OR gates. The function is optimized for use in byte organized systems. The device can generate or check 9 bits of parity in 2 gate delays. Larger word lengths to 27 bits can be checked in 3 gate delays by connecting output A of other 10170's to the carry inputs. The carry inputs may also be used for ODD/EVEN parity control.

Output A goes high with ODD parity on input pins 3 through 12. (That is if there are 1,3,5,7, or 9 '1's on these inputs). Output B goes high for ODD parity on output A and carry input pins 13 and 14. (That is if there are 1,3,5,7,9 or 11 '1's on input pins 3 through 14).

LOGIC DIAGRAM



FEATURES

- OPTIMIZED FOR BYTE-ORGANIZED SYSTEMS
- FAST PROPAGATION DELAY
  - = 4.0 ns TYP (INPUT TO OUTPUT A)
  - = 6.0 ns TYP (INPUT TO OUTPUT B)
  - = 2.0 ns TYP (CARRY TO OUTPUT B)
- CARRY INPUTS FOR EASY EXPANSION OR ODD/EVEN CONTROL
- UP TO 9 BIT CHECK IN 4.0 ns
- UP TO 27 BIT CHECK IN 6.0 ns WITH NO ADDITIONAL GATES REQUIRED
- LOW POWER DISSIPATION = 280 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER OUTPUTS FOR LOGIC AND BUSSING CAPABILITY

ELECTRICAL CHARACTERISTICS

Conditions: T_A = 25°C, V_{EE} = –5.2 V ±1%

1. I_E = 54 mA dc, typ.
2. I_{inH} = 265 μA dc, max.

Conditions: T_A = 25°C, V_{CC} = +2.0 V±1%, V_{EE} = –3.2 V ±1%, 50 Ω loads

3. t_{pd} = 4.0 ns (inputs to output A)
   = 6.0 ns (inputs to output B)
   = 2.0 ns (carry to output B)
4. t_r, t_f = 2.0 ns typ. (20% to 80%)

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

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DUAL 1 OF 4 DEMULTIPLEXER/DECODER (SELECTED OUTPUT IS LOW) 10171

10171F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

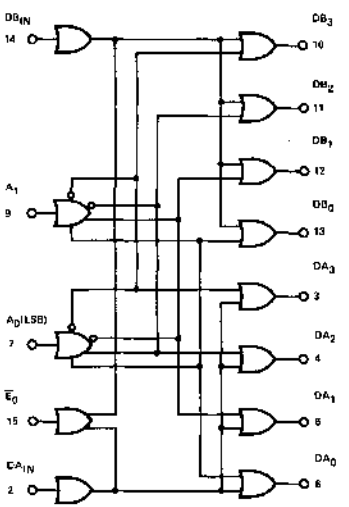
DESCRIPTION

The 10171 is a binary coded 2 line to dual 4 line decoder/demultiplexer. Outputs are normally high with the selected outputs going low. There are two parallel 1 line to 4 line non-inverting data paths and a common enable input. Each data input when high forces its four outputs high. The enable input when high forces all eight outputs high.

The 10171 is a true parallel decoder using internal emitter dotting techniques. Hence it eliminates unequal delay times found in other decoders. The 10171 is a low power, high speed device with high Z input pulldown resistors and open emitter outputs.

LOGIC DIAGRAM

10171



(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- FAST PROPAGATION DELAY
  = 4.0 ns TYP ADDRESS TO OUTPUT
  = 4.5 ns TYP ENABLE OR DATA TO OUTPUT
- LOW POWER DISSIPATION = 310 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE EIGHT 50 Ω LINES
- TRUE PARALLEL DECODER – ELIMINATES UNEQUAL DELAY TIMES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- OPEN EMITTER OUTPUTS
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

APPLICATIONS

- Dual 1 line to 4 line Demultiplexer
- Crossbar Switch Applications
- High Fanout 1 of 4 Decoder
- Memory Chip Select Decoder

TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{E0}$	A1	A0	DAIN	DA0	DA1	DA2	DA3
L	L	L	L	L	H	H	H
L	L	L	H	H	H	H	H
L	L	H	L	H	L	H	H
L	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H
L	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L
L	H	H	H	H	H	H	H
H	φ	φ	φ	H	H	H	H

DB is Similar. φ = Don't Care.

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS

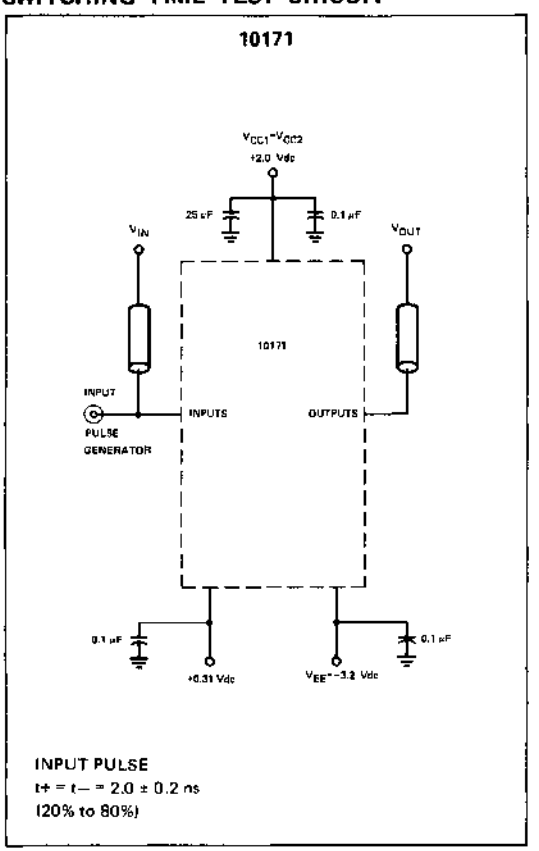
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

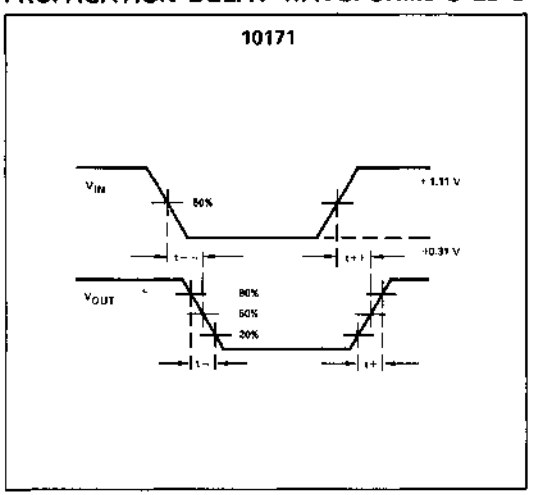
Characteristic	Symbol	Pin Under Test	10171 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14		–		–	265			µAdc	14		–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	−1.050	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	14		–	–	8	1,16
		13	−1.050	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	14	–	8	1,16
		13	−1.080	–	−0.980		–	−0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	14	8	1,16
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{p+}	13	–	–	–	4.0	–	–	–	ns	–	–	9	13	8	1,16
	t_{p-}	13	–	–	–	4.0	–	–	–		–	–				
Rise Time (20% to 80%)	t_{13+}	13	–	–	–	2.0	–	–	–		–	–				
Fall Time (20% to 80%)	t_{13-}	13	–	–	–	2.0	–	–	–		–	–				

*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

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DUAL 1 OF 4 DEMULTIPLEXER/DECODER (SELECTED OUTPUT IS HIGH) 10172

10172F: –30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10172 is a binary coded 2 line to 4 line decoder/demultiplexer. Outputs are normally low with the selected outputs going high. The enable input when high forces all eight outputs low. Each data input when low forces its four outputs low. Hence, when using as a decoder the data inputs should be connected to a logic "1" level. Data paths are non-inverting.

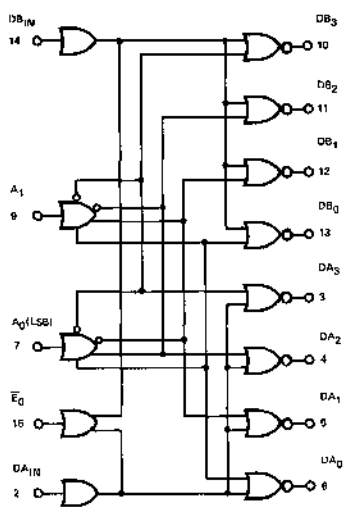
The 10172 is a true parallel decoder using internal emitter dotting techniques. Hence it eliminates unequal delay times found in other decoders. The 10172 is a low power, high speed device with high Z input pulldown resistors and open emitter outputs.

FEATURES

- FAST PROPAGATION DELAY
  = 4.0 ns TYP ADDRESS TO OUTPUT
  = 4.5 ns TYP ENABLE OR DATA TO OUTPUT
- LOW POWER DISSIPATION = 310 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE EIGHT 50 Ω LINES
- TRUE PARALLEL DECODER – ELIMINATES UNEQUAL DELAY TIMES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- OPEN EMITTER OUTPUTS
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

LOGIC DIAGRAM

10172



(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

APPLICATIONS

- Dual 1 line to 4 line Demultiplexer
- Crossbar Switch Applications
- High Fanout 1 of 4 Decoder
- Memory Chip Select Decoding

TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{E0}$	A1	A0	DA IN	DA0	DA1	DA2	DA3
L	L	L	H	H	L	L	L
L	L	L	L	L	L	L	L
L	L	H	H	L	H	L	L
L	L	H	L	L	L	L	L
L	H	L	H	L	L	H	L
L	H	L	L	L	L	L	L
L	H	H	H	L	L	L	H
L	H	H	L	L	L	L	L
H	ϕ	ϕ	ϕ	L	L	L	L

DB is Similar. ϕ = Don't Care

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS

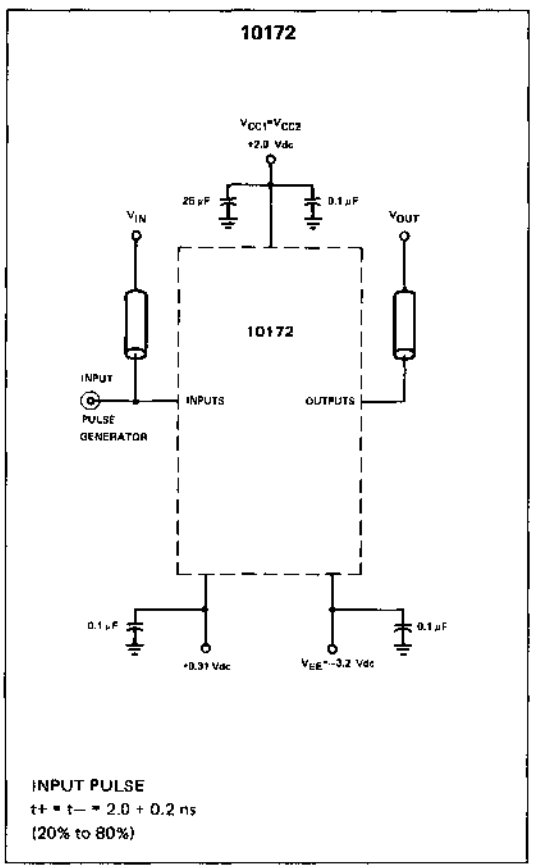
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10172 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	265	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	−0.60	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	–	–	–	8	1,16
		13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	9,14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	−1.658	–	–	−1.630	–	−1.595	Vdc	–	–	–	14	8	1,16
		13	–	−1.666	–	–	−1.630	–	−1.596	Vdc	–	–	9	–	8	1,16
Switching Times * (50 ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{pl} 13−	13	–	–	–	4.0	–	–	–	ns	–	–	9	13	8	1,16
	t_{p} − 13−	13	–	–	–	4.0	–	–	–		–	–				
Rise Time (20% to 80%)	t_+	13	–	–	–	2.0	–	–	–		–	–				
Fall Time (20% to 80%)	t_-	13	–	–	–	2.0	–	–	–		–	–				

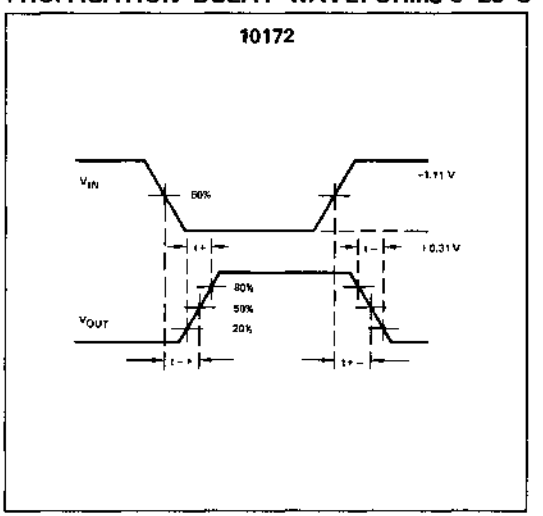
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t_+ = t_- = 2.0 \pm 0.2$ ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

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QUAD 2 TO 1 MULTIPLEXER - LATCH 10173

10173F: –30 TO +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

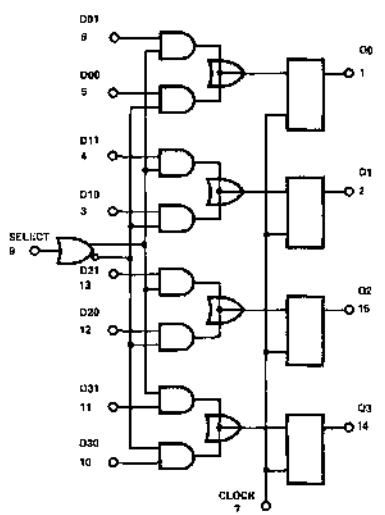
The 10173 is a quad clocked D-type latch with 2 to 1 data multiplexing.

Any change at the selected D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data or select inputs will not affect the output information.

When the select input is false, the D_n0 inputs are selected and when select is true the D_n1 inputs are selected. As a quad 2-Input Multiplexer, with the added feature of a latch output, the 10173 provides the data select and store function in the same package. The result is a savings in system delay and package count.

LOGIC DIAGRAM

10173



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- SIMULTANEOUS MULTIPLEXING AND LATCHING FUNCTION IMPROVES SYSTEM PERFORMANCE
- QUAD LATCH AND MULTIPLEXER ON ONE CHIP INCREASES SYSTEM DENSITY
- FAST PROPAGATION DELAY
  = 2.5 ns TYP (DATA TO OUTPUT)
  = 3.7 ns TYP (SELECT TO OUTPUT)
  = 4.3 ns TYP (CLOCK TO OUTPUT)
- LOW POWER DISSIPATION = 325 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩPULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER OUTPUTS – ALLOW WIRE OR AND DATA BUSSING

APPLICATIONS

COMBINED MULTIPLEXER – REGISTER FOR:
- high speed central processors
- high speed peripherals
- high speed minicomputers
- communication systems
- instrumentation

TRUTH TABLE

D_n	C	Q_n (N + 1)
L	L	L
H	L	H
ϕ	H	Q_n (N)

$D_n = \overline{S} \cdot D_{n0} + S \cdot D_{n1}$
ϕ = Don't Care.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16 Pin CERDIP

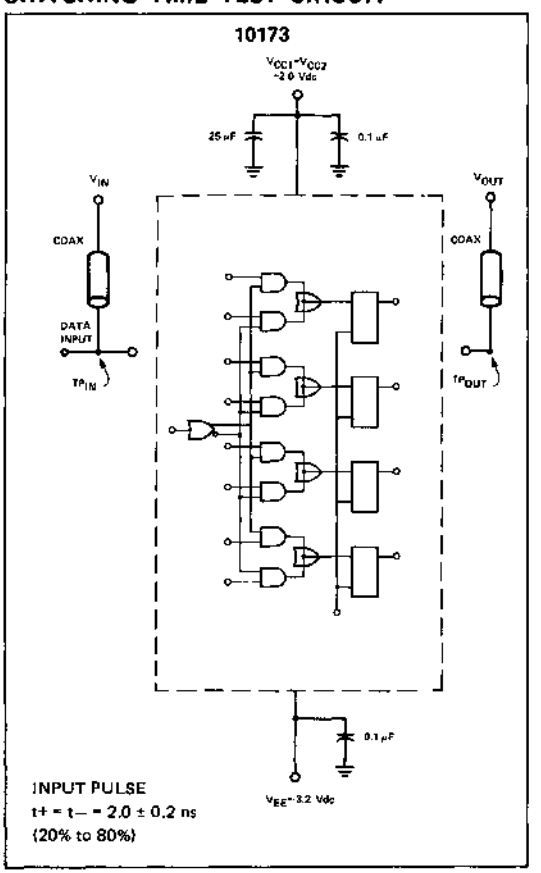
ELECTRICAL CHARACTERISTICS
(At Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	1.500	5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.826	−1.035	−1.440	−5.2

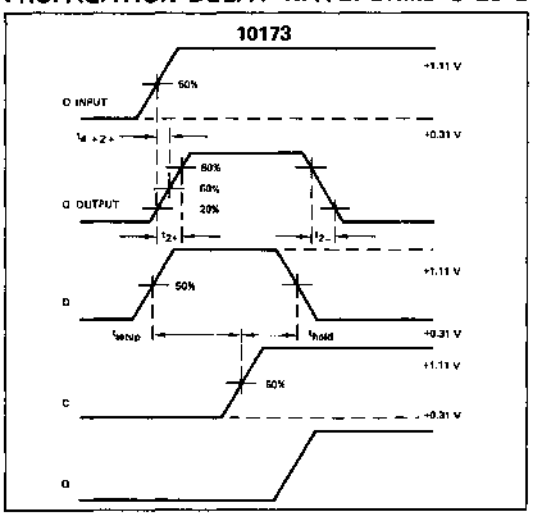
Characteristic	Symbol	Pin Under Test	10173 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	78	–	–	mAdc	7,9	–	–	–	8	16
Input Current	I_{inH}	5				290	–	–	µAdc	5	–	–	–	8	16
		6	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	290	–	–		7	–	–	–		
		9	–	–	–	220	–	–		9	–	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	µAdc		4	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	−0.810	−0.880	−0.700	Vdc	4	7,9	–	–	8	16
		2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	3,9	7	–	–	8	16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	–	4,7,9	–	–	8	16
		2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	9	3,7	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	−0.910	–	Vdc	–	7,9	4	–	8	16
		2	−1.080	–	−0.980	–	−0.910	–	Vdc	9	7	3	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	−1.630	–	−1.595	Vdc	–	7,9	–	4	8	16
		2	–	−1.655	–	−1.630	–	−1.595	Vdc	9	7	–	3	8	16
Switching Times (50-ohm load) (See Figure 1)					Typ	Max				+1.11 V	+0.31 V	Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay Data		t_{d+2+}	2	–	–	2.6	–	–	–	ns	9	7	4	2	8	16
Clock		t_{2-2+}	↓	–	–	4.3	–	–	–	↓	4,9	–	7	↓	↓	↓
Select		t_{g+2+}	2	–	–	3.7	–	–	–	ns	4	7	9	2	8	16
Setup Time Data		t_{setup}	2	–	–	1.6	–	–	–	ns	–	7,9	4	2	8	16
Select		t_{setup}	2			2.5				ns	3	7	9	2	8	16
Hold Time Data		t_{hold}	2	–	–	0.0	–	–	–	ns	–	7,9	4	2	8	16
Select		t_{hold}	2	–	–	−0.5	–	–	–	ns	3	7	9	2	8	16
Rise Time (20% to 80%)		t_{2+}	2	–	–	2.0	–	–	–	ns	–	7,9	4	2	8	16
Fall Time (80% to 80%)		t_{2-}	2	–	–	2.0	–	–	–	ns	–	7,9	4	2	8	16

*All other inputs tested in the same manner

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

DUAL 4 LINE TO 1 LINE MULTIPLEXER (WITH ENABLE) 10174

10174F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

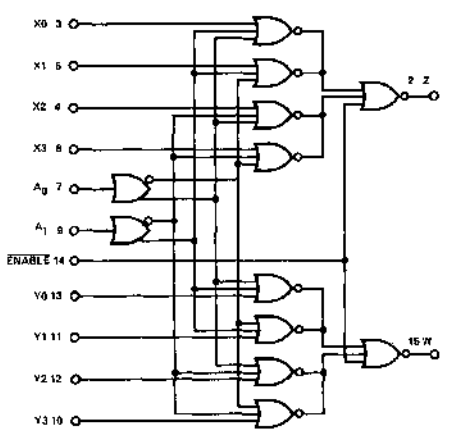
The 10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state. The enable is also useful in wire-ORing several multiplexers to achieve additional channel capability. Delay from data input to output is typically 3.5 nanoseconds.

FEATURES

- FAST PROPAGATION DELAY
  - = 3.5 ns TYP DATA TO OUTPUT
  - = 5.0 ns TYP ADDRESS TO OUTPUT
  - = 2.0 ns TYP ENABLE TO OUTPUT
- OUTPUT ENABLE TO PERMIT OUTPUT BUSSING
- LOW POWER DISSIPATION = 290 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE TWO 50 Ω LINES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

LOGIC DIAGRAM

10174



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

APPLICATIONS

- Dual 4 to 1 Multiplexer
- Dual 4 to 1 Data Selector
- Cross Bar Switch Applications

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	A1	A0	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care.

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16 Pin CERDIP

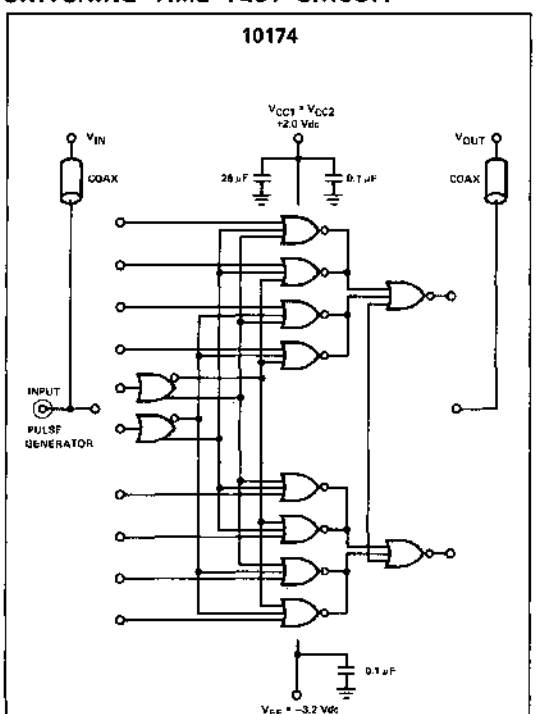
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10174 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	73	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	220	–	–	µAdc	4	–	–	–	8	1,16
		14	–	–	–	–	330	–	–		14	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	14	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	14	8	1,16
Switching Times* (50 Ω load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{13+\ 15+}$	15		–	–	3.5	–	–	–	ns	–	–	13	15	8	1,16
	$t_{13-\ 15-}$	15	–	–	–	3.5	–	–	–		–	–	13			
	$t_{7+\ 15-}$	16	–			5.0	–				11	–	7			
	$t_{7-\ 15+}$	16	–	–	–	5.0	–	–	–		11	–	7			
	$t_{14+\ 15-}$	16	–	–	–	2.0	–	–	–		–	–	14			
	$t_{14-\ 15+}$	16	–	–	–	2.0	–	–	–		–	–	14			
Rise Time (20% to 80%)	t_+	15	–	–	–	2.0	–	–	–		–	–	14			
Fall Time (80% to 80%)	t_-	15	–	–	–	2.0	–	–	–		–	–	14			

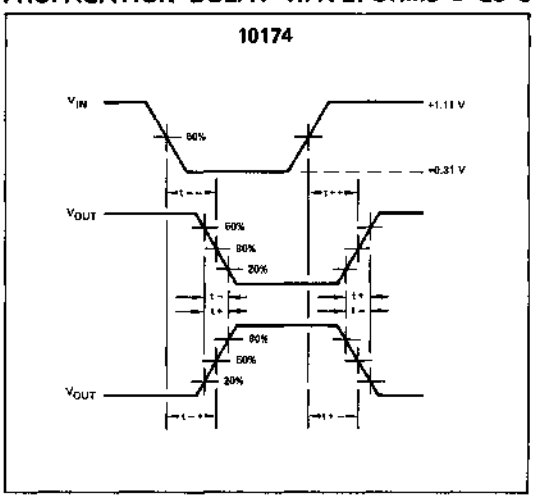
*Unused outputs connected to a 50 Ω resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope channel input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

signetics

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR | 10181

ADVANCE INFORMATION
TO BE ANNOUNCED

10181F: −30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10181 is an extremely versatile high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic functions on two four-bit words. Using advanced circuit design techniques and double layer metalization the 10181 represents the state-of-the-art in standard ECL/LSI functions. As a result, the 10181 has the same power dissipation as the comparable TTL function, while increasing the speed of operation by a factor of 4.

The $\overline{M}$ input selects the arithemetic or logic mode of operation on 2 four-bit words. The desired arithmetic or logic function is selected by applying the appropriate binary word to the select inputs ($\overline{S0}$ thru $\overline{S3}$). Full internal carry is incorporated for ripple-through operation. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast addition of very long words using a second order look-ahead in conjunction with the 10179 full look-ahead carry block. The internal carry is enabled when the mode control input (M) has a low-level voltage applied (arithmetic operation). Full addition of two 32-bit words, with carry in and carry out can be performed in 18 ns. All inputs have 50kΩ internal pulldown resistors, and outputs are all open emitters for versatility in interconnect techniques.

FEATURES

- FAST PROPAGATION DELAYS:
  - = 3.1 ns TYP ($\overline{C}_n$ TO $\overline{C}_{n+4}$)
  - = 5.0 ns TYP ($\overline{C}_n$ TO $\overline{F}_1$)
  - = 7.0 ns TYP ($\overline{A}1$, $\overline{B}1$ TO $\overline{F}1$)
  - = 5.0 ns TYP ($\overline{A}1$ TO $\overline{C}_{n+4}$)
- 16 LOGIC OPERATIONS
- 16 ARITHMETIC OPERATIONS
- POWER DISSIPATION = 600 mW/PACKAGE TYP (NO LOAD)
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

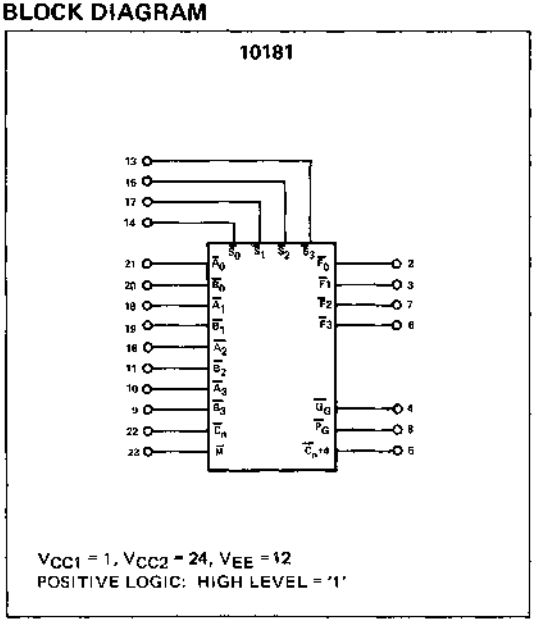
TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 24-Pin CERDIP

BLOCK DIAGRAM



V_{CC1} = 1, V_{CC2} = 24, V_{EE} = 12
POSITIVE LOGIC: HIGH LEVEL = '1'

FUNCTIONAL TRUTH TABLE

POSITIVE LOGIC

Function Select $\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Logic Functions $\overline{M}$ is High $\overline{F}$	Arithmetic Operation $\overline{M}$ is Low $\overline{C}_n$ of LSB must be High $\overline{F}$*
L	L	L	L	$\overline{F} = A$	F = A minus 1
L	L	L	H	$\overline{F} = A + B$	F = A plus (A + $\overline{B}$)
L	L	H	L	$\overline{F} = A + \overline{B}$	F = A plus (A + B)
L	L	H	H	$\overline{F}$ = Logical "1"	F = A times 2
L	H	L	L	$\overline{F} = A \cdot B$	F = (A · B) minus 1
L	H	L	H	$\overline{F} = B$	F = (A · B) plus (A + $\overline{B}$)
L	H	H	L	$\overline{F} = A \oplus B$	F = A plus B
L	H	H	H	$\overline{F} = \overline{A} + B$	F = A plus (A · B)
H	L	L	L	$\overline{F} = A \cdot \overline{B}$	F = (A · $\overline{B}$) minus 1
H	L	L	H	$\overline{F} = A \oplus B$	F = A minus B minus 1
H	L	H	L	$\overline{F} = \overline{B}$	F = (A · $\overline{B}$) plus (A + B)
H	L	H	H	$\overline{F} = \overline{A} + \overline{B}$	F = (A · $\overline{B}$) plus A
H	H	L	L	$\overline{F}$ = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$\overline{F} = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H	H	H	L	$\overline{F} = \overline{A} \cdot \overline{B}$	F = (A + B) plus 0
H	H	H	H	$\overline{F} = \overline{A}$	F = A plus 0

*$\overline{F}$ outputs of ALU are one's complement of function listed below.

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.600	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10181 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	–	–	–	145	–	–	mAdc	–	–	–	–	12	1,24
Input Current	I_{inH}	9	–	–	–	–	245	–	–	μAdc	9	–	–	–	12	1,24
		10	–	–	–	–	220	–	–		10	–	–	–		
		11	–	–	–	–	245	–	–		11	–	–	–		
		13	–	–	–	–	200	–	–		13	–	–			
		14	–	–	–	–	265	–	–		14	–	–	–		
		15	–	–			265				15	–		–		
		16	–	–	–	–	220	–	–		16	–	–	–		
		17	–	–	–	–	265	–	–		17	–	–	–		
		18	–	–	–	–	220	–	–		18	–	–			
		19	–	–	–	–	245	–	–		19	–	–	–		
		20	–	–	–		245	–	–		20	–	–	–		
		21	–	–	–	–	220	–	–		21	–	–	–		
		22	–	–	–	–	290	–	–		22	–	–	–		
		23	–	–	–	–	200	–	–		23	–	–			
Input Leakage Current	I_{inL}	9	–	–	0.5	–	–	–	–	μAdc	–	9	–	–	12	1,24
		10	–	–		–			–		–	10	–			
		11	–	–		–	–	–	–		–	11	–	–		
		13	–	–								13	–	–		
		14	–			–	–	–	–		–	14	–			
		15				–	–	–	–		–	15	–	–		
		16	–	–		–			–		–	16		–		
		17	–	–		–	–	–	–		–	17	–	–		
		18	–	–		–	–	–	–		–	18	–	–		
		19	–	–		–			–		–	19	–			
		20	–	–			–	–	–		–	20	–			
		21	–	–		–	–	–	–		–	21	–	–		
		22	–	–		–		–	–		–	22	–			
		23	–	–		–	–	–	–		–	23	–	–		
High Output Voltage	V_{OH}	*	−1.060	−0.890	−0.960		−0.810	−0.890	0.700	Vdc	*	*		–	12	1,24
Low Output Voltage	V_{OL}	*	−2.000	−1.875	−1.990	–	−1.650	−1.920	−1.815	Vdc	*	*	–		12	1,24
High Threshold Voltage	V_{OHA}	*	−1.060		0.980	–	–	−0.910	–	Vdc	–	–	**	**	12	1,24
Low Threshold Voltage	V_{OLA}	*	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	**	**	12	1,24

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time

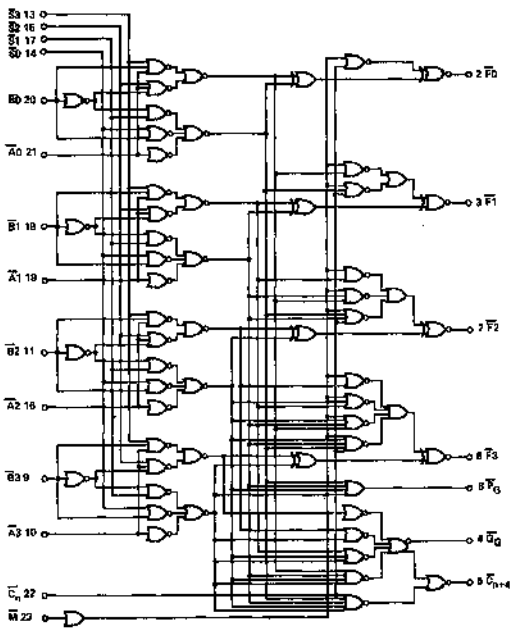
Each ECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics +25°C Min	Typ	Max	Unit
Propagation Delay	t + +	$\overline{C_n}$	$\overline{C_{n+4}}$	–	–	3.1	–	ns
	t − −				–	3.1	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{C_n}$	$\overline{F_1}$	$\overline{M}$ is Low	–	4.9	–	ns
	t + −				–	5.0	–	
	t − +				–	4.9	–	
	t − −				–	5.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{A1}$	$\overline{F_1}$	–	–	7.0	–	ns
	t + −				–	7.0	–	
	t − +				–	7.0	–	
	t − −				–	7.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{A1}$	$\overline{P_G}$	–	–	3.0	–	ns
	t − −				–	3.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{A1}$	$\overline{G_G}$	–	–	5.0	–	ns
	t − −				–	5.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{A1}$	$\overline{C_{n+4}}$		–	5.4	–	ns
	t − +				–	4.4	–	
Rise Time	t +					2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{B1}$	$\overline{F_1}$	$\overline{S1}$ and $\overline{S2}$ High, $\overline{S0}$ or $\overline{S3}$ Low	–	7.0	–	ns
	t + −				–	7.0	–	
	t − +				–	7.0	–	
	t − −				–	7.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics +25°C Min	Typ	Max	Unit
Propagation Delay	t + +	$\overline{B1}$	$\overline{P_G}$	$\overline{S0}$ Low, $\overline{S1}$ High	–	3.0	–	ns
	t − −				–	3.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{B1}$	$\overline{G_G}$	$\overline{S2}$ High, $\overline{S3}$ Low	–	4.0	–	ns
	t − −				–	5.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{B1}$	$\overline{C_{n+4}}$	$\overline{S1}$ and $\overline{S2}$ High, $\overline{S0}$ or $\overline{S3}$ Low		5.4	–	ns
	t − +				–	4.4	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{B1}$	$\overline{F_1}$	$\overline{S1}$ or $\overline{S2}$ Low	–	7.5	–	ns
	t +					8.0		
	t − +				–	7.5	–	
	t − −					8.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t +	$\overline{B1}$	$\overline{P_G}$	$\overline{S1}$ Low		4		ns
	t − +				–	4	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t − +	$\overline{B1}$	$\overline{G_G}$	$\overline{S2}$ Low	–	5.2	–	ns
	t + −					5.7		
Rise Time	t +					2.0		
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{B1}$	$\overline{C_{n+4}}$	$\overline{S0}$ or $\overline{S1}$ or $\overline{S2}$ or $\overline{S3}$ Low		6.0		ns
	t − +				–	5.6		
Rise Time	t +				–	2.0	–	
Fall Time	t −					2.0		

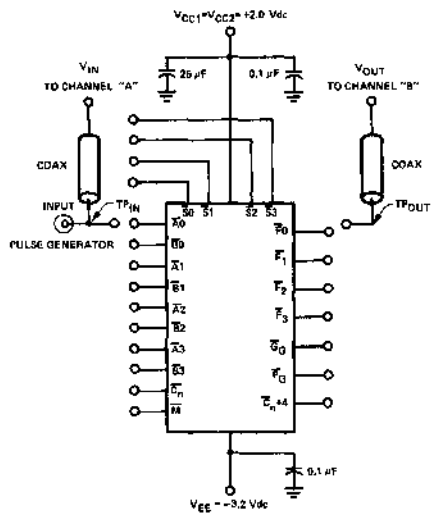
†High = −0.81 V
Low = −0.31 V
$V_{CC1} = V_{CC2} = +2.0$ Vdc = −3.2 Vdc, $V_{EE} = -3.2$ Vdc

LOGIC DIAGRAM



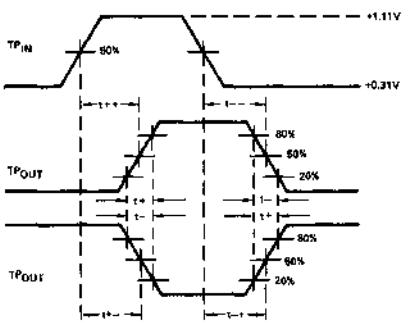
Positive logic: High Level = "1"

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORM @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

signetics

DUAL 3-INPUT 3-OUTPUT HIGH PERFORMANCE GATES

10210
10211
10212

ADVANCE INFORMATION
TO BE ANNOUNCED

10210 B, F, 10211 B, F 10212 B, F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10210/10211/10212 are designed to drive up to six transmission lines simultaneously. The multiple outputs of these devices also allow the wire-"OR"ing of several levels of gating for minimization of gate and package count.

Three logic functions are available:

10210 – Triple OR outputs
10211 – Triple NOR outputs
10212 – Two NOR/One OR Outputs

The 10210/10211/10212 are high performance versions of the 10110/10111/10112.

The ability to control three parallel lines with minimum propagation delay from a single point makes the 10210/10211/10212 particularly useful in clock distribution applications where minimum clock skew is desired. The 10212 is particularly useful as a clock amplifier on a board using clock signals with both polarities.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPES

- B: 16-Pin Silicone Dip
- F: 16-Pin CERDIP

FEATURES

- **FAST PROPAGATION DELAY = 1.7 ns TYP. (ALL OUTPUTS LOADED)**
- **POWER DISSIPATION = 150 mW/PACKAGE TYP. (NO LOAD)**
- **VERY HIGH FANOUT CAPABILITY – CAN DRIVE SIX 50 Ω LINES**
- **INTERNAL 50 kΩ PULLDOWN RESISTORS**
- **OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY**

ELECTRICAL CHARACTERISTICS

Conditions; $T_A = 25°C$, $V_{EE} = -5.2$ V ±1%

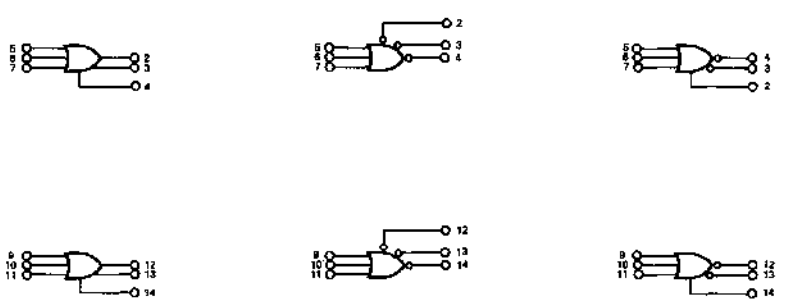
1. I_E = 38 mA dc max.
2. I_{inH} = 425 μA dc max.

Conditions: $T_A = 25°C$, $V_{CC} = +2.0$ V ±1%, $V_{EE} = -3.2$ V ±1%, 50 Ω loads

3. t_{pd} = 1.7 ns typ.
4. t_r, t_f = 1.5 ns typ. (20% to 80%)

LOGIC DIAGRAMS

10210 10211 10212



V_{CC1} = 1, 15 V_{CC2} = 16 V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

SECTIONS
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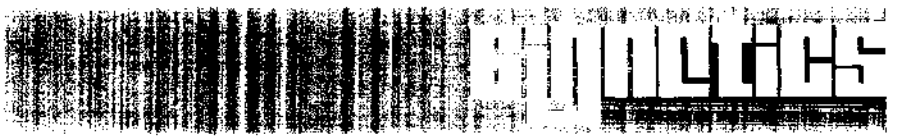


LINEAR
PRODUCT
SPECIFICATIONS

SECTIONS
SECTIONS
SECTIONS
SECTIONS
SECTIONS
SECTIONS
SECTIONS
SECTIONS
SECTIONS
SECTIONS

Comparators and Sense Amplifiers

Communications Circuits

Consumer Circuits

Operational Amplifiers

Phase Locked Loops

Voltage Regulators

EXPLANATION

The following table has been presented to assist the designer in selecting the optimum device for his application. For the majority of applications, the primary considerations are "Input Bias Current" and "Offset Voltage". For additional specifications refer to the appropriate device data page.

SELECTION GUIDE FOR GENERAL PURPOSE APPLICATIONS

INPUT CURRENT (nA)		SIGNETICS NUMBER	PACKAGE TYPE
MAXIMUM	TYPICAL		
0.030	0.005	SU536	T
0.100	0.030	NE536	T
0.200	0.100	μA740	T
2.0	0.100	μA740C	T
2.0	0.8	SE537	T
2.0	0.8	LM108	T
2.0	0.8	LM108A	T
7.0	1.5	NE537	T
7.0	1.5	LM308	T
7.0	1.5	LM308A	T
10.0	2.0	SE533	T
10.0	5.0	NE533	T, V
15.0	8.0	S5556	T
30.0	15.0	N5556	T, V
75.0	30.0	LM101A	T
75.0	30.0	LM107	T
250.0	70.0	LM301A	T, V
500.0	80.0	μA748	T
500.0	80.0	μA748C	A, T, V
500.0	120.0	LM101	T
500.0	200.0	μA709	T
500.0	200.0	μA741C	A, T, V
500.0	200.0	μA741	A, T, V
500.0	200.0	SE531	T
1500.0	250.0	LM201	A, T, V
1500.0	300.0	μA709	A, T, V
1500.0	400.0	NE531	T, V
OFFSET VOLTAGE (mV)			
0.5	0.3	LM108A	T
0.5	0.3	LM308A	T
1.0	0.5	SE533	T
2.0	0.6	SE537	T
2.0	0.7	LM101	T
2.0	0.7	LM107	T
2.0	0.7	LM108	T
2.0	1.0	NE533	T, V
5.0	1.0	LM101	T
5.0	1.0	μA709	T
5.0	1.0	μA741	T
5.0	1.0	μA748	T
5.0	2.0	NE531	T
5.0	2.0	S5556	T
6.0	1.0	μA741C	A, T, V
6.0	2.0	NE531	T, V
6.0	2.0	μA748C	A, T, V
7.5	1.6	NE537	T
7.5	1.6	LM201	A, T, V
7.5	2.0	LM301	T, V
7.5	2.0	LM308	T
7.5	2.0	μA709C	A, T, V
10.0	4.0	N5556	T, V
20.0	10.00	μA740	T
20.0	7.5	SU536	T
90.0	30.0	NE536	T
90.0	30.0	μA740C	T

COMMERCIAL TEMPERATURE RANGE
(0°C – 70°C)

PARAMETER	T_A	NE531	NE533 Note 1	NE933 Note 2	NE536	NE537	NE5558	NE5559	LM201	LM301A	LM307	LM308	µA709	µA740	µA741	µA747	µA748	UNITS
Input Offset Voltage	25°C	6	2	2	90	7.5	10		7.5	7.5	7.5	7.5	7.5		6		6	mV
(Max)	Over Temp	7.5	3	3		10	14		10	10	10	10	10		7.5		7.5	mV
Input Current	25°C	1500	10	10	0.1	7	30		1500	250	250	7	1500		500		500	nA
(Max)	Over Temp	2000	15	18		10	40		2000	300	300	10	2000		600		800	nA
Input Offset Current	25°C	200	5	5		1	10		500	50	50	1	500		200		200	nA
(Max)	Over Temp	300	10	10		1.5	14	DUAL 741	750	70	70	1.5	750		300	DUAL 741	300	nA
Large Signal Voltage Gain (Min)	25°C	20	40	12	25	25	70		20	25	25	25	15		20		50	V/mV
C.M.R.R. (Min)	25°C	70	90	84	64	80	70		85	70	70	90	85		70		70	dB
P.S.R.R. (Min)	25°C	150	50	50	300	100	200		300	300	300	100	200		150		150	µV/V
Slew Rate A = +1 (Typ)	25°C	30	0.03	0.005	6	0.2	2.5		0.5	0.5	0.5	0.2	0.5	6	0.5		0.5	V/µS
Power Dissipation (Max)	25°C	300	1.5	0.12	240	60	90		90	90	90	24	200	240	85		85	mW
Compensation		No	No	No	Yes	No	Yes	Yes	No	No	Yes	No	No	Yes	Yes	Yes	No	

Note 1: $V_{CC} = \pm 15V$

Note 2: $V_{CC} = \pm$ 3V

MILITARY TEMPERATURE RANGE
(-55°C – +125°C)

PARAMETER	T_A	SE531	SE533 Note 1	SE533 Note 2	SU536 Note 3	SE537	SE5558	SE5559	LM101	LM101A	LM107	LM108	µA709	µA741	µA747	µA748	UNITS
Input Offset Voltage	25°C	5	1	1	20	2	4		5	2	2	2	5	5		5	mV
(Max)	Over Temp	6	2	2	30	3	6		6	3	3	3	6	6		6	mV
Input Current	25°C	500	10	10	0.03	2	15		500	75	75	2	500	500		500	nA
(Max)	Over Temp	1500	15	15	3	3	30		1500	100	100	3	1500	1500		1500	nA
Input Offset Current	25°C	200	5	5		0.2	2		200	10	10	0.2	200	200		200	nA
(Max)	Over Temp	500	10	10		0.3	5	DUAL 741	500	20	20	0.4	500	500	DUAL 741	500	nA
Large Signal Voltage Gain (Min)	25°C	50	50	16	50	50	100		50	50	50	50	25	50		50	V/mV
C.M.R.R. (Min)	25°C	70	100	90	70	80	80		70	80	80	80	70	70		70	dB
P.S.R.R. (Min)	25°C	150	25	25	150	100	100		300	100	100	100	150	150		150	µV/V
Slew Rate A = +1 (Typ)	25°C	30	0.03	0.005	6	0.2	2.5		0.5	0.5	0.5	0.2	0.5	0.5		0.5	V/µS
Power Dissipation (Max)	25°C	210	0.9	0.096	165	45	45		90	80	90	18	165	85		85	mW
Compensation		No	No	No	Yes	No	Yes	Yes	No	No	Yes	No	No	Yes	Yes	No	

Note 1: $V_{CC} = \pm 15V$

Note 2: $V_{CC} = \pm$ 3V

Note 3: -55°C – +85°C

DESCRIPTION

The Signetics NE501 is a direct-coupled broad-band amplifier fabricated within a monolithic silicon substrate by planar and epitaxial techniques. Typical applications include video amplifiers.

Application flexibility is provided by several external pin connections which adjust the amplifier characteristics to individual needs.

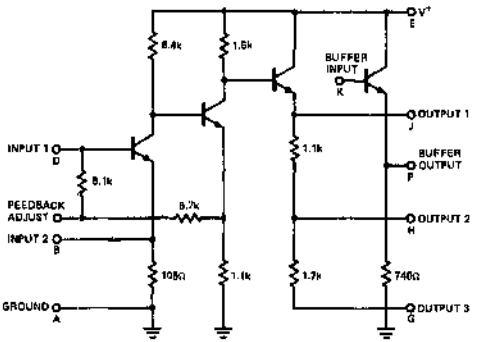
FEATURES

- **ADJUSTABLE GAIN AND IMPEDANCE CHARACTERISTICS**
- **UNITY GAIN FREQUENCY – 150 MHz**
- **NOISE FIGURE – 5.0dB**
- **POWER DISSIPATION – 20mW**

ABSOLUTE MAXIMUM RATINGS

Voltage Applied $V_{G,H,E,C}$		+8.0V
Voltage Applied V_B		±3.0V
Voltage Applied $V_{K,D}$		+4.0V
Current Rating $I_{F,J}$		±30mA
Storage Temperature		-65°C to +150°C
Operating Temperature	NE501	0°C to +70°C
	SE501	-55°C to +125°C

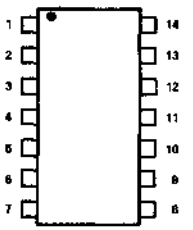
CIRCUIT SCHEMATIC



NOTE: Component values are typical.

PIN CONFIGURATIONS

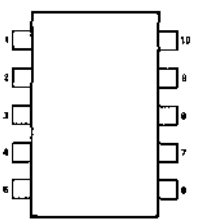
A PACKAGE
(Top View)



1. Feedback adjust
2. Input 1
3. NC
4. NC
5. Output 3
6. Input 2
7. Ground
8. Output 2
9. V^+
10. NC
11. NC
12. Buffer output
13. Buffer input
14. Output 1

ORDER PART NOS.
SE501A/NE501A

Q PACKAGE



1. Ground
2. Output 3
3. Input 2
4. Output 2
5. V^+
6. Buffer output
7. Buffer input
8. Output 1
9. Feedback adjust
10. Input 1

ORDER PART NOS.
SE501Q/NE501Q

K PACKAGE

1. Ground
2. Output 3
3. Input 2
4. Output 2
5. V^+
6. Buffer output
7. Buffer input
8. Output 1
9. Feedback adjust
10. Input 1

ORDER PART NOS.
SE501K/NE501K

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	NE501			SE501			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	f = 50 kHz; Notes 1, 2, 6	22.5	24	26.5	23	24	26	dB
Bandwidth (-3dB)	Notes 1, 2, 6	11			14			MHz
Unity Gain Frequency	A_{Vo} = 0dB; Notes 2, 6	100	150		100	150		MHz
Voltage Gain Stability	f = 50 kHz; T = 0°C; Notes 2, 6	-1.0						dB
	f = 50 kHz; T = +70°C; Notes 2, 6			+0.6				dB
	f = 50 kHz; T = -55°C; Notes 2, 6				-1.0			dB
	f = 50 kHz; T = +125°C; Notes 2, 6						+0.6	dB
Output Voltage	Notes 1, 2, 6, 9	0.71	1.0		0.71	1.0		V_{RMS}
Input Impedance	Notes 1, 6; f = 50 kHz; $V_J = V_K$	470		1200	540		1100	Ω
Output Impedance	Notes 1, 2; f = 50 kHz; V_D = AC ground		12	18		12	18	Ω
Output Impedance	Notes 1, 5; f = 50 kHz; V_D = AC ground		25	65		25	50	Ω
Power Dissipation				24			21	mW
Power Dissipation	$V_K = V_J$			60			53	mW
Pulse Response								
Delay Time	Notes 2, 6, 7			15			15	ns
Rise Time	Notes 2, 6, 7		12	20		12	16	ns
Noise Figure	f = 100 kHz; BW = 100 Hz; Z_s = 600Ω		5.0	8.0				dB
	f_c = 100 kHz, BW = 100 Hz; Z_s = 500Ω, $V_J = V_K$					5.0	7.0	dB

(Notes: 3, 4, 5, 8) Standard Conditions: V_E = +6.0V, V_A = 0V, $V_G = V_B$, T = +25°C (except as noted)

NOTES:

1. Variations in this parameter depend on optional alternate connections as indicated in accompanying curves.
2. Measured at Pin F, with Pins J and K connected.
3. Pins not specifically referenced are left electrically open. All voltages are referenced to Pin A. Letter subscripts denote pins on circuit schematic.
4. Positive current flow is defined as into the terminal referenced.
5. Measured at Pin J.
6. Load Resistance = 600Ω, capacitively coupled.
7. Delay time is defined as the time interval between the 50% points of e_D and e_F. Rise time = 20% to 80% points of e_F. Input Pulse Characteristics: Amplitude = 25mV; PW = 100ns.
8. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance test Sub-Groups. Sub-Group A-7 is used for the electrical end points for Linear Products.
9. Total harmonic distortion less than 5% at e_o = 0.71 V_{RMS}.

DESCRIPTION

The 510 is a dual high-frequency differential amplifier with associated constant current sources and biasing elements contained within a silicon monolithic epitaxial substrate. The large number of accessable internal points provide extreme flexibility of application. The 510 is intended for RF-IF amplifier service to beyond 100 MHz. Circuit layout provides for connection as either a high-gain, common-emitter, common-base, cascode amplifier or a common-collector, common-base, differential amplifier that is useful in critical limiter applications. Automatic gain control may be applied to either circuit.

The SE510Q and SE510A meet or exceed the mechanical and environmental requirements of MIL-S-19500 over the temperature range of -55°C to +125°C.

The NE510A and NE510J are intended for industrial applications over the temperature range of 0°C to +75°C.

FEATURES

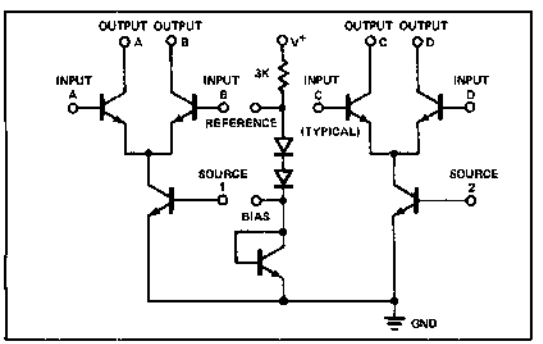
- LOW INPUT OFFSET VOLTAGE = ±2mV
- LOW INPUT OFFSET CURRENT = ±3μA
- SINGLE POWER SUPPLY
- AGC CAPABILITY
- HIGH FORWARD TRANSADMITTANCE
- LOW FEEDBACK CAPACITANCE

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V^+)	20V
Output Collector Voltage	25V
Current (Pin K)	-25mA
Current (All Other Pins)	±15mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE510J, SE510A	-55°C to +125°C
NE510A, NE510J	0°C to +75°C
Junction Temperature	150°C

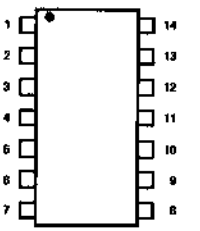
Maximum ratings are limiting values above which serviceability may be impaired.

BASIC CIRCUIT SCHEMATIC



PIN CONFIGURATIONS

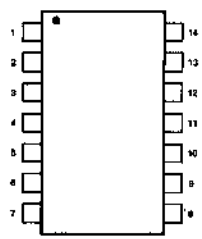
A PACKAGE
(Top View)



1. Output B
2. Output A
3. Input A
4. Input B
5. Reference
6. Source 1
7. Ground
8. Source 2
9. Bias
10. Input D
11. Input C
12. Output C
13. Output D
14. V^+

ORDER PART NOS. SE510A/NE510A

Q PACKAGE



1. Input C
2. Output C
3. Output D
4. V^+
5. Output B
6. Output A
7. Input A
8. Input B
9. Reference
10. Source 1
11. Ground
12. Source 2
13. Bias
14. Input D

ORDER PART NOS. SE510Q/NE510Q

ELECTRICAL CHARACTERISTICS

PARAMETERS	TEMPERATURE	TEST CONDITIONS	LIMITS						UNITS
			NE510			SE510			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	+25°C			0.5	3		0.5	2	mV
	0°C to +70°C			1.0	4				
	-55°C to +125°C						1.5	3.5	
Input Offset Current	+25°C			2.0	6		2.0	3.5	μA
	0°C to +70°C			2.5	9				
	-55°C to +125°C						2.5	7.5	
Input Bias Current	+25°C			8.0	25		8.0	20	μA
	0°C to +70°C			10.0	40				
	-55°C to +125°C						16.0	40	
Differential Collector Current per Differential Pair	+25°C	V_{in} = 0		45	75		45	62.5	μA
	0°C to +70°C			50	100				
	-55°C to +125°C						50	100	
Differential Current in the Current Sources	+25°C			30	75		30	62.5	μA
	0°C to +70°C			35	100				
	-55°C to +125°C						35	100	
Total Current	+25°C			11.0	15.0		11.0	15.0	mA
Common Mode Rejection Ratio	+25°C		60	80		60	80		dB

ELECTRICAL CHARACTERISTICS (V^+ = +12V, T = 25°C applicable from DC to 10 MHz, unless otherwise noted)

PARAMETER	EMITTER COUPLED CONFIGURATION	CASCODE CONFIGURATION V_{AGC} = 0V	UNITS
Input Conductance [$R_e(Y_{11})$]	0.7	3.0	mmho
Output Conductance [$R_e(Y_{22})$]	0.01	0.01	mmho
Input Capacitance	4.5	10	pF
Output Capacitance	2.5	2.5	pF
Reverse Transfer Capacitance	0.05	0.05	pF
Forward Transconductance	25	90	mmho

DESCRIPTION

The 511 is a monolithic dual high frequency differential amplifier with associated constant current source transistors and biasing diode. It is useful from DC to 100 MHz. The circuit arrangement provides for connection as two completely independent emitter coupled (differential) or cascode amplifiers. The bias diode allows stabilization of the current source currents over a large temperature range.

FEATURES

- LOW INPUT OFFSET VOLTAGE = ±2mV
- LOW INPUT OFFSET CURRENT = ±3μA
- AGC CAPABILITY
- HIGH FORWARD TRANSADMITTANCE
- LOW FEEDBACK CAPACITANCE
- SINGLE POWER SUPPLY

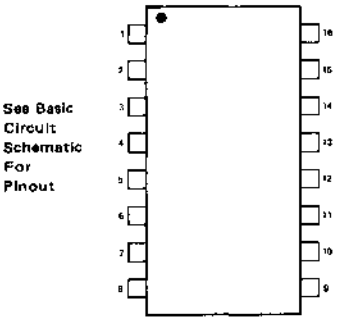
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+)	20V
Output Collector Voltage	25V
Current (All Pins)	±15mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE511Q, SE511B	-55°C to +125°C
NE511B, NE511Q	0°C to +75°C
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

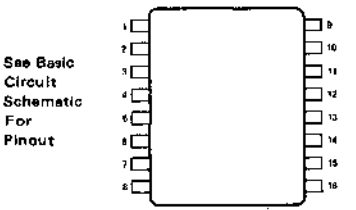
PIN CONFIGURATIONS

B PACKAGE
(Top View)



ORDER PART NOS. SE511B/NE511B

Q PACKAGE

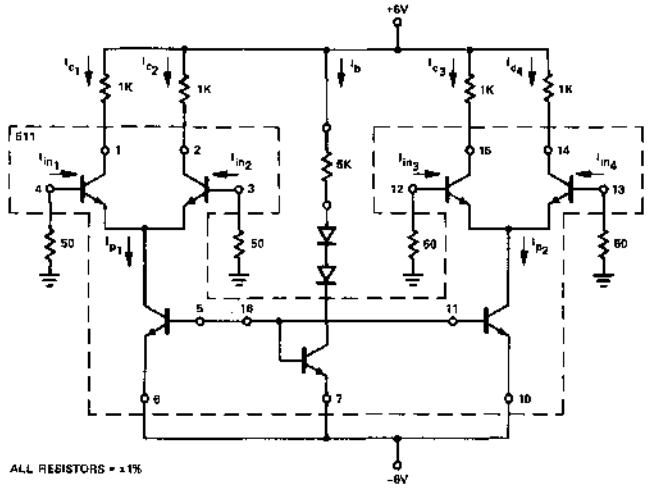


ORDER PART NOS. SE511Q/NE511Q

ELECTRICAL CHARACTERISTICS (Standard Test Circuit)

ACCEPTANCE TEST SUBGROUP	PARAMETERS	SYMBOL	LIMITS MIN SE511	LIMITS MIN NE511	LIMITS TYP SE511	LIMITS TYP NE511	LIMITS MAX SE511	LIMITS MAX NE511	UNITS	TEMPERATURE	TEST CONDITIONS
A-3	Input Offset Voltage	ΔV_{in}			0.5	0.5	2	3	mV	+25°C	
A-4		ΔV_{in}				1.0		4.0		0°C to +75°C	
A-5		ΔV_{in}			1.5		3.5			-55°C to +125°C	
A-3	Input Offset Current	ΔI_{in}			2.0	2.0	3.5	6	μA	+25°C	
A-4		ΔI_{in}				2.5		9		0°C to +75°C	
A-5		ΔI_{in}			2.5		7.5			-55°C to +125°C	
A-3	Input Bias Current	I_{in}			8.0	8.0	20	25	μA	+25°C	
A-4		I_{in}				10.0		40		0°C to +75°C	
A-5		I_{in}			16.0		40			-55°C to +125°C	
A-3	Differential Collector Current	ΔI_c			45	45	62.5	75	μA	+25°C	V_{in} = 0;
A-4	per differential pair	ΔI_c				60		100		0°C to +75°C	I_p = 2mA
A-5		ΔI_c			50		100			-55°C to +125°C	
A-3	Differential Current in the	ΔI_p			30	30	62.5	75	μA	+25°C	
A-4	Current Sources	ΔI_p				35		100		0°C to +75°C	
A-5		ΔI_p			35		100			-55°C to +125°C	
A-2	Total Current	I_{cc}			11.0	11.0	15.0	15.0	mA	+25°C	
A-3	Common Mode Rejection Ratio	CMRR	60	60	80	80			dB	+25°C	
A-3	Output Conductance	G_{22}			0.01	0.01			mmho	+25°C	
C-2	Output Capacitance	C_{ob}			2.5	2.5			pF	+25°C	
C-2	Input Capacitance	C_{ib}			10	10			pF	+25°C	

STANDARD TEST CIRCUIT



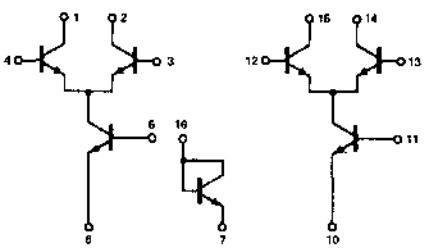
$\Delta I_{ib} = I_{in_1} - I_{in_2}$ or $I_{in_3} - I_{in_4}$

$\Delta I_c = I_{c_1} - I_{c_2}$ or $I_{c_3} - I_{c_4}$

$\Delta I_p = I_{p_1} - I_{p_2}$

$I_{cc} = I_{c_1} + I_{c_2} + I_{c_3} + I_{c_4} + I_b$

BASIC CIRCUIT SCHEMATIC



DESCRIPTION

The 515 is a general purpose high-gain amplifier with differential input and output. It is fabricated within a monolithic silicon substrate by planar and epitaxial techniques. A pair of compensation points is provided to allow frequency compensation for stable closed loop operation.

This device is not internally referenced to ground and with proper input bias may be operated from a single power supply.

FEATURES

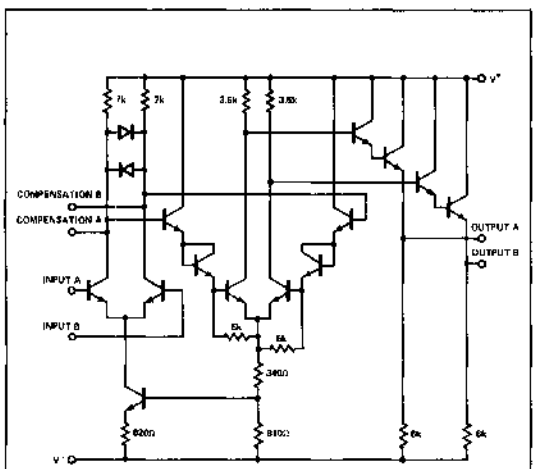
- **DIFFERENTIAL VOLTAGE GAIN (Open Loop) = 4,500**
- **INPUT OFFSET VOLTAGE = 0.5mV**
- **INPUT OFFSET VOLTAGE STABILITY = 5.0μV/°C**
- **INPUT COMMON MODE RANGE = +1.5V, -1.0V**
- **COMMON MODE REJECTION RATIO = 100dB**
- **BANDWIDTH (Open Loop) = 1.0 MHz**

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+ to V-)	12V
Differential Input Voltage (V_5 to V_7)	±5.0V
Input Current (I_5, I_7)	±2.0mA
Output Current (I_2, I_{10})	±30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +75°C
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

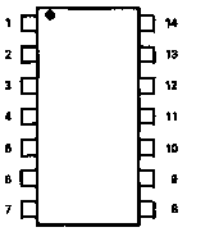
EQUIVALENT CIRCUIT



NOTE: Component values are typical.

PIN CONFIGURATIONS

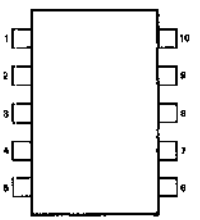
A PACKAGE
(Top View)



1. Input B
2. NC
3. NC
4. Compensation
5. NC
6. Output B
7. V^-
8. Output A
9. NC
10. NC
11. Compensation
12. NC
13. Input A
14. V^+

ORDER PART NO. NE515A

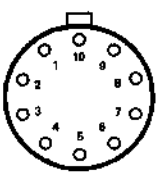
Q PACKAGE



1. V^-
2. Output A
3. NC
4. Compensation
5. Input A
6. V^+
7. Input B
8. Compensation
9. NC
10. Output B

ORDER PART NOS. SE515Q/NE515Q

K PACKAGE



1. V^-
2. Output A
3. NC
4. Compensation
5. Input A
6. V^+
7. Input B
8. Compensation
9. NC
10. Output B

ORDER PART NOS. SE515K/NE515K

NE515 ELECTRICAL CHARACTERISTICS (Standard Conditions: V_7 = 0V, V_1 = -3.0V; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTIC	V_6 = +4.0V	V_6 = +6.0V			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	2,500	3,500	4,500		V/V	+25°C	Note 2
	1,800		3,000		V/V	+125°C	
Open Loop Voltage Gain (ac)	2,000	2,500	3,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	3.0	mV	-55°C	Note 1
	0.5		0.5	2.0	mV	+25°C	
	0.5		0.5	3.0	mV	+125°C	
Input Bias Current	18		25	40	μA	-55°C	Note 1
	12		16	24	μA		
Differential Input Resistance	2.0	1.0	1.5		kΩ	-55°C	Note 10
	4.0	2.0	3.2		kΩ	+25°C	
Input Common Mode Range	±1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2		V	-55°C	Note 1
	+0.3		+1.6	+1.8	V	+25°C	
	+0.6		+1.9		V	+125°C	
Output Voltage Swing	4.7	5.7	6.3		V	-55°C	Note 3
	4.7	5.7	6.3		V	+25°C	
	4.7	5.7	6.3		V	+125°C	
High Output Level	+2.3	+4.0	+4.3		V	-55°C	V_5 = 10mV
	+2.6	+4.3	+4.6		V	+25°C	
	+3.0	+4.7	+5.0		V	+125°C	
Low Output Level	-2.4	-1.7	-2.0		V	-55°C	V_5 = 10mV
	-2.1	-1.4	-1.7		V	+25°C	
	-1.7	-1.0	-1.3		V	+125°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB		
Power Supply Current				7.0	mA		Note 1
	3.5		5.5	7.0	mA		
				7.0	mA		

NOTES:

1. Adjust V_5 to obtain $V_2 = V_{10}$.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers.
5. All measurements are referenced to power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins 5 and 7.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The SE515K has Pins 1, 3 and 9 connected to the case. The SE515Q has Pins 3 and 9 open.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.

NE515 ELECTRICAL CHARACTERISTICS (Standard Conditions: V_B = 0V, V_A = 3.0V; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTIC	V_F = +4.0V	V_F = +6.0V			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	1,800	2,500	3,200		V/V	+25°C	Note 2
	1,350		2,200		V/V	+75°C	
Open Loop Voltage Gain (ac)	1,500	1,700	2,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	4.0	mV	0°C	Note 1
	0.5		0.5	3.0	mV	+25°C	
	0.5		0.5	4.0	mV	+75°C	
Input Bias Current	18		25	40	μA	0°C	Note 1
	15		20	31	μA	+25°C	
Differential Input Resistance	3.2	1.4	2.3		kΩ	0°C	Note 10
	3.5	1.7	2.6		kΩ	+25°C	
Input Common Mode Range	±1.0		+1.5		V	+25°C	
			−1.0				
Balanced Output dc Level	−0.1		+1.2		V	0°C	Note 1
	+0.3		+1.6	+1.8	V	+25°C	
	+0.6		+1.9		V	+75°C	
Output Voltage Swing	4.5	5.3	6.1		V	0°C	Note 3
	4.5	5.3	6.1		V	+25°C	
	4.5	5.3	6.1		V	+75°C	
High Output Level	+2.3	+3.9	+4.3		V	0°C	V_C = 10mV
	+2.5	+4.1	+4.5		V	+25°C	
	+2.8	+4.3	+4.8		V	+75°C	
Low Output Level	−2.2	−1.4	−1.8		V	0°C	V_C = 10mV
	−2.0	−1.2	−1.6		V	+25°C	
	−1.7	−1.0	−1.3		V	+75°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB	+25°C	
Power Supply Current				7.0	mA	0°C	Note 1
	3.5		5.5	7.0	mA	+25°C	
				7.0	mA	+75°C	

Letter subscripts refer to pins on circuit schematic.

NOTES:

1. Adjust V_C to obtain $V_G = V_H$.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers.
5. All measurements are referenced by power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins B and C.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The NE515K has Pins 1, 3 and 9 connected to the case. The NE515G has Pins 3 and 9 open.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.

DESCRIPTION

The 516 is a high gain operational amplifier with differential input and output. Features include large gain-bandwidth product, stable open-loop operation, high output voltage swing under load, high input resistance, wide common mode voltage range and high common mode rejection.

FEATURES

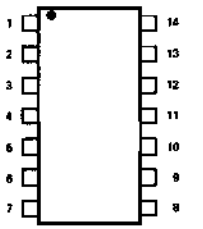
- **OPEN LOOP VOLTAGE GAIN =** NE516 15,000 / SE516 18,000
- **OPEN LOOP GAIN STABILITY =** ±20%
- **OUTPUT VOLTAGE SWING =** NE516 +10 Volts / SE516 +11 Volts
- **DIFFERENTIAL INPUT RESISTANCE =** NE516 100KΩ / SE516 400KΩ
- **INPUT COMMON MODE VOLTAGE RANGE = 23 Volts**
- **COMMON MODE REJECTION RATIO =** 100 db
- **INPUT OFFSET CURRENT =** NE516 100nA / SE516 300nA
- **OPEN LOOP BANDWIDTH =** 300 kHz

ABSOLUTE MAXIMUM RATINGS

Voltage Applied (Between Pins 1 and 6)	
NE516	34V
SE516	36V
Voltage Applied (Differential)	10V
Current Rating (Pins 1, 2, 6 and 10)	25mA
Current Rating (Other Pins)	10mA
Output Short Circuit Duration (25°C)	10sec
Storage Temperature	-65°C to +150°C
Operating Temperature	
NE516	0°C to +75°C
SE516	-55°C to +125°C
Junction Temperature	
NE516	150°C
SE516	175°C

PIN CONFIGURATION

A PACKAGE
(Top View)



1. Input B
2. Com. 1A
3. NC
4. Com. 2B
5. NC
6. Output B
7. V^-
8. Output A
9. NC
10. Com 2A
11. Com. 1B
12. NC
13. Input A
14. V^+

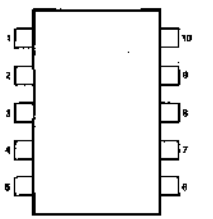
ORDER PART NOS.
SE516A/NE516A

K PACKAGE

1. V^-
2. Output A
3. Com. 2A
4. Com. 1B
5. Input A
6. V^+
7. Input B
8. Com. 1A
9. Com. 2B
10. Output B

ORDER PART NOS.
SE516K/NE516K

Q PACKAGE

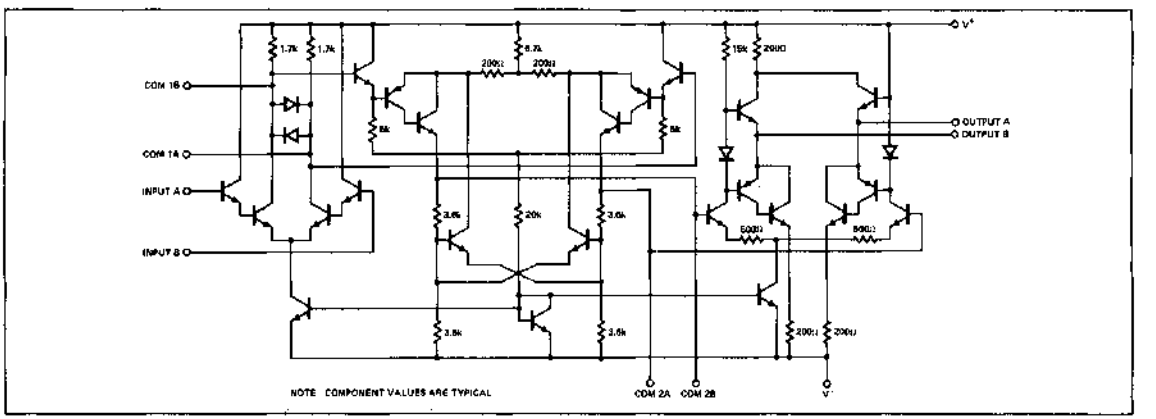


1. V^-
2. Output A
3. Com. 2A
4. Com. 1B
5. Input A
6. V^+
7. Input B
8. Com. 1A
9. Com. 2B
10. Output B

ORDER PART NOS.
SE516Q/NE516Q

Maximum ratings are limiting values above which serviceability may be impaired.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 8) (Standard Conditions: V_E = +15V, V_K = -15V, V_A = 0V)

PARAMETERS	TEST CONDITIONS	NE516				SE516				UNITS
		MIN	TYP	MAX	TEMP.	MIN	TYP	MAX	TEMP.	
Open Loop Voltage Gain (DC)	$R_L \geq 2k\Omega$,		16,000		0°C		22,000		-55°C	V/V
	Notes 5, 7	10,000	15,000		+25°C	13,000	18,000		+25°C	V/V
		8,000	13,000		+75°C	10,000	15,000		+125°C	V/V
Open Loop Voltage Gain (AC)	$R_L \geq 2k\Omega$, f = 250 kHz, Note 7	8,000	12,000		+25°C	10,000	15,000		+25°C	V/V
Input Offset Voltage	Note 6		5.0	15	0°C		3.0	10	-55°C	mV
			5.0	15	+25°C		3.0	10	+25°C	mV
			5.0	15	+75°C		3.0	10	+125°C	mV
Input Bias Current	Note 6		1.5	4.5	0°C		0.6	2.0	-55°C	µA
			1.0	3.0	+25°C		0.3	1.0	+25°C	µA
			0.6		+75°C		0.15		+125°C	µA
Input Offset Current	Note 6						0.06		-55°C	µA
			0.1	0.6	+25°C		0.03	0.2	+25°C	µA
							0.02		+125°C	µA
Differential Input Resistance	Notes 4, 6					40	150		-55°C	kΩ
		40	100		+25°C	100	400		+25°C	kΩ
							1,000		+125°C	kΩ
Input Common Mode Range		+8.0	+10		+25°C	+8.0	+10		+25°C	V
		-12	-13			-12	-13			
Power Supply Sensitivity			50		+25°C	50			+25°C	µV/V
(Referred to Input)			50		+25°C	50			+25°C	µV/V
Balanced Output dc Level	$R_L \geq 2k\Omega$, Note 6					-2.0	+0.5	+2.5	-55°C	V
		-2.5	0	+2.5	+25°C	-1.5	0	+1.5	+25°C	V
						-2.5	-0.5	+2.0	+125°C	V
Output Voltage Swing	$R_L \geq 2k\Omega$	±8.0	±10		0°C	±10	±11		-55°C	V
		±8.0	±10		+25°C	±10	±11		+25°C	V
		±8.0	±10		+75°C	±10	±11		+125°C	V
Output Resistance	Note 6		500		+25°C		500		+25°C	Ω
Common Mode Rejection Ratio			100		+25°C		100		+25°C	dB
Power Supply Current	Note 6		5.0		0°C		5.0		-55°C	mA
			5.0	6.0	+25°C		5.0	6.0	+25°C	mA
			5.0	6.0	+75°C		5.0	6.0	+125°C	mA

Letter subscripts refer to pins on circuit schematic.

NOTES:

1. Voltage and current subscripts refer to pin numbers.
2. All measurements are referenced to an external ground. Positive current flow is defined as into the terminal indicated.
3. All specifications herein apply for interchange of voltages and currents at Pins 6 and 7.
4. Differential Input Resistance is a value computed from input bias current limits.
5. Output voltage swing = 5V peak to peak.
6. Adjust V_B to obtain V_2 = V10.
7. Differential input, single ended output.

DESCRIPTION

The 526 is a high speed analog comparator intended for use in systems where low propagation delay and fast recovery from common mode or differential input overdrive is required. The device is specifically designed to provide a wide input common mode range while operating from power supplies commonly found in digital logic systems.

The 526 consists of a medium gain, high frequency differential amplifier and a high speed TTL gate fabricated within a single substrate by planar and epitaxial techniques. The output gate of the 526 has voltage and current capabilities compatible with DCL, DTL and TTL. The 526 output gate has a full fan-out of 10 to standard TTL loads.

The amplifier and gate may be used independently or cascaded for applications as a voltage comparator, digital line receiver or sense amplifier. The second gate input is used to provide strobe capability when operating the amplifier and gate in cascade.

FEATURES

- **PROPAGATION DELAY** — **30ns**
- **INPUT COMMON MODE RANGE** — **+4.5V, −3.5V**
- **DIFFERENTIAL OVERDRIVE RECOVERY** — **20ns**
- **OUTPUT COMPATIBLE WITH STANDARD LOGIC FORMS**
- **OPERATES FROM STANDARD ±5V SUPPLIES**

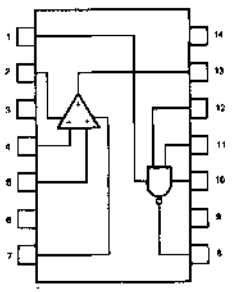
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+7.0V
Gate Input Voltage		+6.0V
Differential Input Voltage		+5.0V
Common Mode Input Voltage		+5.0V
Gate Output Current		+100 mA
Storage Temperature		-65°C to +150°C
Operating Temperature	SE526	-55°C to +125°C
	NE526	0°C to +75°C

Absolute Maximum Ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION

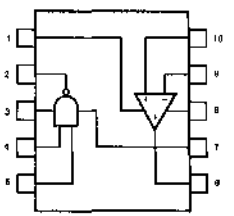
A PACKAGE



ORDER PART NOS.
SE526A/NE526A

1. V_2^+
2. V_1^+
3. NC
4. V_{IN}
5. V_{IN}
6. NC
7. V^-
8. V_O
9. NC
10. Ground
11. V_{IN}
12. V_{IN}
13. e_o
14. NC

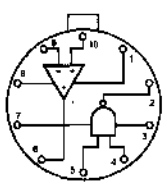
Q PACKAGE



ORDER PART NOS.
SE526Q/NE526Q

1. V_1^-
2. V_O
3. Ground
4. V_{IN}
5. V_{IN}
6. e_{o+}
7. V_2^+
8. V_1^+
9. e_{in}
10. e_{in}

K PACKAGE



ORDER PART NOS.
SE526K/NE526K

1. V_1^-
2. V_O
3. Ground
4. V_{IN}
5. V_{IN}
6. e_{o+}
7. V_2^+
8. V_1^+
9. e_{in}
10. e_{in}

ELECTRICAL CHARACTERISTICS (Standard Conditions: $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$; Notes 1,2,3,4,13,14)

CHARACTERISTIC	SYMBOL	LIMITS				TEMPERATURE		NOTES
		MIN.	TYP.	MAX.	UNIT	SE526	NE526	
Input Offset Voltage	V_{io}		2.0	5.0	mV	−55°C	0°C	5
	V_{io}		2.0	5.0	mV	+25°C	+25°C	5
	V_{io}		2.0	5.0	mV	+125°C	+75°C	5
Input Bias Current	I_{in}		30.0	35.0	µA	−55°C	0°C	6
	I_{in}		25.0	35.0	µA	+25°C	+25°C	6
	I_{in}		22.0	35.0	µA	+125°C	+75°C	6
Input Offset Current	I_{io}		0.6	5.0	µA	−55°C	0°C	
	I_{io}		0.5	5.0	µA	+25°C	+25°C	
	I_{io}		0.4	5.0	µA	+125°C	+75°C	
Input Common Mode Range	V_{cm}	+4.2	+4.7		V	−55°C	0°C	
	V_{cm}	+4.2	+4.5		V	+25°C	+25°C	
	V_{cm}	+4.2	+4.4		V	+125°C	+75°C	
	V_{cm}	−3.2	−3.5		V	−55°C	0°C	
	V_{cm}	−3.2	−3.5		V	+25°C	+25°C	
	V_{cm}	−3.2	−3.5		V	+125°C	+75°C	
Amplifier Output Voltage	V_{ohi}	3.5			V	−55°C	0°C	
	V_{ohi}	3.5			V	+25°C	+25°C	
	V_{ohi}	3.5			V	+125°C	+75°C	
	V_{olo}			0.6	V	−55°C	0°C	
	V_{olo}			0.5	V	+25°C	+25°C	
	V_{olo}			0.4	V	+125°C	+75°C	
Amplifier Power Consumption	P_d		90	120	mW	−55°C	0°C	
	P_d		100	120	mW	+25°C	+25°C	
	P_d		110	120	mW	+125°C	+75°C	
Gate Output Voltage	$V1_o$	2.8	3.5		V	−55°C	0°C	7, 8
	$V1_o$	2.8	3.2		V	+25°C	+25°C	7, 8
	$V1_o$	2.8	3.0		V	+125°C	+75°C	7, 8
	$V0_o$		0.3	0.4	V	−55°C	0°C	7, 8
	$V0_o$		0.2	0.4	V	+25°C	+25°C	7, 8
	$V0_o$		0.3	0.4	V	+125°C	+75°C	7, 8
Gate Output Sink Current	$t0_o$	16.0			mA	+25°C	+25°C	8
Gate Output Source Current	$I1_o$	1.0			mA	+25°C	+25°C	7
Gate Input Threshold Voltage	$V1_i$	2.0			V	−55°C	0°C	9
	$V1_i$	2.0			V	+25°C	+25°C	9
	$V1_i$	2.0			V	+125°C	+75°C	9
	$V0_i$			1.0	V	−55°C	0°C	10
	$V0_i$			0.9	V	+25°C	+25°C	10
	$V0_i$			0.8	V	+125°C	+75°C	10
Gate Input Current (Input "0")	$I0_i$	−0.1	−1.2	−1.6	mA	−55°C	0°C	
	$I0_i$	−0.1	−1.4	−1.6	mA	+25°C	+25°C	
	$I0_i$	−0.1	−1.2	−1.6	mA	+125°C	+75°C	
(Input "1")	$I1_i$		5	25	µA	−55°C	0°C	
	$I1_i$		10	25	µA	+25°C	+25°C	
	$I1_i$		15	25	µA	+125°C	+75°C	
Gate Current Consumption (Output "1")	I_{CC}^1			2.00	mA	−55°C	0°C	
	I_{CC}^1			2.00	mA	+25°C	+25°C	
	I_{CC}^1			2.00	mA	+125°C	+75°C	
(Output "0")	I_{CC}^0			5.00	mA	−55°C	0°C	
	I_{CC}^0			5.00	mA	+25°C	+25°C	
	I_{CC}^0			5.00	mA	+125°C	+75°C	
Gate Input Latch Voltage Rating	BV_i			6.0	V	+25°C	+25°C	
Gate Output Short Circuit Current	I_{so}	−10.0		−70.0	mA	+25°C	+25°C	
Switching Times								
Gate Turn-On Delay	T_{on}		15	17	ns	+25°C	+25°C	11
Gate Turn-Off Delay	T_{off}		15	17	ns	+25°C	+25°C	11
Propagation Delay	T_{pd}^0		30	42	ns	+25°C	+25°C	11
Propagation Delay	T_{pd}^1		40	48	ns	+25°C	+25°C	11
Differential Overload Recovery	t_{dm}		30	40	ns	+25°C	+25°C	11, 12

Recommended Operating Supply Voltages ($V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

NOTES:
1. All measurements are referenced to the ground terminal.
2. Positive current is defined as into the pin referenced.
3. Pins not specifically referenced are left electrically open.
4. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
5. Input Offset Voltage is tested at guaranteed Input Common Mode Range voltage limits and includes the worst-case variations of voltage gain and input impedance. These are the maximum values required to drive the output down to "0" or up to "1".
6. Input Bias Current is defined as the maximum current required to bias either input.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_2^+.
9. These limits are guaranteed by Gate Output Voltage ($V0_o$) test.
10. These limits are guaranteed by Gate Output Voltage ($V1_o$) tests.
11. Load capacitance includes test fixture and probe capacitance.
12. Differential Input Voltage = 500mV for this test.
13. Acceptance Test Subgroup A-7 provides end point parameters for linear devices processed to Signetics SURE Program. See Signetics SURE Bulletin 5001.
14. Manufacturer reserves the right to make design and process changes and improvements.

DESCRIPTION

The SE/NE 527 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T^2L gates with a precision linear amplifier on a single monolithic chip.

The SE/NE 527 is similar in design to the Signetics SE/NE 529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

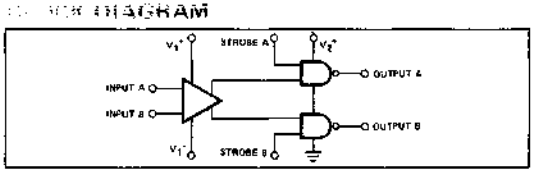
FEATURES

- **15 nsec PROPAGATION DELAY**
- **COMPLEMENTARY OUTPUT GATES**
- **TTL OR ECL COMPATIBLE OUTPUTS**
- **WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE**

APPLICATIONS

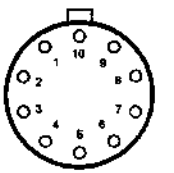
A/D CONVERSION
ECL TO TTL INTERFACE
TTL TO ECL INTERFACE
MEMORY SENSING
OPTICAL DATA COUPLING

BLOCK DIAGRAM



PIN CONFIGURATION

K PACKAGE
(Top View)



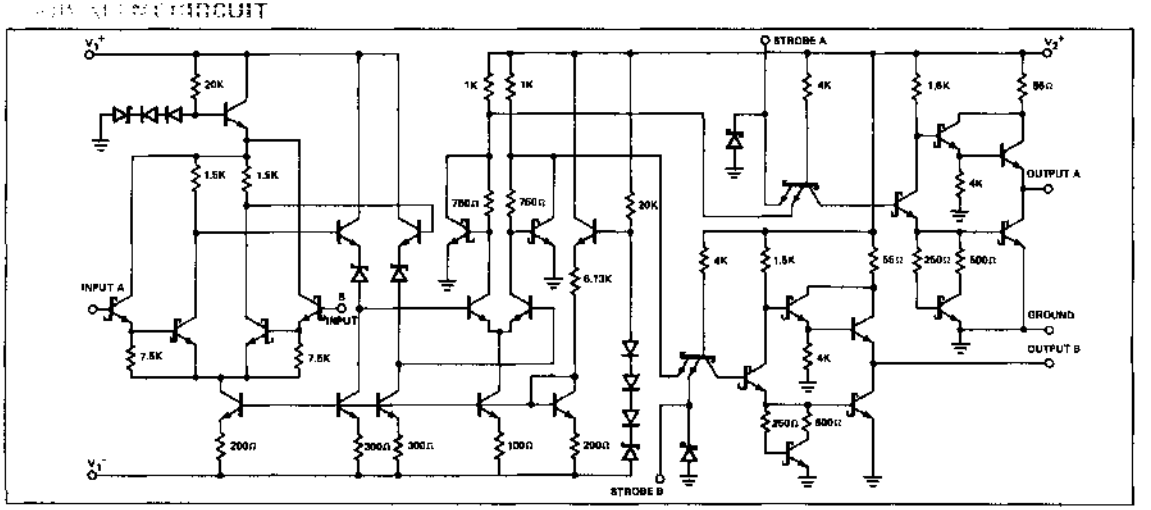
1. Input A
2. Input B
3. V_1^-
4. Strobe B
5. Output B
6. Ground
7. Output A
8. Strobe A
9. V_2^+
10. V_1^+

ORDER PART NOS. SE527K/NE527K

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_1^+)	+15 volts
Negative Supply Voltage (V_1^-)	-15 volts
Gate Supply Voltage (V_2^+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE 527	0°C to +70°C
SE 527	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 seconds)	+300°C

SCHEMATIC CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_1^+ = +10V$, $V_1^- = -10V$, $V_2^+ = +5.0V$, $V_{in} = 0V$)

PARAMET	TEST CONDITIONS	SE 527			NE 527			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage @25°C				4			6	mV
over temperature range				6			10	mV
Input Bias Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$			2			2	μA
over temperature range	$V_{in} = 0V$			4			4	μA
Input Offset Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$			0.5			0.75	μA
over temperature range	$V_{in} = 0V$			1			1	μA
Voltage Gain	$T_A = 25°C$		5			5		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		500			500		KΩ
GATE CHARACTERISTICS								
Output Voltage								
"1" State	$V_2^+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_2^+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe Inputs								
"0" Input Current	$V_2^+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" Input Current @25°C	$V_2^+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
over temperature range				200			200	μA
"0" Input Voltage	$V_2^+ = 4.75V$			0.8			0.8	V
"1" Input Voltage	$V_2^+ = 4.75V$	2.0			2.0			V
Short Circuit Output Current	$V_2^+ = 5.25V$, $V_{out} = 0V$	-40		-100	-40		-100	mA
POWER SUPPLY REQUIREMENTS								
Supply Voltage								
V_1^+		5		10	5		10	V
V_1^-		-6		-10	-6		-10	V
V_2^+		4.5	5	5.5	4.75	5	5.25	V
Supply Current	$V_1^+ = 10V$, $V_1^- = -10V$ $V_2^+ = 5.25V$							
I_1^+	$T_A = 125°C$			3.25				mA
	$T_A = 25°C$			3.75				mA
	$T_A = -55°C$			4.0				mA
	$0°C \leq T_A \leq 70°C$						5	mA
I_1^-	$T_A = 125°C$			7.0				mA
	$T_A = 25°C$			7.5				mA
	$T_A = -55°C$			8.5				mA
	$0°C \leq T_A \leq 70°C$						10	mA
I_2^+	$T_A = 125°C$			15				mA
	$T_A = 25°C$			16				mA
	$T_A = -55°C$			18				mA
	$0°C \leq T_A \leq 70°C$						20	mA
TRANSIENT RESPONSE	V_{in} = 50 mV overdrive							
Propagation Delay Time								
t_{pd} (0)	$T_A = +25°C$		14	24		14	24	ns
t_{pd} (1)	$T_A = +25°C$		16	28		16	26	ns
Delay between Output A and B	$T_A = +25°C$		2	5		2	5	ns
Strobe Delay Time								
Turn On	$T_A = +25°C$		6			6		ns
Turn Off	$T_A = +25°C$		6			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

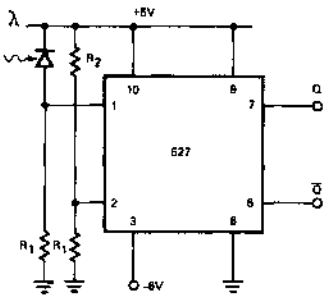
APPLICATIONS

One of the main features of the device is that supply voltages (V_1^+, V_1^-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_1^-) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_1^+ and V_1^-) up to a maximum of ±6 volts as supply voltages are increased.

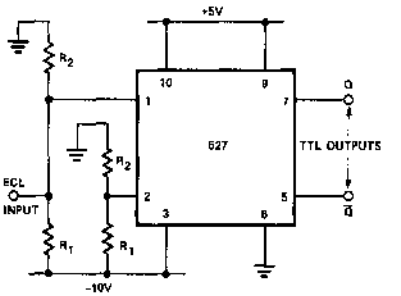
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

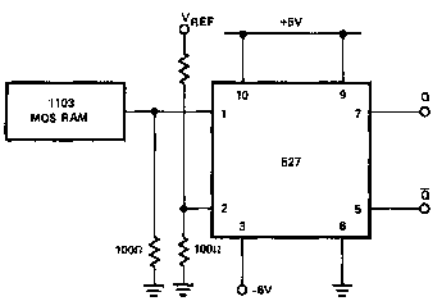
PHOTODIODE DETECTOR



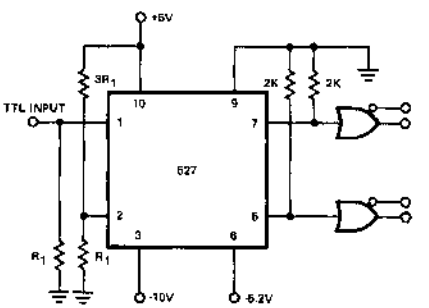
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP.

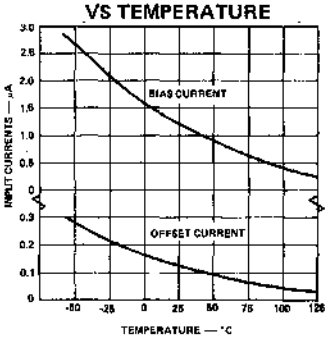


TTL TO ECL INTERFACE

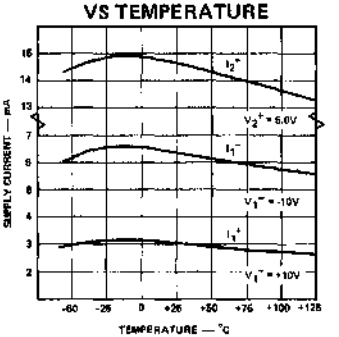


TYPICAL PERFORMANCE CURVES

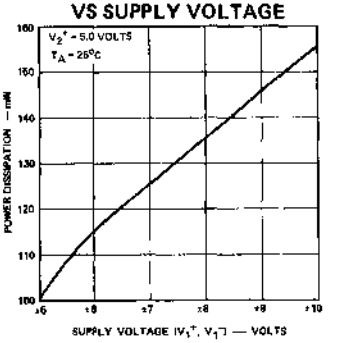
INPUT CURRENTS VS TEMPERATURE



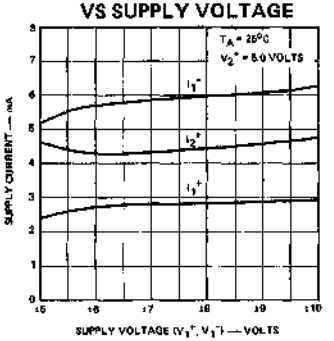
SUPPLY CURRENT VS TEMPERATURE



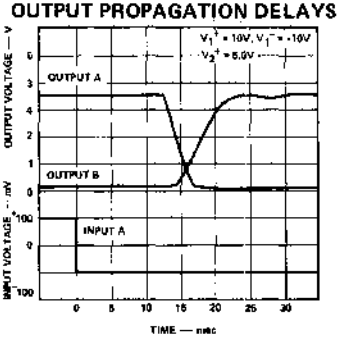
POWER DISSIPATION VS SUPPLY VOLTAGE



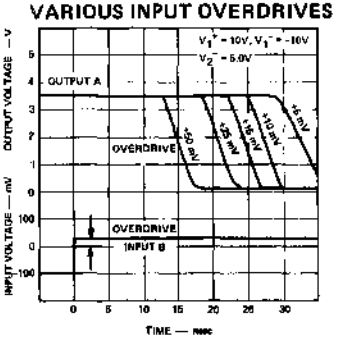
SUPPLY CURRENT VS SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

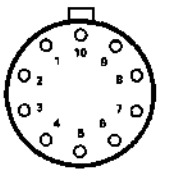


The SE/NE 529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T^2L gates with a precision linear amplifier on a single monolithic chip.

- **10 nsec PROPAGATION DELAY**
- **COMPLEMENTARY OUTPUT GATES**
- **TTL OR ECL COMPATIBLE OUTPUTS**
- **WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE**

A/D CONVERSION
ECL TO TTL INTERFACE
TTL TO ECL INTERFACE
MEMORY SENSING
OPTICAL DATA COUPLING

K PACKAGE
(Top View)

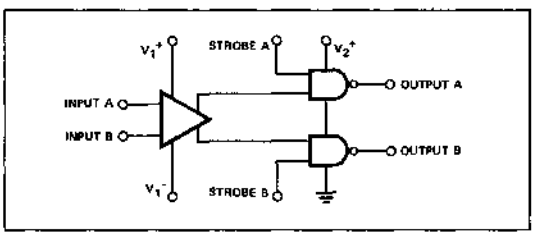


1. Input A
2. Input B
3. V_1^-
4. Strobe B
5. Output B
6. Ground
7. Output A
8. Strobe A
9. V_2^+
10. V_1^+

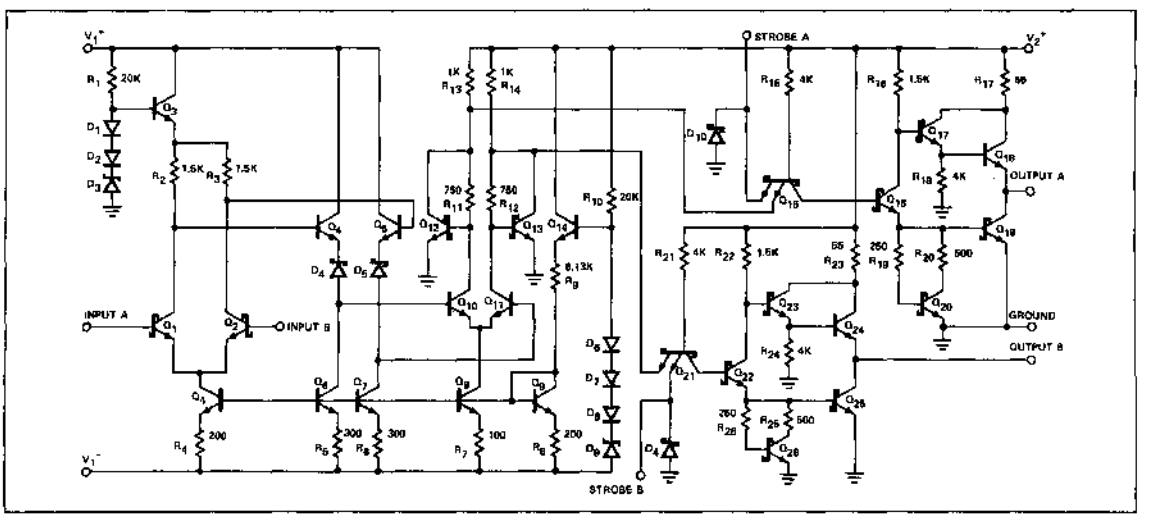
ORDER PART NOS. SE529K/NE529K

Positive Supply Voltage (V_1^+)	+15 volts
Negative Supply Voltage (V_1^-)	-15 volts
Gate Supply Voltage (V_2^+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE 529	0°C to +70°C
SE 529	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 seconds)	+300°C

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($V_1^+ = +10V$, $V_2^+ = +5.0V$, $V_1^- = -10V$, $V_{in} = 0V$)

PARAMETER	TEST CONDITIONS	SE 529			NE 529			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage @25°C				4			6	mV
over temperature range				6			10	mV
Input Bias Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$		5	12		5	20	µA
over temperature range	$V_{in} = 0V$			36			50	µA
Input Offset Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$		2	3		2	5	µA
over temperature range	$V_{in} = 0V$			9			15	µA
Voltage Gain	$T_A = 25°C$		5			5		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		10			10		KΩ
GATE CHARACTERISTICS								
Output Voltage								
"1" State @25°C	$V_2^+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State @25°C	$V_2^+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe Inputs								
"0" Input Current	$V_2^+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" Input Current @25°C	$V_2^+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	µA
over temperature range				200			200	µA
"0" Input Voltage	$V_2^+ = 4.75V$			0.8			0.8	V
"1" Input Voltage	$V_2^+ = 4.75V$	2.0			2.0			V
Short Circuit Output Current	$V_2^+ = 5.25V$, $V_{out} = 0V$	-40		-100	-40		-100	mA
POWER SUPPLY REQUIREMENTS								
Supply Voltage								
V_1^+		5		10	5		10	V
V_1^-		-6		-10	-6		-10	V
V_2^+		4.5	5	5.5	4.75	5	5.25	V
Supply Current	$V_1^+ = 10V$, $V_1^- = -10V$ $V_2^+ = 5.25V$							
I_1^+	$T_A = 125°C$			3.25				mA
	$T_A = 25°C$			3.75				mA
	$T_A = -55°C$			4.0				mA
	$0°C \leq T_A \leq 70°C$						5	mA
I_1^-	$T_A = 125°C$			7.0				mA
	$T_A = 25°C$			7.5				mA
	$T_A = -55°C$			8.5				mA
	$0°C \leq T_A \leq 70°C$						10	mA
I_2^+	$T_A = 125°C$			15				mA
	$T_A = 25°C$			16				mA
	$T_A = -55°C$			18				mA
	$0°C \leq T_A \leq 70°C$						20	mA
TRANSIENT RESPONSE	V_{in} = 50 mV overdrive							
Propagation Delay Time								
t_{pd} (0)	$T_A = +25°C$		10	20		10	20	ns
t_{pd} (1)	$T_A = +25°C$		12	22		12	22	ns
Delay between Output A and B	$T_A = +25°C$		2	5		2	5	ns
Strobe Delay Time								
Turn On	$T_A = +25°C$		6			6		ns
Turn Off	$T_A = +25°C$		6			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

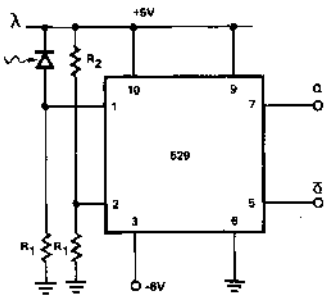
APPLICATIONS

One of the main features of the device is that supply voltages (V_1^+, V_1^-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_1^-) should always be at least five volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_1^+ and V_1^-) up to a maximum of ±6 volts as supply voltages are increased.

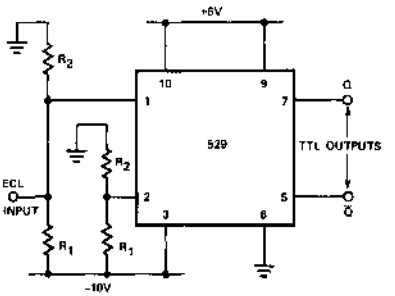
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

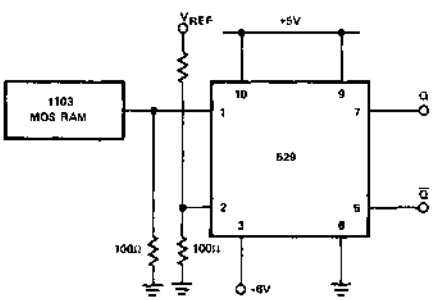
PHOTODIODE DETECTOR



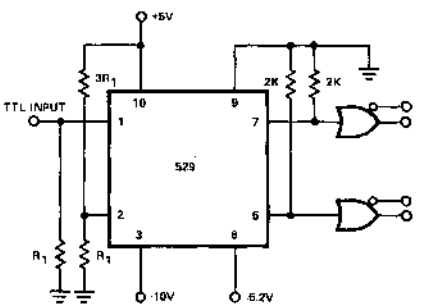
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP

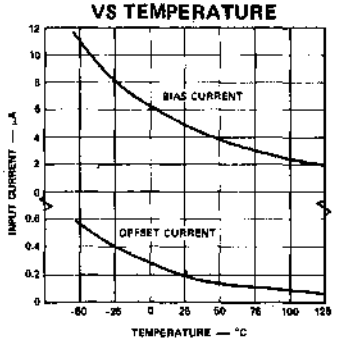


TTL TO ECL INTERFACE

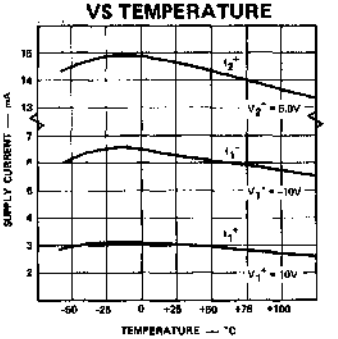


TYPICAL PERFORMANCE CURVES

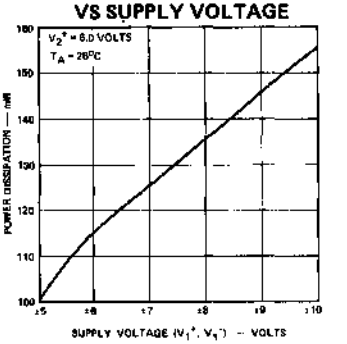
INPUT CURRENTS VS TEMPERATURE



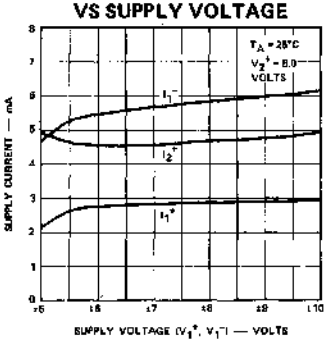
SUPPLY CURRENT VS TEMPERATURE



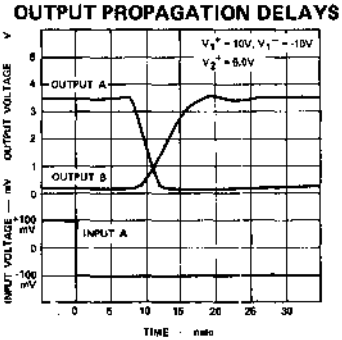
POWER DISSIPATION VS SUPPLY VOLTAGE



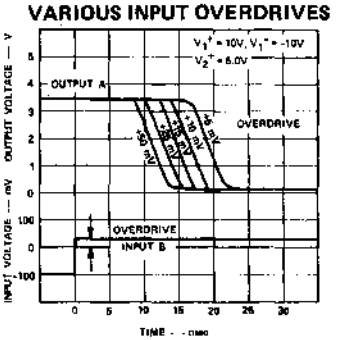
SUPPLY CURRENT VS SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains D.C. performance equal to the best general purpose types while providing far superior large signal A.C. performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier can be compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec SLEW RATE AT UNITY GAIN**
- **PIN FOR PIN REPLACEMENT FOR μA709, μA748 OR LM101**
- **COMPENSATED WITH A SINGLE CAPACITOR**
- **SAME LOW DRIFT OFFSET NULL CIRCUITRY AS μA741**
- **SMALL SIGNAL BANDWIDTH 1 MHz**
- **LARGE SIGNAL BANDWIDTH 500KHz**
- **TRUE OP AMP D.C. CHARACTERISTICS MAKE THE 531 THE IDEAL ANSWER TO ALL SLEW RATE LIMITED OPERATIONAL AMPLIFIER APPLICATIONS.**

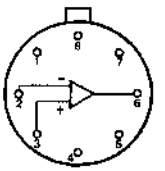
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	300mW
Differential Input Voltage	±15V
Common Mode Input Voltage (Note 2)	±15V
Voltage Between Offset Null and V^-	±0.5V
Operating Temperature Range	
NE531	0°C to +70°C
SE531	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

NOTES:
1. Rating applies for case temperatures to 125 °C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATION

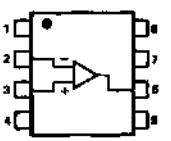
T PACKAGE
(Top View)



1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
SE531T/NE531T

V PACKAGE

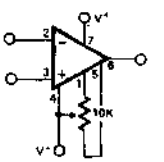


1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

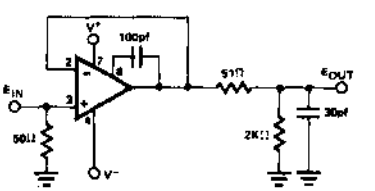
ORDER PART NO. NE531V

TYPICAL CIRCUITS

OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



GENERAL ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C Unless Otherwise Specified)

NE531

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10K\Omega$		2.0	6	mV
Input Offset Current			50	200	nA
Input Bias Current			0.4	1.5	µA
Input Resistance			20		MΩ
Input Voltage Range		±10			Volts
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		10	150	µV/V
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	20,000	60,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Full Power Bandwidth			500		KHz
Settling Time, 1%	A_V = +1, V_{IN} = ±10V		1.5		µsec
Settling Time, .01%	A_V = +1, V_{IN} = ±10V		2.5		µsec
Large Signal Overshoot	A_V = +1, V_{IN} = ±10V		2		%
Small Signal Overshoot	A_V = +1, V_{IN} = 400mV		5		%
Small Signal Risetime	A_V = +1, V_{IN} = 400mV		300		nsec
The Following Apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10K\Omega$			7.5	mV
Input Offset Current	T_A = +70°C			200	nA
	T_A = 0°C			300	nA
Input Bias Current	T_A = +70°C			1.5	µA
	T_A = 0°C			2.0	µA
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	15,000			
Output Voltage Swing	$R_L \geq 2K\Omega$	±10	±13		Volts
Slew Rate	A_V = 100		35		V/µs
	A_V = 10		35		V/µs
	A_V = 1 (non-inverting)	20	30		V/µs
	A_V = 1 (inverting)	25	35		V/µs
Supply Current	T_A = +70°C		4.5	5.5	mA

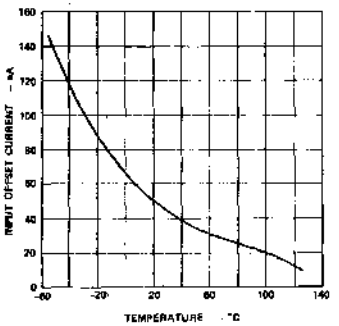
SE531

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10K\Omega$		2.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			300	500	nA
Input Resistance			20		MΩ
Input Voltage Range		±10			Volts
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	50,000	100,000		
Output Resistance			75		Ω
Supply Current			5.5	7.0	mA
Power Consumption			165	210	mW
Full Power Bandwidth			500		KHz
Settling Time, 1%	A_V = +1, V_{IN} = ±10V		1.5		µsec
Settling Time, .01%	A_V = +1, V_{IN} = ±10V		2.5		µsec
Large Signal Overshoot	A_V = +1, V_{IN} = ±10V		2		%
Small Signal Risetime	A_V = +1, V_{IN} = 400mV		300		nsec
Small Signal Overshoot	A_V = +1, V_{IN} = 400mV		5		%
Slew Rate	A_V = 100		35		V/µs
	A_V = 10		35		V/µs
	A_V = 1 (non-inverting)		30		V/µs
	A_V = 1 (inverting)		35		V/µs
The following apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10K\Omega$			6	mV
Input Offset Current	T_A = +125°C			200	nA
	T_A = -55°C			500	nA
Input Bias Current	T_A = +125°C			500	nA
	T_A = -55°C			1.5	µA
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		10	150	µV/V
Large Signal Voltage Gain	R_L = 2KΩ, V_{OUT} = ±10V	25,000			
Output Voltage Swing	R_L = 2KΩ	±10	±13		V
Supply Current	T_A = +125°C		4.5	5.5	mA

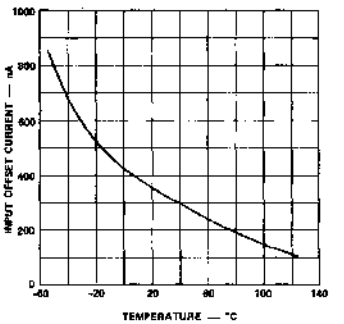
NOTES:
All AC parametric testing is performed using the conditions of the transient response test circuit, page 1.

TYPICAL PERFORMANCE CHARACTERISTICS (V_S = ±15V, T_A = +25°C unless otherwise noted)

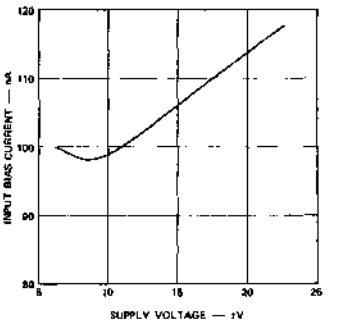
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



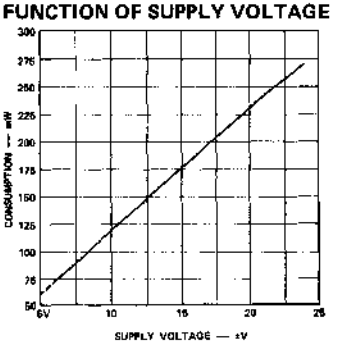
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



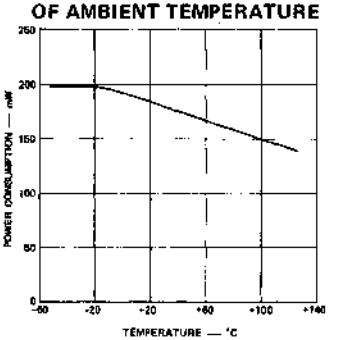
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



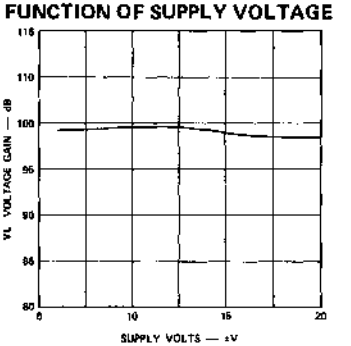
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



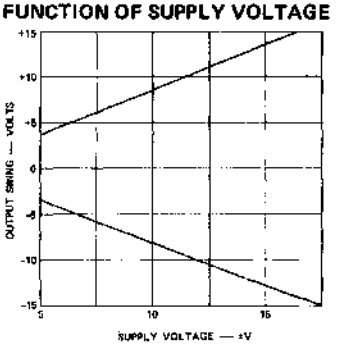
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



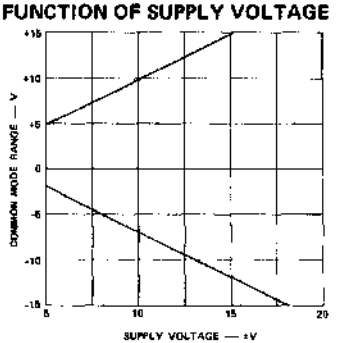
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



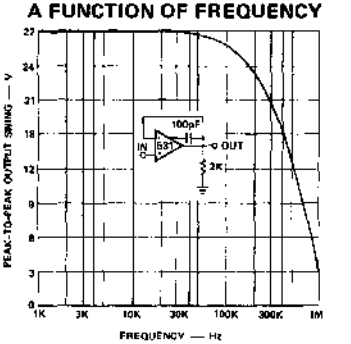
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

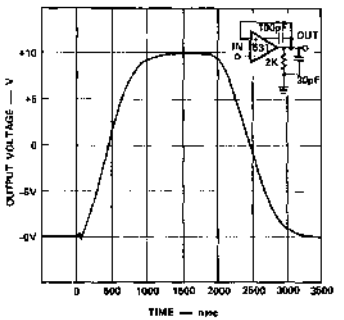


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

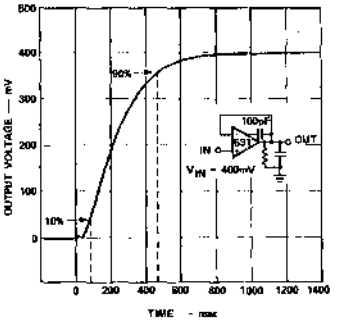


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

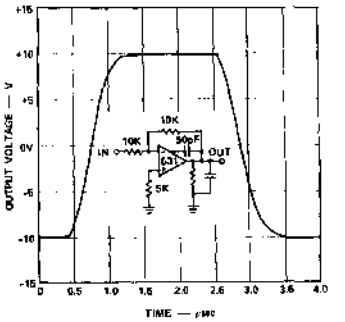
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



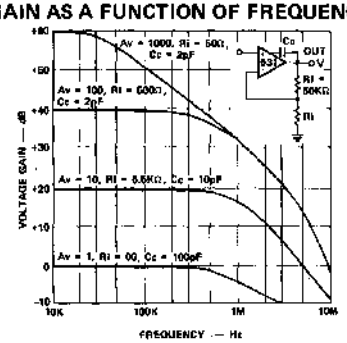
VOLTAGE FOLLOWER TRANSIENT RESPONSE



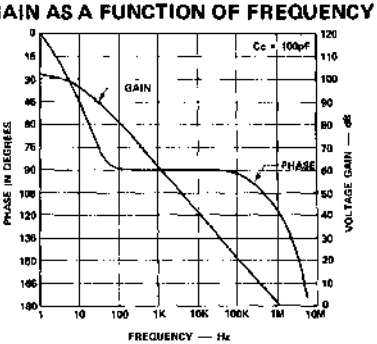
UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE



CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

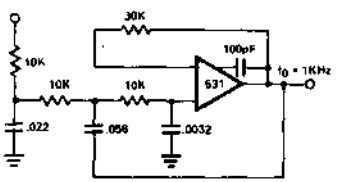


OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

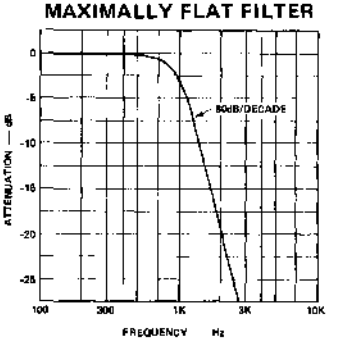


TYPICAL APPLICATIONS

3 POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



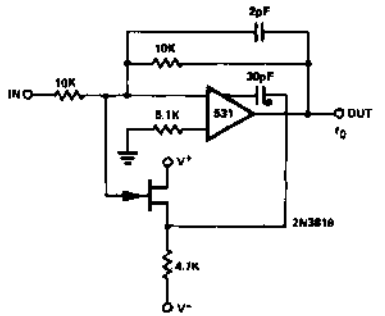
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



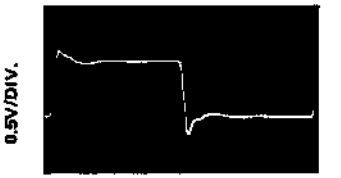
*Reference — EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokaw

TYPICAL APPLICATIONS (Cont'd.)

HIGH SPEED INVERTER (10MHz Bandwidth)

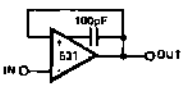


PULSE RESPONSE
HIGH SPEED INVERTER

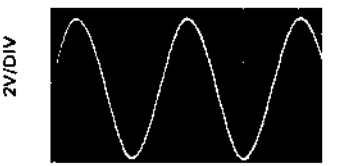


200nsec/DIV

FAST SETTLING VOLTAGE FOLLOWER



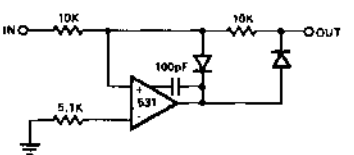
LARGE SIGNAL RESPONSE
VOLTAGE FOLLOWER



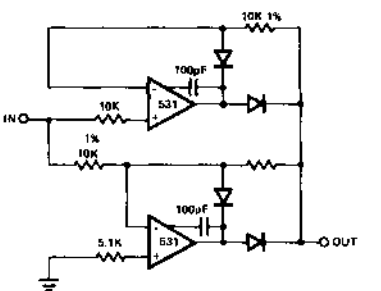
0.5μs/DIV f = 500KHz

PRECISION RECTIFIERS

(a) HALF WAVE

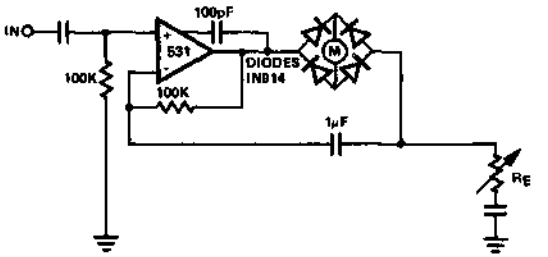


(b) FULL WAVE

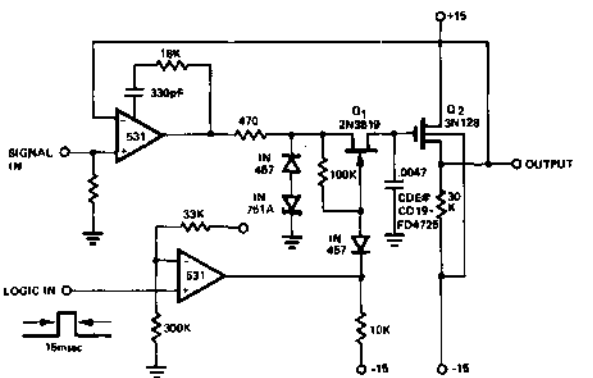


TYPICAL APPLICATIONS (Cont'd.)

AC MILLIVOLTMETER



SAMPLE AND HOLD



DESCRIPTION

The PA239 is a dual low noise preamplifier featuring two identically-matched 68dB gain amplifiers fed from an internal zener regulated power supply.
Operation requires only a single power supply and a minimum number of external frequency shaping components.

FEATURES

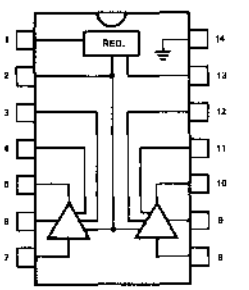
- MATCHED OPEN LOOP VOLTAGE GAIN
- LOW AUDIO NOISE
- SINGLE POWER SUPPLY
- WIDE POWER SUPPLY RANGE
- BUILT-IN POWER SUPPLY FILTER
- HIGH INPUT IMPEDANCE
- EMITTER FOLLOWER OUTPUT
- LOW DISTORTION
- SELF BIASING
- MINIMUM NUMBER OF EXTERNAL COMPONENTS
- OUTPUT CIRCUIT IS SHORT CIRCUIT PROTECTED
- HIGH CHANNEL SEPARATION
- VARIETY OF FEEDBACK OPTIONS
- NO CIRCUIT DAMAGE IF PLUGGED IN BACKWARDS
- 7.5V REGULATOR BIAS SOURCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	16V
Temperature	
Storage	-55°C to +150°C
Operating	-30°C to +85°C

PIN CONFIGURATION

A PACKAGE
(Top View)



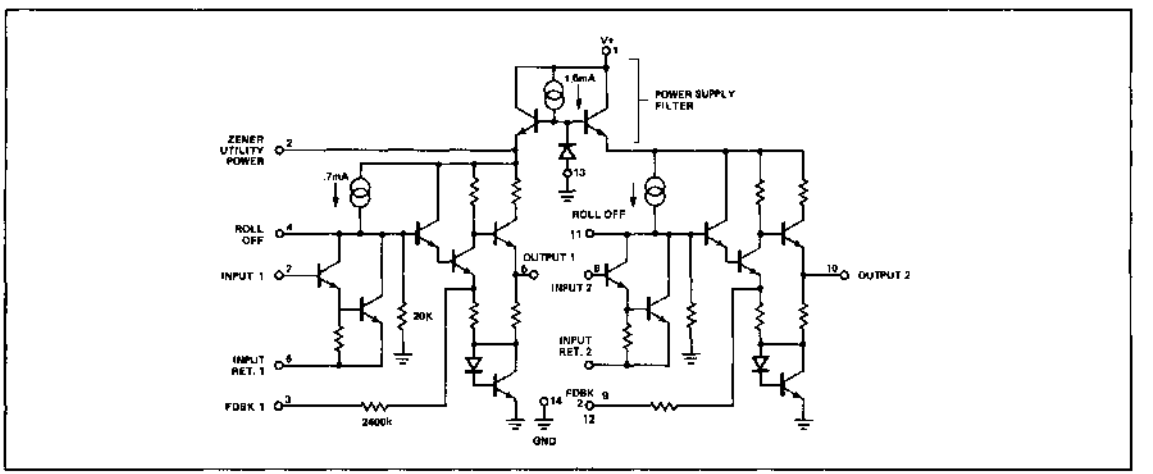
1. V+
2. Zener
3. Feedback 1
4. Roll 1
5. Out 1
6. Input Ret. 1
7. Input 1
8. Input 2
9. Input Ret. 2
10. Out 2
11. Roll 2
12. Feedback 2
13. Reg. Gnd.
14. Amp. Gnd.

ORDER PART NO.
PA239A

APPLICATIONS

STEREO TAPE PLAYERS/RECORDERS
DICTATING EQUIPMENT
MOVIE PROJECTORS
PHONOGRAPHS
TV REMOTE CONTROL RECEIVER
MICROPHONE AMPLIFIERS
STEREO RADIO RECEIVER SYSTEMS
VIDEO PREAMPLIFICATION
NARROW BAND AMPLIFICATION
DRIVER-PREAMP FOR LOSSY NETWORKS
SUPER GAIN CASCADED AMPLIFIERS

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (25°C) (V_{CC} = 12V)

PARAMETERS	MIN	TYP	MAX	UNITS
Supply Current (V_{CC} = 12V)		16	22	mA
Voltage Gain	65	68	71	dB
Gain Balance		0.3	2	dB
Channel Separation (f = 1 kHz), Figure 1	45	90		dB
Input Resistance	100K	250K		Ω
Signal Output		1.5		Vrms
Output Resistance		100		Ω
Power Supply Rejection (f = 1 kHz), Figure 2	45	55		dB
Total Harmonic Distortion Without Feedback (0.5V rms into 3kΩ Load, 1 kHz)		0.5	0.9	%
Input dc Bias Current		0.8	3	μA
Gain to Feedback Terminal 3, 12		45		dB
Impedance at Feedback Terminal		2400		Ω
Amplifier Noise Figure (100Hz to 10 kHz, 5kΩ Rs)		1.8		dB
Equivalent Input Noise (100Hz to 10 kHz, 680Ω Rs)		0.7	1.2	μV

TEST CIRCUITS

CHANNEL SEPARATION

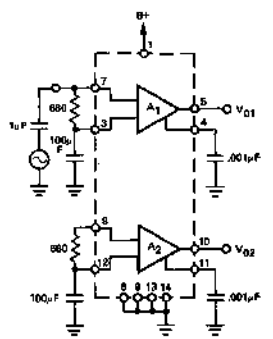


Figure 1

POWER SUPPLY REJECTION

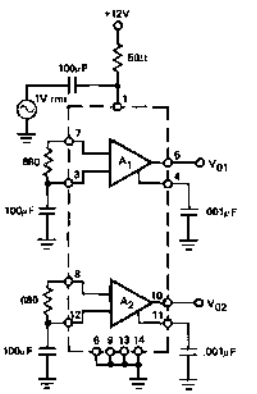


Figure 2

NOISE

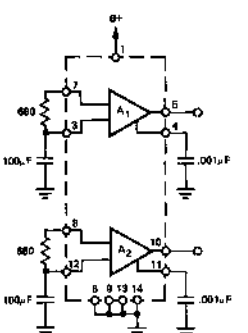


Figure 3

DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing a FET input stage for extremely high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

- 5pA INPUT BIAS CURRENT
- INPUT AND OUTPUT PROTECTION
- OFFSET NULL CAPABILITY
- INTERNALLY COMPENSATED
- 6V/μsec SLEW RATE
- STANDARD PINOUT
- 1 MHz UNITY GAIN BANDWIDTH

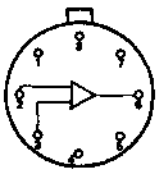
ABSOLUTE MAXIMUM GUARANTEED RATINGS

Supply Voltage		±22V
Differential Input Voltage Range		±30V
Common Mode Input Voltage Range		$\pm V_s$
Power Dissipation (Note 1)		500mW
Operating Temperature Range	SU536T	−55°C to +85°C
	NE536T	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Solder, 60 sec)		300°C
Output Short Circuit Duration (Note 2)		Indefinite

NOTES:
1. Rating applies for case temperatures to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75 °C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATION

T PACKAGE
(Top View)

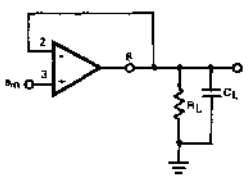


1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

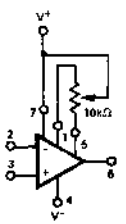
ORDER PART NOS. SE536T/NE536T

TYPICAL APPLICATIONS

VOLTAGE FOLLOWER CIRCUIT



OFFSET NULL CIRCUIT



ELECTRICAL CHARACTERISTICS (SU536: $\pm 6V \leq V_S \leq \pm 20V$; NE536: $V_S = \pm 15V$ unless otherwise noted.)

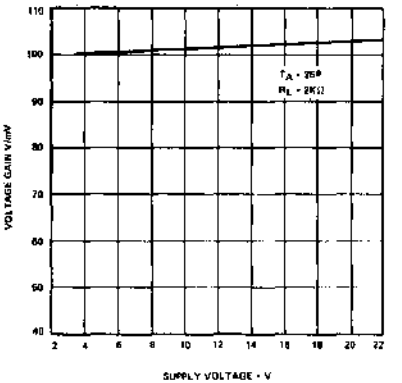
PARAMETER	TEST CONDITIONS	SU536			NE536			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISITICS								
Large Signal Voltage Gain @ +25°C	$V_S = \pm 15$ V, $V_{OUT} = \pm 10V$	50	100		50	100		V/mV
Over Temperature Range	$R_L \geq 2k\Omega$	50	100		25	100		V/mV
Input Offset Voltage @ +25°C			7.5	20		30	90	mV
Over Temperature Range			7.5	30		30		mV
vs Temperature (drift)			20			30		µV/°C
vs Common Mode Voltage (C.M.R.R.)	$V_{IN} = \pm 10V$, $R_S \leq 10k\Omega$	70	80		64	80		dB
vs Power Supply (P.S.R.R.)	Note 1, $R_S \leq 10k\Omega$		50	150		100	300	µV/V
Input Current @ +25°C			5	30		30	100	pA
Over Temperature Range	Either Input		250	3000				pA
vs Temperature (drift)			Typ. Doubles Every 10°C					
Input Offset Current @ +25°C			5			5		pA
Over Temperature (drift)								
Input Impedance								
Differential Resistance	$T_A = +25°C$		10^{14}			10^{14}		Ω
Differential Capacitance	$T_A = +25°C$		6			6		pF
Input Noise (0.1Hz – 100kHz)								
Voltage Noise			20			20		µVrms
Common Mode Voltage Range	$V_S = \pm 15V$	±10	±11		±10	±11		V
OUTPUT CHARACTERISTICS								
Output Current	$V_S = \pm 15V$	5			5			mA
Open Loop Output Impedance			100			100		Ω
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 2k\Omega$	±10	±12		±10	±10		V
	$V_S = \pm 15V$, $R_L \geq 10k\Omega$	±12	±13		±12	±13		V
Short Circuit Current	$V_S = \pm 15V$, $T_A = +25°C$		17			17		mA
FREQUENCY AND TRANSIENT RESPONSE								
Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = +25°C$, A = 100		1			1		MHz
Unity Gain Frequency	$V_S = \pm 15V$, $T_A = +25°C$		1			1		MHz
Full Power Bandwidth	$V_S = \pm 15V$, $T_A = +25°V$		100			100		kHz
Slew Rate								
Inverter	$V_S = \pm 15V$, $T_A = +25°C$, A = –1		6			6		V/µs
Follower	$V_S = \pm 15V$, $T_A = +25°C$, A = +1		6			6		V/µs
POWER SUPPLY REQUIREMENT								
Power Supply Range		±6		±20	±6		±18	V
Quiescent Supply Current	$V_S = \pm 20V$, $V_{OUT} = 0V$, $T_A = +25°C$		4.5	5.5				mA
	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = +25°C$					6.0	8.0	mA
Quiescent Power Dissipation	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = +25°C$		180			180		mW

Parameters are tested over temperature range unless otherwise noted.

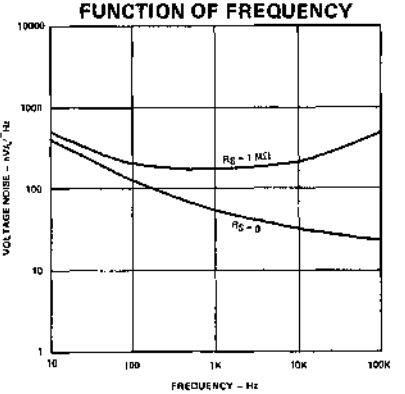
NOTE 1: SU536: $V_S = \pm 6V$ to $\pm 20V$
NE536: $V_S = \pm 6V$ to $\pm 15V$

TYPICAL CHARACTERISTIC CURVES

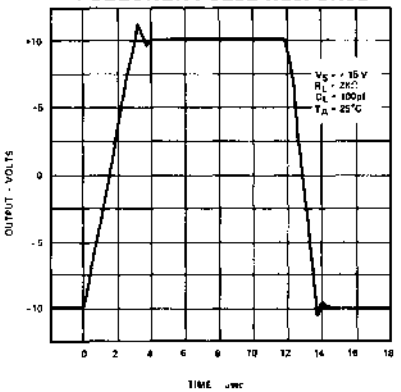
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



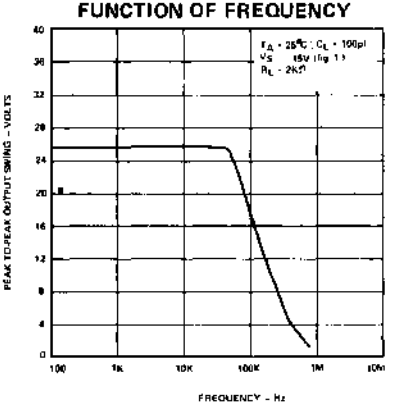
INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



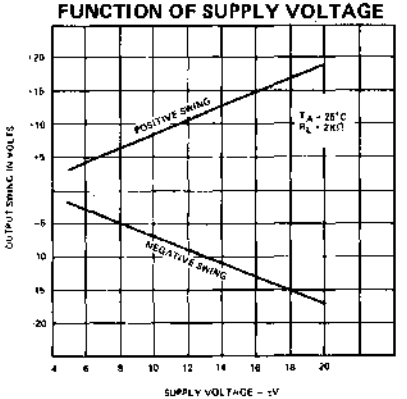
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



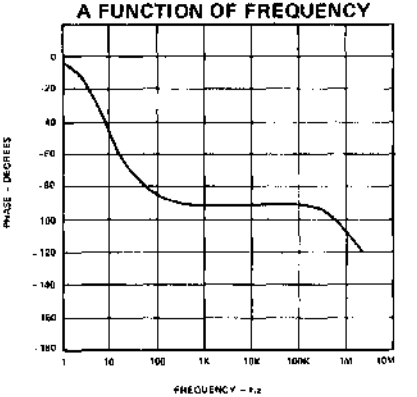
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

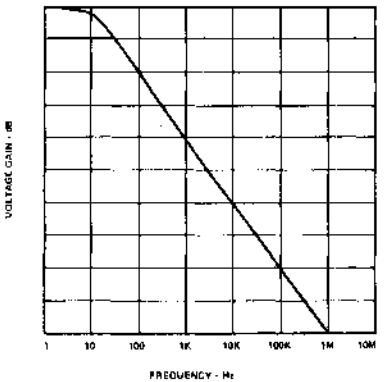


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

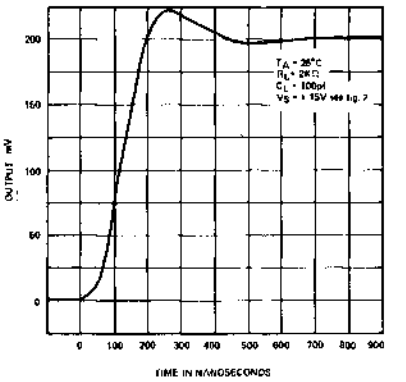


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

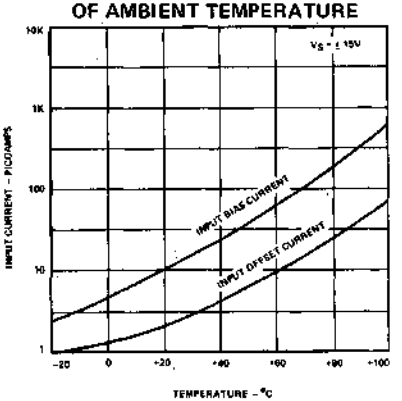
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



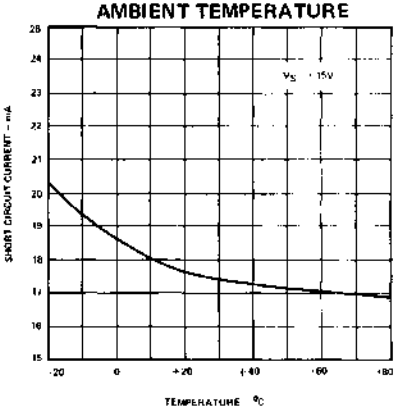
VOLTAGE FOLLOWER TRANSIENT RESPONSE



INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



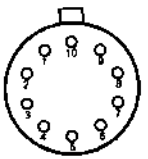
LINEAR INTEGRATED CIRCUITS

The 540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

- **INTERNAL CURRENT LIMITING**
- **LOW STANDBY CURRENT**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **WIDE POWER BANDWIDTH**
- **LOW DISTORTION**

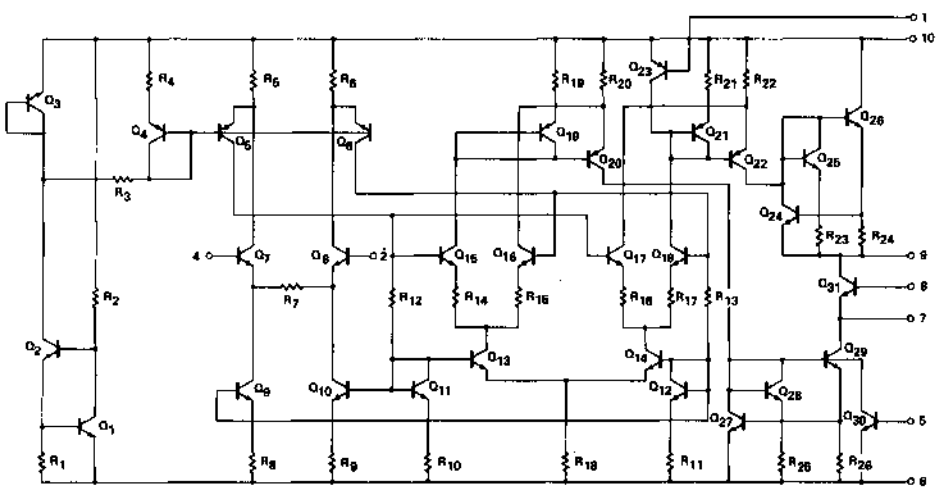
Supply Voltage	± 27 Volts SE540
	± 22 Volts NE540
Operating Temperature Range	-55°C to +125°C SE540
	0°C to +70°C NE540
Storage Temperature Range	-65°C to +150°C
Output Short Circuit Duration (Not exceeding maximum dissipation.)	Indefinite

L PACKAGE
(Top View)



1. Power Limit
2. Non Inverting Input
3. NC
4. Inverting Input
5. Power Limit
6. V^-
7. Output 1 (emmitter)
8. Output 2 (base)
9. Output 3 (collector)
10. V^+

ORDER PART NOS. SE540L/NE540L

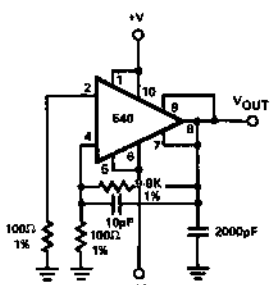


ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 540			NE 540			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Temperature Range		-55		+125	0		+70	°C
Operating Supply Voltage		±5		±25	±5		±20	Volts
Quiescent Current			13	20		13	20	mA
Input Offset Voltage			5	7		7	10	mV
Input Offset Current			0.3	0.7		0.5	1	μA
Input Bias Current			1.5	3		2	5	μA
Input Impedance	40 dB Gain		20			20		kΩ
Current Gain		80	100		70	90		dB
Gain Variation Over Temperature Range	40 dB Gain		±0.1			±0.1		dB
Frequency Response	40 dB Gain ±1 dB		500			100		kHz
Distortion	40 dB Gain Output 3 dB below maximum R_L = 600Ω		0.25	0.5		0.5	1.0	%
	R_L = 2K Ω		0.06			0.06		
Equivalent Input Noise Voltage	R_S = 600Ω 50 Hz to 500 kHz		10			10		μV
Power Supply Rejection Ratio	40 dB Gain	80	90		60	80		dB
Common Mode Rejection Ratio			110			90		dB
Output Drive Current		±120	±150		±80	±100		mA
Slew Rate	V_S = ±20V V_{OUT} = ±15V		200			200		V/μs

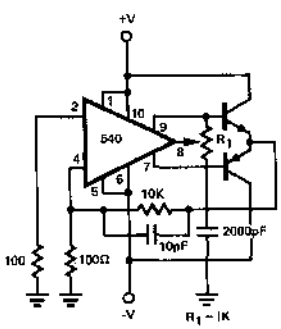
TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT



$V_{OFFSET} = \frac{V_{OUT}}{100}$

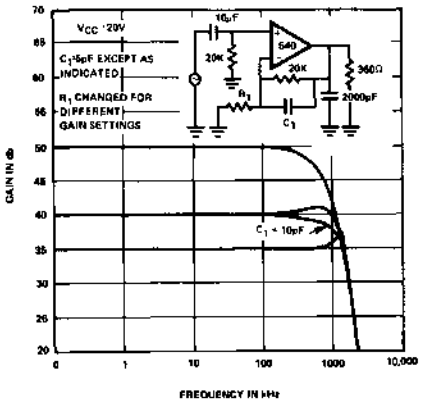
OUTPUT BIAS CONTROL



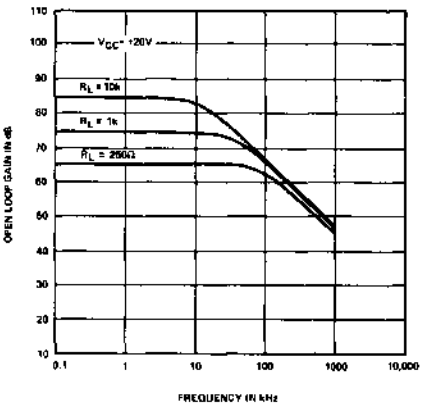
BIAS CONTROL FOR OUTPUT TRANSISTORS

TYPICAL PERFORMANCE CHARACTERISTICS

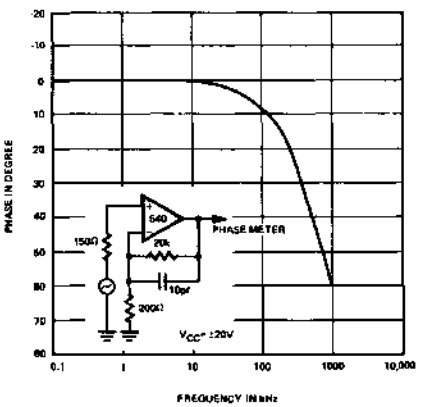
CLOSED LOOP FREQUENCY RESPONSE



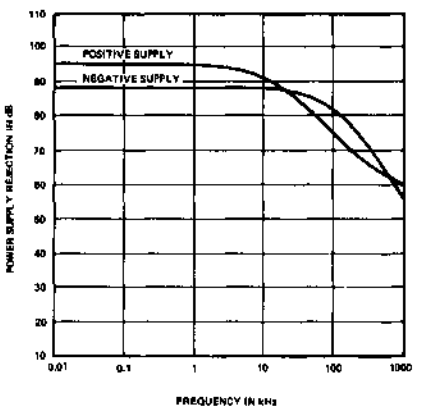
OPEN LOOP GAIN AND FREQUENCY RESPONSE



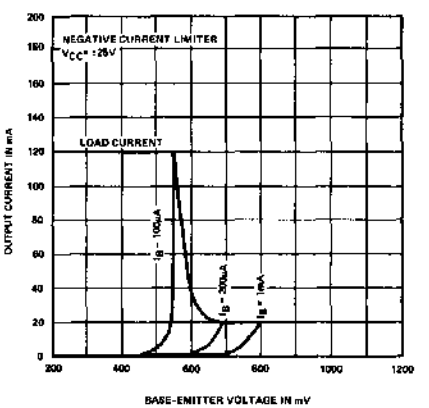
PHASE RESPONSE VERSUS FREQUENCY



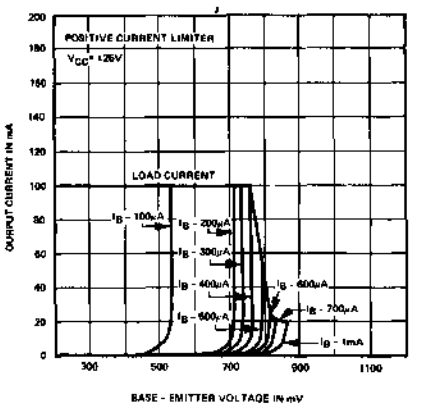
POWER SUPPLY REJECTION VERSUS FREQUENCY



OUTPUT CURRENT VERSUS I_B/V_{BE} OF CURRENT LIMITER

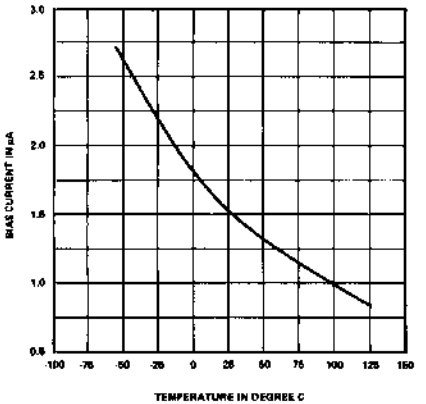


OUTPUT CURRENT VERSUS I_B/V_{BE} OF CURRENT LIMITER

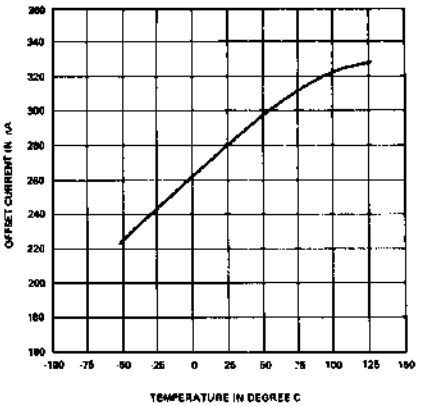


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd.)

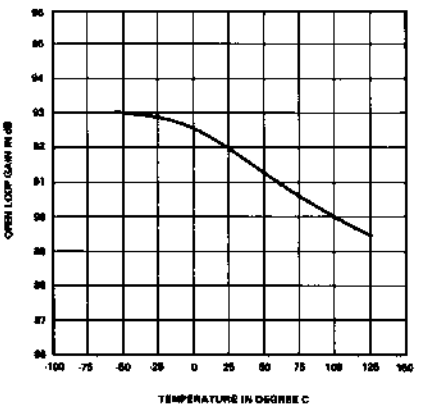
BIAS CURRENT VERSUS TEMPERATURE



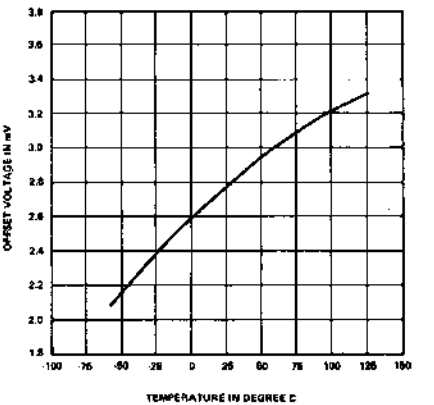
OFFSET CURRENT VERSUS TEMPERATURE



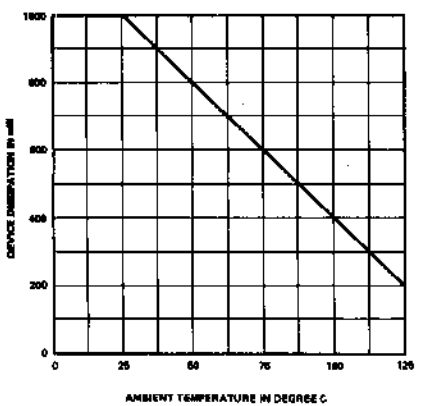
OPEN LOOP GAIN VERSUS TEMPERATURE



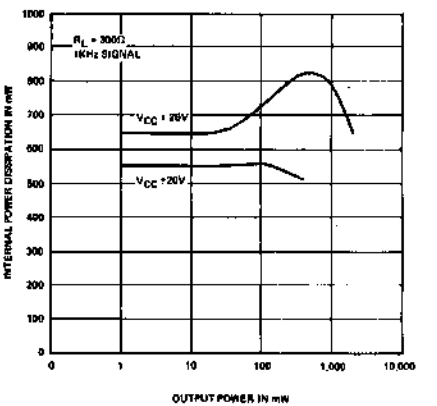
OFFSET VOLTAGE VERSUS TEMPERATURE



MAXIMUM DISSIPATION VERSUS AMBIENT TEMPERATURE

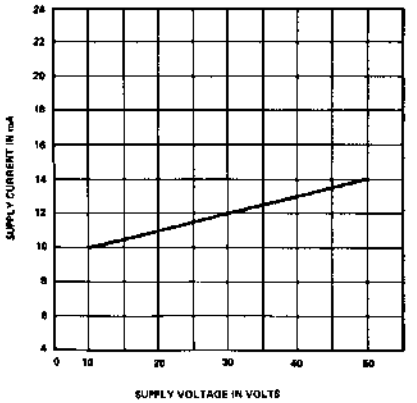


INTERNAL POWER DISSIPATION VERSUS LOAD POWER

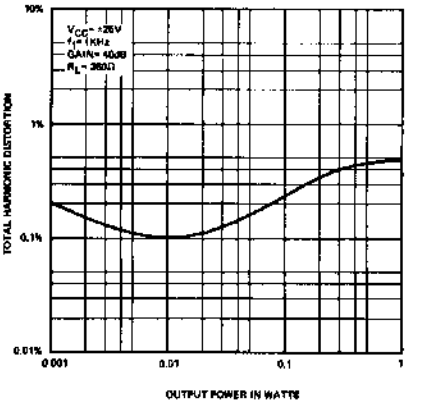


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd.)

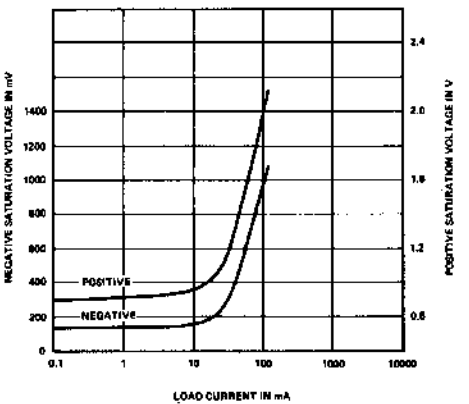
QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE



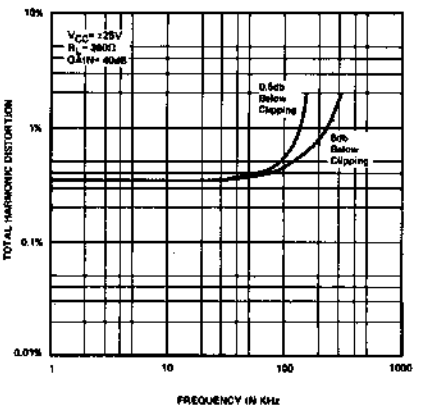
TOTAL HARMONIC DISTORTION VERSUS OUTPUT



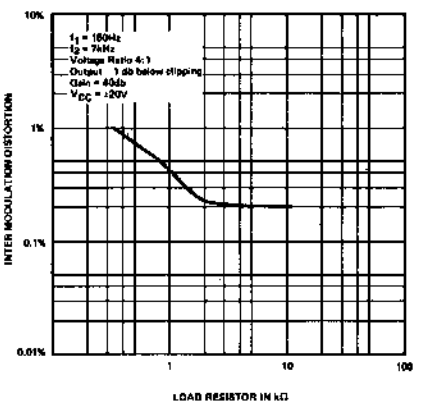
OUTPUT SATURATION VOLTAGE VERSUS LOAD



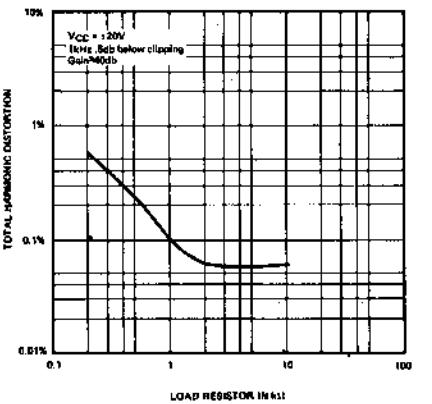
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



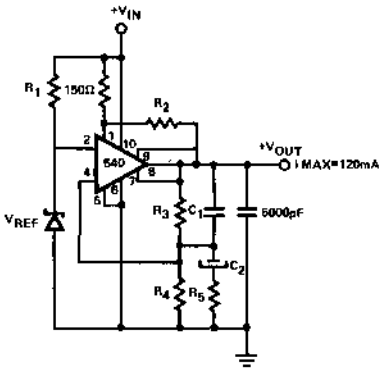
INTERMODULATION DISTORTION VERSUS LOAD

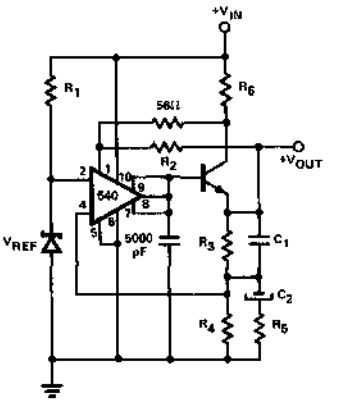


TOTAL HARMONIC DISTORTION VERSUS LOAD



POSITIVE VOLTAGE REGULATORS



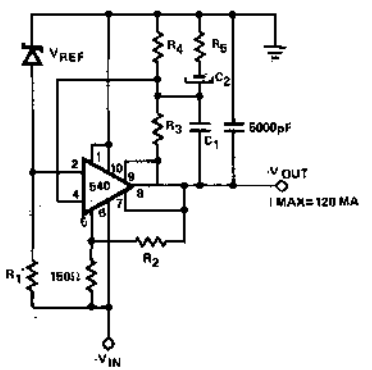


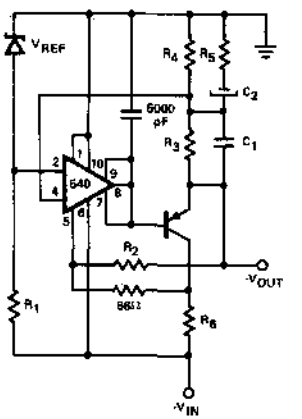
$$V_{OUT} \simeq \frac{R_3 + R_4}{R_4} V_{REF} \qquad R_6 \simeq \frac{R_3}{100}$$

$$R_1 \simeq \frac{V_{IN} - V_{REF}}{I_{ZENER}} \qquad C_1 \simeq \frac{0.2}{R_3}\ \mu F$$

$$R_2 \simeq \frac{2\ V_{IN} - V_{OUT}}{4mA} \qquad C_2 \simeq 10\ \mu F$$

NEGATIVE VOLTAGE REGULATORS





$$V_{OUT} \simeq \frac{R_3 + R_4}{R_4} V_{REF} \qquad R_6 \simeq \frac{R_3}{100}$$

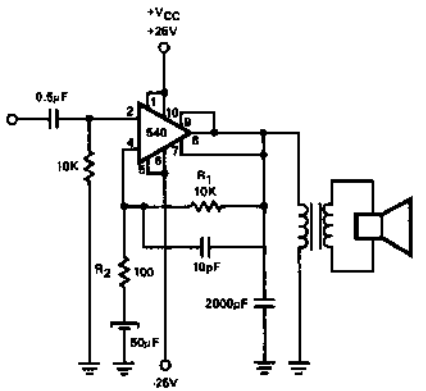
$$R_1 \simeq \frac{V_{IN} - V_{REF}}{I_{ZENER}} \qquad C_1 \simeq \frac{0.2}{R_3}\ \mu F$$

$$R_2 \simeq \frac{2\ V_{IN} - V_{OUT}}{4mA} \qquad C_2 \simeq 10\ \mu F$$

TYPICAL APPLICATIONS

POWER AMPLIFIERS

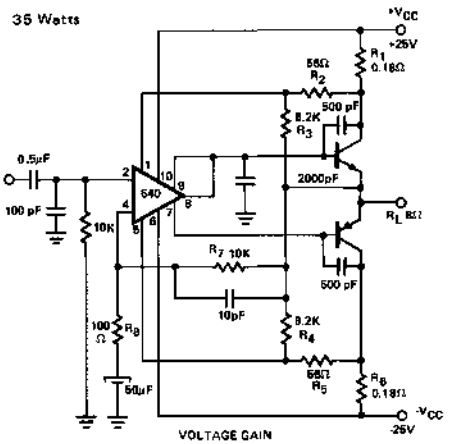
1 Watt



VOLTAGE GAIN

$A_V \simeq \frac{R_1 + R_2}{R_2}$

35 Watts



VOLTAGE GAIN

$A_V \simeq \frac{R_7 + R_8}{R_8}$

CURRENT LIMITING

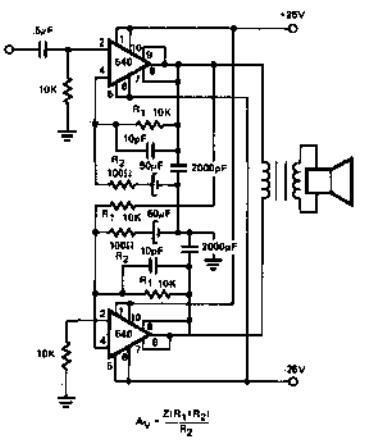
$R_1 = R_6 \simeq \frac{650mV}{I_{peak}}$

POWER LIMITING

$R_2 = R_5 \simeq 56\Omega$

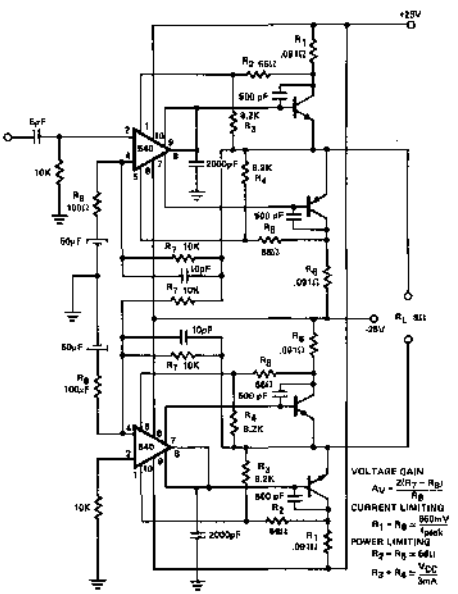
$R_3 = R_4 \simeq \frac{V_{CC}}{5mA}$

3 Watts



$A_V \simeq \frac{2(R_1 + R_2)}{R_2}$

70 Watts



VOLTAGE GAIN

$A_V \simeq \frac{2(R_7 + R_8)}{R_8}$

CURRENT LIMITING

$R_1 = R_6 \simeq \frac{650mV}{I_{peak}}$

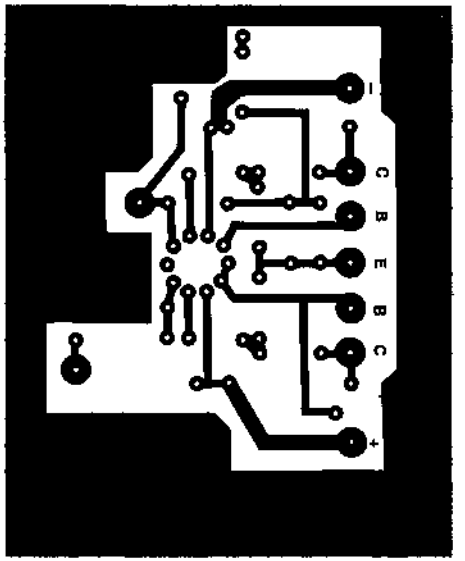
POWER LIMITING

$R_2 = R_5 \simeq 56\Omega$

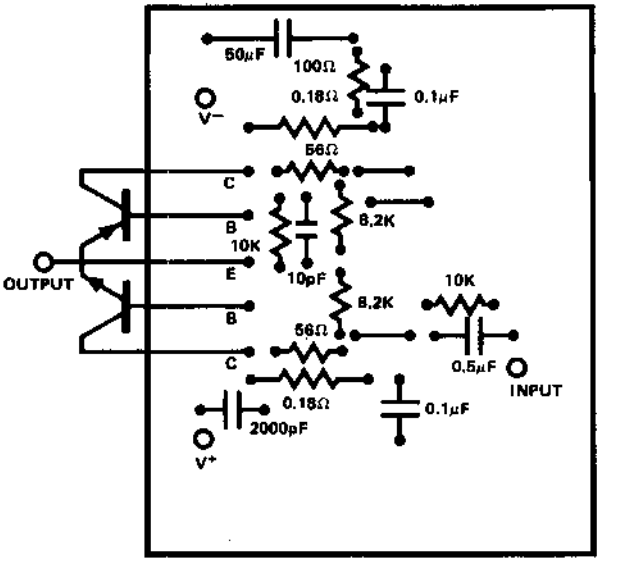
$R_3 + R_4 \simeq \frac{V_{CC}}{5mA}$

35 WATT AMPLIFIER

P.C. BOARD LAYOUT (BOTTOM VIEW)



PARTS LAYOUT (TOP VIEW)



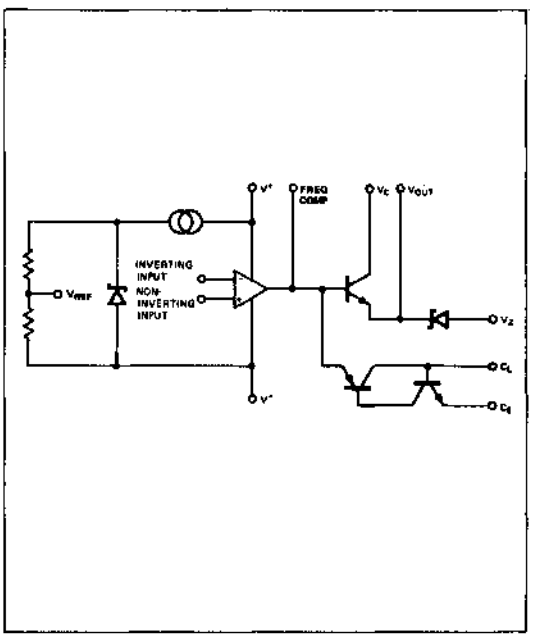
DESCRIPTION

The 550 is a precision monolithic voltage regulator capable of positive or negative supply operation as series, shunt, switching or floating regulator. Guaranteed line regulation is provided for input voltages ranging from 8.5 volts to as high as 50 volts. The output voltage can be continuously adjusted from 2 volts to 40 volts. Foldback current limiting can be accomplished through the use of one external resistor. Internal circuitry permits on and off strobing with DTL and TTL logic inputs and latched shut-down with a pulsed input.

FEATURES

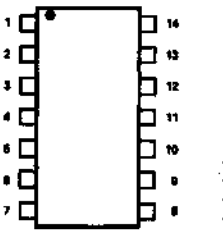
- **LINE REGULATION GUARANTEED OVER INPUT VOLTAGE RANGE OF 8.5 VOLTS TO AS HIGH AS 50 VOLTS.**
- **OUTPUT VOLTAGE CONTINUOUSLY ADJUSTABLE FROM 2 VOLTS TO 40 VOLTS**
- **.01% LINE AND LOAD REGULATION**
- **ADJUSTABLE LIMITING OF SHORT CIRCUIT CURRENT**
- **FOLDBACK CURRENT LIMITING WITH ONE EXTERNAL RESISTOR**
- **REMOTE AND LATCHING SHUTDOWN**
- **OUTPUT CURRENT UP TO 150mA WITHOUT EXTERNAL POWER TRANSISTORS**

BASIC CIRCUIT SCHEMATIC



PIN CONFIGURATIONS

A PACKAGE
(Top View)



1. NC
2. Current Limit
3. Current Sense
4. Inverting Input
5. Noninverting Input
6. V_{REF}
7. V^-
8. NC
9. V_Z
10. V_{out}
11. V_C
12. V^+
13. Frequency Compensation
14. NC

ORDER PART NO. NE550A

L PACKAGE

1. Current Sense
2. Inverting Input
3. Noninverting Input
4. V_{REF}
5. V^-
6. V_{out}
7. V_C
8. V^+
9. Frequency Compensation
10. Current Limit

ORDER PART NOS. NE550L/SE550L

ABSOLUTE MAXIMUM RATINGS:

	SE550	NE550
Voltage from V^+ to V^-	50V	40V
Input-Output Voltage Differential	45V	37V
Maximum Output Current	150mA	150mA
Current from V_Z	15mA	15mA
Internal Power Dissipation (Note 1)	800mW	800mW
Operating Temperature Range	−55°C to +125°C	−0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature	300°C	300°C

NOTE:
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Notes 1 and 2)

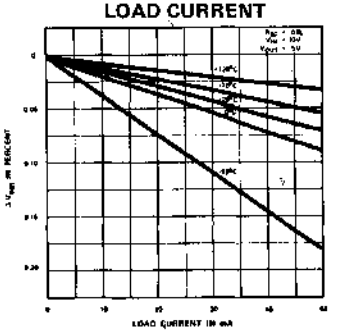
PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
NE550					
Line Regulation		.08	0.3	% V_{out}	V_{in} = 8.5 to 40V
			0.35	% V_{out}	0°C ≤ T_A ≤ 70°C, V_{in} = 12 to 40V
Load Regulation		.03	0.2	% V_{out}	I_L = 1mA to 50mA
			0.4	% V_{out}	0°C ≤ T_A ≤ 70°C, I_L = 1mA to 50mA
Ripple Rejection		75		dB	f = 50 Hz to 10 kHz, CREF = 0
		90		dB	f = 50 Hz to 10 kHz, CREF = 5μF
Average Temperature Coefficient of Output Voltage		.002	.015	%/°C	0°C ≤ T_A ≤ 70°C
Short Circuit Current Limit	50	60	70	mA	RSC = 10Ω, V_{out} = 0
Reference Voltage	1.53	1.63	1.73	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long Term Stability		0.1		%/1000 hrs.	
Standby Current Drain		1.6	3.0	mA	I_L = 0, V_{in} = 40V
Input Voltage Range	8.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
SE550					
Line Regulation		0.05	0.1	% V_{out}	V_{in} = 12 to 40V
		0.2	0.6	% V_{out}	V_{in} = 8.5 to 50V
			0.25	% V_{out}	-55°C ≤ T_A ≤ +125°C, V_{in} = 12 to 40V
Load Regulation		0.03	.10	% V_{out}	I_L = 1mA to 50mA
			.6	% V_{out}	-55°C ≤ T_A ≤ +125°C, I_L = mA to 50mA
Ripple Rejection		75		dB	F = 50 Hz to 10 kHz, CREF = 0
		90		dB	F = 50 Hz to 10 kHz, CREF = 5μF
Average Temperature Coefficient of Output Voltage		.002	.012	%/°C	-55°C ≤ T_A ≤ +125°C
Short Circuit Limit	50	60	70	mA	RSC = 10Ω, V_{out} = 0
Reference Voltage	1.58	1.63	1.68	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long Term Stability		0.1		%/1000 hrs.	
Standby Current Drain		1.3	2.0	mA	I_L = 0, V_{in} = 50V
Input Voltage Range	8.5		50	V	
Output Voltage Range	2.0		40	V	
Input-Output Voltage Differential	3.0		45	V	

NOTES

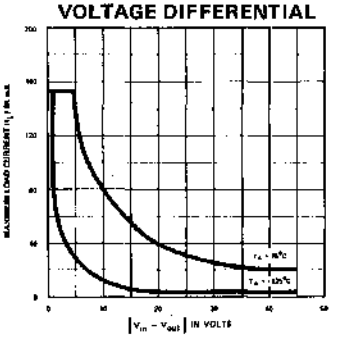
1. Unless otherwise specified, T_A = 25°C, V_{in} = V^+ = V_C = 12V, V^- = 0V, V_{out} = 5V, I_L = 1mA, R_{sc} = 0, C_1 = 100pF, and divider impedance as seen by error amplifier ≃ 2kΩ when connected as shown in Figure 1.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

TYPICAL CHARACTERISTIC CURVES

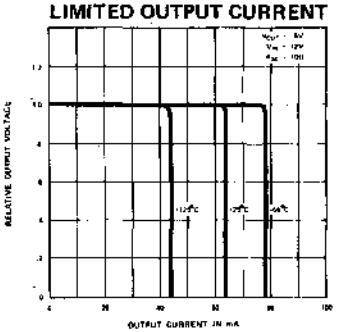
LOAD REGULATION AS A FUNCTION OF LOAD CURRENT



MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

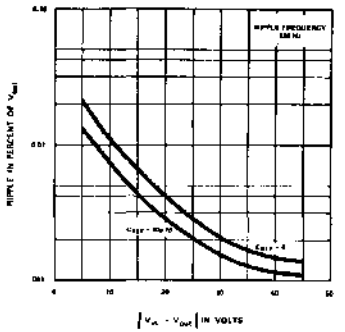


RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LIMITED OUTPUT CURRENT

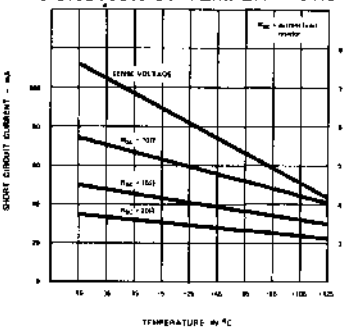


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

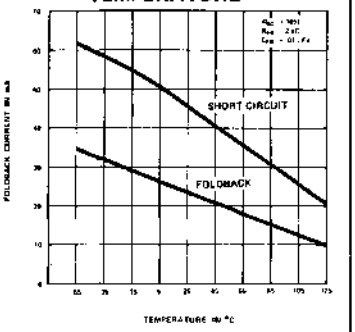
RIPPLE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



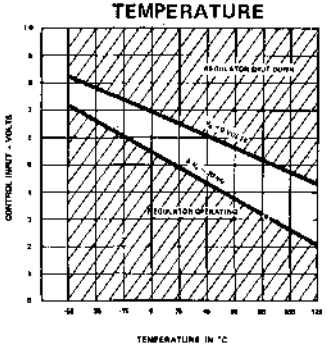
SENSE VOLTAGE AND SHORT CIRCUIT CURRENT LIMIT AS A FUNCTION OF TEMPERATURE



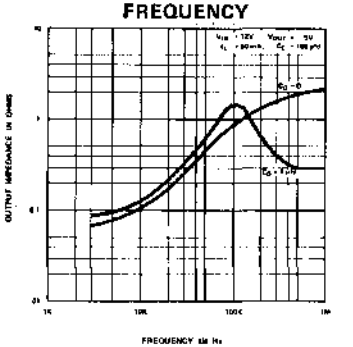
SHORT CIRCUIT AND FOLDBACK CURRENTS AS A FUNCTION OF TEMPERATURE



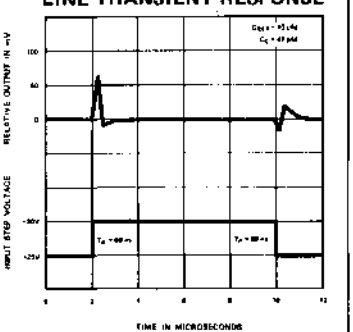
REMOTE CONTROL CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



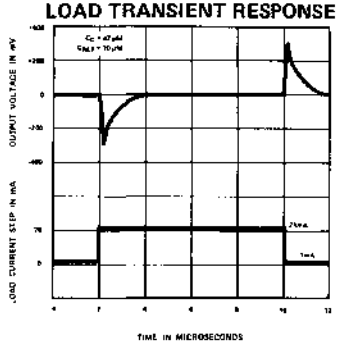
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



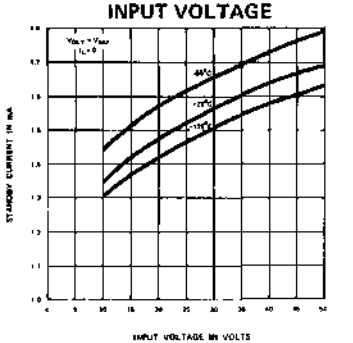
LINE TRANSIENT RESPONSE



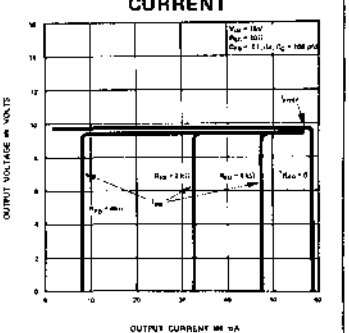
LOAD TRANSIENT RESPONSE



STANDBY CURRENT AS A FUNCTION OF INPUT VOLTAGE

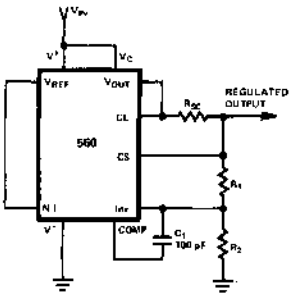


FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



TYPICAL APPLICATIONS

BASIC POSITIVE VOLTAGE REGULATOR

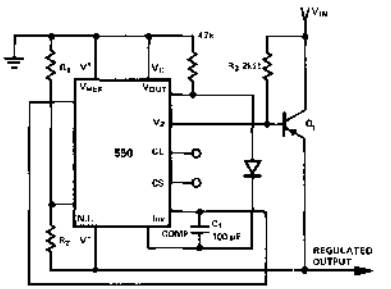


$$V_{out} = V_{REF}\ \frac{R_1 + R_2}{R_2}\ I_{SE} = \frac{V_{SENSE}}{R_{SC}}$$

$\frac{R_1\ R_2}{R_1 + R_2}$ = 2kΩ for minimum temperature drift

FIGURE 1

NEGATIVE VOLTAGE REGULATOR



$$V_{out} = -V_{REF} \times \frac{R_1 + R_2}{R_2}$$

$\frac{R_1\ R_2}{R_1 + R_2}$ = 2kΩ for minimum temperature drift

NOTE 1

FIGURE 2

POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)

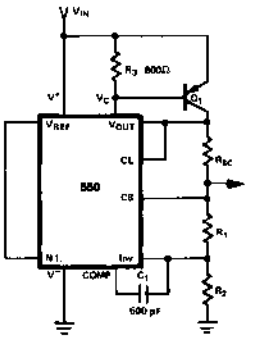


FIGURE 3

POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)

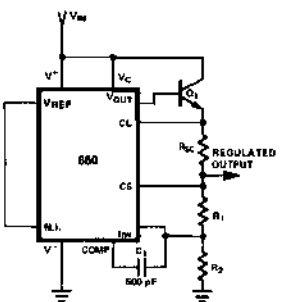
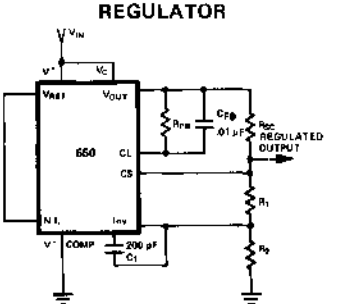


FIGURE 4.

FOLDBACK CURRENT LIMITED REGULATOR



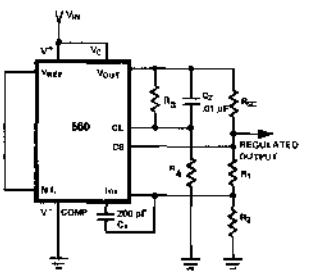
$$I_{KNEE} = \frac{V_{SENSE}}{R_{SC}}$$

$$I_{FB} = \frac{V_{SENSE} - (R_{FB} \cdot I_{CL})}{R_{SC}}$$

$I_{CL} \cong 125\ \mu A$

FIGURE 5A

SECOND ORDER FOLDBACK CURRENT LIMITED REGULATOR



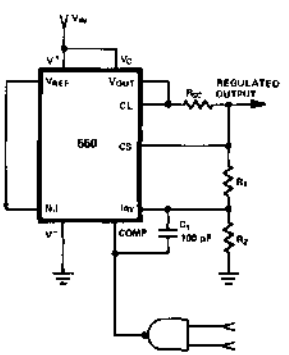
$$R_3 = \frac{V_{SENSE} \cdot I_{CL} \cdot R_4 (I_{FB} \cdot I_{SC})}{V_{OUT} \cdot I_{SC} \cdot V_{SENSE} (I_{FB} \cdot I_{SC})}$$

$$R_{SC} = \frac{(V_{OUT} \cdot I_{SC} \cdot V_{SENSE}) R_3 / R_4 \cdot V_{SENSE}}{I_{KNEE}}$$

$I_{CL} \cong 125\ \mu A$

FIGURE 5B

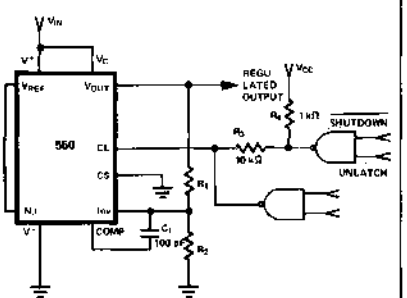
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



1/4 8T80, 1/6 8T90, 1/10 8T01B, etc.

FIGURE 6

REMOTE LATCHING SHUTDOWN REGULATOR

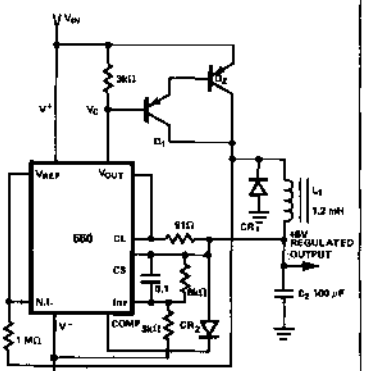


8415, 8417, 2/3 8471, 1/3 8891, 8T90, 1/2 8481, 8881, 8T90

NOTE 2

FIGURE 7

POSITIVE SWITCHING REGULATOR



L_1 is 50 turns of #22 wire wound on Ferroxcube. 42/29-377 A400

FIGURE 8

TYPICAL APPLICATIONS (Cont'd.)

POSITIVE FLOATING REGULATOR

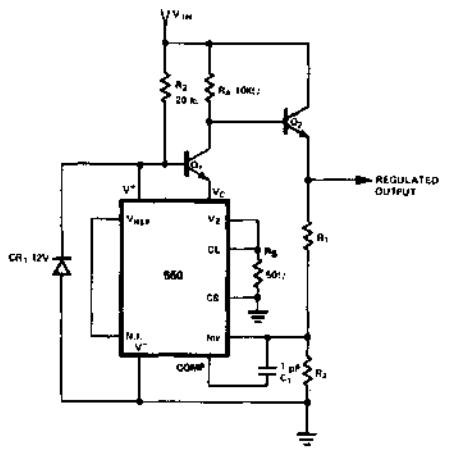


FIGURE 9

NEGATIVE FLOATING REGULATOR

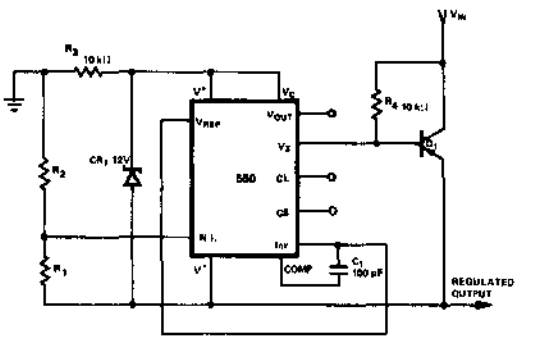
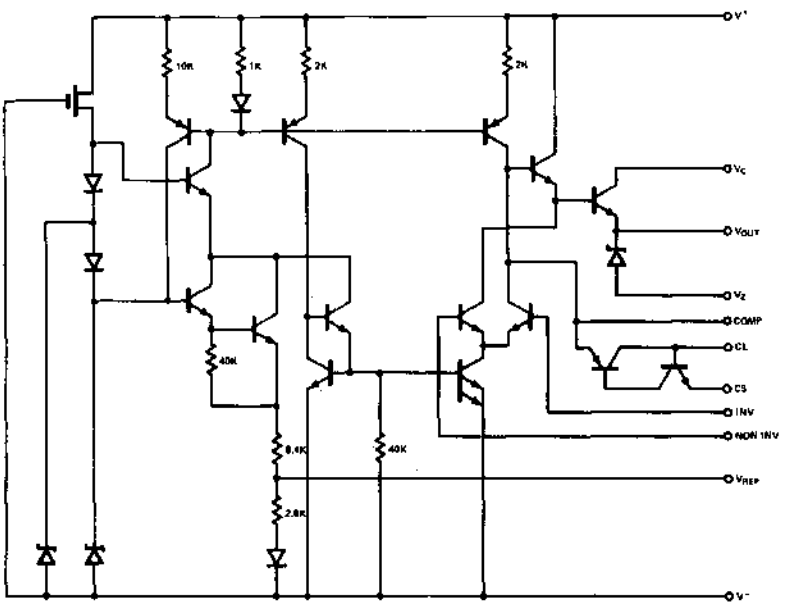


FIGURE 10

NOTES:

1. To utilize the SE550L in applications which require V_Z, an external 6.2 volt zener diode should be connected in series with V_{OUT}.
2. The "Shut-down" gate need only be pulsed to latch the regulator output to zero. R_4 may be omitted for active pull-up devices. The "Unlatch" gate must have an open collector.

EQUIVALENT CIRCUIT



DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

FEATURES

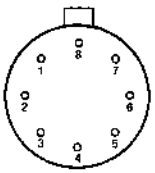
- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

PIN CONFIGURATIONS

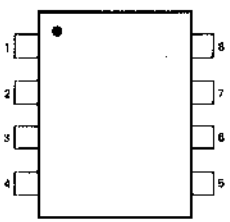
T PACKAGE
(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555T/NE555T

V PACKAGE
(Top View)



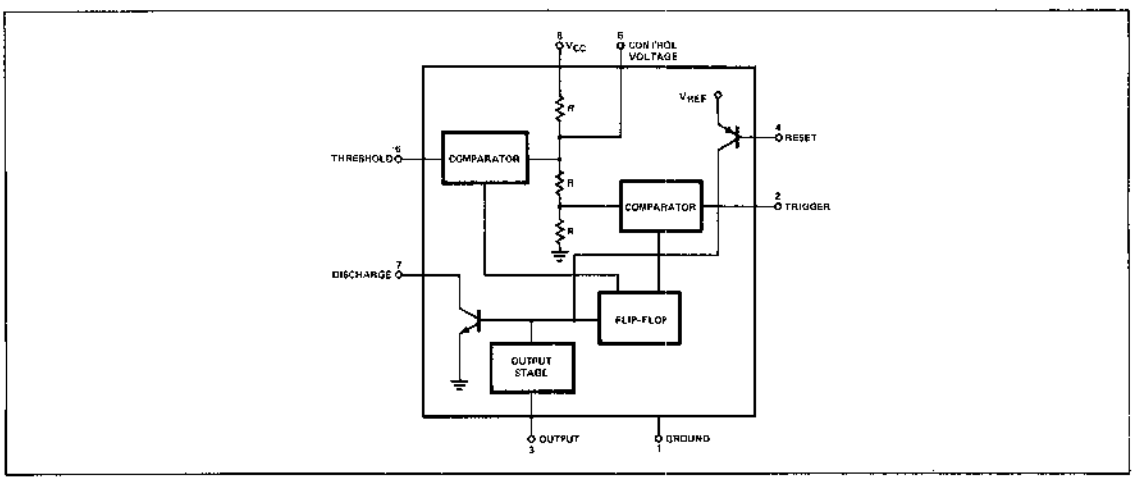
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555V/NE555V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

BLOCK DIAGRAM



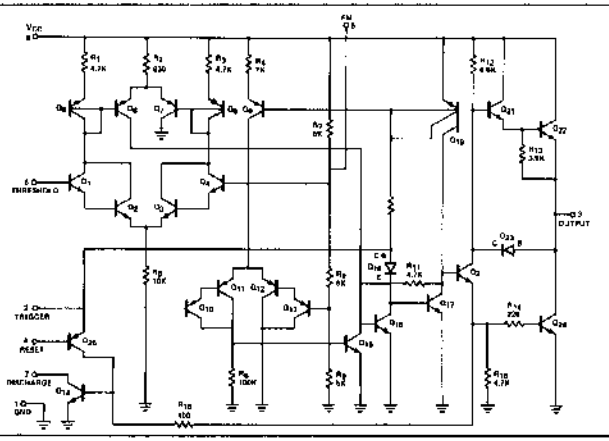
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 555			NE 555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
	Low State, Note 1							
Timing Error	R_A, R_B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1 μF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					.25	.35	
Output Voltage Drop (high)								
	I_{SOURCE} = 200mA V_{CC} = 15V		12.5			12.5		
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec

NOTES:

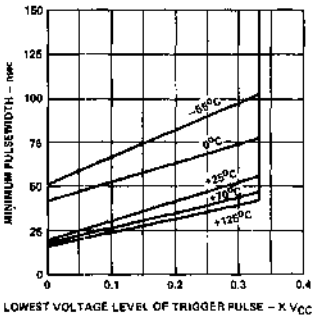
1. Supply Current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. This will determine the maximum value of R_A + R_B. For 15V operation, the max total R = 20 megohm.

EQUIVALENT CIRCUIT

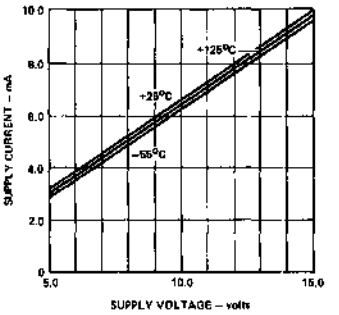


TYPICAL CHARACTERISTICS

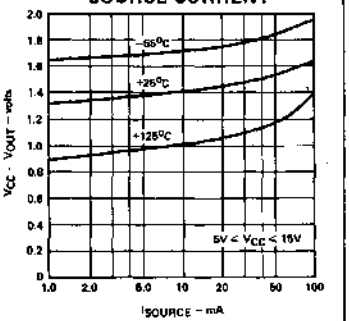
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



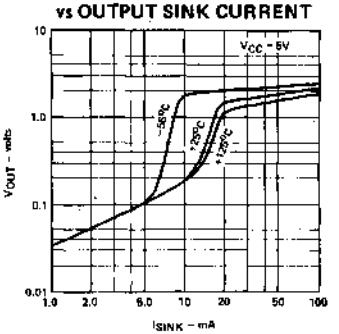
SUPPLY CURRENT vs SUPPLY VOLTAGE



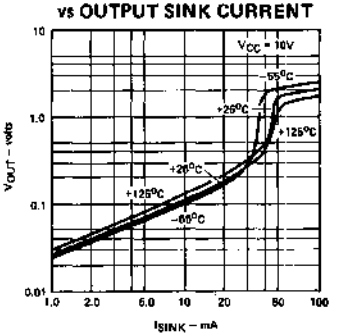
HIGH OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT



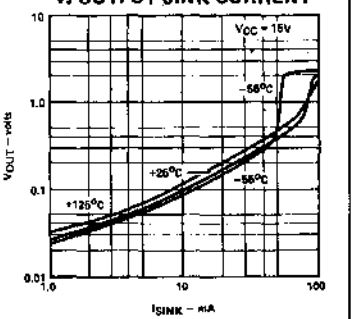
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



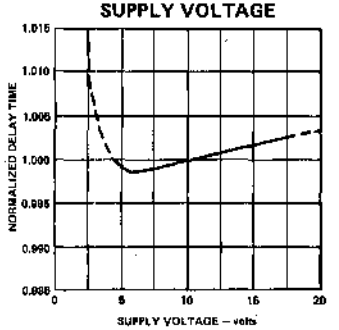
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



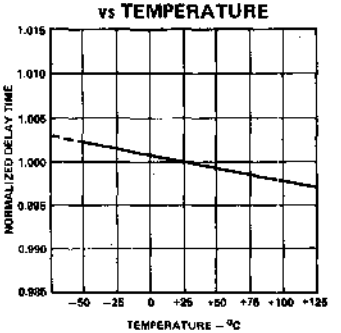
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



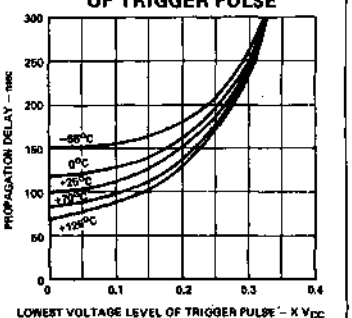
DELAY TIME vs SUPPLY VOLTAGE



DELAY TIME vs TEMPERATURE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



APPLICATIONS INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.

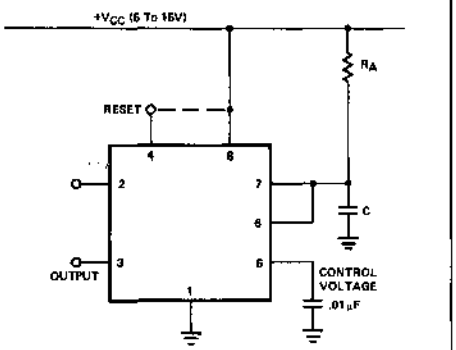


FIGURE 1a.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant $\tau = R_AC$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t = 1.1\ R_AC$ and can easily be determined by Figure 1c. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

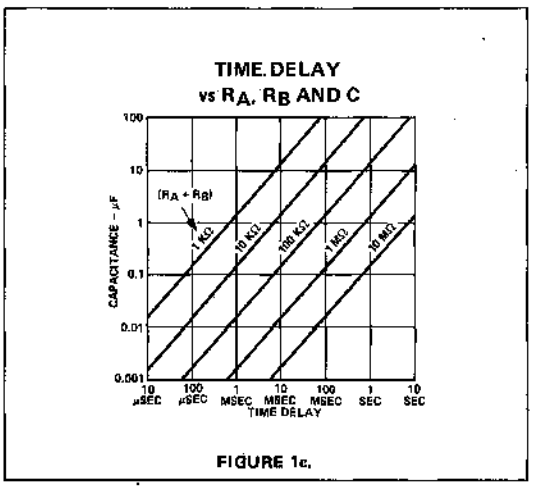
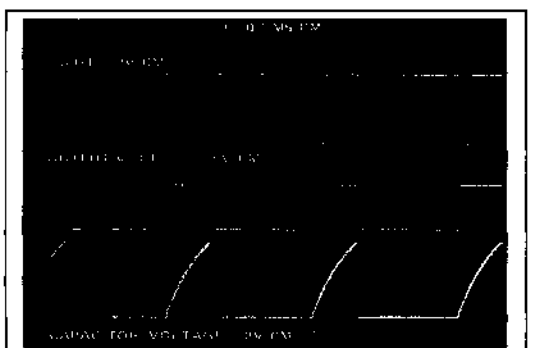


FIGURE 1c.



R_A = 9.1 KΩ, C = .01 µF, R_L = 1 KΩ

FIGURE 1b.

ASTABLE OPERATION

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

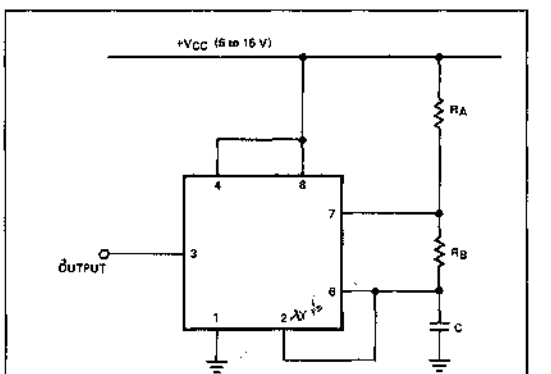
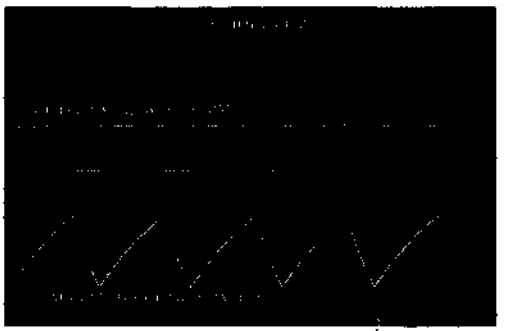


FIGURE 2a.

APPLICATIONS INFORMATION (Cont'd)

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.



R_A = 4 KΩ, R_B = 3 KΩ, R_L = 1 KΩ

FIGURE 2b.

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

and the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

and may be easily found by Figure 2c.

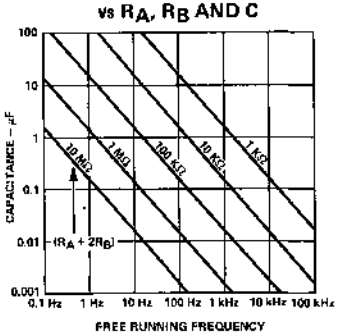


FIGURE 2c.

The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

MISSING PULSE DETECTOR

Using the circuit of Figure 3a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 3b shows the actual waveforms seen in this mode of operation.

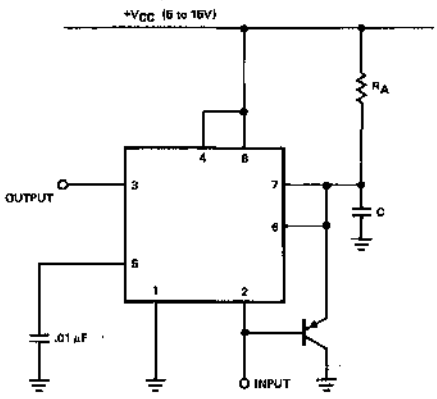
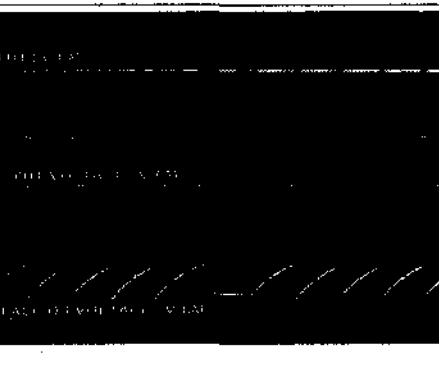


FIGURE 3a.



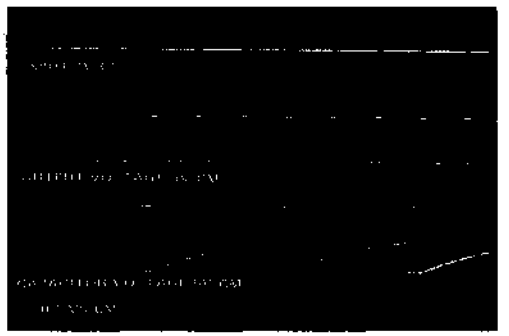
R_A = 1KΩ, C = .09 μF

FIGURE 3b.

APPLICATIONS INFORMATION (Cont'd)

FREQUENCY DIVIDER

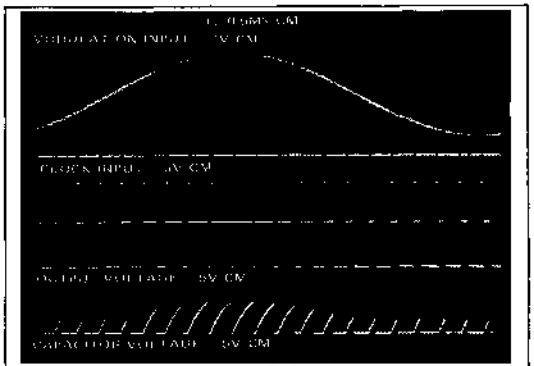
If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle. Figure 4 shows the waveforms of the timer in Figure 1a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.



R_A = 1250Ω, C = .02 μF, R_L = 1KΩ
FIGURE 4.

PULSE WIDTH MODULATION (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 5a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 5b shows the actual waveforms generated with this circuit.



R_A = 10KΩ, C = .02 μF
FIGURE 5b.

PULSE POSITION MODULATION (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 6a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 6b shows the waveforms generated for triangle wave modulation signal.

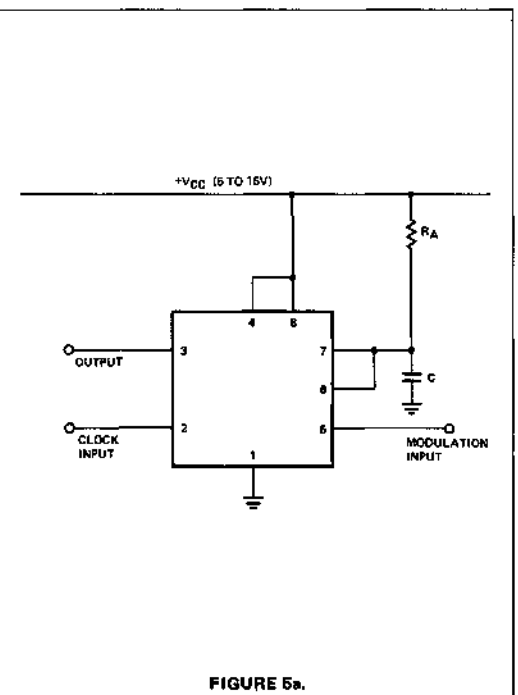


FIGURE 5a.

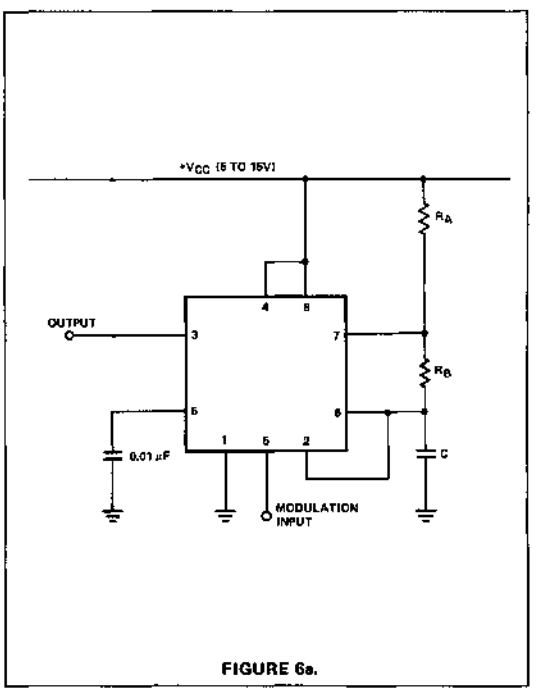
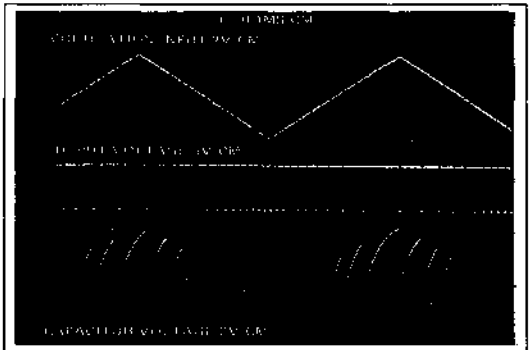


FIGURE 6a.

APPLICATIONS INFORMATION (Cont'd)

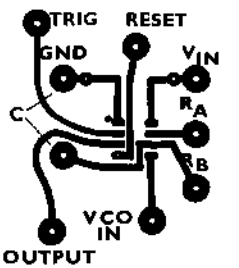


R_A = 3KΩ, R_B = 500Ω, C = .01 μF, R_L = 1KΩ
FIGURE 6b.

TEST SEQUENCER

Figure 7 shows several timers connected sequentially. The first timer is started by momentarily connecting pin 2 to ground, and runs for 10 msec. At the end of its timing cycle, it triggers the second circuit which runs for 50 msec. After this time, the third circuit is triggered. Note that the timing resistors and capacitors can be programmed digitally and that each circuit could easily trigger several other timers to start concurrent sequences.

555 TIMER



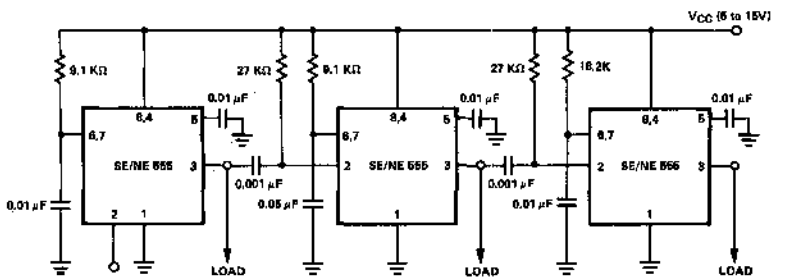


FIGURE 7.

DESCRIPTION

The NE560B Phase Locked Loop (PLL) is a monolithic signal conditioner, and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional Potentiometer. The low pass filter, which determines the capture characteristics of the loop, is formed by the two capacitors and two resistors at the Phase Comparator output.

The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output, in differential form, is available for signal conditioning frequency synchronization, multiplication and division applications. Terminals are provided for optional extended control of the tracking range, VCO frequency, and output DC level.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%.

- FM DEMODULATION WITHOUT TUNED CIRCUITS
- NARROW BANDPASS - TO ± 1% ADJUSTABLE
- TRACKING RANGE
- EXACT FREQUENCY DUPLICATION IN HIGH
- NOISE ENVIRONMENT
- WIDE TRACKING RANGE ±15%
- HIGH LINEARITY - 1% DISTORTION MAX
- FREQUENCY MULTIPLICATION AND DIVISION
- THROUGH HARMONIC LOCKING

APPLICATIONS

TONE DECODERS
FM IF STRIPS
TELEMETRY DECODERS
DATA SYNCHRONIZERS
SIGNAL RECONSTITUTION
SIGNAL GENERATORS
MODEMS
TRACKING FILTERS
SCA RECEIVERS
FSK RECEIVERS
WIDE BAND HIGH LINEARITY DETECTORS

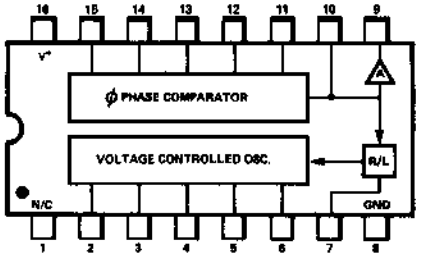
ABSOLUTE MAXIMUM RATINGS

Maximum Operating Voltage	26V
Input Voltage	1V Rms
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300 mw

Limiting values above which serviceability may be impaired

PIN CONFIGURATION

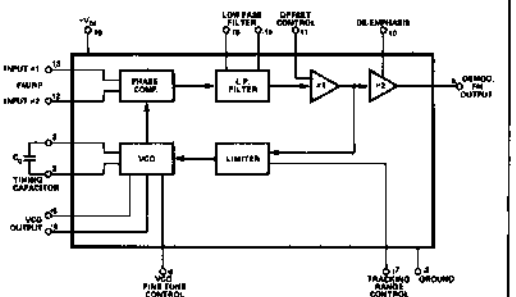
B PACKAGE
(Top View)



1. No Connection
2. VCO Timing Capacitor
3. VCO Timing Capacitor
4. VCO Output #2
5. VCO Output #1
6. Fine Tuning
7. Range Control
8. Ground (or Negative Power Supply)
9. Demodulated FM Output (an open emitter)
10. De-emphasis terminal (Audio bandshaping)
11. Offset Adjustment
12. FM/RF Input #1
13. FM/RF Input #2
14. Low Pass Loop Filter
15. Low Pass Loop Filter
16. Positive Power Supply

ORDER PART NO. NE560B

BLOCK DIAGRAM



GENERAL ELECTRICAL CHARACTERISTICS

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	7	9	11	Ma	
Minimum Input Signal for Lock		100		μV	
Dynamic Range		60		dB	
VCO Temp Coefficient*		±0.06	±0.12	%/°C	Measured at 2 MHz, with both inputs AC grounded
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		KΩ	
Input Capacitance		4		Pf	
Input DC Level		+4		V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		V_{p-p}	Measured at Pin 9
AM Rejection*	30	40		dB	See Figure 1
De-emphasis Resistance		8		KΩ	

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For FM Applications, Figure 2) (15KΩ Pin 9 to GND, Input Pin 12 or 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

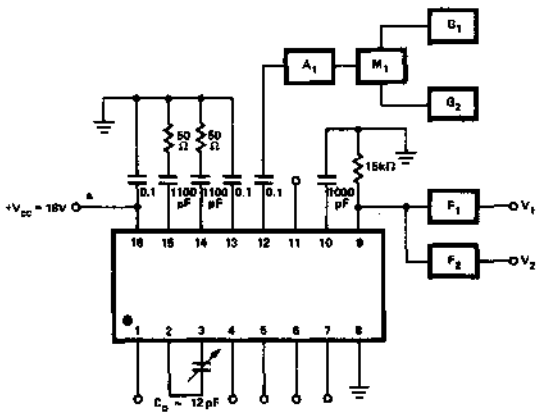
CHARACTERISTICS	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
10.7 MHz Operation **Deviation 75 kHz Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		.3	1	% T.H.D.	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
4.5 MHz Operation **Deviation = 25 kHz, Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.3	1.0	% T.H.D.	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Wide Deviation **$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz Modulation Rate**					
Detection Threshold		1	5	mV	
Demodulated Output	0.2	0.5		Vrms	V_{in} = 5 mv Rms
Distortion		0.8		% T.H.D.	V_{in} = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	V_{in} = 5 mv Rms

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For Tracking Filter, Figure 3) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
Tracking Range	±5	±15		% of f_o	V_{in} = 5 mv Rms
Minimum Signal to Sustain Lock 0°C to 70°C		0.8		mv Rms	Input 2 MHz - See Characteristic Curves
VCO Output Impedance		1		kΩ	
VCO Output Swing	0.4	0.6		V_{p-p}	Input 2 MHz Measured with high impedance Probe with less than 10 Pf Capacitance
VCO Output DC Level		+6.5		V	
Side Band Suppression		35		dB	Input 2 MHz with ±100 kHz Side Band Seperation and 3 kHz Low Pass Filter Input 1 mv Peak for Carrier Each Side Band C_1 = 0.01 μF R_1 = 0

AM REJECTION



G_1 = FM Generator with $f_C = f_O \approx 4$ MHz, $\Delta f = 40$ kHz, $f_{mod} = 1$ kHz

G_2 = Audio Generator with $f_A = 400$ Hz

M_1 = Balanced Modulator Carrier Supplied by G_1, AM modulation provided by G_2.

A_1 = 50 Ω attenuator pad with signal level into pin 12 adjusted to 1 mV rms.

F_1 = 1 kHz Bandpass filter, Q = 20

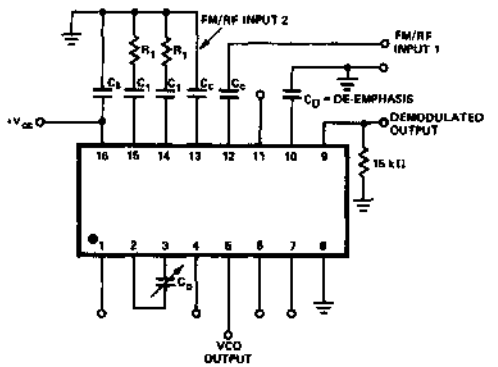
F_2 = 400 Hz Bandpass filter with Q = 50, with 1 kHz trap.

$$AMR = \frac{V_1}{V_2} \text{ in dB}$$

V_1 and V_2 are rms voltmeter readings.

Fig. 1

FM DEMODULATION

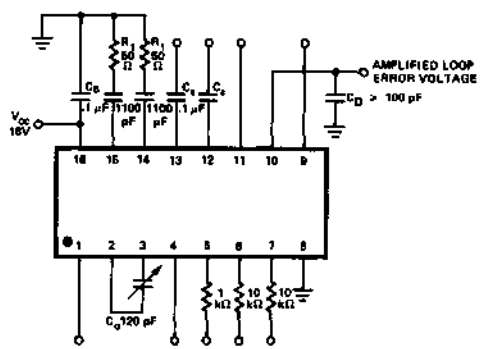


C_B = Bypass Capacitor
C_C = Coupling Capacitors
C_1 = Low Pass Filter Capacitors
C_o = Frequency Determining Capacitor

T_D = De-emphasis time constant
= (C_D) (8kΩ)

Fig. 2

TRACKING FILTER

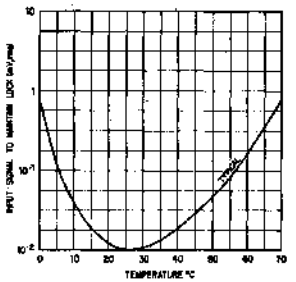


C_C = Coupling Capacitors
C_B = Bypass Capacitor
C_1 = Low Pass Filter Capacitor
C_o = VCO Frequency Set Capacitor

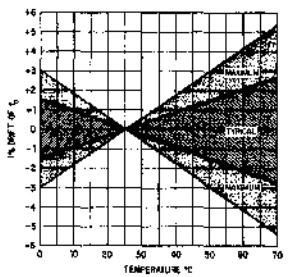
Fig. 3

TYPICAL CHARACTERISTIC CURVES

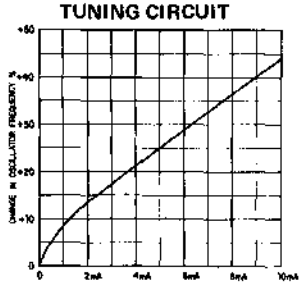
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{signal} = f_{o25°C} = 2.0$ MHz



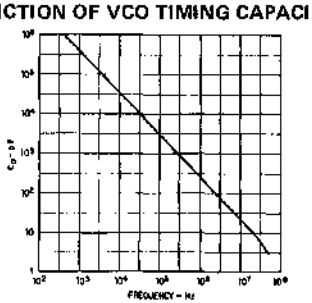
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (f_o)



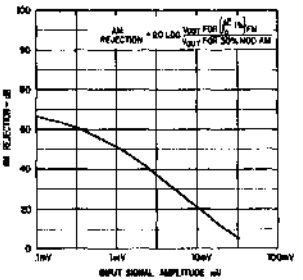
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CIRCUIT



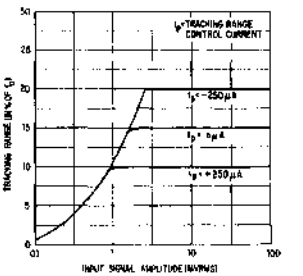
FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE



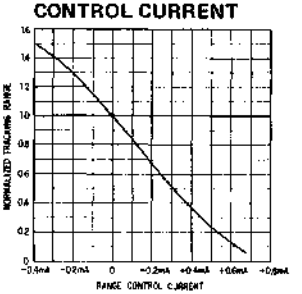
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL $f_o = 10$ MHz



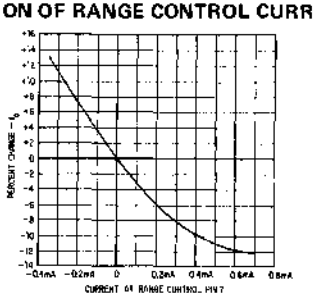
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT

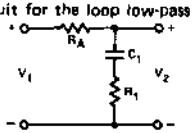


NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



INTERNAL CONTROLS

1. **Loop Low Pass Filter (Pins 14 and 15)**
The equivalent circuit for the loop low-pass filter can be represented as:



where RA (6K Ω) is the effective resistance seen looking into Pin #14 or Pin #15.
The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = (S) = \frac{1 + S R_1 C_1}{1 + S (R_1 + R_A) C_1}$$

where S is the complex frequency variable.

2. **Loop Gain (Threshold) Control**
The overall Phase Locked Loop gain can be reduced by connecting a feedback resistor, R_F, across the low-pass filter terminals, Pins #14 and, #15. This causes the loop gain and the detection sensitivity to decrease by a factor α (α<1)
where:

$$\alpha = \frac{R_F}{2 R_A + R_F}$$

Reduction of loop gain may be desirable at high input signal levels (V_{in} > 30 mV) and at high frequencies (f_o >5 MHz) where excessively high loop gain may cause instability.

3. **Tracking Range Control (Pin 7)**
Any bias current, I_p, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_p, are shown in the characteristic curves with I_p defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 Volts and presents an impedance of 600 Ω.

4. **External Fine Tuning (Pin 6)**
Any bias current injected into the fine tuning terminal increases the frequency of oscillation, f_o, as shown in the characteristic curves. This current is defined Positive into the fine tuning terminal. This terminal is at a typical DC level of +1.3 Volts and has a dynamic impedance of 100Ω to ground.

5. **Offset Adjustment (Pin 11)**
Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the DC level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

Nominally this terminal is at +4V DC and has an input impedance of 3K Ω. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. **De-emphasis Filter (Pin 10)**
The de-emphasis terminal is normally used when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier in the system block diagram (see Figure 2 .) is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2 R_B C_D}$$

where R_D is the 8000 ohm resistance seen looking into the de-emphasis terminal.
When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, de-emphasis terminal should be AC grounded.

DESCRIPTION

The NE561B Phase Locked Loop (PLL) is a monolithic signal conditioner, and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional Potentiometer. The low pass filter, which determines the capture characteristics of the loop is formed by the two capacitors and two resistors at the Phase Comparator output.

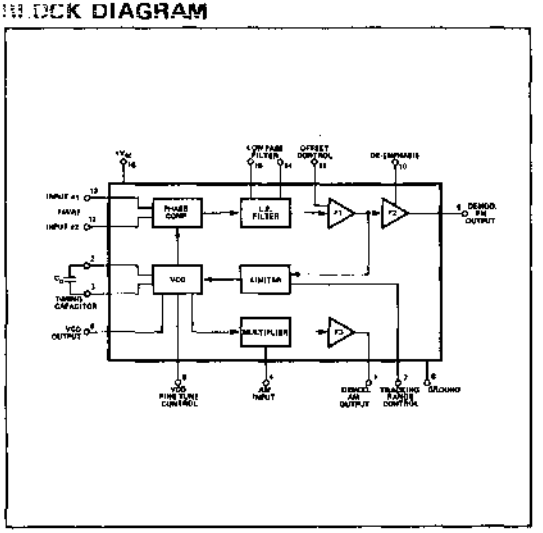
The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output is available for signal conditioning, frequency synchronization, multiplication and division applications. Terminals are provided for optional external control of the tracking range, VCO frequency, and output DC level. An analog multiplier block is incorporated into the PLL system to provide frequency selective synchronous AM detection capability.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%.

FEATURES

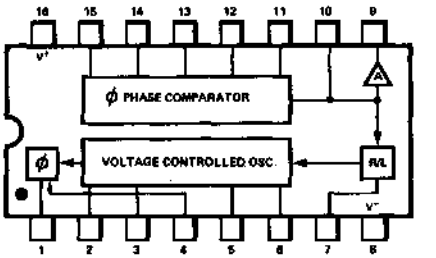
- **FM DEMODULATION WITHOUT TUNED CIRCUITS**
- **SYNCHRONOUS AM DETECTION**
- **NARROW BAND PASS TO ± 1%**
- **EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT**
- **ADJUSTABLE TRACKING RANGE**
- **WIDE TRACKING RANGE ±15%**
- **HIGH LINEARITY - 1% DISTORTION MAX**
- **FREQUENCY MULTIPLICATION AND DIVISION THROUGH HARMONIC LOCKING**

BLOCK DIAGRAM



PIN CONFIGURATION

B PACKAGE



1. Demodulated Am Output
2. VCO Timing Capacitor
3. VCO Timing Capacitor
4. AM Input
5. VCO Output
6. Fine Tuning
7. Range Control
8. Ground (V⁻)
9. Demodulated FM Output (an open emitter)
10. De-emphasis terminal (audio band shaping)
11. Offset Adjustment
12. FM/RF Input #1
13. FM/RF Input #2
14. Low Pass Loop Filter
15. Low Pass Loop Filter
16. V⁺

ORDER PART NO. NE561B

ABSOLUTE MAXIMUM RATINGS

Maximum Operating Voltage	26V
Input Voltage	1V RMS
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

Limiting values above which serviceability may be impaired

APPLICATIONS

TONE DECODERS
AM-FM-IF STRIPS
TELEMETRY DECODERS
DATA SYNCHRONIZERS
SIGNAL RECONSTITUTION
SIGNAL GENERATORS
MODEMS
TRACKING FILTERS
SCA RECEIVERS
FSK RECEIVERS
WIDE BAND HIGH LINEARITY DETECTORS
SYNCHRONOUS DETECTORS
AM RECEIVER

GENERAL ELECTRICAL CHARACTERISTICS

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	8	10	12	Ma	
Minimum Input Signal for Lock		100		μV	
Dynamic Range		60		dB	
VCO Temp Coefficient*		±0.06	±0.12	%/°C	Measured at 2 MHz, with both inputs AC grounded
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level		+4		V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		V_{p-p}	Measured at Pin 9
AM Rejection*	30	40		dB	See Figure 3
De-emphasis Resistance		8		kΩ	

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For FM Applications, Figure 2) (15KΩ Pin 9 to GND, Input Pin 12 or 13, AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
10.7 MHz Operation — **Deviation 75 kHz Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	Vin = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		.3	1	% T.H.D.	Vin = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	Vin = 1 mv Rms Modulation Frequency 1 kHz
4.5 MHz Operation — **Deviation = 25 kHz, Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	Vin = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.3	1.0	% T.H.D.	Vin = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	Vin = 1 mv Rms Modulation Frequency 1 kHz
Wide Deviation — **$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz modulation rate**					
Detection Threshold		1	5	mV	
Demodulated Output	0.2	0.5		Vrms	Vin = 5 mv Rms
Distortion		0.8		% T.H.D.	Vin = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	Vin = 5 mv Rms

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For Tracking Filter, Figure 1) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

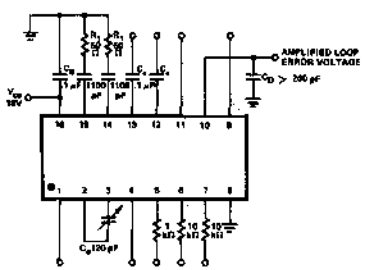
CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Tracking Range	±5	±20		% of f_o	Vin 5 mv Rms
Minimum Signal to Sustain Lock 0°C to 70°C		0.8		mv Rms	Input 2 MHz - See Characteristic Curves
VCO Output Impedance		1		kΩ	
VCO Output Swing	0.4	0.6		V_{p-p}	Input 2 MHz Measured with high impedance. Probe with less than 10 pF capacitance.
VCO Output DC Level		+6.5		V	
Side Band Suppression		35		dB	Input 2 MHz with ±100 kHz Sideband Separation and 3 kHz Low Pass Filter. Input 1 mv Peak for Carrier and each Sideband C_1 = 0.01 μF R_1 = 0

ELECTRICAL CHARACTERISTICS (For AM Synchronous Detector, Figure 4) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Input Impedance		3		kΩ	
Output Impedance		8		kΩ	
Output DC Level	+10	+14	+17	V	
AM Conversion Gain	3	12		dB	See Definition of Terms
Out of Band Rejection		30		dB	See Definition of Terms
Distortion		1•		% T.H.D.	

TYPICAL TEST CIRCUITS

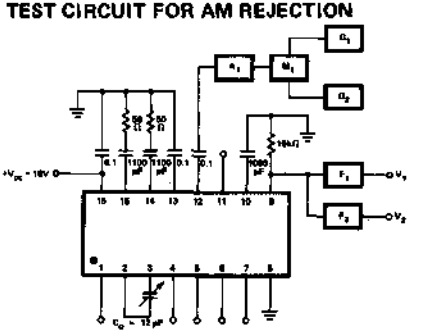
TEST CIRCUIT FOR TRACKING FILTER



C_C = Coupling Capacitors
C_B = Bypass Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = VCO Frequency Set Capacitor

FIGURE 1

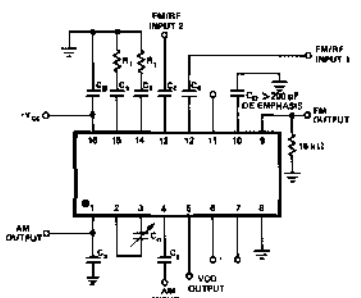
TEST CIRCUIT FOR AM REJECTION



G_1 = FM Generator with f_c = fo ≈ 4 MHz, Δf = 40 kHz, f_{mod} = 1 kHz
G_2 = Audio Generator with f_A = 400 Hz
M_1 = Balanced Modulator Carrier Supplied by G_1, AM modulation provided by G_2
A_1 = 50Ω attenuator pad with signal level into pin 12 adjusted to 1 mV rms.
F_1 = 1 kHz Bandpass filter, Q = 20
F_2 = 400 Hz Bandpass filter with Q = 50, with 1 kHz trap.
AMR = $\frac{V_1}{V_2}$ in dB V_1 and V_2 are rms voltmeter readings.

FIGURE 3

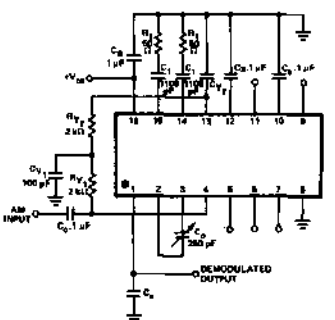
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitors
C_1 = Low Pass Filter Capacitors
C_0 = Frequency Determining Capacitors
C_x = AM Post Detection Filter

FIGURE 2

TEST CIRCUIT FOR AM SYNCHRONOUS DETECTOR

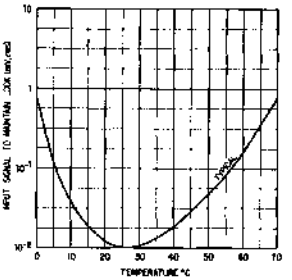


C_B = Bypass Capacitor
C_C = Coupling Capacitor
$RV_1CV_1 = RV_2CV_2 = \frac{1}{2\pi fo}$
C_x = AM Post Detection Filter

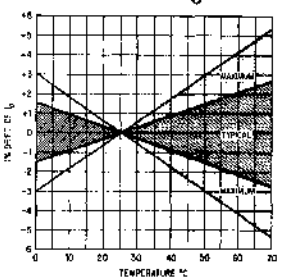
FIGURE 4

TYPICAL CHARACTERISTIC CURVES

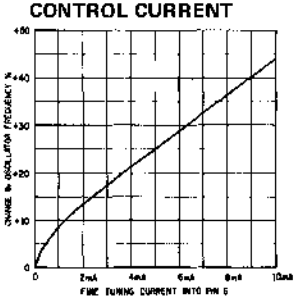
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{signal} = f_{o_{25^oC}} = 2.0$ MHz



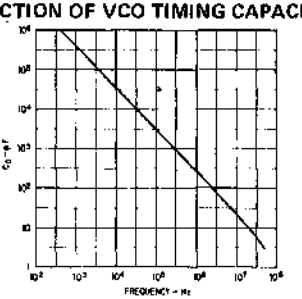
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (f_o)



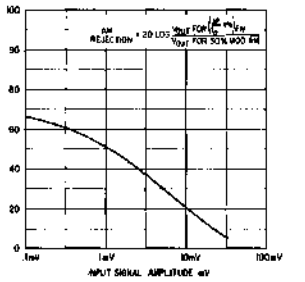
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



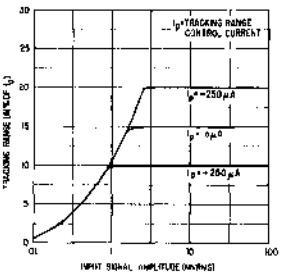
FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE



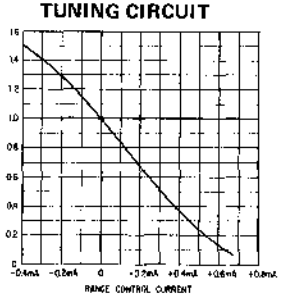
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL $f_o = 10$ MHz



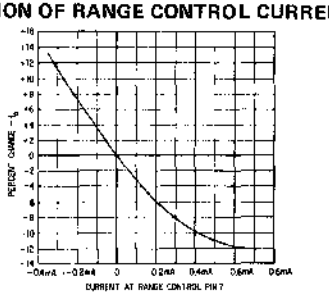
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CIRCUIT



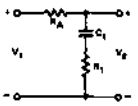
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

1. **Loop Low Pass Filter (Pins 14 and 15)**

The equivalent circuit for the loop low-pass filter can be represented as:



where RA (6kΩ) is the effective resistance seen looking into Pin #14 or Pin #15.

The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = F(S) = \frac{1 + S R_1 C_1}{1 + S (R_1 + R_A) C_1}$$

where S is the complex frequency variable.

2. **Loop Gain (Threshold) Control**

The overall Phase Lock of loop gain can be reduced by connecting a feedback resistor, R_F, across the low-pass filter terminals, Pins #14 and #15. This causes the loop gain and the detection sensitivity to decrease by a factor ($\alpha < 1$), where

$$\alpha = \frac{R_F}{2R_A + R_F}$$

Reduction of loop gain may be desirable at high input signal levels (V_{in} >30 mV) and at high frequencies (f_o > 5MHz) where excessively high PLL loop gain may cause instability within the loop.

3. **Tracking Range Control (Pin 7)**

Any bias current, I_p, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_p, are shown in the characteristic curves with I_p defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 Volts and presents an impedance of 600Ω.

4. **External Fine Tuning (Pin 6)**

Any bias current injected into the fine tuning terminal increases the frequency of oscillation, f_o, as shown in the characteristic curves. This current is defined Positive into the fine tuning terminal. This terminal is at a typical DC level of +1.3 Volts and has a dynamic impedance of 100Ω to ground.

5. **Offset Adjustment (Pin 11)**

Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the DC level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

Nominally this terminal is at +4V DC and has an input impedance of 3kΩ. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. **De-emphasis Filter (Pin 10)**

The de-emphasis terminal is normally used when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier in the system block diagram (see Figure 2 .) is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where R_D is the 8000 ohm resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, de-emphasis terminal should be AC grounded.

7. **AM Post-Detection Filter (Pin 1)**

The capacitor C_x connected between Pin #1 and ground serves as a low-pass filter for synchronous AM detection with a transfer characteristic, $F_2(S)$, given as:

$$F_2(S) = \frac{1}{1 + SR_x C_x}$$

where R_x = 8kΩ is the resistance seen looking into Pin #1.

DESCRIPTION

The NE562B Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system, comprising a VCO, phase comparator, amplifier and low pass filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by two capacitors and two resistors at the phase comparator output.

This PLL has two sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signal conditioning and synchronization, frequency multiplication and division applications. Terminals are also provided for the optional extension of the tracking range.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%

FEATURES

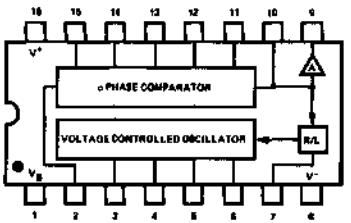
- FREQUENCY MULTIPLICATION AND DIVISION
- SIGNAL CONDITIONING AND SIDE-BAND SUPPRESSION
- FM DEMODULATION WITHOUT TUNED CIRCUITS
- NARROW BANDPASS – TO ±1%
- ADJUSTABLE TRACKING RANGE – TO ±15%
- EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT
- HIGH LINEARITY – 1% DISTORTION MAXIMUM AT 1% DEVIATION

APPLICATIONS

FREQUENCY SYNTHESIZERS
DATA SYNCHRONIZERS
SIGNAL CONDITIONING
TRACKING FILTERS
TELEMETRY DECODERS
MODEMS
FM IF STRIPS AND DEMODULATORS
TONE DECODERS
FSK RECEIVERS
WIDEBAND HIGH LINEARITY FM DEMODULATORS

PIN CONFIGURATION

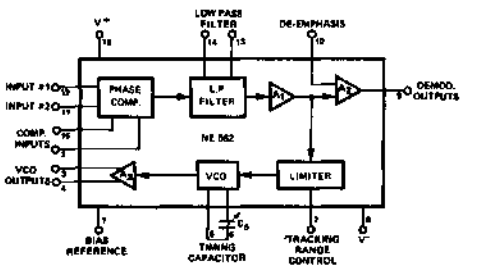
B PACKAGE
(Top View)



1. Bias Reference Voltage
2. Phase Comparator Input #1
3. VCO Output #1
4. VCO Output #2.
5. VCO Timing Capacitor
6. VCO Timing Capacitor
7. Range Control
8. Negative Power Supply (Ground)
9. Demodulated FM Output (an open emitter)
10. De-emphasis (Audio Bandshaping)
11. RF Input #1
12. RF Input #2
13. Low-Pass Loop Filter
14. Low-Pass Loop Filter
15. Phase Comparator Input #2
16. Positive Power Supply

ORDER PART NO. NE562B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

Maximum Operating Voltage	30V
Input Voltage	3V rms
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

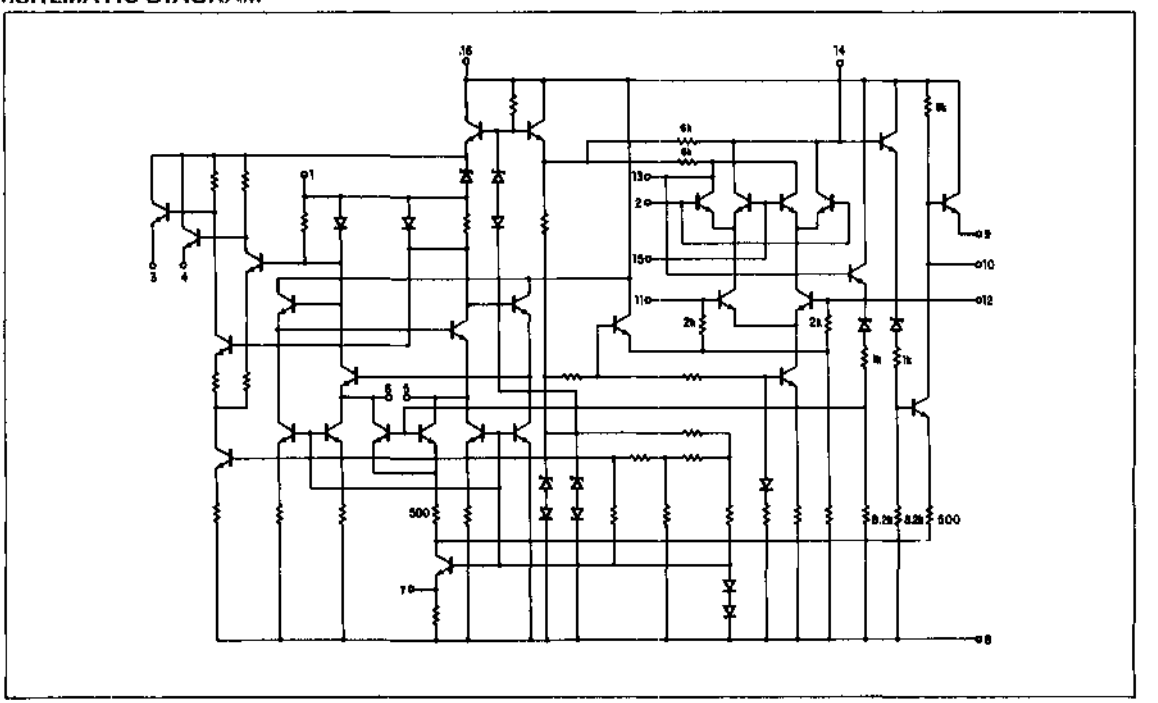
GENERAL ELECTRICAL CHARACTERISTICS

(15,000 ohms pin 9 to ground, 12,000 ohms pins 3 and 4 to ground, pins 2 and 15 to pin 1 through 1000 ohms, input to pin 11 or 12 with unused input at AC ground, range control not connected and V^+ = 18 volts unless otherwise specified. T_A = 25°C.)

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	MIN	TYP	MAX		
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	10	12	14	mA	
Minimum Input Signal for Lock		200		μV	
Dynamic Range		80		dB	
VCO Temp Coefficient*		±0.06	±0.15	%/°C	Measured at 2 MHz
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level	+12	+14	+16	V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		$V_{p\text{-}p}$	Measured at Pin 9
AM Rejection*	30	40		dB	See Definition of Terms
De-emphasis Resistance		8		kΩ	
Bias Reference		+8		V	

*ACC Test Sub Group C.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS FOR FM APPLICATIONS (15,000 ohms pin 9 to ground, input to pin 11 or pin 12, AC ground unused input, range control not connected and V^+ = 18 volts. T_A = =25°C.)

CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
10.7 MHz Operation	**Deviation 75 kHz Source Impedance = 50Ω**				
Detection Threshold		200	500	μV	
Demodulated Output Amplitude	30	70		mV rms	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Distortion*		0.5		% T.H.D.	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB*	V_{in} = 1 mV rms Modulation Frequency 1 kHz
4.5 MHz Operation	**Deviation = 25 kHz, Source Impedance = 50Ω**				
Detection Threshold		200	500	μV	
Demodulated Output Amplitude	30	60		mV rms	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Distortion		0.5		% T.H.D.	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Wide Deviation	**$\Delta F/f_0$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz Modulation Rate**				
Detection Threshold		1	5	mV	
Demodulated Output		1		V rms	V_{in} = 5 mV rms
Distortion	0.3	0.8		% T.H.D.	V_{in} = 5 mV rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	V_{in} = 5 mV rms

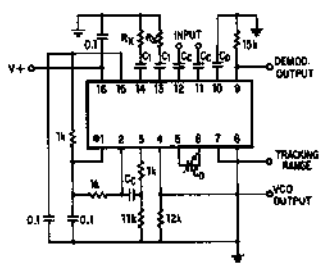
*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS (Input to pin 11 or pin 12, AC ground unused input, range control not connected, V^+ = 18 volts. T_A = 25°C.)

CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Tracking Range	±5	±15		% of f_0	200 mV p-p square wave input
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level		4		V	
VCO Output Impedance		1.3	2.5	kΩ	
VCO Output Swing	3	4.5		V p-p	
VCO Output DC Level		12		V	
VCO Signal/Noise Ratio		60		dB	Inputs at AC ground

TEST CIRCUIT

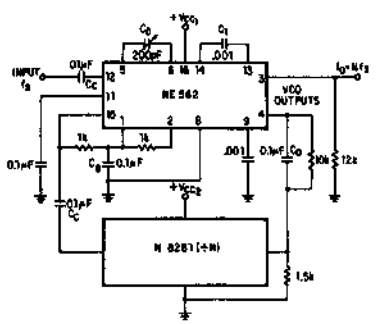
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_D = .01μF for Standard FM Broadcasting
C_1 and R_X = Low Pass Filter
C_0 = Frequency set Capacitor

FIGURE 1

TEST CIRCUIT FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS

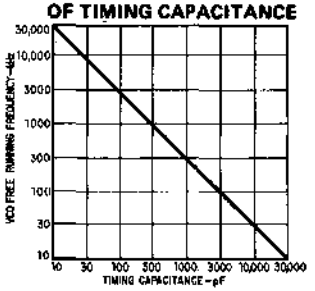


C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = Frequency Capacitor Set
Note: Fanout to divide by N counter is one.

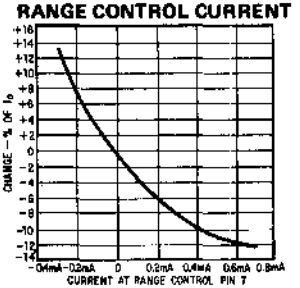
FIGURE 2

TYPICAL CHARACTERISTIC CURVES

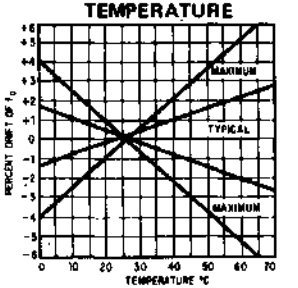
FREE RUNNING VOLTAGE CONTROLLED OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING CAPACITANCE



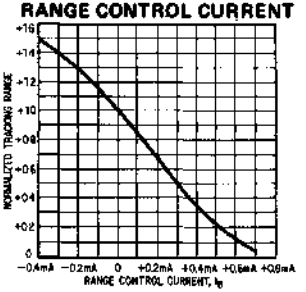
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



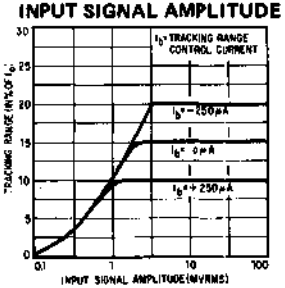
THERMAL DRIFT OF FREE RUNNING FREQUENCY AS A FUNCTION OF TEMPERATURE



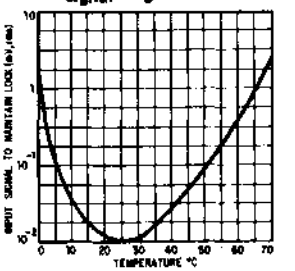
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



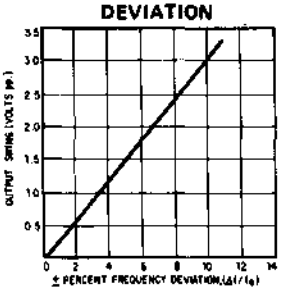
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



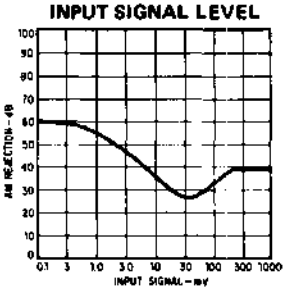
INPUT SIGNAL AMPLITUDE TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE ($f_{signal} = f_o = 2.0$ MHz)



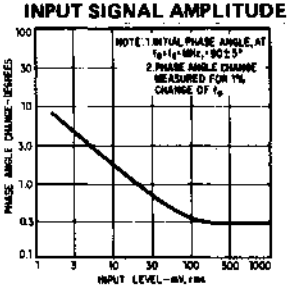
562 PHASE LOCKED LOOP DEMODULATED OUTPUT SWING AS A FUNCTION OF % FM DEVIATION



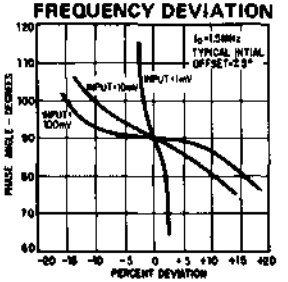
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL



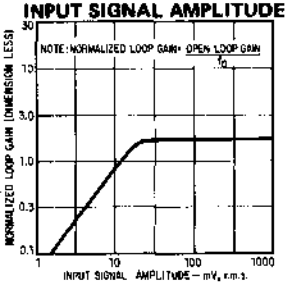
CHANGE IN PHASE ANGLE, f_o RELATIVE TO f_s, AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



VCO OUTPUT PHASE AS A FUNCTION OF PERCENT FREQUENCY DEVIATION



NORMALIZED LOOP GAIN AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



APPLICATIONS INFORMATION

1. BIAS REFERENCE

Pin 1 of the 562 is an internally regulated bias reference voltage supply which should be used as a source of bias current for the phase comparator input terminals, Pins 2 and 15. Biasing may be achieved as shown in Figure 3.

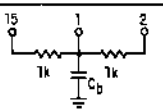


FIGURE 3

2. PHASE COMPARATOR LOOP INPUTS

Of the Signetics high frequency phase locked loops, the 562 is unique in that the loop is open between the VCO and the phase comparator. Once biasing of the comparator is accomplished, as described in Bias Reference above, loop closure can be accomplished by capacitive coupling between either one or both inputs of the phase comparator and the VCO output. A divider or counter may be enclosed in the loop at this point for frequency synthesis applications or a flip-flop may be used to ensure that the output waveform has a 50% duty cycle. If large signal swings, greater than 2 volts, are to be applied to the phase comparator inputs, a 1000 ohm current limiting buffer resistor should be used in series with the coupling capacitors.

3. VCO OUTPUT

Square wave VCO outputs of both polarities (0°C and 180°C) buffered by an amplifier are available at pins 3 and 4. For proper operation of the buffer amplifier, pins 3 and 4 must be returned to ground (or the negative supply) through resistors, typically 12,000 ohms. The value of these resistors may be reduced provided that total power dissipated in the 562 does not exceed 300 milliwatts or the total average current in each emitter does not exceed 4 mA. The output amplitude is typically 4.5 volts peak referenced at +12 volts with respect to pin 8.

4. VCO TUNING

Setting the free-running frequency of the VCO is accomplished easily with one timing capacitor connected between pins 5 and 6. For the 562 Phase Locked Loop, fine tuning of the free-running frequency may be accomplished in either or both of two ways. The first method uses a trimmer capacitor connected in parallel with the VCO timing capacitor. This is the simplest technique and requires the smallest number of extra components but at the lower frequencies may be difficult to implement. The second technique incorporates two resistors and a voltage source. The resistors are connected between each of the timing capacitor terminals and a voltage source as shown in Figure 4.

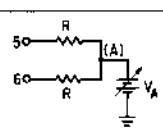


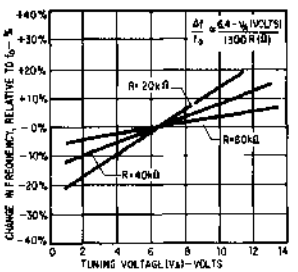
FIGURE 4

The percent change in the VCO free-running frequency, f_o, as a function of the voltage applied to point (A) is shown in the curves of Figure 5. Note that with this fine tuning technique, it is possible to *increase* the VCO free-running frequency to a value greater than possible with just a trimmer capacitor alone. A formula for the approximation of the VCO frequency as a function of the voltage at point (A), the resistance values and the starting frequency, is given below:

$$f = f_o\left[1 - \frac{V_A - 6.4}{1300R}\right]$$

The recommended resistance range of R is 20,000 to 60,000 ohms.

CHANGE IN VCO FREQUENCY AS A FUNCTION OF FINE TUNING VOLTAGE



5. LOOP GAIN CHARACTERISTICS

The overall open loop gain of the 562 PLL can be expressed as:

$$K_0 = K_1K_2$$

where:

K_0 = total open loop gain

K_1 = phase comparator and amplifier conversion gain

K_2 = VCO conversion gain

The VCO conversion gain, K_2, is the change of VCO frequency per unit of error voltage. In this particular design, it is numerically equal to the VCO frequency, i.e.,

$$K_2 = f_o \text{ Hz/Volt}$$

or

$$K_2 = 2\pi f_o \text{ radians/Volt-second}$$

The phase comparator and amplifier conversion gain, K_1, is proportional to input signal amplitude for low input levels, $V_s \leq 40$mV rms, and it is constant and equal to about 1.5 volts/radian for higher input amplitudes. Therefore, K_1 can be approximated as:

$$K_1 \cong \frac{.04\ V_s}{\sqrt{1 + \left(\frac{V_s}{40}\right)^2}}$$

where

V_s = input signal in mV rms.

APPLICATIONS INFORMATION (Cont'd.)

6. SIGNAL INPUT

The input structure is basically differential and may be used in this manner. Biasing is supplied to the input terminals from an internal regulated supply so signal inputs must be capacitively coupled. In most applications where the input is single-ended, the unused input should be bypassed to ground.

7. DEMODULATED OUTPUT

Pin 9 is a low impedance output terminal for the loop error voltage. It is at this point that the demodulated FM output is obtained. When used, it must be biased by a resistor to ground (or negative supply), and the resistor value may be adjusted downward provided that the output current does not exceed 5mA or the dissipation in the 562 does not exceed the absolute maximum ratings. When not used, pin 9 may be left open.

8. DE-EMPHASIS FILTER

The de-emphasis terminal, pin 10, is normally required when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications it may be used to shape the output response. The 3 dB bandwidth of the output amplifier is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where R_D is 8000 ohms.

When the PLL system is utilized for applications not requiring the use of the output amplifier, pin 10 should be by-passed to ground.

9. TRACKING RANGE CONTROL (Pin 7)

Any bias current, I_p, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_p, are shown in the characteristic curves with I_p defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 volts and presents an impedance of 600Ω.

10. LOW-PASS FILTER

In most applications, a loop low-pass filter should be connected between pins 13 and 14 and ground. It is used to set the loop response time, controlling the capture range and the rejection of out of band information. Four filter configurations and their transfer functions are shown in Figures 6 through 9. For VCO operating frequencies below 5 MHz, configurations shown in Figures 6 and 7 may be used. At higher frequencies, configurations shown in Figures 8 and 9 should be used to ensure loop stability. R is the impedance seen looking into the low pass filter terminals, Pins 13 and 14; and, in the 562, is nominally 6000 ohms.

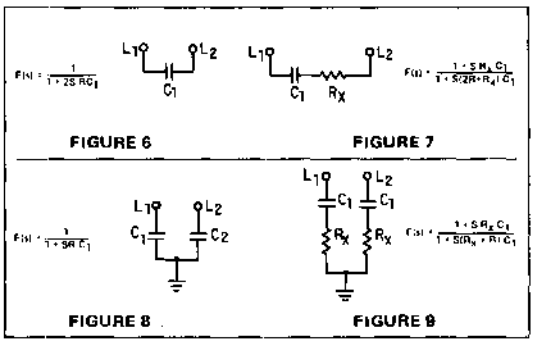


FIGURE 6 FIGURE 7

FIGURE 8 FIGURE 9

11. LOOP GAIN (Threshold) CONTROL

The overall Phase Locked Loop gain can be reduced by connecting a resistor, R_F, across the low-pass filter terminals, pins 13 and 14. This causes the loop gain and the detection sensitivity to decrease by a factor α, where:

$$\alpha = \frac{R_F}{12{,}000 + R_F}$$

Reduction of loop gain may be desirable at operating frequencies greater than 5 MHz because, at these frequencies, high loop gain may cause instability.

12. STATIC LOOP PHASE-ERROR

When the PLL is in lock, the VCO outputs have a nominal ±90°C phase shift with respect to the input signal. Due to internal offsets, this nominal angle at perfect lock condition may shift a few degrees, typically ±5°C or less.

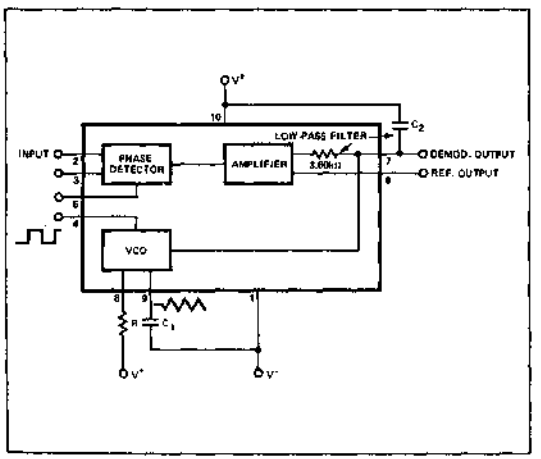
DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500 kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

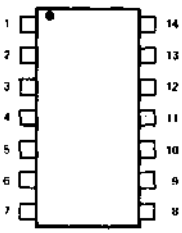
- **EXTREME STABILITY OF CENTER FREQUENCY (200ppm/°C typ)**
- **WIDE RANGE OF OPERATING VOLTAGE (±5 to ±12 VOLTS) WITH VERY SMALL FREQUENCY DRIFT (100ppm/% typ)**
- **VERY HIGH LINEARITY OF DEMODULATED OUTPUT (0.2% typ)**
- **CENTER FREQUENCY PROGRAMMING BY MEANS OF A RESISTOR, CAPACITOR, VOLTAGE OR CURRENT**
- **TTL AND DTL COMPATIBLE SQUARE-WAVE OUTPUT; LOOP CAN BE OPENED TO INSERT DIGITAL FREQUENCY DIVIDER**
- **HIGHLY LINEAR TRIANGLE WAVE OUTPUT**
- **REFERENCE OUTPUT FOR CONNECTION OF COMPARATOR IN FREQUENCY DISCRIMINATOR**
- **BANDPASS, ADJUSTABLE FROM <±1% to >±60%**
- **FREQUENCY ADJUSTABLE OVER 10 TO 1 RANGE WITH SAME CAPACITOR**

BLOCK DIAGRAM



PIN CONFIGURATIONS

A PACKAGE
(Top View)



1. V^-
2. Input
3. Input
4. VCO Output
5. Phase Comparator VCO Input
6. Reference Output
7. Demodulated Output
8. External R for VCO
9. External C for VCO
10. V^+
11. NC
12. NC
13. NC
14. NC

ORDER PART NOS. SE565A/NE565A

K PACKAGE

1. V^-
2. Input
3. Input
4. VCO Output
5. Phase Comparator VCO Input
6. Reference Output
7. Demodulated Output
8. External R for VCO
9. External C for VCO
10. V^+

ORDER PART NOS. SE565K/NE565K

APPLICATIONS

FREQUENCY SHIFT KEYING
MODEMS
TELEMETRY RECEIVERS
TONE DECODERS
SCA RECEIVERS
WIDEBAND FM DISCRIMINATORS
DATA SYNCHRONIZERS
TRACKING FILTERS
SIGNAL RESTORATION
FREQUENCY MULTIPLICATION & DIVISION

ABSOLUTE MAXIMUM RATINGS (limiting values above which serviceability may be impaired)

Maximum Operating Voltage	26V
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±6 Volts unless otherwise noted)

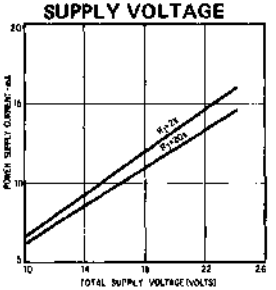
PARAMETER	TEST CONDITIONS	SE565			NE565			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY REQUIREMENTS								
Supply Voltage		±5		±12	±5		±12	V
Supply Current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input Impedance	$-4V \leqslant V_2, V_3 \leqslant +1V$	7	10		5	10		kΩ
Input Level Required for Tracking	f_0 = 50 kHz, ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center Frequency								
Maximum Value	C_1 = 2.7 pF	300	500			500		kHz
Distribution	Distribution taken about $f_0 \simeq 50$ kHz, R_1 = 5.0k, C_1 = 1200 pF	-10	0	+10	-30	0	+30	%
Drift with Temperature	f_0 = 50 kHz	+75	+100	+525		+200		ppm/°C
Drift with Supply Voltage	f_0 = 50 kHz, V_{CC} = ±6 to ±7 Volts		0.1	1.0		0.2	1.5	%/V
Triangle Wave								
Output Voltage Level			0			0		V
Amplitude		2	2.4	3	2	2.4	3	Vp-p
Linearity			0.2			0.5		%
Square Wave								
Logical "1" Output Voltage	f_0 = 50 kHz, V_{CC} = ±6 Volts	+4.9	+5.2		+4.9	+5.2		V
Logical "0" Output Voltage	f_0 = 50 kHz, V_{CC} = ±6 Volts		-0.2	+0.2		-0.2	+0.2	V
Duty Cycle	f_0 = 50 kHz	45	50	55	40	50	60	%
Rise Time			20	100		20		nsec
Fall Time			50	200		50		nsec
Output Current (sink)		0.6	1		0.6	1		mA
Output Current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output Voltage Level	(pin 7) V_{CC} = ±6 Volts	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum Voltage Swing	(pin 7)		2			2		Vp-p
Output Voltage Swing	±10% frequency deviation	250	300		200	300		mVp-p
Total Harmonic Distortion			0.2	0.75		0.2	1.5	%
Output Impedance			3.6			3.6		kΩ
Offset Voltage $\lvert V_6 - V_7 \rvert$	T_A = 25°C		30	100		50	200	mV
vs Temperature (drift)			50			100		µV/°C
AM Rejection		30	40			40		dB

NOTES:

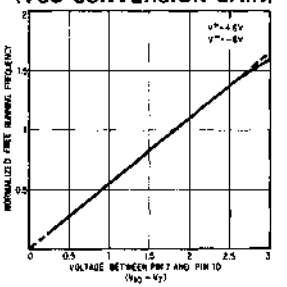
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

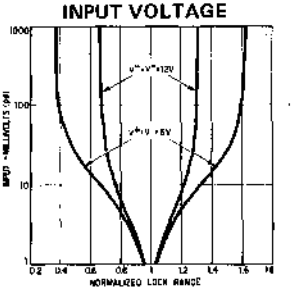
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



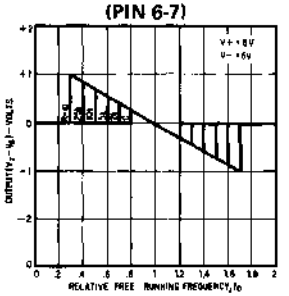
FREE-RUNNING VCO FREQ. AS A FUNCTION OF VOLTAGE BETWEEN PIN 7 & 10 (VCO CONVERSION GAIN)



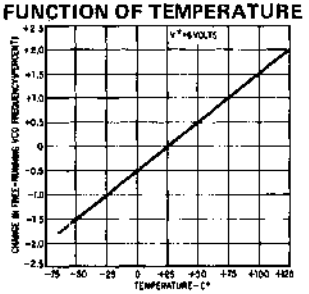
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



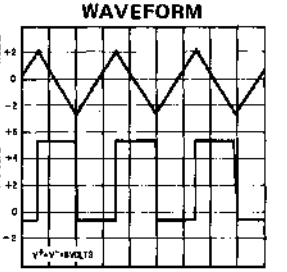
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



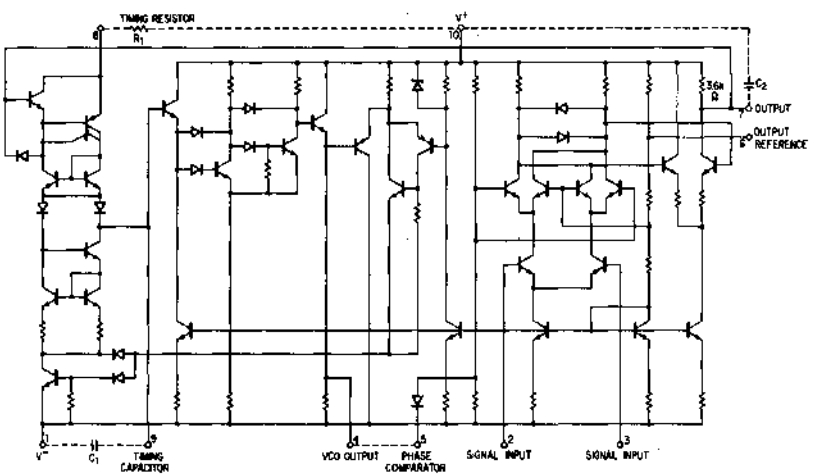
CHANGE IN FREE-RUNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



SCHEMATIC DIAGRAM



DESIGN FORMULAS

Free-running frequency of VCO $f_o = \frac{1.2}{4R_1C_1}$ in Hz

Lock-range $f_L = \pm\frac{8f_o}{V_{cc}}$ in Hz

Capture-range $f_C \simeq \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

DEFINITION OF TERMS

FREE-RUNNING FREQUENCY (f_o)

Frequency of VCO without input signal, both inputs grounded.

CAPTURE-RANGE

That range of frequencies about f_o over which the loop will acquire lock with an input signal initially starting out of lock.

LOCK-RANGE OR TRACKING-RANGE

That range of frequencies in the vicinity of f_o over which the VCO, once locked to the input signal, will remain locked.

TYPICAL APPLICATIONS

FM DEMODULATION

The 565 Phase Locked Loop is a general purpose circuit designed for highly-linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide range (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by $f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance (R_2 in Figure 1) is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C_2, connected between pin 7 and positive supply, and an internal resistance of approximately 3600 ohms.

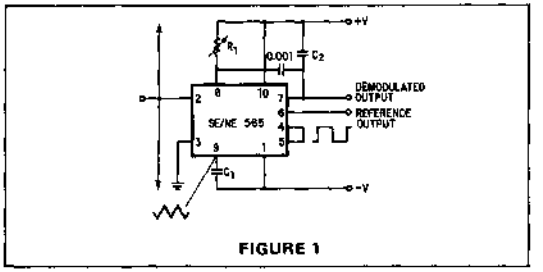


FIGURE 1

FREQUENCY SHIFT KEYING (FSK)

FSK refers to data transmission by means of carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070 Hz and 1270 Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150 Hz) and twice the input frequency (approximately 2200 Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output at f_{in} = 1070 Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

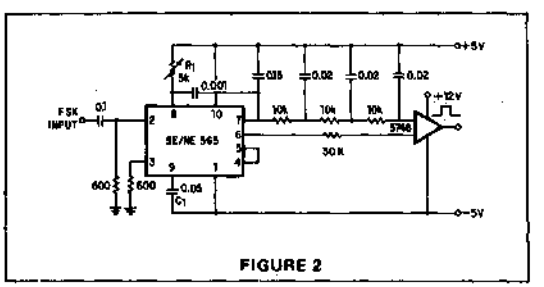


FIGURE 2

FREQUENCY MULTIPLICATION

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_1) as long as the loop is in lock.

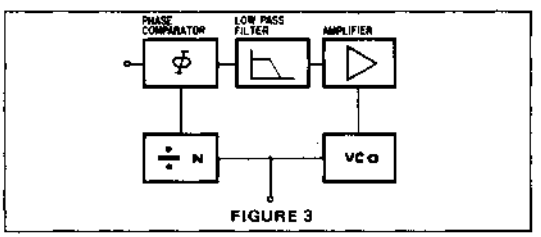


FIGURE 3

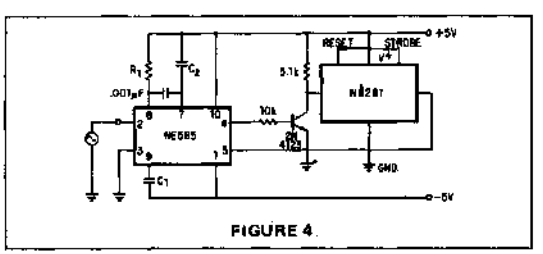


FIGURE 4

SCA (BACKGROUND MUSIC) DECODER

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67 kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80 mV and 300 mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67 kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50 mV and the frequency response extends to 7 kHz.

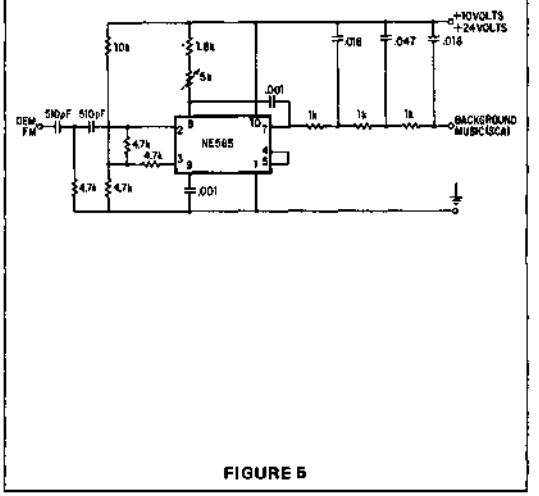


FIGURE 5

DESCRIPTION

The SE/NE 566 Function Generator is a voltage controlled oscillator of exceptional stability and linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

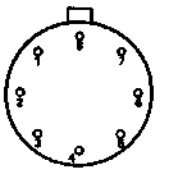
- WIDE RANGE OF OPERATING VOLTAGE (10 to 24 volts)
- VERY HIGH LINEARITY OF MODULATION
- EXTREME STABILITY OF FREQUENCY (100 ppm/°C typical)
- HIGHLY LINEAR TRIANGLE WAVE OUTPUT
- HIGH ACCURACY SQUARE WAVE OUTPUT
- FREQUENCY PROGRAMMING BY MEANS OF A RESISTOR, CAPACITOR, VOLTAGE OR CURRENT
- FREQUENCY ADJUSTABLE OVER 10 TO 1 RANGE WITH SAME CAPACITOR

APPLICATIONS

TONE GENERATORS
FREQUENCY SHIFT KEYING
FM MODULATORS
CLOCK GENERATORS
SIGNAL GENERATORS
FUNCTION GENERATORS

PIN CONFIGURATION (Top View)

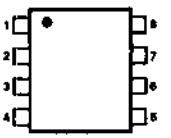
T PACKAGE



1 Ground
2 NC
3 Square Wave Output
4 Triangle Wave Output
5 Modulation Input
6 R_1
7 C_1
8 V+

ORDER PART NOS. SE566T/NE566T

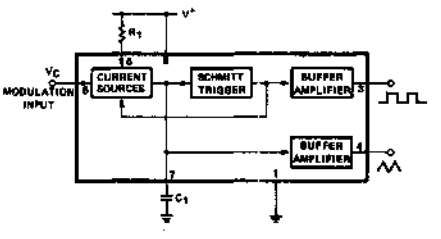
V PACKAGE



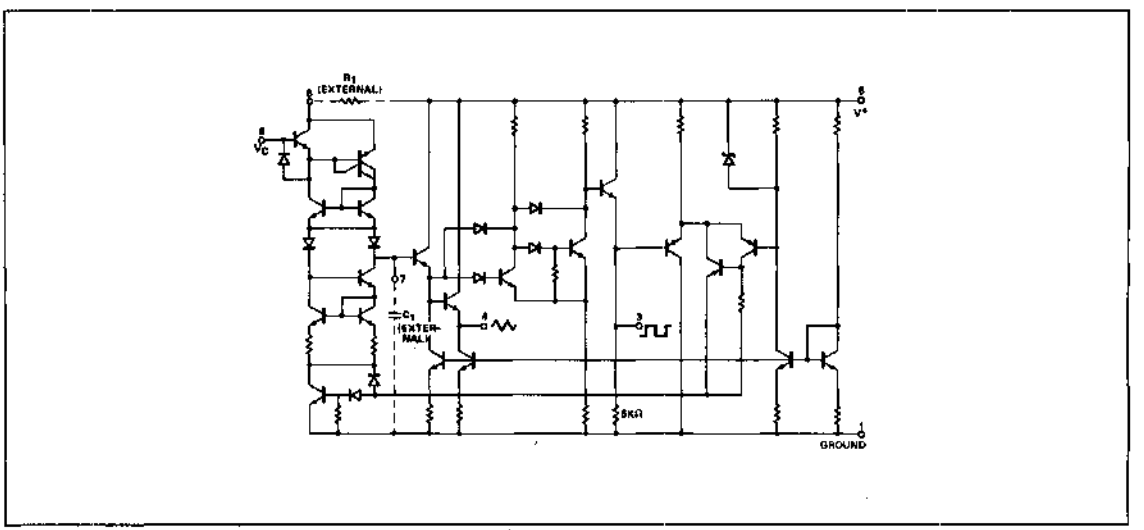
1 Ground
2 NC
3 Square Wave Output
4 Triangle Wave Output
5 Modulation Input
6 R_1
7 C_1
8 V+

ORDER PART NO. NE566V

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

Maximum Operating Voltage	26V
Storage Temperature	−65°C to 150° C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (25°C, 12 Volts, unless otherwise stated)

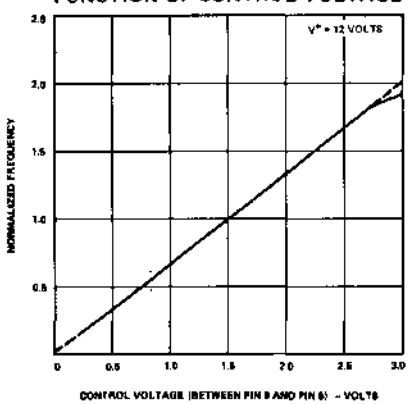
CHARACTERISTICS	SE566			NE566			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
GENERAL							
Operating Temperature Range	-55		125	0		70	°C
Operating Supply Voltage			24			24	Volts
Operating Supply Current		7	12.5		7	12.5	mA
VCO (Note 1)							
Maximum Operating Frequency		1			1		MHz
Frequency Drift with Temperature		100			200		ppm/°C
Frequency Drift with Supply Voltage		1			2		%/volt
Control Terminal Input Impedance (Note 2)		1			1		MΩ
FM Distortion (±10% Deviation)		0.2	0.75		0.2	1.5	%
Maximum Sweep Rate		1			1		MHz
Sweep Range		10:1			10:1		
OUTPUT							
Triangle Wave Output -							
Impedance		50			50		Ω
Voltage	2	2.4		2	2.4		Volts pp
Linearity		0.2			0.5		%
Square Wave Output -							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Volts pp
Duty Cycle	45	50	55	40	50	60	%
Rise Time		20			20		nsec
Fall Time		50			50		nsec

NOTES:

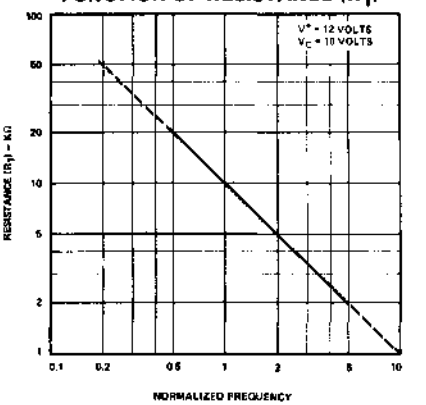
1. The external resistance for frequency adjustment (R_1) must have a value between 2KΩ and 20KΩ.
2. The bias voltage (Vc) applied to the control terminal (pin 5) should be in the range $3/4\ V^+ \leq V_C \leq V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS

NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE

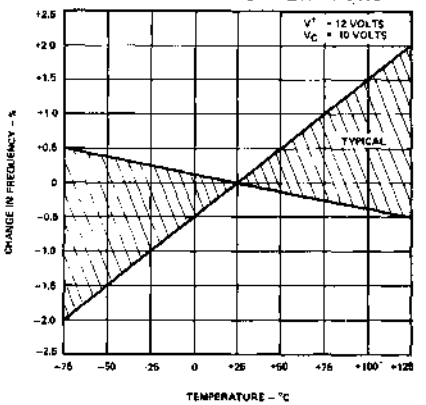


NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R_1)

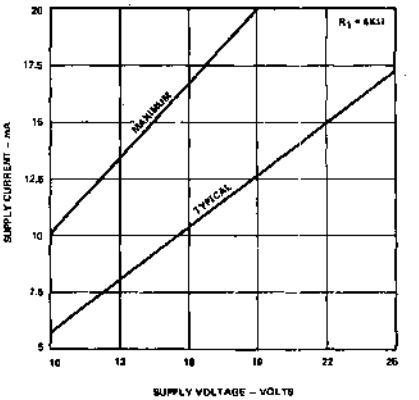


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

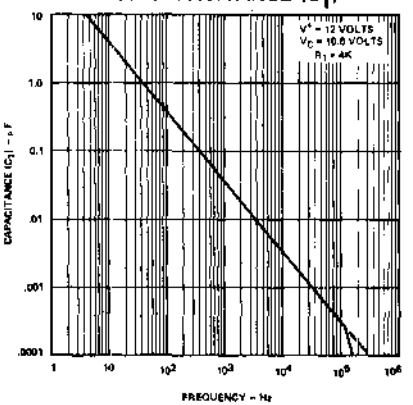
CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE



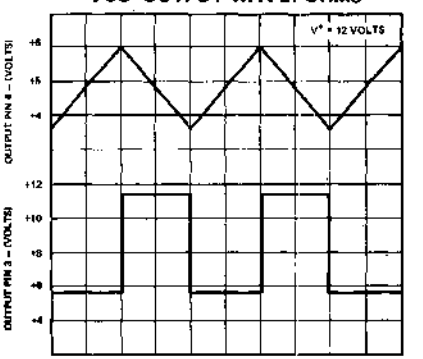
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C_1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1 MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4\ V^+ \leq V_C \leq V^+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_o \simeq \frac{2(V^+ - V_C)}{R_1 C_1 V^+}$$

and R_1 should be in the range $2K < R_1 < 20K\Omega$.

A small capacitor (typically 0.001µf) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

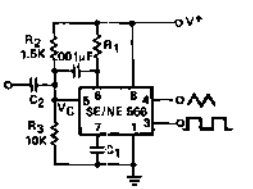


FIGURE 1

OPERATING INSTRUCTIONS (Cont'd)

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T^2L gates, which require a current sink of more than 1 mA, it is usually necessary to connect a 5KΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2 mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T^2L circuitry which requires a fast fall time (< 50 nsec) and a large current sinking capability.

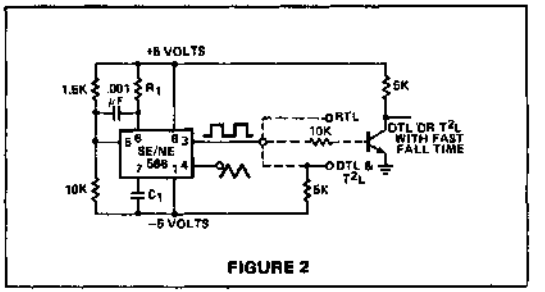


FIGURE 2

DESCRIPTION

The SE/NE 567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

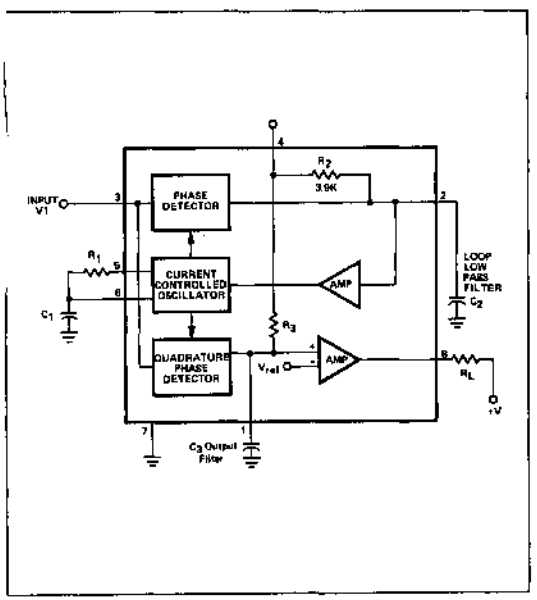
FEATURES

- WIDE FREQUENCY RANGE (.01Hz TO 500kHz)
- HIGH STABILITY OF CENTER FREQUENCY
- INDEPENDENTLY CONTROLLABLE BANDWIDTH (0 TO 14 PERCENT)
- HIGH OUT-BAND SIGNAL AND NOISE REJECTION
- LOGIC-COMPATIBLE OUTPUT WITH 100mA CURRENT SINKING CAPABILITY
- INHERENT IMMUNITY TO FALSE SIGNALS
- FREQUENCY ADJUSTMENT OVER A 20 TO 1 RANGE WITH AN EXTERNAL RESISTOR

APPLICATIONS

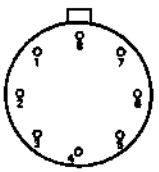
TOUCH TONE® DECODING
CARRIER CURRENT REMOTE CONTROLS
ULTRASONIC CONTROLS (REMOTE TV, ETC.)
COMMUNICATIONS PAGING
FREQUENCY MONITORING AND CONTROL
WIRELESS INTERCOM
PRECISION OSCILLATOR

BLOCK DIAGRAM



PIN CONFIGURATION

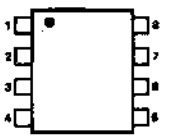
T PACKAGE
(Top View)



1. Output Filter Capacitor C_3
2. Low Pass Filter Capacitor C_2
3. Input
4. Supply Voltage +V
5. Timing Element R_1
6. Timing Elements R_1 and C_1
7. Ground
8. Output

ORDER PART NOS. SE567T/NE567T

V PACKAGE



1. Output Filter Capacitor C_3
2. Low Pass Filter Capacitor C_2
3. Input
4. Supply Voltage +V
5. Timing Element R_1
6. Timing Elements R_1 and C_1
7. Ground
8. Output

ORDER PART NO. NE567V

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to 70°C NE567 -55°C to 125°C SE567
Operating Voltage	10V
Positive Voltage at Input	0.5V above Supply Voltage (Pin 4)
Negative Voltage at Input	-10 VDC
Output Voltage (collector of output transistor)	15 VDC
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (V+ = 5.0 Volts, T_A = 25°C unless noted)

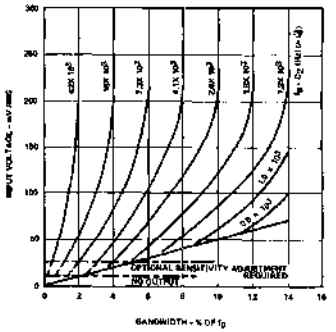
CHARACTERISTICS	SE567 MIN	SE567 TYP	SE567 MAX	NE567 MIN	NE567 TYP	NE567 MAX	UNITS	TEST CONDITIONS
CENTER FREQUENCY (NOTE 1)								
Highest Center Frequency (f_o)	100	500		100	500		kHz	
Center Frequency Stability (Note 2)		35±140 35±60			35±140 35±60		ppm/°C ppm/°C	−55 to 125°C 0 to 70°C
Center Frequency Shift with Supply Voltage		0.5	1		0.7	2	%/Volt	f_o = 100KHz
DETECTION BANDWIDTH								
Largest Detection Bandwidth	12	14	16	10	14	18	% of f_o	f_o = 100KHz
Largest Detection Bandwidth Skew		1	2		2	3	% of f_o	
Largest Detection Bandwidth – Variation with Temperature		±0.1			±0.1		%/°C	V_i = 300mVrms
Largest Detection Bandwidth – Variation with Supply Voltage		±2			±2		%/Volt	V_i = 300mVrms
INPUT								
Input Resistance		20			20		KΩ	
Smallest Detectable Input Voltage(V_i)		20	25		20	25	mV rms	I_L = 100mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		10	15		mV rms	I_L = 100mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6			+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6			−6		dB	Bn = 140KHz
OUTPUT								
Fastest On-Off Cycling Rate		f_o/20			f_o/20			
"1" Output Leakage Current		0.01	25		0.01	25	μA	
"0" Output Voltage		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	Volt Volt	I_L = 30mA I_L = 100mA
Output Fall Time (Note 3)		30			30		n sec	R_L = 50Ω
Output Rise Time (Note 3)		150			150		n sec	R_L = 50Ω
GENERAL								
Operating Voltage Range	4.75		9.0	4.75		9.0	Volts	
Supply Current – Quiescent		6	8		7	10	mA	
Supply Current – Activated		11	13		12	15	mA	R_L = 20KΩ
Quiescent Power Dissipation		30			35		mW	

NOTES:

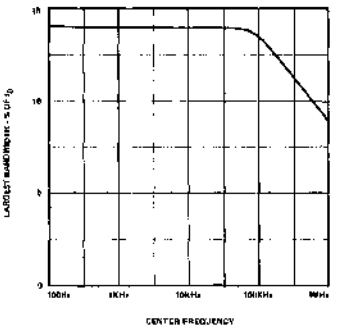
1. Frequency determining resistor R_1 should be between 1 and 20KΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL CHARACTERISTIC CURVES

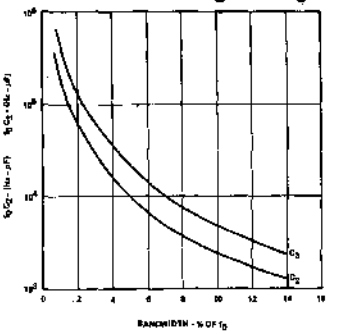
BANDWIDTH VERSUS INPUT SIGNAL AMPLITUDE



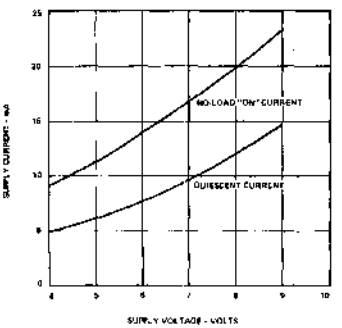
LARGEST DETECTION BANDWIDTH VERSUS OPERATING FREQUENCY



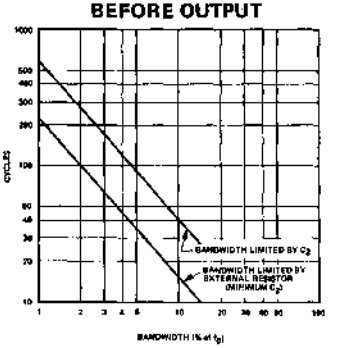
DETECTION BANDWIDTH AS A FUNCTION OF C_2 AND C_3



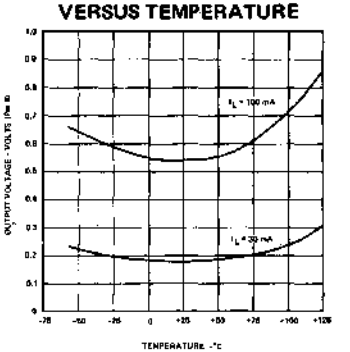
TYPICAL SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



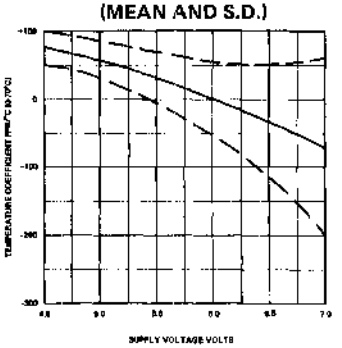
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



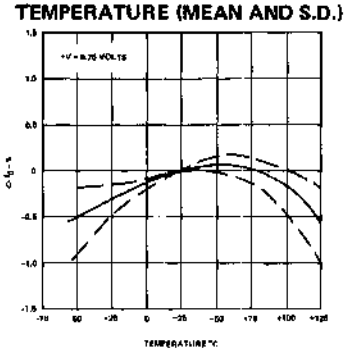
TYPICAL OUTPUT VOLTAGE VERSUS TEMPERATURE



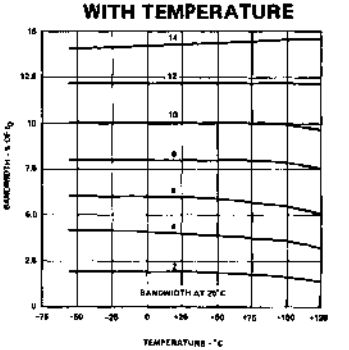
CENTER FREQUENCY COEFFICIENT TEMPERATURE (MEAN AND S.D.)



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)

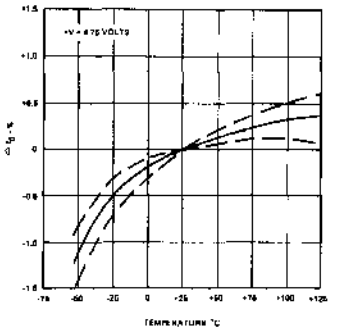


TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE

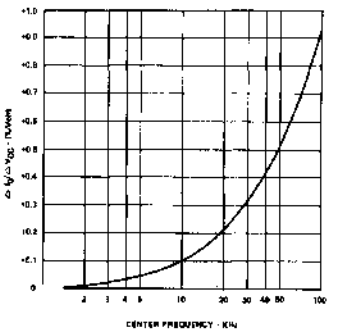


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

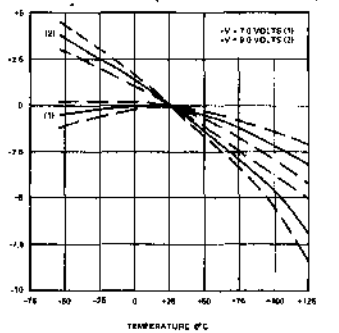
TYPICAL FREQUENCY DRIFT WITH (MEAN AND S.D.) TEMPERATURE

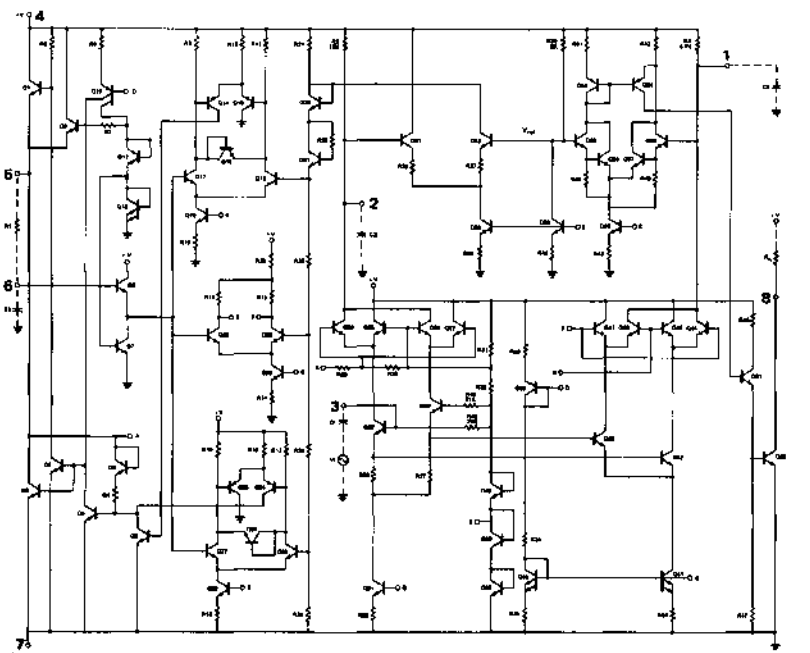


CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE VERSUS OPERATING FREQUENCY



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)





DESIGN FORMULAS

$$f_0 \simeq \frac{1.1}{R_1 C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_i}{f_0 C_2}} \quad \text{in \% of } f_0,\ V_i \lesssim 200mV$$

Where

V_i = Input Voltage (mV)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY

CENTER FREQUENCY (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

DETECTION BANDWIDTH (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mV rms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

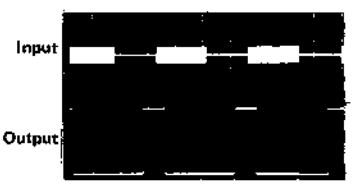
LARGEST DETECTION BANDWIDTH

The largest frequency range within which an input signal above the threshold voltage will cause a logical zero state on the output. The maximum detection bandwidth corresponds to the loop lock range.

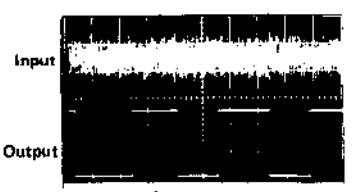
DETECTION BAND SKEW

A measure of how well the largest detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/f_0$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

TYPICAL RESPONSE



Response to 100mV RMS tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.

$\frac{S}{N}$ = -6db $\qquad R_L$ = 100 ohms

Noise Bandwidth = 140 Hz

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the R_1C_1 product should have sufficient stability, over the projected temperature range to meet the necessary requirements.

2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product(F_0 (Hz), C_2 (μfd)..).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such a delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

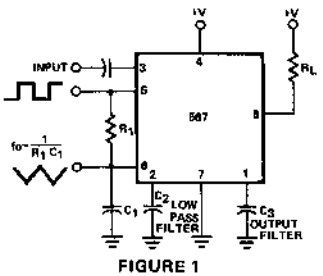


FIGURE 1

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output, a linear function of frequency, over the range of 0.95 to 1.05 f_0, with a slope of about 20mV/% frequency deviation. The average voltage at pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(V^+ - 2Vbe) \approx (V^+ - 1.4V)$ having a dc average of $V^+/2$. A 1KΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak

SQUARE WAVE OUTPUTS (Cont'd.)

with an average dc level of $V^+/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

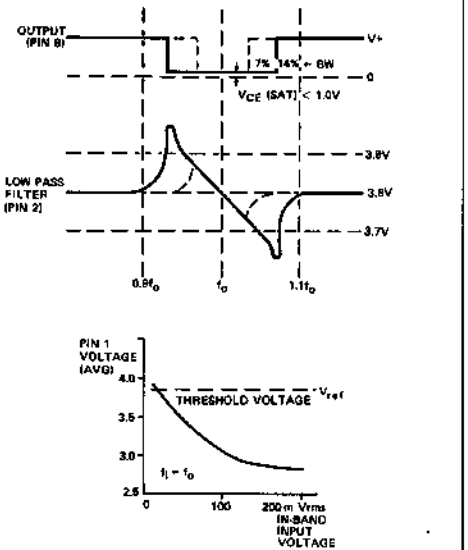


FIGURE 2

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user attain the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.

2. The 567 will lock onto signals near $(2n+1)\ f_o$, and will give an output for signals near $(4n+1)\ f_o$ where n = 0, 1, 2, etc. Thus, signals at 5 f_o and 9 f_o can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (Below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs. Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with an 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply, or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_0/10$ baud.

$$C_2 = \frac{130}{f_o}\mu F$$

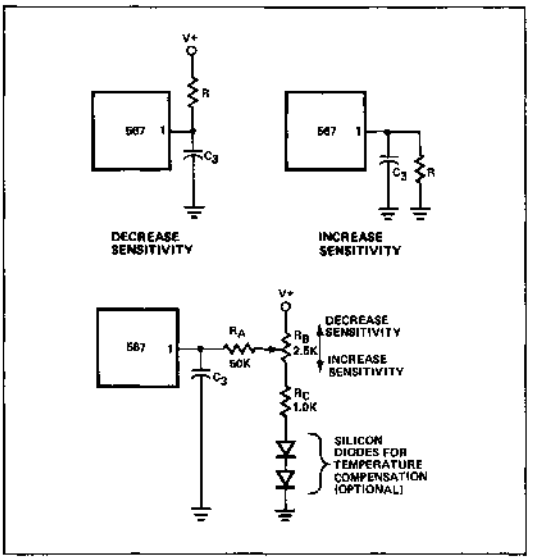
$$C_3 = \frac{260}{f_o}\mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased low-voltage zeners or forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

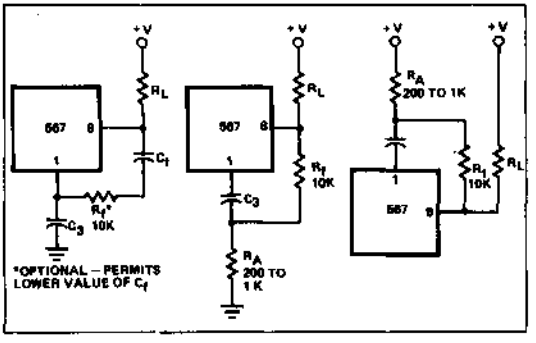
SENSITIVITY ADJUSTMENT



When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10m or lower).

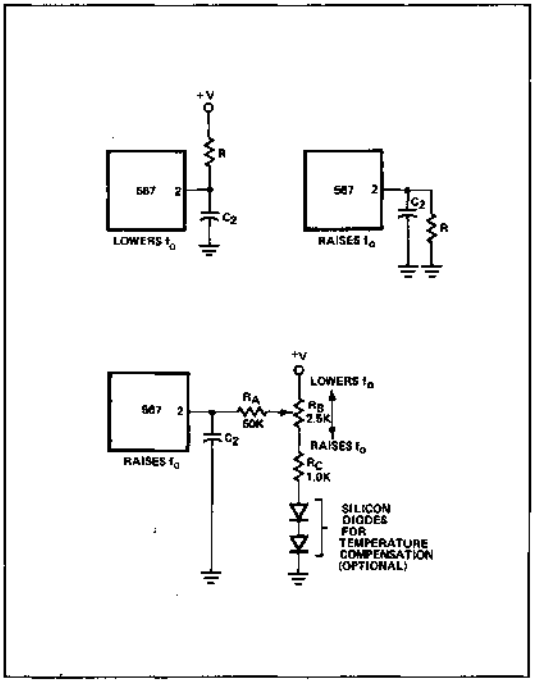
By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION

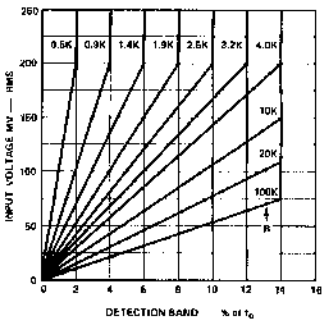


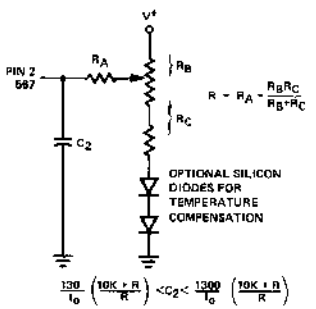
Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input, (pin 1) the chatter can be eliminated. Three schemes for doing this are given above. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT



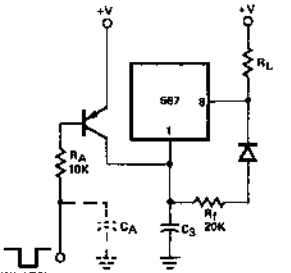
When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the largest detection band (lock range), the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

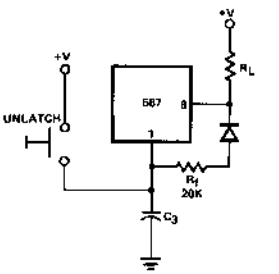




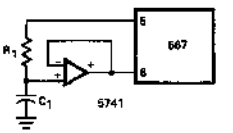
NOTE: Adjust control for symmetry of detection band edges about f_o.

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band operation. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the R_B, R_C network can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.





To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

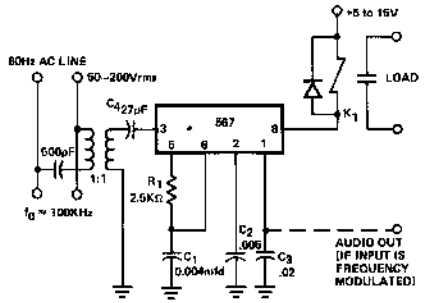


For precision, very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

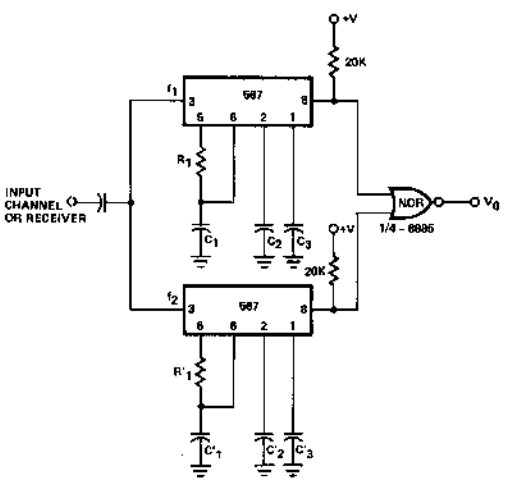
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

TYPICAL APPLICATIONS

CARRIER-CURRENT REMOTE CONTROL OR INTERCOM

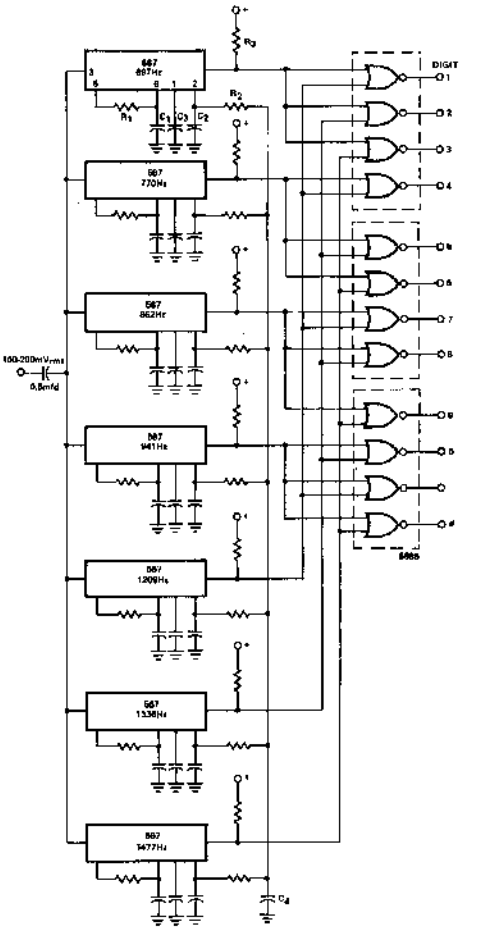


DUAL-TONE DECODER



1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1, f_2) tones is possible.

TOUCH-TONE® DECODER

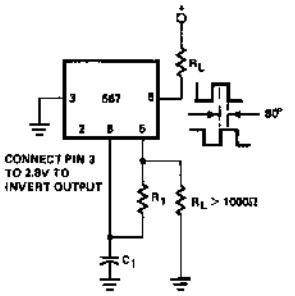


Component Values (Typical)

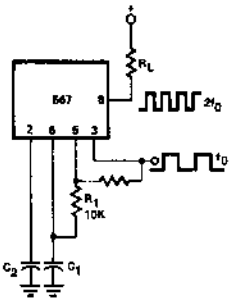
R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10 mfd
C_2	1.0 mfd 6V
C_3	2.2mfd 6V
C_4	250 6V

APPLICATIONS (Cont'd.)

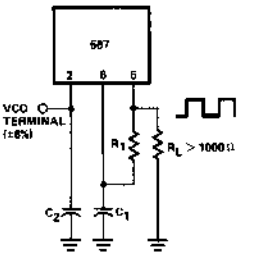
OSCILLATOR WITH QUADRATURE OUTPUT



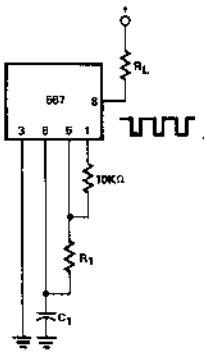
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



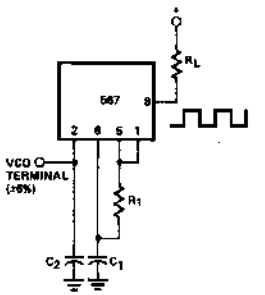
PRECISION OSCILLATOR WITH 20nsec SWITCHING



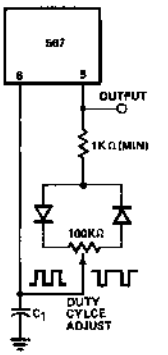
PULSE GENERATOR WITH 25% DUTY CYCLE



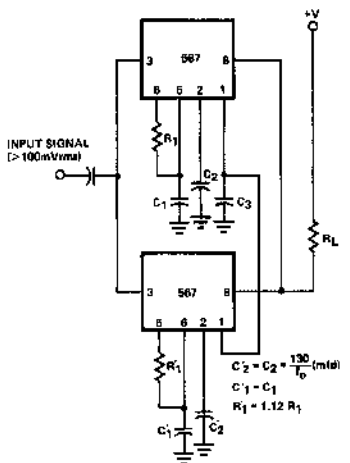
PRECISION OSCILLATOR TO SWITCH 100ma LOADS



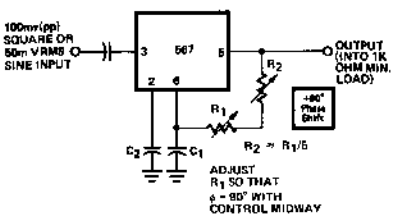
PULSE GENERATOR



24% BANDWIDTH TONE DECODER



0° TO 180° PHASE SHIFTER



DESCRIPTION

The SE/NE 592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the μA733.

FEATURES

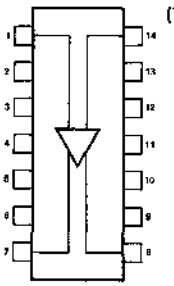
- **120 MHz BANDWIDTH**
- **ADJUSTABLE GAINS FROM 0 TO 400**
- **ADJUSTABLE PASS BAND**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8V
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
Output Current	10mA
Operating Temperature Range	
SE592K	−55°C to +125°C
NE592K	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C

PIN CONFIGURATIONS

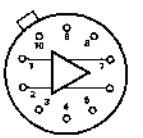
A PACKAGE
(Top View)



1. Input 2
2. NC
3. G_{2B} Gain Select
4. G_{1B} Gain Select
5. V^-
6. NC
7. Output 2
8. Output 1
9. NC
10. V^+
11. G_{1A} Gain Select
12. G_{2A} Gain Select
13. NC
14. Input 1

ORDER PART NOS. SE592A/NE592A

K PACKAGE



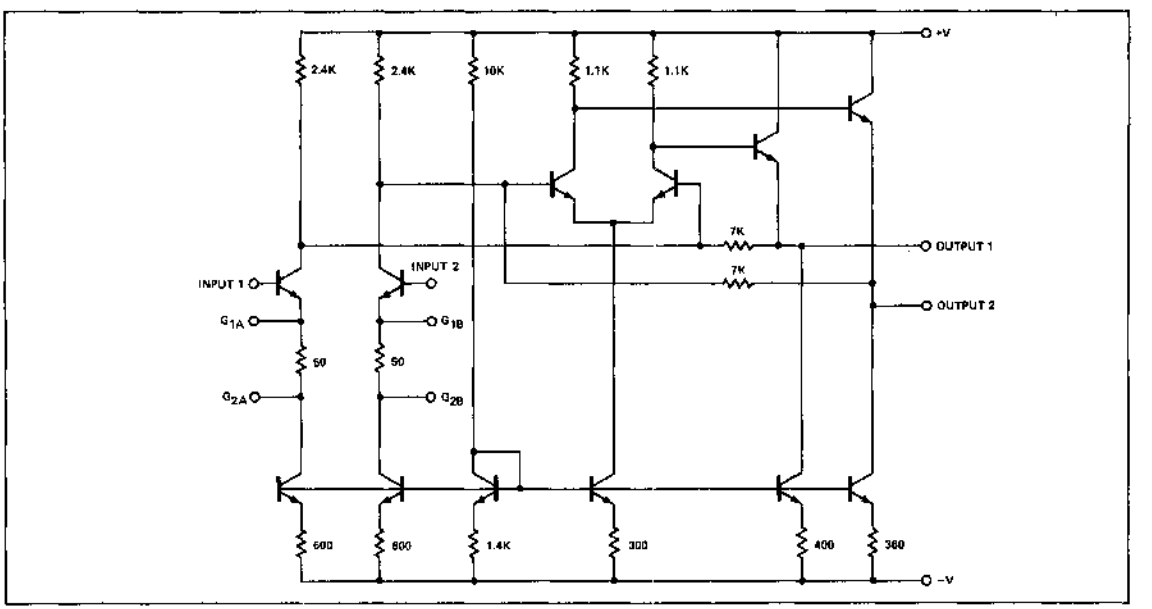
1. Input 1
2. Input 2
3. G_{2B} Gain Select
4. G_{1B} Gain Select
5. V^-
6. Output 2
7. Output 1
8. V^+
9. G_{1A} Gain Select
10. G_{2A} Gain Select

NOTE: Pin 5 connected to case.
ORDER PART NOS. SE592K/NE592K

Thermal Resistance (θ_{J-A}, Junction to Ambient for each package):

A Package	0.16°C/mW
K Package	0.145°C/mW
Power Dissipation	500mW

EQUIVALENT CIRCUIT



Standard Conditions (T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified)

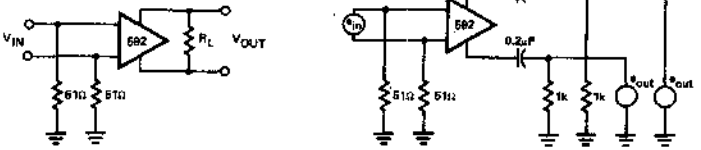
PARAMETER	TEST CONDITIONS	NE 592			SE 592			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain								
Gain 1	Note 1 R_L = 2KΩ, V_{OUT} = 3V p-p	250	400	600	300	400	600	
Gain 2	Note 2	80	100	120	90	100	110	
Bandwidth								
Gain 1	Note 1		40			40		MHz
Gain 2	Note 2		90			90		MHz
Rise Time								
Gain 1	Note 1 V_{OUT} = 1V p-p		10.5			10.5		ns
Gain 2	Note 2		4.5	12		4.5	10	ns
Propagation Delay								
Gain 1	Note 1 V_{OUT} = 1V p-p		7.5			7.5		ns
Gain 2	Note 2		6.0	10		6.0	10	ns
Input Resistance								
Gain 1	Note 1		4.0			4.0		KΩ
Gain 2	Note 2	10	30		20	30		KΩ
Input Capacitance	Gain 2, Note 2		2.0			2.0		pF
Input Offset Current			0.4	5.0		0.4	3.0	μA
Input Bias Current			9.0	30		9.0	20	μA
Input Noise Voltage	BW 1 kHz to 10 kHz		12			12		μV rms
Input Voltage Range				±1.0			±1.0	V
Common Mode Rejection Ratio								
Gain 2	VCM ±1V, F < 100 kHz	60	86		60	86		dB
Gain 2	VCM ±1V, F = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio								
Gain 2	ΔVS = ±0.5V	50	70		50	70		dB
Output Offset Voltage								
Gain 3	R_L = ∞, Note 3		0.35	0.75		0.35	0.75	V
Output Common Mode Voltage	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	R_L = 2K	3.0	4.0		3.0	4.0		
Output Resistance			20			20		Ω
Power Supply Current	R_L = ∞		18	24		18	24	mA

Recommended Operating Supply Voltages (V_S = ±6.0V)

NOTES:

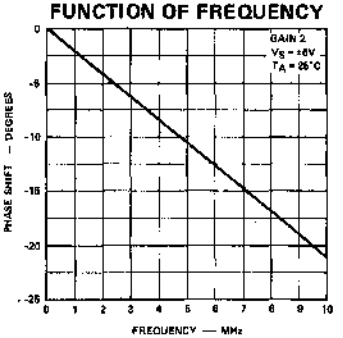
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TEST CIRCUITS (T_A = 25°C unless otherwise specified)

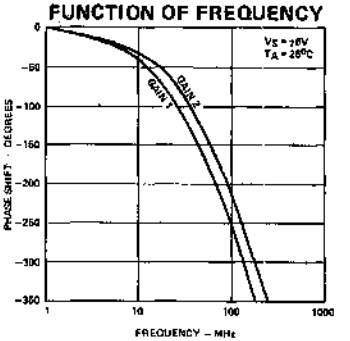


TYPICAL CHARACTERISTICS

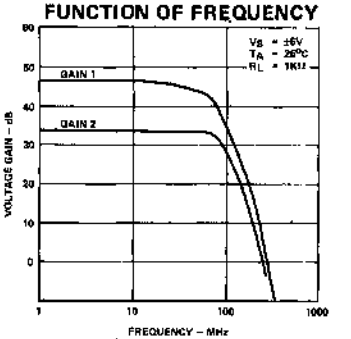
PHASE SHIFT AS A FUNCTION OF FREQUENCY



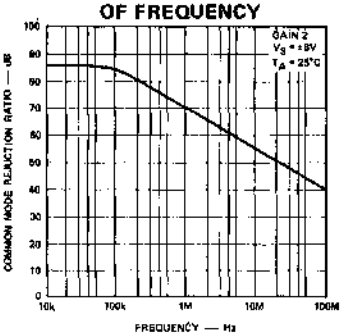
PHASE SHIFT AS A FUNCTION OF FREQUENCY



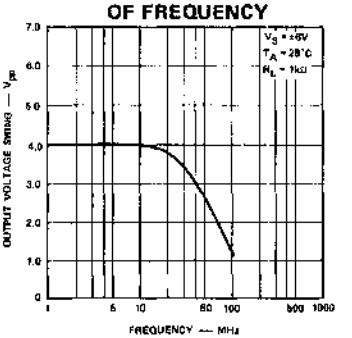
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



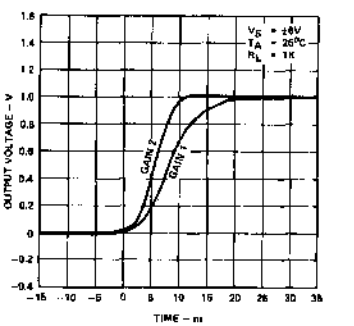
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

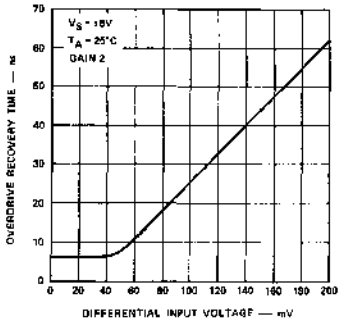


PULSE RESPONSE

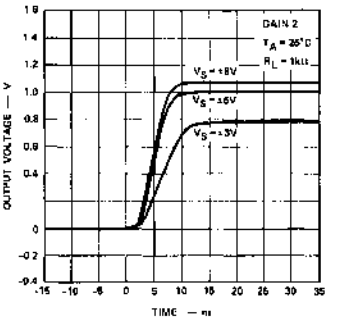


TYPICAL CHARACTERISTIC CURVES (Cont'd)

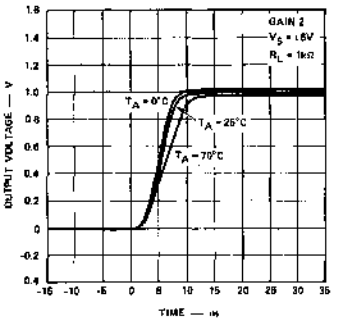
DIFFERENTIAL OVERDRIVE RECOVERY TIME



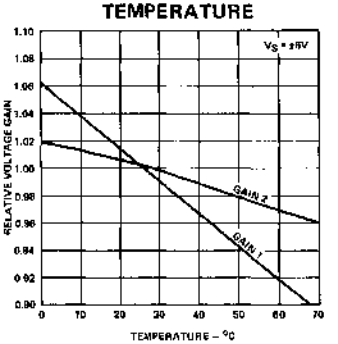
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



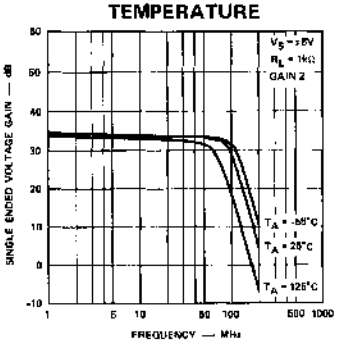
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



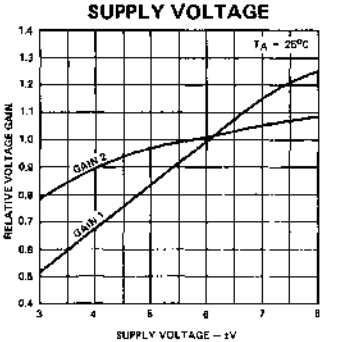
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



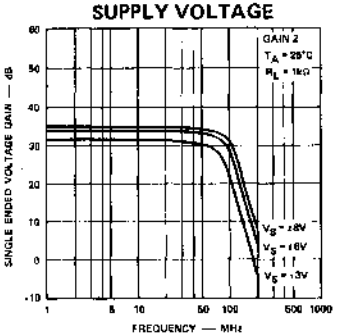
GAIN VS FREQUENCY AS A FUNCTION OF TEMPERATURE



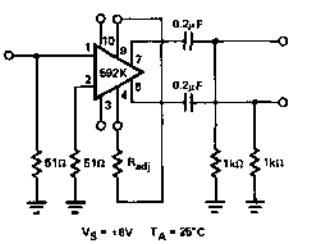
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN VS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE GAIN ADJUST CIRCUIT



(Pin numbers apply to K Package)

VOLTAGE GAIN AS A FUNCTION OF R_{ADJ} (FIGURE 3)

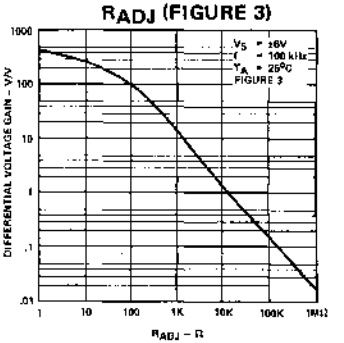
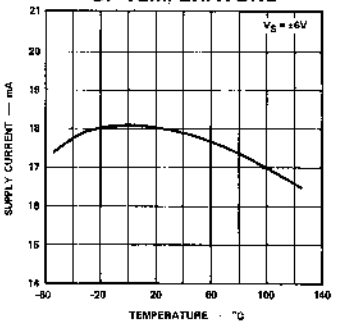


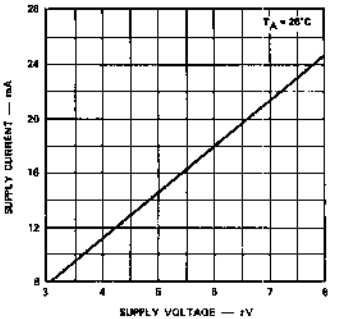
FIGURE 3

TYPICAL CHARACTERISTIC CURVES (Cont'd)

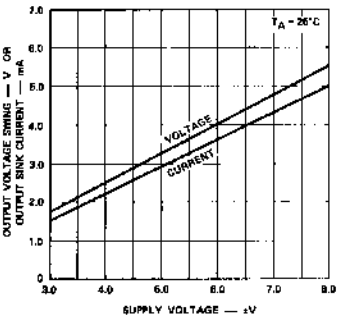
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



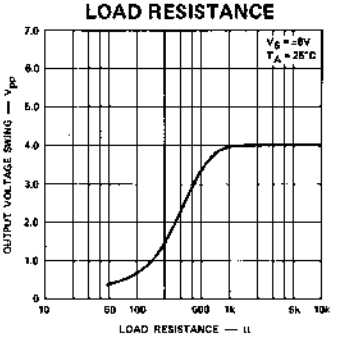
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



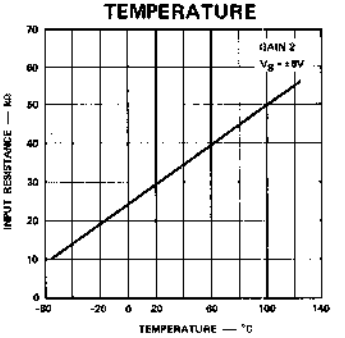
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



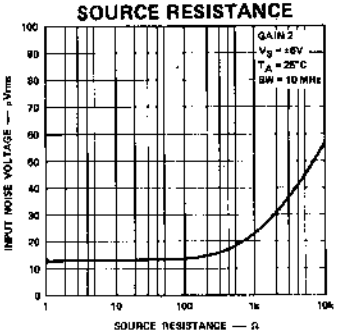
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



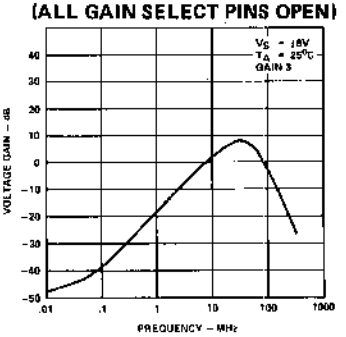
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



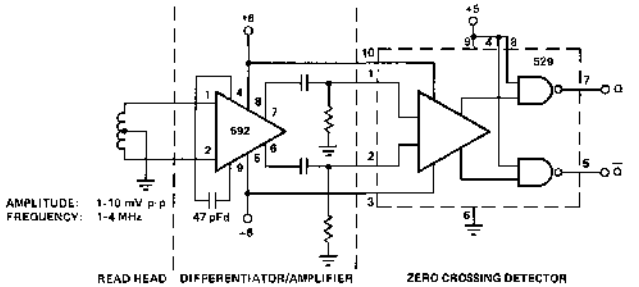
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



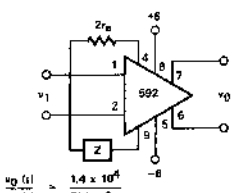
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



DISC/TAPE PHASE MODULATED READBACK SYSTEMS



FILTER NETWORKS



$$\frac{v_0(s)}{v_1(s)} \simeq \frac{1.4 \times 10^4}{Z(s) + 2r_g}$$

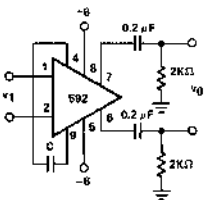
$$\simeq \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$v_0(s)/v_1(s)$ TRANSFER FUNCTION
R, L	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R, C	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R, L, C	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
L; R, C	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: IN THE NETWORKS ABOVE, THE R VALUE USED IS ASSUMED TO INCLUDE 2 r_g, OR APPROXIMATELY 32 OHMS.

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $f_1 << 1/2\pi(32)C$

$$v_0 \simeq 1.4 \times 10^4\, C \frac{dv_i}{dT}$$

DESCRIPTION

The μA709 is a high performance monolithic operational amplifier with differential inputs. High open loop gain, high input impedance, wide input common mode and output voltage ranges plus low temperature drift enable it to be used in many applications formerly satisfied only by discrete amplifiers.

FEATURES

- OPEN LOOP VOLTAGE GAIN = 45,000
- OUTPUT VOLTAGE SWING = ±14V
- INPUT COMMON MODE RANGE = ±10V
- DIFFERENTIAL INPUT RESISTANCE = μA709 250kΩ, μA709C 400kΩ

ABSOLUTE MAXIMUM RATINGS

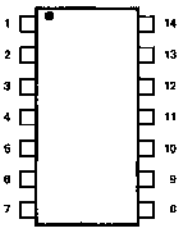
Supply Voltage	±18V
Internal Power Dissipation (Note 1)	N5709 250 mW S5709 300 mW
Differential Input Voltage	±5.0V
Input Voltage	±10V
Open Short-Circuit Duration (T_A = 25°C)	-25°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	μA709C 0°C to +75°C μA709 -55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTE:

1. Rating applied for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.

PIN CONFIGURATIONS

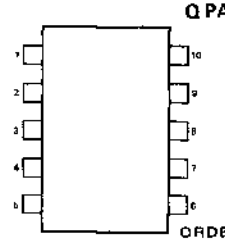
A PACKAGE
(Top View)



1. NC
2. NC
3. Input compensation A
4. Inverting input
5. Non-inverting input
6. V^-
7. NC
8. NC
9. Output Compensation
10. Output
11. V^+
12. Input compensation B
13. NC
14. NC

ORDER PART NOS. μA790A/μA709CA

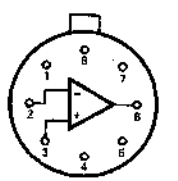
Q PACKAGE



1. NC
2. Input compensation A
3. Inverting input
4. Non-inverting input
5. V^-
6. Output compensation
7. Output
8. V^+
9. Input compensation B
10. NC

ORDER PART NOS. μA709Q/μA709CQ

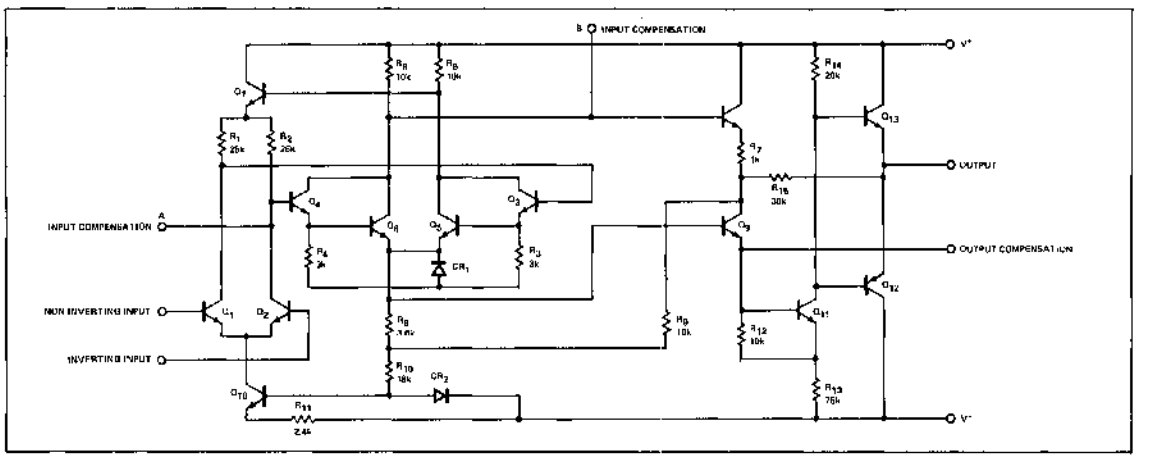
T PACKAGE



1. Input compensation A
2. Inverting input
3. Non-inverting input
4. V^-
5. Output compensation
6. Output
7. V^+
8. Input compensation B

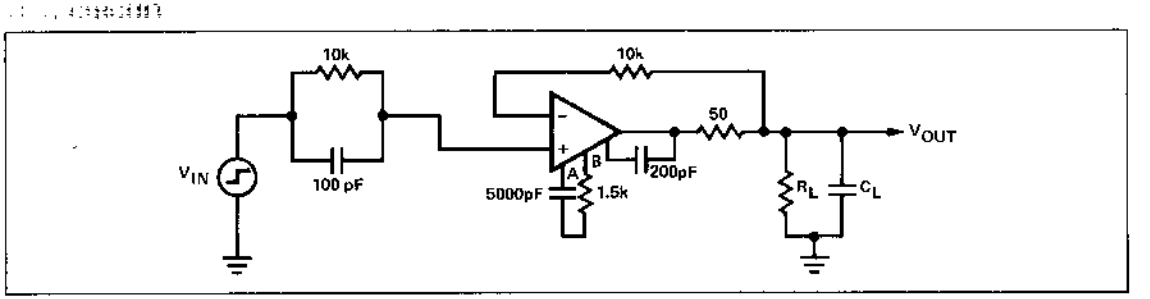
ORDER PART NOS. μA709T/μA709CT

TYPICAL CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = ±25°C, V_S = ±15V (709C); ±9 ≤ V_S ≤ ±15 (709) unless otherwise specified)

PARAMETER	TEST CONDITIONS	μA709			μA709C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
Offset Voltage @ 25°C	$R_S \leq 10K\Omega$, +9V, $\leq V_S \leq$ +15V		1	5		2	7.5	mV
Over Temperature	$R_S \leq 10K\Omega$, ±9V ≤ ±15V			6			10	mV
Offset Current @ 25°C			50	200		100	500	nA
Over Temperature	T_A = +125°C		20	200				nA
	T_A = -55°C		100	500				nA
	0°C ≤ T_A ≤ 75°C						750	nA
Bias Current @ 25°C			200	500		300	1500	nA
Over Temperature	T_A = -55°C		0.5	1.5				μA
INPUT RESISTANCE @ 25°C		150	400		50	250		kΩ
Over Temperature		40	100		35			kΩ
INPUT VOLTAGE RANGE @ 25°C					±8.0	±10		V
Over Temperature	V_S = ±15V	±8.0	±10					V
OUTPUT CHARACTERISTICS								
Resistance @ 25°C			150			150		Ω
Voltage Swing	$R_L \geq 10K\Omega$				±12	±14		V
	$R_L \geq 2k\Omega$				±10	±13		V
Over Temperature	V_S = ±15V, $R_L \geq 10K\Omega$	±12	±14					V
	V_S = ±15V, $R_L \geq 2K\Omega$	±10	±13					V
POWER CONSUMPTION	V_S = +15V		80	165		80	200	mW
TRANSIENT RESPONSE (Figure 1)	V_{in} = 10mV, R_L = 2KΩ							
Rise Time			0.3	1.0		0.3	1.0	μW
Overshoot	$C_L \leq 100$ pF		10	30		10	30	%
LARGE SIGNAL VOLTAGE GAIN @ 25°C	$R_L \geq 25K\Omega$; V_{out} = ±10V				15,000	45,000		V/V
Over Temperature	$R_L \geq 25K\Omega$, V_{out} = ±10V	25,000	45,000	70,000	12,000			V/V
COMMON MODE REJECTION RATIO @ 25°C	$R_S \leq 10K\Omega$				65	90		dB
Over Temperature	$R_S \leq 10K\Omega$	70	90					dB
SUPPLY VOLTAGE REJECTION RATIO @ 25°C	$R_S \leq 10K\Omega$					25	200	μV/V
Over Temperature	$R_S \leq 10K\Omega$	25	150					μV/V
AVERAGE TEMPERATURE								
Coefficient of Input	R_S = 50Ω		3.0					μV/°C
Offset Voltage	$R_S \leq 10K\Omega$		6.0					μV/°C



DESCRIPTION

The μA710 is a High Speed Differential Voltage Comparator featuring low offset voltage, high sensitivity and a wide input voltage range. It is ideally suited for use as a pulse height discriminator, an analog comparator or a digital line receiver. The output structure of the μA710 is compatible with DTL, TTL and Utilogic integrated circuits.

The μA710 is specified for operation over the MIL temperature range of -55°C to +125°C. The μA710C is specified for operation over the commercial/industrial temperature range of 0°C to +75°C.

FEATURES

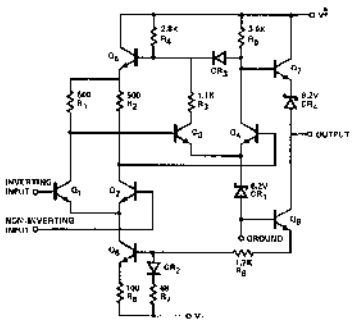
- **FAST RESPONSE – 40ns**
- **HIGH SENSITIVITY – 1.7V/mv**
- **LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT – 3.5μV/°C**
- **HIGH INPUT VOLTAGE RANGE – ±5.0V**

ABSOLUTE MAXIMUM RATINGS

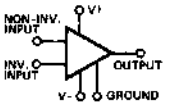
Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	10mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Internal Power Dissipation (Note 4)	
TO-99	300mW
TO-91	200mW
Operating Temperature Range	
μA710	-55°C to +125°C
μA710C	0°C to +75°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Maximum Ratings are limiting values above which serviceability may be impaired.

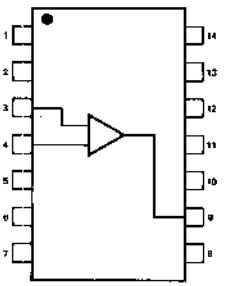
BASIC CIRCUIT SCHEMATIC



PIN CONFIGURATION



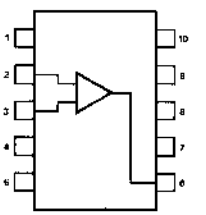
A PACKAGE
(Top View)



1. NC
2. Ground
3. Non-Inverting Input
4. Inverting Input
5. NC
6. V^-
7. NC
8. NC
9. Output
10. NC
11. V^+
12. NC
13. NC
14. NC

ORDER PART NOS. μA710A/μA710CA

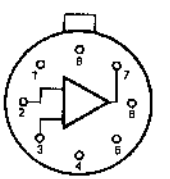
Q PACKAGE



1. Ground
2. Non-Inverting Input
3. Inverting Input
4. NC
5. V^-
6. Output
7. NC
8. V^+
9. NC
10. NC

ORDER PART NOS. μA710Q/μA710CJ

T PACKAGE



1. Ground
2. Non-Inverting Input
3. Inverting Input
4. V^-
5. NC
6. NC
7. Output
8. V^+

ORDER PART NOS. μA710T/μA710CT

ELECTRICAL CHARACTERISTICS (Note 1)

(Standard Conditions: T_A = +25°C, V^+ = 12V, V^- = -6.0V unless otherwise specified)

PARAMETERS	TEST CONDITIONS	MIN		TYP		MAX		UNITS
		μA710	μA710C	μA710	μA710C	μA710	μA710C	
Input Offset Voltage	$R_S \leq 200\Omega$ Note 3			0.6	1.6	2.0	5.0	mV
Input Offset Current	Note 3			0.75	1.8	3.0	5.0	μA
Input Bias Current				13	16	20	25	μA
Voltage Gain		1250	1000	1700	1600			
Output Resistance				200	200			Ω
Output Sink Current	$\Delta V_{in} \geq 5mV$, V_{out} = 0	2.0	1.6	2.5				mA
Response Time	Note 2			40	40			ns
Except as noted, the following specifications apply over the temperature ranges of: -55°C ≤ T_A ≤ +125°C for the S5710 0°C ≤ T_A ≤ +75°C for the N5710								
Input Offset Voltage	$R_S \leq 200\Omega$ Note 3					3.0	6.5	
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = +25°C to +125°C			3.5		10		μV/°C
	R_S = 50Ω, T_A = +25°C to -55°C			2.7		10		
	R_S = 50Ω, T_A = 0°C to +75°C				5		20	
Input Offset Current	T_A = +125°C Note 3			0.25		3.0		μA
	T_A = -55°C			1.8		7.0		μA
	T_A = 0°C to +75°C						7.5	μA
Average Temperature Coefficient of Input Offset Current	T_A = +25°C to +125°C			6.0		25		nA/°C
	T_A = +25°C to -55°C			15		75		nA/°C
	T_A = +25°C to +75°C				15		50	μA/°C
	T_A = +25°C to 0°C				24		100	μA/°C
Input Bias Current	T_A = -55°C			27		45		μA
	T_A = 0°C				25		40	μA
Input Common Mode Voltage Range	V^- = -7.0V	±5.0	±5.0					V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	70	100	98			dB
Differential Input Voltage Range		±5.0	±5.0					
Voltage Gain		1000	800					
Positive Output Level	$\Delta V_{in} \geq 5mV$, 0 ≤ I_{out} ≤ 5.0mA	2.5	2.5	3.2	3.2	4.0	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5mV$	-1.0	-1.0	-0.6	-0.6	0	0	V
Output Sink Current	T_A = +125°C, $\Delta V_{in} \geq 5ma$, V_{out} = 0	0.5		1.7				mA
	T_A = -55°C, $\Delta V_{in} \geq 5mV$, V_{out} = 0	1.0		2.3				mA
	T_A = 0°C to +75°C, $\Delta V_{in} \geq 5mV$, V_{out} = 0		0.5					mA
Positive Supply Current	$V_{out} \leq 0$			5.2	5.2	9.0	9.0	mA
Negative Supply Current				4.6	4.6	7.0	7.0	mA
Power Consumption				90	90	150	150	mW

(Recommended Operating Supply Voltages: V^+ = 12V, V^- = -6V)

NOTES:

1. All voltages are referenced to pin F.
2. The response time specified is measured with a 100mV input step, and a 5mV overdrive.
3. Input Offset Voltage and Input Offset Current are specified for output voltage levels of:

μA710	μA710C
1.8V at -55°C	1.5V at 0°C
1.4V at +25°C	1.4V at +25°C
1.0V at +125°C	1.2V at +75°C

4. Rating applies for temperatures up to: μA710 — +125°C
   μA710C — +75°C

DESCRIPTION

The μA711 High Speed Dual Voltage Comparator features low offset voltage, high sensitivity and a wide input voltage range. It is ideal for use as a bi-directional limit detector in automatic test equipment.

Due to fast response and strobe control capabilities the μA711 performs well as a sense amplifier in core memory systems.

The μA711 is specified over the military temperature range of -55°C to +125°C. The μA711 is specified over the commercial/industrial temperature range of 0°C to +75°C.

FEATURES

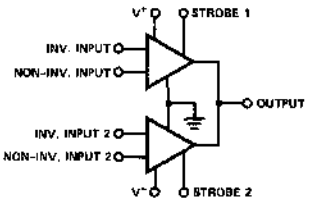
- **FAST RESPONSE – 40ns**
- **HIGH SENSITIVITY – 1.5V/mV**
- **LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT – 5μV/°C**
- **HIGH INPUT VOLTAGE RANGE – ±5.0V**

ABSOLUTE MAXIMUM RATINGS

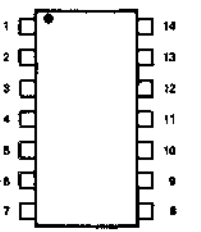
Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	50mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Internal Power Dissipation (Note 4)	
TO-99	300mW
Operating Temperature Range	
μA711	-55°C to +125°C
μA711C	0°C to +75°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Maximum ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION



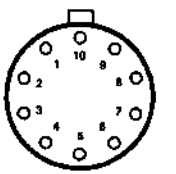
A PACKAGE
(Top View)



ORDER PART NOS.
μA711A/μA711CA

1. NC
2. Inverting Input 1
3. Non-Inverting Input 1
4. V⁻
5. Non-Inverting Input 2
6. Inverting Input 2
7. NC
8. NC
9. Strobe 2
10. Output
11. V⁺
12. Ground
13. Strobe 1
14. NC

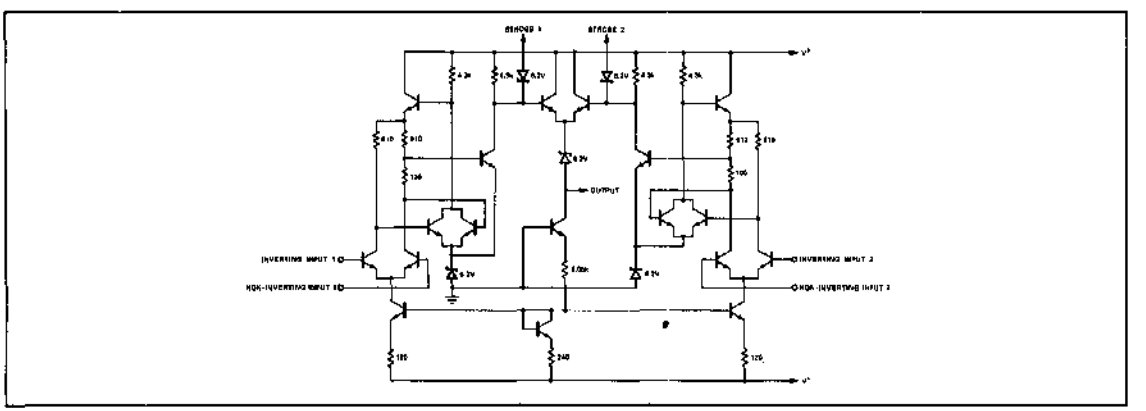
K PACKAGE



ORDER PART NOS.
μA711K/μA711CK

1. Ground
2. Strobe 1
3. Inverting Input 1
4. Non-Inverting Input 1
5. V⁻
6. Non-Inverting Input 2
7. Inverting Input 2
8. Strobe 2
9. Output
10. V⁺

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Note 1)

(Standard Conditions: $T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETERS	TEST CONDITIONS	MIN		TYP		MAX		UNITS
		μA711	711C	μA711	711C	μA711	711C	
Input Offset Voltage	$V_{out} = +1.4V$, $R_S \leq 200\Omega$, $V_{cm} = 0$			1.0	1.0	3.5	5.0	mV
	$V_{out} = +1.4V$, $R_S \leq 200\Omega$			1.0	1.0	5.0	7.5	mV
Input Offset Current	$V_{out} = +1.4V$			0.5	0.5	10.0	15.0	μA
Input Bias Current				25	25	75	100	μA
Voltage Gain		750	700	1500	1500			
Response Time	Note 2			40	40			ns
Strobe Release Time				12	12			ns
Input Common Mode Voltage Range	$V^- = -7.0V$	±5.0	±5.0					V
Differential Input Voltage Range		±5.0	±5.0					V
Output Resistance				200	200			Ω
Positive Output Level	$V_{in} \geq 10mV$			4.5	4.5	5.0	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10mV$, $I_o = 5mA$	2.5	2.5	3.5	3.5			
Negative Output Level	$V_{in} \geq 10mV$	-1.0	-1.0	-0.5	-0.5	0	0	V
Strobed Output Level	$V_{strobe} < 0.3V$	-1.0	-1.0			0	0	V
Output Sink Current	$V_{in} \geq 10mV$, $V_{out} \geq 0$	0.5	0.5	0.8	0.8			mA
Strobe Current	$V_{strobe} = 100mV$			1.2	1.2	2.5	2.5	mA
Positive Supply Current	$V_{out} \leq 0$			8.6	8.6			mA
Negative Supply Current				3.9	3.9			mA
Power Consumption				130	130	200	200	mW
The following specifications apply over the temperature ranges of: $-55°C \leq T_A \leq +125°C$ for the μA711 $0°C \leq T_A \leq +75°C$ for the μA711C								
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{cm} = 0$, Note 3					4.5	6.0	mV
	$R_S \leq 200\Omega$					6.0	10.0	mV
Input Offset Current	Note 3					20	25	μA
Input Bias Current						150	150	μA
Temperature Coefficient of Input Offset Voltage				5.0	5.0			μV/°C
Voltage Gain		500	500					

Recommended Operating Supply Voltages: $V^+ = 12V$, $V^- = -6V$

NOTES:

1. All voltages are referenced to pin 1.
2. The response time specified is for a 100mV input step, with a 5mV overdrive.
3. The Input Offset Voltage and Input Offset Current are specified for a logic threshold voltage of: 1.8V at 0°C.

μA711	μA711C
1.8V at 0°C	1.5V at 0°C
1.4V at +25°C	1.4V at +25°C
1.0V at +125°C	1.2V at +75°C

4. Rating applies for temperatures up to: μA711 — +125°C
   μA711C — +75°C

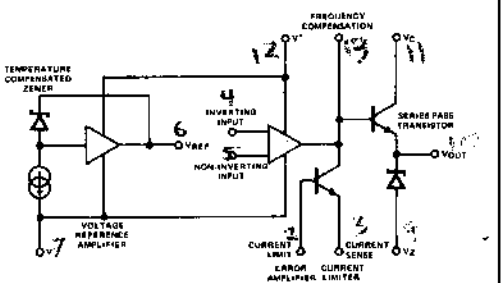
DESCRIPTION

The μA723 is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The μA723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

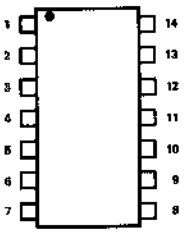
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- .01% LINE AND LOAD REGULATION
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR

EQUIVALENT CIRCUIT



PIN CONFIGURATION

A PACKAGE
(Top View)



1. NC
2. Current Limit
3. Current Sense
4. Inverting Input
5. Noninverting Input
6. V_{REF}
7. V^-
8. NC
9. V_z
10. V_{out}
11. V_c
12. V^+
13. Frequency Compensation
14. NC

ORDER PART NOS. μA723A/μA723CA

L PACKAGE

1. Current Sense
2. Inverting Input
3. Noninverting Input
4. V_{REF}
5. V^-
6. V_{out}
7. V_c
8. V^+
9. Frequency Compensation
10. Current Limit

ORDER PART NOS. μA723L/μA723CL

ABSOLUTE MAXIMUM RATINGS

	μA723	μA723C
Pulse Voltage from V^+ to V^- (50ms)	50V	
Continuous Voltage from V^+ to V^-	40V	40V
Input-Output Voltage Differential	40V	40V
Maximum Output Current	150mA	150mA
Current from V_{REF}	15mA	
Current from V_z		25mA
Internal Power Dissipation (Note 1)	800mW	800mW
Operating Temperature Range	−55 to +125°C	0 to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature	300°C	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified — Note 1)

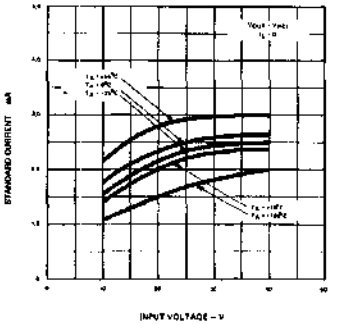
PARAMETER (See definitions)	MIN	TYP	MAX	UNITS	CONDITIONS
μA723C					
Line Regulation (Note 2)		0.01	0.1	% V_{out}	V_{in} = 12V to V_{in} = 15V
		0.1	0.5	% V_{out}	V_{in} = 12V to V_{in} = 40V
Load Regulation (Note 2)		0.03	0.2	% V_{out}	I_L = 1mA to I_L = 50mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5μF
Short Circuit Current Limit		65		mA	R_{sc} = 10Ω, V_{out} = 0
Reference Voltage	6.80	7.15	7.50	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 5μF
Long Term Stability		0.1	0.1	%/1000 hrs.	
Standby Current Drain		2.3	4.0	mA	I_L = 0, V_{in} = 30V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation			0.3	% V_{out}	
Load Regulation			0.6	% V_{out}	
Average Temperature Coefficient of Output Voltage		0.003	0.015	%/°C	V_{in} = 12V to V_{in} = 15V, I_L = 1mA to I_L = 50mA
μA723					
Line Regulation (Note 2)		0.01	0.1	%V_{out}	V_{in} = 12V to V_{in} = 15V
		0.02	0.2	%V_{out}	V_{in} = 12V to V_{in} = 40V
Load Regulation (Note 2)		0.03	0.15	%V_{out}	I_L = 1mA to I_L = 50mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5μF
Short Circuit Current Limit		65		mA	R_{SC} = 10Ω, V_{out} = 0
Reference Voltage	6.95	7.15	7.35	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 5μF
Long Term Stability		0.1		%/1000 hrs	
Standby Current Drain		2.3	3.5	mA	I_L = 0, V_{in} = 30V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation			0.3	% V_{out}	
Load Regulation			0.6	% V_{out}	
Average Temperature Coefficient of Output Voltage		0.002	0.015	%/°C	V_{in} = 12V to V_{in} = 15V, I_L = 1mA to I_L = 50mA

NOTES

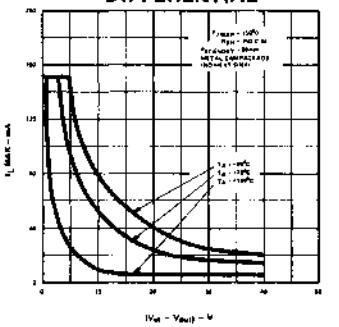
1. Unless otherwise specified, T_A = 25°C, V_{in} = V+ = V_c = 12V, V− = 0V, V_{out} = 5V, I_L = 1mA, R_{sc} = 0, C_1 = 100pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10kΩ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL CHARACTERISTIC CURVES

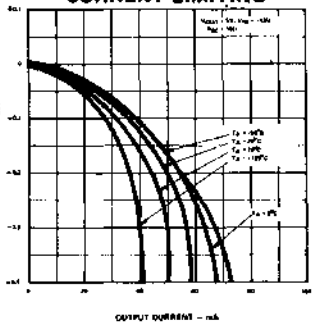
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



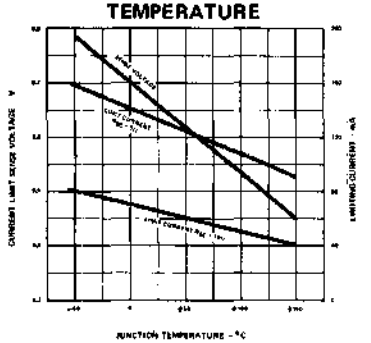
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



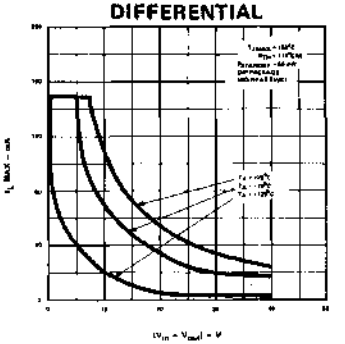
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



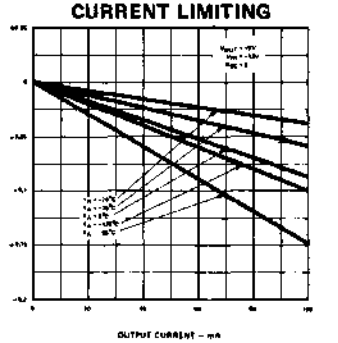
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



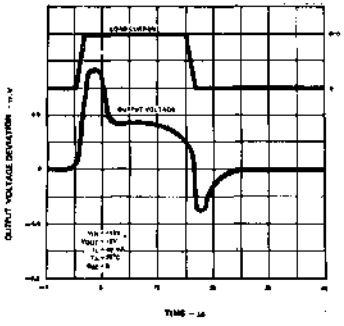
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



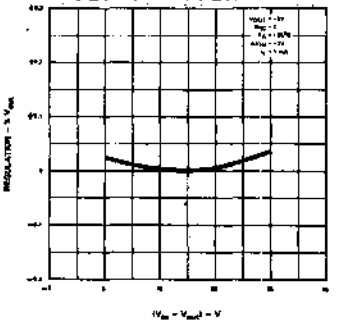
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



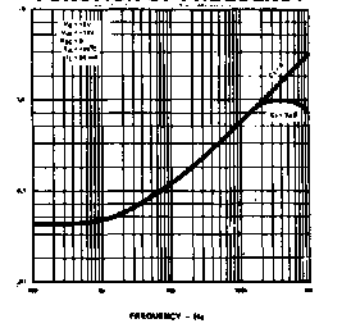
LOAD TRANSIENT RESPONSE



LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

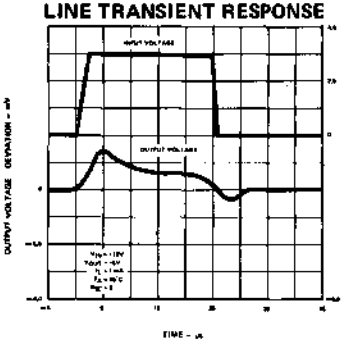


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

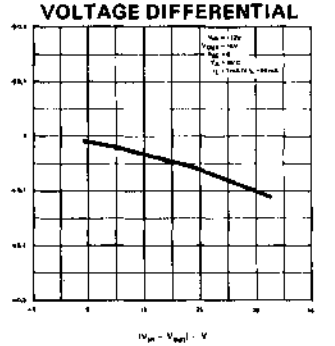


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

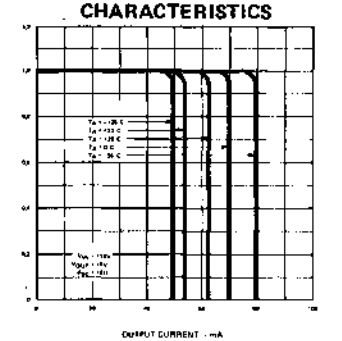
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

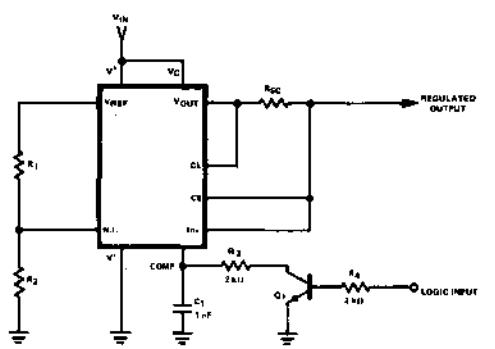


CURRENT LIMITING CHARACTERISTICS



BASIC μA723 REGULATOR APPLICATIONS

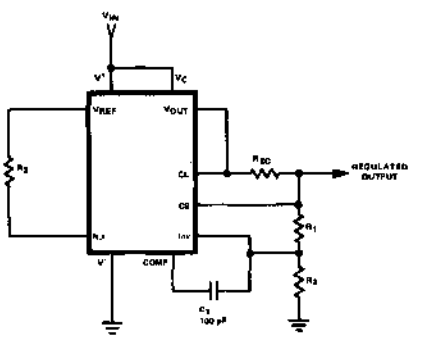
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{out} = 2 to 7 Volts)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

FIGURE 1

HIGH VOLTAGE REGULATOR (V_{out} = 7 to 37 Volts)



$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2} \right]$$

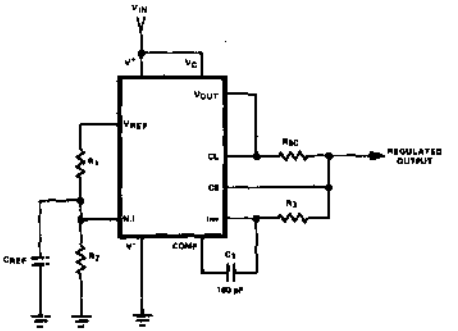
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

R_3 may be eliminated for minimum component count

FIGURE 2

BASIC μA723 REGULATOR APPLICATIONS (Cont'd.)

LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

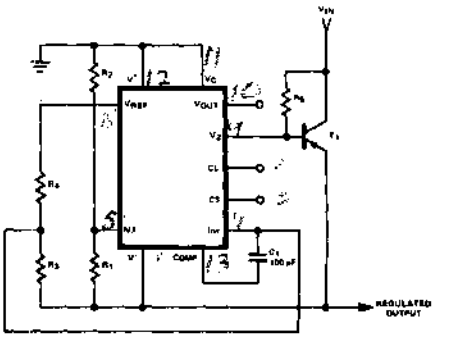


$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

$$R_3 = \frac{R_1 R_2}{R_2 + R_2} \quad \text{for minimum temperature drift}$$

FIGURE 3

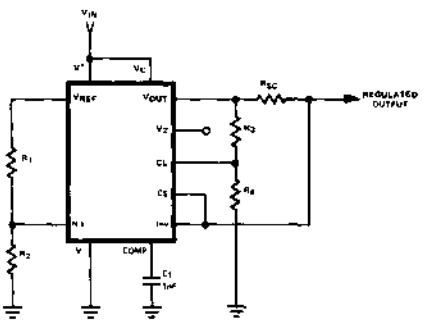
NEGATIVE VOLTAGE REGULATOR

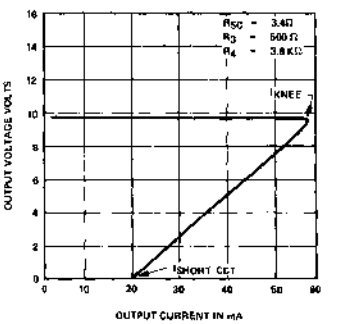


$$V_{out} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right] \quad ; R_3 = R_4$$

FIGURE 4

FOLDBACK CURRENT LIMITING REGULATOR
(V_{out} = 2 to 7 Volts)





$$I_{KNEE} = \left[\frac{V_{out} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}\right]$$

$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT}\, I_{SC}}{V_{SENSE}(I_{KNEE} - I_{SHORTCCT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

FIGURE 5

DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

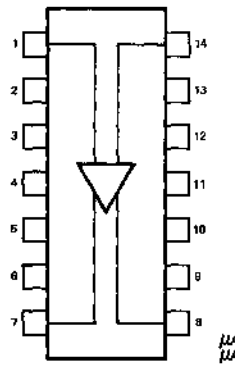
- **120 MHz BANDWIDTH**
- **250kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10,100 and 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10mA
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Operation Temperature Range	
μA733C	0°C to +75°C
μA733	-55°C to +75°C

PIN CONFIGURATIONS

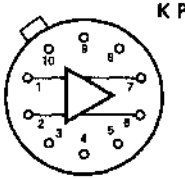
A & I PACKAGE



1. Input 2
2. NC
3. G_{2B} Gain Select
4. G_{1B} Gain Select
5. V^-
6. NC
7. Output 2
8. Output 1
9. NC
10. V^+
11. G_{1A} Gain Select
12. G_{2A} Gain Select
13. NC
14. Input 1

ORDER PART NOS.
μA733A/ μA733CA/ μA733I / μA733CI

K PACKAGE



NOTE: Pin 5 connected to case.

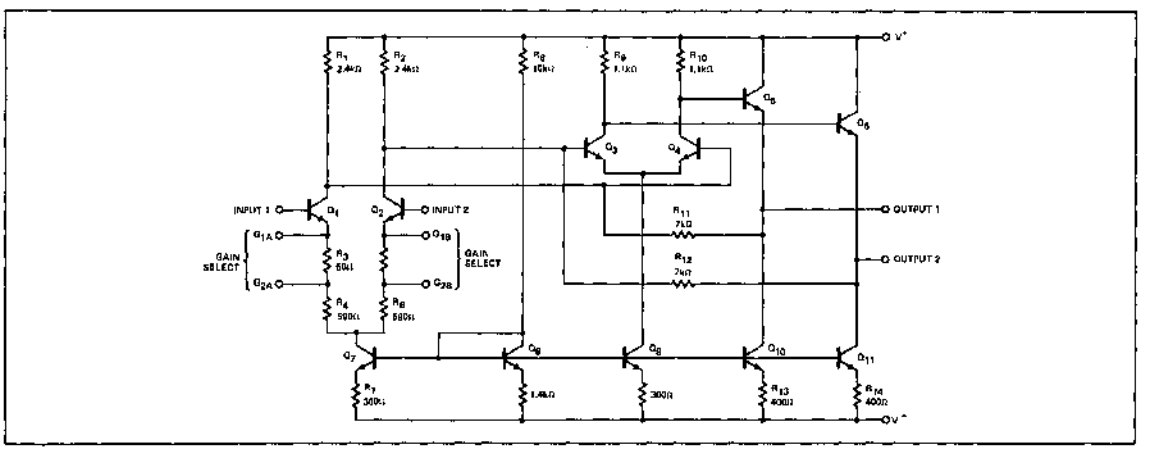
ORDER PART NOS.
μA733K/μA733CK

1. Input 1
2. Input 2
3. G_{2B} Gain Select
4. G_{1B} Gain Select
5. V^-
6. Output 2
7. Output 1
8. V^+
9. G_{1A} Gain Select
10. G_{2A} Gain Select

Thermal Resistance (θ_{J-A}, Junction to Ambient for each package):

A Package	0.16°C/mW
I Package	0.10°C/mW
K Package	0.145°C/mW
Power Dissipation	500mW

SCHEMATIC CIRCUIT SCHEMATIC



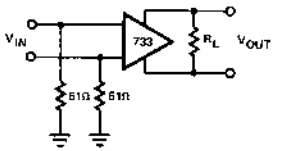
ELECTRICAL CHARACTERISTICS Standard Conditions (T_A = +25°C, V_S = ±V, V_{CM} = 0 unless otherwise specified)

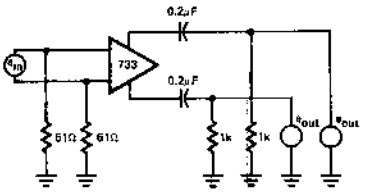
PARAMETERS	TEST CONDITIONS		μA733C			μA733			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain									
Gain 1		Note 1	250	400	600	300	400	500	
Gain 2	R_l = 2kΩ, V_{out} = $3V_{p-p}$	Note 2	80	100	120	90	100	110	
Gain 3		Note 3	8.0	10	12	9.0	10	11	
Bandwidth									
Gain 1		Note 1		40			40		MHz
Gain 2		Note 2		90			90		MHz
Gain 3		Note 3		120			120		MHz
Rise Time									
Gain 1		Note 1		10.5			10.5		ns
Gain 2	V_{out} = $1V_{p-p}$	Note 2		4.5	12		4.5	10	ns
Gain 3		Note 3		2.5			2.5		ns
Propagation Delay									
Gain 1		Note 1		7.5			7.5		ns
Gain 2	V_{out} = $1V_{p-p}$	Note 2		6.0	10		6.0	10	ns
Gain 3		Note 3		3.6			3.6		ns
Input Resistance									
Gain 1		Note 1		4.0			4.0		kΩ
Gain 2		Note 2	10	30		20	30		kΩ
Gain 3		Note 3		250			250		kΩ
Input Capacitance	Gain 2	Note 2		2.0			2.0		pF
Input Offset Current				0.4	5.0		0.4	3.0	μA
Input Bias Current				9.0	30		9.0	20	μA
Input Noise Voltage	BW = 1 kHz to 10 MHz			12			12		μV_{rms}
Input Voltage Range			±1.0			±1.0			V
Common Mode Rejection Ratio									
Gain 2	V_{CM} = ±1V, f ≤ 100 kHz		60	86		60	86		dB
Gain 2	V_{CM} = ±1V, F = 5 MHz			60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	ΔV_S = ±0.5V		50	70		50	70		dB
Output Offset Voltage									
Gain 1	R_L = ∞	Note 1		0.6	1.5		0.6	1.5	V
Gain 2 and 3		Notes 2,3		0.35	1.5		0.35	1.0	V
Output Common Mode Voltage	R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	R_L = 2k		3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	R_L = ∞			18	24		18	24	mA

Recommended Operating Supply Voltages (V_S = ±6.0V)

NOTES
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

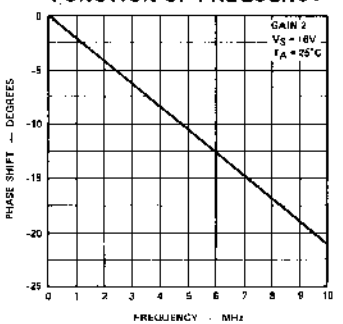
TEST CIRCUITS (T_A = 25°C unless otherwise specified)



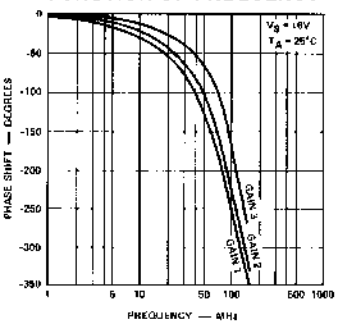


TYPICAL CHARACTERISTIC CURVES

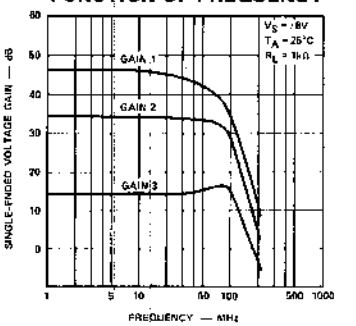
PHASE SHIFT AS A FUNCTION OF FREQUENCY



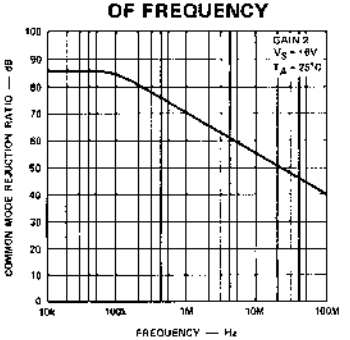
PHASE SHIFT AS A FUNCTION OF FREQUENCY



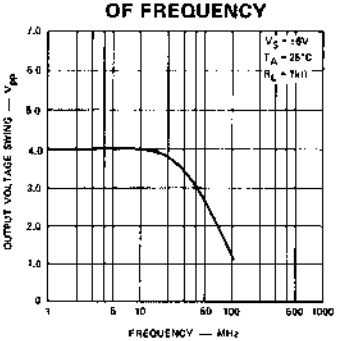
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



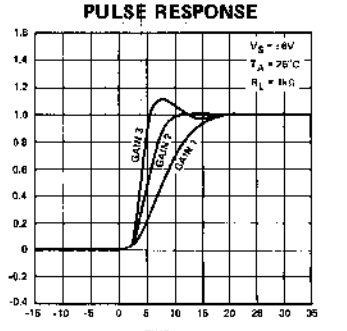
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

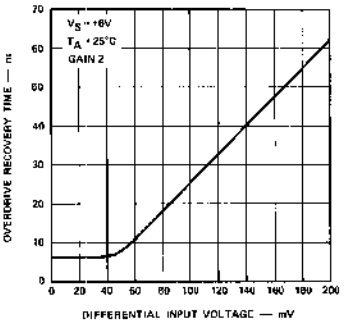


PULSE RESPONSE

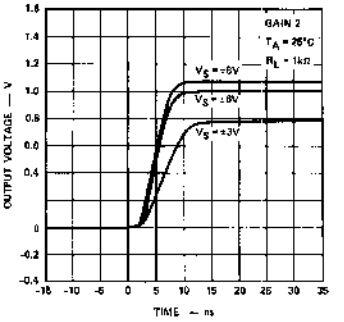


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

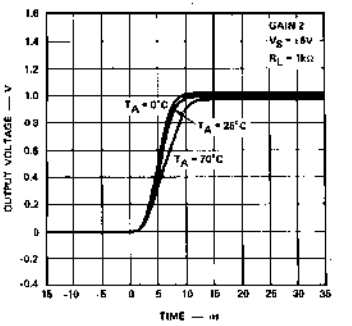
DIFFERENTIAL OVERDRIVE RECOVERY TIME



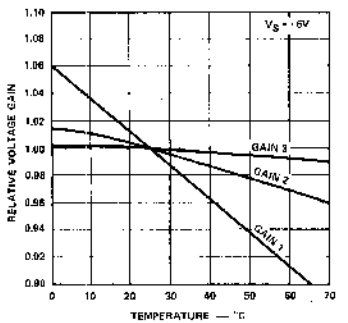
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



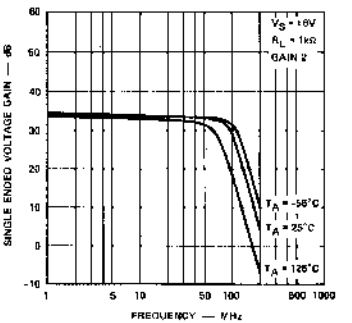
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



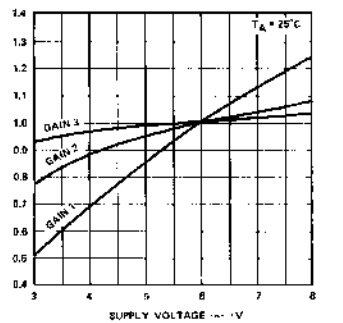
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



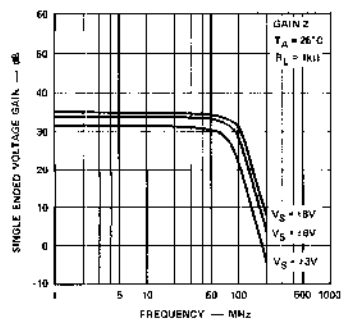
GAIN VS FREQUENCY AS A FUNCTION OF TEMPERATURE



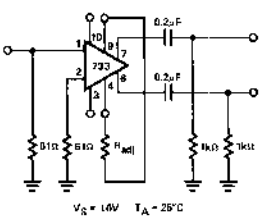
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN VS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



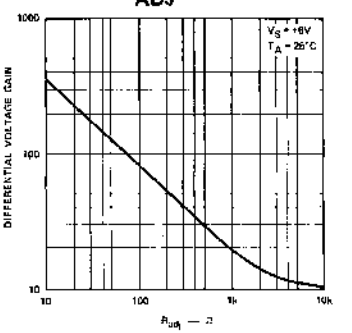
VOLTAGE GAIN ADJUST CIRCUIT



(Pin numbers apply to K Package)

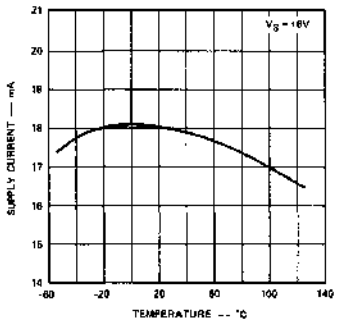
FIGURE 3

VOLTAGE GAIN AS A FUNCTION OF R_{ADJ} (FIGURE 3)

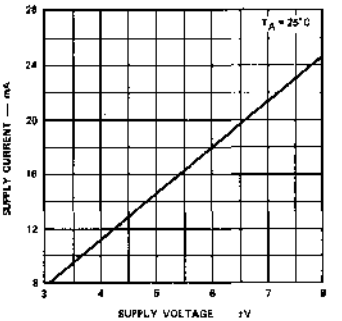


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

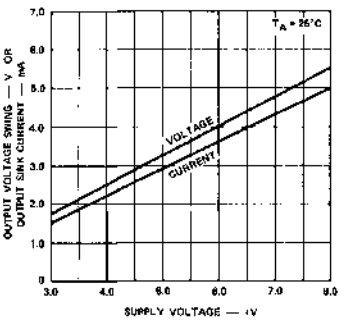
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



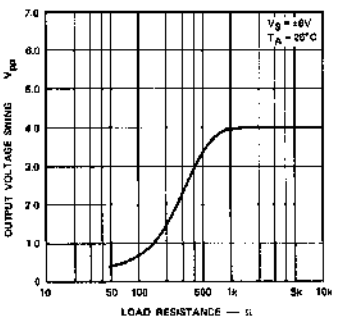
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



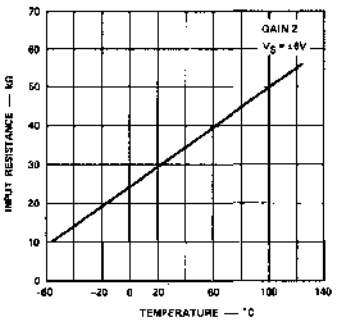
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



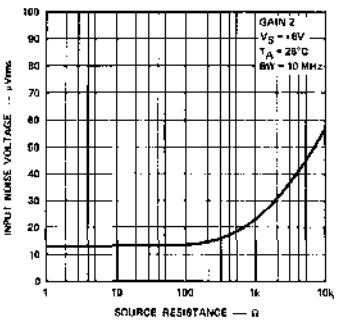
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



DESCRIPTION

The μA740 is a special purpose high performance operational amplifier utilizing a FET input stage for high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

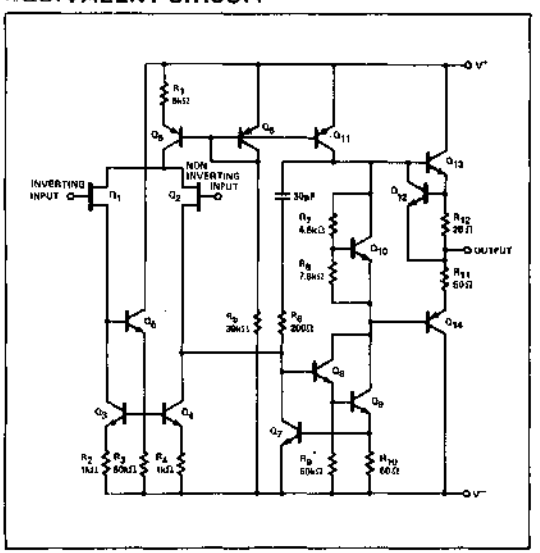
- **0.1 nA INPUT BIAS CURRENT**
- **INPUT AND OUTPUT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **INTERNALLY COMPENSATED**
- **6V/μsec SLEW RATE**
- **STANDARD PINOUT**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATING

Supply Voltage	±22V
Differential Input Voltage Range	±30V
Common Mode Input Voltage Range	$\pm V_S$
Power Dissipation (Note 1)	500mW
Operating Temperature Range	0°C to +70° C
Storage Temperature Range	−65°C to +150° C
Lead Temperature (Solder, 60 sec)	300° C
Output short Circuit Duration (Note 2)	Indefinite

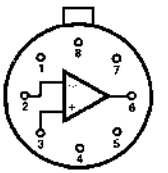
1. Rating applies for case temperatures to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

EQUIVALENT CIRCUIT



PIN CONFIGURATION (Top View)

T PACKAGE

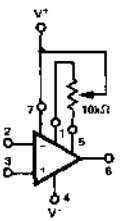


1. Offset Null
2. Inverting Input
3. Non-Inverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

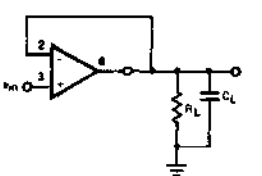
ORDER PART NOS. μA740T/μA740CT

TEST CIRCUITS

OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER CIRCUIT

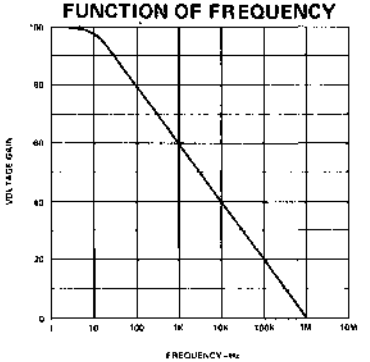


ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_C = 25°C unless otherwise specified)

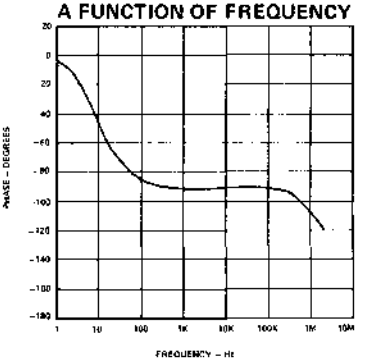
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		30		mV
Input Offset Current			60		pA
Input Current (either input)			0.1	2.0	nA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$kΩ, V_{out} = ±10V		1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Supply Current			4.2	3.0	mA
Power Consumption			126	240	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, R_L = 2 kΩ, V_{in} = 100 mV				
Risetime			300		ns
Overshoot			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Voltage Range			±12		V
Common Mode Rejection Ratio			80		db
Supply Voltage Rejection Ratio			70		μV/V
Large Signal Voltage Gain			500,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Offset Voltage			30		mV
Input Offset Current			60		pA
Input Current (either input)			1.1	10	nA

TYPICAL CHARACTERISTIC CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



signetics

HIGH PERFORMANCE OPERATIONAL AMPLIFIER | μA741

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- INTERNAL FREQUENCY COMPENSATION
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- EXCELLENT TEMPERATURE STABILITY
- HIGH INPUT VOLTAGE RANGE
- NO LATCH-UP

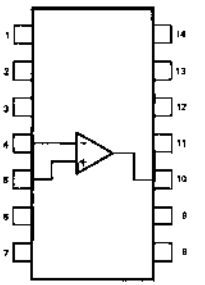
ABSOLUTE MAXIMUM RATINGS

	μA741C	μA741
Supply Voltage	±18V	±22V
Internal Power Dissipation (Note 1)	500mW	500mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Voltage between Offset Null and V⁻	±0.5V	±0.5V
Operating Temperature Range	0°C to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Solder, 60 sec)	300°C	300°C
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite

Notes
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATIONS

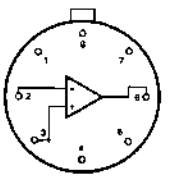
A PACKAGE
(Top View)



1. NC
2. NC
3. Offset Null
4. Inv. Input
5. Non-Inv. Input
6. V⁻
7. NC
8. NC
9. Offset Null
10. Output
11. V⁺
12. NC
13. NC
14. NC

ORDER PART NO. μA741CA

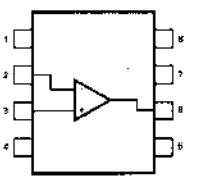
T PACKAGE



1. Offset Null
2. Inverting Input
3. Non-Inverting Input
4. V⁻
5. Offset Null
6. Output
7. V⁺
8. NC

ORDER PART NOS. μA741T/μA741CT

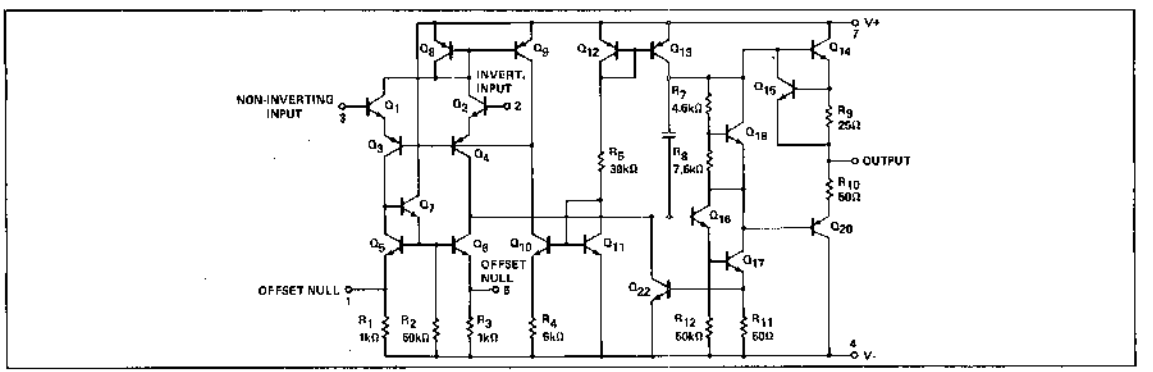
V PACKAGE



1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V⁻
5. Offset Null
6. Output
7. V⁺
8. NC

ORDER PART NO. μA741CV

EQUIVALENT CIRCUIT

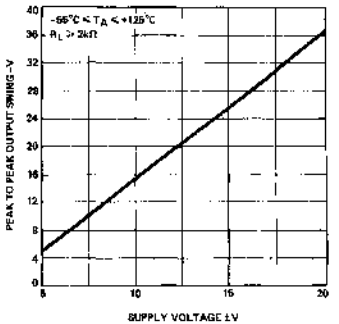


ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

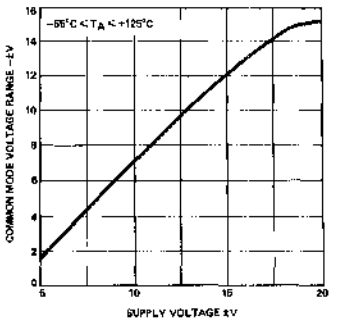
PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
μA741C					
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		20	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		MΩ	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		±15		mV	
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		10	150	μV/V	$R_S \leq 10k\Omega$
Large-Signal Voltage Gain	20,000	200,000			$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Output Resistance		75		Ω	
Output Short-Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					V_{in} = 20mV, R_L = 2kΩ, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Offset Voltage			7.5	mV	
Input Offset Current			300	nA	
Input Bias Current			800	nA	
Large-Signal Voltage Gain	15,000				$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Voltage Swing	±10	±13		V	$R_L \geq 2k\Omega$
μA741					
Input Offset Voltage		1.0	5.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		10	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		MΩ	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		±15		mV	
Large-Signal Voltage Gain	50,000	200,000			$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Resistance		75		Ω	
Output Short Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					V_{in} = 20mV, R_L = 2kΩ, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Input Offset Voltage		1.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		7.0	200	nA	T_A = +125°C
		20	500	nA	T_A = −55°C
Input Bias Current		0.03	0.5	μA	T_A = +125°C
		0.3	1.5	μA	T_A = −55°C
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Refection Ratio		10	150	μV/V	$R_S \leq 10k\Omega$
Large-Signal Voltage Gain	25,000				$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Supply Current		1.5	2.5	mA	T_A = +125°C
		2.0	3.3	mA	T_A = −55°C
Power Consumption		45	75	mW	T_A = +125°C
		45	100	mW	T_A = −55°C

TYPICAL CHARACTERISTIC CURVES

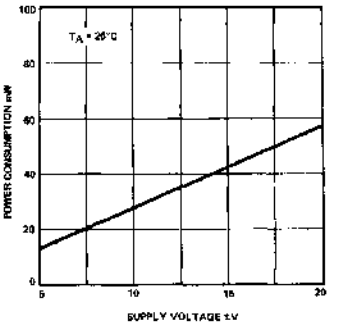
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



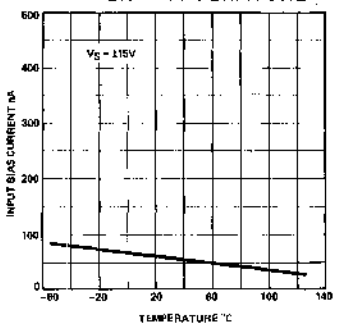
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



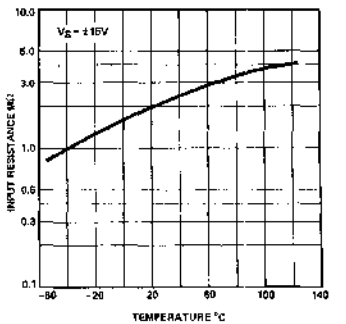
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



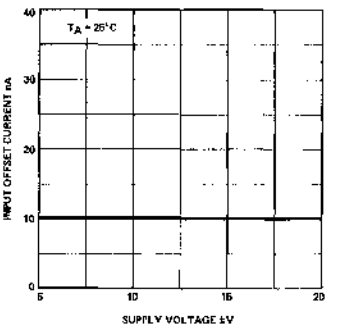
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



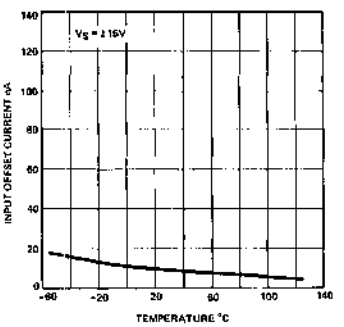
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



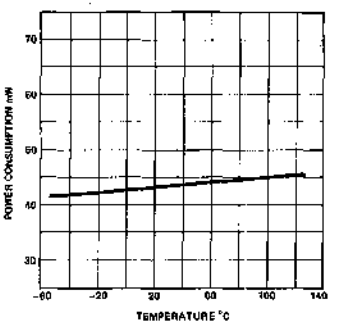
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



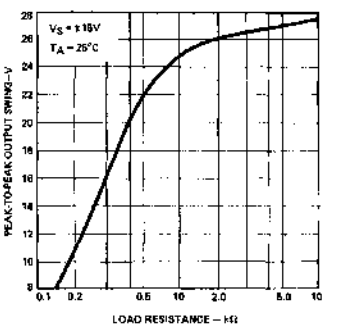
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

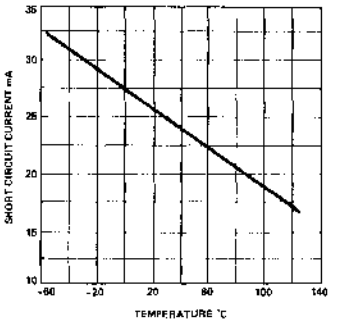


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

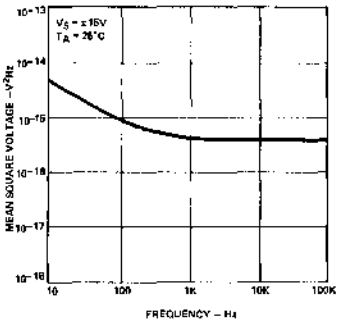


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

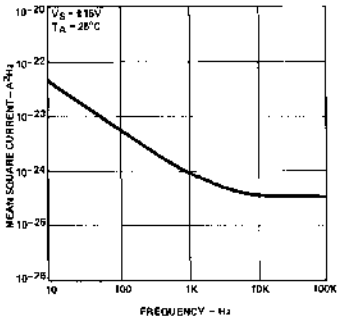
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



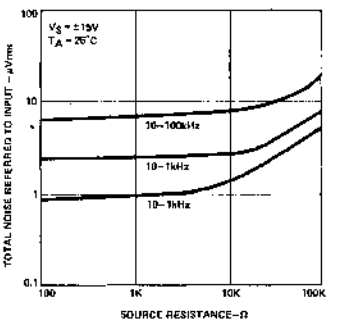
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



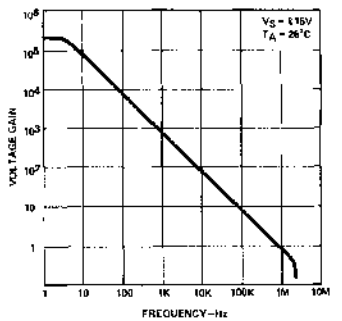
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



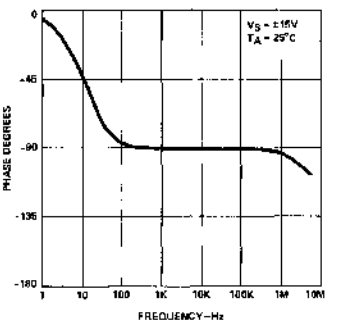
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



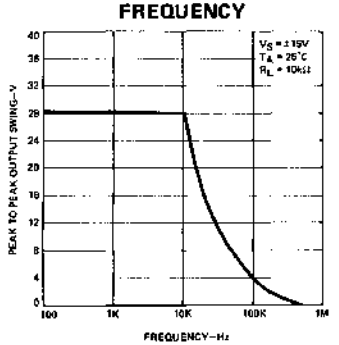
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



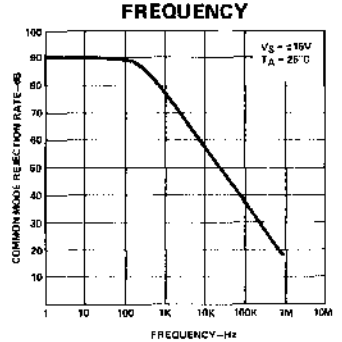
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



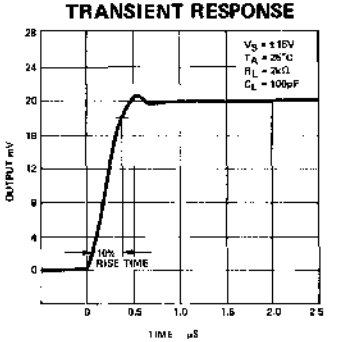
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



DESCRIPTION

The μA747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6 db/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

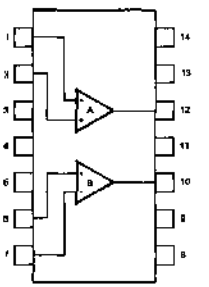
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage μA747		+22V
μA747C		+18V
Internal Power Dissipation (Note 1)	Metal Can	500 mW
	DIP	670 mW
Differential Input Voltage		+30V
Input Voltage (Note 2)		+15V
Voltage between Offset Null and V^-		+0.5V
Storage Temperature Range		-65°C to +155°C
Operating Temperature Range μA747		-55°C to +125°C
μA747C		0°C to +70°C
Lead Temperature (Soldering 60 seconds)		300°C
Output Short Circuit Duration (Note 3)		Indefinite

PIN CONFIGURATION

A PACKAGE
(Top View)



1. Inv Input A
2. Non-Inv Input A
3. Offset Null A
4. V^-
5. Offset Null B
6. Non-Inv Input B
7. Inv Input B
8. Offset Null B
9. V+ B
10. Output B
11. No Connect
12. Output A
13. V+ A
14. Offset Null A

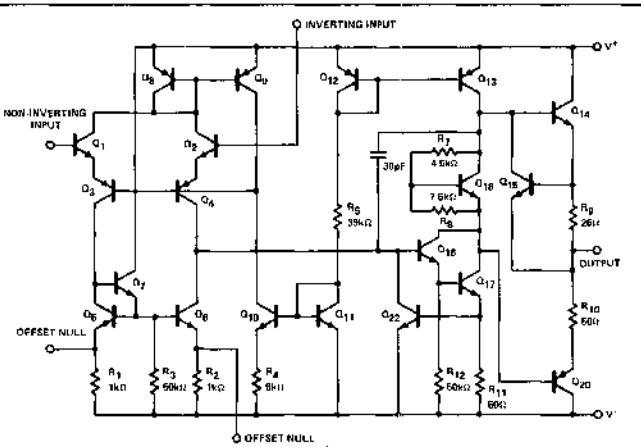
ORDER PART NOS.
μA747A
μA747CA

K PACKAGE

1. Output A
2. V^+ A
3. Inverting Input A
4. Non-Inverting Input A
5. V^-
6. Non-Inverting Input B
7. Inverting Input B
8. V^+B
9. Output B
10. NC

ORDER PART NOS.
μA747K
μA747CK

EQUIVALENT CIRCUIT (Each Side)



ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

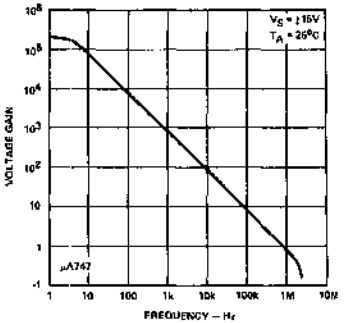
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0		mV
μA747			5.0		mV
μA747C			6.0		mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2K\Omega, V_{out} = \pm 10V$		200,000		
μA747		50,000			
μA747C		25,000			
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	V_{in} = 20 mV, R_L = 2kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μS
Overshoot			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		0.5		V/μS
Channel Separation			120		dB
μA747					
The following specifications apply for $-65^\circ C \leq T_A \leq +125^\circ C$					
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	6.0	mV
Input Offset Current	$T_A = +125^\circ C$		7.0	200	nA
	$T_A = -55^\circ C$		85	500	nA
Input Bias Current	$T_A = +125^\circ C$		0.03	0.5	μA
	$T_A = -55^\circ C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2k\Omega, V_{out} = \pm 10V$	25,000			
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		V
Supply Current	$T_A = +125^\circ C$		1.5	2.5	mA
	$T_A = -55^\circ C$		2.0	3.3	mA
Power Consumption	$T_A = +125^\circ C$		45	75	mW
	$T_A = -55^\circ C$		60	100	mW
μA747C					
The following specifications apply for $0^\circ C \leq T_A \leq +70^\circ C$					
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2k\Omega, V_{out} = \pm 10V$	15,000			
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

NOTES:

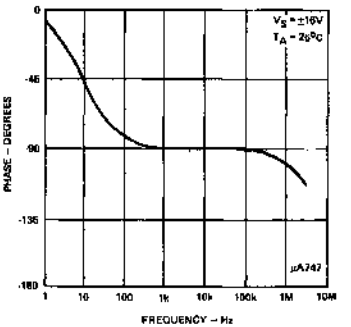
1. Rating applied to ambient temperatures up to 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can and 8.3 mW/°C for the Ceramic DIP package.
2. For supply voltages less than +15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Military rating applies to +125°C case temperature or +60°C ambient temperature for each side.

TYPICAL CHARACTERISTIC CURVES

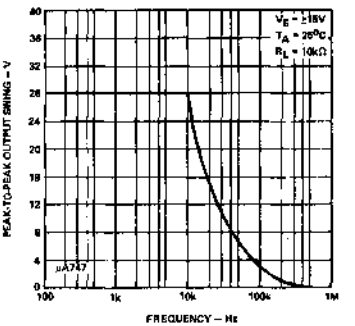
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



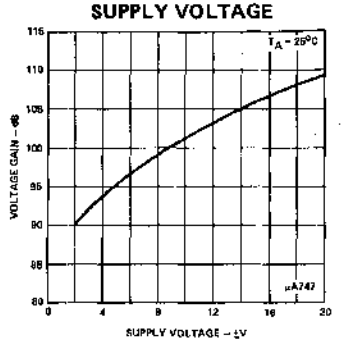
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



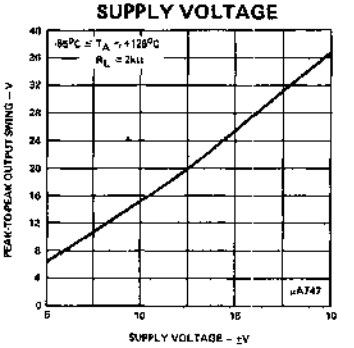
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



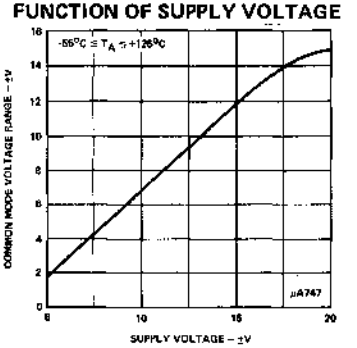
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



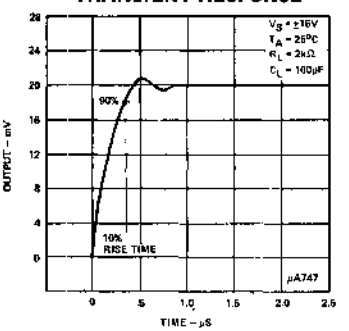
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



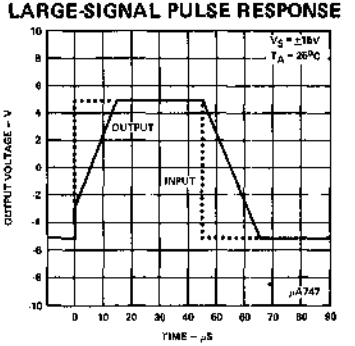
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



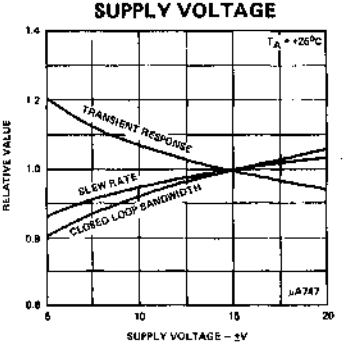
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

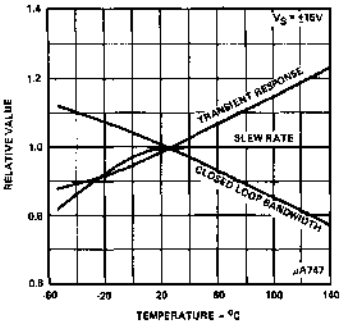


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

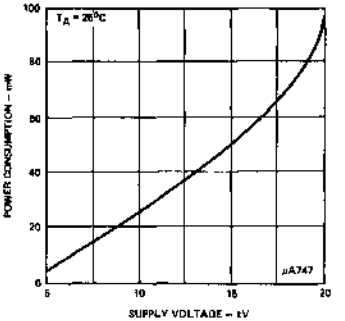


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

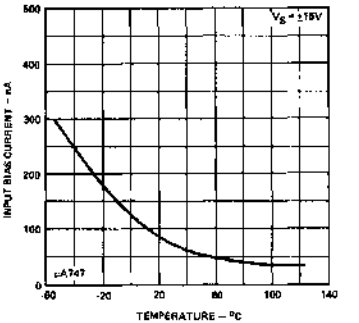
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



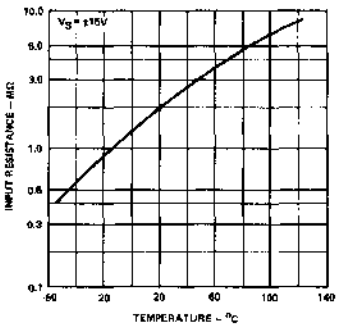
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



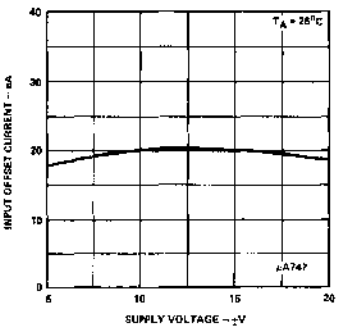
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



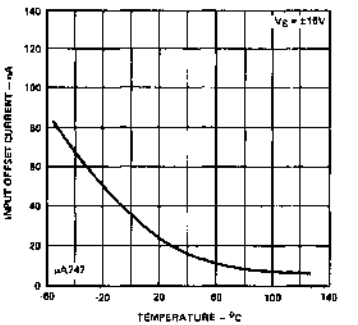
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



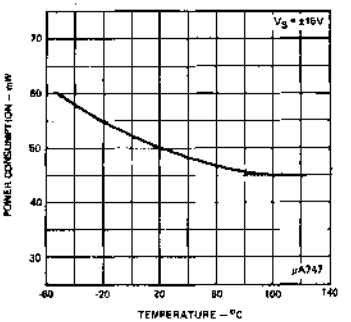
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



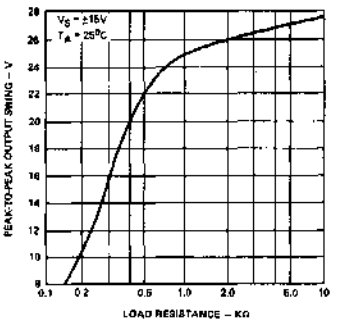
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



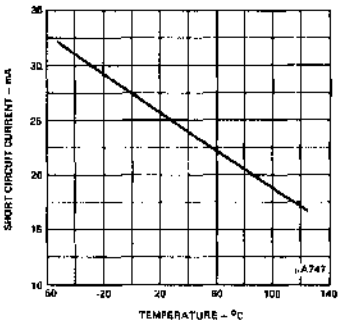
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

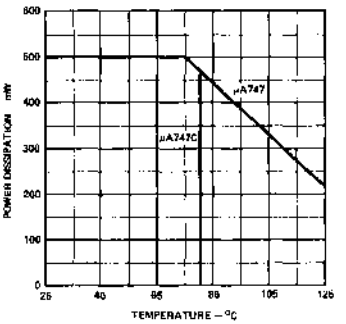


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

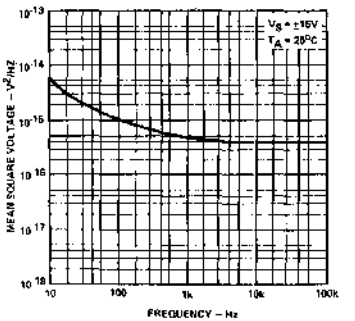


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

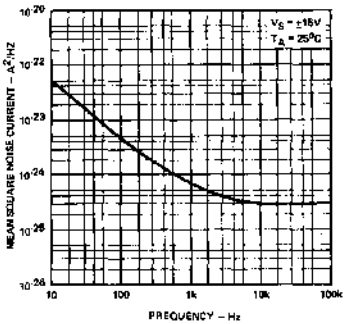
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION AMBIENT TEMPERATURE



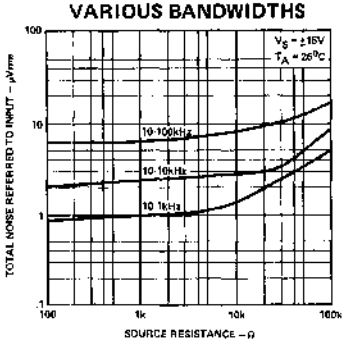
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



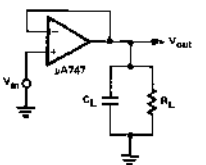
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



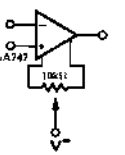
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



DESCRIPTION

The μA748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

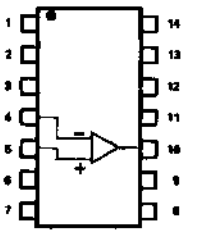
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA748	±22V
μA748C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
μA748	−55°C to +125°C
μA748C	0°C to +70°C
Lead Temperature	300°C
Output Short Circuit Duration (Note 3)	Indefinite

PIN CONFIGURATIONS

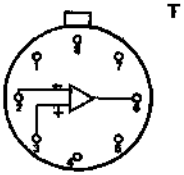
A PACKAGE
(Top View)



ORDER PART NOS.
μA748A/μA748CA

1. NC
2. NC
3. Freq. Comp. A/Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq. Comp. B
13. NC
14. NC

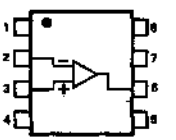
T PACKAGE



ORDER PART NOS.
μA748T/μA748CT

1. Freq. Comp A/Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp. B

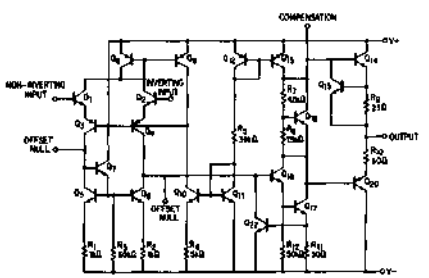
V PACKAGE



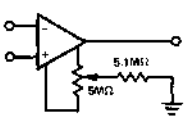
ORDER PART NO.
μA748CV

1. Freq. Comp. A/ Offset Null.
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp. B

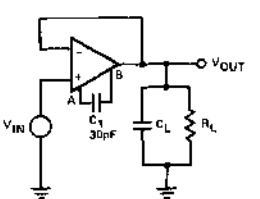
EQUIVALENT CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



NOTES:

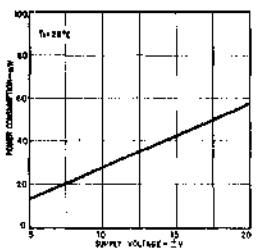
1. Rating applies for case temperatures to +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

ELECTRICAL CHARACTERISTICS: (V_S = ±15V, T_A = 25°C unless otherwise specified)

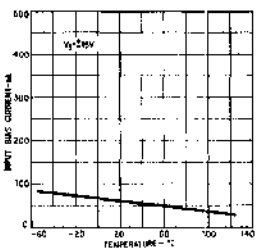
PARAMETER	CONDITIONS	μA748C			μA748			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{out} = ±10V	50K	200K		50K	200K		
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{in} = 20mV, R_L = 2 kΩ, $C_L \leq 100$ pF							
Risetime	C_1 = 30 pF		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2\ k\Omega$ C_1 = 30pF		0.5			0.5		V/μs
The Following Specifications Apply Over the Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			7.5			6.0	mV
Input Offset Current	T_A max		9.0	300		7.0	200	nA
	T_A min		35	300		85	500	nA
Input Bias Current	T_A max		0.04	0.8		0.03	0.5	μA
	T_A min		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{out} = ±10V	25			25			V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Supply Current	T_A max		1.6	3.3		1.5	2.5	mA
	T_A min		1.8	3.3		2.0	3.3	mA
Power Consumption	T_A max		48	100		45	75	mW
	T_A min		54	100		60	100	mW

TYPICAL CHARACTERISTIC CURVES

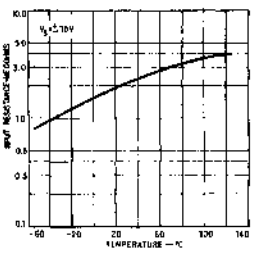
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

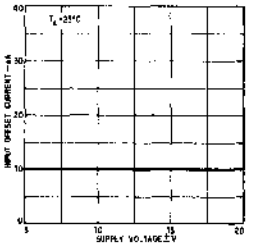


INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

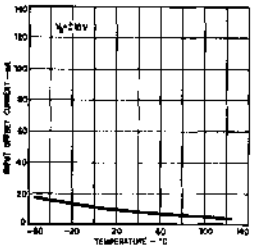


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

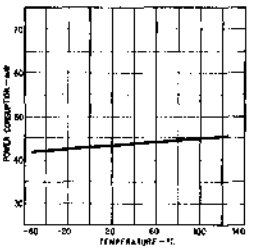
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



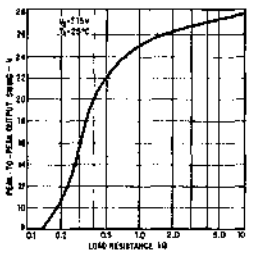
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



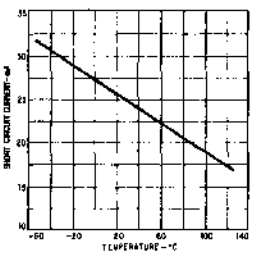
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



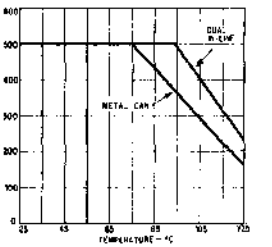
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



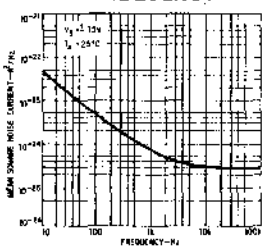
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



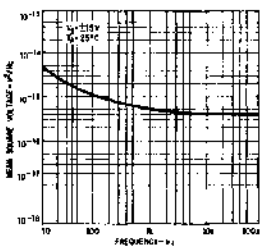
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



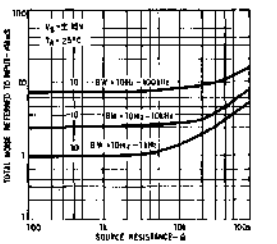
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



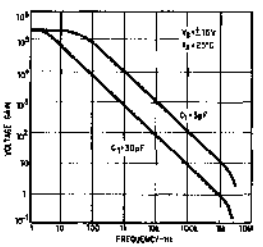
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



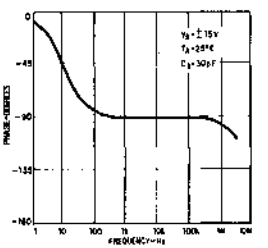
BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



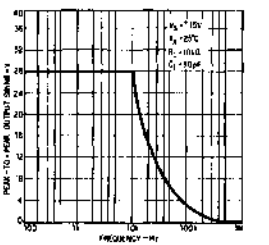
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

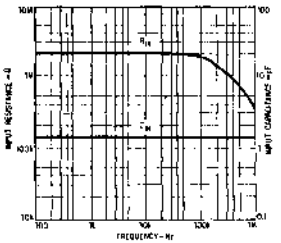


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

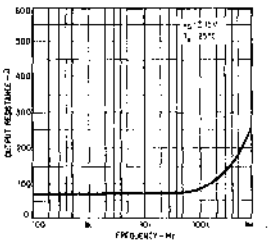


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

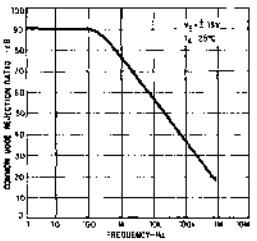
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



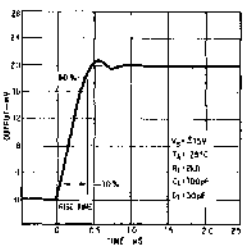
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



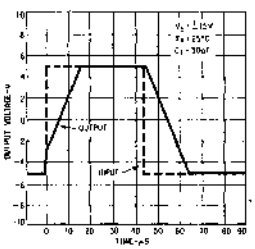
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



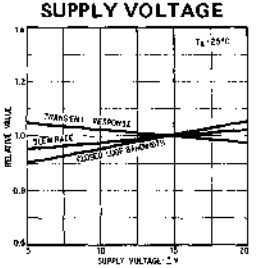
TRANSIENT RESPONSE



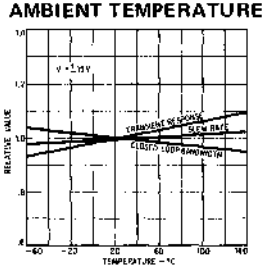
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



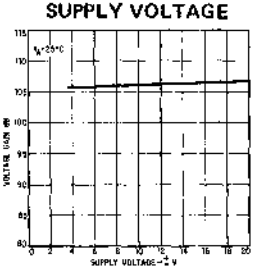
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



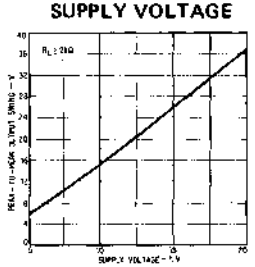
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



DESCRIPTION

A unique method of FM detection by a new technique of linear gating is featured in the ULN2111 monolithic integrated circuit. This linear device comprises a three-stage limiter and a balanced product detector. Applications for the ULN2111 device include TV sound channels, FM receivers, automatic frequency control systems, and communication receivers.

Other applications for the ULN2111 device are in the more sophisticated circuitry in telemetry receivers, automatic control systems, and servo amplifiers.

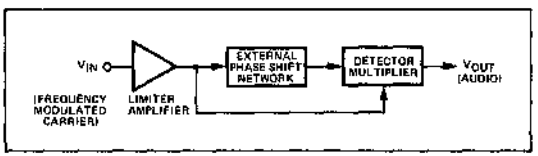
An outstanding feature of the ULN2111 is that only one, simple, low-cost, single winding coil is required for tuning. Consequently, only one screwdriver adjustment is required to tune a detector employing the ULN2111. The frequency range of the ULN2111 extends from 5 kHz to 50 MHz.

Outputs of 0.6V with a total distortion of less than 1% and a limiting threshold voltage of 400μV_{rms} are typical.

FEATURES

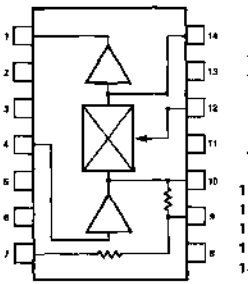
- **HIGH SENSITIVITY – INPUT LIMITING VOLTAGE AT 4.5MHz = 400μV**
- **HIGH IF VOLTAGE GAIN – 60dB**
- **SIMPLIFIED TUNING – ONE RLC PHASE SHIFT NETWORK**
- **HIGH STABILITY**
- **LOW DISTORTION – 1.0%**
- **WIDE FREQUENCY CAPABILITY – 5kHz to 50MHz**

BLOCK DIAGRAM



PIN CONFIGURATION

A PACKAGE
(Top View)



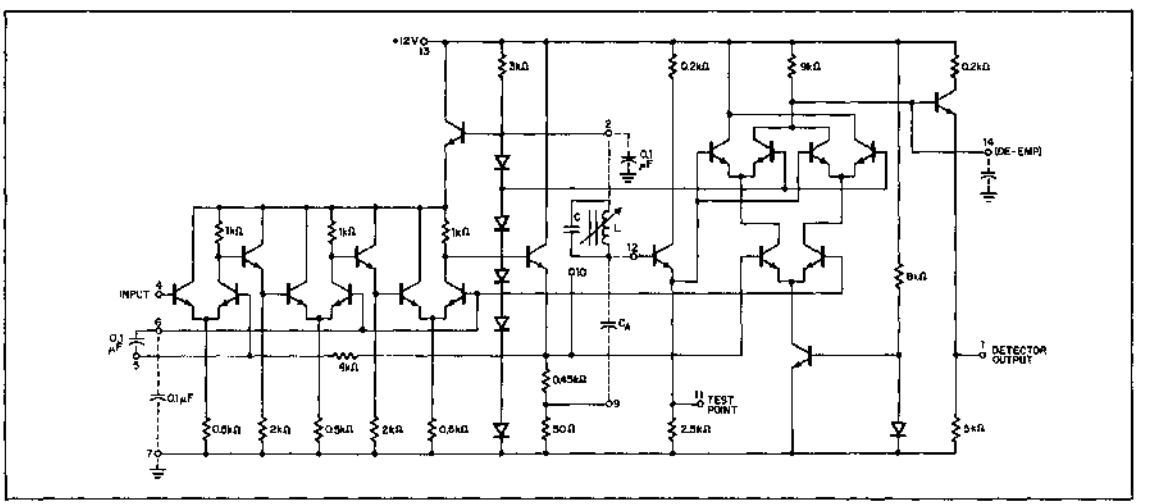
1. Audio Output
2. Detector Input Reference
3. No Connection
4. Input
5. Decoupling
6. Amplifier Input Reference
7. GND
8. No Connection
9. Amplifier Low Output
10. Amplifier High Output
11. Test Point
12. Detector Input
13. V^+
14. De-emphasis

ORDER PART NO. ULN2111A

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Pin 4)	+3.5V
Output Voltage	+15V
Supply Voltage (V+)	+15V
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Operating Temperature	0°C to +85°C
Thermal Resistance	0.15°C/mW
$\theta_{J\text{-}A}$, Junction to Ambient	
Power Dissipation	300mW

SIMPLIFIED CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS: Standard Conditions: V_{CC} = +12V ±10%, T_A = 25°C

CHARACTERISTICS	SYMBOL	LIMITS				TEST CONDITIONS		TEST FIGURE	NOTES
		MIN	TYP	MAX	UNITS		Pin		
Supply Current	I_{CC}	12.0	17	22	mA		13		
Amplifier Input Reference	V_{bias}		1.45		V	Internally derived	6		
Detector Input Reference	V_{bias}		3.65		V	Internally derived	2		
Amplifier High Output Level	V_{oh}		1.45		V		10		
Amplifier Low Output Level	V_{ol}		0.145		V		9		
Detector Output Level	V_o	4.3	5.0	5.7	V		1		
Amplifier Input Resistance	R_{in}		5.0		KΩ		4		
Amplifier Input Capacitance	C_{in}		11		pF		4		
Detector Injection Input Resistance	R_{in}		70		KΩ		12		
Detector Injection Input Capacitance	C_{in}		2.7		pF		12		
Amplifier High Output Resistance	R_{out}		60		Ω		10		
Detector Output Resistance	R_{out}		200		Ω		1		
De-Emphasis Resistance	R_{de}		9		KΩ		14		
FM Detection for Television Applications:						Detector injection voltage = 60mV$_{rms}$, f_o = 4.5 MHz, F deviation = 25 kHz, Peak separation = 150 kHz, FM modulating frequency = 400 Hz, Amplifier source resistance = 50Ω.			
Amplifier Voltage Gain	V_g	55	58		dB	$V_{in} \leq$ 0.3mV$_{rms}$, V_{cc} = 12V ±5%	10	1	
Amplifier Output Voltage	V_{oa}		1.45		V_{pp}	V_{in} = 10mV$_{rms}$	10	1	
Input Limiting Threshold	V_{th}		400	800	μV_{rms}		4	2	1
Recovered Audio Output	A_{vo}	0.5	0.6		V_{rms}		1	2	
Output Distortion	T_{hd}		1.5		%	100% FM Modulation	1	2	
AM Suppression	AMR	40	46		dB	V_{in} = 10mV$_{rms}$	1	3	2
FM Detection for 10.7 MHz Applications:						Detector injection voltage = 60mV$_{rms}$, f_o = 10.7 MHz, F deviation = 75 kHz, Peak separation = 550 kHz, FM modulating frequency = 400 Hz, Amplifier source resistance = 50Ω.			
Amplifier Voltage Gain	V_g		53		dB	$V_{in} \leq$ 0.3mV$_{rms}$, V_{cc} = 12V ±5%.	10	1	
Amplifier Output Voltage	V_{oa}		1.45		V_{pp}	V_{in} = 10mV$_{rms}$	10	1	
Input Limiting Threshold	V_{th}		500		μV_{rms}		4	2	1
Recovered Audio Output	A_{vo}		0.45		V_{rms}		1	2	
Output Distortion	T_{hd}		1.0		%	100% FM modulation	1	2	
AM Suppression	AMR		40		dB	V_{in} = 10mV$_{rms}$	1	3	2

NOTES

1. The limiting threshold voltage is the FM input voltage V_I, expressed in rms volts, for a recovered V_{out} which is 3dB less than the recovered V_{out} at a V_I of 200mV$_{rms}$.

2. The Amplitude Modulation Rejection in decibels, often abbreviated AMR, is given by the following formula:

$$AMR = 20 \log \frac{V_{out} \text{ for 100\% FM modulated } V_i}{V_{out} \text{ for a 30\% AM } V_i}$$

APPLICATION INFORMATION

1. FM DETECTION.
   a. Tuning. Apply FM modulated signal through DC decoupling network to pin 4, V_{in} = 5mV$_{rms}$. Tune for maximum recovered audio at pin 1 or maximum RF voltage at pin 11.
   b. General
      (1) A DC path less than 100Ω shall be provided between pins 2 and 12. No other biasing provisions are required.
      (2) A DC path less than 300Ω should be provided between pins 4 and 6. No other biasing provisions are required.
      (3) The maximum AC load current can be increased by adding an external resistor between pins 1 and 7. The minimum value for this resistor is 800Ω, giving a maximum load current of 4mA$_{rms}$.
2. EXTERNAL DECOUPLING AND MOUNTING CONSIDERATIONS.
   a. All decoupling capacitors should be ceramic type with minimum residual inductance at the operating frequency.
   b. Decoupling capacitor leads at pins 5, 6, and 12 should be as short as possible.
   c. Connections from pin 4 should be as far removed as possible from connections at pins 9, 10, and 12.
   d. The power supply pin 13 should be decoupled with a 0.1μF ceramic capacitor, keeping the leads as short as possible.
   e. When using a large internal impedance power supply (voltage dropping resistor), decouple pin 13 for the lowest audio demodulation frequency.
   f. Keep appropriate distances between the input coil and any other coil in the phase shift network for the voltage gain between these points is high (40 to 60dB).

TYPICAL CIRCUITS

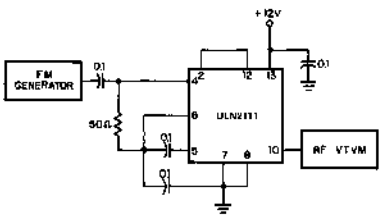


FIGURE 1

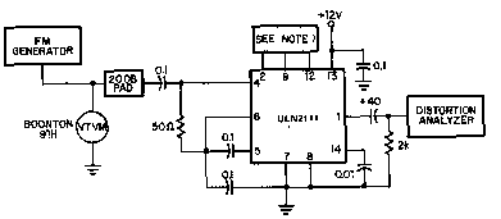


FIGURE 2

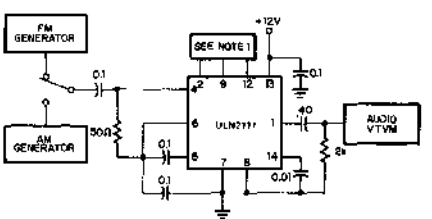


FIGURE 3

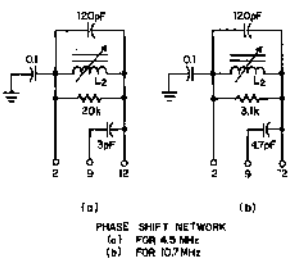
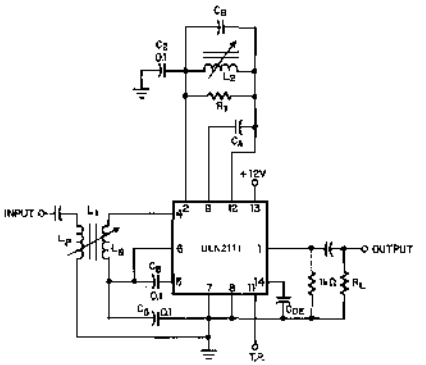


FIGURE 4

NOTES: 1. Phase shift network is specified in Figure 4. 2. All capacitors in microfarads unless otherwise noted.

APPLICATIONS

TYPICAL CIRCUIT REQUIREMENTS FOR FM DETECTION



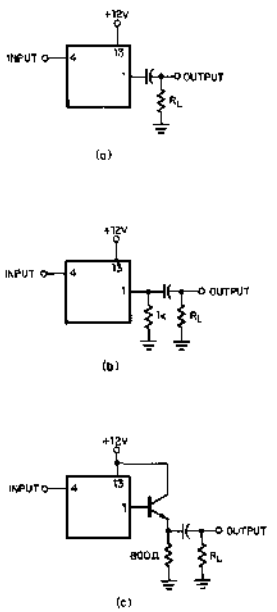
	Component Value		Notes
	TV (4.5 MHz)	FM (10.7 MHz)	
L_1 Inductance	7 - 14μH	1.5 - 3μH	1
L_2 Nom. Unloaded Q	50	50	
L_2 Nom. DC Resistance	50Ω	50Ω	
C_A	3.0pF	4.7pF	
C_B	120pF	120pF	2
R_1	20kΩ	3.1kΩ	
C_5 and C_6	30	20	
C_2	0.1μF	0.1μF	
C_{de}	0.01μF	0.01μF	

NOTES:

1. Suggested coil source: 1.5 - 3μH Miller 9050, 7 - 14μH Miller 9052.
2. Use NPO type capacitor.

Figure 5

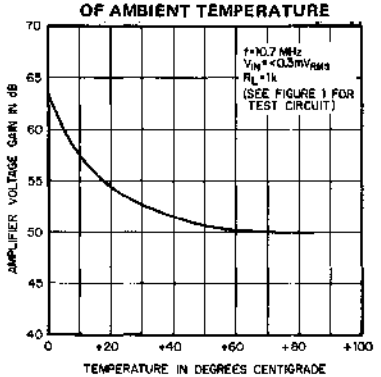
TYPICAL DRIVING CAPABILITIES at f_o = 4.5MHz



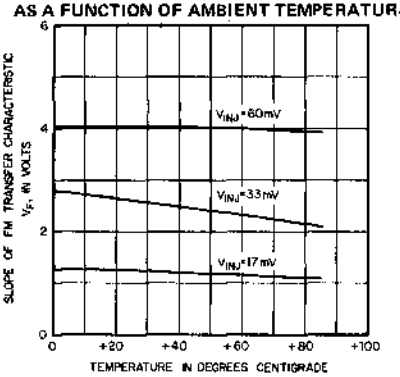
		V_o (mV_{rms})		
Figure	R_L (Ω)	Δf = 7.5 kHz	Δf = 25 kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o=500mV_{rms}

Figure 6

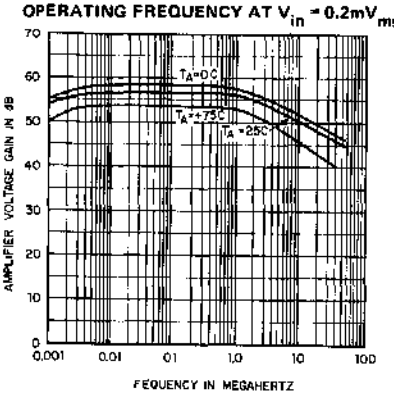
AMPLIFIER GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

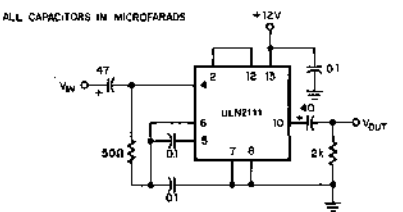


SLOPE OF FM TRANSFER CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

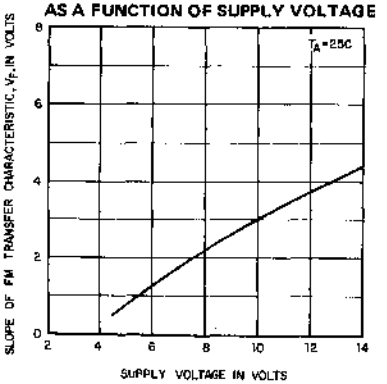


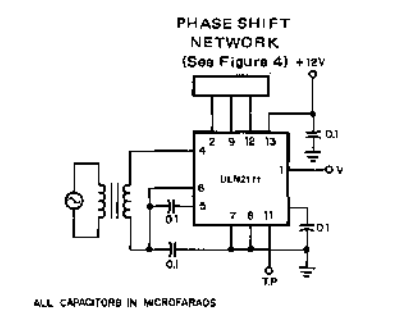
AMPLIFIER VOLTAGE GAIN AS A FUNCTION OF OPERATING FREQUENCY AT V_{in} = 0.2mV$_{rms}$





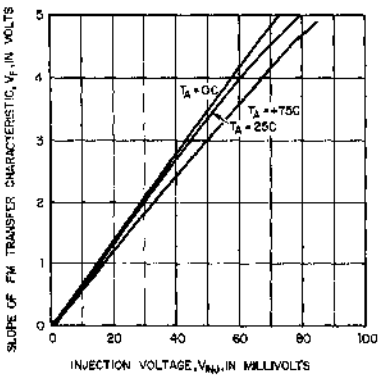
SLOPE OF FM TRANSFER CHARACTERISTIC AS A FUNCTION OF SUPPLY VOLTAGE

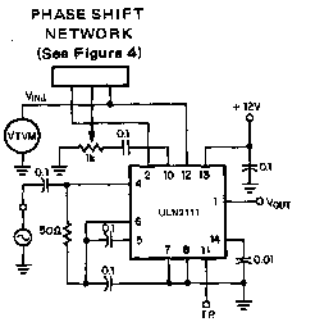




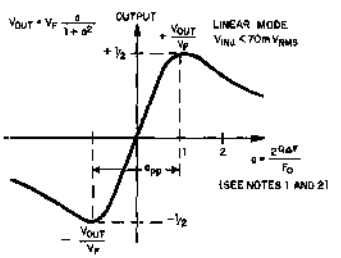
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

SLOPE OF FM TRANSFER CHARACTERISTICS AS A FUNCTION OF INJECTION VOLTAGE





TRANSFER CHARACTERISTICS FOR A SIMPLE LC NETWORK



OUTPUT = ƒ (NORMALIZED DEVIATION)
(The units along the vertical axis are arbitrary units.)
Linear mode: Operation of the FM detector with no limiting after the phase shift network.

NOTES:

1. V_F defines the slope of the FM transfer characteristic, at orgin:

$$V_f = \frac{dV_{out}}{da} \qquad a = 0$$

V_F is primarily a function of bias current in the detector and injection voltage.

V_F will decrease with decreasing V_{CC} or V_{INJ}.

2. a = normalized frequency deviation:

$$a = \frac{2\Omega\Delta F}{F_0}$$

DESCRIPTION

The 5070, 5071, and 5072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The 5070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The 5071 is a chroma amplifier system and the 5072 performs the demodulation function.

The 5070 utilizes the 16-lead plastic dual-in-line package; the 5071 and 5072 are supplied 14-lead plastic dual-in-line packages.

FEATURES

5070

- VOLTAGE CONTROL OSCILLATOR
- KEYED APC & ACC DETECTORS
- DC HUE CONTROL
- SHUNT REGULATOR

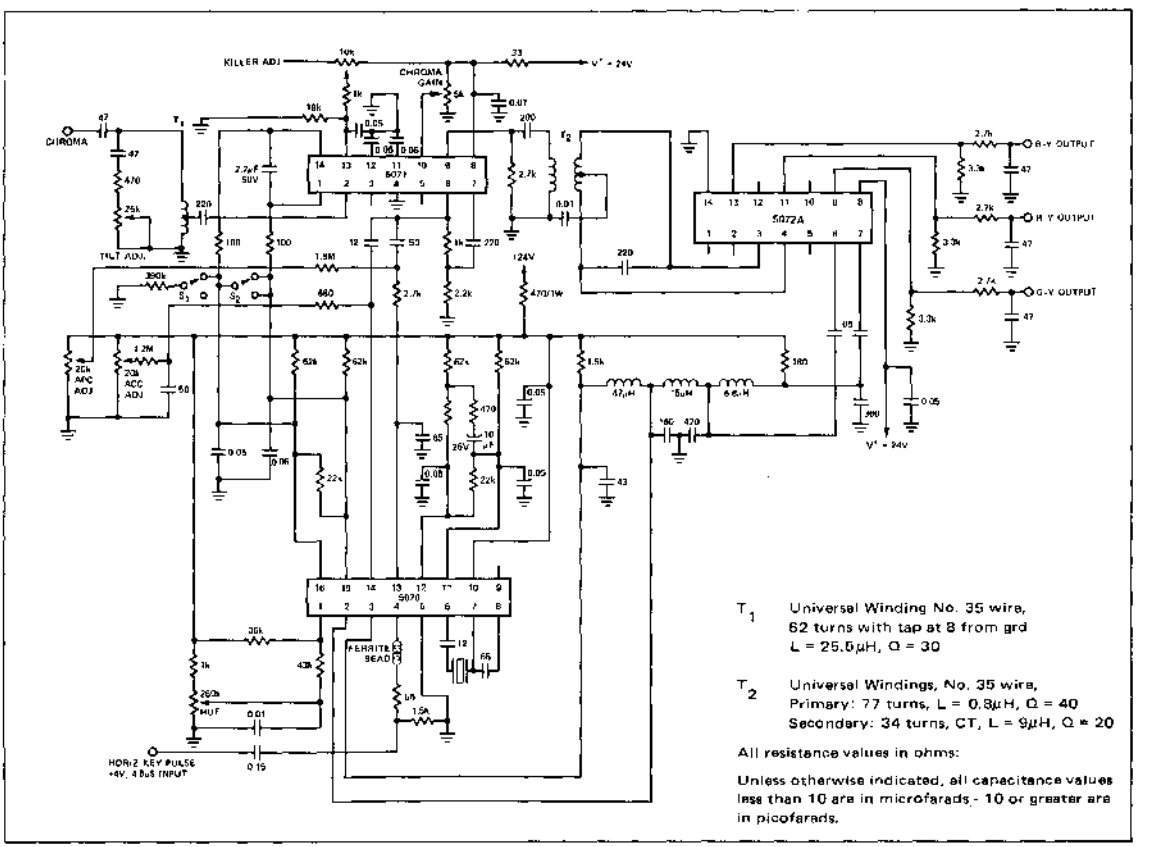
5071

- ACC CONTROLLED CHROMA AMPLIFIER
- DC CHROMA GAIN CONTROL
- COLOR KILLER
- AMPLIFIER SHORT-CIRCUIT PROTECTION

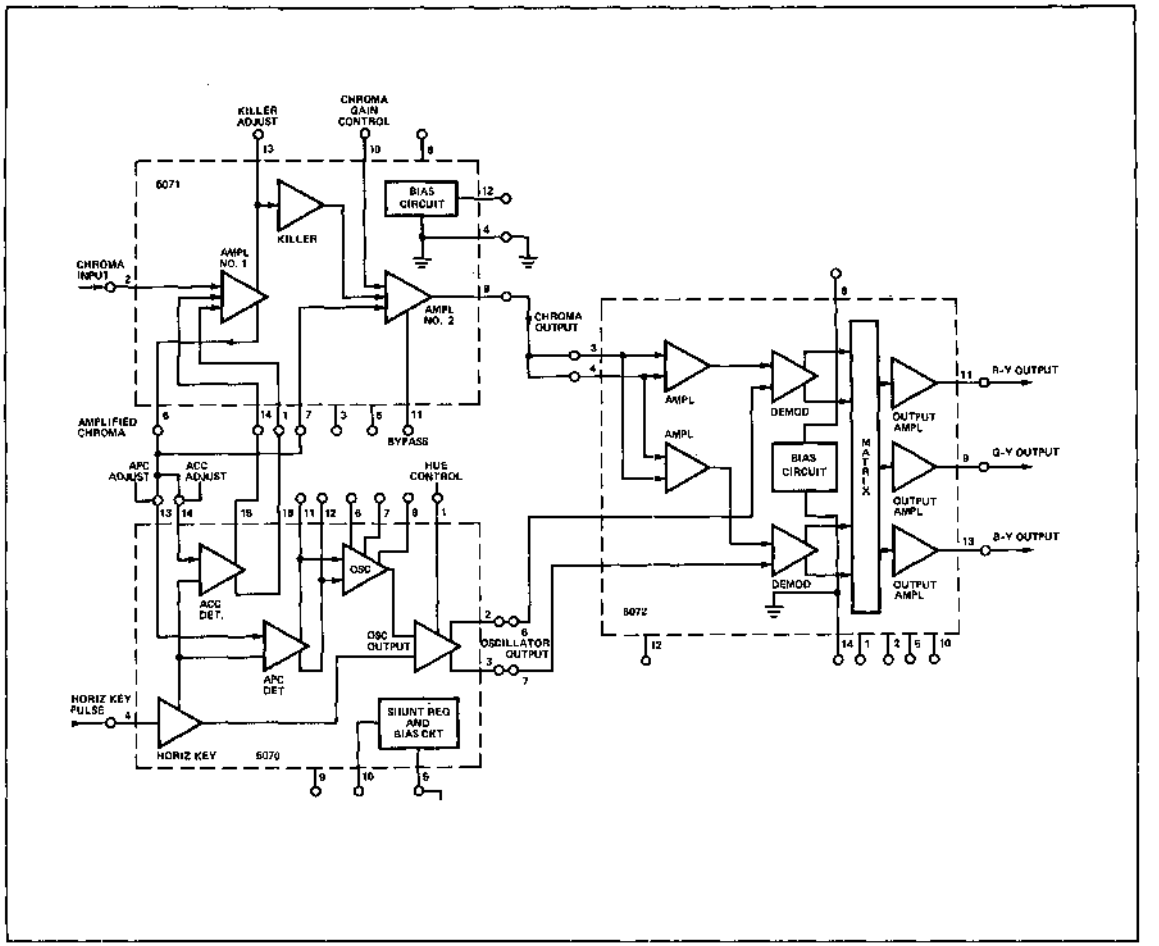
5072

- SYNCHRONOUS DETECTOR WITH COLOR DIFFERENCE MATRIX
- EMITTER-FOLLOWER OUTPUT AMPLIFIERS WITH SHORT-CIRCUIT PROTECTION

TYPICAL SCHEMATIC DIAGRAM



TYPICAL FUNCTIONAL DIAGRAM



DESCRIPTION

The 5070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplifier chroma signal from the 5071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 and 16. This control signal is applied to the input terminal Nos. 1 and 14 of the 5071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

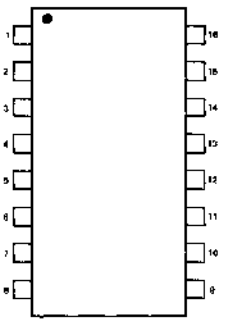
To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback I_{cop}, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The 5070 includes a shunt regulator to establish a 12Vdc supply.

FEATURES

- VOLTAGE CONTROLLED OSCILLATOR
- KEYED APC & ACC DETECTORS
- DC HUE CONTROL
- SHUNT REGULATOR

PIN CONFIGURATION

B PACKAGE
(Top View)



1. Tint Control
2. Oscillator Output
3. Oscillator Output
4. Gate Input
5. Ground
6. Oscillator Feedback
7. Oscillator Control
8. Oscillator Control
9. NC
10. Supply
11. APC Detector Output
12. APC Detector Output
13. APC Detector Input
14. ACC Detector Input
15. ACC Detector Output
16. ACC Detector Output

ORDER PART NO. N5070B

ABSOLUTE MAXIMUM RATINGS

(Values at T_A = 25°C)

DC Supply Voltage and Current	See Charts
Device Dissipation:	
Up to T_A = +70°C	530mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in. (3.17 mm) from seating plane for 10s max	+265°C

Voltage (Note 1)

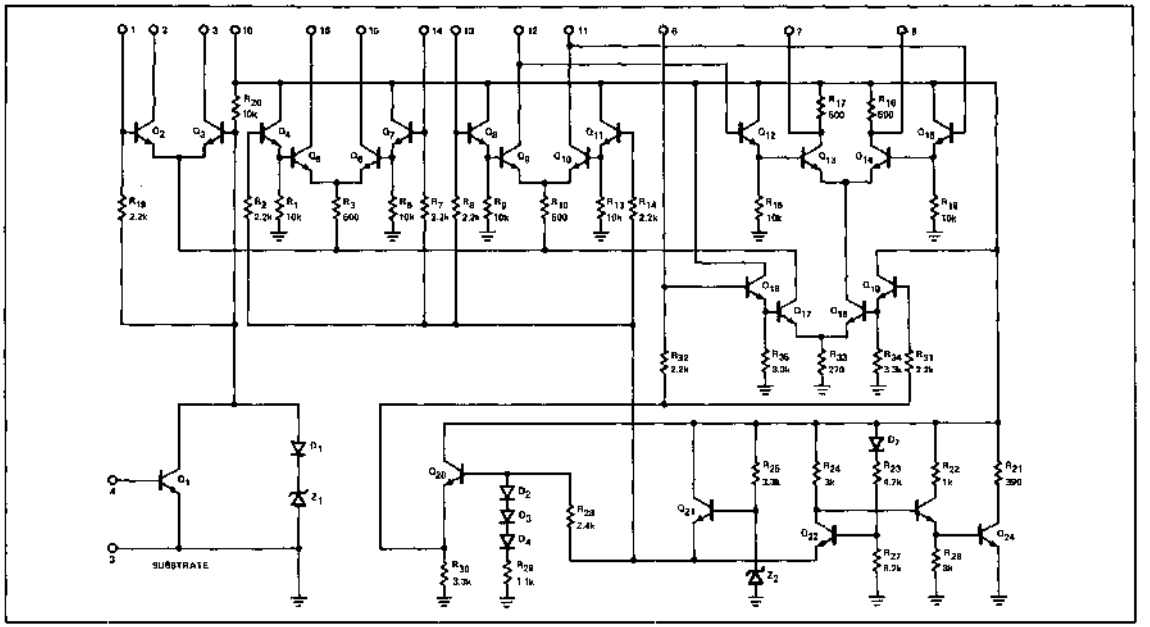
TERM NO.	MIN. VOLTS	MAX. VOLTS
1	0	*
2	0	+16
3	0	+16
4	-5	Note 3
6	–	–
7	–	–
8	–	–
10	0	Note 4
11	0	Note 2
12	0	Note 2
13	0	Note 2
14	0	Note 2
15	0	+16
16	0	+16

Current

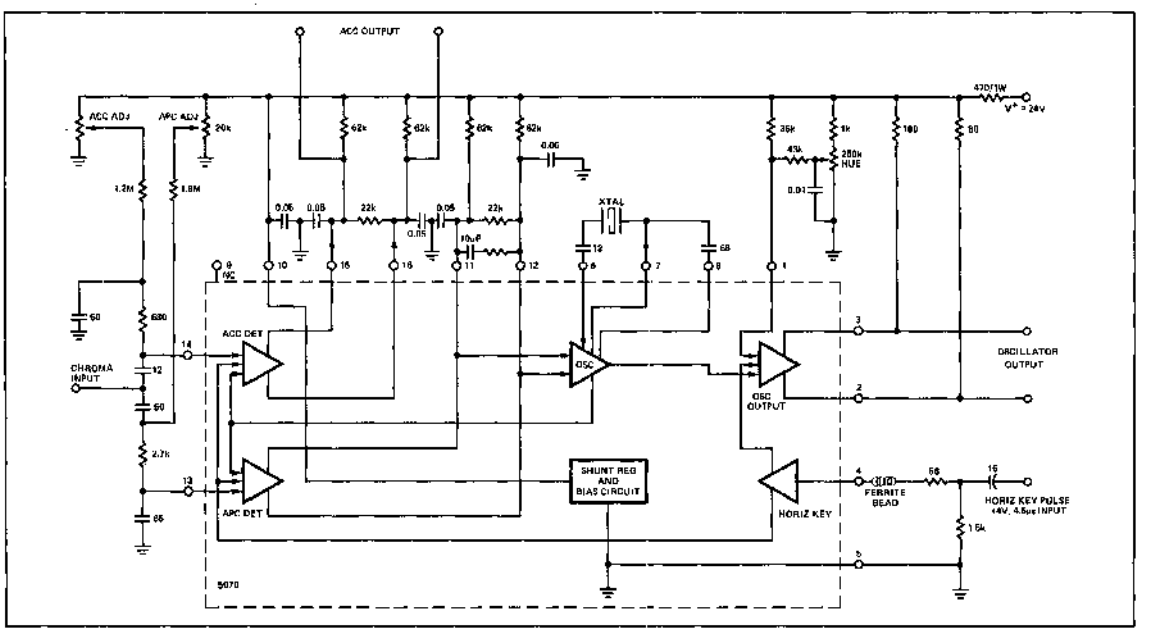
TERM NO.	I_I mA	I_O mA
1	20	1
2	–	–
3	–	–
4	–	1
10	Note 4	1
11	–	–
12	–	–
13	20	1
14	20	1

NOTES:
1. With respect to terminal No. 6 and with terminal No. 10 connected through 470Ω to +24V.
2. Regulated voltage at terminal No. 10.
3. Controlled by max. input current.
4. Limited by dissipation.

SCHEMATIC DIAGRAM



FUNCTIONAL DIAGRAM



NOTES:

1. All resistance values are in ohms
2. Unless otherwise indicated all capacitance values less than 10 are in microfarads – 10 or greater are in picofarads.

DESCRIPTION

The 5071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the 5070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment or dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

FEATURES

- **ACC CONTROLLED CHROMA AMPLIFIER**
- **DC CHROMA GAIN CONTROL**
- **COLOR KILLER**
- **AMPLIFIER SHORT-CIRCUIT PROTECTION**

ABSOLUTE MAXIMUM RATINGS

(Values at $T_A = 25^\circ C$)

DC Supply Voltage (Terminal 8 to Terminal 14) — 30Vdc

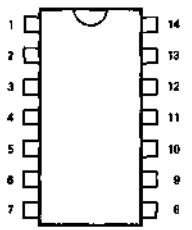
Device Dissipation:
- Up to $T_A = +70^\circ C$ — 530mW
- Above $T_A = +70^\circ C$ — Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:
- Operating — -40 to +85°C
- Storage — -65 to +150°C

Lead Temperature (During Soldering):
- At distance 1/32 in (3.17 mm) from seating plane for 10s max. — +265°C

PIN CONFIGURATION

A PACKAGE
(Top View)



1. ACC Input
2. Chroma Input 1
3. Gain Preselect
4. Ground
5. NC
6. Chroma Output 1
7. Chroma Output 2
8. V+
9. Chroma Output 2
10. Chroma Level Control
11. Decouple
12. Decouple
13. Killer Adjust
14. ACC Input

ORDER PART NO. N5071A

MAXIMUM RATINGS MAXIMUM VOLTAGE & CURRENT RATINGS $T_A = 25^\circ C$

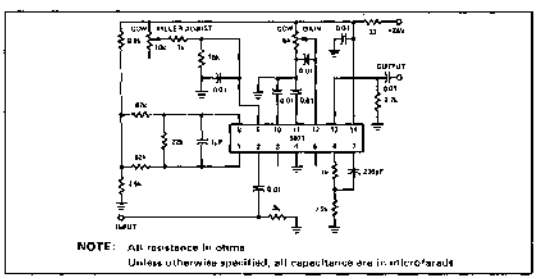
TERM NO.	Voltage (Note 1) MIN. VOLTS	MAX. VOLTS	TERM NO.	Current I_I* mA	I_O mA
1	-5	+15	1	5	1.0
2	-5	+5	2	5	1.0
6	0	+24	6	1.0	20
7	-5	+5	7	5	1.0
8	0	+30	9	1.0	20
9	0	+24	12	1.0	5
10	0	+24	14	5	1.0
11	0	+24			
12	0	+20			
13	0	+20			
14	-5	+15			

NOTES:
1. With reference to terminal No. 4 and with +24V on terminal No. 8 except for the rating given for terminal No. 8.

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V^+ = +24V)

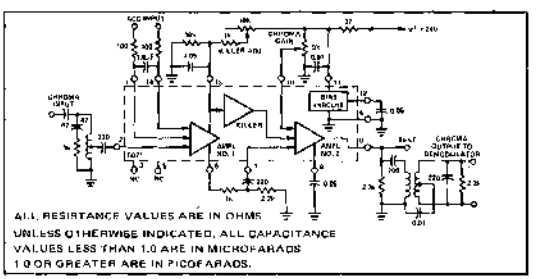
PARAMETERS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC CHARACTERISTICS					
Voltages					
Bias Reference Terminal	S_1 Open, S_2 Open		17.3		V
Ampl No. 1 Chroma Input	S_1 Open, S_2 Open		1.75		V
Ampl No. 1 Chroma Output Balanced	S_1 Open, S_2 Open		20		V
Unbalanced	S_1 Open, S_2 Closed		13.5		V
Ampl No. 2 Chroma Input	S_1 Open, S_2 Open		1.5		V
Ampl No. 2 Chroma Output	S_1 Closed, S_2 Open		20.6		V
Supply Current	S_1 Open, S_2 Open	17		31	mA
DYNAMIC CHARACTERISTICS					
Amplifier No. 1 Voltage Gain	E_g = 30 mVrms Measure V6	14			dB
Amplifier No. 2 Voltage Gain	V_g = 10 Vrms		14		dB
Max. Chroma Output Voltage			2		Vrms
10% Chroma Gain Control Reference Voltage	E_g = 50 mVrms, adjust Chroma Gain Control to Change V_9 to 10% of Maximum Chroma Output		20.2		V
Output Voltage Killer Off	S_1 in Position 2 E_g = 50 mVrms, adjust "Killer Adjust" for an abrupt decrease in V_9			12	mV rms
Output Voltage, Chroma Off	E_g = 50 Vrms, adjust Chroma control to min. Chroma Output			12	mV rms
Bandwidth					
Amplifier No. 1			12		MHz
Amplifier No. 2			30		MHz
Ampl. No. 1 Input Impedance			2		kΩ
			4		pF
Ampl. No. 1 Output Impedance			35		Ω
Ampl. No. 2 Input Impedance			2.1		kΩ
			3.5		pF
Ampl. No. 2 Output Impedance			85		Ω

AMPLIFIER DIAGRAM



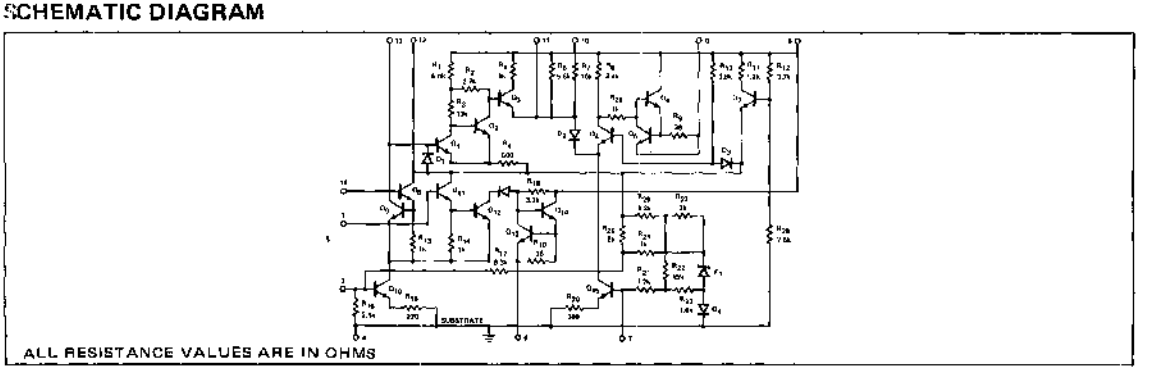
NOTE: All resistance in ohms
Unless otherwise specified, all capacitance are in microfarads

FUNCTIONAL DIAGRAM



ALL RESISTANCE VALUES ARE IN OHMS
UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES LESS THAN 1.0 ARE IN MICROFARADS
1.0 OR GREATER ARE IN PICOFARADS.

SCHEMATIC DIAGRAM



ALL RESISTANCE VALUES ARE IN OHMS

DESCRIPTION

The 5072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the 5072 are suitable to driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

FEATURES

- **SYNCHRONOUS DETECTOR WITH COLOR DIFFERENCE MATRIX**
- **EMITTER-FOLLOWER OUTPUT AMPLIFIERS WITH SHORT-CIRCUIT PROTECTION**

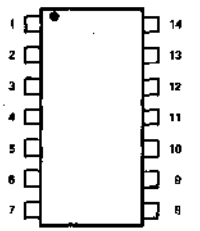
ABSOLUTE MAXIMUM RATINGS

(Values at $T_A = 25^\circ C$)

DC Supply Voltage (Terminal 8 to Terminal 14)	27V
Reference Input Voltage	$5V_{p-p}$
Chroma Input Voltage	$5V_{p-p}$
Device Dissipation:	
Up to $T_A = +70^\circ C$	530mW
Above $T_A = +70^\circ C$	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in (3.17 mm) from seating plane for 10s max.	+165°C

PIN CONFIGURATION

A PACKAGE
(Top View)



1.	NC	8.	V^+
2.	NC	9.	$E_G - E_Y$
3.	Chroma (–)	10.	NC
4.	Chroma (+)	11.	$E_R - E_Y$
5.	NC	12.	NC
6.	Ref "B"	13.	$E_B - E_Y$
7.	Ref "A"	14.	GND

ORDER PART NO N5072A

MAXIMUM VOLTAGE & CURRENT RATINGS

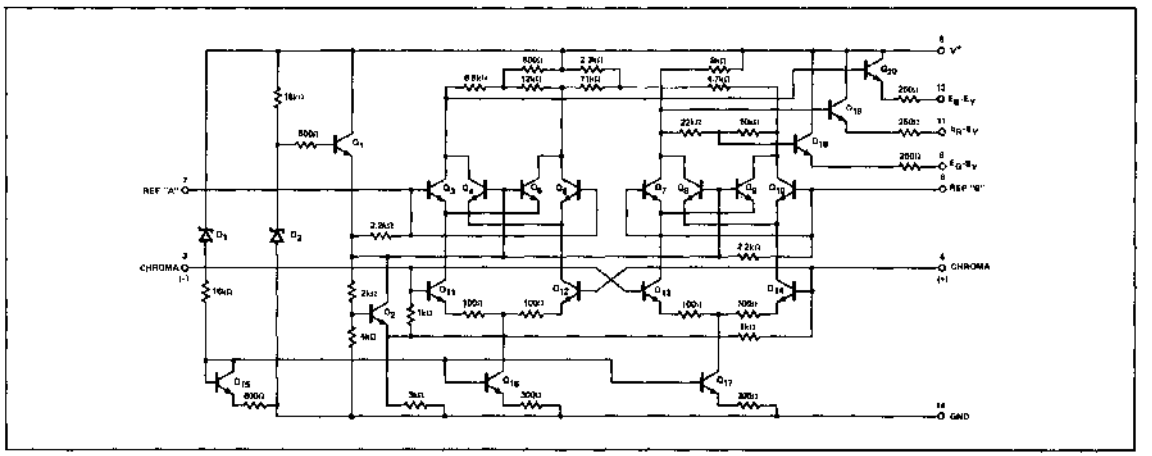
$T_A = 25^\circ C$ VOLTAGE (Note 1) CURRENT

Terminal No.	MIN. VOLTS	MAX. VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	-	-
4	0	+5	4	-	-
6	0	+12	6	-	-
7	0	+12	7	-	-
8	0	+27	8	-	-
9	0	-20	9	10	20
11	0	+20	11	10	20
13	0	+20	13	10	20

NOTE:

1. With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

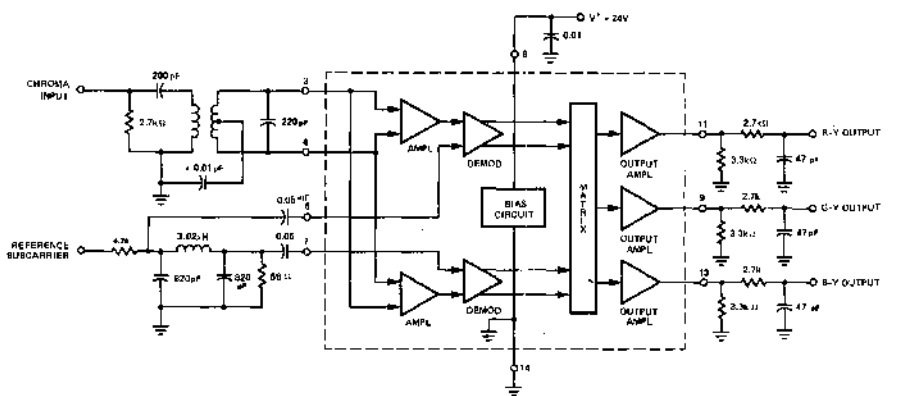
SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C and V^+ = +24V unless otherwise specified)

PARAMETERS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC CHARACTERISTICS					
Supply Current With Output Loads	S_1 Closed	16.5		26.5	mA
With No Output Loads	S_1 Open		9		mA
G-Y, R-Y, B-Y Outputs	S_1 Closed	13.2	14.7	15.8	V
Chroma Inputs	S_1 Open		3.3		V
Reference Subcarrier	S_1 Open		6.2		V
DYNAMIC CHARACTERISTICS					
Demodulator Unbalance	$V_3 = V_4 = 0$			0.8	
Maximum Color Difference Output Voltage	$V_3 = V_4 = 0.6$ Vp-p	8.0			Vp-p
		5.5			Vp-p
		1.2			Vp-p
Chroma Input Sensitivity	Adjust e_c for 5.0 Vp-o @ term		0.2	0.35	Vp-p
Relative R-Y Output	No. 13 (B-Y)	3.5		4.2	Vp-p
Relative G-Y Output		0.75		1.25	Vp-p
V_{DC} Difference Between any two Output Terminals	$e_c = 0$			0.6	V
Input Impedance Reference Subcarrier Inputs			1.7		kΩ
			6		pF
Input Impedance at Chroma Inputs			0.95		kΩ
			6		pF
Output Resistance			180		Ω

FUNCTIONAL DIAGRAM



LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The 5556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The 5556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

The 5556 features industry standard pinout and is a direct pin-for-pin replacement for the MC15556G and MC1456G.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage

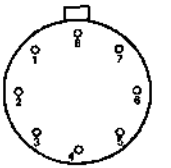
S5556	±22V
N5556	±18V
Differential Input Voltage	± V^+
Common Mode Input Voltage	± V^+
Load Current	20mA
Output Short Circuit Duration	Indefinite
Power Dissipation	680mW
Derate Above T_A = 25°C	4.6mW/°C
Operating Temperature Range	
S5556	−55°C to +125°C
N5556	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FEATURES

- **LOW INPUT BIAS CURRENT - 15nA maximum**
- **LOW INPUT OFFSET CURRENT - 2.0nA maximum**
- **LOW INPUT OFFSET VOLTAGE - 4.0mV maximum**
- **HIGH SLEW RATE - 2.5 V/μs typical**
- **LARGE POWER BANDWIDTH - 40kHz typical**
- **LOW POWER CONSUMPTION - 45mW maximum**
- **OFFSET VOLTAGE NULL CAPABILITY**

PIN CONFIGURATIONS (Top View)

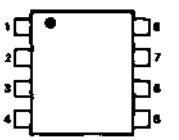
T PACKAGE



1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. V_{OUT}
7. V^+
8. NC

Order Part Nos. S5556T/N5556T

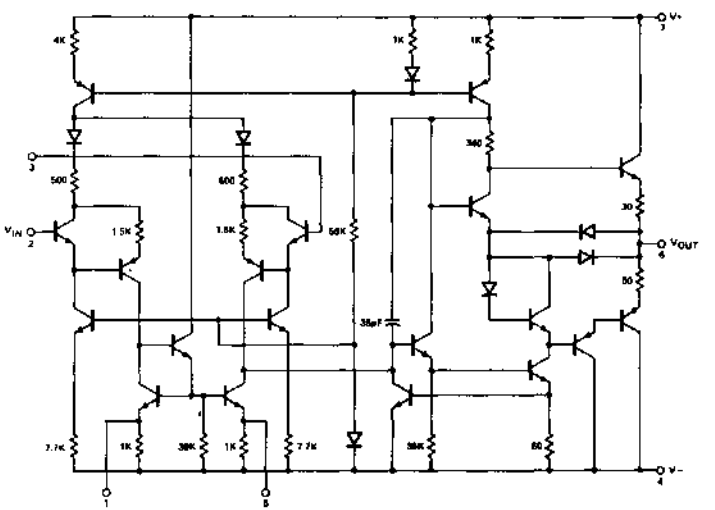
V PACKAGE



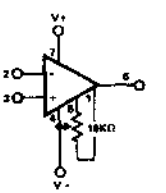
1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. V_{OUT}
7. V^+
8. NC

Order Part Nos. S5556V/N5556V

EQUIVALENT SCHEMATIC



OFFSET ADJUST CIRCUIT



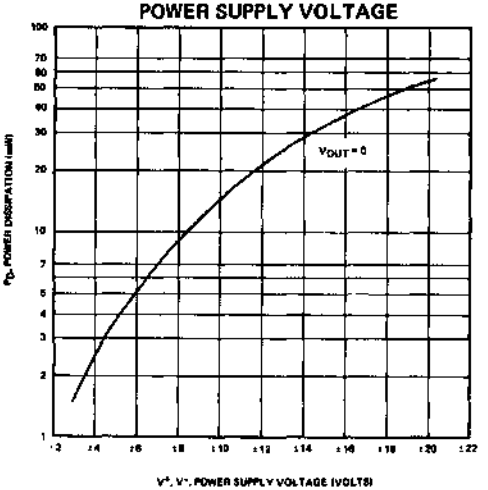
ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $T_A = +25°C$ Unless Otherwise Noted)

PARAMETER	SYMBOL	MIN		TYP		MAX		UNITS
		S5556	N5556	S5556	N5556	S5556	N5556	
Input Bias Current	I_B							
$T_A = 25°C$				8	15	15	30	nA
$T_A = T_{LOW}$ to T_{HIGH} (Note 1)						30	40	nA
Input Offset Current	I_{io}							
$T_A = 25°$				1.0	5.0	2.0	10	nA
$T_A = 25°C$ to T_{High}						3.0	14	nA
$T_A = T_{LOW}$ to $25°C$						5.0	14	nA
Input Offset Voltage	V_{io}							
$T_A = 25°C$				2.0	5.0	4.0	10	mV
$T_A = T_{LOW}$ to T_{HIGH}						6.0	14	mV
Differential Input Impedance (Open Loop–f = 20Hz)								
Parallel Input Resistance	R_p			5.0	3.0			M
Parallel Input Capacitance	C_p			6.0	6.0			pF
Common Mode Input Impedance (f = 20Hz)	Z_{IN}			250	250			M
Common Mode Input Voltage Swing	CMV_{IN}	±12	±11	±13	±12			V
Equivalent Input Noise Voltage	E_{IN}			45	45			$nV/\sqrt{Hz}$
(Av = 100, Rs = 10KΩ, F = 1.0KHz, BW = 1.0Hz)								
Common Mode Rejection Ratio (f = 100Hz)	CMRR	80	70	110	110			dB
Open Loop Voltage Gain (V_{Out} = ±10V, R_L = 2KΩ)	AVO							
$T_A = 25°C$		100K	70K	200K	100K			V/V
$T_A = T_{LOW}$ to T_{HIGH}		40K	40K					V/V
Power Bandwidth Av = 1, R_L = 2KΩ, THD ≤ 5%, V_{OUT} = ±10V)	P_{BW}			40	40			KHz
Unity Gain Crossover Frequency (open-loop)				1.0	1.0			MHz
Phase Margin (open-loop, unity gain)				70	70			Degrees
Gain Margin				18	18			dB
Slew Rate (unity gain)	dV_{OUT}/dt			2.5	2.5			V/µsec
Output Impedance (f = 20Hz)	Z_{OUT}			1.0	1.0	2.0	2.5	KΩ
Output Voltage Swing (R_L = 2KΩ)	V_{OUT}	±12	±11	±13	±12			V
Power Supply Sensitivity								
V^- = Constant, RS ≤ 10K	S^+			50	75	100	200	µV/V
V^+ = Constant, RS ≤ 10K	S^-			50	75	100	200	µV/V
Power Supply Current	I_{D+}			1.0	1.3	1.5	3.0	mA
	I_{D-}			1.0	1.3	1.5	3.0	mA
DC Quiescent Power Dissipation (V_{OUT} = 0)	P_D			30	40	45	90	mW

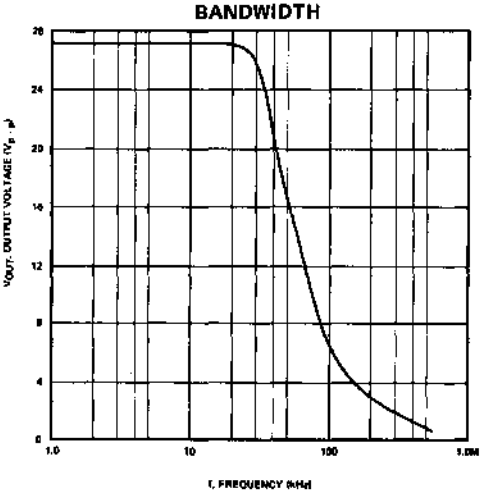
NOTE:
1. $T_{LOW} = 0°C$ for N5556, $-55°C$ for S5556; $T_{HIGH} = 70°C$ for N5556, $125°C$ for S5556

TYPICAL PERFORMANCE CHARACTERISTICS

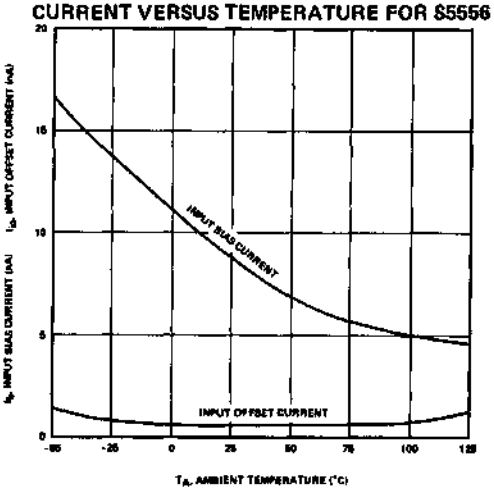
POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGE



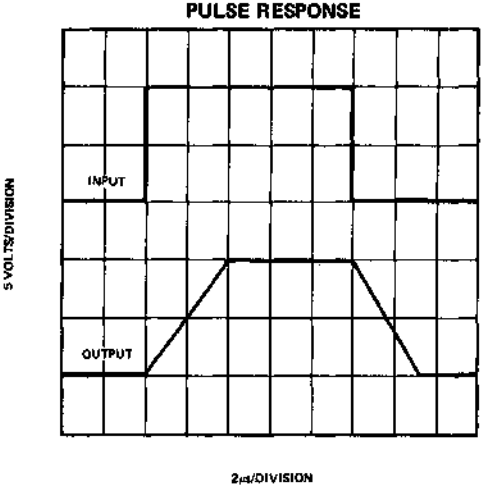
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VERSUS TEMPERATURE FOR S5556



VOLTAGE-FOLLOWER PULSE RESPONSE



DESCRIPTION

The 5558 consists of a pair of high performance monolithic operational amplifiers constructed on a single chip. It features internal compensation and is intended for use in a variety of analog applications. High common mode voltage range and immunity to latch-up makes the 5558 ideal for use as a voltage follower. The high gain and wide range of operating voltage achieves superior performance in integrator, summing amplifier, and general feedback applications. The device is short-circuit protected. For single amplifier performance see the 5741 data sheet. The 5558 is a pin-for-pin replacement for the MC1558G.

ABSOLUTE MAXIMUM RATINGS

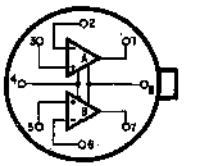
Power Supply Voltages	
S5558	±22V
N5558	±18V
Differential Input Voltage	±30V
Common-mode Input Swing	±15V
Output Short Circuit Duration	Continuous
Power Dissipation (Note 1)	
T Package – (MO-002-AG)	680mW
V Package	625mW
Operating Temperature Range	
S5558	–55°C to +125°C
N5558	0°C to +75°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTE:

1. Derate T package linearly at 4.6 mW/°C for ambient temperatures above +25°C
2. Derate V package at 5mW/°C above 25°C

PIN CONFIGURATIONS

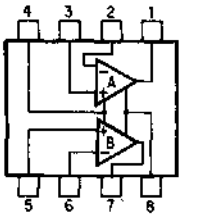
T-PACKAGE
(Top View)



1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V^+

ORDER PART NOS. S5558T/N5558T

V-PACKAGE



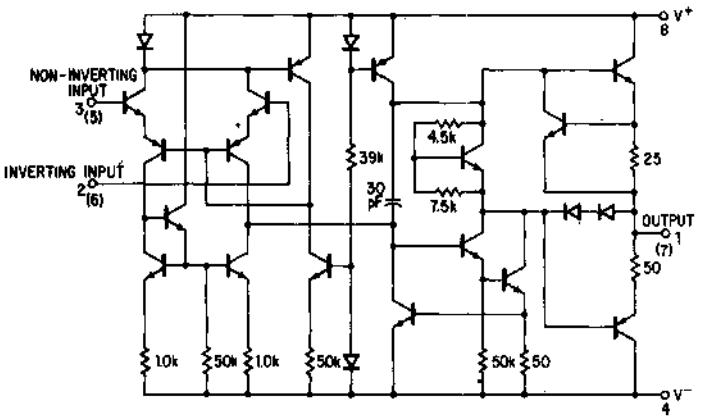
1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V^+

ORDER PART NO. N5558V

FEATURES:

- 2 "OP AMPS" IN SPACE OF ONE 741 V PACKAGE
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- LOW POWER CONSUMPTION
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

EQUIVALENT SCHEMATIC



The numbers without parenthesis represent the pin numbers for ½ of the dual circuit. The numbers in parenthesis represent the pin numbers for the other half.

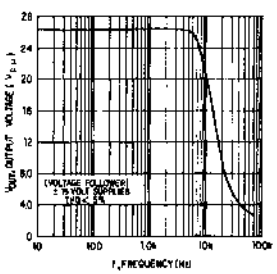
ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

CHARACTERISTICS	SYMBOL	MIN		TYP		MAX		UNIT
		S5558	N5558	S5558	N5558	S5558	N5558	
Input Bias Current	I_b							μAdc
T_A = +25°C				0.2	0.2	0.5	0.5	
T_A = T_{low} to T_{high} (See Note 1)						1.5	0.8	
Input Offset Current	$\|I_{io}\|$							μAdc
T_A = +25°C				0.03	0.03	0.2	0.2	
T_A = T_{low} to T_{high}						0.5	0.3	
Input Offset Voltage ($R_S \leq 10k\Omega$)	$\|V_{io}\|$							mVdc
T_A = +25°C				1.0	2.0	5.0	6.0	
T_A = T_{low} to T_{high}						6.0	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_P	0.3	0.3	1.0	1.0			Megohm
Parallel Input Capacitance	C_P			6.0	6.0			pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$			200	200			Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±12	±13	±13			V_{pk}
Equivalent Input Noise Voltage	e_n							nV(Hz)½
(A_V = 100, R_S = kΩ, f = 1.0 kHz, BW = 1.0 Hz)				45	45			
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	70	90	90			dB
Open-Loop Voltage Gain, (V_{out} = ±10V, R_L = 2.0kΩ)	A_{VOL}							V/V
T_A = +25°C		50,000	20,000	200,000	100,000			
T_A = T_{low} to T_{high}		25,000	15,000					
Power Bandwidth (A_V = 1, R_L = 2.0kΩ, THD≤5%, V_{out} = $20V_{p-p}$)	P_{BW}			14	14			kHz
Unity Gain Crossover Frequency (open-loop)				1.1	1.1			MHz
Phase Margin (open-loop, unity gain)				65	65			degrees
Gain Margin				11	11			dB
Slew Rate (Unity Gain)	dV_{out}/dt			0.8	0.8			V/μs
Output Impedance (f = 20 Hz)	Z_{out}			300	300			ohms
Short-Circuit Output Current	I_{SC}			20	20			mAdc
Output Voltage Swing	V_{out}							V_{pk}
(R_L = 10kΩ)		±12	±12	±14	±14			
R_L = 2kΩ (T_A = T_{low} to T_{high})		±10	±10	±13	±13			
Power Supply Sensitivity								μV/V
V^- = constant, $R_S \leq 10k\Omega$	S^+			30	30	150	150	
V^+ = constant, $R_S \leq 10k\Omega$	S^-			30	30	150	150	
Power Supply Current	I_D^+			2.3	2.3	5.0	5.6	mAdc
	I_D^-			2.3	2.3	5.0	5.6	
DC Quiescent Power Dissipation (V_{out} = 0)	P_D			70	70	150	170	mW
Channel Separation	e_{o1}/e_{o2}			120	120			dB

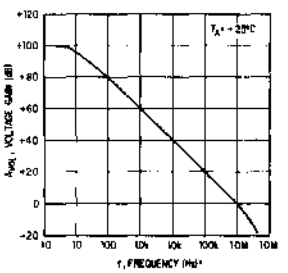
Note 1: T_{low}: 0°C for N5558, −55°C for S5558; T_{high}: +75°C for N5558, +125°C for S5558

TYPICAL CHARACTERISTIC CURVES

POWER BANDWIDTH (Large Signal Swing versus Frequency)



OPEN LOOP FREQUENCY RESPONSE



DESCRIPTION

The 5596 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The S5596 will operate over the full military temperature range of -55°C to +125°C. The N5596 is intended for applications within the range of 0°C to +70°C.

FEATURES

- **EXCELLENT CARRIER SUPPRESSION**

  65dB typ @ 0.5 MHz

  50dB typ @ 10 MHz

- **ADJUSTABLE GAIN AND SIGNAL HANDLING**
- **BALANCED INPUTS AND OUTPUTS**
- **HIGH COMMON-MODE REJECTION – 85dB typ**

APPLICATIONS

SUPPRESSED CARRIER AND AMPLITUDE MODULATION
SYNCHRONOUS DETECTION
FM DETECTION
PHASE DETECTION
SAMPLING
SINGLE SIDEBAND
FREQUENCY DOUBLING

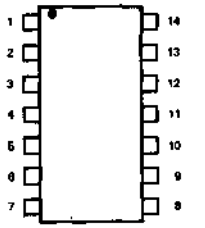
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (Note 1)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$\pm(5 + I_5 R_e)$V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	10mA
Power Dissipation (Pkg. Limitation)	
K-Package	680mW
Derate above 25°C	5.4mW/°C
A-Package (TO-116)	900mW
Derate above 25°C	7.2mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

NOTES:
1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to K package pinout only.

PIN CONFIGURATIONS

A PACKAGE
(Top View)



ORDER PART NOS.
S5596A/N5596A

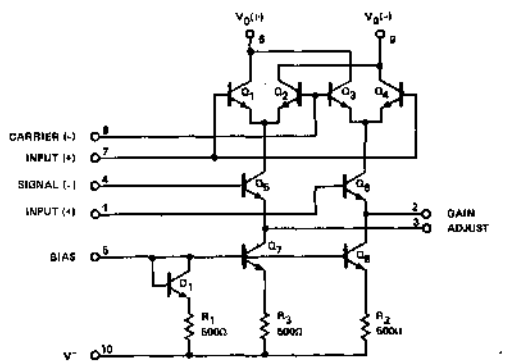
1. Positive Signal Input
2. Gain Adjust
3. NC
4. Gain Adjust
5. Negative Signal Input
6. Bias
7. NC
8. Positive Output
9. Positive Carrier Input
10. Negative Carrier Input
11. NC
12. NC
13. Negative Output
14. V^-

K PACKAGE

ORDER PART NOS.
S5596K/N5596K

1. Positive Signal Input
2. Gain Adjust
3. Gain Adjust
4. Negative Signal Input
5. Bias
6. Positive Output
7. Positive Carrier Input
8. Negative Carrier Input
9. Negative Output
10. V^-

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS* (All input and output characteristics are single-ended unless otherwise noted.)

PARAMETER		S5596			N5596			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Carrier Feedthrough								μV(rms)
V_C = 60 mV(rms) sine wave and	f_C = 1.0 kHz		40			40		
offset adjusted to zero	f_C = 10 MHz		140			140		
V_C = 300 mVp-p square wave:								mV(rms)
offset adjusted to zero	f_C = 1.0 kHz		0.04	0.2		0.04	0.4	
offset not adjusted	f_C = 1.0 kHz		20	100		20	200	
Carrier Suppressions								dB
f_S = 10 kHz, 300 mV(rms)								
f_C = 500 kHz, 60 mV(rms) sine wave		50	65		40	65		
f_C = 10 MHz, 60 mV(rms) sine wave			50			50		
Transadmittance Bandwidth (Magnitude) (R_L = 50Ω)								MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave			300			300		
f_S = 1.0 kHz, 300 mV(rms) sine wave								
Signal Input Port, V_S = 300 mV(rms) sine wave			80			80		
$\|V_C\|$ = 0.5V dc								
Signal Gain		2.5	3.5		2.5	3.5		V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\|V_C\|$ = 0.5V dc								
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz								
Parallel Input Resistance			200			200		kΩ
Parallel Input Capacitance			2.0			2.0		pF
Single-Ended Output Impedance, f = 10 MHz								
Parallel Output Resistance			40			40		kΩ
Parallel Output Capacitance			5.0			5.0		pF
Input Bias Current								μA
$I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$			12	25		12	30	
			12	25		12	30	
Input Offset Current								μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$			0.7	5.0		0.7	7.0	
			0.7	5.0		0.7	7.0	
Average Temperature Coefficient of Input Offset Current			2.0			2.0		nA/°C
(T_A = -55°C to +125°C)								
Output Offset Current			14	50		15	80	μA
($I_6 - I_9$)								
Average Temperature Coefficient of Output Offset Current			90			90		nA/°C
(T_A = -55°C to +125°C)								
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz			5.0			5.0		Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz,			-86			-85		dB
$\|V_C\|$ = 0.5V dc								
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)			8.0			8.0		Vdc
Differential Output Voltage Swing Capability			8.0			8.0		Vp-p
Power Supply Current								mAdc
$I_6 + I_9$			2.0	3.0		2.0	4.0	
I_{10}			3.0	4.0		3.0	5.0	
DC Power Dissipation			33			33		mW

(V^+ = +12V dc, V^- = -8.0V dc, I_5 = 1.0mA dc, R_L = 3.9kΩ, R_e = 1.0kΩ, T_A = +25°C unless otherwise noted)

*Pin number references pertain to K package pinout only.

signetics DUAL CORE MEMORY SENSE AMPLIFIERS

SN7520
SN7521
SN7522
SN7523
SN7524
SN7525

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The 7520 Series Dual Core Memory Sense Amplifiers are designed for use in high speed core memory systems. Three separate logic configurations allow flexibility of system design.

The 7520 and 7521 can be used to perform the function of a flip-flop or a data register which responds to the sense and strobe-input conditions.

The 7522 and 7523 features an open collector stage which may be used to perform the wired-OR function.

The 7524 and 7525 features two independent sense channels with separate outputs.

FEATURES

- DUAL SENSE AMPS
- ±4mV THRESHOLD UNCERTAINTY
- DESIGN VERSATILITY
- 25ns PROPAGATION DELAY

ABSOLUTE MAXIMUM RATINGS

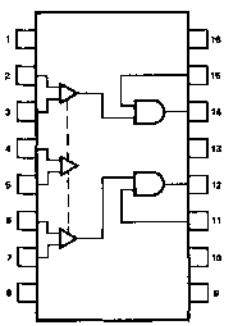
Differential Input Voltage	±5V
V_{CC}	±7V
Strobe & Gain Input Voltages	+5.5V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation	500mW

PIN CONFIGURATIONS

B PACKAGE (Top View)

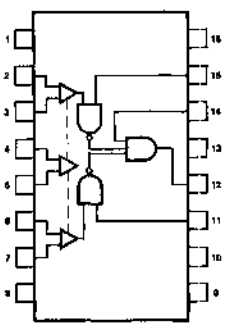
7520/21

ORDER PART NOS.
SN7520N/
SN7521N



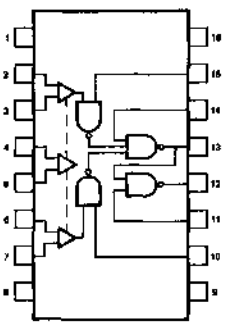
7522/23

ORDER PART NOS.
SN7522N/
SN7523N



7524/25

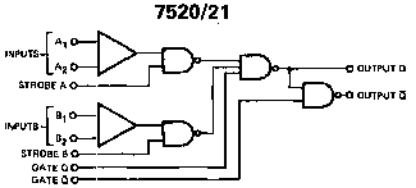
ORDER PART NOS.
SN7524N/
SN7525N



*The Signetics 7520/21/22/23/24/25 does not require an external capacitor (C_{ext}) to stabilize the pre-amplifier. Pin 1 may be used as a test point, giving access to the pre-amplifier output. No degradation of performance will result if a 100pF capacitor is connected from Pin 1 to GND.

LOGIC DIAGRAMS

7520/21



$\overline{\text{Output Q}} = \overline{G_Q} + (S_A\ IN_A + S_B\ IN_B)\ G_Q$

$\text{Output } \overline{Q} = G_Q\ (\overline{G_Q} + S_A\ IN_A + S_B\ IN_B)$

where:

G_Q = Gate Q ≥ 2V

S_A = Strobe A ≥ 2V

IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

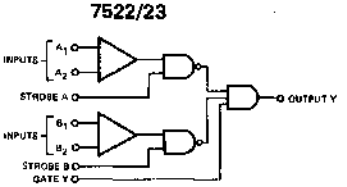
S_B = Strobe B ≥ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

$\overline{G_Q}$ = Gate Q ≤ 0.8V

$G_{\overline{Q}}$ = Gate $\overline{Q}$ ≥ 2V

7522/23



$\overline{\text{Output Y}} = G(S_A\ IN_A + S_B\ IN_B) + \overline{G}$

where:

G = Gate ≥ 2V

S_A = Strobe A ≥ 2V

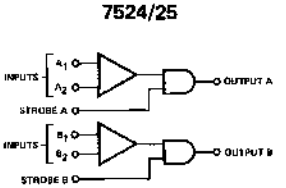
IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

S_B = Strobe B ≥ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

G = Gate ≤ 0.4V

7524/25



Output A = $S_A\ IN_A$

Output B = $S_B\ IN_B$

where:

S_A = Strobe A ≥ 2V

IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

S_B = Strobe B ≥ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_T	Differential-Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7520	11	15	18	mV
			7521	8	15	22	mV
		V_{ref} = 40mV	7520	36	40	44	mV
			7521	33	40	47	mV
		Strobe Input: $V_{inS} = V_{in(1)}$					
V_{CMF}	Common-Mode Input Firing Voltage (See Note 2)	Common-Mode Input Pulse: $t_r = t_f \leq 15ns$, $t_{p(in)}$ = 50ns T_A = 25°C			±3		V
I_{in}	Differential-Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential-Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential-Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (gate	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA			0.25	0.4	V
$I_{OS(Q)}$	Q Output Short-Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		3.3		5	mA
$I_{OS(\overline{Q})}$	$\overline{Q}$ Output Short-Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			28		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			-14		mA
$t_{or\ D}$	Differential-Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or\ CM}$	Common-Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum cycle time				200		ns

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)DQ}$, $t_{pd(0)DQ}$	$A_1 - A_2$ or $B_1 - B_2$	Q		20 30	40	ns ns
$t_{pd(1)D\overline{Q}}$, $t_{pd(0)D\overline{Q}}$	$A_1 - A_2$ or $B_1 - B_2$	$\overline{Q}$		25 35	 55	ns ns
$t_{pd(1)SQ}$, $t_{pd(0)SQ}$	Strobe A or B	Q		15 25	30 	ns ns
$t_{pd(1)S\overline{Q}}$, $t_{pd(0)S\overline{Q}}$	Strobe A or B	$\overline{Q}$		15 35	 55	ns ns
$t_{pd(1)G_QQ}$, $t_{pd(0)G_QQ}$	Gate Q	Q		10 15	20 	ns ns
$t_{pd(1)G_Q\overline{Q}}$, $t_{pd(0)G_Q\overline{Q}}$	Gate Q	$\overline{Q}$		15 20	 30	ns ns
$t_{pd(1)G_Q\overline{Q}}$, $t_{pd(0)G_Q\overline{Q}}$	Gate $\overline{Q}$	$\overline{Q}$		15 10	 20	ns ns

(SEE NOTES PAGE 128)

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7522	11	15	19	mV
			7523	8	15	22	mV
		V_{ref} = 40mV	7522	36	40	44	mV
			7523	33	40	47	mV
V_{CMF}	Common Mode Input Firing Voltage (See Note 2)	Strobe Input: $V_{inS} = V_{in(1)}$ Common Mode Input Pulse: $t_r = t_f \geq 15ns$, $t_{p(in)} = 50ns$ $T_A = 25°C$			±3		V
I_{in}	Differential Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V			-1	-1.6	mA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
$I_{in(1)}$	Logical 1 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA, V_{in} = 2V		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA, V_{in} = 0.8V			0.2	0.4	V
$I_{out(1)}$	Output Reverse Current	V_{cc1} = 4.75V, V_{cc2} = -4.75V V_{out} = 5.25V, V_{in} = 2V				250	μA
I_{OS}	Output Short Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			27		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			15		mA
$t_{or\ D}$	Differential Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or\ CM}$	Common Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = ±2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum Cycle Time				200		ns

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)D}$	A_1 - A_2 or B_1 - B_2	Y		20		ns
$t_{pd(0)D}$				30	45	ns
$t_{pd(1)S}$	Strobe A or B	Y		15		ns
$t_{pd(0)S}$				25	40	ns
$t_{pd(1)G}$	Gate	Y		10		ns
$t_{pd(0)G}$				15	25	ns

(SEE NOTES PAGE 128)

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7524	11	15	19	mV
			7525	8	15	22	mV
		V_{ref} = 40mV	7524	36	40	44	mV
			7525	33	40	47	mV
V_{CMF}	Common Mode Input Firing Voltage (See Note 2)	Strobe Input: $V_{inS} = V_{in(1)}$ Common Mode Input Pulse: $t_r = t_f \leq 15ns$, $t_{p(in)} = 60ns$ T_A = 25°C			±3		V
I_{in}	Differential Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V			-1	-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA, $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA, $V_{in(0)}$ = 0.8V			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			25		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			-15		mA
$t_{or D}$	Differential Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or CM}$	Common Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = ±2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum Cycle Time				200		ns

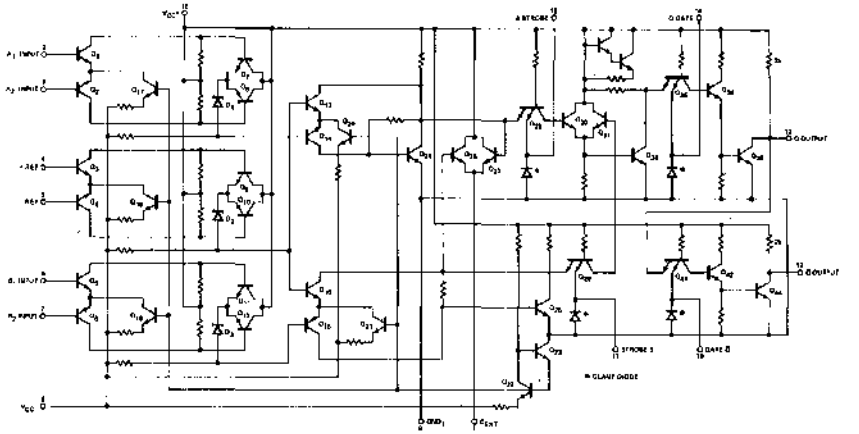
PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)D}$	$A_1 - A_2$ or $B_1 - B_2$	A or B		25	40	ns
$t_{pd(0)D}$				20		ns
$t_{pd(1)S}$	Strobe A or B	A or B		15	30	ns
$t_{pd(0)S}$				20		ns

NOTES:

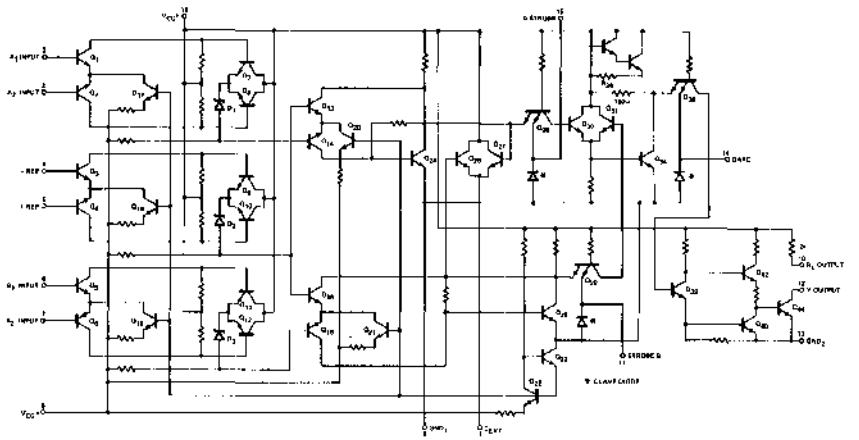
1. The differential input threshold voltage (V_T) is defined as the DC input voltage (V_{in}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
2. Common mode input firing voltage is the common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable signal present.
3. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
4. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

SCHEMATIC DIAGRAMS

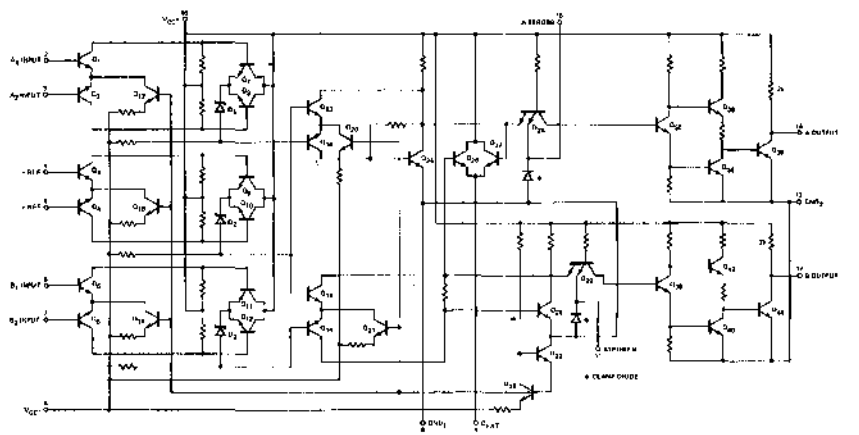
7520/21



7522/23

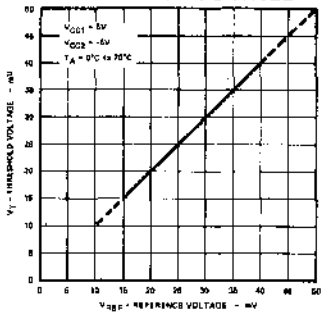


7524/25

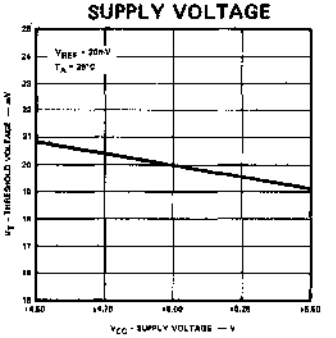


TYPICAL CHARACTERISTIC CURVES

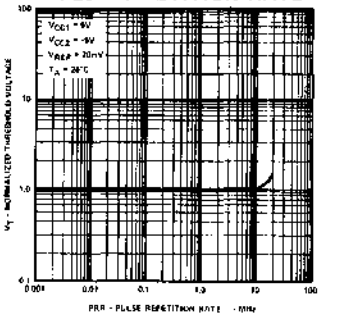
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



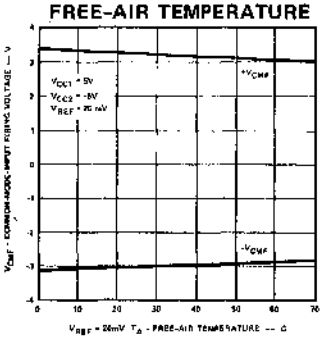
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



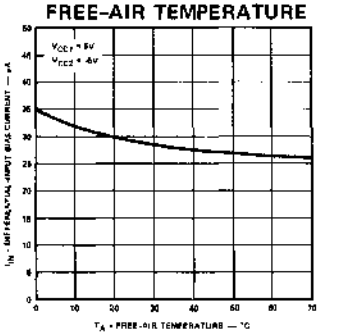
NORMALIZED THRESHOLD VOLTAGE VERSUS PULSE REPETITION RATE



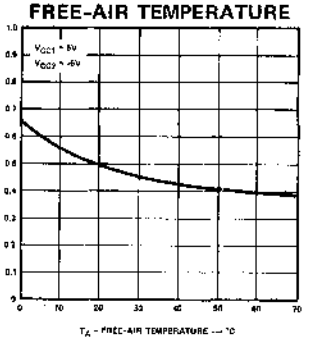
COMMON-MODE FIRING VOLTAGE VERSUS FREE-AIR TEMPERATURE



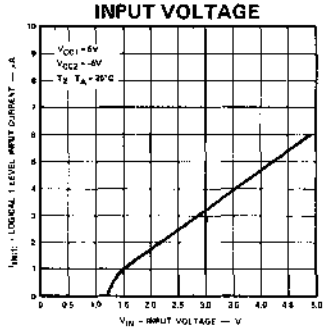
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



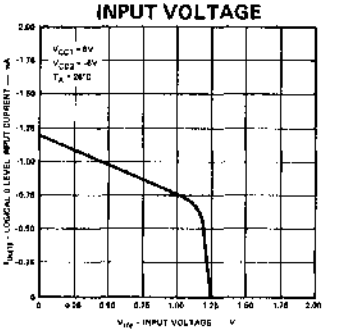
DIFFERENTIAL-INPUT OFFSET CURRENT VS FREE-AIR TEMPERATURE



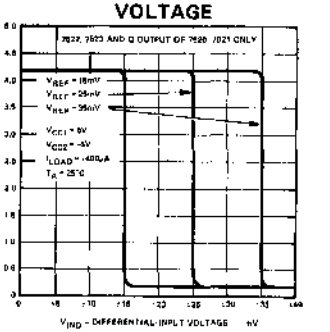
LOGICAL 1 LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



LOGICAL 0 LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE

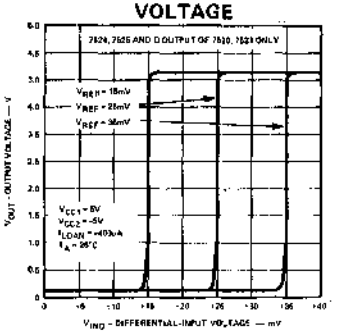


OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE

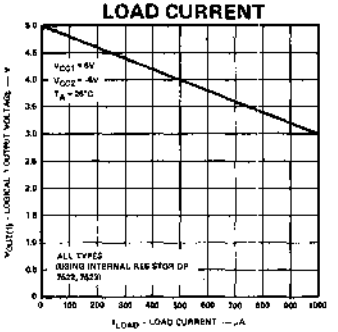


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

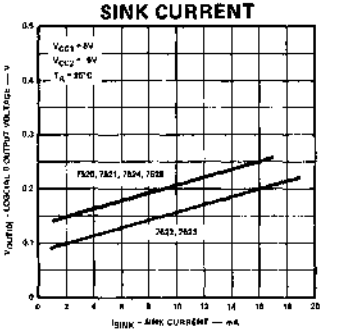
OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE



LOGICAL 1 OUTPUT VOLTAGE VERSUS LOAD CURRENT



LOGICAL 0 OUTPUT VOLTAGE VERSUS SINK CURRENT



SWITCHING CHARACTERISTICS (Propagation Delay Times)

TEST CIRCUIT — DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS

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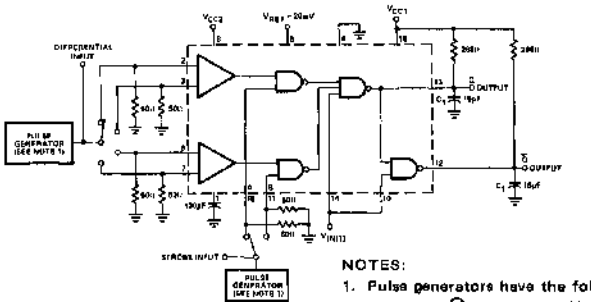
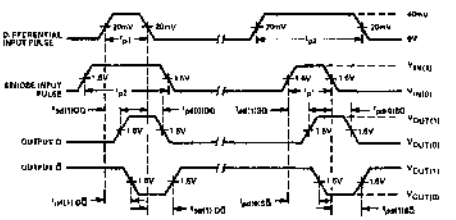
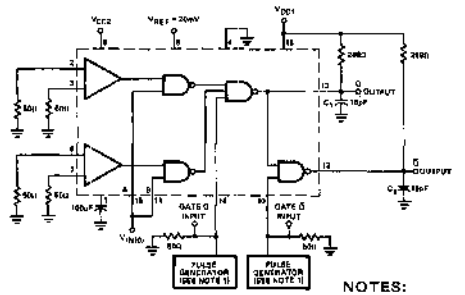


VOLTAGE WAVEFORMS — DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS

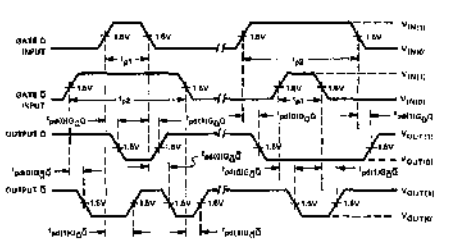


NOTES:
1. Pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 16(\pm5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1 MHz.
2. C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
1. Pulse generators have the following characteristics: $Z_{OUT} = 50\Omega$, $t_r = t_f = 16(\pm5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1 MHz.
2. C_L includes probe and jig capacitance.

SWITCHING CHARACTERISTICS (Propagation Delay Times)(Cont'd)

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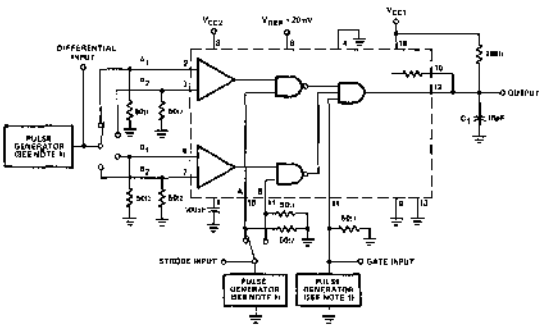
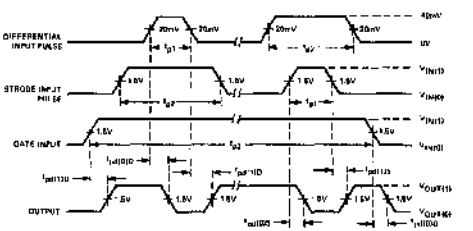
TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:

1. Pulse generators have the following characteristics:
   $Z_{out} = 50\Omega$, $t_r = t_f = 15(\pm 5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs $A_1 - A_2$ are being tested and to Strobe B when inputs $B_1 - B_2$ are being tested.
3. C_1 includes probe and jig capacitance.

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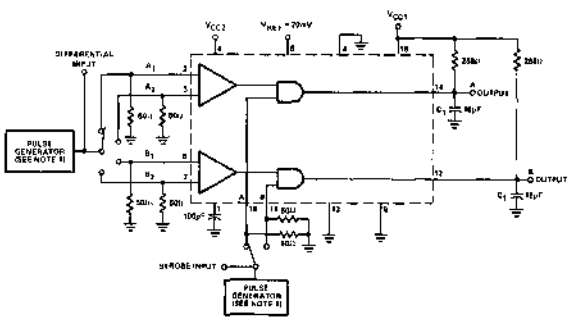
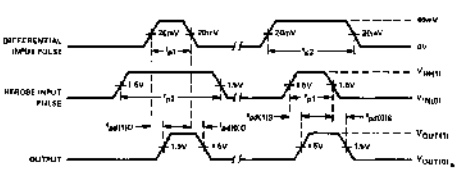
TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:

1. Pulse generators have the following characteristics:
   $Z_{out} = 50\Omega$, $t_r = t_f = 15(\pm 5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs $A_1 - A_2$ are being tested and to Strobe B when inputs $B_1 - B_2$ are being tested.
3. C_1 includes probe and jig capacitance.

DESCRIPTION

The 75450 and 75450A are dual peripheral drivers designed for use in systems that employ TTL or DTL logic. These circuits feature two standard 7400 series gates and two uncommitted, high current, high voltage, npn output driver transistors.

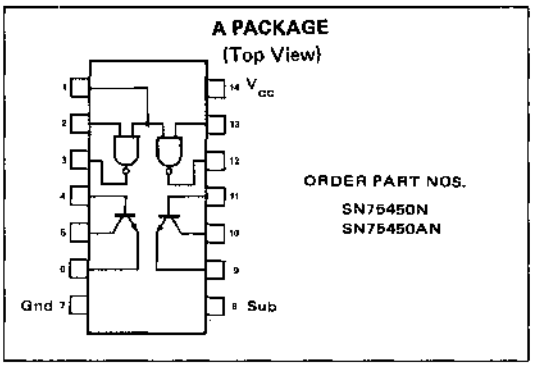
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V
Input Voltage	+5.5V
Collector-Emitter Voltage	+30V
Continuous Collector Current	300mA
Continuous Total Power Dissipation	800mW

NOTES:

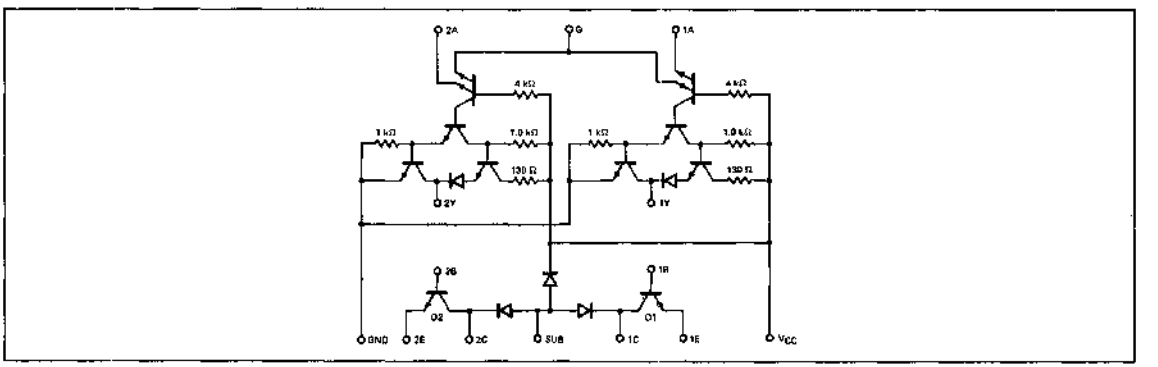
Positive Logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

PIN CONFIGURATION



ORDER PART NOS.
SN75450N
SN75450AN

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS - TTL GATES (V_{CC} = 5V, T_A = 25°C)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage		V_{CC} = 4.75V, I_I = −12mA			−1.5	V
V_{OH}	High-Level Output Voltage		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OH} = −400µA	2.4	3.3		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.75V, V_{IH} = 2V, I_{OL} = 16mA		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A Input G	V_{CC} = 5.25V, V_I = 5.5V			1 2	mA
I_{IH}	High-Level Input Current	Input A Input G	V_{CC} = 5.25V, V_I = 2.4V			40 80	µA
I_{IL}	Low-Level Input Current	Input A Input G	V_{CC} = 5.25V, V_I = 0.4V			−1.6 −3.2	mA
I_{OS}	Short Circuit Output Current		V_{CC} = 5.25V	−18		−55	mA
I_{CCH}	Supply Current, High-Level Output		V_{CC} = 5.25V, V_I = 0		2	4	mA
I_{CCL}	Supply Current, Low-Level Output		V_{CC} = 5.25V, V_I = 5V		6	11	mA

ELECTRICAL CHARACTERISTICS - OUTPUT TRANSISTORS (Cont'd)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)\,CBO}$ Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0	35			V
$V_{(BR)\,CER}$ Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω	30			V
$V_{(BR)\,EBO}$ Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0	5			V
h_{FE} Static Forward Current Transfer Ratio	V_{CE} = 3V, I_C = 100mA, T_A = 25°C	25			
	V_{CE} = 3V, I_C = 300mA, T_A = 25°C	30			
	V_{CE} = 3V, I_C = 100mA T_A = 0°C	20			
	V_{CE} = 3V, I_C = 300mA, T_A = 0°C	25			
V_{BE} Base-Emitter Voltage	I_B = 10mA, I_C = 100mA		0.85	1	V
	I_B = 30mA, I_C = 300mA		1.05	1.2	V
$V_{CE\,(sat)}$ Collector-Emitter Saturation Voltage	I_B = 10mA, I_C = 100mA		0.25	0.4	V
	I_B = 30mA, I_C = 300mA		0.5	0.7	V

SWITCHING CHARACTERISTICS - TTL GATES (V_{CC} = 5V, T_A = 25°C)

PARAMETER	TEST CONDITIONS	75450			75450A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL GATES								
t_{PLH} Propagation Delay Time Low-to-High-Level Output	C_L = 15pF, R_L = 400Ω		12	22		20		ns
t_{PHL} Propagation Delay Time, High-to-High-Level Output			8	15		8		ns
OUTPUT TRANSISTORS								
t_D Delay Time	I_C = 200mA, $I_{B(1)}$ = 20mA		8	15		8		ns
t_r Rise Time	$I_{B(2)}$ = −40mA,		12	20		12		ns
t_s Storage Time	$V_{BE(off)}$ = −1V		7	15		7		ns
t_f Fall Time	C_L = 15pF, R_L = 50		6	15		6		ns
GATES AND TRANSISTORS COMBINED								
t_{PLH} Propagation Delay Time, Low-to-High-Level Output	I_C = 200mA, C_L = 15pF, R_L = 50		17			40		ns
t_{PHL} Propagation Delay Time, High-to-Low-Level Output			16			25		ns
t_{TLH} Transition Time, Low-to-High-Level Output			7			10		ns
t_{THL} Transition Time, High-to-Low-Level Output			9			12		ns

DESCRIPTION

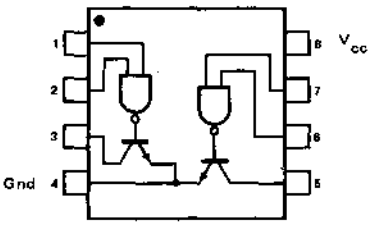
The SN75451 and SN75451A dual peripheral drivers are versatile devices designed for use in systems that employ TTL or DTL logic. These circuits are dual AND drivers (positive logic) with the gate outputs internally connected to the npn output transistors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	+7V
Input Voltage	+5.5V
Output Voltage	+30V
Continuous Output Current	300mA
Continuous Power Dissipation	800mW
Positive Logic	Y = AB

PIN CONFIGURATION

V PACKAGE
(Top View)

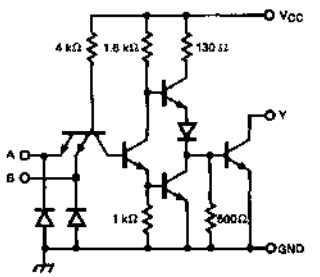


ORDER PART NO. SN75451P/SN75451AP

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

EQUIVALENT CIRCUIT (Each Driver)



ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.75V, I_I = −12mA			−1.5	V
I_{OH}	High-Level Output Current	V_{CC} = 4.75V, V_{IH} = 2V, V_{OH} = 30V			100	μA
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 100mA		0.25	0.4	V
		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 300mA		0.5	0.7	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_I = 5.5V			1	mA
I_{IH}	High-Level Input Current	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Low-Level Input Current	V_{CC} = 5.25V, V_I = 0.4V		−1	−1.6	mA
I_{CCH}	Supply Current, High-Level Output	V_{CC} = 5.25V, V_I = 5V		7	11	mA
I_{CCL}	Supply Current, Low-Level Output	V_{CC} = 5.25V, V_T = 0		52	65	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER	TEST CONDITIONS	75451			75451A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation Delay Time Low-toHigh-Level Output			20	25		45		ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	$I_O \approx 200mA, C_L = 15pF$		20	30		25		ns
t_{TLH} Transition Time, Low-to-High-Level Output	$R_L = 50\Omega$		10			10		ns
t_{THL} Transition Time, High-to-Low-Level Output			10			12		ns

DESCRIPTION

The DM8880 is a High Voltage Seven-Segment Decoder/Driver designed to decode BCD and drive gas filled seven-segment display tubes.

Decoding is performed by a 16x7 read only memory. Thus, for applications desiring other fonts, or applications not using standard BCD inputs, the ROM contents can be altered via metal mask change to produce any seven-segment combination for any 16 binary input combinations.

The output of the ROM is used to drive high voltage constant current sink generators. The current sinks will withstand 80V output min. The current sinks are ratioed to the B output current as required for even illumination of the segments. Output currents may be varied over a 0.2 to 1.5 mA range through use of the external current programming input.

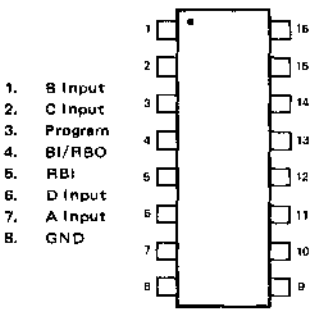
Blanking input provides unconditional blanking of any output display, while the ripple blanking pins allow simple leading or trailing zero blanking.

FEATURES

- CURRENT SOURCE OUTPUTS
- ADJUSTABLE OUTPUT CURRENT – 0.2 TO 1.5 mA
- HIGH OUTPUT BREAKDOWN VOLTAGE – 110V TYP
- SUITABLE FOR MULTIPLEX OPERATION
- BLANKING AND RIPPLE BLANKING PROVISIONS
- LOW FAN-IN AND LOW POWER

PIN CONFIGURATION

B PACKAGE

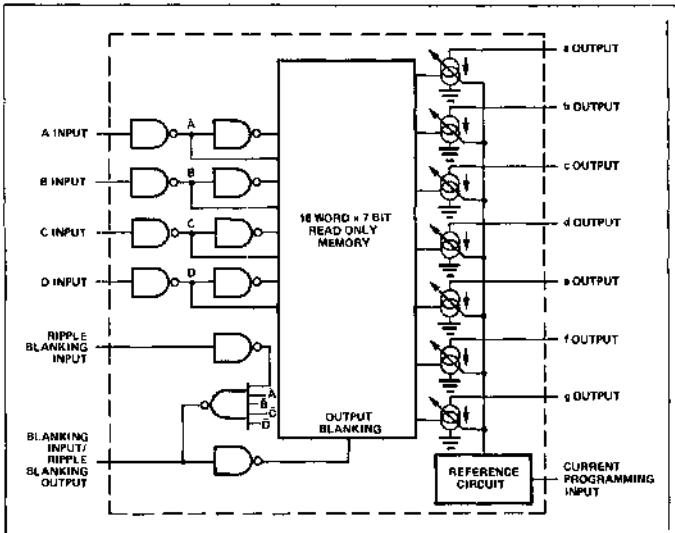


1. B Input
2. C Input
3. Program
4. BI/RBO
5. RBI
6. D Input
7. A Input
8. GND

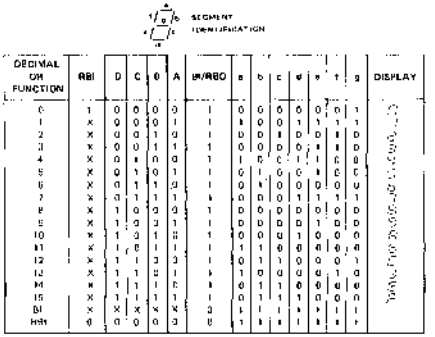
16. V_{CC}
15. f Output
14. g Output
13. a Output
12. b Output
11. c Output
10. d Output
9. e Output

ORDER PART
DM8880N-16

LOGIC AND CONNECTION DIAGRAMS



TRUTH TABLE



DECIMAL OR FUNCTION	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	
1	X	0	0	0	1	1	1	0	0	1	1	1	1	
2	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	X	0	1	1	0	1	0	1	0	0	0	0	0	
7	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	X	1	0	0	1	1	0	0	0	0	1	0	0	
10	X	1	0	1	0	1	1	1	1	0	0	0	0	
11	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	X	1	1	1	0	1	1	1	1	1	0	0	0	
15	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	0	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

ABSOLUTE MAXIMUM RATINGS

V_{CC}	7V	Power Dissipation (Note 1)	600mW
Input Voltage (Except B1)	6V	Operating Temperature Range	0°C to 70°C
Input Voltage (B1)	V_{CC}	Storage Temperature Range	−65°C to 150°C
Segment Output Voltage	80V	Lead Temperature (Soldering, 10 sec)	300°C

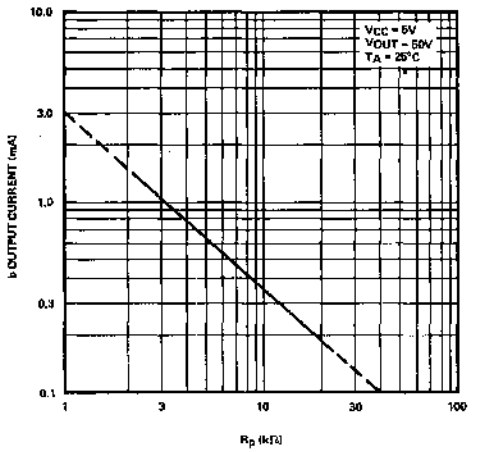
ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logic "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logic "1" Output Voltage (RBO)	V_{CC} = 4.75V, I_{OUT} = −200μA	2.4	3.7		V
Logic "0" Output Voltage (RBO)	V_{CC} = 4.75V, I_{OUT} = 8mA		0.13	0.4	V
Logic "1" Input Current (Except B1)	V_{CC} = 5.25V, V_{IN} = 2.4V		2	15	μA
	V_{CC} = 5.25V, V_{IN} = 5.5V		4	400	μA
Logic "0" Input Current (Except B1)	V_{CC} = 5.25V, V_{IN} = 0.4V		−300	−600	μA
Logic "0" Input Current (B1)	V_{CC} = 5.25V, V_{IN} = 0.4V		−1.2	−2.0	mA
Power Supply Current	V_{CC} = 5.25V, All Inputs = 0V, R_P = 2.2k		27	43	mA
Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12mA, T_A = 25°C		−0.9	−1.5	V
Segment Outputs:					
Outputs a, f, g On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.88	0.93	0.98	
Output c On Current Ratio	All Outputs = 50 V, Output b Curr. = Ref.	1.19	1.25	1.31	
Output d On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.95	1.00	1.05	
Output e On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	1.04	1.10	1.16	
Output b On Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 18.1k	0.18	0.20	0.22	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 7.03k	0.45	0.50	0.55	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 3.40k	0.90	1.00	1.10	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 2.20k	1.45	1.50	1.65	mA
Output Saturation Voltage	V_{CC} = 4.75V, I_{OUT} = 2mA, R_P = 1k ±5%		0.8	2.5	V
Output Leakage Current	V_{OUT} = 75V, BI = 0V		.003	3	μA
Output Breakdown Voltage	I_{OUT} = 250μA, BI = 0V	80	110		V
Propagation Delays:					
BCD Input to Segment Output	V_{CC} = 5V, T_A = 25°C		0.4	10	μs
BI to Segment Output	V_{CC} = 5V, T_A = 25°C		0.4	10	μs
RBI to Segment Output	V_{CC} = 5V, T_A = 25°C		0.7	10	μs
RBI to RBO	V_{CC} = 5V, T_A = 25°C		0.4	10	μs

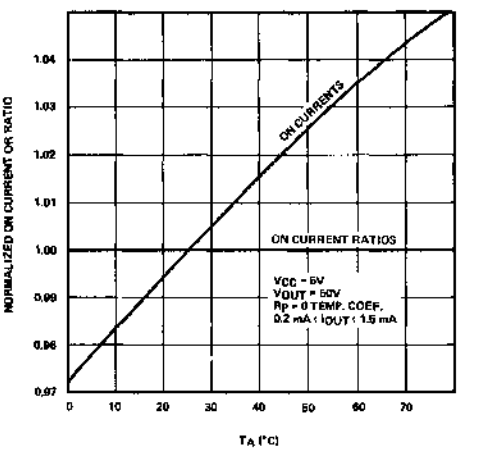
Note 1: Min/max limits apply across the guaranteed operating temperature range of 0°C to 70°C unless otherwise specified. Typicals are for V_{CC} = 5V, T_A = 25°C. Positive current is defined as current into the referenced pin.

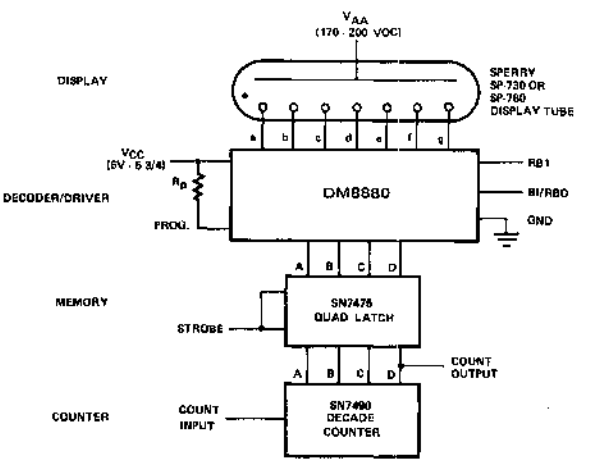
TYPICAL APPLICATION

OUTPUT CURRENT PROGRAMMING



ON CURRENTS vs. TEMPERATURE





DESCRIPTION

The LM101A, LM201A, and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

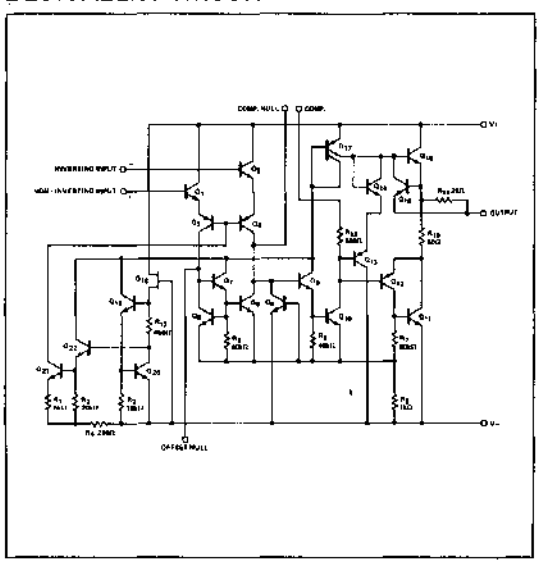
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	LM101A/LM201A	±22V
	LM301A	±18V
Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM101A	-55°C to 125°C
	LM201A	-25°C to 85°C
	LM301A	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES:

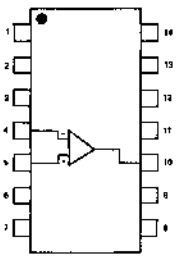
1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101A and 100°C for the LM201A and the LM301A. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

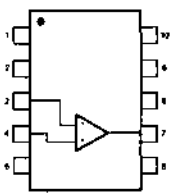
A & I PACKAGE (Top View)



1. NC
2. NC
3. Freq. Comp./Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq. Comp.
13. NC
14. NC

ORDER PART NOS.
LM101AD/LM201A/LM301AD LM101AN-14/LM301AN-14/ LM301AN-14

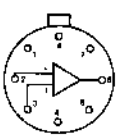
Q PACKAGE



1. NC
2. Bal/Comp
3. Input
4. Input
5. V^-
6. Bal
7. Output
8. V^+
9. Comp
10. NC

ORDER PART NOS.
LM101AQ/LM201AQ/LM301AQ

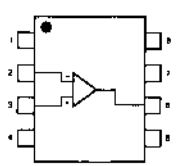
T PACKAGE



1. Freq. Comp/Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
LM101AH/LM201AH/LM301AH

V PACKAGE



1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NO.
LM101AN/LM201AN/LM301AN

ELECTRICAL CHARACTERISTICS

LM101A: $-55°C \leq T_A \leq 125°C$
LM201A: $-25°C \leq T_A \leq 85°C$ $\pm 5V \leq V_S \leq \pm 20V$ and $C_1 = 30pF$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		0.7	2.0	mV
Input Offset Current	$T_A = 25°C$		1.5	10	nA
Input Bias Current	$T_A = 25°C$		30	75	nA
Input Resistance	$T_A = 25°C$	1.5	4		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	60	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		dB

LM301A

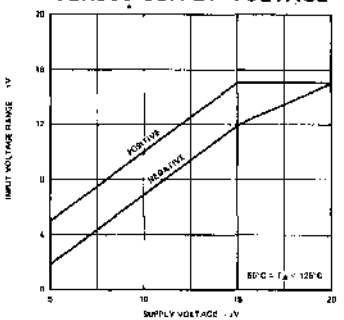
ELECTRICAL CHARACTERISTICS ($0°C \leq T_A < 70°C$, $\pm 5V \leq V_S \leq \pm 15V$ and $C_1 = 30pF$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		3	50	nA
Input Bias Current	$T_A = 25°C$		70	250	nA
Input Resistance	$T_A = 25°C$	0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$; $R_L \geq 2k\Omega$	25	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	μV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	70	96		dB

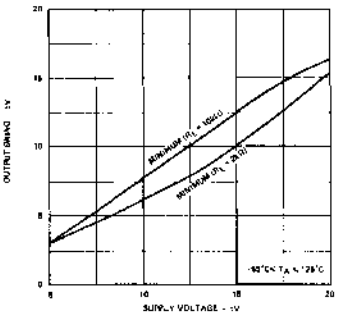
TYPICAL CHARACTERISTIC CURVES

LM101A/LM201A/

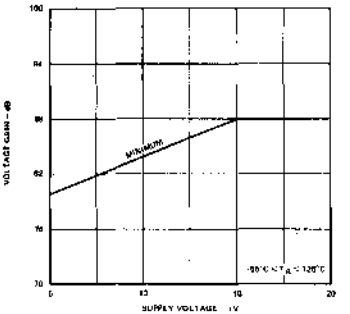
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

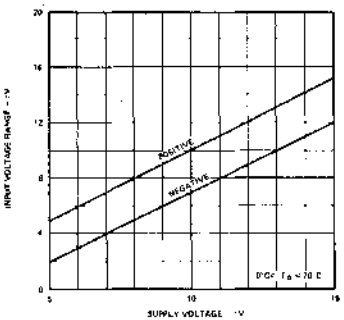


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

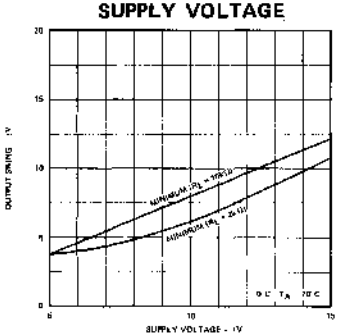


LM301A

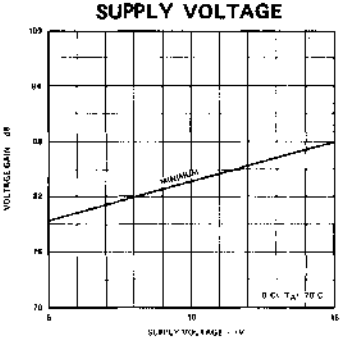
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

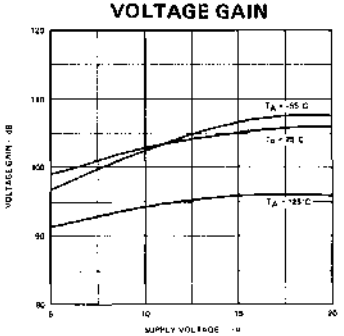


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

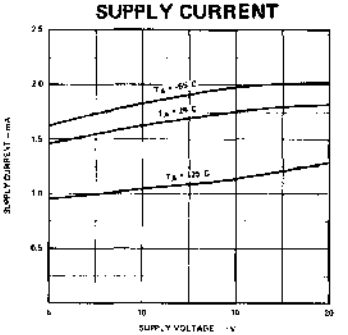


LM101A/LM201A

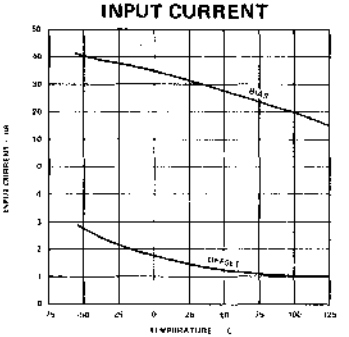
VOLTAGE GAIN



SUPPLY CURRENT



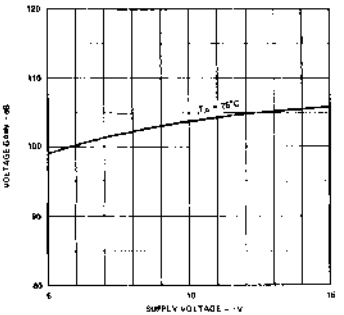
INPUT CURRENT



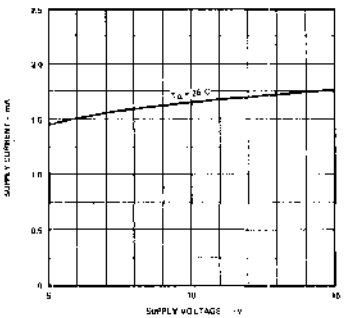
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

LM301A

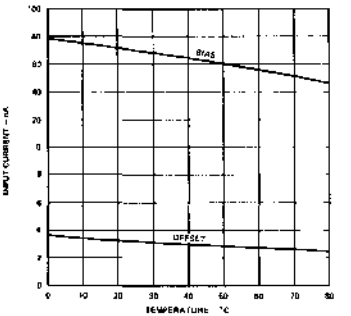
VOLTAGE GAIN



SUPPLY CURRENT

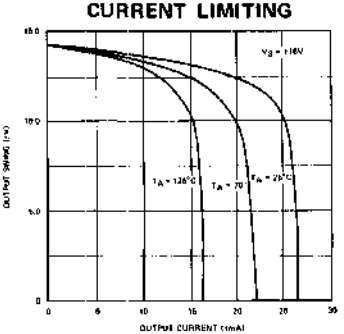


INPUT CURRENT

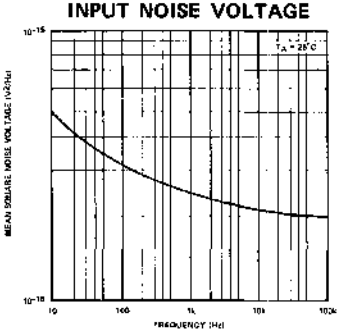


LM101A/LM201A/LM301A

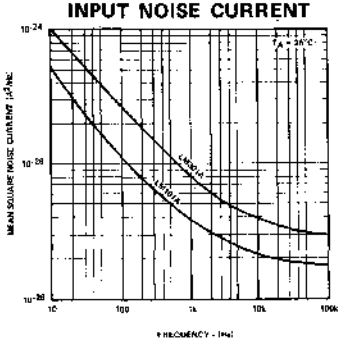
CURRENT LIMITING



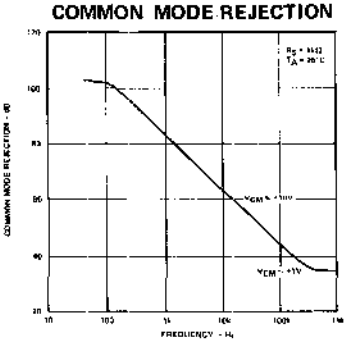
INPUT NOISE VOLTAGE



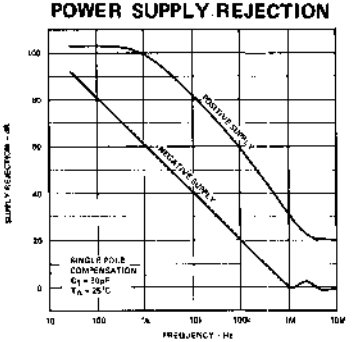
INPUT NOISE CURRENT



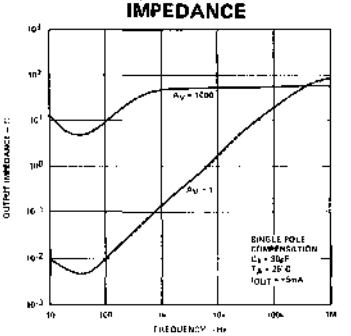
COMMON MODE REJECTION



POWER SUPPLY REJECTION

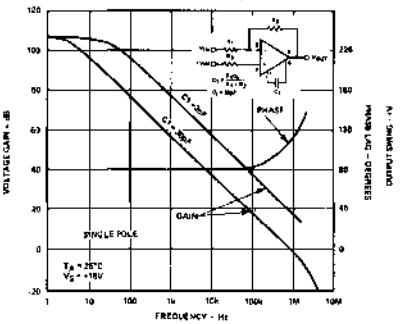


CLOSED LOOP OUTPUT IMPEDANCE

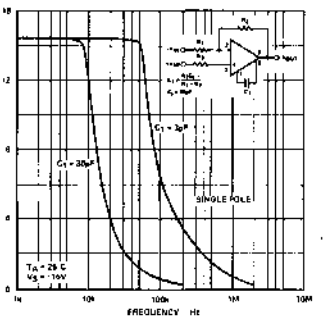


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

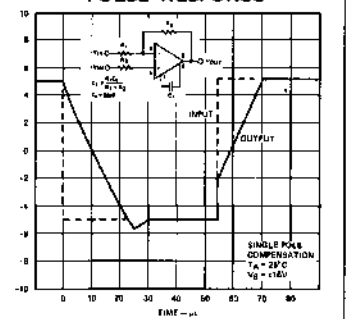
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



DESCRIPTION

The LM101 and LM201 are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

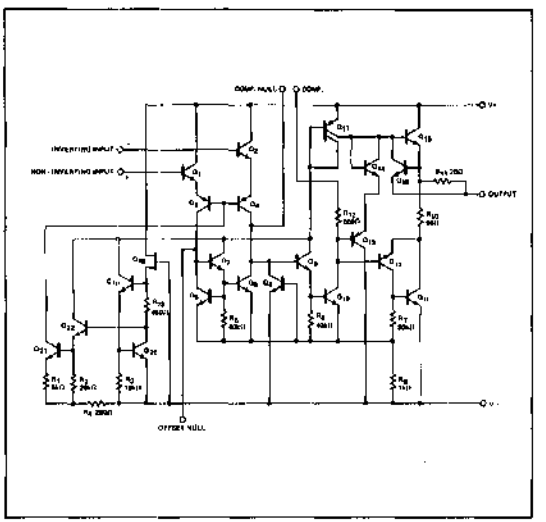
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±22V
Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM101	−55°C to 125°C
	LM201	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES

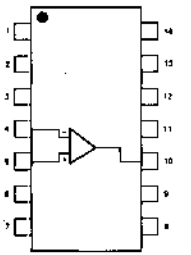
1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101 and 100°C for the LM201. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

A & I PACKAGE (Top View)

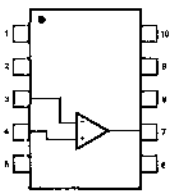


1. NC
2. NC
3. Freq. Comp./Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq. Comp.
13. NC
14. NC

ORDER PART NOS.

LM101N-14, LM201N-14 } Silicone — LM101D, LM201D } Ceramic

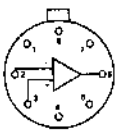
Q PACKAGE



1. NC
2. Bal/Comp
3. Input
4. Input
5. V^-
6. Bal
7. Output
8. V^+
9. Comp
10. NC

ORDER PART NOS.
LM101Q/LM201Q

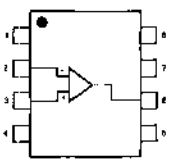
T PACKAGE



1. Freq. Comp/Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
LM101H/LM201H

V PACKAGE



1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NO. LM201N

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$, $\pm 15V \leq V_S \leq \pm 20V$ and $C_1 = 30$ pF unless otherwise specified).

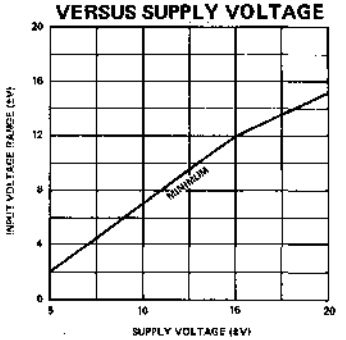
LM101 PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_s \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		40	200	nA
Input Bias Current	$T_A = 25°C$		120	500	nA
Input Resistance	$T_A = 25°C$	300	800		kΩ
Supply Current	$T_A = 25°C$, $V_s = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_s = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
Input Offset Voltage	$R_s \leq 10k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s \leq 50\Omega$		3.0		μV/°C
	$R_s \leq 10k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		100	500	nA
Input Bias Current	$T_A = -55°C$		0.28	1.5	μA
Supply Current	$T_A = +125°C$, $V_s = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_s = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_s = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_s = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_s \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_s \leq 10k\Omega$	70	90		dB

LM201 PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_s \leq 10k\Omega$		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		100	500	nA
Input Bias Current	$T_A = 25°C$		0.25	1.5	μA
Input Resistance	$T_A = 25°C$	100	400		kΩ
Supply Current	$T_A = 25°C$, $V_s = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_s = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	20	150		V/mV
Input Offset Voltage	$R_s \leq 10k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s \leq 50\Omega$		6		μV/°C
	$R_s \leq 10k\Omega$		10		μV/°C
Input Offset Current	$T_A = +70°C$		50	400	nA
	$T_A = 0°C$		150	750	nA
Input Bias Current	$T_A = 0°C$		0.32	2.0	μA
Large Signal Voltage Gain	$V_s = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_s = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_s \leq 10k\Omega$	65	90		dB
S Supply Voltage Rejection Ratio	$R_s \leq 10k\Omega$	70	90		dB

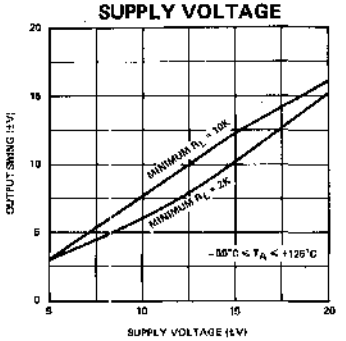
TYPICAL CHARACTERISTIC CURVES

LM101

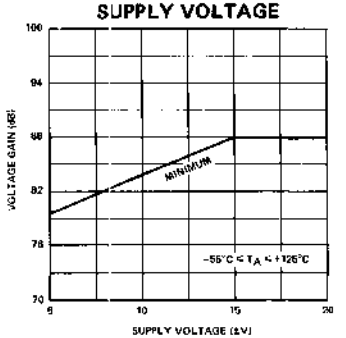
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

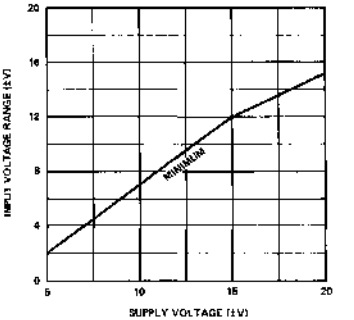


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

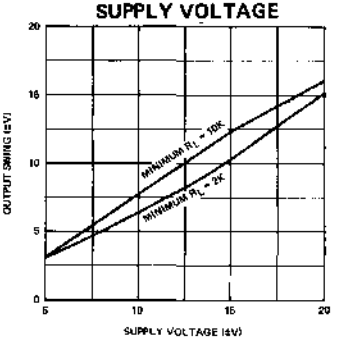


LM201

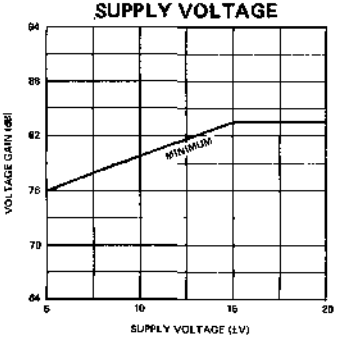
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE



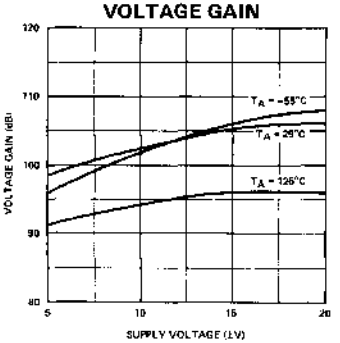
VOLTAGE GAIN VERSUS SUPPLY VOLTAGE



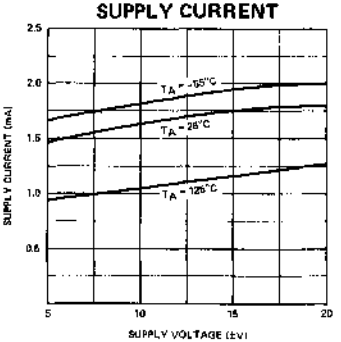
(Cont'd.)

LM101

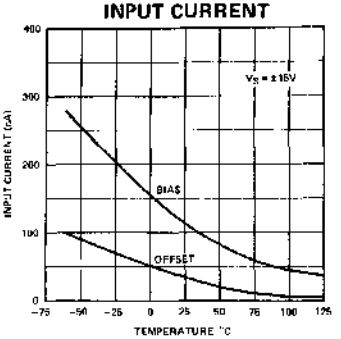
VOLTAGE GAIN



SUPPLY CURRENT

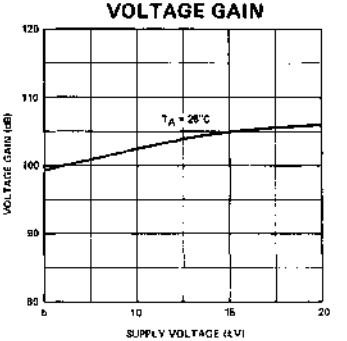


INPUT CURRENT

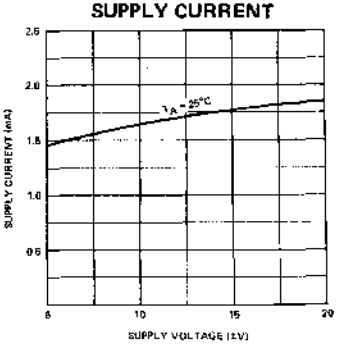


LM201

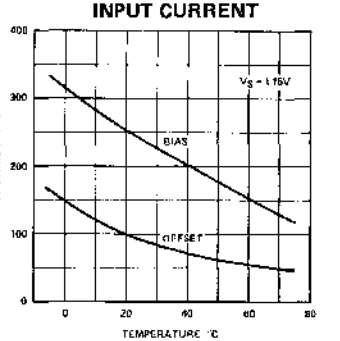
VOLTAGE GAIN



SUPPLY CURRENT



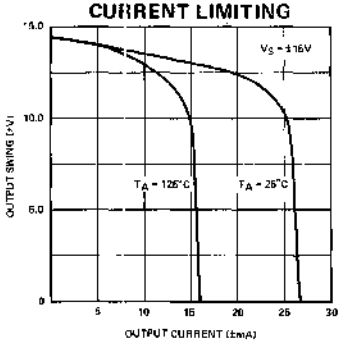
INPUT CURRENT



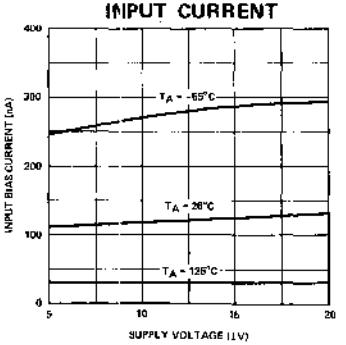
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

LM101

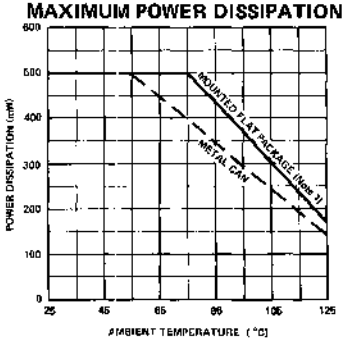
CURRENT LIMITING



INPUT CURRENT

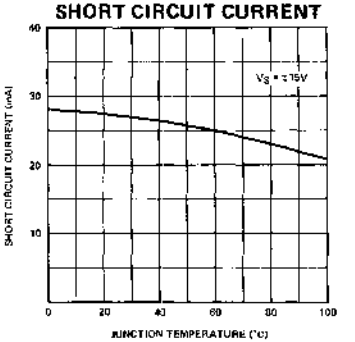


MAXIMUM POWER DISSIPATION

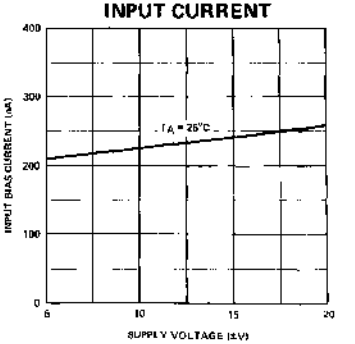


LM201

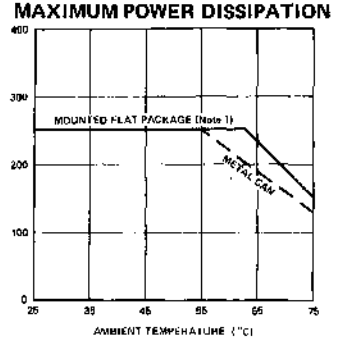
SHORT CIRCUIT CURRENT



INPUT CURRENT

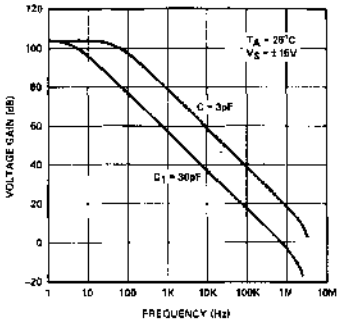


MAXIMUM POWER DISSIPATION

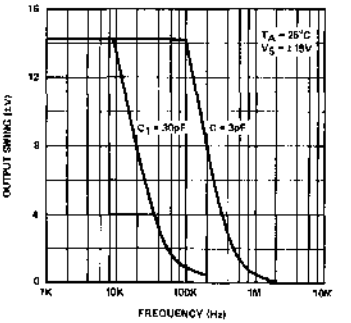


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

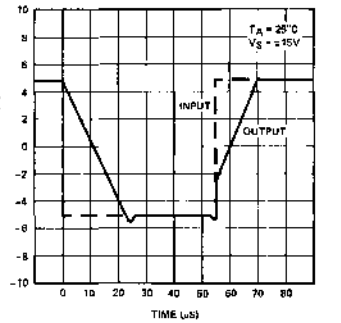
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

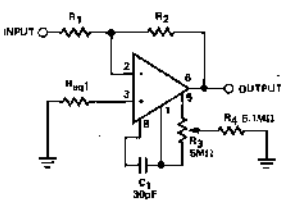


VOLTAGE FOLLOWER PULSE RESPONSE



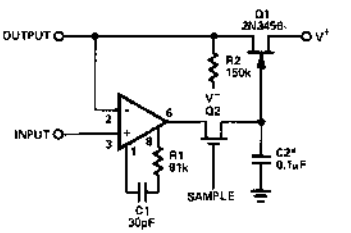
TYPICAL APPLICATIONS (Pin numbers shown refer to T or V package only)

INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

LOW DRIFT SAMPLE AND HOLD



*POLYCARBONATE DIELECTRIC CAPACITOR

DESCRIPTION

The LM107/207/307 is a general purpose internally compensated operational amplifier. Advanced processing techniques provide input currents which are an order of magnitude lower than the μA709. Standard pin out allows plug in replacement for the μA709, LM101, LM101A, and the μA741.

FEATURES

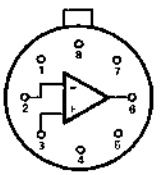
- 3mV MAX OFFSET VOLTAGE OVER TEMP
- 100 nA MAX INPUT CURRENT OVER TEMP
- 20 nA MAX INPUT OFFSET CURRENT OVER TEMP
- OFFSETS GUARANTEED OVER COMMON MODE RANGE
- INPUT/OUTPUT SHORT CIRCUIT PROTECTED

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	LM107	±22V
	LM307	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short-Circuit Duration (Note 3)		Indefinite
Operating Temperature Range	LM107	−55°C to 125°C
	LM207	−25°C to 85°C
	LM307	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 60 sec)		300°C

PIN CONFIGURATIONS

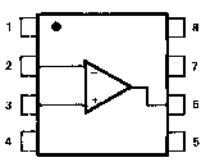
T PACKAGE
(Top View)



1. NC
2. Inverting Input
3. Noninverting Input
4. V^-
5. NC
6. Output
7. V^+
8. NC

ORDER PART NOS.
LM107H/LM207H/LM307H

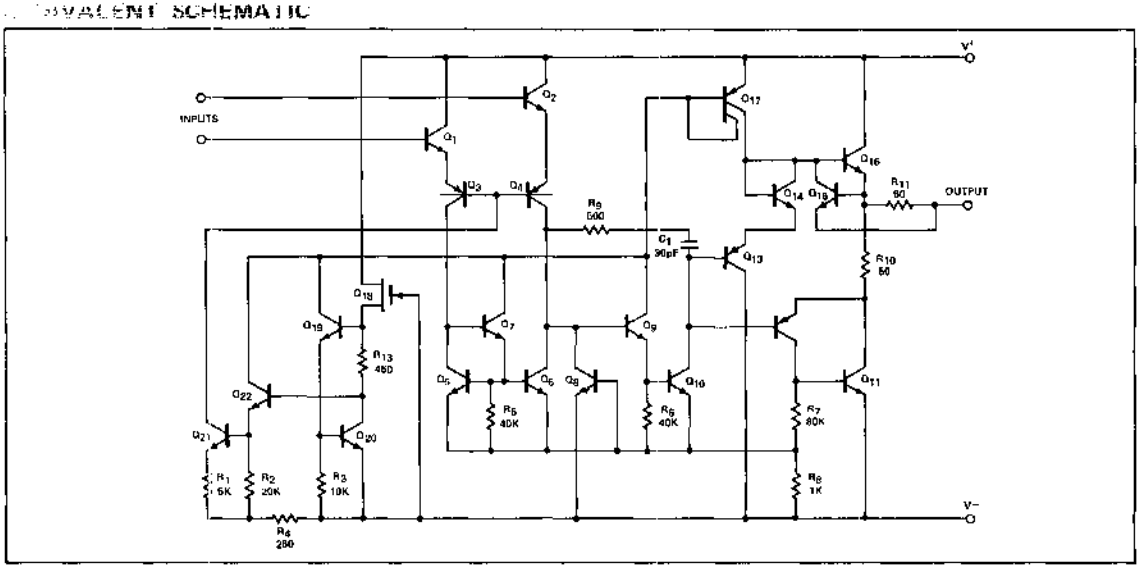
V PACKAGE



1. NC
2. Inverting Input
3. Noninverting Input
4. V^-
5. NC
6. Output
7. V^+
8. NC

ORDER PART NO.
LM107N/LM207N/LM307N

EQUIVALENT SCHEMATIC



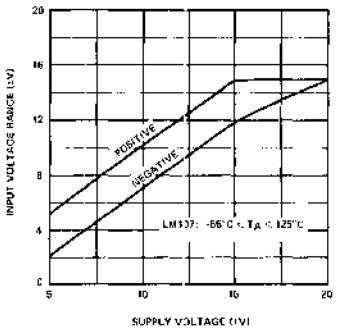
ELECTRICAL CHARACTERISTICS

		LM101/207			LM307			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10K\Omega$	–	0.7	2.0	–	–	–	mV
	$T_A = 25°C$, $R_S \leq 50K\Omega$	–	–	–	–	2.0	7.5	–
Input Offset Current	$T_A = 25°C$	–	1.5	10	–	3	50	nA
Input Bias Current	$T_A = 25°C$	–	30	75	–	70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4	–	0.5	2	–	MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	–	1.8	3.0	–	–	–	mA
	$T_A = 25°C$, $V_S = \pm 15V$	–	–	–	–	1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	50	160	–	25	160	–	V/mV
Input Offset Voltage	$R_S \leq 10K\Omega$	–	–	3.0	–	–	–	mV
	$R_S \leq 50K\Omega$	–	–	–	–	–	10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	–	6.0	30	μV/°C
Input Offset Current		–	–	20	–	–	70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$	–	0.01	0.1	–			nA/°C
	$-55°C \leq T_A \leq 25°C$	–	0.02	0.2	–			nA/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$	–	–	–	–	0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$	–	–	–	–	0.02	0.6	nA/°C
Input Bias Current		–	–	100	–	–	300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	–	1.2	2.5	–	–	–	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	25	–	–	15	–	–	V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10K\Omega$	±12	±14	–	±12	±14	–	V
	$R_L = 2K\Omega$	±10	±13	–	±10	±13	–	V
Input Voltage Range	$V_S = \pm 20V$	±15	–	–	–	–	–	V
	$V_S = \pm 15V$	–	–	–	±12	–	–	V
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	80	96	–	–	–	–	dB
	$R_S \leq 50K\Omega$	–	–	–	70	90	–	dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$	80	96	–	–	–	–	dB
	$R_S \leq 50K\Omega$	–	–	–	70	96	–	dB

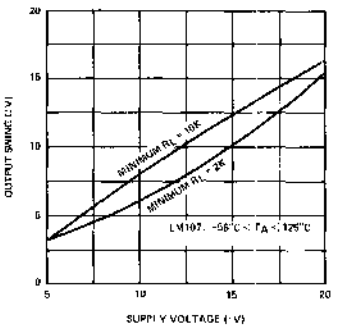
NOTES:
1. For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case (for T Package).
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.
4. The specifications apply for -55°C to 125°C for LM107 and 0°C to 70°C for LM307 unless otherwise specified.
5. $\pm 5V \leq V_S \leq \pm 15V$ unless otherwise specified.

LM107/207

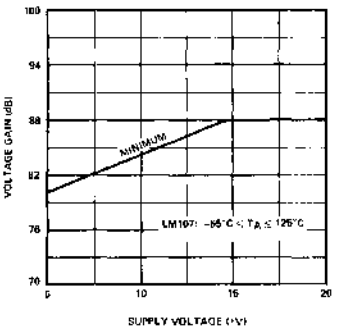
INPUT VOLTAGE RANGE



OUTPUT SWING

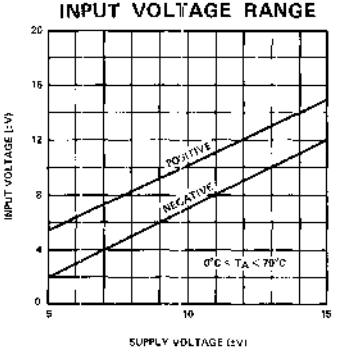


VOLTAGE GAIN

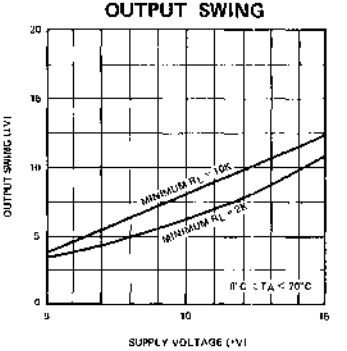


LM307

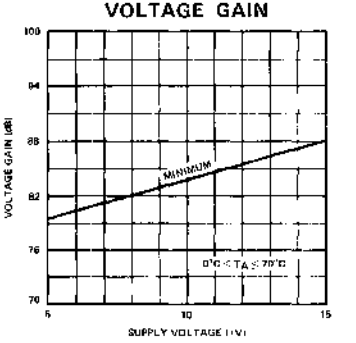
INPUT VOLTAGE RANGE



OUTPUT SWING

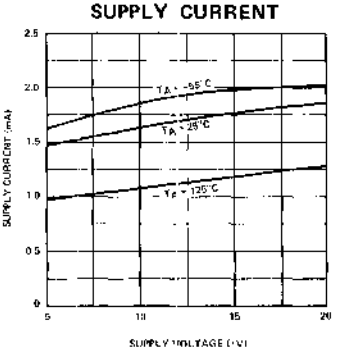


VOLTAGE GAIN

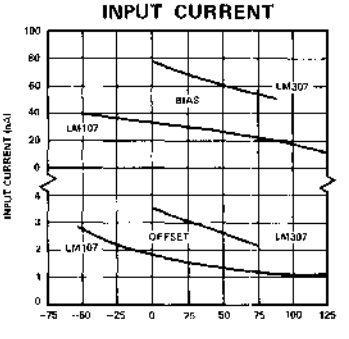


TYPICAL PERFORMANCE CURVES

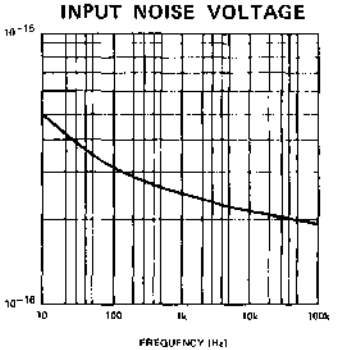
SUPPLY CURRENT



INPUT CURRENT

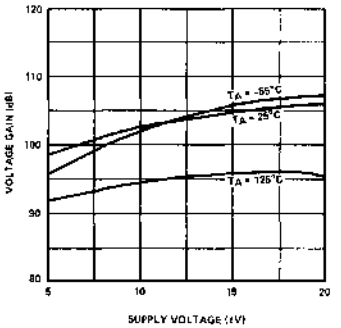


INPUT NOISE VOLTAGE

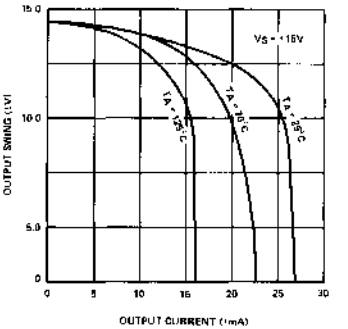


TYPICAL PERFORMANCE CURVES (cont'd)

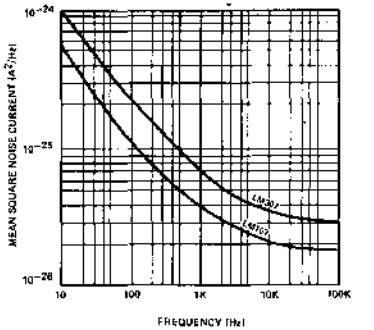
VOLTAGE GAIN



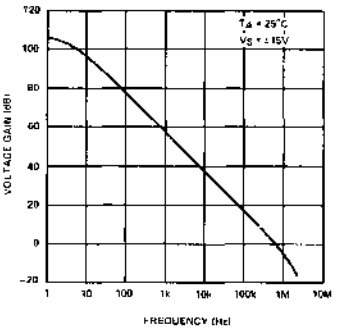
CURRENT LIMITING



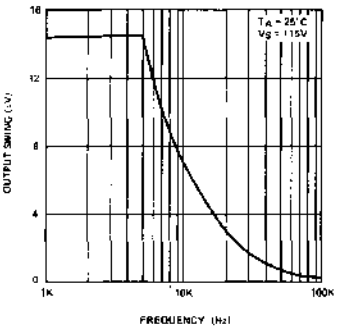
INPUT NOISE CURRENT



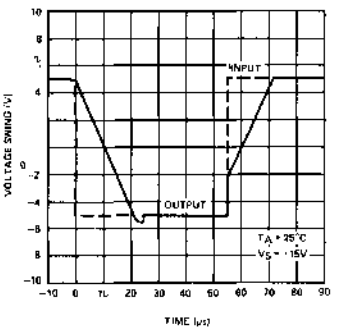
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

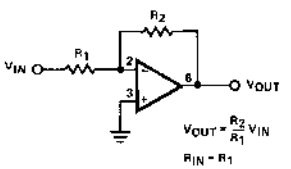


VOLTAGE FOLLOWER PULSE RESPONSE

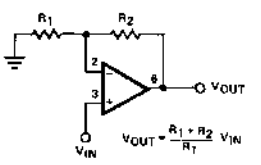


TYPICAL APPLICATIONS

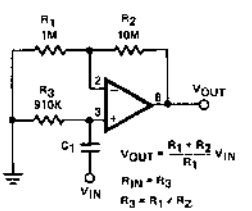
INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



NON-INVERTING AC AMPLIFIER



DESCRIPTION

The LM109 and LM309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blow-out proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

FEATURES

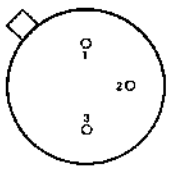
- **OUTPUT CURRENTS IN EXCESS OF 1 amp**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL CURRENT LIMITING**
- **NO EXTERNAL COMPONENTS REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	-55°C to 150°C
LM309	0°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATIONS

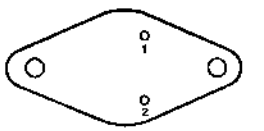
H PACKAGE
(Bottom View)



1. Input
2. Output
3. Ground

ORDER PART NOS. LM109H/LM209H/LM309H

K PACKAGE
(Bottom View)

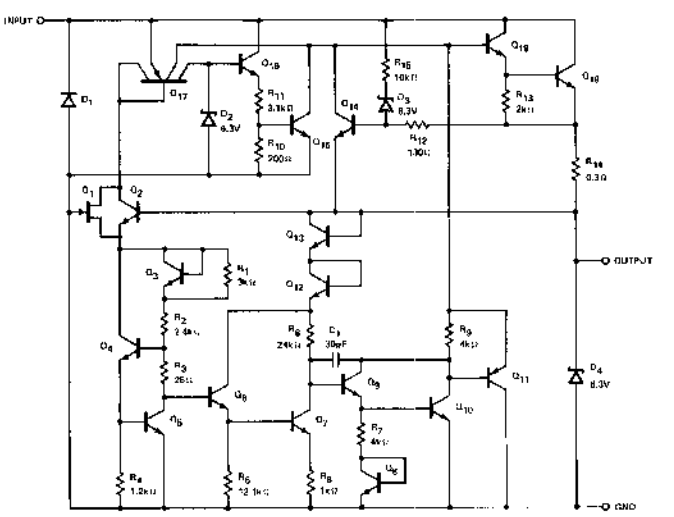


1. Input
2. Output

Case is connected to ground.

ORDER PART NOS. LM109K/LM209K/LM309K

EQUIVALENT CIRCUIT



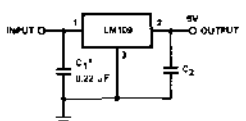
(Note 1)

PARAMETER	CONDITIONS	LM109			LM309			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$							
	$7V \leqslant V_{IN} \leqslant 25V$		4	50		4	50	mV
Load Regulation	$T_j = 25°C$							
TO-5	$5mA \leqslant I_{OUT} \leqslant 0.5A$		20	50		20	50	mV
TO-3	$5mA \leqslant I_{OUT} \leqslant 1.5A$		50	100		50	100	mV
Output Voltage	$7V \leqslant V_{IN} \leqslant 25V$							
	$5mA \leqslant I_{OUT} \leqslant I_{max}$							
	$P < P_{max}$	4.6		5.4	4.75		5.25	V
Quiescent Current	$7V \leqslant V_{IN} \leqslant 25V$		5.2	10		5.2	10	mA
Quiescent Current Change	$7V \leqslant V_{IN} \leqslant 25V$			0.5			0.5	mA
	$5mA \leqslant I_{OUT} \leqslant I_{max}$			0.8			0.8	mA
Output Noise Voltage	$T_A = 25°C$							
	$10Hz \leqslant f \leqslant 100\ kHz$		40			40		μV
Long Term Stability				10			20	mV
Thermal Resistance								
Junction to Case (Note 2)								
TO-5			15			15		°C/W
TO-3			3			3		°C/W

NOTES:

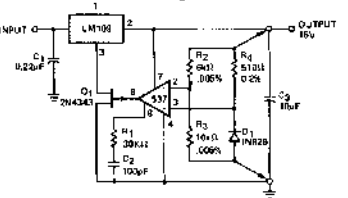
1. Unless otherwise specified, these specifications apply for $-55°C \leqslant T_j \leqslant 150°C$ for the 5109 or $0°C \leqslant T_j \leqslant 125°C$ for the 5309, V_{IN} = 10V and I_{OUT} = 0.1A for the TO-5 package or I_{OUT} = 0.5A for the TO-3 package. For the TO-5 package, I_{max} = 0.2A and P_{max} = 2.0W. For the TO-3 package, I_{max} = 1.0A and P_{max} = 20W.
2. Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

FIXED 5V REGULATOR



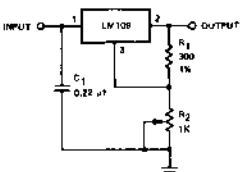
NOTES: *Required if regulator is located an appreciable distance from power supply filter.
†Although no output capacitor is needed for stability, it does improve transient response.

PRECISION VOLTAGE REGULATOR

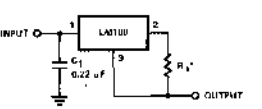


NOTES: *Regulation better than 0.01% load, line and temperature, can be obtained.
†Determines zener current. May be adjusted to minimize thermal drift.
‡Solid tantalum.

ADJUSTABLE OUTPUT REGULATOR



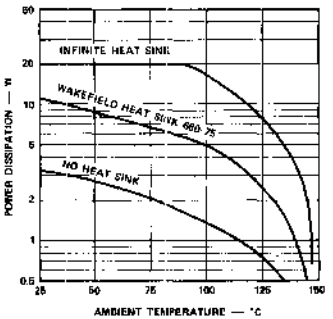
CURRENT REGULATOR



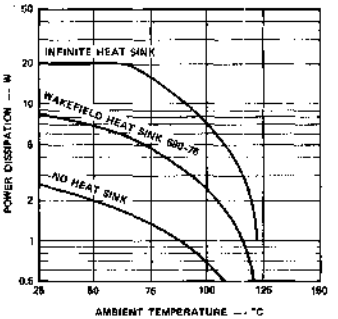
NOTES: *Determines output current.

TYPICAL PERFORMANCE CURVES

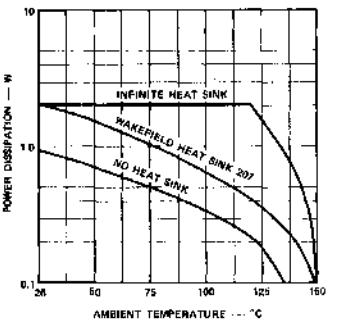
MAXIMUM AVERAGE POWER DISSIPATION LM109/LM209 (TO-3)



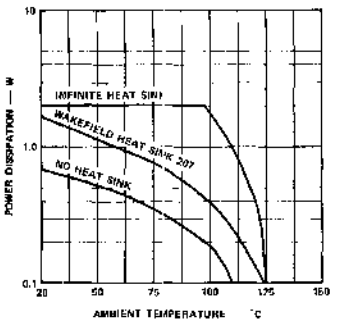
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-3)



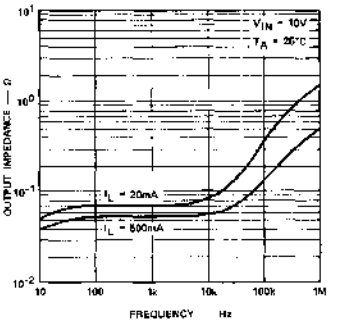
MAXIMUM AVERAGE POWER DISSIPATION LM109/LM209 (TO-5)



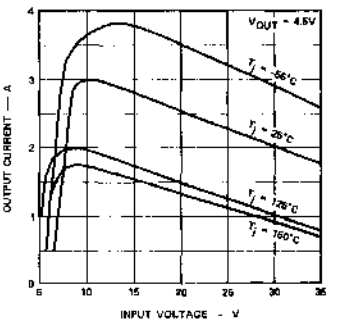
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-5)



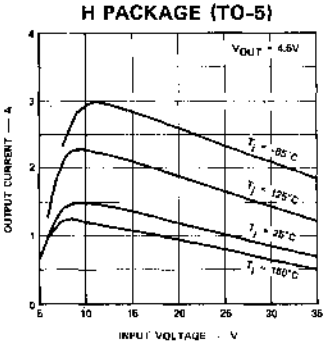
OUTPUT IMPEDANCE



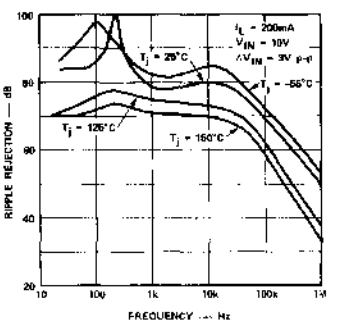
PEAK OUTPUT CURRENT K PACKAGE (TO-3)



PEAK OUTPUT CURRENT H PACKAGE (TO-5)

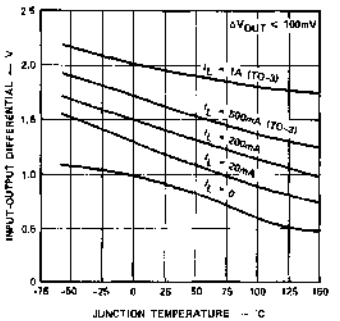


RIPPLE REJECTION

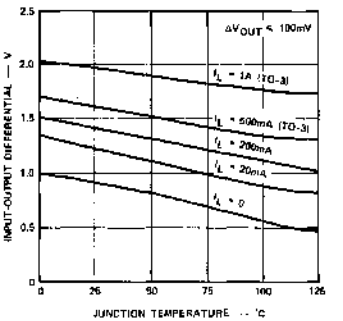


(Cont'd.)

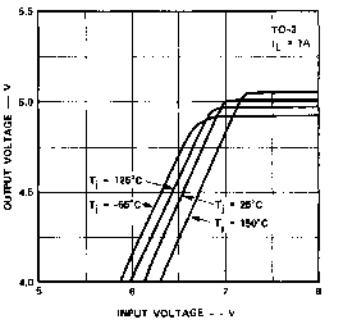
DROPOUT VOLTAGE



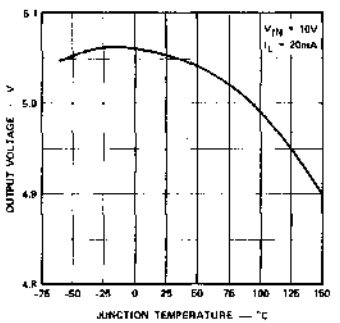
DROPOUT VOLTAGE



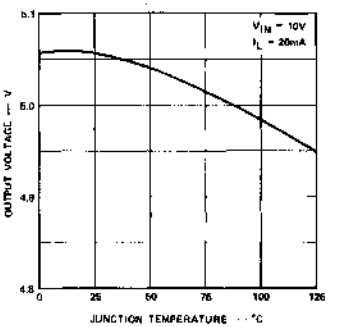
DROPOUT CHARACTERISTIC



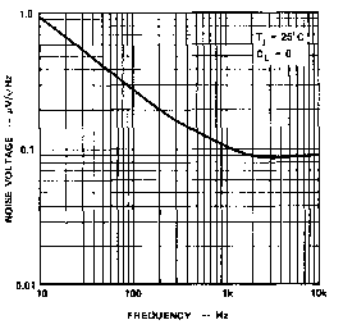
OUTPUT VOLTAGE



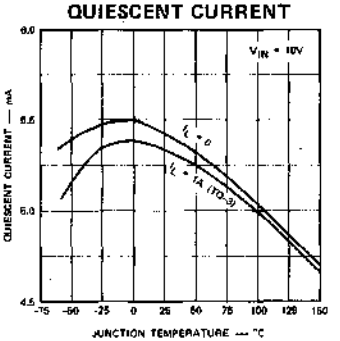
OUTPUT VOLTAGE



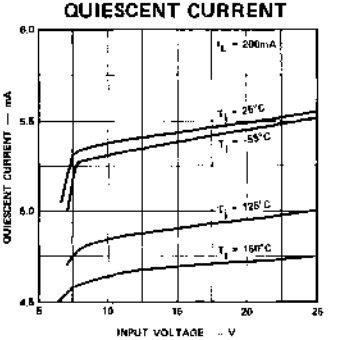
OUTPUT NOISE VOLTAGE



QUIESCENT CURRENT



QUIESCENT CURRENT



AMPS

AVERAGE INPUT OFFSET CURRENT t° COEFF – The change in input offset current divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET VOLTAGE t° COEFF – The change in input offset voltage divided by the change in ambient temperature producing it.

COMMON MODE INPUT RESISTANCE – The resistance looking into both inputs tied together.

COMMON MODE REJECTION RATIO (CMRR) – The ratio of the change of input offset voltage to the input common mode voltage change producing it.

FULL POWER BANDWIDTH – The maximum frequency at which the full sinewave output might be obtained.

INPUT BIAS CURRENT – The average of the two input currents at zero output voltage. In some cases, the input current for either input independently.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

INPUT CURRENT – The current into an input terminal.

INPUT NOISE VOLTAGE – The square root of the mean square narrow-band noise voltage referred to the input.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE – The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltages producing it.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

SLEW RATE – The maximum rate of change of output voltage under large signal condition.

SUPPLY CURRENT – The current required from the power supply to operate the amplifier with no load and the output at zero.

TEMPERATURE STABILITY OF VOLTAGE GAIN – The maximum variation of the voltage gain over the specified temperature range.

REGULATORS

DROPOUT VOLTAGE – The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL – The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

LINE REGULATOR – The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATOR – The percentage change in output voltage for a specified change in load current.

MAXIMUM POWER DISSIPATION – The maximum total device dissipation for which the regulator will operate within specifications.

OUTPUT NOISE VOLTAGE – The rms output noise voltage with constant load and no input ripple.

OUTPUT VOLTAGE RANGE – The range of output voltage over which the regulator will operate.

QUIESCENT CURRENT – That part of input current to the regulator that is not delivered to the load.

REGULATORS (Cont'd.)

REFERENCE VOLTAGE – The output of the reference amplifier measured with respect to the negative supply.

RIPPLE REJECTION – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

SENSE VOLTAGE – The voltage between current sense and current limit terminals necessary to cause current limiting.

SHORT CIRCUIT CURRENT LIMIT – The output current of the regulator with the output shorted to the negative supply.

STANDBY CURRENT DRAIN – The supply current drawn by the regulator with no output load and no reference voltage load.

COMPARATORS/SENSE INTERFACE

COMMON MODE FIRING VOLTAGE – The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

COMMON MODE RECOVERY TIME – The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE – The change in input offset voltage due to common mode input noise.

LOGIC INPUT HIGH VOLTAGE – The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE – The maximum voltage allowed at a bit control gate to hold the bit on.

OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage overdrive.

STROBE CURRENT – The maximum current drawn by the strobe terminals when it is at the zero logic level.

STROBE DELAY – The time delay measured from strobe to output threshold with a signal present exceeding the input threshold.

STROBE RELEASE TIME – The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

STROBED OUTPUT LEVEL – The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

SWITCHING SPEED – The time required to turn on the least significant bit.

THRESHOLD UNCERTAINTY – With all sense amps sharing the same input threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

THRESHOLD VOLTAGE – The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0"

ZERO SCALE OUTPUT CURRENT – The output current for all bits turned off.

COMMUNICATIONS CIRCUITS

ACC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the ACC Detector Output Terminals to the incremental change in peak-to-peak voltage at the ACC Detector Input Terminal for a specified burst input level, with the local oscillator locked.

APC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the APC Detector Output Terminals to the incremental change in relative phase at the APC Detector Input Terminal for a specified burst input level.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE – The percentage change in output voltage for a specified change in ambient temperature.

BANDWIDTH – The frequency at which the differential gain is 3dB below its low frequency value.

COLOR-DIFFERENCE DEMODULATION ANGLE – A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(-) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (-) Chroma input.

DIFFERENTIAL OUTPUT VOLTAGE SWING – The peak differential output swing that can be obtained without clipping.

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in differential output voltage to the change in differential input voltage producing it.

OSCILLATOR CONTROL SENSITIVITY – The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC Detector Output Terminals.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

OUTPUT OFFSET VOLTAGE – The difference between the voltages at the two output terminals with the inputs grounded.

TOTAL HARMONIC DISTORTION – The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

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MOS Functional Index

WHY SILICON GATE TECHNOLOGY?

INTRODUCTION

There are many MOS processes available today, ranging from high threshold, 1-1-1 orientation silicon, P-MOSTs to the less common dielectrically isolated, complementary MOS, ion implanted, silicon nitride, and silicon gate monolithic circuit. The problems which arise for MOS manufacturers and users can be summarized many times as one question: Which technology?

In this section, a brief comparison of the available MOS technologies is made. This is followed by a description of the silicon gate process flow sequence and a comparison of its advantages and disadvantages.

MOS TECHNOLOGIES

The numbers of MOS technologies available are numerous and each has its own advantages and disadvantages. Figure 1 shows a process ranking for some of the major technologies now available. The processes are weighted on five different factors: speed, chip area, power dissipation, bipolar compatibility and cost. The Silicon Gate Process which ranks highest forms the basis for the 2500 Series.

PROCESS RANKING

MOS	SPEED	AREA	POWER	COMPATIBILITY	COST
P Channel					
1-1-1 Crystal, Metal Gate	6	2	3	3	1
1-0-0 Crystal, Metal Gate	7	2	2	2	1
Nitride	5	2	2	2	2
Silicon Gate, (111) Crystal	3	1	2	1	2
Ion Impl. (Metal Gate)					
Low Threshold Approach	5	2	2	1	2
Self Aligned Gate	4	3	3	3	2
N Channel	2	2	2	1	3
Complementary	1	4	1	1	4

FIGURE 1.

SILICON GATE PROCESS

FABRICATION SEQUENCE

Basic process flow is illustrated in Figure 2. Using this chart as a guide, the process can be described as follows.

STEP A

The wafers are thoroughly inspected, cleaned, oxidized and masked to delineate the area where the drain, source and channel will eventually be formed. The gate dielectric is then grown. Both the initial oxide and the gate dielectric can be grown in any manner, to any desired thickness, without affecting junction characteristics. The initial oxide thickness is normally chosen to minimize poly-to-substrate capacitance, maximize poly-to-substrate parasitic field turn-on voltage and thin enough to minimize the step over which metal lines may eventually have to travel.

STEP B

The poly-crystalline silicon is deposited, a masking oxide is formed and the sandwich is then masked and etched to delineate the gate structure and the drain-source beds. The quality, cleanliness and thickness uniformity of the deposited poly is important. Also delineating the poly-crystalline lines is a critical step, since some of these lines determine the channel length of the completed MOS transistors.

STEP C

Boron is deposited to dope the poly-crystalline silicon and to form the P^+ beds for source and drain. The doping of the poly lines and P^+ beds is straightforward and virtually any clean source of boron can be used. Because the pre-deposited poly-silicon gate is used to mask the boron diffusion, the gate,source and drain are automatically self aligned.

STEP D

A clean layer of oxide is deposited over the entire wafer to passivate the P^+ beds and provide isolation between poly-silicon and metal lines. Deposition of the passivating oxide requires strict control over the cleanliness of the deposition system to minimize oxide defects and contamination.

STEP E

Contacts are opened and metallization is deposited, delineated and sintered. The metallization is fairly standard. As with the metal gate processes which may have high oxide steps, care must be taken with the silicon gate process to minimize the height of the steps over which metal must travel in order to minimize metal microcracking problems.

A multi-layered protective glass is deposited over the finished structure and holes are opened to the bonding pads to give the final cross-section shown in Figure 3. Glass passivation is mandatory, even with the silicon gate process, to protect the aluminum metalization from mechanical abrasion and particulate contamination.

SILICON GATE PROCESS FLOW

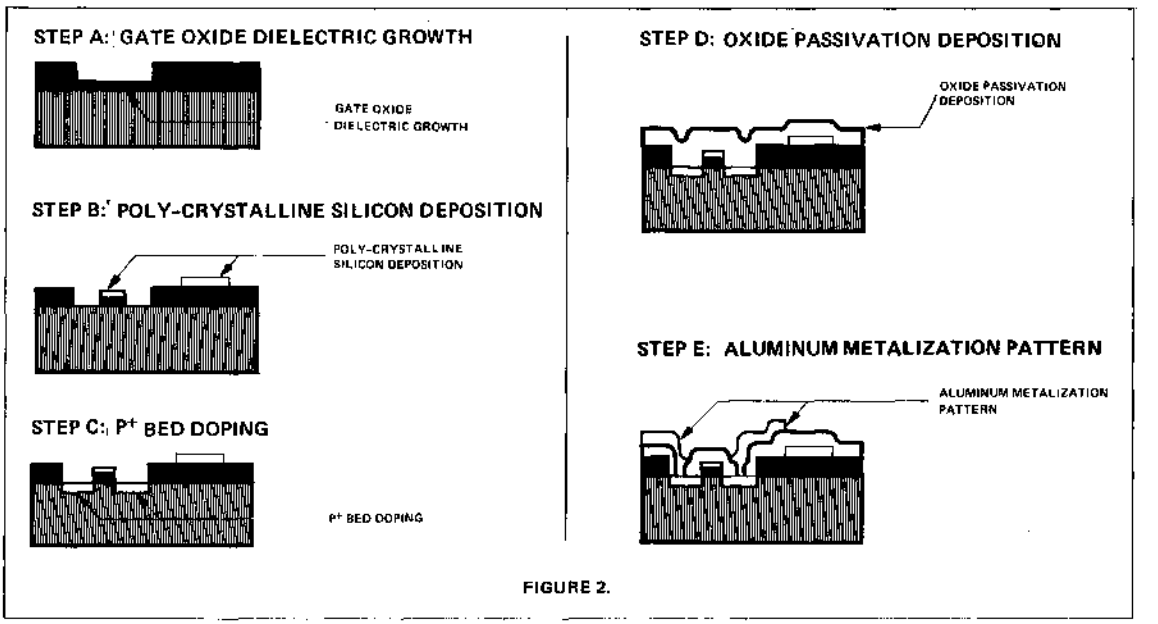


FIGURE 2.

FINAL DEVICE CROSS – SECTION

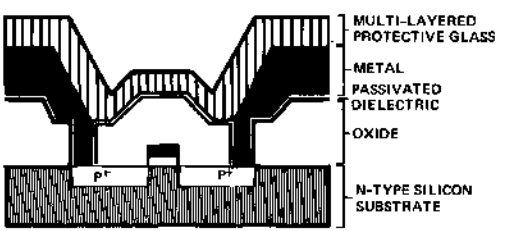


FIGURE 3.

ADVANTAGES AND DISADVANTAGES OF SILICON GATE

The silicon gate process has a number of advantages which make it attractive for the production of complex, high density circuits. Before expanding on these advantages, we will first explore two of the more prominent disadvantages of the process:

Ratio Versus Ratioless
Because of the self-aligned gate feature, the parasitic drain-to-source capacitance is small. In designing dynamic shift registers, it is advantageous to design "ratioless" devices where parasitic capacitance is used to momentarily store charge. Using silicon gate, a ratioless type design is not feasible, so the more area consuming ratio type must be used. However, the silicon gate ratio design is competitive in size with the metal gate ratioless version, since area is saved by the smaller gate area (no need for alignment tolerance allowance), plus the use of the poly-silicon as a interconnecting layer.

Additional Depositions
Silicon gate processing requires more deposition steps than is required by standard metal gate processes. However, these processes can be easily controlled using modern, automated deposition equipment and built-in process control monitors.

The potential disadvantages of the silicon gate process are outweighted by the following advantages.

Low Threshold Voltage
Doped poly-silicon, used in place of the usual aluminum gate electrode, yields threshold voltages typically around -2.0 volts. This low threshold voltage is obtained using 1-1-1 orientation silicon, so the corresponding parasitic field turn-on voltage is still very high.

High Gain
The gain of the silicon gate device is high since 1-1-1 orientation is used as the starting material. Gain is typically higher than low threshold voltage devices fabricated on 1-0-0 silicon because of higher carrier mobility.

Low Power
The silicon gate device dissipates less power:

(1) Because of its low threshold it operates with lower power supply voltages.
(2) Its self-aligned gate essentially eliminates overlap of the gate over the drain, so the capacitive load on the clock drive is less.

High Speed
High speeds are obtained because of low threshold voltages, high gain and low gate capacitance.

Minimum Area
The poly-crystalline silicon layer provides yet another "half-layer" of interconnection. We call it a "half-layer" since the crossing of poly-silicon over P^+ beds is not allowed. Shallow junctions allow close P^+ bed spacings and the self-aligned gate feature means no mask alignment tolerances are needed to register the gate to the P^+ beds. In addition, direct contact of poly-to-substrate allows further area reduction.

To illustrate the size advantages, consider Figure 4. The 2005 and 2510 are both dual 100-bit static shift registers. However, the silicon gate 2510 is 15 percent smaller than its metal gate equivalent. Not only is it smaller but it has additional functions such as recirculate logic, tri-state outputs, TTL compatibility and an on-chip clock generator. The silicon gate 2511 Dual 200-Bit Static Shift Register, offers twice the number of bits as the metal gate 2005 plus four additional functions in only 36 percent more area.

SIZE COMPARISON OF DICE

PART NUMBER	DESCRIPTION	DIE SIZE	AREA
2005	Dual 100 Bit S.S.R. (Metal Gate)	91 x 90	8,190mil^2
2510	Dual 100 Bit S.S.R. (Silicon Gate)	85 x 82	6,970mil^2
2511	Dual 200 Bit S.S.R. (Silicon Gate)	136 x 82	11,152mil^2

FIGURE 4.

High Yield
The process of forming the gate oxide at the first stage of wafer fabrication and coating with a protective layer of silicon inherently gives higher yields. In addition, the ability to compact a given circuit function into a smaller area gives a lower probability that a processing defect will occur on a die. This is especially true since the decrease in area does not come at the expense of masking tolerances. The higher yields result in lower costs.

Process Flexibility
The silicon process gate is compatible with other MOS technologies. Ion implantation can be used to adjust thresholds and/or minimize gate-to-drain capacitance. Gate dielectrics can easily be changed without affecting junction characteristics, and C-MOST and N-MOST can easily be adapted to silicon gate processing.

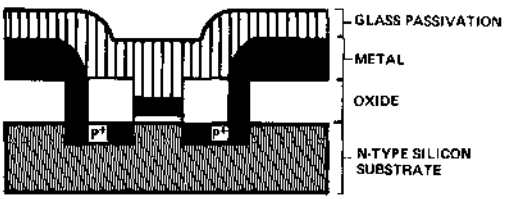
Low Cost Packaging
Because the gate dielectric is protected by poly-silicon and the overlying layers of oxides, it is possible to reliably package silicon gate devices in silicone packages. Cross-sections of metal gate and silicon gate devices are shown in Figure 5. The metal gate devices are protected by two layers: aluminum metallization and glass passivation. On the other hand, the silicon gate device is protected by four layers: (1) thick poly-

LOW COST PACKAGING (Cont'd)

crystalline silicon (impervious to most harmful contaminants). (2) thick clean oxide, (3) a passivated dielectric which also serves as a sodium barrier and, (4) a multi-layered protective glass.

The silicon gate process is a technology which gives all of the advantages needed to fabricate the next generation of circuits: high packing density, high speed, low power and low cost. Because of these characteristics, silicon gate MOS technology has become an industry standard for state-of-the-art MOS LSI designs.

METAL GATE PROCESS



SIGNETICS SILICON GATE PROCESS

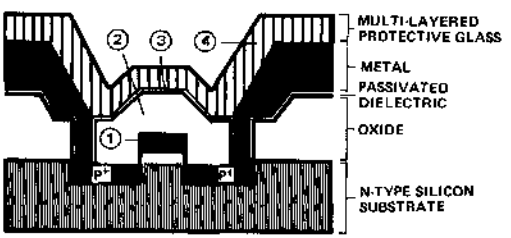


FIGURE 5.

DESIGNING WITH SILICON GATE

INTRODUCTION

Large scale, bipolar compatible MOS integrated circuits are now available to the systems designer because of the unique benefits of Signetics' Silicon Gate Technology. Using complex MOS functions to form major systems blocks, joined and controlled by today's wide variety of low cost TTL and DTL MSI and SSI functions, economical state-of-the-art systems are being produced with ease and efficiency.

THE SILICON GATE MOS BIPOLAR COMBINATION

Silicon Gate MOS - Bipolar designs offer the best of both worlds. MOS designs are most efficient when providing large, medium-speed arrays of identical cells, such as required for long serial shift registers, large Random Access Memories (RAMs) and large Read-Only-Memories (ROMs).

Bipolar designs are most efficient when providing high-speed connective logic functions (gates), small parallel registers, and small specialized logic combinations such as adders, comparators, counters, decoders, and power drivers.

MOS-BIPOLAR COMPATIBILITY

Today's systems are designed to utilize the benefits of both MOS and bipolar technology for maximum performance at minimum cost. Signetics recognizes the benefits of direct MOS-Bipolar interfacing and has created the Silicon Gate 2500 Series MOS with the express purpose of providing MOS density and bipolar compatibility.

INPUT INTERFACE

All 2500 series devices are manufactured with the P-channel enhancement mode silicon gate process. A typical data input structure is shown in Figure 1.

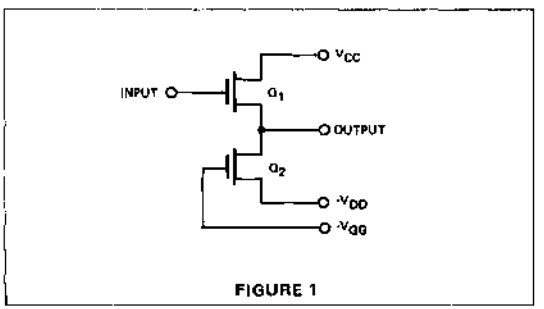


FIGURE 1

The input transistor exhibits the transfer curve shown in Figure 2. The device is fully OFF at -1.8 volts or less (V_{GS}) and fully ON at -3.5 volts or more. To simplify the interfacing of TTL and 2500 Series devices, the source voltage for the input transistor is specified at +5.0 volts. In practice, this point is tied to the +5.0 volt TTL V_{CC} supply. The required MOS input levels are then specified as positive levels referenced to the TTL ground.

Series 2500 Input Thresholds

"0" Input Voltage = V_{IL} = +1.05 maximum@ V_{CC} = 5V

"1" Input Voltage = V_{IH} = +3.2V minimum @ V_{CC} = 5V

The input levels are specified assuming V_{CC} is exactly +5.0V. The allowable V_{CC} tolerance is ±5%, however any variation in actual V_{CC} will be tracked directly by the input threshold point.

Example (a): +5% V_{CC}
@ V_{CC} = +5.25V
V_{IL} = 1.3V max.
V_{IH} = +3.45V minimum

Example (b): -5% V_{CC}
@V_{CC} = +4.75V
V_{IL} = 0.8V max.
V_{IH} = +2.95V minimum

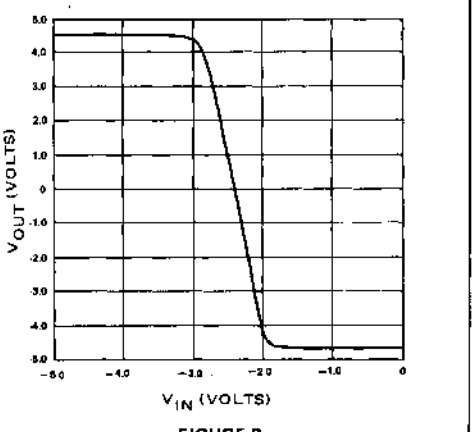


FIGURE 2

In actual practice, tying the TTL V_{CC} to the MOS V_{CC} will ensure maximum noise margin since the TTL output levels and MOS input thresholds will track.

54/7400 TTL

Figure 3(a) and (b) show a typical 7400 Series gate circuit and transfer characteristic.

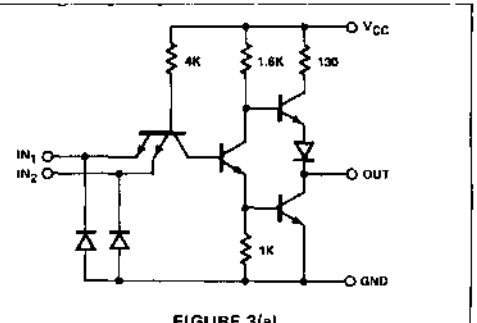


FIGURE 3(a)

54/7400 TTL

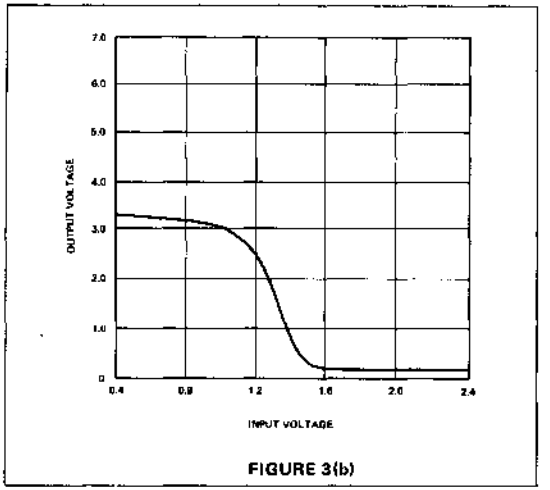


FIGURE 3(b)

The output structure shown in Figure3(a) is normally specified as follows:

@ V_{CC} = +5V ±5%

V_{OL} = +0.4V maximum @ 16 mA sink

V_{OH} = +2.4V minimum @ 400 μA source

MOS devices require only negligible D.C. input current (approximately 1μA), so the current available from the TTL output is of no interest for steady state conditions. V_{OL} is perfectly compatible with the MOS offering at least 400mV of noise margin in the 0 state. V_{OH} however, is not sufficient to guarantee a 1 level to the MOS input since the TTL V_{OH} allows a V_{CC} - V_{OH} separation of as much as 2.85V (V_{CC} = 5.25V, V_{OH} = +2.4V; 5.25V - 2.4V = 2.85V). Assuming a common V_{CC}, this results in a virtual V_{OH} of 2.15V, far too low for MOS. In practice, the TTL V_{OH} will track V_{CC}, rather than the opposite case just noted. Also V_{OH} will be higher than +2.4 at 1μA I_{OH}. However, the TTL circuit is tested and guaranteed as in the example.

The 7400 TTL output structure will typically provide a V_{OH} approximately 1.5V (two V_{be} drops) below V_{CC}. When the MOS and TTL V_{CC} are tied, a 300mV noise margin (1.8V - 1.5V = 0.3V) is obtained. If V_{CC} is not tied common, the worst case typical noise margin is a negative 200mV. In other words, a satisfactory 1 input level cannot be assured, even under typical conditions.

TO ASSURE A SATISFACTORY 1 OUTPUT LEVEL FROM SERIES 7400 IN DRIVING SERIES 2500 MOS, AN EXTERNAL PULL-UP RESISTOR SHOULD BE CONNECTED FROM THE OUTPUT TO V_{CC} AS SHOWN IN FIGURE 4.

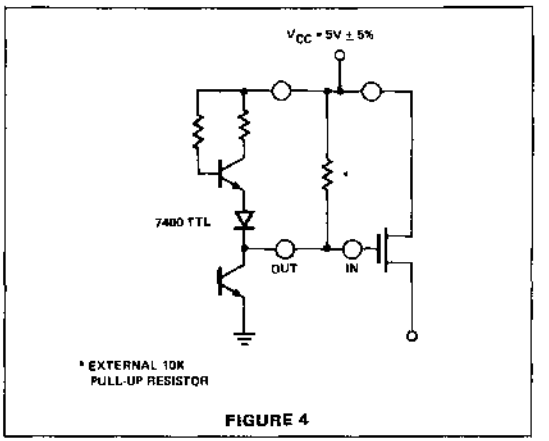


FIGURE 4

8000 TTL

Figure 5 illustrates a typical 8800 series output structure.

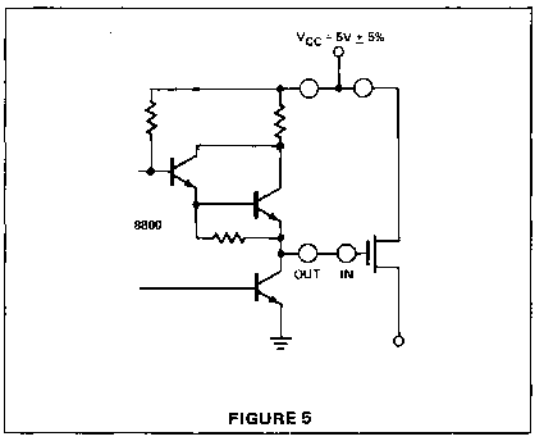


FIGURE 5

The 8800 series circuit typically offers an unloaded output voltage separated from V_{CC} by one V_{be}. Therefore the output level driving MOS will always be approximately 0.75V — higher than the preceeding example for 7400 series circuits — resulting in at least 550mV 1 level noise margin under any conditions. Noise margin at 0 level is 400 mV, the same as in the case of 7400 TTL.

Signetics guarantees 8000 Series TTL (See figure 6) V_{OH} at 3.6V @ 10μA. Under worst case conditions, this results in a minimum guaranteed 0 level noise margin of 400mV for tied V_{CC}. If the MOS and TTL V_{CC} are not tied (may vary independently), worst case guaranteed noise margin is -150mV. This configuration requires a pull-up resistor.

WHEN V_{CC}'S ARE TIED COMMON, SERIES 8000 TTL IN FIGURE 6 WILL INTERFACE DIRECTLY WITH SERIES 2500 MOS, WITHOUT THE NEED FOR AN EXTERNAL PULL-UP RESISTOR.

GATES		FLIP-FLOPS	
8808	Single 8-Input NAND Gate		
8815	Dual 4-Input NOR Gate		
8816	Dual 4-Input NAND Gate	8821	Dual Master-Slave J-K Binary
8840	Dual Expandable AND-OR-INVERT Gate	8822	Dual Master-Slave J-K Binary
8848	Expandable AND-OR-INVERT Gate	8824	Dual Master-Slave J-K Binary
8870	Triple 3-Input NAND Gate	8825	DC Clocked J-K Binary
8875	Triple 3-Input NOR Gate	8826	Dual J-K Binary
8880	Quad 2-Input NAND Gate	8827	Dual J-K Binary
8885	Quad 2-Input NOR Gate	8829	High Speed J-K Binary
	*See Note Below		

FIGURE 6

*For devices not listed, add an external pull-up resistor as in the 7400 example (Fig. 4).

DTL/UTILOGIC®

Logic forms utilizing an internal passive pull-up resistor (such as DTL) will interface directly with 2500 Series MOS. Utilogic is guaranteed to provide output levels equivalent to those noted for Series 800 circuits.

WHEN V_{CC}'S ARE COMMON, SERIES 2500 MOS MAY BE DIRECTLY DRIVEN BY SERIES 600 DTL AND SERIES 300 UTILOGIC CIRCUITS WITHOUT THE NEED FOR AN EXTERNAL PULL-UP RESISTOR.

2500 SERIES MOS-TTL INPUT CONSIDERATIONS (TTL Level data and clock inputs)

DRIVING DEVICE	EXTERNAL PULL-UP RESISTOR(6)	WORST CASE GUAR. 1 LEVEL NOISE MARGIN	WORST CASE GUAR. 0 LEVEL NOISE MARGIN
Common V_{CC}			
8000(1) Series TTL	not req.	400	400
8000(2) Series TTL	10K	1300	400
7400 Series TTL	10K	1300	400
600 Series DTL (3)	not req.	400	400
600 Series DTL (4)	not req.	400	400
300 Series Utilogic (3)	not req	1300	400
300 Series Utilogic (4)	not req.	400	400
Independent V_{CC}			
All TTL	10K	800	400
600 Series DTL (3)	not req.	550	150 (5)
600 Series DTL (4)	not req.	550	150 (5)
300 Series Utilogic	10K (7)	550	150 (5)

NOTES:

FIGURE 7

(1) From List in Table I
(2) Not listed in Table I
(3) Passive Pull-up (resistor), ±10% power supply
(4) Active Pull-up, ±10% power supply
(5) Use ±5% DTL or Utilogic power supply to maintain 400 mV noise margin
(6) From driving output to V_{CC}
(7) Certain Series 300 devices utilize a passive pull-up and require no external pull-up.

OUTPUT INTERFACE

TTL/DTL INPUT STRUCTURES

Standard TTL circuits employ the input structure shown in Figure 8.

TYPICAL TTL INPUT STRUCTURE

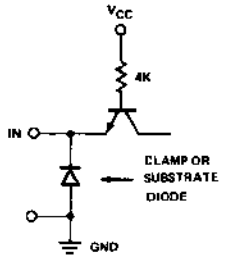


FIGURE 8

DTL circuits employ the structure shown in Figure 9.

TYPICAL DTL INPUT STRUCTURE

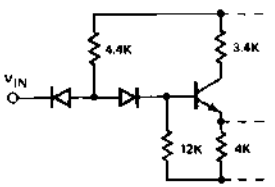


FIGURE 9

2500 SERIES OUTPUT STRUCTURES

Four basic types of output structures are used in the 2500 series:

1. Bare drain
2. Internal resistor pull-down
3. Push-pull
4. Three-state

See Figure 10.

TYPICAL 2500 SERIES OUTPUT CIRCUITS

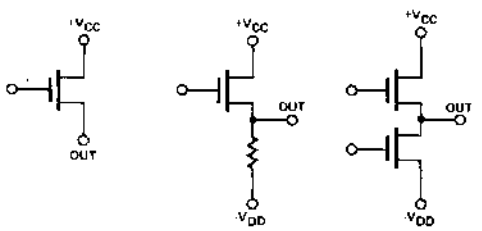


FIGURE 10

BARE DRAIN:

The bare drain output is the simplest structure and requires an external pull-down resistor. Bare drain is used where several outputs are to be tied together in a WIRED-OR configuration as shown in Figure 11.

WIRED-OR CONFIGURATION OF TWO BARE DRAIN DEVICES

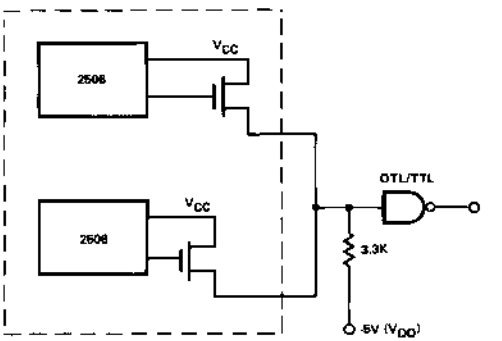


FIGURE 11

The external resistor is chosen to sink the 1.6mA required by a TTL gate. In Figure 11, a 3.3K resistor is tied to the V_{DD} supply. The output voltage will be +0.4V or less depending on the actual I_{OI} of the TTL input.

When the bare drain device is ON, it represents approximately 500 ohms. For the circuit of Figure 9, V_{OH} is approximately +3.7V – more than sufficient to drive a TTL or DTL gate. Bare drain 2500 devices are listed in Figure 12.

BARE DRAIN SERIES 2500 DEVICES

2502	2505	2519
2503	2512	2524
2504	2518	2525

FIGURE 12

RESISTOR PULL-DOWN

The second type of output has a pull-down resistor on the chip. The 2507 and 2517 are examples of this. The 2517 has a 20K ohm internal resistor for interfacing with MOS.

Resistor pull-down series 2500 devices are listed in Figure 13. The 2507 has a 7.5Kohm resistor, and if used in the WIRED-OR configuration with another 2507 output, will drive TTL directly as shown in Figure 14.

RESISTOR PULL-DOWN SERIES 2500 DEVICES

2507	7.5K
2517	20K

FIGURE 13

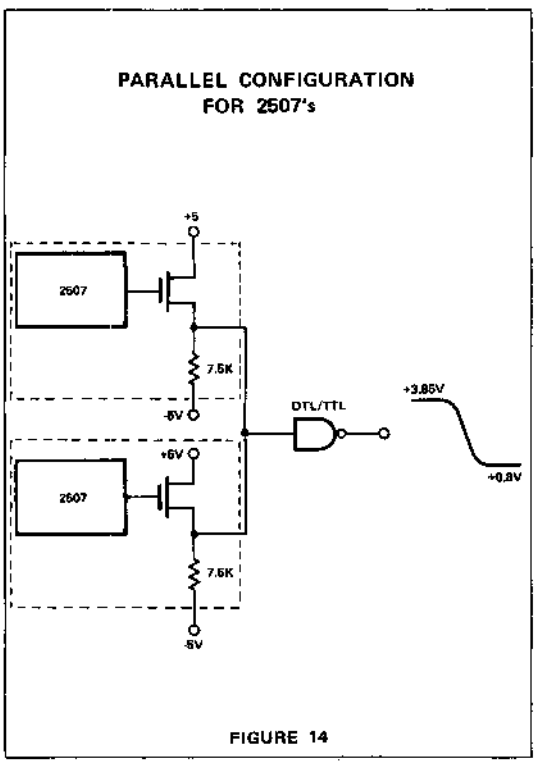


FIGURE 14

PUSH-PULL

The third type of output structure used in the 2500 Series is the push-pull circuit shown in Figure 10c. In the push-pull configuration, the gates of the two output devices are driven from complementary signals such that only one device is ON at a time. When the upper device is ON, the output is tied to V_{CC} through approximately 500 ohms. When the lower device in ON, the output is tied to V_{DD} through 500 ohms.

The advantage of this circuit is that no additional power is dissipated in either state. Both states have low impedance to the power supplies. Push-Pull output series 2500 devices are listed in Figure 15.

PUSH-PULL OUTPUT SERIES 2500 DEVICES

2521	2527	
2522	2528	2529

FIGURE 15

THREE-STATE

A disadvantage of the push-pull circuit is that paralleling of the outputs is not possible because two low impedance devices would be ON simultaneously directly across the power supplies. To avoid this condition, a three-state output is used. The third state is an open output configuration where both devices are OFF and is accomplished by using an OUTPUT ENABLE line tied to the gates of both output devices as shown in Figure 16. Three-state series 2500 devices are listed in Figure 17.

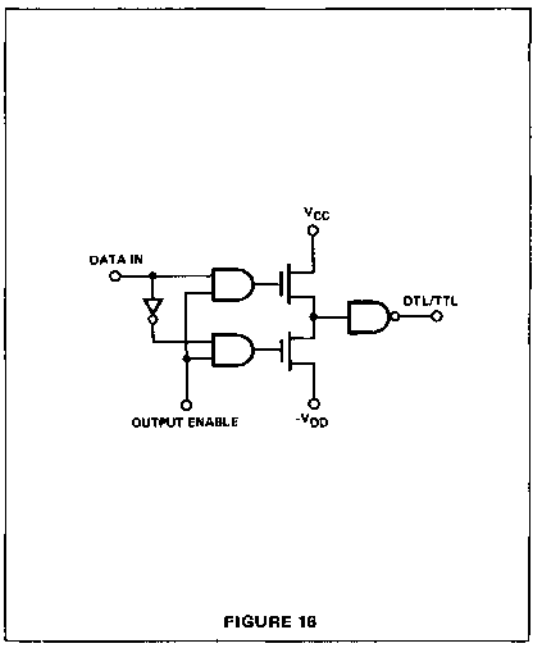


FIGURE 16

THREE-STATE SERIES 2500 DEVICES

2501	2510	2513	2516
2509	2511	2514	

FIGURE 17

Figure 18 summarizes the output configurations used on the 2500 Series circuits.

OUTPUT CONSIDERATIONS FOR 2500 LINE

PRODUCT NUMBER	DESCRIPTION	OUTPUT STRUCTURE	TO DRIVE ONE TTL/DTL USE*
1103	1024 x 1 dynamic RAM	Bare Drain	Sense Amp
2501	256 x 1 Static RAM	3-State	Direct
2502	256 x 4 Dynamic Shift Register	Bare Drain	3.0K
2503	512 x 2 Dynamic Shift Register	Bare Drain	3.0K
2504	1024 x 1 Dynamic Shift Register	Bare Drain	3.0K
2505/2524	512 x 1 Dynamic Shift Register	Bare Drain	3.0K
2506	100 x 2 Dynamic Shift Register	Bare Drain	3.0K
2507	100 x 2 Dynamic Shift Register	7.5K Resistor	6.8K
2509	50 x 2 Static Shift Register	3-State	Direct
2510	100 x 2 Static Shift Register	3-State.	Direct
2511	200 x 2 Static Shift Register	3-State	Direct
2512/2525	1024 x 1 Dynamic Shift Register	Bare Drain	3.0K
2513	64 x 7 x 5 Character Generator	3-State	Direct
2514	512 x 5 ROM	3-State	Direct
2516	64 x 6 x 8 Character Generator	3-State	Direct
2517	100 x 2 Dynamic Shift Register	20K Resistor	3.3K
2518	32 x 6 Static Shift Register	Bare Drain	6.8K
2519	40 x 6 Static Shift Register	Bare Drain	6.8K
2521	128 x 2 Static Shift Register	Push-Pull	Direct
2522	132 x 2 Static Shift Register	Push-Pull	Direct
2527	256 x 2 Static Shift Register	Push-Pull	Direct
2528	250 x 2 Static Shift Register	Push-Pull	Direct
2529	240 x 2 Static Shift Register	Push-Pull	Direct

*NOTE: Values are given for the maximum value of pull-down resistor, output to V_{DD}.

FIGURE 18

"OR" TYING OUTPUTS

The characteristics of the four types of output structures differ when tied together. A basic feature of MOS is that the design limitation on output "OR"ing is related to the output voltage levels required and the RC time constant of the resulting network.

BARE DRAIN

The number of bare drain devices which can be tied together is limited by the output time constant and the V_{OH} level required.

Switching time for the pull-down condition is determined by the load resistor R_{PD} and load capacitance C_L. The MOS pull-up device is turned off and does not contribute to the negative going time constant. See Figure 19.

C_L is comprised of wiring capacitance (C_W) and output capacitance (C_{OUT}) from each of the paralleled outputs.

As the number of paralleled devices increases, the value of R_{PD} must be decreased to maintain speed.

When driving loads having significant input capacitance, C_L should be increased accordingly.

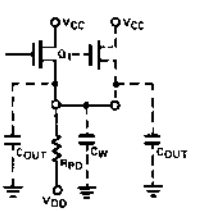


FIGURE 19

As R_{PD} is decreased, V_{OH} decreases since the impedance of Q1 when ON (approx. 500 ohms) will ratio with R_{PD} to produce V_{OH}. If R_{PD} is reduced too far, the output voltage will be insufficient to turn off the TTL gate being driven.

Figure 20 gives the recommended value of R_{PD} as a function of fan-out for 2500 series bare drain devices.

Fan-Out	C_L	R_{PD}*	V_{OH}
1	15pF	3.3K	3.7V
2	20pF	2.5K	3.3V
3	25pF	2K	3.0V
4	30pF	1.67K	2.7V
5	35pF	1.43K	2.4V

* For t_F = 50ns

FIGURE 20

Figure 20 assumes 10pF of wiring capacitance and 5pF per output. It should be noted that when the MOS device is OFF, the TTL input current of 1.6mA is sunk to -5V. When set up for a fanout of 5, the 1.6mA from the TTL gate will bring the output to only -2.7V. In actuality the input clamp or substrate diode of the TTL gate will turn on and clamp the output to -1.0V. The diode will supply the additional current (approximately 1.9mA).

INTERNAL PULL-DOWN

When 2500 Series devices with internal pull-down resistors are paralleled, the equivalent resistance R_{PD} is the parallel combination of all the internal resistors. A chart of the equivalent resistance, output time constant and V_{OH} for the 2507 with a 7.5K internal pull-down resistor is shown in Figure 21.

Fan-Out	C_L	R_{PD}	t_f	V_{OH}
1	15	7.5K	110nS	4.4V
2	20	3.75K	75nS	3.8V
3	25	2.5K	63nS	3.3V
4	30	1.87K	56nS	2.9V
5	35	1.5K	53nS	2.5V

FIGURE 21

PUSH-PULL OUTPUTS

Push-Pull outputs allow low rise and fall times but cannot be paralleled because it would then be possible to have both a push and a pull device on at the same time resulting in a low impedance between the power supplies (and indeterminate output level).

THREE STATE OUTPUTS

The three state output is designed to take advantage of push-pull drive capability plus the ability to OR the outputs.

The third (or open) state is used when the chip is unselected. The selected output is free to drive the load without being affected by the other outputs tied to the bus.

Output rise and fall times for the WIRED OR configuration of three-state devices is a function of the ON resistance of the individual pull-up and pull-down devices together with the load capacitance.

A CLOCK DRIVER FOR 2500 SERIES MOS

In order to obtain optimum performance from MOS devices, they must be provided with clock signals of the proper amplitude, shape and timing. This section will present a simple clock generator and driver scheme suitable for use with 2500 Series MOS devices.

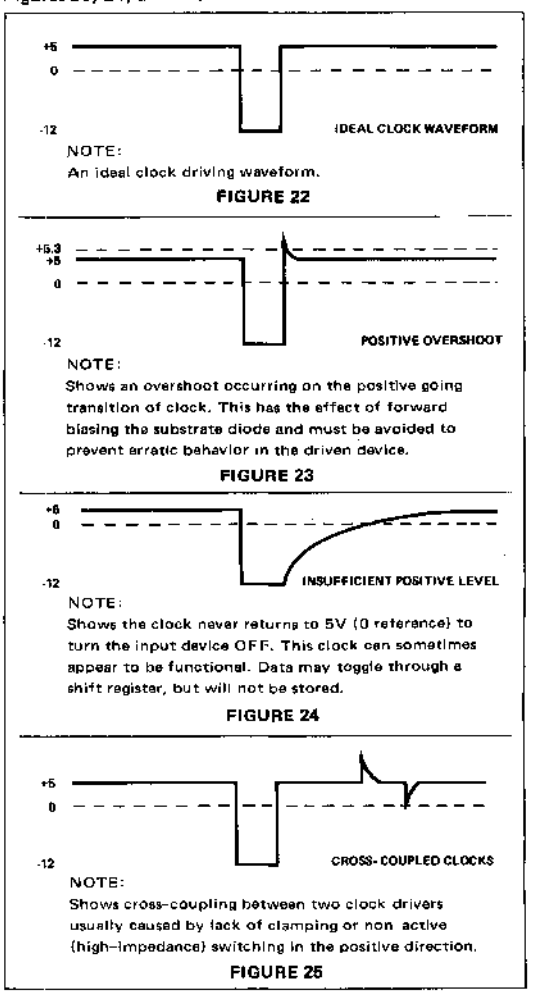
NOTE: The following devices employ on-chip clock generators and may be driven directly by TTL gates:

2509 2510 2511 2518 2519 2621 2522

The clock driver must provide relatively large voltage swings for the clock lines. In the case of 2500 Series MOS, the clock signal must swing from +5V to -12V. And it must provide a clean waveform having reasonable rise and fall times (under 40 ns.) and lack of positive overshoot.

IMPROPER CLOCK WAVEFORMS

Some common examples of improper clocking are shown in Figures 23, 24, and 25.



NOTE:
An ideal clock driving waveform.

FIGURE 22

NOTE:
Shows an overshoot occurring on the positive going transition of clock. This has the effect of forward biasing the substrate diode and must be avoided to prevent erratic behavior in the driven device.

FIGURE 23

NOTE:
Shows the clock never returns to 5V (0 reference) to turn the input device OFF. This clock can sometimes appear to be functional. Data may toggle through a shift register, but will not be stored.

FIGURE 24

NOTE:
Shows cross-coupling between two clock drivers usually caused by lack of clamping or non active (high-impedance) switching in the positive direction.

FIGURE 25

The positive overshoots illustrated in Figure 23 and Figure 25 are the most common sources of clock driving trouble. When the clock line goes positive relative to the circuit substrate (V_{CC}) by more than approximately 0.3V, the substrate diode may become forward biased. When this occurs, device operation may become erratic. And because the forward characteristics of the substrate diode may be different for different processing techniques, a clock driver may work properly with one device but not with another.

A properly designed driver utilizing level clamping will prevent the overshoot problem.

THE DRIVER OUTPUT STRUCTURE

Figures 26, 27, and 28 show possible output driver structures together with their advantages and disadvantages.

RESISTOR PULL-UP, POOR NOISE IMMUNITY, AND SLOW RISE TIME

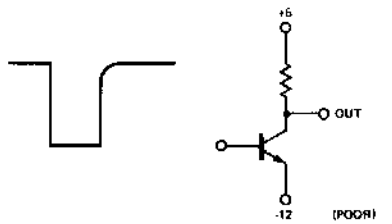


FIGURE 26

PUSH-PULL, SLOW RISE AND FALL TIME

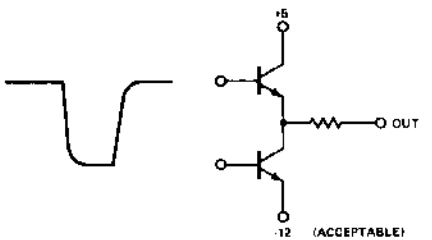


FIGURE 27

COMPLEMENTARY, EXCELLENT NOISE IMMUNITY, FAST RISE AND FALL TIME

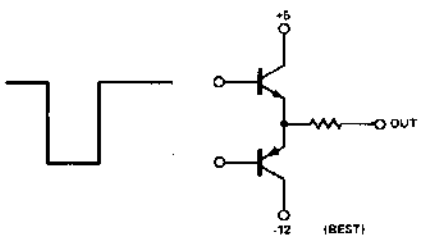
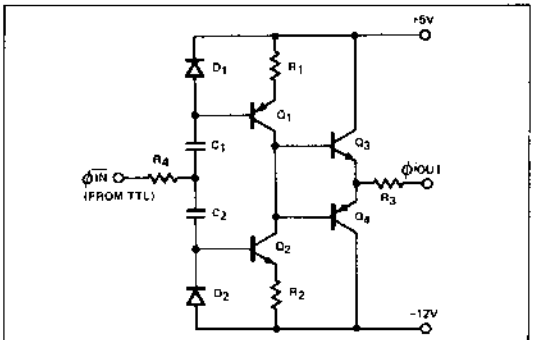


FIGURE 28

The driver circuit recommended here (Figure 29) utilizes a complementary output structure to obtain maximum noise immunity and fast rise and fall time under heavy capacitive load. It is capacitively coupled to the TTL clock generator. Resistor R_4 is required only when operating at a clock frequency of lower than 750 KHz. This resistor shifts the response of the driver input circuit toward the lower frequencies by lengthening the input time constant. One clock driver is required for each clock phase.



Q_1, Q_4 2N2905, Heat Sink Required
Q_2, Q_3 2N2222, Heat Sink Required
C_1, C_2 100pF
D_1, D_2 1N914
R_1, R_2, R_3 33 Ohm
R_4 2.2K Ohm (Required only for operation below 750KHz)

FIGURE 29

GENERATING MULTIPLE PHASES

The 2500 Series MOS devices which require high level clocks also require more than one phase. The dynamic shift registers require two phases and the 2508 dynamic RAM requires four phases.

TWO PHASE SYSTEM

The clock generator in Figure 30 produces alternate pulses – the width of which are one quarter of the input clock period (assuming a square wave clock). See Figure 32.

TWO PHASE TTL CLOCK GENERATOR

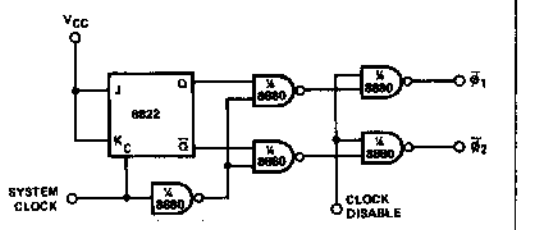


FIGURE 30

When required, the clock pulse widths can be varied by using one-shot multivibrators such as the 8162 or 74121. Each phase width can be varied independently (the limiting factor being the clock period), see Figure 31(a), or a single one-shot ahead of the clock generator will change both phases simultaneously. See Figure 31(b).

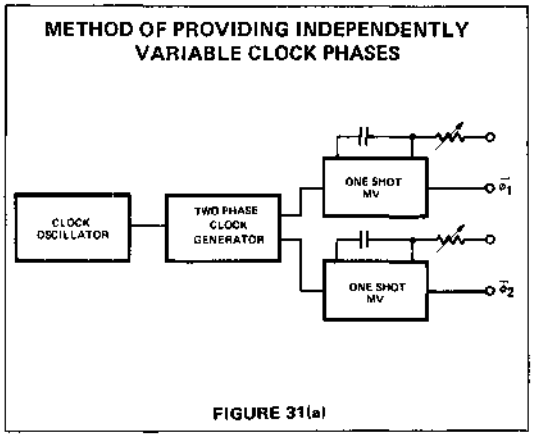


FIGURE 31(a)

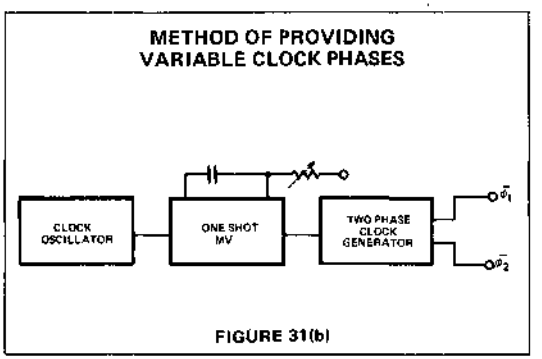


FIGURE 31(b)

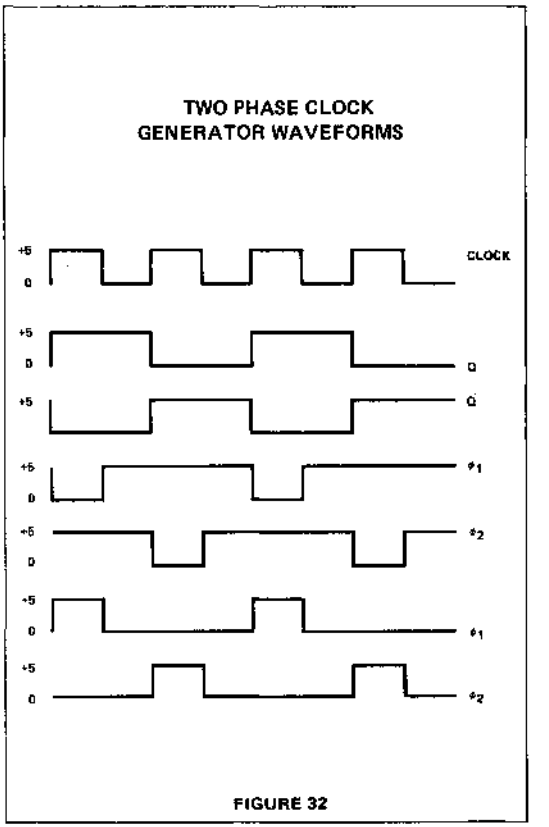


FIGURE 32

FOUR PHASE SYSTEM

The circuit shown in Figure 33(a) and (b) can be used to generate four phase clock signals for the 2508 1024 RAM.

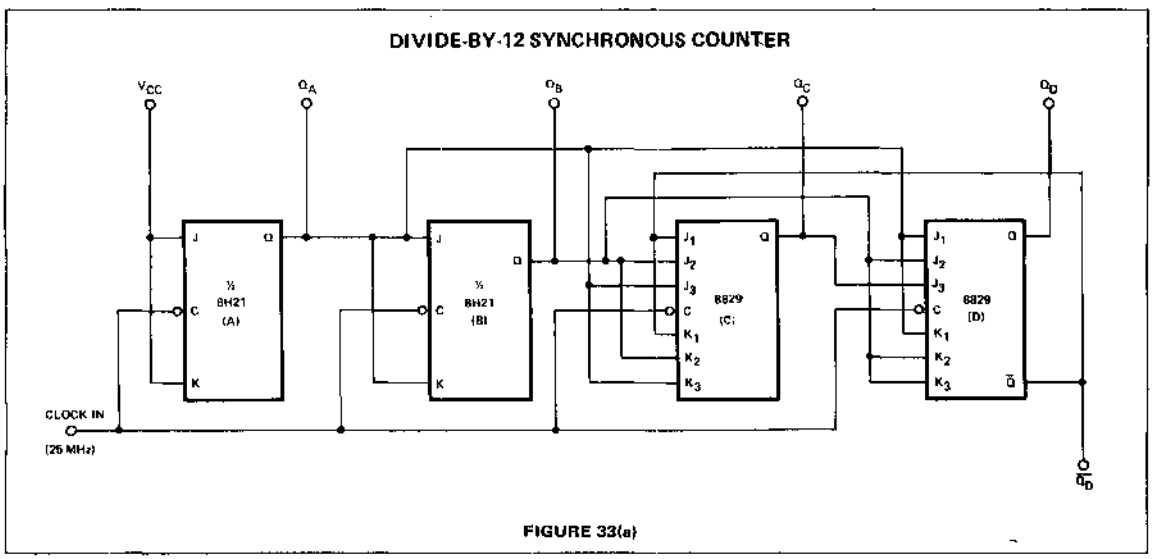


FIGURE 33(a)

FOUR PHASE SYSTEM

FOUR PHASE DECODER

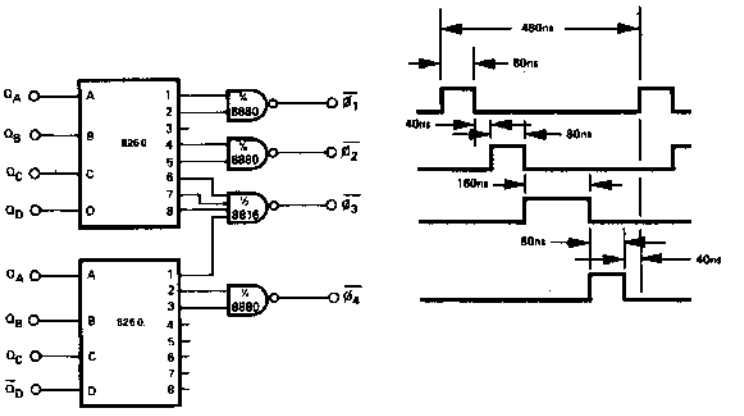


FIGURE 33(b)

Figure 34 shows typical clock input capacitances for 2500 Series devices. The number of similar devices which can be driven by one clock driver is indicated.

DEVICE	TYPICAL CLOCK CAPACITANCE (pF)	NO. OF UNITS WHICH CAN BE DRIVEN (INCLUDES ALLOWANCE FOR WIRING CAPACITANCE)	
		≤2MHz (1)	2-4MHz (2)
2502	140	8	6
2503	140	8	6
2504	140	8	6
2505	80	12	9
2506	25	40	30
2507	25	40	30
2508	25	40	30
2512	100	11	7
2517	25	40	30
2524	80	12	9
2626	100	11	7

(1) Drive capacity 1200pF
(2) Drive capacity 750pF

FIGURE 34

signetics

FULLY DECODED RANDOM ACCESS 1024-BIT DYNAMIC MEMORY

1103

SILICON GATE 2500 SERIES

DESCRIPTION

The Signetics 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T26 Sense Amp, and 3207 Clock Driver.

FEATURES

- LOW POWER DISSIPATION – DISSIPATES POWER PRIMARILY ON SELECTED CHIPS
- ACCESS TIME – 300 nsec.
- CYCLE TIME – 580 nsec.
- REFRESH PERIOD – 2 MILLISECONDS FOR 0-70°C AMBIENT
- OR-TIE CAPABILITY
- SIMPLE MEMORY EXPANSION WITH CHIP ENABLE
- FULLY DECODED – ON-CHIP ADDRESS DECODE
- INPUTS PROTECTED – ALL INPUTS HAVE PROTECTION AGAINST STATIC CHARGE.
- LOW COST PACKAGING – 18 PIN SILICONE AND 18 PIN CERAMIC DUAL IN-LINE

APPLICATIONS

CORE MEMORY REPLACEMENT
BUFFER STORES
MAIN MEMORY

PROCESS TECHNOLOGY

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

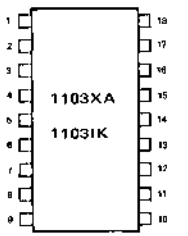
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric

SILICONE PACKAGING (Cont'd)

material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

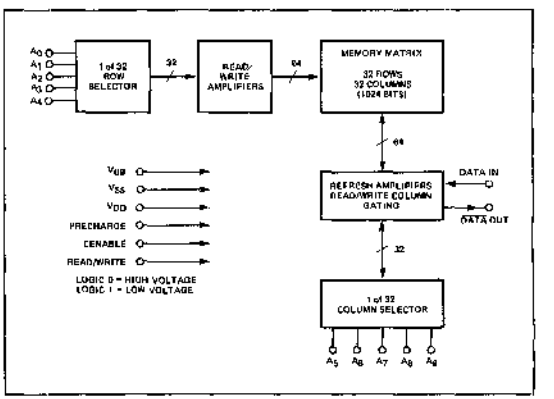


1. Address 3
2. Address 2
3. Address 0
4. Address 1
5. Precharge
6. Address 9
7. Address 6
8. Address 5
9. Address 7
10. V_{BB}
11. V_{DD}
12. Data In
13. Address 8
14. $\overline{\text{Data Out}}$
15. Address 4
16. Cenable
17. V_{SS}
18. Read/write

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
1103XA	18-Pin DIP Silicone	0-70°C
1103IK	18-Pin DIP Ceramic	0-70°C

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS(10)

Operating Ambient Temperature	0°C to 70°C	Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.0W
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V		

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS}(1) = 16V ± 5%, (V_{BB} − V_{SS})(6) = 3V to 4V, V_{DD} = 0V unless otherwise specified (Note 9).

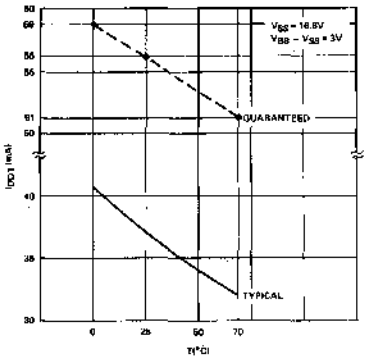
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All input pins)			1	μA	V_{IN} = 0V, T_A = 25°C
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0V, T_A = 25°C
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}(2)	Supply Current During t_{PC}		37	56	mA	All Addresses = 0V Precharge = 0V Cenable = V_{SS}; T_A = 25°C
I_{DD2}(2)	Supply Current During t_{OV}		38	59	mA	All Addresses = 0V Precharge = 0V Cenable = 0V; T_A = 25°C
I_{DD3}(2)	Supply Current During t_{POV}		5.5	11	mA	Precharge = V_{SS} Cenable = 0V; T_A = 25°C
I_{DD4}(2)	Supply Current During t_{CP}		3	4	mA	Precharge = V_{SS} Cenable = V_{SS}; T_A = 25°C
I_{DD}(5)AV	Average Supply Current		17	25	mA	Cycle Time = 580 ns; Precharge Width = 190 ns; T_A = 25°C
V_{IL1}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
V_{IL2}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
V_{IL3}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
V_{IL4}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
V_{IH1}(7)	Input High Voltage (All Inputs)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
V_{IH2}(7)	Input High Voltage (All Inputs)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	Output High Current	600	900	4000	μA	T_A = 25°C
I_{OH2}	Output High Current	500	800	4000	μA	T_A = 70°C
I_{OL}	Output Low Current	See Note 3				R_{LOAD} = 100Ω(4)
V_{OH1}	Output High Voltage	60	90	400	mV	T_A = 25°C
V_{OH2}	Output High Voltage	50	80	400	mV	T_A = 70°C
V_{OL}	Output Low Voltage	See Note 3				

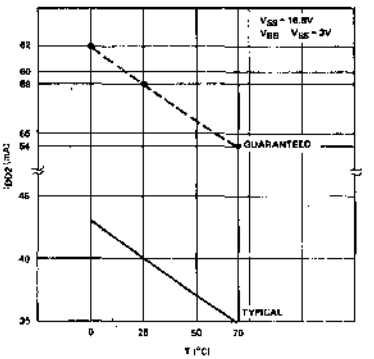
NOTES:

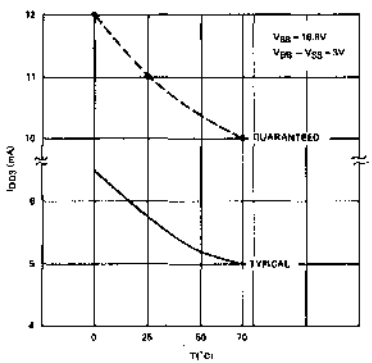
1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.
5. This parameter is periodically sampled and is not 100% tested.
6. (V_{BB} − V_{SS}) supply should be applied at or before V_{SS}.
7. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value between 0°C and 70°C can be calculated using a straight-line relationship.
8. The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS}−14.5 @ 70°C (same values as those specified for the address and date-in lines) with a 40 ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

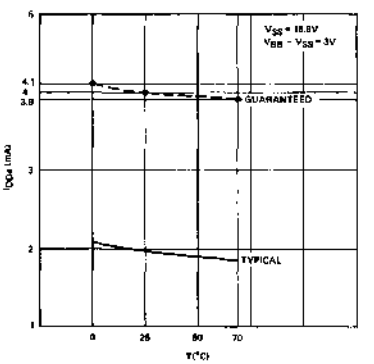
CHARACTERISTIC CURVES

SUPPLY CURRENT VS TEMPERATURE

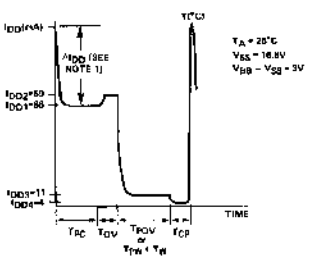








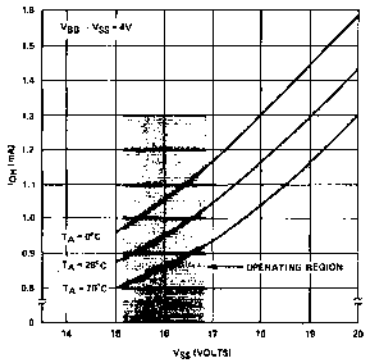
I_{DD} VS TIME

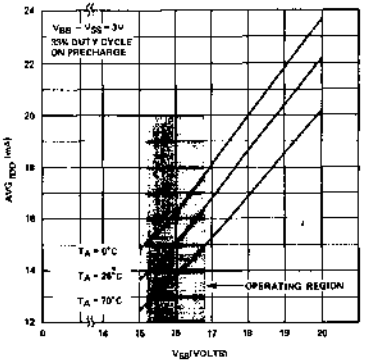


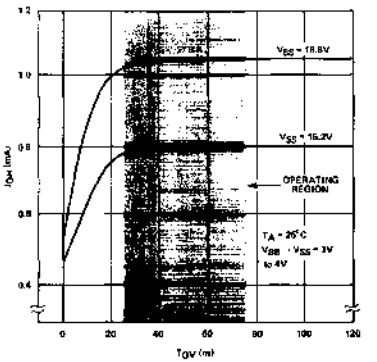
NOTES:

1. ΔI_{DD} is due to charging of internal device node capacitance at precharge.
2. These values are taken from a single pulse measurement.

CHARACTERISTIC CURVES (Cont'd)







AC CHARACTERISTICS $T_A = 25°C$, $V_{SS} = 16 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	Time Between Refresh			2	ms	
t_{AC}(1)	Address to Cenable Set Up Time	115			ns	
t_{CA}	Cenable to Address Hold Time	20			ns	
t_{PC}(1)	Precharge to Cenable Delay	125			ns	
t_{OVL}	Precharge & Cenable Overlap, Low	25		75	ns	
t_{CP}	Cenable to Precharge Delay	85			ns	
t_{OVH}	Precharge & Cenable Overlap, High			140	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	Read Cycle	480			ns	
t_{POV}	Precharge to End of Cenable	165		500	ns	
t_{PO}	End of Precharge to Output Delay			120	ns	$t_T = 20$ ns
t_{ACC1}(1)	Address to Output Access	300			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; $C_{LOAD} = 100$ pF, $R_{LOAD} = 100\Omega$, $V_{REF} = 40$ mV
t_{ACC2}(1)	Precharge to Output Access	310			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; $C_{LOAD} = 100$ pF, $R_{LOAD} = 100\Omega$, $V_{REF} = 40$ mV

AC CHARACTERISTICS (Cont'd)

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}(1)	Write Cycle	580			ns	t_T = 20 ns
t_{RWC}(1)	Read/Write Cycle	580			ns	
t_{PW}	Precharge to Read/Write Delay	165		500	ns	
t_{WP}	Read/Write Pulse Width	50			ns	
t_W	Read/Write Set Up Time	80			ns	
t_{DW}	Data Set Up Time	105			ns	
t_{DH}	Data Hold Time	10			ns	
t_{PO}	End of Precharge to Output Delay			120	ns	C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV
t_P	Time to Next Precharge	0			ns	
t_{CW}	Read/Write Hold Time			10	ns	

CAPACITANCE (note 2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{AD}	Address Capacitance		5	7	pF	V_{IN} = V_{SS}
C_{PR}	Precharge Capacitance		15	18	pF	V_{IN} = V_{SS}
C_{CE}	Cenable Capacitance		15	18	pF	V_{IN} = V_{SS}
C_{RW}	Read/Write Capacitance		11	15	pF	V_{IN} = V_{SS}
C_{IN1}	Data Input Capacitance		4	5	pF	Cenable = 0V V_{IN} = V_{SS}
C_{IN2}	Data Input Capacitance		2	4	pF	Cenable = V_{SS} V_{IN} = V_{SS}
C_{OUT}	Data Output Capacitance		2	3	pF	V_{OUT} = 0V

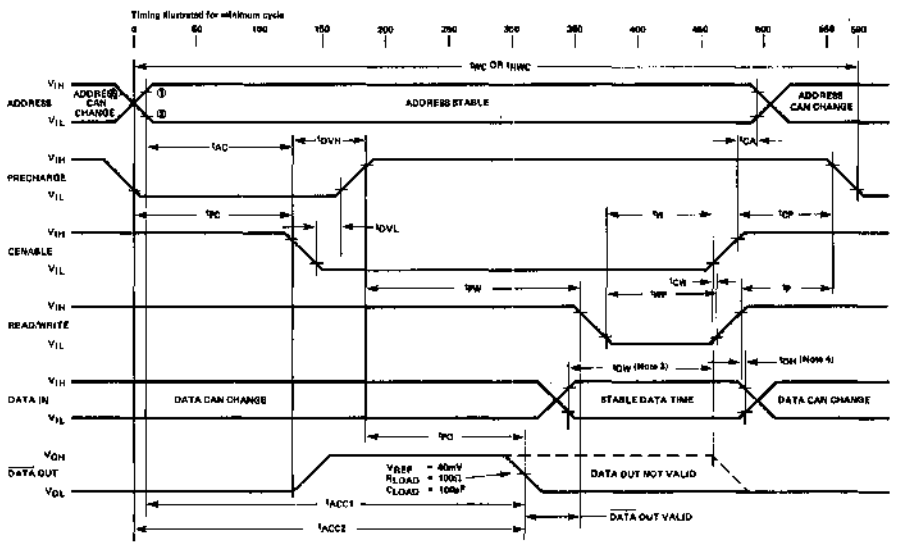
f = 1 MHz
All Unused Pins are at A.C. Ground

(1) These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} − 14.2V @ 0°C and V_{SS}−14.5V @ 70°C as defined on page 2.

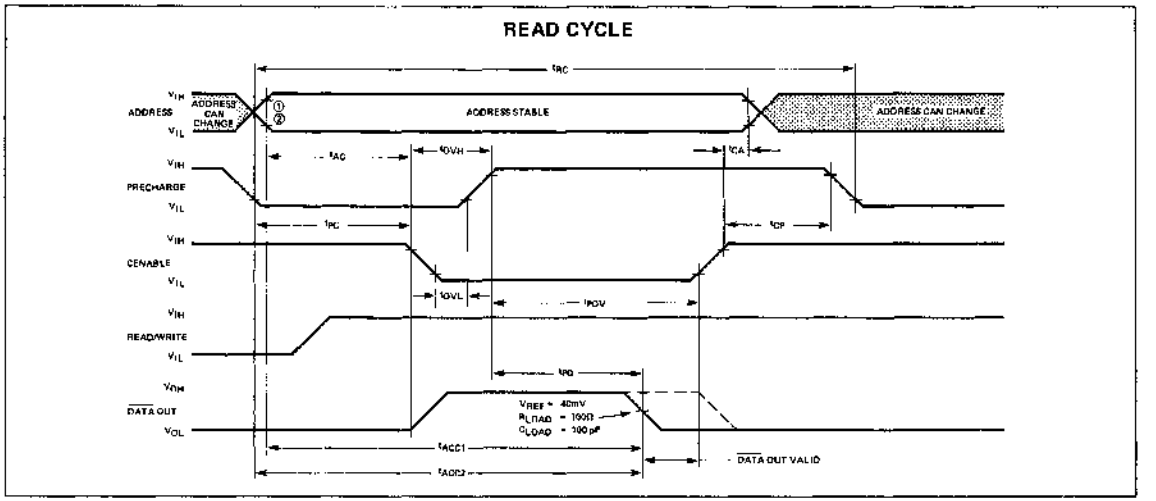
(2) This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic packages only.

TIMING DIAGRAM

WRITE CYCLE OR READ/WRITE CYCLE



TIMING DIAGRAM (Cont'd)



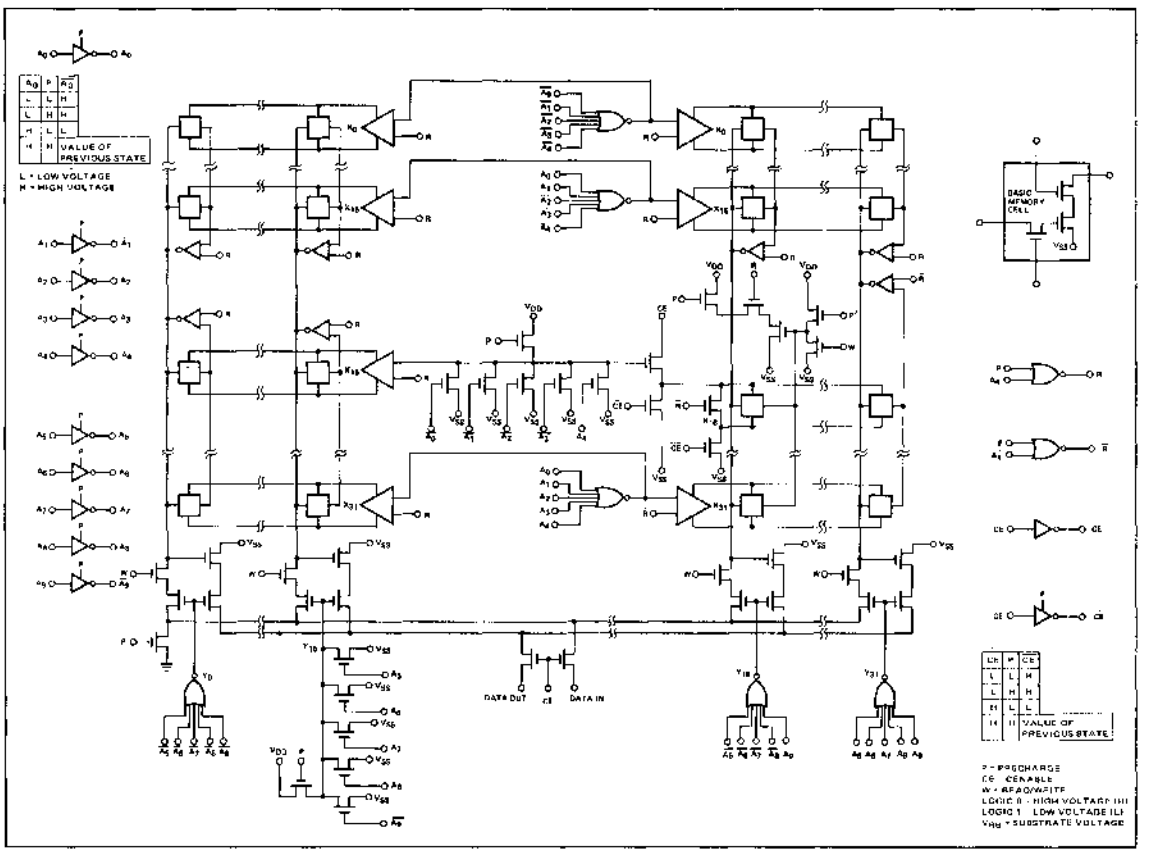
NOTES:

① V_{DD} + 2V, ② V_{SS} - 2V — t_T is defined as the transitions between these two points.

3 t_{DW} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first.

4 t_{DH} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first.

CIRCUIT SCHEMATIC



FULLY DECODED RANDOM ACCESS 1024-BIT DYNAMIC MEMORY (HIGH SPEED VERSION)

1103-1

SILICON GATE MOS

DESCRIPTION

The Signetics 1103-1 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T28 Sense Amp, and 3207 Clock Driver.

FEATURES

- LOW POWER DISSIPATION – DISSIPATES POWER PRIMARILY ON SELECTED CHIPS
- ACCESS TIME – 150 nsec.
- CYCLE TIME – 340 nsec.
- REFRESH PERIOD – 1 MILLISECOND FOR 0-55°C AMBIENT
- OR-TIE CAPABILITY
- SIMPLE MEMORY EXPANSION WITH CHIP ENABLE
- FULLY DECODED – ON-CHIP ADDRESS DECODE
- INPUTS PROTECTED – ALL INPUTS HAVE PROTECTION AGAINST STATIC CHARGE
- LOW COST PACKAGING – 18 PIN SILICONE AND 18 PIN CERAMIC DUAL IN-LINE

APPLICATIONS

CORE MEMORY REPLACEMENT
BUFFER STORES
MAIN MEMORY

PROCESS TECHNOLOGY

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

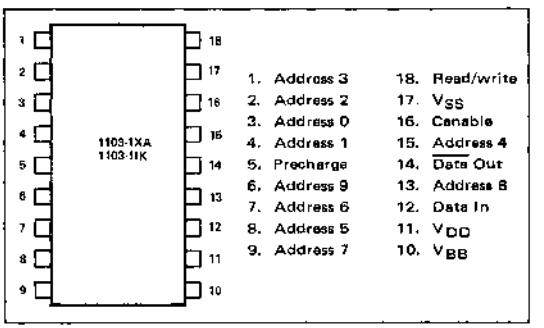
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric

SILICONE PACKAGING (Cont'd)

material over the silicon gate-oxide substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

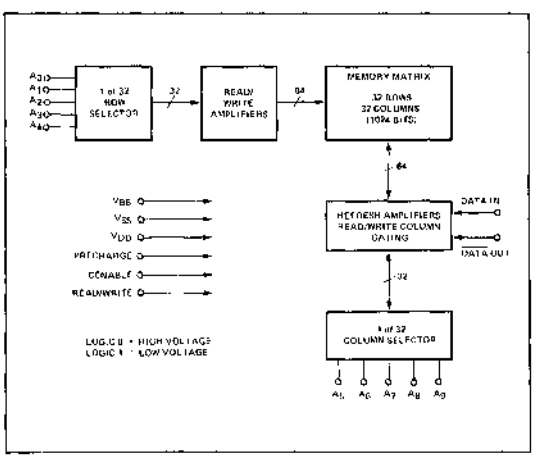
PIN CONFIGURATION (Top View)



PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP RANGE
1103-1XA	18-Pin DIP Silicone	0–55°C
1103-1IK	18-Pin DIP Ceramic	0–55°C

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS [8]

Operating Ambient Temperature	0°C to 55°C	Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.0W
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V		

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to −55°C, V_{SS}[1] = 19V ± 5%, ($V_{BB} - V_{SS}$)[6] = 3V to 4V, V_{DD} = 0V unless otherwise specified (Note 7).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All input pins)			10	µA	V_{IN} = 0V, T_A = 25°C
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0V, T_A = 25°C
I_{BB}	V_{BB} Supply Current			100	µA	
I_{DD1}[2]	Supply Current During t_{PC}		45	60	mA	All Addresses = 0V Precharge = 0V Cenable = V_{SS}; T_A = 25°C
I_{DD2}[2]	Supply Current During t_{0V}		50	68.5	mA	All addresses = 0V Precharge = 0V Cenable = 0V; T_A = 25°C
I_{DD3}[2]	Supply Current During t_{POV}		8.5	11	mA	Precharge = V_{SS} Cenable = 0V; T_A = 25°C
I_{DD4}[2]	Supply Current During t_{CP}		3	4	mA	Precharge = V_{SS} Cenable = V_{SS}; T_A = 25°C
I_{DD}[5]AV	Average Supply Current		20	23	mA	Precharge Width = 150ns @ 50% Cycle Time = 340 ns; T_A = 25°C
V_{IL1}	Input Low Voltage (All address and data-in lines)	V_{SS}−20		V_{SS}−18	V	
V_{IH1}	Input High Voltage (All Inputs)	V_{SS}−1		V_{SS}+1	V	
I_{OH1}	Output High Current	1.15	1.3	7.0	mA	T_A = 25°C, R_{LOAD} = 100Ω[4]
I_{OH2}	Output High Current	0.9	1.15	7.0	mA	T_A = 55°C, R_{LOAD} = 100Ω[4]
I_{OL}	Output Low Current		See Note 3			
V_{OH1}	Output High Voltage	115	130	700	mV	T_A = 25°C, R_{LOAD} = 100Ω[4]
V_{OH2}	Output High Voltage	90	115	700	mV	T_A = 55°C, R_{LOAD} = 100Ω[4]
V_{OL}	Output Low Voltage		See Note 3			

NOTES:

1. The V_{SS} current drain is equal to ($I_{DD} + I_{OH}$) or ($I_{DD} + I_{OL}$).
2. See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
3. The output current when reading a low output is the leakage current of the 1103-1 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.
5. This parameter is periodically sampled and is not 100% tested.
6. ($V_{BB} - V_{SS}$) supply should be applied at or before V_{SS}.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

AC CHARACTERISTICS $T_A = 0°C$ to $+55°C$; $V_{SS} = 19 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	Time Between Refresh			1	ms	
t_{AC}	Address to Cenable Set Up Time	30			ns	
t_{CA}	Cenable to Address Hold Time	10			ns	
t_{PC}	Precharge to Cenable Delay	60			ns	
t_{OVL}	Precharge & Cenable Overlap, Low	5		30	ns	
t_{CP}	Cenable to Precharge Delay	40			ns	
t_{OVH}	Precharge & Cenable Overlap, High			85	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	Read Cycle	300			ns	
t_{POV}	Precharge to End of Cenable	115		500	ns	
t_{PO}(1)	End of Precharge to Output Delay			75	ns	t_T = 20 ns
t_{ACC1}(1)	Address to Output Access	150			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; C_{LOAD} = 50 pF, R_{LOAD} = 100Ω
t_{ACC2}(1)	Precharge to Output Access	180			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$; V_{REF} = 80 mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}	Write Cycle	340			ns	t_T = 20 ns
t_{RWC}(1)	Read/Write Cycle	340			ns	
t_{PW}	Precharge to Read/Write Delay	115		500	ns	
t_{WP}	Read/Write Pulse Width	20			ns	
t_W	Read/Write Set Up Time	20			ns	
t_{DW}	Data Set Up Time	40			ns	
t_{DH}	Data Hold Time	10			ns	
t_{PO}(1)	End of Precharge to Output Delay			75	ns	C_{LOAD} = 50 pF, R_{LOAD} = 100Ω, V_{REF} = 80 mV
t_P	Time to Next Precharge	0			ns	
t_{CW}	Read/Write Hold Time			15	ns	

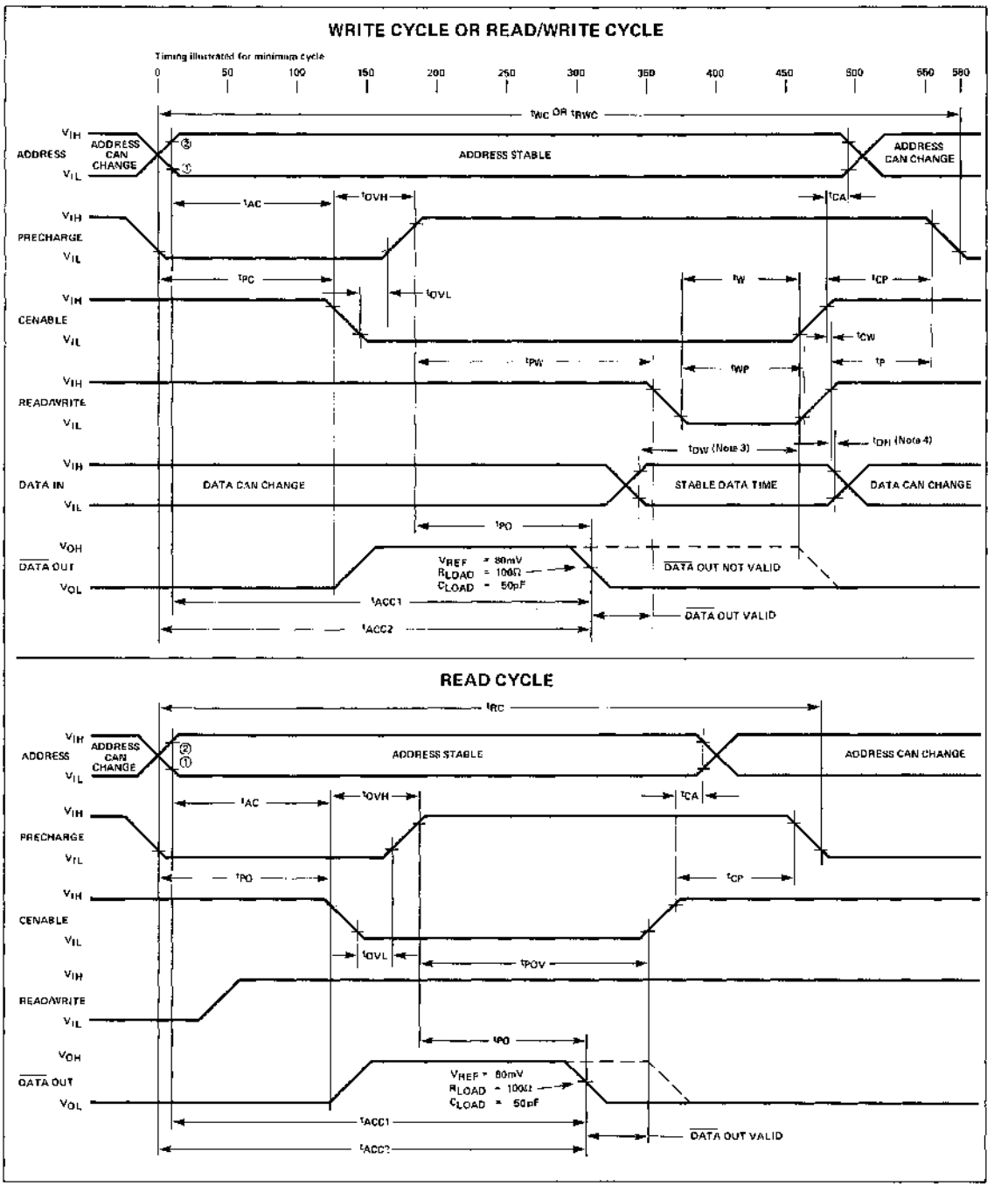
CAPACITANCE (note 2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{AD}	Address Capacitance		5	7	pF	$V_{IN} = V_{SS}$; f = 1 MHz, All Unused Pins are at A.C. Ground
C_{PR}	Precharge Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance		11	15	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance		4	5	pF	Cenable = 0V, $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance		2	4	pF	Cenable = V_{SS}, $V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance		2	3	pF	V_{OUT} = 0V

(1) These times will degrade by 35 ns if a V_{REF} point of 40 mV is chosen instead of the 80 mV point defined in this specification.

(2) This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic packages only.

TIMING DIAGRAM

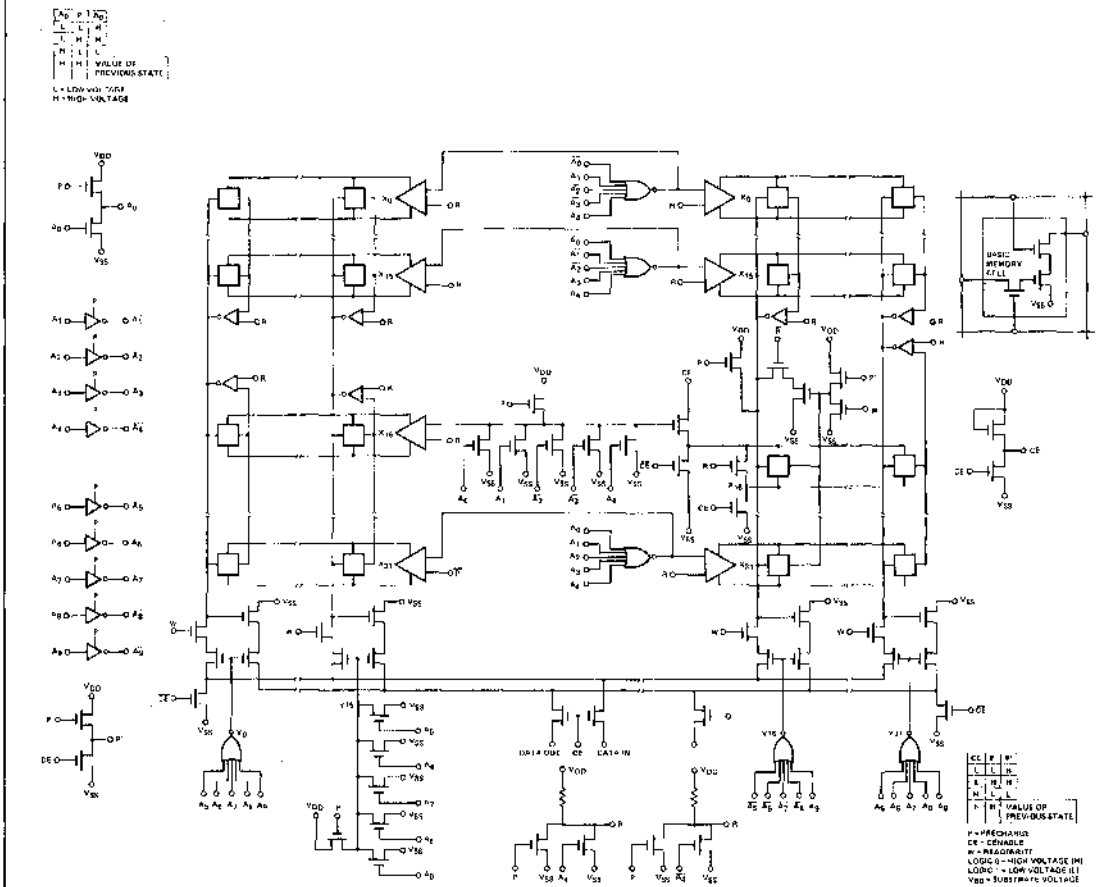


NOTES:

① $V_{DD} + 2V$
② $V_{SS} - 2V$
t_T is defined as the transitions between these two points.

3 t_{DW} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first.
4 t_{DH} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first.

CIRCUIT SCHEMATIC



(FOR REFERENCE ONLY, NOT RECOMMENDED FOR NEW DESIGNS)

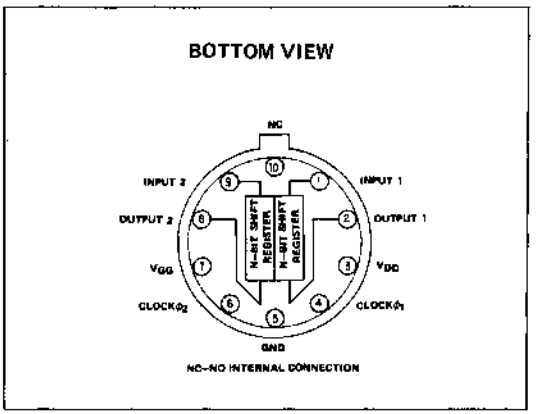
METAL GATE MOS 2000 SERIES

DESCRIPTION

The S2001K, S2002K, S2003K, S2004K, and S2005K are Dual Static Shift Registers manufactured with a "P" channel enhancement mode process.

The registers vary in length from dual 16 to dual 100. Two power supplies and 2 external 28 volt clocks are required. Static operation is assured with a third clock phase that is generated on the chip. The pin configuration allows interchanging of register lengths without rewiring the socket. Data is transferred into the register during ϕ_1 and output data appears on the negative-going edge of ϕ_2. For static operation ϕ_1 must be a "0" and ϕ_2 "1".

PIN CONFIGURATION



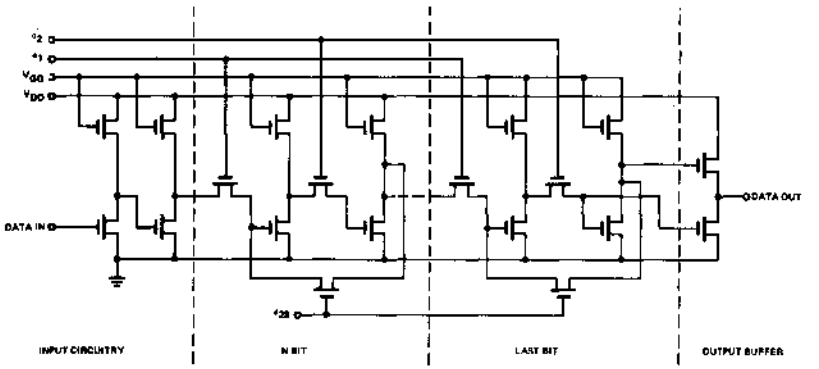
PARTS IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
S2001K	16	10 Pin TO-100
S2002K	25	10 Pin TO-100
S2003K	32	10 Pin TO-100
S2004K	50	10 Pin TO-100
S2005K	100	10 Pin TO-100

ABSOLUTE MAXIMUM RATINGS

V_{dd} with respect to Gnd	-16V to 0.3V
V_{gg} with respect to Gnd	-30V to 0.3V
Clock and in with respect to Gnd	-30V to 0.3V
Operating Temperature	-55°C to +85°C
Storage Temperature	-55°C to +150°C

CIRCUIT SCHEMATIC



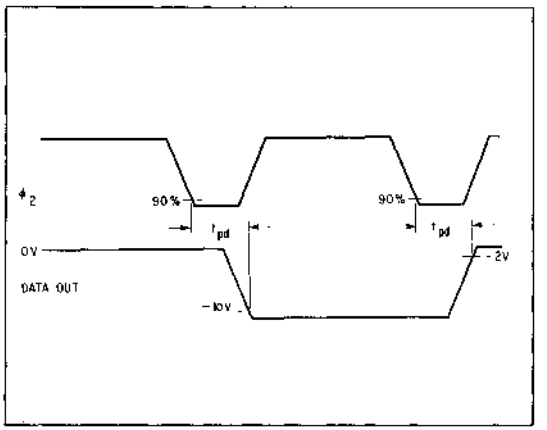
ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4 and 5)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN	TYP	MAX	UNITS	TEMP °C	V_{DD}	V_{GG}	Vin	$V\phi_1$	$V\phi_2$	OUTPUT	
"1" Output Voltage	-11	-13		V		-13	-27	-10	-27	-27		5
"0" Output Voltage		-0.3	-1	V		-15	-29	-2	-29	-29		5
Output Drive Capability												
2001	-8	-10		V		-13	-27	-10	-27	-27		R_L = 17kΩ to Gnd
	-4	-6		V		-13	-27	-10	-27	-27		R_L = 4 kΩ to Gnd
2002/3/4/5	-10	-11		V		-13	-27	-10	-27	-27		R_L = 17 kΩ to Gnd
	-6	-8		V		-13	-27	-10	-27	-27		R_L = 4 kΩ to Gnd
Input Leakage Current												
Data Inputs			0.5	μA	+85	0	0	-20	0	0		
Clock Inputs												
ϕ_1			50	μA	+85	0	0	0	-28	0		
ϕ_2			50	μA	+85	0	0	0	0	-28		
Output Impedance												
2001			2.5	kΩ		-13	-27	-2	-27	-27	0 to -1V	
2002/3/4/5			1.5	kΩ		-13	-27	-2	-27	-27	0 to -1V	
Input Capacitance												
Data Inputs		3	5	pF	25	-14	-28	0	0	0		8
Clock Inputs												
2001		8	10	pF	25	-14	-28	0	0	0		8
2002		8	12	pF	25	-14	-28	0	0	0		8
2003		8	13	pF	25	-14	-28	0	0	0		8
2004		12	18	pF	25	-14	-28	0	0	0		8
2005		16	33	pF	25	-14	-28	0	0	0		8
Power Supply Current												
I_{DD}												
2001		-3	-10	mA	-55	-15	-29		0	-29		
2002		-5	-20	mA	-55	-15	-29		0	-29		
2003		-6	-24	mA	-55	-15	-29		0	-29		
2004		-7	-17	mA	-55	-15	-29		0	-29		
2005		-14	-32	mA	-55	-15	-29		0	-29		
I_{GG}												
2001/2/3		-0.8	-3.5	mA	-55	-15	-29		0	-29		
2004/5		-0.5	-3.0	mA	-55	-15	-29		0	-29		
Propagation Delay (tpd) from ϕ_2												
2001		300	475	ns	25	-14	-28		-28	-28		6, 7
2002/3/4/5		300	450	ns	25	-14	-28		-28	-28		6, 7

NOTES FOR ELECTRICAL CHARACTERISTICS:

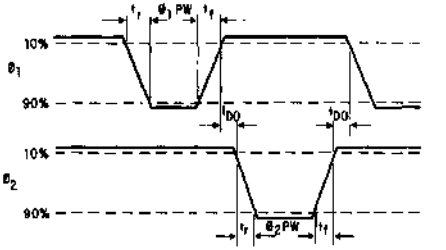
1. Parameter valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to ground.
3. Negative logic definition: "DOWN" Level = "1", "UP" Level = "0".
4. Manufacturer reserves the right to make design and process changes and improvements.
5. Output voltage levels valid from D.C. to 1 MHz.
6. See output timing diagram.
7. Output load is 10 pF and 1 MΩ
8. f = 1 MHz, Vac = 25 mV_{rms}. All pins not specifically referenced are tied to guard terminal for capacitance tests. Output pins are left open.
9. All typical values are at 25°C and nominal supply voltages.

OUTPUT TIMING DIAGRAM



FORCING FUNCTIONS

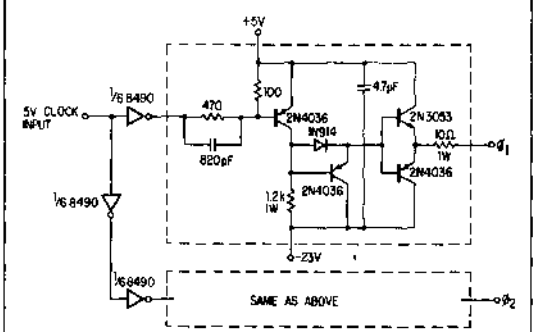
CLOCK REQUIREMENTS



VOLTAGE LEVELS	MIN	TYP	MAX	UNITS
ϕ_1 ϕ_2 "0"	0	-1	-2.0	Volts
ϕ_1 ϕ_2 "1"	-27	-28	-29	Volts
TIMING				
t_r & t_f	.025		5	μsec
ϕ_1 PW	0.4		10	μsec
ϕ_2 PW	0.4			μsec
t_{DO}	0			μsec

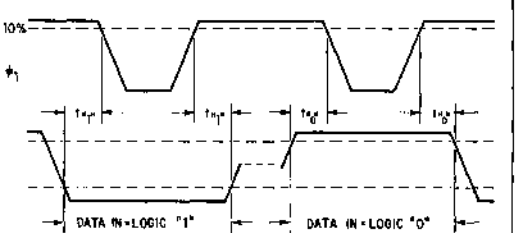
Note: ϕ_2 may not be at "0" logic level for more than 10 μs.

CLOCK DRIVER



Note: At high repetition rates and/or high capacitance loads, the transistors may require heat sinking, i.e., 1000 pF at 1 MHz.

INPUT REQUIREMENTS



CHARACTERISTIC	MIN	MAX	UNITS
Data In "0"	+0.3	-2.0	Volts
Data In "1"	-10		Volts
$t_{s(1)}$ & $t_{h(0)}$	0		μsec

Note. Data In must be stable between the 10% points of ϕ_1.

signetics

DUAL 100-BIT STATIC SHIFT REGISTER DC TO 3 MHZ

2010

(FOR REFERENCE ONLY, NOT RECOMMENDED FOR NEW DESIGNS)

METAL GATE MOS 2000 SERIES

DESCRIPTION

The N2010K Dual 100-Bit Static Shift Register is designed for use at shift rates from 0 to 3 MHz.* The device employs "P" channel enhancement mode MOS techniques. Power supply requirements are −14 and −28 Vdc. Clocking is provided by two external −28 volt clock phases. A delayed second clock phase (ϕ_{2S}) is generated on the chip.

Data is transferred into the register during ϕ_1. Output data appears on the negative going edge of ϕ_2. For static operation, ϕ_1 must be a "0" and ϕ_2 a "1".

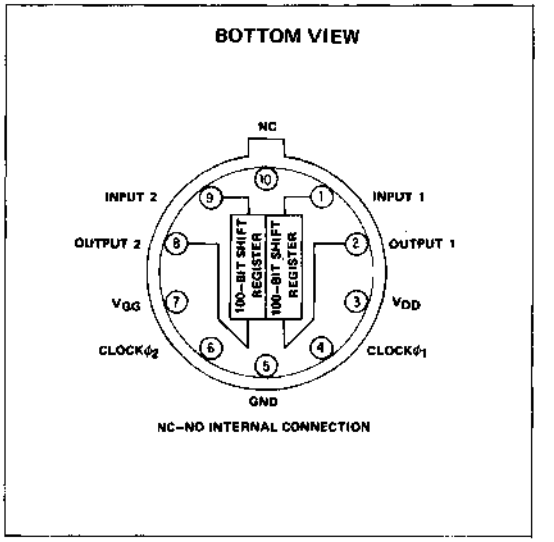
The N2010K is a direct pin replacement for the S2005K/3003 1MHz Static Shift Register.

*(25°)

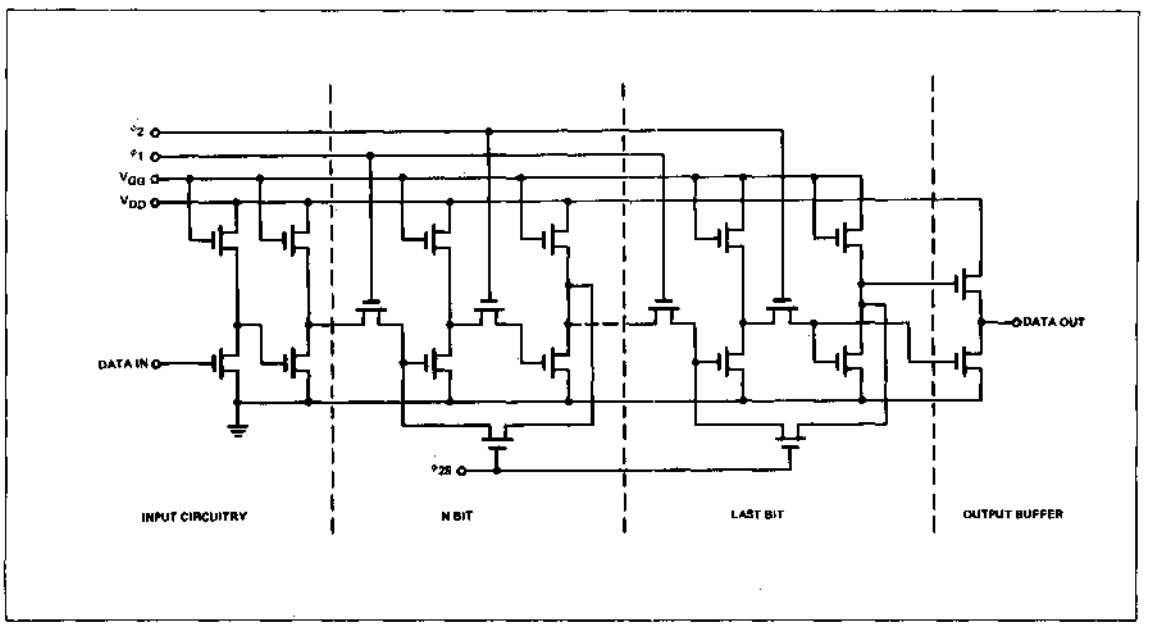
ABSOLUTE MAXIMUM RATINGS:

V_{DD} with respect to Gnd	−16V to 0.3V
V_{GG} with respect to Gnd	−30 to 0.3V
Clock and Input with respect to Gnd	−30V to 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C

PIN CONFIGURATION



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 9)

RECOMMENDED POWER SUPPLY VOLTAGES: V_{DD} = −14 ±1 Vdc, V_{GG} = −28 ±1Vdc

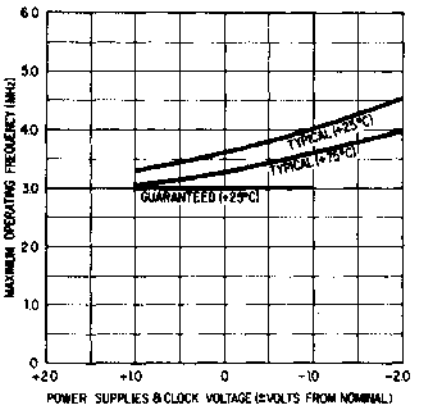
CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS							NOTES
	MIN	TYP	MAX		TEMP °C	V_{DD}	V_{GG}	V_{in}	$V_{\phi1}$	$V_{\phi2}$	OUTPUT	
"1" Output Voltage	−8	−10		V	25	−13	−27	−7	−27	−27		5, 7
"0" Output Voltage		−0.3	−1.0	V	25	−15	−29	−2	−29	−29		5, 7
Output Drive Capability	−4	−6		V	25	−13	−27	−7	−27	−27		R_L = 4kΩ to Gnd
Input Leakage Current												
Data Inputs			−0.5	μA	25	0	0	−15	0	0		
Clock Inputs												
ϕ_1			−50	μA	25	0	0	0	−28	0		
ϕ_2			−50	μA	25	0	0	0	0	−28		
Output Impedance			1.5	kΩ	25	−13	−27	−2	−27	−27	0 to −1V	
Input Capacitance												
Data Inputs		3	5	pF	25	−14	−28	0	0	0		8
Clock Inputs		16	33	pF	25	−14	−28	0	0	0		8
Power Supply Current												
I_{DD}		−14	−20	mA	25	−15	−29		0	−29		
I_{GG}		−0.8	−3.0	mA	25	−15	−29		0	−29		
Propagation Delay (tdp) from ϕ_2		200	250	ns	25	−14	−28		−28	−28		6, 7

NOTES:

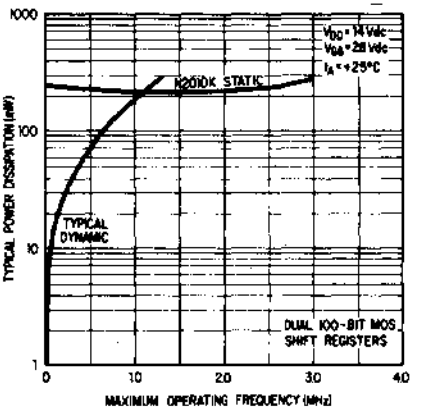
1. Parameter valid at +25°C unless otherwise specified.
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to ground.
3. Negative logic definition: "DOWN" Level = "1", "UP" Level = "0".
4. Manufacturer reserves the right to make design and process changes and improvements.
5. Output voltage levels valid from DC to 3 MHz.
6. See output timing diagram.
7. Output load is 10pF and 1 MΩ.
8. f = 1 MHz, V_{ac} = 25mV rms. All pins not specifically referenced are tied to guard terminal for capacitance tests. Output pins are left open.
9. All typical values are at 25°C and nominal supply voltages.

TYPICAL PERFORMANCE CHARACTERISTICS

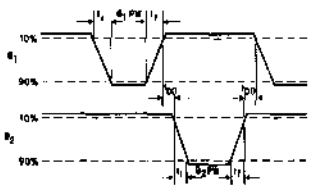
MAXIMUM OPERATION FREQUENCY
VERSUS CLOCK AND SUPPLY VOLTAGE



POWER DISSIPATION
VERSUS OPERATING FREQUENCY



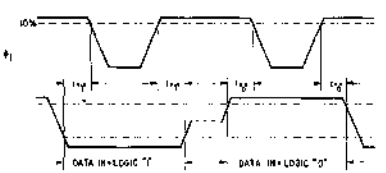
CLOCK REQUIREMENTS



VOLTAGE LEVELS	MIN	NOM	MAX	UNITS
ϕ_1 ϕ_2 "0"	0	-1	-2.0	Volts
ϕ_1 ϕ_2 "1"	-27	-28	-29	Volts
TIMING				
t_r & t_f	.010		5	μsec
ϕ_1 PW	0.10		10	μsec
ϕ_2 PW	0.15			μsec
t_{DO}	0			μsec
Clock Repetition Rate	0		3	MHz

Note: ϕ_2 may not be at "0" logic level for more than 10 μs.

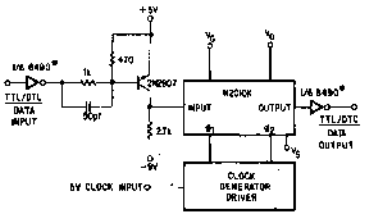
INPUT REQUIREMENTS



CHARACTERISTIC	MIN	MAX	UNITS
Data in "0"	+0.3	-2.0	Volts
Data in "1"	-7.0		Volts
t_{r_1} & t_{f_0}	0		μsec

Note: Data In must be stable between the 10% points of ϕ_1.

TTL INTERFACE REQUIREMENTS

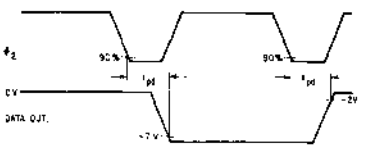


NOTES:

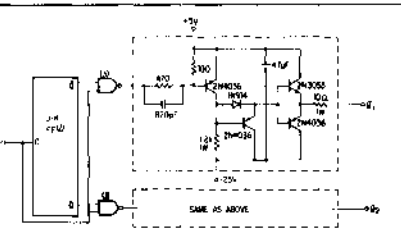
1. Register ground (V_S) is tied to the bipolar integrated circuit V_{CC} power supply for proper biasing.
2. V_S = +5VDC
   V_D = -9 VDC
   V_G = -23 VDC

*3. Signetics Corp. N8490A

OUTPUT TIMING DIAGRAM



CLOCK DRIVER



NOTES:

1. At high repetition rates and/or high capacitance loads, the transistors may require heat sinking, i.e., 1000 pF at 3MHz.
2. ½ N8822B, SP322B etc.
3. ½ N8880A, SP387A etc.

signetics

FULLY DECODED 1024 AND 2048 STATIC READ-ONLY MEMORIES

2400

METAL GATE MOS 2400 SERIES

DESCRIPTION

The Signetics 2400 Series devices are high speed, fully decoded, MOS static 1024 and 2048-bit read-only memories offering 128X8, 256X8, 256X4, and 512X4 organizations.

Two output structure options, plus both single line and 3-bit binary coded chip select options, provide for wide versatility and economy of application. The devices interface directly with standard TTL/DTL or MOS logic circuits. Process technology is P-Channel enhancement mode.

FEATURES

- **128X8, 256X8, 256X4, 512X4 ORGANIZATIONS**
- **STATIC OPERATION – NO CLOCKS**
- **FULLY DECODED ADDRESS**
- **500ns TYPICAL ACCESS TIME**
- **TTL/DTL COMPATIBILITY**
- **OUTPUT OPTIONS:**
  - **BARE DRAIN**
  - **20K OHM PULL-DOWN RESISTOR**
- **TWO CHIP SELECT OPTIONS:**
  - **SINGLE LINE**
  - **3-BIT BINARY CODED**
- **EBCDIC-ASCII CONVERSION TABLE IS CATALOG STANDARD, OTHER STANDARDS AVAILABLE**
- **+12, -12V POWER SUPPLIES**
- **STANDARD PINNING IN 16 AND 24 PIN CERAMIC DUAL IN-LINE PACKAGES**

APPLICATIONS:

CODE CONVERSION
LOOK-UP TABLES
MICRO-PROGRAMMING
RANDOM LOGIC SYNTHESIS
CHARACTER GENERATION

SPECIAL FEATURES

Output Options: Two output structure options allow ease of interfacing with TTL/DTL or other MOS circuits.

Chip Select Options: Both the 2420 and 2430 group may be specified with either single line chip select or a 3 line, 3-bit binary coded chip select. The coded chip select allows one-of-eight chip selection without external logic components for larger memory matrices. The 2410 group is pin limited to single line chip select.

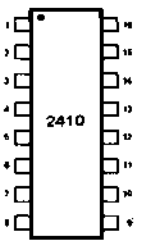
Package Options: The 256X4 organization is available in *either* a 16-pin or 24-pin dual in-line package.

For a detailed listing of part numbers and options see the PART IDENTIFICATION TABLE.

CUSTOM ENCODING

You may describe the particular option you desire in a booklet which will be provided by Signetics. Ask your local Signetics representative for a copy of "SIGNETICS 2400 SERIES STATIC READ-ONLY MEMORIES – MOS-ROM PROGRAMMING". The booklet contains a blank truth table and instructions for preparing punched data cards.

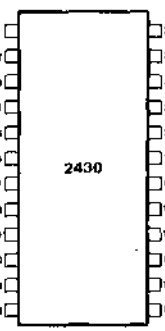
PIN CONFIGURATIONS (Top View)



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
16. V_{DD}
15. Address 4
14. Address 5
13. Address 6
12. Address 7
11. V_{GG}
10. Chip Enable
9. Address 8

1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
24. V_{DD}
23. Chip Enable 3*
22. Chip Enable 2*
21. Address 4
20. Address 5
19. Address 6
18. Address 7
17. V_{GG}
16. Mode Control
15. Chip Enable
14. Address 8
13. No Connection

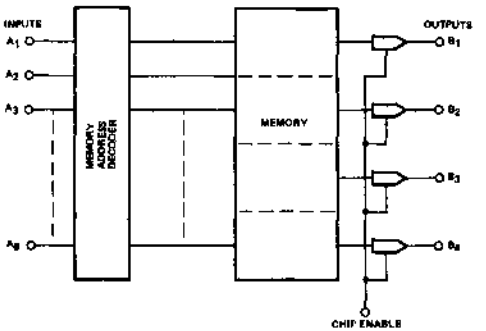
*No connection for single chip enable options.



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
24. V_{DD}
23. Chip Enable 3*
22. Chip Enable 2*
21. Address 4
20. Address 5
19. Address 6
18. Address 7
17. Address 8
16. V_{GG}
15. Mode Control
14. Chip Enable
13. Address 9

*No connection for single chip enable options.

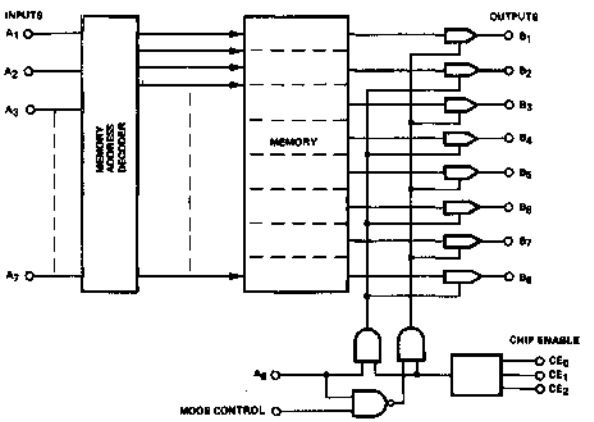
BLOCK DIAGRAMS



2410

OPERATING MODE

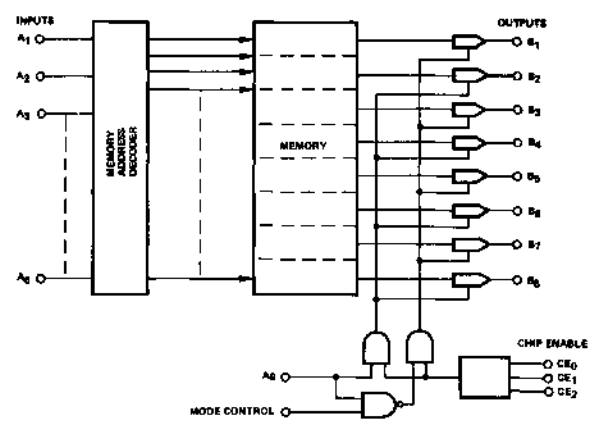
1. Logic "1" level enables outputs.



2420

OPERATING MODES

1. 128 x 8 ROM Connections
   Mode Control – Logic "0"
   A 8 – Logic "1"
2. 256 x 4 ROM Connection
   Mode Control – Logic "1"
   A8 – Logic "0" Enables the odd (B1, B3, B5, B7) outputs.
   – Logic "1" Enables the even (B2, B4, B6, B8) outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.



2430

OPERATING MODES

1. 256 x 8 ROM Connection
   Mode Control – Logic "0"
   A9 – Logic "1"
2. 512 x 4 ROM Connection
   Mode Control – Logic "1"
   A9 – Logic "0" Enables the odd (B1, B3 . . B7) Outputs
   – Logic "1" Enables the even (B2, B4...B8) Outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature		-25°C to +70°C
Storage Temperature		-65°C to + 150°C
Power Dissipation (2)	("Y" Package)	@70°C 1.14W
	("I" Package)	@70°C 0.80W
V_{GG} (3)		-30 to +0.3
V_{DD} (3)		-30 to +0.3
Input Voltage (3, 4)		-30 to +0.3

DC CHARACTERISTICS

T_A = -25°C to +70°C; V_{SS} = +12V (17); V_{DD} = 0V; V_{GG} = -12V ±10% unless otherwise noted (Notes: 10, 11, 12, 13, 14, 16).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input Logic "0"	10			V	
V_{IH}	Input Logic "1"			4	V	
I_{SS}	V_{SS} Power Supply Current		14	20	mA	T_A = 25°C
I_{GG}	V_{GG} Power Supply Current			1	μA	Note 5, T_A = 25°C
I_{IH}	Input Leakage			1	μA	V_{IN} = 0V
R_{PD}	Pull-down Resistor					Note 6
	2410, 20 25, 30, 35		12	20	k ohm	

AC CHARACTERISTICS

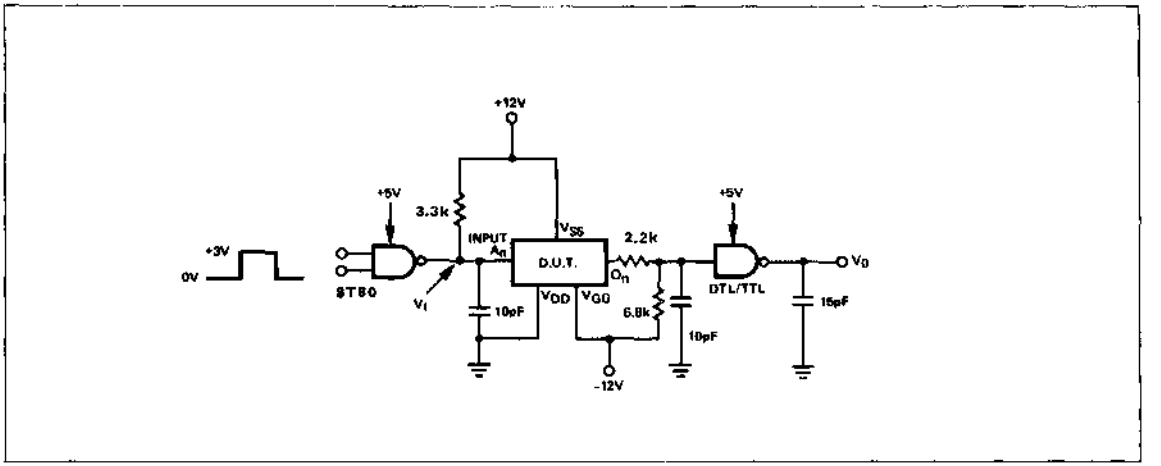
T_A = 25°C; V_{SS} = +12V (17); V_{DD} = 0V; V_{GG} = -12V ±10% unless otherwise noted . (Notes: 11, 12, 13, 14, 16).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0" MOS to MOS	11			V	1 Megohm to Ground, Note 8
V_{OH}	Output Logic "1" MOS to MOS			+3	V	1 Megohm to Ground, Note 8
V_{OL}	Output Logic "0" MOS to TTL	+2.5			V	Note 7, 9
V_{OH}	Output Logic "1" MOS to TTL			+0.4	V	Note 7, 9
t_{A1}	Address Time (bare drain)		500	750	ns	Note 15
t_{A0}	Address Time (bare drain)		400	500	ns	

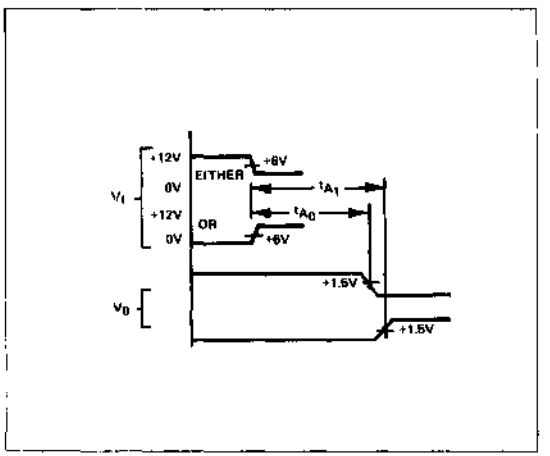
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only. Operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied.
2. For operation at elevated temperatures, the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 70°C/W junction to ambient for the "Y" package. The "I" package is derated based on 100°C/W junction to ambient.
3. These voltages are referenced to network ground terminal (V_{SS}).
4. All inputs are protected against damage by static charge.
5. The V_{GG} supply may be clocked to reduce device power without affecting access time.
6. Output to V_{DD}.
7. 6.8kΩ to V_{GG} plus 1 standard TTL gate input.
8. This test is for devices using a 20kΩ MOS pull down resistor (2410, 20, 25, 30, 35,).
9. This test is for devices supplied with a bare drain output (2411, 21, 26, 31, 36).
10. Parameter valid over operating temperature range unless otherwise specified.
11. All voltage measurements referenced to ground.
12. Manufacturer reserves the right to make design changes and process improvements.
13. Typical values are at 25°C and nominal supply voltages.
14. Negative logic definition is employed for this device, i.e., more negative level is logic "1", most positive level is logic "0".
15. For bare drain devices, T_{A1} is primarily a function of the time constant of the load capacitance and external load resistor ($t_{A1} \cong 4R_L C_L$ +50ns).
16. CAUTION: These devices will be permanently damaged if reversed in board or socket.
17. V_{CC} tolerance is ±10%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 12 volts.

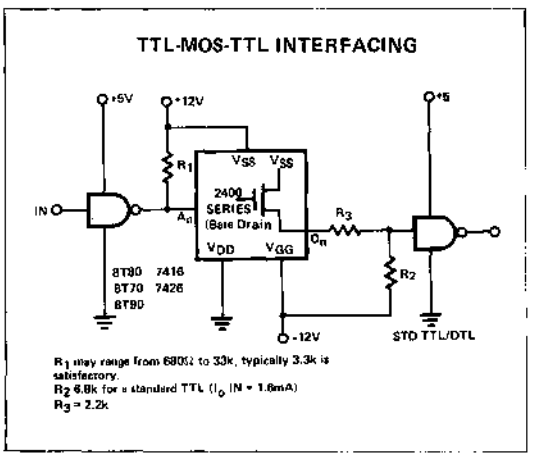
AC TEST SETUP



TIMING DIAGRAM



APPLICATIONS

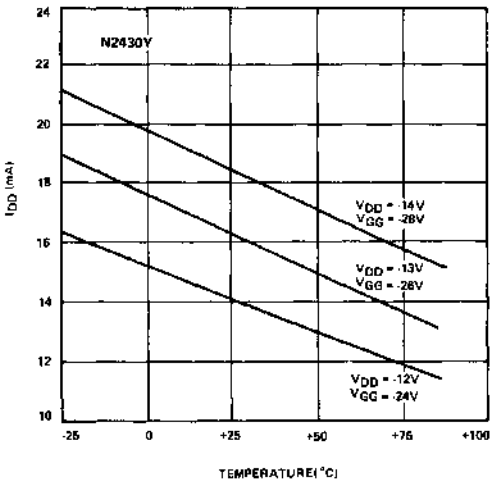


PART IDENTIFICATION TABLE

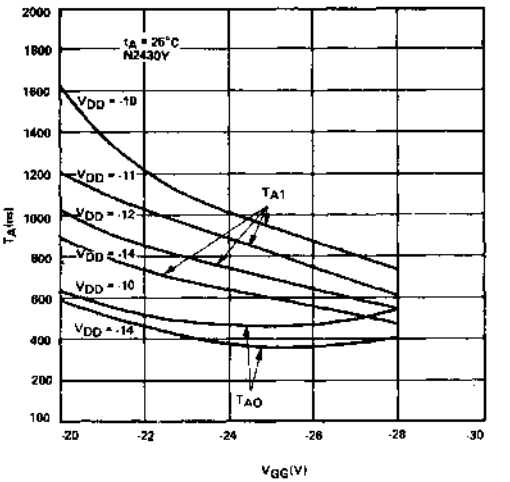
PART	ORGANIZATION	PACKAGE	OUTPUTS	CHIP SELECT CONTROLS
N2410I	256 x 4	16-pin Cer. DIP	20k ohm Pull-down	1
N2411I	256 x 4	16-pin Cer. DIP	Bare Drain	1
N2420Y	128 x 8 or 256 x 4	24-pin Cer. DIP	20k ohm Pull-down	1
N2421Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain	1
N2425Y	128 x 8 or 256 x 4	24-pin Cer. DIP	20k ohm Pull-down	3
N2426Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain	3
N2430Y/CM000	256 x 8 (EBCDIC-ASCII)	24-pin Cer. DIP	20k ohm Pull-down	1
N2430Y	256 x 8 or 512 x 4	24-pin Cer. DIP	20k ohm Pull-down	1
N2431Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain	1
N2435Y	256 x 8 or 512 x 4	24-pin Cer. DIP	20k ohm Pull-down	3
N2436Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain	3

CHARACTERISTIC CURVES

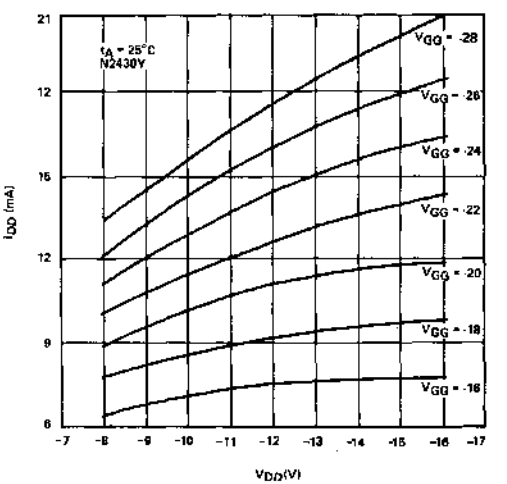
I_{DD} VERSUS TEMPERATURE AND POWER SUPPLY VOLTAGE



ACCESS TIME VERSUS SUPPLY VOLTAGE



I_{DD} VERSUS SUPPLY VOLTAGE



NOTE: For typical curves, V_{SS} = 0V.

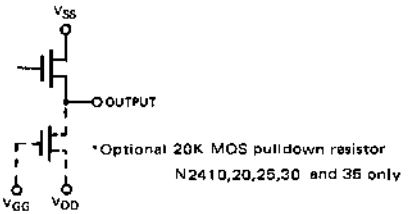
NOTE: Blanks are logic 1's.

CM0000 TRUTH TABLE

EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7	EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7	EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7	EBCDIC WORD #	ASCII Code Bit Number 1 2 3 4 5 6 7
0	0 0 0 0 0 0 0	65		130	0 1 0 0 0 1 1	195	1 1 0 0 0 0 1
1	1 0 0 0 0 0 0	66		131	1 1 0 0 0 1 1	196	0 0 1 0 0 0 1
2	0 1 0 0 0 0 0	67		132	0 0 1 0 0 1 1	197	1 0 1 0 0 0 1
3	1 1 0 0 0 0 0	68		133	1 0 1 0 0 1 1	198	0 1 1 0 0 0 1
4		69		134	0 1 1 0 0 1 1	199	1 1 1 0 0 0 1
5	0 1 1 0 0 0 0	70		135	1 1 1 0 0 1 1	200	0 0 0 1 0 0 1
6		71		136	0 0 0 1 0 1 1	201	1 0 0 1 0 0 1
7	1 1 1 1 1 1 1	72		137	1 0 0 1 0 1 1	202	
8		73		138		203	
9		74		139		204	
10		75	0 1 1 1 0 1 0	140		205	
11	1 1 0 1 0 0 0	76	0 0 1 1 1 1 0	141		106	
12	0 0 1 1 0 0 0	77	0 0 0 1 0 1 0	142		207	
13	1 0 1 1 0 0 0	78	1 1 0 1 0 1 0	143		208	
14	0 1 1 1 0 0 0	79	0 0 1 1 1 1 1	144		209	0 1 0 1 0 0 1
15	1 1 1 1 0 0 0	80	0 1 1 0 0 1 0	145	0 1 0 1 0 1 1	210	1 1 0 1 0 0 1
16	0 0 0 0 1 0 0	81		146	1 1 0 1 0 1 1	211	1 1 1 1 1 1 1
17	1 0 0 0 1 0 0	82		147	0 0 1 1 0 1 1	212	1 0 1 1 0 0 1
18	0 1 0 0 1 0 0	83		148	1 0 1 1 0 1 1	213	0 1 1 1 0 0 1
19	1 1 0 0 1 0 0	84		149	0 1 1 1 0 1 1	214	1 1 1 1 0 0 1
20		85		150	1 1 1 1 0 1 1	215	0 0 0 0 1 0 1
21		86		151	0 0 0 0 1 1 1	216	1 0 0 0 1 0 1
22	0 0 0 1 0 0 0	87		152	1 0 0 0 1 1 1	217	0 1 0 0 1 0 1
23		88		153	0 1 0 0 1 1 1	218	
24	0 0 0 1 1 0 0	89		154		219	
25	1 0 0 1 1 0 0	90	1 0 0 0 0 1 0	155		220	
26		91	0 0 1 0 0 1 0	156		221	
27		92	0 1 0 1 0 1 0	157		222	
28	0 0 1 1 1 0 0	93	1 0 0 1 0 1 0	158		223	
29	1 0 1 1 1 0 0	94	1 1 0 1 1 1 0	159		224	
30	0 1 1 1 1 0 0	95		160		225	
31	1 1 1 1 1 0 0	96	1 0 1 1 0 1 0	161		226	1 1 0 0 1 0 1
32		97	1 1 1 1 0 1 0	162	1 1 0 0 1 1 1	227	0 0 1 0 1 0 1
33		98		163	0 0 1 0 1 1 1	228	1 0 1 0 1 0 1
34		99		164	1 0 1 0 1 1 1	229	0 1 1 0 1 0 1
35		100		165	0 1 1 0 1 1 1	230	1 1 1 0 1 0 1
36		101		166	1 1 1 0 1 1 1	231	0 0 0 1 1 0 1
37	0 1 0 1 0 0 0	102		167	0 0 0 1 1 1 1	232	1 0 0 1 1 0 1
38	1 1 1 0 1 0 0	103		168	1 0 0 1 1 1 1	233	0 1 0 1 1 0 1
39	1 1 0 1 1 0 0	104		169	0 1 0 1 1 1 1	234	
40		105		170		235	
41		106		171		236	
42		107	0 0 1 1 0 1 0	172		237	
43		108	1 0 1 0 0 1 0	173		238	
44		109	1 1 1 1 1 0 1	174		239	
45	1 0 1 0 0 0 0	110	0 1 1 1 1 1 0	175		240	0 0 0 0 1 1 0
46	0 1 1 0 0 0 0	111	1 1 1 1 1 1 0	176		241	1 0 0 0 1 1 0
47	1 1 1 0 0 0 0	112		177		242	0 1 0 0 1 1 0
48		113		178		243	1 1 0 0 1 1 0
49		114		179		244	0 0 1 0 1 1 0
50	0 1 1 0 1 0 0	115		180		245	1 0 1 0 1 1 0
51		116		181		246	0 1 1 0 1 1 0
52		117		182		247	1 1 1 0 1 1 0
53		118		183		248	0 0 0 1 1 1 0
54		119		184		249	1 0 0 1 1 1 0
55	0 0 1 0 0 0 0	120		185		250	
56		121		186		251	
57		122	0 1 0 1 1 1 0	187		252	
58		123	1 1 0 0 0 1 0	188		253	
59		124	0 0 0 0 0 0 1	189		254	
60	0 0 1 0 1 0 0	125	1 1 1 0 0 1 0	190		255	
61	1 0 1 0 1 0 0	126	1 0 1 1 1 1 0	191			
62		127	0 1 0 0 0 1 0	192			
63	0 1 0 1 1 0 0	128		193	1 0 0 0 0 0 1		
64	0 0 0 0 0 1 0	129	1 0 0 0 0 1 1	194	0 1 0 0 0 0 1		

SCHEMATIC DIAGRAM

OUTPUT STRUCTURE



EXERPT FROM SOFTWARE PACKAGE (CARD FORMAT)

CARD 1

COLUMN	DATA
1-4	STARTING AT COLUMN 1 PUNCH "CODED" ON SINGLE
5	E CODED PUNCH THE BINARY CODE CHIP SELECT "101" IF SINGLE LEAVE BLANK
6	LEAVE BLANK
7-8	PUNCH THE ROW ORGANIZATION DESIRED — 64 X 256, 4 X 512, ETC
9	BLANK
10-11	PUNCH "MOS" FOR AN MOS OUTPUT PUNCH "TTL" FOR A TTL OUTPUT (BARE DRAIN)
12-21	BLANK
22-23	PUNCH THE BASIC DEVICE TYPE DESIRED — (N2602, N2620, ETC.)
24-80	COMMENTS PUNCHED HERE WILL APPEAR ON THE LIST ON THE TRUTH TABLE THIS SHOULD INCLUDE CUSTOMER PART IDENTIFICATION

CE_1, $\overline{CE}_2$ and $\overline{CE}_3$ respectively

CARD 2 THROUGH 129 (8 X 128 Organization)
2 THROUGH 257 (8 X 256 Organization)

EACH CARD SPECIFIES THE OUTPUT OF ONE 8-BIT WORD IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS FOR THAT WORD IS PUNCHED IN COLUMNS 78, 79, AND 80.

COLUMNS	DATA
1-8	PUNCH OUTPUTS B1 THROUGH B8 IN COLUMNS ONE THROUGH EIGHT RESPECTIVELY
9-71	LEAVE BLANK
72-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS WHICH CORRESPONDS TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 128 (4 X 256 Organization only)

EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHED IN COLUMNS 78, 79, AND 80.

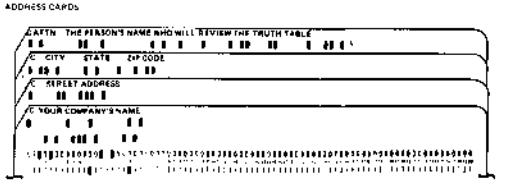
COLUMN	DATA
1-4	PUNCH OUTPUT FOR WORDS 0-255
5-8	PUNCH OUTPUT FOR WORD 256-511
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS OF THE WORD FOR RESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 28714 X 512 Organization only)

EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHES IN COLUMNS 78, 79, AND 80.

COLUMN	DATA
1-4	PUNCH OUTPUT FOR WORDS 0-127
5-8	PUNCH OUTPUT FOR WORDS 128-255
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

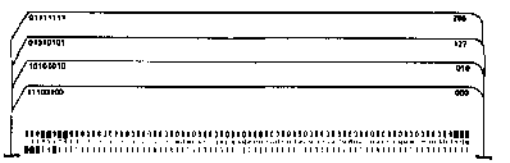
EXAMPLE:
ADDRESS CARDS



EXAMPLE
CARD 1

THE ABOVE SPECIFIES A "CODED" ROM WITH THE BINARY CODE CHIP SELECT "101" ORGANIZED 8 X 256 WITH TTL OUTPUTS (BARE DRAIN). THE BASIC DEVICE TYPE IS A N2436Y ("Y" INDICATES A 24 P-W CERAMIC DIP. "N" INDICATES TEMPERATURE RANGE 25°C +70°C)

EXAMPLE
CARDS 2-129 AND CARDS 2-257



- OUTPUTS B1 THROUGH B8 ARE IN COLUMNS 1 THROUGH 8 RESPECTIVELY
- DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS IS IN COLUMNS 78, 79, AND 80
- FOR 8 X 128 AND 8 X 256 ORGANIZATIONS – OUTPUTS ARE B1 THROUGH B8 RESPECTIVELY.
- FOR 4 X 512 ORGANIZATION:

DATA CARD 2	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 256 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 266 OUTPUTS B5 THROUGH B8 RESPECTIVELY

ETC.

- FOR 4 X 256 ORGANIZATION:

DATA CARD 2	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 128 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 138 OUTPUTS B5 THROUGH B8 RESPECTIVELY

signetics

FULLY DECODED 1024 AND 2048 STATIC READ-ONLY MEMORIES

METAL GATE MOS

2441
2451
2461
2462

DESCRIPTION

These Signetics devices are high speed, fully decoded, MOS static 1024 and 2048-bit read-only memories offering 128X8, 126X4, and 512X4 organizations.

Both single line and 3-bit binary coded chip select options, provide for wide versatility and economy of application. The devices interface directly with standard TTL/DTL logic circuits. Process technology is P-Channel enhancement mode.

FEATURES

- 128X8, 256X8, 256X4, 512X4 ORGANIZATIONS
- STATIC OPERATION – NO CLOCKS
- FULLY DECODED ADDRESS
- ACCESS TIME 950ns MAX.
- TTL/DTL COMPATIBILITY
- BARE DRAIN OUTPUT
- TWO CHIP SELECT OPTIONS:
  - SINGLE LINE
  - 3-BIT BINARY CODED
- EBCDIC-ASCII CONVERSION (CM4030) TABLE IS CATALOG STANDARD, OTHER STANDARDS AVAILABLE
- +5, -12V POWER SUPPLIES
- STANDARD PINNING IN 16 AND 24 PIN CERAMIC DUAL IN-LINE PACKAGES

APPLICATIONS

CODE CONVERSION
LOOK-UP TABLES
MICRO-PROGRAMMING
RANDOM LOGIC SYNTHESIS
CHARACTER GENERATION

SPECIAL FEATURES

Chip Select Options: Both the 2451 and 2461 may be specified with either single line chip select or a 3 line, 3-bit binary coded chip select. The coded chip select allows one-of-eight chip selection without external logic components for larger memory matrices. The 2441 and 2462 are pin limited to single line chip select.

Package Options: The 256X4 organization is available in *either* a 16-pin or 24-pin dual in-line package.

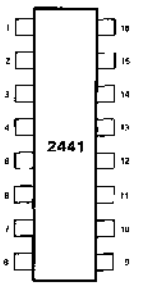
For a detailed listing of part numbers and options see the PART IDENTIFICATION TABLE.

CUSTOM ENCODING

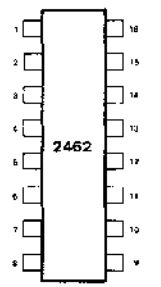
You may describe the particular option you desire in a booklet which will be provided by Signetics. Ask your local Signetics representative for a copy of "SIGNETICS 2400 SERIES STATIC READ-ONLY MEMORIES – MOS-ROM PROGRAMMING". The booklet contains a blank truth table and instructions for preparing punched data cards.

PIN CONFIGURATIONS (Top View)

I PACKAGE

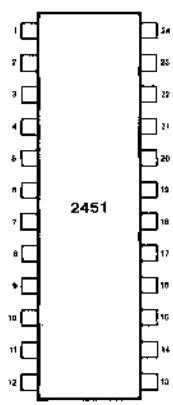


1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
16. V_{DD}
15. Address 4
14. Address 5
13. Address 6
12. Address 7
11. V_{GG}
10. Chip Enable
9. Address 8



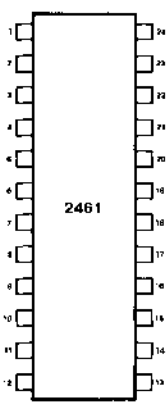
1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
16. Address 4
15. Address 5
14. Address 6
13. Address 7
12. Address 8
11. V_{GG}, V_{DD}
10. Chip Enable
9. Address 9

Y PACKAGE



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
24. V_{DD}
23. Chip Enable 3*
22. Chip Enable 2*
21. Address 4
20. Address 5
19. Address 6
18. Address 7
17. V_{GG}
16. Mode Control
15. Chip Enable
14. Address 8
13. No Connection

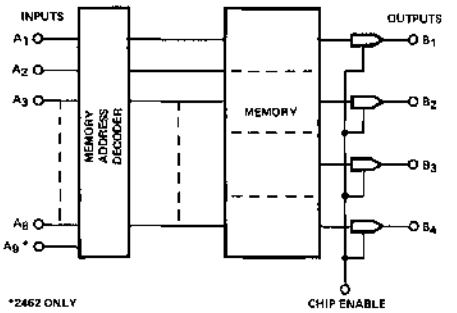
* No connection for single chip enable options.



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
24. V_{DD}
23. Chip Enable 3*
22. Chip Enable 2*
21. Address 4
20. Address 5
19. Address 6
18. Address 7
17. Address 8
16. V_{GG}
15. Mode Control
14. Chip Enable
13. Address 9

* No connection for single chip enable options.

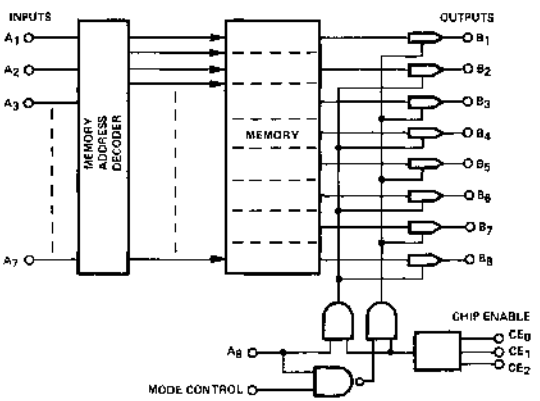
BLOCK DIAGRAMS



2441, 2462

OPERATING MODE

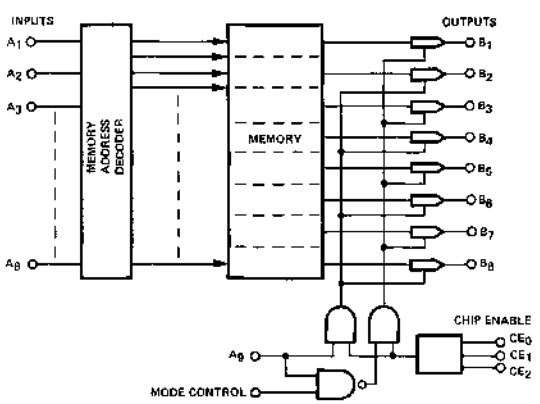
1. Logic "1" level enables outputs.



2451

OPERATING MODES

1. 128 x 8 ROM Connections
   Mode Control – Logic "0"
   A8 – Logic "1"
2. 256 x 4 ROM Connection
   Mode Control – Logic "1"
   A8 – Logic "0" Enables the odd (B1, B3, B5, B7) outputs.
   – Logic "1" Enables the even (B2, B4, B6, B8) outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.



2461

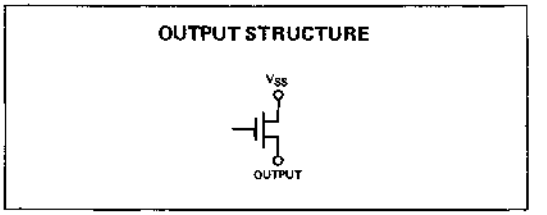
OPERATING MODES

1. 256 x 8 ROM Connection
   Mode Control – Logic "0"
   A9 – Logic "1"
2. 512 x 4 ROM Connection
   Mode Control – Logic "1"
   A9 – Logic "0" Enables the odd (B1, B3 . . B7) Outputs
   – Logic "1" Enables the even (B2, B4, . . B8) Outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.

ABSOLUTE MAXIMUM RATINGS (1)

Operating Ambient Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2) ("Y" Package)	@70°C 1.14W
("I" Package)	@70°C 0.80W
V_{GG}(3)	−20 to +0.3
V_{DD}(3)	−15 to +0.3
Input Voltage (3,4)	−20 to +0.3

SCHEMATIC DIAGRAM



DC CHARACTERISTICS

T_A = −25°C to +70°C; V_{SS} = +5V ±5%; V_{DD} = V_{GG} = −12V ±5% unless otherwise noted (Notes: 8, 9, 10, 11, 12, 14)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input Logic "0"	3			V	
V_{IH}	Input Logic "1"			0.8	V	
I_{SS}	V_{SS} Power Supply Current		14	20	mA	T_A = 25°C
I_{GG}	V_{GG} Power Supply Current			1	µA	Note 5, T_A = 25°C
I_{IH}	Input Leakage			1	µA	V_{IN} = −12V

AC CHARACTERISTICS

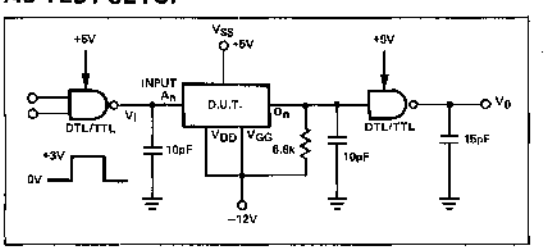
T_A = 25°C; V_{SS} = +5V ±5%; V_{DD} = V_{GG} = −12V ±5% unless otherwise noted (Notes 9, 10, 11, 12, 14)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0" MOS to TTL	+2.4			V	Note 6
V_{OH}	Output Logic "1"			+0.4	V	Note 6
t_{A1}	Access Time			750	ns	Note 13
t_{A0}	Access Time			950	ns	
C_{IN}	Input Capacitance		5		pF	Note 7, f = 1 MHz, V_{IN} = 0

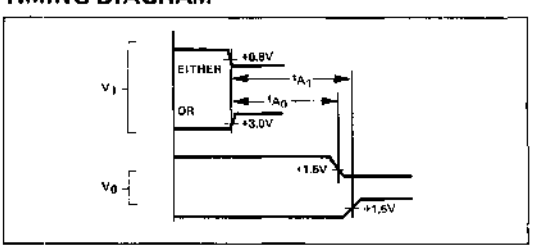
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only. Operation of the device at those or any other conditions above those indicated in the operational sections of the specification is not implied.
2. For operation at elevated temperatures, the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 70°C/W junction to ambient for the "Y" package. The "I" package is derated based on 100°C/W junction to ambient.
3. These voltages are referenced to network ground terminal (V_{SS}).
4. All inputs are protected against damage by static charge.
5. The V_{GG} supply may be clocked to reduce device power without affecting access time.
6. 6.8kΩ to V_{GG} plus 1 standard TTL gate input.
7. Capacitance measured on lot sample basis only.
8. Parameter valid over operating temperature range unless otherwise specified.
9. All voltage measurements referenced to ground.
10. Manufacturer reserves the right to make design changes and process improvements.
11. Typical values are at 25°C and nominal supply voltages.
12. Negative logic definition is employed for this device. I.e., more negative level is logic "1", most positive level is logic "0".
13. For bare drain devices, T_{A1} is primarily a function of the time constant of the load capacitance and external load resistor ($t_{A1} \cong 4R_L C_L$ +50 ns).
14. CAUTION: These devices will be permanently damaged if reversed in board or socket.

AC TEST SETUP



TIMING DIAGRAM



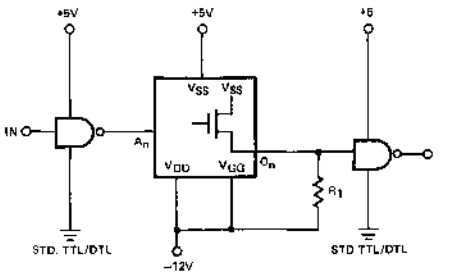
PART IDENTIFICATION TABLE

PART	ORGANIZATION	PACKAGE	OUTPUTS
N2441I	256 x 4	16-pin Cer. DIP	Bare Drain
N2451Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain
N2461Y/CM4030	256 x 8 (EBCDIC-ASCII)*	24-pin Cer. DIP	Bare Drain
N2461Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain
N2462I	512 x 4	16-pin Cer. DIP	Bare Drain

* Demonstrator

APPLICATIONS

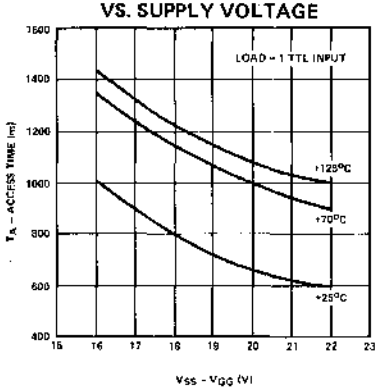
MOS-TTL INTERFACING



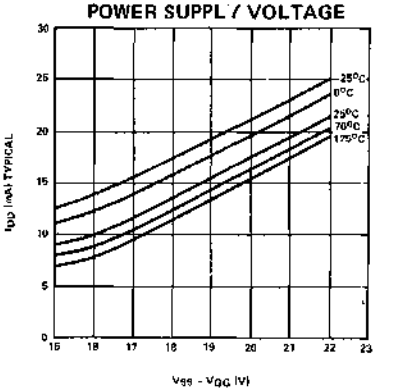
R_1 = 6.8k for a standard TTL (I_O IN = 1.6mA)

CHARACTERISTIC CURVES

TYPICAL ACCESS TIME VS. SUPPLY VOLTAGE



TYPICAL POWER SUPPLY CURRENT VS. POWER SUPPL / VOLTAGE



NOTE: For typical curves, V_{SS} = 0V.

NOTE: Blanks are logic 1's.

CM 4030 TRUTH TABLE

EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EDCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	65								130	0	1	0	0	0	1	1	195	1	1	0	0	0	0	1
1	1	0	0	0	0	0	0	66								131	1	1	0	0	0	1	1	196	0	0	1	0	0	0	1
2	0	1	0	0	0	0	0	67								132	0	0	1	0	0	1	1	197	1	0	1	0	0	0	1
3	1	1	0	0	0	0	0	68								133	1	0	1	0	0	1	1	198	0	1	1	0	0	0	1
4								69								134	0	1	1	0	0	1	1	199	1	1	1	0	0	0	1
5	0	1	1	0	0	0	0	70								135	1	1	1	0	0	1	1	200	0	0	0	1	0	0	1
6								71								136	0	0	0	1	0	1	1	201	1	0	0	1	0	0	1
7	1	1	1	1	1	1	1	72								137	1	0	0	1	0	1	1	202							
8								73								138								203							
9								74								139								204							
10								75	0	1	1	1	0	1	0	140								205							
11	1	1	0	1	0	0	0	76	0	0	1	1	1	1	0	141								206							
12	0	0	1	1	0	0	0	77	0	0	0	1	0	1	0	142								207							
13	1	0	1	1	0	0	0	78	1	1	0	1	0	1	0	143								208							
14	0	1	1	1	0	0	0	79	0	0	1	1	1	1	1	144								209	0	1	0	1	0	0	1
15	1	1	1	1	0	0	0	80	0	1	1	0	0	1	0	145	0	1	0	1	0	1	1	210	1	1	0	1	0	0	1
16	0	0	0	0	1	0	0	81								146	1	1	0	1	0	1	1	211	1	1	1	1	1	1	1
17	1	0	0	0	1	0	0	82								147	0	0	1	1	0	1	1	212	1	0	1	1	0	0	1
18	0	1	0	0	1	0	0	83								148	1	0	1	1	0	1	1	213	0	1	1	1	0	0	1
19	1	1	0	0	1	0	0	84								149	0	1	1	1	0	1	1	214	1	1	1	1	0	0	1
20								85								150	1	1	1	1	0	1	1	215	0	0	0	0	1	0	1
21								86								151	0	0	0	0	1	1	1	216	1	0	0	0	1	0	1
22	0	0	0	1	0	0	0	87								152	1	0	0	0	1	1	1	217	0	1	0	0	1	0	1
23								88								153	0	1	0	0	1	1	1	218							
24	0	0	0	1	1	0	0	89								154								219							
25	1	0	0	1	1	0	0	90	1	0	0	0	0	1	0	155								220							
26								91	0	0	1	0	0	1	0	156								221							
27								92	0	1	0	1	0	1	0	157								222							
28	0	0	1	1	1	0	0	93	1	0	0	1	0	1	0	158								223							
29	1	0	1	1	1	0	0	94	1	1	0	1	1	1	0	159								224							
30	0	1	1	1	1	0	0	95								160								225							
31	1	1	1	1	1	0	0	96	1	0	1	1	0	1	0	161								226	1	1	0	0	1	0	1
32								97	1	1	1	1	0	1	0	162	1	1	0	0	1	1	1	227	0	0	1	0	1	0	1
33								98								163	0	0	1	0	1	1	1	228	1	0	1	0	1	0	1
34								99								164	1	0	1	0	1	1	1	229	0	1	1	0	1	0	1
35								100								165	0	1	1	0	1	1	1	230	1	1	1	0	1	0	1
36								101								166	1	1	1	0	1	1	1	231	0	0	0	1	1	0	1
37	0	1	0	1	0	0	0	102								167	0	0	0	1	1	1	1	232	1	0	0	1	1	0	1
38	1	1	1	0	1	0	0	103								168	1	0	0	1	1	1	1	233	0	1	0	1	1	0	1
39	1	1	0	1	1	0	0	104								169	0	1	0	1	1	1	1	234							
40								105								170								235							
41								106								171								236							
42								107	0	0	1	1	0	1	0	172								237							
43								108	1	0	1	0	0	1	0	173								238							
44								109	1	1	1	1	1	0	1	174								239							
45	1	0	1	0	0	0	0	110	0	1	1	1	1	1	0	175								240	0	0	0	0	1	1	0
46	0	1	1	0	0	0	0	111	1	1	1	1	1	1	0	176								241	1	0	0	0	1	1	0
47	1	1	1	0	0	0	0	112								177								242	0	1	0	0	1	1	0
48								113								178								243	1	1	0	0	1	1	0
49								114								179								244	0	0	1	0	1	1	0
50	0	1	1	0	1	0	0	116								180								245	1	0	1	0	1	1	0
51								116								181								246	0	1	1	0	1	1	0
52								117								182								247	1	1	1	0	1	1	0
53								118								183								248	0	0	0	1	1	1	0
54								119								184								249	1	0	0	1	1	1	0
55	0	0	1	0	0	0	0	120								185								250							
56								121								186								251							
57								122	0	1	0	1	1	1	0	187								252							
58								123	1	1	0	0	0	1	0	188								253							
59								124	0	0	0	0	0	0	1	189								254							
60	0	0	1	0	1	0	0	125	1	1	1	0	0	1	0	190								255							
61	1	0	1	0	1	0	0	126	1	0	1	1	1	1	0	191															
62								127	0	1	0	0	0	1	0	192															
63	0	1	0	1	1	0	0	128	0	1	0	0	0	1	0	193	1	0	0	0	0	0	1								
64	0	0	0	0	0	1	0	129	1	0	0	0	0	1	1	194	0	1	0	0	0	0	1								

EXERPT FROM SOFTWARE PACKAGE (CARD FORMAT)

CARD 1

COLUMN	DATA
1-8	STARTING AT COLUMN 1 PUNCH CODED OR SINGLE
9 (11)	IF CODED PUNCH THE BINARY CODE CHIP SELECT (i.e. 101 IF SINGLE LEAVE BLANK
10	LEAVE BLANK
11-12	PUNCH THE ROM ORGANIZATION DESIRED (i.e. 8 X 256 OR 8 X 512 ETC)
13	BLANK
14-21	PUNCH MOS FOR AN MOS OUTPUT PUNCH TTL FOR A TTL OUTPUT (BARE DRAIN)
22-23	PUNCH THE BASIC DEVICE TYPE DESIRED (i.e. 24 FOR 2432 ETC.)
24-80	COMMENTS PUNCHED HERE WILL APPEAR AS THE TITLE ON THE TRUTH TABLE (THIS SHOULD INCLUDE CUSTOMER PART IDENTIFICATION

(END OF SINGLE CARD INSTRUCTIONS)

CARD 2 THROUGH 129 (8 X 128 Organization) 2 THROUGH 256 (8 X 256 Organization)

EACH CARD SPECIFIES THE OUTPUT OF ONE 8 BIT WORD IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS FOR THAT WORD IS PUNCHED IN COLUMNS 78, 79 AND 80

COLUMNS	DATA
1-8	PUNCH OUTPUTS B1 THROUGH B8 IN COLUMNS ONE THROUGH EIGHT RESPECTIVELY
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 129 (4 X 256 Organization only)

EACH CARD SPECIFIES THE OUTPUT OF TWO 4 BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS FOR THE FIRST WORD IS PUNCHED IN COLUMNS 78, 79, AND 80

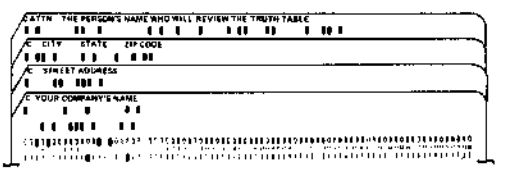
COLUMN	DATA
1-4	PUNCH OUTPUT FOR WORDS 0-127
5-8	PUNCH OUTPUT FOR WORDS 128-255
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-4 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 256 X 512 Organization only

EACH CARD SPECIFIES THE OUTPUT OF TWO 4 BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHED IN COLUMNS 78, 79, AND 80

COLUMN	DATA
1-4	PUNCH OUTPUT FOR WORDS 0-127
5-8	PUNCH OUTPUT FOR WORDS 128-255
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

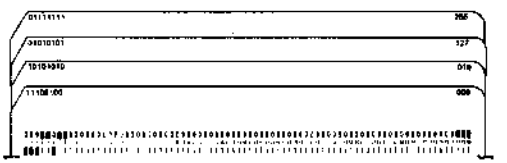
EXAMPLE
ADDRESS CARDS



EXAMPLE
CARD 1

THE ABOVE SPECIFIES A "CODED" ROM WITH THE BINARY CODED CHIP SELECT "101" ORGANIZED 8 X 256 WITH TTL OUTPUTS (BARE DRAIN). THE BASIC DEVICE TYPE IS A N24S8V ("V" INDICATES A 24 PIN CERAMIC DIP. "N" INDICATES TEMPERATURE RANGE -25°C +70°C.)

EXAMPLE
CARDS 2 129 AND CARDS 2 257



- OUTPUTS B1 THROUGH B8 ARE IN COLUMNS 1 THROUGH 8 RESPECTIVELY
- DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS IS IN COLUMNS 78, 79, AND 80
- FOR 8 X 128 AND 8 X 256 ORGANIZATIONS – OUTPUTS ARE B1 THROUGH B8 RESPECTIVELY
- FOR A 4 X 512 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 256 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 266 OUTPUTS B5 THROUGH B8 RESPECTIVELY
ETC	

- FOR 4 X 256 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 128 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 138 OUTPUTS B5 THROUGH B8 RESPECTIVELY

signetics

FULLY DECODED, 256 X 1 STATIC RANDOM ACCESS MEMORY

2501

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2500 Series 256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking.

FEATURES

- FULLY DECODED ADDRESS
- ACCESS TIME – 1.0μs GUARANTEED
- POWER DISSIPATION -1.6mW/BIT MAXIMUM DURING ACCESS
- STANDBY POWER DISSIPATION – 50 μW/BIT
- DTL AND TTL COMPATIBLE
- CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY FOR EASY EXPANSION
- STANDARD 16-PIN DIP SILICONE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY
- V_{CC} = +5V, V_{DD} = V_D = -9V

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

BIPOLAR COMPATIBILITY

All inputs of the 2501 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 2.0 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.6mW/bit is required only during Read or Write. For standby operation, 50μW/bit is obtained by removing V_D and reducing V_{DD} to −2.0V. Removal of V_D alone will cut power dissipation by a factor of 1.5.

SPECIAL FEATURE

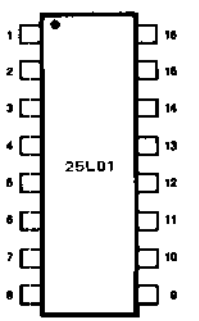
The outputs of the 2501 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-Tying for memory expansion.

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
2501B	16-pin Silicone DIP	0°C. to +70°C.
2501I	16-pin Ceramic DIP	0°C. to +70 C.

PIN CONFIGURATION (Top View)

B/I PACKAGE



1. Address 6
2. Address 8
3. Address 7
4. V_D
5. V_{CC}
6. Address 5
7. Address 1
8. V_{DD}
16. $\overline{\text{Chip Select}}$
15. R/W
14. $\overline{\text{Data Out}}$
13. Data Out
12. Data In
11. Address 4
10. Address 2
9. Address 3

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to -20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	-18V
Power Dissipation at T_A = 70°C	640mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

NOTE: Special devices are available for operation at V_{DD} = -7V, V_D = -10V. Contact your Signetics Representative for details.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V (8), V_{DD} = V_D = -9V ±5%, unless otherwise specified. See notes below)

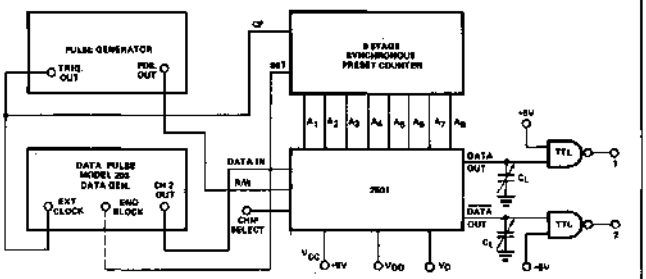
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		13.0	18	mA	T_A = +25°C, V_{DD} = V_D = -9V
I_D	Power Supply Current, V_D		8.5	12	mA	I_{OL} = 0.0mA T_A = +25°C V_{DD} = V_D = -9V
V_{IL}	Input "Low" Voltage	−12		V_{CC}−4.5	V	
V_{IH}	Input "High" Voltage	V_{CC}−2.0		V_{CC}+0.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = −0.7 V
I_{OH1}	Output Source Current	−3.0	4		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	−2.0	3		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		−0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = −100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS

Guaranteed Limits $T_A = 0°$ C to +70°C, V_{CC} = +5V (8) , V_{DD}= V_D = -9V ± 5% except as noted.

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1.0μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

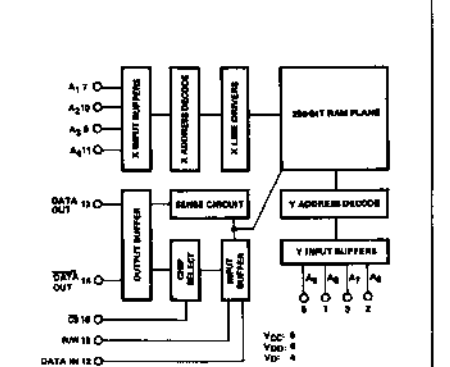
TEST SETUP FOR SPEED MEASUREMENT



NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. "PCM" mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.
3. All inputs to the 2501 are standard TTL outputs with V_{CC} = +5V ±5%.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.

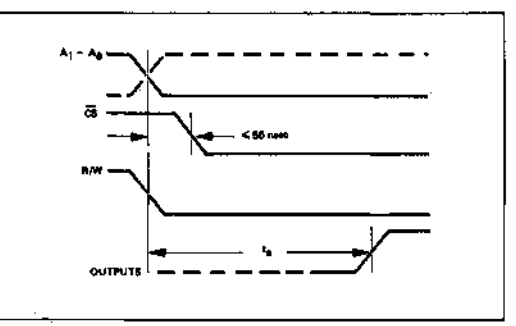
BLOCK DIAGRAM



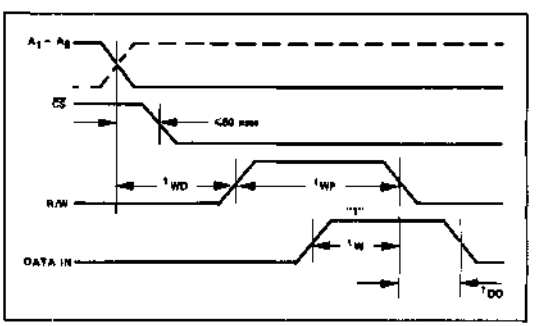
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate (t_{pd} ≤ 10 nsec)

READ CYCLE (For Measurement Purpose Only)

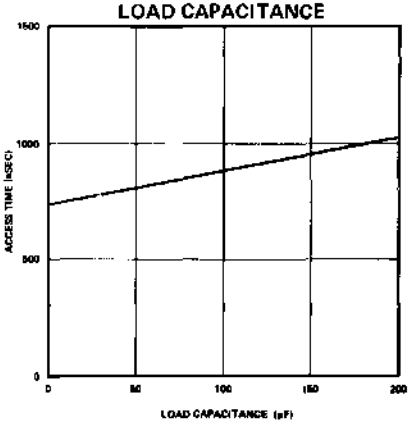


WRITE CYCLE (For Measurement Purpose Only)

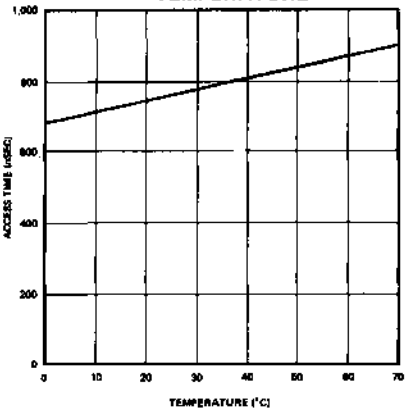


TYPICAL CHARACTERISTICS (1)

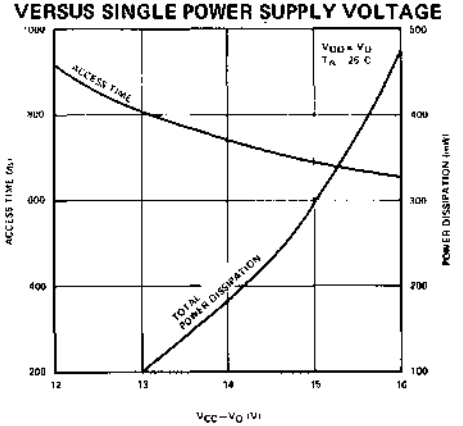
ACCESS TIME VERSUS LOAD CAPACITANCE



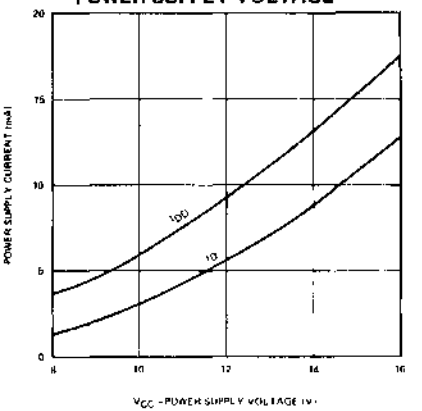
ACCESS TIME VERSUS TEMPERATURE



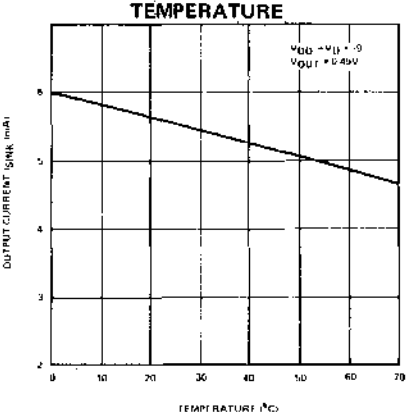
TYPICAL ACCESS TIME AND POWER DISSIPATION VERSUS SINGLE POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



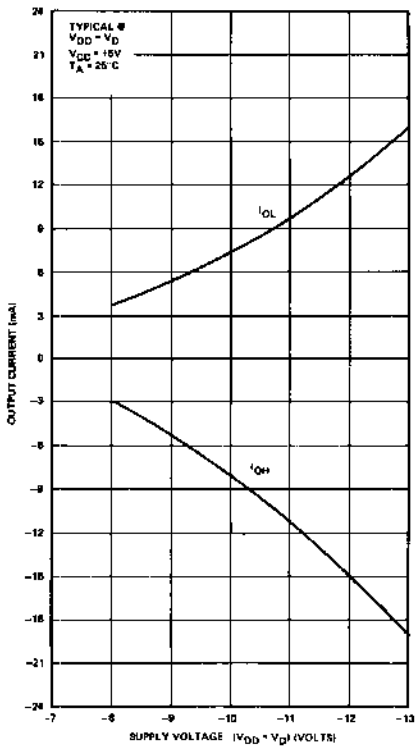
OUTPUT CURRENT VERSUS TEMPERATURE



(1) NOTE: For all typical curves, V_{CC} = 5V, V_{DD} = V_D = -9V, T_A = 25°C (unless otherwise noted).

TYPICAL CHARACTERISTICS (Cont'd)

OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



APPLICATION INFORMATION

OPERATION

The 2501 is a 256 x 1 Random Access Memory element. It is fully decoded and provides control for Read/Write and Chip Select modes. The operation of this element is described below.

ADDRESSING

An 8-bit address code will select any one of 256 bits for either Read or Write operation. All address input logic levels are compatible with standard bipolar TTL or DTL logic levels.

READ

A logic "0" level (∿0V) applied to the R/W control will result in a Read operation. This can be presented to the R/W control simultaneously or before application of an address code. In this mode the information from the memory will be available on the outputs less than 1μsec later than the application of an address code. Note that there is no need to rewrite the data into the memory after a read operation since the read is non-destructive.

WRITE

A "Write" command is a logic "1" (≥+3.3V) level to the R/W control. This should be presented to the chip no sooner than 300 nsec after the application of an address code. This time delay is necessary for proper address decoding. This "Write" command has to be present for at least 400 nsec to insure that the information is written into the memory. The "Write" command should be off (i.e., memory should be in "Read" mode) by the time the address code is changed. The input data should be present for at least the last 300 nsec of the "Write" command.

CHIP SELECT

The memory array is inhibited with the application of a logic "1" (≥+3.3V) to the Chip Select control. This will render both R/W and Data Input leads ineffective and will stop information transfer through the output buffer. The address decoder, however, will not be inhibited. This feature allows an effective increase in memory speed. (See below) The output leads are open while the memory array is inhibited. This allows OR-Tying of many memory arrays.

RANDOM ACCESS MEMORY

Arbitrary size memories can be built by tying appropriate numbers of 2501's together. Figure 1 shows a block diagram of a memory system containing 256 N words by M bits. For example, if the memory size were 4096 words by 12 bits, N = 16 and M = 12. Thus the number of 2501's required is M x N = 192. The address inputs A_1 through A_8 are common to all the rows. Inputs C_1 through C_n provide the column select and are wired to the Chip Select inputs of the 2501's. For the example of the 4096 word memory, a 12-bit address must be specified. The first 8 bits would drive inputs A_1 through A_8 directly. The remaining 4 bits would have to be decoded externally into the 16 lines required for the 16 columns. A block diagram of the 4096 x 12 memory is shown in Figure 2. Any number of 2501's can be OR-tied together, however, access time is affected by capacitive loading (approximately 1 nsec/pF). Each 2501 output represents 7 pF (typical) of loading, but the amount of stray capacitance contributed by the printed circuit board wiring can vary greatly and must be determined for each application. Figure 3 shows two different bit line organizations where the capacitive load that must be driven by the 2501 is reduced by employing logic gates to perform the OR-ing function. The organization of Figure 3b results in the minimum load capacitance but requires more gates per bit line than other organizations.

SEQUENTIAL MEMORY

On applications such as program memory or table lookup, where memory operations are highly sequential, but non-synchronous, the memory may be organized for a faster

SEQUENTIAL MEMORY (Cont'd).

average memory cycle than in the true random access case. This involves using the fact that access may be made through the chip select input in 0.2 μsec (typically) where a typical access time if one of the address inputs (A_1-A_8) changes, is 0.8 μsec. For the case of the 4096 word memory organized in this fashion information can be read out at an average access time of 0.25 μsec since access is made through the Chip Select input 15/16 of the time.

LOW POWER OPERATION

Another feature of this memory element is its capability of operating at very low standby power levels. The only time the element has to dissipate full power (~1.6mW/bit) is when it is exercised by either "Write" or "Read" operation. In the standby mode, when the chip will only store information, but does not need to be accessed, the peripheral power supply (V_D) is completely shut off. This will immediately cut the total power drain by a factor of 1.5.

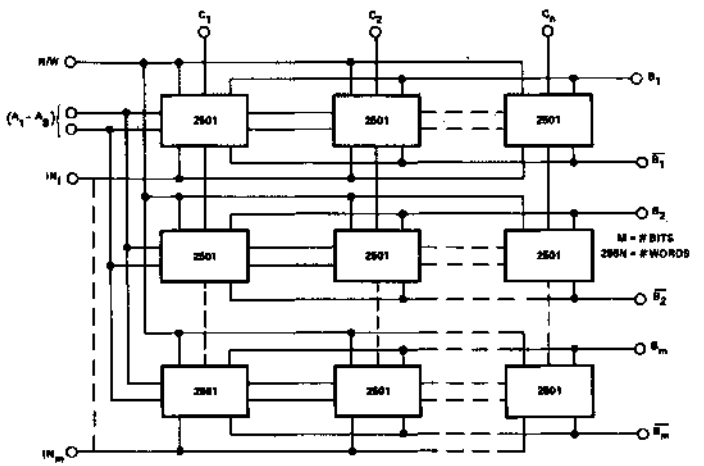


FIGURE 1. ORGANIZATION OF 2501's INTO LARGER MEMORY

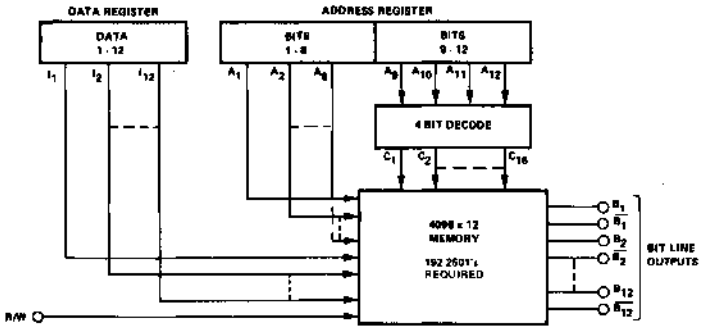
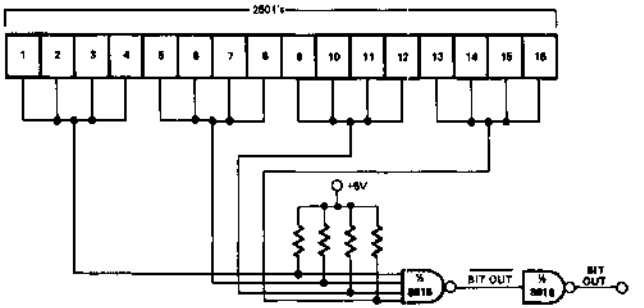
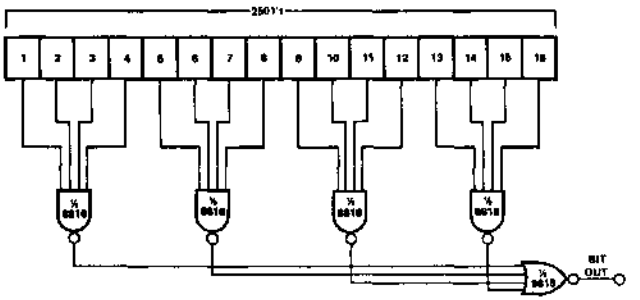


FIGURE 2. ORGANIZATION OF 4096 WORD BY 12-BIT MEMORY



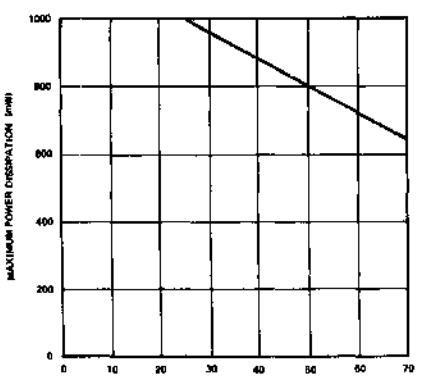
a. Combination of wire-ORing and logic-ORing of 2501's



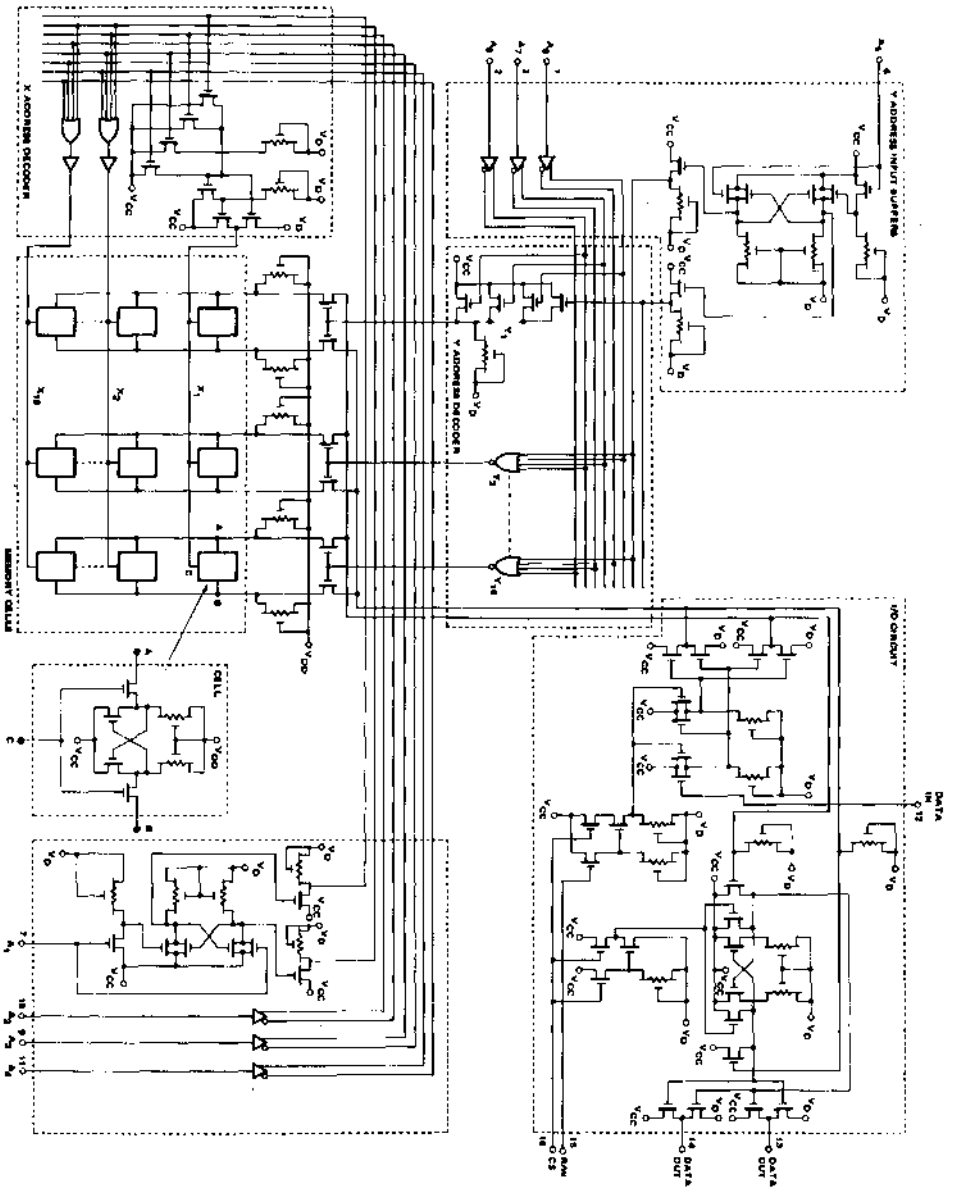
b. Logic-ORing of 2501's

FIGURE 3. BIT LINE ORGANIZATIONS TO MINIMIZE CAPACITIVE LOAD–4096 WORDS

PACKAGE MAXIMUM POWER DISSIPATION



CIRCUIT SCHEMATIC



Signetics 2501 256 X 1 Static Random Access Memory

signetics

FULLY DECODED 256×1 STATIC RANDOM ACCESS MEMORY | 25L01

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 25L01 256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking. The 25L01 is optimized with +5 and -12V supplies.

FEATURES

- FULLY DECODED ADDRESS
- ACCESS TIME – 1.0 μs GUARANTEED
- POWER DISSIPATION – 1.7 MW BIT MAXIMUM DURING ACCESS
- STANDBY POWER DISSIPATION – 100 μW/BIT
- DTL AND TTL COMPATIBLE
- CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY FOR EASY EXPANSION
- STANDARD 16-PIN DIP SILICONE OR CERAMIC PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY
- V_{CC} = +5V, V_{DD} = V_D = -12V

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

All inputs of the 25L01 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 2.0 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.7 mW/bit is required only during Read or Write. For standby operation 100 μW/bit is obtained by removing V_D and reducing V_{DD} to −8.0V. Removal of V_D alone will cut power dissipation by a factor of almost 3.

TRI-STATE OUTPUT

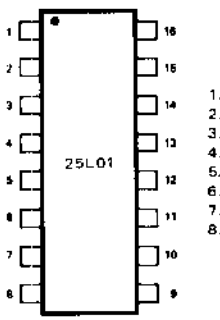
The outputs of the 25L01 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-tieing for memory expansion.

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
25L01B	16-pin Silicone DIP	0°C to +70°C
25L01I	16-pin Ceramic DIP	0°C to +70°C

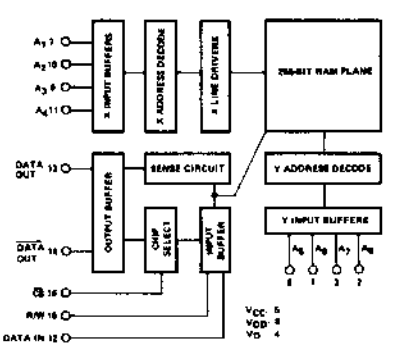
PIN CONFIGURATION (Top View)

B/I PACKAGE



1. Address 6
2. Address 8
3. Address 7
4. V_D
5. V_{CC}
6. Address 5
7. Address 1
8. V_{DD}
9. Address 3
10. Address 2
11. Address 4
12. Data In
13. Data Out
14. $\overline{\text{Data Out}}$
15. R/W
16. $\overline{\text{Chip Select}}$

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	−18V
Power Dissipation at T_A = 25°C "B" pkg.	640 mW
"I" pkg.	800 mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" pkg.) ("I" pkg., 100°C/W).
3. All inputs protected against static charge.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.

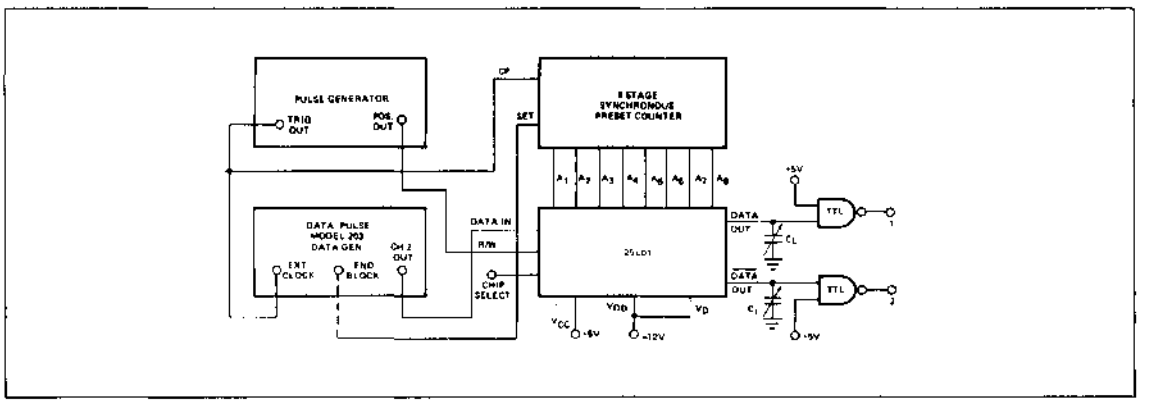
DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = V_D = −12V ± 5% unless otherwise specified. See notes above).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		5	9	mA	T_A = +25°C
I_D	Power Supply Current, V_D		11	16	mA	I_{OL} = 0.0 mA T_A = +25°C
V_{IL}	Input "Low" Voltage	−12		V_{CC}−4.5	V	
V_{IH}	Input "High" Voltage	V_{CC}−2.0		V_{CC}+0.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = −0.7 V
I_{OH1}	Output Source Current	−3.0	4		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	−2.0	3		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		−0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = −100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS Guaranteed Limits T_A = 0 to +70°C, V_{CC} = +5V ±5%, V_{DD} = V_D = -12V ±5%

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1 μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

TEST SETUP FOR SPEED MEASUREMENT



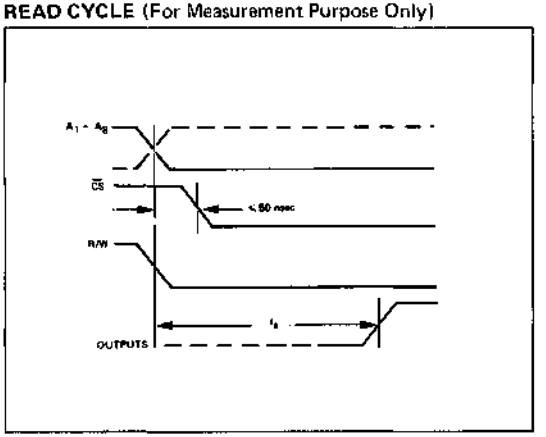
NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. "PCM" mode used so data can be changed in 32 bits of the 25L01 from one cycle to the next.
3. All inputs to the 25L01 are standard TTL outputs with V_{CC} = +5V ±5%.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.

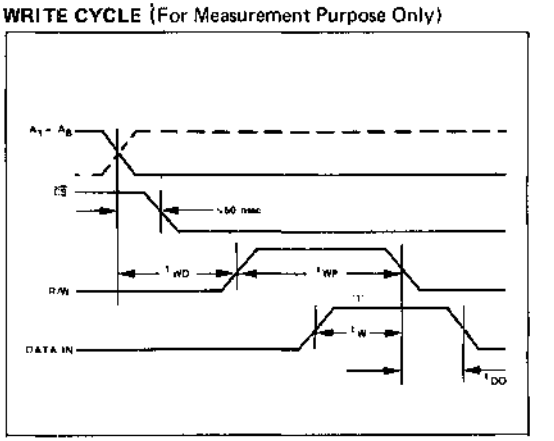
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{pd} \leq$ 10 nsec).

READ CYCLE (For Measurement Purpose Only)



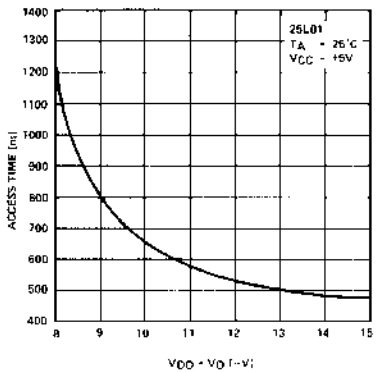
WRITE CYCLE (For Measurement Purpose Only)



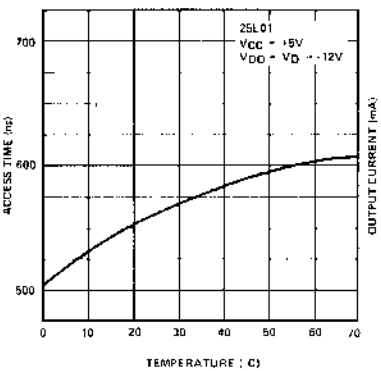
APPLICATION INFORMATION: Reference 2501 specifications.

TYPICAL CHARACTERISTIC CURVES

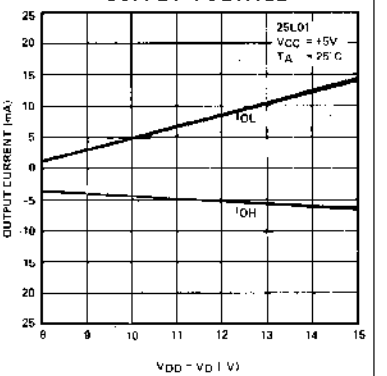
ACCESS TIME VERSUS SUPPLY VOLTAGE



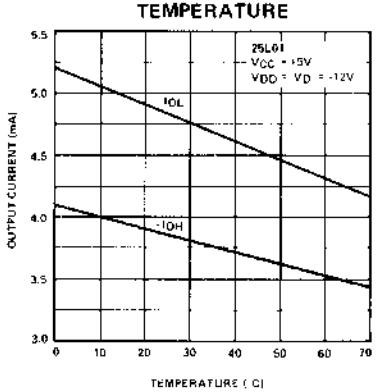
ACCESS TIME VERSUS TEMPERATURE



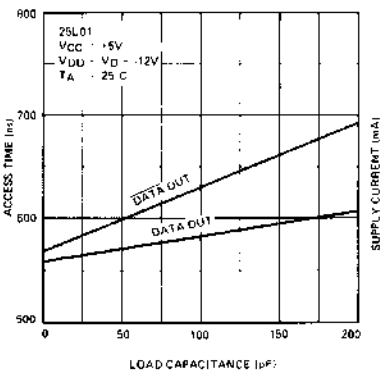
OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



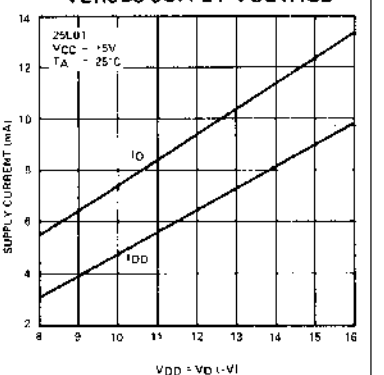
OUTPUT CURRENT VERSUS TEMPERATURE



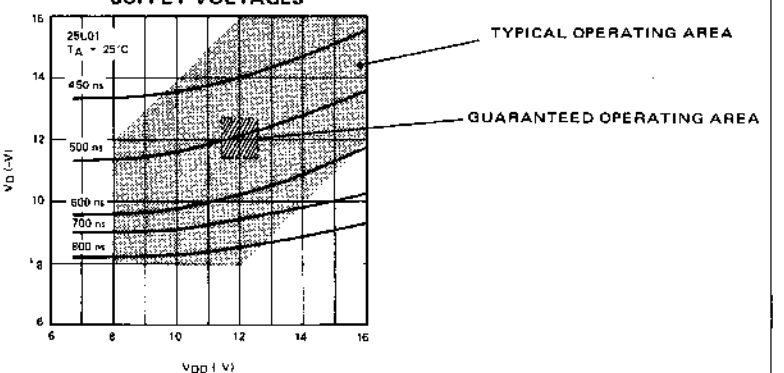
ACCESS TIME VERSUS LOAD CAPACITANCE



POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



ACCESS TIME VERSUS SUPPLY VOLTAGES



Signetics

1024-BIT CAPACITY MULTIPLEXED DYNAMIC SHIFT REGISTERS

SILICON GATE MOS 2500 SERIES

2502
2503
2504

DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

FEATURES

- 10 MHz TYPICAL DATA RATE
- THREE CONFIGURATIONS—QUAD 256, DUAL 512, SINGLE 1024
- LOW POWER DISSIPATION—40 μW/bit at 1 MHz DATA RATE
- LOW CLOCK CAPACITANCE—140 pF
- TTL, DTL COMPATIBLE
- STANDARD PACKAGES - 8 LEAD TO-99, 8-PIN AND 16-PIN DUAL IN-LINE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (10 MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.

The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

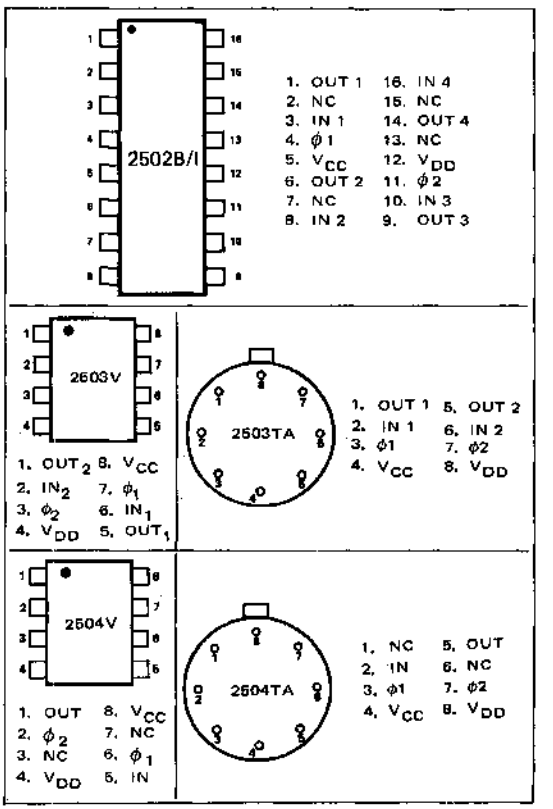
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

The data inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

PIN CONFIGURATIONS (Top View)



PART IDENTIFICATION TABLE

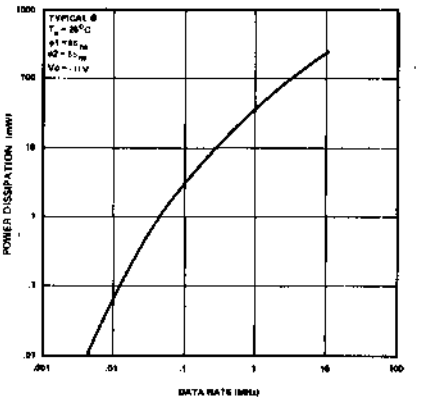
TYPE	FUNCTION	PACKAGE
2502B	Quad 256-bit	16-Pin Silicone DIP
2502I	Quad 256-bit	16-Pin Ceramic DIP
2503TA	Dual 512-bit	TO-99
2503V	Dual 512-bit	8-Pin DIP
2504TA	Single 1024-bit	TO-99
2504V	Single 1024-bit	8-Pin DIP

MAXIMUM SIGNETICS GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	-65°C to + 150°C
Power Dissipation(2) at T_A = 70°C	
TA and V Package	535mW
B Package	640mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}(3)	+0.3V to -20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (TA and V package)or 125° C/W (B package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. When cascading use 140_{ns} minimum to allow data set-up time for driver register.

POWER DISSIPATION VERSUS DATA RATE



DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5V(8) unless otherwise noted. (See Notes 4,5,6,7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = V_{CC} to V_{DD}, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1}$ = $V_{\phi2}$ = -10V V_{OUT} = 0.0V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -10V T_A = 25°C
I_{DD}	Power Supply Current		15	25	mA	Outputs at logic "0", 4 MHz data rate, $\phi1$ = $\phi2$ = 85ns continuous operation, V_{ILC} = -12V T_A = 25°C
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-10		-12	V	

AC CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$, (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0.0005		4	MHz	
Frequency	Data Rep Rate	0.001		8	MHz	
ϕ pw	Clock Pulse Width (9)	85			ns	See note 9
ϕ d	Clock Pulse Delay	10			ns	
t_r, t_f	Clock Pulse Transition	10		1000	ns	
t_w	Data Write Time (Setup)	50			ns	
t_{DO}	Data in Overlap	10			ns	
t_a+	Data Out			90	ns	
C_{IN}	Input Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
C_{OUT}	Output Capacitance	2.5		5	pF	@ 1 MHz 25 mV p-p
$C\phi$	Clock Capacitance	130		150	pF	@ 1 MHz 25 mV p-p
V_{OL}	Output "Low" Voltage		-0.3		V	R_L=3k, depends on R_L and TTL Gate
V_{OH1}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6k
V_{OH2}	Output "High" Voltage Driving TTL	3.0	3.5		V	R_L = 3k

MULTIPLEXED 4-BIT MOS SHIFT REGISTER

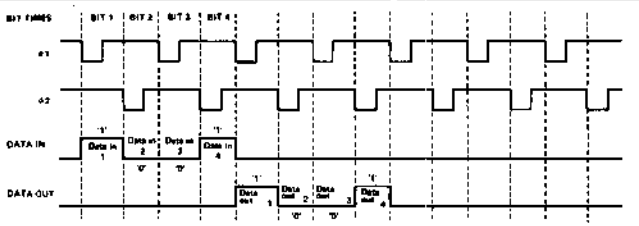


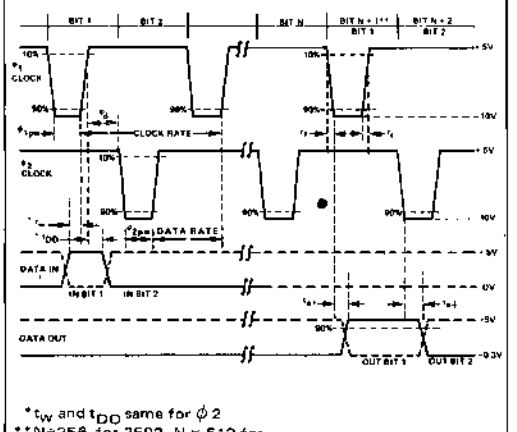
Figure 1

Figure 1 is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ1 time, it exits at ϕ1 time, (beginning on ϕ1's negative going edge and ending on the succeeding ϕ2's negative going edge).

CONDITIONS OF TEST

Input rise and fall times: 10nsec. Output load is 1 TTL gate.

TIMING DIAGRAM

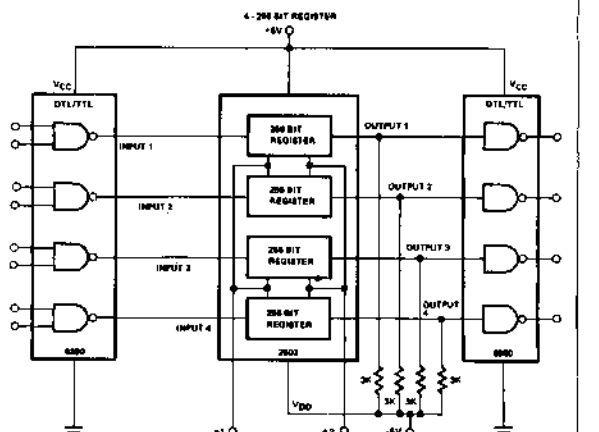


* t_W and t_{DO} same for ϕ 2

** N=256 for 2502, N = 512 for 2503, N = 1024 for 2504

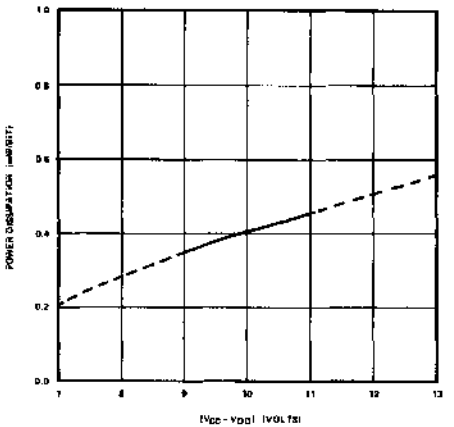
APPLICATIONS INFORMATION

DTL/TTL/MOS INTERFACES

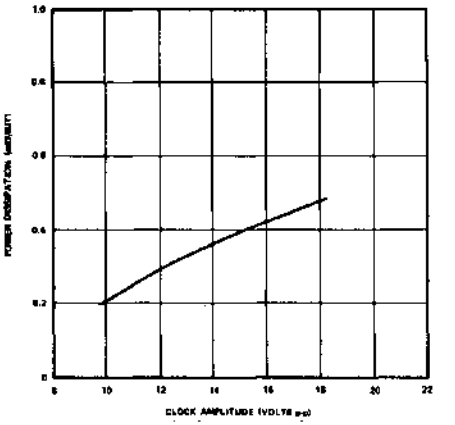


NOTE: When interfacing MOS to MOS output resistors should be 4.7K min.

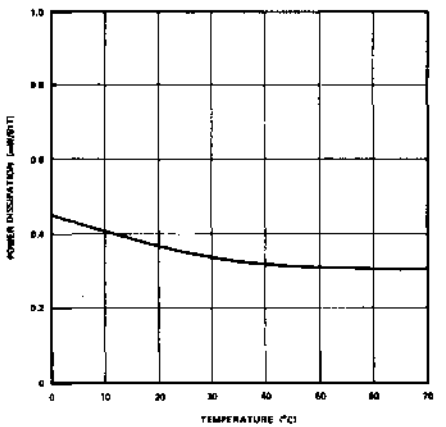
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



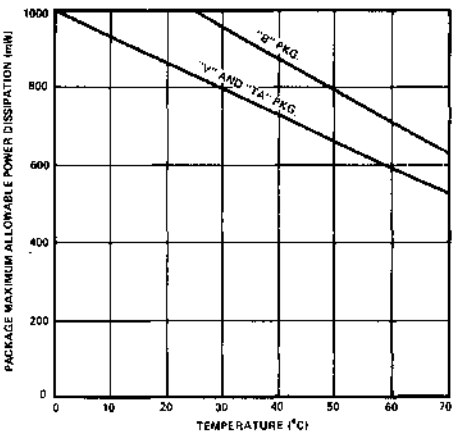
POWER DISSIPATION/BIT VERSUS CLOCK AMPLITUDE



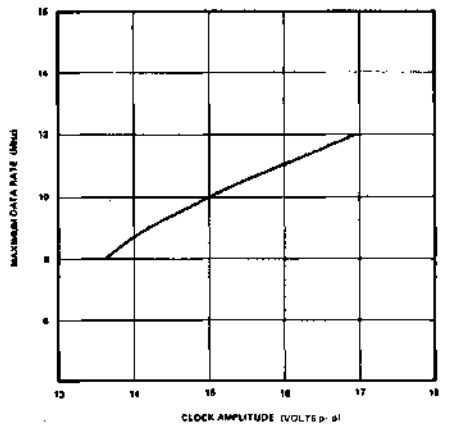
POWER DISSIPATION/BIT VERSUS TEMPERATURE



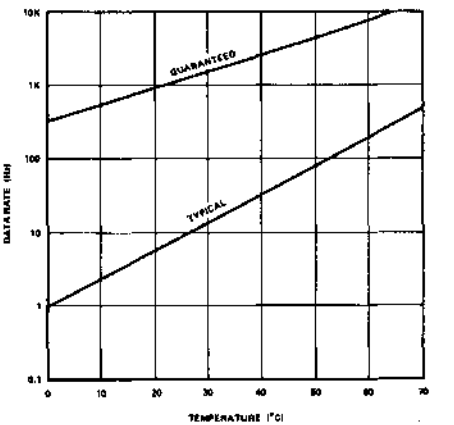
MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



CLOCK AMPLITUDE V_Φ VERSUS MAXIMUM DATA RATE



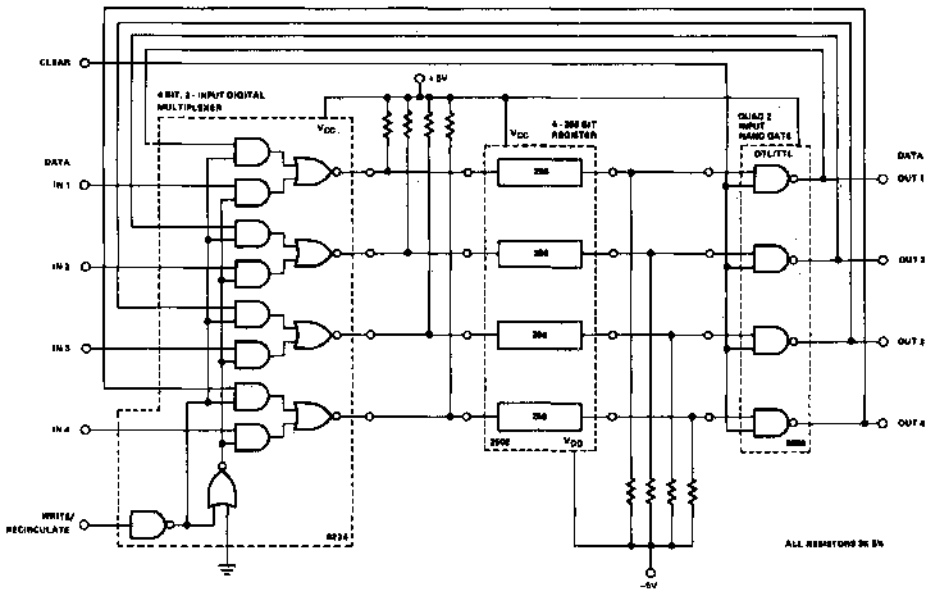
MINIMUM OPERATING DATA RATE VERSUS TEMPERATURE



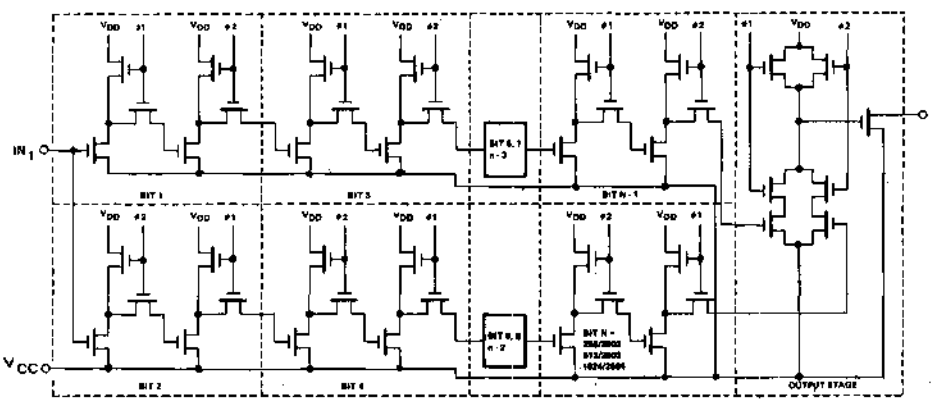
NOTE:
Conditions for Typical Curves; V_{CC} = +5V, V_{DD} = -5V, ϕ_{1PW} and ϕ_{2PW} = 85ns, V_ϕ = +11V, T_A = 25°C, f_{DATA} = 10MHz unless otherwise noted.

APPLICATIONS (Cont'd)

WRITE/RECIRCULATE LOGIC



CIRCUIT SCHEMATIC



NOTES:

1. N = 1024 on 2504
2. N = 512 on 2503 schematic for second register same as above.
3. N = 256 on 2502 schematic for second, third and fourth registers same as above.

signetics

512 AND 1024-BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2505
2512

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION–3 MHz TYPICAL CLOCK RATE
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- 2-CHIP SELECT CONTROLS FOR XY MATRIX SELECTION
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION–150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE–80pF for 512, 160pF for 1024 Bits
- +5, -5V POWER SUPPLIES
- STANDARD PACKAGE–10 LEAD TO-100
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

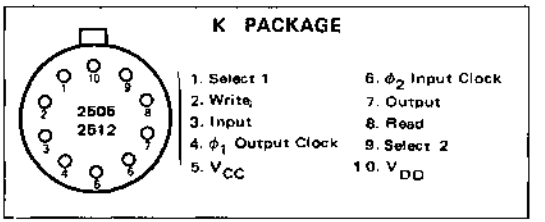
PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (3MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

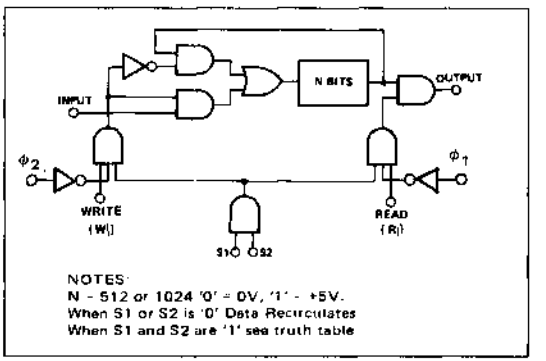
BIPOLAR COMPATIBILITY

The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



NOTES:
N = 512 or 1024 '0' = 0V, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2505K	512	10 pin TO - 100
2512K	1024	10 pin TO - 100

MAXIMUM GUARANTEED RATINGS (1)

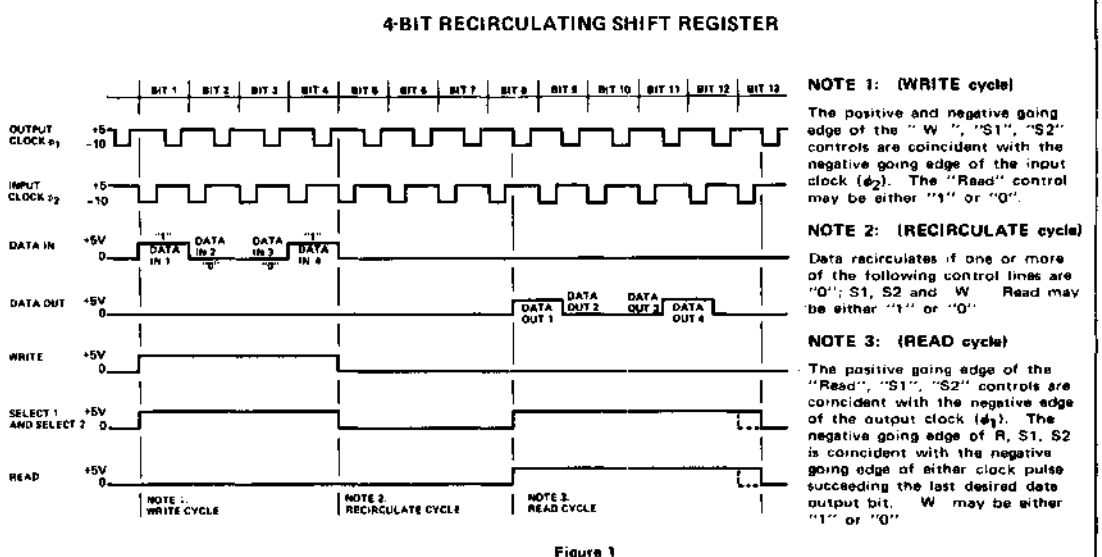
Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	–65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to –20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and nominal supply voltages.
9. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = +5V$ (9); $V_{DD} = -5V$ ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	$V_{IN} = -5.5V$; $T_A = 25°C$
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1} = V_{\phi2} = -12V$, $V_{DD} = -5V$; $V_{OUT} = -5.5V$; $T_A = 25°C$
I_{LC}	Clock Leakage Current		10	1000	nA	$V_{ILC} = -12V$; $T_A = 25°C$
I_{DD}	Power Supply Current: 2505		15	25	mA	Continuous Operation; ϕ pW = 150nS, 1MHz
	2512		25	35	mA	$V_{ILC} = -12V$; $T_A = 25°C$ $V_{DD} = -5.5V$
V_{IL}	Input "Low" Voltage	-5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM



NOTE 1: (WRITE cycle)

The positive and negative going edge of the "W", "S1", "S2" controls are coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0".

NOTE 2: (RECIRCULATE cycle)

Data recirculates if one or more of the following control lines are "0": S1, S2 and W. Read may be either "1" or "0".

NOTE 3: (READ cycle)

The positive going edge of the "Read", "S1", "S2" controls are coincident with the negative edge of the output clock (ϕ_1). The negative going edge of R, S1, S2 is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. W may be either "1" or "0".

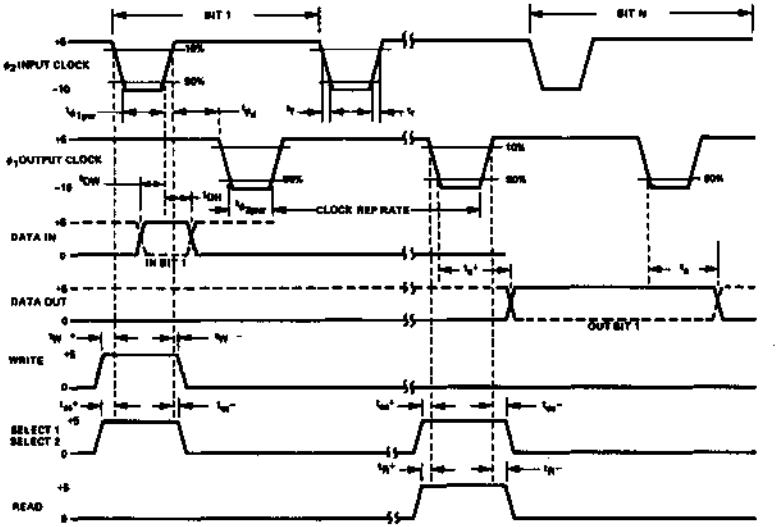
Figure 1

Figure 1 is a simplified illustration of the timing of a 4-bit recirculating shift register showing the 3 basic modes of operation.

CONDITIONS OF TEST

Input rise and fall times: 10 nsec Output load is 1 TTL gate

TIMING DIAGRAM



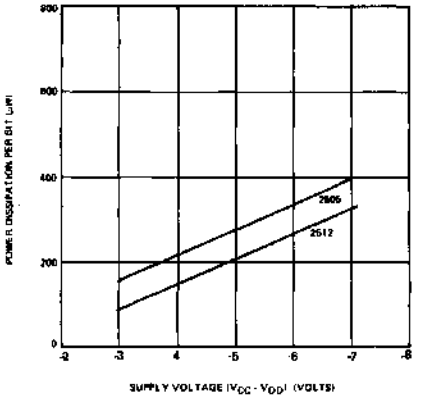
NOTE:
1. N=512 for 2505, N=1024 for 2512
2. Note that the Read input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS T_A=+25°C V_{CC}=+5V (9) ; V_{DD}=−5V ± 5%; V_{ILC}=-11V

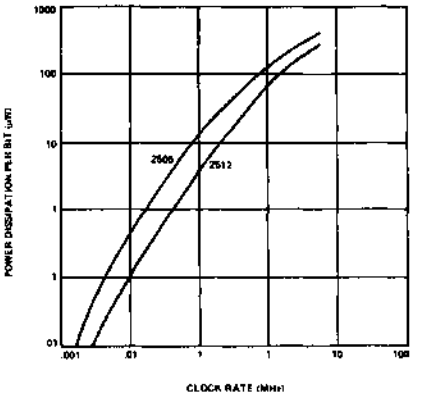
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	3	2.5	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	180			nsec	
$t_{\phi d}$	Clock Pulse Delay	10			nsec	
t_r;t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Setup) Time	150			nsec	
t_{DH}	Data to Clock Hold Time	10			nsec	
t_{a+};t_{a-}	Clock to Data Out Delay			100	nsec	
t_{R-};t_{CS-} $t_{W\ -}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
t_{R-};t_{CS+} $t_{W\ +}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
C_{in}	Input Capacitance			5	pF	1 MHz; V_I=V_{CC}; V_{AC}=25mV_{P-P}
C_{out}	Output Capacitance			5	pF	1 MHz; V_O=V_{CC}; V_{AC}= 25mV_{P-P}
C_ϕ	Clock Capacitance 2505 2512			50 100	pF pF	1 MHz; V =V_{CC};V_{AC}= 25mV p-p
V_{OL}	Output "Low" Voltage		-1.0		V	R_L = 3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L = 3.0K; 1 TTL Load (I_L = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 6.6K; C_L = 10 pF

CHARACTERISTICS CURVES

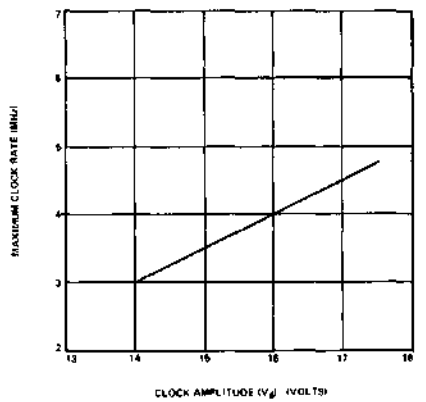
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



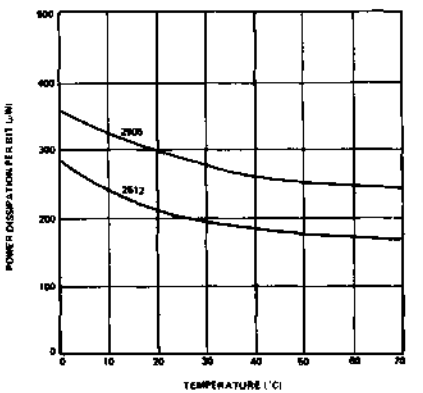
POWER DISSIPATION/BIT VERSUS CLOCK RATE



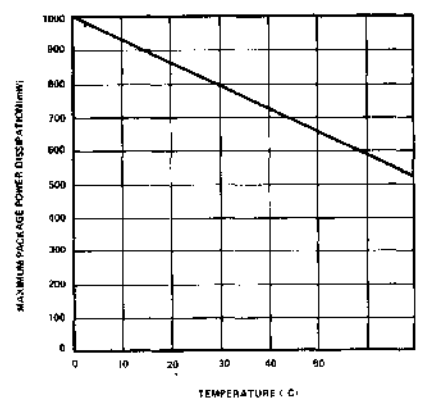
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



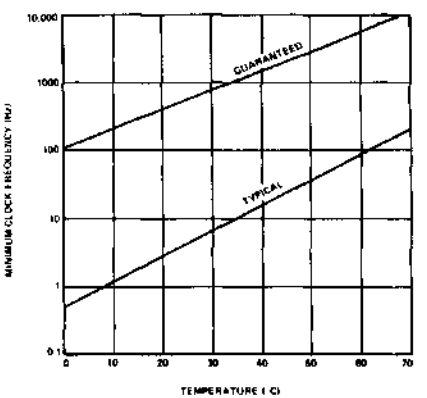
POWER DISSIPATION/BIT VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



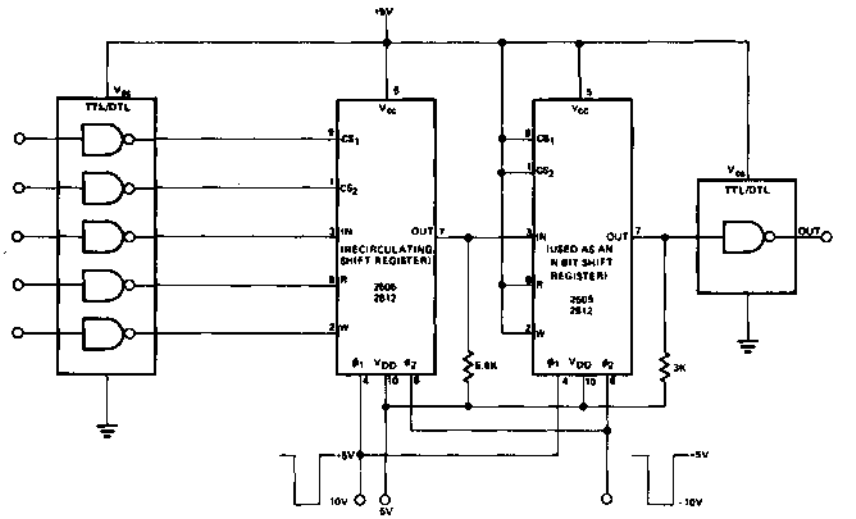
MINIMUM OPERATING CLOCK FREQUENCY



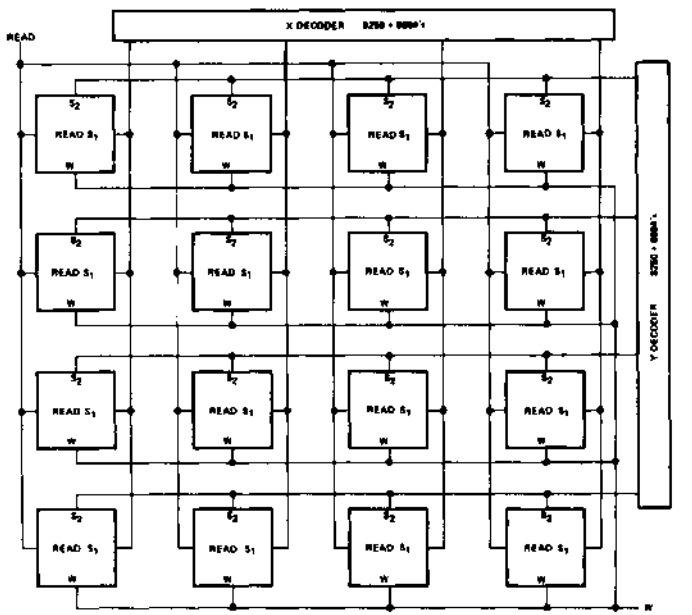
NOTE:
Conditions for Typical Curves = V_{CC}=+5V, V_{DD}=−5V, Clock Duty Cycle=35°C, f_{CLK}=2.5MHz, $V_{\phi p\text{-}p}$=16V, ϕ_{PW} =180ns, T_A=25°C unless otherwise noted

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES

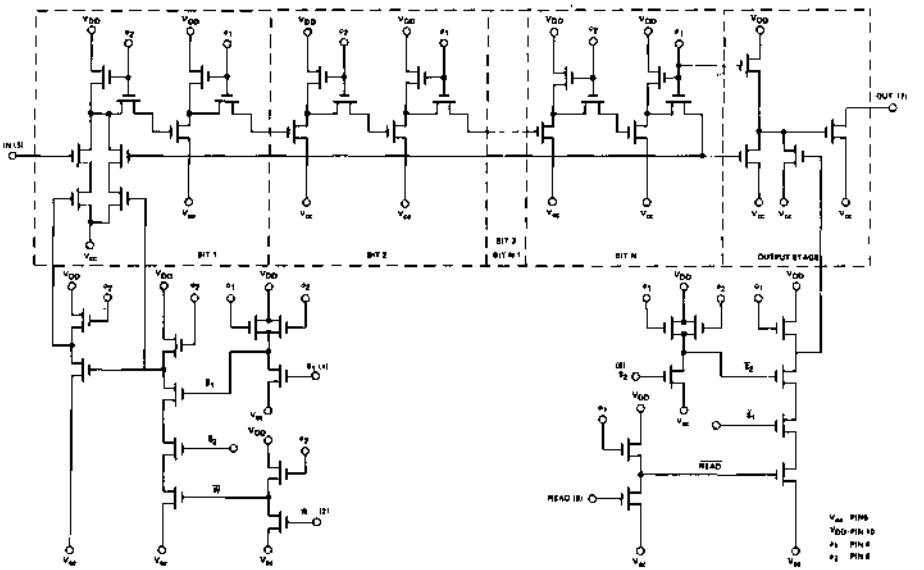


MATRIX CHIP SELECT LOGIC



NOTES:
1. Outputs common for each plane
2. All inputs common for each plane
3. All ϕ_1's common
4. All ϕ_2's common
5. All V_{CC} common
6. All V_{DD} common

CIRCUIT SCHEMATIC



NOTE: N = 512 for 2505
N = 1024 for 2512

signetics

DUAL 100-BIT DYNAMIC SHIFT REGISTER

SILICON GATE MOS 2500 SERIES

2506
2507
2517

DESCRIPTION

These Signetics 2500 Series dual 100-Bit dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. They use two clock phases.

FEATURES

- HIGH FREQUENCY OPERATION
  4 MHz TYPICAL CLOCK RATE
- TTL, DTL COMPATIBLE
- LOW POWER DISSIPATION — 400 μW/BIT AT 1 MHz
- LOW CLOCK CAPACITANCE 40pF MAXIMUM
- LOW OUTPUT IMPEDANCE — 300 OHMS TYPICAL
- BARE DRAIN AND MOS RESISTOR VERSIONS AVAILABLE
- STANDARD PACKAGES — 8 LEAD TO-5 AND 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES

PROCESS TECHNOLOGY

Use of the low threshold silicon gate technology allows high speed (3 MHz guaranteed), while reducing power dissipation by a factor of 2 and reducing clock input capacitance dramatically as compared to conventional MOS technologies.

SILICONE PACKAGING

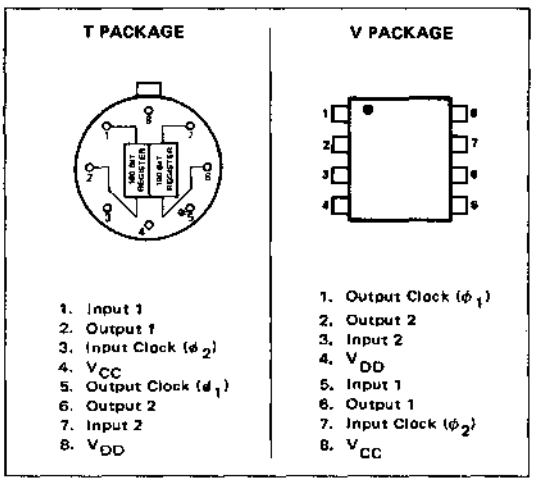
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

BIPOLAR COMPATIBILITY

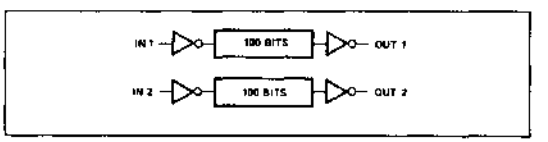
The dual 100 bit device can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for MOS or bipolar IC's.

It is available in bare drain configuration or with internal pull down resistor values of 7.5k or 20k to provide easier interfacing with other MOS circuitry.

PIN CONFIGURATIONS (TOP VIEW)



BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NO.	OUTPUT	PACKAGE
2506 T	Bare Drain	8 Pin TO-5
2506 V	Bare Drain	8 Pin DIP
2507 T	7.5k Pull Down	8 Pin TO-5
2507 V	7.5k Pull Down	8 Pin DIP
2517 T	20k Pull Down	8 Pin TO-5
2517 V	20k Pull Down	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient	0°C + 70°C
Storage Temperature	-65°C + 150°C
Power Dissipation (Note 2) @ T_A=70°C	
T Package	535mW
V Package	455mW
Clock Input Voltages with respect to V_{CC}(3)	+0.3 to -20V
Supply and Data Input Voltages with respect to V_{CC}(3)	+0.3 to -12V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175° C/W (V package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor, (R_{PD}).
10. See Figure 2 for definitions.
11. Logic Convention: Data Lines - Positive; Clocks - Negative.

DC CHARACTERISTICS

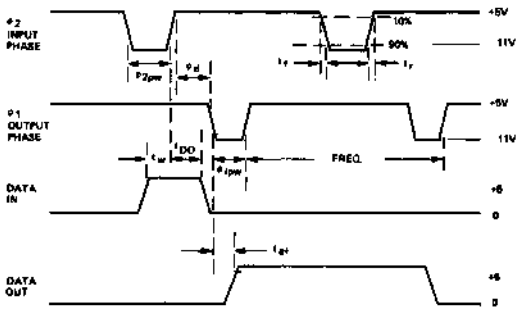
T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5 (8); unless otherwise noted(Notes: 4,5,6,7).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (Input 1)		10	500	nA	+5V ON OUT 1, ϕ1, ϕ2, V_{CC}, IN 2, OUT 2, IN 1 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LI}	Input Load Current (Input 2)		10	500	nA	+5V ON OUT 2, ϕ1, ϕ2, V_{CC}, IN 1, OUT 1, IN 2 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LO}	Output Leakage Current (OUT 1) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, V_{CC}, OUT 2, ϕ2, IN 2, V_{DD}, OUT 1 = −5.5V ϕ1 = −10V, T_A = 25°C (2506 Only)
I_{LO}	Output Leakage Current (OUT 2) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, OUT 1, V_{CC}, ϕ2, IN 2, V_{DD}, OUT 2 = −5.5V, ϕ = −10V, T_A = 25°C (2506 Only)
I_{LC}	Clock Leakage Current (ϕ1)		10	1000	nA	Vϕ1 = −12V, V_{DD} = −4.5V All other pins +5V, T_A = 25°C
I_{LC}	Clock Leakage Current (ϕ2)		10	1000	nA	Vϕ2 = −12V, V_{DD} = −4.5V All other pins +5V T_A = 25°C
V_{IL}	Input "Low" Voltage (Note 11)	−5		1.05	V	
V_{IH}	Input "High" Voltage (Note 11)	3.2		5.3	V	
C_{IN}	Input Capacitance (Inputs 1 & 2)		2.5	5	pF	V_{IN} = V_{CC}, 1 MHz, 25 mV p-p
$C_ϕ$	Clock Input Capacitance (ϕ1, ϕ2)		25	40	pF	$V_ϕ$ = V_{CC}, 1 MHz, 2.5 mV p-p
V_{IHC}	Clock Input "High" Voltage	4		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	−12		−10	V	

CONDITIONS OF TEST

Data amplitude +1.05 to +3.2 Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

TIMING DIAGRAM



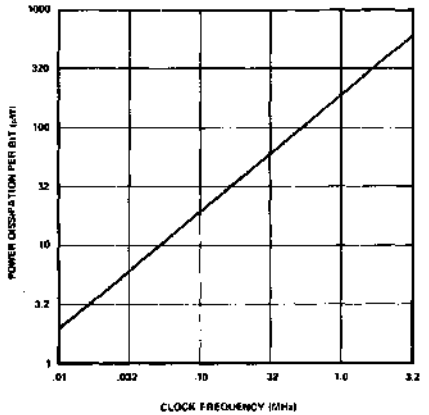
AC CHARACTERISTICS

$T_A = 25°C$; $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$

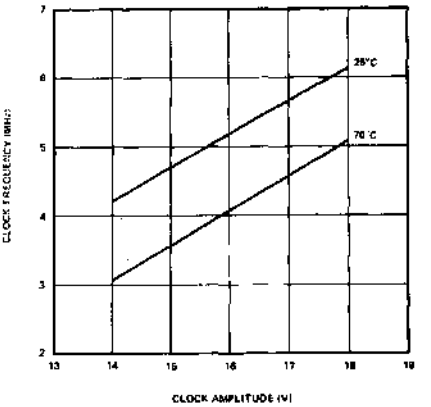
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0006	4	3	MHz	
ϕ IPW	Clock Pulse Width ϕ 1	150			nsec	@ 3MHz.
ϕ 2PW	Clock Pulse Width ϕ 2	100			nsec	@ 3MHz.
ϕ_d	Clock Pulse Delay	10			nsec	@ 3MHz
t_r, t_f	Clock Pulse Transition	10		1000	nsec	
t_W	Data Write Time (Set-Up)	75				
t_{DO}	Data In Overlap	10				$t_{r\phi 2} = t_{r\phi 1} = 10nS$
t_a+	Clock to Data Out		90	150		$V\phi = V_{CC} - 16V$, DATA OUT =+2.5V
V_{OH1}	Output "High" Voltage driving MOS (Note 11)	3.4	4.0		V	$R_{INT} = 7.5k$ nom., $C_L = 10pF$, 2507 Only, $R_{INT} = 20k$ nom. 2517 only
V_{OH2}	Output "High" Voltage driving TTL (Note 11)	3.0	3.5		V	$R_L = 3.3k$, $V_{DD} = -5V$ 2506 only
I_{DD}	Power Supply Current (V_{DD})		12	26	mA	Outputs @ logic "0" or "1", 3MHz, ϕ 1 = 150ns, ϕ 2 = 100ns

CHARACTERISTIC CURVES

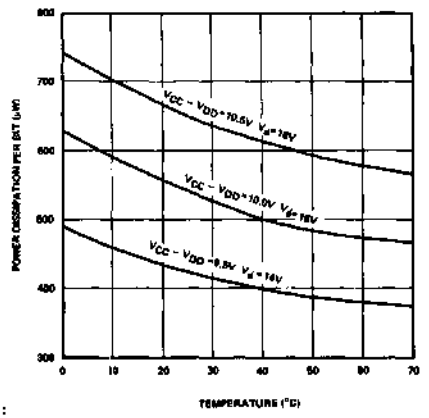
POWER DISSIPATION PER BIT VERSUS FREQUENCY



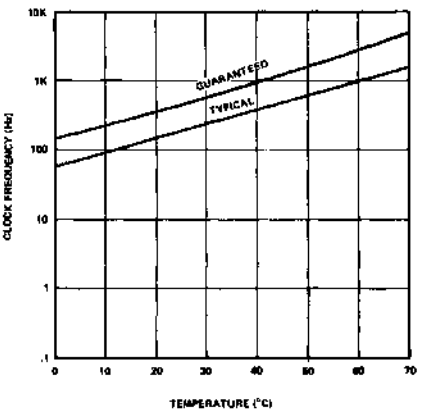
TYPICAL CLOCK FREQUENCY VERSUS CLOCK AMPLITUDE



POWER DISSIPATION BIT VERSUS TEMPERATURE



MINIMUM OPERATING CLOCK RATE

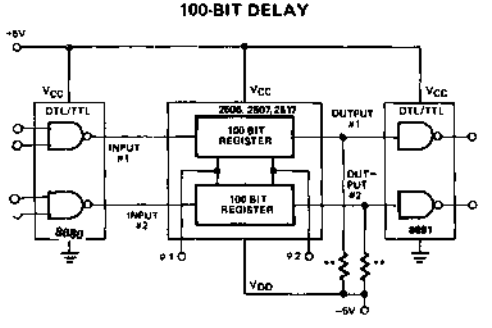


NOTE:
Conditions for Typical Curves: V_{CC}=+5V, V_{DD}=-5V, V_{ILC}=-1V, ϕ_{PW1}=150ns, ϕ_{PW2}=100ns, f=3MHz, T_A=+25°C unless otherwise noted.

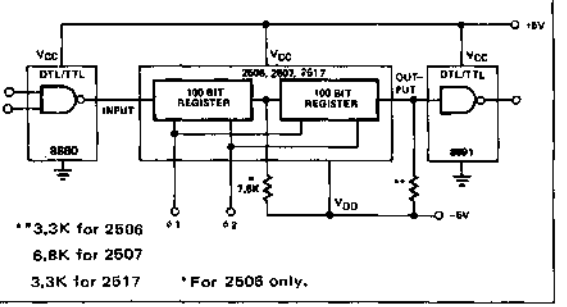
APPLICATIONS DATA

DTL/TTL/MOS INTERFACES

100-BIT DELAY



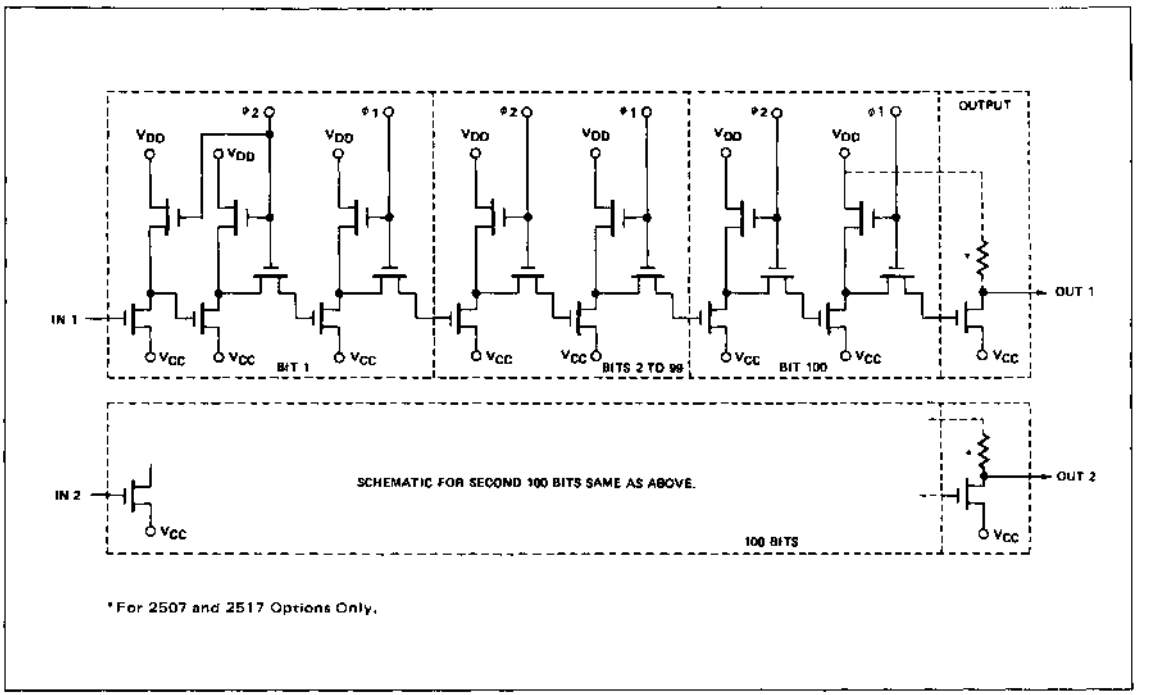
200-BIT DELAY



**3.3K for 2506
6.8K for 2507
3.3K for 2517

*For 2506 only.

CIRCUIT SCHEMATIC



*For 2507 and 2517 Options Only.

signetics

TRI-STATE OUTPUT DUAL 50-100-200 BIT STATIC SHIFT REGISTERS

SILICON GATE MOS 2000 SERIES

2509
2510
2511

DESCRIPTION

These Signetics 2500 Series Dual 50, 100, and 200 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus TRI-STATE outputs are provided for maximum interfacing capability.

FEATURES

- TRI-STATE MOS OUTPUTS - PROVIDE POWERFUL BUSSING CAPABILITY
- TTL/DTL COMPATIBLE CLOCKS - PROVIDE EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION
- 2MHz GUARANTEED CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGES - 10 LEAD TO-100, 14 PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES - LINE STORAGE

SPECIAL FEATURES

The three clock phases used by the register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

The output has three states:
"1" low impedance to +5V
"0" low impedance to -5V
"OFF" high impedance ≃ 10 M ohm
The "OFF" state is controlled by the Output Enable control input.

PROCESS TECHNOLOGY

Use of low threshold silicon gate technology allows high speed (2 MHz Guaranteed) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.

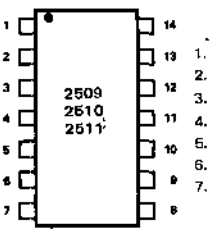
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The TRI-STATE output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

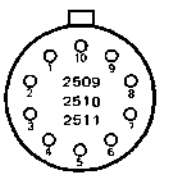
PIN CONFIGURATIONS (Top View)

A PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. NC
5. NC
6. NC
7. V_{DD}
8. ϕ_{IN}
9. Output Enable
10. V_{GG}
11. NC
12. OUT_2
13. IN_2
14. V_{CC}

K PACKAGE



1. IN_1
2. OUT_1
3. V_{DD}
4. ϕIN
5. V_{CC}
6. Output Enable
7. V_{GG}
8. OUT_2
9. IN_2
10. $\overline{\text{Recirculate}}$

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2509K	Dual 50	10 Pin, TO-100
2509A	Dual 50	14 Pin, DIP
2510K	Dual 100	10 Pin, TO-100
2510A	Dual 100	14 Pin, DIP
2511K	Dual 200	10 Pin, TO-100
2511A	Dual 200	14 Pin, DIP

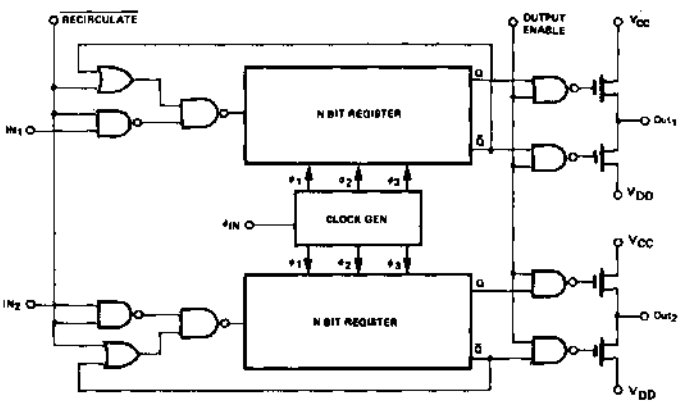
MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation (A & K) (Note 2) @ T_A = 70°C	535mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC} (3)	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off".
2: If output enable = "1", see Truth Table.

TRUTH TABLE:

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

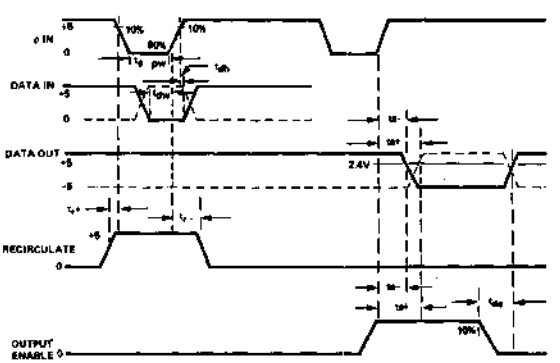
NOTE: "0" = 0V; "1" = +5V.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8), V_{DD} = -5V ±5%; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{CE} =1.05V,T_A = 25°C, V_{OUT} = -5V
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{DD}	Power Supply Current					
	(Dual 50)		6.5	15	mA	Continuous Operation
	(Dual 100)		12	30	mA	F = 2MHz, T_A = 25°C
	(Dual 200)		20	40	mA	
I_{GG}	Power Supply Current		4.5	7.5	mA	
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-5		1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

TIMING DIAGRAM

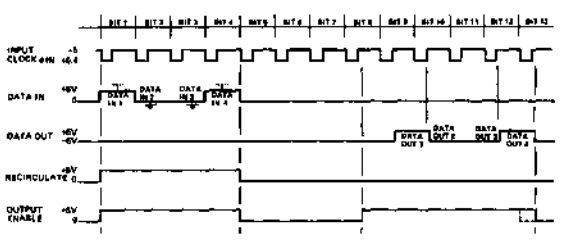


AC CHARACTERISTICS

V_{CC} = +5V (8); V_{DD} = -5V ±5%; V_{ILC} = +0.4V to 4V; V_{GG} = -12V ±5%; T_A = 0° C to +70°C

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3	1.5	MHz	
$t_{\phi PW}$	Clock Pulse Width	.290	.150	100	μsec	
$\overline{t_{\phi PW}}$	Clock Pulse Width	.210		DC	μsec	
t_r; t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Set-up) Time	50			nsec	
t_{DH}	Data to Clock Hold Time	50			nsec	
t_{a+}; t_{a-}	Clock to Data Out Delay		200	350	nsec	
t_a+; t_a−	Clock to Data Out Delay			500	nsec	I_{OL} = 0, I_{OL} = 1.6mA
t_{cs-}, t_{cs+}	Output Enable to Data Out			300	nsec	
t_{DE}	Output Enable to Data Out Disconnect			300	nsec	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz; V_{OUT} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load I_L = 1.6mA
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load (I_L = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4		V	

TIMING DIAGRAM



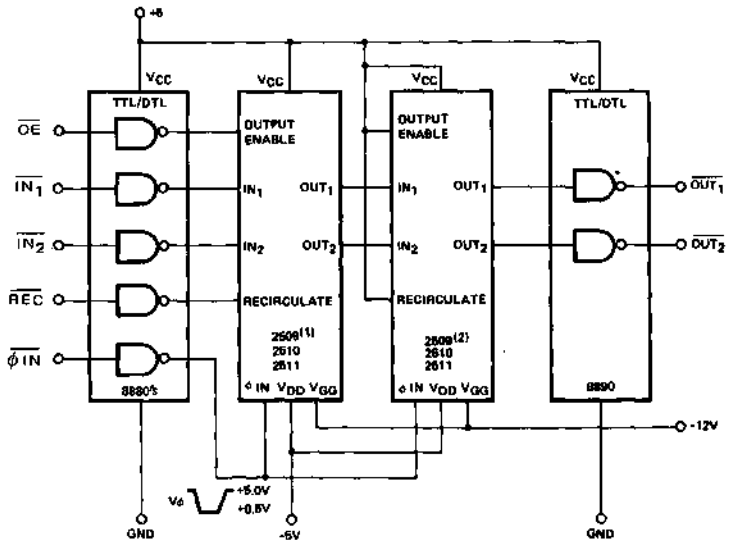
NOTE 1: WRITE CYCLE
The positive going edge of the recirculate control is coincident with the negative going edge of the input clock (ϕ_{IN}). The output enable control may be either "1" or "0".

NOTE 2: RECIRCULATE CYCLE
Data recirculates if the recirculate control is a "0"; the output enable may be either "1" or "0".

NOTE 3: READ CYCLE
The negative going edge of the output enable control is coincident with the positive edge of the clock (ϕ_{IN}). Recirculate may be either "1" or "0".

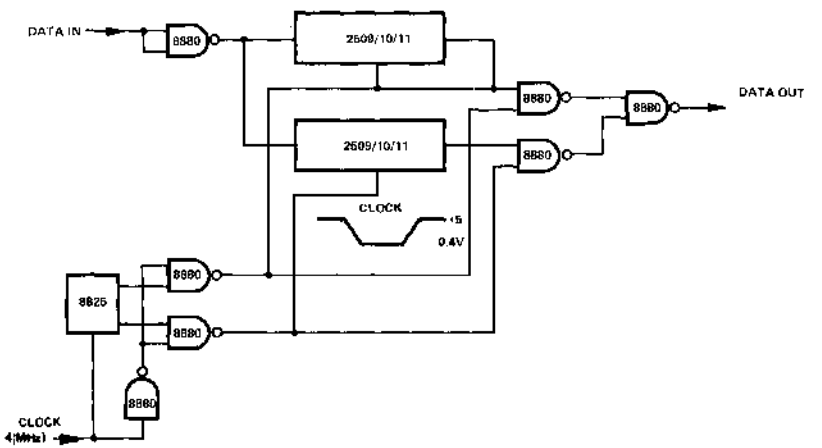
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES



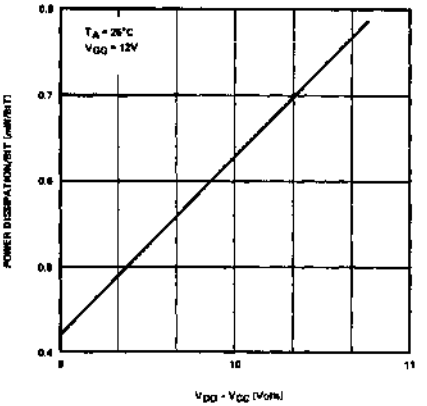
NOTES:
1. Register used as a recirculating register.
2. Register used as serial in/serial out shift register.

MULTIPLEXING MEMORY REGISTERS AT 4MHz DATA RATE

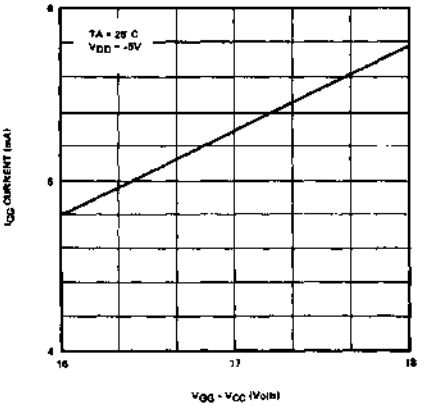


CHARACTERISTIC CURVES

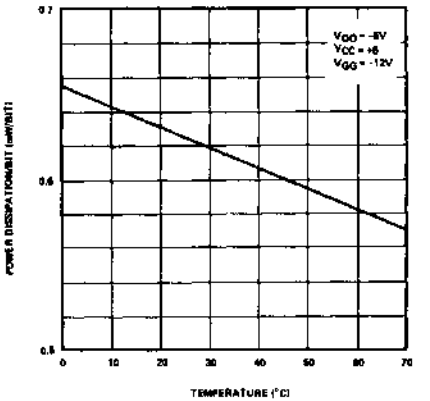
POWER DISSIPATION/BIT VERSUS V_{DD} SUPPLY VOLTAGE



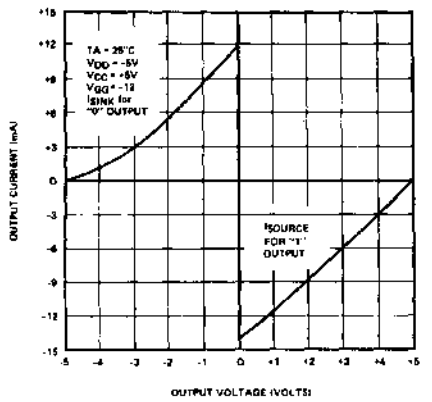
I_{GG} CURRENT VERSUS V_{GG} SUPPLY VOLTAGE



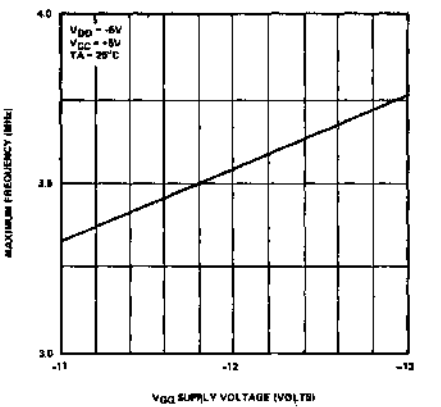
POWER DISSIPATION/BIT VERSUS TEMPERATURE



OUTPUT VOLTAGE VERSUS OUTPUT CURRENT

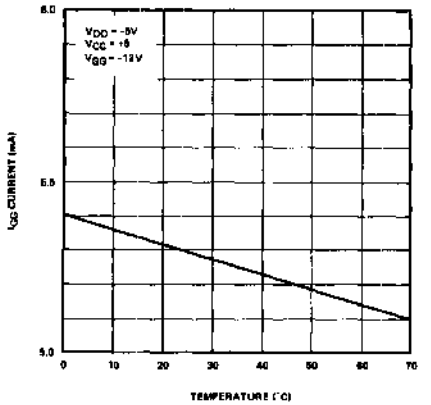


MAXIMUM FREQUENCY VERSUS V_{GG} SUPPLY VOLTAGE

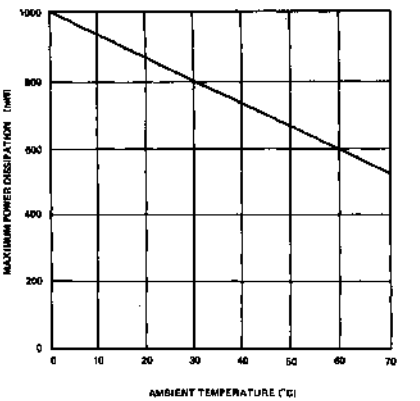


CHARACTERISTIC CURVES (Cont'd.)

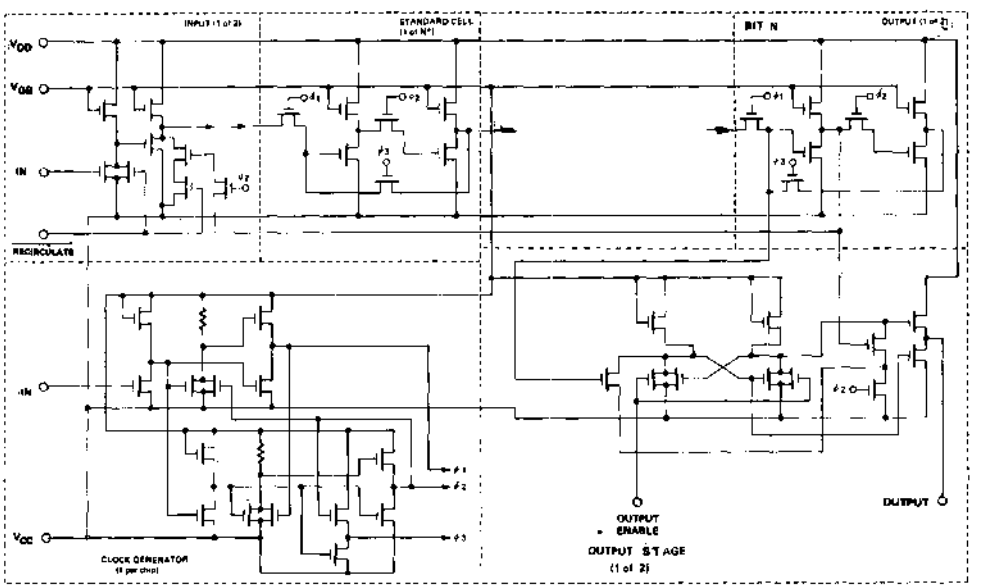
I_{GG} CURRENT VERSUS TEMPERATURE



PACKAGE MAXIMUM POWER DISSIPATION



SCHEMATIC DIAGRAM



Signetics HIGH SPEED 64 X 7 X 5 CHARACTER GENERATOR | 2513

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2513 is a high speed 2560-bit Static ROM available in 64x7x5, and 64x8x5 versions. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State-Outputs for directs, low cost interfacing with TTL, DTL and 2500 Series MOS.

FEATURES

- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR POWERFUL BUSSING CAPABILITY
- 2513/CM2140 ASCII FONT STANDARD (7 X 5)
- 24-PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

SILICONE PACKAGING

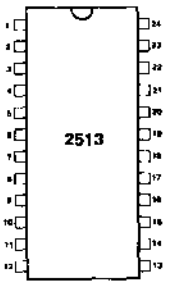
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

BIPOLAR COMPATIBILITY

All inputs of the 2513 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc). The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N/I PACKAGE



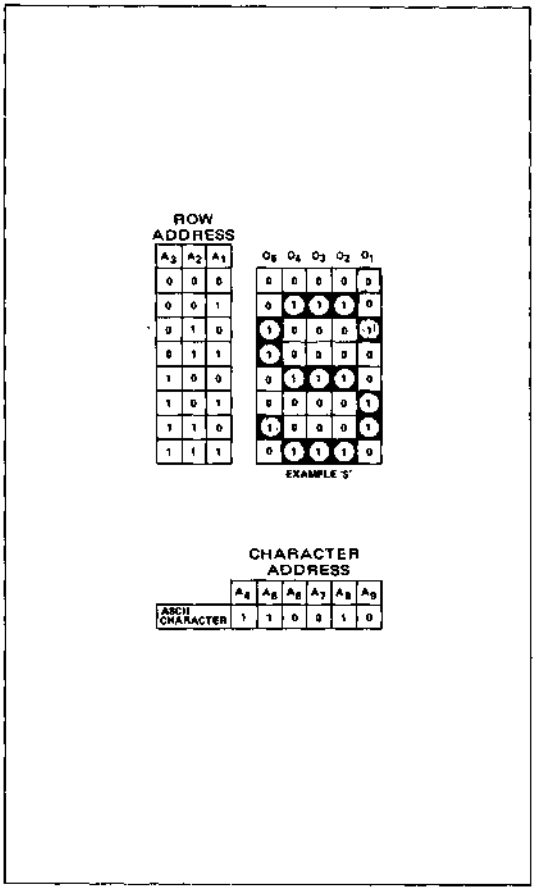
1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

PART IDENTIFICATION TABLE

PART	ORGANIZATION	PROGRAMMING
2513N/I CM2140	64X8X5	ASCII Font
2513N/I CMXXXX	64X7X5 64X8X5	Custom*

*Ask for "Signetics 2513/2514 Read Only Memory Software Package"

CHARACTER FORMAT



MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T_A 70°C	730mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8) ; V_{DD} =-5V; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

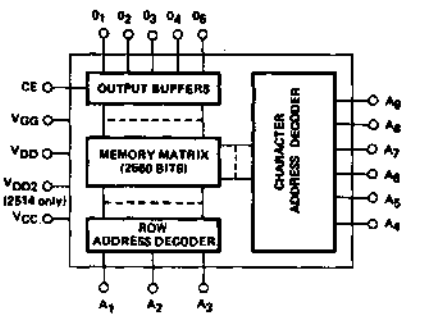
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C V_{CE} = V_{CC}
I_{DD}	V_{DD} Power Supply Current		12	15	mA	Outputs Open
I_{GG}	V_{GG} Power Supply Current		10	15	mA	Outputs Open V_{CE} = V_{CC}
V_{IL}	Input Logic "0"			1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5V (8); V_{DD} =-5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted.

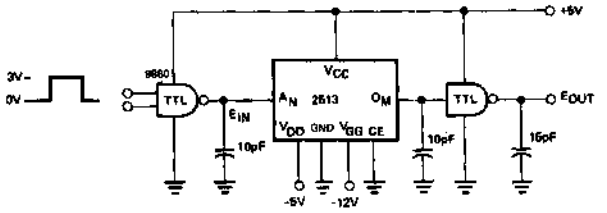
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.4	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
$^tCA_{(CM2140)}$	Character Access Time		500	600	ns	See AC Test Setup
^tRA	Row Access Time ($A_1 - A_3$)		450	500	ns	See AC Test Setup
^tCE	Chip Enable to Output		150		ns	
C_{IN}	Address Input Capacitance			10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25mV p - p

BLOCK DIAGRAM

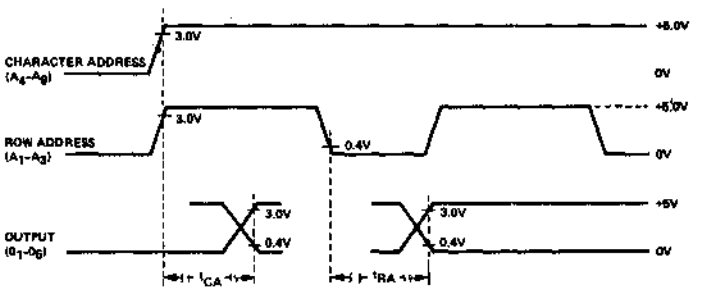


CE	OUTPUT
0	DATA
1	OPEN

AC TEST SETUP



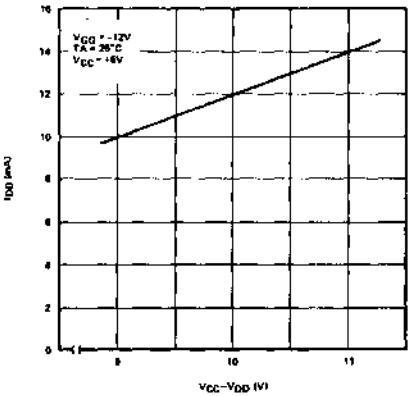
TIMING DIAGRAM (ADDRESS TIME)



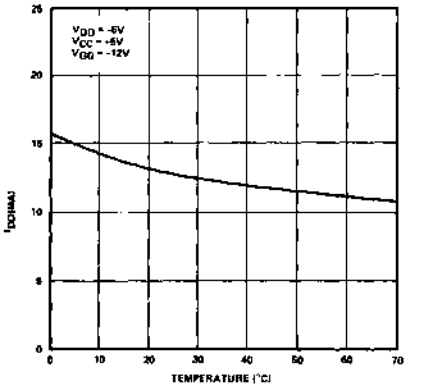
t_{CA} = Character Access Time
t_{RA} = Row Access Time

CHARACTERISTIC CURVES

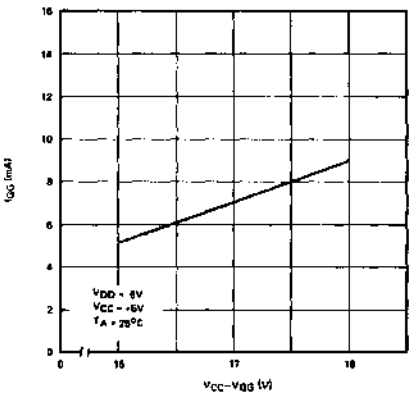
V_{DD} POWER SUPPLY CURRENT VERSUS VOLTAGE



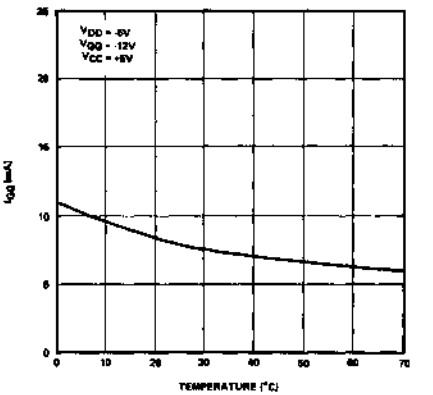
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



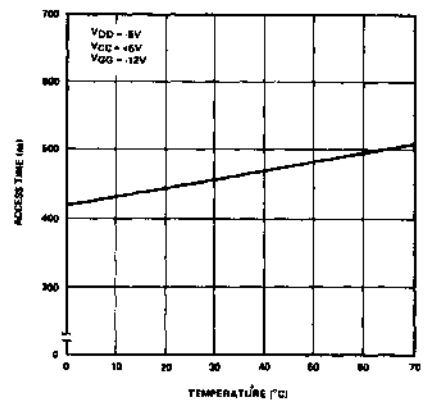
V_{GG} POWER SUPPLY CURRENT VERSUS VOLTAGE



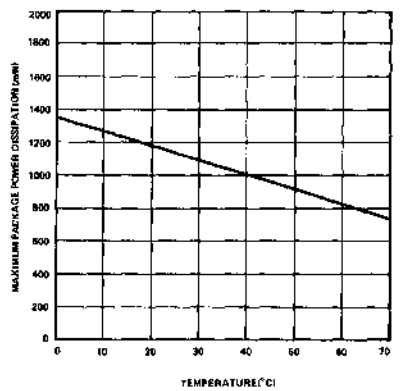
V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL ACCESS TIME VERSUS TEMPERATURE

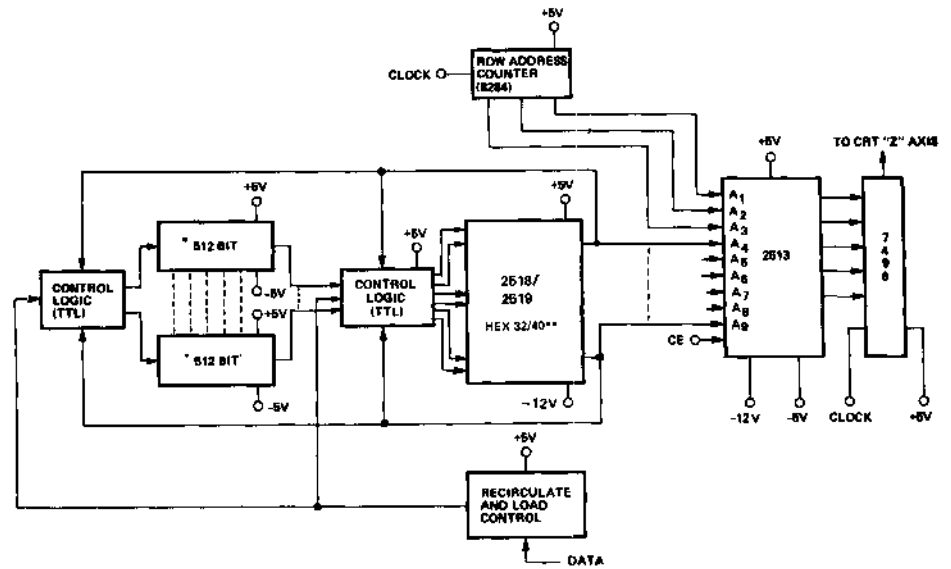


MAXIMUM PACKAGE POWER DISSIPATION



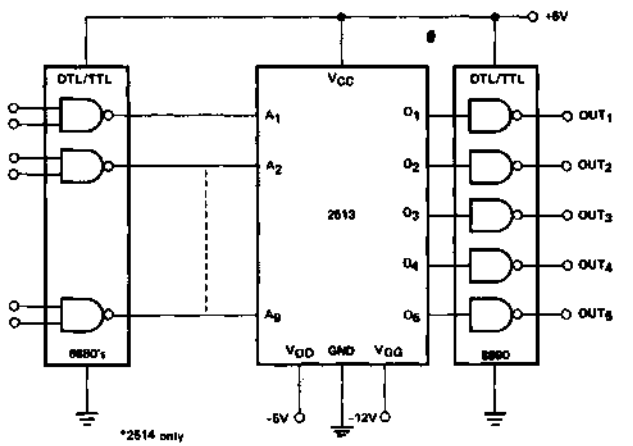
APPLICATIONS INFORMATION

CRT DISPLAY MEMORY AND CHARACTER GENERATOR



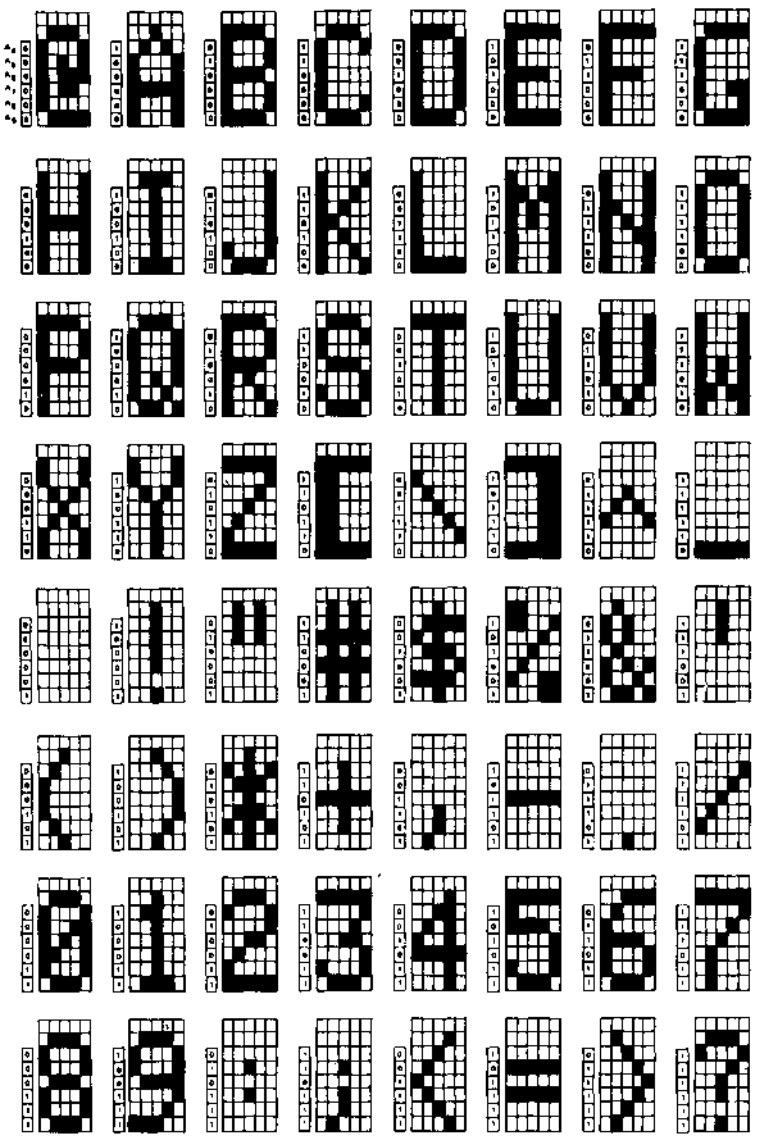
NOTE: *512 or 1024 Bit Shift Registers (2503, 2504, 2505, 2512)
** or Hex 64 BIT Two 2518's
Hex 72 BIT 2518 + 2519's

DTL/TTL INTERFACING

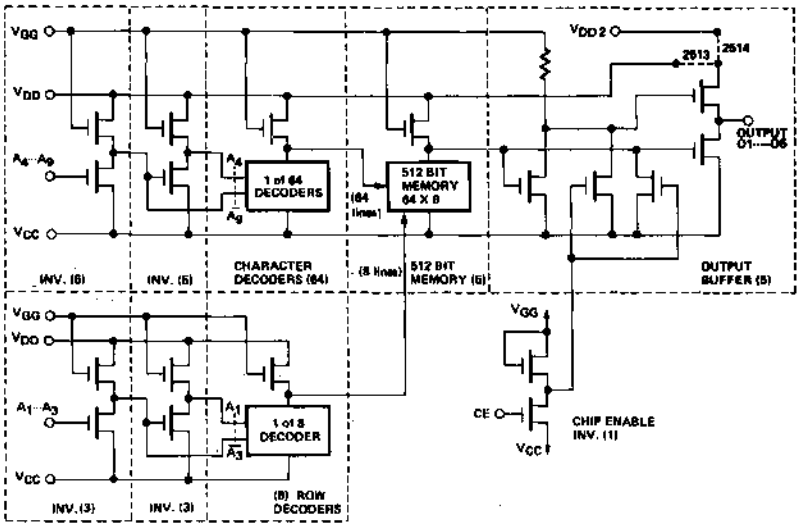


ASCII CHARACTER FONT

2513NX/CM2140



CIRCUIT SCHEMATIC



signetics

HIGH SPEED 64 X 6 X 8 STATIC CHARACTER GENERATOR | 2516

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2516 is a high speed 3072-bit Static ROM available in a 64 x 6 x 8 organization. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State-Outputs for direct, low cost interfacing with TTL, DTL and 2500 Series MOS.

FEATURES

- COLUMN OUTPUT
- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR POWERFUL BUSSING CAPABILITY
- 2516/CM 2150 ASCII FONT STANDARD (5 x 7)
- OPTIONAL SEPARATE OUTPUT V_{DD} FOR POWER REDUCTION
- OPTIONAL CHIP ENABLE "2" FOR 4 BIT WORD ORGANIZATION
- 24-PIN DIP PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

VERTICAL SCAN CRT DISPLAYS (COLUMN OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

BIPOLAR COMPATIBILITY

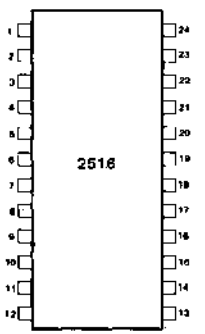
All inputs of the 2516 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA, sufficient to drive one standard TTL load.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report."

PIN CONFIGURATION (Top View)

N/I PACKAGE



1.	Chip Enable	24.	V_{CC}
2.	NC	23.	V_{GG}
3.	Output 8	22.	Address 9
4.	Output 7	21.	Address 8
5.	Output 6	20.	Address 7
6.	Output 5	19.	Address 6
7.	Output 4	18.	Address 5
8.	Output 3	17.	Address 4
9.	Output 2	16.	Address 3
10.	Output 1	15.	Address 2
11.	Ground	14.	Address 1
12.	V_{DD}	13.	NC

PART IDENTIFICATION TABLE

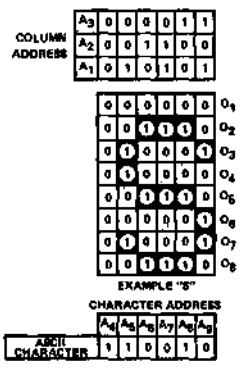
PART	ORGANIZATION	PROGRAMMING
2516N/I. CM 2150	64 x 6 x 8	ASCII Font
2516N/I CMXXXX	64 x 6 x 8	Custom*

*Ask for "Signetics 2516 Read-Only-Memory Software Package"

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @ 70°C	730 mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

CHARACTER FORMAT



NOTE:
Undefined (column) addresses result in "1" level (high) outputs.

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V; V_{DD} = -5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted. (Notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C
I_{DD}	V_{DD} Power Supply Current		14	21	mA	V_{CE} = V_{CC} Outputs Open
I_{GG}	V_{GG} Power Supply Current		8	12	mA	Outputs Open
V_{IL}	Input Logic "0"	-5		1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

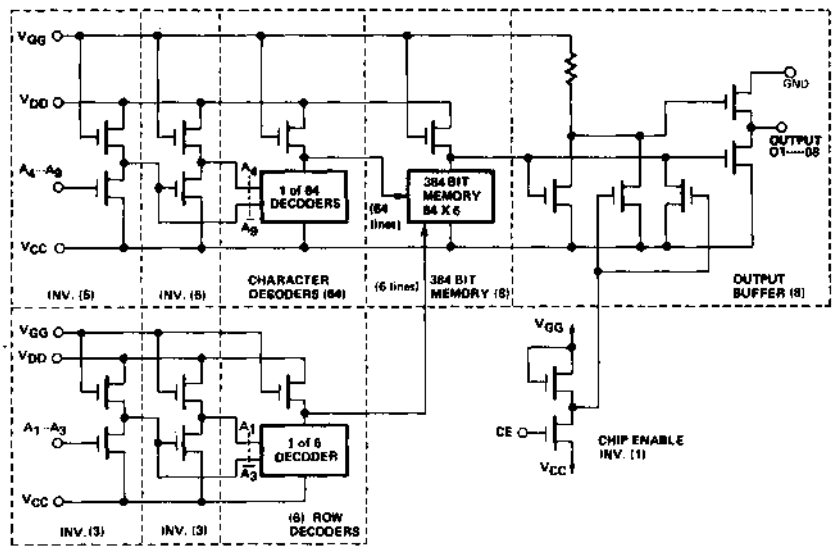
AC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5V(8); V_{DD} = -5%; V_{GG} = -12V +5%; unless otherwise noted.

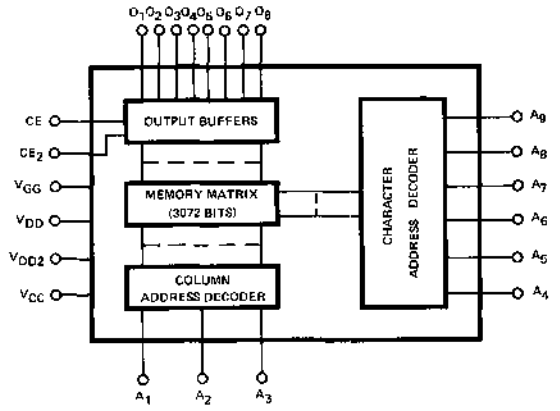
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.8	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
t_{CA}	Character Access Time		500	600	ns	See AC Test Setup*
t_{CA}	Column Access Time (A_1 - A_3)		400	500	ns	See AC Test Setup*
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{IH} = V_{CC}, 25mV p-p

*T_A=0°C to +70°C

CIRCUIT SCHEMATIC



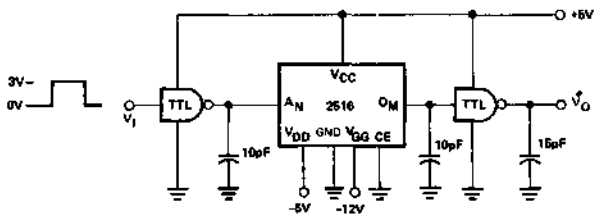
BLOCK DIAGRAM



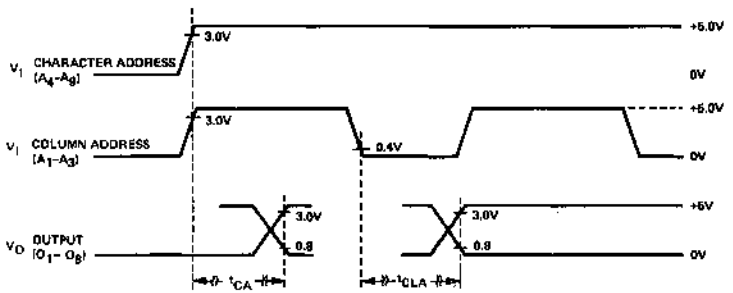
Note: For 4-Bit organization Chip Enable 1 controls $O_1 - O_4$, Chip Enable 2 controls $O_5 - O_8$.

CE	OUTPUT
0	DATA
1	OPEN

AC TEST SETUP



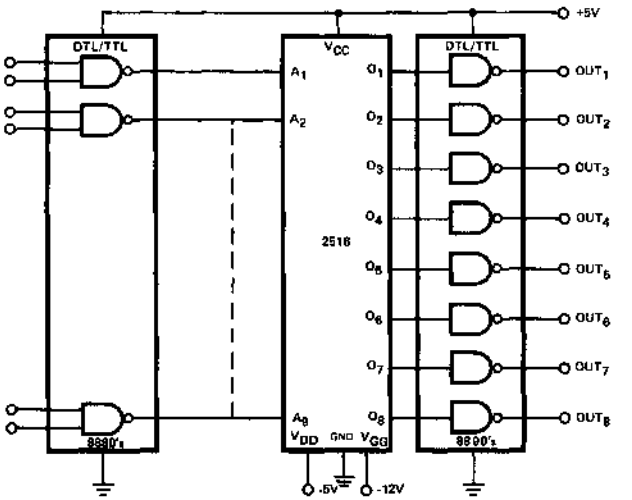
TIMING DIAGRAM (ADDRESS TIME)



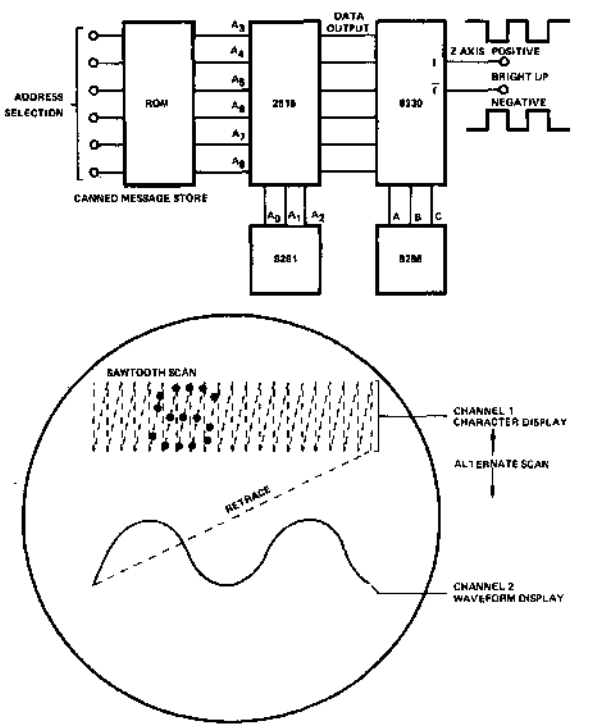
t_{CA}=CHARACTER ACCESS TIME
t_{CLA}=COLUMN ACCESS TIME

APPLICATIONS INFORMATION

DTL/TTL INTERFACING

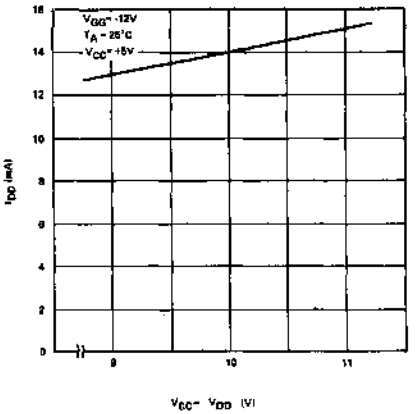


CRT DISPLAY MEMORY AND CHARACTER GENERATOR

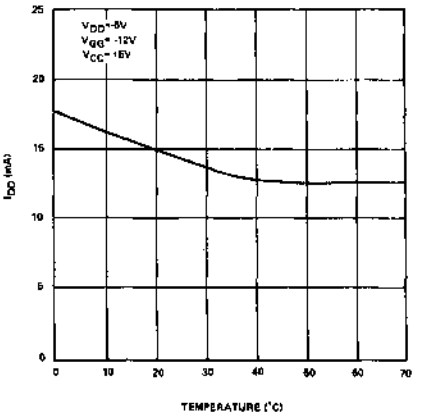


CHARACTERISTIC CURVES

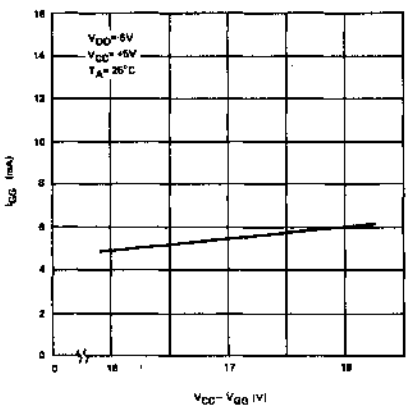
V_{DD} POWER SUPPLY CURRENT VERSUS VOLTAGE



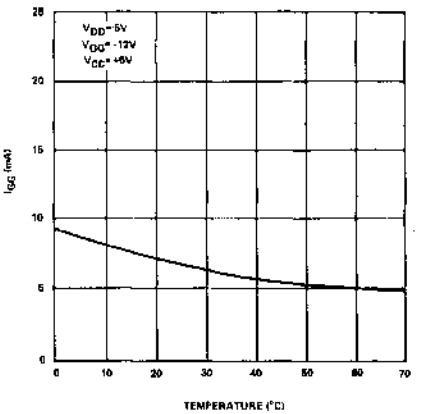
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



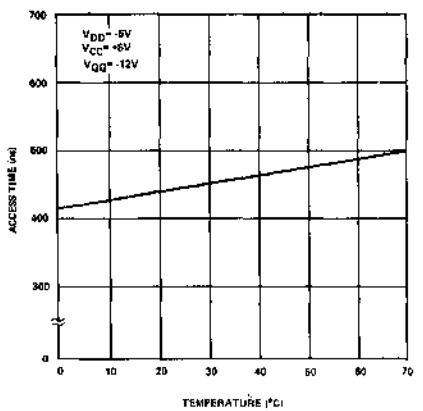
V_{GG} POWER SUPPLY CURRENT VERSUS VOLTAGE



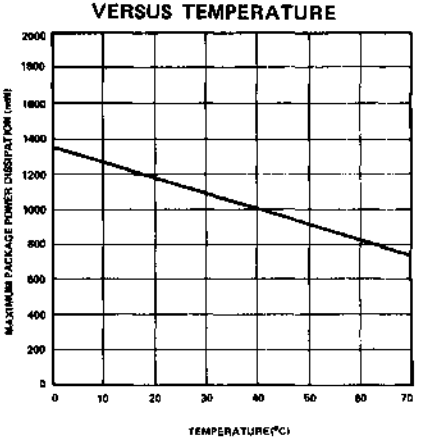
V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL ACCESS TIME VERSUS TEMPERATURE

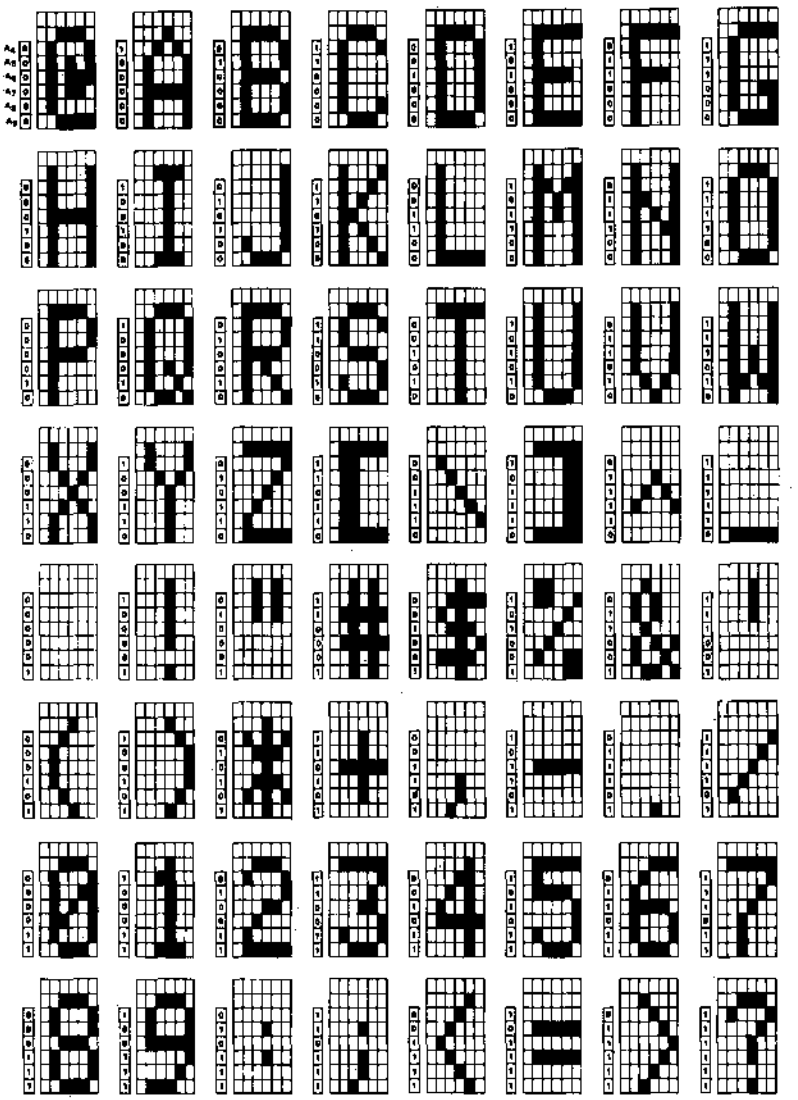


MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



ASCII CHARACTER FONT

2516NX/CM2150



NOTE: Forbidden addresses yield logic "1" outputs.

APPLICATIONS DATA:

OUTPUT INTERFACING NOTES

The tri-state outputs on this device exhibit three states:

"1" – low impedance to +5V
"0" – low impedance to -5V
OFF – high impedance = 10 megohm

The "off" state is controlled by the chip enable control inputs.

CUSTOM ROM ORGANIZATIONS

The 2516 is a static ROM with a total 64 x 6 x 8 bit capacity. This allows a standard 5 x 7 font to be encoded in the ROM, e.g., the 2516/CM2150 ASCII font standard product. Also custom coding of up to 6 x 8 character generators, also 256 x 8, 384 x 8, or 768 x 4 ROMs are available using Signetics "2516 Read Only Memory Software Package."

For applications requiring a 708 x 4 organization, CHIP ENABLE and CHIP ENABLE 2 are used to control outputs 1-4 and 5-8 respectively. The outputs are externally hard wired in pairs for this organization.

Custom versions of the 2516 can be supplied with a separate V_{DD} supply terminal for the output buffer. This feature permits operation at reduced power dissipation.

signetics

HEX 32-HEX 40-BIT STATIC SHIFT REGISTERS

2518
2519

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Hex 32 and 40-bit recirculating static shift registers consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing capability.

FEATURES

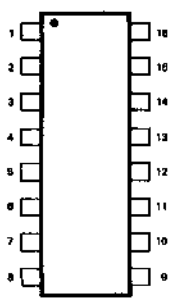
- TYPICAL CLOCK AND DATA RATE = 3MHz
- TTL/DTL COMPATIBLE CLOCK (SINGLE) PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- SINGLE-ENDED (BARE DRAIN) BUFFERS
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 16 PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CARD EQUIPMENT BUFFERS

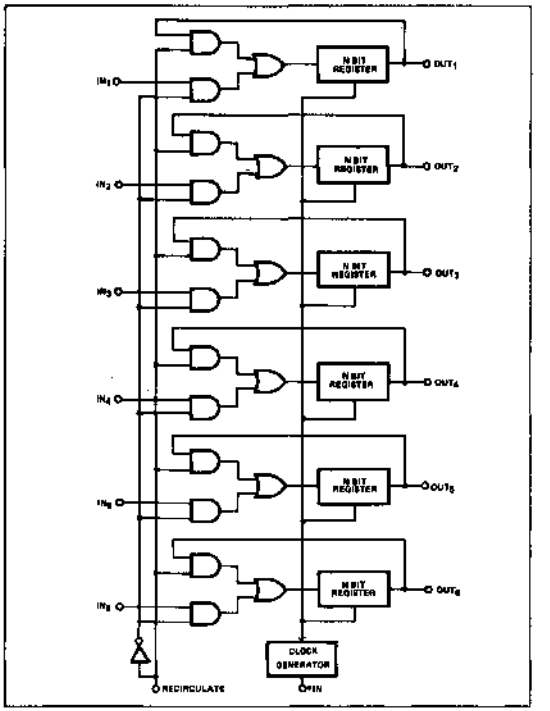
PIN CONFIGURATION (Top View)

B/I PACKAGE



1. IN_4	16. V_{CC}
2. IN_5	15. IN_3
3. IN_6	14. IN_2
4. Recirculate	13. IN_1
5. V_{GG}	12. OUT_1
6. Clock	11. OUT_2
7. OUT_6	10. OUT_3
8. OUT_5	9. OUT_4

BLOCK DIAGRAM



TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2518B	HEX 32	16-Pin Silicone DIP
2518I	HEX 32	16-Pin Ceramic DIP
2519B	HEX 40	16-Pin Silicone DIP
2519I	HEX 40	16-Pin Ceramic DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	640 mW
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to -20V

NOTES:

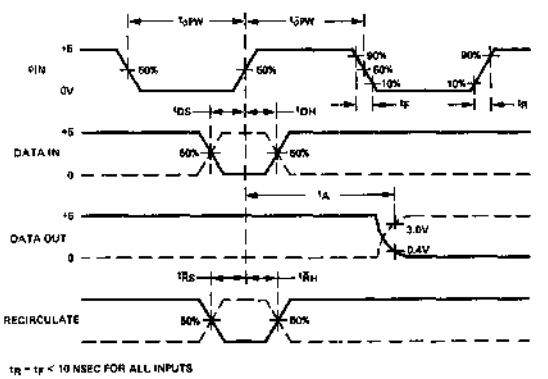
1. Strasses above those listed under "Maximum Guaranteed Rating" may causa parmanent damage to tha device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5% Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} is dependent on R_L and characteristics of driven gate.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8); V_{GG} = -12V ± 5% unless otherwise noted. (Notes: 3,4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} =-5,5V, T_A = 25°C
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		16	25	mA	CONTINUOUS OPERATION T_A = 25°C F = 2MHz
V_{IL}	INPUT "LOW" VOLTAGE			1.05	V	
V_{IH}	INPUT "HIGH"VOLTAGE	3.2		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			1.05	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.3	V	

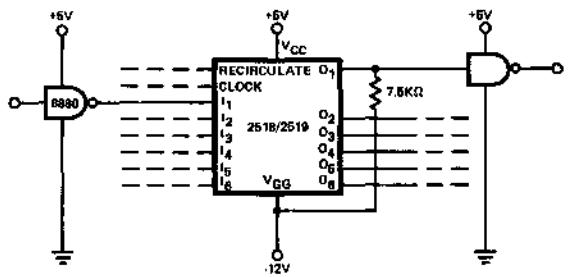
TIMING DIAGRAM



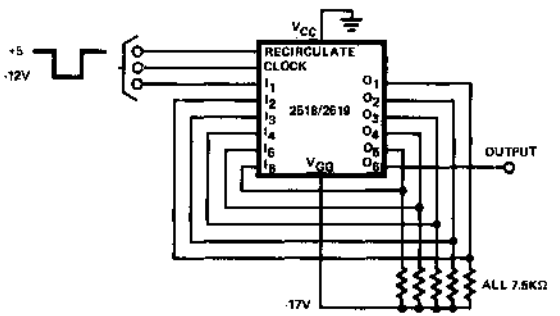
Note: Input rise and fall times: 10nsec. Output load is 1 TTL gate.

AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V$;(8) $V_{GG} = -12V \pm 5\%$, $V_{ILC} = 0.4V$ to $4.0V$

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC	3	2	MHz	See Max Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.300		100	μsec	
$t_{\overline{\phi} PW}$	$\overline{\text{CLOCK}}$ PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			5	μsec	
t_{DS}	DATA WRITE (SET-UP) TIME	100			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		300	350	nsec	
t_{RS}	RECIRCULATE SET-UP TIME	150			ns	
t_{RH}	RECIRCULATE HOLD TIME	50			ns	
$t_{\overline{\phi} PW}$	$\overline{\text{CLOCK}}$ PULSE WIDTH	.200		DC	μsec	
C_{in}	INPUT CAPACITANCE		5	7	pF	@ 1MHz; $V_{in} = V_{CC}$; $V_{AC} = 25mV$ p-p
C_{ϕ}	CLOCK CAPACITANCE		6	7	pF	@ 1MHz; $V_{\phi} = V_{CC}$; $V_{AC} = 25mV$ p-p
V_{OL}	OUTPUT "LOW" VOLTAGE		0.4		V	Note 9
V_{OH}	OUTPUT "HIGH" VOLTAGE	3.6			V	$R_L = 7.5K\Omega$ to V_{GG}



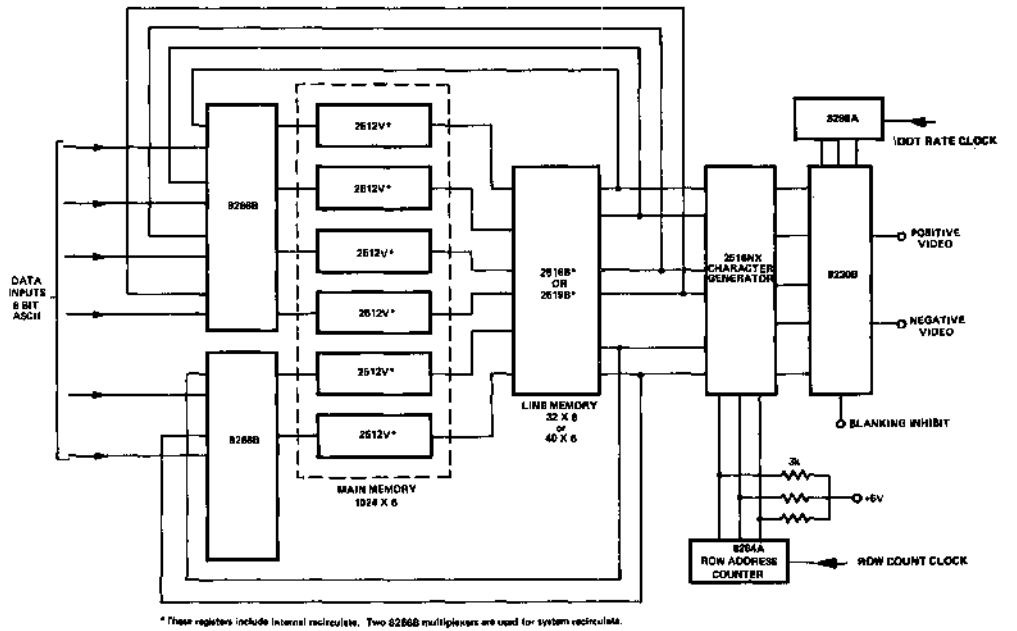
TTL INTERFACE



MOS INTERFACE

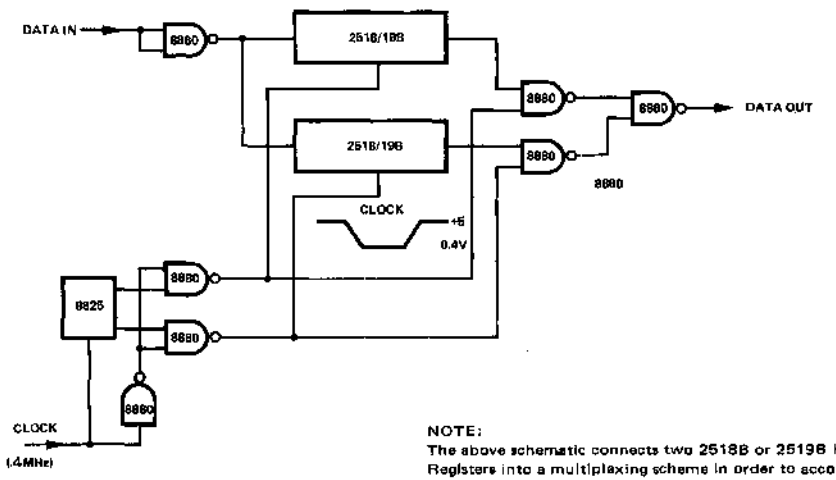
APPLICATIONS DATA

32 or 40 POSITION CRT DISPLAY MEMORY SYSTEM



* These registers include internal recirculate. Two 8286B multiplexers are used for system recirculate.

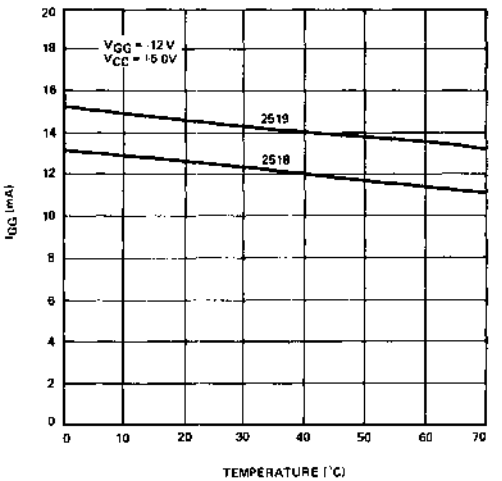
MULTIPLEXING LINE MEMORY REGISTERS AT 4MHz DATA RATE



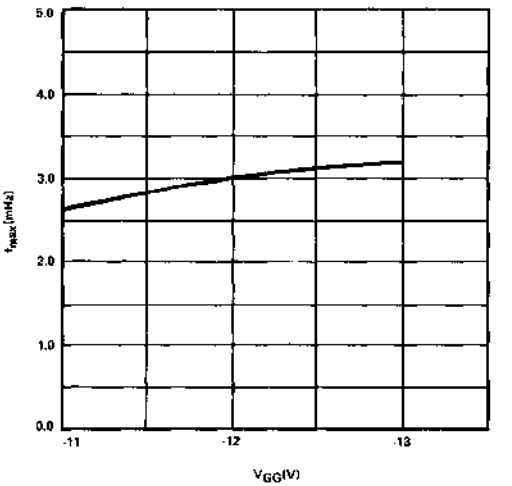
NOTE:
The above schematic connects two 2518B or 2519B Hex Shift Registers into a multiplexing scheme in order to accomplish a 64 or 80 character/line display at 4MHz data rate.

CHARACTERISTIC CURVES

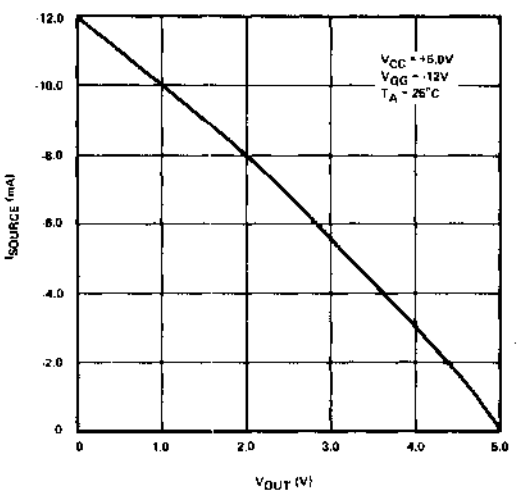
I_{GG} VERSUS TEMPERATURE



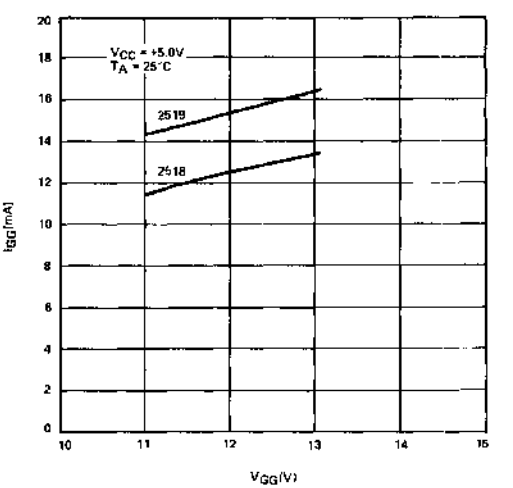
MAXIMUM SHIFT FREQUENCY VERSUS V_{GG}



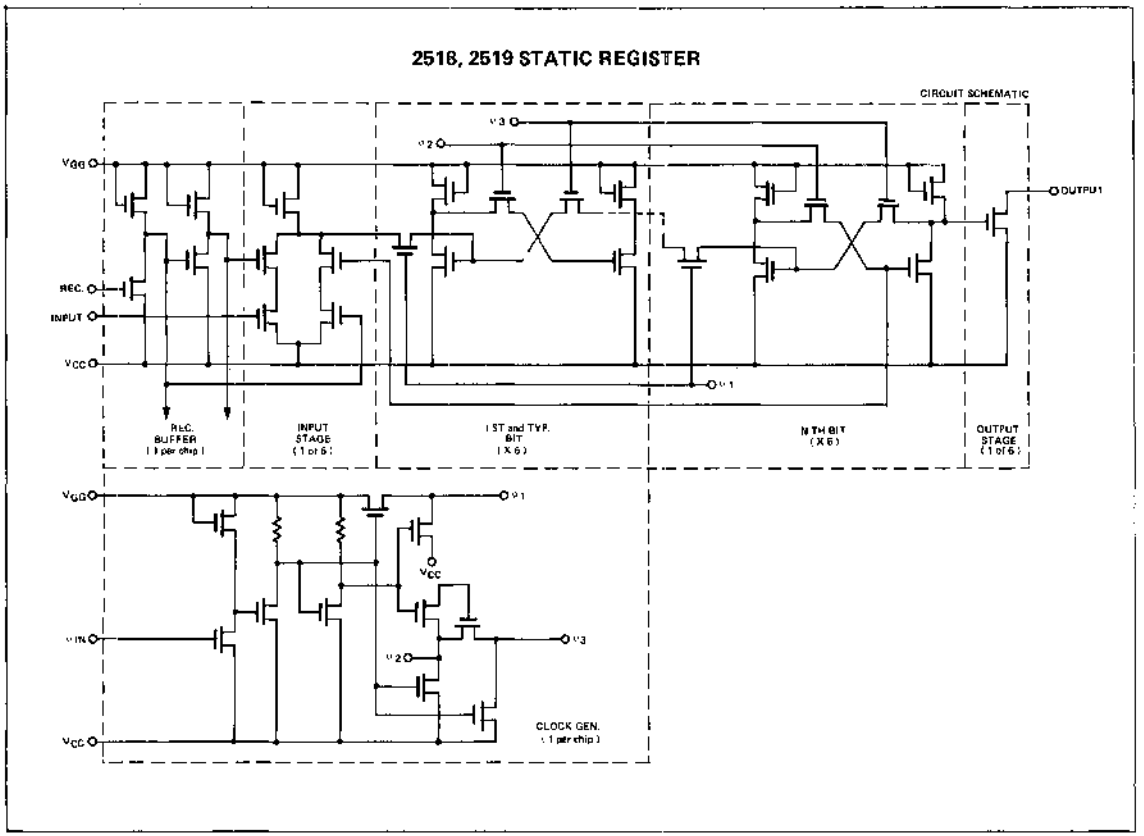
I_{SOURCE} VERSUS V_{OUT}



I_{GG} VERSUS V_{GG}



CIRCUIT SCHEMATIC



signetics

DUAL 128-132 BIT STATIC SHIFT REGISTERS

2521
2522

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Dual 128 and 132 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 2MHz TYPICAL CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

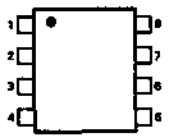
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CASSETTE RECORDERS

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
8. V_{CC}
7. IN_2
6. OUT_2
5. ϕ_{IN}

TRUTH TABLE

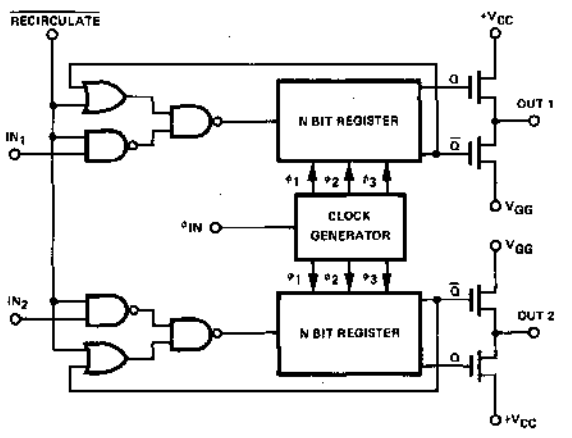
$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V.

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2521V	Dual 128	8 Pin DIP
2522V	Dual 132	8 Pin DIP

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:

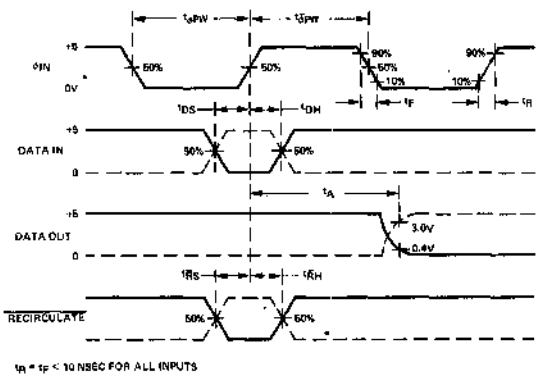
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nomin. supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} = 5.5V, T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		28	32	mA	CONTINUOUS OPERATION F = 1.5MHz, T_A=25°C
V_{IL}	INPUT "LOW" VOLTAGE			1.05	V	
V_{IH}	INPUT "HIGH" VOLTAGE	3.2		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			1.05	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.3	V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate

TIMING DIAGRAM



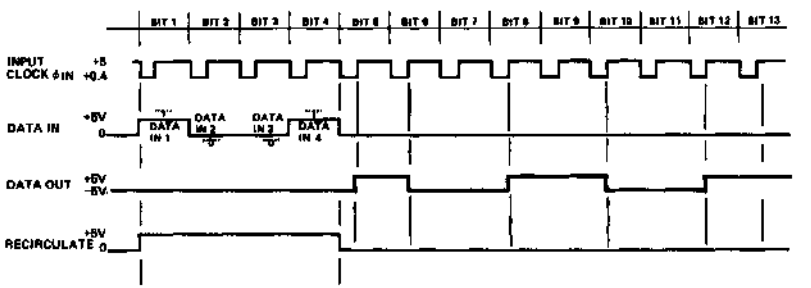
tR = tF < 10 NSEC FOR ALL INPUTS

AC CHARACTERISTICS V_{CC} = +5V (8); V_{GG} = -12V ±5%, V_{IC} = 0.4 to 4.0; T_A=0° to +70°C

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC		1.5	MHz	See Maximum Frequency Curve
$t\phi_{PW}$	CLOCK PULSE WIDTH	.350	.700	100	μsec	
$t_{\overline{\phi}PW}$	CLOCK PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			1	usec	
t_{DS}	DATA WRITE (SET-UP) TIME	75			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		250	350	nsec	
$t_{\overline{RS}}$	$\overline{\text{RECIRCULATE}}$ SET-UP TIME	60			ns	
$t_{\overline{RH}}$	$\overline{\text{RECIRCULATE}}$ HOLD TIME	50			ns	
C_{IN}	INPUT CAPACITANCE			5	pF	@ 1MHz; $V_{in} = V_{CC}$; V_{AC} = 25mV p-p
$C\phi$	CLOCK CAPACITANCE			5	pF	@ 1MHz; $V_\phi = V_{CC}$; V_{AC} = 25mV p-p
V_{OL}	OUTPUT "LOW" VOLTAGE	-4.0		0.4	V	1 TTL load (I_L=1.6mA)
V_{OH1}	OUTPUT "HIGH" VOLTAGE DRIVING 1 TTL LOAD	3.0	3.5		V	1 TTL load (I_I = 100μA)
V_{OH2}	OUTPUT "HIGH" VOLTAGE DRIVING MOS	3.5	4.0		V	

TIMING DIAGRAM

4 BIT RECIRCULATING SHIFT REGISTER *

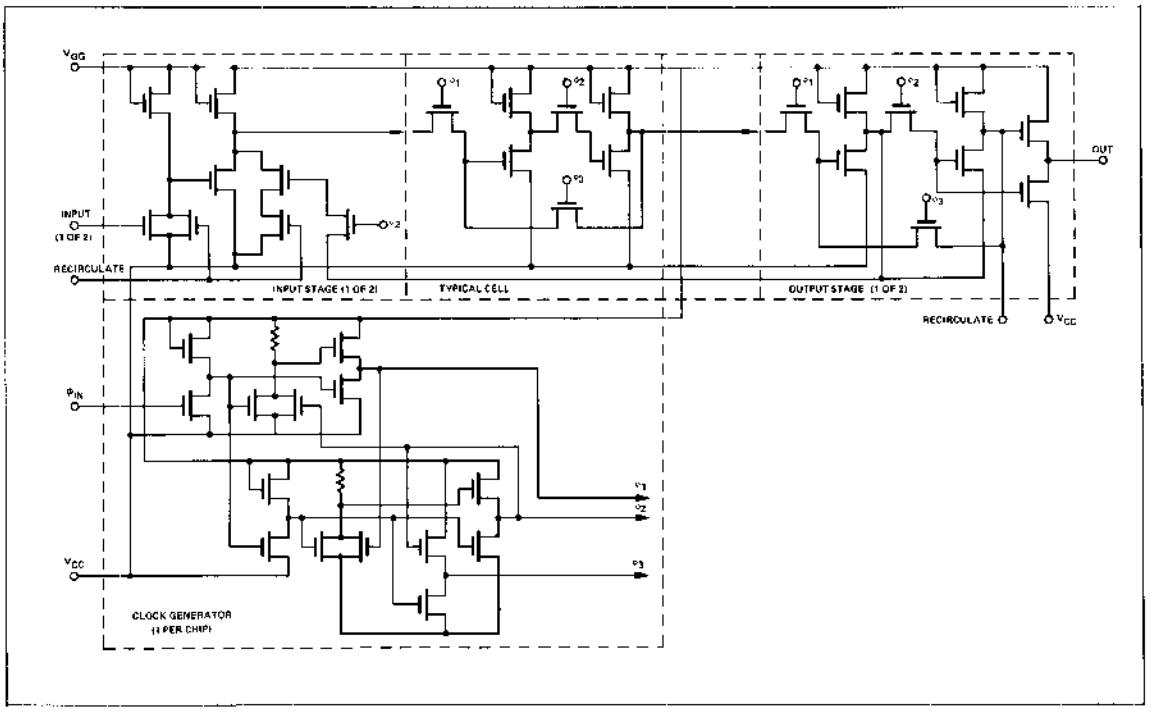


NOTE 1: WRITE CYCLE
The positive going edge of the recirculative control is coincident with the negative going edge of the input clock (ϕ_{IN}).

NOTE 2: RECIRCULATE CYCLE
Data recirculates if the recirculate control is a "0"

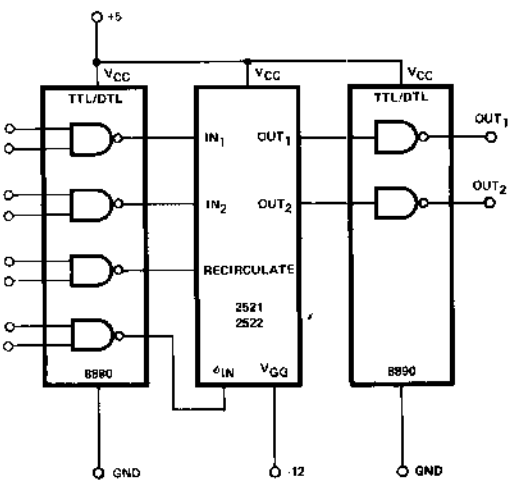
*For clarity, a four bit hypothetical example is shown

SCHEMATIC DIAGRAM



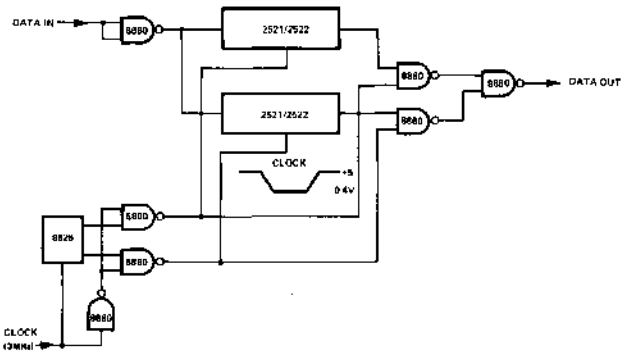
APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



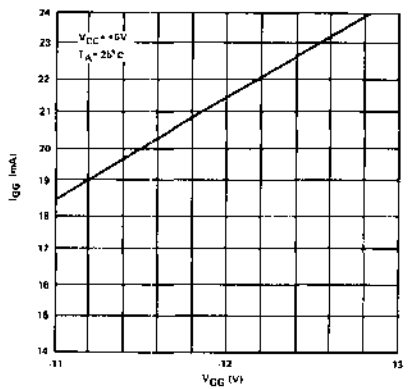
APPLICATIONS INFORMATION

MULTIPLEXING LINE MEMORY REGISTERS AT 3MHz DATA RATE

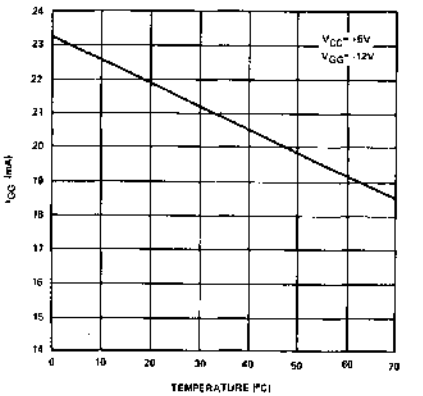


CHARACTERISTIC CURVES

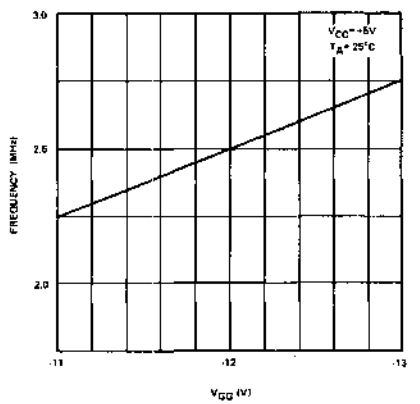
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



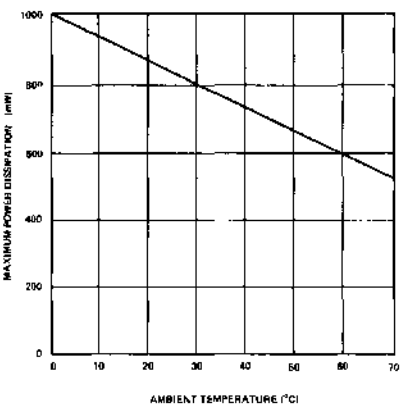
POWER SUPPLY CURRENT VERSUS TEMPERATURE



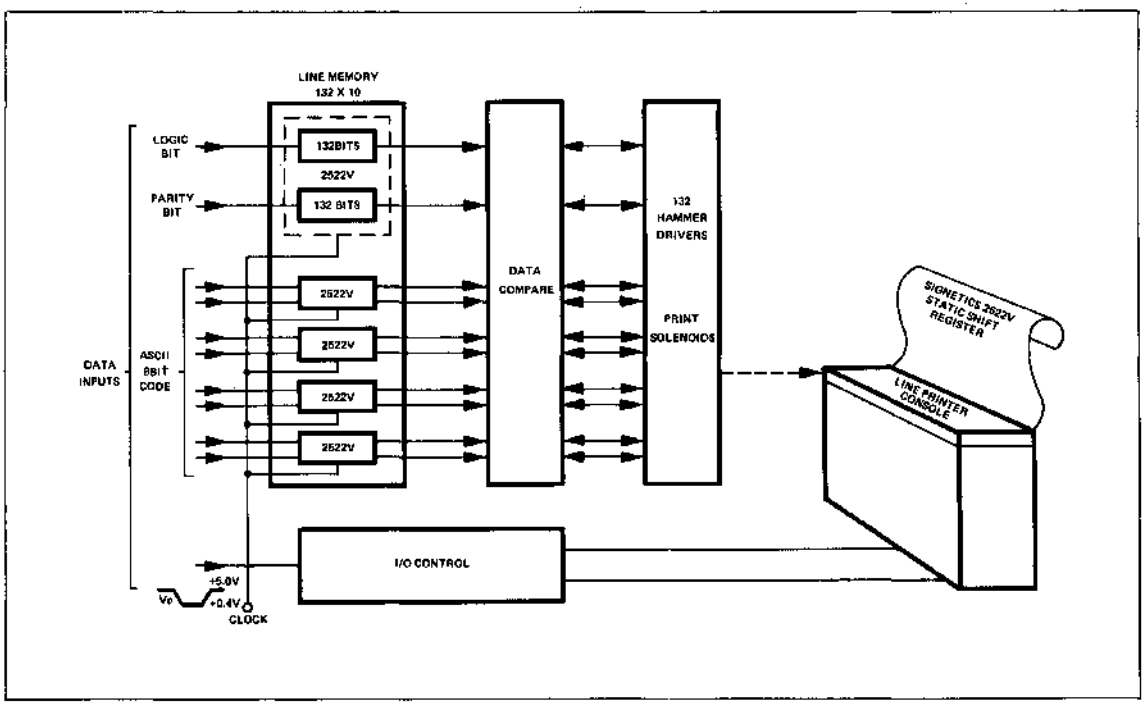
TYPICAL OPERATING FREQUENCY VERSUS SUPPLY VOLTAGE



PACKAGE MAXIMUM POWER DISSIPATION



132 COLUMN LINE PRINTER



signetics

512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2524
2525

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION-5 MHz Typical Clock Rate
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION-150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE-80pF for 512, 160pF for 1024 Bits
- +5, -5 POWER SUPPLIES
- STANDARD PACKAGE 8-LEAD DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (5MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

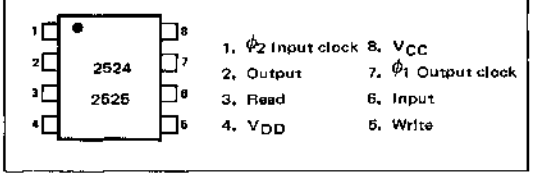
The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

SILICONE PACKAGING

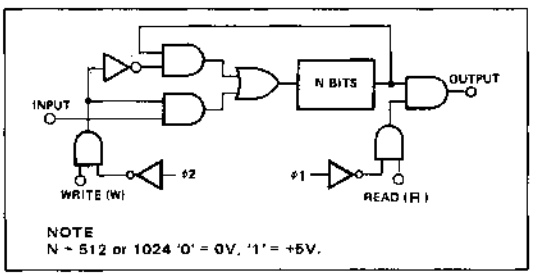
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

V PACKAGE



BLOCK DIAGRAM



NOTE
N = 512 or 1024 '0' = 0V, '1' = +5V.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2524V	512	8 pin DIP
2525V	1024	8 pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to 20V

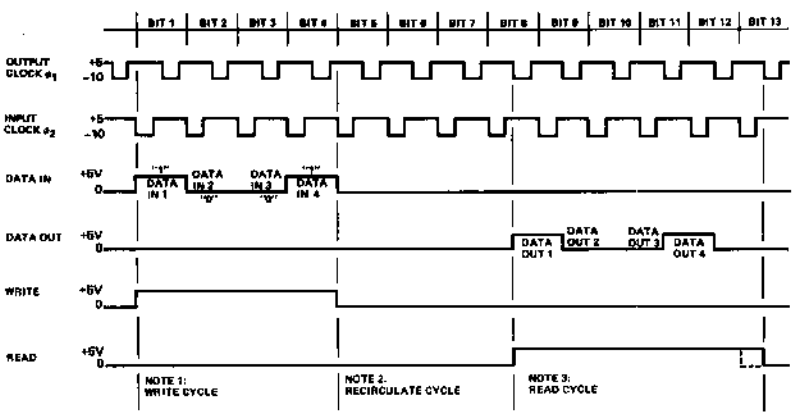
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Parameters are valid over operating temperature range unless otherwise specified.
9. V_{CC} tolerance is ± 5%. Any variation is actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(9); V_{DD} = 5V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYPICAL	MAX	UNIT	CONDITION
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V; T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1}$ = $V_{\phi2}$ = -12V; V_{DD} = -5 V_{OUT} =-5.5V; T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -12V ; T_A = 25°C
I_{DD}	Power Supply Current: 2524		15	35	mA	Continuous Operation; ϕpW = 150nS; 1MHz
	2525		25	35	mA	V_{ILC} = -12V; T_A = 25°C V_{DD} = -5.5V
V_{IL}	Input "Low" Voltage	-5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM



NOTE:
This is a simplified illustration of the timing of a 4 bit recirculating shift register showing the 3 basic modes of operation.

NOTE 1: (WRITE cycle)

The positive and negative going edge of the "Write" control is coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0"

NOTE 2: (RECIRCULATE cycle)

Data recirculates if the "Write" control line is "0". "Read" may be either "1" or "0".

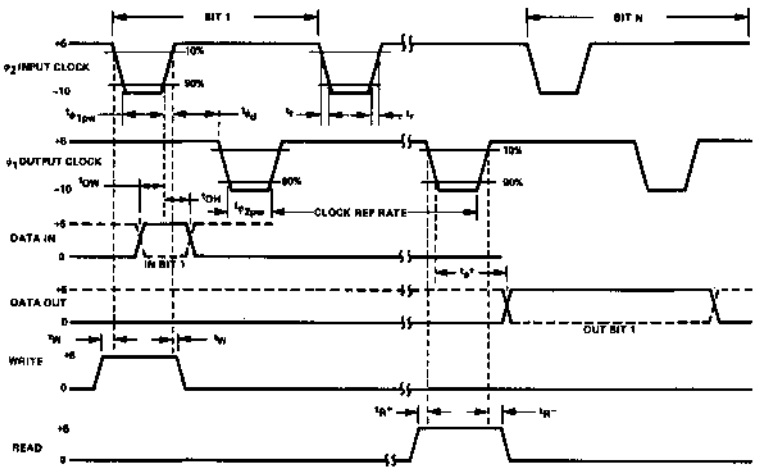
NOTE 3: (READ cycle)

The positive going edge of the "Read" control is coincident with the negative edge of the output clock (ϕ_1). The negative going edge of "Read" is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. "Write" may be either "1" or "0"

CONDITIONS OF TEST

Input rise and fall times: 10 sec Output load is 1 TTL gate

TIMING DIAGRAM



NOTE:

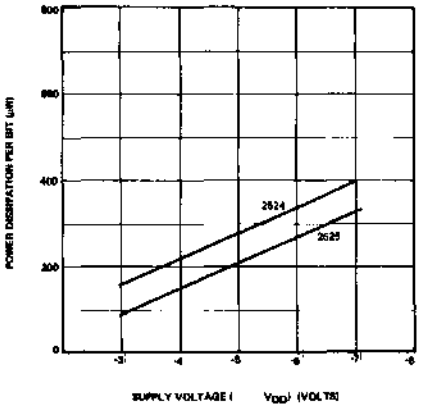
1. N = 512 for 2524 N= 1024 for 2525
2. Note that the Read Input is AND'ed with $\overline{\phi}_1$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS $T_A = +25°C$ $V_{CC} = +5V(9)$; $V_{DD} = -5V \pm 5\%$; $V_{ILC} = -11V$

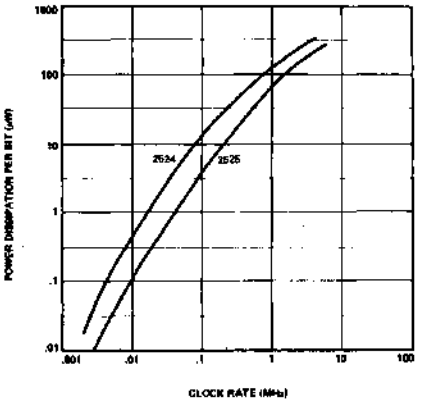
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	5	3	MHz	$W = R = V_{CC}$
$t_{\phi pw}$	Clock Pulse Width	135	85		ns	
$t_{\phi d}$	Clock Pulse Delay	10			ns	
t_r;t_f	Clock Pulse Transition	10		1000	ns	
t_{DW}	Data Write (Setup) Time	70			ns	
t_{DH}	Data to Clock Hold Time	20			ns	
t_{a+}	Clock to Data Out Delay			100	ns	
t_{R-}; t_{W-}	Clock to "Read" or "Write" Timing	0			ns	
t_{R-}; t_{W+}	Clock to "Read" or "Write" Timing	0			ns	
C_{in}	Input Capacitance			5	pF	1MHz; $V_I=V_{CC}$;V_{AC}=25m V_{P-P}
C_{out}	Output Capacitance			5	pF	1MHz; $V_0=V_{CC}$;V_{AC}=25m V_{P-P}
C_ϕ	Clock Capacitance 2524 2525			 80 160	 pF pF	1MHz; $V=V_{CC}$; V_{AC}=25m V_{P-P}
V_{OL}	Output "Low" Voltage		-1.0		V	R_L =3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L=3.0K; 1 TTL Load (I_L=100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10pF

CHARACTERISTIC CURVES

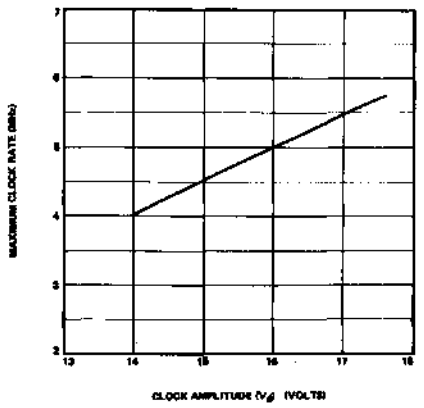
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



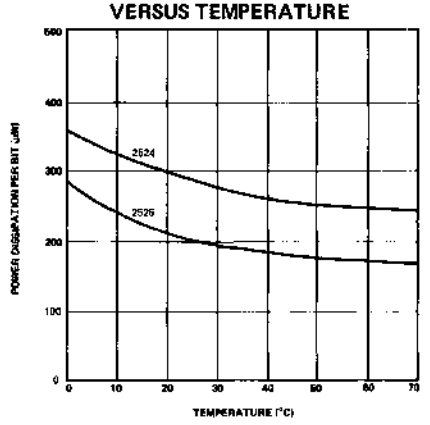
POWER DISSIPATION/BIT VERSUS CLOCK RATE



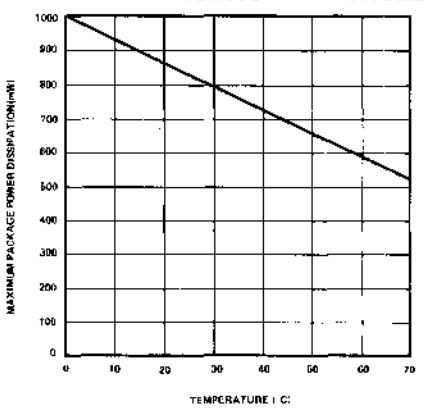
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



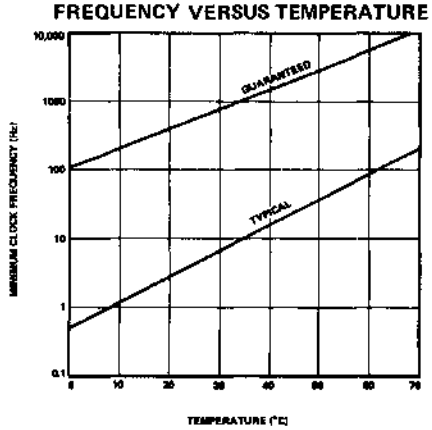
POWER DISSIPATION/BIT VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



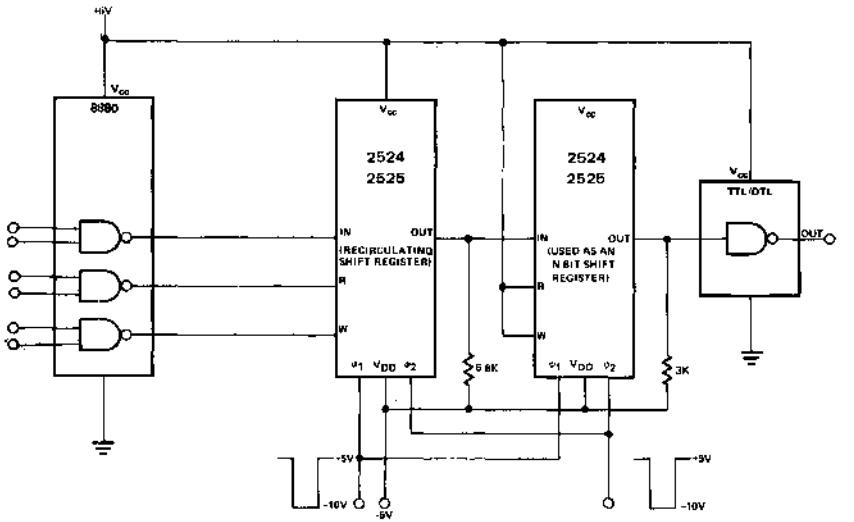
MINIMUM OPERATING CLOCK FREQUENCY VERSUS TEMPERATURE



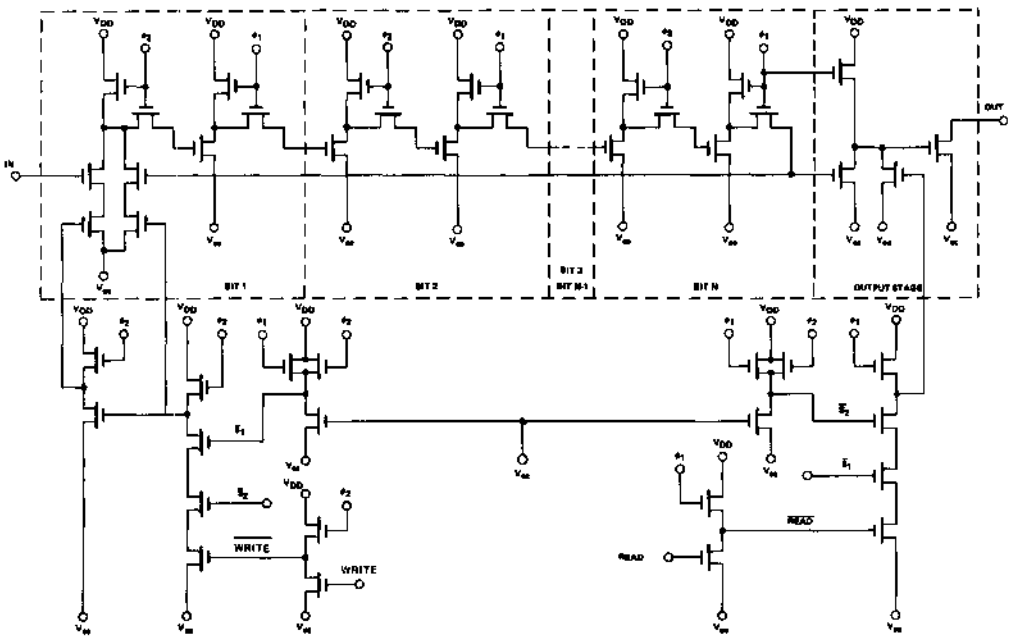
NOTE:
Conditions for typical curves: V_{CC} = +5V, V_{DD} = -5V, clock duty cycle = 35%, f_{CLK} = 3MHz, $V\phi_{p\text{-}p}$ = 16V, $\phi_{PW1} = \phi_{PW2}$ = 80ns, T_A = +25°C unless otherwise noted.

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



CIRCUIT SCHEMATIC



NOTE
N = 512 for 2524
N = 1024 for 2525

signetics

HIGH SPEED 64 x 9 x 9 STATIC CHARACTER GENERATOR | 2526

ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2526 is a high speed 5,184-bit Static Read-Only Memory available in a 64x9x9 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. OUTPUT ENABLE controls the nine output devices without affecting address circuitry.

FEATURES

- 64x9x9 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- STATIC OPERATION
- OUTPUT LATCHES
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE-STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = −12V
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

VERTICAL OR RASTER SCAN DISPLAYS (7x9 MATRIX)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

BIPOLAR COMPATIBILITY

All inputs of the 2526 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

STANDARD TRUTH TABLES

The 2526N/CM3940 is a 7x9 matrix, ASCII character set (raster scan)* utilizing the two unused left-most columns for BCDIC-ASCII and BAUDOT-ASCII code converters. Use this device for evaluation or for suitable application. Other standards will be announced as they become available.

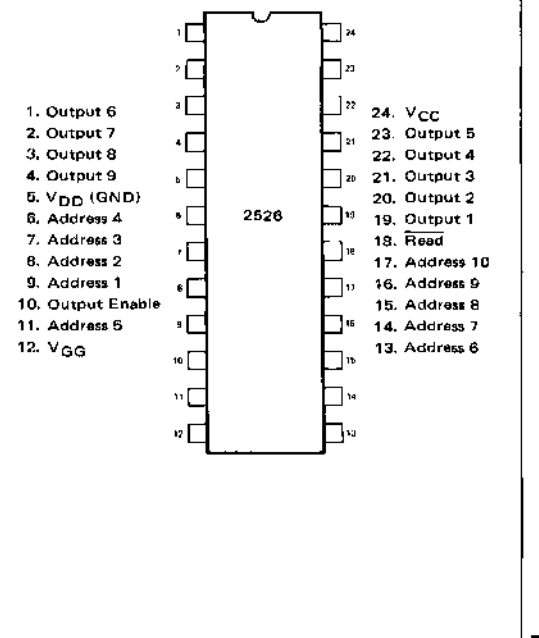
*for vertical scan specify CM3400

CUSTOM TRUTH TABLES

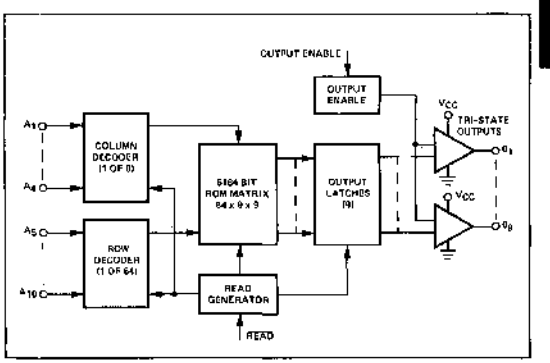
See page 7-197.

PIN CONFIGURATION (Top View)

N PACKAGE



BLOCK DIAGRAM



PART IDENTIFICATION

PART	OP. TEMP. RANGE	PACKAGE
2526N	0-70°C	24-Pin Silicone DIP
2526I	0-70°C	24-Pin Ceramic DIP

NOTE: "0" = 0V, "1" = +5V

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70°C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A=0° to +70°C, V_{CC}= +5V; V_{GG}= −12V ±5%; unless otherwise noted. (See notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		30	45	mA	(8)
I_{GG}	V_{GG} Power Supply Current		30	45	mA	(8)
V_{IL}	Input Logic "0"	-5		1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

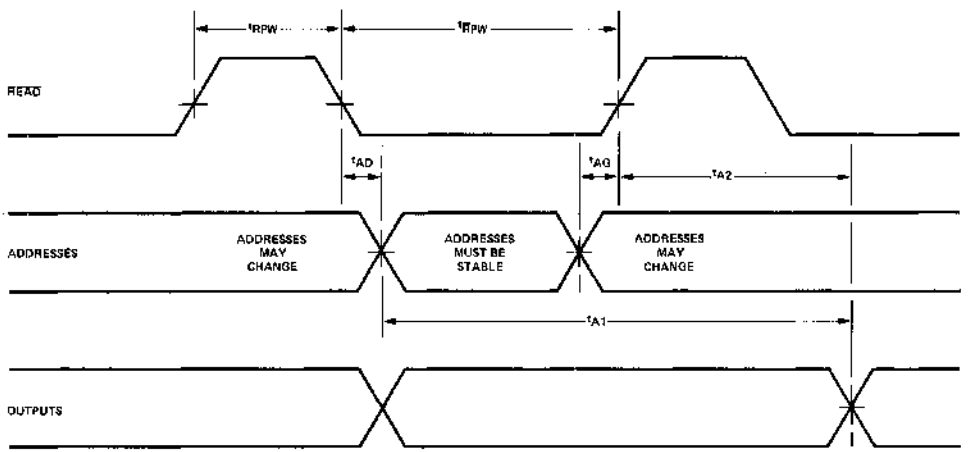
T_A=0°C to +70°C; V_{GG}=−12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output Logic "zero"			0.8	V	One TTL Load
V_{OH}	Output Logic "one"	3.0			V	One TTL Load
t_{RPW}[11]	Read Pulse Width	250	200		ns	
$t_{\overline{RPW}}$[10]	$\overline{\text{Read}}$ Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (12)			50	ns	
t_{AG}	Address-Read Pulse Gap (12)			50	ns	
t_{A1}	Address to Output Delay		625	700	ns	(9)
t_{A2}	End of $\overline{\text{Read}}$ Pulse to Output Delay		200	250		(9)
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}
t_{OE}	Output Enable to Output Delay		100	250	ns	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs Open, t_{RPW} = 250ns, $t_{\overline{RPW}}$ = 500ns.
9. t_A = 0°C to +70°C
10. During $t_{\overline{RPW1}}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
11. During $t_{\overline{RPW1}}$ addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{READ}}$ pulse. After t_{A2}, data appears at the output terminals.
12. Addresses must be stable within 50ns after the $\overline{\text{READ}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{READ}}$ line goes high.

TIMING DIAGRAM

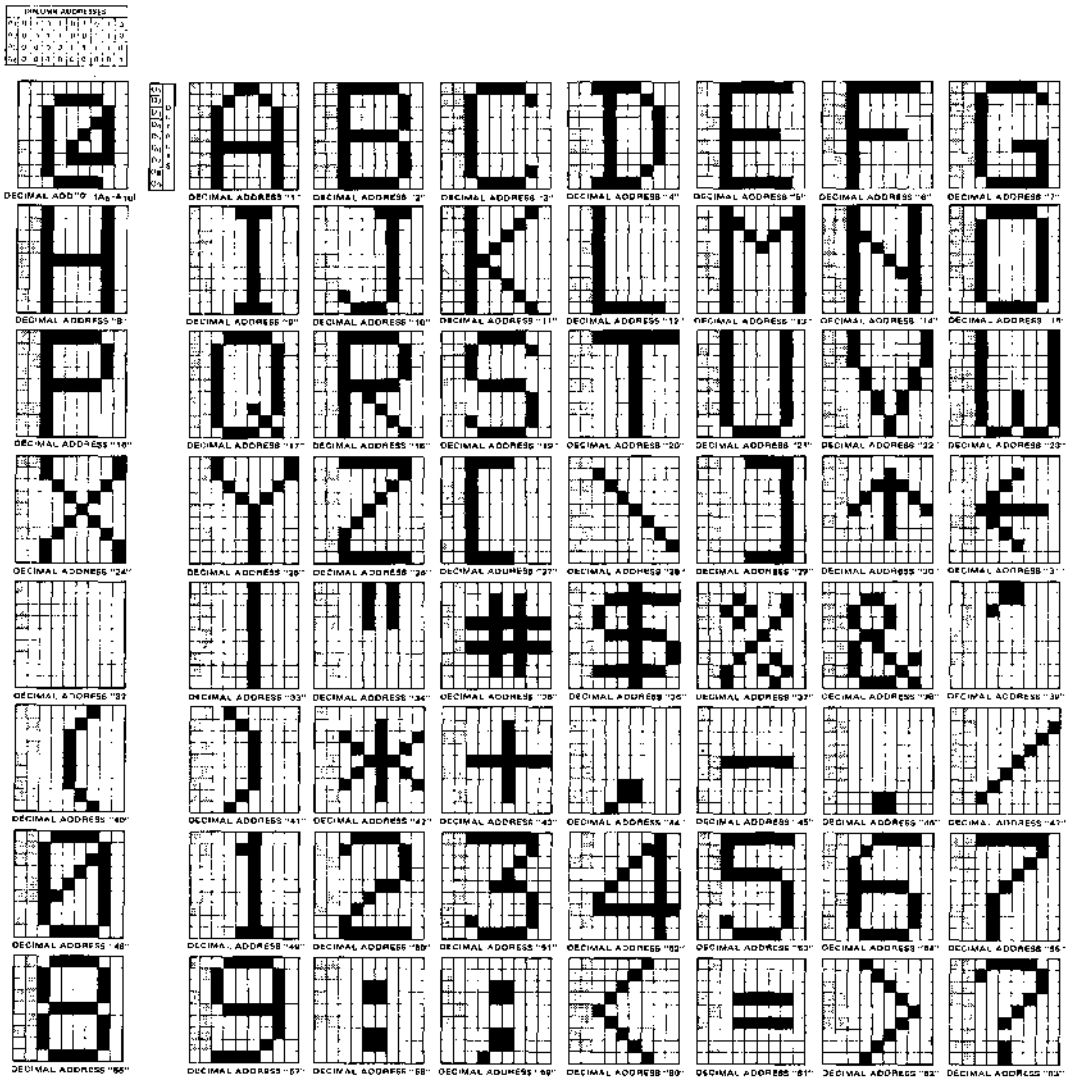


Note: All times measured from 50% points, for all input waveforms tr = t_f<10nsec.

CHARACTER FONTS

CM 3400

ASC I I SET, VERTICAL SCAN 7X9 WITH CODE CONVERSION[1]

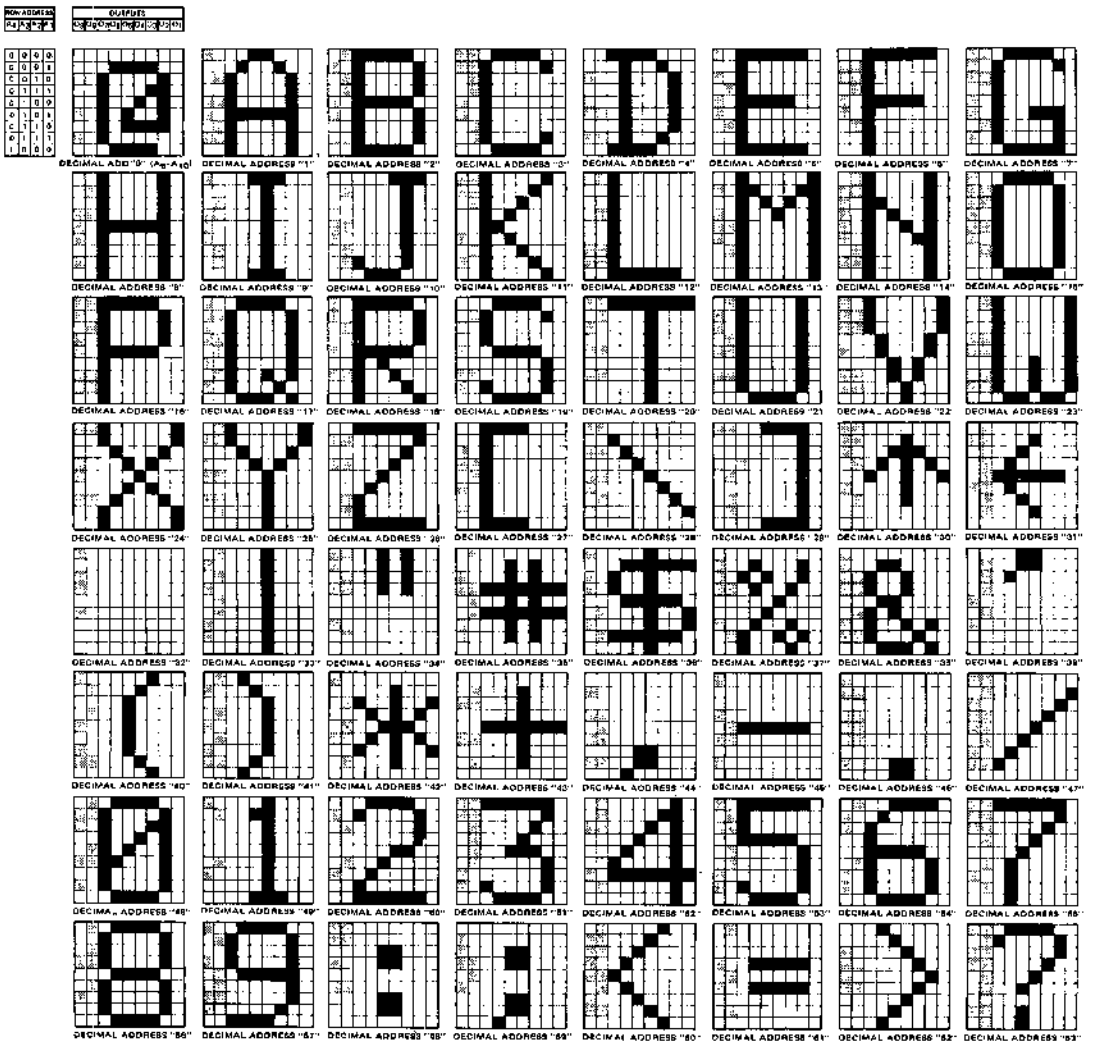


NOTES
1. BCDIC to ASC I I in leftmost column, Baudot to ASC I I in next column to right.
2. Undefined addresses result in all outputs going low (TTL "0").
3. Blank squares in character font are high (TTL "1").

CHARACTER FONTS (Cont'd)

CM 3940

ASC I I SET, RASTER SCAN 7X9 WITH CODE CONVERSION(1)



NOTES
1. BCDIC to ASC I I in leftmost column, Baudot to ASC I I in next column to right.
2. Undefined addresses result in all outputs going low (TTL "0").
3. Blank squares in character font are high (TTL "1").

signetics

DUAL 256-250-240 BIT STATIC SHIFT REGISTERS

PRELIMINARY SPECIFICATION

SILICON GATE 2500 SERIES

2527
2528
2529

DESCRIPTION

The Signetics 2500 Series Dual 256, 250 and 240 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

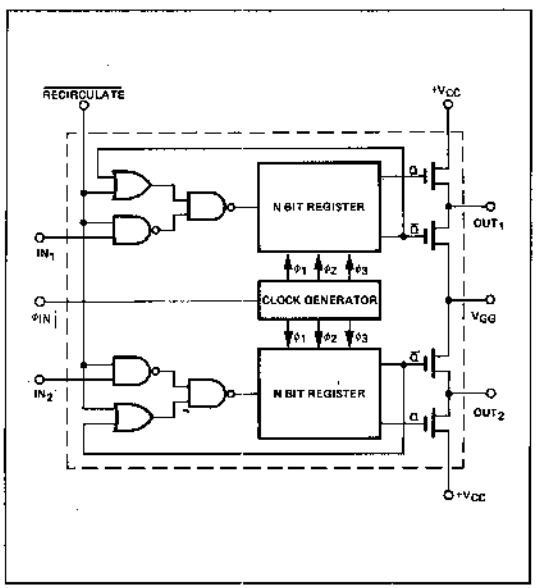
FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 3 MHz TYPICAL CLOCK & DATA RATE
- TTL, DTL COMPATIBLE INPUTS AND OUTPUTS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
CASSETTE RECORDERS

BLOCK DIAGRAM

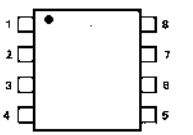


BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The outputs drive directly into TTL/DTL without requiring external resistors.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
5. ϕ_{IN}
6. OUT_2
7. IN_2
8. V_{CC}

TRUTH TABLE

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2527V	Dual 256	8 Pin DIP
2528V	Dual 250	8 Pin DIP
2529V	Dual 240	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	–65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

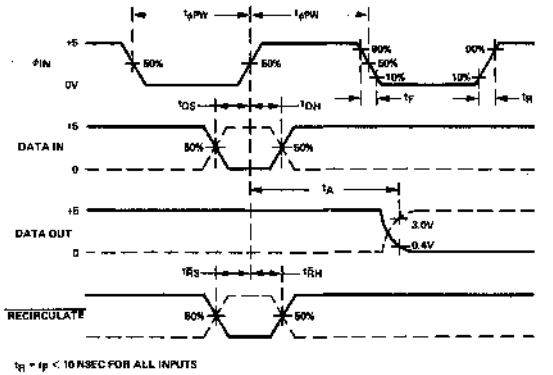
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		28	35	mA	Continuous Operation F = 2.5 MHz, T_A = 25°C Outputs Open
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage			1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

AC CHARACTERISTICS T_A =0° to +70°C, V_{CC} = +5V(8); V_{GG} = -12V +5%, V_{IC} = 0,4 to 4,0V

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	Clock Rep Rate	DC	2.5	1.5	MHz	See Maximum Frequency Curve
$t_{\phi PW}$	Clock Pulse Width	0.2	0.1	100	μs	
$t_{\bar{\phi} PW}$	$\overline{\text{Clock}}$ Pulse Width	0.2		DC	μs	
t_R t_F	Clock Pulse Transition			1	μs	
t_{DS}	Data Set-up Time	50			ns	
t_{DH}	Data Hold Time	50			ns	
t_A	Clock to Data Out Delay		330	450	ns	I_{OL} = 1.6mA
$t_{\overline{RS}}$	$\overline{\text{Recirculate}}$ Set-up Time	50			ns	
$t_{\overline{RH}}$	$\overline{\text{Recirculate}}$ Hold Time	50			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I_L = 1.6mA)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load (I_l = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.5	4.0		V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

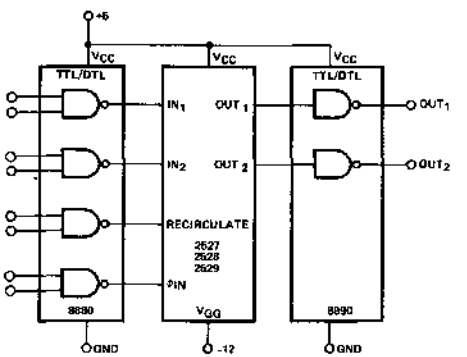
TIMING DIAGRAM



$t_R = t_F < 10$ NSEC FOR ALL INPUTS

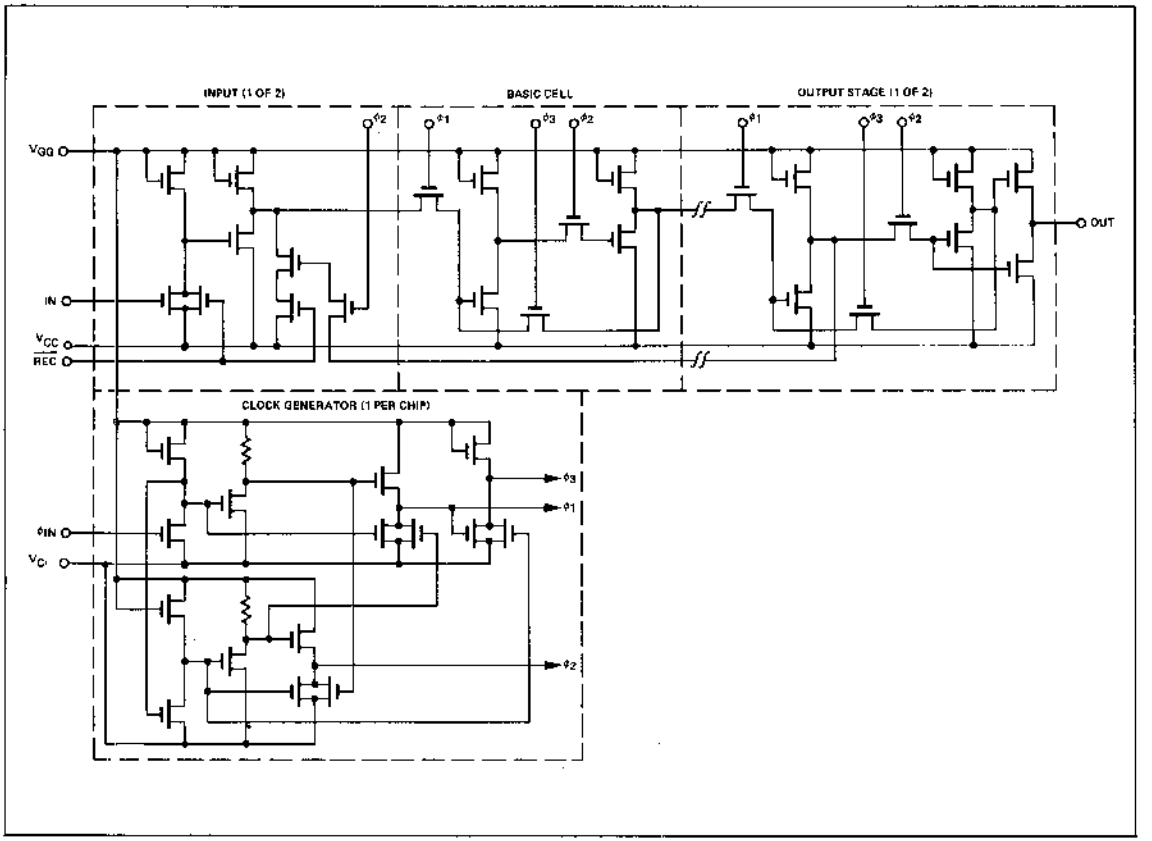
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES

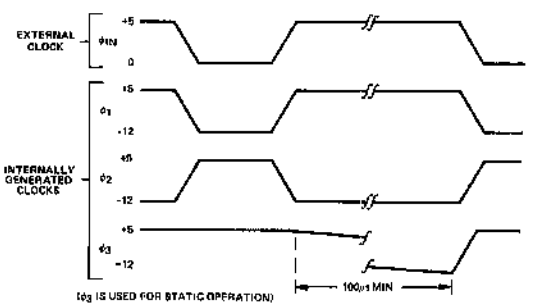


Note: When using 7400 series data, recirculate and clock drivers, connect 10k resistor from driver output to V_{CC}. This insures an adequate "1" level input for the MOS register. See page 13 of MOS Handbook.

SCHEMATIC DIAGRAM

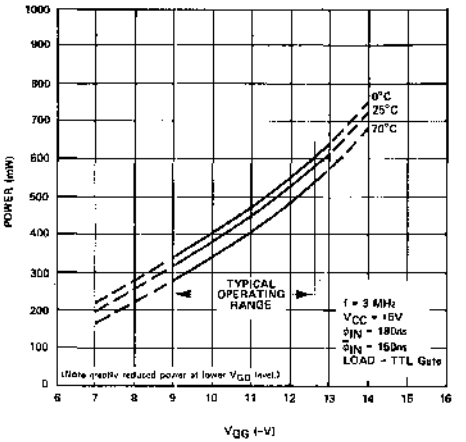


CLOCKING WAVEFORMS

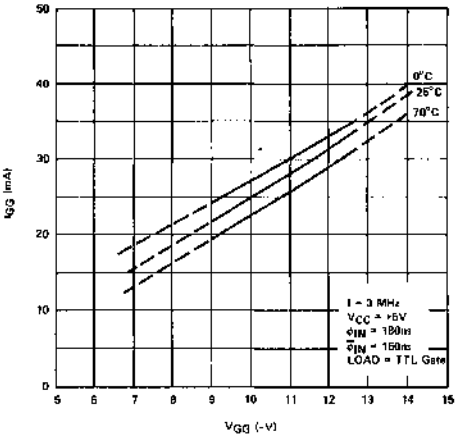


CHARACTERISTIC CURVES

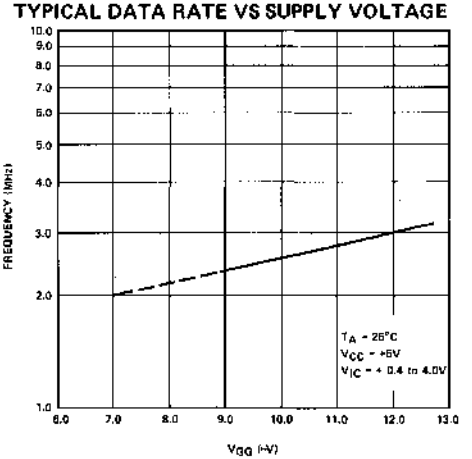
POWER DISSIPATION VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE

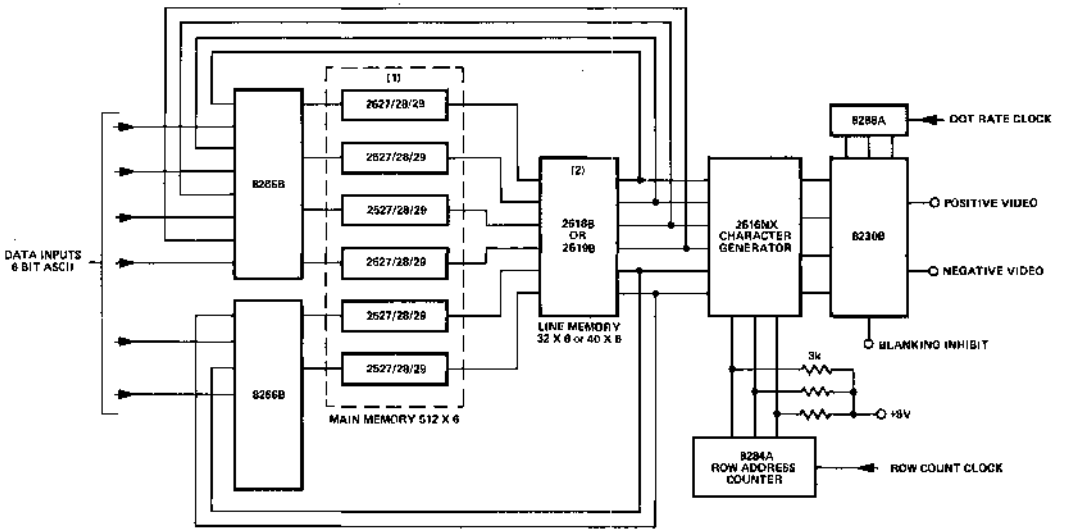


TYPICAL DATA RATE VS SUPPLY VOLTAGE



APPLICATIONS INFORMATION (Cont'd)

12 LINE, 32 OR 40 CHARACTER PER LINE CRT DISPLAY MEMORY SYSTEM



(1) Duals connected in series.
(2) These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.

signetics HIGH SPEED 512x8 STATIC READ-ONLY MEMORY | 2530

ADVANCE SPECIFICATION | **SILICON GATE MOS 2500 SERIES**

DESCRIPTION

The 2530 is a high speed 4,096-bit Static Read-Only Memory available in a 512x8 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. Two OUTPUT ENABLES control the eight output devices without affecting address circuitry.

FEATURES

- 512x8 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- STATIC OPERATION
- ADDRESS LATCHES
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = −12V
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

MICRO-PROGRAMMING
CODE-CONVERSION

BIPOLAR COMPATIBILITY

All inputs of the 2530 can be driven directly by standard bipolar integrated circuits, (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

STANDARD TRUTH TABLES

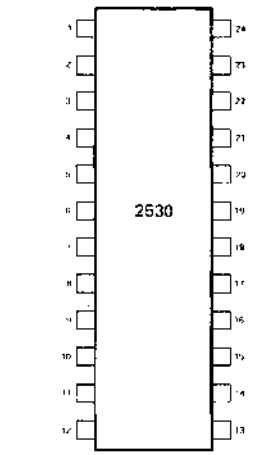
The 2530NX/CM3530 is an ASCII-EBCDIC and EBCDIC-ASCII code converter. Use this device for evaluation or for applications requiring this conversion. Other standards will be announced as they become available.

PART IDENTIFICATION

PART	OP. TEMP. RANGE	PACKAGE
2530N	0-70°C	24-Pin Silicone DIP
2530I	0-70°C	24-Pin Ceramic DIP

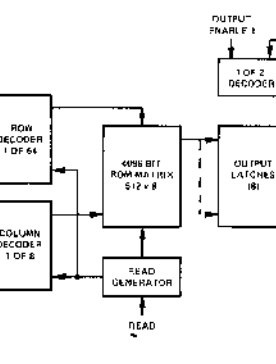
PIN CONFIGURATION (Top View)

N/I PACKAGE



1.	Output 6	24.	V_{CC}
2.	Output 7	23.	Output 5
3.	Output 8	22.	Output 4
4.	V_{DD} (Gnd)	21.	Output 3
5.	Address 1	20.	Output 2
6.	Address 2	19.	Output 1
7.	Address 3	18.	$\overline{\text{Read}}$
8.	Output Enable 1	17.	NC
9.	Output Enable 2	16.	Address 9
10.	Address 4	15.	Address 8
11.	Address 5	14.	Address 7
12.	V_{GG}	13.	Address 6

BLOCK DIAGRAM



CUSTOM TRUTH TABLES

See page 7-196.

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70°C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A=0° to +70°C, V_{CC}= +5V; V_{GG}= −12V ±5%; unless otherwise noted. (See notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		30	45	mA	(8)
I_{GG}	V_{GG} Power Supply Current		30	45	mA	(8)
V_{IL}	Input Logic "0"	-5		1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

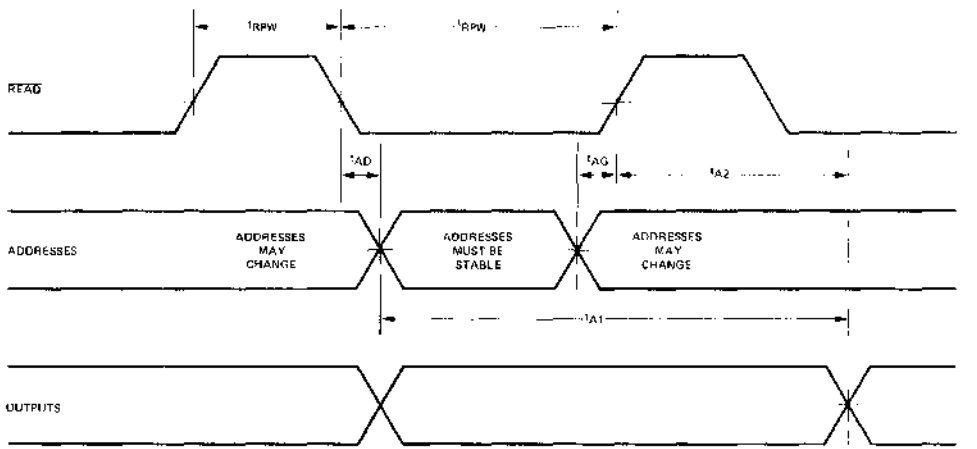
T_A = 0°C to 70°C; V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output Logic "zero"			0.8	V	One TTL Load
V_{OH}	Output Logic "one"	3.0			V	One TTL Load
t_{RPW}[11]	Read Pulse Width	250	200		ns	
$t_{\overline{RPW}}$[10]	$\overline{\text{Read}}$ Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (12)			50	ns	
t_{AG}	Address-Read Pulse Gap (12)			50	ns	
t_{A1}	Address to Output Delay		625	700	ns	(9)
t_{A2}	End of $\overline{\text{Read}}$ Pulse to Output Delay		200	250		(9)
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p V_{IN} = V_{CC}
t_{OE}	Output Enable to Output Delay		100	250	ns	

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs Open, t_{RPW} = 250ns, $t_{\overline{RPW}}$ = 500ns.
9. t_A = 0°C to +70°C
10. During $t_{\overline{RPW}1}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
11. During $t_{\overline{RPW}1}$ addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{READ}}$ pulse. After t_{A2}, data appears at the output terminals.
12. Addresses must be stable within 50ns after the $\overline{\text{READ}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{READ}}$ line goes high.

TIMING DIAGRAM



Note: All times measured from 50% points, for all input waveforms tr = t_f<10nsec

signetics

QUAD 80-BIT STATIC SHIFT REGISTER | 2532

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2532 Static Shift Register consists of enhancement mode P-Channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all four registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low. When the Recirculate control is at a logic "1", data recirculates and is continuously available at the output, data input is inhibited. With the Recirculate control is at a logic "0", data is entered.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- RECIRCULATE PATH ON CHIP
- DC TO 2.5 MHz OPERATION GUARANTEED
- LOW POWER (TYPICALLY 400 μW/BIT)
- PIN-FOR-PIN REPLACEMENT FOR (DYNAMIC) MK1007P AND TMS3409
- POWER SUPPLIES +5V AND −12V

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
DIGITAL FILTERING

SPECIAL FEATURES

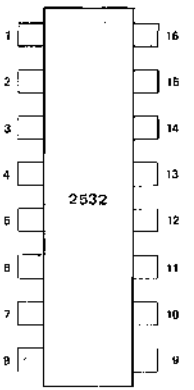
The three clock phases used by the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL logic level input.

BIPOLAR COMPATIBILITY

All inputs of these registers, including the clock can be driven directly by bipolar TTL/DTL integrated circuits without external components. Outputs are push-pull operating between 0V and +5V and provide a sink current of 1.6mA for one TTL fanout.

PIN CONFIGURATION (Top View)

B PACKAGE



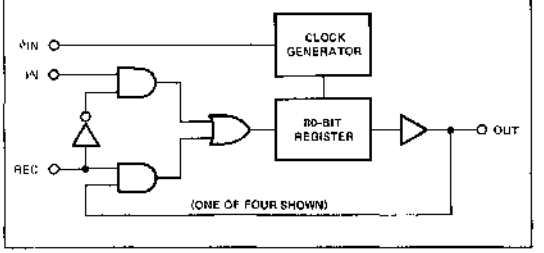
1.	OUT 1	16.	V_{CC}
2.	Recirculate 1	15.	IN 4
3.	IN 1	14.	Recirculate 4
4.	OUT 2	13.	OUT 4
5.	Recirculate 2	12.	V_{GG}
6.	IN 2	11.	ϕ IN
7.	OUT 3	10.	IN 3
8.	V_{DD} (Ground)	9.	Recirculate 3

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	"0" is Written
0	1	"1" is Written
1	0	Recirculate
1	1	Recirculate

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



PART IDENTIFICATION

PART NUMBER	BIT LENGTH	PACKAGE
2532B	Quad 80	16-Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C	Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V
Storage Temperature	-65°C to +150°C		
Package Power Dissipation at T_A = 70°C	640 mW		

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		6	10	mA	Continuous Operation F = 2.5 MHz, T_A = 25°C Outputs Open
I_{CC}	Power Supply Current		12	20	mA	
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage			1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

AC CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = +5V(8); V_{GG} = -12V + 5%, V_{IC} = 0.4 to 4.0V

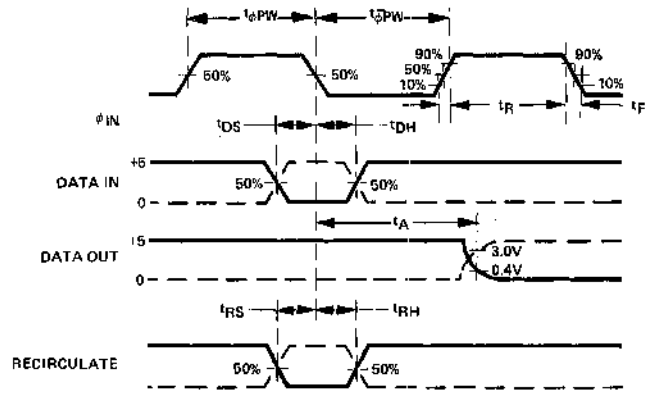
(CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL Gate.)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3.0	1.5	MHz	
$t_{\phi PW}$	Clock Pulse Width	0.18		100	μs	
$t_{\overline{\phi}PW}$	$\overline{\text{Clock}}$ Pulse Width	0.22		DC	μs	
t_R,t_F	Clock Pulse Transition			5	μs	
t_{DS}	Data Set-up Time	120			ns	
t_{DH}	Data Hold Time	0			ns	
t_A	Clock to Data Out Delay			400	ns	I_{OL} = 1.6mA
t_{RS}	Recirculate Set-up Time	150			ns	
t_{RH}	Recirculate Hold Time	0			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I_L = 1.6mA)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	4.0			V	1 TTL load (I_I = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	4.0			V	

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

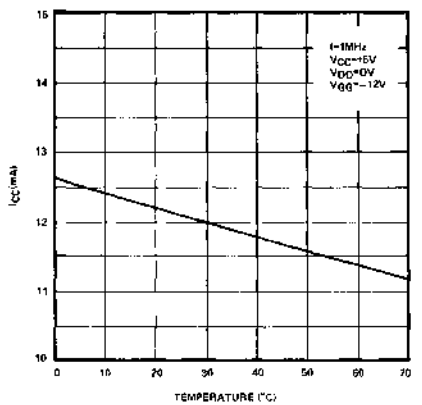
TIMING DIAGRAM



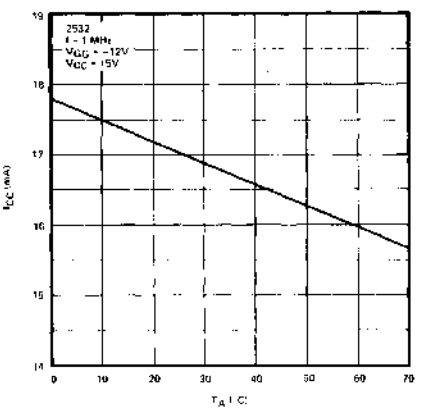
t_R = t_F < 10 NSEC FOR ALL INPUTS

CHARACTERISTIC CURVES

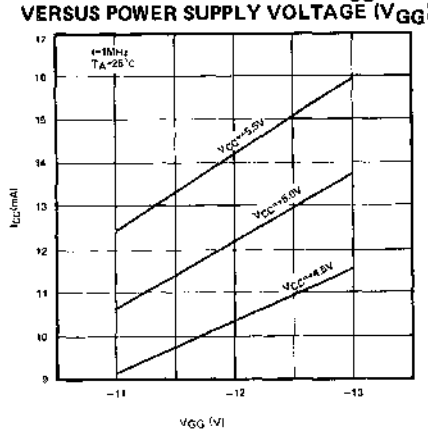
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



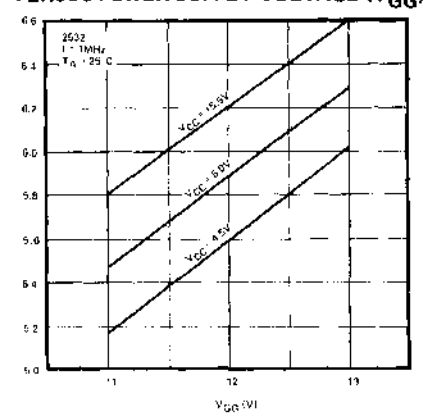
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{CC}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})

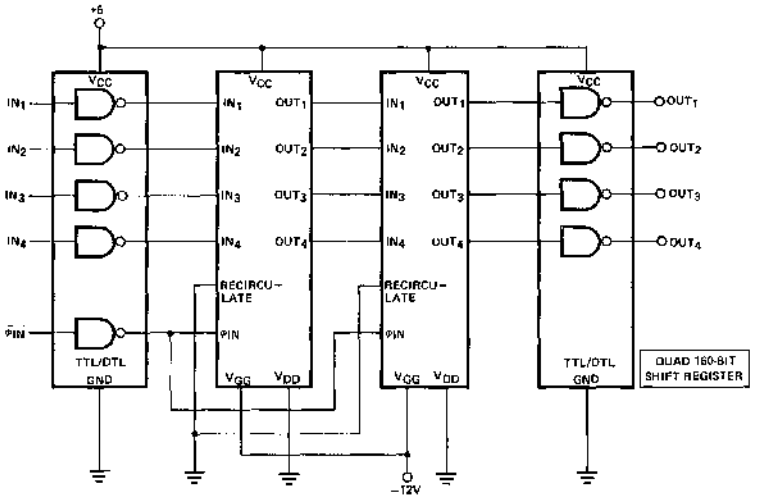


POWER SUPPLY CURRENT (I_{GG}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



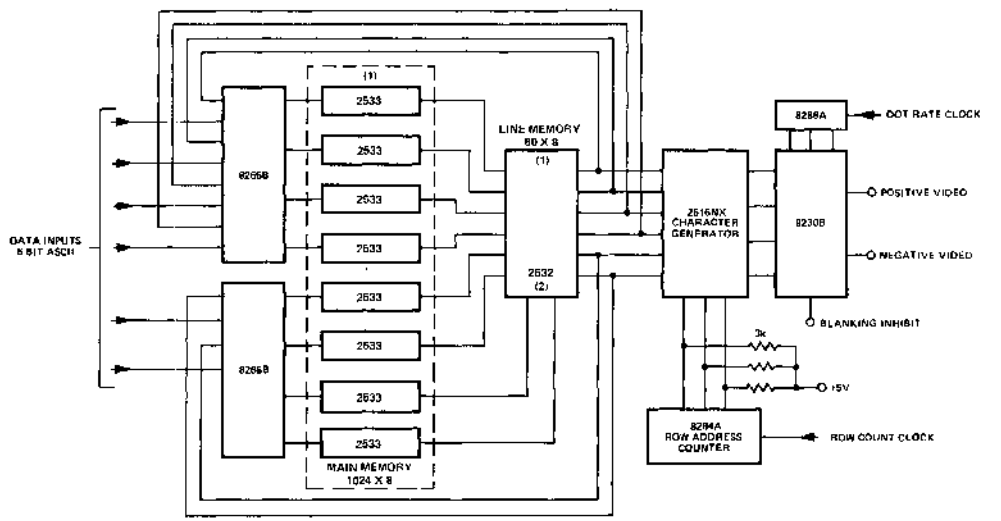
APPLICATIONS INFORMATION

DTL/TTL – MOS – MOS – DTL/TTL INTERFACING



NOTE: All unused inputs must be tied to a "1" or a "0", i.e., MOS inputs cannot be left floating.

12 LINE, 80 CHARACTER PER LINE CRT DISPLAY MEMORY SYSTEM



(1) These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.

signetics

1024-BIT STATIC SHIFT REGISTER | 2533

PRELIMINARY SPECIFICATIONS

DESCRIPTION

The Signetics 2533 Static Shift Register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

The 1024-bit register is equipped with two data inputs together with a "Stream Select" control to facilitate external recirculation.

The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- DC TO 1.5MHz GUARANTEED
- LOW POWER (TYPICALLY 250μW/BIT)
- POWER SUPPLIES +5V AND −12V
- 8-PIN DIP
- STREAM SELECT FOR EASY RECIRCULATION

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH – LINE AND PAGE
DELAY LINES
DRUM MEMORY REPLACEMENT

SPECIAL FEATURES

The three clock phases used in the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

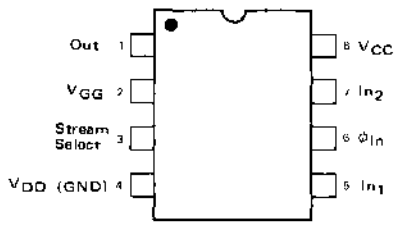
Recirculation of data in the 2533 is accomplished by simply jumpering the output back to In 2. The stream select control then becomes a Data Entry/Recirculate Control.

BIPOLAR COMPATIBILITY

All inputs of this register, including the clock, can be driven directly by bipolar TTL/DTL integrated circuits without external components. Each input is equipped with an internal pull-up resistor to enhance the "1" level of the TTL driver. The output is push-pull, operating between 0V and +5V, and provides a sink current of 1.6mA for one TTL fanout.

PIN CONFIGURATION: (Top View)

"V" PACKAGE

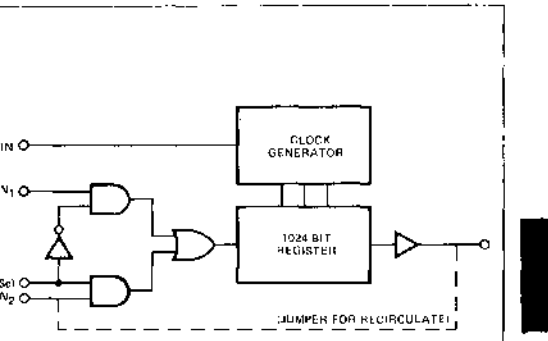


TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1
1	IN 2

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2533 V	1024	8-Pin DIP

MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (Note 2)	535mW @ T_A >25°C
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to −20V

DC CHARACTERISTICS

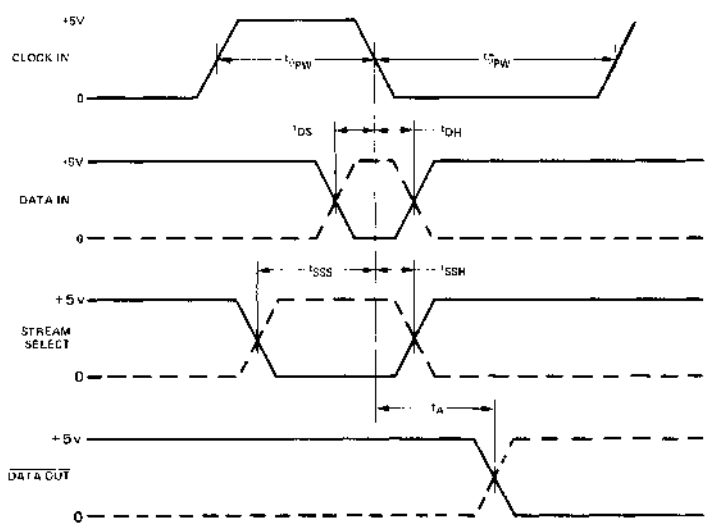
(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{GG} = −12V ±5% unless otherwise noted.)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 0, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{CC}	Power Supply Current		16	30	mA	Continuous Operation
I_{GG}	Power Supply Current		5.0	7.5	mA	F = 1.5MHz
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = +5V
V_{IH}	Input "High" Voltage	3.2			V	V_{CC} = +5V
V_{ILC}	Clock Input "Low" Voltage			0.8	V	V_{CC} = +5V
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	V_{CC} = +5V

NOTES.

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated corresponding to a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at 125°C and nominal supply voltages.

TIMING DIAGRAM

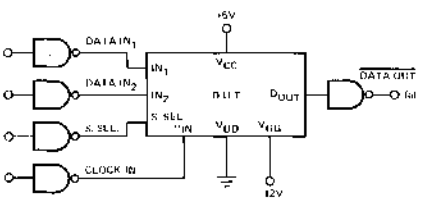


NOTE: Times measured at 50% points with input tr, tf ≤ 10ns.

AC CHARACTERISTICS V_{CC} = +5V ± 5%; V_{GG} = -12V ± 5%; T_A = 0° to +70°C

SYMBOL	TEST	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Frequency	Clock & Data Rep Rate	DC	2	1.5	MHz	
$t_{\phi PW}$	Clock Pulse Width	.350		100	μs	
$t_{\overline{\phi} PW}$	Clock Pulse Width	250		DC	ns	
t_r, t_f	Clock Pulse Transition			1	μs	
t_{DS}	Data Write Set-Up Time	50			ns	
t_{DH}	Data to Clock Hold Time	50			ns	
t_A	Clock to Data Out Delay		200	400	ns	I_{OL} = 1.6mA
t_{SSH}	Stream Select Hold Time	50			ns	
t_{SSS}	Stream Select Set-Up Time	80			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz, V_{IN} = V_{CC} V_{AC} = 25mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz, V_{OUT} = V_{CC} V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz, V_ϕ = V_{CC} V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I=1.6mA)
V_{OH}	Output "High" Voltage	2.4	3.5		V	1 TTL load (I=-100μA)

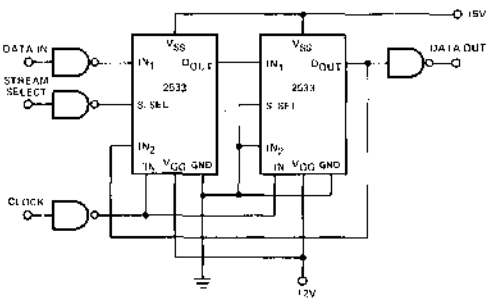
A.C. TEST SETUP



NOTES:
Measure T_A between device input and point (a).
Gates are standard 8800 or 7400.

APPLICATIONS INFORMATION

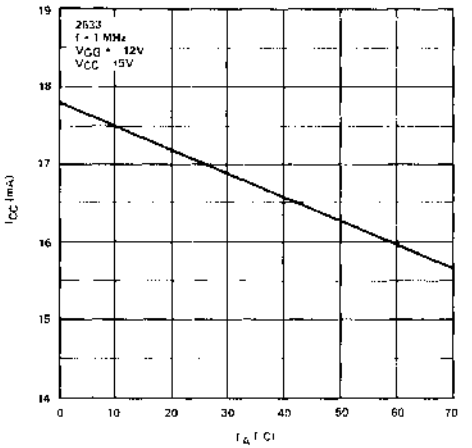
2048-BIT STORAGE REGISTER WITH RECIRCULATE



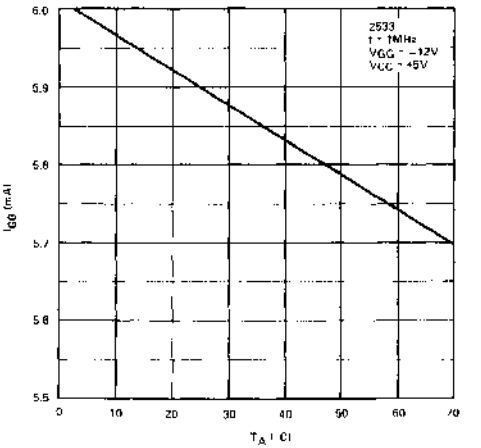
NOTE.
Gates are standard DTL or TTL.

CHARACTERISTIC CURVES

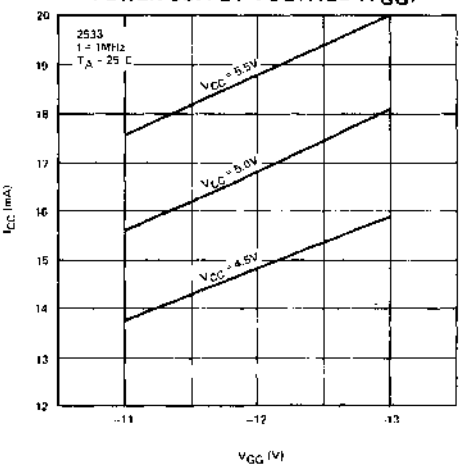
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



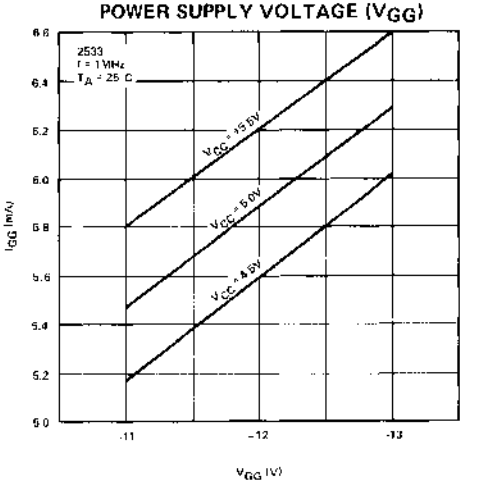
POWER SUPPLY CURRENT (I_{GG}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{CC}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



POWER SUPPLY CURRENT (I_{GG}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



signetics

UNIVERSAL ASYNCHRONOUS FIRST-IN, FIRST-OUT BUFFER REGISTER 2535

PRELIMINARY SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2535 is a P-Channel MOS asynchronous buffer memory consisting of 32 8-bit words. Both input and output can be either serial or parallel with a data rate of DC to 1 MHz in either mode of operation.

The register is designed so that information entered at the input will "fall through" to the lowest unoccupied location. Input and output may be accessed asynchronously. Control logic provides flag signals indicating presence of data and availability status of empty storage locations.

The 2535 may be expanded in either the bit or word direction. All inputs and outputs are directly DTL/TTL compatible.

FEATURES

- ASYNCHRONOUS LOAD AND DUMP
- 32 WORD BY 8-BIT ELASTIC STORAGE
- DC TO 1 MHz OPERATION
- SERIAL OR PARALLEL OPERATION
- TTL COMPATIBLE
- 28-PIN DIP PACKAGE
- V_{CC} = +5 V, V_{GG} = −12 V

APPLICATIONS

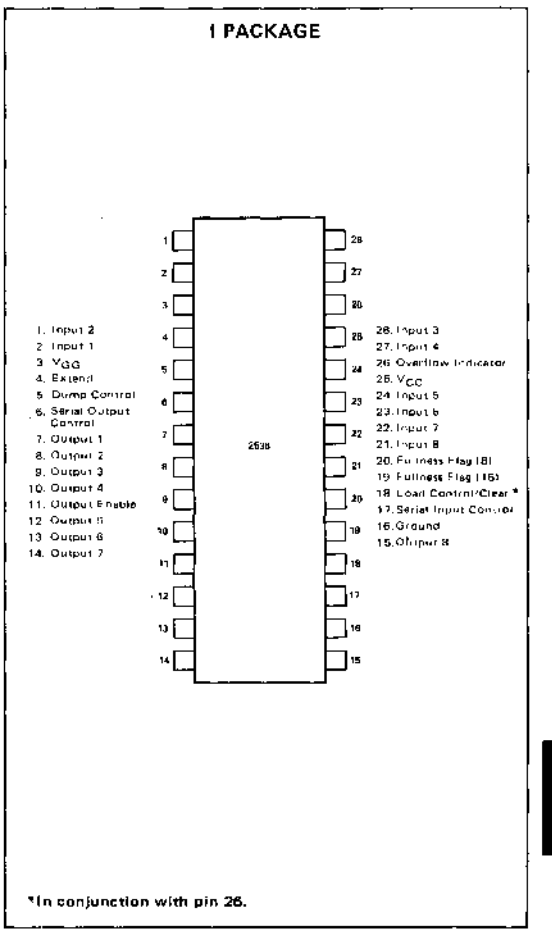
INTERFACE BETWEEN INDEPENDENTLY CLOCKED SYSTEMS
KEYBOARD TO LINE BUFFER MEMORY
DISC AND TAPE BUFFER MEMORIES
DATA CONCENTRATORS
DATA "SILO'S"
BIT RATE SMOOTHING
MODEMS
CPU/TERMINAL BUFFERING

BIPOLAR COMPATIBILITY

All inputs of the 2535 can be driven directly from TTL output levels. Outputs will sink and source sufficient current for one TTL fan-out.

PIN CONFIGURATION (TOP VIEW)

1 PACKAGE



*In conjunction with pin 26.

PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP. RANGE
2535I	28-Pin Ceramic DIP	0–70°C

MAXIMUM GUARANTEED RATINGS[1]

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Package Power Dissipation[2] @ T_A 70°C	3.13 W
Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to −20 V

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V (8), V_{DD} = GND, V_{GG} = −12 V ±5% unless otherwise noted. (Notes 4,5,6,7,8)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Leakage			500	na	V_{in} = GND
I_{LO}	Output Leakage (Tri-State Outputs)			500	na	V_{out} = Chip Enable = GND
V_{IH}	Input High Level Voltage (all inputs)	V_{CC} −1.5		V_{CC} +0.3	V	
V_{IL}	Input Low Level Voltage (all inputs)			V_{CC} −3.8	V	
V_{OH}	Output High Voltage (all outputs)	V_{CC} −2.0			V	I_{OH} = 2.6 mA (source)
V_{OL}	Output Low Voltage (all outputs)			0.4	V	I_{OL} = 1.6 mA (sink)
C_{IN}	Input Capacitance (any input)		5	10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25 mVp-p
C_{OUT}	Output Capacitance (any output)		5	10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25 mVp-p
I_{CC}	Power Supply Current		60		mA	Outputs open, Output Enable = 5 V
I_{GG}	Power Supply Current		10		mA	Outputs open, Output Enable = 5 V

AC CHARACTERISTICS

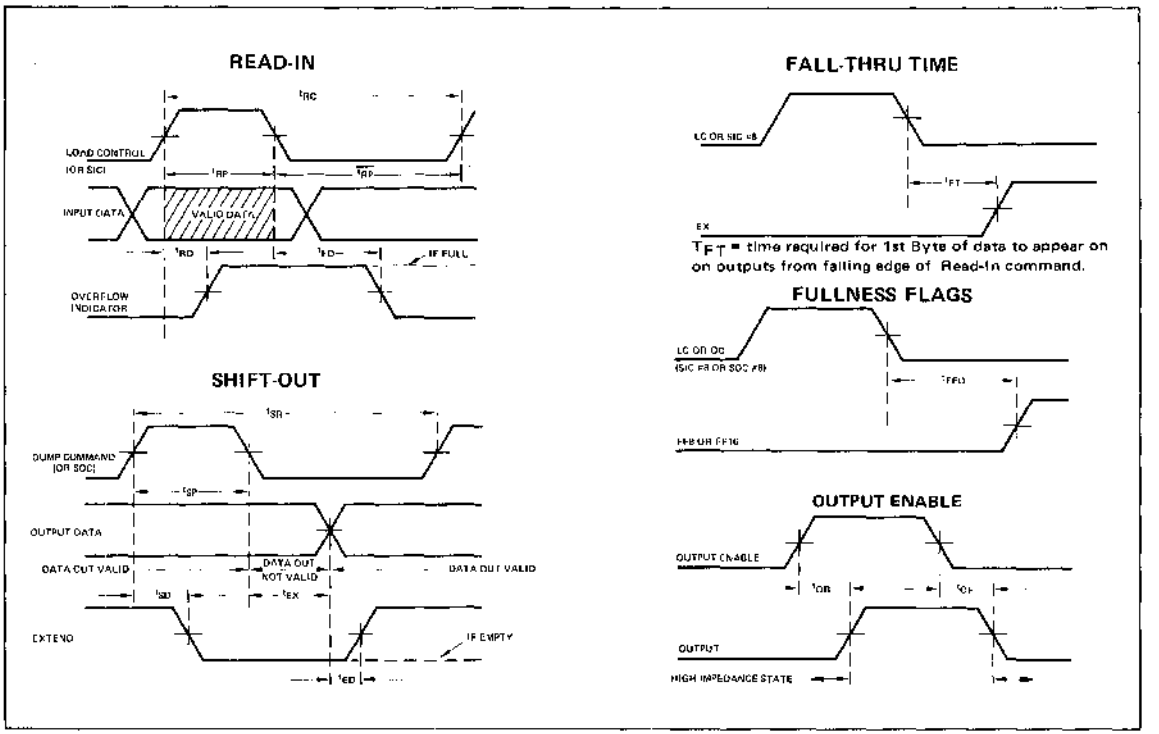
T_A = 0°C to 70°C, V_{CC} = 5 V (8), V_{DD} = GND, V_{GG} = −12 V ±5% unless otherwise noted. (Notes 4,5,6,7,8)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}	Read-In Cycle Time	1			µs	
t_{RP}	Read-In Pulse Width	200			ns	
$\overline{t_{RP}}$	Read-In Pulse Width	400			ns	
t_{RD}	Delay from Read-In Rising Edge Time			200	ns	1 TTL Load shunted by 20 pF
t_{FD}	Delay from Read-In Falling Edge Time			350	ns	1 TTL Load shunted by 20 pF
t_{RD}	Delay from Read-In Rising Edge Time			120	ns	MOS Loading Equivalent to 20 pF
t_{FD}	Delay from Read-In Falling Edge Time			275	ns	MOS Loading Equivalent to 20 pF
t_{SR}	Shift-Out Cycle Time	1			µs	
t_{SP}	Shift-Out Pulse Width	200			ns	
t_{SD}	Delay from Shift-Out Rising Edge			200	ns	1 TTL Load shunted by 20 pF
t_{EX}	Extend Time			500	ns	1 TTL Load shunted by 20 pF
t_{SD}				130	ns	MOS Loading Equivalent to 20 pF
t_{EX}				375	ns	MOS Loading Equivalent to 20 pF
t_{ED}	Data Out to Extend Delay	0			ns	All Data Outputs & Ex with either TTL or MOS loading but not mixed loading
t_{FFD}	Fullness-Flag Delay Time			800	ns	1 TTL Load shunted by 20 pF
t_{OR}	Delay from Output Enable Rising Edge			500	ns	
t_{OF}	Delay from Output Enable Falling Edge			500	ns	
t_{FT}	Fall-Thru Time			2	µs	1 TTL Load with 20 pF shunt capacity

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 48°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts

TIMING DIAGRAMS



CIRCUIT DESCRIPTION

INTERNAL ORGANIZATION

The Block Diagram in Figure 1 shows how the data is moved and controlled within the FIFO. The input register accepts either parallel or serial data. Input data is written into the storage array in a location specified by the Write Address Counter. At the same time, the Available Storage Counter is incremented to indicate the fullness condition of the FIFO.

The current output byte is automatically available at the output register. Data may be extracted from the register in parallel or serial form. After the current byte of data is used, the next output byte is read from the storage array at the location specified by the Read Address Counter. At the same time, the Available Storage Counter is decremented to maintain the proper fullness indication.

Two bits of the Available Storage Counter are supplied to the user as Fullness Flags. They indicate the buffer capacity status so that the empty or full conditions can be anticipated. FF8 indicates 1/4 full status, FF16 indicates 1/2 full status and when both flags are up the buffer is 3/4 full.

INPUT CONTROL

When parallel data is presented to the eight input lines, the Load Command (LC) is pulsed positive to enter the data into the buffer. The input data should remain valid for the width of the LC, and the LC should occur only when the Overflow Indicator (OI) output is low. The OI low signal

BLOCK DIAGRAM

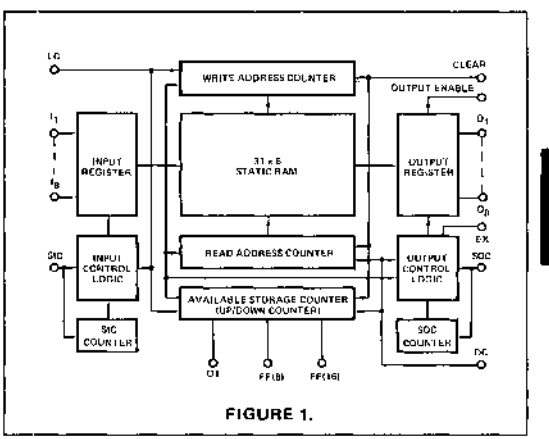


FIGURE 1.

indicates that the input is available for loading. After a delay following the leading edge of the LC, the OI will acknowledge the input by going high. If the OI remains high, then the buffer is full and no new data should be entered. When the OI goes low, the buffer is again available for loading.

Serial data is entered into the input register on Input 1. The Serial Input Clock (SIC) is used to shift the data into the register. OI acknowledges each SIC and the 8th SIC causes the byte in the input register to be inserted into the storage

If LC is pulsed during a serial entry before the 8th SIC, the byte actually entered into the buffer will be a logical OR of the partially entered serial data and the data at the parallel inputs. Bit positions in the input register that have not been shifted into will contain logical zeros.

OUTPUT CONTROL

When a byte is available in the buffer, it falls through to the output register and is available on the output pins (assuming the Output Enable signal is on). The Extend (EX) signal goes high to indicate that data is available at the output. When the using system is ready for the next byte, it should pulse the Dump Command (DC) line. EX will then go low until the next byte is available. EX stays low if the FIFO is empty.

Serial data is shifted from the output register on Output 8. The Serial Output Clock (SOC) is used to shift the data out of the register and EX responds to each clock pulse. The 8th SOC causes the output control logic to retrieve the next output byte and insert it into the output register.

If DC is pulsed during serial extraction before the 8th SOC, the next output byte is inserted into the output register and the remaining partially shifted data is lost. As the output register is shifted, it is filled with logical zeros.

BUFFER STORAGE

The first byte inserted into an empty buffer falls all the way through directly to the 8-bit output register. Succeeding input bytes are written into a random access memory array with a capacity of 31 x 8. The array is designed so that it may be addressed at different locations simultaneously. In that way, data may be inserted and removed at the same time. The Write Address Counter controls the locations for storing input data and the Read Address Counter controls the locations from which data is extracted for the output. Both counters are implemented as 31-bit shift registers that move a single bit along their length to directly select the desired word lines in the storage array. This control approach eliminates binary decoding networks and is possible because both the read and write locations are always sequentially accessed.

The use of random access memory to implement the required storage means that the stored data need not be moved around internally. Only the counters that point to the data are manipulated in response to loading and dumping the FIFO. It also means that the fall-through time is minimized since new data in an empty buffer does not have to be shifted sequentially through the buffer before it is available.

RESET

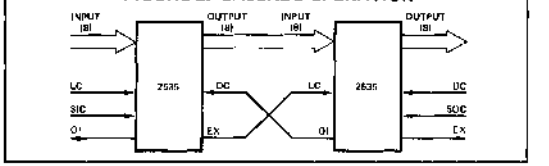
To clear the buffer to its empty state and thus reset all the control counters, two control signals are used. The OI signal, which is normally an output from the FIFO, should be held in a low state by the external reset logic. LC is then pulsed positive for at least 2 microseconds and returned low. The hold on OI is then released, concluding the reset operation.

EXPANSION

Increased FIFO capacity can be obtained by using multiple 2535's in serial/parallel organizations. Sixteen-bit words, for example, may be buffered by operating two eight bit streams in parallel. In applications where the timing is not critically fast, the LC, SIC, DC, and SOC may be tied together and operated in parallel, but only one each of the OI, EX, and FF signals should be used to control the data flow.

Cascaded operation of more than one FIFO allows expansion to any word depth that is a multiple of 32. The 2535 control signals may be inter-connected without intervening logic to form a FIFO of the desired depth. See Figure 2. Data will automatically fall through to the end of the chain.

FIGURE 2. CASCADE OPERATION



To control two cascaded devices using parallel data interconnection between them, it is only necessary to connect EX from the first device to LC of the second, and OI from the second device to DC of the first. The inputs to the first device and the outputs from the second device may then be operated in the normal modes. When data is entered into the two device combination it falls through to the output of the first device and causes the first EX to go high. The second device sees the EX as a LC, accepts the data, and responds with an OI signal which the first device sees as a DC. In this way the combination acts like one device with twice the capacity and twice the fall-through time of a single 2535.

FIFO USAGE

Asynchronous FIFO data stream buffering can come in handy in many situations. When a data sink, for example, requires data at a constant rate, the FIFO can provide the constant data stream while at the same time it can absorb data at highly variable rates from the data source.

The reverse situation can also apply. Consider a CRT terminal connected to a computer via a high speed data line. The terminal uses a large recirculating serial memory for data storage. A FIFO in the terminal can accept the constant speed data from the communication line, while at the same time it can wait for synchronization with the circulating memory and then dump a burst of data at high speed.

The circuitry required to implement a FIFO function using SSI and MSI logic can be considerable indeed. In addition to the cost of the logic replaced, the economic evaluation of the FIFO should consider inventory, ordering, testing, reliability, board space, production, design, and debugging problems associated with the old approach. In all of these areas the 2535 can provide significant advantages.

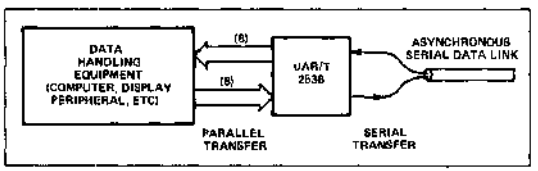
Signetics

UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UAR-T) 2536

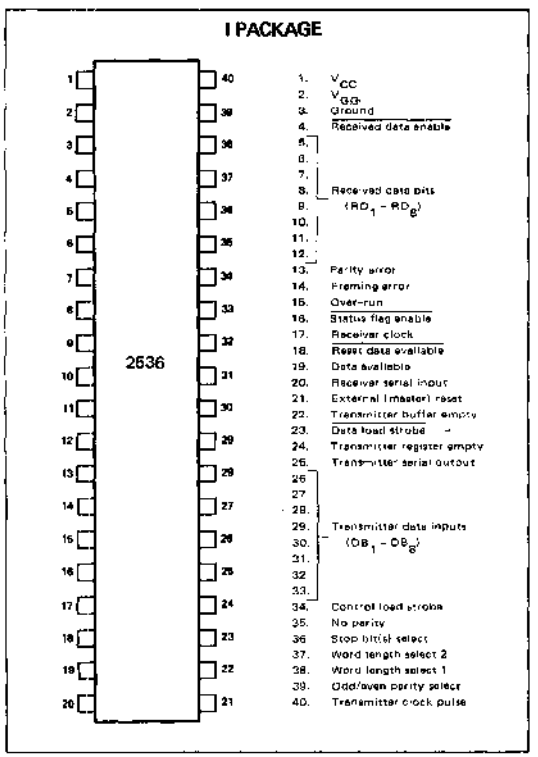
PRELIMINARY SPECIFICATION — SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2536 Universal Asynchronous Receiver-Transmitter is a general purpose, programmable MOS/LSI subsystem integrated on a single monolithic chip. The device can simultaneously convert asynchronous serial binary characters to a parallel format (receiver) and parallel binary characters to serial, asynchronous output (transmitter) with start, parity, and stop bits added or verified. Both receiver and transmitter are double buffered and fully compatible with bipolar logic. The UAR-T may be programmed as follows: the word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited; the parity may be even or odd; and the number of stop bits may be either one or two. The 2536 is pin compatible with the TMS 6010, AY-5-1012, TR-1402A, S1757 & COM2502.



PIN CONFIGURATION (Top View)



FEATURES

- DIRECTLY TTL/DTL COMPATIBLE - NO INTERFACING CIRCUITS REQUIRED
- FULL DUPLEX OR HALF DUPLEX OPERATION - TRANSMITS AND RECEIVES DATA SIMULTANEOUSLY OR ALTERNATELY (AT INDEPENDENT INFORMATION RATES)
- FULLY BUFFERED - ELIMINATES NEED FOR SYSTEM SYNCHRONIZATION: FACILITATES HIGH SPEED OPERATION.
- FULLY PROGRAMMABLE - EXTERNALLY SELECTABLE:
  - WORD LENGTH: 5, 6, 7, 8 DATA BITS
  - INFORMATION RATE - UP TO 20K BAUD
  - EVEN/ODD PARITY
  - PARITY INHIBIT
  - SINGLE OR DOUBLE STOP BIT GENERATION
- AUTOMATIC DATA STATUS GENERATION:
  - TRANSMISSION COMPLETE
  - TRANSMITTER BUFFER REGISTER EMPTY
  - RECEIVED DATA AVAILABLE
  - PARITY ERROR
  - FRAMING ERROR
  - OVERRUN ERROR
- THREE-STATE OUTPUTS, RESETABLE - BUSSING CAPABILITY:
  - DATA OUTPUTS
  - STATUS FLAGS
- INTERNAL PULL-UPS ON ALL INPUTS
- CLOCK BITS TO DATA BITS RATIO - 16 OPTIONS AVAILABLE- 32, (8, 4, 2)
- HIGH SPEED OPERATION - FROM D.C. TO 320KHz GUARANTEED
- START BIT VERIFICATION-MINIMIZES ERROR RATE
- STATIC LOGIC - STABLE
- STANDARD POWER SUPPLIES - +5V, −12V
- DUAL IN-LINE PACKAGE - CERAMIC

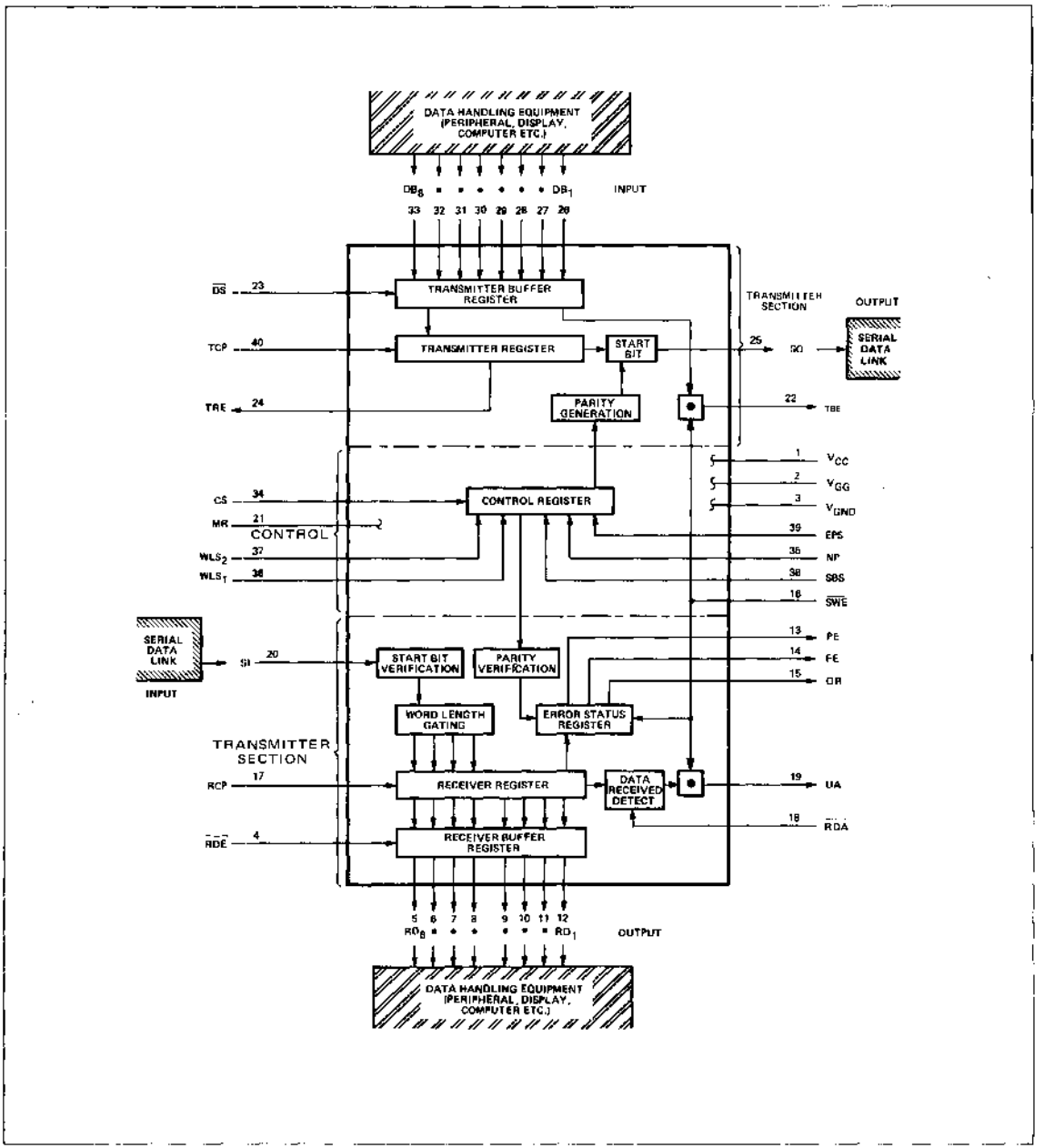
APPLICATIONS

PERIPHERALS	MULTIPLEXERS
TERMINALS	CONTROLLERS
PRINTERS	CARD AND TAPE READERS
MINI-COMPUTERS	KEYBOARD ENCODERS
MODEMS	REMOTE DATA ACQUISITION
CONCENTRATORS	SYSTEMS

PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP RANGE
2536I	40-Pin Ceramic DIP	0-70°C

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

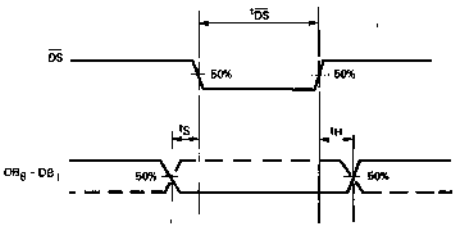
		Package Power Dissipation (2) @T_A = 70°C	3.0W(14)
Operating Ambient Temperature	0°C to 70°C	Input (3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V
Storage Temperature	-65°C to +150°C		

DC CHARACTERISTICS

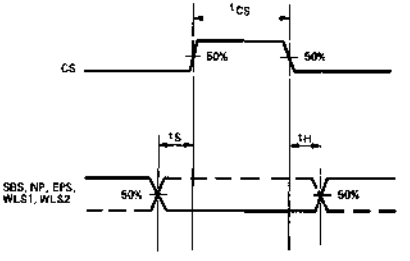
T_A = 0°C to 70°C, V_{CC} = 5V (8), V_{DD} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7, 8)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Input "High" Voltage (9)	3.2		5.3	V	
V_{IL}	Input "Low" Voltage			1.05	V	
$V_{IH\phi}$	Clock Input "High" Voltage (9)	3.2		5.3	V	
$V_{IL\phi}$	Clock Input "Low" Voltage			1.05	V	
I_{IH}	Input "High" Current			10	ua	V_{IN} = 5.0V
I_{IL}	Input "Low" Current			1.6	ma	V_{IN} = 0V
$I_{IH\phi}$	Clock Input "High" Current			10	ua	V_{IN} = 5.0V
$I_{IL\phi}$	Clock Input "Low" Current			1.6	ma	V_{IN} = 0V
I_{CC}	V_{CC} Supply Current		20		ma	All Inputs Logic "High"
I_{GG}	V_{GG} Supply Current		10		ma	All Inputs Logic "High"
P_D	Power Dissipation		200		mW	All Inputs Logic "High"

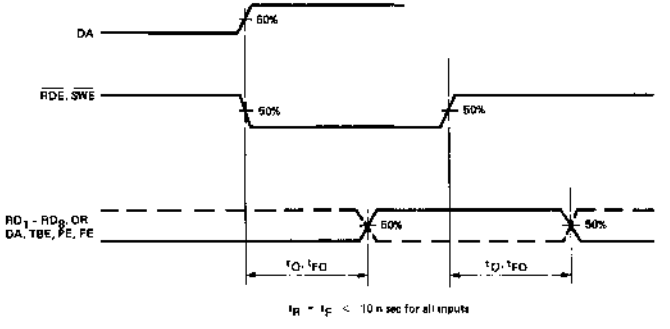
TIMING DIAGRAM AND VOLTAGE WAVEFORMS



TRANSMITTER DATA INPUT LOAD CYCLE



CONTROL REGISTER LOAD CYCLE



OUTPUT DELAYS

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V(8), V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7, 8, 10, 11, 13)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
f_C	Clock Frequency (12)	DC	480	320	KHz	
BR	Baud Rate		30	20	kBaud	(Clock/Data ratio = 16)
$t_{PW\phi}$	Clock Pulse Width	1.5	1.0	100	us	
$t_{PW\overline{\phi}}$	$\overline{\text{Clock}}$ Pulse Width	1.5	1.0	DC	us	
$t_{\overline{DS}}$	$\overline{\text{Data}}$ Strobe Width	200			ns	
t_{CS}	Control Strobe Width	200			ns	
t_{MR}	Master Reset Pulse Width	1.0			us	
$t_{\overline{RDA}}$	Receiver Data Available Reset Pulse Width	300			ns	
$t_{\overline{RDE}}$	Receiver Data Enable Pulse Width	400			ns	
$t_{S\overline{WE}}$	Status Word Enable Pulse Width	400			ns	
t_{NP}	Parity Inhibit Pulse Width (11)	400			ns	
t_{EPS}	Even/Odd Parity Pulse Width (11)	400			ns	
t_{SBS}	Stop Bit Select Pulse Width (11)	400			ns	
T_{WLS}	Word Length Select Pulse Width (11)	400			ns	
t_S	Data and Control Set-up Time	10			ns	
t_H	Data and Control Hold Time	20			ns	
t_{RR}	Receiver Reset Delay (RDA to DA)		0.5		us	
t_{FO}	Flag Output Delay (SWE to Flag)	0.3			us	
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL Load (I_{OUT} = 1.6ma)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL Load (I_{OUT} = -100ua)
V_{OH2}	Output "High" Voltage Driving MOS	3.5	4.0		V	
t_{OL}	Receiver Output Logic "Low" Delay		300	500	ns	1 TTL Load
t_{OH}	Receiver Output Logic "High" Delay		300	500	ns	1 TTL Load
C_{IN}	Input Capacitance (all inputs)			10	pF	@1MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Input Capacitance			10	pF	@1MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 50° C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. The 2536 is equipped with an internal pull-up device on all input terminals to enhance the "1" level of driving TTL gate. The pull-up impedance is typically 10K ohms to V_{CC}.
10. Output load capacitance 20pF max.
11. Input rise and fall times 10ns. Output load is one standard TTL gate.
12. Clock frequency is 16 times Baud rate for a standard 2536.
13. NP, EPS, WLS1, WLS2, and SGS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.
14. Note that this figure is the maximum dissipation allowed in this package. Actual device power dissipation can be found in the D.C. Characteristics Table.

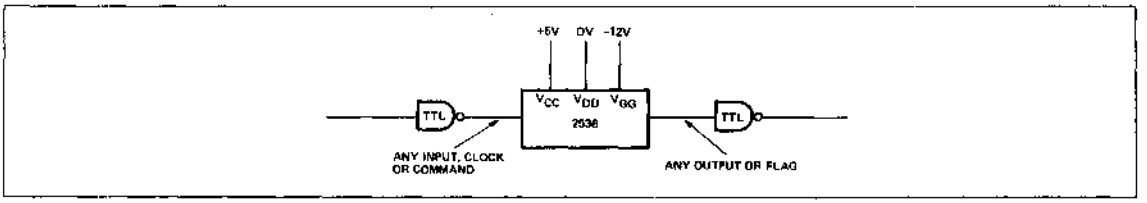
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	V_{CC} Power Supply	V_{CC}	+5V Supply
2	V_{GG} Power Supply	V_{GG}	-12V Supply
3	Ground	V_{GND}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" input enables the outputs (RD_8-RD_1) of the receiver buffer register.
5-12	Receiver Data Outputs	$RD_8 - RD_1$	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD_1. These lines have resettable three-state outputs; i.e., they have normal TTL output characteristics when $\overline{RDE}$ is "0" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be "bus" structured. Unused data output lines, as selected by WLS_1 and WLS_2, have a "0" output.
13	Receiver Parity Error	PE	This three-state output (enabled by "0" on $\overline{SWE}$) goes to a logic "1" if the received character parity bit does not agree with the selected parity.
14	Receiver Framing Error	FE	This three-state output (enabled by "0" on $\overline{SWE}$) goes to a logic "1" if the received character does not have a valid stop bit.
15	Receiver Over-Run Error	OR	This three-state output (enabled by "0" on $\overline{SWE}$) goes to a logic "1" if the previously received character is not read (DA output not reset with $\overline{RDA}$) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line enables three-state outputs (PE, FE, OR, DA, TBE) of the status buffer register.
17	Receiver Clock	RCP	Receiver clock line input. Frequency is 16 times (16X) the desired receiver baud rate. Other versions available on special order (contact Signetics) (32X, 8X, 4X, 2X).
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line to a "0".
19	Receiver Data Available	DA	This three-state output (enabled by "0" on $\overline{SWE}$ goes to a logic "1" when an entire character has been received and transferred to the receiver buffer register.
20	Receiver Serial Input	SI	This input accepts the serial bit input stream into receiver register at a point determined by the character length, parity, and the number of stop bits. A Mark (logic "1") to Space (logic "0") transition is required for initiation of data reception. A logic "1" must be present when data is not being received.
21	External (Master) Reset	MR	This line is strobed to a logic "1" to clear the logic after power turn-on. It resets all registers and sets the transmitter serial output line, SO and all three-state outputs to a logic "0".
22	Transmitter Buffer Empty	TBE	The transmitter buffer empty flag (enabled by "0" on $\overline{SWE}$) goes to a logic "1" when the transmitter buffer register has transferred its content to the transmitter register and may be loaded with a new character.
23	Transmitter Data Strobe	$\overline{DS}$	A "0" strobe on this line enters a character into the transmitter buffer register. A rising (positive) edge transition of that strobe transfers the character into the transmitter register if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is transferred simultaneously with the initiation of its serial transmission (start bit).

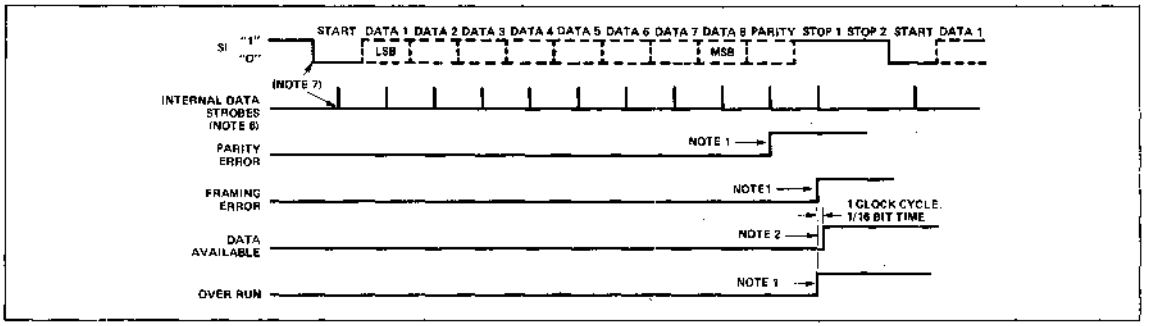
DESCRIPTION OF PIN FUNCTIONS (Cont'd)

PIN NO.	NAME	SYMBOL	FUNCTION
24	Transmitter End of Character	TRE	A logic "1" on this output indicates that the transmitter register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	Transmitter Serial Output	SO	The content of the transmitter register (start bit, data bits, parity bit, and stop bit(s)), are serially shifted out on this line. It will remain at logic "1" when no data is being transmitted. A start of transmission is defined as the transition from logic "1" to a logic "0" of the start bit.
26-33	Transmitter Data	DB_1 - DB_8	There are 8 data input lines (strobed by DS) available. Unused data input lines, as selected by WLS1 and WLS2, may be in either logic state. The LSB should always be placed on DB_1. A logic "1" input will cause a logic "1" output to be transmitted.
34	Control Strobe	CS	A "1" strobe on this line enters the control bits (EPS, NP, SBS, WLS2, and WLS1) into the control register. This line may be strobed or hard-wired to a logic "1" level.
35	Parity Inhibit	NP	A logic "1" on this line inhibits the parity generation and verification circuits. It clamps the PE line to a logic "0". The stop bit(s) will immediately follow the last data bit. If not used, this line must be tied to a logic "0".
36	Number of Stop Bits Select	SBS	This line selects the number of stop bits (logic "1") generated after a parity bit during transmission. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Data Bits/ Character Select	WLS1 WLS2	These two lines will be internally decoded to select either 5, 6, 7, or 8 data bits per character. WLS1 / WLS2 / Bits/Character 0 / 0 / 5 1 / 0 / 6 0 / 1 / 7 1 / 1 / 8
39	Odd/Even Parity Select	EPS	The logic level on this pin, in conjunction with the NP input, selects the t ype of parity mode which will be generated by the transmitter and checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock	TCP	Transmitter clock line input. Frequency is 16 times (16X) the desired baud rate. Note: other versions are available on special order (32X, 8X, 4X, 2X).

TTL INTERFACE CIRCUIT



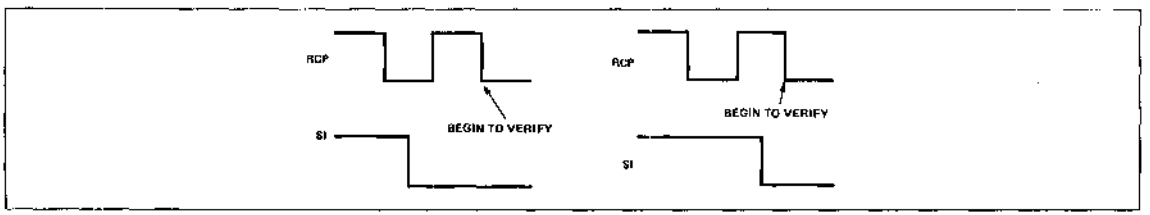
UAR-T RECEIVER OPERATION TIMING DIAGRAM



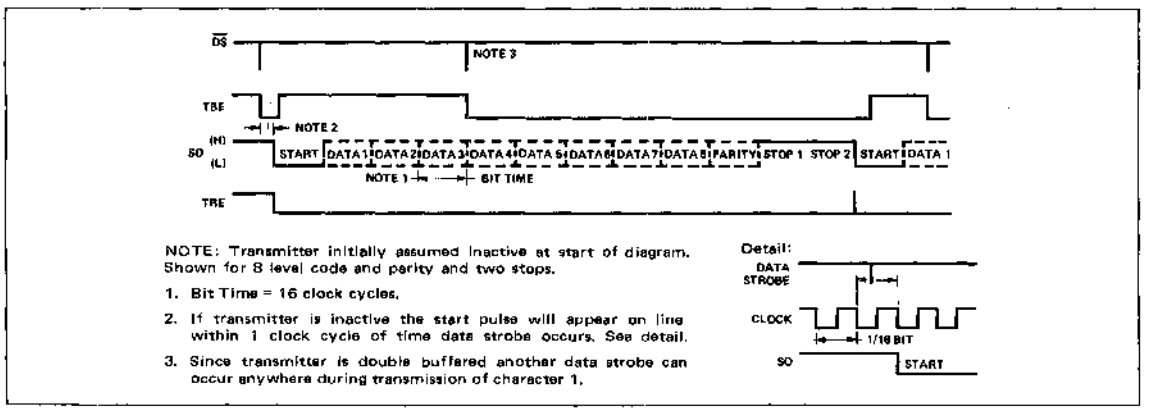
NOTES:

1. This is the time when the error conditions are detected, if error occurs.
2. Data available is set only when the received data PE, FE, OR has been transferred to the buffer registers.
3. All information is good in buffer register until date available tries to set for next character.
4. Above shown for 8 level coda parity and two stop for no parity stop bits follow data.
5. For all level codes, the data in the holding register is right justified; that is, LSB always appears in RD1 (Pin 12).
6. These data strobes are internally generated to sample at the center of a bit.
7. If the receiver serial input (SI) line remains "Spacing" (Logic "0") for 1/2 a bit time, a genuine start bit is verified. Should the line return to a "Marking" condition (logic "1") prior to a 1/2 of a bit time, the start bit verification process will be reset (invalid start bit). See Detail.

DETAIL



UAR-T TRANSMITTER OPERATION TIMING DIAGRAM



NOTE: Transmitter initially assumed inactive at start of diagram. Shown for 8 level code and parity and two stops.

1. Bit Time = 16 clock cycles.
2. If transmitter is inactive the start pulse will appear on line within 1 clock cycle of time data strobe occurs. See detail.
3. Since transmitter is double buffered another data strobe can occur anywhere during transmission of character 1.

Detail:

RECEIVER OPERATION

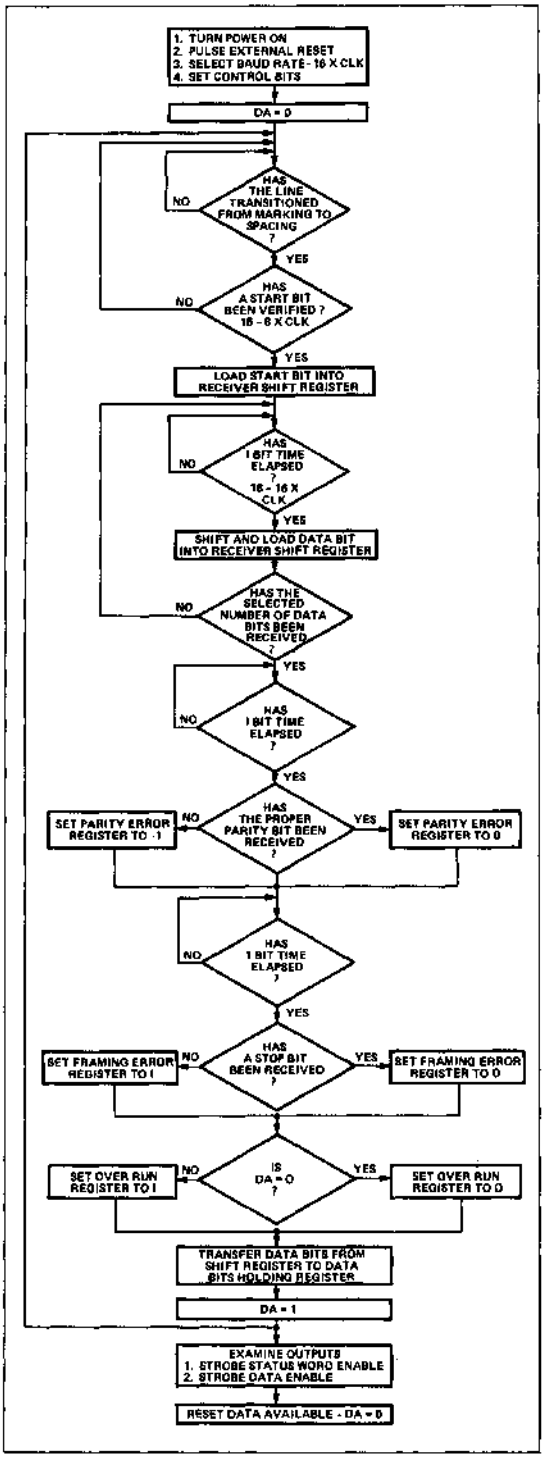
INITIALIZING

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to Spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (Marking to Spacing) when the 16X clock is in logic "1" state, the bit time for center sampling, will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception, and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected, the PE (parity error) will be set to a logic "0"

Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status buffer register will be set to a logic "1". If the DA signal is at a logic "0", the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.



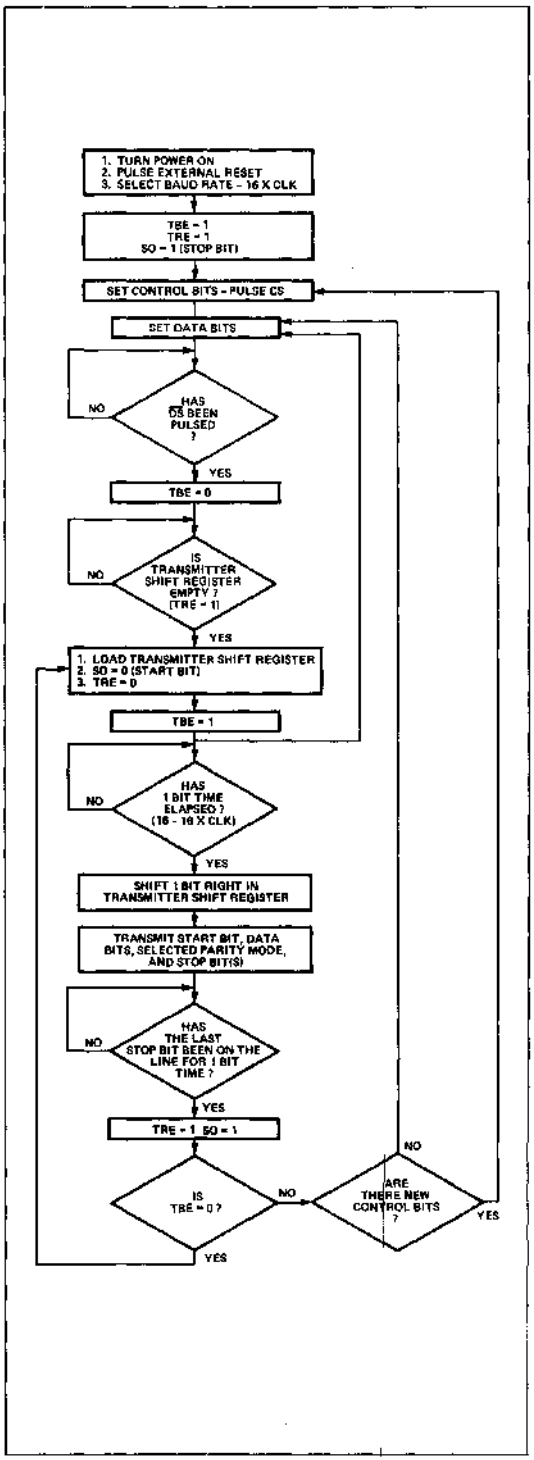
TRANSMITTER OPERATION

INITIALIZING

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBE, TRE, and SO to logic "1" (line is Marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed, the TBE signal will change from a logic "1" to a logic "0" indicating that the data bits buffer register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. When transmitter shift register is empty, data bits in the buffer register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and TRE going to a logic "0", and TBE will also go to a logic "1" indicating that the shifting operation is completed and that the data bits buffer register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits buffer register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, TRE will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBE is a logic "0" as was previously discussed.



Signetics

FULLY DECODED, 2048-BIT RANDOM ACCESS MEMORY 2548

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2548 2048x1 Dynamic Random Access Memory employs enhancement mode P-channel devices integrated on a single monolithic chip. The device is fully decoded and contains built-in refresh amplifiers. All address input data and control lines are directly TTL compatible. Clocking is performed by three high level (0V to -20V) nonoverlapping clock inputs. (Use Signetics N575 Clock Driver.) The output data line supplies a minimum "1" level output of 600μA. (Use Signetics 8T25 Sense Amplifier.)

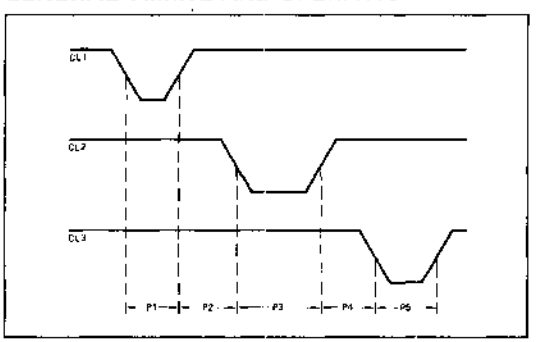
FEATURES

- HIGH STORAGE DENSITY
- READ ACCESS TIME 345ns MAX.
- READ/WRITE CYCLE TIME 560ns MAX.
- REFRESH PERIOD – 2mS FOR 0°C TO 70°C AMBIENT
- AUTOMATIC REFRESH OF A 64 BIT COLUMN DURING EACH READ
- LOW POWER DISSIPATION 150μW/BIT MAX. (AT 1.8MHz)
- STANDBY POWER 2μW/BIT MAX.
- STANDARD 22 PIN DIP PACKAGE, 400 MIL ROW SPACING
- V_{CC} = 5V, V_{BB} = 8.5V, V_{DD} = –15V
- ALL INPUTS EXCEPT CL1, CL2, CL3 ARE TTL COMPATIBLE
- ADDRESS AND CHIP SELECT INPUT LATCHES PROVIDED ON CHIP
- CHIP SELECT PERMITS SIMPLE MEMORY EXPANSION

APPLICATIONS

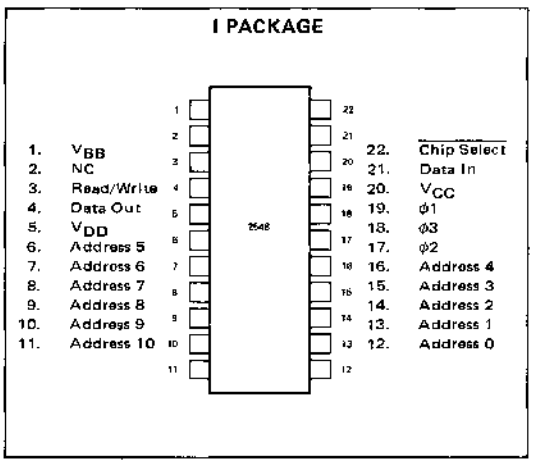
CORE MEMORY REPLACEMENT
DOUBLED STORAGE CAPACITY (OVER 1K RAMS)
BUFFER STORES
MAIN MEMORY

GENERAL TIMING AND OPERATION



PIN CONFIGURATION (TOP VIEW)

I PACKAGE



BIPOLAR COMPATIBILITY

All address lines, control lines and data input lines are directly TTL compatible and defined in positive logic. The three clocks require high level drivers. The data out line is a non-inverted current source output requiring a sense amplifier or high impedance gate. (Signetics N575 Clock Driver and 8T25 Sense Amplifier are recommended.)

GENERAL TIMING AND OPERATION

1. During period 1 internal nodes are precharged. The rising edge of CL1 (end of Period 1) clocks input address and CS data into storage elements.
2. During period 2 the row and column decoders select the desired bit.
3. During period 3 the information in the bit is exclusive OR'd with the selected information contained in the column inversion memory. The result is sent to the output. The output information is stable near the end of period 3.
4. During period 4 the write enable circuitry is activated. The internal data-in level is determined by exclusive OR'ing the actual input with the selected information contained in the column inversion memory.
5. If a write is desired during period 5, data is written into the selected bit. The information stored in all other bits sharing the same addressed column is inverted and refreshed. The appropriate bit of the column inversion memory is also inverted and refreshed.

   If a refresh is desired during period 5, the information stored in all bits sharing the same addressed column is inverted and refreshed. The appropriate bit of the column inversion memory is also inverted and refreshed.

PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP. RANGE
2548I	22-Pin Ceramic DIP (0.4")	0–70°C
2548XC	22-Pin Plastic DIP	0–70°C

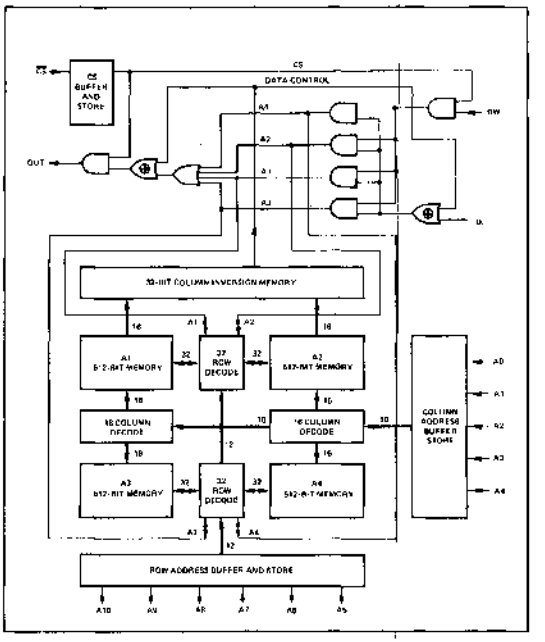
NOTE: "0" = 0 V, "1" = +5 V

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	−65°C to 150°C
All Input or Output Voltage with respect to the most positive supply V_{BB}	+0.3 V to −25 V
Supply Voltages with respect to V_{BB}	+0.3 V to −25 V
Package Power Dissipation at T_A = 25°C	800 mW

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. The V_{BB} supply should be applied at or before the V_{CC} supply.
3. t_r and t_f = 20ns for all inputs. All timing measurements are made at the 50% points.
4. Only CL1 and CL2 are required for a short read cycle. 60 ns after CL2 the next cycle can start. No refresh occurs when using short read cycles.

BLOCK DIAGRAM



DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V, V_{BB} = 8.5 V ±0.5 V, V_{DD} = −15 ±1 V unless otherwise noted.(2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LC}	Clock Load Current			5.0	μA	$V_{CLK} = V_{DD}$
I_{LI}	Input Load Current			1.0	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage Current			1.0	μA	$V_{OUT} = V_{DD}$, CL1 = V_{DD}, CL2 = V_{CC}, CL3 = V_{CC}
I_{DD}	Average Power Supply Current			10.0	mA	T_A = 25°C, T_{cyc} = 560 ns
I_{BB}	Average Power Supply Current			500.0	μA	T_A = 25°C, T_{cyc} = 560 ns
V_{IL}	Input Low Voltage	V_{DD} −1.0		V_{CC} −4.5	V	
V_{IH}	Input High Voltage	V_{CC} −1.5		V_{CC}	V	
V_{ILC}	Clock Input Low Voltage	-16		-14	V	
V_{IHC}	Clock Input High Voltage	V_{CC} −1.5		V_{CC}	V	
I_{OH}	Output High Source Current	0.6			mA	R_L = 1.1 K connected to 0 V
I_{OL}	Output Low Source Current			25.0	μA	R_L = 1.1 K connected to 0 V
C_{ADD}	Address Input Capacitance			5.0	pF	$V_{IN} = V_{CC}$, = 1 MHz
C_{CS}	$\overline{CS}$ Input Capacitance			5.0	pF	
C_{RW}	R/W Input Capacitance			5.0	pF	
C_{DI}	DI Input Capacitance			6.0	pF	
C_{CL1}	CL1 Input Capacitance			35.0	pF	
C_{CL2}	CL2 Input Capacitance			16.0	pF	
C_{CL3}	CL3 Input Capacitance			25.0	pF	
C_{OUT}	Output Capacitance			5.0	pF	$V_{CL1} = V_{DD}$, $V_{OUT} = V_{CC}$, $V_{CL2} = V_{CL3} = V_{CC}$, f = 1 MHz

AC CHARACTERISTICS [3]

$T_A = 0°C$ to $70°C$, $V_{CC} = 5$ V, $V_{BB} = 8.5$ V ±0.5 V, $V_{DD} = -15$ V ±1 V unless otherwise noted. [2]

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
General Memory Cycle Timing						
T_{REF}	Time Between Refresh			2.0	ms	
T_{1PW}	CL1 Pulse Width	75			ns	
T_{12}	CL1 to CL2 Gap	75			ns	
T_{2PW}	CL2 Pulse Width	240			ns	
T_{23}	CL2 to CL3 Gap	50			ns	
T_{3PW}	CL3 Pulse Width	70			ns	
T_{31}	CL3 to CL1 Gap	50			ns	
T_{AS}	Address & Chip Select Setup Time	40			ns	
T_{AH}	Address & Chip Select Hold Time	60			ns	
T_{OUT}	CL2 to Output Access Time	230			ns	$R_L = 1.1$ K, $C_L = 30$pF, $V_{REF} = 500\ \mu$A
T_{CYC}	Cycle Time	560			ns	
T_{SRC} [4]	Short Read Cycle Time	450			ns	
T_{21} [4]	CL2 to CL1 Gap (for SRC only)	60			ns	
Read/Refresh Cycle Timing						
T_{ACC1}	CL1 to Output Access	380			ns	$T_{1PW} + T_{12} + T_{OUT}$
T_{ACC1}	Address or Chip Select to Output	345			ns	$T_{AS} + T_{12} + T_{OUT}$
T_{RWS3}	Read Setup Time	60			ns	
T_{RWH3}	Read Hold Time	20			ns	
Read/Write Cycle Timing						
T_{RWS2}	Write Setup Time	0			ns	
T_{DS1}	Data High Setup Time	100			ns	
T_{DS0}	Data Low Setup Time	60			ns	
T_{DH}	Data Hold Time	20			ns	

GENERAL NOTES:

A. Everytime a column is accessed during a normal memory cycle (either a READ or a WRITE, but not a SHORT READ), all 64 bits in that column are refreshed.

B. Refreshing continues to occur even if the device is not selected ($\overline{CS}$ = "1").

C. When $\overline{CS}$ = "1" the Data In and Read/Write inputs are disabled so that no data can be written into the device. When $\overline{CS}$ = "1", the output of the device is left floating so that many device outputs can easily be OR'ed together.

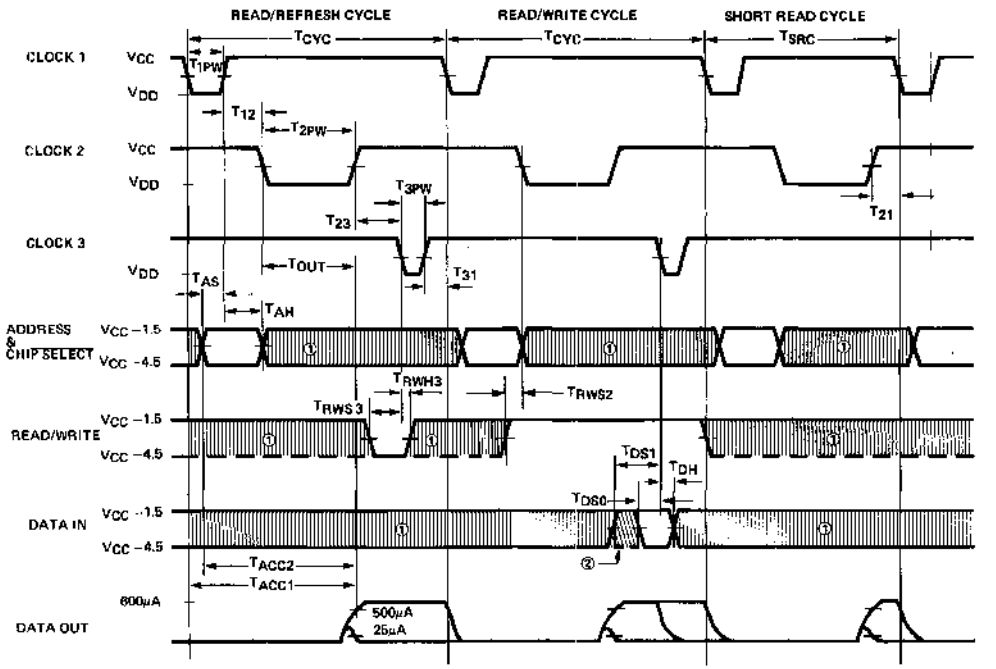
D. A_0 through A_4 are the column address lines. A_5 through A_{10} are the row address lines.

E. For proper refreshing, all column addresses (32 of them) must be selected at least once during every 2 ms period.

F. Inputs A_0 through A_{10} and $\overline{CS}$ are essentially clocked into the device on the rising edge of CL1. They are then held by internal latches for the duration of each memeory cycle.

G. The RAM is non-inverting such that data written in as a "1" (DI = "1") is read out as a positive current greater than 600 μA. Data written in as a "0" is read out as a very small current less than 25 μA.

TIMING DIAGRAM



NOTES:
1. Signal may change with no effect.
2. Data In can go low but cannot go high during this time.

signetics

8192- BIT HIGH SPEED STATIC READ-ONLY MEMORY 2580

PRELIMINARY SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2580 is a high speed 8,192 Static Read-Only Memory available in a 2048x4 organization. This device has TTL compatible inputs and outputs and requires +5V and -12V power supplies. A READ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. The outputs are enabled by a programmable four bit select code applied to four binary chip select terminals.

FEATURES

- 2048x4 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- STATIC OPERATION, NO REFRESHING
- OUTPUT LATCHES
- BUILT-IN 1 OF 16 CHIP ENABLE DECODER
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE-STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = -12V, V_{DD} = 0V
- 24 PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

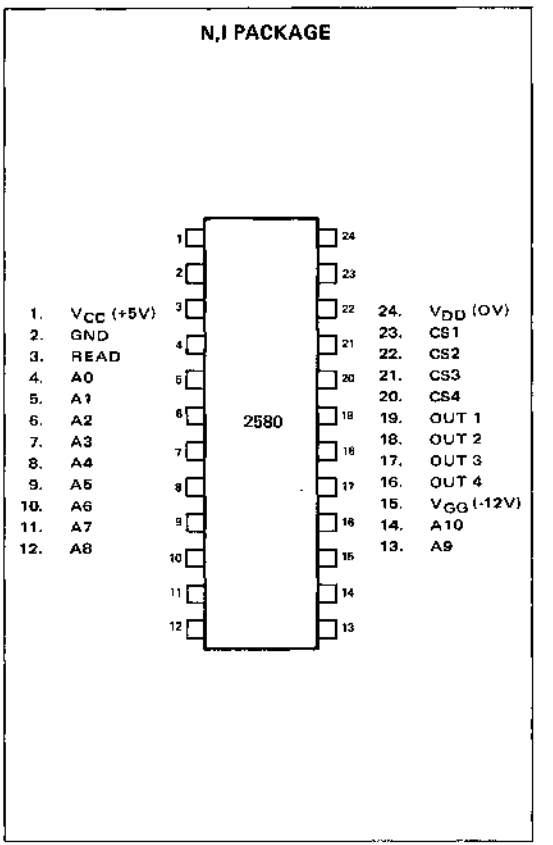
- MICRO-PROGRAMMING
- LOOK-UP TABLES
- CODE CONVERSION
- RANDOM LOGIC SYNTHESIS
- CHARACTER GENERATION

BIPOLAR COMPATIBILITY

All inputs of the 2580 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N,I PACKAGE

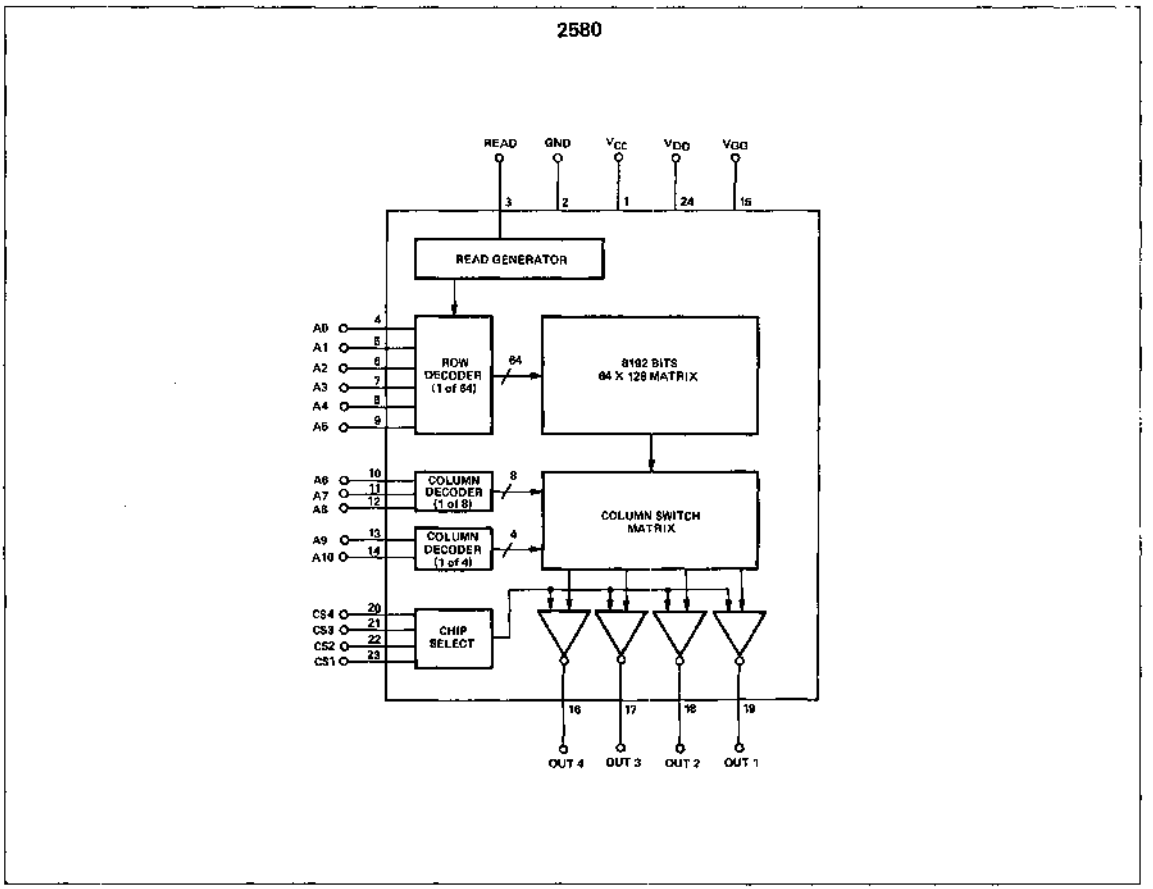


PART IDENTIFICATION

PART NUMBER	OP. TEMP. RANGE	PACKAGE
2580N	0-70°C	24-PIN DIP
2580I	0-70°C	24-PIN DIP

Note: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70°C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted. (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		23	35	mA	(8)
I_{GG}	V_{GG} Power Supply Current		23	35	mA	(8)
V_{IL}	Input Logic "0"			1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

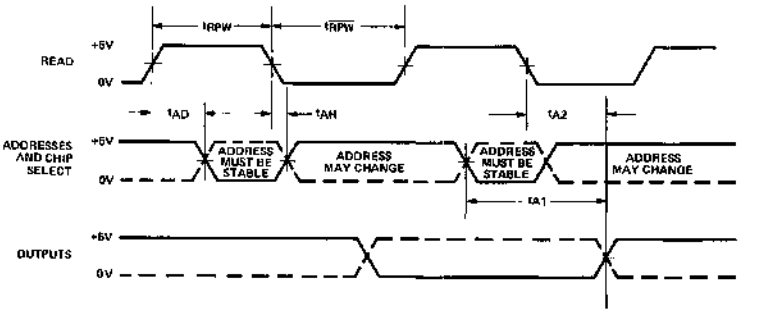
T_A = 25°C; V_{CC} = 5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0"			0.8	V	One TTL Load
V_{OH}	Output Logic "1"	3.5			V	One TTL Load
t_{RPW}[10]	Read Pulse Width	500	400		ns	
t_{RPW}[9]	Read Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (11)			50	ns	
t_{AH}	Address Hold Time	0			ns	
t_{A1}	Address to Output Delay		625	700	ns	
t_{A2}	End of Read Pulse to Output Delay		200	250		
C_{IN}	Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p V_{IN} = V_{CC}

NOTES:

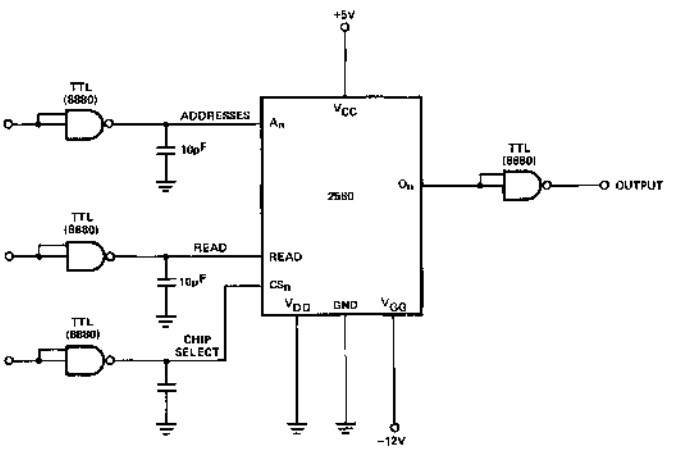
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs open, t_{RPW} = 500ns, $t_{\overline{RPW}}$ = 500ns.
9. During $t_{\overline{RPW}}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
10. During t_{RPW} addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (falling edge) of the READ pulse. After t_{A2}, data appears at the output terminals.
11. Addresses must be stable within 50ns after the READ line rises and must remain stable until the READ line falls.

TIMING DIAGRAM



Note: All measurements made at 50% points.
Input $t_r = t_f = 10ns$.

AC TEST SETUP

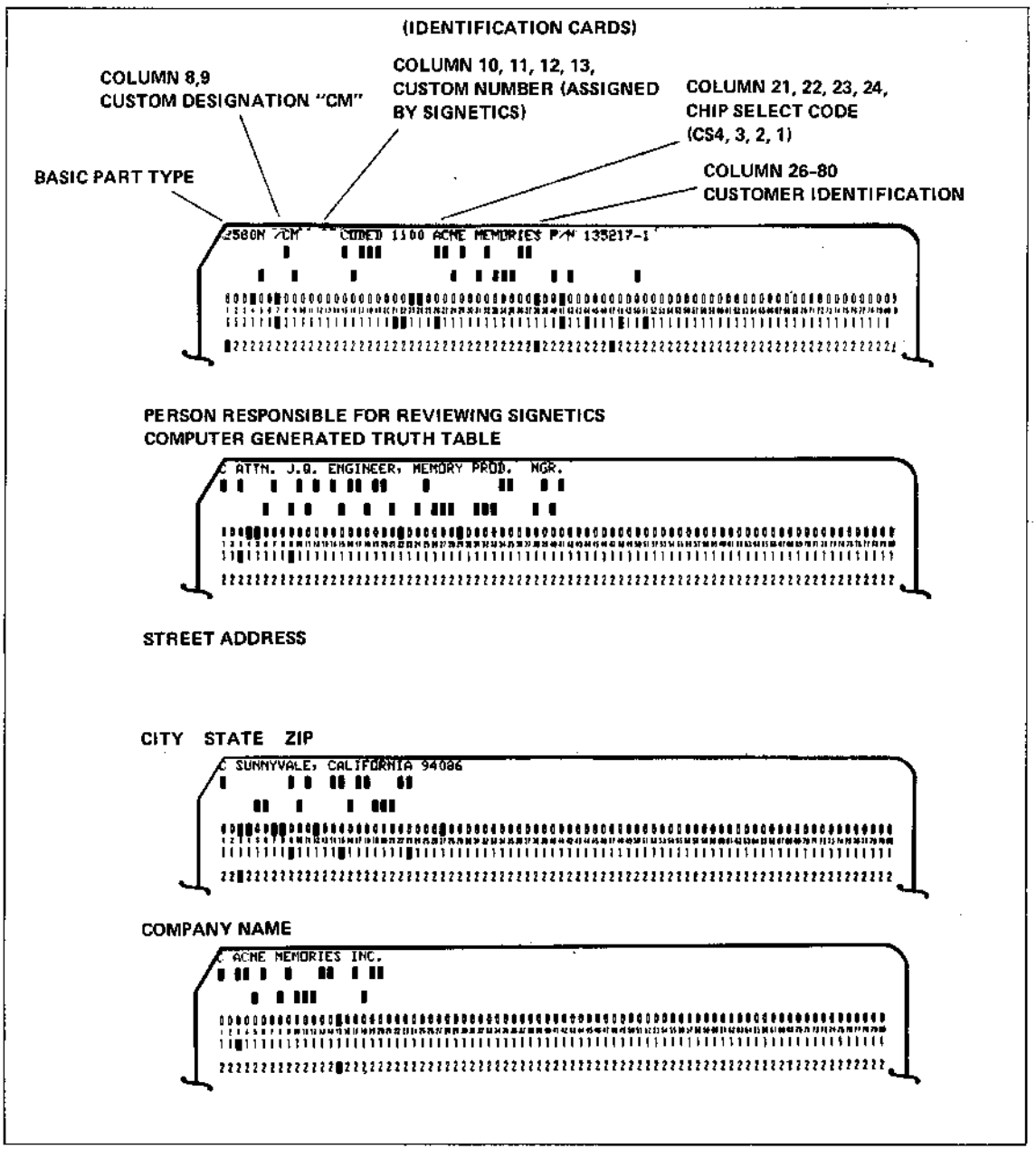


CODING FORMAT

Coding data for the 2580 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computor Aided Design (CAD) facility. The truth table will then be sent to the customer requesting engineer for final approval. On receipt of final approval, Signetics will cut the rubylith mask and proceed with manufacture.

CARD FORMAT



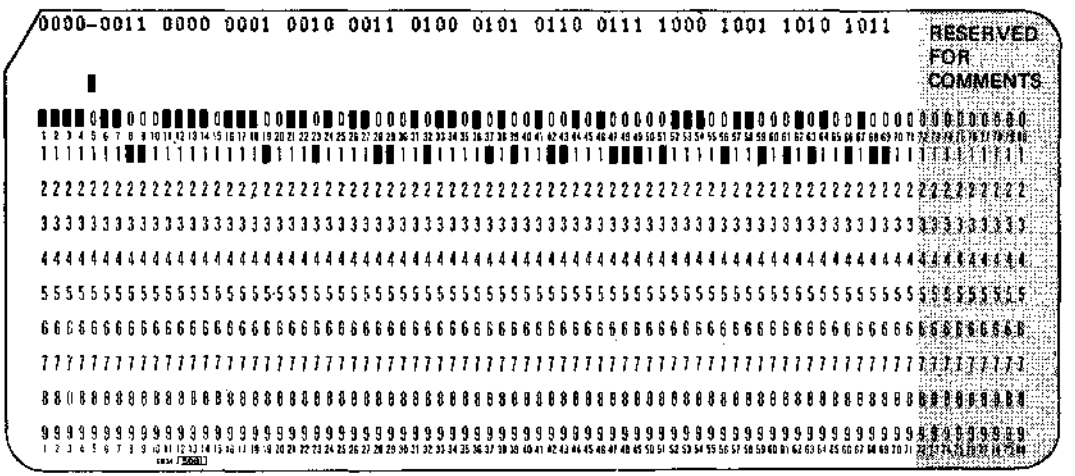
CODING FORMAT (Cont'd)

DATA CARD FORMAT

Col 1-4	Decimal equivalent of first data word location. Example: 0124 Note: leading zeros must be used for addresses from 0000 to 0999.
Col 5	Dash (-) to separate numbers
Col 6-9	Address of last data word on card
Col 10	Blank
Col 11-14	First data word (0_4, 0_3, 0_2, 0_1)
Col 15	Blank
Col 16-19	Second data word
Etc. thru column 71	
Col 72-80	Reserved for comments (These columns are ignored by the computer)

Up to twelve (12) data words can be coded on one card. Less than 12 may be used as long as the first and last addresses are given in columns 1-9.

EXAMPLE



TRUTH TABLE WORKSHEET

DECIMAL ADDRESS	O_4	O_3	O_2	O_1

DECIMAL ADDRESS	O_4	O_3	O_2	O_1

Note:
"1" = +5V
"0" = 0V
(Copy this form when submitting written truth table)

signetics

FULLY DECODED, 1024-BIT STATIC RANDOM ACCESS MEMORY

2602
2602-1

ADVANCED SPECIFICATION

SILICON GATE MOS 2600 SERIES

DESCRIPTION

The Signetics 2602 is a medium speed, static random access memory offering a 1024x1 organization. Fabricated with low threshold N-Channel silicon gate technology, the 2602 yields an access and read cycle time of less than 1 μs for the standard version and 500ns for the -1 version. Write cycle time is 500ns.

The 2602 is fully static, requiring no clocks and is completely DTL/TTL compatible including the single +5V power supply requirement.

FEATURES

- 1024x1 STATIC OPERATION
- 100% TTL COMPATIBLE
- LOW ACCESS AND CYCLE TIME: 2602 1μs
  2602-1 500ns
- LOW POWER DISSIPATION 0.2mW/BIT
- STANDARD PACKAGE 16-PIN DIP
- V_{CC} = +5V
- SIGNETICS N-CHANNEL SILICON GATE TECHNOLOGY
- TRI-STATE OUTPUT

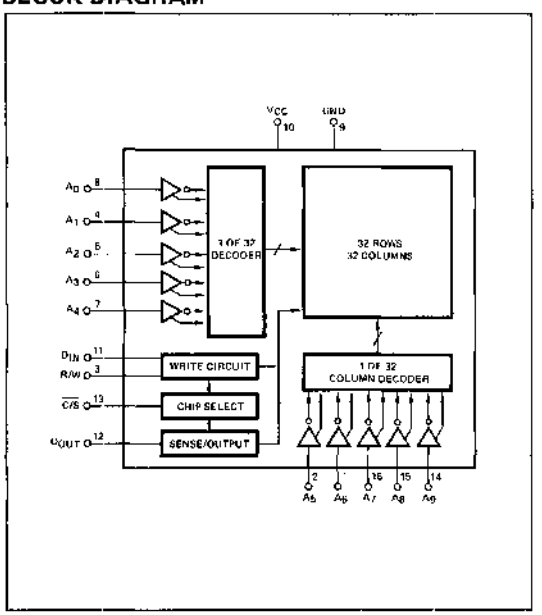
APPLICATIONS

PERIPHERAL MEMORIES

BUFFER MEMORIES

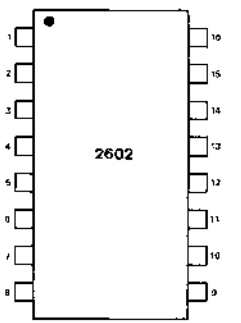
MINICOMPUTER MEMORY

BLOCK DIAGRAM



PIN CONFIGURATION

B & 1 PACKAGES



1. Address 6
2. Address 5
3. Read/$\overline{\text{Write}}$
4. Address 1
5. Address 2
6. Address 3
7. Address 4
8. Address 0
16. Address 7
15. Address 8
14. Address 9
13. $\overline{\text{Chip Select}}$
12. Data Out
11. Data In
10. V_{CC}
9. Ground

PART IDENTIFICATION

TYPE	PACKAGE	T_A	OP. TEMP. RANGE
2602B	16-Pin Plastic DIP	1μs	0-70°C
2602-1B	16-Pin Plastic DIP	500ns	0-70°C
2602 I	16-Pin Ceramic DIP	1μs	0-70°C
2602-1I	16-Pin Ceramic DIP	500ns	0-70°C

MAXIMUM GUARANTEED RATINGS:

Operating Ambient Temperature	0°C to +70°C
Storage Temperature; All Input,	−65°C to +150°C
Output, and Supply Voltages with respect to V_{SS}	−0.5 V to +12 V
Package Power Dissipation "B" Pkg.	640 mW
"I" Pkg.	800 mW

DC AND OPERATING CHARACTERISTICS:

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{SS} = 0V unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			500	nA	V_{IN} = 5.25V
I_{LO}	Output Leakage			500	nA	V_{OUT} = 5.25V
V_{IH}	Input High Level Voltage (All Inputs)	2.2		5.25	V	
V_{IL}	Input Low Level Voltage (All Inputs)	−0.3		0.65	V	
V_{OL}	Output Low Voltage	0		0.4	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = −100 μA
I_{CC}	Supply Current		35	50	mA	Output Open
C_{IN}	Input Capacitance (Any Input)		5	10	pF	
C_{OUT}	Output Capacitance		5	10	pF	

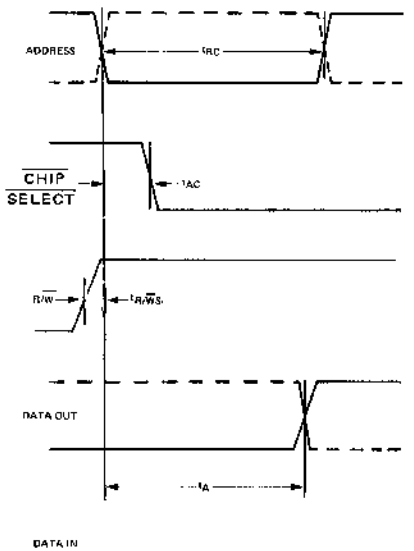
AC CHARACTERISTICS:

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{SS} = 0V unless otherwise noted.

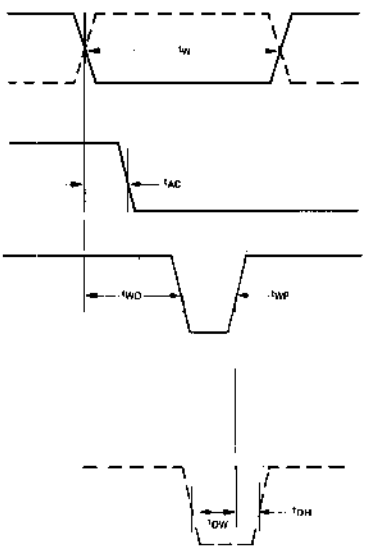
SYMBOL	TEST	MIN	TYP	MAX	UNITS	CONDITIONS
	READ CYCLE					
t_{RC}	Read Cycle 2602	1.0			μs	
	2602−1	0.6			μs	
t_{AC}	Address to Chip Select Delay 2602			0.4	μs	At Minimum
	2602−1			0.2	μs	Read Cycle
t_A	Access Time 2602			1.0	μs	
	2602−1			0.5	μs	
	WRITE CYCLE					
t_W	Write Cycle	1μs			μs	
t_{AC}	Address to Chip Select Delay	0.05			μs	
t_{WD}	Address to Write Pulse Delay	0.4			μs	
t_{WP}	Write Pulse Width	0.5			μs	
t_{DW}	Data Set-up Time	0.25			μs	
t_{DH}	Data Hold Time	0.1			μs	
	CHIP SELECT AND DESELECT					
t_{CW}	Chip Select Pulse Width			0.3	μs	
t_{CS}	Access Time Through Chip Select Input			0.2	μs	
t_{CD}	Chip Deselect Time			0.2	μs	
$t_{R/\overline{WS}}$	Read/$\overline{\text{Write}}$ Set-Up Time	0.5			μs	

TIMING DIAGRAMS

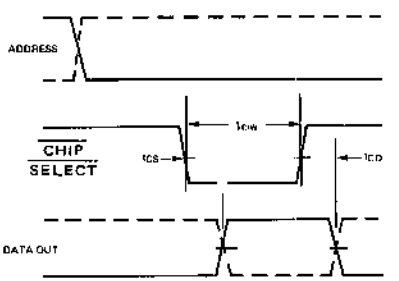
READ CYCLE



WRITE CYCLE



CHIP SELECT AND DESELECT



NOTE: Timing measured from 50% points.

CUSTOM CODING INFORMATION

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

TEL. _____

AUTHORIZED SIGNATURE _____

BASIC PRODUCT TYPE _____

DATE _____

CUSTOMER PRINT OR I.D. NUMBER _____

PURCHASE ORDER NUMBER _____

_____

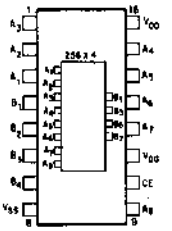
BASIC INFORMATION

- DEVICE TYPE N24 ☐ ☐
- NUMBER OF CHIP SELECTS ☐ 1 ☐ 3
- CHIP SELECT CODE ☐ CE_3 ☐ CE_2 ☐ CE_1
- OUTPUT DEVICE ☐ MOS RESISTOR
  ☐ TTL (Bare Drain)
- ORGANIZATION ☐ 8 X 256 ☐ 4 X 512
  ☐ 8 X 128 ☐ 4 X 256
- PACKAGE ☐ 16 PIN ☐ 24 PIN
- LOGIC "1" MORE NEGATIVE VOLTAGE
  LOGIC "0" MORE POSITIVE VOLTAGE
- INSTRUCTIONS FOR COMPLETING TRUTH TABLE
  (Required only if computer punch cards are not used)
  FOR 8 X 256 USE COLUMN I ADDRESS– OUTPUTS B1–B8
  FOR 8 X 128 USE COLUMN I ADDRESS– OUTPUTS B1–B8
  FOR 4 X 256 USE COLUMN I ADDRESS WORDS 0–127, OUTPUTS B1–B4; COLUMN II ADDRESS WORDS 128–255, OUTPUTS B5–B8
  FOR 4 X 512 USE COLUMN I ADDRESS WORDS 0–255, OUTPUTS B1–B4; COLUMN III ADDRESS WORDS 256–511, OUTPUTS B5–B8

ORGANIZATION

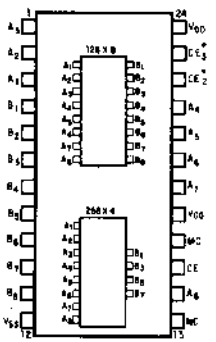
The Signetics 2400 Series is a family of read-only memories. The 2410, 2420, and 2430 Series are offered with the following organizations.

2410



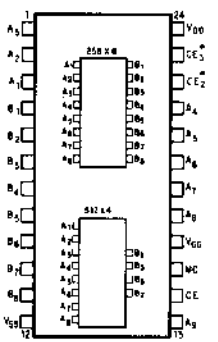
2410 Series- 1024 bit read-only memory organized as 256 words of 4 bits in a 16 pin dip.

2420



2420 Series- 1024 bit read-only memory organized a 128 words by 8 bits or 256 words by 4 bits If the 256 words by 4 organization is specified outputs will appear on pins 4, 6, 8, and 10.

2430



2430 Series- 2048 bit read-only memory organized as 256 words by 8 bits or 512 words by 4 bits. If the 512 word by 4 organization is specified outputs will appear on pins 4, 6, 8, and 10.

ROM SELECTION CHART

TYPE	ORGANIZATION	PACKAGE	OUTPUTS	CHIP SELECT CONTROLS
N2410I	256 x 4	16-Pin Ceramic DIP	MOS Pull-up	1
N2411I	256 x 4	16-Pin Ceramic DIP	Bare Drain	1
N2420Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	MOS Pull-up	1
N2421Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	Bare Drain	1
N2425Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	MOS Pull-up	3 (binary coded)*
N2426Y	128 x 8, 256 x 4	24-Pin Ceramic DIP	Bare Drain	3 (binary coded)*
N2430Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	MOS Pull-up	1
N2431Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	Bare Drain	1
N2435Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	MOS Pull-up	3 (binary coded)*
N2436Y	512 x 4, 256 x 8	24-Pin Ceramic DIP	Bare Drain	3 (binary coded)*

*Mask Programmable

CIRCUIT OPTION

The following circuit options are available for the user's particular needs:

OUTPUT BUFFER

For all series the user has the option of MOS or TTL outputs. This must be specified by the user.

- MOS output- an output having an MOS resistor connected to V_{DD}. This allows interfacing with other MOS devices.
- TTL output- an output having no MOS resistor connected to V_{DD}. Commonly called a "bare drain" output; this allows direct interfacing with TTL circuits and external "wired AND" capability.

CHIP SELECT

- "Single" ROM- one which has only one chip select. A logical "0" on the chip select line places all outputs in the "1" state (or open-circuited in the case of a "TTL" output).
- "Coded" ROM- one which has a three digit binary code chip select. This allows paralleling up to eight devices without external chip select logic thereby allowing the user to save the cost of extra packages and PC board space.
- 2410 Series may only be ordered as a "single" ROM (one chip select).
- 2420 and 2430 Series may be ordered as "single" or "coded" ROM's (one chip select or three chip selects).

DEFINITIONS

Logic definition:
All logic is assumed negative
"0" is the more positive voltage
"1" is the more negative voltage

Input definition:
A1 is the least significant input address
A8 is the most significant input address

INPUT FORMAT

Programming information for Signetics' 2400 Series should be transmitted to Signetics in the form of computer punched cards accompanied by information on the various circuit options desired. Upon receipt of each deck and the circuit option desired for that deck a computer generated truth table will be made and a copy of this truth table returned to the customer. This minimizes the possibility of error and allows the best possible delivery (normally 4 weeks after receipt of card deck).

Upon receipt of the computer generated truth table check it carefully and if any errors are discovered notify Signetics immediately.

The Signetics' 2400 Series Read-Only Memory can be programmed so that for any binary input A1 through A8 the outputs B1 through B8 are uniquely determined. Each deck of cards sent to Signetics must contain a card describing the options desired (card 1), the unique outputs for each word in memory (cards 2 through 129 or 257, depending on organization), and cards specifying the address to which the computer generated truth table should be sent. Cards should be punched according to the format on the following pages.

If it is not feasible to use computer punched cards, the user should describe the circuit option desired and complete the truth table. Upon receipt of pages Signetics will punch the computer cards and return a copy of the computer generated truth table. (the user can realize a substantial savings associated with the coding charge by using computer cards).

CARD 1

COLUMN	DATA
1-8	Starting at column 1- punch "coded" or "single"
9-11*	If "coded", punch the binary code chip select (i.e., 101), if "single" leave blank
12	Leave blank
13-17	Punch the ROM organization desired (i.e., 8 X 256, 4 X 512), etc.
18	Leave blank
19-21	Punch MOS for an MOS output. Punch TTL for a TTL output (bare drain)
22-27	Leave blank (For CM No.)
28-33	Punch the basic device type desired (i.e., N2410I, N2420Y), etc.
34-80	Comments punched here will appear as the title on the truth table. This should include customer part identification

*CE_3, CE_2 and CE_1 respectively

CARDS 2 THROUGH 257 (4 X 512 Organization only)

Each card specifies the output of two 4-bit words in columns 1 through 8. The decimal equivalent of the binary coded input address is punched in columns 78. 79, and 80.

COLUMN	DATA
1-4	Punch output for words 0-255
5-8	Punch output for words 256-511
9-77	Leave blank
78-8	Punch decimal equivalent of binary coded input address of the word corresponding to the outputs punched in Columns 1-4

Column 78- Hundreds Digit
Column 79- Tens Digit
Column 80- Units Digit

CARD 2 THROUGH 129 (8 X 128 Organization) 2 THROUGH 257 (8 X 256 Organization)

Each card specifies the output of one 8-bit word in columns 1 through 8. The decimal equivalent of the binary coded input address for that word is punched in columns 78, 79, and 80.

COLUMN	DATA
1-8	Punch outputs B1 through B8 in columns one through eight respectively
9-77	Leave blank
78-80	Punch decimal equivalent of binary coded input address which corresponds to the outputs punched in Columns 1-8

Column 78- Hundreds Digit
Column 79- Tens Digit
Column 80- Units Digit

CARDS 2 THROUGH 129 (4 X 256 Organization only)

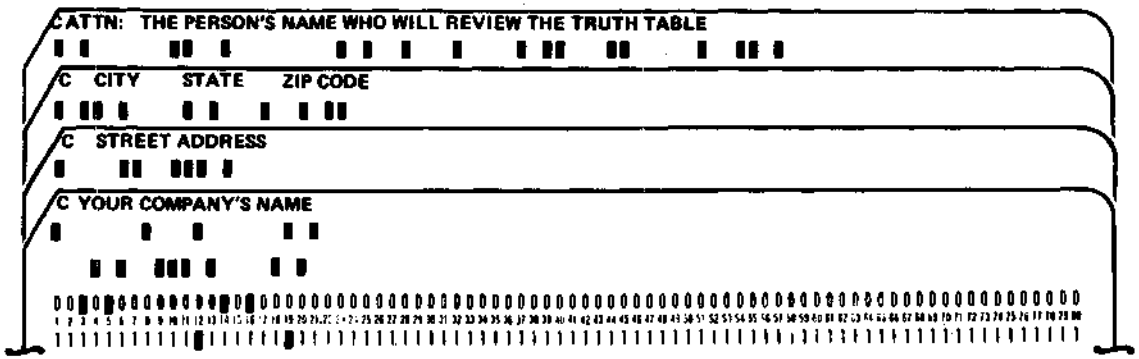
Each card specifies the output of two 4-bit words in columns 1 through 8. The decimal equivalent of the binary coded input address is punched in columns 78, 79, and 80.

COLUMN	DATA
1-4	Punch output for words 0-127
5-8	Punch output for words 128-255
9-77	Leave blank
78-80	Punch decimal equivalent of binary coded input address corresponding to the outputs punched in Columns 1-4

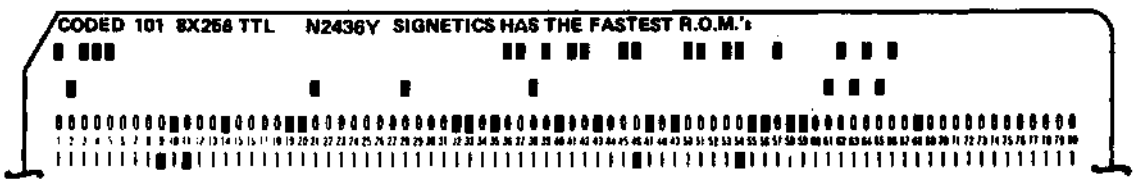
Column 78-Hundreds Digit
Column 79- Tens Digit
Column 80- Units Digit

EXAMPLE CARDS:

ADDRESS CARDS

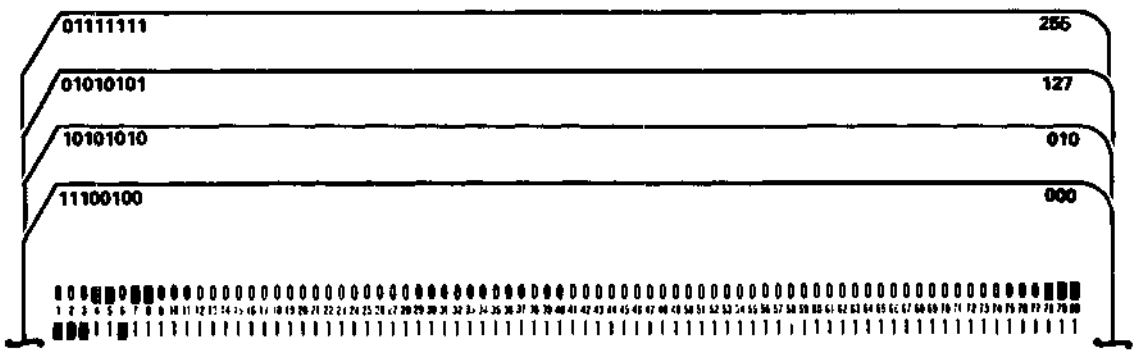


CARD 1



The above specifies a "coded" ROM with the binary coded chip select "101" organized 8 X 256 with TTL outputs (bare drain). The basic device type is a N2436Y ("Y" indicates a 24-pin ceramic DIP. N indicates temperature range: -25°C– +70°C).

CARDS 2-129 AND CARDS 2-257



- Outputs B1 through B8 are in columns 1 through 8 respectively
- Decimal equivalent of binary coded input address is in columns 78, 79, and 80
- For 8 X 128 and 8 X 256 organizations- outputs are B1 through B8 respectively
- For 4 X 512 organization:

  Data card 0 Word 000 outputs B1 through B4 respectively
  Word 256 outputs B5 through B8 respectively
  Data card 10 Word 010 outputs B1 through B4 respectively
  Word 266 outputs B5 through B8 respectively
- For 4 X 256 Organization:

  Data card 0 Word 000 outputs B1 through B4 respectively
  Word 128 outputs B5 through B8 respectively
  Data card 10 Word 010 outputs B1 through B4 respectively
  Word 138 outputs B5 through B8 respectively

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHARACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	0	0	0	0	0	0	0	000	128	256									
0	0	0	0	0	0	0	1	001	129	257									
0	0	0	0	0	0	1	0	002	130	258									
0	0	0	0	0	0	1	1	003	131	259									
0	0	0	0	0	1	0	0	004	132	260									
0	0	0	0	0	1	0	1	005	133	261									
0	0	0	0	0	1	1	0	006	134	262									
0	0	0	0	0	1	1	1	007	135	263									
0	0	0	0	1	0	0	0	008	136	264									
0	0	0	0	1	0	0	1	009	137	265									
0	0	0	0	1	0	1	0	010	138	266									
0	0	0	0	1	0	1	1	011	139	267									
0	0	0	0	1	1	0	0	012	140	268									
0	0	0	0	1	1	0	1	013	141	269									
0	0	0	0	1	1	1	0	014	142	270									
0	0	0	0	1	1	1	1	015	143	271									
0	0	0	1	0	0	0	0	016	144	272									
0	0	0	1	0	0	0	1	017	145	273									
0	0	0	1	0	0	1	0	018	146	274									
0	0	0	1	0	0	1	1	019	147	275									
0	0	0	1	0	1	0	0	020	148	276									
0	0	0	1	0	1	0	1	021	149	277									
0	0	0	1	0	1	1	0	022	150	278									
0	0	0	1	0	1	1	1	023	151	279									
0	0	0	1	1	0	0	0	024	152	280									
0	0	0	1	1	0	0	1	025	153	281									
0	0	0	1	1	0	1	0	026	154	282									
0	0	0	1	1	0	1	1	027	155	283									
0	0	0	1	1	1	0	0	028	156	284									
0	0	0	1	1	1	0	1	029	157	285									
0	0	0	1	1	1	1	0	030	158	286									
0	0	0	1	1	1	1	1	031	159	287									
0	0	1	0	0	0	0	0	032	160	288									
0	0	1	0	0	0	0	1	033	161	289									
0	0	1	0	0	0	1	0	034	162	290									
0	0	1	0	0	0	1	1	035	163	291									
0	0	1	0	0	1	0	0	036	164	292									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHARACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	0	1	0	0	1	0	1	037	165	293									
0	0	1	0	0	1	1	0	038	166	294									
0	0	1	0	0	1	1	1	039	167	295									
0	0	1	0	1	0	0	0	040	168	296									
0	0	1	0	1	0	0	1	041	169	297									
0	0	1	0	1	0	1	0	042	170	298									
0	0	1	0	1	0	1	1	043	171	299									
0	0	1	0	1	1	0	0	044	172	300									
0	0	1	0	1	1	0	1	045	173	301									
0	0	1	0	1	1	1	0	046	174	302									
0	0	1	0	1	1	1	1	047	175	303									
0	0	1	1	0	0	0	0	048	176	304									
0	0	1	1	0	0	0	1	049	177	305									
0	0	1	1	0	0	1	0	050	178	306									
0	0	1	1	0	0	1	1	051	179	307									
0	0	1	1	0	1	0	0	052	180	308									
0	0	1	1	0	1	0	1	053	181	309									
0	0	1	1	0	1	1	0	054	182	310									
0	0	1	1	0	1	1	1	055	183	311									
0	0	1	1	1	0	0	0	056	184	312									
0	0	1	1	1	0	0	1	057	185	313									
0	0	1	1	1	0	1	0	058	186	314									
0	0	1	1	1	0	1	1	059	187	315									
0	0	1	1	1	1	0	0	060	188	316									
0	0	1	1	1	1	0	1	061	189	317									
0	0	1	1	1	1	1	0	062	190	318									
0	0	1	1	1	1	1	1	063	191	319									
0	1	0	0	0	0	0	0	064	192	320									
0	1	0	0	0	0	0	1	065	193	321									
0	1	0	0	0	0	1	0	066	194	322									
0	1	0	0	0	0	1	1	067	195	323									
0	1	0	0	0	1	0	0	068	196	324									
0	1	0	0	0	1	0	1	069	197	325									
0	1	0	0	0	1	1	0	070	198	326									
0	1	0	0	0	1	1	1	071	199	327									
0	1	0	0	1	0	0	0	072	200	328									
0	1	0	0	1	0	0	1	073	201	329									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	1	0	0	1	0	1	0	074	202	330									
0	1	0	0	1	0	1	1	075	203	331									
0	1	0	0	1	1	0	0	076	204	332									
0	1	0	0	1	1	0	1	077	205	333									
0	1	0	0	1	1	1	0	078	206	334									
0	1	0	0	1	1	1	1	079	207	335									
0	1	0	1	0	0	0	0	080	208	336									
0	1	0	1	0	0	0	1	081	209	337									
0	1	0	1	0	0	1	0	082	210	338									
0	1	0	1	0	0	1	1	083	211	339									
0	1	0	1	0	1	0	0	084	212	340									
0	1	0	1	0	1	0	1	085	213	341									
0	1	0	1	0	1	1	0	086	214	342									
0	1	0	1	0	1	1	1	087	215	343									
0	1	0	1	1	0	0	0	088	216	344									
0	1	0	1	1	0	0	1	089	217	345									
0	1	0	1	1	0	1	0	090	218	346									
0	1	0	1	1	0	1	1	091	219	347									
0	1	0	1	1	1	0	0	092	220	348									
0	1	0	1	1	1	0	1	093	221	349									
0	1	0	1	1	1	1	0	094	222	350									
0	1	0	1	1	1	1	1	095	223	351									
0	1	1	0	0	0	0	0	096	224	352									
0	1	1	0	0	0	0	1	097	225	353									
0	1	1	0	0	0	1	0	098	226	354									
0	1	1	0	0	0	1	1	099	227	355									
0	1	1	0	0	1	0	0	100	228	356									
0	1	1	0	0	1	0	1	101	229	357									
0	1	1	0	0	1	1	0	102	230	358									
0	1	1	0	0	1	1	1	103	231	359									
0	1	1	0	1	0	0	0	104	232	360									
0	1	1	0	1	0	0	1	105	233	361									
0	1	1	0	1	0	1	0	106	234	362									
0	1	1	0	1	0	1	1	107	235	363									
0	1	1	0	1	1	0	0	108	236	364									
0	1	1	0	1	1	0	1	109	237	365									
0	1	1	0	1	1	1	0	110	238	366									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
0	1	1	0	1	1	1	1	111	239	367									
0	1	1	1	0	0	0	0	112	240	368									
0	1	1	1	0	0	0	1	113	241	369									
0	1	1	1	0	0	1	0	114	242	370									
0	1	1	1	0	0	1	1	115	243	371									
0	1	1	1	0	1	0	0	116	244	372									
0	1	1	1	0	1	0	1	117	245	373									
0	1	1	1	0	1	1	0	118	246	374									
0	1	1	1	0	1	1	1	119	247	375									
0	1	1	1	1	0	0	0	120	248	376									
0	1	1	1	1	0	0	1	121	249	377									
0	1	1	1	1	0	1	0	122	250	378									
0	1	1	1	1	0	1	1	123	251	379									
0	1	1	1	1	1	0	0	124	252	380									
0	1	1	1	1	1	0	1	125	253	381									
0	1	1	1	1	1	1	0	126	254	382									
0	1	1	1	1	1	1	1	127	255	383									
1	0	0	0	0	0	0	0	128		384									
1	0	0	0	0	0	0	1	129		385									
1	0	0	0	0	0	1	0	130		386									
1	0	0	0	0	0	1	1	131		387									
1	0	0	0	0	1	0	0	132		388									
1	0	0	0	0	1	0	1	133		389									
1	0	0	0	0	1	1	0	134		390									
1	0	0	0	0	1	1	1	135		391									
1	0	0	0	1	0	0	0	136		392									
1	0	0	0	1	0	0	1	137		393									
1	0	0	0	1	0	1	0	138		394									
1	0	0	0	1	0	1	1	139		395									
1	0	0	0	1	1	0	0	140		396									
1	0	0	0	1	1	0	1	141		397									
1	0	0	0	1	1	1	0	142		398									
1	0	0	0	1	1	1	1	143		399									
1	0	0	1	0	0	0	0	144		400									
1	0	0	1	0	0	0	1	145		401									
1	0	0	1	0	0	1	0	146		402									
1	0	0	1	0	0	1	1	147		403									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
1	0	0	1	0	1	0	0	148		404									
1	0	0	1	0	1	0	1	149		405									
1	0	0	1	0	1	1	0	150		406									
1	0	0	1	0	1	1	1	151		407									
1	0	0	1	1	0	0	0	152		408									
1	0	0	1	1	0	0	1	153		409									
1	0	0	1	1	0	1	0	154		410									
1	0	0	1	1	0	1	1	155		411									
1	0	0	1	1	1	0	0	156		412									
1	0	0	1	1	1	0	1	157		413									
1	0	0	1	1	1	1	0	158		414									
1	0	0	1	1	1	1	1	159		415									
1	0	1	0	0	0	0	0	160		416									
1	0	1	0	0	0	0	1	161		417									
1	0	1	0	0	0	1	0	162		418									
1	0	1	0	0	0	1	1	163		419									
1	0	1	0	0	1	0	0	164		420									
1	0	1	0	0	1	0	1	165		421									
1	0	1	0	0	1	1	0	166		422									
1	0	1	0	0	1	1	1	167		423									
1	0	1	0	1	0	0	0	168		424									
1	0	1	0	1	0	0	1	169		425									
1	0	1	0	1	0	1	0	170		426									
1	0	1	0	1	0	1	1	171		427									
1	0	1	0	1	1	0	0	172		428									
1	0	1	0	1	1	0	1	173		429									
1	0	1	0	1	1	1	0	174		430									
1	0	1	1	1	1	1	1	175		431									
1	0	1	1	0	0	0	0	176		432									
1	0	1	1	0	0	0	1	177		433									
1	0	1	1	0	0	1	0	178		434									
1	0	1	1	0	0	1	1	179		435									
1	0	1	1	0	1	0	0	180		436									
1	0	1	1	0	1	0	1	181		437									
1	0	1	1	0	1	1	0	182		438									
1	0	1	1	0	1	1	1	183		439									
1	0	1	1	1	0	0	0	184		440									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHARACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
1	0	1	1	1	0	0	1	185		441									
1	0	1	1	1	0	1	0	186		442									
1	0	1	1	1	0	1	1	187		443									
1	0	1	1	1	1	0	0	188		444									
1	0	1	1	1	1	0	1	189		445									
1	0	1	1	1	1	1	0	190		446									
1	0	1	1	1	1	1	1	191		447									
1	1	0	0	0	0	0	0	192		448									
1	1	0	0	0	0	0	1	193		449									
1	1	0	0	0	0	1	0	194		450									
1	1	0	0	0	0	1	1	195		451									
1	1	0	0	0	1	0	0	196		452									
1	1	0	0	0	1	0	1	197		453									
1	1	0	0	0	1	1	0	198		454									
1	1	0	0	0	1	1	1	199		455									
1	1	0	0	1	0	0	0	200		456									
1	1	0	0	1	0	0	1	201		457									
1	1	0	0	1	0	1	0	202		458									
1	1	0	0	1	0	1	1	203		459									
1	1	0	0	1	1	0	0	204		460									
1	1	0	0	1	1	0	1	205		461									
1	1	0	0	1	1	1	0	206		462									
1	1	0	0	1	1	1	1	207		463									
1	1	0	1	0	0	0	0	208		464									
1	1	0	1	0	0	0	1	209		465									
1	1	0	1	0	0	1	0	210		466									
1	1	0	1	0	0	1	1	211		467									
1	1	0	1	0	1	0	0	212		468									
1	1	0	1	0	1	0	1	213		469									
1	1	0	1	0	1	1	0	214		470									
1	1	0	1	0	1	1	1	215		471									
1	1	0	1	1	0	0	0	216		472									
1	1	0	1	1	0	0	1	217		473									
1	1	0	1	1	0	1	0	218		474									
1	1	0	1	1	0	1	1	219		475									
1	1	0	1	1	1	0	0	220		476									
1	1	0	1	1	1	0	1	221		477									

ADDRESS INPUT GATE								DECIMAL ADDRESS			OUTPUT DATA								USER'S CHAR-ACTER
A8	A7	A6	A5	A4	A3	A2	A1	I	II	III	B1	B2	B3	B4	B5	B6	B7	B8	
1	1	0	1	1	1	1	0	222		478									
1	1	0	1	1	1	1	1	223		479									
1	1	1	0	0	0	0	0	224		480									
1	1	1	0	0	0	0	1	225		481									
1	1	1	0	0	0	1	0	226		482									
1	1	1	0	0	0	1	1	227		483									
1	1	1	0	0	1	0	0	228		484									
1	1	1	0	0	1	0	1	229		485									
1	1	1	0	0	1	1	0	230		486									
1	1	1	0	0	1	1	1	231		487									
1	1	1	0	1	0	0	0	232		488									
1	1	1	0	1	0	0	1	233		489									
1	1	1	0	1	0	1	0	234		490									
1	1	1	0	1	0	1	1	235		491									
1	1	1	0	1	1	0	0	236		492									
1	1	1	0	1	1	0	1	237		493									
1	1	1	0	1	1	1	0	238		494									
1	1	1	0	1	1	1	1	239		495									
1	1	1	1	0	0	0	0	240		496									
1	1	1	1	0	0	0	1	241		497									
1	1	1	1	0	0	1	0	242		498									
1	1	1	1	0	0	1	1	243		499									
1	1	1	1	0	1	0	0	244		500									
1	1	1	1	0	1	0	1	245		501									
1	1	1	1	0	1	1	0	246		502									
1	1	1	1	0	1	1	1	247		503									
1	1	1	1	1	0	0	0	248		504									
1	1	1	1	1	0	0	1	249		505									
1	1	1	1	1	0	1	0	250		506									
1	1	1	1	1	0	1	1	251		507									
1	1	1	1	1	1	0	0	252		508									
1	1	1	1	1	1	0	1	253		509									
1	1	1	1	1	1	1	0	254		510									
1	1	1	1	1	1	1	1	255		511									

COMPANY_____

ADDRESS_____

CITY_____STATE_____ZIP____

TELEPHONE_____

AUTHORIZED SIGNATURE_____

DATE_____

CUSTOMER PRINT OR ID NO._____

PURCHASE ORDER NUMBER_____

DEVICE TYPE_____2513_____

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS)_____

INTRODUCTION

The Signetics 2513 is a high speed silicon gate MOS 2560-Bit read-only memory whose organization is specially suited for 64 X 8 X 5 raster scan character generation.

MAJOR FEATURES OF THE 2513

- ACCESS TIME 450ns TYPICALLY
- STATIC OPERATION
- TTL/DTL COMPATIBLE
- TRI-STATE OUTPUTS (HIGH-LOW-DISCONNECTED) FOR POWERFUL BUSSING CAPABILITY
- +5, -5, -12V POWER SUPPLIES
- 24-PIN SIGNETICS SILICONE DIP
- SIGNETICS SILICON GATE PROCESS TECHNOLOGY FOR PERFORMANCE AND RELIABILITY

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A three bit binary address code (A_1 through A_3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix. See Figure 1. The devices may also be used in pairs to provide 9 X 7 and 10 X 8 vertical scan formats.

CHARACTER FORMAT

ROW ADDRESS

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0

EXAMPLE 'S'

FIGURE 1

CHARACTER ADDRESS

COLUMN ADDRESS

ASCII CHARACTER	A_4	A_5	A_6	A_7	A_8	A_9
	1	1	0	0	1	0

FIGURE 2

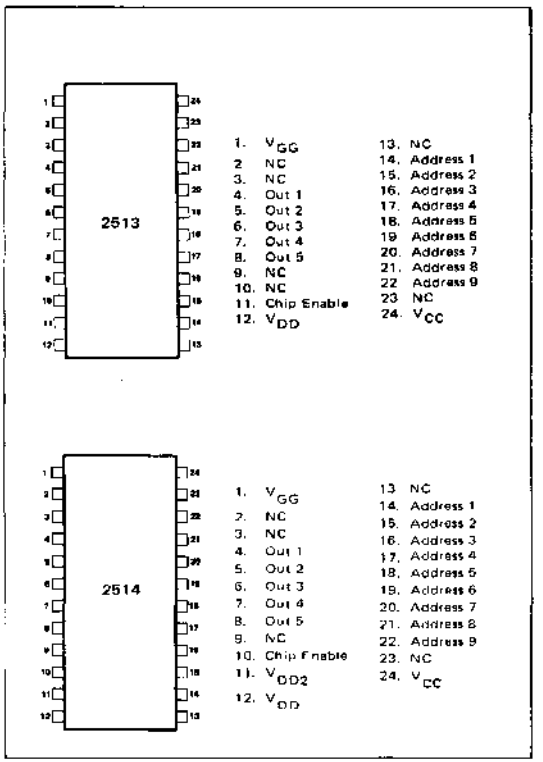
ORGANIZATION AS READ-ONLY MEMORY

For a straight 512 X 5 read-only memory, the five outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1 through A_9.

STANDARD PATTERN

A standard ASCII character font is available for the 2513. This device (2513NX/CM2140) may be used for ASCII character generation or for device evaluation.

PIN CONFIGURATION (Top View)



CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of the basic product type followed by a unique CM number assigned by Signetics. For example, "2513NX/CM2141"

- **PROGRAMMING WITH PUNCHED CARDS**
  For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- **PROGRAMMING WITH WRITTEN TRUTH TABLE**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. 3.2V minimum). Similarly, a "1" address input level is interpreted as 3.2V minimum.

IDENTIFICATION CARDS

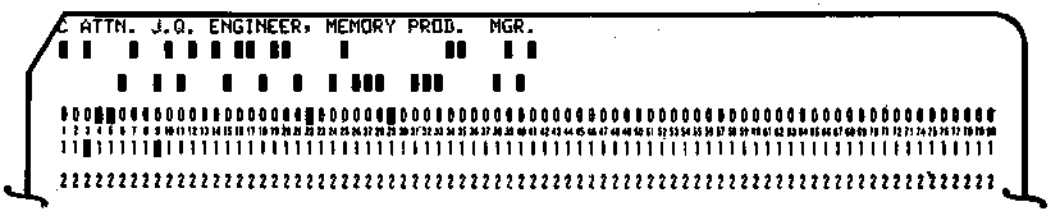
INDICATES "COMMENT" CARD

LEAVE COLS. 22, 23, 24, 25 BLANK
FOR ASSIGNMENT OF CM NO. BY SIGNETICS

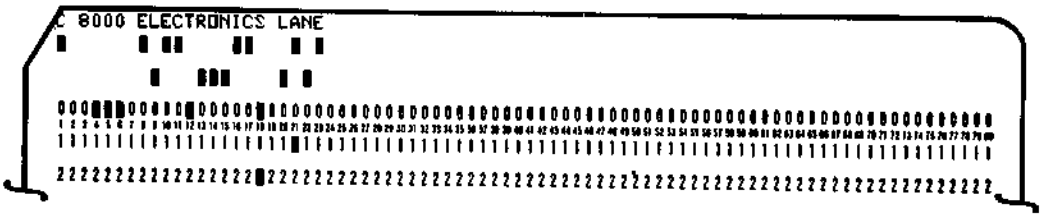
BASIC PART TYPE

CUSTOMER P/N IDENTIFICATION

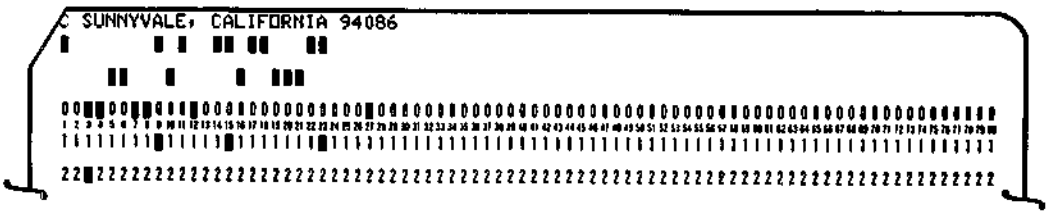
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS
COMPUTER GENERATED TRUTH TABLE



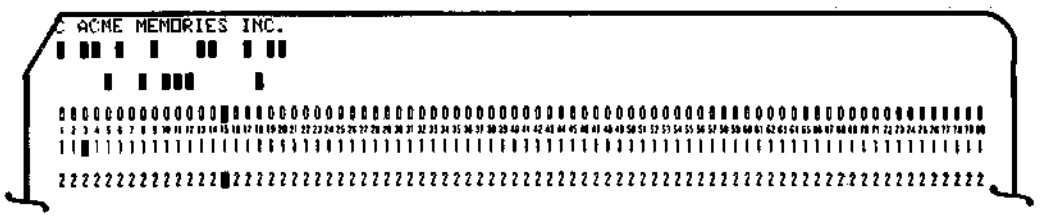
STREET ADDRESS



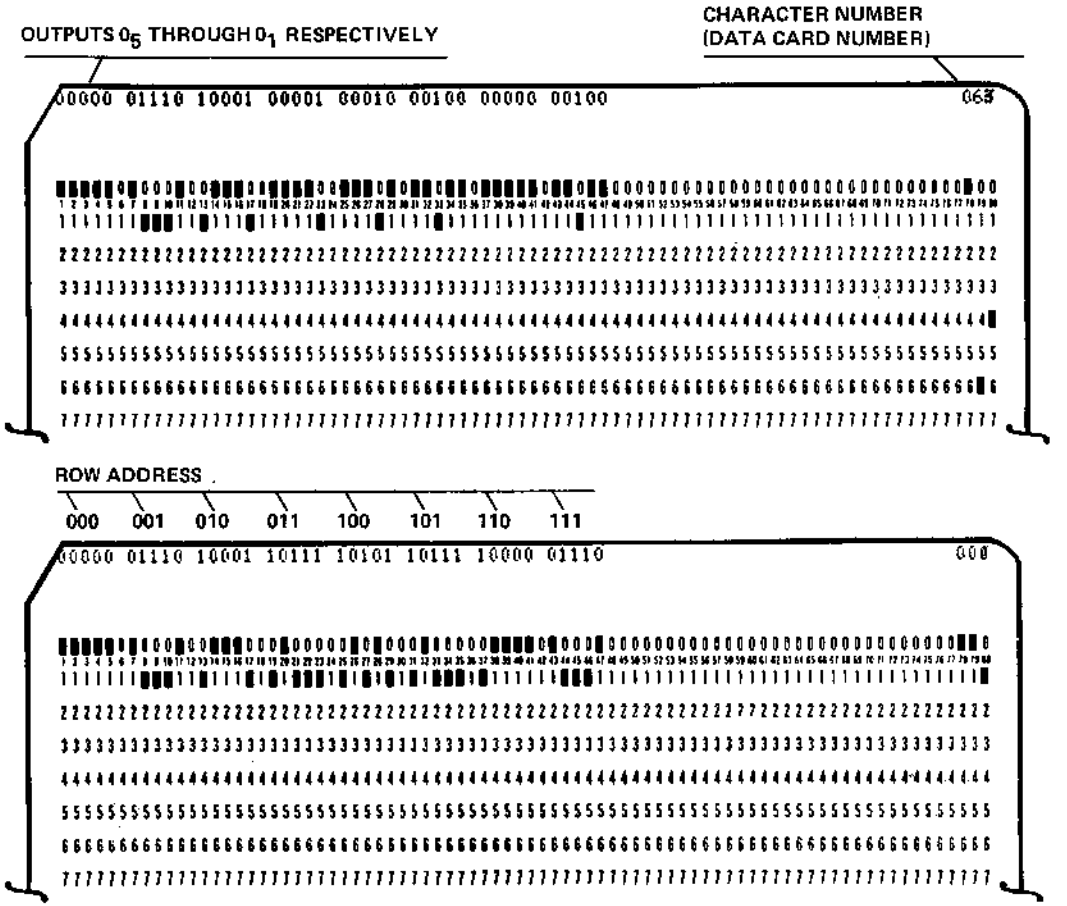
CITY STATE ZIP



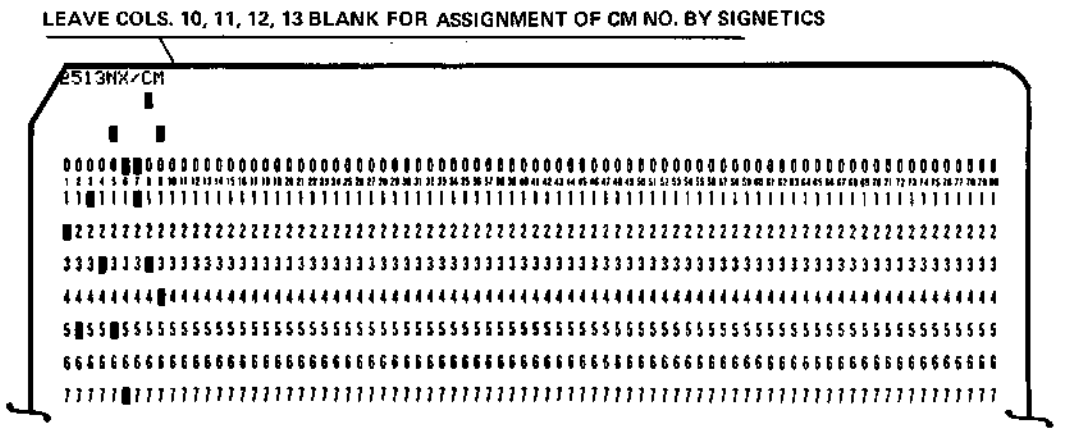
COMPANY NAME



DATA CARDS



BASIC DEVICE TYPE



NOTE:
"Character" number is in columns 78, 79, and 80. Note that each group of eight 6-bit words is treated as a character for convenience of coding.

ADDRESS A9 A8 A7 A6 A5 A4 A3 A2 A1	DECIMAL ADDRESS	OUTPUT DATA O5	O4	O3	O2	O1	USER'S CHAR.
0 0 0 0 0 0 0 0 0	000						
0 0 0 0 0 0 0 0 1	001						
0 0 0 0 0 0 0 1 0	002						
0 0 0 0 0 0 0 1 1	003						
0 0 0 0 0 0 1 0 0	004						
0 0 0 0 0 0 1 0 1	005						
0 0 0 0 0 0 1 1 0	006						
0 0 0 0 0 0 1 1 1	007						
0 0 0 0 0 1 0 0 0	008						
0 0 0 0 0 1 0 0 1	009						
0 0 0 0 0 1 0 1 0	010						
0 0 0 0 0 1 0 1 1	011						
0 0 0 0 0 1 1 0 0	012						
0 0 0 0 0 1 1 0 1	013						
0 0 0 0 0 1 1 1 0	014						
0 0 0 0 0 1 1 1 1	016						
0 0 0 0 1 0 0 0 0	016						
0 0 0 0 1 0 0 0 1	017						
0 0 0 0 1 0 0 1 0	018						
0 0 0 0 1 0 0 1 1	019						
0 0 0 0 1 0 1 0 0	020						
0 0 0 0 1 0 1 0 1	021						
0 0 0 0 1 0 1 1 0	022						
0 0 0 0 1 0 1 1 1	023						
0 0 0 0 1 1 0 0 0	024						
0 0 0 0 1 1 0 0 1	025						
0 0 0 0 1 1 0 1 0	026						
0 0 0 0 1 1 0 1 1	027						
0 0 0 0 1 1 1 0 0	028						
0 0 0 0 1 1 1 0 1	029						
0 0 0 0 1 1 1 1 0	030						
0 0 0 0 1 1 1 1 1	031						

ADDRESS A9 A8 A7 A6 A5 A4 A3 A2 A1	DECIMAL ADDRESS	OUTPUT DATA O5	O4	O3	O2	O1	USER'S CHAR.
0 0 0 1 0 0 0 0 0	032						
0 0 0 1 0 0 0 0 1	033						
0 0 0 1 0 0 0 1 0	034						
0 0 0 1 0 0 0 1 1	035						
0 0 0 1 0 0 1 0 0	036						
0 0 0 1 0 0 1 0 1	037						
0 0 0 1 0 0 1 1 0	038						
0 0 0 1 0 0 1 1 1	039						
0 0 0 1 0 1 0 0 0	040						
0 0 0 1 0 1 0 0 1	041						
0 0 0 1 0 1 0 1 0	042						
0 0 0 1 0 1 0 1 1	043						
0 0 0 1 0 1 1 0 0	044						
0 0 0 1 0 1 1 0 1	045						
0 0 0 1 0 1 1 1 0	046						
0 0 0 1 0 1 1 1 1	047						
0 0 0 1 1 0 0 0 0	048						
0 0 0 1 1 0 0 0 1	049						
0 0 0 1 1 0 0 1 0	050						
0 0 0 1 1 0 0 1 1	051						
0 0 0 1 1 0 1 0 0	052						
0 0 0 1 1 0 1 0 1	053						
0 0 0 1 1 0 1 1 0	054						
0 0 0 1 1 0 1 1 1	055						
0 0 0 1 1 1 0 0 0	056						
0 0 0 1 1 1 0 0 1	057						
0 0 0 1 1 1 0 1 0	058						
0 0 0 1 1 1 0 1 1	059						
0 0 0 1 1 1 1 0 0	060						
0 0 0 1 1 1 1 0 1	061						
0 0 0 1 1 1 1 1 0	062						
0 0 0 1 1 1 1 1 1	063						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
0 0 1 0 0 0 0 0 0	064						
0 0 1 0 0 0 0 0 1	065						
0 0 1 0 0 0 0 1 0	066						
0 0 1 0 0 0 0 1 1	067						
0 0 1 0 0 0 1 0 0	068						
0 0 1 0 0 0 1 0 1	069						
0 0 1 0 0 0 1 1 0	070						
0 0 1 0 0 0 1 1 1	071						
0 0 1 0 0 1 0 0 0	072						
0 0 1 0 0 1 0 0 1	073						
0 0 1 0 0 1 0 1 0	074						
0 0 1 0 0 1 0 1 1	075						
0 0 1 0 0 1 1 0 0	076						
0 0 1 0 0 1 1 0 1	077						
0 0 1 0 0 1 1 1 0	078						
0 0 1 0 0 1 1 1 1	079						
0 0 1 0 1 0 0 0 0	080						
0 0 1 0 1 0 0 0 1	081						
0 0 1 0 1 0 0 1 0	082						
0 0 1 0 1 0 0 1 1	083						
0 0 1 0 1 0 1 0 0	084						
0 0 1 0 1 0 1 0 1	085						
0 0 1 0 1 0 1 1 0	086						
0 0 1 0 1 0 1 1 1	087						
0 0 1 0 1 1 0 0 0	088						
0 0 1 0 1 1 0 0 1	089						
0 0 1 0 1 1 0 1 0	090						
0 0 1 0 1 1 0 1 1	091						
0 0 1 0 1 1 1 0 0	092						
0 0 1 0 1 1 1 0 1	093						
0 0 1 0 1 1 1 1 0	094						
0 0 1 0 1 1 1 1 1	095						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
0 0 1 1 0 0 0 0 0	096						
0 0 1 1 0 0 0 0 1	097						
0 0 1 1 0 0 0 1 0	098						
0 0 1 1 0 0 0 1 1	099						
0 0 1 1 0 0 1 0 0	100						
0 0 1 1 0 0 1 0 1	101						
0 0 1 1 0 0 1 1 0	102						
0 0 1 1 0 0 1 1 1	103						
0 0 1 1 0 1 0 0 0	104						
0 0 1 1 0 1 0 0 1	105						
0 0 1 1 0 1 0 1 0	106						
0 0 1 1 0 1 0 1 1	107						
0 0 1 1 0 1 1 0 0	108						
0 0 1 1 0 1 1 0 1	109						
0 0 1 1 0 1 1 1 0	110						
0 0 1 1 0 1 1 1 1	111						
0 0 1 1 1 0 0 0 0	112						
0 0 1 1 1 0 0 0 1	113						
0 0 1 1 1 0 0 1 0	114						
0 0 1 1 1 0 0 1 1	116						
0 0 1 1 1 0 1 0 0	116						
0 0 1 1 1 0 1 0 1	117						
0 0 1 1 1 0 1 1 0	118						
0 0 1 1 1 0 1 1 1	119						
0 0 1 1 1 1 0 0 0	120						
0 0 1 1 1 1 0 0 1	121						
0 0 1 1 1 1 0 1 0	122						
0 0 1 1 1 1 0 1 1	123						
0 0 1 1 1 1 1 0 0	124						
0 0 1 1 1 1 1 0 1	125						
0 0 1 1 1 1 1 1 0	126						
0 0 1 1 1 1 1 1 1	127						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 0 0 0 0 0 0 0	128						
0 1 0 0 0 0 0 0 1	129						
0 1 0 0 0 0 0 1 0	130						
0 1 0 0 0 0 0 1 1	131						
0 1 0 0 0 0 1 0 0	132						
0 1 0 0 0 0 1 0 1	133						
0 1 0 0 0 0 1 1 0	134						
0 1 0 0 0 0 1 1 1	135						
0 1 0 0 0 1 0 0 0	136						
0 1 0 0 0 1 0 0 1	137						
0 1 0 0 0 1 0 1 0	138						
0 1 0 0 0 1 0 1 1	139						
0 1 0 0 0 1 1 0 0	140						
0 1 0 0 0 1 1 0 1	141						
0 1 0 0 0 1 1 1 0	142						
0 1 0 0 0 1 1 1 1	143						
0 1 0 0 1 0 0 0 0	144						
0 1 0 0 1 0 0 0 1	145						
0 1 0 0 1 0 0 1 0	146						
0 1 0 0 1 0 0 1 1	147						
0 1 0 0 1 0 1 0 0	148						
0 1 0 0 1 0 1 0 1	149						
0 1 0 0 1 0 1 1 0	150						
0 1 0 0 1 0 1 1 1	151						
0 1 0 0 1 1 0 0 0	152						
0 1 0 0 1 1 0 0 1	153						
0 1 0 0 1 1 0 1 0	154						
0 1 0 0 1 1 0 1 1	155						
0 1 0 0 1 1 1 0 0	156						
0 1 0 0 1 1 1 0 1	157						
0 1 0 0 1 1 1 1 0	158						
0 1 0 0 1 1 1 1 1	159						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 0 1 0 0 0 0 0	160						
0 1 0 1 0 0 0 0 1	161						
0 1 0 1 0 0 0 1 0	162						
0 1 0 1 0 0 0 1 1	163						
0 1 0 1 0 0 1 0 0	164						
0 1 0 1 0 0 1 0 1	165						
0 1 0 1 0 0 1 1 0	166						
0 1 0 1 0 0 1 1 1	167						
0 1 0 1 0 1 0 0 0	168						
0 1 0 1 0 1 0 0 1	169						
0 1 0 1 0 1 0 1 0	170						
0 1 0 1 0 1 0 1 1	171						
0 1 0 1 0 1 1 0 0	172						
0 1 0 1 0 1 1 0 1	173						
0 1 0 1 0 1 1 1 0	174						
0 1 0 1 0 1 1 1 1	175						
0 1 0 1 1 0 0 0 0	176						
0 1 0 1 1 0 0 0 1	177						
0 1 0 1 1 0 0 1 0	178						
0 1 0 1 1 0 0 1 1	179						
0 1 0 1 1 0 1 0 0	180						
0 1 0 1 1 0 1 0 1	181						
0 1 0 1 1 0 1 1 0	182						
0 1 0 1 1 0 1 1 1	183						
0 1 0 1 1 1 0 0 0	184						
0 1 0 1 1 1 0 0 1	185						
0 1 0 1 1 1 0 1 0	186						
0 1 0 1 1 1 0 1 1	187						
0 1 0 1 1 1 1 0 0	188						
0 1 0 1 1 1 1 0 1	189						
0 1 0 1 1 1 1 1 0	190						
0 1 0 1 1 1 1 1 1	191						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
0 1 1 0 0 0 0 0 0	192						
0 1 1 0 0 0 0 0 1	193						
0 1 1 0 0 0 0 1 0	194						
0 1 1 0 0 0 0 1 1	195						
0 1 1 0 0 0 1 0 0	196						
0 1 1 0 0 0 1 0 1	197						
0 1 1 0 0 0 1 1 0	198						
0 1 1 0 0 0 1 1 1	199						
0 1 1 0 0 1 0 0 0	200						
0 1 1 0 0 1 0 0 1	201						
0 1 1 0 0 1 0 1 0	202						
0 1 1 0 0 1 0 1 1	203						
0 1 1 0 0 1 1 0 0	204						
0 1 1 0 0 1 1 0 1	205						
0 1 1 0 0 1 1 1 0	206						
0 1 1 0 0 1 1 1 1	207						
0 1 1 0 1 0 0 0 0	208						
0 1 1 0 1 0 0 0 1	209						
0 1 1 0 1 0 0 1 0	210						
0 1 1 0 1 0 0 1 1	211						
0 1 1 0 1 0 1 0 0	212						
0 1 1 0 1 0 1 0 1	213						
0 1 1 0 1 0 1 1 0	214						
0 1 1 0 1 0 1 1 1	215						
0 1 1 0 1 1 0 0 0	216						
0 1 1 0 1 1 0 0 1	217						
0 1 1 0 1 1 0 1 0	218						
0 1 1 0 1 1 0 1 1	219						
0 1 1 0 1 1 1 0 0	220						
0 1 1 0 1 1 1 0 1	221						
0 1 1 0 1 1 1 1 0	222						
0 1 1 0 1 1 1 1 1	223						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
0 1 1 1 0 0 0 0 0	224						
0 1 1 1 0 0 0 0 1	225						
0 1 1 1 0 0 0 1 0	226						
0 1 1 1 0 0 0 1 1	227						
0 1 1 1 0 0 1 0 0	228						
0 1 1 1 0 0 1 0 1	229						
0 1 1 1 0 0 1 1 0	230						
0 1 1 1 0 0 1 1 1	231						
0 1 1 1 0 1 0 0 0	232						
0 1 1 1 0 1 0 0 1	233						
0 1 1 1 0 1 0 1 0	234						
0 1 1 1 0 1 0 1 1	235						
0 1 1 1 0 1 1 0 0	236						
0 1 1 1 0 1 1 0 1	237						
0 1 1 1 0 1 1 1 0	238						
0 1 1 1 0 1 1 1 1	239						
0 1 1 1 1 0 0 0 0	240						
0 1 1 1 1 0 0 0 1	241						
0 1 1 1 1 0 0 1 0	242						
0 1 1 1 1 0 0 1 1	243						
0 1 1 1 1 0 1 0 0	244						
0 1 1 1 1 0 1 0 1	245						
0 1 1 1 1 0 1 1 0	246						
0 1 1 1 1 0 1 1 1	247						
0 1 1 1 1 1 0 0 0	248						
0 1 1 1 1 1 0 0 1	249						
0 1 1 1 1 1 0 1 0	250						
0 1 1 1 1 1 0 1 1	251						
0 1 1 1 1 1 1 0 0	252						
0 1 1 1 1 1 1 0 1	253						
0 1 1 1 1 1 1 1 0	254						
0 1 1 1 1 1 1 1 1	255						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O6	O4	O3	O2	O1	
1 0 0 0 0 0 0 0 0	256						
1 0 0 0 0 0 0 0 1	257						
1 0 0 0 0 0 0 1 0	258						
1 0 0 0 0 0 0 1 1	259						
1 0 0 0 0 0 1 0 0	260						
1 0 0 0 0 0 1 0 1	261						
1 0 0 0 0 0 1 1 0	262						
1 0 0 0 0 0 1 1 1	263						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O6	O4	O3	O2	O1	
1 0 0 1 0 0 0 0 0	288						
1 0 0 1 0 0 0 0 1	289						
1 0 0 1 0 0 0 1 0	290						
1 0 0 1 0 0 0 1 1	291						
1 0 0 1 0 0 1 0 0	292						
1 0 0 1 0 0 1 0 1	293						
1 0 0 1 0 0 1 1 0	294						
1 0 0 1 0 0 1 1 1	295						

1 0 0 0 0 1 0 0 0	264						
1 0 0 0 0 1 0 0 1	265						
1 0 0 0 0 1 0 1 0	266						
1 0 0 0 0 1 0 1 1	267						
1 0 0 0 0 1 1 0 0	268						
1 0 0 0 0 1 1 0 1	269						
1 0 0 0 0 1 1 1 0	270						
1 0 0 0 0 1 1 1 1	271						

1 0 0 1 0 1 0 0 0	296						
1 0 0 1 0 1 0 0 1	297						
1 0 0 1 0 1 0 1 0	298						
1 0 0 1 0 1 0 1 1	299						
1 0 0 1 0 1 1 0 0	300						
1 0 0 1 0 1 1 0 1	301						
1 0 0 1 0 1 1 1 0	302						
1 0 0 1 0 1 1 1 1	303						

1 0 0 0 1 0 0 0 0	272						
1 0 0 0 1 0 0 0 1	273						
1 0 0 0 1 0 0 1 0	274						
1 0 0 0 1 0 0 1 1	275						
1 0 0 0 1 0 1 0 0	276						
1 0 0 0 1 0 1 0 1	277						
1 0 0 0 1 0 1 1 0	278						
1 0 0 0 1 0 1 1 1	279						

1 0 0 1 1 0 0 0 0	304						
1 0 0 1 1 0 0 0 1	305						
1 0 0 1 1 0 0 1 0	306						
1 0 0 1 1 0 0 1 1	307						
1 0 0 1 1 0 1 0 0	308						
1 0 0 1 1 0 1 0 1	309						
1 0 0 1 1 0 1 1 0	310						
1 0 0 1 1 0 1 1 1	311						

1 0 0 0 1 1 0 0 0	280						
1 0 0 0 1 1 0 0 1	281						
1 0 0 0 1 1 0 1 0	282						
1 0 0 0 1 1 0 1 1	283						
1 0 0 0 1 1 1 0 0	284						
1 0 0 0 1 1 1 0 1	285						
1 0 0 0 1 1 1 1 0	286						
1 0 0 0 1 1 1 1 1	287						

1 0 0 1 1 1 0 0 0	312						
1 0 0 1 1 1 0 0 1	313						
1 0 0 1 1 1 0 1 0	314						
1 0 0 1 1 1 0 1 1	315						
1 0 0 1 1 1 1 0 0	316						
1 0 0 1 1 1 1 0 1	317						
1 0 0 1 1 1 1 1 0	318						
1 0 0 1 1 1 1 1 1	319						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
1 0 1 0 0 0 0 0 0	320						
1 0 1 0 0 0 0 0 1	321						
1 0 1 0 0 0 0 1 0	322						
1 0 1 0 0 0 0 1 1	323						
1 0 1 0 0 0 1 0 0	324						
1 0 1 0 0 0 1 0 1	325						
1 0 1 0 0 0 1 1 0	326						
1 0 1 0 0 0 1 1 1	327						
1 0 1 0 0 1 0 0 0	328						
1 0 1 0 0 1 0 0 1	329						
1 0 1 0 0 1 0 1 0	330						
1 0 1 0 0 1 0 1 1	331						
1 0 1 0 0 1 1 0 0	332						
1 0 1 0 0 1 1 0 1	333						
1 0 1 0 0 1 1 1 0	334						
1 0 1 0 0 1 1 1 1	335						
1 0 1 0 1 0 0 0 0	336						
1 0 1 0 1 0 0 0 1	337						
1 0 1 0 1 0 0 1 0	338						
1 0 1 0 1 0 0 1 1	339						
1 0 1 0 1 0 1 0 0	340						
1 0 1 0 1 0 1 0 1	341						
1 0 1 0 1 0 1 1 0	342						
1 0 1 0 1 0 1 1 1	343						
1 0 1 0 1 1 0 0 0	344						
1 0 1 0 1 1 0 0 1	345						
1 0 1 0 1 1 0 1 0	346						
1 0 1 0 1 1 0 1 1	347						
1 0 1 0 1 1 1 0 0	348						
1 0 1 0 1 1 1 0 1	349						
1 0 1 0 1 1 1 1 0	350						
1 0 1 0 1 1 1 1 1	351						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
1 0 1 1 0 0 0 0 0	352						
1 0 1 1 0 0 0 0 1	353						
1 0 1 1 0 0 0 1 0	354						
1 0 1 1 0 0 0 1 1	355						
1 0 1 1 0 0 1 0 0	356						
1 0 1 1 0 0 1 0 1	357						
1 0 1 1 0 0 1 1 0	358						
1 0 1 1 0 0 1 1 1	359						
1 0 1 1 0 1 0 0 0	360						
1 0 1 1 0 1 0 0 1	361						
1 0 1 1 0 1 0 1 0	362						
1 0 1 1 0 1 0 1 1	363						
1 0 1 1 0 1 1 0 0	364						
1 0 1 1 0 1 1 0 1	365						
1 0 1 1 0 1 1 1 0	366						
1 0 1 1 0 1 1 1 1	367						
1 0 1 1 1 0 0 0 0	368						
1 0 1 1 1 0 0 0 1	369						
1 0 1 1 1 0 0 1 0	370						
1 0 1 1 1 0 0 1 1	371						
1 0 1 1 1 0 1 0 0	372						
1 0 1 1 1 0 1 0 1	373						
1 0 1 1 1 0 1 1 0	374						
1 0 1 1 1 0 1 1 1	375						
1 0 1 1 1 1 0 0 0	376						
1 0 1 1 1 1 0 0 1	377						
1 0 1 1 1 1 0 1 0	378						
1 0 1 1 1 1 0 1 1	379						
1 0 1 1 1 1 1 0 0	380						
1 0 1 1 1 1 1 0 1	381						
1 0 1 1 1 1 1 1 0	382						
1 0 1 1 1 1 1 1 1	383						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
1 1 0 0 0 0 0 0 0	384						
1 1 0 0 0 0 0 0 1	385						
1 1 0 0 0 0 0 1 0	386						
1 1 0 0 0 0 0 1 1	387						
1 1 0 0 0 0 1 0 0	388						
1 1 0 0 0 0 1 0 1	389						
1 1 0 0 0 0 1 1 0	390						
1 1 0 0 0 0 1 1 1	391						
1 1 0 0 0 1 0 0 0	392						
1 1 0 0 0 1 0 0 1	393						
1 1 0 0 0 1 0 1 0	394						
1 1 0 0 0 1 0 1 1	395						
1 1 0 0 0 1 1 0 0	396						
1 1 0 0 0 1 1 0 1	397						
1 1 0 0 0 1 1 1 0	398						
1 1 0 0 0 1 1 1 1	399						
1 1 0 0 1 0 0 0 0	400						
1 1 0 0 1 0 0 0 1	401						
1 1 0 0 1 0 0 1 0	402						
1 1 0 0 1 0 0 1 1	403						
1 1 0 0 1 0 1 0 0	404						
1 1 0 0 1 0 1 0 1	405						
1 1 0 0 1 0 1 1 0	406						
1 1 0 0 1 0 1 1 1	407						
1 1 0 0 1 1 0 0 0	408						
1 1 0 0 1 1 0 0 1	409						
1 1 0 0 1 1 0 1 0	410						
1 1 0 0 1 1 0 1 1	411						
1 1 0 0 1 1 1 0 0	412						
1 1 0 0 1 1 1 0 1	413						
1 1 0 0 1 1 1 1 0	414						
1 1 0 0 1 1 1 1 1	415						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
1 1 0 1 0 0 0 0 0	416						
1 1 0 1 0 0 0 0 1	417						
1 1 0 1 0 0 0 1 0	418						
1 1 0 1 0 0 0 1 1	419						
1 1 0 1 0 0 1 0 0	420						
1 1 0 1 0 0 1 0 1	421						
1 1 0 1 0 0 1 1 0	422						
1 1 0 1 0 0 1 1 1	423						
1 1 0 1 0 1 0 0 0	424						
1 1 0 1 0 1 0 0 1	425						
1 1 0 1 0 1 0 1 0	426						
1 1 0 1 0 1 0 1 1	427						
1 1 0 1 0 1 1 0 0	428						
1 1 0 1 0 1 1 0 1	429						
1 1 0 1 0 1 1 1 0	430						
1 1 0 1 0 1 1 1 1	431						
1 1 0 1 1 0 0 0 0	432						
1 1 0 1 1 0 0 0 1	433						
1 1 0 1 1 0 0 1 0	434						
1 1 0 1 1 0 0 1 1	435						
1 1 0 1 1 0 1 0 0	436						
1 1 0 1 1 0 1 0 1	437						
1 1 0 1 1 0 1 1 0	438						
1 1 0 1 1 0 1 1 1	439						
1 1 0 1 1 1 0 0 0	440						
1 1 0 1 1 1 0 0 1	441						
1 1 0 1 1 1 0 1 0	442						
1 1 0 1 1 1 0 1 1	443						
1 1 0 1 1 1 1 0 0	444						
1 1 0 1 1 1 1 0 1	445						
1 1 0 1 1 1 1 1 0	446						
1 1 0 1 1 1 1 1 1	447						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
1 1 1 0 0 0 0 0 0	448						
1 1 1 0 0 0 0 0 1	449						
1 1 1 0 0 0 0 1 0	450						
1 1 1 0 0 0 0 1 1	451						
1 1 1 0 0 0 1 0 0	452						
1 1 1 0 0 0 1 0 1	453						
1 1 1 0 0 0 1 1 0	454						
1 1 1 0 0 0 1 1 1	455						
1 1 1 0 0 1 0 0 0	456						
1 1 1 0 0 1 0 0 1	457						
1 1 1 0 0 1 0 1 0	458						
1 1 1 0 0 1 0 1 1	459						
1 1 1 0 0 1 1 0 0	460						
1 1 1 0 0 1 1 0 1	461						
1 1 1 0 0 1 1 1 0	462						
1 1 1 0 0 1 1 1 1	463						
1 1 1 0 1 0 0 0 0	464						
1 1 1 0 1 0 0 0 1	465						
1 1 1 0 1 0 0 1 0	466						
1 1 1 0 1 0 0 1 1	467						
1 1 1 0 1 0 1 0 0	468						
1 1 1 0 1 0 1 0 1	469						
1 1 1 0 1 0 1 1 0	470						
1 1 1 0 1 0 1 1 1	471						
1 1 1 0 1 1 0 0 0	472						
1 1 1 0 1 1 0 0 1	473						
1 1 1 0 1 1 0 1 0	474						
1 1 1 0 1 1 0 1 1	475						
1 1 1 0 1 1 1 0 0	476						
1 1 1 0 1 1 1 0 1	477						
1 1 1 0 1 1 1 1 0	478						
1 1 1 0 1 1 1 1 1	479						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		O5	O4	O3	O2	O1	
1 1 1 1 0 0 0 0 0	480						
1 1 1 1 0 0 0 0 1	481						
1 1 1 1 0 0 0 1 0	482						
1 1 1 1 0 0 0 1 1	483						
1 1 1 1 0 0 1 0 0	484						
1 1 1 1 0 0 1 0 1	485						
1 1 1 1 0 0 1 1 0	486						
1 1 1 1 0 0 1 1 1	487						
1 1 1 1 0 1 0 0 0	488						
1 1 1 1 0 1 0 0 1	489						
1 1 1 1 0 1 0 1 0	490						
1 1 1 1 0 1 0 1 1	491						
1 1 1 1 0 1 1 0 0	492						
1 1 1 1 0 1 1 0 1	493						
1 1 1 1 0 1 1 1 0	494						
1 1 1 1 0 1 1 1 1	495						
1 1 1 1 1 0 0 0 0	496						
1 1 1 1 1 0 0 0 1	497						
1 1 1 1 1 0 0 1 0	498						
1 1 1 1 1 0 0 1 1	499						
1 1 1 1 1 0 1 0 0	500						
1 1 1 1 1 0 1 0 1	501						
1 1 1 1 1 0 1 1 0	502						
1 1 1 1 1 0 1 1 1	503						
1 1 1 1 1 1 0 0 0	504						
1 1 1 1 1 1 0 0 1	505						
1 1 1 1 1 1 0 1 0	506						
1 1 1 1 1 1 0 1 1	507						
1 1 1 1 1 1 1 0 0	508						
1 1 1 1 1 1 1 0 1	509						
1 1 1 1 1 1 1 1 0	510						
1 1 1 1 1 1 1 1 1	511						

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP ____

TELEPHONE _____

AUTHORIZED SIGNATURE _____

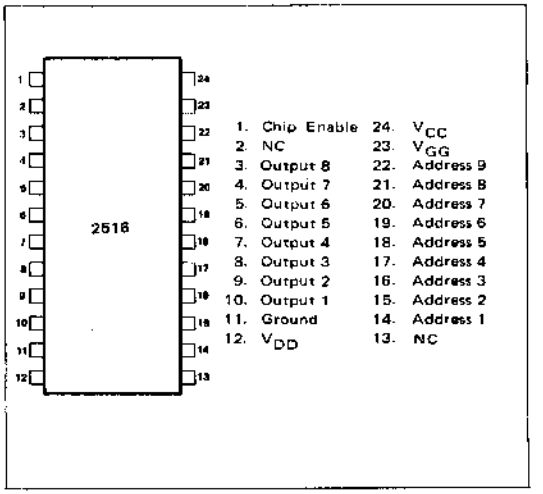
DATE _____

CUSTOMER PRINT OR ID NO. _____

PURCHASE ORDER NUMBER _____

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS) _____

PIN CONFIGURATION



INTRODUCTION

The Signetics 2516 is a high speed silicon gate MOS read-only memories whose organization is specially suited for 64 X 6 X 8 vertical scan character generation.

MAJOR FEATURES OF THE 2516

- 64 X 6 X 8 CHARACTER MATRIX
- COLUMN OUTPUT
- ACCESS TIME 450ns TYPICALLY
- STATIC OPERATION
- TTL/DTL COMPATIBLE
- TRI-STATE OUTPUTS (HIGH-LOW-DISCONNECTED) FOR POWERFUL BUSSING CAPABILITY
- +5, -5, -12V POWER SUPPLIES
- 24-PIN SIGNETICS SILICONE DIP
- SIGNETICS SILICON GATE PROCESS TECHNOLOGY FOR PERFORMANCE AND RELIABILITY

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 6 dots horizontally and 8 dots vertically. A three bit-binary address code (A_1 through A_3) selects 1 or 6 columns. Eight outputs display a complete column of the character matrix. See Figure 1.

CHARACTER FORMAT

ROW ADDRESS

COLUMN ADDRESS							
A_3	0	0	0	0	1	1	
A_2	0	0	1	1	0	0	
A_1	0	1	0	1	0	1	
	0	0	0	0	0	0	O_1
	0	0	1	1	1	0	O_2
	0	1	0	0	0	1	O_3
	0	1	0	0	0	0	O_4
	0	0	1	1	1	0	O_5
	0	0	0	0	0	1	O_6
	0	1	0	0	0	1	O_7
	0	0	1	1	1	0	O_8

EXAMPLE "8"

FIGURE 1

CHARACTER ADDRESS

	CHARACTER ADDRESS					
	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

FIGURE 2

STANDARD PATTERN

A standard ASCII Character Font is available for the 2516. This device (2516NX/CM2150) may be used for ASCII character generation or for device evaluation.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for custom device will consist of the basic product type followed by a unique "CM" number assigned by Signetics. For example, "2516NX/CM2151"

- **Programming with punched cards.**
  For maximum accuracy and minimum cost and turnaround time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- **Programming with written truth table.**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

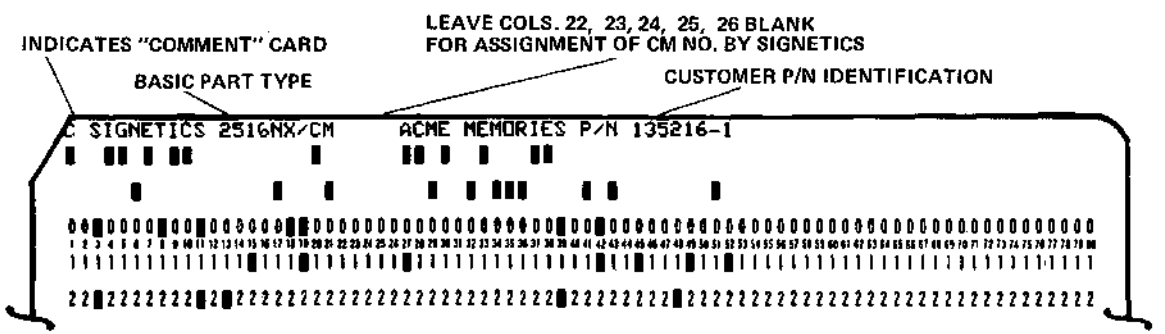
Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. +3.6V minimum). Similarly, a "1" address input level is interpreted as +3.2V minimum.

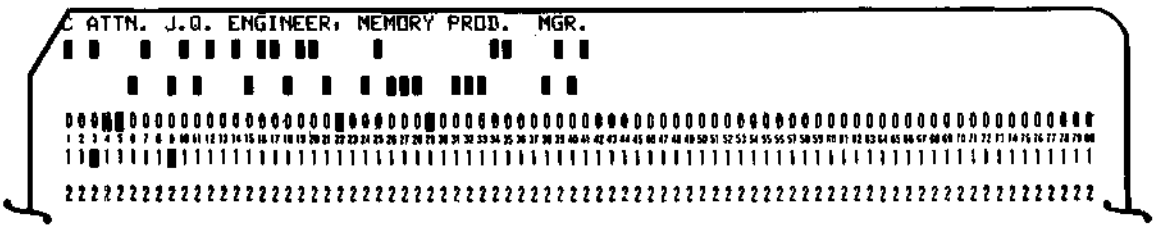
Undefined addresses result in "1" level outputs.

IDENTIFICATION CARDS

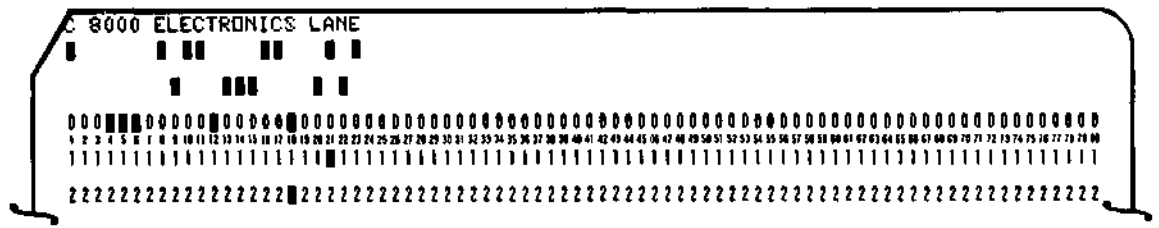


IDENTIFICATION CARDS (Cont'd)

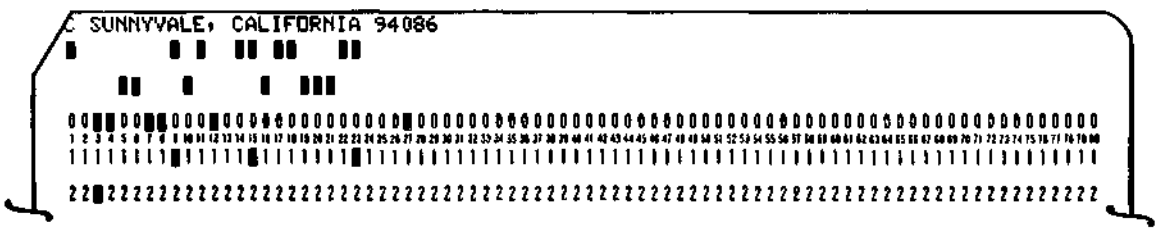
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS COMPUTER GENERATED TRUTH TABLE



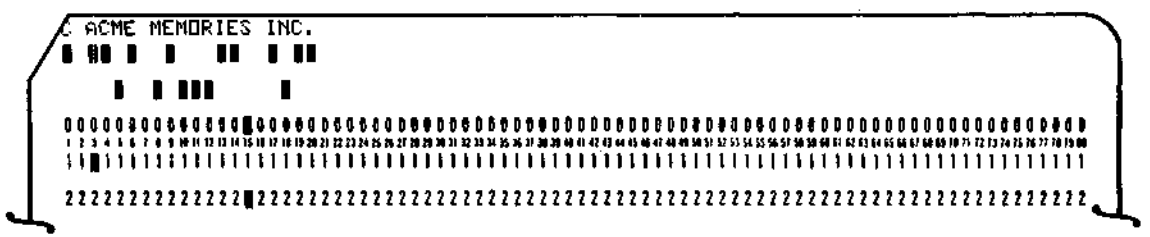
STREET ADDRESS



CITY STATE ZIP



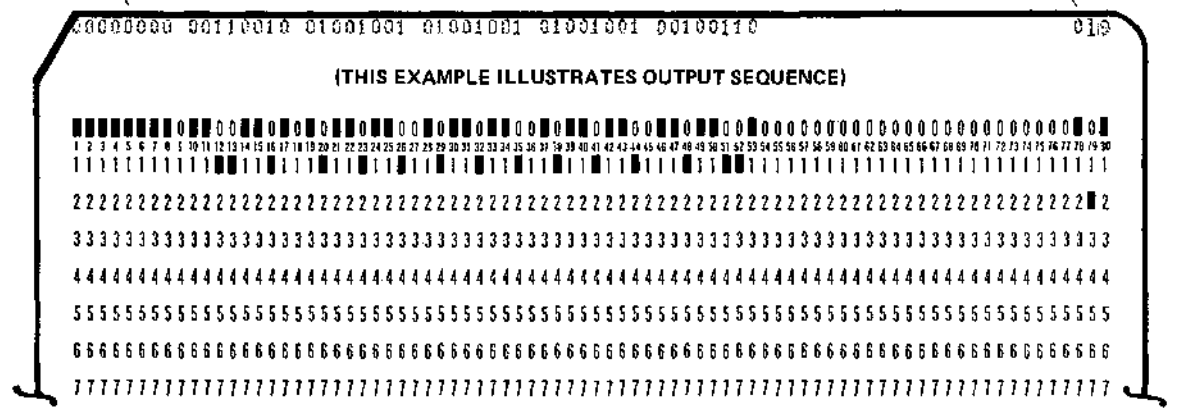
COMPANY NAME



DATA CARDS

OUTPUTS O_8 THROUGH O_1 RESPECTIVELY

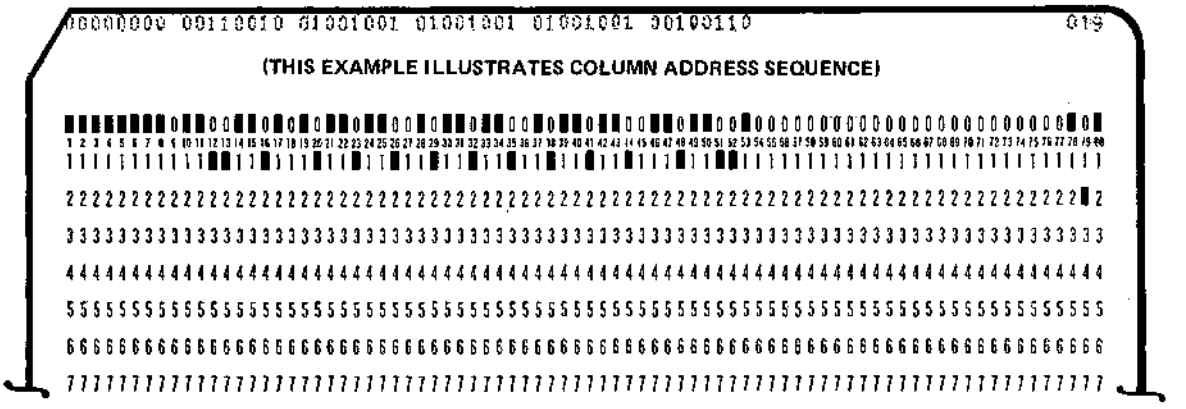
DECIMAL CHARACTER ADDRESS
(DATA CARD NUMBER 001 THRU 064)



(THIS EXAMPLE ILLUSTRATES OUTPUT SEQUENCE)

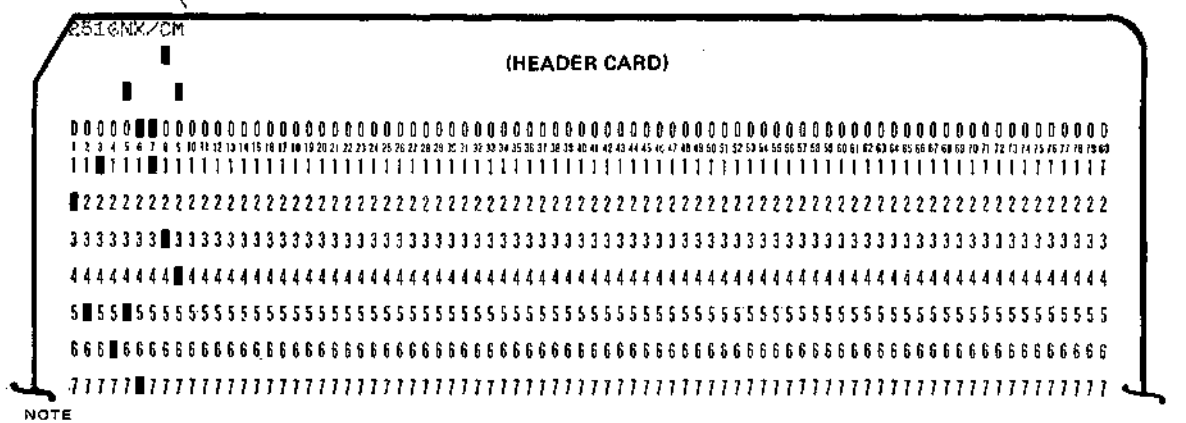
COLUMN ADDRESS(A_3,A_2,A_1)

000 001 010 011 100 101



(THIS EXAMPLE ILLUSTRATES COLUMN ADDRESS SEQUENCE)

BASIC DEVICE TYPE
LEAVE COLS. 10, 11, 12, 13 BLANK FOR ASSIGNMENT OF CM NO. BY SIGNETICS



(HEADER CARD)

NOTE

"Character" number is in columns 78, 79, and 80.

Character Number						001
Column Binary Address	Column Decimal Address					
	000	001	002	003	004	005
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						002
Column Binary Address	Column Decimal Address					
	008	009	010	011	012	013
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						003
Column Binary Address	Column Decimal Address					
	016	017	018	019	020	021
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						004
Column Binary Address	Column Decimal Address					
	024	026	026	027	028	029
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						005
Column Binary Address	Column Decimal Address					
	032	033	034	035	036	037
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						006
Column Binary Address	Column Decimal Address					
	040	041	042	043	044	045
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						007
Column Binary Address	Column Decimal Address					
	048	049	060	051	052	053
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number						008
Column Binary Address	Column Decimal Address					
	056	057	058	059	060	061
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 009						
Column Binary Address	Column Decimal Address					
	064	065	066	067	068	069
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 010						
Column Binary Address	Column Decimal Address					
	072	073	074	075	076	077
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 011						
Column Binary Address	Column Decimal Address					
	080	081	082	083	084	085
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 012						
Column Binary Address	Column Decimal Address					
	088	089	090	091	092	093
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 013						
Column Binary Address	Column Decimal Address					
	096	097	098	099	100	101
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 014						
Column Binary Address	Column Decimal Address					
	104	105	106	107	108	109
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 015						
Column Binary Address	Column Decimal Address					
	112	113	114	115	116	117
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 016						
Column Binary Address	Column Decimal Address					
	120	121	122	123	124	125
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	017					
Column Binary Address	Column Decimal Address					
	128	129	130	131	132	133
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	018					
Column Binary Address	Column Decimal Address					
	136	137	138	139	140	141
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	019					
Column Binary Address	Column Decimal Address					
	144	145	146	147	148	149
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	020					
Column Binary Address	Column Decimal Address					
	152	153	154	155	156	157
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	021					
Column Binary Address	Column Decimal Address					
	160	161	162	163	164	165
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	022					
Column Binary Address	Column Decimal Address					
	168	169	170	171	172	173
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	023					
Column Binary Address	Column Decimal Address					
	176	177	178	179	180	181
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	024					
Column Binary Address	Column Decimal Address					
	184	185	186	187	188	189
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	025					
Column Binary Address	Column Decimal Address					
	192	193	194	195	196	197
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	026					
Column Binary Address	Column Decimal Address					
	200	201	202	203	204	205
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	027					
Column Binary Address	Column Decimal Address					
	208	209	210	211	212	213
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	028					
Column Binary Address	Column Decimal Address					
	216	217	218	219	220	221
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	029					
Column Binary Address	Column Decimal Address					
	224	225	226	227	228	229
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	030					
Column Binary Address	Column Decimal Address					
	232	233	234	235	236	237
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	031					
Column Binary Address	Column Decimal Address					
	240	241	242	243	244	245
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	032					
Column Binary Address	Column Decimal Address					
	248	249	250	251	252	253
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 033						
Column Binary Address	Column Decimal Address					
	256	257	258	259	260	261
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 034						
Column Binary Address	Column Decimal Address					
	264	265	266	267	268	269
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 035						
Column Binary Address	Column Decimal Address					
	272	273	274	275	276	277
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 036						
Column Binary Address	Column Decimal Address					
	280	281	282	283	284	285
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 037						
Column Binary Address	Column Decimal Address					
	288	289	290	291	292	293
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 038						
Column Binary Address	Column Decimal Address					
	296	297	298	299	300	301
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 039						
Column Binary Address	Column Decimal Address					
	304	305	306	307	308	309
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 040						
Column Binary Address	Column Decimal Address					
	312	313	314	315	316	317
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 041						
Column Binary Address	Column Decimal Address					
	320	321	322	323	324	326
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 042						
Column Binary Address	Column Decimal Address					
	328	329	330	331	332	333
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 043						
Column Binary Address	Column Decimal Address					
	336	337	338	339	340	341
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 044						
Column Binary Address	Column Decimal Address					
	344	345	346	347	348	349
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 045						
Column Binary Address	Column Decimal Address					
	352	353	354	355	356	357
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 046						
Column Binary Address	Column Decimal Address					
	360	361	362	363	364	365
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 047						
Column Binary Address	Column Decimal Address					
	368	369	370	371	372	373
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 048						
Column Binary Address	Column Decimal Address					
	376	377	378	379	380	381
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 049						
Column Binary Address	Column Decimal Address					
	384	385	386	387	388	389
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 050						
Column Binary Address	Column Decimal Address					
	392	393	394	395	396	397
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 051						
Column Binary Address	Column Decimal Address					
	400	401	402	403	404	405
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 052						
Column Binary Address	Column Decimal Address					
	408	409	410	411	412	413
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 053						
Column Binary Address	Column Decimal Address					
	416	417	418	419	420	421
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 054						
Column Binary Address	Column Decimal Address					
	424	425	426	427	428	429
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 055						
Column Binary Address	Column Decimal Address					
	432	433	434	435	436	437
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number 056						
Column Binary Address	Column Decimal Address					
	440	441	442	443	444	445
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	057					
Column Binary Address	Column Decimal Address					
	448	449	450	451	452	453
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	058					
Column Binary Address	Column Decimal Address					
	456	457	458	459	460	461
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	059					
Column Binary Address	Column Decimal Address					
	464	465	466	467	468	469
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	060					
Column Binary Address	Column Decimal Address					
	472	473	474	475	476	477
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_6						
O_7						
O_8						

Character Number	061					
Column Binary Address	Column Decimal Address					
	480	481	482	483	484	485
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	062					
Column Binary Address	Column Decimal Address					
	488	489	490	491	492	493
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	063					
Column Binary Address	Column Decimal Address					
	496	497	498	499	500	501
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	064					
Column Binary Address	Column Decimal Address					
	504	505	506	507	508	509
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

2530 HIGH SPEED 512 X 8 STATIC READ ONLY MEMORY

PUNCHED CARD INPUT

Header Card

Card No.	Column	Information
1	1-8	"2530N/CM"
	9-14	Blank
	15-19	"CODED"
	20	Blank
	21	Logic state of Output Enable #2, (CS2) - Most Significant Bit.
	22	Logic state of Output Enable #1.
	23	Blank
	24-71	Customer company name.
	72	Blank
	73-80	Date

I.D./Comment Cards:

Card No.	Column	Information
1	1	"C"
	2	Blank
	3-80	Person responsible for reviewing Signetics truth table and Company Name.
2	1	"C"
	2	Blank
	3-80	Customer Street Address
3	1	"C"
	2	Blank
	3-80	Customer City, State, Zip.

Data Cards:

Card No.	Column	Information
1	1-3	Decimal address (blank, blank, 0.)
	4	Blank
	5-12	8-digit binary output (MSB-left)
	13-20	Blank
	21-33	Decimal address, (blank, blank, 1.)
	24	Blank
	25-32	8-Digit binary output (MSB-left)
	33-40	Blank
	41-43	Decimal address, (Blank, blank, 2.)
	44	Blank
	45-52	8-digit binary output (MSB-left)
	53-60	Blank
	61-63	Decimal address, (Blank, blank, 3.)
	64	Blank
	65-72	8-digit binary output (MSB-left)
	73-80	Blank
2		
128		Same format as data card #1.

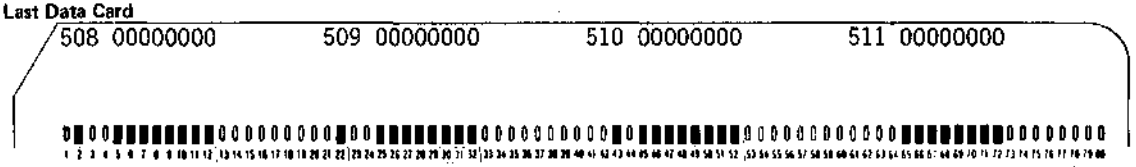
NOTE: MSB = O_9

EXAMPLES:

Header Card

First Data Card

Last Data Card



TRUTH TABLE INPUT:

A truth table may be submitted at a greater non-recurring cost to the customer. A format similar to the one shown below is satisfactory.

INPUT ADDRESS									DECIMAL ADDRESS	OUTPUT							
A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0	0	0	0	0	0	0	0	0	000								
0	0	0	0	0	0	0	0	0	001								
1	1	1	1	1	1	1	1	1	510								
1	1	1	1	1	1	1	1	1	511								

Plus Output Enable 1 and 2 coding.

2526 HIGH SPEED 64 X 9 X 9 CHARACTER GENERATOR

PUNCHED CARD INPUT

Comment/I.D. Cards:

Card No.	Column	Information
1	1	"C"
	2	Blank
	3-17	"SIGNETICS 2526N/CM"
	18-26	Blank
	27-71	Customer I.D. (Company, Project, Part No., etc.)
	72	Blank
	73-80	Date
2	1	"C"
	2	Blank
	3-80	Person responsible for reviewing Signetics truth table.
3	1	"C"
	2	Blank
	3-80	Customer Street Address
4	1	"C"
	2	Blank
	3-80	Customer City, State, Zip.

Card No.	Column	Information
5	1	"C"
	2	Blank
	3-80	Name

Data Cards:

Card No.	Column	Information
1	1-9	Binary outputs of rows 9 through 1, (MSB at 9), first column, first character, (first character is "000"). Logic "1" is high output (3.2V, min.)
	10	Blank
	11-19	Binary outputs of second column, first character.
	20	Blank
	21-29	Third column

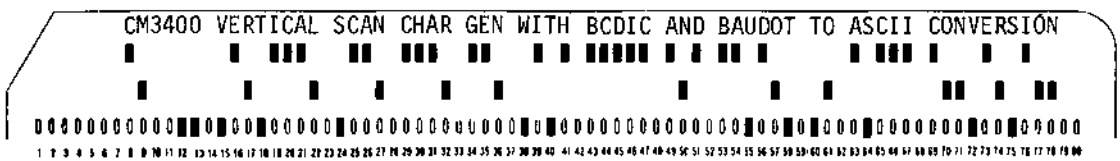
Data Cards (Continued)

Card No.	Column	Information
1 (Cont'd)	30	Blank
	31-39	Fourth column
	40	Blank
	41-49	Fifth column
	50	Blank
	51-59	Sixth column
	60	Blank
	61-69	Seventh column
	70-71	Blank
	72	Data card number of first character, ("1").
	73	Blank
	74-76	Anything - customer option.
	77	Blank
	78-80	Decimal character number, ("000")
2	1-9	Eight column
	10	Blank
2 (Cont'd)	11-19	Ninth column
	20-70	Anything - customer option.
	71	Blank
	72	Data card number of first character, ("2").
	73	Blank
	74-76	Customer option
	77	Blank
	78-80	Decimal character number ("000").
3	1-9 (Etc., as Card 1)	First column, second character, rows 9 through 1 (MSB at 9). Second character is "001".
4	(Etc., as Card 2)	
128	78-80	Decimal character number, ("063").

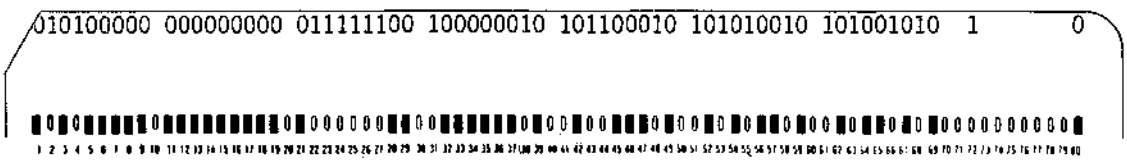
Note: MSB = O_9

EXAMPLES:

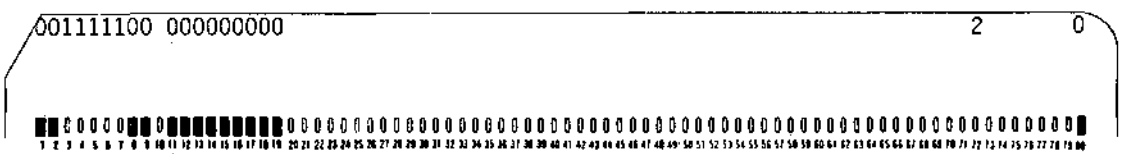
I.D. Card



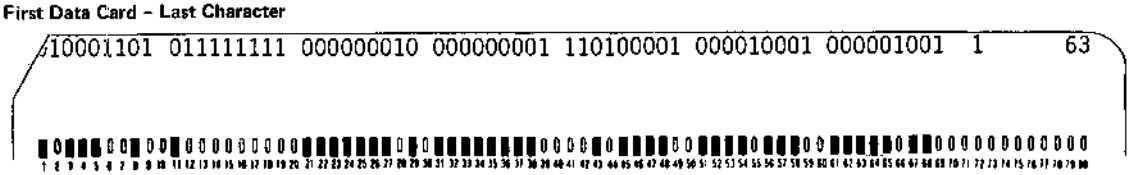
First Data Card - First Character



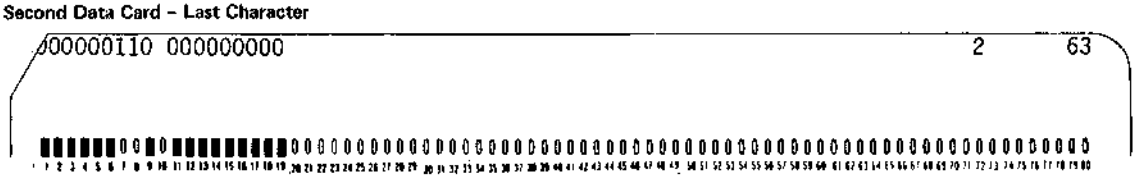
Second Data Card - First Character



First Data Card - Last Character



Second Data Card - Last Character



TRUTH TABLE INPUT:

A truth table may be submitted at a greater non-recurring cost to the customer. A format similar to the one shown below is satisfactory.

ADDRESS										DECIMAL ADDRESS	OUTPUT DATA									CHARACTER
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1		O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	
0	0	0	0	0	0	0	0	0	0	000										FIRST CHARACTER
0	0	0	0	0	0	0	0	0	1	001										
0	0	0	0	0	0	0	0	1	0	002										
0	0	0	0	0	0	0	0	1	1	003										
0	0	0	0	0	0	0	1	0	0	004										
0	0	0	0	0	0	0	1	0	1	005										
0	0	0	0	0	0	0	1	1	0	006										
0	0	0	0	0	0	0	1	1	1	007										
0	0	0	0	0	0	1	0	0	0	008										
0	0	0	0	0	0	1	0	0	0	009										
0	0	0	0	0	0	1	0	0	1	010										
										Etc.										
										503										LAST CHARACTER
										504										
										505										
										506										
										507										
										508										
										509										
										510										
										511										

INTRODUCTION

The 2526 is a high speed 5,184-bit Static Read-Only Memory. It may be organized as 64 x 9 x 9 for use as a character generator in dot matrix displays, or as a 512 x 9 ROM for general purpose use. It features TTL compatible inputs, three-state TTL compatible outputs, two standard supply voltages (+5, −12), output data latches, and less than 700ns access time. The 2526 is fabricated using Signetics P-MOS silicon gate process and is packaged in a 24-pin silicone dual in-line package.

INPUT CIRCUITS

The inputs to the 2526 use a configuration similar to that used in most of the other 2500 series products. Interface requirements with TTL circuitry are described in detail in the Signetics MOS Handbook. In general, a standard TTL gate driving only the 2526 does not require any interfacing resistors. See Figure 1. If another TTL gate is driven in addition to the 2526, a 10k ohm pull-up resistor will improve the input noise margins.

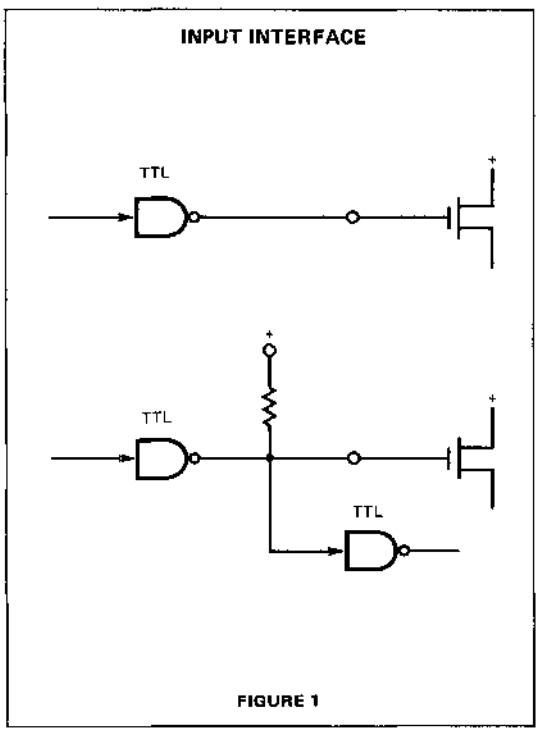


FIGURE 1

OUTPUT CIRCUITS

The outputs from the 2526 use a three-state push-pull configuration that allows wired-OR connection of several circuits for expanded capacity. The push-pull circuitry provides low impedance outputs for both high and low output voltages. See Figure 2. For a low output voltage Q_2 is turned ON and Q_1 is turned OFF with Q_3 and Q_4 kept OFF by a high Output Enable voltage. For a high output voltage Q_1 is turned ON and Q_2 is turned OFF while Q_3 and Q_4 are OFF. When the Output Enable voltage goes low, however, both Q_3 and Q_4 are turned ON, keeping Q_1 and Q_2 both OFF for any condition the output latch assumes. In this state the output of the 2526 is essentially floating,allowing other circuits to dominate the output line.

Figure 3 shows one way to make use of this three-state output. Two 2526 Character Generators are tied together at their outputs and fed to the receiving logic circuitry, e.g., a parallel to serial converter. One 2526 can contain the dot matrix information for upper case characters and the other can contain the lower case information, thus providing a full 128 character set. All inputs for the two generators are tied in parallel except the Output Enables which serve as A11 address inputs. One 2526 receives the A11 signal and the other receives $\overline{A11}$. In this way only one set of outputs at a time will activate the output lines. If the system configuration requires periods where neither output is active, that fact can be gated with A11 to turn off both Output Enable signals. To reduce power dissipation, the A11 information can be gated with the READ signals to avoid turning on the unused 2526.

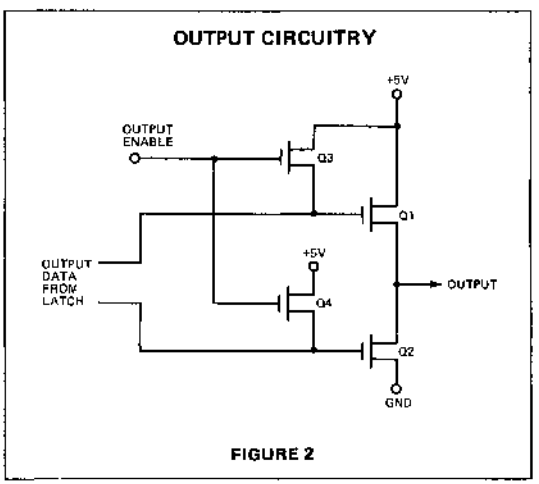


FIGURE 2

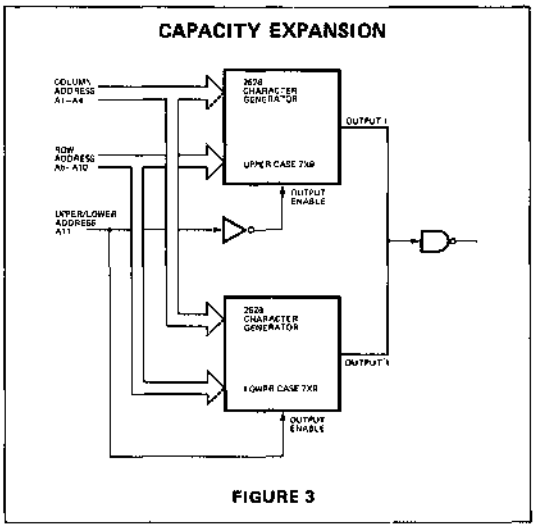


FIGURE 3

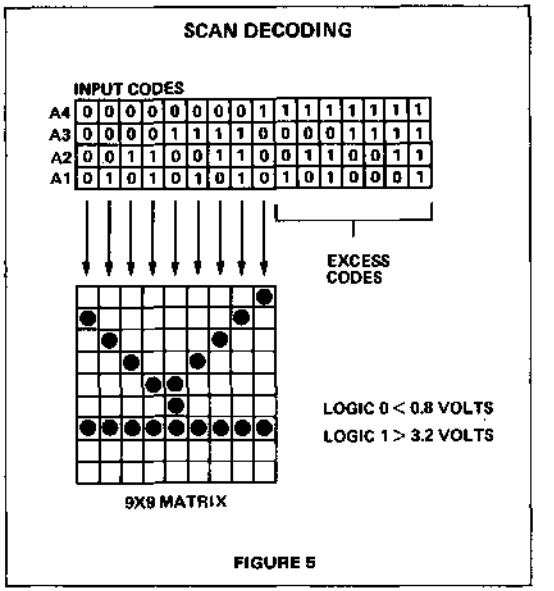


FIGURE 5

ADDRESS DECODING

The Signetics 2526 Character Generator is organized to provide 64 character locations with each location described by a 9 x 9 matrix of bits. The block diagram in Figure 4 shows the address assignments for the character and scan functions. The six address inputs A5 through A10 are decoded directly to provide a 1-of-64 character selection. The four address inputs A1 through A4 are decoded to provide a 1-of-9 selection of scans within each character. Since four address lines can generate 16 scan selections instead of only 9, there are seven excess codes. See Figure 5. The 1-of-9 scan decoder forces the excess input codes to generate all logic "1's" at the output latches. The address decoding circuits are only activated during a READ operation in order to save power when the memory is not being used.

TIMING

The timing diagram in Figure 6 shows how the READ signal controls the operation of the memory. The address inputs propagate through the decoders and the bit matrix when READ goes low. The output data are strobed into the latches when READ goes high. The state of the OUTPUT ENABLE signal determines whether or not the latched data are transferred to the outputs. With OUTPUT ENABLE high, the worst case access time from stable addresses to valid output data is 700ns. Notice that addresses must be stable for only a short period of time so that address changes may be made in parallel with the access operations. Once the data are set into the latches, they remain stable for a full READ cycle until the next cycle's data are available.

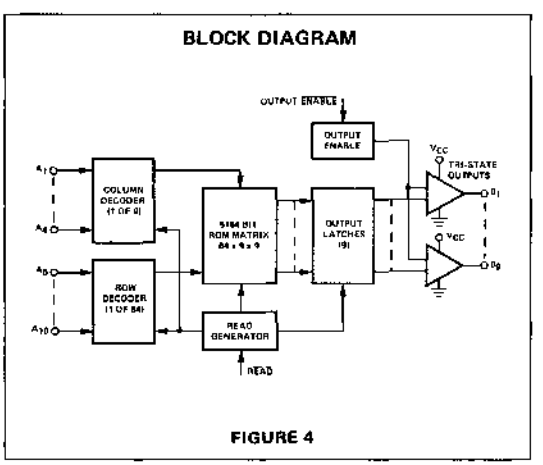


FIGURE 4

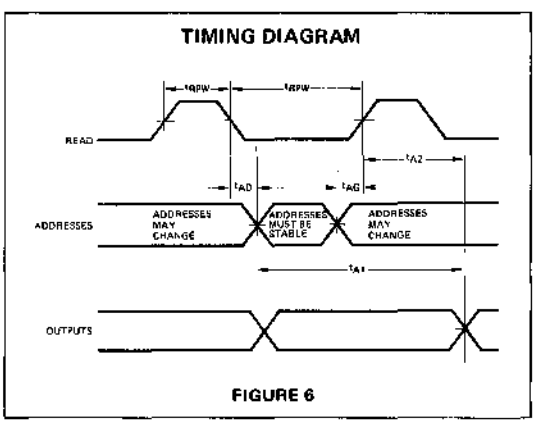


FIGURE 6

MEMORY ORGANIZATION

The 2526 is intended primarily for use as a 7 x 9 dot matrix character generator, and the address decoding scheme reflects this purpose. Address lines A1 through A4 (see Figure 5) generate the required nine scan selects plus seven excess codes. Thus, an attempt to use the 2526 with all ten address lines in a 1024 x 9 configuration would fail because there are only 5,184 bits in the memory and the excess input address codes would not be able to generate relevant output data. However, if address input A4 is tied to a logic "0", the excess codes are eliminated. The remaining nine address lines may then be used to address a 512 x 9 ROM. The ninth scan in each character is ignored along with the excess codes and a subset of 4,608 bits is used to provide the 512 x 9 capacity.

Other organizations are possible, of course, as long as the total memory capacity is not exceeded. 576 x 9 is the real capacity of the memory (576 x 9 = 5,184). The extra 64 x 9 (576 x 9 − 512 x 9 = 64 x 9) can be accessed by careful use of address A4. See Figure 7. The critical condition is stated in the figure: when A4 is logical "1", A0, A2, and A1 should be logical "0's". When A4 is logical "0", any code is allowed in the remaining nine bits. When some form of counter is used to generate the address inputs, it will often be convenient to assign the most significant bit (MSB) to A4 and the six least significant bits to A5 through A10. In this way, the highest allowed bit configuration will correspond to a binary count of 575 and the forced zero states of A3, A2, and A1 will be easier to implement.

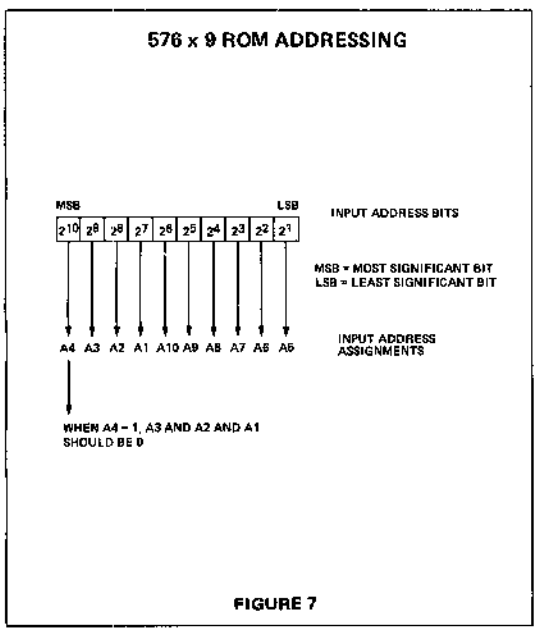


FIGURE 7

CHARACTER ORGANIZATION

When used as a 7 x 9 dot matrix character generator, the 9 x 9 dot configuration of each character allows the 2526 to be used with either vertical or horizontal scanning techniques. Figure 5 shows a 7 x 9 configuration for the letter K that is oriented for use with a horizontal scan. As each horizontal slice through the character is extracted from the ROM, the two extra bits may be ignored and the seven remaining bits serially shifted to control the dot formation.

Figure 8 shows the letter K oriented within the 9 x 9 matrix for use with a vertical scan. Each vertical slice through the character is extracted from the ROM and then serially shifted to control the dot formation. Two complete scans are not used for dots and may supply blank spaces between characters or may be ignored. Alternatively, those extra scan positions may be put to good use for translating character codes. When a code translation is desired, the column address (A1 through A4) is set to the appropriate translate scan instead of one of the dot matrix scans, and the code to be translated forms the row address (A5 through A10). The dot matrix contents of that character location are not related to the input code, but the output from the translate scan provides the desired new code.

Assume that the dot matrix letter K in Figure 8 is placed in the character array at an address corresponding to the ASCII-6 code for K (001011). Then the dots for K can only be retrieved by using the proper ASCII code as an address. The same code pattern in EBCDIC, however, stands for the period. To perform an EBCDIC to ASCII translation it is only necessary to insert the ASCII code for the period (101110) in the translate scan of the K character position. This code can then be used directly for any purpose or it can, in turn, be applied as an input to select the dot matrix for the period.

The spare bits in the 9 x 9 matrix of each character are most convenient to use for translations when the matrix is arranged for vertical scans. In that way a single read operation can perform the translation. A 7 x 9 vertical matrix leaves two spare scans for translations so that a two-way translation between two codes is possible, or two source codes can be translated into a single target code. The spare bits in the horizontal scan case are only available two at a time, so are more awkward to use for translations. In either case, the spare bits can be used to expand the character dot matrix from 7 x 9 to 9 x 9. Several special characters can be constructed (e.g., arrows) and some augmented standard characters (e.g., %) can be more legible.

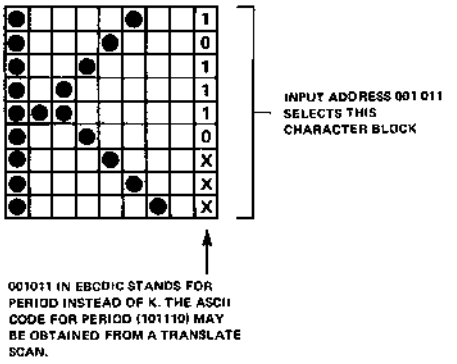


FIGURE 8

APPLICATION AREAS

There are many places where a nine bit wide ROM can be useful. A nine bit output from a function look-up table can provide an extra degree of accuracy. A sine function table, for example, could supply an added bit of resolution in the result. For arithmetic tables with 8-bit operands, the ninth output bit can be used as a sign bit or a carry bit for increased flexibility. Many byte-plus-parity systems are organized around 9-bit data paths and some of their memory requirements can only be satisfied with a 9-bit ROM. 9-bit or 18-bit minicomputers often need Read Only instruction storage for bootstrap loaders and other non-volatile routines.

The added sophistication of new CRT terminal designs is making 7 x 9 characters more and more popular. Increased legibility, decreased errors and better lower case characters are the immediate advantages. The 2526 provides an economical, easy-to-use approach for implementing 7 x 9 character graphics.

INTRODUCTION

The Signetics 2602 is a 1024-bit Random Access Read/Write Memory. It is fabricated with Signetics N-Channel Silicon Gate technology.

FEATURES

- 1024 x 1 ORGANIZATION
- COMPLETELY STATIC OPERATION
- +5 VOLT POWER SUPPLY ONLY
- TTL COMPATIBLE INPUTS
- THREE-STATE TTL OUTPUT
- 16-PIN DIP PACKAGE
- 200mW DISSIPATION
- N-CHANNEL SILICON GATE
- NO CLOCKS, NO REFRESHING, NO SENSING
- DOWN TO 500ns ACCESS/CYCLE TIME GUARANTEED

SUPPORT CIRCUITRY

The dominant system design characteristic for the 2602 is ease of use. This is a result of several unusual features, with fully static operation as perhaps the most important. Since the static memory cell does not depend on stored charge for its data retention, it does not need periodic refreshing. Thus, the memory does not require external circuitry to generate and control refresh cycling and refresh addresses. The on-chip support logic can also be simplified. See the block diagram in Figure 1.

BLOCK DIAGRAM

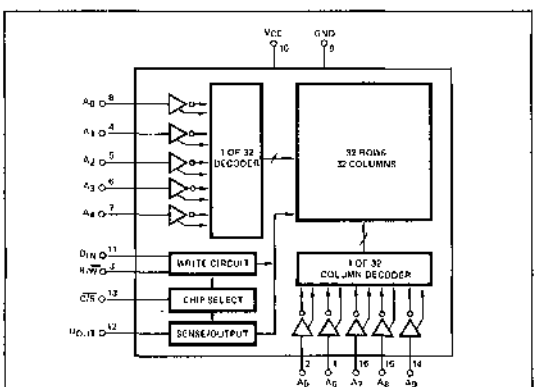


FIGURE 1

In addition to the refresh hardware costs imposed by dynamic memories, there is also a performance price to pay. Each refresh cycle ties up the memory and makes it unavailable for normal data operations. There are several interesting approaches to minimizing the performance impact of the refresh cycles, but each involves an even greater investment in support logic. Both the hardware and performance penalties of dynamic memory refreshing are eliminated by the 2602 since no refreshing of any kind is required by the device.

In the 2602 the on-chip support circuits, as well as the memory cells, are static. Thus no clocks are required for any part of the memory operation. Memory clocks for dynamic memories have proven to be very difficult to drive, distribute, and time properly so that their complete elimination saves design and debug expenses, and reduces support logic and distribution circuitry costs.

The output of the 2602 is a three-state, push-pull circuit that can drive a TTL data bus. For increased capacity several chips may be directly wire-ORed, taking advantage of the three-state output. No sense amplifiers or chip buffers are required. The problems associated with the distribution of low level sense lines and with coupled sense noise are eliminated. Figure 2 shows the output buffer circuit.

With 5 pF of typical input capacitance on any signal input and no pull-up resistors required to achieve a reliable high-level input voltage, any simple TTL logic can be used to drive arrays of the 2602 memory devices. With no high voltage, high current, or low level interface signals, noise and crosstalk problems are practically non-existent.

The net result of all these features is a dramatic decrease in the external support electronics required to implement a memory system. With greatly simplified driving, no clocks, no refreshing, and no sensing, the 2602 has eliminated all the major headaches associated with semiconductor memory system design. The cost of support electronics is also dramatically decreased. The result is that memory system costs per bit relative to dynamic memories are very attractive for 2602 memory systems of less than about 100K bits.

OUTPUT CIRCUITRY

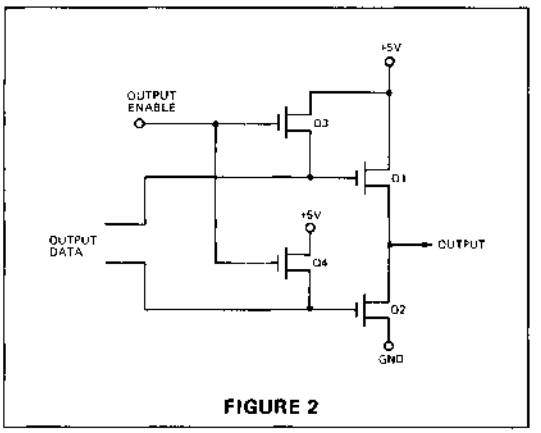


FIGURE 2

POWER

The 2602 contributes in other ways to decreased memory system costs. Only one standard supply voltage, +5V ±5%, is required. Not only are multiple supply costs eliminated, but power distribution and decoupling problems are minimized.

The low average power of less than 200mW typical and the important absence of peak currents both contribute to ease of use and lower costs. The power dissipated by the support circuits in a dynamic memory system — even a small one — can be a large percentage of the system power demands. With the 2602 static memory, the support dissipation is practically eliminated and the memory cell dissipation is very low. Power and cooling costs are, therefore, much less of a factor in the total memory system economics.

CHIP SELECT

The $\overline{\text{Chip Select}}$ signal on the 2602 performs three interrelated functions. It controls the status of the three-state output signal, it acts as the decimal address input for memories of more than 1024 words, and it enables and disables the write circuitry.

For a 1K word memory where the outputs share a data bus with other logic subsystems, the $\overline{\text{Chip Select}}$ signals can be tied together and used simply to connect or disconnect the output data from the data bus. A 2K word version of such a memory (see Figure 3) could then gate the bus connect information with the 11th address bit to form two $\overline{\text{Chip Select}}$ signals. The output data lines from the first 1K words are wire-ORed with the output data lines from the second 1K words. The two $\overline{\text{Chip Select}}$ signals will then connect the first 1K or connect the second 1K or disconnect both from the output data bus. Notice that the Read/Write lines need not be gated with the 11th address bit since an unselected chip automatically has the write circuit disabled.

READ OPERATIONS

The Read Cycle for the 2602 is very easy to execute. See the timing diagram in Figure 4. With the chip selected and in the read state, simply input an address. The data will be valid at the output after the access time has elapsed. Because there are no clocks to define the Read Cycle, it is measured as the time addresses are required to be stable. This interval is from the latest arriving address to the earliest departing address. For the same reason the access time should be measured from the latest address input.

Care should be taken to make sure that the Read/$\overline{\text{Write}}$ line is fully in the Read state before any cycle starts. Notice that one of the memory cells is being addressed at all times;

CHIP SELECT GATING

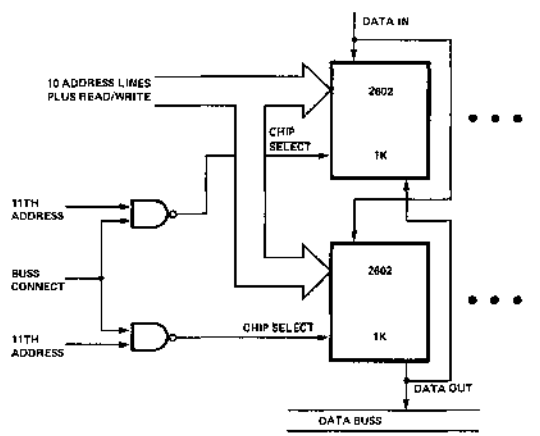


FIGURE 3

TIMING DIAGRAM

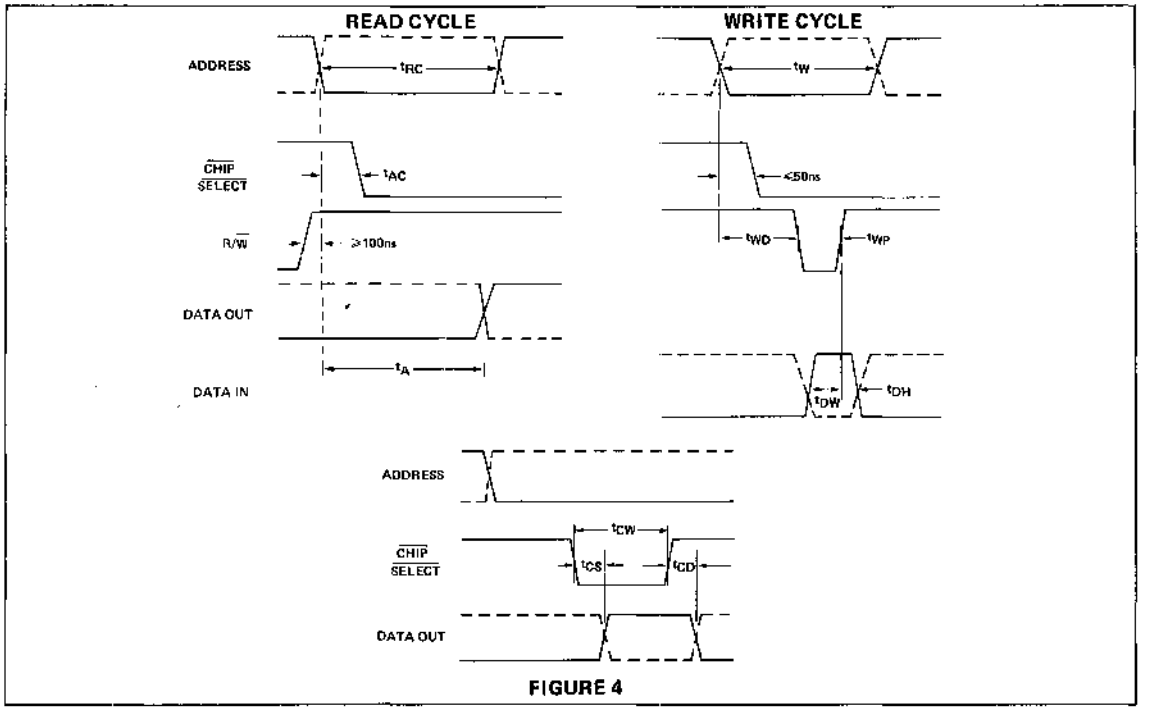


FIGURE 4

there is no quiescent state for the memory array. Thus, any time the Chip Select and Read/Write lines are both low, something will be written somewhere. The Read/Write line should be considered normally high with a negative-going write pulse allowed only under strict conditions.

The Chip Select signal may arrive as late as 200ns after the start of a Read cycle (for the 2602-1) without impacting the access time. This will often come in handy when there are extra levels of address gating involved with generating the Chip Select signal.

WRITE OPERATIONS

The write cycle is also measured by the required stable address time. Since the Chip Select signal gates the write circuitry, it must arrive earlier than in a read cycle so that the write pulse can propagate properly into the cell array. Notice that the stable addresses must overlap both the start and finish of the write pulse. It is important that the desired cell, and only the desired cell, be fully selected before the write pulse arrives and that the write pulse is fully gone before the addresses begin to change at the cell. The propagation path for the write pulse into the cell is shorter than the address path through the decoders.

For a minimum write cycle the timing of the write pulse is important. Notice in the timing diagram that t_{WD} plus t_{WP} is 400ns minimum, which leaves 100ns as the required minimum Read level before the beginning of the next cycle. A longer write cycle would allow more flexibility in the write pulse timing. The minimum write pulse width is the most critical parameter and should be maintained even if the write pulse window within the write cycle is adjusted slightly.

WAVEFORMS

The waveform picture in Figure 5 shows the 2602 in action. The test pattern being run is a simple one designed to check the general operation of every cell. The memory had previously had zeroes stored in all 1024 cells. Then a pattern of Read-Write-Read is executed at every cell location. The first Read at each cell is used to check for the previously written zero. The Write cycle then writes a one in the addressed cell and the second Read confirms that a one was in fact stored. The address then changes and the three operations are repeated on the next sequential cell.

Notice that in situations like the one pictured in Figure 5 where multiple cycles are executed at one address, there is no obvious, well-defined start of each cycle. Simple external time delays (not shown in the picture) serve to mark the transitions from cycle to cycle. The first change in the Data Out signal following the A_0 address change reflects the zero being read at the newly addressed location. During the succeeding Write cycle, the Data Out line indicates the polarity of the data being written in the cell. At the end of the Write cycle, the same cell is read again and the Data Out signal shows that a one was successfully stored. When the addresses change again, this sequence is repeated.

WAVEFORM

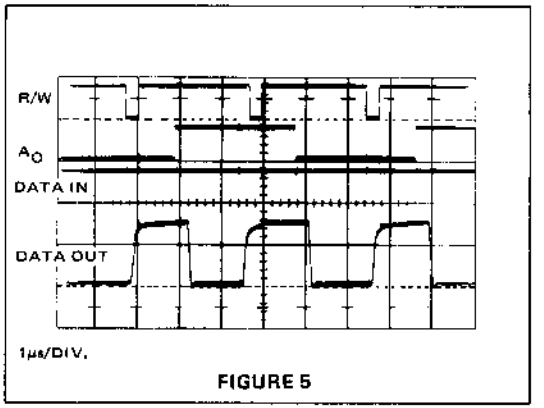


FIGURE 5

STORAGE CELL

Figure 6 is a schematic of the memory bit cell in the 2602. It is a standard six device cell configuration, using two cross-coupled devices (Q1, Q2) with active pull-ups (Q3, Q4). Q5 and Q6 are used to connect the cell to the bit lines.

The cells are arranged in a two-dimensional array of 32 by 32 for a total of 1024 cells. Address lines 0 through 4 are decoded to select 1-of-32 word lines. Each word line drives 32 cells, connecting them to 32 pairs of bit lines. Addresses 5 through 9 are decoded to select 1-of-32 bit line pairs. Thus, the 10 address lines select one cell out of 1024 for reading or writing. The bit lines are ORed together and the selected pair drive the output data amplifier.

When writing, the bit lines are driven by the write amplifiers to force the selected cell in one direction or the other. Because the bit lines are being actively driven instead of passively sensed, the write cycle can always be executed in 500ns or less even when the read cycle is longer.

MEMORY SYSTEMS

For those designers who have worked with dynamic memory systems, the dominant theme with the 2602 is the things that do not have to be done. With no clocks, no refreshing and no sensing, the designer can center his work on optimizing the TTL/MOS interfaces and the system packaging.

MEMORY CELL

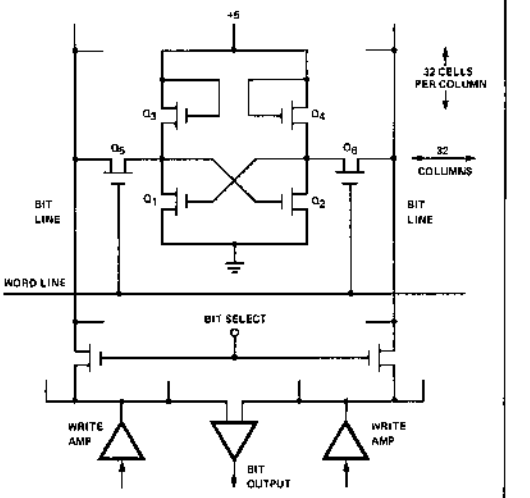


FIGURE 6

Because of the lack of support circuitry around the 2602, the propagation paths to and from the memory chip are much shorter than is the case with dynamic memories. This fact will help to compensate for the somewhat longer access times of the 2602, although there are large numbers of applications where the 2602 offers more than sufficient speed. The lack of support circuits makes it easy to gain performance from the static memory by interleaving. The expensive dynamic support circuitry does not have to be duplicated for a two-way interleave.

The lack of power surge currents, high voltage transitions, low level sense currents, and multiple power supplies simplifies memory system designs in several ways. One significant result is that many systems will work very well on two-sided printed circuit boards, with consequent savings in design and production costs. With less board area devoted to supporting the memory chips, the board bit density can be increased.

STANDARD ROM CODES

CODE CONVERTERS

P/N	DESCRIPTION	TYPE
CM0000	EBCDIC–ASCII	2430
CM2810	ASCII to Selectric	2430
CM3421	ASCII–Selectric, Selectric–ASCII	2431
CM3480	EBCDIC to Packed Hollerith	2431
CM3501	Quick Brown Fox Generator (MM522DF)	2420
CM3511	Quick Brown Fox Generator (MM522DZ)	2420
CM3530	ASCII–EBCDIC; EBCDIC–ASCII	2530

CHARACTER GENERATORS

P/N	DESCRIPTION		TYPE
CM2140	ASCII Alphanumeric, 7x5, Row Output		2513
CM2143	Katakana, 7x5, Row Output (Obsolete, See (CM4800)		2513
CM2170	ASCII with yen sign, 7x5, Row Output		2513
CM3001/3010	Upper case ASCII, 10x7, Row Output	(set of 2)	2516
CM3021	Lower case ASCII, 7x6, Row Output		2513
CM3030	Upper case ASCII, 7x5, Row Output		2513
CM3041	Lower case ASCII, 10x7, Row Output (split character)		2516
CM3410	Upper case ASCII, 9x7, Row Output		2526
CM3400	Upper case ASCII, 7x9, with EBCDIC–ASCII and BAUDOT–ASCII in spare left columns, Vert. Output		2526
CM3940	Same as CM3400 but Row Output		2526
CM2150	ASCII Alphanumeric, 5x7, Column Output		2516
CM3970	12x8 ASCII A thru_ 1st half	(set of 2)	2516
CM3980	12x8 ASCII null thru ? 2nd half		2516
CM4800	Katakana 7x5		2513

NOTE: Customer shall ask for and approve a copy of our truth table for any of these ROMs. We do not guarantee the suitability of the contained truth table for any particular application.

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PACKAGE INFO
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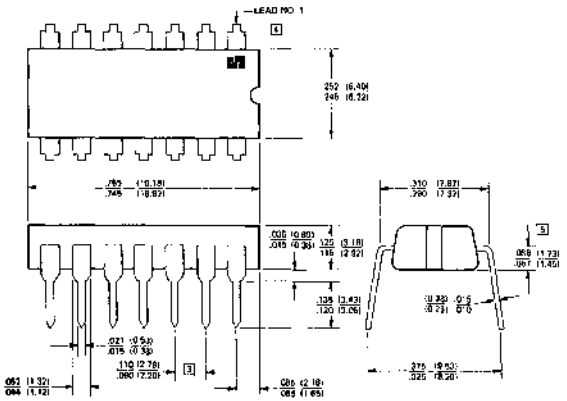
CROSS-REFERENCE
GUIDE

8

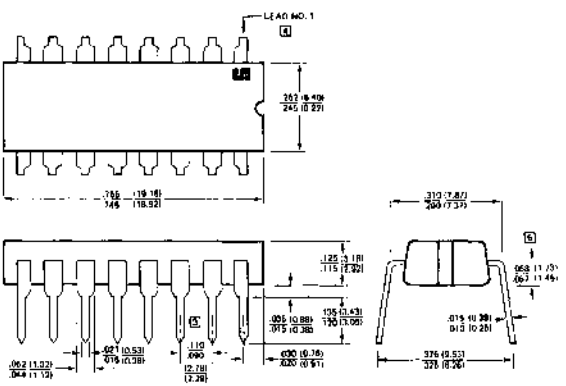
SECTIONS
SECTIONS

A PACKAGE



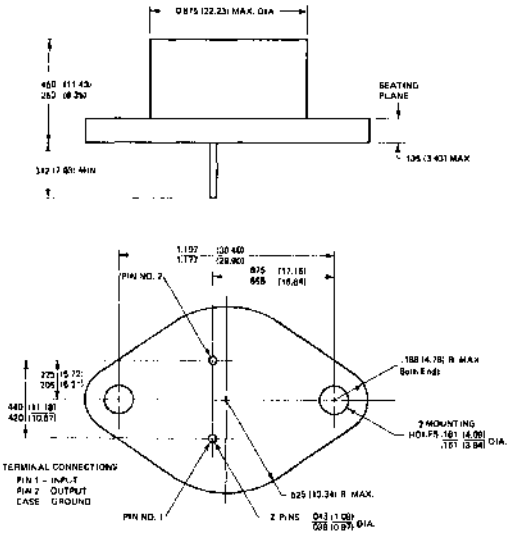
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θJa = .16 C/mW, θJc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

B PACKAGE



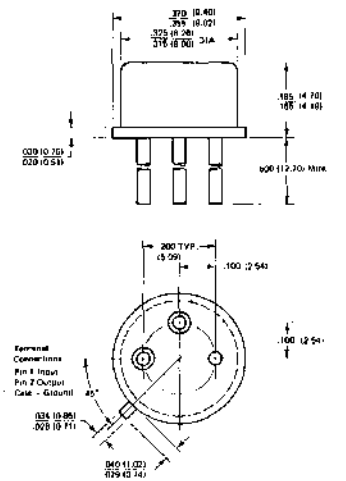
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θJa = .16 C/mW, θJc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DA PACKAGE



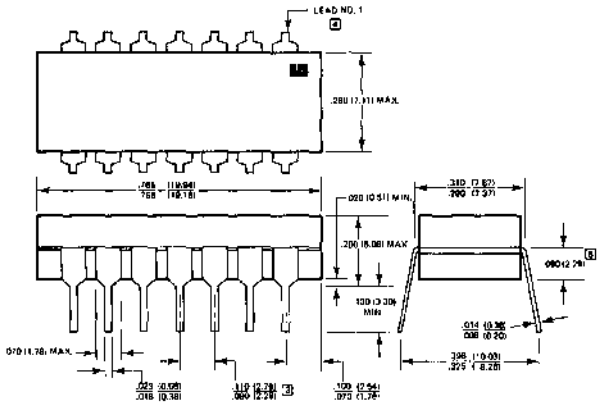
NOTES:
1. LEAD MATERIAL: NO. 52 ALLOY GOLD PLATED.
2. BODY MATERIAL: 1010 STEEL GOLD PLATED.
3. LID MATERIAL: STEEL NICKEL PLATED, WELD SEAL.
4. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

DB PACKAGE



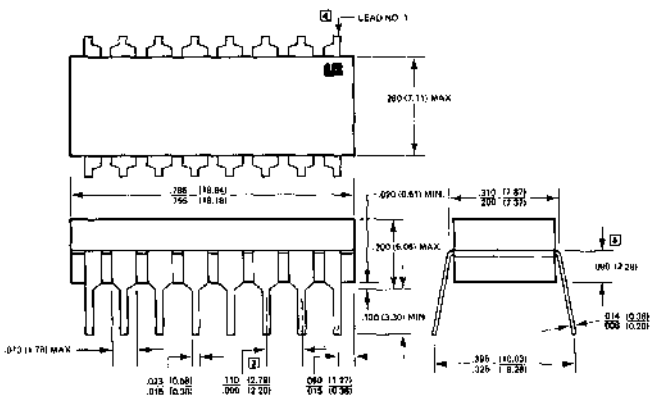
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED GLASS BODY
3. LID MATERIAL: NICKEL, WELD SEAL.
4. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

F PACKAGE



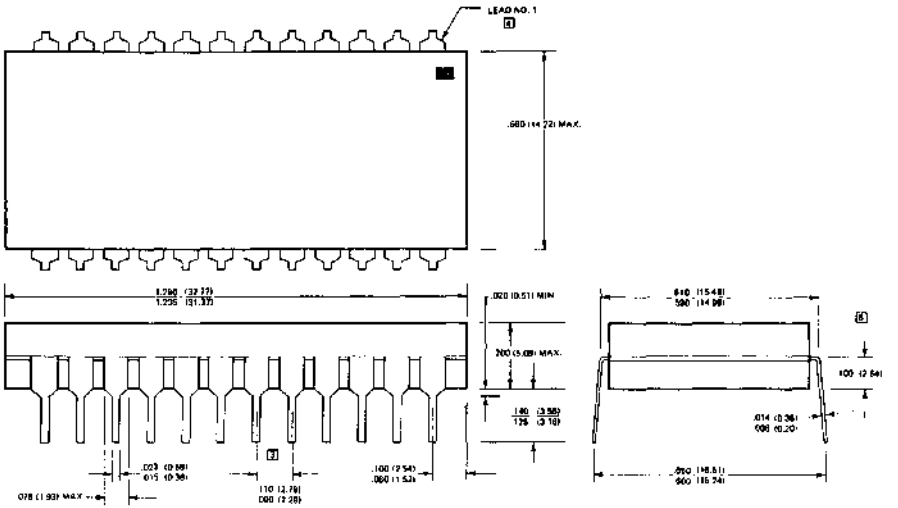
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Jc = .055°C/mW, Θ Ja = .020°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

F PACKAGE



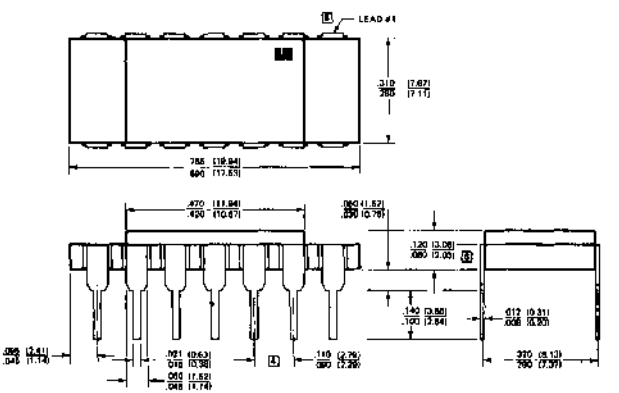
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Jc = .050°C/mW, Θ Ja = .023°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

F PACKAGE



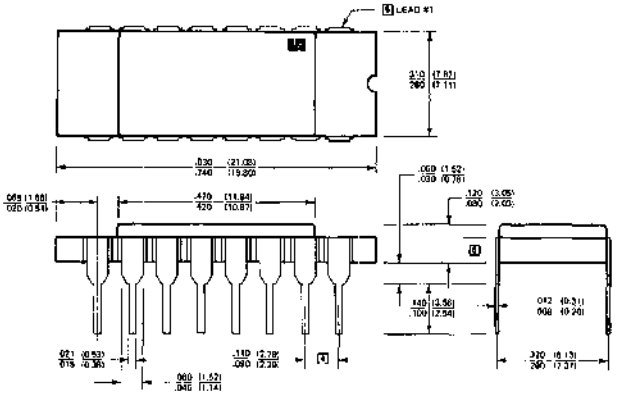
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: θ_{JA} = .066°C/mW, θ_{JC} = .012°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



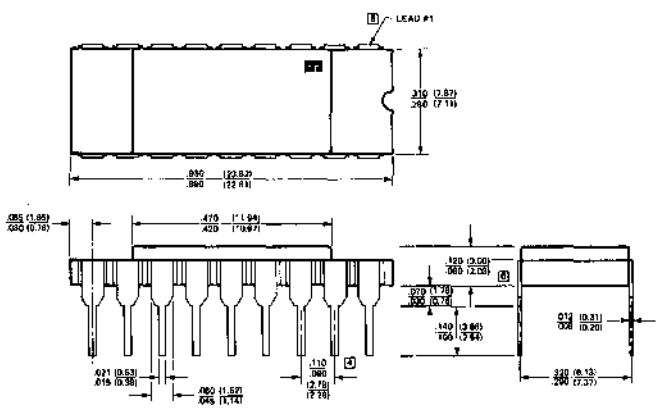
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL
4. TOLERANCES NON CUMULATIVE
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: θ_{JA} = .065°C/mW, θ_{JC} = .020°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



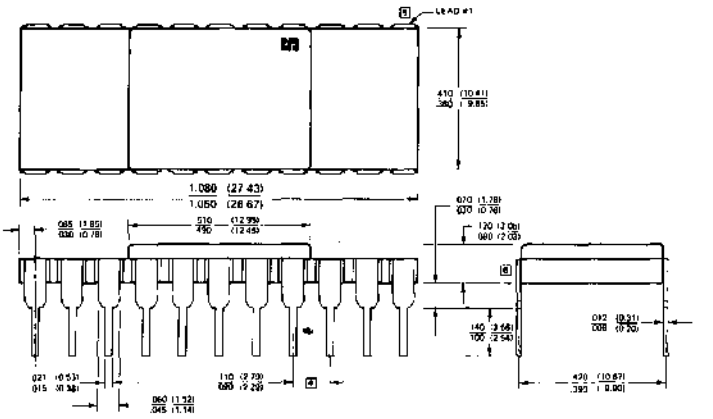
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED. ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: $\Theta Ja = 062^{\circ}C/mW$, $\Psi Jc = .018^{\circ}C/mW$.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



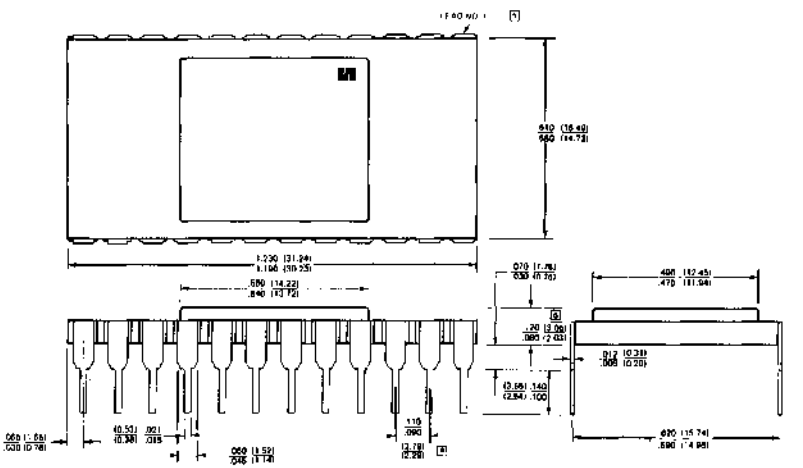
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: $\Theta Ja = .060^{\circ}C/mW$, $\Psi Jc = .016^{\circ}C/mW$.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



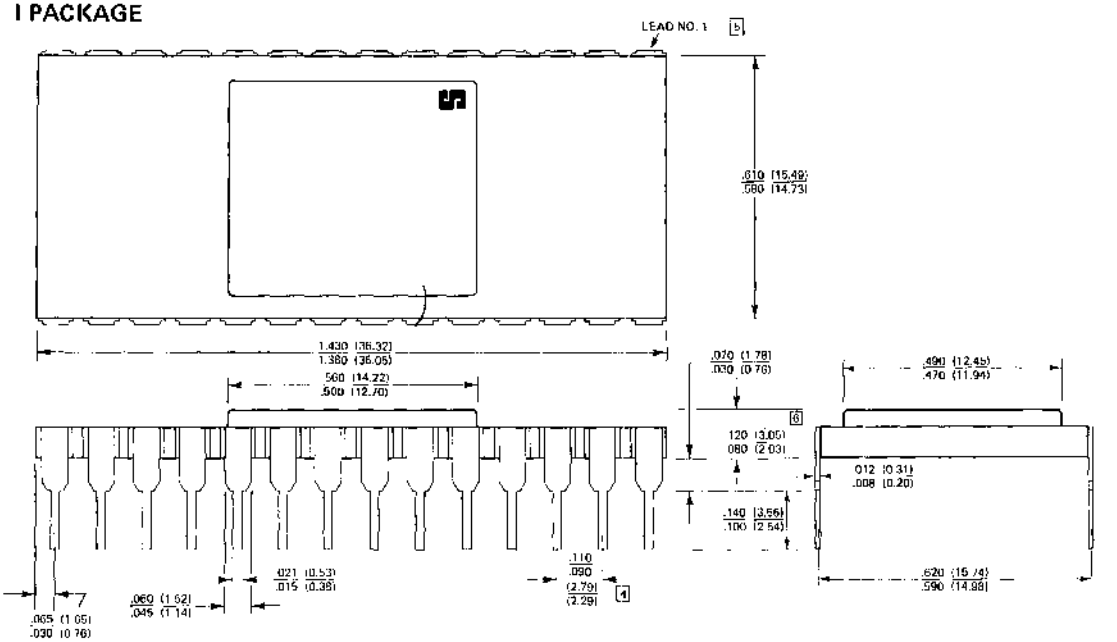
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .055°C/mW, Θ Jc = .012°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



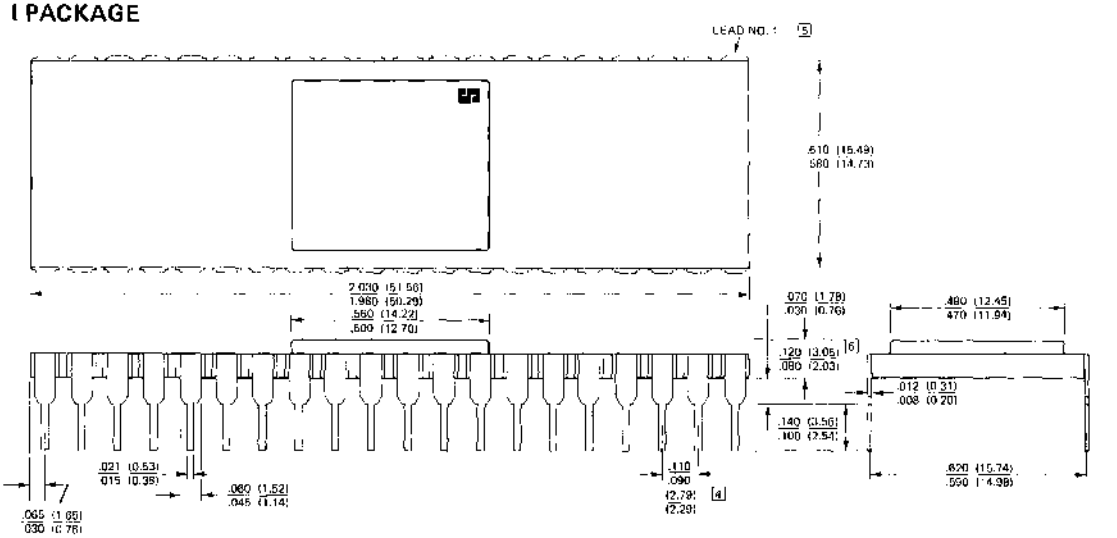
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = 060°C/mW, Θ Jc = 010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

I PACKAGE



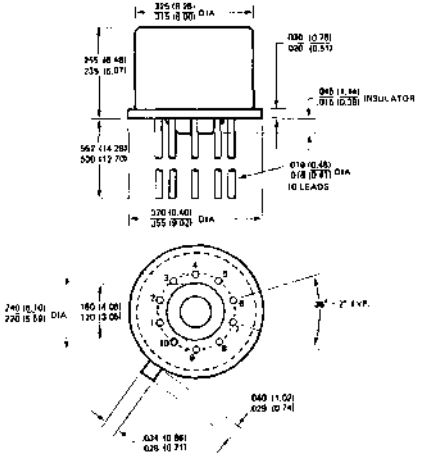
Notes:
1. Lead Material: Kovar or Equivalent, Gold Plated.
2. Body Material: Ceramic with Kovar or Equivalent
3. Lid Material: Kovar or Equivalent, Gold Plated. Alloy Seal
4. Tolerances Non Cumulative.
5. Signetics Symbol Denotes Lead No. 1.
6. Lead Spacing Shall be Measured within this Zone.
7. Thermal Resistance: θ Ja = .050°C/mW, θ Jc = .010°C/mW
8. All Dimensions Shown in Parentheses are Metric Equivalents. (Millimeters)

I PACKAGE



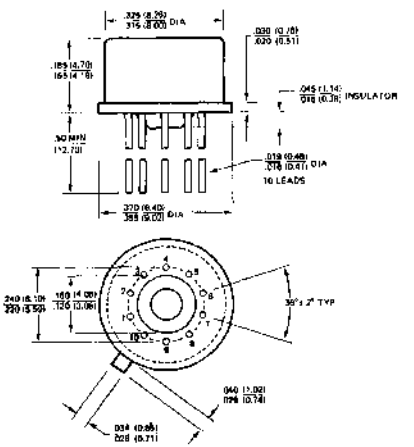
Notes:
1. Lead Material: Kovar or Equivalent, Gold Plated
2. Body Material: Ceramic with Kovar or Equivalent,
3. Lid Material: Kovar or Equivalent, Gold Plated. Alloy Seal.
4. Tolerances Non Cumulative,
5. Signetics Symbol Denotes Lead No. 1.
6. Lead Spacing Shall be Measured within this Zone
7. Thermal Resistance: θ Ja = .090°C/mW, θ Jc = .010°C/mW
8. All Dimensions Shown in Parentheses are Metric Equivalents. (Millimeters)

K PACKAGE



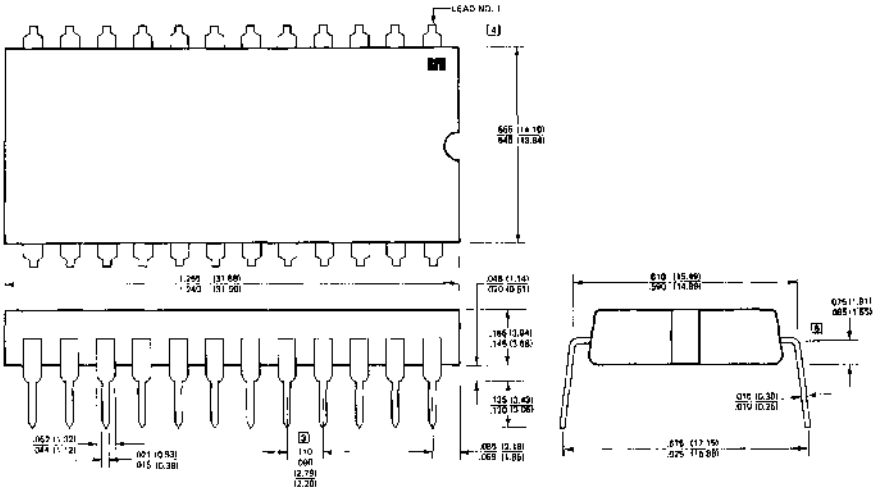
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED, GLASS BODY
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, θ_{JA} = 150°C/mW, Π_{JA} = .025°C/mW
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

L PACKAGE



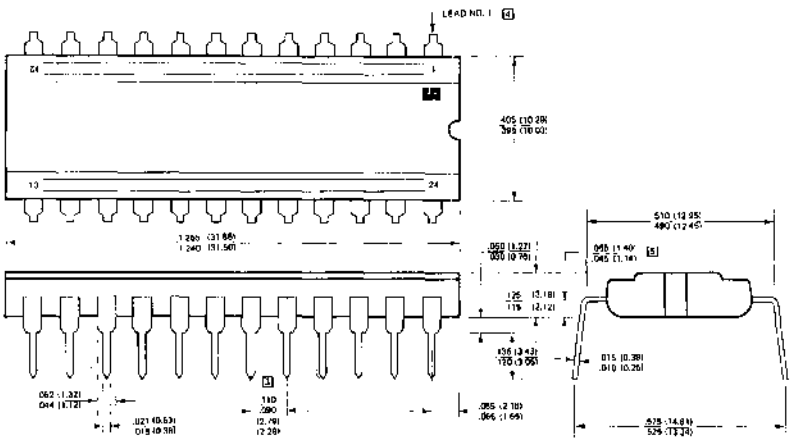
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED, GLASS BODY.
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, θ_{JA} = 150°C/mW, Π_{JC} = .025°C/mW
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

N PACKAGE



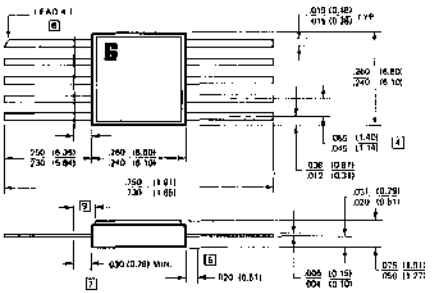
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θ_{JA} = .12°C/mW, θ_{JC} = .05°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

NX PACKAGE



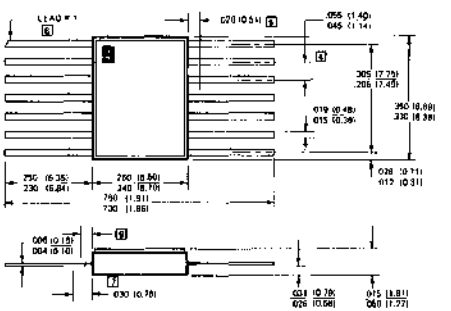
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: θ_{JA} = .12° C/mW, θ_{JC} = .05°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS (MILLIMETERS)

Q PACKAGE



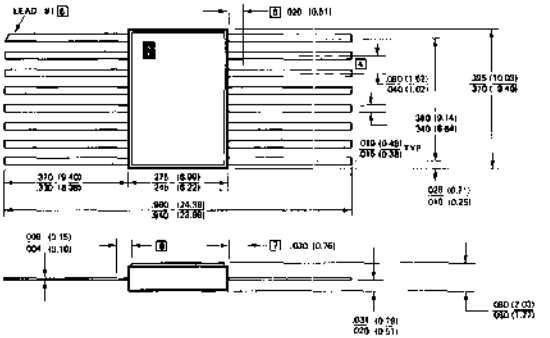
NOTES.
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. THERMAL RESISTANCE: θ_{JA} = .170°C/mW, θ_{JC} = .060°C/mW.
9. MAXIMUM GLASS CLIMB, LID SKEW, OR FRIT SQUEEZE OUT IS .010.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

Q PACKAGE



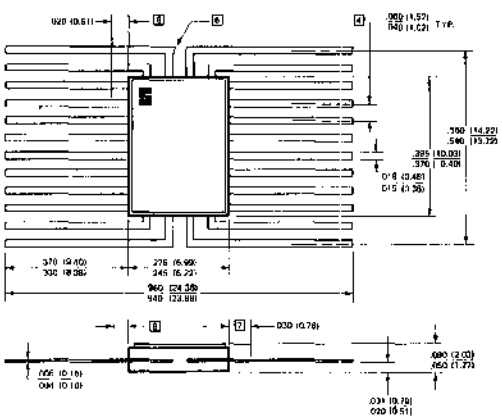
NOTES
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL DENOTES LEAD NO. 1
7. MAXIMUM GLASS CLIMB, LID SKEW OR FRIT SQUEEZE OUT .010.
8. THERMAL RESISTANCE: θ_{JA} = 150°C/mW, θ_{JC} = .060°C/mW.
9. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS).

Q PACKAGE



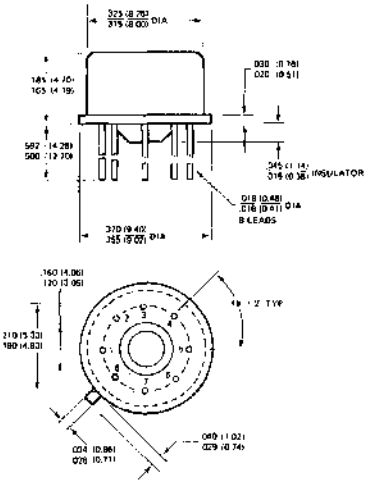
NOTES
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. THERMAL RESISTANCE: ΘJa = .150°C/mW, ΘJc = .050°C/mW.
9. MAXIMUM GLASS CLIMB, LID SKEW, OR FRIT SQUEEZE OUT IS .010.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

Q PACKAGE



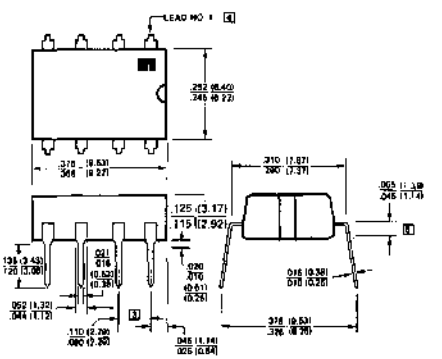
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. THERMAL RESISTANCE: ΘJa = 150°C/mW, ΘJc = .050°C/mW.
9. MAXIMUM GLASS CLIMB, LID SKEW, OR FRIT SQUEEZE OUT IS .010.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS (MILLIMETERS)

T PACKAGE



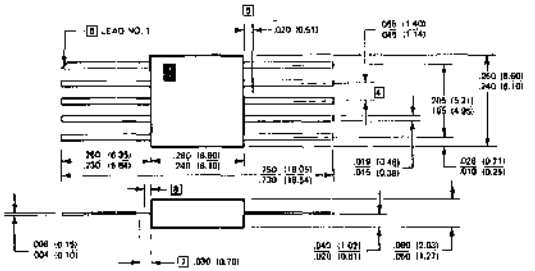
NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED
2. BODY MATERIAL: EYELET, KOVAR OR EQUIVALENT, GOLD PLATED, GLASS BODY.
3. LID MATERIAL: NICKEL, WELD SEAL.
4. THERMAL RESISTANCE FROM JUNCTION TO CASE, θ_{JA} = 150 C/mW, θ_{JC} = .025 C/mW
5. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

V PACKAGE



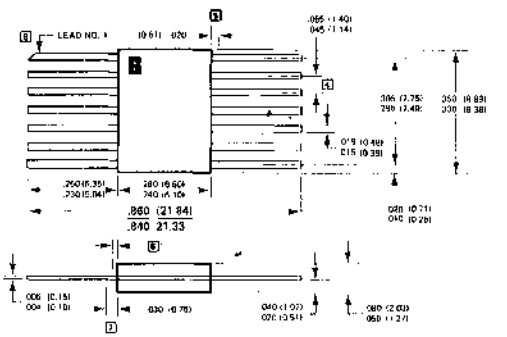
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE θ_{JA} = .16°C/mW, θ_{JC} = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE



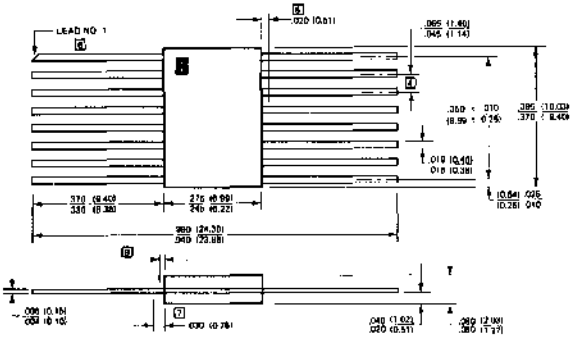
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. MAXIMUM GLASS CLIMB .010.
9. THERMAL RESISTANCE: H θ_{JA} = 220°C/mW, H θ_{JC} = 085°C/mW
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE



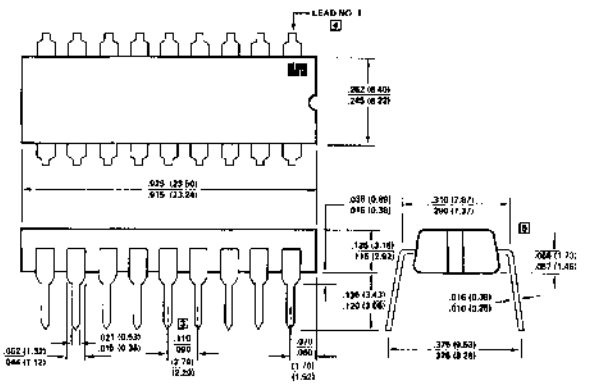
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS
3. LID MATERIAL: CERAMIC GLASS SEAL
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. MAXIMUM GLASS CLIMB .010.
9. THERMAL RESISTANCE: θ_{JA} = 200°C/mW, θ_{JC} = 085°C/mW.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE



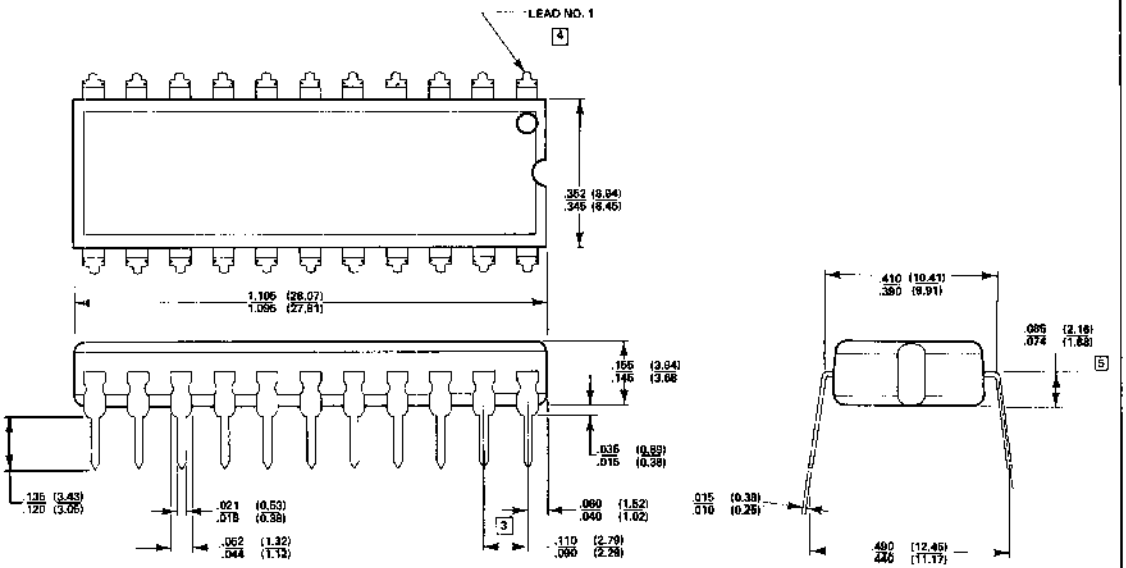
NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND
8. MAXIMUM GLASS CLIMB .010
9. THERMAL RESISTANCE: Θ_{JA} = .200 C/mW, Θ_{JC} = .085°C/mW.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS (MILLIMETERS)

XA PACKAGE



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ_{JA} = .16°C/mW, Θ_{JC} = .08°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

XC PACKAGE



NOTES
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT
2. BODY MATERIAL: PLASTIC
3. TOLERANCES NON CUMULATIVE
4. SIGNETICS SYMBOL DENOTES LEAD NO.1
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH
7. THERMAL RESISTANCE θ_{JA} = 120 C/mW, θ_{JC} = 055 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESIS ARE METRIC EQUIVALENTS. (MILLIMETERS)

INTRODUCTION

Increasingly, users are demanding ultra high quality and reliability commercial temperature range ICs for their use in certain electronic systems. This trend toward a "Zero Defects" philosophy has been prompted by the inability of previously available "one or two percent" defective device lots to meet board rework cost requirements and system reliability goals.

The need for nearly perfect, but low cost, devices is being met by the industry with varying degrees of success. Several IC manufactures have programs which partially meet these requirements, and many users have implemented specifications designed to accomplish this goal.

Signetics has been supplying devices to these general requirements for some time, but only now, and for the first time in the industry, has a fully evaluated and comprehensive program been instituted. We call it SUPR DIP.

DESCRIPTION OF PROCESS STEPS
(see Page 7)

SUPR DIP utilizes the best provisions of various user specifications and adds a few of our own. SUPR DIP is a COMPREHENSIVE program which results in the HIGHEST QUALITY and RELIABILITY commercial products AVAILABLE IN THE INDUSTRY. Other suppliers' user specifications offer SOME of the advantages of our program, but only SUPR DIP gives ALL of the following provisions:

- **Visual Die Sort Inspection, MIL-STD-883, Method 2010, Condition B Criteria**
- **Preseal Visual Inspection, MIL-STD-883, Method 2010, Condition B Criteria**
- **100% Thermal Shock, MIL-STD-883, Method 1011, Condition A Criteria**
- **100% Production Electrical Testing**
- **100% High Temperature Functional Testing for elimination of functional rejects and temperature sensitive (intermittent) bonds**
- **Outgoing Lot Quality Acceptance Testing including 0.15% AQL for functionality and 0.15% to 1.0% for other electrical and mechanical criteria**

BENEFITS

The above processing steps are efficiently performed in volume, and users realize the following benefits at both

LOW INITIAL COST and LOW EVENTUAL COST:

- **Eliminates need for 100% incoming electrical testing and mechanical inspection**
- **No need for additional preconditioning prior to board assembly**
- **Significantly reduces requirement for board rework (page 8)**
- **Reduction in system field failures**
- **Permits the following Signetics GUARANTEES:**

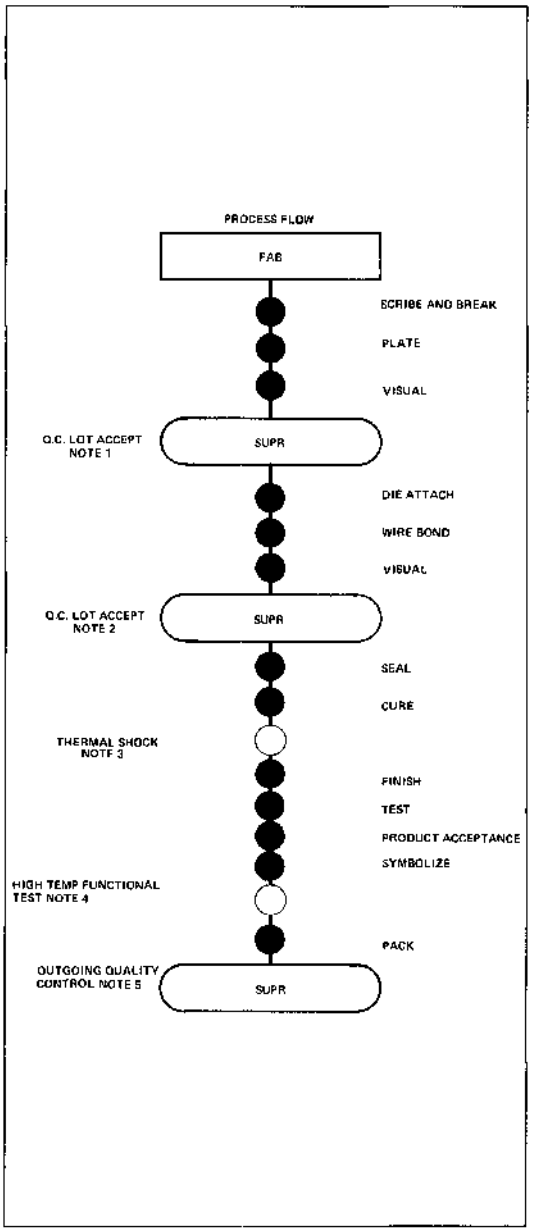
GUARANTEES

TEST	CONDITIONS	AQL	CUMULATIVE	NOTES
Electrically Functional	25°C	0.15%	0.15%	1
	100°C	0.15%		
DC	25°C	.65%	2.5%	
	At Temperatures	1.0%		
AC	25°C	1.0%		
Mechanical	Major	.25%	1.0%	2
	Minor	1.0%		

NOTE 1: The functional test not only checks for opens and shorts but also performs an operating test where the device is driven from standard outputs and drives inputs under full load.

NOTE 2: MAJOR DEFECTS: those that make the circuit inoperable such as missing pin, wrong symbol, no solder, shorted pins, holes in package. MINOR DEFECTS: physical dimensions, illegible type, solderability to MIL S-202C-208B.

WHAT FLOW AND GUARANTEES DO I GET WITH SUPR?



PROCESS NOTES AND DESCRIPTIONS

NOTE 1: Q.C. Lot Acceptance of Die
From reports covering all reported 1971 failures an analysis was compiled to determine the need for improved inspection at die sort. The inspection derived from this study was to lot accept to a 4.0% AQL to MIL-STD-883, 2010B. This is statistically adequate to reject all lots with repetitive type masking errors and lots that exhibit potential high yield losses. Critical random defects which constitute reliability problems and which may not be detected at final test are inspected to a 1.0% AQL. These include:

1. scratches
2. smears
3. glassivated bonding pads

NOTE 2: Q.C. Lot Acceptance of Preseal Parts
From the above study an analysis was completed on parts prior to encapsulation. The same inspection at this point is being performed in accordance with MIL-STD-883, 2010-B to a 2.5% AQL, and with critical defects to a 0.65% AQL. Critical defects include:

1. scratches caused by assembly operators
2. contamination
3. smeared ball bonds on bonding pads decreasing the aluminum

NOTE 3: Preconditioning
Various types of preconditioning were examined including thermal shock, temperature cycle, and high temperature storage. Thermal shock (MIL-STD-883, 1011, A) was selected as the most effective method of removing potential package problems that could not be detected by other processing screens. This processing weakens loose bonds so that they may be tested out at temperature without degrading the quality of good bonds. Other tests have either no effect on quality and reliability or significantly degraded the good parts during the preconditioning period.

Some users, attempting to incorporate tighter screening, have instituted various preconditioning steps before testing or board assembly. Many of these steps create problems which would not occur if preconditioning was performed prior to shipment. Examples of a few of these problems are opens at high temperature due to extremes of thermal shock or temperature cycles, symbolization coming off after exposure to liquids used for shock testing, handling loss and mechanical damage, solderability problems due to contamination within ovens.

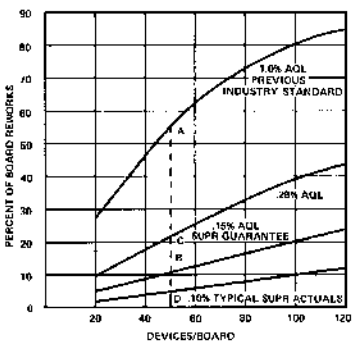
NOTE 4: High Functional Temperature Test
Analysis of user incoming quality and system failure reports has yielded four significant results:

A. Due to supplier processing and handling from final test to shipment, parts may become mixed to a low percent defective.

B. Some decives, due to internal differential expansion coefficients, become non-functional when operated in a system in which the ambient is above room temperature and the junctions receive continuous power. This is normally due to weak bonds. These parts create considerable system detection problems since they test good at room temperature and may also become system life test failures.

C. Most customers building boards of 40 or more units complexity perform 100% parts testing upon receipt of a shipment. This is to obtain a low percentage board rework. This is normally performed at room temperature using a large test system. These testers have the potential for destroying or degrading units due to faulty relay controls which force excessive currents into devices. In an ordinary electronic system, parts are never subjected to these conditions. In many cases, this type of inspection results in a greater percent lot defective than was received and can result in additional board rework. 100% testing normally only reduces percent defective to a .28% AQL level. (see Page 8)

AQL LEVELS VS. BOARD REWORKS



D. Most integrated circuits will never be used in a circuit that requires all worst case load and threshold conditions. If a part will function under load at 100 degrees C ambient, it will consistently work in a system.

Signetics has addressed to all these problems by designing a test system that repetitively tests devices functionally at a temperature in excess of 100 degrees C. This testing circuit is the same electrical environment as in a computer.

NOTE 5: Outgoing Quality Control

The task of this function is to ensure that parts have been processed to the required flow and that the tightened inspection criteria are being met. An additional sample will be selected to assure electrical specification conformance. Each shipment will be sealed by Quality Assurance personnel.

RECOMMENDED INCOMING TEST

Signetics recommends that parts from this program be sampled at incoming inspection by using the following technique:

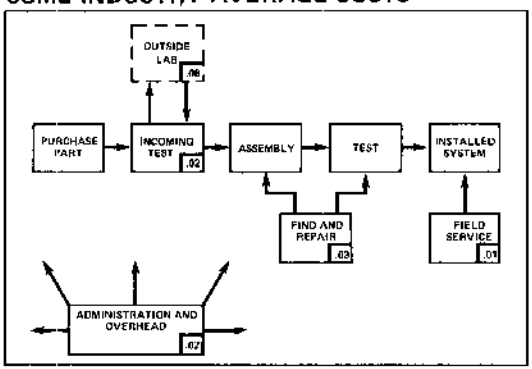
1. One sample is selected to check functionality, using a tester which has no potential for degrading units. No relay switching or current forcing modules should be used.

2. From this sample another sample is tested for AC and DC conformance to specifications. Only devices which have a marginal AC or high temp quality history need be tested.

3. In most cases skip lot testing can be instituted immediately.

In this manner a great savings can be realized in incoming control and board rework costs.

A TYPICAL IC USER'S ASSEMBLY FLOW AND SOME INDUSTRY AVERAGE COSTS



Costs added to parts because of quality problems (based on current industry averages)

Incoming inspection (sampling, 100% test, preconditioning) labor and material only. Outside labs were kept separate since they tend to distort this number. Present average cost for outside lab usage is $.08 per part.	.02
Find and repair defective parts in boards and systems. This includes location of defects, scrapped parts, replacement of bad parts, engineering support during system burn-in. Labor and material only.	.03
Field service support. Labor, material, travel, revenue lost due to equipment being down. Calculated only on first year expenses. No customer ill will, lost accounts, maintenance, organization overhead is included.	.01
Administration and overhead. Test equipment for parts and systems (depreciation, only) support costs of this equipment, inventory of parts and systems necessary because of delays due to quality problems. No additional hidden costs such as added supervision, field service overhead, quality and reliability overhead is included.	.02
TOTAL (not including outside labs)	.08

SUPR DIP WAS ENGINEERED TO CUT THIS EXPENSE BY ONE ORDER OF MAGNITUDE

SIGNETICS SURE 883 PROGRAM

FOR DIGITAL DEVICES .
BULLETIN 5001A

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical tests. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables IIIA, IIIB, and IIIC provide a complete process qualification and verification program in accordance with the conditions of MIL-STD-883, Group A, B and C tests. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period. A summary of these test results is available on request at the time of order placement.

* Systematic Uniformity and Reliability Evaluation

All of the applicable Electrical Parameters of Table IIIA are performed at pretest on the Table IIIC samples. This provides the MIL-STD-883 electrical parameter and design verification Group A tests. These tests are performed on representative circuit types from every die process family type in manufacturing during this period.

Table IIIB consists of the package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these package and assembly qualification tests.

Table IIIC consists of the die process oriented qualification electrical stress or operational tests at high temperature per MIL-STD-883, Groups B and C. Representative devices from each die process family are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

An additional screening series is available at extra cost. Details are given in Table V, MIL-STD-883, method 5004, high reliability screening.

Table I — 100% Production Screen Tests

TEST	CONDITIONS
Pressal Visual	High Power — Low Power
Thermal Shock	Liquid to Liquid, 5 Cycles, 60 Seconds at 0°C, 60 Seconds at 100°C, transfer time 5 Seconds. (See Note 1.)
Centrifuge	Y_1 Axis; 30,000 g minimum, 1 minute. (See Note 1.)
Hermeticity	Gross leak test (Bubble Test). (See Note 1.)
Production Electrical Tests	

Table II — Signetics Acceptance Tests (See Notes 2 and 3)

SIGNETICS SUBGROUP	TEST	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
A-2	DC Parameters	T_A = +25°C	1.0%	II
A-3	DC Parameters	T_A = +25°C	1.0%	II
A-4	DC Parameters	T_A = +125° C	1.0%	II
A-5	DC Parameters	T_A = -55°C	1.0%	II
A-6	AC Parameters	T_A = +25°C	1.0%	II

TABLE IIIA. MIL-STD-883 GROUP A ELECTRICAL TESTS

MIL-STD-883 GROUP A SUBGROUP	SIGNETICS SUBGROUP	TEST DESCRIPTION
A1	A-2, A-3	Static tests at 25°C
A2	A-4	Static tests at maximum rated operating temperature.
A3	A-5	Static tests at minimum rated operating temperature.
A4	A-6	Dynamic tests at 25°C.
A5	C-2, when applicable	Dynamic tests at maximum rated operating temperature.
A6	C-2, when applicable	Dynamic tests at minimum rated operating temperature.
A7	*	Functional tests at 25°C.
A8	A-4, A-5	Functional tests at maximum and minimum rated operating temperatures.
A9	A-6	Switching tests at 25°C.
A10	C-2, when applicable	Switching tests at maximum rated operating temperature.
A11	C-2, when applicable	Switching tests at minimum rated operating temperature.

TABLE IIIB. MIL-STD-883 GROUPS B AND C ENVIRONMENTAL TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
B_1	Physical Dimensions	2008	Test Condition A	15
B_2	Marking Permanency Visual and Mechanical Bond Strength	2008 2008 2011	Test Condition B, Para. 3.2.1 Test Condition B Test Condition D	4 devices/no failure 1 device/no failure 15
B_3	Solderability	2003	Solder Temperature 260°C ±10°C	15
B_4	Lead Fatigue Hermeticity a. Fine b. Gross	2004 1014	Test Condition B_2 See Note 4 Test Condition A or B Test Condition C	15
C_1	Pre Test Electrical Parameters Thermal Shock Temperature Cycle Hermeticity a. Fine b. Gross Moisture Resistance End Point Electrical Parameters FAILURE CRITERIA	 1011 1010 1014 1004	Signetics Subgroup A-3 15 Cycles, Test Condition C, +150°C to -65°C 10 Cycles, Test Condition C, 150°C to -65°C See Note 4 Test Condition A or B Test Condition C Omit initial conditioning Signetics Subgroup A-3 Refer to Table IV.	15
C_2	Pre Test Electrical Parameters Mechanical Shock Vibration Variable Frequency Constant Acceleration End Point Electrical Parameters FAILURE CRITERIA	 2002 2007 2001	Signetics Subgroup A-3 Test Condition B Test Condition A Test Condition E Signetics Subgroup A-3 Refer to Table IV.	15
C_3	Salt Atmosphere	1009	Test Condition A. Omit initial conditioning	15
C_4	Pre-Test Electrical Parameters High Temperature Storage End Point Electrical Parameters FAILURE CRITERIA	 1008	Signetics Subgroup A-3 T_A = +150°C, t = 1000 hours Signetics Subgroup A-3 Refer to Table IV.	λ = 15

TABLE IIIC. MIL-STD-883 GROUPS B AND C HIGH TEMPERATURE OPERATING LIFE TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
	Pre-Test and Design Verification Electrical Parameters		Table IIIA as applicable, data sheet groups A & C.	
C_5	High Temperature Operating Life End Point Electrical Parameters FAILURE CRITERIA	1005	Test Condition D or E as applicable. T_A = +125°C or +85°C, per Part Data Sheet. t = 1000 hours. Signetics Subgroup A-3 Refer to Table IV.	λ = 10

* Signetics performs a truth table test.

Table IV – Signetics Failure Criteria

TEST	"1" Input Current	"1" Output Voltage	"0" Input Current	"0" Output Voltage	Expansion Node Current
LIMITS	Data Sheet Limits and: 10X Initial Value for DTL 5X (nitial Value for TTL	Data Sheet Limits and: ±20% Initial Value	Data Sheet Limits ±20% Initial Value	Data Sheet Limits and: ±0.1V	Data Sheet Limits and: ±20% Initial Value

Optional High Reliability Screening

To maximize reliability in critical application, the Optional High Reliability Screening of Table V provides for three levels of 100% screening per MIL-STD-883, Method 5004 at extra cost. This series eliminates the necessity for special specification, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal Group A acceptance test. Circuits subjected to this Preconditioning Series are clearly distinguishable from standard products in the following ways:

1. Individual serial number on each circuit (Class A only).
2. The first letters of a part number are either RA, RB, or RC.

   RA = Class A
   RB = Class B
   RC = Class C
   i.e., RA8880J = 100% screening of Table V, Class A.
3. Individual device variables parametric test data is supplied with each shipment (Class A only).

Consult your local representative for price information. Device types should be specified with the appropriate letter prefixes.

Notes:

1. Not applicable to solid molded packaged devices.
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL C 45662A.
3. Detailed tests, conditions, and limits applicable to each subgroup are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table. See Table IIIA for the corresponding Group A tests of MIL STD 883.
4. The Hermeticity tests are not employed for solid molded packages.
5. Class B and Class C may be subjected to thermal shock as an alternate.
6. The test sequence of fine and gross leak may be reversed when fluorocarbons are utilized for gross leak.
7. The individual MIL-STD-883 Test Methods are, in many cases designed to "stand alone" as a sole screen or sole Group B environmental sampling test. But since 5004 specifies a screening series or flow, some of the measurements, etc., specified in an individual Test Method are not intended to be applicable in the screening series.

TABLE V – MIL-STD-883 METHOD 5004, HIGH RELIABILITY SCREENING

TEST	MIL-STD-883 METHOD	CLASS A	CLASS B	CLASS C	CLARIFICATIONS (See Note 7)
Internal Visual (presal)	2010.1	Cond. A	Cond. B	Cond. B	Test Condition A, Paragraph 3.1.1 7. a. delete the words "and parameter"
Stabilization Bake	1008 (24 hours)	Cond. C	Cond. C	Cond. C	Condition C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements at this point
Thermal Shock	1011	Cond C	Not required. NOTE 5	Not required. NOTE 5	Cond. C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection at this point
Temperature Cycling	1010	Cond. C	Cond. C NOTE 5	Cond. C NOTE 5	(150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection, no hermeticity tests at this point.
Mechanical Shock	2002, Y1 plane only	Cond. B	Not Required	Not Required	No electrical measurements at this point.
Centrifuge	2001	Cond. E Y2 then Y1 plane	Cond. E Y1 plane	Cond. E Y1 plane	
Hermeticity A. Fine Leak B. Gross Leak	1014, Note 6 (Hermetic devices only)	Cond. A or B Cond. C	Cond. A or B Cond. C	Cond. A or B Cond. C	
Critical Electrical Parameters	Signetics Subgroup A 3	Read and Record	Not Required	Not Required	
Burn In Test	1015, T_A = +125°C	240 hours Cond. D or E (as applicable)	168 hours Cond. D or E (as applicable)	Not Required	
Critical Electrical Parameters	Signetics Subgroup A 3	Read and Record	Not Required	Not Required	
Signetics FAILURE CRITERIA		Table IV	Not Required	Not Required	
Reverse Bias Burn In	1015, T_A = +150°C t = 72 hours	Cond. A or C	Not Required	Not Required	Required only when specified in the applicable procurement document. Signetics standard burn in (above) includes reverse bias of unused junctions
Final Electrical Test	Perform go no-go measurements of Signetics Subgroup A Parameters	Signetics Subgroups A 2, A 4, A 5, A 6, Functional tests, truth table when applicable	Signetics Subgroups A 2, A 3 Functional tests, truth table when applicable	Signetics Subgroups A 2, A 3 Functional tests, truth table when applicable	
Radiographic Inspection	2012	Yes	Not Required	Not Required	
External Visual	2009	Yes	Yes	Yes	

SIGNETICS QUALIFICATION AND SCREENING PROGRAM IN ACCORDANCE WITH MIL-STD-883, METHOD 5004 & 5005

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical test. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables IIIA, IIIB, and IIIC provide a complete process qualification and verification program in accordance with the conditions of MIL-STD-883, Group A, B and C tests. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period. A summary of these test results is available on request at the time of order placement.

All of the applicable Electrical Parameters of Table IIIA are performed at pretest on the Table IIIC samples. This provides the MIL-STD-883 electrical parameter design verification Group A tests. These tests are performed on representative circuit types from every die process family type in manufacturing during this period.

Table IIIB consists of the package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these packages and assembly qualification tests.

Table IIIC consists of the die process oriented qualification electrical stress or operational tests at high temperature per MIL-STD-883, Groups B and C. Representative devices from each die process family are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

An additional screening series is available at extra cost. Details are given in Table V, MIL-STD-883, Method 5004, HIGH RELIABILITY SCREENING.

TABLE I — SIGNETICS 100% PRODUCTION SCREEN TESTS

TEST	CONDITIONS
Preseal Visual	
Thermal Shock	High Power—Low Power Liquid to Liquid, 5 Cycles, 60 Seconds at 0°C, 60 Seconds at 100°C, transfer time 5 seconds. (Note 1)
Centrifuge	Y_1 Axis; 30,000 g minimum, 1 minute. (Note 1)
Hermeticity	Gross leak test (Bubble Test) (Note 1)
Production Electrical Tests	

NOTE:
1. Not applicable to solid molded packaged devices.

*Systematic Uniformity and Reliability Evaluation

TABLE II – SIGNETICS ACCEPTANCE TESTS (Notes 2, 3)

SIGNETICS SUBGROUP	TEST	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
A-2	DC Parameters	$T_A = +25^\circ C$	1.0%	II
A-7	DC End Point*	$T_A = +25^\circ C$	1.0%	II
A-4	DC Parameters	$T_A = +125^\circ C$	1.0%	II
A-5	DC Parameters	$T_A = -55^\circ C$	1.0%	II
A-6	AC Parameters	$T_A = +25^\circ C$	1.0%	II

*Applies to Data Sheets Published After 6/11/70

NOTES:
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
3. Detailed tests, conditions, and limits applicable to each subgroup are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table. See Table IIIA for the Corresponding Group A tests of MIL-STD-883.

TABLE IIIA – SIGNETICS MIL-STD-883 GROUP A ELECTRICAL TESTS

MIL-STD-883 GROUP A SUBGROUP	SIGNETICS SUBGROUP	TEST DESCRIPTION
A1	A-2, A-7	Static tests at 25°C
A2	A-4	Static tests at maximum rated operating temperature
A3	A-5	Static tests at minimum rated operating temperature
A4	A-7	Dynamic tests at 25°C
A5	A_4	Dynamic tests at maximum rated operating temperature
A6	A_5	Dynamic tests at minimum rated operating temperature
A7		Functional tests at 25°C
A8		Functional tests at maximum and minimum rated operating temperature
A9	A-6	Switching tests at 25°C
A10		Switching tests at maximum rated operating temperature
A11		Switching tests at minimum rated operating temperature

TABLE IIIB – SIGNETICS MIL-STD-883 GROUPS B AND C ENVIRONMENTAL TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
B1	Physical Dimensions	2008	Test Condition A	15
B2	Marking Permanency	2008	Test Condition B, Para. 3, 2, 1	4 devices/no failures
	Visual and Mechanical	2008	Test Condition B	1 device/no failure
	Bond Strength	2011	Test Condition D, Para. 3, 7	15
B3	Solderability	2003	Solder Temperature 260°C ±10°C	15
B4	Lead Fatigue	2004	Test Condition B2	15
	Hermeticity	1014	Note 4	
	a. Fine		Test Condition A or B	
	b. Gross		Test Condition C	
C1	Pre-Test Electrical Parameters		Table IV as applicable	
	Thermal Shock	1011	15 Cycles. Test Condition C, +150°C to −65°C	15
	Temperature Cycle	1010	10 Cycles. Test Condition C, +150°C to −65°C	
	Hermeticity	1014	Note 4	
	a. Fine		Test Condition A or B	
	b. Gross		Test Condition C	
	Moisture Resistance	1004	Omit vibration and initial conditioning	
	End Point Electrical Parameters		Table IV as applicable	
	FAILURE CRITERIA		Refer to Table IV	
C2	Pre-Test Electrical Parameters		Table IV as applicable	
M	Mechanical Shock	2002	Test Condition B	15
	Vibration Variable Frequency	2007	Test Condition A	
	Constant Acceleration	2001		
	End Point Electrical Parameters		Table IV as applicable	
	FAILURE CRITERIA		Refer to Table IV	
C3	Salt Atmosphere	1009	Test Condition A. Omit initial conditioning	15
C4	Pre-Test Electrical Parameters		Table IV as applicable	
	High Temperature Storage	1008	T_A = +150°C, t = 1000 hours	15
	End Point Electrical Parameters		Table IV as applicable	
	FAILURE CRITERIA		Refer to Table IV	

NOTE:
4. The Hermeticity tests are not employed for solid molded packages.

TABLE IIIC – SIGNETICS MIL-STD-883 GROUPS B & C HIGH TEMPERATURE OPERATING LIFE TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
	Pre-Test and Design Verification Electrical Parameters		Table IIIA, as applicable, data sheet groups A & C	
B5 & C5	High Temperature Operating Life	1005	Test Condition B, T_A = +125°C or +85°C, per Part Data Sheet t = 1008 hours	10
	End Point Electrical Parameters		Table IV as applicable	
	FAILURE CRITERIA		Refer to Table IV	

TABLE IV – SIGNETICS FAILURE CRITERIA (Note 5)

FUNCTION	PARAMETER	DELTA LIMITS
Operational Amplifier	Input Offset Voltage	±1mV Data Sheet Limits
	Open Loop Voltage Gain (Note 6)	±20%
Comparators	Input Offset Voltage	±1mV Data Sheet Limits
	Open Loop Gain	
Sense Amplifiers	Input Threshold Voltage	±1mV Data Sheet Limits
	Input Bias Current	±30%
Video Amplifiers	Voltage Gain	±20% Data Sheet Limits
Voltage Regulators	Quiescent Current	±15%
RF/IF Amplifiers	Voltage Gain	±15% Data Sheet Limits
Phase Lock Loop	Center Frequency of Oscillation	±10% Initial Value

NOTES:
5. For limits of specific devices, consult Signetics Product Marketing
6. For 5709 only

OPTIONAL HIGH RELIABILITY SCREENING

To maximize reliability in critical applications, the Optional High Reliability Screening of Table V provides for three levels of 100% screening of MIL-STD-883, Method 5004 at extra cost. This series eliminates the necessity for special specifications, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal Group A acceptance test. Circuits subjected to this Preconditioning Series are clearly distinguishible from standard products in the following ways:

(1) Individual serial number on each circuit (Class A only)

(2) The first letters of a part number are either RA, RB, or RC
RA = Class A
RB = Class B
RC = Class C
i.e., RA5709G – 100% screening of Table V, Class A.

(3) Individual device variables parametric test data is supplied with each shipment (Class A only).

Consult your local representative for price information. Device types should be specified with the appropriate letter prefixes.

TABLE V – SIGNETICS MIL-STD-883, METHOD 5004, HIGH RELIABILITY SCREENING

TEST	MIL-STD-883 METHOD	CLASS A	CLASS B	CLASS C	CLARIFICATIONS (Notes 7, 8, 9)
Internal Visual (pre-seal)	2010.1	Cond. A	Cond. B	Cond. B	Test Cond. A, Para. 3.1.1.7 delete the words "and parameter"
Stabilization Bake	1008 (24 hrs.)	Cond. C	Cond. C	Cond. C	Cond. C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, at this point.
Thermal Shock	1011	Cond. A	Not. Req'd	Not Req'd	Cond. C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection at this point.
Temperature Cycling	1010	Cond. C	Cond. C Note 7	Cond. C Note 7	(150°C) max. for au/al metallization Cond. D (200°C) max. for al/al metallization system. No electrical measurement, no external visual inspection, no hermeticity tests at this point.
Mechanical Shock	200, Y1 plane only	Cond. B	Not Req'd	Not Req'd	No electrical measurements at this point.
Centrifuge	2001	Cond. E Y2 then Y1 plane	Cond. E Y1 plane	Cond. E Y1 plane	
Hermeticity a. Fine Leak b. Gross Leak	1014, Note 6 (Hermetic devices only)	 Cond. A or B Cond. C	 Cond. A or B Cond. C	 Cond. A or B Cond. C	
Critical Electrical Parameters	Table IV as applicable	Read & Record	Not Req'd	Not Req'd	
Burn-In Test	1015, T_A = +125°C	240 hrs. Cond. B	168 hrs. Cond. B	Not Req'd	
Critical Electrical Parameters	Table IV as applicable	Read & Record	Not Req'd	Not Req'd	
Signetics FAILURE CRITERIA		Table IV	Not Req'd	Not Req'd	
Reverse Bias Burn-In	1005, T_A = +150°C t = 72 hours	Cond. A or C	Not Req'd	Not Req'd	Not required unless specified on Purchase Order
Final Electrical Test	Perform go-no-go measurements of Signetics sub Group A Parameters	Signetics Sub Groups A-2, A-4 A-5, A-6	Signetics Sub Groups A-2, A-7	Signetics Sub Groups A-2, A-7	
Radiographic Inspection	2012	Yes	Req'd	Not Req'd	
External Visual	2009	Yes	Yes	Yes	

NOTES:

7. Class B and Class C may be subjected to thermal shock as an alternate.
8. The test sequence of fine and gross leak may be reversed when fluorocarbons are utilized for gross leak.
9. The individual MIL-STD-883 Test Methods are, in many cases designed to "stand alone" as a sole screen or sole Group B environmental sampling test. But since 5004 specifies a screening series or flow, some of the measurements, etc., specified in an individual Test Method are not intended to be applicable in the screening series.

QUALIFICATION AND SCREENING PROGRAM FOR MOS DEVICES

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical tes . Any unit failing either the environmental screens or th final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed test limits and conditions applicable to test group are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables III, and IV provide a complete process qualification and verification program. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period.

All of the applicable Electrical Parameters on the data sheets are performed at pretest on the Table IV samples. These tests are performed on representative circuit types from every die process family type in manufacturing during this period.

Table III consists of the Package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these package and assembly qualification tests.

Table IV consists of the die process oriented qualification electrical stress or operational tests at high temperature. Representative devices from each die process are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

TABLE I — 100% PRODUCTION SCREEN TESTS

TEST	CONDITIONS
Preseal Visual	High Power Low Power Liquid to Liquid
Thermal Shock	5 Cycles; 60 Seconds at 0°C, 60 Seconds at 100°C, Transfer Time 5 Seconds. Note 1.
Centrifuge	Y_1 Axis; 30,000 G Minimum 1 Minute. Note 1.
Hermeticity	Gross Leak Test (Bubble Test) Note 1.
Production Electrical Tests	AC and DC, $T_A = 25°C$

NOTE:
1. Not applicable to solid molded packaged devices.

TABLE II — SIGNETICS ACCEPTANCE TESTS (See Notes 2 and 3)

TEST GROUP	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
DC Parameters	$T_A = +25°C$	1.0%	II
DC Parameters	$T_A = 70°C$	1.0%	II
DC Parameters	$T_A = 0°C$	1.0%	II
AC Parameters	$T_A = +25°C$	1.0%	II

*Systematic Uniformity and Reliability Evaluation

NOTES:
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
3. Detailed tests, conditions, and limits applicable to each test group are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table.

TABLE III – MIL-STD-833 GROUPS B AND C ENVIRONMENTAL TESTS

TEST DESCRIPTION	MIL-STD-833 METHOD	CONDITIONS	LTPD
Physical Dimensions	2008	Test Condition A	15
Marking Permanency	2008	Test Condition B, Para. 3.2.1	4 devices/no failures
Visual and Mechanical	2008	Test Condition B	1 device/no failures
Bond Strength	2011	Test Condition D, Para. 3.7	15
Solderability	2003	Solder Temperature 260°C ±10°C	15
Lead Fatigue	2004	Test Condition B_2	15
Hermeticity	1014	Note 4	
a. Fine		Test Condition A or B	
b. Gross		Test Condition C	
Pre-Test Electrical Parameters		Table V as Applicable	
Thermal Shock	1011	15 Cycles. Test Condition C, +150°C to -65°C	15
Temperature Cycle	1010	10 Cycles. Test Condition C, +150°C to -65°C	
Hermeticity	1014	Note 4	
a. Fine		Test Condition A or B	
b. Gross		Test Condition C	
Moisture Resistance	1004	Omit Vibration and Initial Conditioning	
End Point Electrical Parameters		Table V as Applicable	
FAILURE CRITERIA		Refer to Table V	
Pre-Test Electrical Parameters		Table V as Applicable	
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001		
End Point Electrical Parameters		Table V as Applicable	
FAILURE CRITERIA		Refer to Table V	
Salt Atmosphere	1009	Test Condition A. Omit Initial Conditioning.	
Pre-Test Electical Parameters		Table V as Applicable	
High Temperature Storage	1008	T_A = +150°C, t = 1000 hours	15
End Point Electrical Parameters		Table V as Applicable	
FAILURE CRITERIA		Refer to Table V	

NOTE:
4. The hermeticity tests are not employed for solid molded packages.

TABLE IV – HIGH TEMPERATURE OPERATING LIFE TESTS

TEST DESCRIPTION	CONDITIONS	LTPD
Pre-Test Electrical Parameters	Refer to Table V	
Operating Life	T_A = 70°C; t = 1000 hours	10
Shift Registers	Logic 1's Clocked Through Register	
ROMs, RAMs	Addresses Being Counted Through in a Binary Fashion	

TABLE V – SIGNETICS FAILURE CRITERIA

SHIFT REGISTERS

TEST	INPUT LEAKAGE	I_{DD}	t_{ACCESS}	"1" LEVELS	"0" LEVELS
Delta Limit	5X or 100nA whichever is greater	20%	Data Sheet Limits	20%	20%

ROMs

TEST	INPUT LEAKAGE	CLOCK LEAKAGE	I_{DD}	"1"LEVELS	"0" LEVELS
Delta Limit	5X or 100nA whichever is greater	5X or 100nA whichever is greater	20%	20%	20%

RAMs

TEST	INPUT LEAKAGE	t_{ACCESS}	t_{REFESH}*	"1" LEVELS	"0" LEVELS
Data Limit	5X or 100nA whichever is greater	Data Sheet Limit	Data Sheet Limits	20%	20%

*For dynamic memories.

AMD	SIGNETICS	PAGE
LM202	LM101H	6-169
LM101A	LM101AH	6-164
LM201	LM201H	6-169
LH201D	LM201N	6-164
LM301A	LM301AH	6-164
LM301AD	LM301AV	6-164
LM307	LM307H	6-175
AM1101A	2601B	7-45
AM1402A	2502B	7-57
AM1403A	2503TA	7-57
AM1404A	2504TA	7-57
AM1506	2506T	7-68
AM1507	2517T	7-68

ANALOG DEVICES	SIGNETICS	PAGE
AD101AH	LM101AH	6-164
AD201H	LM201AH	6-164
AD301AH	LM301AH	6-164
AD710CH	µA710CT	6-99
AD710CN	µA710CA	6-99
AD710H	µA710T	6-99
AD711CH	µA711CK	6-101
AD711CN	µA711CA	6-101
AD711H	µA711K	6-101
AD741CH	µA741CT	6-115
AD741CN	µA741CA	6-115
AD741H	µA741T	6-115

CMI	SIGNETICS	PAGE
CM1101/ 11011	2501B/P 1101A1	7-45
CM1103	1103XA/ 1103-1XA	7-15 7-21
CM1402	2502B/ 1402A	7-57
CM1403	2503TA/ 1403A	7-57
CM1404	2504TA/ 1404A	7-57
CM2512	2512K	7-62
CM4500	2525V	7-108
CM7601	N24101	7-32
CM7602	N2420Y	7-32
CM7603	N2430Y	7-32

FAIRCHILD	SIGNETICS	PAGE
*µA709	µA709	6-97
*µA710	µA710	6-99
*µA711	µA711	6-101
*µA741	µA741	6-115
*µA748	µA748	6-124
9N00	S5400A/F	2-2
9N00	N7400A/F	2-2
9N01	S5401A/F	2-4
9N01	N7401A/F	2-4

* = Requires definition of Temp. Range and Pkg.

FAIRCHILD	SIGNETICS	PAGE
9N02	S5402A/F	2-6
9N02	N7402A/F	2-6
9N03	S5403A/F	2-8
9N03	N7403A/F	2-8
9N04	S5404A/F	2-10
9N04	N7404A/F	2-10
9N05	S5405A/F	2-12
	N7405A/F	2-12
9N06	S5406A/F	2-14
	N7406A/F	2-14
9N07	S5407A/F	2-16
	N7407A/F	2-16
9N08	S5408A/F	2-18
	N7408A/F	2-18
9N09	N7409A/F	2-20
9N10	S5410A/F	2-22
9N11	S5411A/F	2-24
	N7411A/F	2-24
9N20	S5420A/F	2-28
	N7420A/F	2-28
9N26	S5426A/F	2-32
9N30	S5430A/F	2-34
	N7430A/F	2-34
9N40	S5440A/F	2-38
	N7440A/F	2-38
9N50	S5450A/F	2-58
	N7450A/F	2-58
9N51	S5451A/F	2-58
	N7451A/F	2-58
9N53	S5453A/F	2-60
	N7453A/F	2-60
9N54	S5454A/F	2-60
	N7454A/F	2-60
9N60	S5460A/F	2-62
	N7460A/F	2-62
9N70	S5470A/F	2-66
	N7470A/F	2-66
9N72	S5472A/F	2-68
	N7472A/F	2-68
9N73	S5473A/F	2-70
	N7473A/F	2-70
9N74	S5474A/F	2-72
	N7474A/F	2-72
9N76	S5476B/F	2-77
	N7476B/F	2-77
9N88	S5488B/F	2-88
	N7486A/F	2-88
9N107	S54107A/F	2-110
	N74107A/F	2-110
9H00	S54H00A/F	2-183
	N74H00A/F	2-183
9H01	S54H01A/F	2-185
	N74H01A/F	2-185
9H04	S54H04A/F	2-187
	N74H04A/F	2-187
9H05	S54H05A/F	2-189
	N74H05A/F	2-189

FAIRCHILD	SIGNETICS	PAGE
9H08	S54H08A/F	2-191
	N74H08A/F	2-191
9H10	S54H10A/F	2-193
	N74H10A/F	2-193
9H11	S54H11A/F	2-195
	N74H11A/F	2-195
9H20	S54H20A/F	2-197
	N74H20A/F	2-197
9H22	S54H22A/F	2-201
	N74H22A/F	2-201
9H30	S54H30A/F	2-203
	N74H30A/F	2-203
9H40	S54H40A/F	2-205
	N74H40A/F	2-205
9H50	S54H50A/F	2-206
	N74H50A/F	2-206
9H51	S54H51A/F	2-207
	N74H51A/F	2-207
9H61	S54H61A/F	2-219
	N74H61A/F	2-219
9H62	S54H62A/F	2-221
	N74H62A/F	2-223
9H71	S54H71A/F	2-225
	N74H71A	2-225
9H72	S54H72A/F	2-227
	N74H72A/F	2-227
9H73	S54H73A/F	2-229
	N74H73A/F	2-229
9H74	S54H74A/F	2-231
	N74H74A/F	2-231
9H76	S54H76B/F	2-233
	N74H76B/F	2-233
9H101	S54H101F	2-235
	N74H101A/F	2-235
9H102	S54H102F	2-237
	N74H102A/F	2-237
9H106	S54H106B/F	2-241
	N74H106B/F	2-241
9H108	S54H108F	2.244
	N74H108A/F	2-244
	N74141B	2-119
9341	S54181F	2-281
	N74181N	2-281
9342	S54182B/F	2-164
	N74182B/F	2-164
9345	S5445F	2-48
	N7445B/F	2-48
9349	S54180A/F	2-158
	N74180N/F	2-158
9352	S5442B/F	2-42
	N7442B/F	2-42
9353	S5443B/F	2-44
	N7443B/F	2-44
9354	S5444B/F	2-46
	N7444B/F	2-46
9357A	N7446B/F	2-50
9357B	N7447B/F	2-50
9358	N7448B/F	2-54

FAIRCHILD	SIGNETICS	PAGE
9360	S74192B/F	2-166
	N74192B/F	2-166
9366	S54192B/F	2-166
	N74192B/F	2-166
9375	S7475B/F	2-75
	N7475B/F	2-75
9380	S5480A/F	2-81
	N7480A/F	2-81
9383	S5483B/F	2-85
	N7483B/F	2-85
9390	S5490A/F	2-94
	N7490A/F	2-94
9391	S5491A/F	2-96
	N7491A/F	2-96
9392	S5492A/F	2-98
	N7492A/F	2-98
9393	S5493A/F	2-100
	N7493A/F	2-100
9394	S5494F	2-102
	N7494B/F	2-102
9395	S5495A/F	2-104
	N7495A/F	2-104
9396	S5496B/F	2-106
	N7496F/F	2-106
93198	S54198F	2-178
	N74198N	2-178
9603	S54121A/F	2-112
	N74121A/F	2-112
9S00	N74S00A	2-247
9S03	N74S03A	2-247
9S04	N74S04A	2-249
9S05	N74S05A	2-249
9S20	N74S20A	2-254
9S22	N74S22A	2-256
9S40	N74S40A	2-258
9S64	N74S64A	2-260
9S65	N74S65A	2-260
9S140	N74S140A	2-258
U5B101A312	LM101AH	6-164
U5B301A393	LM301A	6-164
U5B770939X	µA7041T	6-97
U5B7710312	µA710T	6-99
U5B7710393	µA710LT	6-99
U5B7101312	LM101H	6-164
U5B7101333	LM201H	6-164
U5B7740312	SE536T	6-32
U5B7740393	NE536T	6-32
U5B7709393	µA709CT	6-97
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U6A740559X	N7405A/F	2-12
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MC204F	SE110G*	
MC204G	SE110K*	
MC205F	SE150G*	
MC205G	SE150K*	
MC206F	SE115G*	
MC206G	SE115K*	
MC206G	SE115K*	
MC207F	CS700G*	
MC207G	CS700K*	
MC208F	CS701G*	
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MC209F	SE124G*	
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MC210F	CS704G*	
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MC215F	CS705G*	
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MC217F	CS709G*	
MC217G	CS709K*	
MC251F	NE101G*	
MC251G	NE101K*	
MC252F	NE102G*	
MC252G	NE102K*	
MC253F	NE105G*	
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MC254F	NE110G*	
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MC255F	NE150G*	
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MC5400P	S5400A	2-2
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MC5402F	S5402Q	2-6
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MC5453L	S5453F	2-60
MC5453P	S5453A	2-60
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MC5493P	S5493A	2-100
MC5495L	S5495F	2-104
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MC7400L	N7400F	2-2
MC7400P	N7400A	2-2
MC7401F	N7401Q	2-4
MC7401L	N7401F	2-4
MC7401P	N7401A	2-4
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MC7402L	N7402F	2-6
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SG709CT	µA709CT	6-97
SG709T	µA709T	6-97
SG710CN	µA710CA	6-99
SG710CT	µA710CT	6-99
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