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A Standard Microsystems Company

COM2601

Universal Synchronous Receiver/Transmitter

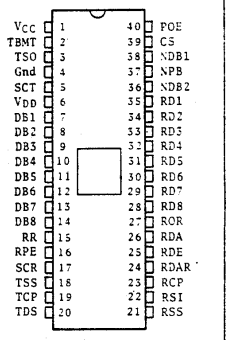
FEATURES

- **STR, BSC**—Bi-sync and interleaved bi-sync modes of operation
- **Fully Programmable**—data word length, parity mode, receiver sync character, transmitter sync character
- **Full or Half Duplex Operation**—can receive and transmit simultaneously at different baud rates
- **Fully Double Buffered**—eliminates need for precise external timing
- **Directly TTL Compatible**—no interface components required
- **Tri-State Data Outputs**—bus structure oriented
- **IBM Compatible**—internally generated SCR and SCT signals
- **High Speed Operation**—250K baud, 200ns strobes
- **Low Power**—300mW
- **Input Protected**—eliminates handling problems
- **Hermetic Dip Package**—easy board insertion

GENERAL DESCRIPTION

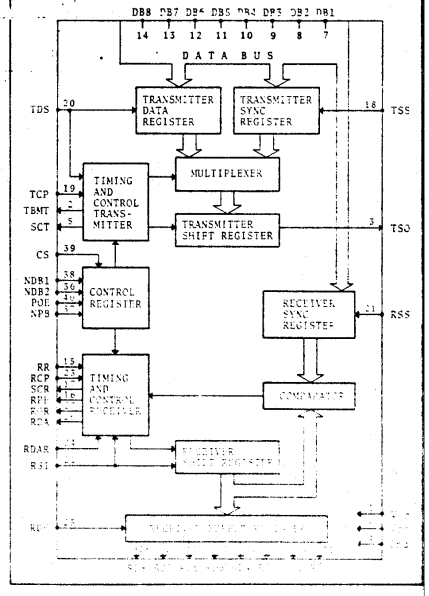
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



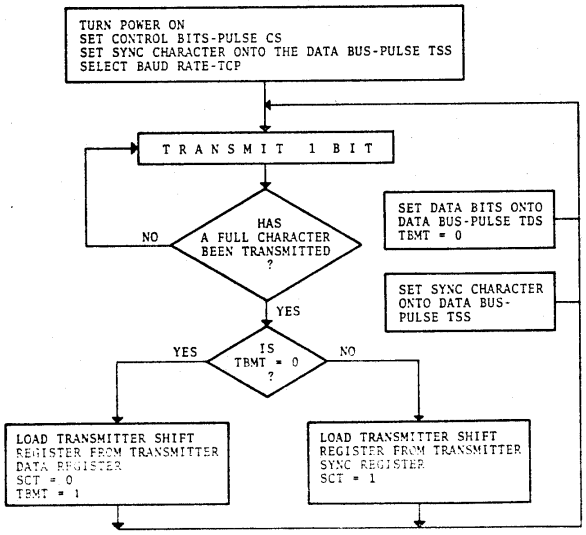
DESCRIPTION OF OPERATION - RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

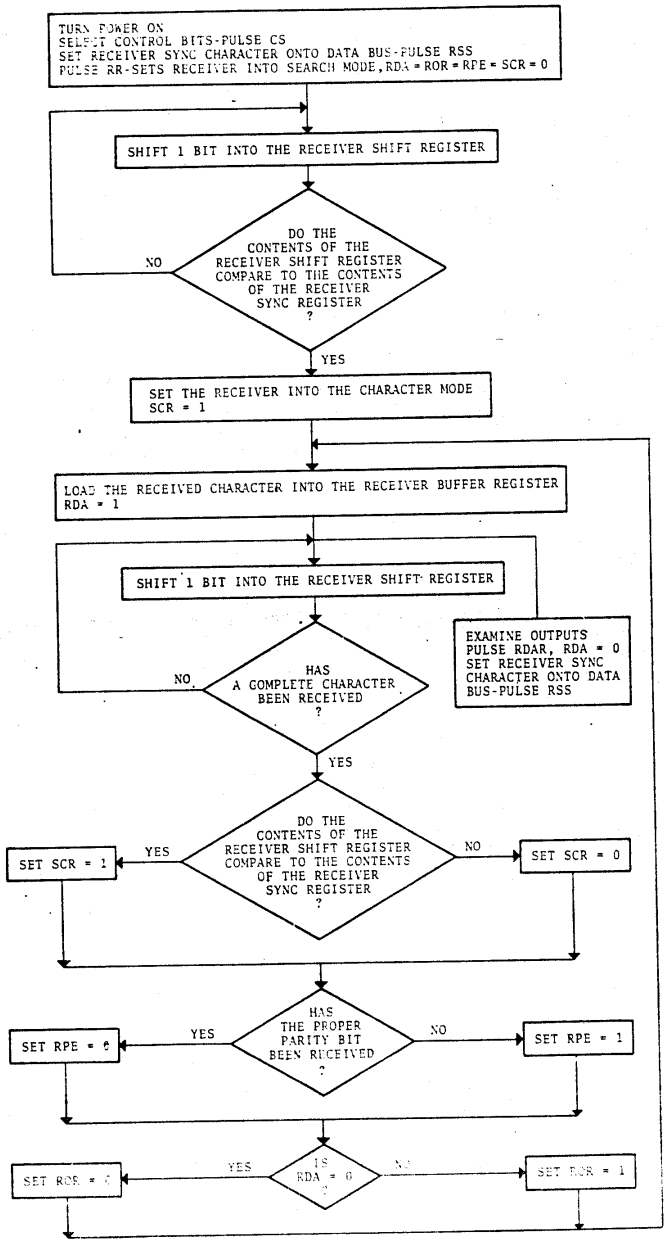
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data outputs levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

FLOW CHART - TRANSMITTER



FLOW CHART - RECEIVER



DESCRIPTION OF PIN FUNCTIONS

Pin No.	Symbol	Name	Function
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitted shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	-12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs should be at a high level. The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transition of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded int the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table:

NDB2	NDB1	data bits/character
L	L	5
L	H	6
H	L	7
H	H	8

Description of Pin Functions (cont.)

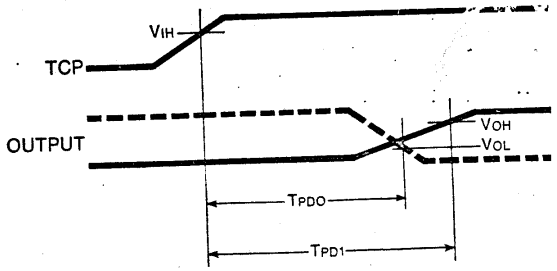
Pin No.	Symbol	Name	Function
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity

X=don't care

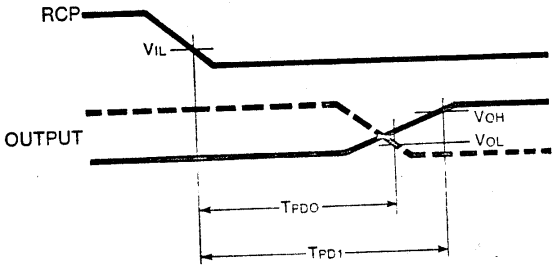
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter



OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	µs
SCT	1.0	1.5	µs
TSO	1.0	1.0	µs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	µs
ROR	2.0	2.5	µs
RPE	2.0	2.5	µs
SCR	2.0	2.5	µs
RD1-RD8	2.5	2.5	µs

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	-25 V

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0-+70°C, V_{CC}=+5V±5%, V_{DD}=-12V±5%, unless otherwise noted

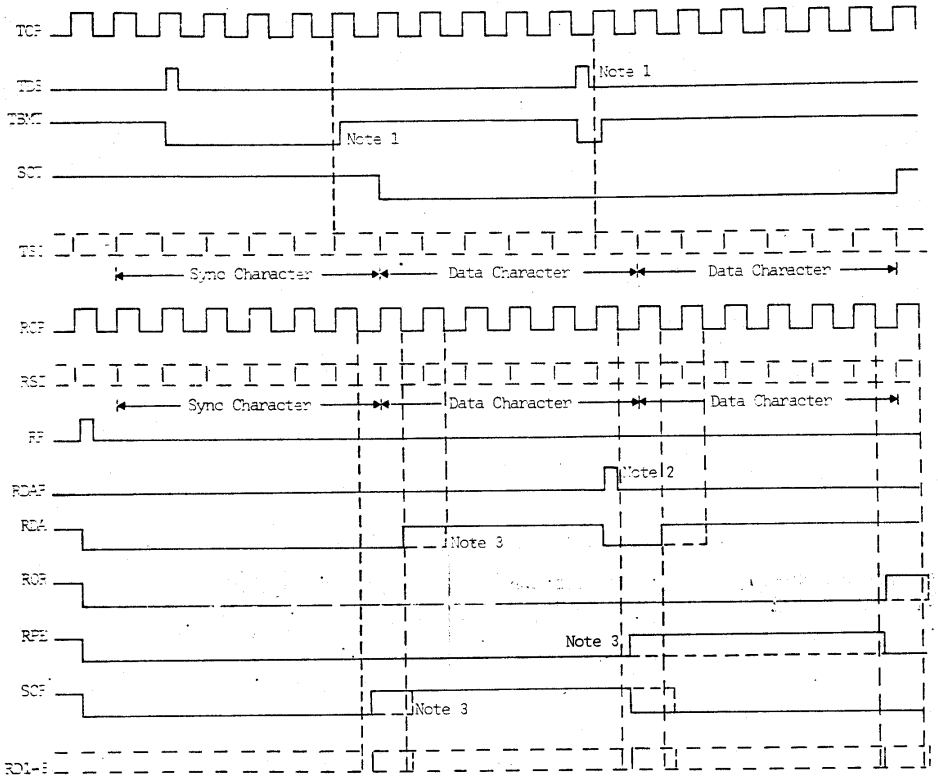
Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} =-100µA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	µA	RDE=V_{IL}, 0≤V_{OUT}≤+5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			20	mA	All outputs = V_{OH}
I_{DD}			15	mA	
A.C. CHARACTERISTICS					T_A =+25°C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			µs	RCP, TCP
Receiver reset	1			µs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	0			ns	DB1-DB8
Control bits	0			ns	NPB,NDB2,NDB1,POE
INPUT HOLD TIME					
Data bits	0			ns	DB1-DB8
Control bits	0			ns	NPB,NDB2,NDB1,POE
STROBE TO OUTPUT DELAY					Load =20pf+1TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

** Not more than one output should be shorted at a time.

NOTES:

1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF = 10M ohms
   The OFF state is controlled by the RDE input.

USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

3-4.2 MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER

3-4.2.1 Input/Output Configuration

The MC6850 Asynchronous Communications Interface Adapter (ACIA) provides a means of efficiently interfacing the MPU to devices requiring an asynchronous serial data format. The ACIA includes features for formatting and controlling such peripherals as Modems, CRT Terminals, and teletype printer/readers. An Input/Output Diagram of the MC6850 is shown in Figure 3-4.2.1-1.

Data flow between the MPU and the ACIA is via 8 bi-directional lines, DB0 through DB7, that interface with the MPU Data Bus. The direction of data flow is controlled by the MPU via the Read/Write input to the ACIA.

The "MPU side" of the ACIA also includes (see Figure 3-4.1.3-2) three chip select lines, CS0, CS1, and $\overline{CS2}$, for addressing a particular ACIA. An additional addressing input, Register Select (RS), is used to select specific registers within the ACIA. The MPU can read or write into the internal registers by addressing the ACIA via the system Address Bus using these four input lines. From the MPU's addressing point of view, each ACIA is simply two memory locations that are treated in the same manner as any other read/write memory.

The MPU also provides a timing signal to the ACIA via the Enable input. The Enable (E) pulse is used to condition the ACIA's internal interrupt control circuitry and for the timing of status/control changes. Since all data transfers take place during the $\phi 2$ portion of the clock cycle, $\phi 2$ is applied as the E signal.

The "Peripheral side" of the ACIA includes two serial data lines and three control lines. Data is transmitted and received via the Tx Data output and Rx Data inputs, respectively. Control signals Clear-To-Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$), and Request-To-Send ($\overline{RTS}$) are provided for interfacing with Modems such as the MC6860. Two clock inputs are available for supplying individual data clock rates to the receiver and transmitter portions of the ACIA.

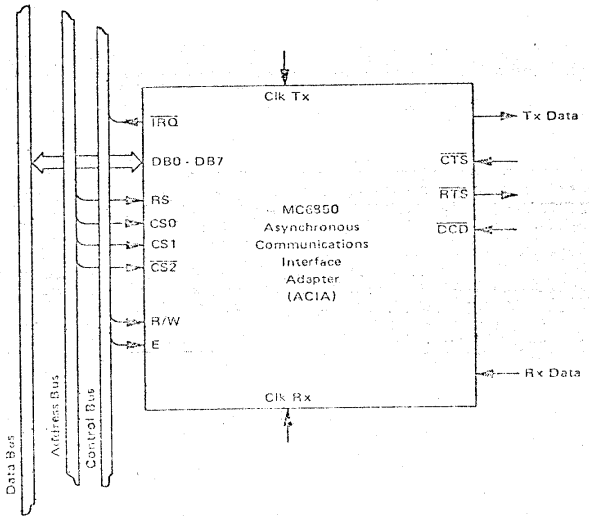


FIGURE 3-4.2.1-1: MC6850 ACIA I/O Diagram

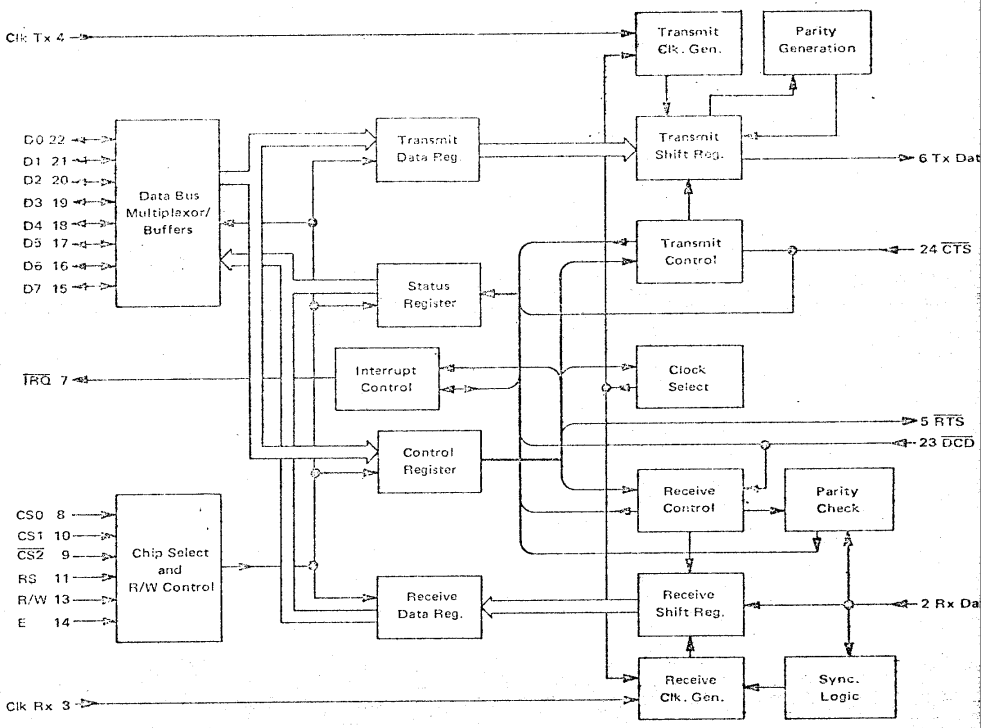


FIGURE 3-4.2.2-1: ACIA Block Diagram

3-4.2.2 Internal Organization

An expanded Block Diagram of the ACIA is shown in Figure 3-4.2.2-1. While the ACIA appears to the MPU as two addressable memory locations, internally there are four registers, two that are Write Only and two that are Read Only. The Read Only registers are for status and received data and the Write Only registers are for ACIA control and transmit data.

The Status Register format and a summary of the status bits is shown in Figure 3-4.2.2-2. The first two bits b0 and b1 indicate whether the Receiver Data Register is full (RDRF) or if the Transmit Data Register is empty (TDRE). b0 will go high when Rx data has been transferred to the Receiver Data Register (RDR). b0 will go low on the trailing edge of the Read Data command (reading the Receiver Data Buffer) or by a master reset command from bits b0 and b1 of the Control Register.

Status bit b1 (Tx Data Register Empty) will go high when a transmitter data transfer has taken place indicating that the Transmit Data Register (TDR) is available for new data entry from the MPU Bus. Bit b1 will return low on the trailing edge of a write data command. b1 will be held low if Clear-To-Send is not received from a peripheral device ($\overline{CTS}$ = "1")

Status bits b2 (Data Carrier Detect) and b3 (Clear-To-Send) are flag indicators from an external modem. Bit b2 ($\overline{DCD}$) will be high when the received carrier at the modem has been lost (ACIA's $\overline{DCD}$ input is high). Bit b2 will remain high until the interrupt is cleared by reading the Status Register and the Receiver Data Register. Bit b3 ($\overline{CTS}$) is low during reception of a Clear-To-Send command from a modem or other peripheral device.

Bit b4 (Framing Error) will be high whenever a data character is received with an improper start/stop bit character frame. The framing error flag b4 is cleared by the next data transfer signal if the condition causing the framing error has been rectified. Bit b5 (Receiver Overrun) being high indicates that the Receiver Data Register has not been read prior to a new character being received by the ACIA. This bit is cleared by reading the Receiver Data Register. Status Register bit b6 (Parity Error) is set whenever the number of high (''1's'') in the received character does not agree with the preselected odd or even parity. Bit b7 (Interrupt Request) when high indicates the ACIA is requesting interrupt to the MPU via the ACIA $\overline{IRQ}$ output and may be caused by b0 or b1 or b2 being set. All of the Status Register bits (except b3) will be cleared by an ACIA Master Reset.

The Control Register is an eight bit write only buffer which controls operation of the ACIA receiver, transmitter, interrupt enables, and the modem Request-To-Send control line. The Control Register format and a summary of its features is shown in Figure 3-4.2.2-3.

Control bits b0 and b1 select a Master Reset function for the ACIA when both bits are high and selects different clock divide ratios for the transmitter and receiver sections for the other combinations:

b1 (CDS2)	b0 (CDS1)	Clock Division
0	0	÷ 1
0	1	÷16
1	0	÷64
1	1	Master Reset

The next 3 control bits, b2, b3, and b4, are provided for character length, parity, and stop bit selection. The encoding format is as follows:

b4 (WS3)	b3 (WS2)	b2 (WS1)	Character Frame
0	0	0	7 Bit + Even Parity + 2 Stop Bits
0	0	1	7 Bit + Odd Parity + 2 Stop Bits
0	1	0	7 Bit + Even Parity + 1 Stop Bit
0	1	1	7 Bit + Odd Parity + 1 Stop Bit
1	0	0	8 Bit + No Parity + 2 Stop Bits
1	0	1	8 Bit + No Parity + 1 Stop Bit
1	1	0	8 Bit + Even Parity + 1 Stop Bit
1	1	1	8 Bit + Odd Parity + 1 Stop Bit

The ACIA transmitter section is controlled by control bits b5 (TC1) and b6 (TC2). The four combinations of these two inputs provide transmission of a break command, Modem Request-To-Send ($\overline{RTS}$) command, and a transmitter inhibit/enable for the ACIA Interrupt Request output. When both b5 and b6 are low, the Request-To-Send ($\overline{RTS}$) output will be active low and the transmitter data register empty flag is inhibited to the ACIA's Interrupt Request ($\overline{IRQ}$) output. If b5 is high and b6 is low the $\overline{RTS}$ output remains active low but the transmit IRQ input is enabled. To turn off the $\overline{RTS}$ output b6 should be high and b5 low. This selection also inhibits the transmitter interrupt input to the $\overline{IRQ}$ output. When both b5 and b6 of the control register are high, Request-To-Send is on ($\overline{RTS}$) = 0, $\overline{IRQ}$ is inhibited for the transmitter, and a break is transmitted (a space).

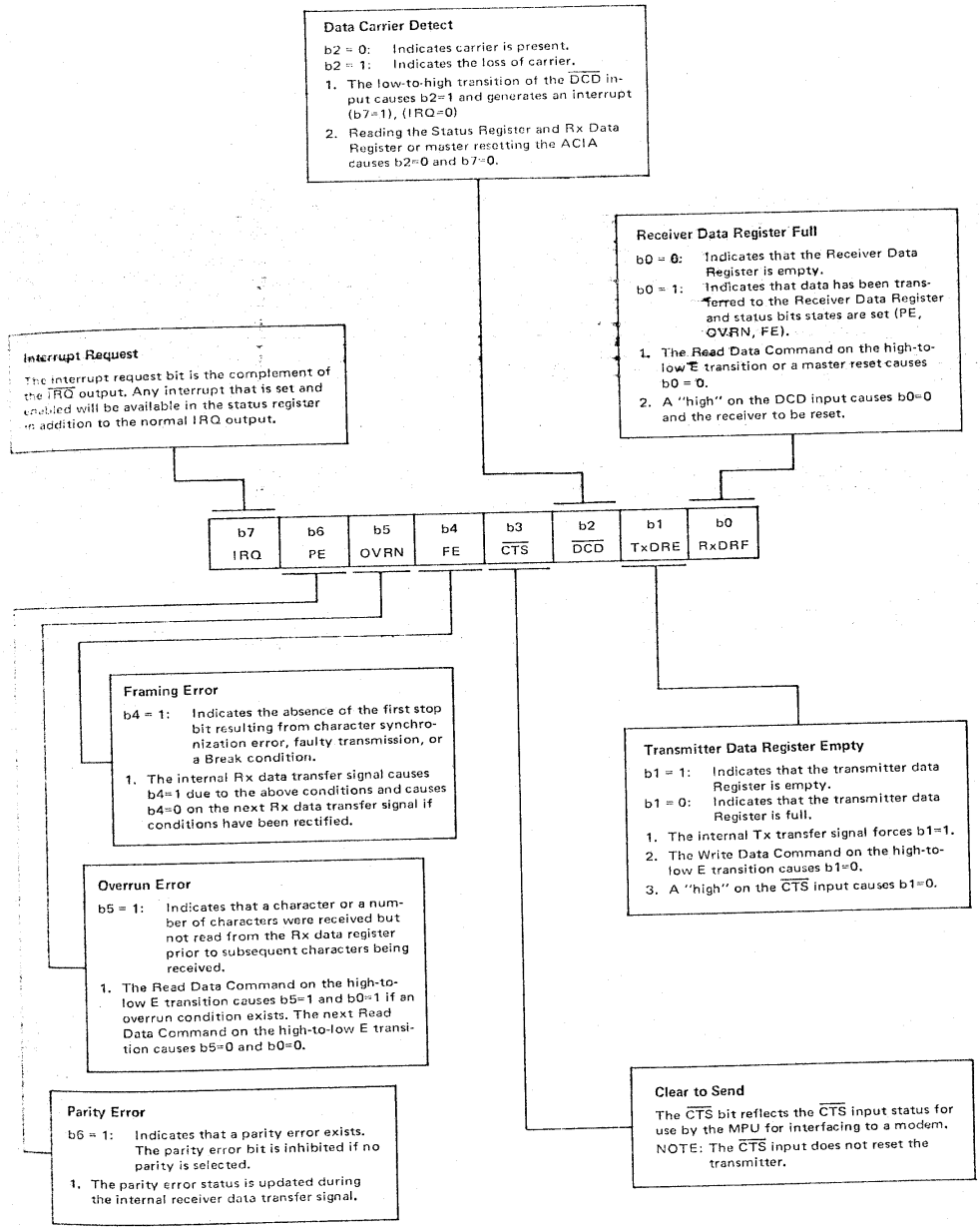


FIGURE 3-4.2.2-2: ACIA Status Register Format

$\overline{CS2}$	CS1	CSϕ	RS	R/W	
ϕ	1	1	ϕ	ϕ	Control Register
ϕ	1	1	ϕ	1	Status Register
ϕ	1	1	1	ϕ	Transmit Data Register
ϕ	1	1	1	1	Receive Data Register
X	X	ϕ	X	X	ACIA Not Selected
X	ϕ	X	X	X	ACIA Not Selected
1	X	X	X	X	ACIA Not Selected

X = Don't Care

FIGURE 3-4.2.3-1: ACIA Register Addressing

R/W = 1 = Read, Status Register is selected. Similarly, when RS = 1, either the Receive Data Register (R/W = 1 = Read) or the Transmit Data Register (R/W = 0 = Write) is selected.

Addressing the ACIA can be illustrated in conjunction with the simple system configuration shown in Figure 3-4.1.3-2[10]. The method shown is typical for assigning mutually exclusive memory addresses to the family devices without the use of additional decode logic. The connections shown assign memory addresses as follows:

RAM	0000 – 007F
PIA	4004 – 4007
ACIA	4008 – 4009
ROM	C000– C3FF

(Hexadecimal notation)

As voltage is applied to the ACIA during the power-on sequence, its internal registers are cleared to zero[11] by circuitry within the ACIA to prevent spurious outputs. This initial condition means that interrupts are disabled, IRQ to the MPU is high (no interrupt request), and the Ready-To-Send, $\overline{RTS}$, output is high. The first step in preparation for using the ACIA must be a master reset via bits b0 and b1 of the Control Register, that is, the MPU must write ones into those positions. Once reset, the ACIA operating mode is established by writing the appropriate data into the Control Register.

3-4.2.4 System Considerations

The ACIA is used primarily to transfer serial data between the microprocessor and real time peripheral devices such as teletypes, CRT terminals, etc. The most common data format used for the transfer of real-time data is the asynchronous data format. Use of this format is generally limited to low transmission rates — below 1200 bps or 120 char/sec. For example, the maximum transmission rate of a teletype is 10 char/sec. Here, the transmission of data to the MPU depends on the operator's dexterity of depressing a key on the keyboards. Since the transmission of data is dependent on the operator, gaps (non transmission of data) between data characters occur as a general rule.

In the transmission of asynchronous data, there is no pre-synchronized clock provided along with the data. Also, the gaps between data characters in this transmission mode requires that synchronization be re-established for each character. Therefore, the receiving device must be capable of establishing bit and

[10] Figure 3-4.1.3-1 is identical to Figure 1-1.2-1 and is discussed in Section 1-1.2 of Chapter 1.

[11] If external high signals are present on the $\overline{DCD}$ and $\overline{CTS}$ inputs, their respective bits, b2 and b3, in the Status Register will also be high.

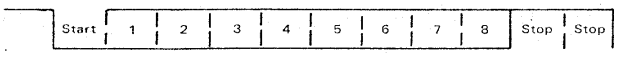
character synchronization from the characteristics of the asynchronous format. Each character consists of a specified number of data bits preceded by a start bit and followed by one or more stop bits as shown in Figure 3-4.2.4-1.

These start and stop elements do not contain any information and they actually slow down the effective transmission rate. Since the asynchronous format is used in real time systems, the effect of the start and stop bits on the transmission rate is negligible. The purpose of the start bit is to enable a receiving system to synchronize its clock to this bit for sampling purposes and thereby establish character synchronization. The stop bit is used as a final check on the character synchronization.

Since the MPU processes eight bit parallel bytes that do not include start and stop elements, received serial data in an asynchronous format must be converted to parallel form with the start and stop elements stripped from the character. Likewise, in order to transmit serial data the parallel data byte from the MPU must be converted to serial form with the start and stop elements added to the character. This serial-to-serial/parallel-to-parallel conversion is the primary function of the ACIA.

Desired options such as variable clock divider ratios, variable word length, one or two stop bits, odd or even parity, etc. are established by writing an appropriate constant into the ACIA's Control Register. The combination of options selected depends on the desired format for a particular application. The general characteristics of data flow-through the ACIA are described in the following paragraphs.

A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence may be continued until all the characters have been transmitted.



Start Bit – "Space" – Logic Zero
Start Bits – "Mark" – Logic One
Idling Bits – "Mark"

FIGURE 3-4.2.4-1: Asynchronous Data Format

Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an external clock that is synchronized to its data; the divide by 16 and 64 ratios may be used for internal synchronization. Bit synchronization in the divide by 16 and 64 modes is obtained by detecting the leading mark-to-space transition of the start bit. False start bit detection capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the possible error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the Data Bus when the MPU reads the ACIA Receive Data Register. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence may be continued until all characters have been received.

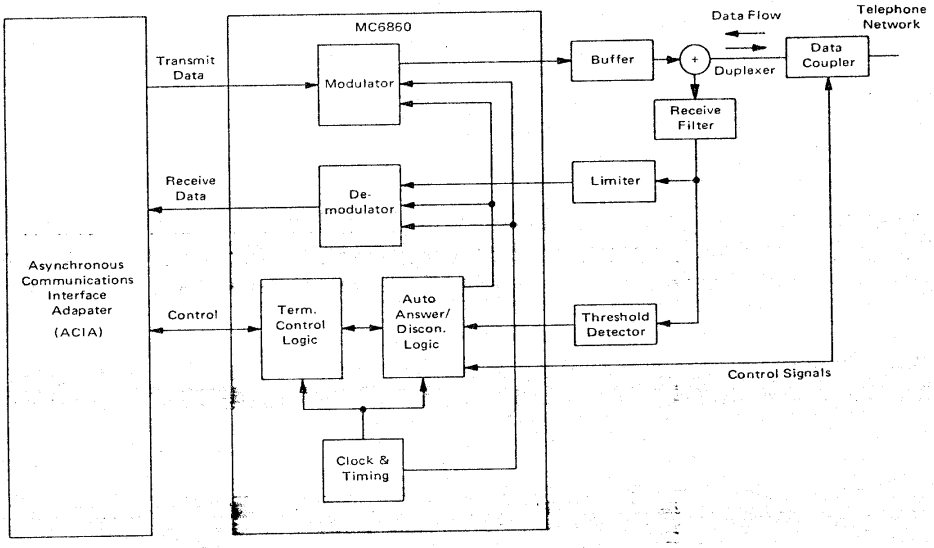


FIGURE 3-4.3.1-1: Typical MC6860 System Configuration

3-4.3 MC6860 LOW SPEED MODEM

3-4.3.1 Input/Output Configuration

The MC6860 Modem provides a very effective method of interfacing a MPU based system, via a MC6850 ACIA, to a telephone network as shown in Figure 3-4.3.1-1. The modem provides full automatic answer/originate and initiate disconnect capability under MPU program control thru the ACIA. Data may be asynchronously sent and received over the telephone network at data rates up to 600 bits per second.

The Input/Output configuration of the MC6860 when used with the MC6850 ACIA and the MC6800 MPU family is shown in Figure 3-4.3.1-2. Data flow from the terminal side of the modem enters in serial digital format via the transmit data line of the modem. It is then digitally processed by the modulator section and exits the telephone network side of the modem via the transmit carrier line. This digitized sinewave FSK signal is post filtered by an output buffer/low pass filter. The filtered analog sinewave passes through a line duplexer to the telephone line via a data coupler.

The returning analog signal from the remote modem at the other end of the telephone line passes through the data coupler and duplexer and is applied to a bandpass filter/amplifier. The receive bandpass filter bandlimits the incoming signal to remove noise and adjacent transmit channel interference. After being bandlimited the analog signal is full limited to a 50% duty cycle TTL level signal by the input limiter. This digital signal is the receive carrier that is applied to the modem. The output signal from the bandpass filter is also routed to a threshold detector to determine if the input signal to the limiter is above the minimum detectable signal level presented to the modem. When the signal input level exceeds the bias point of the threshold detector, the detector's output goes low at the threshold input pin to the MC6860 modem indicating that carrier is present.

A complete listing and functional description of all I/O pins for the MC6860 (Figure3-4.3.2-1) is provided in the following:

Data Terminal Ready ($\overline{DTR}$)

The Data Terminal Ready signal must be low before the modem function will be enabled. To initiate a disconnect, $\overline{DTR}$ is held high for 34 msec minimum. A disconnect will occur 3 seconds later.

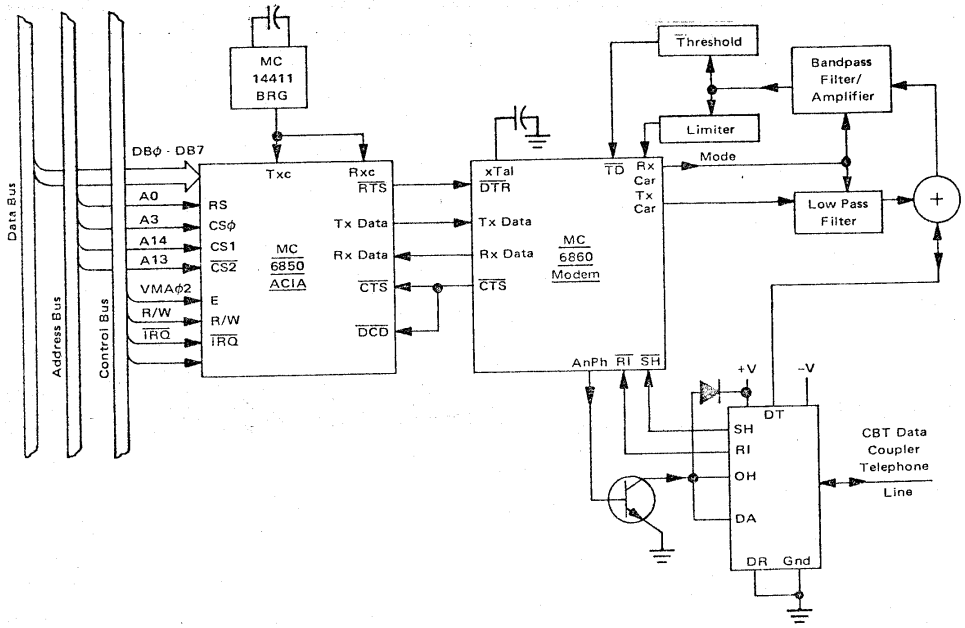


FIGURE 3-4.3.1-2: I/O Configuration For MC6860 Modem

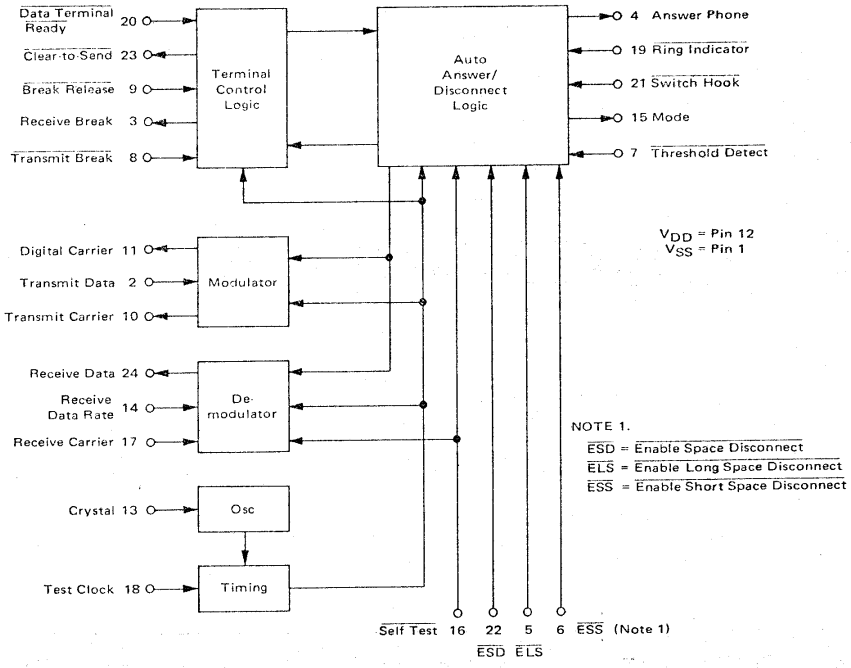


FIGURE 3-4.3-2-1: MC6860 Modem Block Diagram

Clear-To-Send ($\overline{CTS}$)

A low on the $\overline{CTS}$ output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.

Ring Indicator ($\overline{RI}$)

The modem function will recognize a receipt of a call from the CBT if at least 20 cycles of the 20-47 Hz ringing signal are present. The CBS $\overline{RI}$ signal must be level-converted from EIA RS-232 levels before interfacing it with the modem function. The receipt of a call from the CBS is recognized if the $\overline{RI}$ signal is present for at least 51 msec. This input is held high except during ringing. A $\overline{RI}$ signal automatically places the modem function in the Answer Mode.

Switch Hook ($\overline{SH}$)

$\overline{SH}$ interfaces directly with the CBT and via a EIA RS-232 level conversion for the CBS. An $\overline{SH}$ signal automatically places the modem function in the Originate Mode.

$\overline{SH}$ is low during origination of a call. The modem will automatically hang up 17 seconds after the release of $\overline{SH}$ if the handshaking routine between the local and remote modem has not been accomplished.

Threshold Detect ($\overline{TD}$)

This input is derived from an external threshold detector. If the signal level is sufficient, the $\overline{TD}$ input must be low for 20μs at least once every 32 msec to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for greater than 32 msec will not cause channel establishment to be lost; however, data during this interval will be invalid.

Answer Phone (An Ph)

Upon receipt of Ring Indicator or Switch Hook signal and Data Terminal Ready, the Answer Phone output goes high [($\overline{SH}$ + $\overline{RI}$) • $\overline{DTR}$]. This signal drives the base of a transistor which activates the Off Hook (OH) and Data Transmission (DA) control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.

Mode

The Mode output indicates the Answer (low) or Originate (high) status of the modem. This output changes state when a Self Test command is applied.

Transmit Break ($\overline{Tx\ Brk}$)

The Break command is used to signal the remote modem to stop sending data.

A Transmit Break (low) greater than 34 msec forces the modem to send a continuous space signal for 233 msec. Transmit Break must be initiated only after $\overline{CTS}$ has been established. This is a negative edge sense input. Prior to initiating $\overline{Tx\ Brk}$, this input must be held high for a minimum of 34 msec.

Receive Break (Rx Brk)

Upon receipt of a continuous 150 msec space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-To-Send is established.

Break Release ($\overline{Brk\ R}$)

After receiving a 150 msec space signal, the clamped high condition of the Receive Break output can be removed by holding Break Release low for at least 20 μs.

Transmit Data (Tx Data)

Transmit Data is the binary information presented to the modem function for modulation with FSK techniques. A high level represents a Mark.

Receive Data (Rx Data)

The Receive Data output is the data resulting from demodulating the Receive Carrier. A Mark is a high level.

Receive Data Rate (Rx Rate)

The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input should be low for 0-600 bps and should be high for 0-300 bps.

Digital Carrier (FO)

A test signal output is provided to decrease the chip test time. The signal is a square wave at the transmit frequency.

Transmit Carrier (Tx Car)

The Transmit Carrier is a digitally-synthesized sinewave derived from the 1.0 MHz crystal reference. The frequency characteristics are as follows:

Mode	Data	Transmit Frequency	Accuracy*
Originate	Mark	1270 Hz	−0.15 HZ
Originate	Space	1070 Hz	+0.09 Hz
Answer	Mark	2225 Hz	−0.31 Hz
Answer	Space	2025 Hz	−0.71 Hz

*The reference frequency tolerance is not included.

The proper output frequency is transmitted within the 3.0 μs following a data bit change with no more than 2.0 μs phase discontinuity. The typical output level is 0.35 V (RMS) into a 200 k-ohm load impedance.

The second harmonic is typically 32 dB below the fundamental.

Receive Carrier (Rx Car)

The Receive Carrier is the FSK input to the demodulator. The local Transmit Carrier must be balanced or filtered out prior to this input, leaving only the Receive Carrier in the signal. The Receive Carrier must also be hard limited. Any half-cycle period greater than or equal to 429 ± 1.0 μs for the low band or 235 ± 1.0 μs for the high band is detected as a space.

Enabled Space Disconnect ($\overline{\text{ESD}}$)

When $\overline{\text{ESD}}$ is strapped low and $\overline{\text{DTR}}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 seconds or until a loss of threshold is detected, whichever occurs first. If $\overline{\text{ESD}}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 seconds.

Enable Short Space Disconnect ($\overline{\text{ESS}}$)

$\overline{\text{ESS}}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 seconds. *$\overline{\text{ESS}}$ and $\overline{\text{ELS}}$ must not be simultaneously strapped low.*

Enable Long Space Disconnect ($\overline{\text{ELS}}$)

ELS is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 seconds.

Crystal (Xtal)

A 1.0-MHz crystal with the following parameters is required to utilize the on-chip oscillator. A 1.0-MHz square wave can also be fed into this input to satisfy the clock requirement.

Mode:	Parallel
Frequency:	1.0 MHz ±0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0-70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

When utilizing the 1.0-MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be ≤9 pF at the crystal input.

Test Clock ($\overline{TST}$)

A test signal input is provided to decrease the test time of the chip. In normal operation this input *must be strapped low.*

Self Test ($\overline{ST}$)

When a low voltage level is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occurred during the initial handshake, is not lost during self test. The Mode Control output changes state during $\overline{Self\ Test}$, permitting the receive filters to pass the local Transmit Carrier.

INPUTS			OUTPUT
ST	SH	RI	Mode
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

MODE CONTROL TRUTH TABLE

3-4.3.2 Internal Organization

The MC6860 Modem may be broken down into internal functional sections as shown in Figure 3-4.3.2-1. The terminal control logic and auto answer/disconnect logic sections are referred to as the supervisory control section. This section contains digital counters which provide the required time out intervals and necessary control gating logic. This provides logic outputs Clear-To-Send and Answer Phone from inputs Ring Indicator, Switch Hook, and Data Terminal Ready. Also the control section has some local strapping options available on pins 5, 6, and 22. These options provide time outs for line hang-up or termination of the data communication channel.

The oscillator/timing blocks accept a 1.0 MHz clock into pin 13 either from an external clock source or by connecting a 1.0 MHz crystal between pin 13 and ground. A test clock input is provided to allow more rapid testing of the MC6860 timing chains used for various timeouts. This input must be strapped low during normal operation.

The modulator section takes the input digital data and converts it to one of two FSK tones for transmission over the telephone network. There are two tones for transmission and two tones used for reception during full depulx operation. During data transmission from the call origination modem the transmit tones are: 1270 Hz for a Mark and 1070 Hz for a Space. This originating modem will receive two frequencies in the high band which are: 2225 Hz for a Mark and 2025 Hz for a space. If the local modem answers the data call it will transmit in the high band 2225/2025 Hz and receive in the low band 1270/1070 Hz. The modulator section generates these frequencies digitally by synthesizing a sinewave with an 8 step D to A available on pin 10 and a digital square wave output at the above frequencies available on pin 11.

The demodulator accepts a 50% duty cycle TTL level square wave derived from amplifying, filtering, and limiting the incoming line FSK analog signal. The binary data is recovered from the FSK signal by detecting when the signal has a zero crossing and digitally using post detection techniques to discriminate

between the two incoming mark/space tones. A receive data rate input (pin 14) is used to optimize the post detection filter at either 300 or 600 bits per second.

3-4.3.3 Handshaking and Control

The supervisory control section of the modem can function in four different modes. Two are associated with data communication channel initialization (Answer Mode and Originate Mode) and two are for channel termination or hang-up (Automatic Disconnect and Initiate Disconnect).

Answer Mode

Automatic answering is first initiated by a receipt of a Ring Indicator ($\overline{RI}$) signal. This can be either a low level for at least 51 msec as would come from a CBS data coupler, or at least 20 cycles of a 20-47 Hz ringing signal as would come from a CBT data coupler. The presence of the Ring Indicator signal places the modem in the Answer Mode; if the Data Terminal Ready line is low, indicating the communication terminal is ready to send or receive data, the Answer Phone output goes high. This output is designed to drive a transistor switch which will activate the Off Hook (OH) and Data Transmission (DA) relays in the data coupler. Upon answering the phone the 2225-Hz transmit carrier is turned on.

The originate modem at the other end detects this 2225-Hz signal and after a 450 msec delay (used to disable any echo suppressors in the telephone network) transmits a 1270-Hz signal which the local answering modem detects provided the amplitude and frequency requirements are met. The amplitude threshold is set external to the modem chip. If the signal level is sufficient the $\overline{TD}$ input should be low for 20 μs at least once every 32 msec. The absence of a threshold indication for a period greater than 51 msec denotes the loss of Receive Carrier and the modem begins hang-up procedures. Hang-up will occur 17 seconds after $\overline{RI}$ has been released provided the handshaking routine is not re-established. The frequency tolerance during handshaking is $\pm$100 Hz from the Mark frequency.

After the 1270-Hz signal has been received for 150 msec, the Receive Data is unclamped from a Mark condition and data can be received. The Clear-To-Send output goes low 450 msec after the receipt of carrier and data presented to the answer modem is transmitted.

Automatic Disconnect

Upon receipt of a space of 150 msec or greater duration, the modem clamps the Receive Break high. This condition exists until a Break Release command is issued at the receiving station. Upon receipt of a 0.3 second space, with Enable Short Space Disconnect at the most negative voltage (low), the modem automatically hangs up. If Enable Long Space Disconnect is low, the modem requires 1.5 seconds of continuous space to hang up.

Originate Mode

Upon receipt of a Switch Hook ($\overline{SH}$) command the modem function is placed in the Originate Mode. If the Data Terminal Ready input is enabled (low) the modem will provide a logic high output at Answer Phone. The modem is now ready to receive the 2225-Hz signal from the remote answering modem. It will continue to look for this signal until 17 seconds after SH has been released. Disconnect occurs if the handshaking routine is not established.

Upon receiving 2225 $\pm$100 Hz for 150 msec at an acceptable amplitude, the Receive Data output is unclamped from a Mark condition and data reception can be accomplished. 450 msec after receiving a 2225-Hz

signal, a 1270-Hz signal is transmitted to the remote modem. 750 msec after receiving the 2225-Hz signal, the Clear-To-Send output is taken low and data can now be transmitted as well as received.

Initiate Disconnect

In order to command the remote modem to automatically hang up, a disconnect signal is sent by the local modem. This is accomplished by pulsing the normally low Data Terminal Ready into a high state for greater than 34 msec. The local modem then sends a 3 second continuous space and hangs up provided the Enable Space Disconnect is low. If the remote modem hangs up before 3 seconds, loss of Threshold Detect will cause loss of Clear-To-Send, which marks the line in Answer Mode and turns the carrier off in the Originate Mode.

If $\overline{\text{ESD}}$ is high the modem will transmit data until hang-up occurs 3 seconds later. Transmit Break is clamped 150 msec following the Data Terminal Ready interrupt.

Each of the four above operational modes are shown in Figures 3-4.3.3-1 through 3-4.3.3-4.

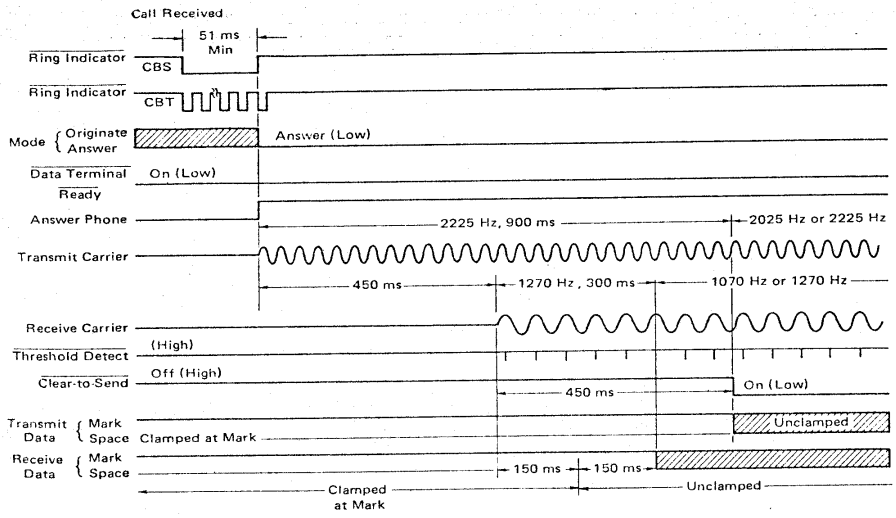


FIGURE 3-4.3.3-1: Answer Mode

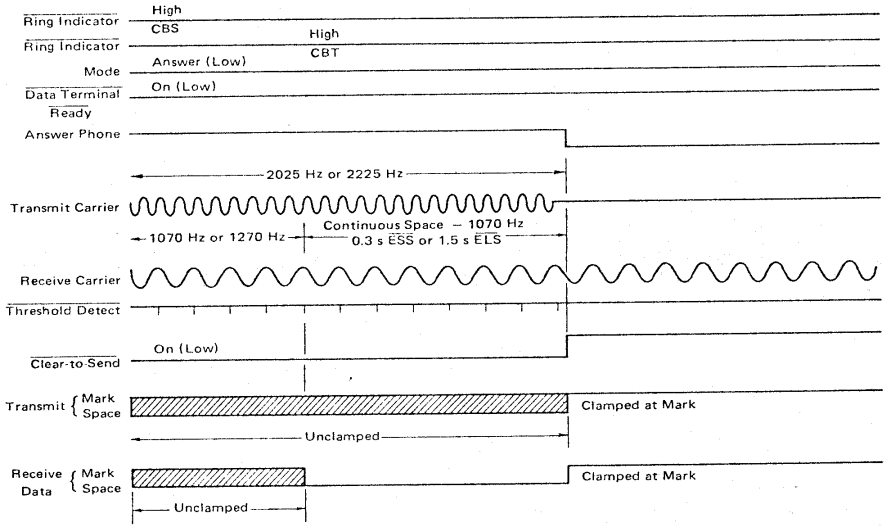


FIGURE 3-4.3.3-2: Automatic Disconnect - Long or Short Space

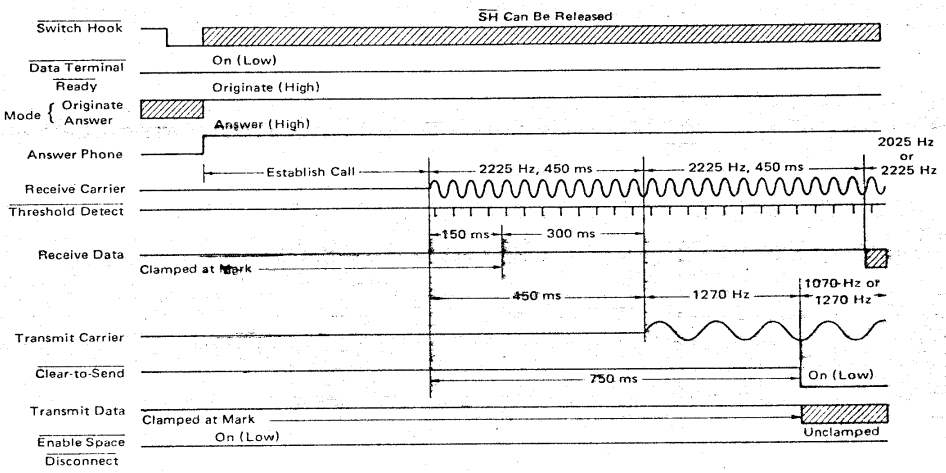


FIGURE 3-4.3.3-3: Originate Mode

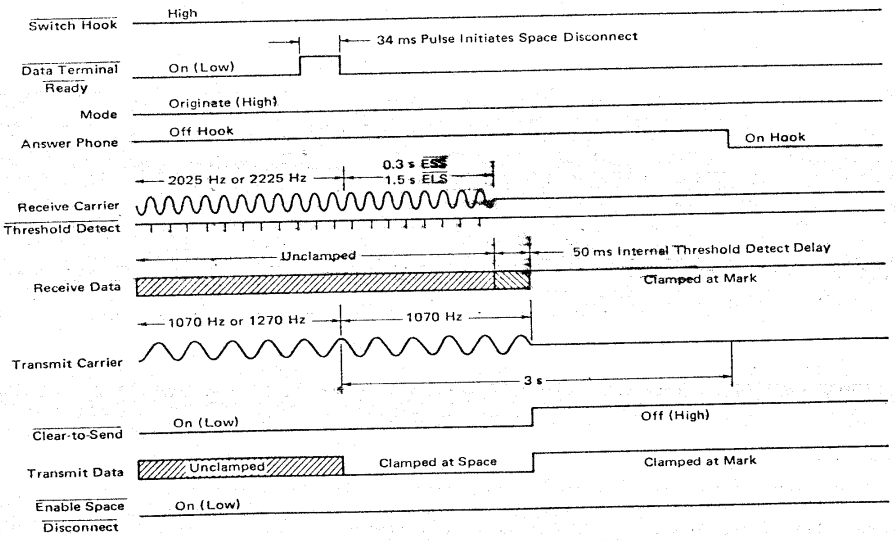


FIGURE 3-4.3.3-4: Initiate Disconnect