National Semiconductor

MOS EPROMs

MM4203/MM5203 2048-Bit (256 × 8 or 512 × 4) UV Erasable PROM

General Description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

Applications

- Code conversion
- Random logic synthesis
- Table look-up
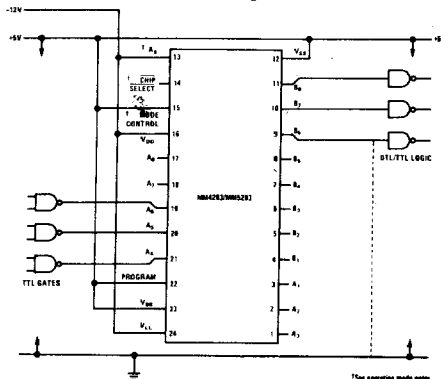- Character generator
- Micro-programming

Features

- Field programmable
- Bipolar compatibility   +5V, −12V operation
- High speed operation   1μs max access time

Block and Connection Diagrams

Dual-In-Line Package
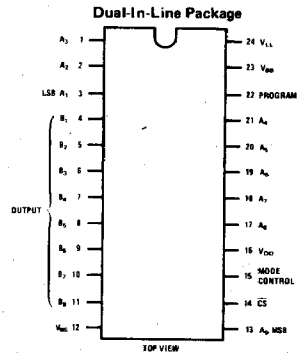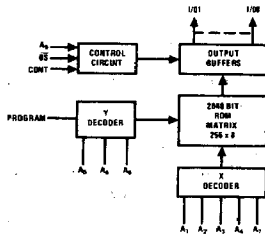
Order Number MM4203Q or MM5203Q
See NS Package J24CQ

Typical Applications

256 x 8 PROM Showing TTL Interface

Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A_9 — LOW
512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A_9 — Logic HIGH enables the odd $(B_1, B_3..B_7)$ outputs
— Logic LOW enables the even $(B_2, B_4.. B_8)$ outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

Absolute Maximum Ratings

All Input or Output Voltages with
Respect to V_{BB} Except During Programming   +.3V to –20V
Power Dissipation   1W
Storage Temperature Range   –65°C to 125°C
Lead Temperature (Soldering, 10 sec)   300°C

Operating Conditions

Operating Temperature Range MM4203   –55°C to 85°C
MM5203   0°C to 70°C

Electrical Characteristics T_A within operating temperature range,

$V_{SS} = +5V \pm 5\%$, $V_{DD} = V_{LL} = -12V$, $\pm 5\%$, $V_{BB} = $ PROGRAM $= V_{SS}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Current	$V_{IN} = 0V$			1	μA
I_{LO}	Output Leakage	$V_{OUT} = 0V$ $\overline{CS} = V_{SS} - 2.0$			1	μA
I_{SS}	Power Supply Current	$T_A = 25°C$ $\overline{CS} = V_{SS} - 2.0$		35	55	mA
V_{IL}	Input LOW Voltage		$V_{SS} - 10$		$V_{SS} - 4.0$	V
V_{IH}	Input HIGH Voltage		$V_{SS} - 2.0$		$V_{SS} + .3$	V
V_{OL}	Output LOW Voltage	1.6 mA sink $-12.6V < V_{LL} < -3V$			.40	V
I_{CF}	Output Clamp Current	$V_{LL} = -3.0V$ $V_{OUT} = -1.0V$ (Note 8) $T_A = 0°C$		3.5	6.0	mA
		$V_{LL} = -12.6V$ $V_{OUT} = -1.0V$ (Note 8) $T_A = 0°C$		8.0	15.0	mA
V_{OH}	Output HIGH Voltage	0.8 mA source	2.4			V
T_{OH}	Data Hold Time	(Min Access Time) Figures 1 & 2			100	ns
T_{ACC}	Access Time	$T_A = 25°C$ Figures 1 & 2 (Note 6)		.700	1	μs
T_{CO}	Chip Select Time	Figures 1 & 3			500	ns
T_{OD}	Chip Deselect Time	Figures 1 & 3			500	ns
t_{CS}	Allowable Chip Select Delay	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
C_{IN}	Input Capacitance	$V_{IN} = V_{SS}$ } f = 1.0 MHz (Note 2)		8	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = V_{SS}$ } $\overline{CS} = V_{SS} - 2.0$		8	15	pF

Programming Characteristics (see Figure 4)

$T_A = 25°C$, $V_{SS} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LD}	Address and Data Input Load Current	$V_{IN} = -50V$		0	10	mA
I_{LP}	Program Load Current	$V_{IN} = -50V$		0	10	mA
I_{LB}	V_{BB} Supply Load Current			0	10	mA
I_{LDD}	Peak I_{DD} Supply Load Current (Note 3)	$V_{DD} = V_{program} = -50V$		650		mA
V_{IHP}	Input High Voltage		-2		$+.3$	V
V_{ILP}	Address and Data Input Low Voltage		-50		-40	V
	Pulsed Input Low Voltage:					
	V_{DD}, and Program, V_{DLP}		-50		-48	V
	V_{LL}	(Note 5)	-50		0	V
	V_{DD} Pulse Duty Cycle				2	%
t_{PW}	Program Pulse Width (Note 4)	$V_{DD} = V_{program} = -50V$			20	ms
t_{DW}	Data and Address Set Up Time			1		μs
t_{DH}	Data and Address Hold Time,			0		μs
t_{SS}	Pulsed V_{DD} Supply Overlap,			1	100	μs
t_{SH}	Pulsed V_{DD} Supply Overlap,			$-.1$	3	ms
	V_{DD}, Program, Address, and Input Rise and Fall Times				1	μs

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of A_9 and MODE CONTROL.
Note 2: Capacitances are not tested on a production basis but are periodically sampled.
Note 3: I_{DP} flows only during program period t_{PW}. Average power supply current I_{LDD} is typically 15 mA at 2% duty cycle.
Note 4: Maximum duty cycle of t_{PW} should not be greater than 2% of cycle time so that power dissipation is minimized. The program cycle should be repeated until the data reads true, then over-program three times that number of cycles (symbolized as X+3X programming.
Note 5: V_{LL} is not needed during programming but may be tied to V_{DD} for convenience.
Note 6: $T_{ACC} = 1000$ ns + 25(N–1) where N is the number of chips wired-OR together.
Note 7: Measured under continuous operation.
Note 8: I_{CF} flows out the V_{LL} pin, it does not flow out the V_{DD} pin.
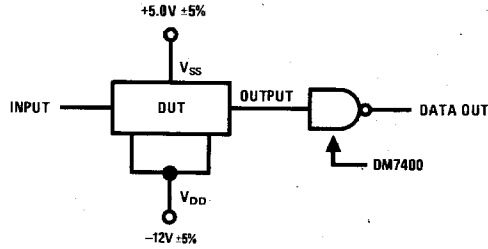
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Access Time Diagrams

+5.0V ±5%

V_{SS}

INPUT — DUT — OUTPUT — DATA OUT

DM7400

V_{DD}

−12V ±5%

Figure 1

H
ADDRESS
L
$V_{SS} - 2.0V$
$V_{SS} - 4.0V$

T_{CS}

CHIP SELECT
$V_{SS} - 2.0V$
T_{OH}
L
$V_{SS} - 4.0V$

H
DATA OUT NOT VALID
DATA OUT VALID
DATA OUT NOT VALID
DATA OUT
T_{ACC}

Figure 2

H
CHIP SELECT
L
$V_{SS} - 2.0V$
$V_{SS} - 4.0V$

H
DATA OUT
DATA OUT NOT VALID
DATA VALID
DATA OUT NOT VALID
L
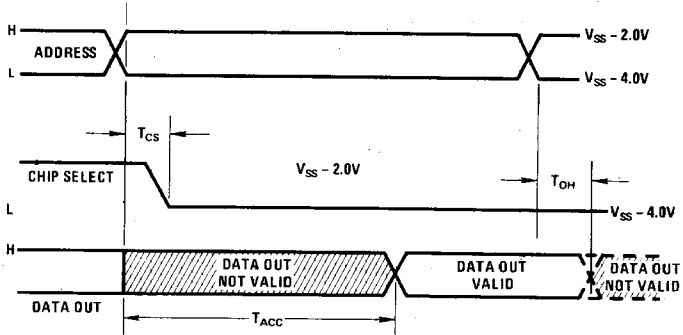
Figure 3

Program Waveforms

ADDRESS & DATA INPUTS
MAY CHANGE
INPUT STABLE
MAY CHANGE
V_{IHP}
V_{ILP}

t_{DW}
t_{DH}

V_{DD}
V_{IHP}
V_{DLP}

t_{SS}
t_{SH}

V_{PROG}
V_{IHP}
V_{DLP}

t_{PW}

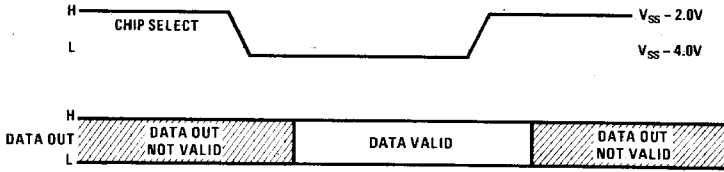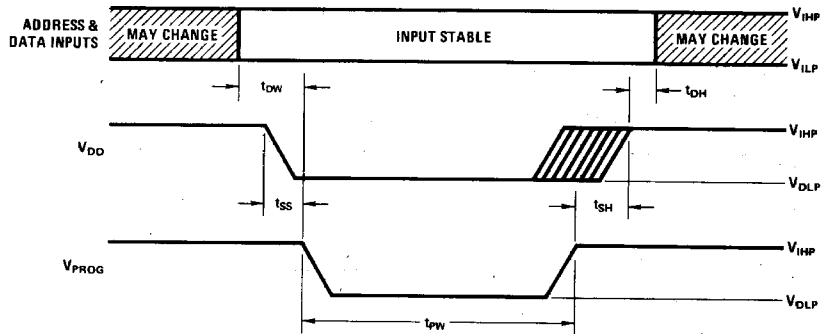**Figure 4**

Operation of the MM4203/MM5203 in Program Mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. (Note 1)

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (–50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. The address should be applied for at least 1 μs before application of the Program pulse. In programming mode, data inputs

1–8 are pins 4–11 respectively regardless of the logic state of A_9 and mode control. Chip select should be disabled (HIGH).

Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

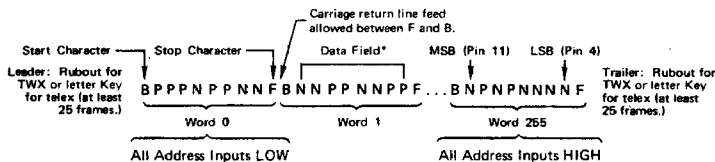| MODE	DATA AND ADDRESS LINES		V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
	HIGH	LOW						
Read	V_{SS} – 2.0	V_{SS} – 4.0	+5	V_{SS}	–12	V_{SS}	V_{SS} – 4V	–3V to –12V
Program	V_{SS} –2.0	V_{SS} – 40	GND	+12	–48 (Pulse)	–48 (Pulse)	GND	GND to –50V

Erasing Procedure

The MM4203Q/MM5203Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24

minutes. Examples of UV sources include the Model UVS-54 and Model S-2 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4203/MM5203 should be placed about one inch away from the lamp for about 20–30 minutes.
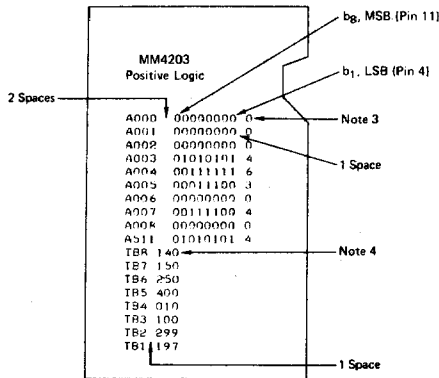
Preferred Tape Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code

from model 33 teletype or TWX. The paper tape should be as the following example:

Carriage return line feed
allowed between F and B.

Start Character —┐ ┌— Stop Character —┐   ┌— Data Field*   MSB (Pin 11)   LSB (Pin 4)
Leader: Rubout for   Trailer: Rubout for
TWX or letter Key   TWX or letter Key
for telex (at least   B P P P N P P N N F B N N P P N N P P F ... B N P N P N N N N F   for telex (at least
25 frames.)   25 frames.)
                       └———— Word 0 ————┘ └— Word 1 —┘   └— Word 255 —┘

                       └———————————————┘   └——————————————┘
                       All Address Inputs LOW   All Address Inputs HIGH

*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N
characters between B and F. Any characters except B and F may be typed between the F stop character and the B start
character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must
be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

Alternate Format [Punched Tape (Note 1) or Cards]

```
                              bg, MSB (Pin 11)

        MM4203
        Positive Logic            b1, LSB (Pin 4)

2 Spaces

        A000  00000000 0         Note 3
        A001  00000000 0
        A002  00000000 0
        A003  01010101 4         1 Space
        A004  00111111 6
        A005  00111100 3
        A006  00000000 0
        A007  00111100 4
        A008  00000000 0
        A511  01010101 4
        TB8  140                 Note 4
        TB7  150
        TB6  250
        TB5  400
        TB4  010
        TB3  100
        TB2  299
        TB1  197

                                 1 Space
```

Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

Typical Performance Characteristics

Maximum Supply Current I_{SS} as a Function of Temperature

Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage