NEC

NEC Electronics Inc.

μPD27256
32,768 x 8-BIT
NMOS UV EPROM

Revision 2

Description

The μPD27256 is a 262,144-bit electrically programmable read-only memory utilizing NMOS double-polysilicon technology. The device is organized as 32K words by 8 bits and operates from a single +5V ±5% power supply. All inputs and outputs are TTL-compatible. The μPD27256 has single location programming, three-state outputs and is pin-compatible with the 27C256 EPROM. It is available as a 28-pin DIP.

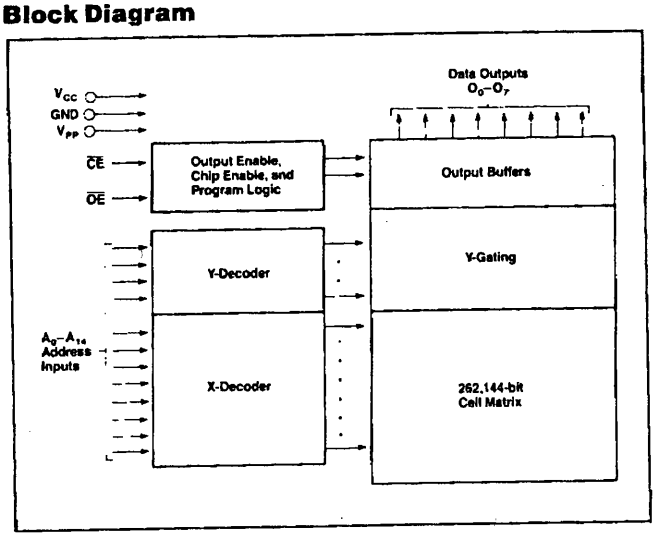
The μPD27256 is available in a cerdip package with a quartz window as an ultraviolet (UV), erasable EPROM.

Features

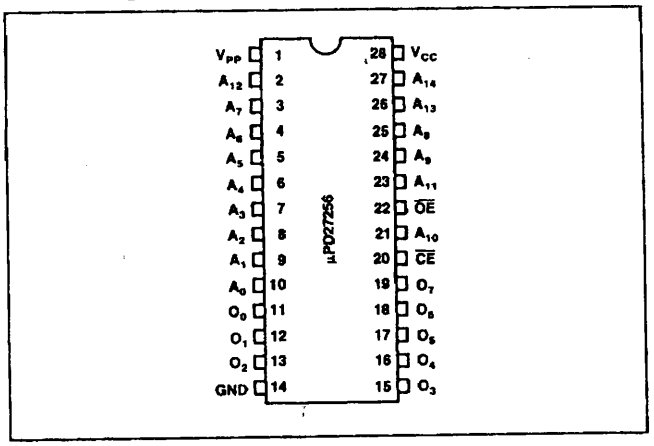
- ☐ 32K by 8 organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time — 200ns max
- ☐ Single location programming
- ☐ High-speed programming mode
- ☐ Low power dissipation: 100mA max (active)
  25mA max (standby)
- ☐ Input/output TTL-compatible for reading and programming
- ☐ Single +5V ±5% power supply
- ☐ Three-state outputs
- ☐ Pin-compatible with μPD27C256 EPROM
- ☐ NMOS double-polysilicon technology
- ☐ 28-pin DIP
- ☐ 3 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD27256	250ns	100mA	25mA
μPD27256-3	300ns	100mA	25mA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Description
1	V_{PP}	Program Voltage
2–10, 21, 23–27	A_0–A_{14}	Address Inputs
11–13, 15–19	O_0–O_7	Data Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22	$\overline{OE}$	Output Enable
28	V_{CC}	+5V ±5% Power Supply

Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{PP}	V_{CC}	High-Z

Note: X can be either V_{IL} or V_{IH}.

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Absolute Maximum Ratings*

Operating Temperature, T_{OPR}	−10°C to +80°C
Storage Temperature, T_{STG}	−65°C to +125°C
Output Voltage, V_{OH}	−0.6V to V_{CC} +6.5V
Input Voltage, V_{IH}	−0.6V to V_{CC} +6.5V
Supply Voltage, V_{CC}	−0.6V to +7V
Supply Voltage, V_{PP}	−0.6V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance ①

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0V

Note: ① This parameter is sampled periodically.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{PP} = V_{CC}

Read and Standby Modes

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 to V_{CC}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
V_{CC} Current	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC2}			100	mA	$\overline{CE}$ = V_{IL} (active)
V_{PP} Current	I_{PP1}			15	mA	V_{PP} = 5.25V

T_A = 25°C ± 5°C; V_{CC} = 6V ± 0.25V; V_{PP} = +21V ± 0.5V

Program, Program Verify, and Program Inhibit Modes

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage	V_{OH}	2.4			V	V_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	I_{CC2}			100	mA	
V_{PP} Current	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}

AC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{PP} = V_{CC}

Read and Standby Modes

Parameter	Symbol	Limits 27256 Min	27256 Max	27256-3 Min	27256-3 Max	Unit	Test Conditions ①
Address to Output Delay	t_{ACC}		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
CE to Output Delay	t_{CE}		250		300	ns	$\overline{CE}$ = V_{IL}
Output Enable to Output Delay	t_{OE}		100		120	ns	$\overline{CE}$ = V_{IL}
Output Enable High to Output Float	t_{DF}	0	85		105	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE}$ = V_{IL}

Notes: ① Output load: see Figure 1.
Input rise and fall times: 20ns.
Input pulse levels: 0.45V to 2.4V.
Input and output timing measurement reference levels: 0.8V and 2.0V.

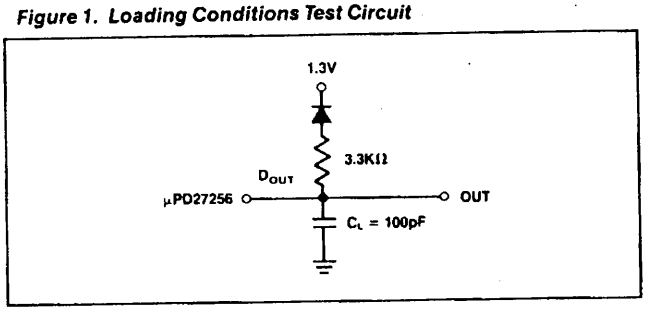
T_A = 25°C ± 5°C; V_{CC} = +6V ± 0.25V; V_{PP} = 21V ± 0.5V

Program, Program Verify, and Program Inhibit Modes ① ②

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Set-up Time	t_{AS}	2			μs	
Data Set-up Time	t_{DS}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Address Hold Time	t_{AH}	2			μs	Input pulse levels = 0.45V to 2.4V
Chip Enable to Output Float Delay	t_{DF}			130	ns	Input and output timing reference levels = 0.8V and 2.0V
V_{CC} = Set-up Time	t_{VS}	2			μs	
Program Pulse Width	t_{PW}	0.95	1	1.05	ms	Input rise and fall times = 20ns
$\overline{CE}$ Set-up Time	t_{CES}	2			μs	
$\overline{OE}$ Set-up Time	t_{OES}	2			μs	
$\overline{OE}$ Hold Time ③	t_{OEH}	2			μs	
$\overline{OE}$ Recovery Time ③	t_{OR}	2			μs	
$\overline{CE}$ to Output Valid ③	t_{DV}			1	μs	

Notes: ① V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
② V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.
③ These parameters are sampled periodically.

Figure 1. Loading Conditions Test Circuit



Programming Operation

High Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to +6 V ±.25 V; then raise V_{PP} to +21 V ±.5 V. Apply a 1 ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 20 times. If the bit is programmed within 20 tries, apply an additional overprogram pulse of (1 x number of tries) ms and input the next address. If the bit is not programmed in 20 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to +5 V ±5% and verify all data again.

Programming Inhibit Mode

Use the programing inhibit mode to program multiple μPD27256s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27256 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed data to determine that the data was correctly programmed. The program verification can be performed with the $\overline{CE}$ and $\overline{OE}$ at low levels (0).

Erasure

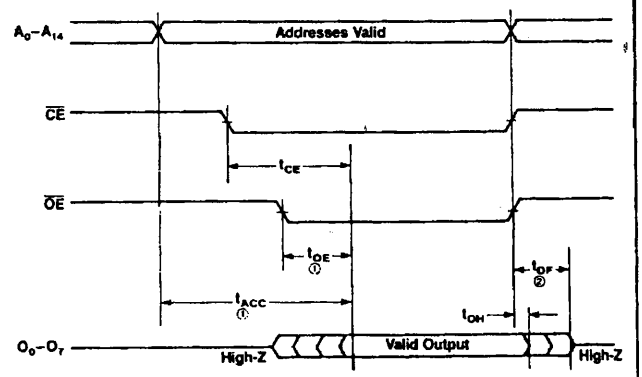
Erase data on the μPD27256 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm² (min) is required to completely erase written data (ultraviolet ray intensity x exposure time.)

An ultraviolet lamp rated at 12,000 μW/cm² takes approximately 15 to 20 minutes to complete erasure. Place the μPD27256 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode