MICROCHIP

27HC256

256K (32K x 8) High-Speed CMOS EPROM

FEATURES

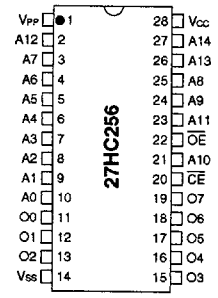
- High speed performance
  - 55 ns access time available
- CMOS Technology for low power consumption
  - 55 mA Active current
  - 100 µA Standby current
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line and SOIC package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin Very Small Outline Package (VSOP)
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

DESCRIPTION

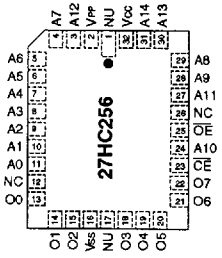
The Microchip Technology Inc. 27HC256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words of 8 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further reduction in the standby power requirement to 100 µA The 27HC256 is configured in a standard 256K EPROM pinout which allows an easy upgrade for present 27C256 users. A complete family of packages are offered to provide the utmost flexibility. The 27HC256 allows high performance microprocessors to run at full speed without the need of wait states. CMOS design and processing makes this part suitable for applications where high reliability and reduced power consumption are essential.

PACKAGE TYPE

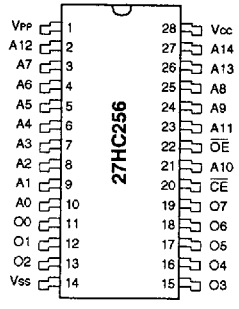
DIP



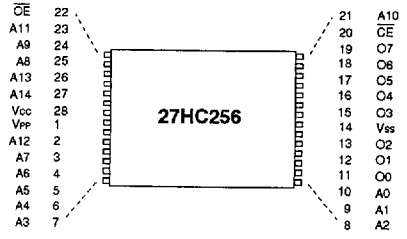
PLCC/LCC



SOIC



VSOP



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} ..... -0.6V to +7.25V

V_{PP} voltage w.r.t. V_{SS} during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. V_{SS} ..... -0.6V to +13.5V

Output voltage w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Temperature under bias ..... -65°C to +125°C

Storage temperature ..... -65°C to +150°C

Maximum exposure to UV ..... 7258Wsec/cm^2

ESD protection on all pins ..... 2 KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O0 - O7	Data Output
V_{CC}	+5V
V_{SS}	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V_{CC} = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	all		I_{LI}	-10	10	µA	V_{IN} = -0.1V to V_{CC} +1.0V
Output Voltages	all	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -4 µA I_{OL} = 16 mA
Output Leakage	all	—	I_{LO}	-10	10	µA	V_{OUT} = -0.1V to V_{CC} +0.1V
Input Capacitance	all	—	C_{IN}	—	6	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	I_{CC1} I_{CC2}	— —	55 65	mA mA	V_{CC} = 5.5V; V_{PP} = V_{CC} f = 2 MHz; $\overline{OE}$ = $\overline{CE}$ = V_{IL}; I_{OUT} = 0 mA; V_{IL} = -0.1 to 0.8V; V_{IH} = 2.0 to V_{CC}; Note 1
Power Supply Current, Standby, Std	C I,E	— —	$I_{CC(S)1}$	—	35 40	mA mA	
Power Supply Current, Standby, "L" version (low power)	C I,E I,E	TTL input TTL input CMOS input	$I_{CC(S)2}$	—	2 3 100	mA mA µA	 $\overline{CE}$ = V_{CC} ± 0.2V
I_{PP} Read Current V_{PP} Read Voltage	all all	Read Mode Read Mode	I_{PP} V_{PP}	V_{CC} -0.7	100 V_{CC}	µA V	V_{PP} = 5.5V Note 2

* Parts: C=Commercial Temperature Range; L = Low Power; I, E=Industrial and Extended Temperature Ranges

Note 1: Active current increases 3 mA per MHz for Commercial part or 5mA per MHz for Industrial or Extended temperature parts up to operating frequency.

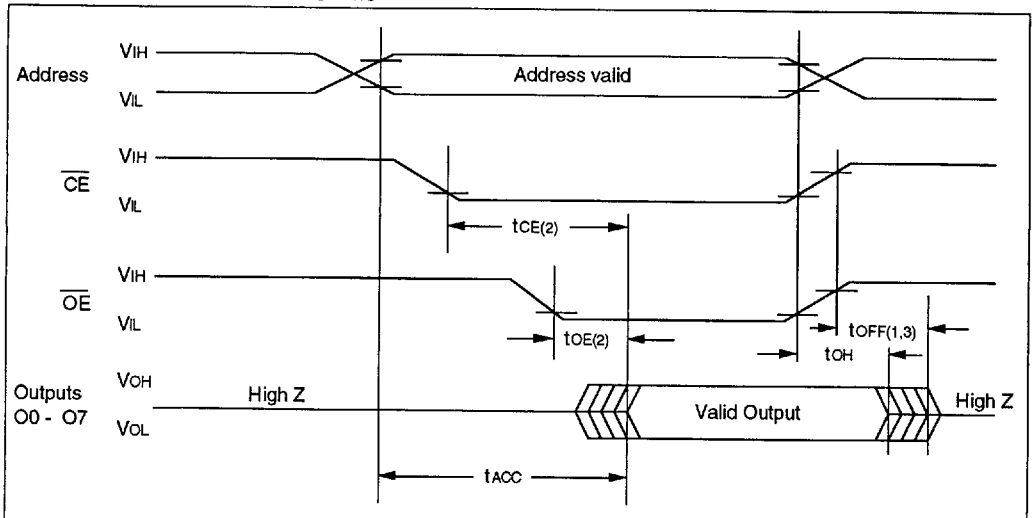
Note 2: V_{CC} must be applied simultaneously or before V_{PP}, and be removed simultaneously or after V_{PP}.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V Output Load: 1 TTL Load + 30 pF Input Rise and Fall Times: 5 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Extended (Automotive): Tamb = -40°C to +125°C										
Parameter	**Part***	**Sym**	**27HC256-55**		**27HC256-70**		**27HC256-90**		**Units**	**Conditions**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	all	t_{ACC}	—	55	—	70	—	90	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	t_{CE1} t_{CE2}	—	55 45	—	70 45	—	90 50	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}	—	30	—	35	—	40	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	25	0	30	0	35	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	t_{OH}	0	—	0	—	0	—	ns	

* Parts: S = Standard Power; L = Low Power

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic"1" Logic"0"	V_{OH} V_{OL}	2.4 —	— 0.45	V V	I_{OH} = -4 mA I_{OL} = 16 mA
V_{CC} Current, program & verify	—	I_{CC}	—	55	mA	
V_{PP} Current, program	—	I_{PP}	—	30	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

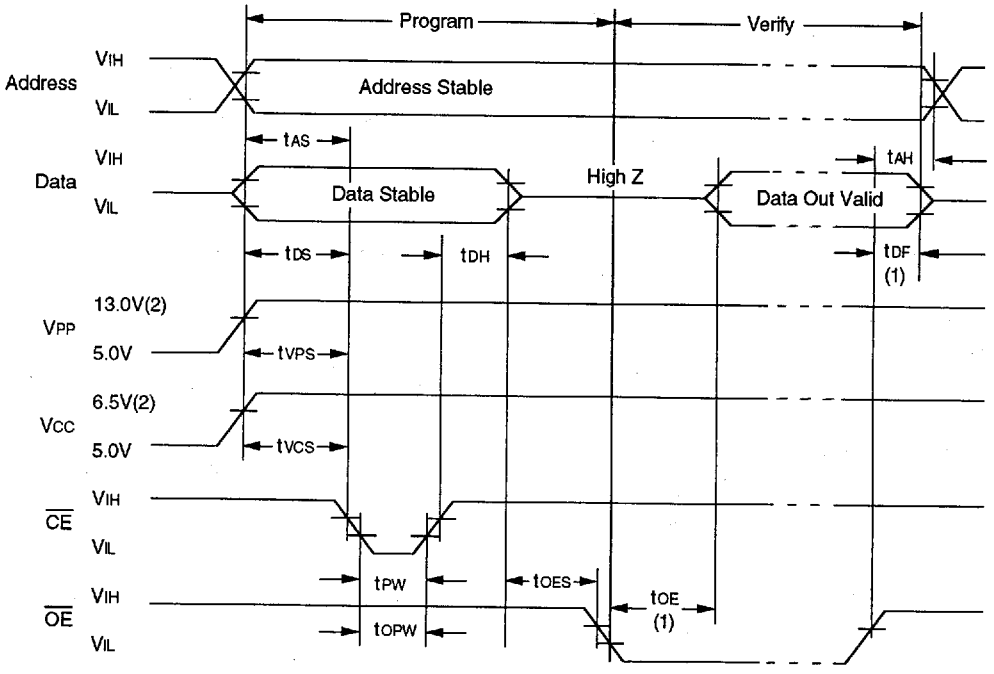
Note 1: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V Ambient Temperature: Tamb=25°C ± 5°C V_{CC}= 6.5V ± 0.25V, V_{PP} =13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

2.0 FUNCTIONAL DESCRIPTION

The 27HC256 has the following functional modes:

- Operation: The 27HC256 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.
- Programming: To receive its permanent data, the 27HC256 must be programmed. Both a program and program/verify procedure are available. It can be programmed with the "Express" algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

2.1 Operations

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table above.

2.2 Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC256's memory data is accessed when

- the chip is enabled by setting the $\overline{CE}$ pin low.
- the data is gated to the output pins by setting the $\overline{OE}$ pin low

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$

2.3 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and a program mode is not defined. When these conditions are met, the supply current will drop from 55 mA to 100 µA on the low power part, and to 35 mA on the standard part.

2.4 Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

2.5 Programming Algorithms

The Express algorithm has been developed to improve programming throughput times in a production environment. Up to 10 pulses of 100 µs each are applied until the byte is verified. No over-programming is required. A flowchart of this algorithm is shown in Figure 2-1.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A14, and the data is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

2.6 Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper VH level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is high, an
d) the $\overline{OE}$ line is low.

2.7 Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

2.8 Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

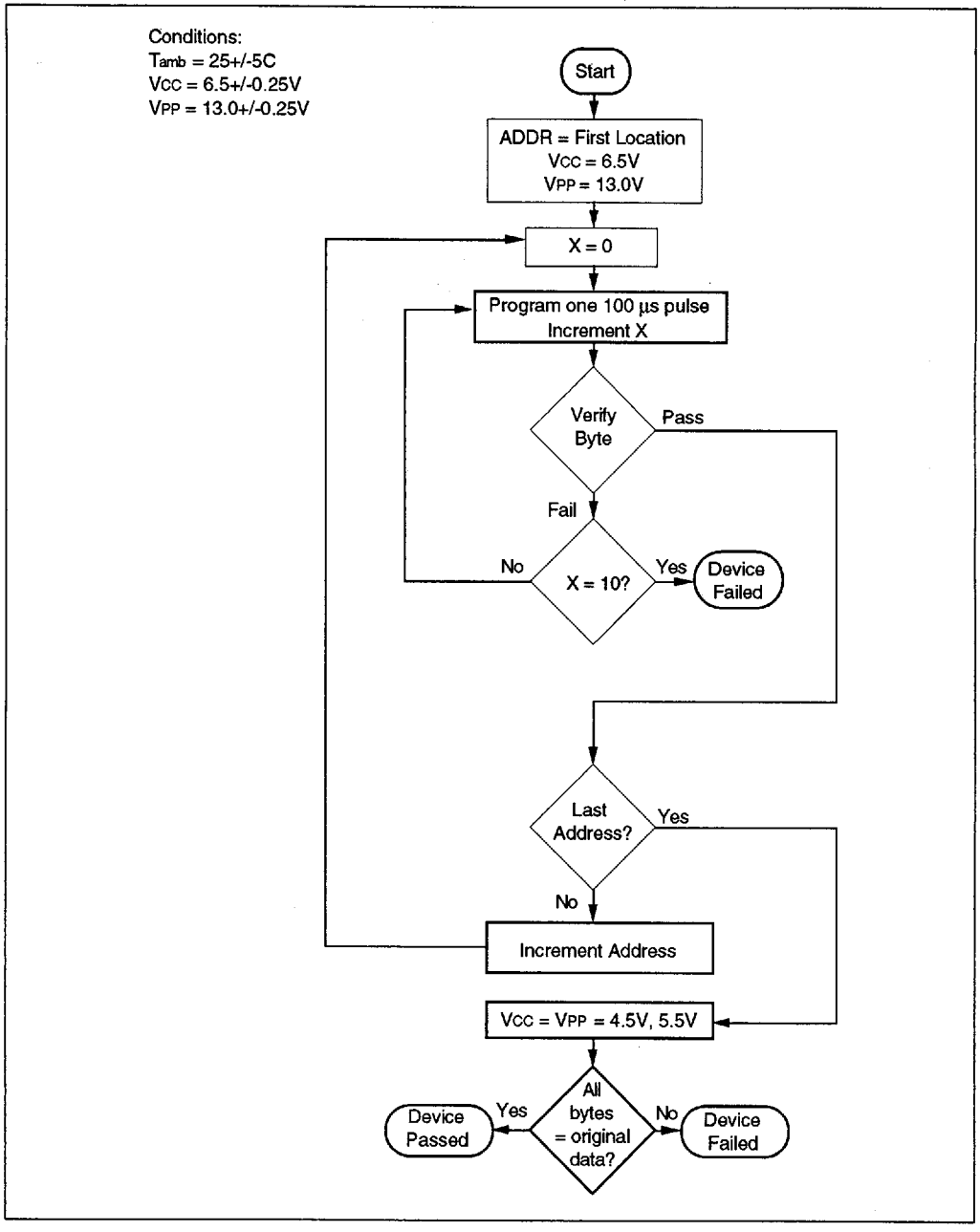
Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	0	0	94

2.9 Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state when exposed to ultraviolet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537 Å with an intensity of 12,000µW/cm^2 at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

FIGURE 2-1: PROGRAMMING EXPRESS ALGORITHM



27HC256 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27HC256 L - 55 I /SO

Package:		J	CERDIP
		K	Ceramic Leadless Chip Carrier
		L	Plastic Leaded Chip Carrier
		P	Plastic DIP
		SO	Plastic SOIC
		VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:		-	0°C to +70°C
		I	–40°C to +85°C
		E	–40°C to +125°C
Access Time:		55	55 ns
		70	70 ns
		90	90 ns (SOIC only)
Power Type:		-	Standard Power
		L	Low Power
Device:	27HC256		256K (32K x 8) High-Speed EPROM