Microchip

Military

27HC641

64K (8K x 8) High Speed CMOS UV Erasable PROM

FEATURES

- Bipolar performance
  - —45 ns maximum access time
- CMOS technology for low power consumption
  - —80 mA active current
- Auto-ID™ aids automated programming
- Two programming algorithms allow improved programming times
  - —Fast programming
  - —Express programming
- Organized 8K x 8: bipolar PROM pinouts
  - —24-pin Dual In-line Package (DIP)
  - —28-pin Leadless Chip Carrier (LCC)
- Extended temperature range:
  - —Military (B): -55°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27HC641 is a CMOS 64K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). An advanced CMOS design allows bipolar speed with a significant reduction in power over bipolar PROMs. The 27HC641 is configured in a standard 64K bipolar PROM pinout, which allows an easy upgrade for PROM sockets. This very high speed device allows digital signal processors (DSP) or other sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

DESC SMD Approved

The 27HC641 is approved and on the released DESC SMD 5962-87515 in Cerdip and leadless chip carrier packages.

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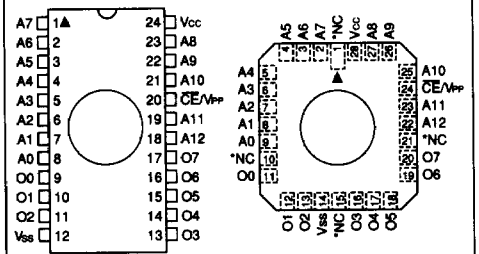
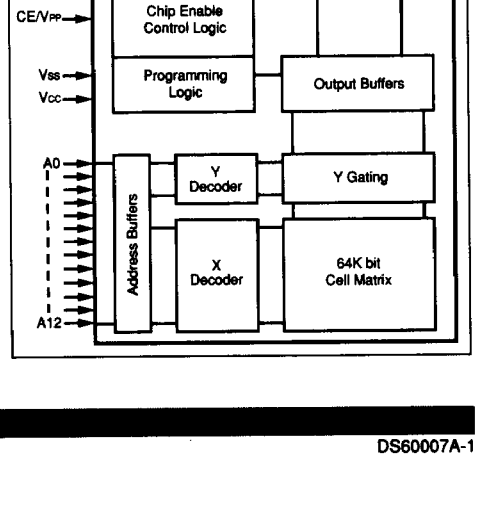
PIN CONFIGURATION
Top View



▲ Pin 1 indicator on LCC and Cerdip on top of package
* NC (don't connect on LCC package)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{CC} and input voltages w.r.t. V_{SS} .....-0.6 V to + 6.25 V
$\overline{CE}/V_{PP}$ voltage w.r.t. V_{SS} during programming .....-0.6 V to + 14 V
Voltage on A9 w.r.t. V_{SS} .....-0.6 V to +13.5 V
Output voltage w.r.t. V_{SS} .....-0.6 V to V_{CC} + 0.6 V
Storage temperature .....-65°C to 150°C
Ambient temp with power applied .....-55°C to 125°C
ESD protection on all pins .....>2 KV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}/V_{PP}$	Chip Enable/V_{PP} Pin
O0 - O7	Data Output
V_{CC}	+5 V
V_{SS}	Ground
NC	No Connection

READ OPERATION
DC Characteristics

V_{CC} = +5 V ±10%
Military (B): Tamb= -55°C to +125°C

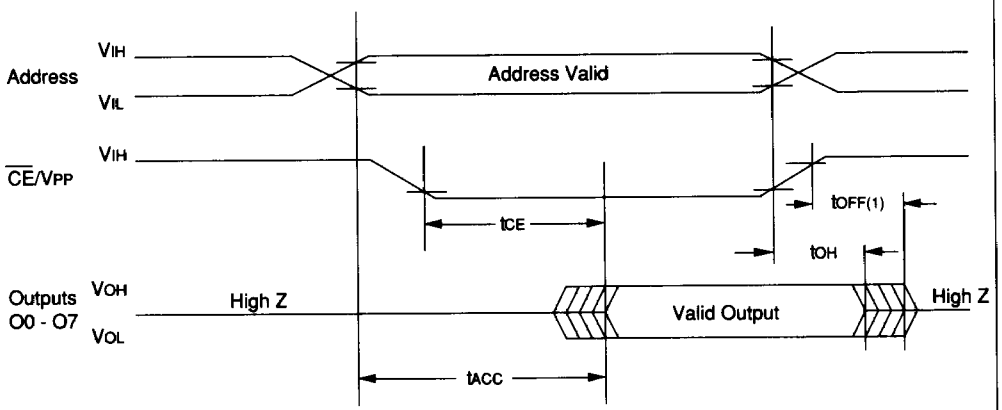
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN}= 0 V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 4 mA I_{OL} = 16 mA
Leakage		I_{LO}	-10	10	µA	V_{OUT}= 0 V to V_{CC}
Input Capacitance		C_{IN}		6	pF	V_{IN} = 0 V; Tamb = 25°C; f = 1 MHz
Output Capacitance	TTL input	C_{OUT}		12	pF	V_{OUT}= 0 V;Tamb = 25°C; f = 1 MHz
Power Suppy Current, Active		I_{CC}		90	mA	V_{CC} = 5.5 V; $\overline{CE}/V_{PP}$ = V_{IL} f = 2 MHz; Iout = 0 mA; V_{IL}= -0.1 V to 0.8 V; V_{IH}= 2.0 V to V_{CC}
Power Supply Current, Standby		$I_{CC(S)}$		40	mA	

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0 V and V_{IL} = 0.0 V; V_{OH} = V_{OL} = 1.5 V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Military (B): Tamb = -55°C to +125°C

Parameter	Sym	27HC641-45		27HC641-55		27HC641-70		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		45		55		70	ns	
$\overline{CE}$/VPP to Output Delay	tCE1 tCE2		30 25		30 30		30 35	ns	
$\overline{CE}$/VPP to O/P High Impedance	tOFF	0	25	0	25	0	25	ns	
Output Hold from Address or $\overline{CE}$/VPP, whichever occurs first	tOH	0		0		0		ns	

READ WAVEFORMS



Note: (1) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25°C ±5°C
For $\overline{CE}$/V_{PP} and V_{CC} Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC} +1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = V_{IL} or V_{IH}
Output Voltages during verification	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 4 mA I_{OL} = 16 mA
V_{CC} Current, program & verify		I_{CC}		35	mA	
V_{PP} Current, program		I_{PP}		30	mA	
A9 Product Identification		V_H	11.5	12.5	V	

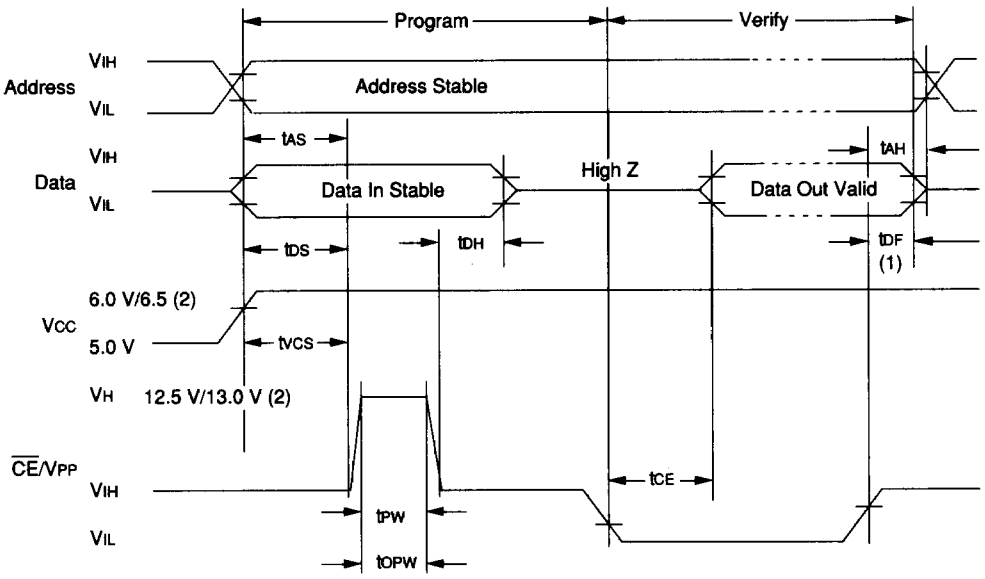
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25°C ±5°C
For $\overline{CE}$/V_{PP} and V_{CC} Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (3)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	0.95	1.05	ms	1 ms typical
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
Overprogram Pulse Width (2)	t_{OPW}	2.85	78.75	ms	
$\overline{CE}$ to Output Delay	t_{CE}		70	ns	

Notes: (1) For Express programming algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF is a characteristics of the device but must be accomodated by the programmer
(2) VCC = 6.0 V ±0.25 V, CE/VPP = VH=12.5 V ±0.5 V for fast programming algorithm
VCC = 6.5 V ± 0.25 V, CE/VPP = VH = 13.0 V ± 0.5 V for Express programmimg algorithm

MODES

Operating Modes	CE/VPP	A9	O0 - O7
Read/Program Verify	VIL	X	DOUT
Program	VH	X	DIN
Standby/Program Inhibit	VIH	X	High Z
Identify	VIL	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the CE/VPP pin is low to power-up (enable) the chip

For Read operations on the low powered version, if the addresses are stable, the address access time (tACC) is equal to the delay from CE/VPP to output (tCE). A faster CE/VPP access time (tCE) is available on the standard part to provide the additional time for decoding for the CE/VPP signal.

Standby Mode

The standby mode is defined when the $\overline{CE}$/VPP pin is high (VIH).

When this condition is met, the supply current will drop from 80 mA to 100 mA on the low power part and to 40 mA on the standard part.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1s" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 µW/cm² for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. The fast programming algorithm is recommended for windowed product only. A flowchart of the fast programming algorithm is shown in Figure 1.

The Express programming algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten (10) 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the Express programming algorithm is shown in Figure 2.

Express is the preferred programming algorithm.

The $\overline{CE}$/VPP is a multifunction pin that controls the programming of the 27HC641.

Programming takes place when:

a) VCC is brought to proper voltage,

b) the $\overline{CE}$ /VPP pin is pulsed at the proper VH level.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A12 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a high voltage pulse (VH) on the $\overline{CE}$/VPP line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,

b) the $\overline{CE}$/VPP line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$/VPP needs to be under separate control to each device. By pulsing the $\overline{CE}$/VPP line to a VH on a particular device, that device will be programmed; all other devices with $\overline{CE}$/VPP held high (VIH) will not be programmed with the data, although address and data will be available on their input pins (i.e., when a level (VIH) is present on $\overline{CE}$/VPP) and the device is inhibited from programming.

Identity Mode

In this mode specific data is outputted which identifies the device type and the manufacturer as Microchip Technology Inc. This mode is entered when Pin A9 is taken to VH (11.5 V - 12.5 V).

The $\overline{CE}$/VPP line must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type	VIH	0	0	0	1	0	0	0	0	10

*Code subject to change.

FIGURE 1 - PROGRAMMING FAST ALGORITHM

(Recommended for windowed product only)

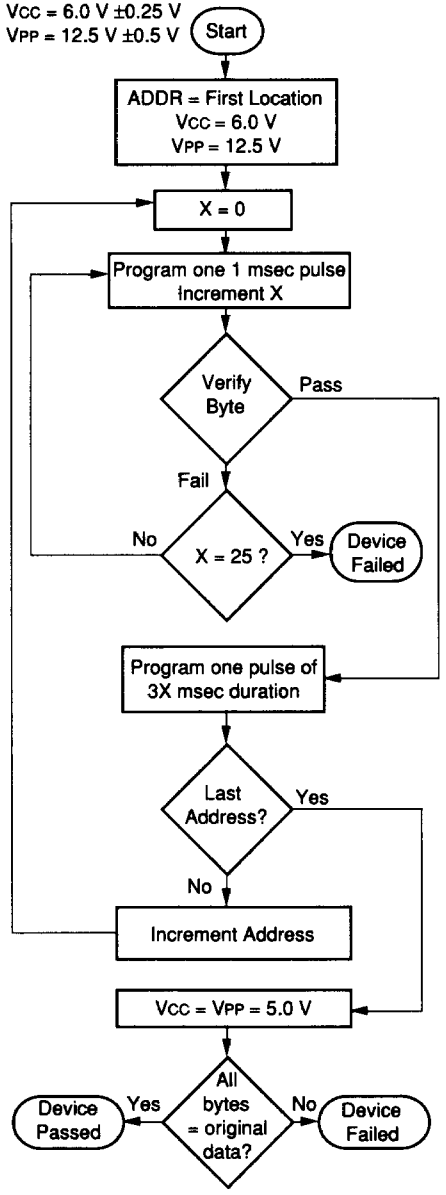
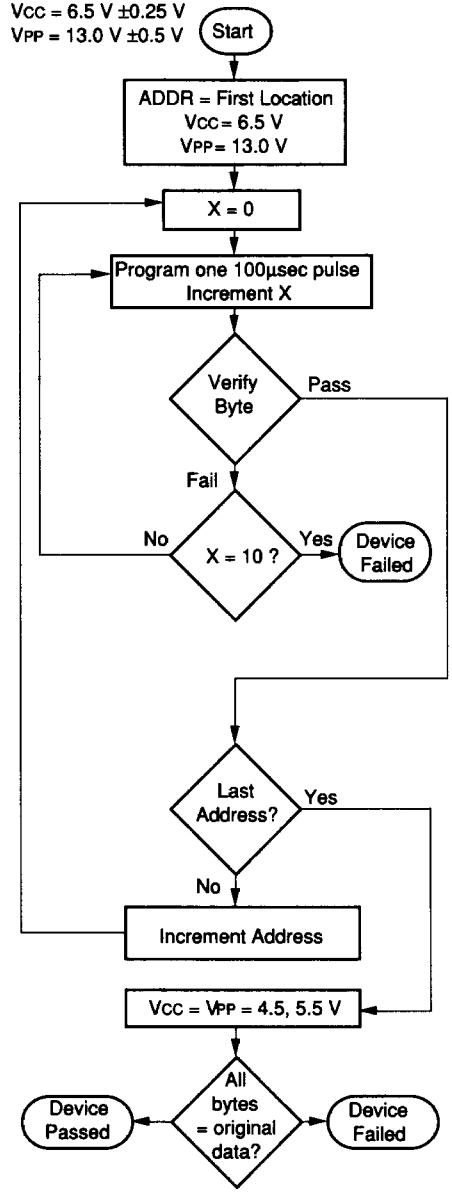


FIGURE 2 - PROGRAMMING EXPRESS ALGORITHM



ORDERING INFORMATION

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers.

PART NUMBERS

27HC641 - 45 B / XA

Lead Finish		A	Solder Dip
		B	Matte Tin
Package:		X	Cerdip DIP
		U	Ceramic Leadless Chip Carrier
Temperature Range:		B	-55°C to +125°C
Access Time:		45	45 nsec
		55	55 nsec
		70	70 nsec
Device	27HC641		64K (8K x 8) High Speed CMOS EPROM

Screening per MIL-STD-883C