8085A

8-Bit Microprocessor

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

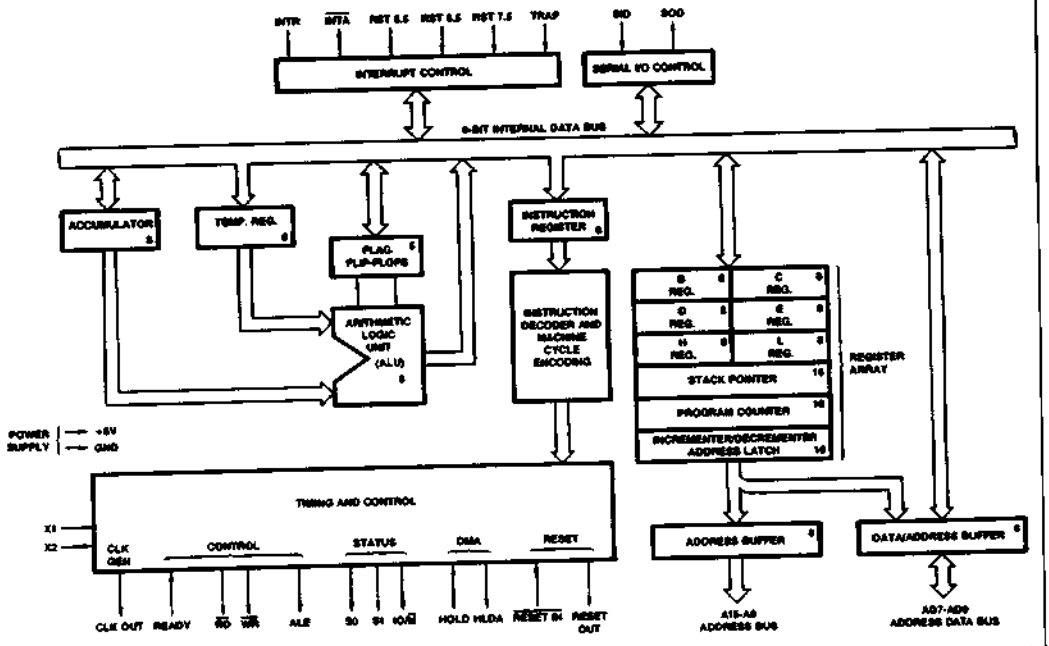
- SMD/DESC qualified
- 3- and 5-MHz selections available
- On-chip system controller; advanced cycle status information available for large system control
- Four vectored interrupts (one is non-maskable)
- On-chip clock generator (with external crystal, LC or R/C network)
- Serial-in/serial-out port
- Decimal, binary, and double-precision arithmetic
- Direct addressing capability to 64K bytes of memory
- 1.3 μs instruction cycle (8085A)
- 0.8 μs instruction cycle (8085A-2)
- 100% software-compatible with 8080A
- Single +5 V power supply

GENERAL DESCRIPTION

The 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor. Specifically, the 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A. The 8085A-2 is a faster version of the 8085A. The 8085A is a 3-MHz CPU with 10% supply tolerances and lower power consumption.

The 8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155H/56H memory products allow a direct interface with 8085A. The 8085A components, including various timing-compatible support chips, allow system speed optimization.

BLOCK DIAGRAM



BD003790

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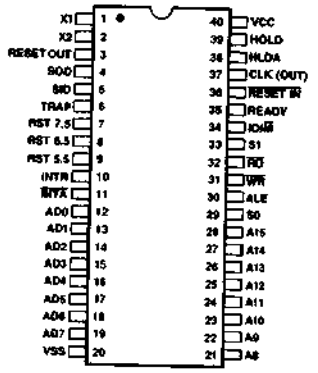
CONNECTION DIAGRAM
Top View
DIPs



CD005564

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

79010 — 01 — Q — X

- **d. LEAD FINISH**
  X = Any Lead Finish Acceptable
- **c. CASE OUTLINE**
  Q = 40-Pin Ceramic DIP (CD 040)
- **b. MILITARY DEVICE TYPE**
  01 = 3 MHz (8085A)
- **a. MILITARY DRAWING PART NUMBER**
  79010
  8-Bit Microprocessor

Valid Combinations	
7901001	QX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

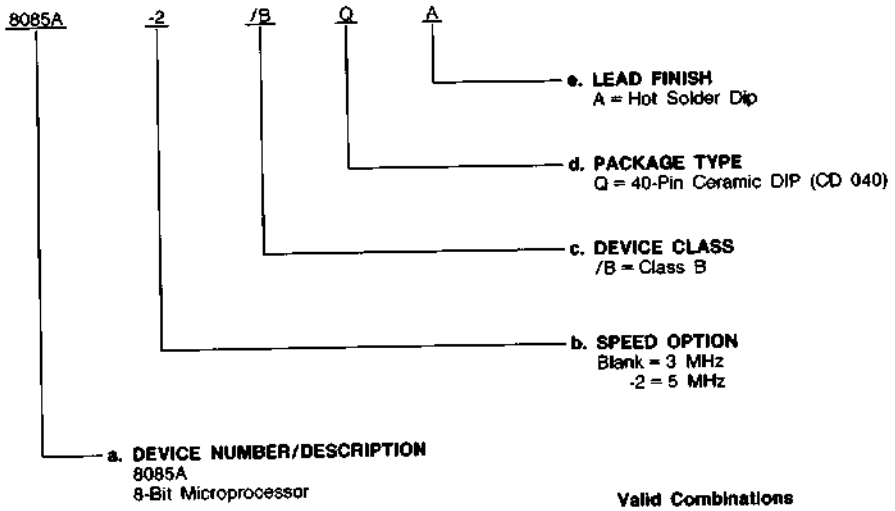
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8085A	/BQA
8085A-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
With Respect to Ground ..... −0.5 to +7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%
Supply Current (I_{CC}) ..... 200 mA

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ±10%	−0.5*	+0.8	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ±10%	2.2	V_{CC} +0.5*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = 5 V ±10%		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA, V_{CC} = 5 V ±10%	2.4		V
I_{CC}	Power Supply Current	V_{CC} = 5 V (NOTE 1)		200	mA
I_{IL1}	Input Leakage, Except Pin 1	V_{CC} = 5.5 V, V_{IN} = V_{CC} to 0 V		±10	μA
I_{IL2}	Input Leakage, Pin 1	V_{CC} = 5.5 V, V_{IN} = V_{CC} to 0 V		±70	μA
I_{LO}	Output Leakage	V_{CC} = 5.5 V, V_{OUT} = V_{CC} to .45 V		±10	μA
V_{ILR}	Input LOW Level, RESET	V_{CC} = 5 V ±10%	−0.5*	+0.8	V
V_{IHR}	Input HIGH Level, RESET	V_{CC} = 5 V ±10%	2.4	V_{CC} +0.5*	V
V_{HY}	Hysteresis, RESET	V_{CC} = 5 V ±10%	0.25		V

*Guaranteed by design; not tested.

Notes: 1. I_{CC} is measured while running a functional pattern with no loads applied.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	8085A (Note 2)		8085A-2 (Note 2)		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK LOW Time (Standard CLK Loading)	80		40		ns
t_2	CLK HIGH Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	20	120	20	100	ns
t_{XKF}	X_1 Rising to CLK Falling	20	150	20	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control (Note 1)	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE (Note 1)	90		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	70		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control LOW ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE LOW During CLK High	100		50		ns
t_{LDR}	ALE to Valid Data During Read		460		270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$ (Note 6)	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

Notes:
1. $A_8 - A_{15}$ address Specs apply to IO/$\overline{M}$, S_0, and S_1, except $A_8 - A_{15}$ are undefined during $T_4 - T_6$ of OF cycle; whereas, IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2); C_L = 100 pF, V_{CC} = 5 V ±10%, V_{IL} = .45 V, V_{IH} = 2.4 V; V_{OL} = .8 V, V_{OH} = 2.0 V.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. To calculate timing specifications at other values of t_{CYC} use Table 3 on page 3-191 of the MOS Microprocessors and Peripherals Data Book (Order #09067A)
6. Data hold time is guaranteed under all loading conditions.

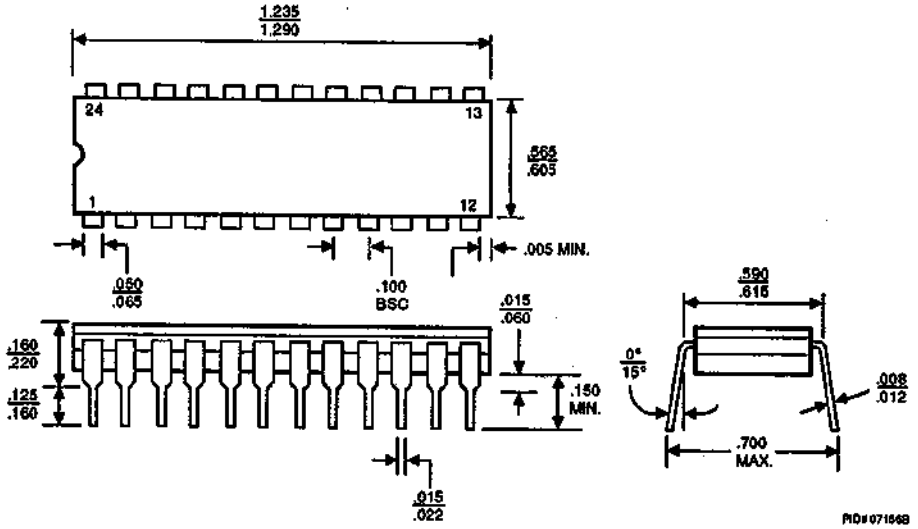
CHAPTER 6
General Information

T-90-20

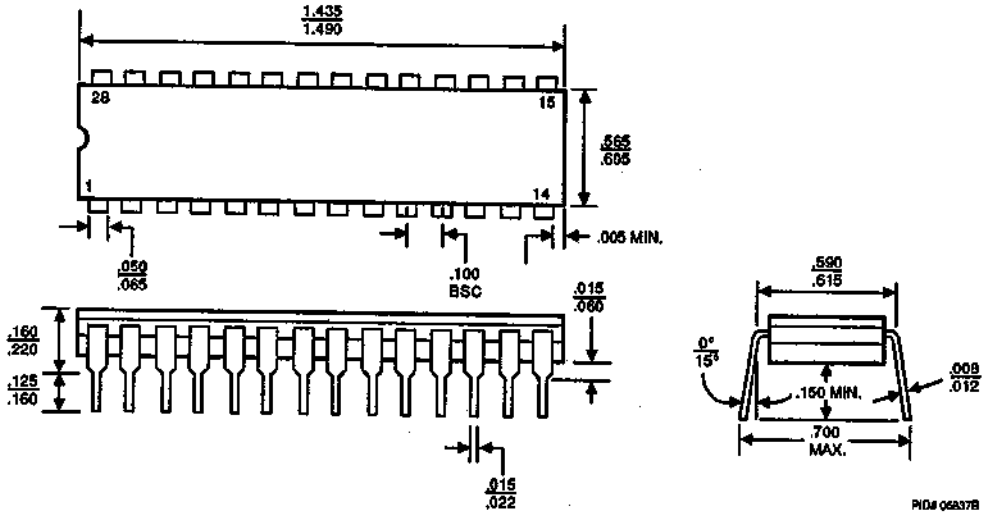
PACKAGE OUTLINES*

Ceramic DIPs (CD)

CD 024



CD 028



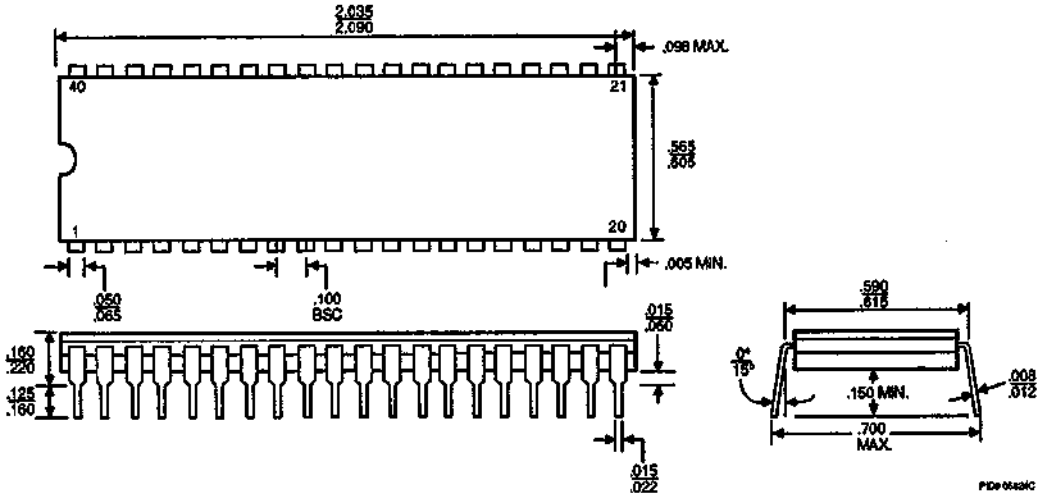
* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

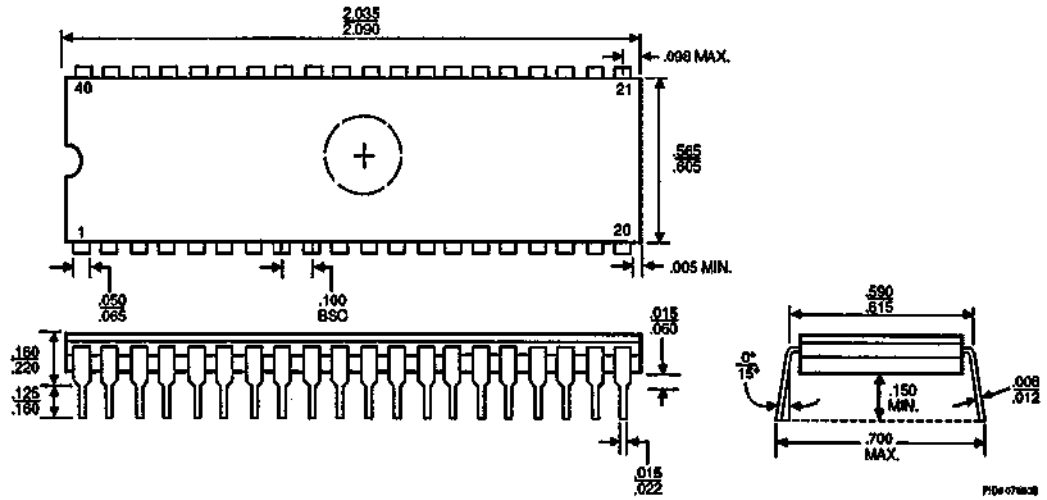
PACKAGE OUTLINES (Continued)

Ceramic DIPs (CD) (Continued)

CD 040



CDV040



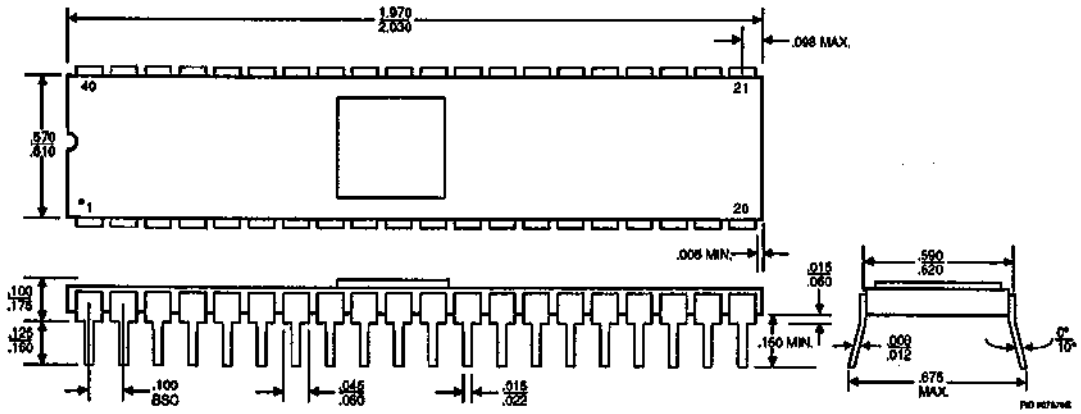
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

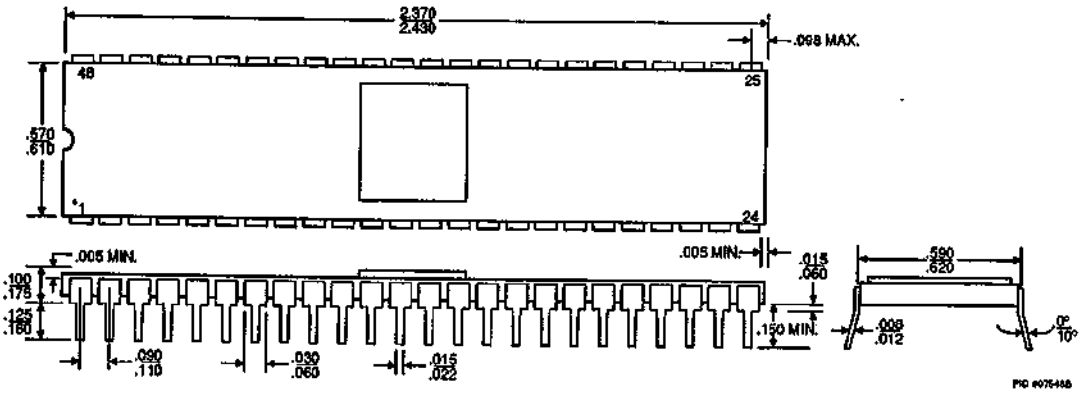
T-90-20

Ceramic Sidebrazed DIPs (SD)

SD 040



SD 048

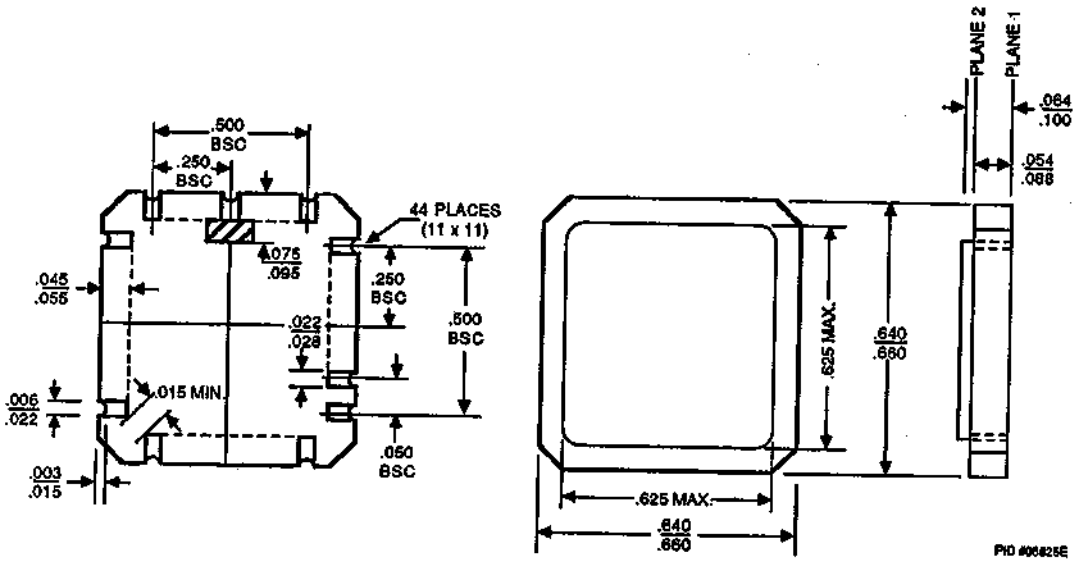


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

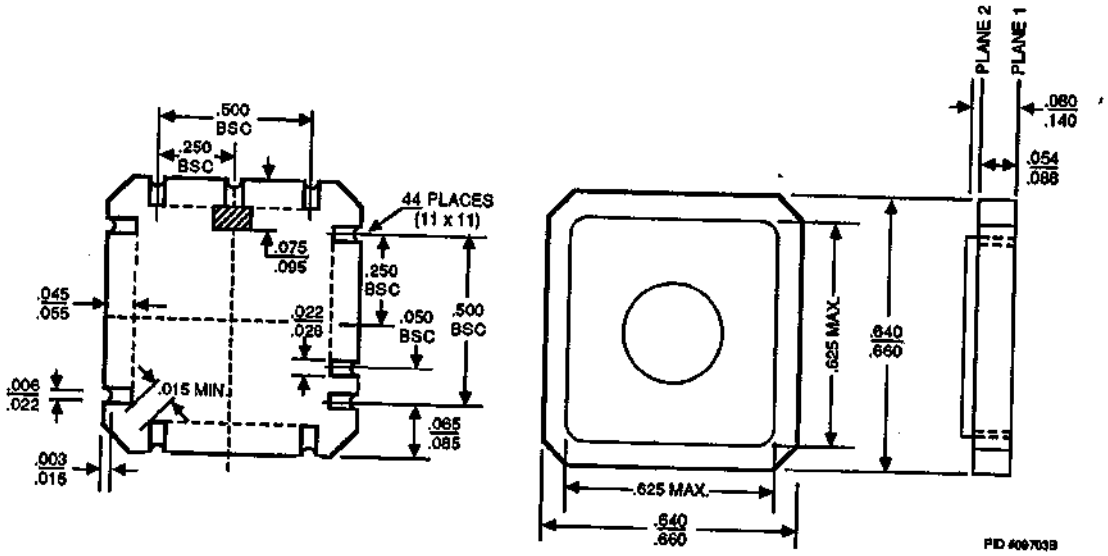
PACKAGE OUTLINES (Continued)

Ceramic Leadless Chip Carriers (CL/CLV)

CL 044



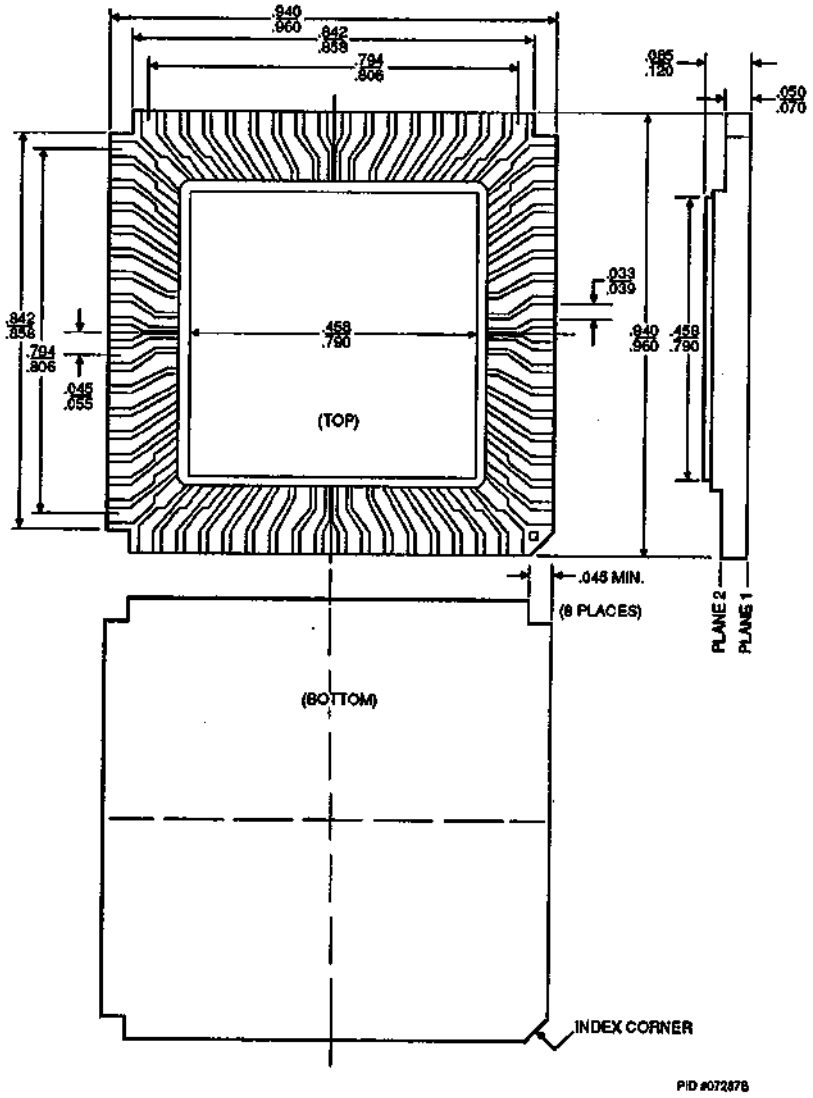
CLV044



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

68-Pin Square Leadless Chip Carrier (CA2)
CA2068

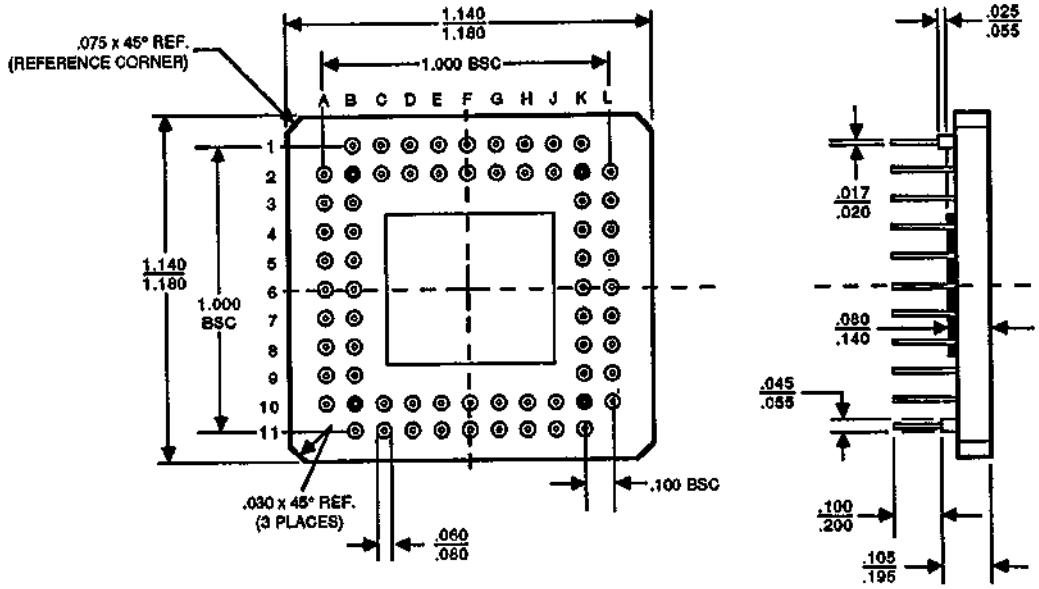


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

Ceramic Pin-Grid-Array Package (CG/CGX)
CGX068

BOTTOM VIEW



PID # 07547B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.