4003

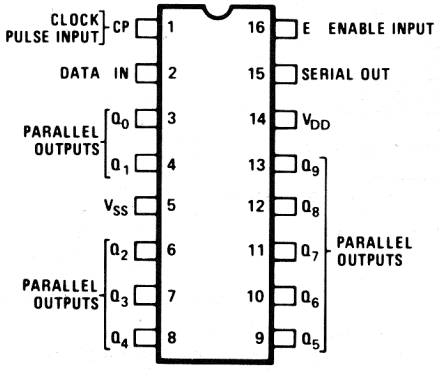
10 BIT SHIFT REGISTER/OUTPUT EXPANDER

- **10 Bit Serial-In/Parallel Out**
- **Serial-Out Capability for Additional I/O Expansion**
- **16 Pin Dual-In-Line Package**
- **Easy Expansion of I/O Output Capability**
- **Enable Output Control**
- **Standard Operating Temperature Range of 0° to 70°C**

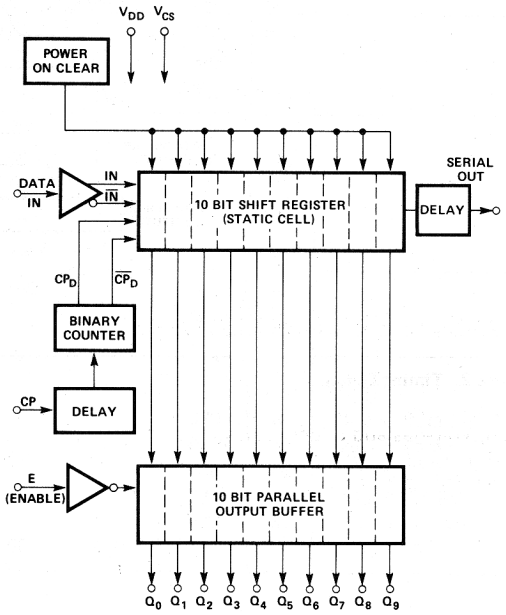
The 4003 is a 10 bit serial-in, parallel-out, serial-out shift register with enable logic. The 4003 is used to expand the number of ROM and RAM I/O ports to communicate with peripheral devices such as keyboards, printers, displays, readers, teletypewriters, etc.

The 4003 is a single phase static shift register; however, the clock pulse (CP) maximum width is limited to 10 msec. Data-in and CP can be simultaneous. To avoid race conditions, CP is internally delayed.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1	CP	The clock pulse input. A "0" (V_{SS}) to "1" (V_{DD}) transition will shift data in.
2	DATA IN	Serial data input line.
3	O_0	Parallel data output lines, when enabled. Each pin may be made TTL compatible with a 5.6K pull-down resistor to V_{DD}.
4	O_1	
6	O_2	
7	O_3	
8	O_4	
9	O_5	
10	O_6	
11	O_7	
12	O_8	
13	O_9	
5	V_{SS}	Most positive supply voltage.
14	V_{DD}	Main supply voltage value must be V_{SS} - 15.0V ± 5% (-10v for TTL operation)
15	Serial out	Serial data output.
16	E	Enable, when E = "1" (V_{DD}) the output lines contain valid data. When E = "0" (V_{SS}) the output lines are at V_{SS}.

Functional Description

The 4003 is designed to be typically appended to an MCS-40 I/O port. This can be the I/O port of a 4001, 4002, 4289, 4308, or a 4265. One I/O line is assigned to be the Enable (E), another the Clock (CP), and still another the Serial Data-Input. For example, to access the 4003 a subroutine of sequential outputs consisting of Data, clock pulse on, Enable – followed by an output of clock pulse off and Enable, will serially load the 4003.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = 1 -- V_{DD}), the shift register contents are read out; when not enabled (E = 0 -- V_{SS}), the parallel-out lines are at Logic "0" (V_{SS}). The serial-out line is not affected by the enable logic to allow longer word cascading.

Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register (outputs = 0 or V_{SS}) between the application of the supply voltage and the first CP signal.

The 4003 output buffers are useful for multiple key depression rejection when a 4003 is used in conjunction with a keyboard. In this mode if up to three output lines are connected together, the state of the output is high (Logic "0" or V_{SS}) if at least one line is high.

Another typical application of the 4003 is for Keyboard or Display Scanning where a single bit of Logic "1" is shifted through the 4003 and is used to activate the various digits, keyboard rows, etc.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec, $t_{\phi D2}$ = 150 nsec, unless otherwise specified.

Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}), Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}).

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		5.0	8.5	mA	t_{WL} = t_{WH} = 8μsec; T_A = 25°C
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3		
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
I_{OL}	Parallel Out Pins Sinking Current, "1" Level	0.6	1.0		mA	V_{OUT} = 0V. For TTL compatibility a 5.6KΩ (±10%) resistor between output and V_{DD} should be added.[2]
I_{OL}	Serial Out Sinking Current, "1" Level	1.0	2.0		mA	V_{OUT} = 0V
V_{OL}	Output Low Voltage	V_{SS}-11	V_{SS}-7.5	V_{SS}-6.5	V	I_{OL} = 10μA
R_{OH}	Parallel-Out Pins Output Resistance "0" Level		400	750	Ω	V_{OUT} = -0.5V
R_{OH}	Serial Out Output Resistance "0" Level		650	1200	Ω	V_{OUT} = -0.5V

Notes: 1. Typical values are to T_A = 25°C and Nominal Supply Voltages.

2. For TTL compatibility on the I/O lines the supply voltages should be V_{DD} = -10V ±5%; V_{SS} = +5V ±5%.

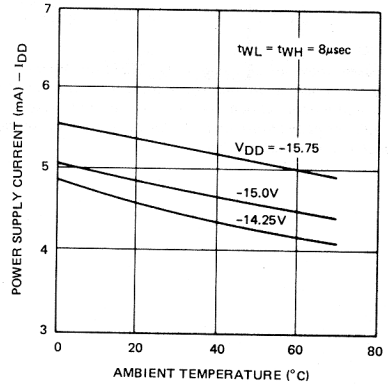
CAPACITANCE

f = 1 MHz; V_{IN} = 0V; T_A = 25°C; Unmeasured Pins Grounded.

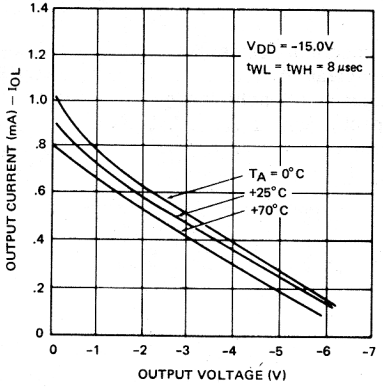
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

T_A = 0°C to +70°C; V_{DD} = -15 ±5%, V_{SS} = GND

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{WL}	CP Low Width	6		10,000	μsec	
t_{WH}[1]	CP High Width	6			μsec	
t_{CD}	Clock-On to Data-Off Time	3			μsec	
t_{Dd}[2]	CP to Data Set Delay			250	nsec	
t_{d1}	CP to Data Out Delay	250		1750	nsec	
t_{d2}	Enable to Data Out Delay			350	nsec	C_{OUT} = 20pF
t_{d3}	CP to Serial Out Delay	200		1250	nsec	C_{OUT} = 20pF
t_{d4}	Enable to Data Out Delay			1.0	μsec	C_{OUT} = 20pF

Notes: 1. t_{WH} can be any time greater than 6μsec.
2. Data can occur prior to CP.

Timing Diagram