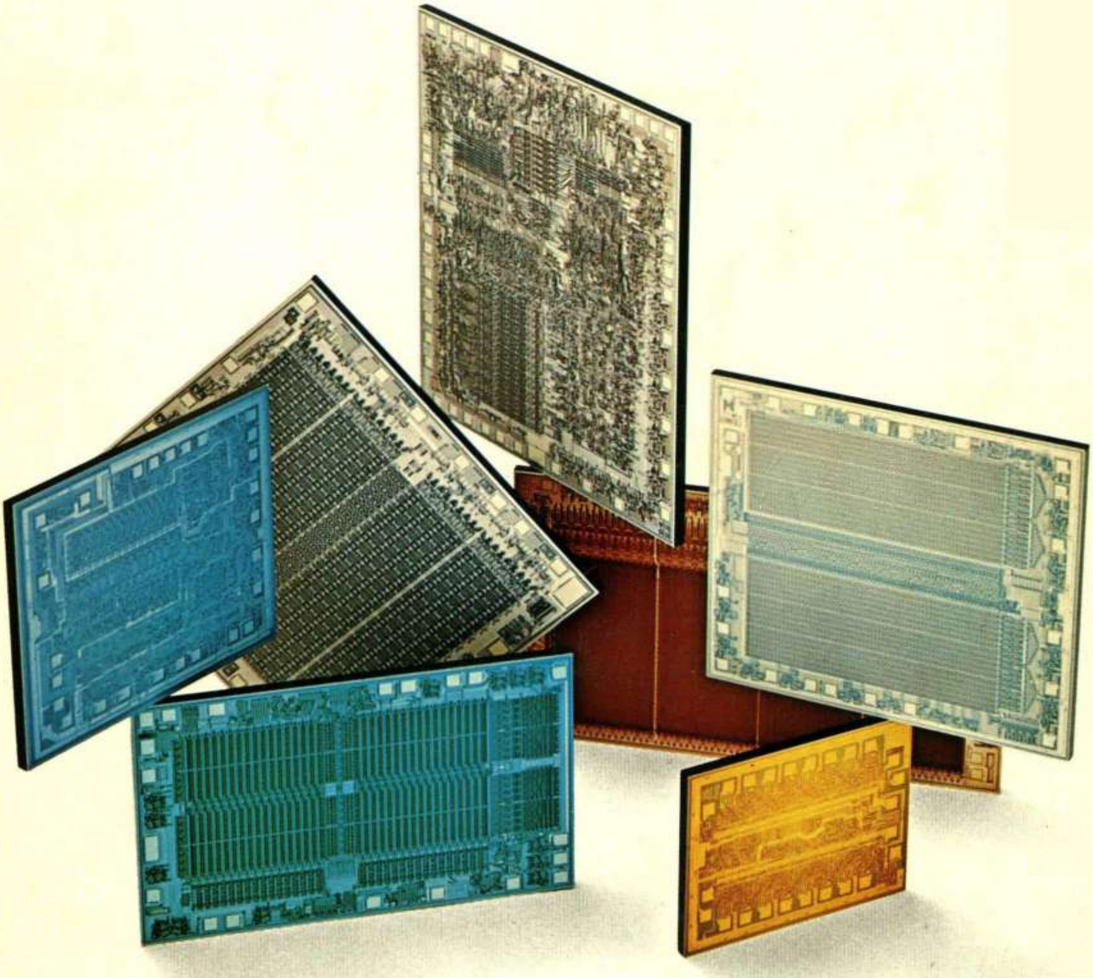
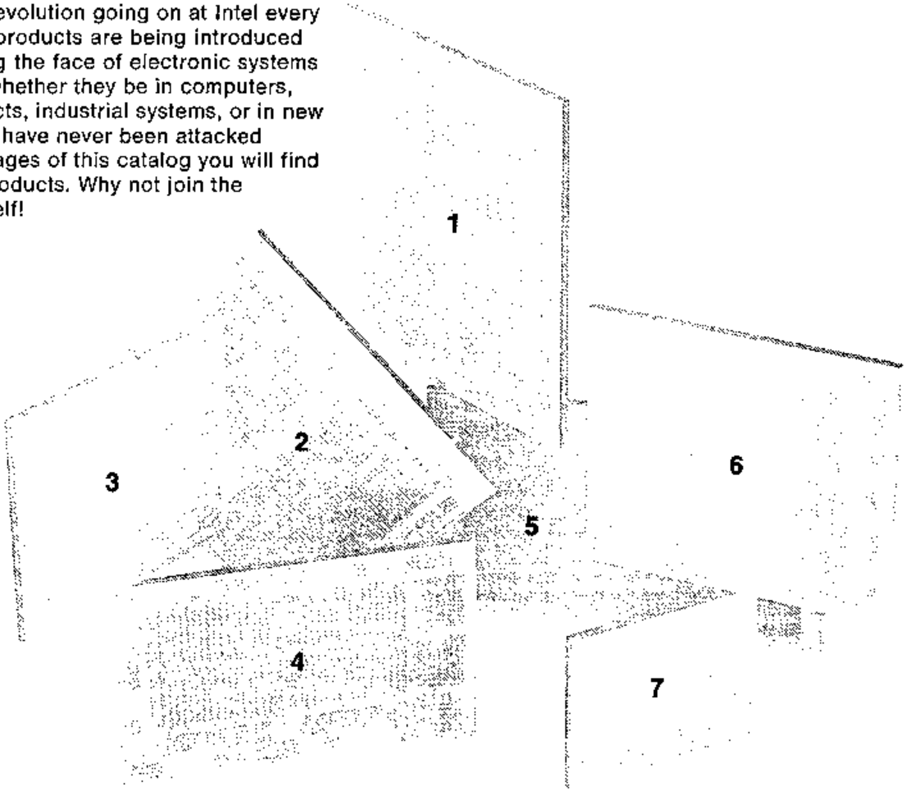
intel DATA CATALOG 1975



THE QUIET REVOLUTION AT INTEL

There's a quiet revolution going on at Intel every day, where new products are being introduced that are changing the face of electronic systems the world over, whether they be in computers, consumer products, industrial systems, or in new applications that have never been attacked before. On the pages of this catalog you will find some of these products. Why not join the revolution yourself!



On the cover:

Pictured on the cover of this 1975 edition of the Intel Data Catalog are seven recently introduced Intel products. Each represents the state of the semiconductor art in its area of application.

1. **Intel® 8080.** Intel Microcomputers have revolutionized the design of logic systems. This 8-bit CPU is Intel's third generation Microcomputer. It has a repertoire of 78 instructions and an instruction cycle time of 2 μsec. The 8080 is manufactured with N-channel silicon-gate technology. Further information on the 8080 may be found on page 6-25.
2. **Intel® 5101.** This 1024 bit CMOS RAM dissipates only 15 μw per bit when active and only 0.28 nw per bit when in power-down standby. It is organized as 256 words by 4 bits and has an access time of 650 nsec. Four versions are available now and extended temperature range options for military applications will be offered beginning in March 1975. Specifications on the 5101 begin on page 2-115.
3. **Intel® 3002.** This Schottky Bipolar 2 bit Central Processing Element contains all of the Central Processing Unit circuits of a 2 bit wide slice of a digital computer. An array of 3002's used in conjunction with other members of the Bipolar Microcomputer Set allows the construction of extremely powerful Microprogrammed High Speed Central Processors. Information on the Intel Bipolar Microcomputer Set begins on page 6-53.
4. **Intel® 2107B.** The 2107B 4K N-channel RAM is expected to be the industry's workhorse memory. The 2107B accesses in 200 ns, cycles in 400 ns and is low in cost due to its single transistor cell design and small chip size. Specifications begin on page 2-81.
5. **Intel® 2416.** This unique new semiconductor memory is a 16,384 bit CCD Memory, organized as 64 registers of 256 bits each. Each register is accessed through a decoding network allowing an average latency time of 100 μs and data transfer rates of up to 64 megabits per second. Information on the 2416 is on page 4-19.
6. **Intel® 3604.** This High Speed 4096 bit PROM is electrically programmed by selectively blowing a unique polysilicon fuse through the application of the appropriate programming pulses. The 3604 is one product of a 28 member family of High Speed Schottky Bipolar 1K, 2K, and 4K PROMS and ROMS. Specifications are on page 3-36.
7. **Intel® 8212.** This Schottky Bipolar circuit is an input/output port consisting of an 8-bit latch with three-state output buffers along with control and device selection logic. Because of their multimode capability 8212's can be used to implement latches, buffers, multiplexers, bi-directional bus drivers, or interrupting input/output ports. Information on the 8212 is on page 6-63.

intel® data catalog

Intel Corporation 3065 Bowers Ave. Santa Clara, CA 95051
Tel: 408/246-7501, TWX: 910-338-0026, Telex: 34-6372

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MEMORY SYSTEMS

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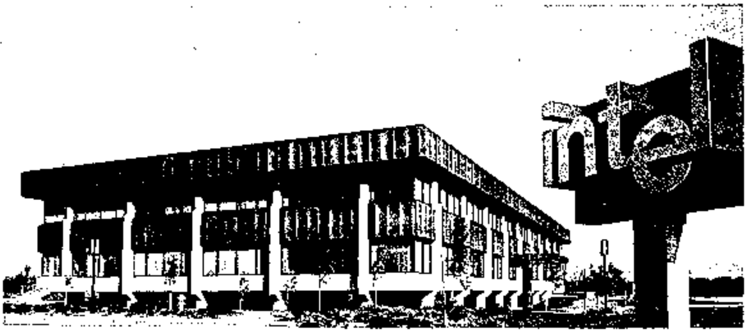
CIRCUITS

TIMEKEEPING CIRCUITS

intel® corporation

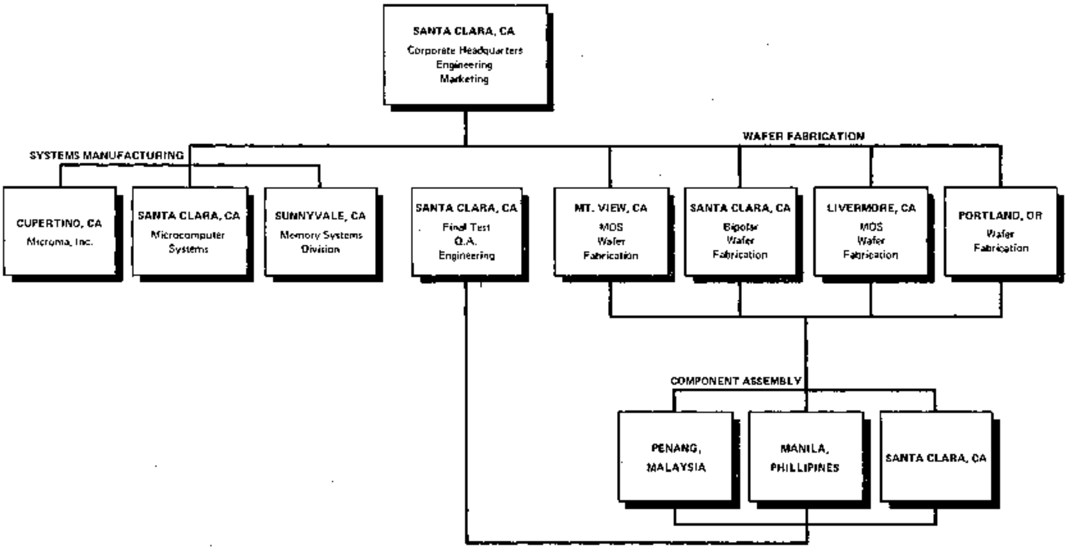
Housed today in approximately 500,000 square feet of facilities, Intel is the world's leading supplier of semiconductor memory components. Process technologies used in production by Intel are p-channel, n-channel, and complementary silicon gate MOS and SCHOTTKY Bipolar. This breadth of process technology allows Intel to make the optimum cost-performance trade off for a particular memory application.



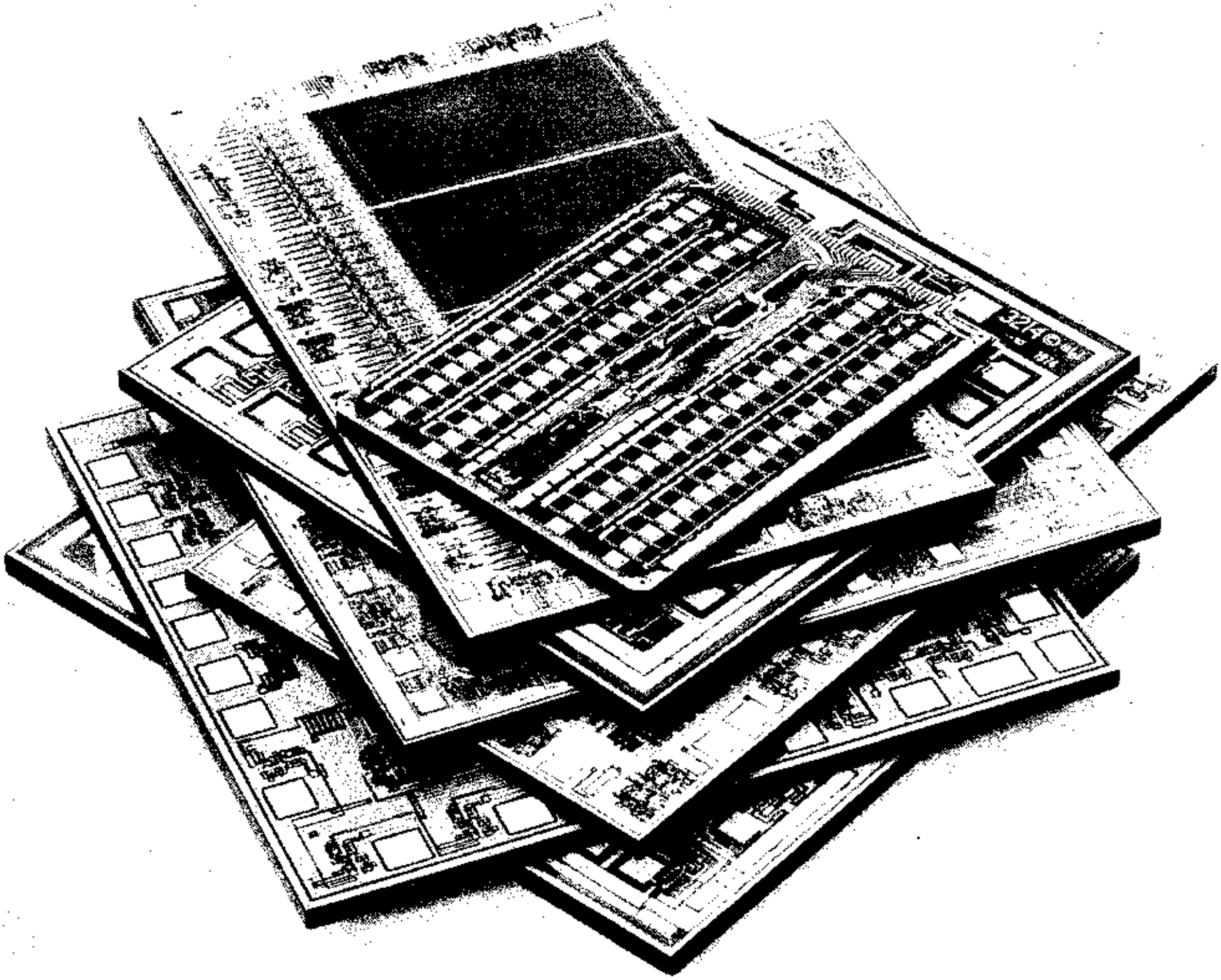
Santa Clara Corporate Headquarters

intel facilities

World-wide facilities: Intel manufacturing facilities are located world-wide. Santa Clara, California serves as corporate headquarters. Wafer fabrication plants are located in Mountain View, Santa Clara, and Livermore, California and Portland, Oregon. Assembly operations are performed in Penang, Malaysia; Manila, Philippines; and Santa Clara, California. Marketing offices are located throughout the U.S., in Europe and Japan. New facilities for our Memory Systems Division, Microma and Micro Computer Systems give Intel a total of approximately 500,00 square feet.



INDEX AND GENERAL INFORMATION



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FUNCTIONAL INDEX

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INTEL MEMORY SYSTEMS

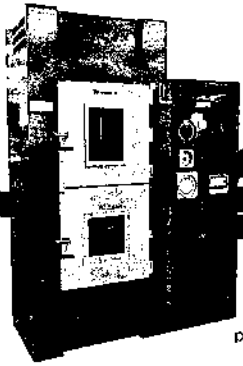
STANDARD PRODUCT PROCESSING AND 100% SCREENING —

Optical inspection of sorted dice per MIL-STD-883 Method 2010.1B to insure that all devices are free from internal defects which could lead to failure in normal applications. (Monitored by QA)

Die Attach
(Monitored by QA)

Lead Bonding (Monitored by QA per MIL-STD-883 Method 2011 Test Condition D.)

Precap Visual Inspection per MIL-STD-883 Method 2010.1B to insure that after assembly all devices are free from defects which could lead to failure in normal applications. (Each lot must pass a QA acceptance)



Temperature Cycling per MIL-STD-883 Method 1010 Test Condition C (10 Cycles: −65°C to +150°C) to insure that all devices are free from metalization, bonding or packaging defects. (Monitored by QA)

Metal Can
Pneupactor for constant acceleration and mechanical shock (15,000G for 0.5 msec) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened. Monitored by QA)

Hermeticity Testing to eliminate devices which show insufficient hermeticity. (Monitored by QA)
Fine leak C DIPs, CERDIPs, and Metal cans (MIL-STD-883 Method 1014A)* **Gross Leak** C DIPs and Cerdips only (Method 1014C; vacuum omitted and 2 hour pressurization).

MIL-STD-883 100% screens for class B devices which are performed on a "Customer Special" basis are:

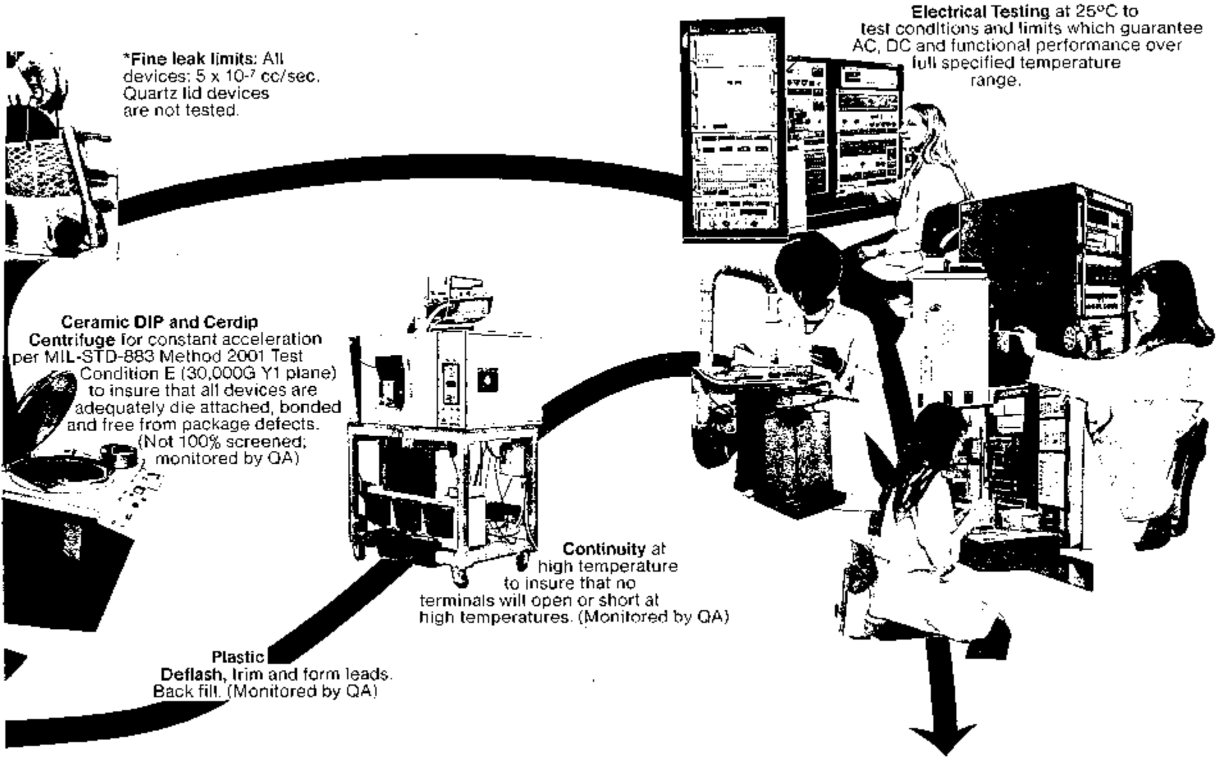
Stabilization Bake	(Method 1008)
Burn-in	(Method 1015, conditions A, B, or C)

MIL-STD-883 Group A Electrical Tests of Method 5005 at maximum and minimum operating temperatures are performed on a "Customer Special" basis.

MIL-STD-883 Group B and C tests are performed periodically to provide generic data. Reprints of the reports on these tests are available from:

Product Marketing
Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

COMPUTER GRADE PRODUCTS*



Ceramic DIP and Cerdip Centrifuge for constant acceleration per MIL-STD-883 Method 2001 Test Condition E (30,000G Y1 plane) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened; monitored by QA)

Plastic Deflash, trim and form leads. Back fill. (Monitored by QA)

Continuity at high temperature to insure that no terminals will open or short at high temperatures. (Monitored by QA)

Electrical Testing at 25°C to test conditions and limits which guarantee AC, DC and functional performance over full specified temperature range.

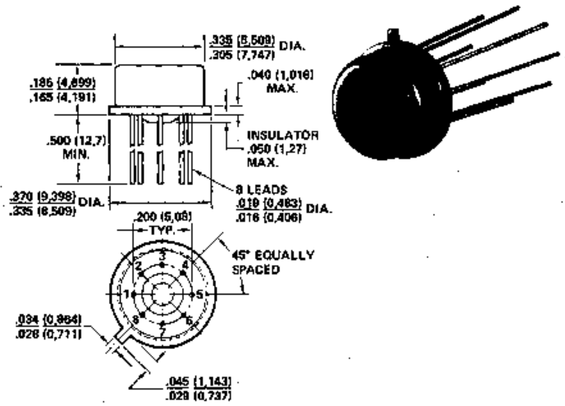
Final QA Acceptance per MIL-STD-883 Method 2009 External Visual (LTPD 7, Max. Acc. 3), and Electrical AC, DC, Functional Tests at 25°C with correlated limits to guarantee performance over full specified temperature range (LTPD 7, Max. Acc. 2)

***Fine leak limits:** All devices: 5×10^{-7} cc/sec. Quartz lid devices are not tested.

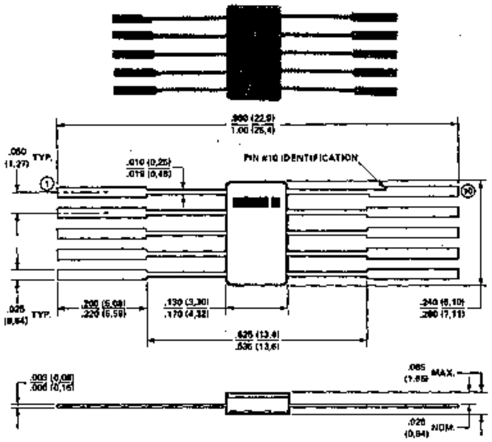
PACKAGING INFORMATION

Dimensions in inches and (millimeters).

8-LEAD METAL CAN PACKAGE (M)



10-LEAD FLAT PACK PACKAGE (F)



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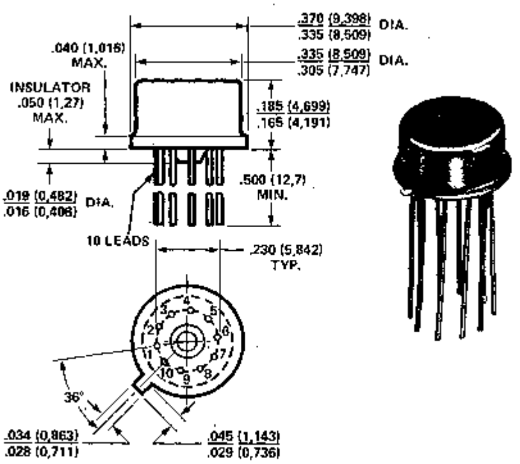
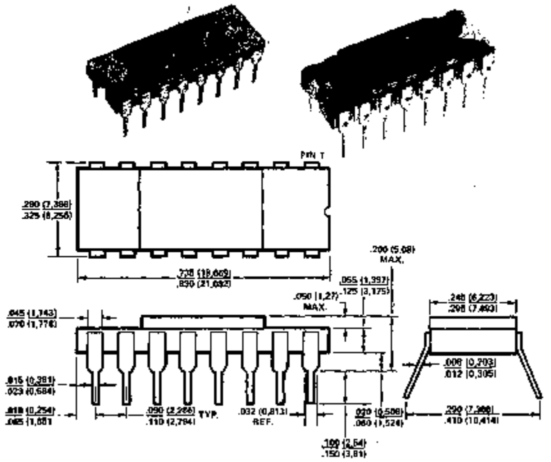
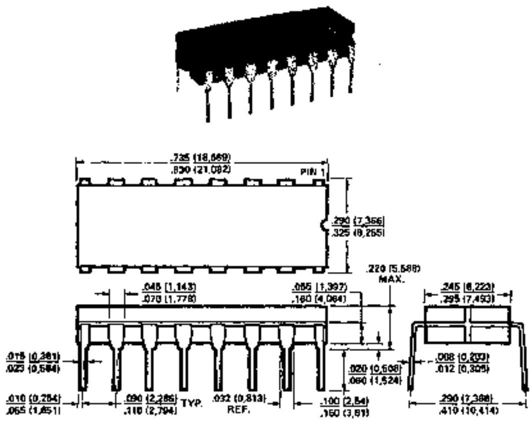


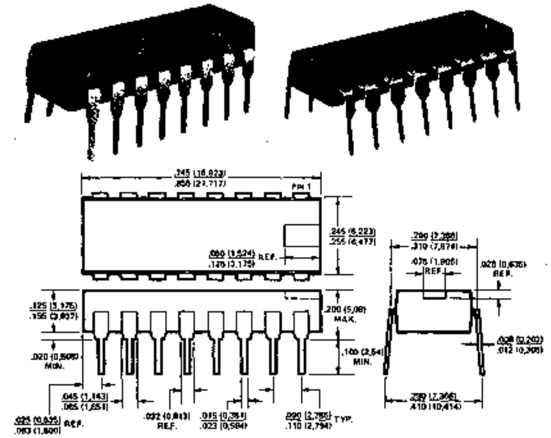
16-LEAD CERAMIC DUAL IN-LINE PACKAGE (C)



16-LEAD CerDIP DUAL IN-LINE PACKAGE (D)



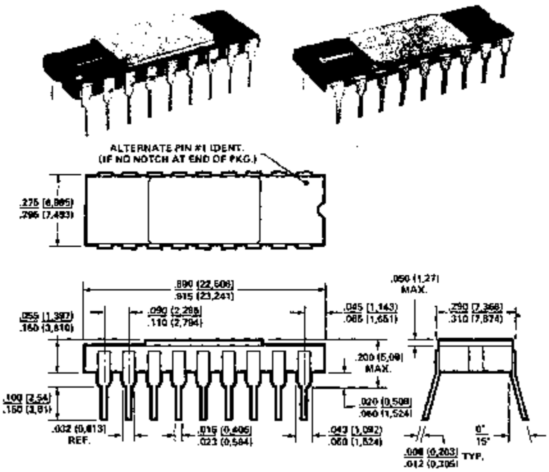
16-LEAD PLASTIC DUAL IN-LINE PACKAGE (P)



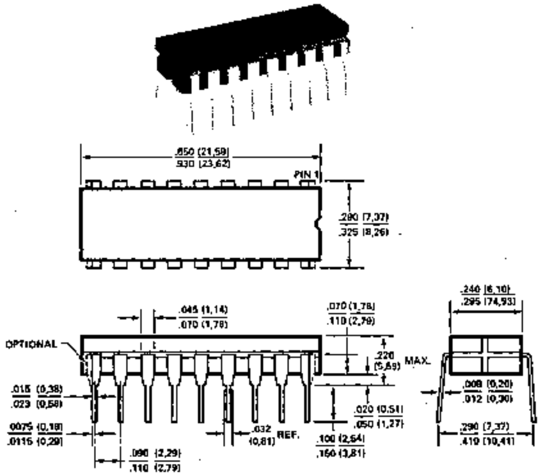
PACKAGING INFORMATION

Dimensions in inches and (millimeters).

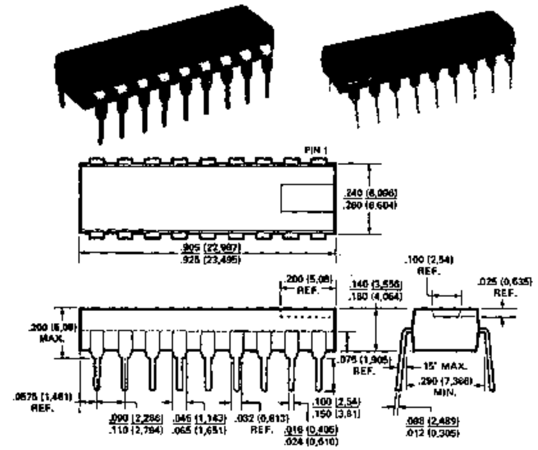
18-LEAD CERAMIC DUAL IN-LINE PACKAGE (C)



18-LEAD CerDIP DUAL IN-LINE PACKAGE (D)



18-LEAD PLASTIC DUAL IN-LINE PACKAGE (P)



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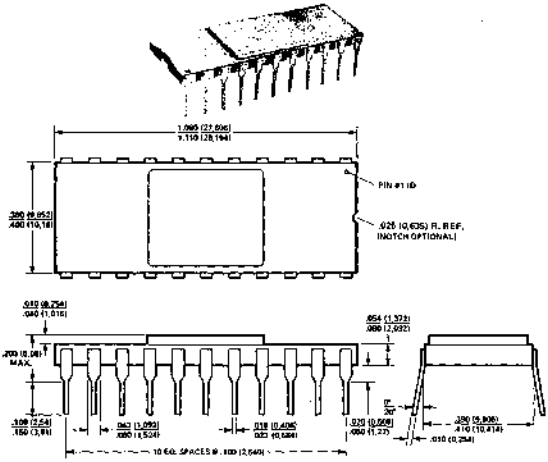

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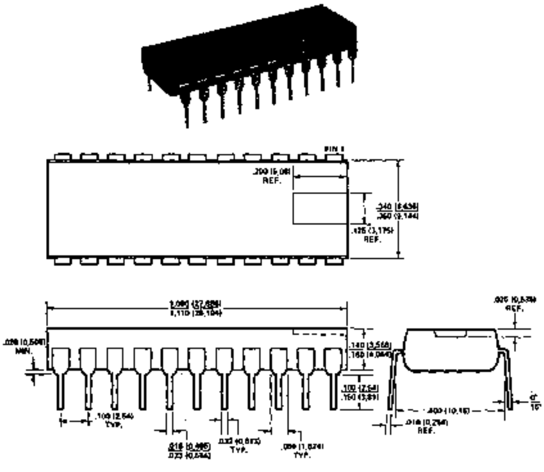

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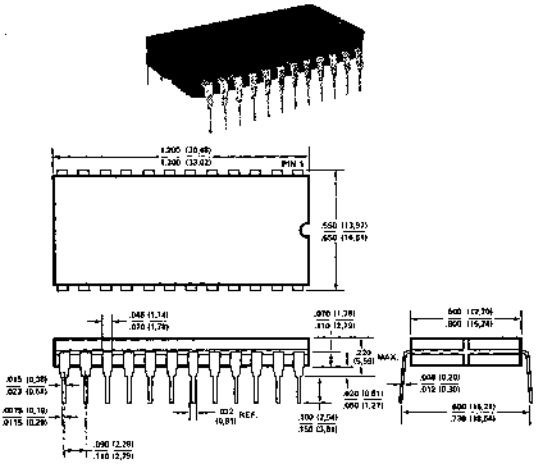
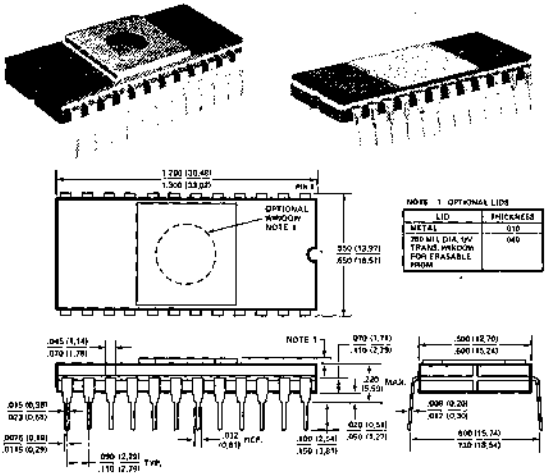


PACKAGING INFORMATION

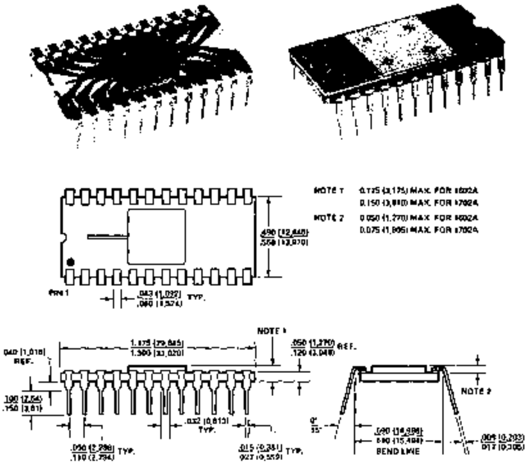
Dimensions in inches and (millimeters).

24-LEAD CERAMIC DUAL IN-LINE PACKAGE (C)



NOTE 1 OPTIONAL LIDS

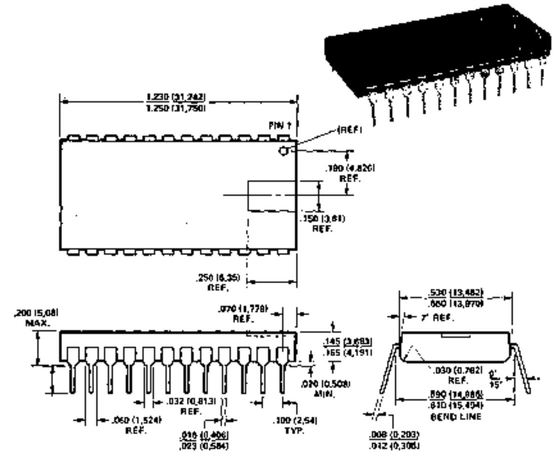
LID	THICKNESS
METAL	.010
780 MIL DIA. UV TRANS. WINDOW FOR ERASABLE PROM	.040



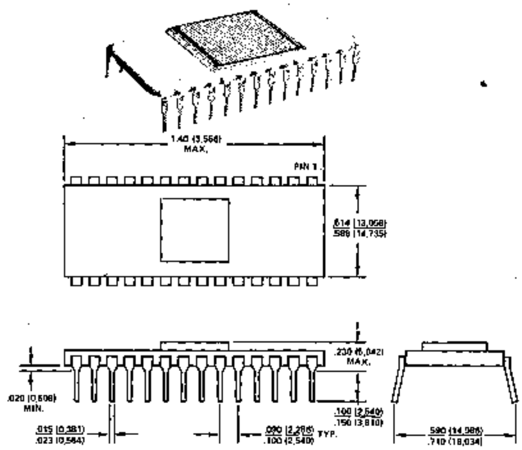
NOTE 1 0.125 (3.175) MAX. FOR 1602A
0.150 (3.810) MAX. FOR 1702A

NOTE 2 0.050 (1.270) MAX. FOR 1602A
0.075 (1.905) MAX. FOR 1702A

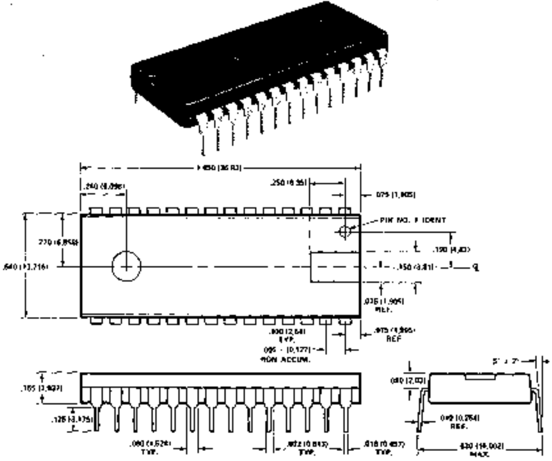
24-LEAD PLASTIC DUAL IN-LINE PACKAGE (P)



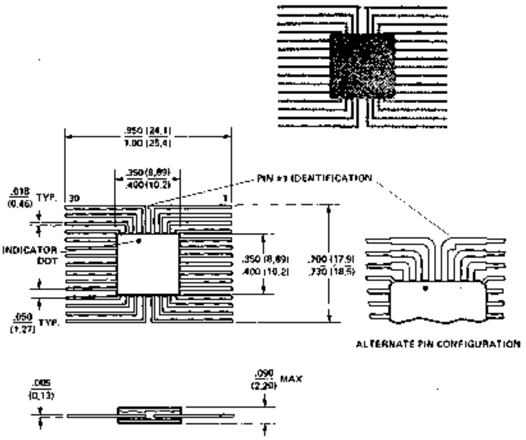
28-LEAD CERAMIC DUAL IN-LINE PACKAGE (C)



28-LEAD PLASTIC DUAL IN-LINE PACKAGE (P)



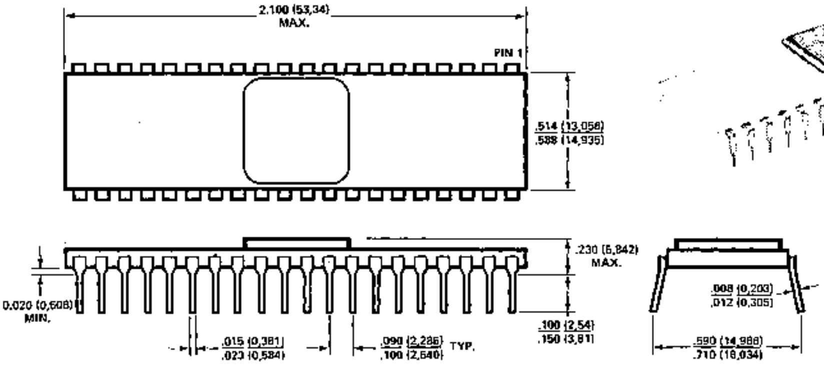
30-LEAD FLAT PACK PACKAGE (F)

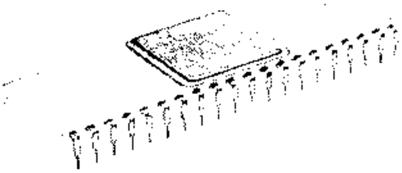


PACKAGING INFORMATION

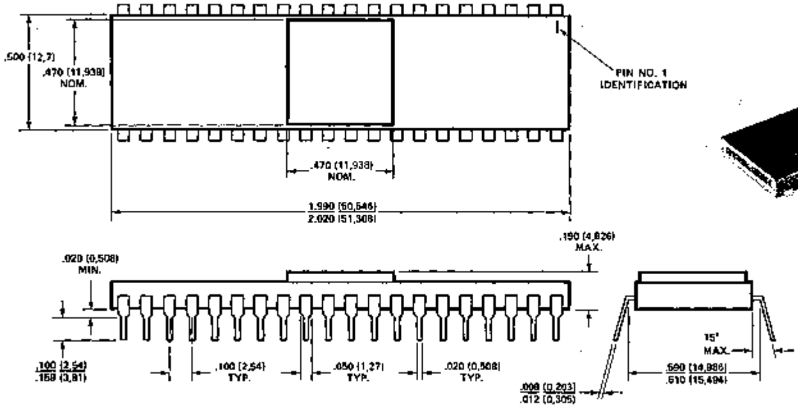
Dimensions in inches and (millimeters).

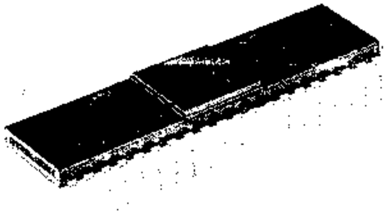
40-LEAD CERAMIC DUAL IN-LINE PACKAGE (C)





40-LEAD PLASTIC DUAL IN-LINE PACKAGE (P)





ORDERING INSTRUCTIONS

I. MEMORY COMPONENTS (Products in Sections 2, 3, 4, 5, and 8)

The following list indicates the basic package type(s) available for each Intel product. To order, place the appropriate package designation letter before the Intel product number. (For example, when ordering Intel's standard 1103 in a plastic dual in-line package, it should be ordered as P 1103.)

Package Designation Letter	Basic Package Type Description
C	Ceramic (Metal Lid) Dual In-line Package (Hermetic)
D	CerDIP (Glass Seal) Dual In-line Package (Hermetic)
P	Plastic Dual In-line Package
M	Metal Can Package (Hermetic)
F	Flat Package

Within each basic package type there are various outlines corresponding to the different number of leads. (See the package outline on page 1-8.)

Intel Product Type	Standard Package Type Available				No. Of Leads
1101A, 1101A-1	P	C			16
1103, 1103-1, 1103A, 1103A, 1103A-2	P	C	D		18
1302	P	C			24
1402A		C			16
1403A				M	8
1404A				M	8
1405A				M	10
1406, 1407, 1506, 1507				M	8
1602A, 1602A-6		C			24
1702A, 1702A-6		C			24
2101, 2101-1, 2101-2	P	C	D		22
2102, 2102-1, 2102-2, 2102-8	P	C			16
2102A, 2102AL, 2102A-2, 2102AL-2, 2102A-4, 2102AL-4	P	C	D		16
M2102A-4, M2102A-6		C			16
2105, 2105-1, 2105-2	P	C			18
2107A, 2107A-1, 2107A-4, 2107A-5, 2107A-8	P	C	D		22
2107B, 2107B-4, 2107B-6	P	C	D		22
2111, 2111-1, 2111-2	P	C	D		18
2112, 2112-2	P	C	D		16
2308	P	C			24
2316A	P	C			24
2401, 2405	P	C			16
C2416		C			22
P2416	P				18
2704		C			24
2708		C			24

Intel Product Type	Standard Package Type Available				No. Of Leads
3101, 3101A	P	C	D		16
3104		C			24
3106, 3106A, 3106-8, 3107, 3107A, 3107-8	P	C	D		16
3205	P	C	D		16
3207A, 3207A-1			D		16
3208A	P		D		18
3210			D		18
3211			D		18
3235			D		16
3301A	P	C	D		16
M3301A		C	D		16
3302, 3302-4, 3302-6	P	C	D		16
3304A, 3304A-4, 3304A-6		C	D		24
3322, 3322-4, 3322-6	P	C	D		16
3324A, 3324A-4		C	D		24
3404	P	C	D		16
3408A	P		D		18
3601, 3601-1			D		16
M3601			D		16
3602, 3602-4, 3602-6			D		16
3604, 3604-4, 3604-6			D		24
3622, 3622-4, 3622-6			D		16
3624, 3624-4			D		24
5101, 5101-3, 5101L, 5101L-3	P	C	D		22
5201, 5201-2				F	30
5202, 5202-2				F	30
5204				F	30
5801				F	10

NOTE: The data sheets in this catalog are subject to change without notice. You can insure your specification is the current revision by contacting your local Intel sales office.

LITERATURE GUIDE

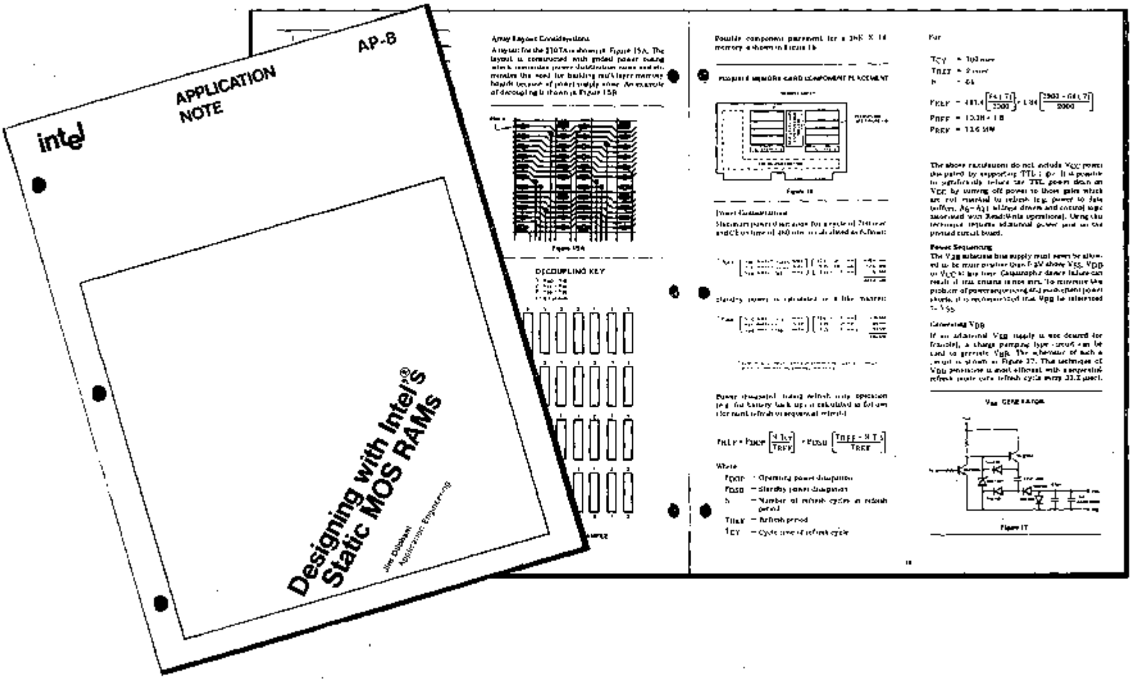
The following literature guide provides further information on many products described in this data catalog. The list includes only a few of our major pieces of literature. If you have specific requirements for more detailed information on one or more of our products, contact your local Intel sales office or Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. If you wish to receive literature on a continuing basis, please fill our the card at the front of this book.

APPLICATION NOTES AND ARTICLE REPRINTS

AP4	Designing Memory Systems with the Intel® 2107A 4K RAM
AP5	Designing High Speed, Low Cost Memory Systems with the Intel® 2105
AP6	Designing with Intel® PROMs & ROMs
AP8	Designing with Intel®s Static MOS RAMs
AP10	Memory System Design with the Intel® 2107B 4K RAM
AR12	Semiconductor Memory Costs Present and Future
AR14	1024 Bit Bipolar RAM

MICROCOMPUTER LITERATURE

AR3 Microcomputers, What they mean to your Company
MCS-40™ User's Manual
MCS-8™ User's Manual
MCS-80™ Systems Manual



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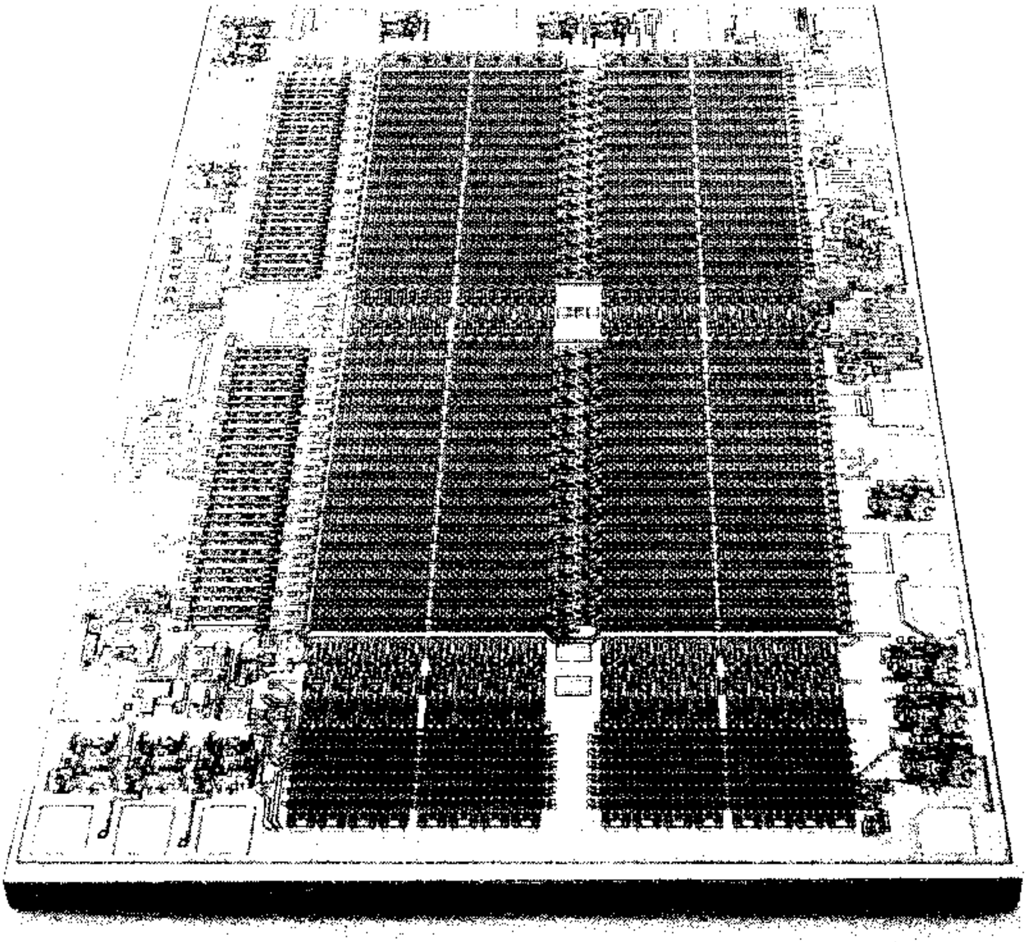
RANDOM ACCESS MEMORIES



RANDOM ACCESS MEMORIES

	Type	No. of Bits	Description	Organization	Electrical Characteristics Over Temperature				
					Access Time Max.	Cycle Time Max.	Power Dissipation Max.(1) Operating/Standby	Supplies [V]	Page No.
SILICON GATE MOS	1101A	256	Static Fully Decoded	256 x 1	1500ns	1500ns	685mW/340mW	+5, −9	2-3
	1101A1	256	Hi-Speed Static Fully Decoded	256 x 1	1000ns	1000ns	685mW/340mW	+5, −9	2-3
	1103	1024	Dynamic Fully Decoded	1024 x 1	300ns	580ns	400mW/67mW	+16, +19	2-7
	1103-1	1024	Dynamic Fully Decoded	1024 x 1	150ns	340ns	400mW/76mW	+19, +22	2-12
	1103A	1024	Dynamic Fully Decoded	1024 x 1	205ns	580ns	400mW/64mW	+16, +19	2-15
	1103A-1	1024	Dynamic Fully Decoded	1024 x 1	145ns	340ns	625mW/10mW	+19, +22	2-20
	1103A-2	1024	Dynamic Fully Decoded	1024 x 1	145ns	400ns	570mW/10mW	+19, +22	2-25
	2101	1024	Static, Separate I/O	256 x 4	1000ns	1000ns	350mW	+5	2-29
	2101-1	1024	Static, Separate I/O	256 x 4	500ns	500ns	350mW	+5	2-29
	2101-2	1024	Static, Separate I/O	256 x 4	650ns	650ns	350mW	+5	2-29
	2102	1024	Static Fully Decoded	1024 x 1	1000ns	1000ns	350mW	+5	2-33
	2102-1	1024	Hi-Speed Static Fully Decoded	1024 x 1	500ns	500ns	350mW	+5	2-37
	2102-2	1024	Static Fully Decoded	1024 x 1	650ns	650ns	350mW	+5	2-39
	2102-8	1024	Static Fully Decoded	1024 x 1	1500ns	1500ns	350mW	+5	2-41
	2102A	1024	Very High Speed Static	1024 x 1	350ns	350ns	350mW/42mW	+5	2-43
	2102A-2	1024	Very High Speed Static	1024 x 1	250ns	250ns	350mW/42mW	+5	2-47
	2102A-4	1024	Very High Speed Static	1024 x 1	450ns	450ns	350mW/42mW	+5	2-49
	M2102A-4	1024	Static, T_A = 55°C to +125°C	1024 x 1	450ns	450ns	350mW	+5	2-51
	M2102A-6	1024	Static, T_A = 55°C to +125°C	1024 x 1	650ns	650ns	350mW	+5	2-53
	2105	1024	Hi-Speed Dynamic Fully Decoded	1024 x 1	95ns	200ns	460mW/97mW	+12, −5.2	2-55
	2105-1	1024	Very High Speed Dynamic Fully Decoded	1024 x 1	80ns	180ns	513mW/97mW	+12, −5.2	2-55
	2105-2	1024	High Speed Dynamic with Invisible Refresh	1024 x 1	85ns	190ns	540mW/97mW	+12, −5.2	2-63
	2107A	4096	Dynamic Fully Decoded	4096 x 1	300ns	700ns	458mW/10mW	+12, +5, −5	2-67
	2107A-1	4096	Dynamic Fully Decoded	4096 x 1	280ns	550ns	516mW/16mW	+12, +5, −5	2-73
	2107A-4	4096	Dynamic Fully Decoded	4096 x 1	350ns	840ns	405mW/10mW	+12, +5, −5	2-75
	2107A-5	4096	Dynamic Fully Decoded	4096 x 1	420ns	970ns	376mW/11mW	+12, +5, −5	2-77
	2107A-8	4096	Dynamic Fully Decoded	4096 x 1	420ns	970ns	376mW/11mW	+12, +5, −5	2-79
	2107B	4096	Dynamic Fully Decoded	4096 x 1	200ns	400ns	960mW/16mW	+12, +5, −5	2-81
	2107B-4	4096	Dynamic Fully Decoded	4096 x 1	270ns	470ns	960mW/18mW	+12, +5, −5	2-89
	2107B-6	4096	Dynamic Fully Decoded	4096 x 1	350ns	800ns	840mW/25mW	+12, +5, −5	2-91
	2111	1024	Static, Common I/O with Output Deselect	256 x 4	1000ns	1000ns	350mW	+5	2-93
	2111-1	1024	Static, Common I/O with Output Deselect	256 x 4	500ns	500ns	350mW	+5	2-93
	2111-2	1024	Static, Common I/O with Output Deselect	256 x 4	650ns	650ns	350mW	+5	2-93
	2112	1024	Static, Common I/O without Output Deselect	256 x 4	1000ns	1000ns	350mW	+5	2-97
	2112-2	1024	Static, Common I/O without Output Deselect	256 x 4	650ns	650ns	350mW	+5	2-97
SCHOTTKY BIPOLAR	3101	64	Fully Decoded	16 x 4	60ns	60ns	525mW	+5	2-101
	3101A	64	High Speed Fully Decoded	16 x 4	35ns	35ns	525mW	+5	2-101
	M3101	64	Fully Decoded (−55°C to +125°C	16 x 4	75ns	75ns	546mW	+5	2-105
	M3101A	64	High Speed Fully Decoded (−55°C to +125°C)	16 x 4	45ns	45ns	546mW	+5	2-105
	3104	16	Content Addressable Memory	4 x 4	30ns	40ns	625mW	+5	2-107
	3106	256	High Speed Fully Decoded (With 3-State Output)	256 x 1	80ns	80ns	650mW	+5	2-111
	3106A	256	High Speed Fully Decoded (With 3-State Output)	256 x 1	60ns	70ns	650mW	+5	2-111
	3106-8	256	High Speed Fully Decoded (With 3-State Output)	256 x 1	80ns	80ns	650mW	+5	2-111
	3107	256	High Speed Fully Decoded (With Open Collector Output)	256 x 1	80ns	80ns	650mW	+5	2-111
	3107A	256	High Speed Fully Decoded (With Open Collector Output)	256 x 1	60ns	70ns	650mW	+5	2-111
	3107-8	256	High Speed Fully Decoded (With Open Collector Output)	256 x 1	60ns	70ns	650mW	+5	2-111
SILICON GATE CMOS	5101	1024	Static CMOS RAM	256 x 4	650ns	650ns	142mW/75µW	+5	2-115
	5101-3	1024	Static CMOS RAM	256 x 4	650ns	650ns	142mW/1mW	+5	2-115
	5101L	1024	Static CMOS RAM	256 x 4	650ns	650ns	142mW/30µW	+5	2-115
	5101L-3	1024	Static CMOS RAM	256 x 4	650ns	650ns	142mW/400µW	+5	2-115

Note 1: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

intel® Silicon Gate MOS 1101A, 1101A1

256 BIT FULLY DECODED RANDOM ACCESS MEMORY

- **Access Time -- Typically Below 650 nsec - 1101A1, 850 nsec - 1101A**
- **Low Power Standby Mode**
- **Low Power Dissipation -- Typically less than 1.5 mW/bit during access**
- **Directly DTL and TTL Compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip Select Input Lead**
- **Fully Decoded -- On Chip Address Decode and Sense**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration**

The 1101A is an improved version of the 1101 which requires only two power supplies (+5V and −9V) for operation. The 1101A is a direct pin for pin replacement for the 1101.

The Intel® 1101A is a 256 word by 1 bit random access memory element using normally off P-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks to operate.

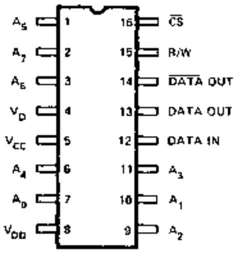
The 1101A is designed primarily for small buffer storage applications where high performance, low cost, and ease of interfacing with other standard logic circuits are important design objectives. The unit will directly interface with standard bipolar integrated logic circuits (TTL, DTL, etc.) The data output buffers are capable of driving TTL loads directly. A separate chip select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

For applications requiring a faster access time we recommend the 1101A1 which is a selection from the 1101A and has a guaranteed maximum access time of 1.0 μsec.

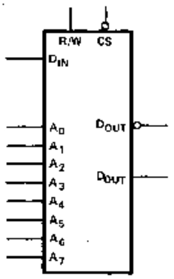
The Intel 1101A is fabricated with **silicon gate technology**. This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's **silicon gate technology** also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

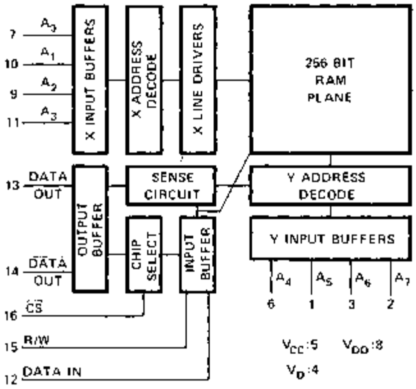
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	CS	CHIP SELECT
$A_0 - A_7$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT		

Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.5V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	−20V
Power Dissipation	1 WATT

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_D = -9V \pm 5\%$, unless otherwise specified

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)		<1.0	500	nA	$V_{IN} = 0.0$ V
I_{LO}	OUTPUT LEAKAGE CURRENT		<1.0	500	nA	$V_{OUT} = 0.0$ V, $\overline{CS} = V_{CC} - 2$
I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		13	19	mA	$T_A = 25°C$ Continuous Operation $I_{OL} = 0.0$ mA
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}			25	mA	$T_A = 0°C$
I_{D1}	POWER SUPPLY CURRENT, V_D		12	18	mA	$T_A = 25°C$,
I_{D2}	POWER SUPPLY CURRENT, V_D			24	mA	$T_A = 0°C$,
V_{IL}	INPUT "LOW" VOLTAGE	−10		$V_{CC}-4.5$	V	
V_{IH}[3]	INPUT "HIGH" VOLTAGE	$V_{CC}-2$		$V_{CC}+0.3$	V	
I_{OL1}	OUTPUT SINK CURRENT	3.0	8		mA	$V_{OUT} = +0.45$ V, $T_A = +25°C$
I_{OL2}	OUTPUT SINK CURRENT	2.0			mA	$V_{OUT} = +0.45$ V, $T_A = +70°C$
I_{CF}	OUTPUT CLAMP CURRENT		6	13	mA	$V_{OUT} = -1.0$ V
I_{OH1}	OUTPUT SOURCE CURRENT	−3.0	−8		mA	$V_{OUT} = 0.0$ V, $T_A = +25°C$
I_{OH2}	OUTPUT SOURCE CURRENT	−2.0	−7		mA	$V_{OUT} = 0.0$ V, $T_A = +70°C$
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	$I_{OL} = 2.0$ mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.5	+4.9		V	$I_{OH} = -100\mu A$
C_{IN}[4]	INPUT CAPACITANCE (ALL INPUT PINS)		7	10	pF	$V_{IN} = V_{CC}$ f = 1 MHz $T_A = 25°C$
C_{OUT}[4]	OUTPUT CAPACITANCE		7	10	pF	$V_{OUT} = V_{CC}$
C_V[4]	V_D POWER SUPPLY CAPACITANCE		20	35	pF	$V_D = V_{CC}$

Note 1: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are at nominal voltages and $T_A = 25°C$.

Note 3: A TTL driving the 1101A, 1101A1 must have its output high $\geq V_{CC}-2$ even if it is loaded by other bipolar gates.

Note 4: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_D = -9V \pm 5\%$, $V_{DD} = -9V \pm 5\%$

READ CYCLE

SYMBOL	TEST		MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle	1101A 1101A1	1.5 1.0			µsec µsec
t_{AC}	Address to Chip Select Delay	1101A 1101A1	-		1.2[1] 0.7[1]	µsec µsec
t_A	Access Time	1101A 1101A1		0.85 0.65	1.5 1.0	µsec µsec
t_{OH}	Previous Read Data Valid		0.05			µsec

WRITE CYCLE

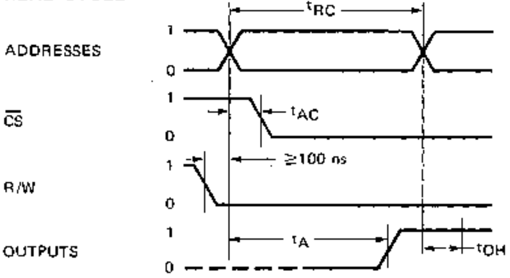
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle	0.8			µsec
t_{WD}	Address to Write Pulse Delay	0.3			µsec
t_{WP}	Write Pulse Width	0.4			µsec
t_{DW}	Data Set up Time	0.3			µsec
t_{DH}	Data Hold Time	0.1			µsec

CHIP SELECT AND DESELECT

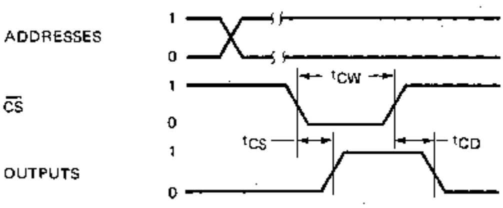
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT
t_{CW}	Chip Select Pulse Width	0.4			µsec
t_{CS}	Access Time Through Chip Select Input		0.2	0.3	µsec
t_{CD}	Chip Deselect Time		0.1	0.3	µsec

CONDITIONS OF TEST:
Input pulse amplitudes: 0 to 5V, Input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5V levels (unless otherwise noted). Output load is 1 TTL gate and $C_L = 20$ pF; measurements made at output of TTL gate ($t_{PD} \leq 10$ nsec)

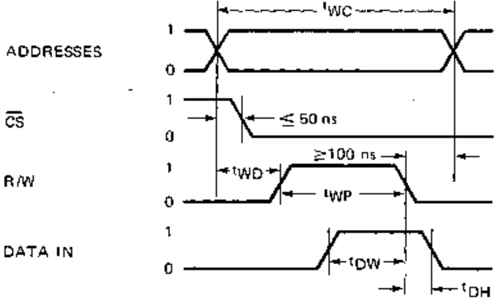
READ CYCLE



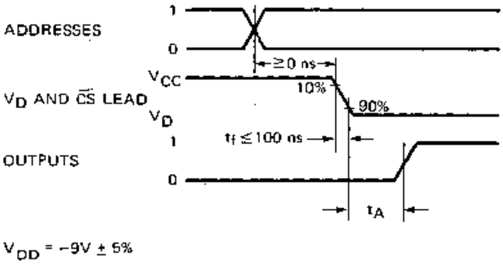
CHIP SELECT AND DESELECT



WRITE CYCLE



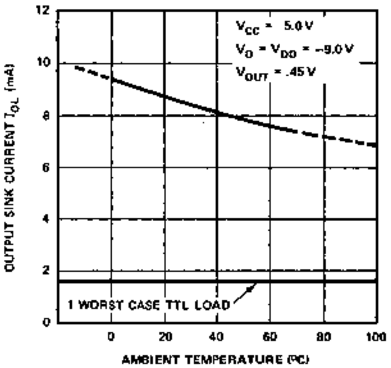
POWER SWITCHING OF V_D



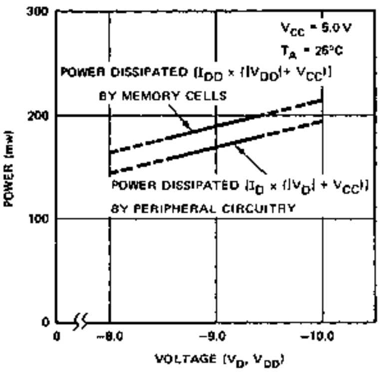
Note 1: Maximum value for t_{AC} measured at minimum read cycle.

Typical D. C. Characteristics

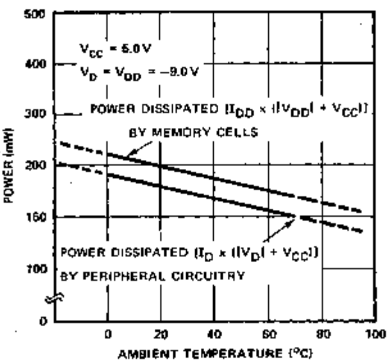
OUTPUT SINK CURRENT VS TEMPERATURE



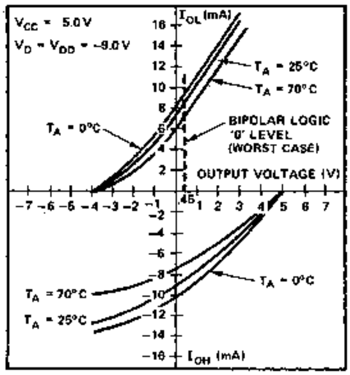
POWER DISSIPATION VS VOLTAGE



POWER DISSIPATION VS TEMPERATURE

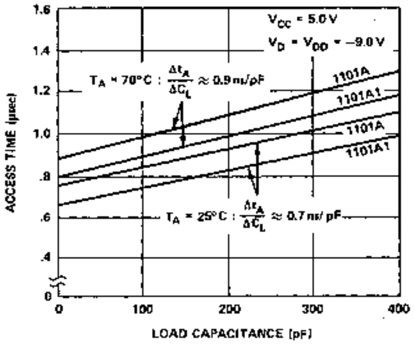


OUTPUT CURRENT VS OUTPUT VOLTAGE

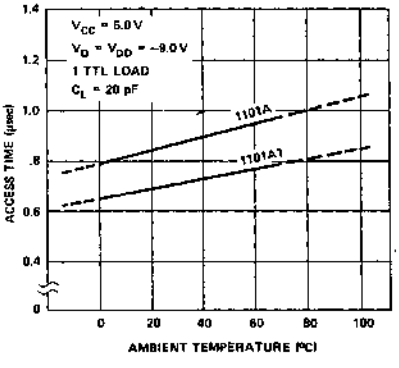


Typical A. C. Characteristics

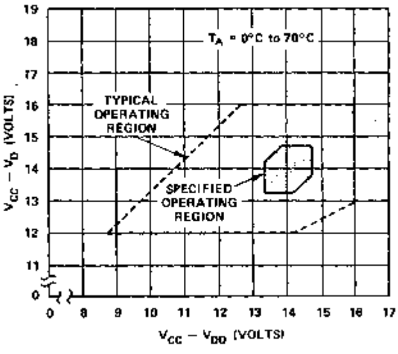
ACCESS TIME VS.
LOAD CAPACITANCE



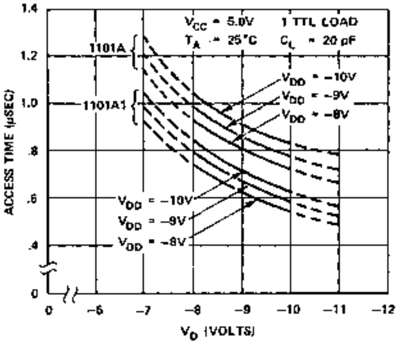
ACCESS TIME VS.
TEMPERATURE



1101A/1101A1
OPERATING REGION



ACCESS TIME VS.
SUPPLY VOLTAGE



intel®

Silicon Gate MOS 1103

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- **Low Power Dissipation — Dissipates Power Primarily on Selected Chips**
- **Access Time — 300 nsec**
- **Cycle Time — 580 nsec**
- **Refresh Period... 2 milliseconds for 0—70° C Ambient**
- **OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input Lead**
- **Fully Decoded—on Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 18 Pin Dual In-Line Configuration.**

The Intel®1103 is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

It is a 1024 word by 1 bit random access memory element using normally off *P*-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18 pin dual in-line package. It uses dynamic circuitry and primarily dissipates power only during precharge.

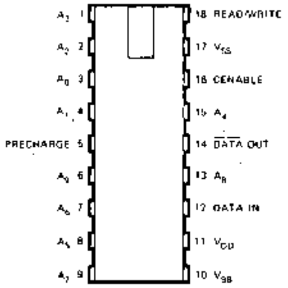
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds.

A separate **cenable** (chip enable) lead allows easy selection of an individual package when outputs are OR-tied.

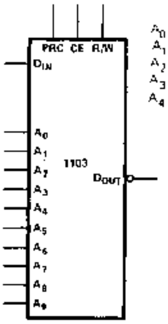
The Intel 1103 is fabricated with **silicon gate technology.** This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

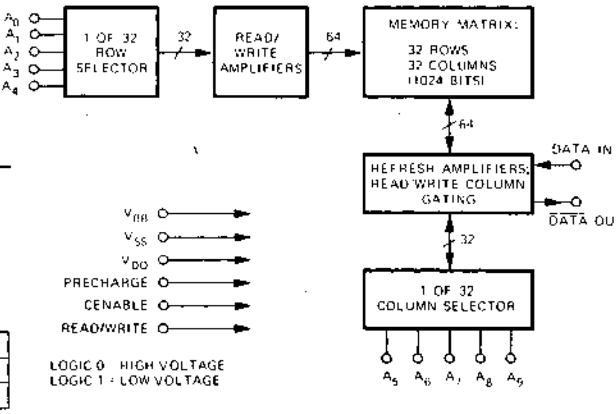
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	PRC	PRECHARGE INPUT
A_0–A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	D_{OUT}	DATA OUTPUT

Maximum Guaranteed Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Power Dissipation	1.0 W

*COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{SS}(1) = 16V ± 5%, $(V_{BB} - V_{SS})$(6) = 3V to 4V, V_{DD} = 0V unless otherwise specified

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT (ALL INPUT PINS)**			**1**	**μA**	**V_{IN} = 0V**
I_{LO}	OUTPUT LEAKAGE CURRENT			1	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			**100**	**μA**	
I_{DD1}(2)	SUPPLY CURRENT DURING T_{PC}		37	56	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS}; T_A = 25°C
I_{DD2}(2)	SUPPLY CURRENT DURING T_{OV}		38	59	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V; T_A = 25°C
I_{DD3}(2)	SUPPLY CURRENT DURING T_{POV}		5.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V; T_A = 25°C
I_{DD4}(2)	SUPPLY CURRENT DURING T_{CP}		3	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS}; T_A = 25°C
$I_{DD\,AV}$(5)	**AVERAGE SUPPLY CURRENT**		**17**	**25**	**mA**	**CYCLE TIME = 580 ns; PRECHARGE WIDTH = 190 ns; T_A = 25°C**
V_{IL1}(7)	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	$V_{SS}-17$		$V_{SS}-14.2$	V	T_A = 0°C
V_{IL2}(7)	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	$V_{SS}-17$		$V_{SS}-14.5$	V	T_A = 70°C
V_{IL3}(7,8)	INPUT LOW VOLTAGE (PRECHARGE CENABLE & READ/WRITE INPUTS)	$V_{SS}-17$		$V_{SS}-14.7$	V	T_A = 0°C
V_{IL4}(7,8)	INPUT LOW VOLTAGE (PRECHARGE CENABLE& READ/WRITE INPUTS)	$V_{SS}-17$		$V_{SS}-15.0$	V	T_A = 70°C
V_{IH1}(7)	INPUT HIGH VOLTAGE (ALL INPUTS)	$V_{SS}-1$		$V_{SS}+1$	V	T_A = 0°C
V_{IH2}(7)	INPUT HIGH VOLTAGE (ALL INPUTS)	$V_{SS}-0.7$		$V_{SS}+1$	V	T_A = 70°C
I_{OH1}	**OUTPUT HIGH CURRENT**	**600**	**900**	**4000**	**μA**	**T_A = 25°C** R_{LOAD} = 100 Ω (4)
I_{OH2}	**OUTPUT HIGH CURRENT**	**500**	**800**	**4000**	**μA**	**T_A = 70°C**
I_{OL}	OUTPUT LOW CURRENT	See Note 3				
V_{OH1}	OUTPUT HIGH VOLTAGE	60	90	400	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	50	80	400	mV	T_A = 70°C,
V_{OL}	OUTPUT LOW VOLTAGE	See Note 3				

Note 1: The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.

Note 2: See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100 Ω to 1 kΩ.

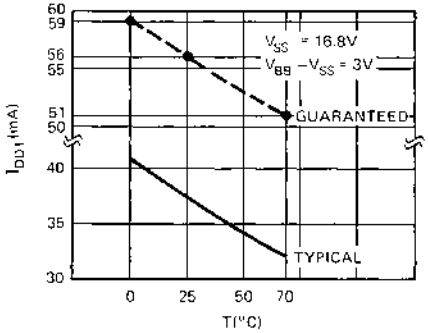
Note 5: This parameter is periodically sampled and is not 100% tested.

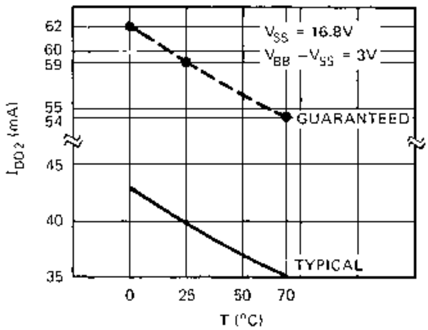
Note 6: $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.

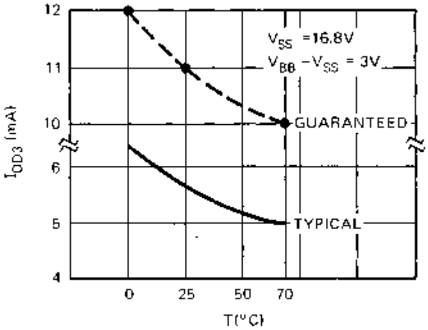
Note 7: The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value in between 0°C and 70°C can be calculated by using a straight-line relationship.

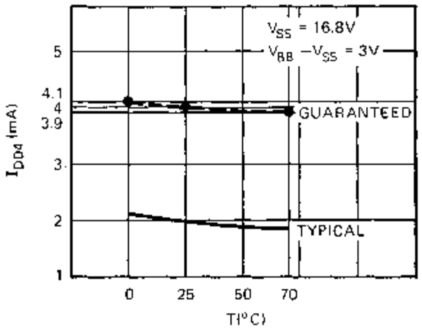
Note 8: The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to $V_{SS}-14.2$ @ 0°C and $V_{SS}-14.5$ @ 70°C (same values as those specified for the address & data-in lines) with a 40ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.

Supply Current vs Temperature

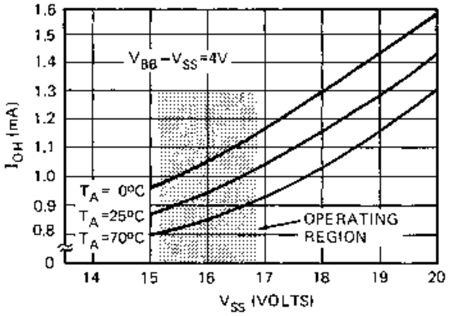


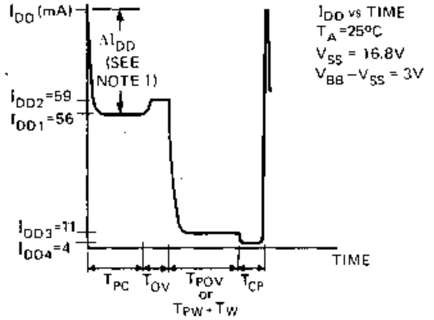






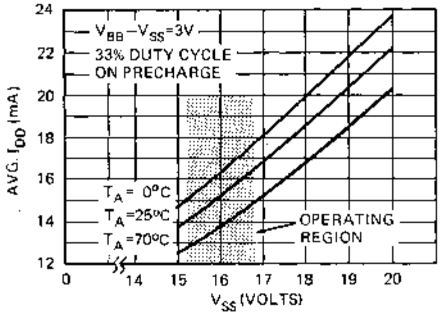
Typical Characteristics

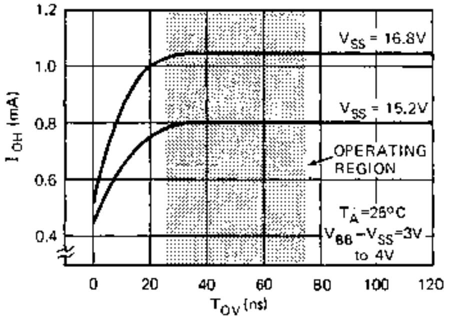




Note 1. ΔI_{DD} is due to charging of internal device node capacitance at precharge

Note 2. These values are taken from a single pulse measurement





AC Characteristics T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, $(V_{BB} - V_{SS})$ = 3.0V to 4.0V, V_{DD} = 0V

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			2	ms	
t_{AC}(1)	ADDRESS TO CENABLE SET UP TIME	115			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	20			ns	
t_{PC}(1)	PRECHARGE TO CENABLE DELAY	125			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	85			ns	
t_{OVL}	PRECHARGE & CENABLE OVERLAP, LOW	25		75	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			140	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	45		95	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
t_{RC}(1)	**READ CYCLE**	480			ns		t_r = 20 ns C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV
t_{POV}	PRECHARGE TO END OF CENABLE	165		500	ns		
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns		
t_{ACC1}(1)	**ADDRESS TO OUTPUT ACCESS**	300			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$	
t_{ACC2}(1)	**PRECHARGE TO OUTPUT ACCESS**	310			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_r$	

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}(1)	**WRITE CYCLE**	580			ns	t_r = 20 ns
t_{RWC}(1)	**READ/WRITE CYCLE**	580			ns	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	165		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	50			ns	
t_W	READ/WRITE SET UP TIME	80			ns	
t_{DW}	DATA SET UP TIME	105			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

Note 1: These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to $V_{SS}-14.2V$ @ 0°C and $V_{SS}-14.5V$ @ 70°C as defined on page 2.

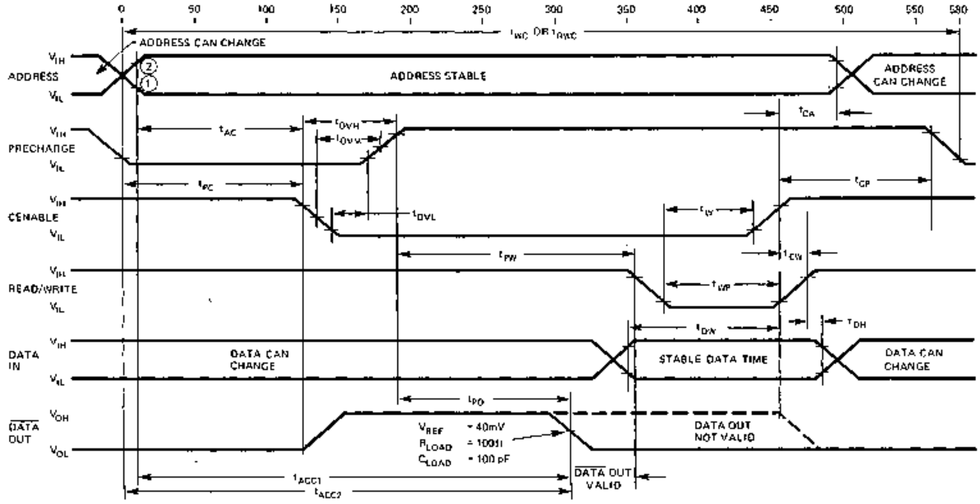
*CAPACITANCE T_A = 25 C

SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS	
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$	f = 1 MHz All Unused Pins Are At A.C. Ground
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$	
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$	
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$	
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V $V_{IN} = V_{SS}$	
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS} $V_{IN} = V_{SS}$	
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V	

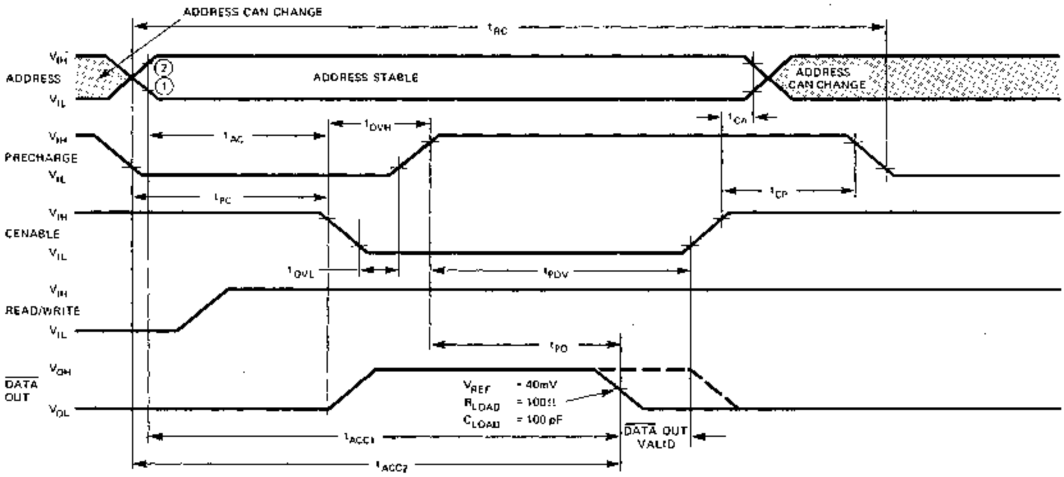
*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTE ① $V_{DD} + 2V$ } t_r IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS
NOTE ② $V_{SS} - 2V$
NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CENABLE OR READ/WRITE WHICHEVER OCCURS FIRST
NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

intel® Silicon Gate MOS 1103-1

The Intel®1103-1 is a high speed 1024 bit dynamic random access memory and is the high speed version of the standard 1103. The DC and AC Characteristics for the 1103-1 are given in the following three pages. The absolute maximum ratings for the 1103-1 are the same as for the 1103 on page 2-8.

- **Access Time — 150 nsec**
- **Cycle Time — 340 nsec**

D.C. and Operating Characteristics

($T_A = 0°C$ to $+55°C$, $V_{SS}^{1} = 19V \pm 5\%$ $(V_{BB} - V_{SS})^{6} = 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			**10**	**μA**	**$V_{IN} = 0V$**
I_{LO}	OUTPUT LEAKAGE CURRENT			10	μA	$V_{OUT} = 0V$
I_{BB}	**V_{BB} SUPPLY CURRENT**			**100**	**μA**	
I_{DD1}^{2}	SUPPLY CURRENT DURING T_{PC}		45	60	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS} $T_A = 25°C$
I_{DD2}^{2}	SUPPLY CURRENT DURING T_{OV}		50	68.5	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V $T_A = 25°C$
I_{DD3}^{2}	SUPPLY CURRENT DURING T_{POV}		8.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V $T_A = 25°C$
I_{DD4}^{2}	SUPPLY CURRENT DURING T_{CP}		3.0	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS} $T_A = 25°C$
$I_{DD\,AVG}^{5}$	**AVERAGE SUPPLY CURRENT**		**20**	**23**	**mA**	**CYCLE TIME = 340 ns** **PRECHARGE WIDTH @50% 105ns, $T_A = 25°C$**
V_{IL}	INPUT LOW VOLTAGE	$V_{SS} - 20$		$V_{SS} - 18$	V	
V_{IH}	INPUT HIGH VOLTAGE	$V_{SS} - 1$		$V_{SS} + 1$	V	
I_{OH1}	**OUTPUT HIGH CURRENT**	**1150**	**1300**	**7000**	**μA**	**$T_A = 25°C$** **$R_{LOAD}^{4} = 100\ \Omega$**
I_{OH2}	**OUTPUT HIGH CURRENT**	**900**	**1150**	**7000**	**μA**	**$T_A = 55°C$**
I_{OL}^{1}	OUTPUT LOW CURRENT	See Note 3				
V_{OH1}	OUTPUT HIGH VOLTAGE	115	130	700	mV	$T_A = 25°C$,
V_{OH2}	OUTPUT HIGH VOLTAGE	90	115	700	mV	$T_A = 55°C$,
V_{OL}^{1}	OUTPUT LOW VOLTAGE	See Note 3				

Note 1: The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.

Note 2: See Supply Current vs. Temperature (p. 2-9) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100 Ω to 1 kΩ.

Note 5: This parameter is periodically sampled and is not 100% tested.

Note 6: $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.

AC Characteristics (T_A = 0°C to 55°C, V_{SS} = 19 ± 5%, $V_{BB} - V_{SS}$ = 3.0V to 4.0V, V_{DD} = 0V)

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			**1**	**ms**	
t_{AC}	ADDRESS TO CENABLE SET UP TIME	30			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	10			ns	
t_{PC}	PRECHARGE TO CENABLE DELAY	60			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	40			ns	
t_{OVL}	PRECHARGE & CENABLE OVERLAP, LOW	5		30	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			85	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP 50% POINTS	25		50	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	**READ CYCLE**	**300**			**ns**	**$t_T = 20$ ns**
t_{POV}	PRECHARGE TO END OF CENABLE	115		500	ns	
t_{PO}(1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	$C_{LOAD} = 50$ pF $R_{LOAD} = 100\Omega$ $V_{REF} = 80$ mV
t_{ACC1}(1)	**ADDRESS TO OUTPUT ACCESS**	**150**			**ns**	**$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$** $C_{LOAD} = 50$ pF $R_{LOAD} = 100\Omega$ $V_{REF} = 80$ mV
t_{ACC2}(1)	**PRECHARGE TO OUTPUT ACCESS**	**180**			**ns**	**$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$** $C_{LOAD} = 50$ pF $R_{LOAD} = 100\Omega$ $V_{REF} = 80$ mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}	**WRITE CYCLE**	**340**			**ns**	**$t_T = 20$ ns**
t_{RWC}(1)	**READ/WRITE CYCLE**	**340**			**ns**	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	115		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	20			ns	
t_W	READ/WRITE SET UP TIME	20			ns	
t_{DW}	DATA SET UP TIME	40			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO}(1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	$C_{LOAD} = 50$ pF $R_{LOAD} = 100\Omega$ $V_{REF} = 80$ mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

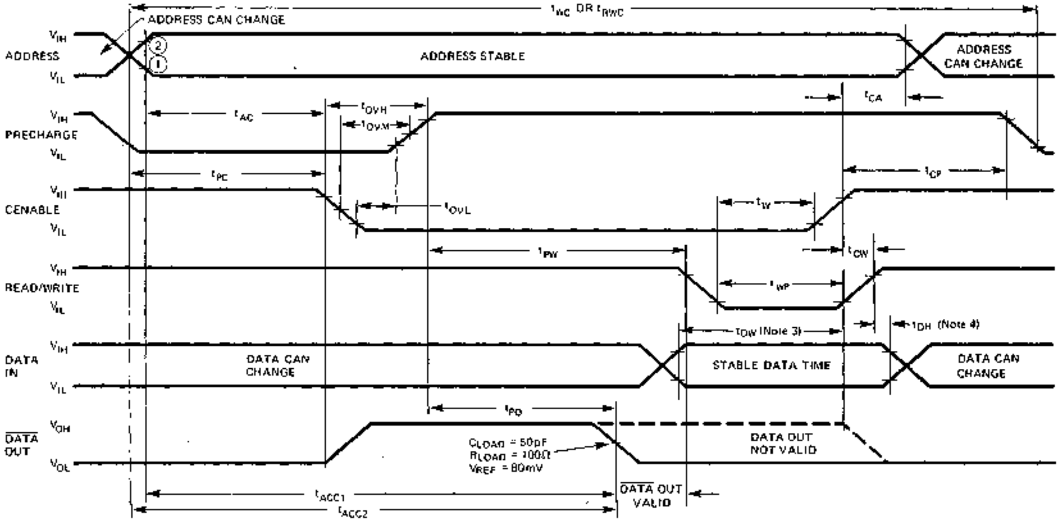
NOTE 1: These times will degrade by 35 nsec if a V_{REF} point of 40 mV is chosen instead of the 80 mV point defined in the spec.

*CAPACITANCE $T_A = 25°C$

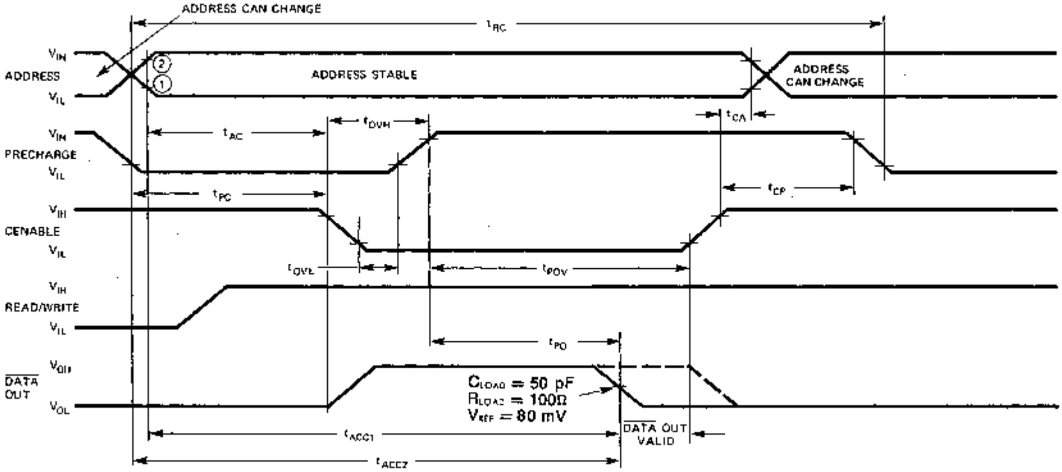
SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS	
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$	f = 1 MHz All Unused Pins Are At A.C. Ground
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$	
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$	
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$	
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V $V_{IN} = V_{SS}$	
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS} $V_{IN} = V_{SS}$	
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	$V_{OUT} = 0V$	

*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE OR READ/WRITE CYCLE



READ CYCLE



NOTE ① $V_{DD}+2V$ ⎤ t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS
NOTE ② $V_{SS}-2V$ ⎦
NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CHIP ENABLE OR READ/WRITE WHICHEVER OCCURS FIRST
NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CHIP ENABLE OR READ/WRITE WHICHEVER OCCURS FIRST

intel® Silicon Gate MOS 1103A

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- ✱No Precharge Required -- Critical Precharge Timing is Eliminated
- Electrically Equivalent to 1103 -- Pin-for-Pin/Functionally Compatible
- Fast Access Time -- 205ns max.
- Low Standby Power Dissipation -- 2 μW/Bit typical
- Address Registers Incorporated on the Chip
- Simple Memory Expansion -- Chip Enable Input Lead
- Inputs Protected -- All Inputs Have Protection Against Static Charge
- Ceramic and Plastic Package -- 18-Pin DIP

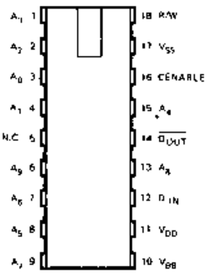
The 1103A is a 1024 word by 1 bit dynamic RAM. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives. The 1103A is electrically equivalent to the 1103.

1103A systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

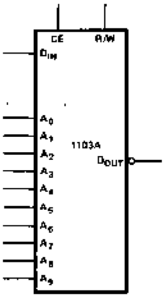
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every two milliseconds. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

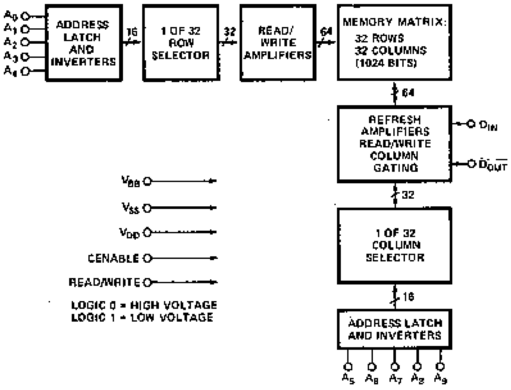
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

Absolute Maximum Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB}	−25V to 0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Power Dissipation	1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

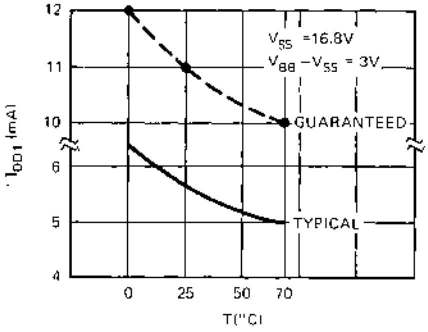
$T_A = 0°C$ to $+70°C$, V_{SS}[1] $= 16V \pm 5\%$, $(V_{BB} - V_{SS})$[2] $= 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified.

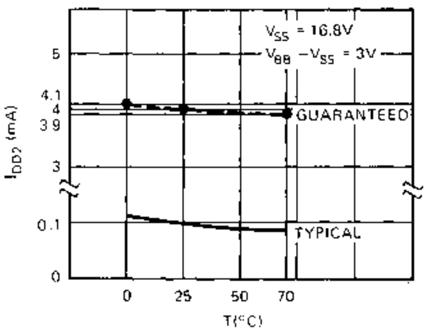
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions	
I_{LI}	Input Load Current (All Input Pins)			1	µA	$V_{IN} = 0V$	
I_{LO}	Output Leakage Current			1	µA	$V_{OUT} = 0V$	
I_{BB}	V_{BB} Supply Current			100	µA		
I_{DD1}	Supply Current During Cenable On		4	11	mA	Cenable = 0V; $T_A = 25°C$	
I_{DD2}	Supply Current During Cenable Off		0.1	4	mA	Cenable = V_{SS}; $T_A = 25°C$	
I_{DDAV}	Average Supply Current		17	25	mA	Cycle Time = 580ns; $T_A = 25°C$	
V_{IL}	Input Low Voltage	$V_{DD} - 1$		$V_{DD} + 1$	V		
V_{IH}	Input High Voltage	$V_{SS} - 1$		$V_{SS} + 1$	V		
I_{OH1}	Output High Current	600	1800	4000	µA	$T_A = 25°C$	R_{LOAD}[4] = 100Ω
I_{OH2}	Output High Current	500	1500	4000	µA	$T_A = 70°C$	
I_{OL}	Output Low Current		See Note Three				
V_{OH1}	Output High Voltage	60	180	400	mV	$T_A = 25°C$	
V_{OH2}	Output High Voltage	50	150	400	mV	$T_A = 70°C$	
V_{OL}	Output Low Voltage		See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1kΩ.

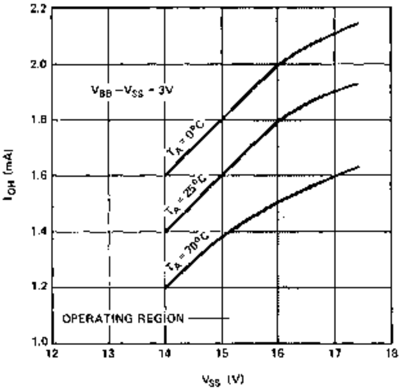
Supply Current vs Temperature



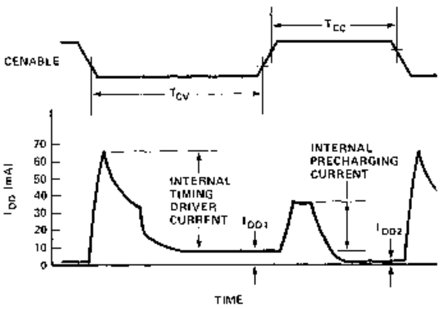


Typical Characteristics

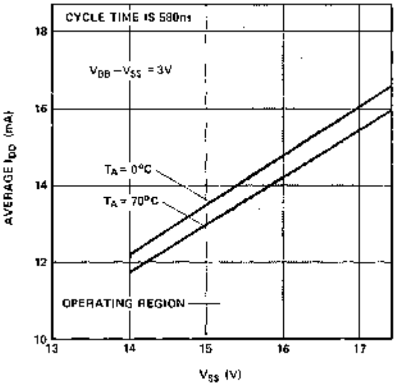
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



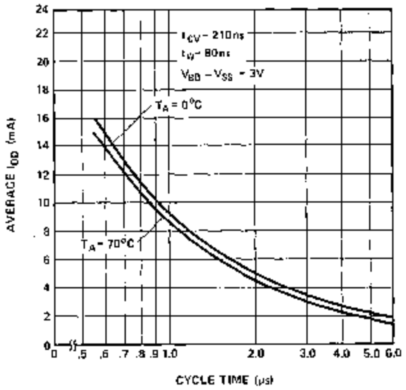
I_{DD} VS. CENABLE



AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. 1103A CYCLE TIME



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} = 16V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	230		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	480		ns	t_T = 20ns; C_{LOAD} = 100pF; R_{LOAD} = 100Ω; V_{REF} = 40mV
t_{CV}	Cenable on Time	210	500	ns	
t_{CO}	Cenable Output Delay		185	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		205	ns	$t_{ACC} = t_{AC\,MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	580		ns	t_T = 20ns
t_{RWC}	Read/Write Cycle	580		ns	
t_{CW}	Cenable to Read/Write Delay	210	500	ns	
t_{WP}	Read/Write Pulse Width	50		ns	
t_W	Read/Write Set Up Time	80		ns	
t_{DW}	Data Set Up Time	105		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		185	ns	C_{LOAD} = 100pF; R_{LOAD} = 100Ω V_{REF} = 40mV
t_{WC}	Read/Write to Cenable	0		ns	

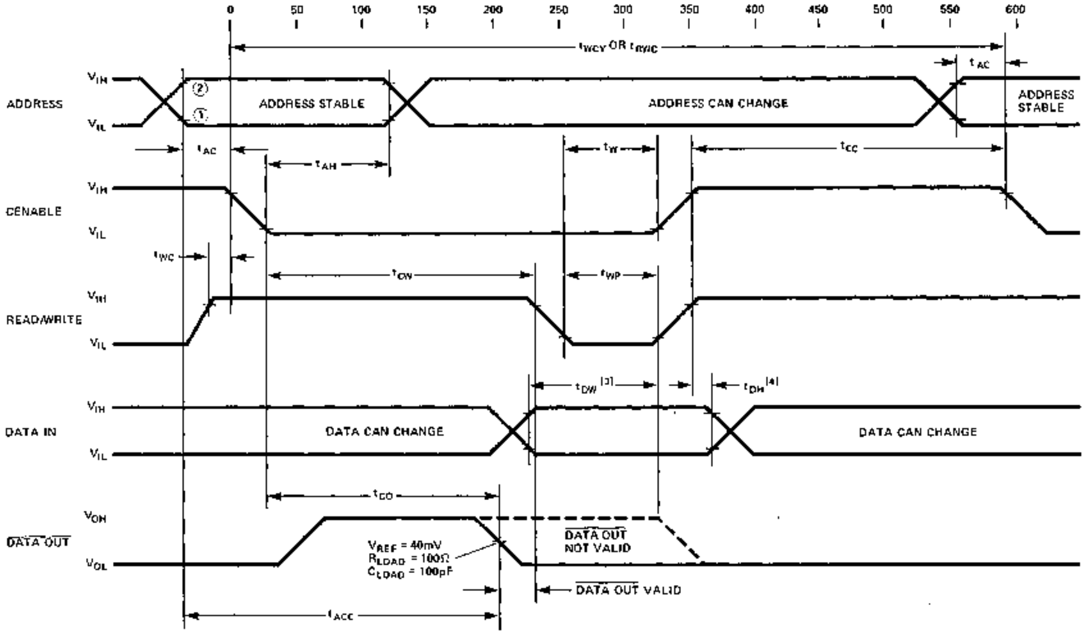
CAPACITANCE[1] $T_A = 25°C$

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions	
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$	f = 1MHz. All unused pins are at A.C. ground.
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$	
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$	
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V $V_{IN} = V_{SS}$	
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}	
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$ V_{OUT} = 0V	

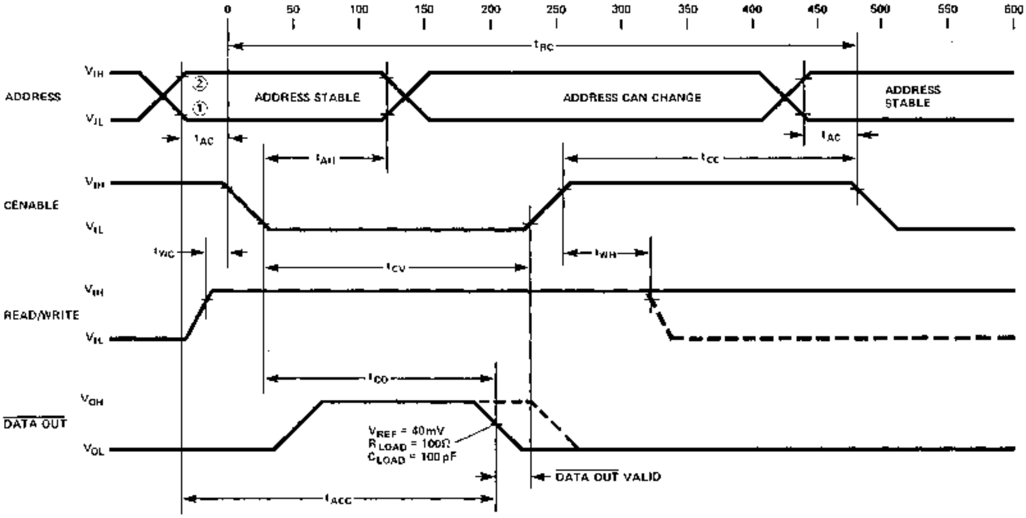
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTES:

① $V_{DD} + 2V$ ⎤
② $V_{SS} - 2V$ ⎦ t_T is defined as the transition between these two points.

3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

intel® Silicon Gate MOS **1103A-1**

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- **High Speed 1103A — Access Time — 145ns/Cycle Time—340ns**

✻ **No Precharge Required -- Critical Precharge Timing is Eliminated**

- **Low Standby Power Dissipation -- 0.2 μW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

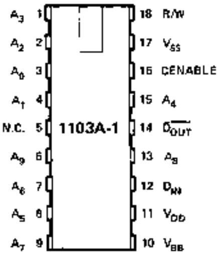
The Intel®1103A-1 is a high speed 1024 bit dynamic random access memory and is the fastest version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-1 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

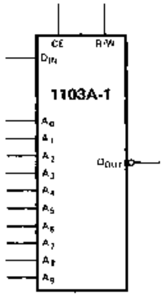
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-1 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



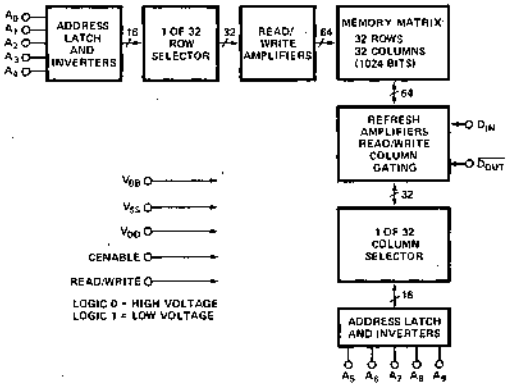
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB}	−25V to 0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Power Dissipation	1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

$T_A = 0°C$ to $+55°C$, V_{SS}[1] = 19V ± 5%, $(V_{BB} - V_{SS})$[2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	µA	V_{IN} = 0V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	µA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		25	33	mA	Cycle Time = 340ns; T_A = 25°C
V_{IL}	Input Low Voltage	$V_{DD}-1$		$V_{DD}+1$	V	
V_{IH}	Input High Voltage	$V_{SS}-1$		$V_{SS}+1$	V	
I_{OH1}	Output High Current	1150	1800	7000	µA	T_A = 25°C
I_{OH2}	Output High Current	900	1600	7000	µA	T_A = 55°C
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] = 100Ω
V_{OH1}	Output High Voltage	115	180	700	mV	T_A = 25°C
V_{OH2}	Output High Voltage	90	160	700	mV	T_A = 55°C
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics T_A = 0°C to 55°C, V_{SS} = 19V ±5%, (V_{BB} − V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V.

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	120		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	300		ns	t_T = 20ns C_{LOAD} = 50pF R_{LOAD} = 100Ω V_{REF} = 80mV
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\,MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

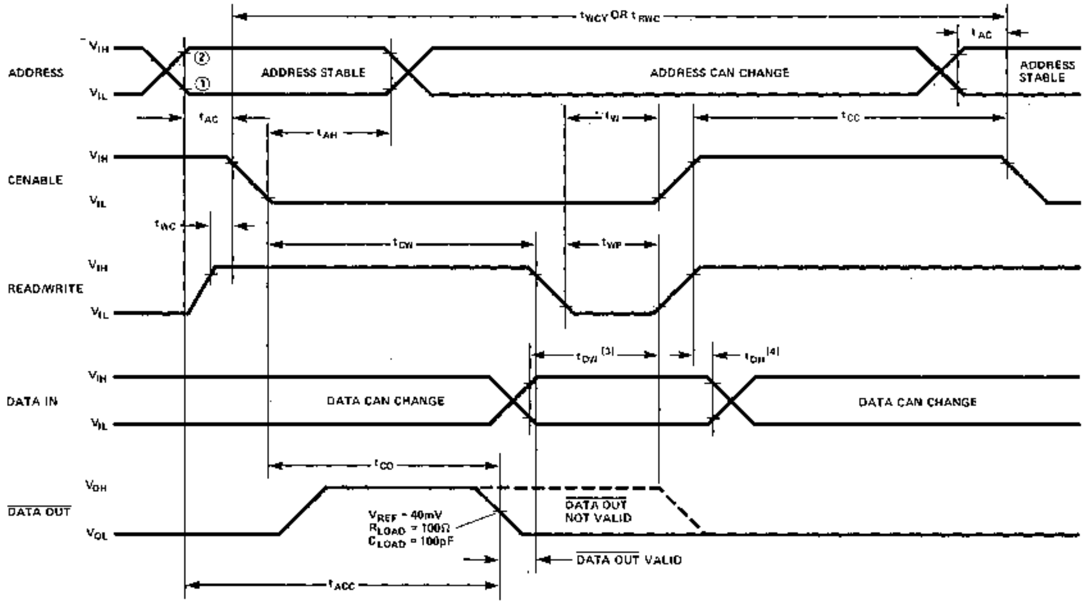
Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	340		ns	t_T = 20ns
t_{RWC}	Read/Write Cycle	340		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	C_{LOAD} = 50pF; R_{LOAD} = 100Ω V_{REF} = 80mV
t_{WC}	Read/Write to Cenable	0		ns	

CAPACITANCE[1] T_A = 25°C

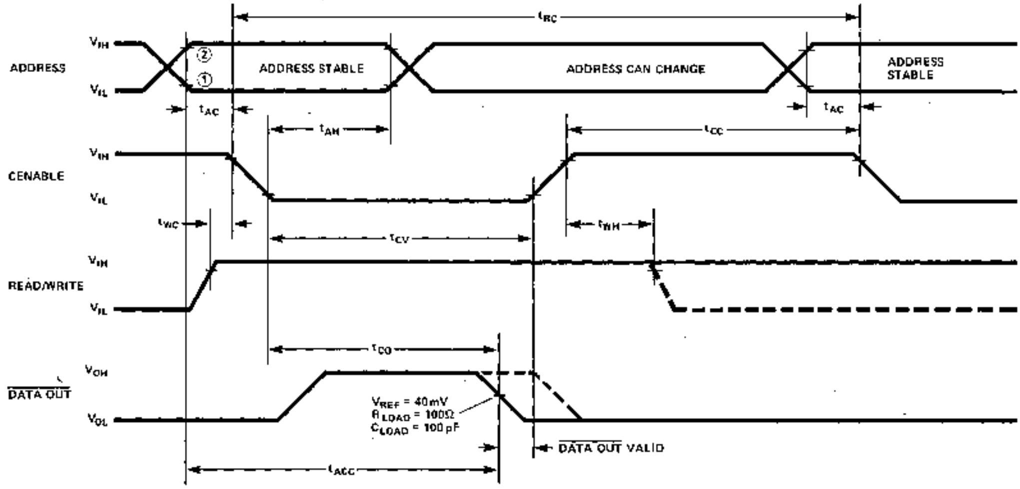
Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions	
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$	f = 1MHz. All unused pins are at A.C. ground.
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$	
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$	
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V $V_{IN} = V_{SS}$	
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}	
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$ V_{OUT} = 0V	

NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE



READ CYCLE

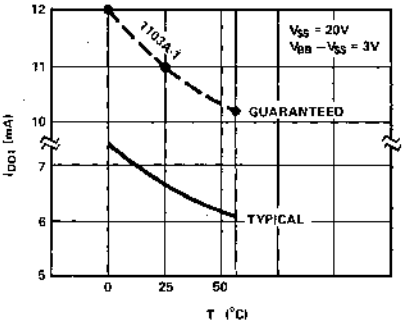


NOTES:

① $V_{DD} + 2V$
② $V_{SS} - 2V$ } t_T is defined as the transition between these two points.

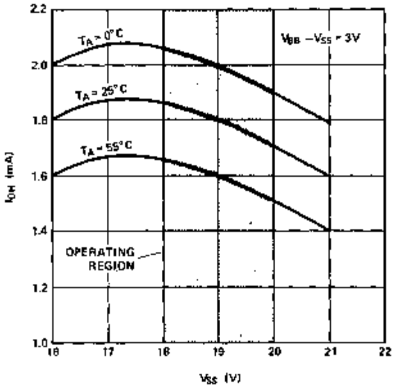
3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

Supply Current vs Temperature

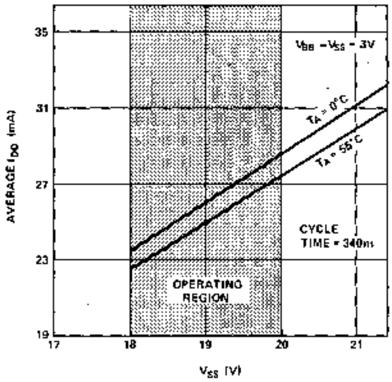


Typical Characteristics

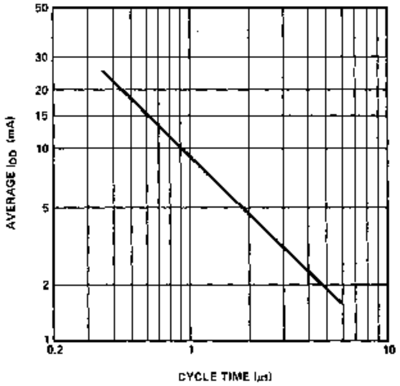
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



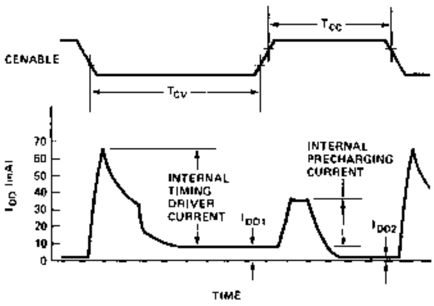
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



intel® Silicon Gate MOS **1103A-2**

FULLY DECODED RANDOM ACCESS 1024 BIT DYNAMIC MEMORY

- **High Speed 1103A – Access Time – 145ns/Cycle Time – 400ns**

✻No Precharge Required -- Critical Precharge Timing is Eliminated

- **Low Standby Power Dissipation -- 0.2 μW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

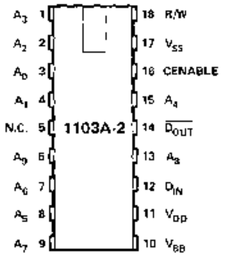
The Intel®1130A-2 is a high speed 1024 bit dynamic random access memory and is the 400ns cycle time version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-2 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

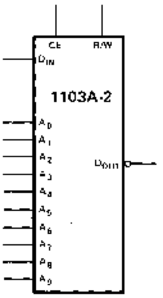
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-2 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



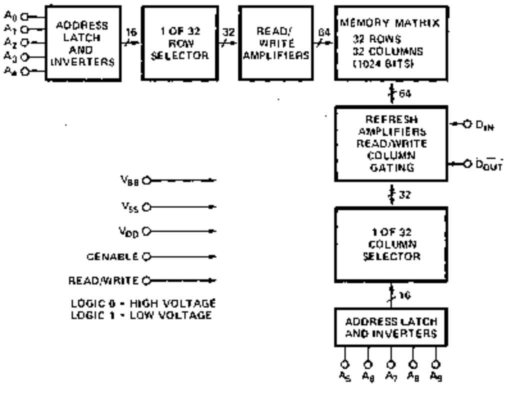
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 70°C

Storage Temperature . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . −25V to 0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to + 55°C, V_{SS}[1] = 19V ± 5%, (V_{BB} − V_{SS})[2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions	
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0V	
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V	
I_{BB}	V_{BB} Supply Current			100	μA		
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; T_A = 25°C	
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; T_A = 25°C	
I_{DDAV}	Average Supply Current		22	30	mA	Cycle Time = 400ns; T_A = 25°C	
V_{IL}	Input Low Voltage	V_{DD} −1		V_{DD} +1	V		
V_{IH}	Input High Voltage	V_{SS} −1		V_{SS} +1	V		
I_{OH1}	Output High Current	1150	1800	7000	μA	T_A = 25°C	R_{LOAD}[4] = 100Ω
I_{OH2}	Output High Current	900	1600	7000	μA	T_A = 55°C	
I_{OL}	Output Low Current		See Note Three				
V_{OH1}	Output High Voltage	115	180	700	mV	T_A = 25°C	
V_{OH2}	Output High Voltage	90	160	700	mV	T_A = 55°C	
V_{OL}	Output Low Voltage		See Note Three				

NOTES:

1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. (V_{BB} −V_{SS}) supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics $T_A = 0°C$ to $55°C$, $V_{SS} = 19V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$.

READ, WRITE, AND READ/WRITE CYCLE

Refer to page 2-23 for definitions.

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	180		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions	
t_{RC}	Read Cycle	360		ns	$t_T = 20ns$	$C_{LOAD} = 50pF$ $R_{LOAD} = 100\Omega$ $V_{REF} = 80mV$
t_{CV}	Cenable on Time	140	500	ns		
t_{CO}	Cenable Output Delay		125	ns		
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\,MIN} + t_{CO} + t_T$	
t_{WH}	Read/Write Hold Time	30		ns		

WRITE OR READ/WRITE CYCLE

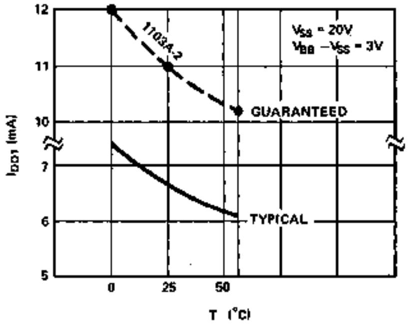
Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	400		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	400		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	$C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$ $V_{REF} = 80mV$
t_{WC}	Read/Write to Cenable	0		ns	

CAPACITANCE[1] $T_A = 25°C$

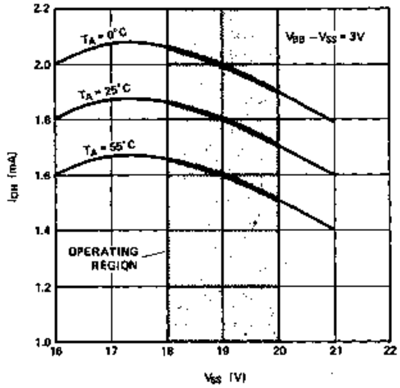
Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions	
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$	f = 1MHz. All unused pins are at A.C. ground.
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$	
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$	
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V $V_{IN} = V_{SS}$	
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}	
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$ $V_{OUT} = 0V$	

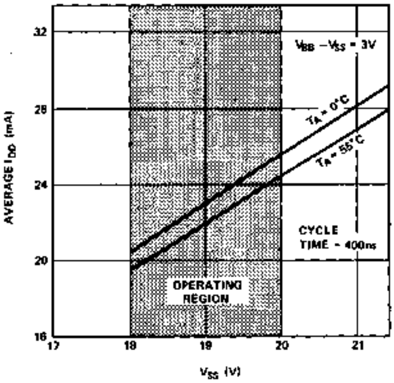
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

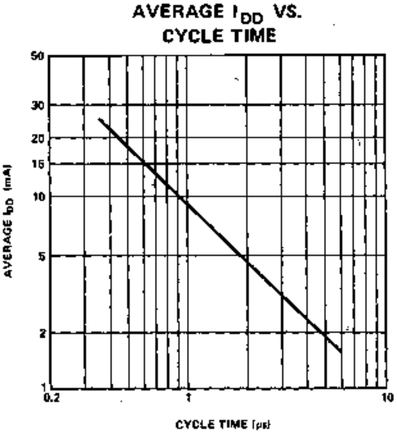
Supply Current vs Temperature

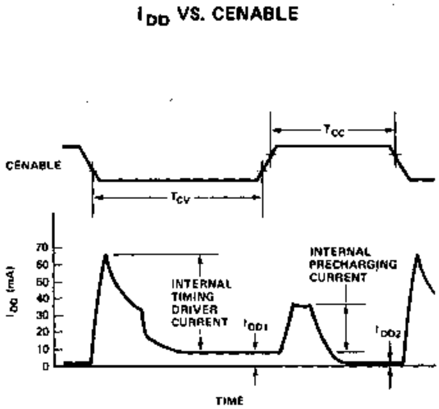


Typical Characteristics









intel® Silicon Gate MOS 2101, 2101-1, 2101-2

1024 BIT (256 x 4) STATIC MOS RAM WITH SEPARATE I/O

- **256 x 4 Organization to Meet Needs for Small System Memories**
- **Access Time — 0.5 to 1 μsec Max.**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Simple Memory Expansion — Chip Enable Input**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel®2101 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

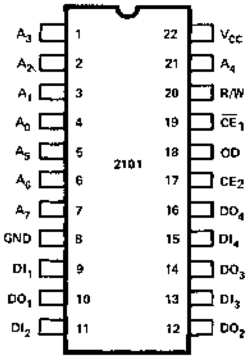
The 2101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system.

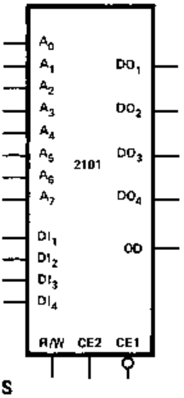
The Intel 2101 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



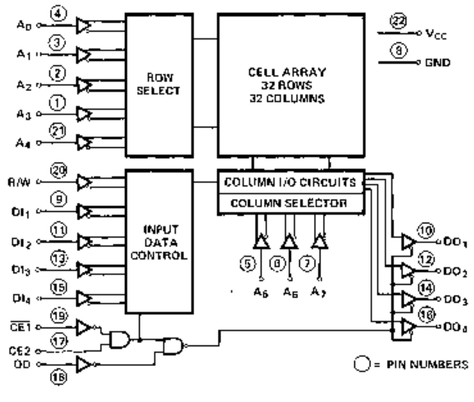
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . . 0°C to 70°C

Storage Temperature . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . -0.5V to +7V

Power Dissipation . . . . 1 Watt

**COMMENT:*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

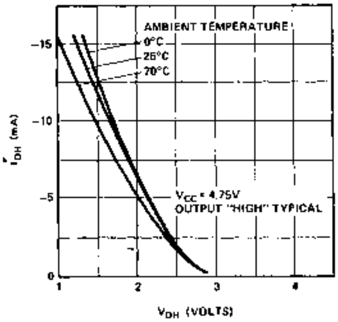
D.C. and Operating Characteristics for 2101, 2101-1, 2101-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

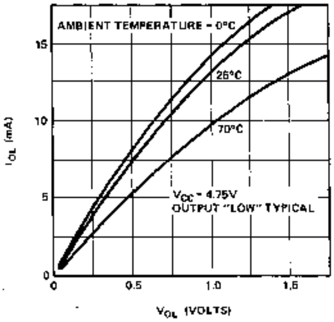
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150 μA

Typical D. C. Characteristics

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. Characteristics for 2101

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			1,000	ns	
t_{CO}	Chip Enable To Output			800	ns	
t_{OD}	Output Disable To Output			700	ns	
t_{DF}[3]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	900			ns	
t_{DW}	Data Setup	700			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	750			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	200			ns	

A. C. CONDITIONS OF TEST

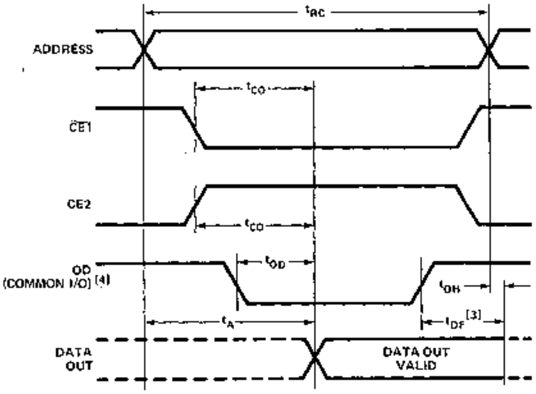
Input Pulse Levels:	+0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100pF

Capacitance[2] $T_A = 25°C$, f = 1MHz

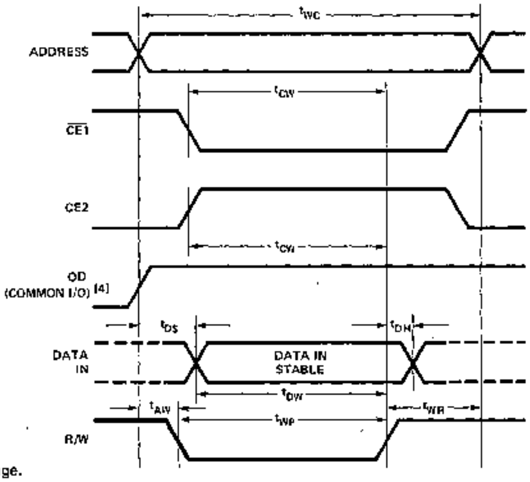
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101-1 (500 ns Access Time)

A.C. Characteristics for 2101-1

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			500	ns	
t_{CO}	Chip Enable To Output			350	ns	
t_{OD}	Output Disable To Output			300	ns	
t_{DF}[2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	100			ns	
t_{CW}	Chip Enable To Write	400			ns	
t_{DW}	Data Setup	280			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	300			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

2101-2 (650 ns Access Time)

A.C. Characteristics for 2101-2

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			650	ns	
t_{CO}	Chip Enable To Output			400	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}[2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.

intel® Silicon Gate MOS 2102

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Low Power — Typically 150 mW**
- **Access Time — Typically 500 nsec**
- **Three-State Output — OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**

The Intel® 2102 is a 1024 word by one bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

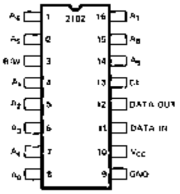
The 2102 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

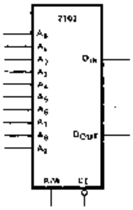
The Intel 2102 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



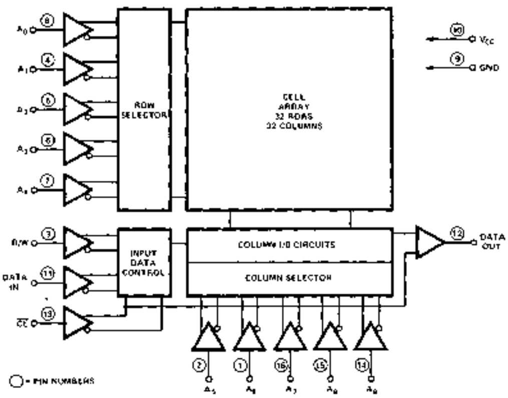
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CE}$	CHIP ENABLE
$A_0 - A_9$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

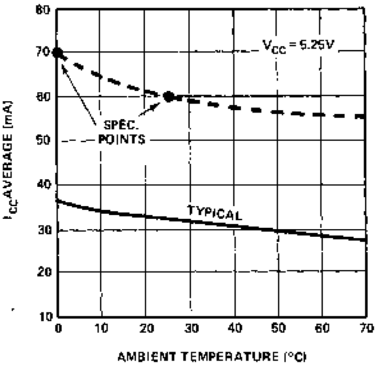
D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

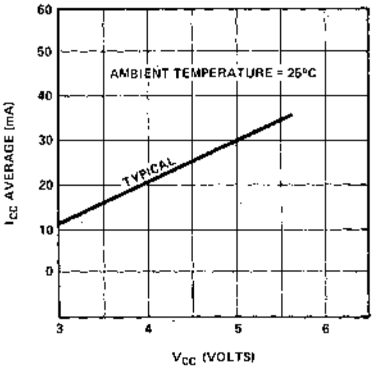
SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.[1]	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	OUTPUT LEAKAGE CURRENT			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 0°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.2		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 1.9mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	I_{OH} = −100μA

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS MIN.	TYP.[1]	MAX.	UNIT
READ CYCLE					
t_{RC}	READ CYCLE	1000			ns
t_A	ACCESS TIME		500	1000	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			500	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	1000			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	200			ns
t_{WP}	WRITE PULSE WIDTH	750			ns
t_{WR}	WRITE RECOVERY TIME	50			ns
t_{DW}	DATA SETUP TIME	800			ns
t_{DH}	DATA HOLD TIME	100			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	900			ns

A. C. CONDITIONS OF TEST

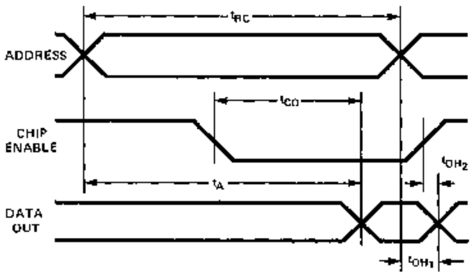
Input Pulse Levels:	+0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

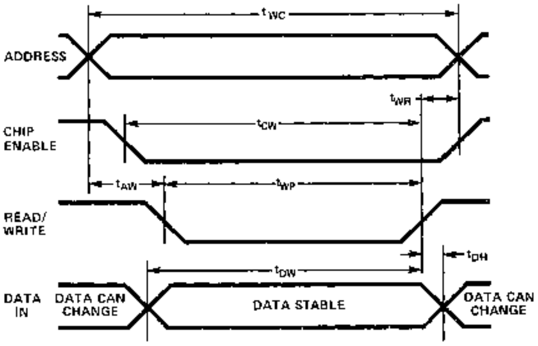
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



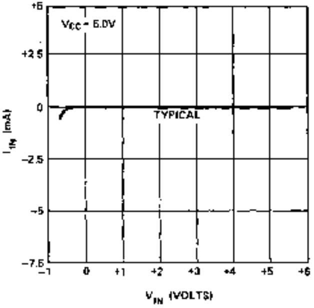
WRITE CYCLE



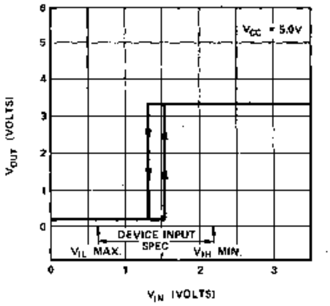
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. Characteristics

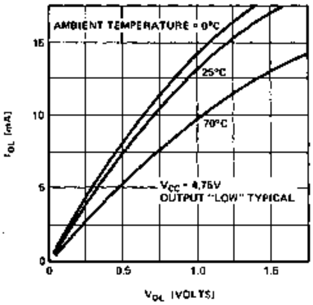
INPUT CURRENT VS.
INPUT VOLTAGE



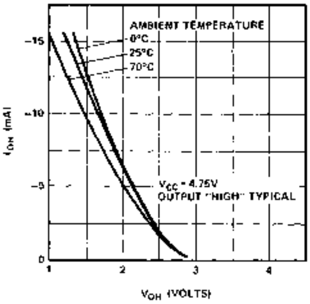
EFFECTIVE INPUT
CHARACTERISTIC



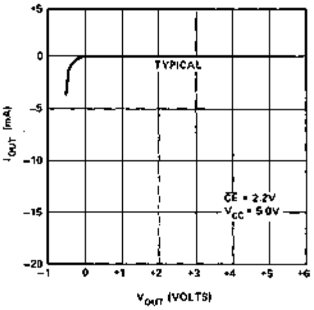
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



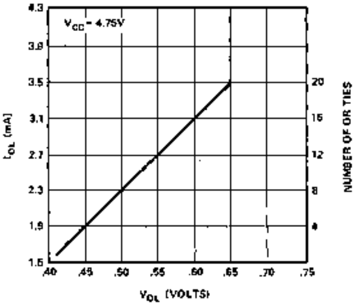
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT
VOLTAGE WITH CHIP DISABLED

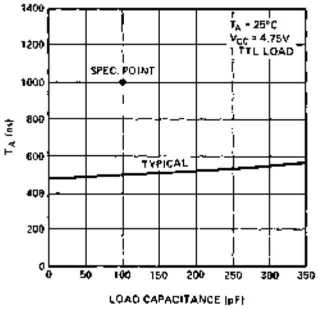


RELATIONSHIP BETWEEN OUTPUT
SINK CURRENT, NUMBER OF OR-TIES,
AND OUTPUT VOLTAGE

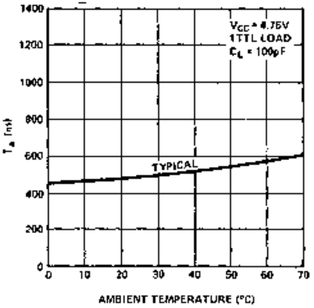


Typical A. C. Characteristics

ACCESS TIME VS.
LOAD CAPACITANCE



ACCESS TIME VS.
AMBIENT TEMPERATURE



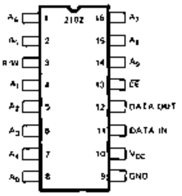
intel® Silicon Gate MOS **2102-1**

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

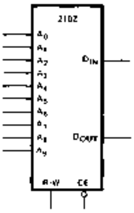
- ***Fast Access Time -- 500 ns max.**
- **Fast Cycle Time -- 500 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel®2102-1 is the fastest (500ns) version of the standard one microsecond 2102. It has all the same features, pin configuration, and D.C. operating characteristics as the standard 2102. The absolute maximum ratings, pin configuration, and D.C. operating characteristics are repeated below for convenience, while the A.C. characteristics appear on the opposite side.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.[1]	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	µA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	OUTPUT LEAKAGE CURRENT			−100	µA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 0°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.2		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 1.9mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	I_{OH} = −100µA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.[1]	MAX.	
READ CYCLE					
t_{RC}	READ CYCLE	500			ns
t_A	ACCESS TIME			500	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			350	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	500			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	150			ns
t_{WP}	WRITE PULSE WIDTH	300			ns
t_{WR}	WRITE RECOVERY TIME	50			ns
t_{DW}	DATA SETUP TIME	330			ns
t_{DH}	DATA HOLD TIME	100			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	400			ns

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

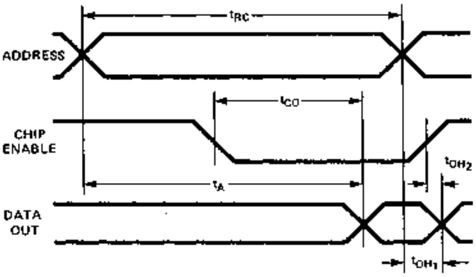
Output Load: 1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1 MHz

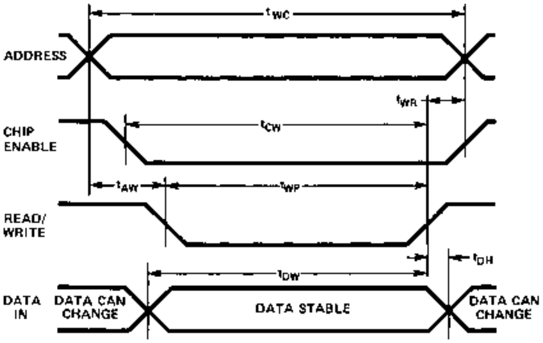
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

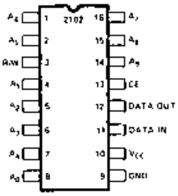
intel® Silicon Gate MOS 2102-2

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

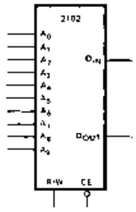
- **Fast Access Time -- 650 ns max.**
- **Fast Cycle Time -- 650 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel® 2102-2 is a fast (650ns) version of the standard one microsecond 2102. It has all the same features, pin configuration, and D.C. operating characteristics as the standard 2102. The absolute maximum ratings, pin configuration, and D.C. operating characteristics are repeated below for convenience, while the A.C. characteristics appear on the opposite side.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature .... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground .... −0.5V to +7V
Power Dissipation .... 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS MIN.	TYP.[1]	MAX.	UNIT	TEST CONDITIONS
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	OUTPUT LEAKAGE CURRENT			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 0°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.2		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 1.9mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	I_{OH} = −100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.[1]	LIMITS MAX.	UNIT
READ CYCLE					
t_{RC}	READ CYCLE	650			ns
t_A	ACCESS TIME			650	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			400	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	650			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	200			ns
t_{WP}	WRITE PULSE WIDTH	400			ns
t_{WR}	WRITE RECOVERY TIME	50			ns
t_{DW}	DATA SETUP TIME	450			ns
t_{DH}	DATA HOLD TIME	100			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	550			ns

A.C. CONDITIONS OF TEST

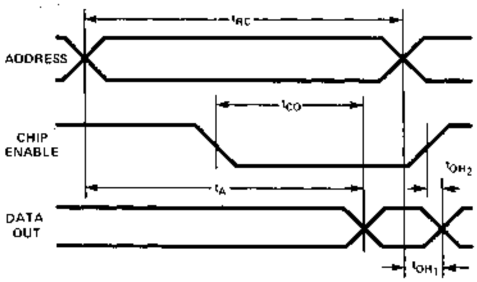
Input Pulse Levels:	+0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

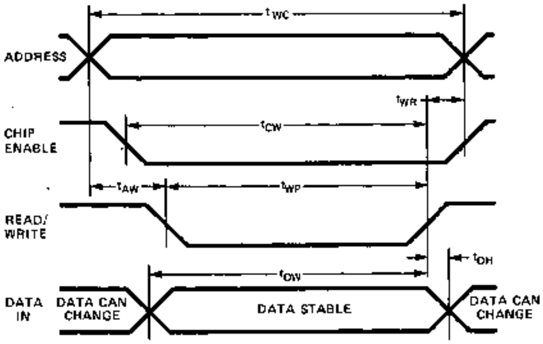
SYMBOL	TEST	LIMITS (pF) TYP.[1]	LIMITS (pF) MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

intel® Silicon Gate MOS **2102-8**

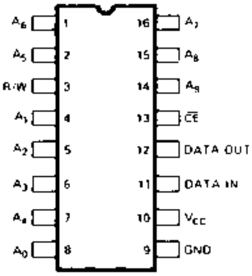
1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- **Access Time--1.5 µs max.**
- **Cycle Time--2.0 µs max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel®2102-8 is a 1.5µs version of the standard 2102. It has all the same features, and pin configuration as the standard 2102. The absolute maximum ratings, and pin configuration are repeated below for convenience, while the D.C. operating characteristics and A.C. characteristics appear as follows.

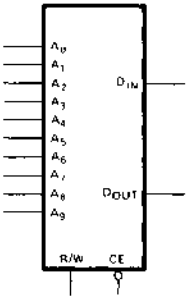
PIN CONFIGURATION

2102-8



LOGIC SYMBOL

2102-8



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 15°C to +55°C
Storage Temperature . . . . –65° C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . –0.5V to +7V
Power Dissipation . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 15°C to +55°C, V_{CC} = 5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.[1]	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	µA	$\overline{CE}$ = 3.0V, V_{OUT} = 4.0V
I_{LOL}	OUTPUT LEAKAGE CURRENT			–100	µA	$\overline{CE}$ = 3.0V, V_{OUT} = 0.5V
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 15°C
V_{IL}	INPUT "LOW" VOLTAGE	–0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	3.0		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			0.5	V	I_{OL} = 1.5mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	I_{OH} = -50µA

(1) Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = 15°C to 55°C, V_{CC} = 5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.[1]	MAX.	
READ CYCLE					
t_{RC}	READ CYCLE	2000			ns
t_A	ACCESS TIME			1500	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			1500	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	0			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	2000			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	900			ns
t_{WP}	WRITE PULSE WIDTH	1000			ns
t_{WR}	WRITE RECOVERY TIME	100			ns
t_{DW}	DATA SETUP TIME	1600			ns
t_{DH}	DATA HOLD TIME	300			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	1800			ns

A. C. CONDITIONS OF TEST

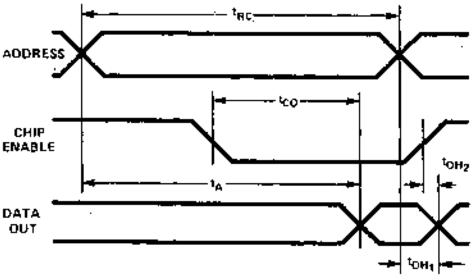
Input Pulse Levels:	+0.65 Volt to 3.0 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

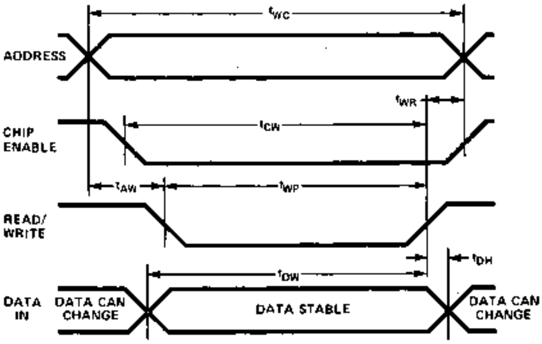
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

*Fast Access Time -- 350 ns max.

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**

The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (order as a 2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 42 mW maximum power dissipation in standby.*

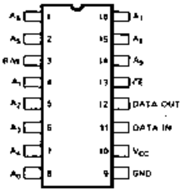
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

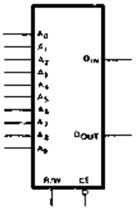
PIN CONFIGURATION

2102A



LOGIC SYMBOL

2102A



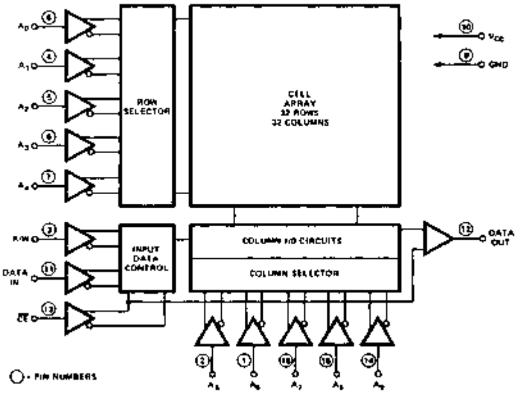
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

ORDERING INFORMATION

Maximum T_{ACC} & T_{CYC}	Standard Part No.	Standby-Mode Part No.
350ns	2102A	2102AL
250ns	2102A-2	2102AL-2
450ns	2102A-4	2102AL-4

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to + 70°C, V_{CC} = 5V ±5% unless otherwise specified.

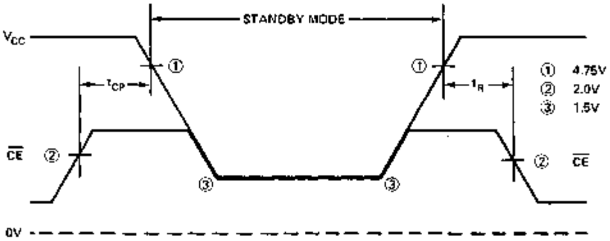
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}	Power Supply Current		30	60	mA	All Inputs = 5.25V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100μA

Standby Characteristics – See Ordering Information on Previous Page

T_A = 0°C to 70°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
V_{PD}	V_{CC} in Standby	1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			V	2.0V ≤ V_{PD} ≤ V_{CC} Max.
		V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
I_{PD1}	Standby Current Drain		15	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current Drain		20	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			ns	
t_R [3]	Standby Recovery Time	t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME).

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	350			ns
t_A	Access Time			350	ns
t_{CO}	Chip Enable to Output Time			180	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	350			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	250			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	250			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	250			ns

A. C. CONDITIONS OF TEST

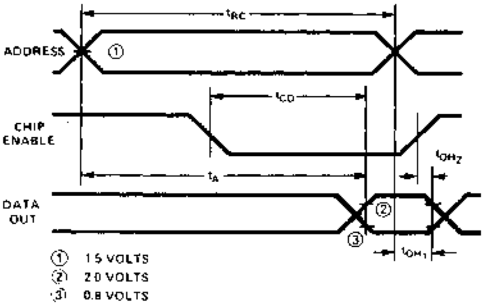
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

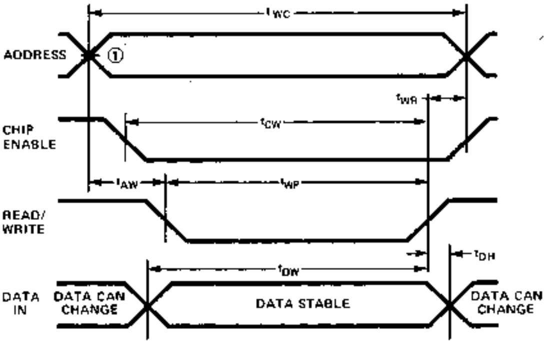
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



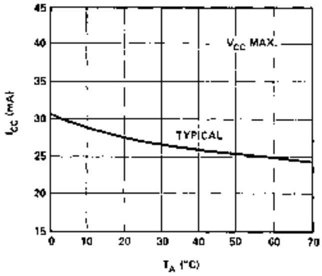
WRITE CYCLE



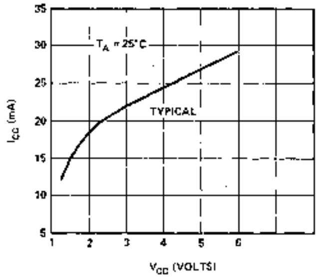
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

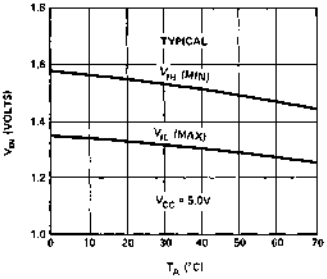
POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



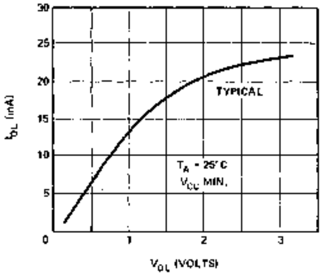
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



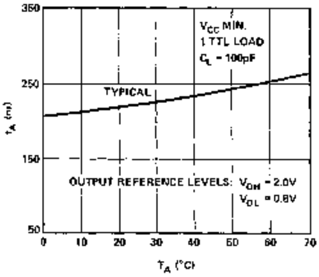
V_{IN} LIMITS VS. TEMPERATURE



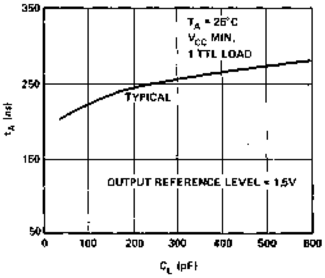
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



intel® Silicon Gate MOS 2102A-2 , 2102AL-2

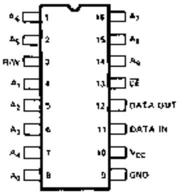
1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- ✻**Fast Access Time -- 250 ns max.**
- **Fast Cycle Time -- 250 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel® 2102A-2 is a faster (250ns) version of the standard 2102A. It has all the same features, pin configuration, and D.C. operating characteristics as the standard 2102A. The absolute maximum ratings, pin configuration, and D.C. operating characteristics are repeated below for convenience, while the A.C. characteristics appear on the opposite side. *A low standby power version (order as a 2102AL-2) is also available. It has all the same operating characteristics of the 2102A-2 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)*

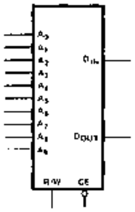
PIN CONFIGURATION

2102A-2



LOGIC SYMBOL

2102A-2



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	µA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	µA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}[2]	Power Supply Current		30	60	mA	All Inputs = 5.25V, Data Out Open, T_A = 25°C
I_{CC2}[2]	Power Supply Current			70	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100µA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

2. A low standby power version (order as a 2102AL-2) is also available. It has all the same operating characteristics of the 2102A-2 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
READ CYCLE					
t_{RC}	Read Cycle	250			ns
t_A	Access Time			250	ns
t_{CO}	Chip Enable to Output Time			130	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	250			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	180			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	180			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	180			ns

A.C. CONDITIONS OF TEST

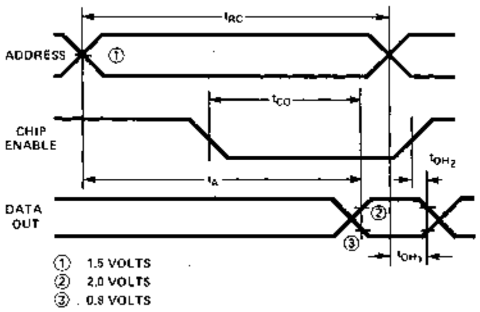
Input Pulse Levels: 0.8 Volt to 2.0 Volt
Input Rise and Fall Times: 10nsec
Timing Measurement Reference Levels Inputs: 1.5 Volts
Output: 0.8 and 2.0 Volts
Output Load: 1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

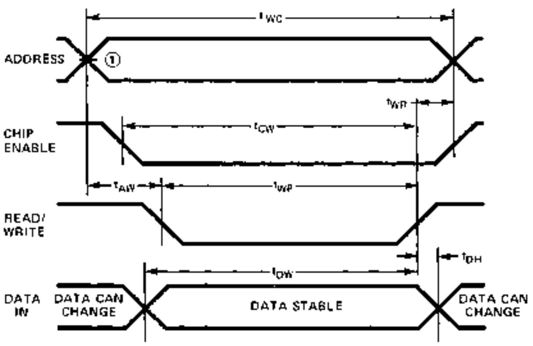
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

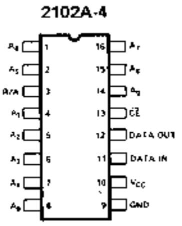
intel® Silicon Gate MOS 2102A-4, 2102AL-4

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

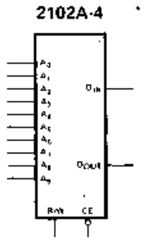
- **Fast Access Time -- 450 ns max.**
- **Fast Cycle Time -- 450 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel® 2102A-4 is a 450ns version of the standard 2102A. It has all the same features, pin configuration, and D.C. operating characteristics as the standard 2102A. The absolute maximum ratings, pin configuration, and D.C. operating characteristics are repeated below for convenience, while the A.C. characteristics appear on the opposite side. *A low standby power version (order as a 2102AL-4) is also available. It has all the same operating characteristics of the 2101A-4 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)*

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}[2]	Power Supply Current		30	60	mA	All Inputs = 5.25V, Data Out Open, T_A = 25°C
I_{CC2}[2]	Power Supply Current			70	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

2. A low standby power version (order as a 2102AL-4) is also available. It has all the same operating characteristics of the 2101A-4 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

A. C. CONDITIONS OF TEST

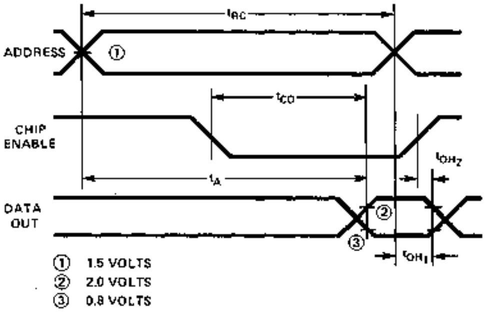
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

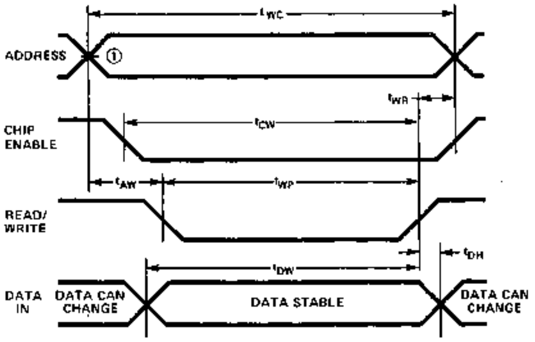
SYMBOL	TEST	LIMITS (pF) TYP.[1]	LIMITS (pF) MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

intel® Silicon Gate MOS **M2102A-4**

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

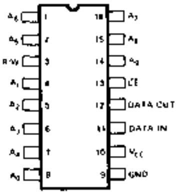
*Expanded Temperature Range–$T_A = -55°C$ to $+125°C$

- *Fast Access Time -- 450 ns max.
- Fast Cycle Time -- 450 ns max.
- N-Channel Silicon Gate
- Maximum Times Apply over Temperature Range and Supply Voltage Variation

The Intel® M2102A-4 is an expanded temperature range 1024 bit static N-channel MOS RAM. It is capable of operating over the full temperature range from −55°C to +125°C, and in addition the single 5 volt power supply can have a tolerance of ± 10%. The access time of the M2102A-4 is 450 nsec.

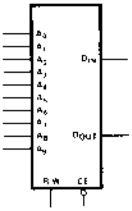
PIN CONFIGURATION

M2102A-4



LOGIC SYMBOL

M2102A-4



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	-55°C to +125°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output Leakage Current			10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.2 to V_{CC}
I_{LOL}	Output Leakage Current			-50	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	All Inputs = 5.5V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	All Inputs = 5.5V, Data Out Open; T_A = −55°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

A. C. CONDITIONS OF TEST

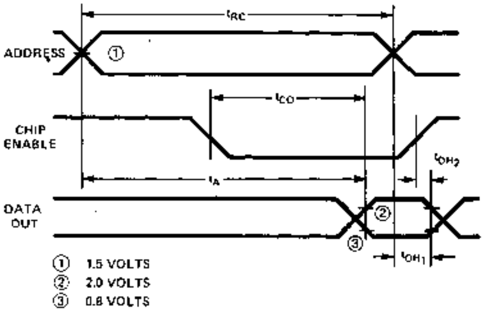
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

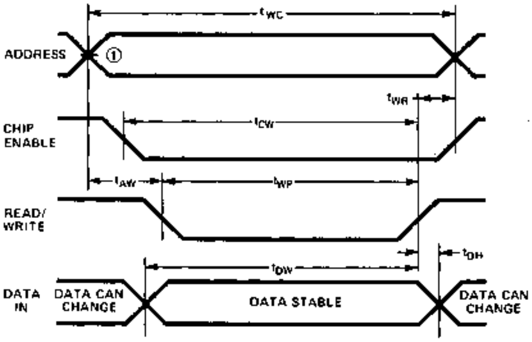
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

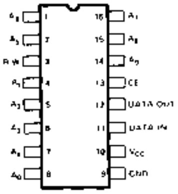
* Expanded Temperature Range: −55°C to +125°C

- **Fast Access Time--650 ns max.**
- **Fast Cycle Time--650 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel® M2102A-6 is an expanded temperature range 1024 bit static N-channel MOS RAM. It is capable of operating over the full temperature range from −55°C to +125°C, and in addition the single 5 volt power supply can have a tolerance of ± 10%. The access time of the M2102A-6 is 650 nsec.

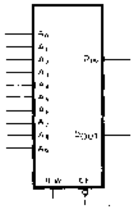
PIN CONFIGURATION

M2102A-6



LOGIC SYMBOL

M2102A-6



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . -55°C to +125°C
Storage Temperature . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . −0.5V to +7V
Power Dissipation . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	OUTPUT LEAKAGE CURRENT			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.5V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.5V DATA OUT OPEN T_A = −55°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.2		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 1.9mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	I_{OH} = −100μA

(1) Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.[1]	MAX.	
READ CYCLE					
t_{RC}	READ CYCLE	650			ns
t_A	ACCESS TIME			650	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			400	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	650			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	200			ns
t_{WP}	WRITE PULSE WIDTH	400			ns
t_{WR}	WRITE RECOVERY TIME	50			ns
t_{DW}	DATA SETUP TIME	450			ns
t_{DH}	DATA HOLD TIME	100			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	550			ns

A.C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

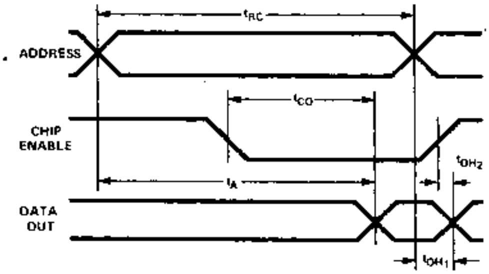
Output Load: 1 TTL Gate and C_L = 100 pF

Capacitance [2] T_A = 25°C, f = 1MHz

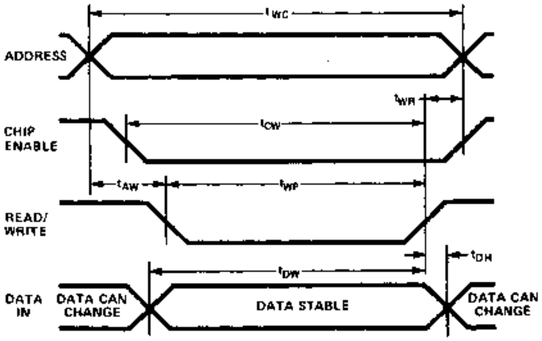
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

intel® Silicon Gate MOS 2105, 2105-1

1024 BIT HIGH SPEED DYNAMIC MOS RANDOM ACCESS MEMORIES

- **High Speed N-Channel— 80 ns Maximum Access Time 2105-1**
  95 ns Maximum Access Time 2105
- **Cycle Times:**
  260 ns Maximum for 2105-1
  270 ns Maximum for 2105
- **Planar Refresh**
- **Standby Power—100 μW/Bit**
- **Fully Decoded—On Chip Address Decode**
- **Low Level Address, Data, Write Enable Inputs**
- **Current Sinking Output**
- **OR-Tie Capability**
- **All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

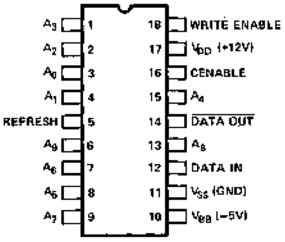
The Intel® 2105 and 2105-1 are very high speed 1024 word by one bit dynamic random access memories using normally off N-Channel MOS devices integrated on a monolithic array.

The 2105 and 2105-1 are designed for memory applications where very high speed, low cost, and low power dissipation are important design objectives. The planar refresh mode of operation simplifies system design and allows all 1024 memory cells to be refreshed at once.

The Intel 2105 and 2105-1 are fabricated with N-Channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-Channel silicon gate technology.

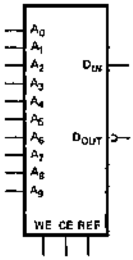
PIN CONFIGURATION

2105 & 2105-1



LOGIC SYMBOL

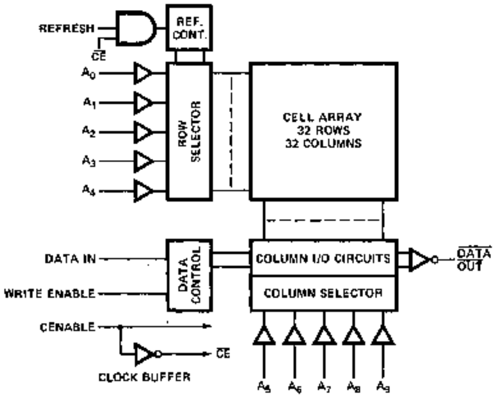
2105 & 2105-1



PIN NAMES

DIN	DATA INPUT	CE	CHIP ENABLE
A0-A9	ADDRESS INPUTS	REF	REFRESH INPUT
WE	WRITE ENABLE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB}	+25V to −0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	+20V to −0.3V
Power Dissipation	1.0W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$[3], $V_{SS} = 0V$[4], unless otherwise specified.[2]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (Address, D_{IN}, WE)			10	μA	$V_{IN} = 0V$ to $6.5V$
I_{LIC}	Input Load Current (CE, Ref)			10	μA	$V_{IN} = 0V$ to $V_{DD} + 0.5V$
I_{LO}	Output Leakage Current			1	μA	$V_O = 0V$
I_{DD1}	V_{DD} Current During Cenable ON		25	40	mA	$V_{CE} = 13.6V$, $V_{IN} = 0V$ to $4V$, $T_A = 25°C$
I_{DD2}	V_{DD} Current During Cenable OFF, Address High		13	20	mA	$V_{CE} = 0V$, $V_{IN} = 4V$, $T_A = 25°C$
I_{DDS}	Average Standby V_{DD} Current During Cenable OFF		3.0	6.0	mA	$V_{CE} = 0V$, $V_{IN} = 0V$, $T_A = 25°C$ $t_{REF} = 10\mu s$
$\lvert I_{BB1} \rvert$	V_{BB} Current During Cenable ON		5.5	10.5	mA	$V_{CE} = 13.6V$, $V_{IN} = 0V$ to $4V$, $D_{OUT} = 0V$, $T_A = 25°C$
$\lvert I_{BBS} \rvert$	Standby V_{BB} Current During Cenable OFF		2.5	5.0	mA	$V_{CE} = 0V$, $V_{IN} = 0V$ to $4V$, $D_{OUT} = 0V$, $t_{REF} = 10\mu s$, $T_A = 25°C$
$I_{DD\ AV}$	Average V_{DD} Supply Current		23	35	mA	$t_{cyc} = 270ns$, $t_{REF} = 10\mu s$, $T_A = 25°C$
			25*	39*	mA	$t_{cyc} = 260ns$, $t_{REF} = 10\mu s$, $T_A = 25°C$
$\lvert I_{BB\ AV} \rvert$	Average V_{BB} Supply Current		4.0	8.0	mA	$t_{cyc} = 270ns$, $t_{REF} = 10\mu s$, $T_A = 25°C$
			4.5*	9.0*	mA	$t_{cyc} = 260ns$, $t_{REF} = 10\mu s$, $T_A = 25°C$
V_{IL}	Input Low Level Voltage (All Inputs)	$V_{SS} - 1$		$V_{SS} + 1$	V	
V_{IH}	Input High Level Voltage (Address, D_{IN}, WE)	4.0		6.5	V	
V_{IHC}	Input High Level Voltage (CE, Ref)	$V_{DD} - 1$		$V_{DD} + 1$	V	
V_{OL}	Output Low Voltage			-150	mV	$R_L = 100\Omega$ at t_{CO}
V_{OH}	Output High Voltage	-80			mV	$R_L = 100\Omega$ at t_{CO}

NOTES:

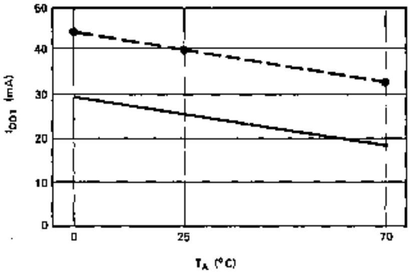
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.
3. The V_{BB} supply also may be equal to $-5.2V \pm 5\%$.
4. The current I_{SS} is $I_{DD} - I_{BB}$.

* These parameters refer to the 2105-1.

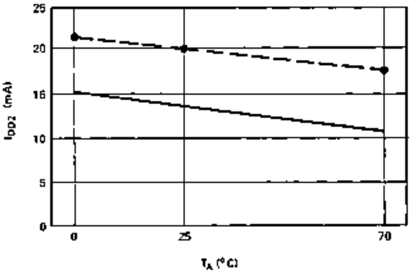
D.C. Characteristics

– – – – – GUARANTEED
——— TYPICAL

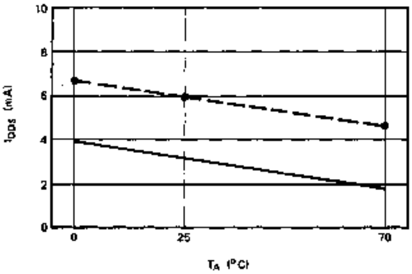
I_{DD1} VS. TEMPERATURE



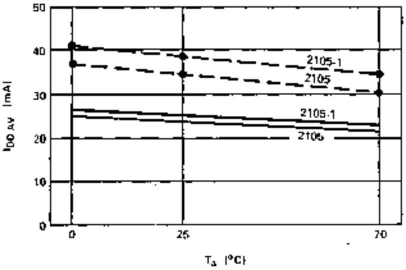
I_{DD2} VS. TEMPERATURE



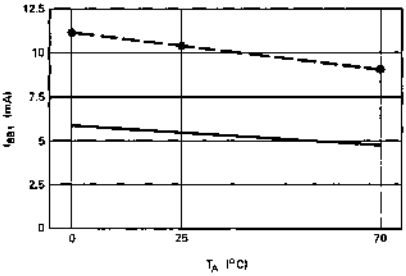
I_{DDS} VS. TEMPERATURE



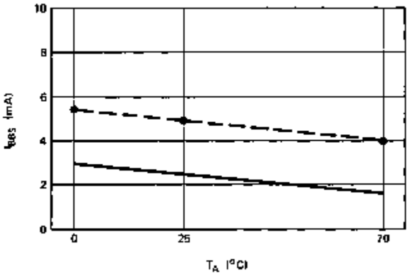
$I_{DD\ AV}$ VS. TEMPERATURE



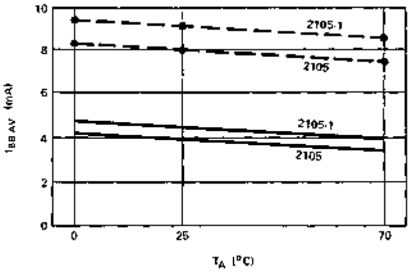
I_{BB1} VS. TEMPERATURE



I_{BBS} VS. TEMPERATURE



$I_{BB\ AV}$ VS. TEMPERATURE

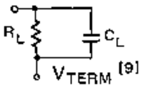


A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5.2V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.[1]

READ, WRITE, and READ MODIFY WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Planar Refresh Pulses	1	10	μs	
t_{AR}	Address Reset Time	Note 2		ns	
t_{AS+}[3][5]	High Address Setup Time	5		ns	
t_{AS-}[4][5]	Low Address Setup Time	35		ns	
t_{AH}	Address Hold Time	50		ns	
t_{CE}	Cenable On Time	90 80*	500 500*	ns ns	
t_{CC}	Cenable Off Time	150		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}[6]	Read Cycle	270 260*		ns ns	$t_T = 15ns$
t_{WS}	Write Enable to Cenable Setup Time	0		ns	
t_{CO}	Cenable Output Delay		75 60 ns*	ns ns	$C_{LOAD} = 50pF$ $R_{LOAD} = 100\Omega$ Refer to Note 8 
t_{ACC}[7]	Address to Output Access		95 80*	ns ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}[6]	Write Cycle	270 260		ns ns	$t_T = 15ns$
t_{WP}	Write Enable Pulse Width	70		ns	
t_{WC}	Write Enable to Cenable End	70	120	ns	
t_{DS}[10]	Data Setup Time	0		ns	
t_{DH}[11]	Data Hold Time	20		ns	

READ MODIFY WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[12]	Read Modify Write Cycle	340 330*		ns ns	$t_T = 15ns$
t_{CEM}[13]	Cenable On Time	160 150*	500 500*	ns ns	

PLANAR REFRESH TIMING

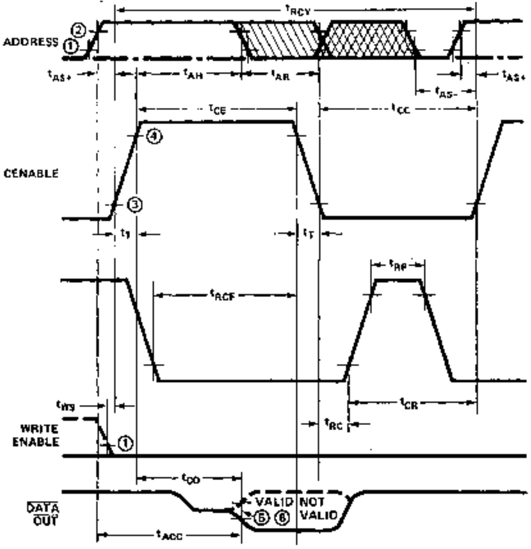
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CR}	Cenable to Refresh Start	50		ns	
t_{RCF}	Refresh to Cenable End	0		ns	
t_{RP}	Refresh Pulse Width	50	500	ns	
t_{RC}	Refresh to Cenable Start	90		ns	
t_{REF}	Time Between Planar Refresh	1	10	μs	

NOTES: 1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}. 2. t_{AR} is defined as $t_{CE} + t_T - t_{AH}$. During t_{AR} addresses may only be reset low or remain stable. Addresses may change after the start of t_{CC} and before the start of t_{AS-}. 3. High addresses must be stable by the start of t_{AS+} time. 4. Low addresses must be stable by the start of t_{AS-} time. 5. To conserve power and reduce sensing noise, it is recommended that all addresses be reset low after t_{CO} time and remain reset until t_{AS+} time. 6. The parameter t_{RCY} and t_{WCY} are defined as $t_T + t_{CE} + t_T + t_{CC}$. 7. The parameter t_{ACC} is defined as $t_{AS+} + t_T + t_{CO}$. 8. The parameter t_{CO} is defined at V_{OL} or V_{OH} whichever occurs last. 9. The load resistor R_L is connected to $V_{termination}$ where $V_{termination} = -1.175V \pm 60mV$ at 25°C, $T_C = 1.3mV/°C$, $V_{BB}/V_{termination} = 4.43$. 10. The parameter t_{DS} is referenced to the rising edge of write enable and the transition of data. 11. The parameter t_{DH} is referenced to the falling edge of Cenable (③) or Write Enable (①), whichever occurs first. 12. The parameter t_{RWC} is defined as $t_{CO} + t_{WC} + 3t_T + t_{CC}$ + modify time or $t_T + t_{CEM} + t_T + t_{CC}$ + modify time. 13. T_{CEM} applies for Read Modify Write Cycle.

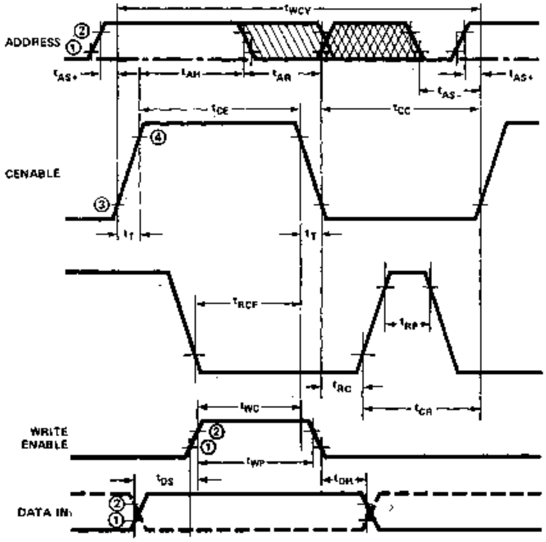
***These parameters refer to the 2105-1.**

Waveforms

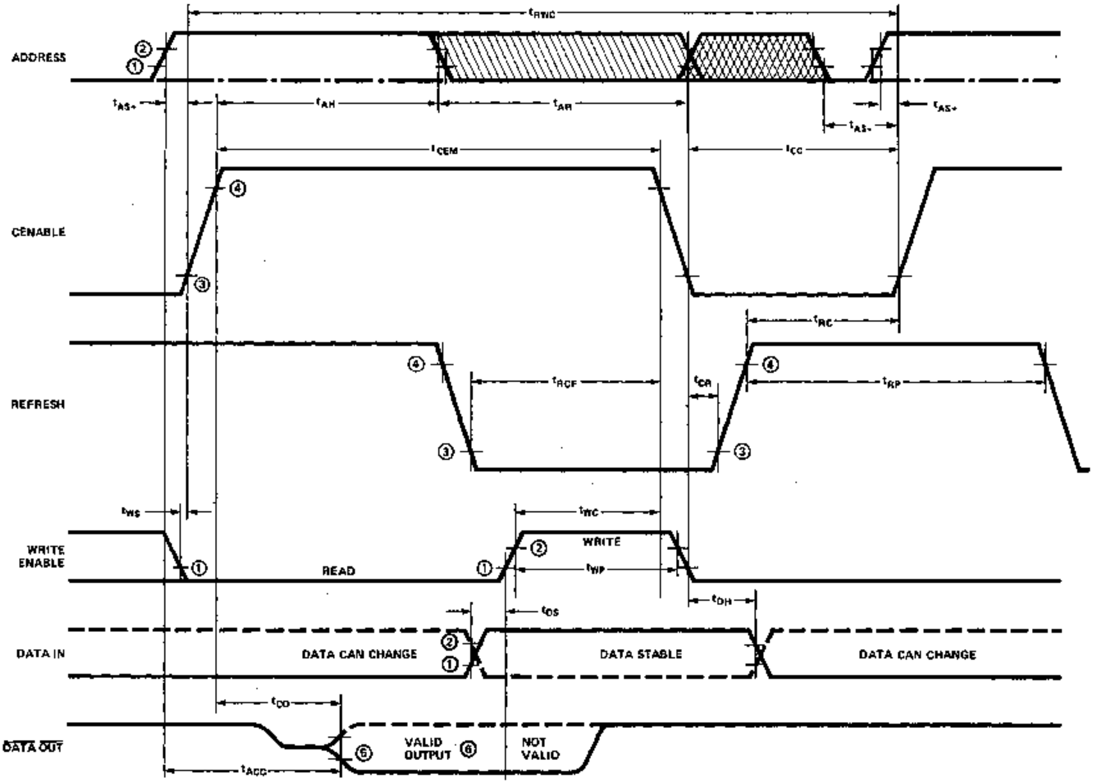
READ CYCLE



WRITE CYCLE



READ MODIFY WRITE CYCLE

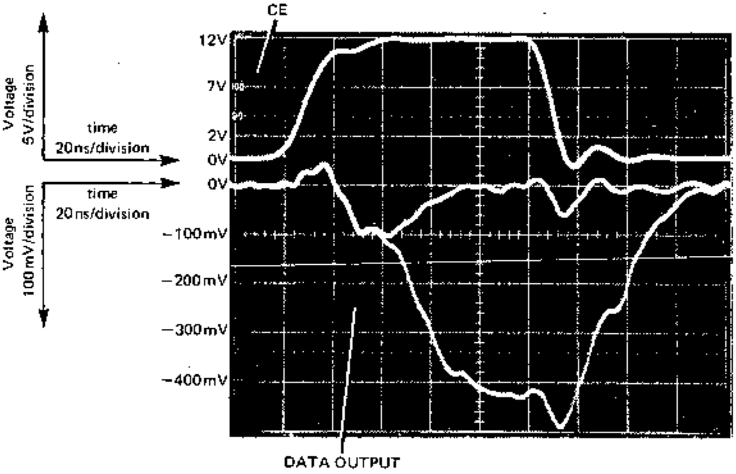


Capacitance $T_A = 25°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

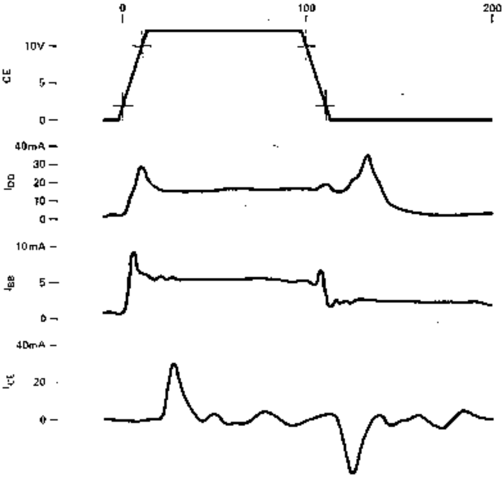
Symbol	Parameter	Plastic Pkg. Typ.	Plastic Pkg. Max.	Unit	Conditions	
C_{IN}	Input Capacitance (Address, D_{IN}, WE, Ref)	4	6	pF	$V_{IN} = V_{SS}$	f = 1MHz. All Unused Pins Are at V_{SS}.
C_{OUT}	Data Out Capacitance	4	6	pF	$V_{IN} = V_{SS}$	
C_{CE}	Effective Cenable Capacitance	65	85	pF	Note 1	

Typical Data Output Characteristics

The actual oscilloscope photo below shows the Cenable input and the resulting data outputs of two address locations during read of a typical device. One location with a one (high) stored and the other with a zero (low) stored. The output would normally be strobed at t_{CO} time. For a high output the condition of V_{OH} between 0V and -80mV must be met. For a low output the condition of V_{OL} more negative than -150mV must be met.



Typical Current Transients vs. Time



Application Information

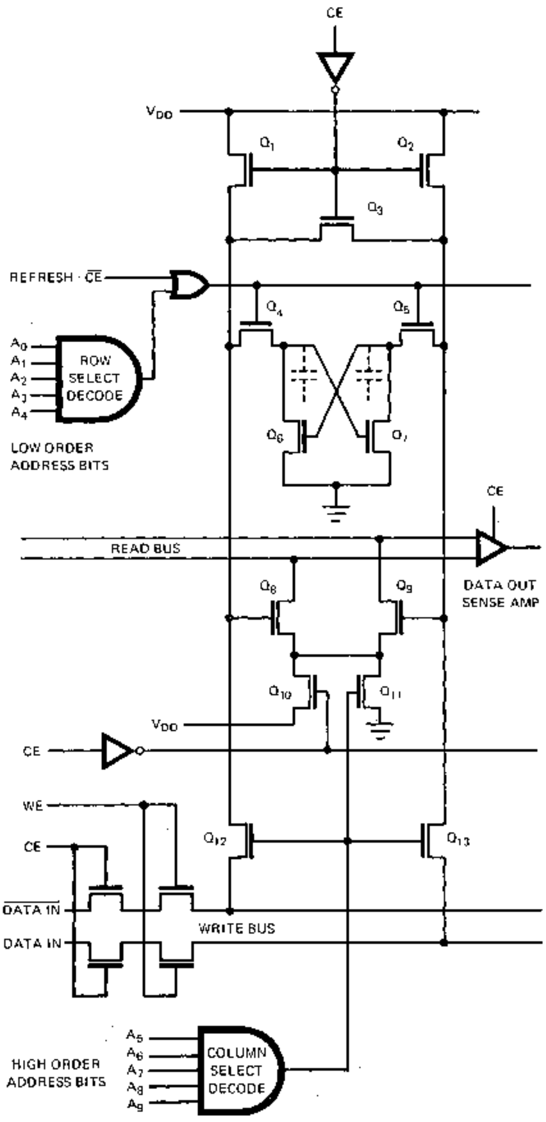
Basic Cell Operation

Read or Write Cycle

The basic 2105 storage element, as shown in the Figure, is comprised of the distributed gate to substrate capacitance of Q_6 and Q_7. A one or a zero is stored by charging one capacitor and discharging the other. Q_6 and Q_7 are cross coupled and provide a stable flip-flop when Q_1, Q_2, Q_4, and Q_5 are turned on. Q_4 and Q_5 are enabled by one of the 32 row select decoders. Enabling Q_4 and Q_5 connects the storage elements to the column I/O bus. A few nanoseconds later Q_1, Q_2, Q_3 are disabled when Cenable becomes true. When Q_1 and Q_2 are disabled, they form a high resistance load to each of the differential column I/O lines. This allows a differential voltage to be developed across the lines. The differential voltage will either originate from Q_6 and Q_7 (in a read mode) or from the data in line if Write, Enable, Cenable and column decode are all true. In the case of a read cycle, the information in the cell is retained. Enabling the write bus will override the Q_6 and Q_7 levels and charge their distributed capacities to the new data value. If the write bus is not enabled, the data from Q_6 and Q_7 is gated to the read bus by way of Q_8 and Q_9 which are also gated by the column select decode signal. The data on the read bus is amplified by the data out sense amplifier and becomes the data out signal from the device. When chip enable goes false, (logic 0), Q_1, Q_2 and Q_3 will conduct. The low resistance of these elements insures a zero volt difference across the I/O lines. Incidentally, this provides a refresh condition on the row which is selected and a data hold condition on the other 31 rows.

Refreshing the Cell

During refresh, Q_1 - Q_3 are on, connecting both sides of the column I/O bus to V_{DD} through a low resistance path. If Q_4 and Q_5 are turned off (rows not selected), the data on the distributed capacitance of Q_4 and Q_5 will eventually leak off. However, applying a refresh signal to all rows will enable Q_4 and Q_5 on all 1024 cells. Q_4 and Q_6 become a voltage divider to the gate of Q_7 as Q_5 and Q_7 form a voltage divider for the gate of Q_6. Both dividers form a regenerative feed back network to re-enforce the initial charges on the distributed capacity of the storage element. Isolation between cells on the same column is provided by the low resistance of Q_1, Q_2 and Q_3. Removing the refresh signal restores the circuits to a data hold condition.



Simplified memory cell and associated circuitry.

Power Supply Requirements

The 2105 N-channel device requires only two voltages for operation. V_{DD}, the most positive voltage, is +12 volts, V_{BB} is either -5 volts or -5.2 volts, and V_{SS} is 0 volts (ground).

V_{BB} is the substrate voltage and is normally equal to the standard ECL -5.2 volt level. V_{BB} is the most negative voltage present and serves to maintain a back bias between the substrate and active elements. Back biasing the substrate increases the MOS threshold levels, and maintains isolation between independent adjacent elements. The current associated with V_{BB}, I_{BB} has three states that are of concern to the designer. I_{BB1} is the V_{BB} current with cenable on, but does not include the leading and trailing edge transition currents. I_{BBS} is the standby current and includes the refresh transient currents. I_{BBAV} is the average V_{BB} current over a memory cycle. All three currents vary inversely with temperature as shown in the figure on the data sheet. Typical I_{BB} transients are presented in the figure below.

A positive voltage on the N-channel substrate could occur if the V_{BB} line becomes accidentally connected to a positive voltage line and if the V_{BB} power supply current limit is set lower than the current limit of the positive supply. A positive N-channel substrate to ground (V_{SS}) bias will result in a substrate current through each 2105 device. By use of current limiting power supplies and connecting a diode from V_{BB} to V_{SS}, (anode to V_{BB} and cathode to V_{SS}) the forward substrate currents will be reduced, thus preventing possible catastrophic results from occurring.

V_{DD} is the most positive voltage associated with an N-channel device, and for the 2105 is equal to 12 volts. The V_{DD} current, I_{DD}, varies depending on the mode of operation of the memory. I_{DD1} is the V_{DD} current with cenable on, but does not include the leading and trailing edge transition currents. I_{DD2} is the current for cenable off and the addresses high which is the maximum current related to addresses cycling on devices that are not selected. I_{DDS} is the standby current with cenable off, and is also related to the refresh frequency. I_{DDAV} is the average V_{DD} current over a memory cycle. Typical I_{DD} transient currents are presented in the last figure.

The I_{DDS} standby current includes the average of the planar refresh current. During each refresh pulse, a typical current surge in the order of 100mA and 20 ns duration is drawn from the V_{DD} supply. The amount of standby current represented by refresh is calculated by averaging this I_{DD} refresh pulse over the 10µs refresh cycle time. Stated in equation form:

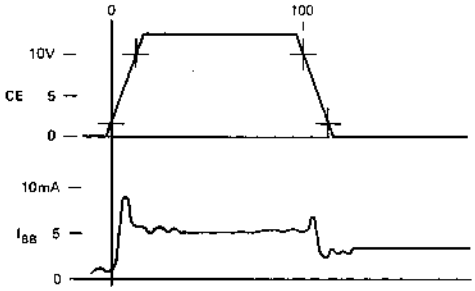
$$I_{REF\ AV} = \frac{\text{ON TIME}}{\text{TOTAL TIME}} \times I_{PREF}$$

OR, numerically

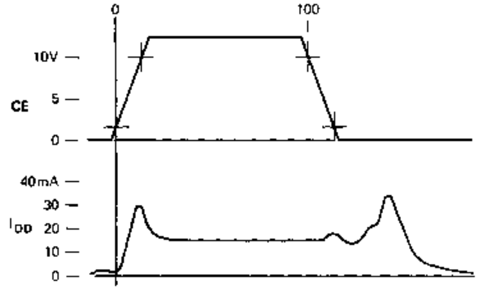
$$I_{REF\ AV} \pm \frac{20 \times 10^{-9}\ \text{SEC}}{10 \times 10^{-6}\ \text{SEC}} \times 100\text{mA} = .2\text{mA}$$

The above equation indicates that the average refresh current is proportional to the refresh frequency. Thus, doubling the refresh rate from 100kHz to 200kHz would double $I_{REF\ AV}$, or, for the I_{DDS} value in Table VII,

$$I_{DDS} = I_{MIN} + I_{REF\ AV}$$
$$= 2.8\text{mA} + .4\text{mA} = 3.2\text{mA}$$



Typical I_{BB} transients.



Typical I_{DD} transients.

intel Silicon Gate MOS **2105-2**

1024 BIT HIGH SPEED DYNAMIC MOS RANDOM ACCESS MEMORY

Invisible Refresh

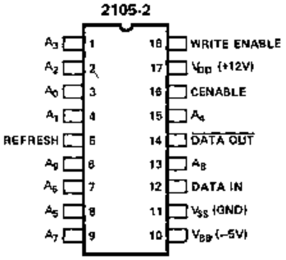
- **High Speed N-Channel— 85 ns Maximum Access Time**
- **Cycle Time--190 ns Maximum**
- **Planar Refresh**
- **Standby Power—100 µW/Bit**
- **Fully Decoded—On Chip Address Decode**
- **Low Level Address, Data, Write Enable Inputs**
- **Current Sinking Output**
- **OR-Tie Capability**
- **All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

The Intel 2105-2 is a very high speed 1024 word by one bit dynamic random access memory element using normally off N-Channel MOS devices integrated on a monolithic array.

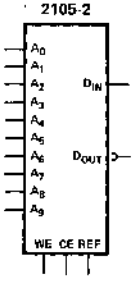
The 2105-2 is designed for memory applications where very high speed, low cost, and low power dissipation are important design objectives. The planar refresh mode of operation simplifies system design and allows all 1024 memory cells to be refreshed at once. The refresh timing is completely asynchronous to all other 2105-2 timing.

The Intel 2105-2 is fabricated with N-Channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-Channel silicon gate technology.

PIN CONFIGURATION



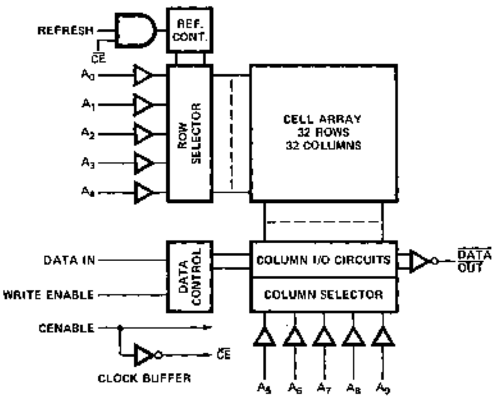
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_9	ADDRESS INPUTS	REF	REFRESH INPUT
WE	WRITE ENABLE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB}	+25V to –0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	+20V to –0.3V
Power Dissipation	1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 0°C$ to $55°C$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5.2V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.[2]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (Address, D_{IN}, WE)			10	μA	$V_{IN} = 0V$ to $6.5V$
I_{LIC}	Input Load Current (CE, Ref)			10	μA	$V_{IN} = 0V$ to $V_{DD} + 0.5V$
I_{LO}	Output Leakage Current			1	μA	$V_O = 0V$
I_{DD1}	V_{DD} Current During Cenable ON		30	44	mA	$V_{CE} = 13.6V$, $V_{IN} = 0V$ to $4V$, $T_A = 25°C$
I_{DD2}	V_{DD} Current During Cenable OFF, Address High		15	21	mA	$V_{CE} = 0V$, $V_{IN} = 4V$, $T_A = 25°C$
I_{DDS}	Average Standby V_{DD} Current During Cenable OFF		3.0	6.0	mA	$V_{CE} = 0V$, $V_{IN} = 0V$, $T_A = 25°C$ $t_{REF} = 10\mu s$
$\lvert I_{BB1} \rvert$	V_{BB} Current During Cenable ON		5.5	10.5	mA	$V_{CE} = 13.6V$, $V_{IN} = 0V$ to $4V$, $D_{OUT} = 0V$, $T_A = 25°C$
$\lvert I_{BBS} \rvert$	Standby V_{BB} Current During Cenable OFF		2.5	5.0	mA	$V_{CE} = 0V$, $V_{IN} = 0V$ to $4V$, $D_{OUT} = 0V$, $t_{REF} = 10\mu s$, $T_A = 25°C$
$I_{DD\,AV}$	Average V_{DD} Supply Current		28	41	mA	$t_{cyc} = 190ns$, $t_{REF} = 10\mu s$, $T_A = 25°C$
$\lvert I_{BB\,AV} \rvert$	Average V_{BB} Supply Current		4.5	9.0	mA	$t_{cyc} = 190ns$, $t_{REF} = 10\mu s$, $T_A = 25°C$
V_{IL}	Input Low Level Voltage (All Inputs)	$V_{SS} - 1$		$V_{SS} + 1$	V	
V_{IH}	Input High Level Voltage (Address, D_{IN}, WE)	4.0		6.5	V	
V_{IHC}	Input High Level Voltage (CE, Ref)	$V_{DD} - 1$		$V_{DD} + 1$	V	
V_{OL}	Output Low Voltage[4]			-150	mV	$R_L = 100\Omega$ at $t_{CO} = 65ns$
V_{OH}	Output High Voltage[4]	-80			mV	$R_L = 100\Omega$ at $t_{CO} = 65ns$

NOTES:

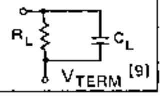
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be more negative than V_{BB}.
3. The current I_{SS} is $I_{DD} - I_{BB}$.
4. Output voltages are measured w.r.t. $V_{termination}$.
5. The load resistor R_L is connected to $V_{termination}$ where $V_{termination} = -1.175V \pm 60$ mV at 25°C, $T_C = 1.3mV/°C$, $V_{BB}/V_{termination} = 4.43$.

A. C. Characteristics T_A = 0°C to 55°C, V_{DD} = 12V ± 5%, V_{BB} = −5.2V ± 5%, V_{SS} = 0V, unless otherwise specified.[1]

READ, WRITE, and READ MODIFY WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Planar Refresh Pulses	1	10	µs	
t_{AR}	Address Reset Time	Note 2		ns	
t_{AS+}[3] [5]	High Address Setup Time	5		ns	
t_{AS-}[4] [5]	Low Address Setup Time	35		ns	
t_{AH}	Address Hold Time	50		ns	
t_{CE}	Cenable On Time	80	360	ns	
t_{CC}	Cenable Off Time	80		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}[6]	Read Cycle	190		ns	t_T = 15ns
t_{WS}	Write Enable to Cenable Set Up Time	0		ns	
t_{CO}	Cenable Output Delay		65	ns	C_{LOAD} = 50pF R_{LOAD} = 100Ω Refer to Note 8 
t_{ACC}[7]	Address to Output Access		85	ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}[6]	Write Cycle	190		ns	t_T = 15ns
t_{WP}	Write Enable Pulse Width	70		ns	
t_{WC}	Write Enable to Cenable End	70	120	ns	
t_{DS}[10]	Data Set Up Time	0		ns	
t_{DH}[11]	Data Hold Time	20		ns	

READ MODIFY WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[12]	Read Modify Write Cycle	270		ns	t_T = 15ns
t_{CEM}[13]	Cenable On Time	160	360	ns	

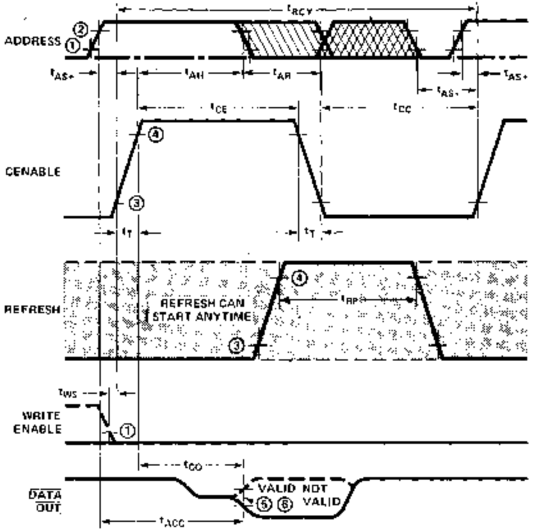
PLANAR REFRESH TIMING

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RP}	Asynchronous Refresh P.W.	t_{CE}+140		ns	The refresh pulse timing is not related to any other signal.
t_{REF}	Time Between Planar Refresh	1	10	µs	

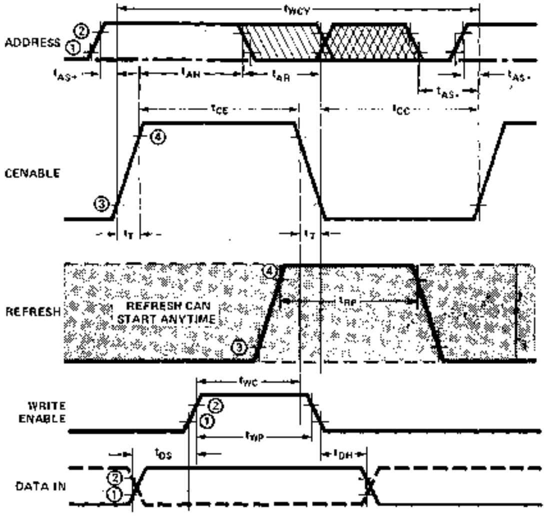
NOTES:
1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.
2. t_{AR} is defined as $t_{CE} + t_T - t_{AH}$. During t_{AR} addresses may only be reset low or remain stable. Addresses may change after the start of t_{CC} and before the start of t_{AS-}.
3. High addresses must be stable by the start of t_{AS+} time.
4. Low addresses must be stable by the start of t_{AS-} time.
5. To conserve power and reduce sensing noise, it is recommended that all addresses be reset low after t_{CO} time and remain reset until t_{AS+} time.
6. The parameter t_{RCY} and t_{WCY} are defined as $t_T + t_{CE} + t_T + t_{CC}$.
7. The parameter t_{ACC} is defined as $t_{AS+} + t_T + t_{CO}$.
8. The parameter t_{CO} is defined at V_{OL} or V_{OH}, whichever occurs last.
9. The load resistor R_L is connected to $V_{termination}$ where $V_{termination}$ = −1.175V ± 60mV at 25°C, T_C ≈ 1.3mV/°C, $V_{BB}/V_{termination}$ = 4.43.
10. The parameter t_{DS} is referenced to the rising edge of Write Enable and the transition of data.
11. The parameter t_{DH} is referenced to the falling edge of Cenable (③) or Write Enable (①), whichever occurs first.
12. The parameter t_{RWC} is defined as $t_{CO} + t_{WC} + 3t_T + t_{CC}$ + modify time or $t_T + t_{CEM} + t_T + t_{CC}$ + modify time.
13. T_{CEM} applies for Read Modify Write Cycle.

Waveforms

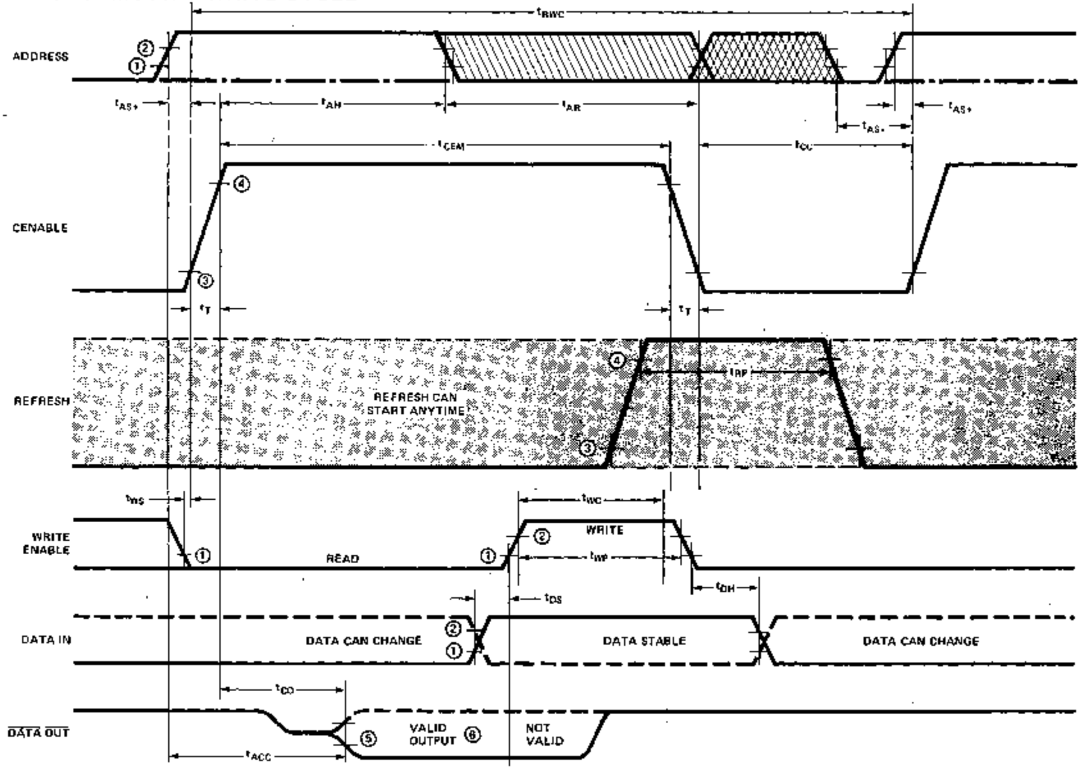
READ CYCLE



WRITE CYCLE



READ MODIFY WRITE CYCLE



NOTES:

① V_{SS} + 1.5V

② V_{SS} + 3.0V

③ V_{SS} + 2.0V

④ V_{DD} −2.0V

⑤ The parameter t_{CO} is defined at V_{OL} or V_{OH}, whichever occurs last. $R_L = 100\Omega$, $C_L = 50pF$.

⑥ Data Out is valid during t_{CE} time or until Write Enable goes high.

intel® Silicon Gate MOS 2107A

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

*** Access Time -- 300 ns max.**
*** Refresh Period -- 2 ms**

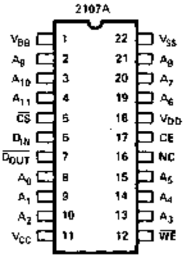
- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal – Chip Enable**
- **Low Level Address, Data, Write Enable, Chip Select Inputs**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion – Chip Select Input Lead**
- **Fully Decoded – On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Ceramic and Plastic 22-Pin DIPs**

The Intel 2107A is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107A uses dynamic circuitry which reduces the operation and standby power dissipation.

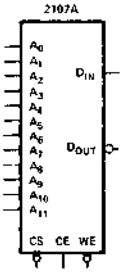
Reading information from the memory is non-destructive. Refreshing is accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107A is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies.

PIN CONFIGURATION



LOGIC SYMBOL

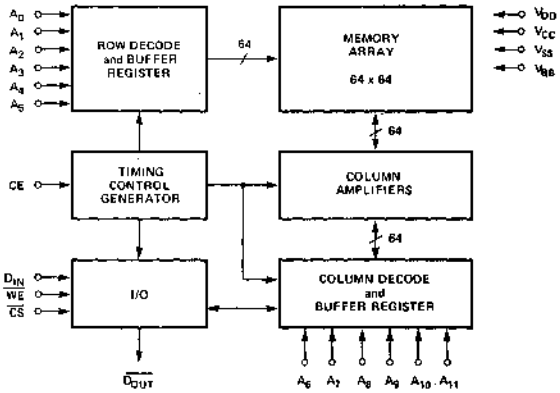


PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_{11}	ADDRESS INPUTS*	$\overline{D_{OUT}}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	NC	NOT CONNECTED

*Refresh Addresses A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . −65° C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . +25V to −0.3V
Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . +20V to −0.3V
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = -5V ± 5%, V_{SS} = 0V, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = -1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = -1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on		14	22	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV}$	Average V_{DD} Supply Current		23	34	mA	Cycle time = 700ns, t_{CEW} = 480ns, T_A = 25°C, Fig. 1,3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = -1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, T_A = 25°C
$I_{CC\ AV}$	Average V_{CC} Supply Current		6	10	mA	Cycle time = 700ns, t_{CEW} = 480ns T_A = 25°C, Fig. 2,4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} −1		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = -100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.

D.C. Characteristics

Fig. 1. I_{DD} AVERAGE VS. TEMPERATURE

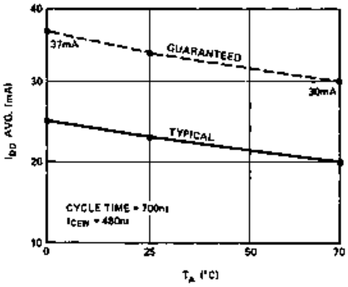


Fig. 2. I_{CC} AVERAGE VS. TEMPERATURE

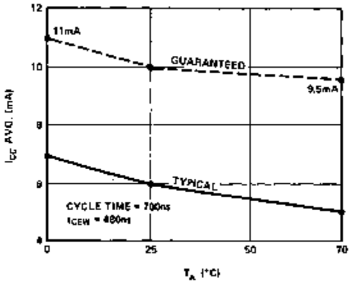


Fig. 3. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

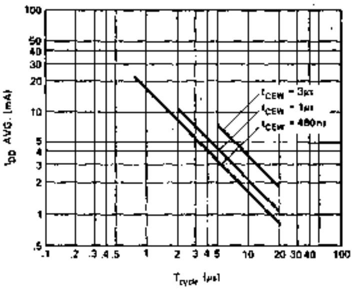


Fig. 4. TYPICAL I_{CC} AVERAGE VS. CYCLE TIME

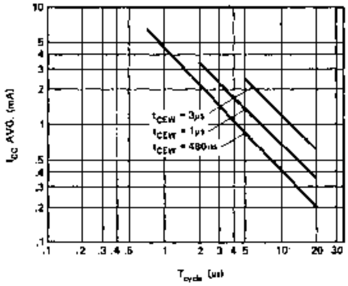


Fig. 5. TYPICAL I_{OH} VS. V_{OH}

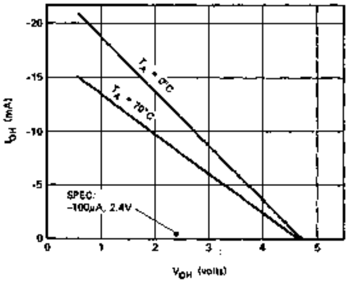


Fig. 6. TYPICAL I_{OL} VS. V_{OL}

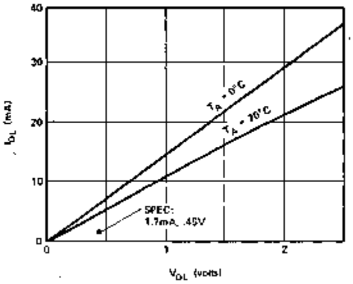


Fig. 7. TYPICAL REFRESH VS. TEMPERATURE

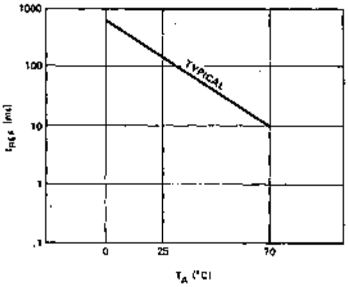
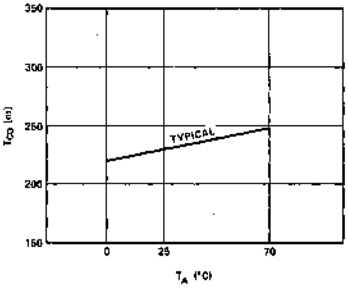


Fig. 8. TYPICAL ACCESS TIME VS. TEMPERATURE



A.C. Characteristics $T_A = 0^\circ C$ to $70^\circ C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to CE Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	180		ns	
t_T	CE Transition Time		50	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	500		ns	$t_T = 20ns$
t_{CER}	CE On Time During Read	280	3000	ns	
t_{CO}	CE Output Delay		280	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		300	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$ Low	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	700		ns	$t_T = 20ns$
t_{CEW}	CE Width During Write	480	3000	ns	
t_W	$\overline{WE}$ to CE Off	340		ns	
t_{CW}	CE to $\overline{WE}$ High	300		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD}[1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	150		ns	
t_{WW}	$\overline{WE}$ Wait	0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Capacitance[2] $T_A = 25^\circ C$

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Plastic And Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$, $\overline{WE}$, D_{IN}	3	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	3	6	pF	$V_{OUT} = 0V$

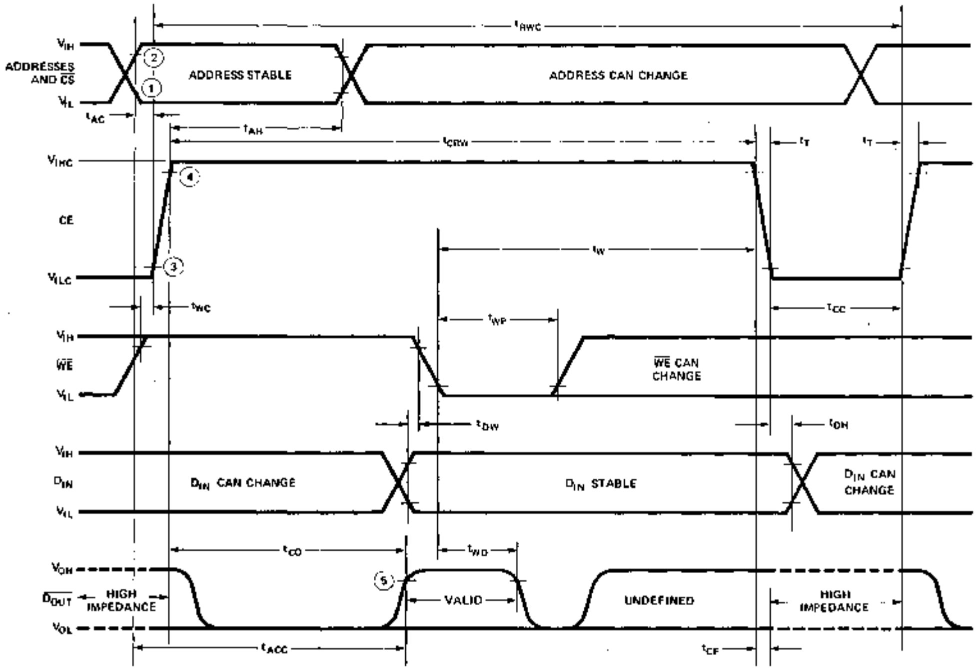
Notes:
1. t_{CO} applies only when $t_W > t_{CEW} - 50$ ns.
2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation

$$C = \frac{I \Delta t}{\Delta V}$$ with the current equal to a constant 20mA.

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[1]	Read Modify Write(RMW) Cycle Time	840		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	620	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	340		ns	$C_{load} = 50pF$, Load = One TTL Gate, Ref = 2.0V for High, 0.8V for Low.
t_{WP}	$\overline{WE}$ Pulse Width	150		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		280	ns	
t_{ACC}	Access Time		300	ns	
t_{WD}	$\overline{D_{OUT}}$ Valid After $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

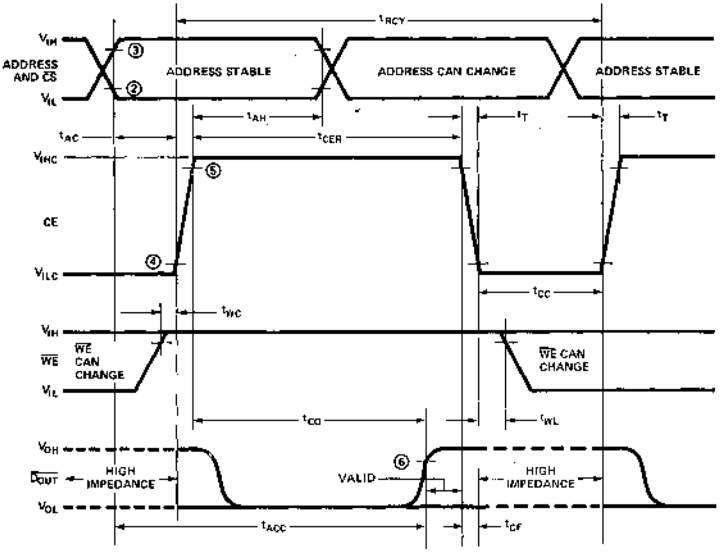
Note 1. $t_{CRW} - t_W = t_{CO}$.



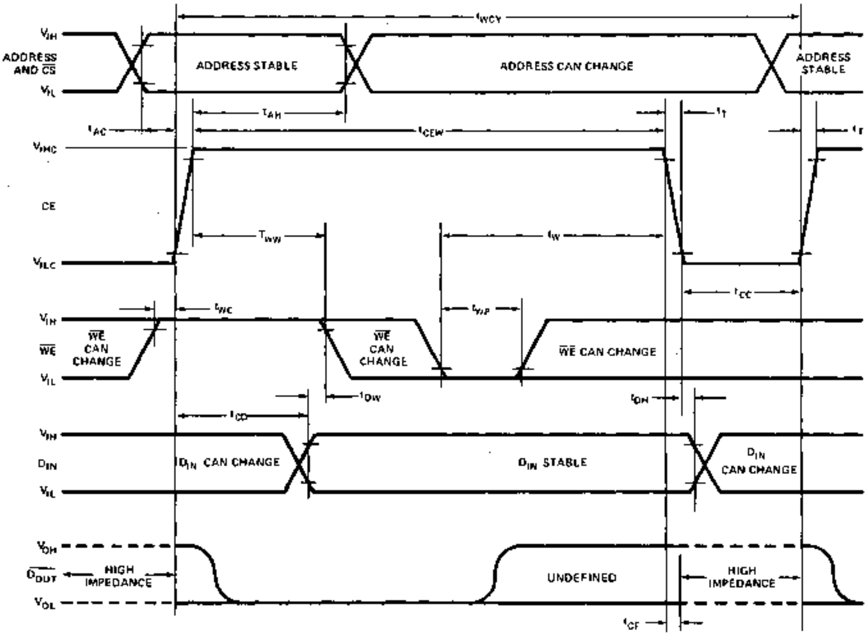
NOTES:

1. $V_{SS} + 1.5V$ is the reference level for measuring timing of the address CS, WE, and D_{IN}.
2. $V_{SS} + 3.0V$ is the reference level for measuring timing of the address, CS, WE, and D_{IN}.
3. $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
4. $V_{DD} -2V$ is the reference level for measuring timing of CE.
5. $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT}.

Read and Refresh Cycle [1]



Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{SS} + 1.5V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{SS} + 3.0V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} + 2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

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Silicon Gate MOS 2107A-1

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

***Access Time--280 ns max.** ***Write Cycle Time--550 ns**
***Read Cycle Time--420 ns**

The 2107A-1 is a high speed version of the 2107A. Please refer to page 2-67 for functional description, pin configuration, logic symbol, and block diagram. See page 2-68 for absolute maximum ratings and page 2-70 for capacitance specification. Refer to page 2-72 for read and write cycle timing definitions, and page 2-71 for read-modify-write cycle timing definitions.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = -5V ± 5%, V_{SS} = 0V, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\lvert I_{LO}\rvert$	Output Leakage Current for high impedance state		.01	10	μA	CE = -1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = -1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on		14	22	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV}$	Average V_{DD} Supply Current		28	38	mA	Cycle time = 550ns, t_{CEW} = 410ns T_A = 25°C, Fig. 1,3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = -1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, T_A = 25°C
$I_{CC\ AV}$	Average V_{CC} Supply Current		8	12	mA	Cycle time = 550ns, t_{CEW} = 410ns T_A = 25°C, Fig. 2,4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} −1		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = -100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	100		ns	
t_T	CE Transition Time		50	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	420		ns	$t_T = 20ns$
t_{CER}	CE On Time During Read	280	3000	ns	
t_{CO}	CE Output Delay		260	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		280	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	550		ns	$t_T = 20ns$
t_{CEW}	CE Width During Write	410	3000	ns	
t_W	$\overline{WE}$ to CE Off	250		ns	
t_{CW}	CE to $\overline{WE}$	250		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD}[1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	150		ns	
t_{WW}	$\overline{WE}$ Wait	0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[1]	Read Modify Write(RMW) Cycle Time	670		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	530	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	250		ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	150		ns	Ref = 2.0V for High, 0.8V for Low.
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		260	ns	
t_{ACC}	Access Time		280	ns	
t_{WD}	D_{OUT} Valid After $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Note 1. $t_{CRW} - t_W = t_{CO}$.

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Silicon Gate MOS 2107A-4

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

*** Access Time -- 350 ns max.** *** Refresh Period -- 2 ms**

The 2107A-4 is a version of the 2107A with 570ns read cycle time and 840ns write cycle time. Please refer to page 2-67 for functional description, pin configuration, logic symbol, and block diagram. See page 2-68 for absolute maximum ratings and page 2-70 for capacitance specification. Refer to page 2-72 for read and write cycle timing definitions, and page 2-71 for read-modify-write cycle timing definitions.

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, V_{BB}[1] $= -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
I_{LC}	Input Load Current		.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	µA	CE = −1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	µA	CE = −1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on		14	22	mA	CE = V_{IHC}, $T_A = 25°C$
$I_{DD\,AV}$	Average V_{DD} Supply Current		20	30	mA	Cycle time = 840ns, t_{CEW} = 600ns, $T_A = 25°C$, Fig. 1, 3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	µA	CE = −1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, $T_A = 25°C$
$I_{CC\,AV}$	Average V_{CC} Supply Current		5	9	mA	Cycle time = 840ns, t_{CEW} = 600ns, $T_A = 25°C$, Fig. 2, 4
I_{BB}	V_{BB} Supply Current		1	100	µA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		$V_{CC}+1$	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	$V_{DD}-1$		$V_{DD}+1$	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = −100µA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for $T_A = 25°C$ and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2 1	ms ms	Ceramic package Plastic package*
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	200		ns	
t_T	CE Transition Time		50	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

*t_{REF} of 2ms available by special request in plastic. Specify P2107AS1226.

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	570		ns	$t_T = 20ns$
t_{CER}	CE On Time During Read	330	3000	ns	
t_{CO}	CE Output Delay		330	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		350	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	840		ns	$t_T = 20ns$
t_{CEW}	CE Width During Write	600	3000	ns	
t_W	$\overline{WE}$ to CE Off	400		ns	
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD}[1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WW}	WE Wait	170		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[1]	Read Modify Write(RMW) Cycle Time	970		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	730	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	400		ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	Ref = 2.0V for High, 0.8V for Low.
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		330	ns	
t_{ACC}	Access Time		350	ns	
t_{WD}	D_{OUT} Valid After $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Note 1. $t_{CRW} - t_W = t_{CO}$.

Silicon Gate MOS **2107A-5**

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

***Access Time -- 420 ns max.** *** Refresh Period -- 2 ms**

The 2107A-5 is a version of the 2107A with 690ns read cycle time and 970ns write cycle time. Please refer to page 2-67 for functional description, pin configuration, logic symbol, and block diagram. See page 2-68 for absolute maximum ratings and page 2-70 for capacitance specification. Refer to page 2-72 for read and write cycle timing definitions and page 2-71 for read-modify-write cycle timing definitions.

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, V_{BB}[1] $= -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\lvert I_{LO} \rvert$	Output Leakage Current for high impedance state		.01	10	μA	CE = −1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = −1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on		14	22	mA	CE = V_{IHC}, $T_A = 25°C$
$I_{DD\ AV}$	Average V_{DD} Supply Current		18	28	mA	Cycle time = 970ns, t_{CEW} = 680ns $T_A = 25°C$, Fig. 1, 3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = −1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, $T_A = 25°C$
$I_{CC\ AV}$	Average V_{CC} Supply Current		4	8	mA	Cycle time = 970ns, t_{CEW} = 680ns $T_A = 25°C$, Fig. 2, 4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} −1		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = −100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for $T_A = 25°C$ and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	Ceramic package
			1	ms	Plastic package*
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	250		ns	
t_T	CE Transition Time		50	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

*t_{REF} of 2ms available by special request in plastic. Specify P2107AS1245.

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	690		ns	$t_T = 20ns$
t_{CER}	CE On Time During Read	400	3000	ns	
t_{CO}	CE Output Delay		400	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		420	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	970		ns	$t_T = 20ns$
t_{CEW}	CE Width During Write	680	3000	ns	
t_W	$\overline{WE}$ to CE Off	450		ns	
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD}[1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WW}	$\overline{WE}$ Wait	200		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[1]	Read Modify Write(RMW) Cycle Time	1140		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	850	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	450		ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	Ref = 2.0V for High, 0.8V for Low.
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		400	ns	
t_{ACC}	Access Time		420	ns	
t_{WD}	$\overline{D_{OUT}}$ Valid After $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Note 1. $t_{CRW} - t_W = t_{CO}$

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

***Access Time -- 420 ns max.** *** Refresh Period -- 2 ms**

The 2107A-8 is the lowest cost version of the 2107A. Please refer to page 2-67 for functional description, pin configuration, logic symbol, and block diagrams. See page 2-68 for absolute maximum ratings and page 2-70 for capacitance specification. Refer to page 2-72 for read and write cycle timing definitions, and page 2-71 for read-modify-write cycle timing definitions.

D.C. and Operating Characteristics

T_A = 0°C to 55°C, V_{DD} = +12V + 5% -2.5%, V_{CC} = +5V ±5%, V_{BB}[1] = -5V ±5%, V_{SS} = 0V, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\lvert I_{LO} \rvert$	Output Leakage Current for high impedance state		.01	10	μA	CE = −1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = -1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on		14	22	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV}$	Average V_{DD} Supply Current		18	28	mA	Cycle time = 970ns, t_{CEW} = 680ns T_A = 25°C, Fig. 1, 3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = -1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, T_A = 25°C
$I_{CC\ AV}$	Average V_{CC} Supply Current		4	8	mA	Cycle time = 970ns, t_{CEW} = 680ns T_A = 25°C, Fig. 2, 4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} -0.8		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = -100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.

A.C. Characteristics T_A = 0°C to 55°C, V_{DD} = 12V +5% –2.5%, V_{CC} = 5V ±5%, V_{BB} = –5V ±5%,

READ, WRITE, AND READ MODIFY/WRITE CYCLE V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	Ceramic package
			1	ms	Plastic package*
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	250		ns	
t_T	CE Transition Time		50	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

*t_{REF} of 2ms is available by special request in plastic. Specify P2107AS987.

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	690		ns	t_T = 20ns
t_{CER}	CE On Time During Read	400	3000	ns	
t_{CO}	CE Output Delay		400	ns	C_{load} = 50pF, Load = One TTL Gate,
t_{ACC}	Address to Output Access		420	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	970		ns	t_T = 20ns
t_{CEW}	CE Width During Write	680	3000	ns	
t_W	$\overline{WE}$ to CE Off	450		ns	
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD}[1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WW}	$\overline{WE}$ Wait	200		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[1]	Read Modify Write(RMW) Cycle Time	1140		ns	t_T = 20ns
t_{CRW}	CE Width During RMW	850	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	450		ns	C_{load} = 50pF, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	Ref = 2.0V for High, 0.8V for Low.
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		400	ns	
t_{ACC}	Access Time		420	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WD}	D_{OUT} Valid After $\overline{WE}$	0		ns	

Note 1. $t_{CRW} - t_W = t_{CO}$.

intel®

Silicon Gate MOS 2107B

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

* Access Time -- 200 ns max.
* Read, Write Cycle Times -- 400 ns max.
* Refresh Period -- 2 ms

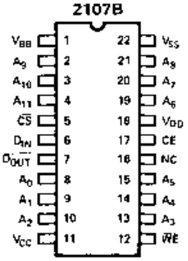
- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal – Chip Enable**
- **TTL Compatible -- All Address, Data, Write Enable, Chip Select Inputs**
- **Read-Modify-Write Cycle Time -- 520 ns**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion – Chip Select Input Lead**
- **Fully Decoded – On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Industry Standard 22-Pin Configuration**

The Intel® 2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

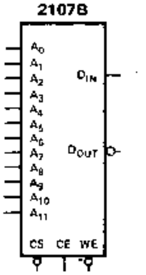
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

PIN CONFIGURATION



LOGIC SYMBOL

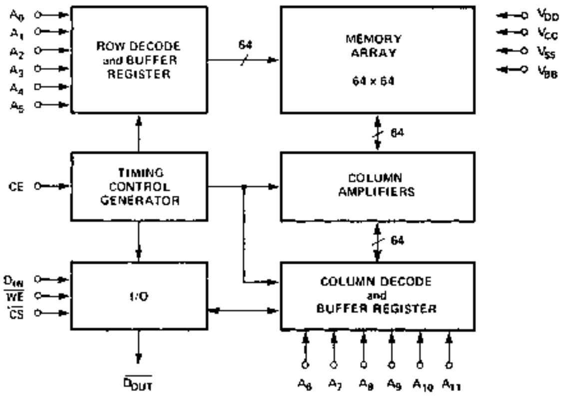


PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 70°C

Storage Temperature . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . +20V to −0.3V

Power Dissipation 1.25W

**COMMENT:*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = −5V ± 5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
$\lvert I_{LO} \rvert$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	μA	CE = −1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on		80	100	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\,AV1}$	Average V_{DD} Current		55	80	mA	Cycle time=400ns, t_{CE} = 230ns T_A = 25°C
$I_{DD\,AV2}$	Average V_{DD} Current		27	40	mA	Cycle time=1000ns, t_{CE} = 230ns
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns — See Figure 4
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

Typical Characteristics

Fig. 1. I_{DD} AV1 VS. TEMPERATURE

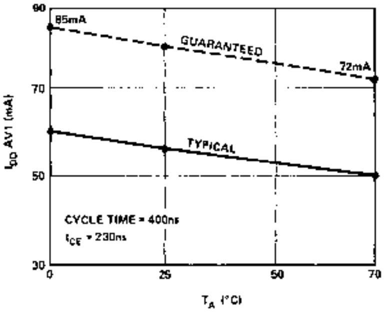


Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

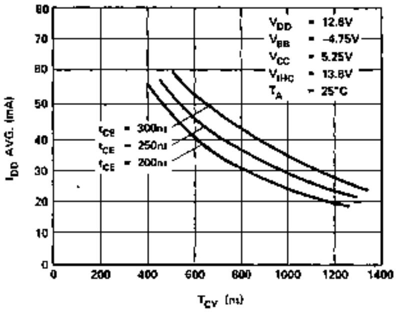


Fig. 3. I_{DD2} VS. TEMPERATURE

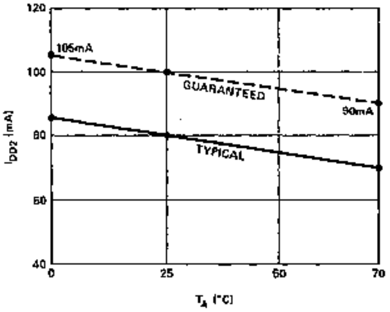


Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME

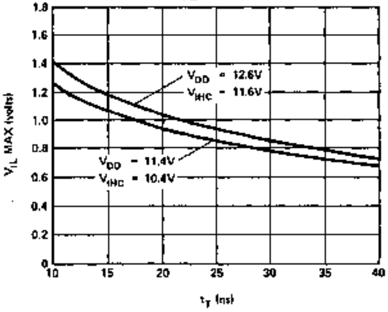


Fig. 5. TYPICAL I_{OH} VS. V_{OH}

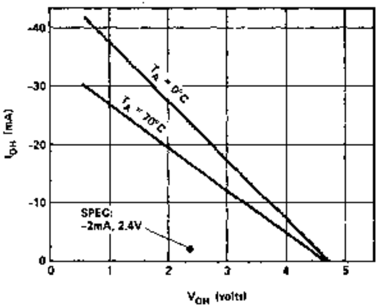


Fig. 6. TYPICAL I_{OL} VS. V_{OL}

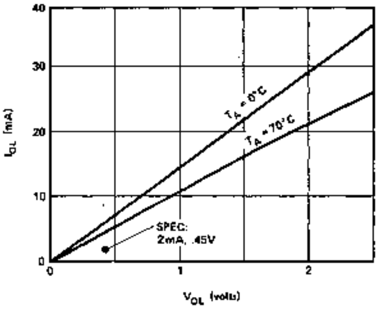


Fig. 7. TYPICAL REFRESH VS. TEMPERATURE

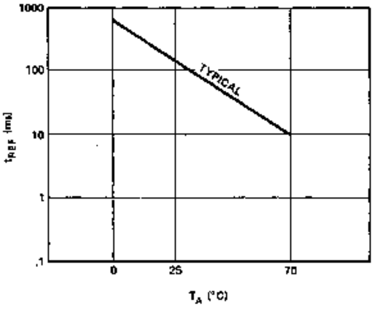
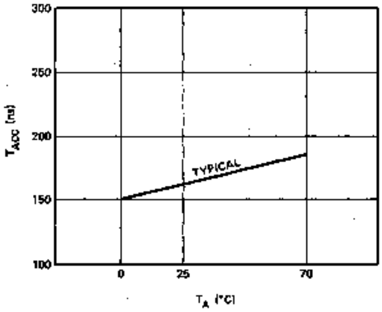


Fig. 8. TYPICAL ACCESS TIME VS. TEMPERATURE



A.C. Characteristics[1] $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	50		ns	
t_{CC}	CE Off Time	130		ns	
t_T	CE Transition Time	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	400		ns	$t_T = 20ns$
t_{CE}	CE On Time	230	3000	ns	
t_{CO}	CE Output Delay		180	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		200	ns	Ref = 2.0V.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	400		ns	$t_T = 20ns$
t_{CE}	CE On Time	230	3000	ns	
t_W	$\overline{WE}$ to CE Off	150		ns	
t_{CW}	CE to $\overline{WE}$	100		ns	
t_{DW} [2]	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	

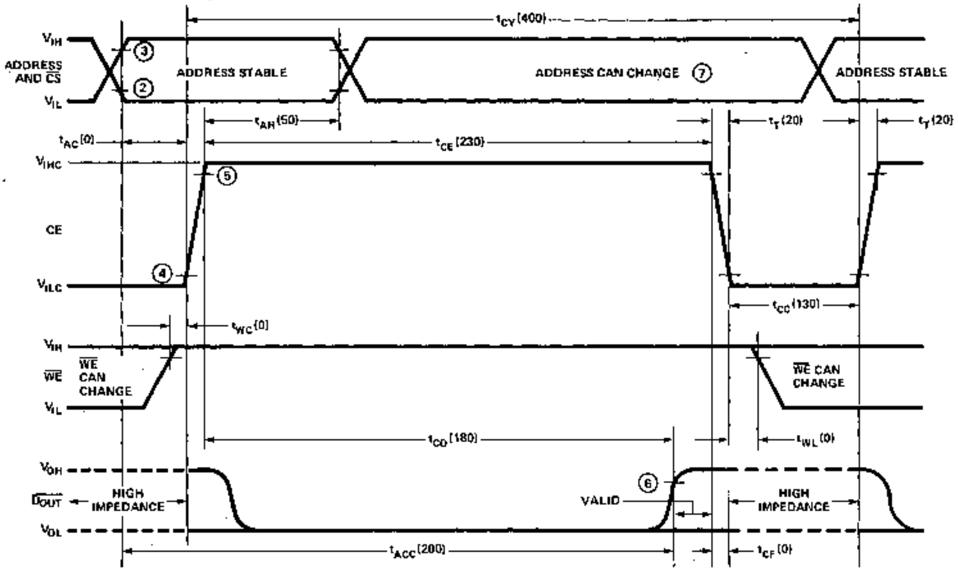
Capacitance[3] $T_A = 25°C$

Symbol	Test	Plastic And Ceramic Pkg. Typ.	 Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	8	10	pF	$V_{IN} = V_{SS}$

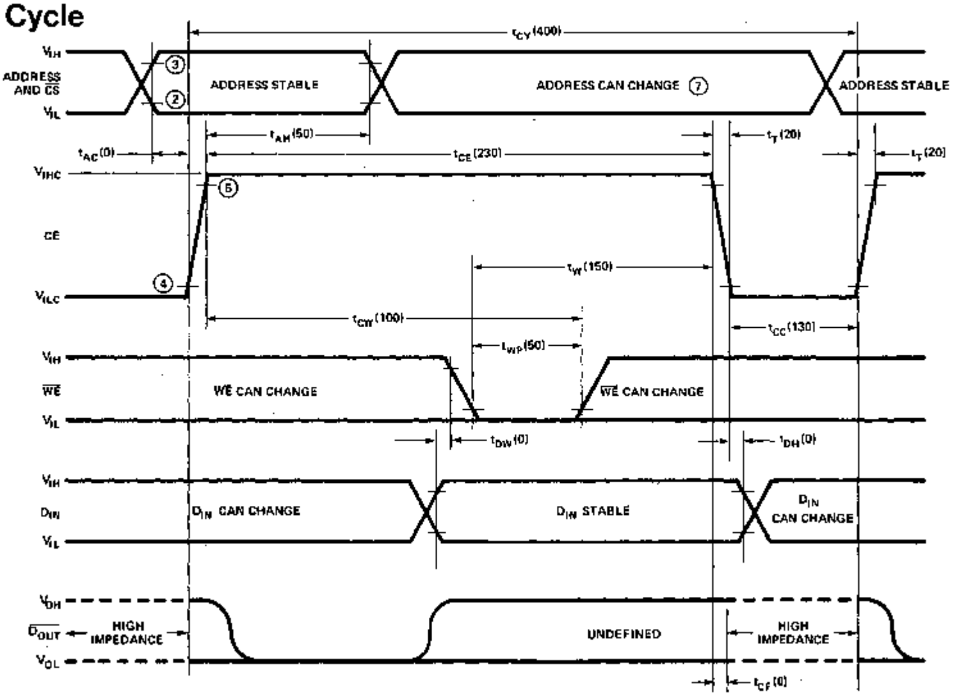
Notes:
1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is $\leqslant$60% of t_{REF}.
2. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
3. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation

$$C = \frac{I\Delta t}{\Delta V}$$ with the current equal to a constant 20mA.

Read and Refresh Cycle (1) (Numbers in parentheses are for minimum cycle timing in ns)



Write Cycle

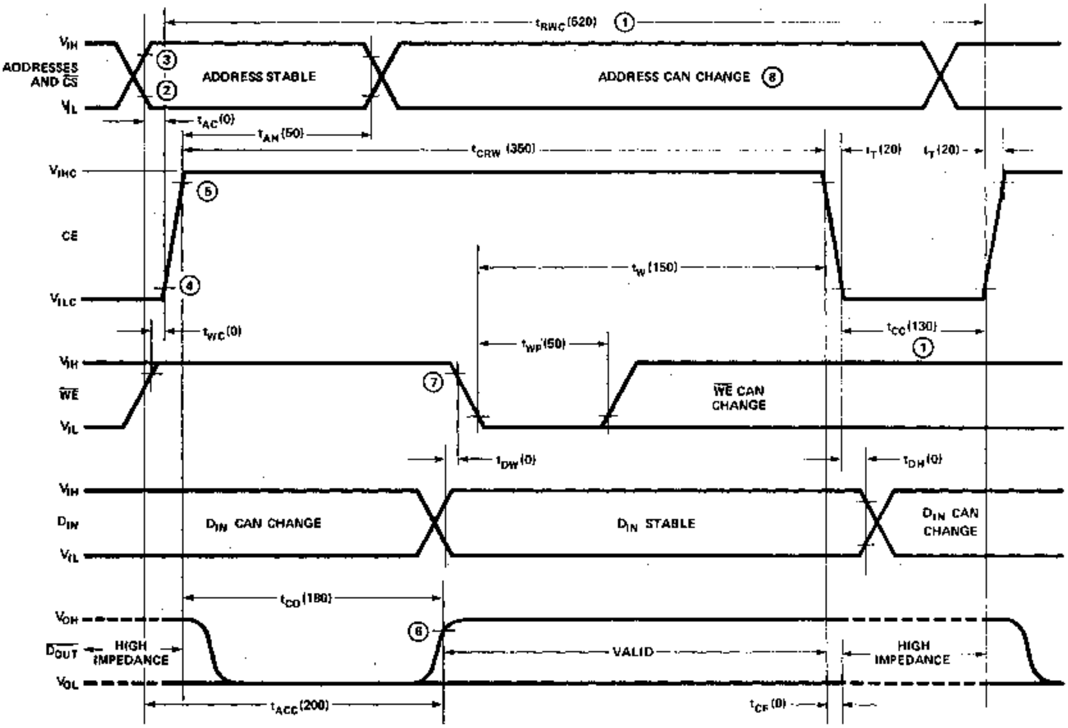


NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle[1]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	520		ns	t_T = 20ns
t_{CRW}	CE Width During RMW	350	3000	ns	C_{load} = 50pF, Load = One TTL Gate, Ref = 2.0V
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		180	ns	
t_{ACC}	Access Time		200	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

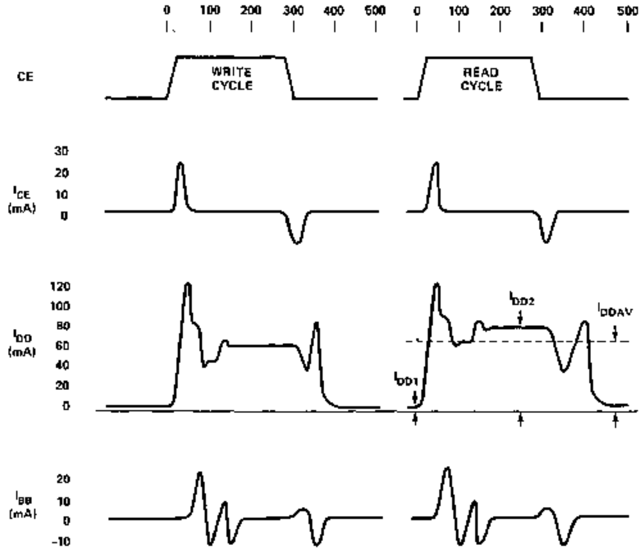
(Numbers in parentheses are for minimum cycle timing in ns.)



NOTES:

1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ≤60% of t_{REF}. For continuous Read-Modify-Write operation t_{CC} and t_{RWC} should be increased to at least 195ns and 585 ns, respectively.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Current Transients vs. Time



Applications

Refresh

The 2107B is refreshed by either a read cycle, write cycle, or read-modify write cycle. Only the selected row of memory array is refreshed. The row address is selected by the input signals A_0 thru A_5. Each individual row address must receive at least one refresh cycle within any two milliseconds time period.

If a read cycle is used for refreshing, then the chip select input, $\overline{CS}$, can be a logic high or a logic low. If a write cycle or read-modify write cycle is used to refresh the device, then $\overline{CS}$ must be a logic high. This will prevent writing into the memory during refresh.

Power Dissipation

The operating power dissipation of a selected device is the sum of $V_{DD} \times I_{DDAV}$ and $V_{BB} \times I_{BB}$. For a cycle of 400ns and t_{CE} of 230ns typical power dissipation is 660mW.

Standby Power

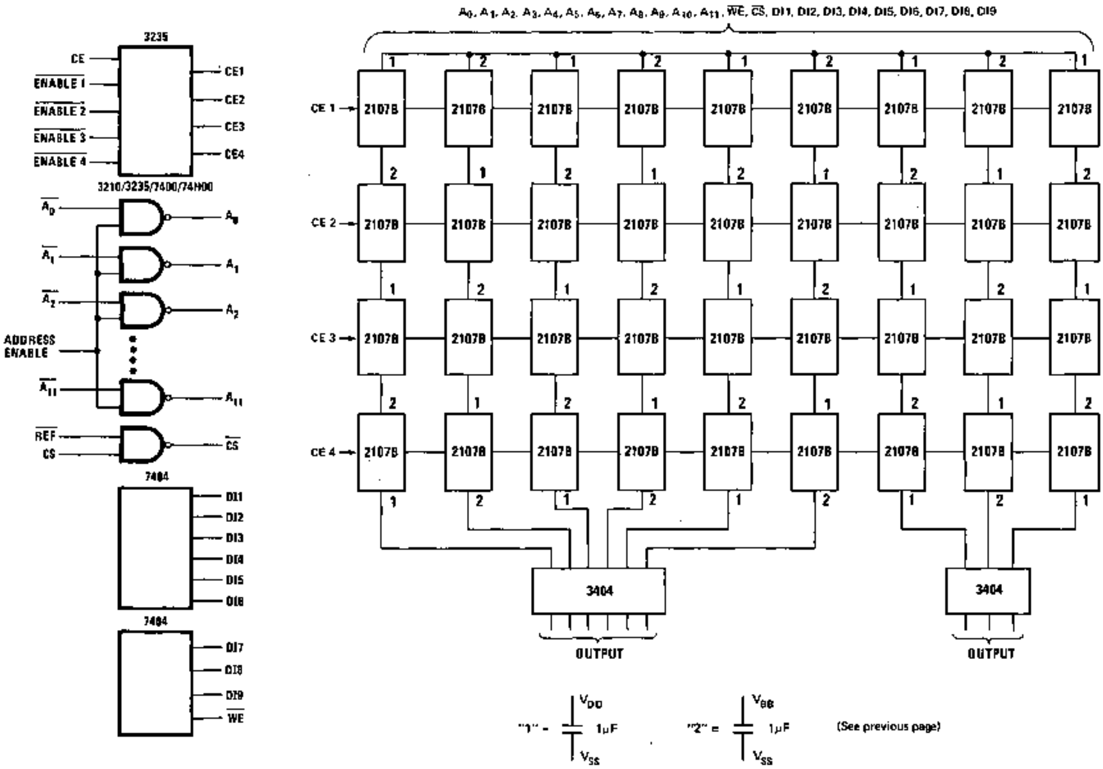
The 2107B is a dynamic RAM therefore when $V_{CE} = V_{ILC}$ very little power is dissipated. In a typical system most devices are in standby with V_{CE} at V_{ILC}. During this time only leakage currents flow (i.e., I_{DD1}, I_{CC1}, I_{BB}, I_{LO}, I_{L1}). The power dissipated during this inactive period is typically 1.4mW. The typical power dissipation required to perform refresh during standby is the refresh duty cycle, 1.3%, multiplied by the operating power dissipation, or 8.6mW. The total power dissipation during standby is then 10.0mW typical.

System Interfaces and Filtering

On the following page is an example of a 16K x 9 bit memory system. Device decoding is done with the CE input. All devices are unselected during refresh with $\overline{CS}$. The 3210, 3230, 3235, and 3404 are standard Intel products. Decoupling is indicated by "1" for V_{DD} to V_{SS} and "2" for V_{BB} to V_{SS}. I_{DD} and I_{BB} current surges at the CE transitions make adequate decoupling of these supplies important. It is recommended that 1µF high frequency, low inductance capacitors be used on double sided boards. V_{CC} to V_{SS} decoupling is required only on the devices located around the periphery of the array. For each 36 devices a 100µF tantalum or equivalent capacitor should be placed from V_{DD} to V_{SS} close to the array.

Typical System

16K X 9 BIT MEMORY CIRCUIT



intel® Silicon Gate MOS **2107B-4**

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

*** Access Time -- 270 ns max.**
*** Read, Write Cycle Times -- 470 ns max.**

The 2107B-4 is a medium speed version of the 2107B. Please refer to page 2-81 for pin configuration, logic symbol, and block diagram. See page 2-82 for absolute maximum ratings and page 2-83 for typical characteristics. Refer to pages 2-85 and 2-86 for timing definitions, page 2-84 for capacitance, and pages 2-87 and 2-88 for applications information.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
$\lvert I_{LO} \rvert$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	μA	CE = -1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on		80	100	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\,AV1}$	Average V_{DD} Current		55	80	mA	Cycle time=470ns, t_{CE} = 300ns T_A = 25°C
$I_{DD\,AV2}$	Average V_{DD} Current		27	40	mA	Cycle time=1000ns, t_{CE} = 300ns
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns — See Figure 4
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

A.C. Characteristics[1] $T_A = 0°C$ to $70°C$, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%,

READ, WRITE, AND READ MODIFY/WRITE CYCLE V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	50		ns	
t_{CC}	CE Off Time	130		ns	
t_T	CE Transition Time	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	470		ns	t_T = 20ns
t_{CE}	CE On Time	300	3000	ns	
t_{CO}	CE Output Delay		250	ns	C_{load} = 50pF, Load = One TTL Gate,
t_{ACC}	Address to Output Access		270	ns	Ref = 2.0V.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	470		ns	t_T = 20ns
t_{CE}	CE On Time	300	3000	ns	
t_W	$\overline{WE}$ to CE Off	150		ns	
t_{CW}	CE to $\overline{WE}$	100		ns	
t_{DW} [2]	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	

Read Modify Write Cycle[1]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	590		ns	t_T = 20ns
t_{CRW}	CE Width During RMW	420	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	C_{load} = 50pF, Load = One TTL Gate, Ref = 2.0V
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		250	ns	
t_{ACC}	Access Time		270	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

NOTE:

1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ≤65% of t_{REF}. For continuous Read-Modify-Write operation, t_{CC} and t_{RWC} should be increased to at least 185ns and 645ns, respectively.

intel® Silicon Gate MOS 2107B-6

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

*** Access Time -- 350 ns max.**

*** Read, Write Cycle Times -- 800 ns max.**

The 2107B-6 is a version of the 2107B which is useful in microcomputer and terminal applications. Please refer to page 2-81 for pin configuration, logic symbol, and block diagram. See page 2-82 for absolute maximum ratings and page 2-83 for typical characteristics. Refer to pages 2-85 and 2-86 for timing definitions, page 2-84 for capacitance and pages 2-87 and 2-88 for applications information.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} [1] = -5V ± 5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS} = V_{IH}$ V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	μA	CE = -1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on		80	100	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV1}$	Average V_{DD} Current		45	70	mA	Cycle time = 800ns. t_{CE} = 380ns T_A = 25°C
I_{CC1} [4]	V_{CC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS} = V_{IH}$
I_{BB}	V_{BB} Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns – See Figure 4
V_{IH}	Input High Voltage	3.5		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

A.C. Characteristics[1] $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to CE Set Up Time	10		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	380		ns	
t_T	CE Transition Time	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	800		ns	$t_T = 20ns$
t_{CE}	CE On Time	380	3000	ns	
t_{CO}	CE Output Delay		320	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		350	ns	Ref = 2.0V.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	800		ns	$t_T = 20ns$
t_{CE}	CE On Time	380	3000	ns	
t_W	$\overline{WE}$ to CE Off	200		ns	
t_{CW}	CE to $\overline{WE}$	150		ns	
t_{DW} [2]	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	100		ns	

Read Modify Write Cycle[1]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	960		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	540	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	200		ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	100		ns	Ref = 2.0V
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		320	ns	
t_{ACC}	Access Time		350	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

NOTES:

1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ≤50% of t_{REF}. For continuous Read-Modify-Write operation t_{CC} and t_{RWC} should be increased to at least 500ns and 1080ns, respectively.

intel® Silicon Gate MOS 2111, 2111-1, 2111-2

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

- **Organization 256 Words by 4 Bits**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Access Time — 0.5 to 1 μsec Max.**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**

The Intel® 2111 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

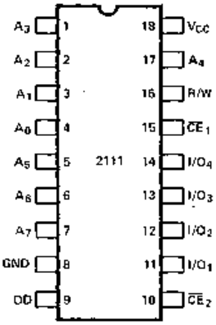
The 2111 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

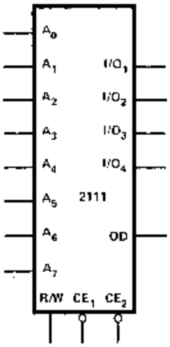
The Intel 2111 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



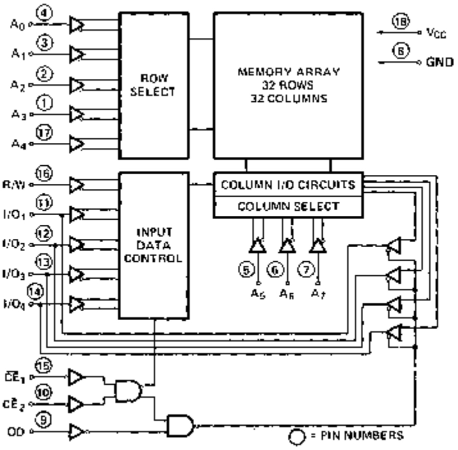
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

**COMMENT:*

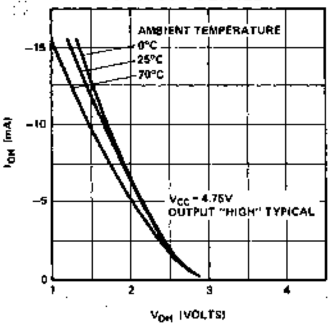
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics for 2111, 2111-1, 2111-2

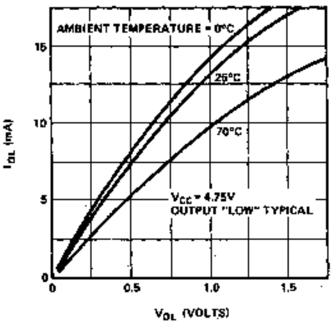
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}_1=\overline{CE}_2$=2.2V, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}_1=\overline{CE}_2$=2.2V, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.2			V	I_{OH} = -150 μA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics for 2111

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			1,000	ns	
t_{CO}	Chip Enable To Output			800	ns	
t_{OD}	Output Disable To Output			700	ns	
t_{DF}[3]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	900			ns	
t_{DW}	Data Setup	700			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	750			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	200			ns	

A. C. CONDITIONS OF TEST

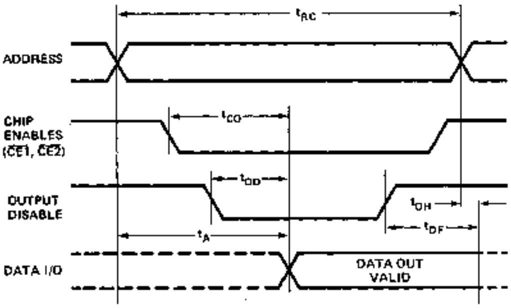
Input Pulse Levels:	+0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100pF

Capacitance[2] $T_A = 25°C$, f = 1MHz

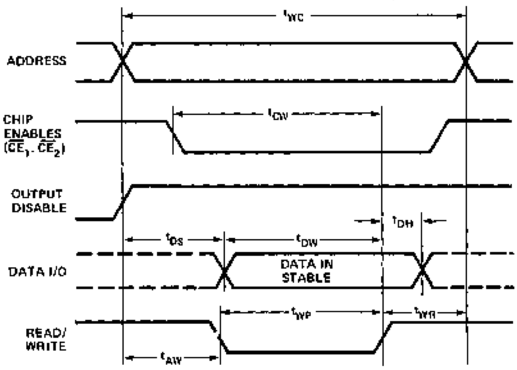
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

2111-1 (500 ns Access Time)

A.C. Characteristics for 2111-1

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			500	ns	
t_{CO}	Chip Enable To Output			350	ns	
t_{OD}	Output Disable To Output			300	ns	
t_{DF}[2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	100			ns	
t_{CW}	Chip Enable To Write	400			ns	
t_{DW}	Data Setup	280			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	300			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

2111-2 (650 ns Access Time)

A.C. Characteristics for 2111-2

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			650	ns	
t_{CO}	Chip Enable To Output			400	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}[2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	150			ns	
t_{CW}	Chip Enable To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

intel® Silicon Gate MOS 2112, 2112-2

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON DATA I/O

- **Organization 256 Words by 4 Bits**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Access Time — 0.65 to 1 μsec Max.**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**

The Intel®2112 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

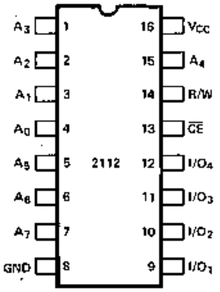
The 2112 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

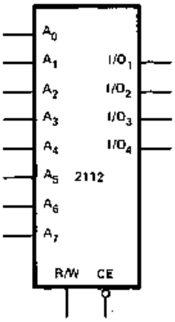
The Intel 2112 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



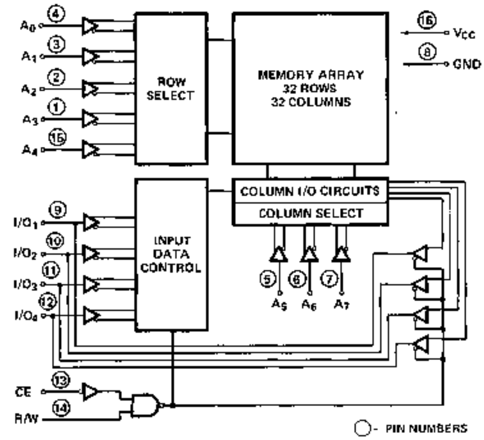
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

**COMMENT:*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics for 2112, 2112-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

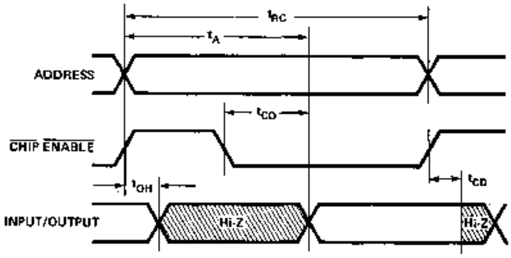
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150μA

A.C. Characteristics for 2112

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	1,000			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			1,000	ns	
t_{CO}	Chip Enable To Output Time			800	ns	
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	

READ CYCLE WAVEFORMS



Capacitance[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics for 2112 (Continued)

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

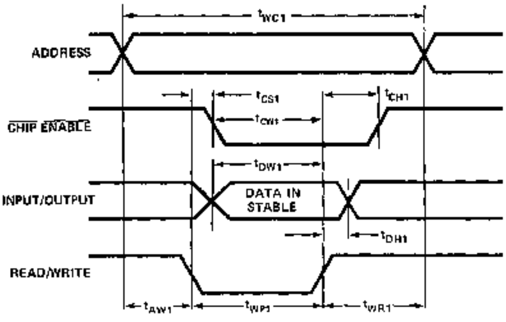
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	850			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW1}	Address To Write Setup Time	150			ns	
t_{DW1}	Write Setup Time	650			ns	
t_{WP1}	Write Pulse Width	650			ns	
t_{CS1}	Chip Enable Setup Time	0			ns	
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	100			ns	
t_{CW1}	Chip Enable To Write Setup Time	650			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

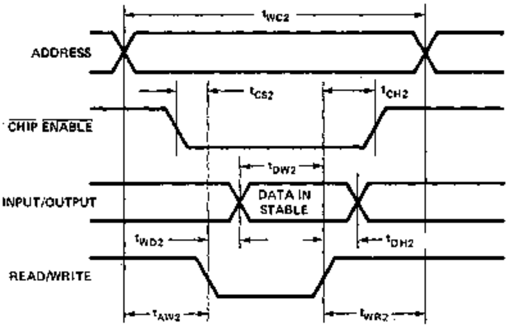
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	1050			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW2}	Address To Write Setup Time	150			ns	
t_{DW2}	Write Setup Time	650			ns	
t_{WD2}	Write To Output Disable Time	200			ns	
t_{CS2}	Chip Enable Setup Time	0			ns	
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	100			ns	

Write Cycle Waveforms

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

2112-2 (650ns Access Time)

A.C. Characteristics for 2112-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			650	ns	
t_{CO}	Chip Enable To Output Time			500	ns	
t_{CD}	Chip Enable To Output Disable Time	0		150	ns	
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	500			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW1}	Address To Write Setup Time	100			ns	
t_{DW1}	Write Setup Time	280			ns	
t_{WP1}	Write Pulse Width	350			ns	
t_{CS1}	Chip Enable Setup Time	0			ns	
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	50			ns	
t_{CW1}	Chip Enable to Write Setup Time	350			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	650			ns	t_r, t_f = 20ns V_{IN} = +0.65V to +2.2V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW2}	Address To Write Setup Time	100			ns	
t_{DW2}	Write Setup Time	280			ns	
t_{WD2}	Write To Output Disable Time	200			ns	
t_{CS2}	Chip Enable Setup Time	0			ns	
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	50			ns	

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

intel® Schottky Bipolar **3101, 3101A**

HIGH SPEED FULLY DECODED 64 BIT MEMORY

- **Fast Access Time -- 35 nsec. max. over 0-75°C Temperature Range.** (3101A)
- **Simple Memory Expansion through Chip Select Input -- 17 nsec. max. over 0-75°C Temperature Range.** (3101A)
- **DTL and TTL Compatible -- Low Input Load Current: 0.25mA. max.**
- **OR-Tie Capability -- Open Collector Outputs.**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration.**

The Intel® 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

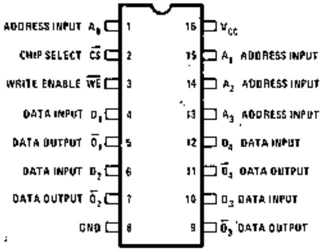
The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0°C to 75°C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

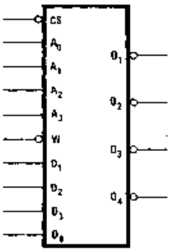
A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

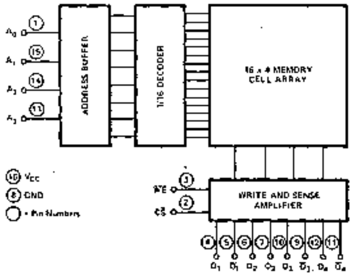
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_1-D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0-A_3	ADDRESS INPUTS	$\overline{O}_1-\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	–	HIGH
HIGH	HIGH	–	HIGH

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

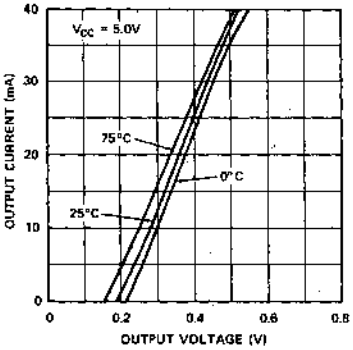
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

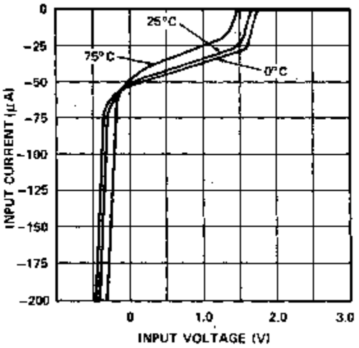
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_{CC}=5.25V, V_D=0.45V
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	V_{CC}=5.25V, V_W=0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	μA	V_{CC}=5.25V, V_A=5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	μA	V_{CC}=5.25V, V_D=5.25V
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	μA	V_{CC}=5.25V, V_W=5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	μA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	V_{CC}=4.75V, I_A=−5.0 mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	V_{CC}=4.75V, I_D=−5.0 mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	V_{CC}=4.75V, I_W=−5.0 mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	V_{CC}=4.75V, I_S=−5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC}=4.75V, I_{OL} = 15 mA Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	μA	V_{CC}=5.25V, V_{CEX}=5.25V V_S=2.5V
I_{CC}	POWER SUPPLY CURRENT		105	mA	V_{CC}=5.25V, V_A=V_S=V_D=0V
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC}=5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC}=5.0V

Typical Characteristics

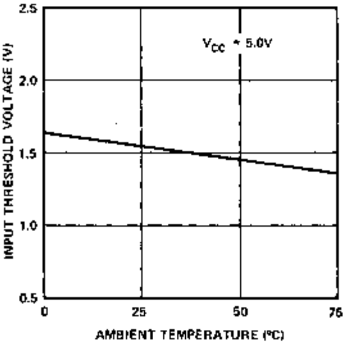
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



Switching Characteristics

Conditions of Test:

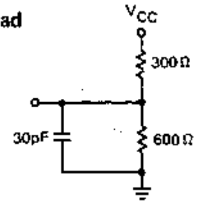
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

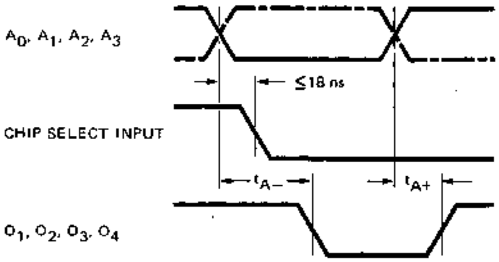
Output loading is 15mA and 30 pF

15 mA Test Load

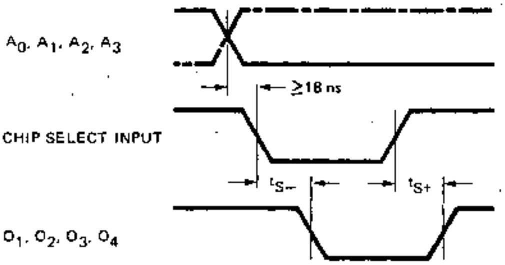


READ CYCLE

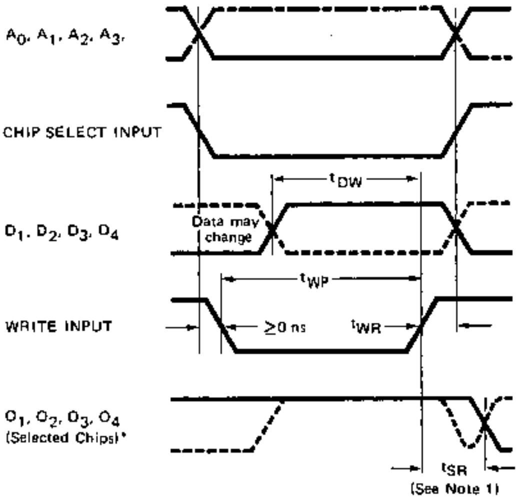
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

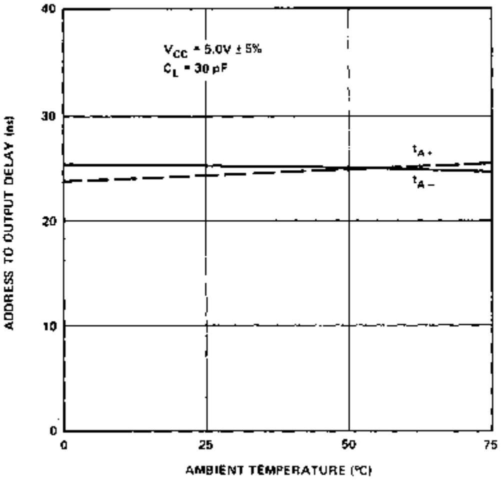
CAPACITANCE[2] T_A = 25° C

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

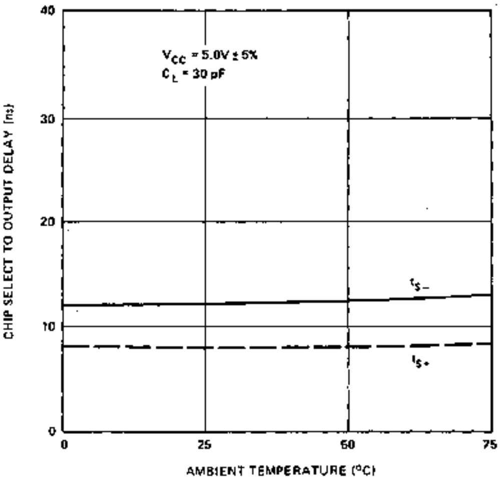
NOTE 2: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

Typical A.C. Characteristics

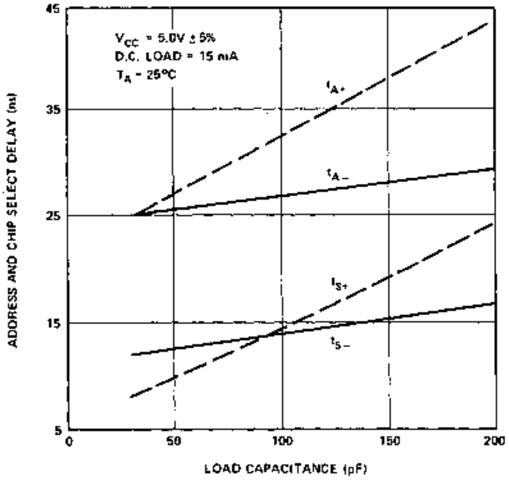
ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



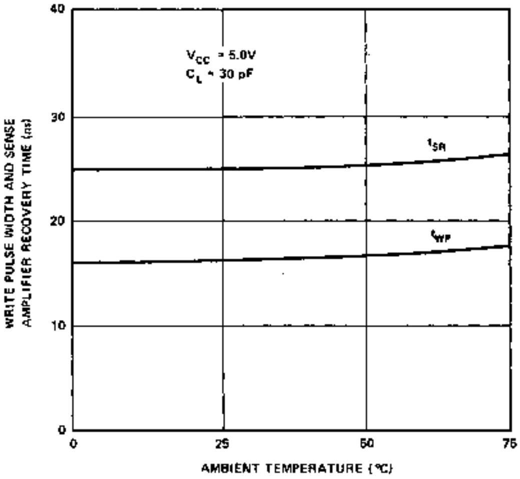
CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE



WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE



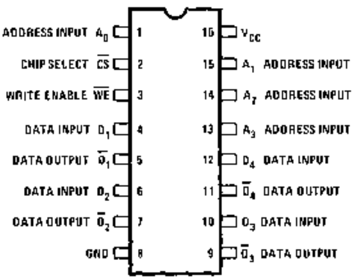
intel® Schottky Bipolar **M3101, M3101A**

HIGH SPEED FULLY DECODED 64 BIT MEMORY

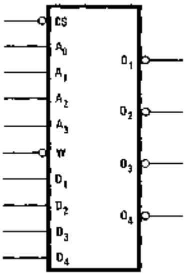
- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time — 45ns Maximum (M3101A)**
- **OR-Tie Capability — Open Collector Outputs**
- **Standard Packaging — 16 Pin Dual In-Line Lead Configuration**

The M3101 and M3101A are military temperature range RAMs, organized as 16 words by 4-bits. Their high speed makes them ideal in scratch pad and small buffer memory applications. The M3101 and M3101A are fabricated with using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 15°C to +55°C
Storage Temperature . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . –0.5V to +7V
Power Dissipation . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	—	HIGH
HIGH	HIGH	—	HIGH

D. C. and Operating Characteristics T_A = –55°C to +125°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FD}	Data Input Load Current		–0.25	mA	V_{CC}=5.25V, V_D=0.45V
I_{FW}	Write Input Load Current		-0.25	mA	V_{CC}=5.25V, V_W=0.45V
I_{FS}	Chip Select Input Load Current		–0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current		10	μA	V_{CC}=5.25V, V_A=5.25V
I_{RD}	Data Input Leakage Current		10	μA	V_{CC}=5.25V, V_D=5.25V
I_{RW}	Write Input Leakage Current		10	μA	V_{CC}=5.25V, V_W=5.25V
I_{RS}	Chip Select Input Leakage Current		10	μA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_A=–5.0mA
V_{CD}	Data Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_D=–5.0mA
V_{CW}	Write Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_W=–5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-1.0	V	V_{CC}=4.75V, I_S=–5.0mA
V_{OL}	Output "Low" Voltage		0.45	V	V_{CC}=4.75V, I_{OL}=10mA Memory Stores "Low"
I_{CEX}	Output Leakage Current		100	μA	V_{CC}=5.25V, V_{CEX}=5.25V, V_S=2.5V
I_{CC}	Power Supply Current		105	mA	V_{CC}=5.25V, V_A=V_S=V_D=0V
V_{IL}	Input "Low" Voltage		0.80	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.1		V	V_{CC}=5.0V

A.C. Characteristics $T_A = -55°C +125°C$, $V_{CC} = 5.0V \pm 5\%$

READ CYCLE					
		3101A		3101	
SYMBOL	PARAMETER	LIMITS (ns)		LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	25	5	55
t_{A-}, t_{A+}	Address to Output Delay	10	45	10	75

WRITE CYCLE					
		3101A		3101	
SYMBOL	TEST	LIMITS (ns)		LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		40		50
t_{WP}	Write Pulse Width	35		40	
t_{DW}	Data-Write Overlap Time	35		40	
t_{WR}	Write Recovery Time	0		0	

CAPACITANCE[1] $T_A = 25°C$

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

NOTE 1: This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1$ MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

Conditions of Test:

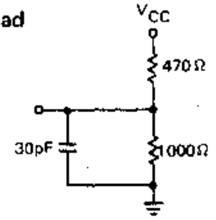
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

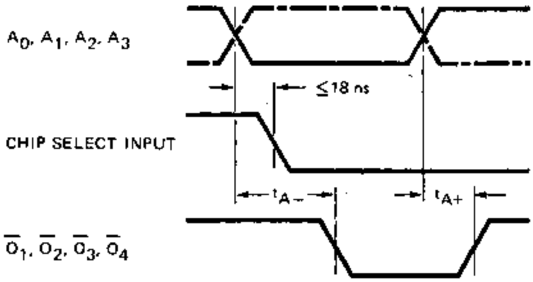
Output loading is 10 mA and 30 pF

10 mA Test Load

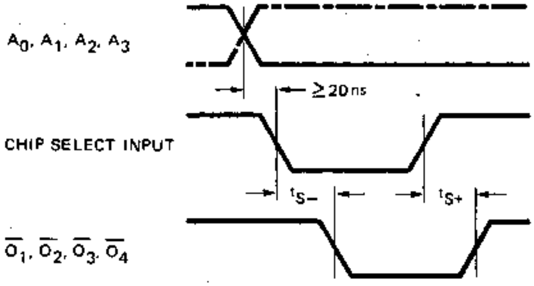


READ CYCLE

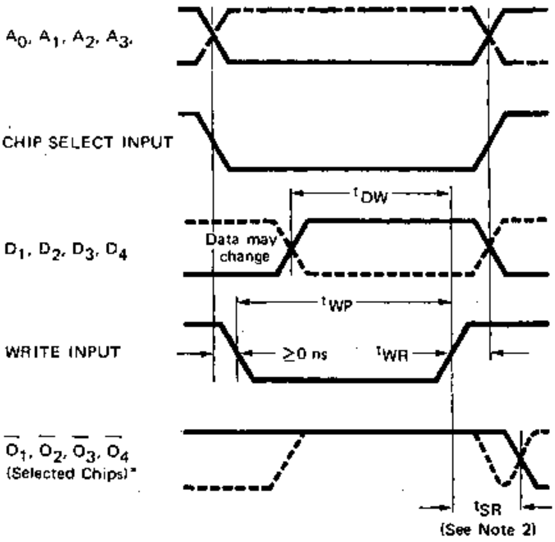
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 2: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

intel®

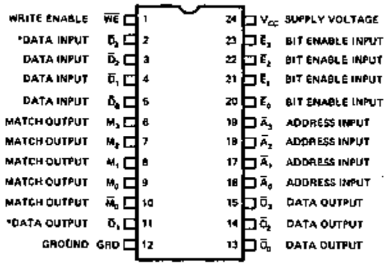
Schottky Bipolar 3104

HIGH SPEED 16 BIT CONTENT ADDRESSABLE MEMORY

- **Organization — 4 Words x 4 Bits**
- **Max. Delay of 30 nsec Over 0° C to 75° C Temperature**
- **Open Collector Outputs — OR Tie Capability**
- **High Current Sinking Capability — 15 mA max.**
- **Low Input Load Current — 0.25 mA max.**
- **DTL & TTL Compatible**
- **Bit Enable Input — Bit Masking**
- **Standard 24 Pin Dual In-Line**

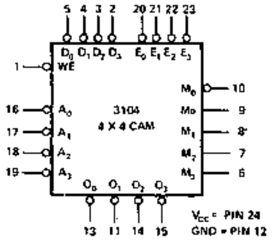
The Intel®3104 is a high speed 16 bit Content Addressable Memory (CAM). It is a linear select 4 word by 4 bit array which is designed to compare data on its inputs with data already stored in its memory and to indicate a match when these data are identical. This equality search is performed on all bits in parallel. The 3104 can also be used as a read/write RAM with linear selection addressing.

PIN CONFIGURATION

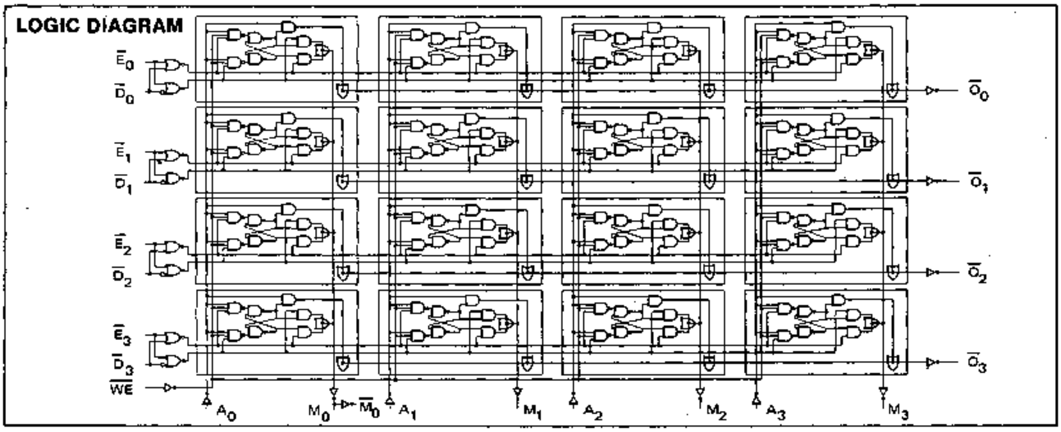


*DATA IN and DATA OUT are of the same logic levels. For a chip that is not selected, the data output is at a high level.

LOGIC SYMBOL



LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

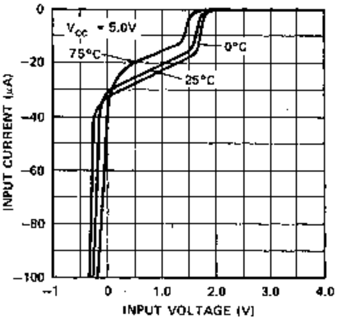
D.C. Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$; unless otherwise specified.

SYMBOL	PARAMETER	LIMIT			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FA}	ADDRESS INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_A = .45V$
I_{FE}	BIT ENABLE INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_E = .45V$
I_{FW}	WRITE ENABLE INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_W = .45V$
I_{FD}	DATA INPUT LOAD CURRENT			−0.25	mA	$V_{CC} = 5.25V$ $V_D = .45V$
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			10	µA	$V_{CC} = 5.25V$ $V_A = 5.25V$
I_{RE}	BIT ENABLE INPUT LEAKAGE CURRENT			10	µA	$V_{CC} = 5.25V$ $V_E = 5.25V$
I_{RW}	WRITE ENABLE INPUT LEAKAGE CURRENT			10	µA	$V_{CC} = 5.25V$ $V_W = 5.25V$
I_{RD}	DATA INPUT LEAKAGE CURRENT			10	µA	$V_{CC} = 5.25V$ $V_D = 5.25V$
I_{CEX}	OUTPUT LEAKAGE CURRENT (ALL OUTPUTS)			50	µA	$V_{CC} = 5.25V$ $V_{CEX} = 5.25V$
V_{OL}	OUTPUT "LOW" VOLTAGE (ALL OUTPUTS)			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 15mA$
V_{IL}	INPUT "LOW" VOLTAGE (ALL INPUTS)			0.85	V	$V_{CC} = 5V$
V_{IH}	INPUT "HIGH" VOLTAGE (ALL INPUTS)	2.0			V	$V_{CC} = 5V$
I_{CC}	POWER SUPPLY CURRENT			125	mA	$V_{CC} = 5.25V$ OUTPUTS HIGH
C_{IN}**	INPUT CAPACITANCE		5		pF	$V_{IN} = +2.0V$, $V_{CC} = 0.0V$ f = 1 MHz
C_{OUT}**	OUTPUT CAPACITANCE		8		pF	$V_{OUT} = +2.0V$, $V_{CC} = 0.0V$ f = 1 MHz

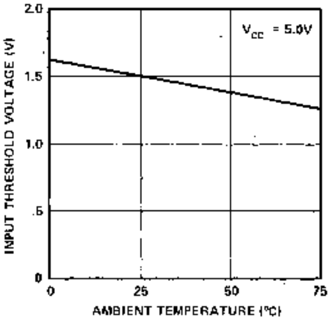
**This parameter is periodically sampled and is not 100% tested.

Typical D.C. Characteristics

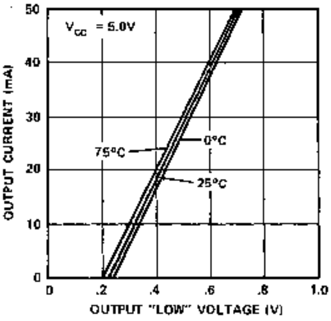
INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



Switching Characteristics

Conditions of Test:

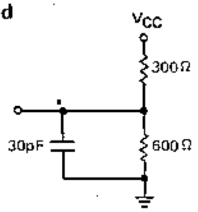
Input Pulse amplitudes · · 2.5V

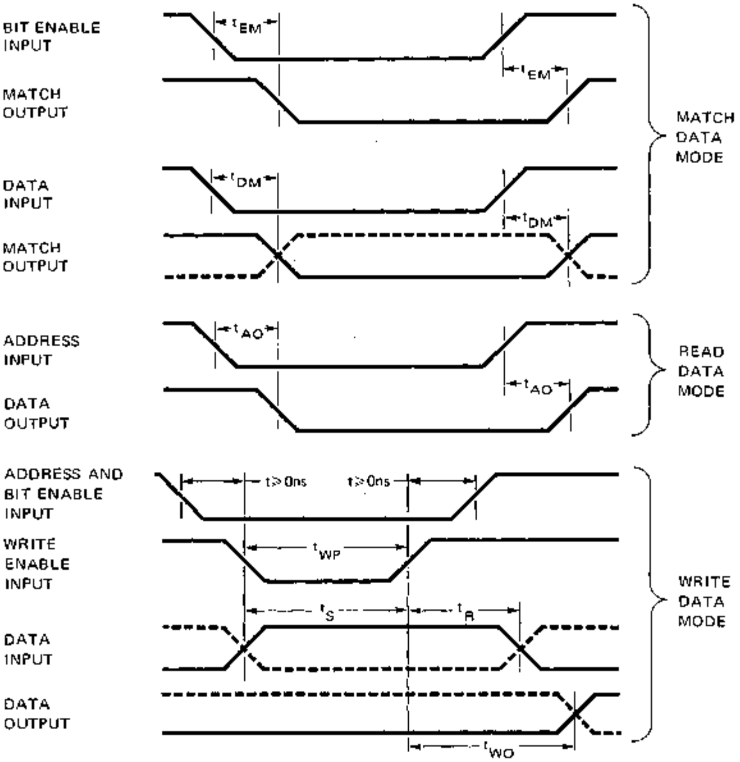
Input pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

Output loading is 15 mA and 30 pF

15mA Test Load





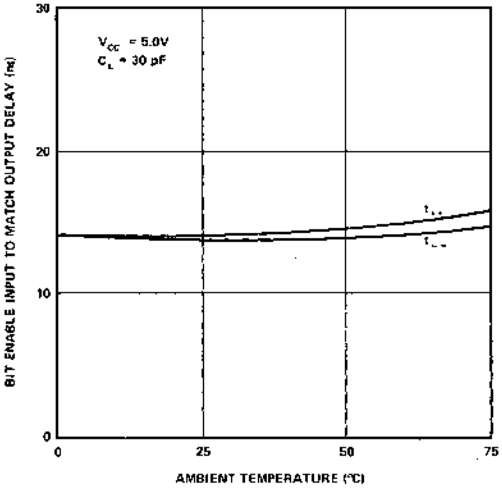
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_{EM}	BIT ENABLE INPUT TO MATCH OUTPUT DELAY		15	30	ns
t_{DM}	DATA INPUT TO MATCH OUTPUT DELAY		16	30	ns
t_{AO}	ADDRESS INPUT TO OUTPUT DELAY		14	30	ns
t_{WP}	WRITE ENABLE PULSE WIDTH	40	25		ns
t_{WO}	WRITE ENABLE TO OUTPUT DELAY		–	40	ns
t_S	SET-UP TIME ON DATA INPUT		–	40	ns
t_R	RELEASE TIME ON DATA INPUT	0	–		ns

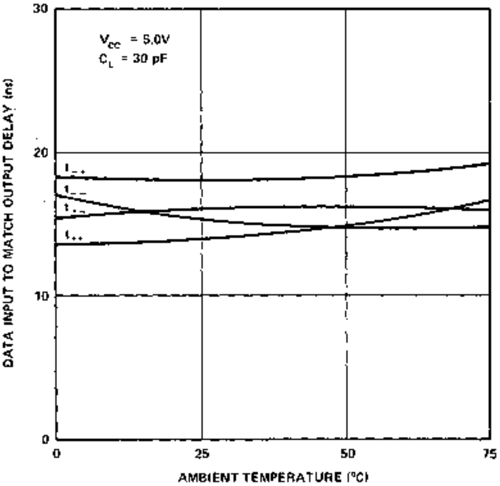
Note 1. Typical values are at nominal voltages and T_A = 25°C.

Typical A.C. Characteristics

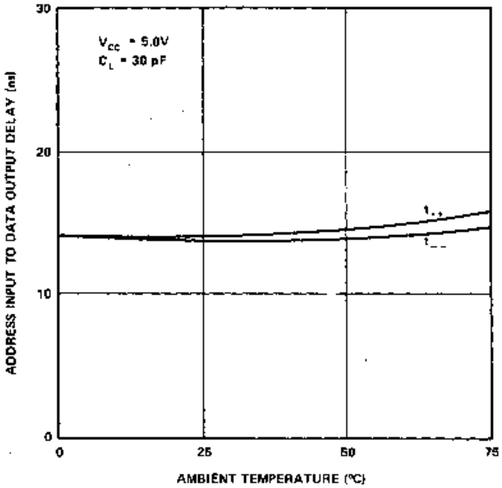
BIT ENABLE INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



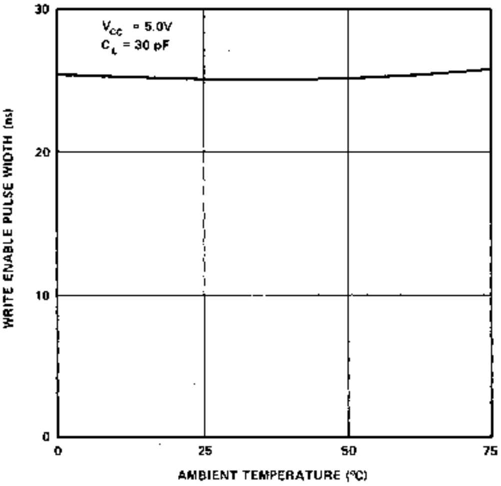
DATA INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



ADDRESS INPUT TO DATA OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. TEMPERATURE



intel® Schottky Bipolar 3106A, 3106, 3106-8, 3107A, 3107, 3107-8

HIGH SPEED FULLY DECODED 256 BIT RAM

- **Fast Access Time—60 nsec max. over 0° to 75° C Temperature Range and ±5% Supply Voltage Tolerance– –3106A and 3107A**
- **Fully Decoded—On Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Low Input Load Current: 0.25mA max.**
- **Open Collector (3107A, 3107, 3107-8) or Three State (3106A, 3106, 3106-8) Output**
- **Simple Memory Expansion through 3 Chip Select Inputs**
- **Minimum Line Reflection—Low Voltage Diode Input Clamp**
- **Standard Packaging--16 Pin DIP**

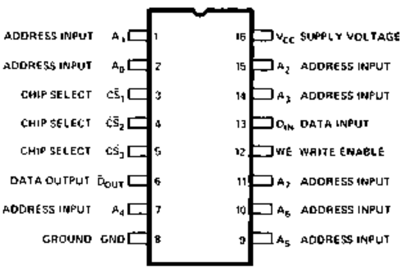
The Intel® 3106A and 3107A family are high speed, fully decoded, 256 bit read/write random access memories. Their organization is 256 words by 1-bit. These devices are designed for high speed scratch pad, buffer, and distributed main memory applications. The 3106A and 3107A are higher speed versions of the 3106 and 3107. The 3106-8 and 3107-8 are ideal for slower performance systems where low system cost is a prime factor.

All devices feature three chip-select inputs. The 3106A, 3106, and 3106-8 have a three-state output and the 3107A, 3107, and 3107-8 provide the user with the popular open collector output. On-chip address decoding and the high speed chip-select facilitate easy memory expansion.

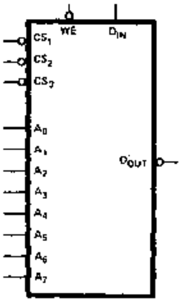
The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process. The performance of these devices is specified over a temperature range from 0°C to +75°C.

The 3106 and 3107 families are compatible with TTL and DTL logic circuits.

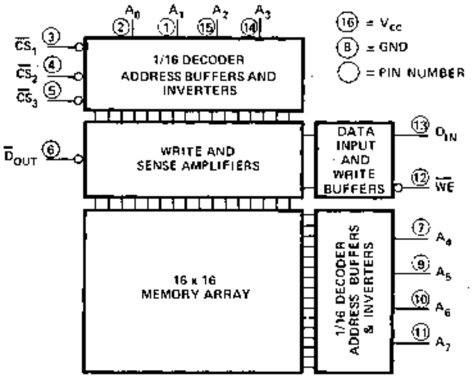
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CS}_1$–$\overline{CS}_3$	CHIP SELECT
A_0–A_7	ADDRESS INPUTS	$\overline{D}_{OUT}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE INPUT		

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
ALL LOW	LOW	WRITE	COMPLEMENT OF DATA INPUT
ALL LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
ONE OR MORE HIGH	DON'T CARE	HOLD	**3106A,3106,3106-8** HIGH IMPEDANCE STATE
			3107A,3107,3107-8 HIGH

Absolute Maximum Ratings*

Temperature Under Bias	−55° C to +125° C
Storage Temperature	−65° C to +160° C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	LIMITS MIN.	TYP.(1)	MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT ALL INPUTS			−0.25	mA	V_{CC} = 5.25V V_{IN} = 0.45V
I_R	INPUT LEAKAGE CURRENT, ALL INPUTS			10	μA	V_{CC} = 4.75V V_R = 5.25V
V_C	INPUT CLAMP VOLTAGE, ALL INPUTS			−1.0	V	V_{CC} = 4.75V I_{IN} = −5.0 mA
V_{OL}	OUTPUT LOW VOLTAGE			0.45	V	V_{CC} = 4.75V I_{OL} = 15 mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC} = V_{CEX} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		90	130	mA	V_{CC} = 5.25V ALL INPUTS OPEN
V_{IL}	INPUT LOW VOLTAGE			0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT HIGH VOLTAGE	2.0			V	
3106A, 3106, 3106-8 ONLY						
$\|I_O\|$	OUTPUT LEAKAGE FOR HIGH IMPEDANCE STATE			100	μA	V_{CC} = 5.25V V_O = 0.45V/5.25V
I_{SC}	OUTPUT SHORT CIRCUIT CURRENT	−15		−65	mA	V_O = 0V V_{CC} = 5V
V_{OH}	OUTPUT HIGH VOLTAGE	2.4			V	I_O = 3.2 mA V_{CC} = 4.75V

(1) Typical values are for T_A = 25° C and nominal supply voltages.

A.C. Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$ unless otherwise specified.

READ CYCLE					
			LIMITS (ns)		
SYMBOL	TEST		MIN.	TYP.	MAX.
t_{A-} t_{A+}	ADDRESS TO OUTPUT DELAY (ALL CHIP SELECTS LOW)	3106A/3107A	15	40	60
		3106, 3107, 3106-8,3107-8	15	50	80
t_{S-} t_{S+}	CHIP SELECT TO OUTPUT DELAY (ALL ADDRESS INPUTS STABLE)		5	25	40

WRITE CYCLE					
			LIMITS (ns)		
SYMBOL	TEST		MIN.	TYP.	MAX.
t_{WP}	WRITE ENABLE PULSE WIDTH	3106A,3107A	50	35	
		3106,3107	60	45	
		3106-8,3107-8	80	70	
t_{SR}	TIME INPUT DATA APPEARS AT THE OUTPUT FOLLOWING A WRITE COMMAND. $t_{WP} \geq$ MIN. LIMIT			10	25

3106A, 3106, 3106-8 ONLY

SYMBOL	TEST	MIN.	MAX.
t_{ON}	TIME OUTPUT REACHES LOW IMPEDANCE STATE AFTER CHIP ENABLED	0	
t_{OFF}	TIME OUTPUT REACHES HIGH IMPEDANCE STATE AFTER CHIP DISABLED		20

CAPACITANCE, $T_A = 25°C$

			LIMITS (pF)	
SYMBOL	TEST	PACKAGE	TYP.	MAX.
C_{IN}*	INPUT CAPACITANCE (ALL INPUT PINS) ALL DEVICES	PLASTIC	6	8
		CERDIP	7	10
C_{OUT}*	OUTPUT CAPACITANCE ALL DEVICES	PLASTIC	8	11
		CERDIP	9	13

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

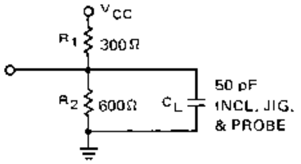
Conditions of Test:

Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times:
5 nanoseconds between 1 volt
and 2 volts

Measurements made at 1.5 volt level

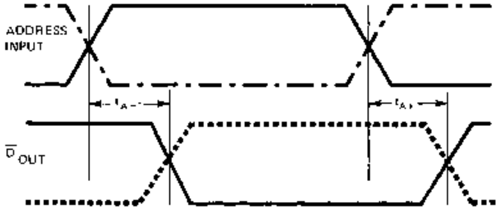
Test Load



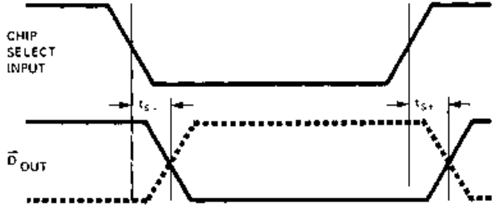
Waveforms

READ CYCLE

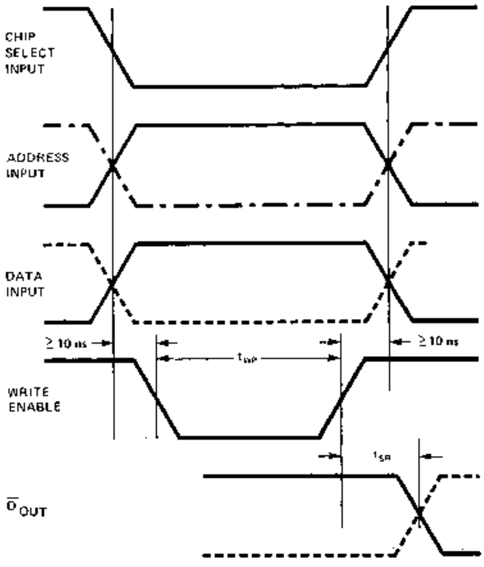
ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY

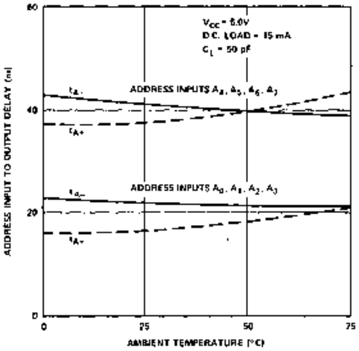


WRITE CYCLE

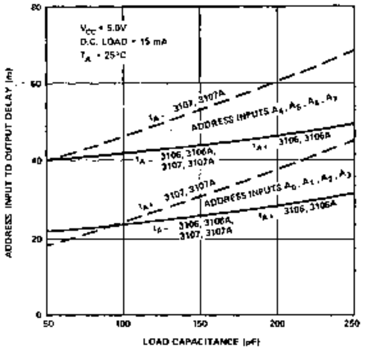


Typical A. C. Characteristics

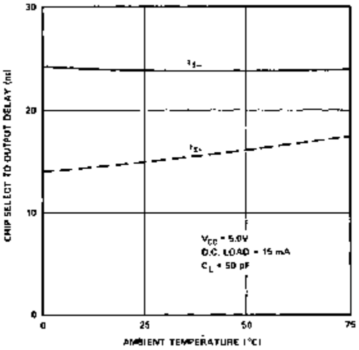
ADDRESS INPUT TO OUTPUT DELAY
VS TEMPERATURE
(3106, 3106A, 3107, 3107A)



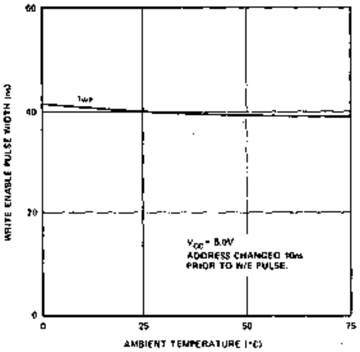
ADDRESS INPUT TO OUTPUT DELAY
VS LOAD CAPACITANCE
(3106, 3106A, 3107, 3107A)



CHIP SELECT TO OUTPUT DELAY
VS TEMPERATURE
(3106, 3106A, 3107, 3107A)

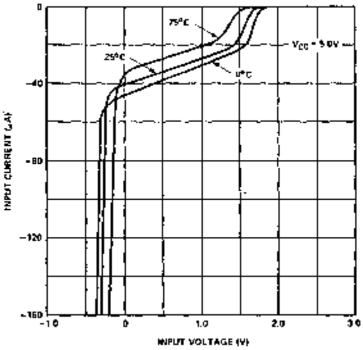


WRITE ENABLE PULSE WIDTH
VS TEMPERATURE
(3106, 3106A, 3107, 3107A)

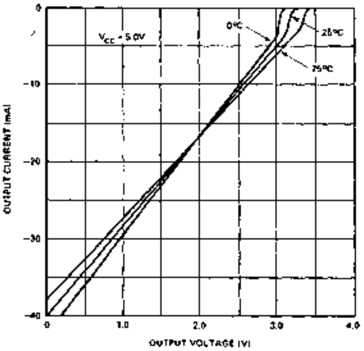


Typical D. C. Characteristics

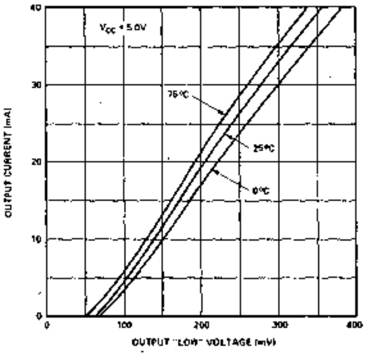
INPUT CURRENT VS
INPUT VOLTAGE
(3106, 3106A, 3107, 3107A)



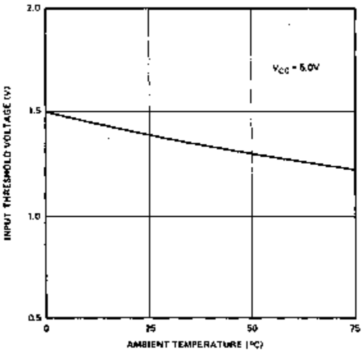
OUTPUT "HIGH" VOLTAGE VS
OUTPUT CURRENT
(3106 & 3106A ONLY)



OUTPUT "LOW" VOLTAGE VS
OUTPUT CURRENT
(3106, 3106A, 3107, 3107A)



INPUT THRESHOLD VOLTAGE VS
TEMPERATURE
(3106, 3106A, 3107, 3107A)



intel® Silicon Gate CMOS 5101, 5101-3, 5101L, 5101L-3

1024 BIT (256 x 4) STATIC CMOS RAM

*Ultra Low Standby Current: 15 nA/Bit for the 5101

- **Fast Access Time — 650 ns**
- **Single +5 V Power Supply**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Three-State Output**

The Intel®5101 and 5101-3 are ultra-low power 1024 bit (256 words x 4-bits) static RAMs fabricated with an advanced ion-implanted silicon gate CMOS technology. The devices have two chip enable inputs. Minimum standby current is drawn by these devices when CE_2 is at a low level. When deselected the 5101 and 5101-3 draw from the single 5 volt supply only 15 microamps and 200 microamps, respectively. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 and 5101-3 use fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 and 5101-3 have separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

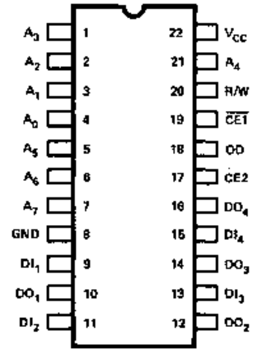
The 5101L and 5101L-3 are identical to the 5101 and 5101-3, respectively, with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

A pin compatible N-channel static RAM, the Intel 2101, is also available for low cost applications where a 256 x 4 organization is needed.

The Intel ion-implanted, silicon gate, complementary MOS (CMOS) allows the design and production of ultra-low power, high performance memories.

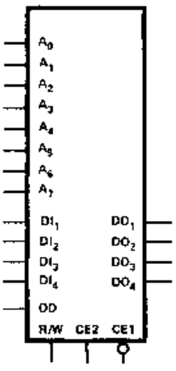
PIN CONFIGURATION

5101



LOGIC SYMBOL

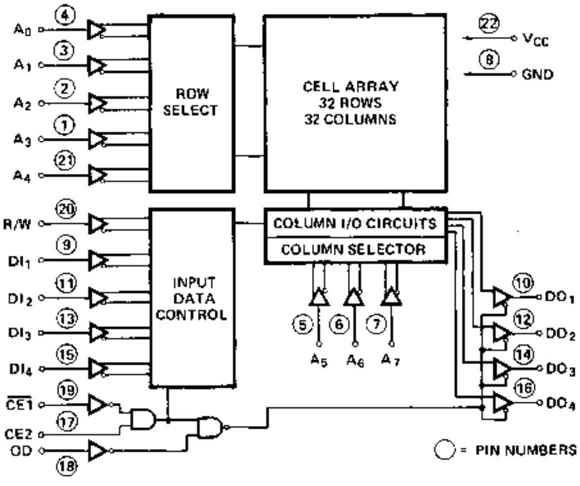
5101



PIN NAMES

DI_1 - DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 – A_7	ADDRESS INPUTS	DO_1 – DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	+7.0V
Power Dissipation	1 Watt

**COMMENT:*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics for 5101, 5101-3, 5101L, 5101L-3

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		5		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0.0V
I_{CC1}	Operating Current		9	22	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ≤ 0.01 Outputs Open
I_{CC2}	Operating Current		13	27	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ≤ 0.01 Outputs Open
5101 I_{CCL}[2]	Standby Current		0.2	15	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
5101-3 I_{CCL}[2]	Standby Current		1	200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = 1.0mA

Low V_{CC} Data Retention Characteristics (For 5101L and 5101L-3) T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V	
5101L I_{CCDR}	Data Retention Current		0.14		μA		V_{DR} = 2.0V
5101L-3 I_{CCDR}	Data Retention Current		0.70		μA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL} measurement. 3. t_{RC} = Read Cycle Time.

A.C. Characteristics for 5101, 5101-3, 5101L, 5101L-3

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	(See below)
t_A	Access Time			650	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			600	ns	
t_{CO2}	Chip Enable (CE2) to Output			700	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

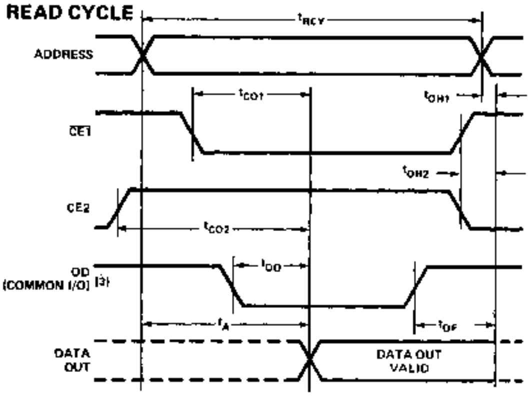
Input Pulse Levels:	+0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20nsec
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and $C_L = 100pF$

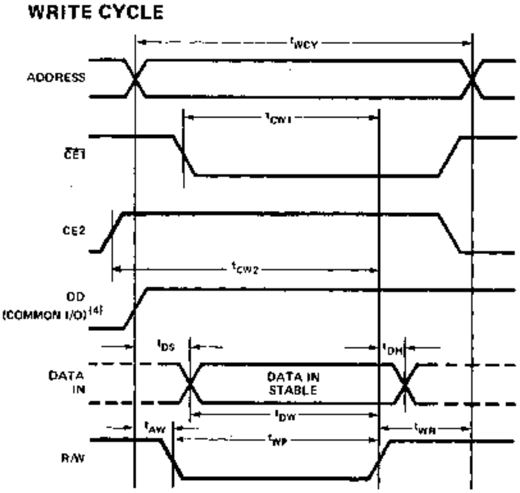
Capacitance[2] $T_A = 25°C$, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. OD may be tied low for separate I/O operation.
4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

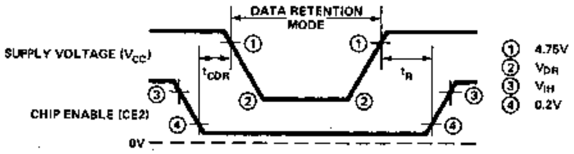
Waveforms



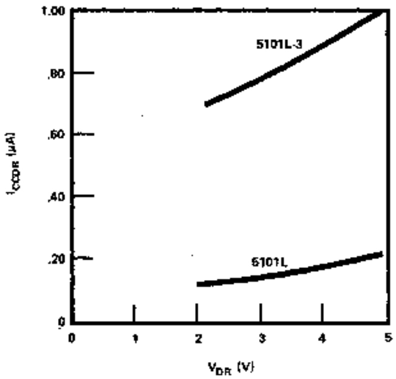


NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. OD may be tied low for separate I/O operation.
4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

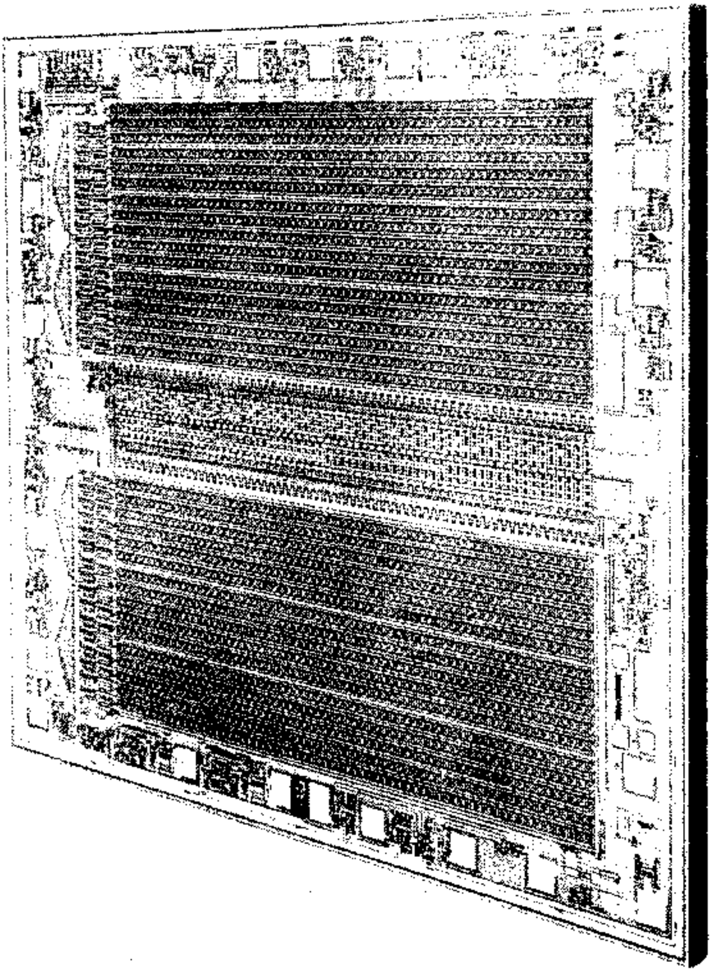
Low V_{CC} Data Retention



Typical I_{CCDR} vs. V_{DR}



READ ONLY MEMORIES



READ ONLY MEMORIES

	Type	No. of Bits	Description	Organization	Electrical Characteristics over Temperature			
					Access Time	Power Dissipation Max.	Supplies (V)	Page No.
SILICON GATE MOS	1302	2048	Mask Programmable (Static)	256 x 8	1.0µs	700mW	+5, –9	3-3
	1602A	2048	Electrically Programmable (Static)	256 x 8	1.0µs	700mW	+5, –9	3-7
	1702A	2048	Erasable Electrically Programmable (Static)	256 x 8	1.0µs	700mW	+5, –9	3-7
	1602A-6	2048	Electrically Programmable (Static)	256 x 8	1.5µs	700mW	+5, –9	3-14
	1702A-6	2048	Erasable Electrically Programmable (Static)	256 x 8	1.5µs	700mW	+5, –9	3-14
	2308	8192	Mask Programmable	1024 x 8	.5µs	700mW	+12, ±5	3-17
	2316A	16,384	Mask Programmable	2048 x 8	.85µs	500mW	+5	3-18
	2704	4096	Erasable and Electrically Programmable	512 x 8	.5µs	750mW	+12, ±5	3-19
	2708	8192	Erasable and Electrically Programmable	1024 x 8	.5µs	750mW	+12, ±5	3-19
SCHOTTKY BIPOLAR	3301A	1024	High Speed, Mask Programmable	256 x 4	45ns	625mW	+5	3-21
	M3301A	1024	–55°C to 125°C ROM	256 x 4	60ns	625mW	+5	3-25
	3302	2048	High Speed, Open Collector ROM	512 x 4	70ns	650mW	+5	3-33
	3302-4	2048	Open Collector ROM	512 x 4	90ns	650mW	+5	3-33
	3302-6	2048	Low Standby Power ROM	512 x 4	90ns	575mW/240mW	+5	3-33
	3322	2048	High Speed, Three State ROM	512 x 4	70ns	650mW	+5	3-33
	3322-4	2048	Three State ROM	512 x 4	90ns	650mW	+5	3-33
	3322-6	2048	Low Standby Power ROM	512 x 4	90ns	575mW/240mW	+5	3-33
	3304A	4096	High Speed, Open Collector	512 x 8	70ns	950mW	+5	3-35
	3304A-4	4096	Open Collector ROM	512 x 8	90ns	950mW	+5	3-35
	3304A-6	4096	Low Standby Power ROM	512 x 8	90ns	700mW/225mW	+5	3-35
	3324A	4096	High Speed, Three State ROM	512 x 8	70ns	950mW	+5	3-35
	3324A-4	4096	Three State ROM	512 x 8	90ns	950mW	+5	3-35
	3601	1024	High Density PROM	256 x 4	70ns	650mW	+5	3-27
	3601-1	1024	High Speed PROM	256 x 4	50ns	650mW	+5	3-27
	M3601	1024	–55°C to 125°C PROM	256 x 4	90ns	650mW	+5	3-31
	3602	2048	High Speed, Open Collector PROM	512 x 4	70ns	650mW	+5	3-34
	3602-4	2048	High Density, Open Collector PROM	512 x 4	90ns	650mW	+5	3-34
	3602-6	2048	Low Standby Power PROM	512 x 4	90ns	650mW/240mW	+5	3-34
	3622	2048	High Speed, Three State PROM	512 x 4	70ns	650mW	+5	3-34
	3622-4	2048	High Density, Three State PROM	512 x 4	90ns	650mW	+5	3-34
	3622-6	2048	Low Standby Power PROM	512 x 4	90ns	650mW/240mW	+5	3-34
	3604	4096	High Speed, Open Collector PROM	512 x 8	70ns	950mW	+5	3-36
	3604-4	4096	High Density, Open Collector PROM	512 x 8	90ns	950mW	+5	3-36
	3604-6	4096	Low Standby Power PROM	512 x 8	90ns	700mW/225mW	+5	3-36
	3624	4096	High Speed, Three State PROM	512 x 8	70ns	950mW	+5	3-40
	3624-4	4096	High Density, Three State PROM	512 x 8	90ns	950mW	+5	3-40

Silicon Gate MOS **1302**

2048 BIT MASK PROGRAMMABLE READ ONLY MEMORY

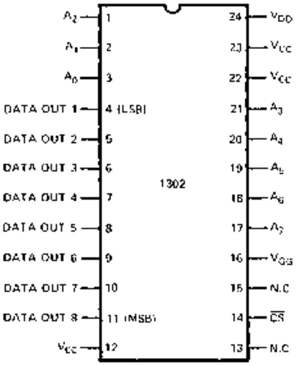
- **Fully Decoded, 256x8 Organization**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-state Output -- OR-tie Capability**
- **Static MOS -- No Clocks Required**
- **Simple Memory Expansion -- Chip Select Input Lead**
- **24-pin Dual-In-Line Hermetically Sealed Ceramic Package**

The Intel®1302 is a fully decoded 256 word by 8-bit metal mask ROM. It is ideal for large volume production runs of systems initially using the 1702A erasable and electrically programmable ROM. The 1302 has the same pinning as the 1602A/1702A.

The 1302 is entirely static — no clocks are required. Inputs and outputs of the 1302 are DTL and TTL compatible. The output is three-state for OR-tie capability. A separate chip select input allows easy memory expansion. The 1302 is packaged in a 24 pin dual-in-line hermetically sealed ceramic package.

The 1302 is fabricated with p-channel silicon gate technology. This low threshold allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

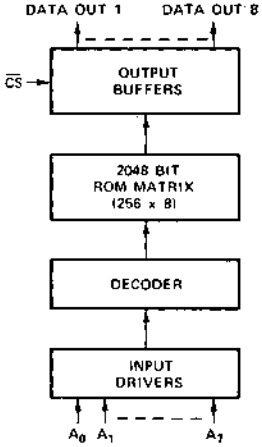
PIN CONFIGURATION



PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: LOGIC 1 AT INPUT AND OUTPUT IS A HIGH AND LOGIC 0 IS LOW.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +125°C
Soldering Temperature of Leads (10 sec)	+300°C
Power Dissipation	2 Watts
Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, $V_{GG}^{(1)}$ = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS	
I_{LI}	Address and Chip Select Input Load Current			1	μA	V_{IN} = 0.0V	
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0.0V, $\overline{CS} = V_{CC} - 2$	
I_{DD0}	Power Supply Current		5	10	mA	$V_{GG}=V_{CC}$, $\overline{CS}=V_{CC}-2$ I_{OL} = 0.0mA, T_A = 25°C	
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}=V_{CC}-2$ I_{OL} = 0.0mA, T_A = 25°C	Continuous Operation
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0 I_{OL} = 0.0mA, T_A = 25°C	
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}=V_{CC}-2$ I_{OL} = 0.0mA, T_A = 0°C	
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C	
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C	
I_{GG}	Gate Supply Current			1	μA		
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V		
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V		
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}−2		V_{CC} +0.3	V		
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V	
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V	
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA	
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 μA	

Note 1. V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle.

Note 2. Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		.700	1	μs
t_{OVGG}	Clocked V_{GG} set up	1			μs
t_{CS}	Chip select delay			200	ns
t_{CO}	Output delay from $\overline{CS}$			500	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	μs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS	
C_{IN}	Input Capacitance		5	10	pF	$V_{IN} = V_{CC}$ $\overline{CS} = V_{CC}$ $V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$	All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		5	10	pF		
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF		

*This parameter is periodically sampled and is not 100% tested.

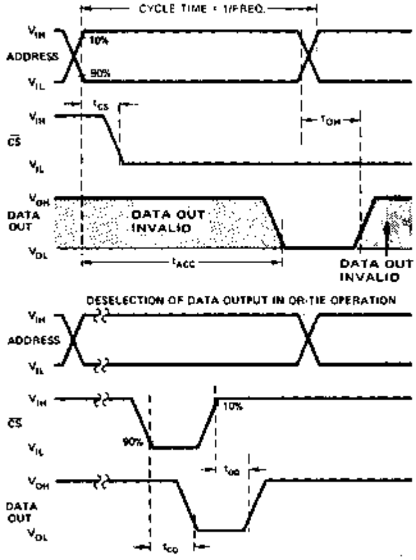
Switching Characteristics

Conditions of Test:

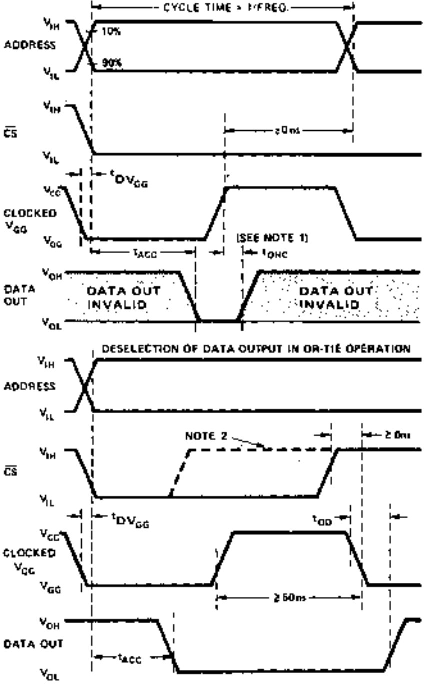
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤ 15 ns)

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation

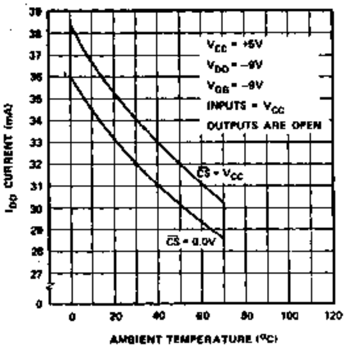


NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

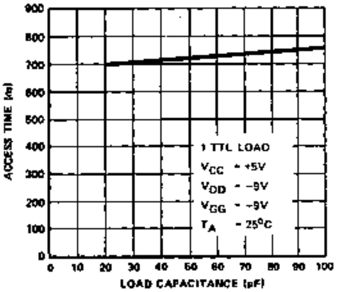
NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

Typical Characteristics

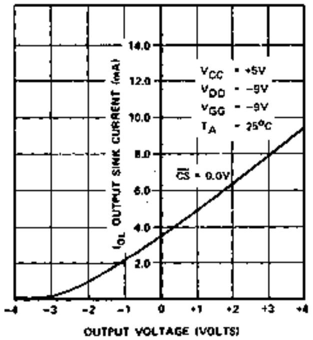
I_{DD} CURRENT VS. TEMPERATURE



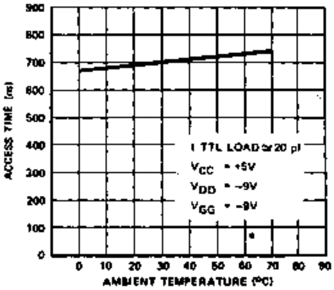
ACCESS TIME VS. LOAD CAPACITANCE



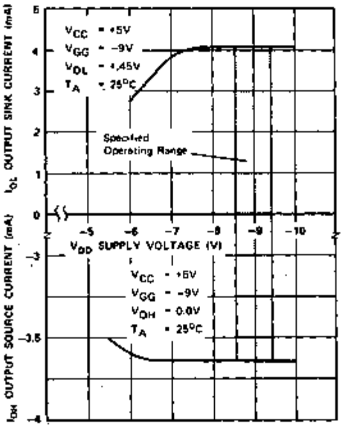
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



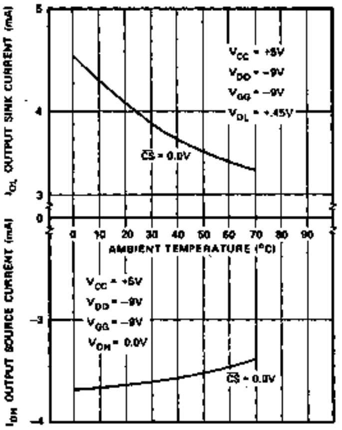
ACCESS TIME VS. TEMPERATURE



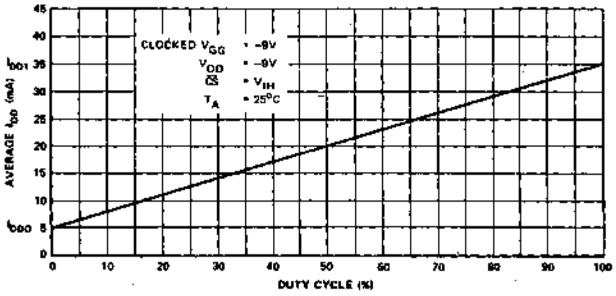
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



OUTPUT CURRENT VS. TEMPERATURE



AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



intel® Silicon Gate MOS **1602A/1702A**

2048 BIT ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

1602A–ELECTRICALLY PROGRAMMABLE
1702A–ERASABLE & ELECTRICALLY REPROGRAMMABLE

- **Fast Programming -- 2 minutes for all 2048 bits**
- **All 2048 bits guaranteed* programmable -- 100% factory tested**
- **Fully Decoded, 256x8 organization**
- **Static MOS -- No Clocks Required**
- **Inputs and Outputs DTL and TTL compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip select input lead**

The 1602A and 1702A are 256 word by 8-bit electrically programmable ROMs ideally suited for uses where fast turn-around and pattern experimentation are important. The 1602A and 1702A undergo complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

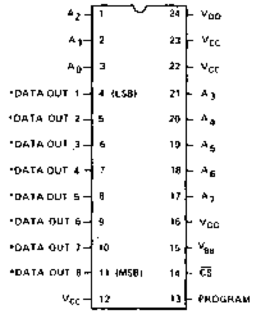
The 1602A and 1702A use identical chips. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The 1602A is packaged in a 24 pin dual in-line package with a metal lid and is not erasable.

The circuitry of the 1602A/1702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs of systems initially using the 1602A or 1702A.

The 1602A/1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



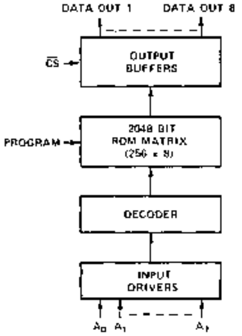
*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

See page 3-8 for operational connection.

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

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*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONNECTIONS

The external lead connections to the 1602A/1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1-8 are pins 4-11 respectively.

PIN MODE	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +125°C
Soldering Temperature of Leads (10 sec)	+300°C
Power Dissipation	2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC}	−48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, V_{GG}[1] = −9V±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C.

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DD0}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2 I_{OL} = 0.0mA, T_A = 25°C — Note 1
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0 I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			1	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}−2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

NOTE 1: POWER-DOWN OPTION: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option please specify 1702AL or 1602AL.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} set up (Note 1)	1			μs
t_{CS}	Chip select delay			100	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	μs

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS	
C_{IN}	Input Capacitance		8	15	pF	V_{IN} = V_{CC}	All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	$\overline{CS}$ = V_{CC} V_{OUT} = V_{CC}	
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)			30	pF	V_{GG} = V_{CC}	

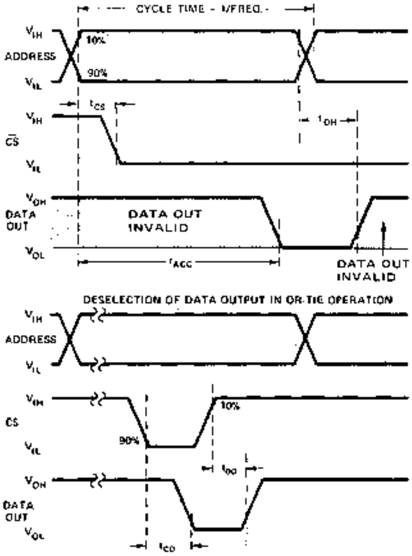
*This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

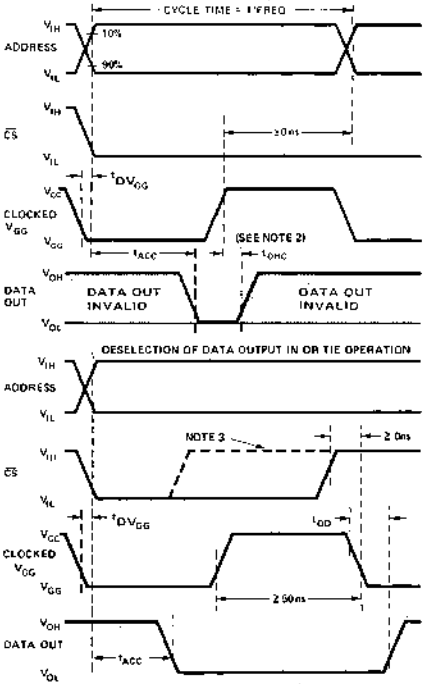
Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) Constant V_{GG} Operation



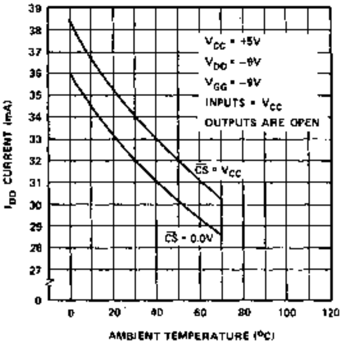
B) Power-Down Option (See Note 1)



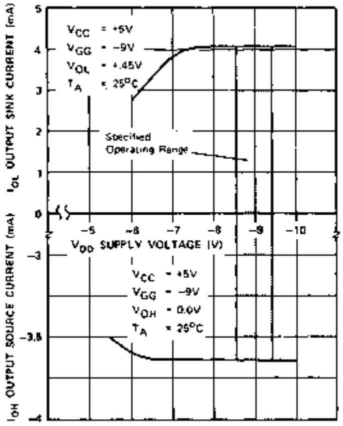
NOTE 2: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

NOTE 3: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

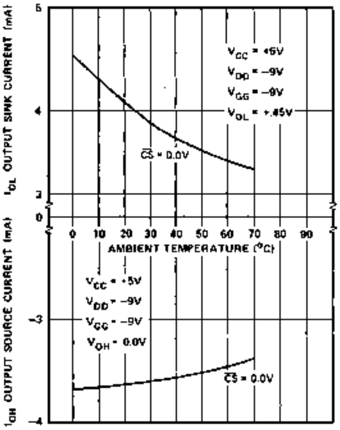
Typical Characteristics



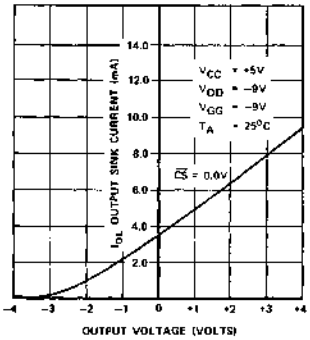
I_{DD} CURRENT VS. TEMPERATURE



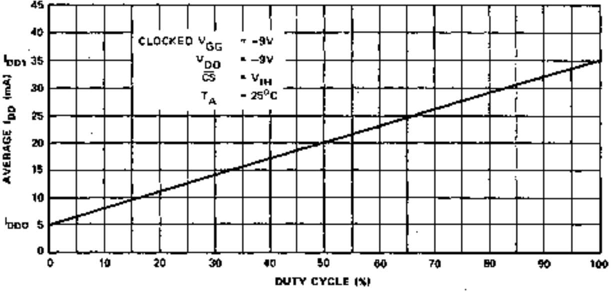
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



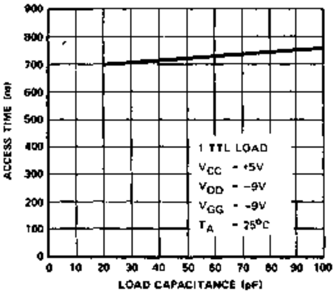
OUTPUT CURRENT VS. TEMPERATURE



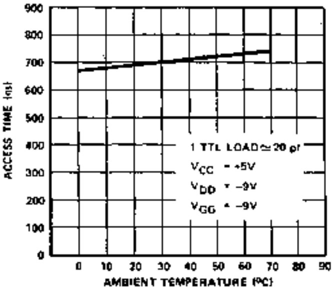
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG} (Note 1)



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE

PROGRAMMING OPERATION

D.C. and Operating Characteristics for Programming Operation

T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = −48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = −48V
I_{BB}	V_{BB} Supply Load Current		10		mA	(Note 5)
I_{DDP}	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{prog} = −48V V_{GG} = −35V (Note 4)
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−46		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−46		−48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100mA max. current to prevent damage to the device.

A.C. Characteristics for Programming Operation

$T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width			3	ms	V_{GG} = −35V, V_{DD} = V_{prog} = −48V
t_{DW}	Data Set Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW} (6)	Address Complement Set Up	25			μs	
t_{ACH} (6)	Address Complement Hold	25			μs	
t_{ATW}	Address True Set Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

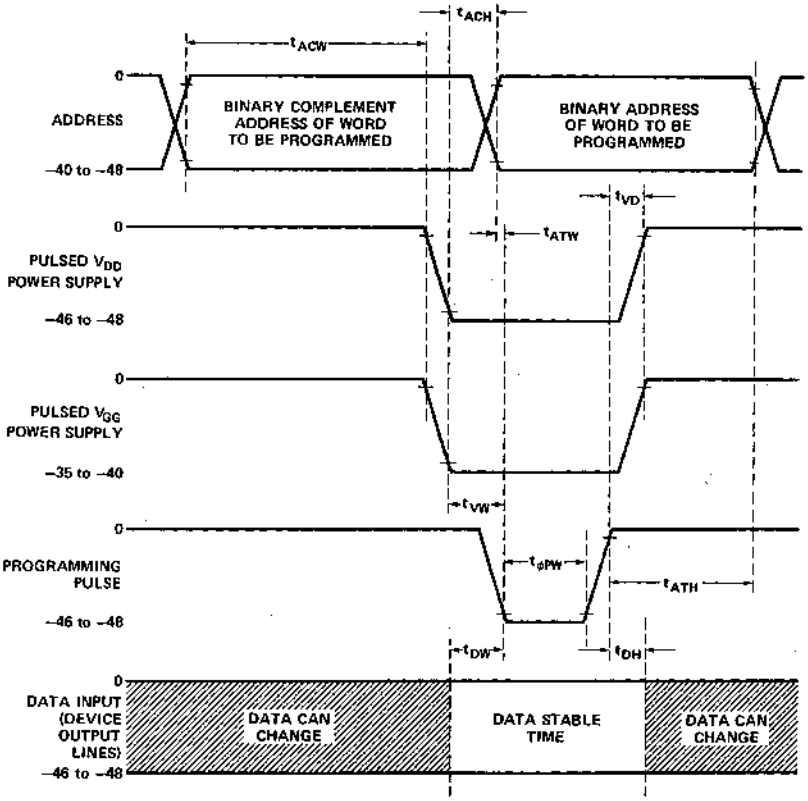
Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0 through 255) must be programmed as shown in the timing diagram for a minimum of 32 times.

Switching Characteristics for Programming Operation

Conditions of Test:

Input pulse rise and fall times ≤ 1μsec
$\overline{CS}$ = 0V

PROGRAM WAVEFORMS



OPERATION OF THE 1602A/1702A IN PROGRAM MODE

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table on page 3-11 for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (-48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 3-11). All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

1702A ERASING PROCEDURE

The 1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W-sec/cm^2. Examples of ultraviolet sources which can erase the 1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the 1702A to be erased should be placed about one inch away from the lamp tubes.

intel® Silicon Gate MOS 1602A-6/1702A-6

2048 BIT ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

1602A-6 ELECTRICALLY PROGRAMMABLE
1702A-6 ERASABLE & ELECTRICALLY REPROGRAMMABLE

- **Fast Programming -- 2 minutes for all 2048 bits**
- **All 2048 bits guaranteed* programmable -- 100% factory tested**
- **Fully Decoded, 256x8 organization**
- **Static MOS -- No Clocks Required**
- **Inputs and Outputs DTL and TTL compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip select input lead**
- **1.5 μs Access Time**

The 1602A-6 and 1702A-6 are 256 word by 8-bit electrically programmable ROMs ideally suited for uses where fast turn-around and pattern experimentation are important. The 1602A-6 and 1702A-6 undergo complete programming and functional testing on each bit position prior to shipment thus insuring 100% programmability.

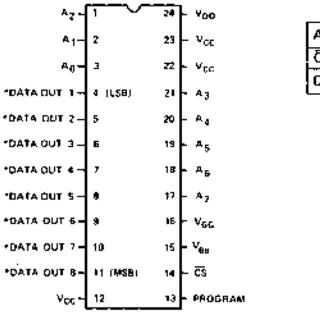
The 1602A-6 and 1702A-6 use identical chips. The 1702A-6 is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The 1602A-6 is packaged in a 24 pin dual in-line package with a metal lid and is not erasable.

The circuitry of the 1602A-6 and 1702A-6 is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs of systems initially using the -6 devices.

The 1602A-6 and 1702A-6 are fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

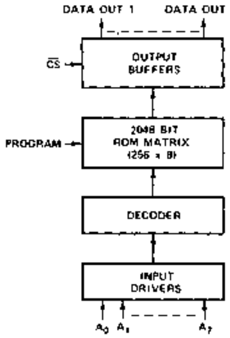
See page 3-15 for operational connection.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1602A-6/1702A-6 differ, depending on whether the device is being programmed or used in the read mode. (See following table.) In the programming mode, the data inputs 1-8 are pins 4-11 respectively.

PIN MODE	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . +300°C
Power Dissipation . . . . 2 Watts
Read Operation: Input Voltages and Supply
  Voltages with respect to V_{CC} . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply
  Voltages with respect to V_{CC} . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, V_{GG} [1] $= -9V \pm 5\%$, unless otherwise noted. Typical values are at nominal voltages and $T_A = 25°C$.

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	μA	$V_{IN} = 0.0V$
I_{LO}	Output Leakage Current			1	μA	$V_{OUT} = 0.0V$, $\overline{CS} = V_{CC} - 2$
I_{DD0}	Power Supply Current		5	10	mA	$V_{GG} = V_{CC}$, $\overline{CS} = V_{CC} - 2$ $I_{OL} = 0.0mA$, $T_A = 25°C$ } Note 1
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS} = V_{CC} - 2$ $I_{OL} = 0.0mA$, $T_A = 25°C$
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS} = 0.0$ $I_{OL} = 0.0mA$, $T_A = 25°C$
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS} = V_{CC} - 2$ $I_{OL} = 0.0mA$, $T_A = 0°C$
I_{CF1}	Output Clamp Current		8	14	mA	$V_{OUT} = -1.0V$, $T_A = 0°C$
I_{CF2}	Output Clamp Current			13	mA	$V_{OUT} = -1.0V$, $T_A = 25°C$
I_{GG}	Gate Supply Current			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		$V_{CC} - 6$	V	
V_{IH}	Address and Chip Select Input High Voltage	$V_{CC} - 2$		$V_{CC} + 0.3$	V	
I_{OL}	Output Sink Current	1.6	4		mA	$V_{OUT} = 0.45V$
I_{OH}	Output Source Current	−2.0			mA	$V_{OUT} = 0.0V$
V_{OL}	Output Low Voltage		−.7	0.45	V	$I_{OL} = 1.6mA$
V_{OH}	Output High Voltage	3.5	4.5		V	$I_{OH} = -100 \mu A$

NOTE 1: POWER DOWN OPTION: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option please specify 1602AL-6 or 1702AL-6.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$ unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			0.66	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		0.7	1.5	μs
t_{DVGG}	Clocked V_{GG} set up (Note 1)	1			μs
t_{CS}	Chip select delay			600	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	μs

Capacitance* $T_A = 25°C$

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS	
C_{IN}	Input Capacitance		8	15	pF	$V_{IN} = V_{CC}$ $\overline{CS} = V_{CC}$ $V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$	All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF		
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)			30	pF		

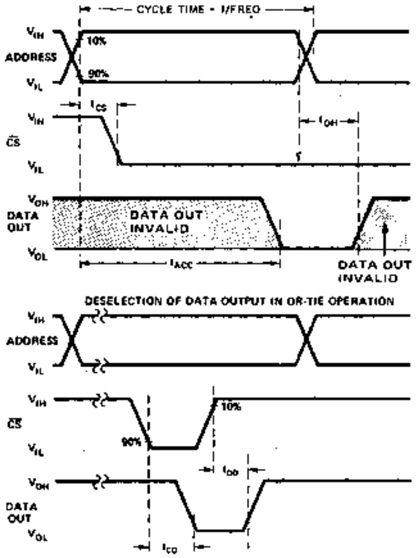
*This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

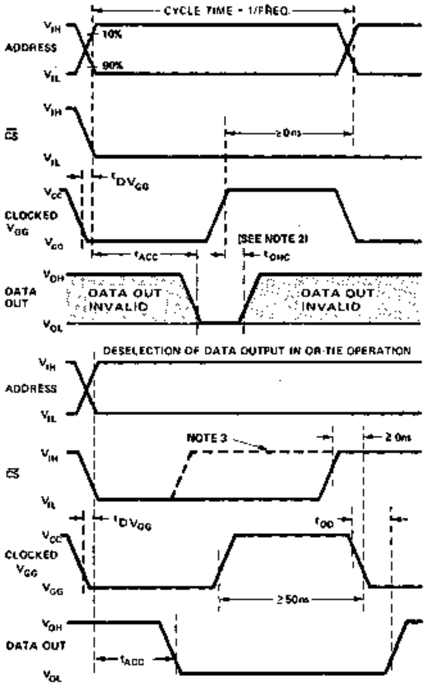
Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, $t_F \leq 50$ ns
Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15pF$

A) Constant V_{GG} Operation



B) Power-Down Option (See Note 1)



NOTE 2: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

NOTE 3: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

All programming operation and erasing characteristics as described on pages 3-11 through 3-13 apply for the 1602A-6/1702A-6.

intel® Silicon Gate MOS ROM 2308

8192 BIT STATIC MOS READ ONLY MEMORY

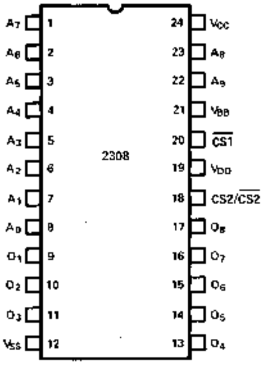
- **Fast Access Time — 500 ns**
- **Standard Power Supplies — +12V, ±5V**
- **TTL Compatible — All Inputs and Outputs**
- **Programmable Chip Select Input for Easy Memory Expansion**
- **Three-State Output — OR-Tie Capability**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**

The Intel 2308 is a 8192 bit static MOS read only memory organized as 1024 words by 8-bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

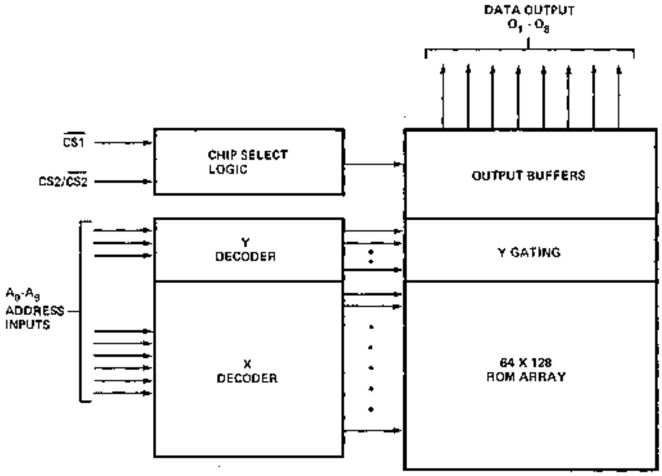
The inputs and outputs are TTL compatible. The chip select input ($CS2/\overline{CS2}$) is programmable. Any combination of active high or low level chip select input can be defined and the desired chip select code is fixed during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. The Intel 2708/2704 are 8K and 4K pin compatible, erasable and electrically reprogrammable read only memories.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS_1}$	CHIP SELECT INPUT
$CS2/\overline{CS2}$	PROGRAMMABLE CHIP SELECT INPUT

intel® Silicon Gate MOS ROM 2316A

16,384 BIT STATIC MOS READ ONLY MEMORY

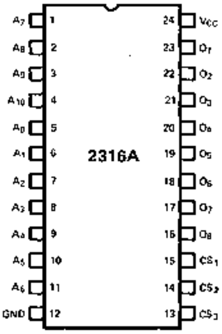
- **Single +5 Volts Power Supply Voltage**
- **Less than 1 μs Access Time**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output — OR-Tie Capability**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**

The Intel 2316A is a 16,384 bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

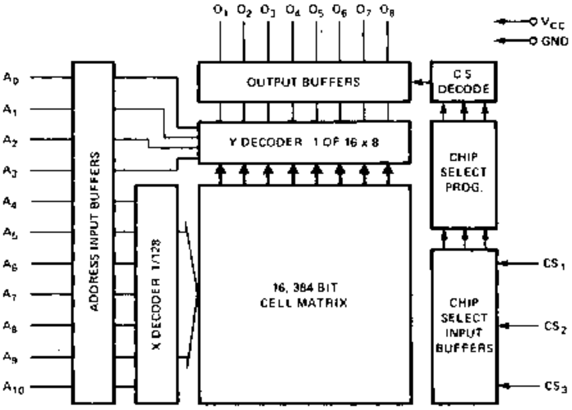
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS

intel® Silicon Gate MOS 2708, 2704

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- **2708 1024x8 Organization**
- **2704 512x8 Organization**

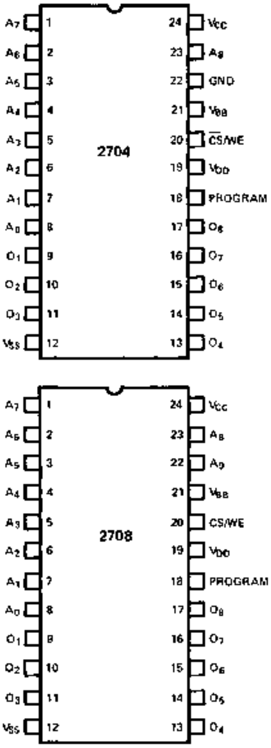
- **Fast Programming — Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time — 500 ns**
- **Standard Power Supplies — +12V, ±5V**
- **Static — No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output — OR-Tie Capability**

The Intel 2708/2704 are high speed 8192/4096 bit erasable and electrically programmable ROMs.

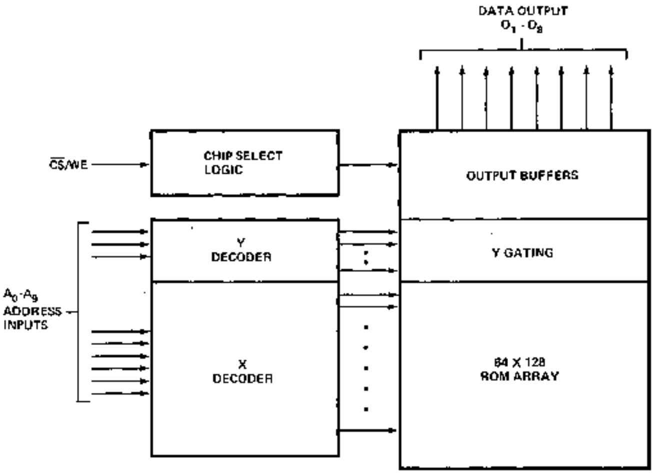
The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

A mask programmable ROM, the Intel 2308, is available for volume production runs of systems initially using the 2708/2704.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$	CHIP SELECT INPUTS

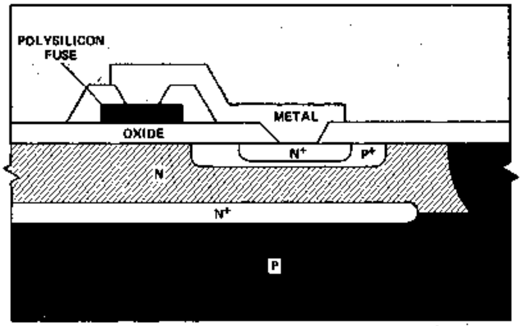
In bipolar PROMs, only polysilicon fuses can stand the test of time.

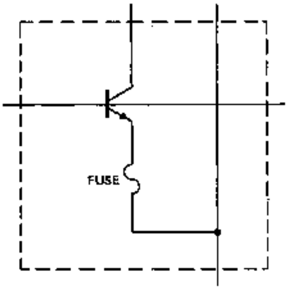
Today, the industry's highest density, highest performance PROMs have polysilicon fuse reliability. Intel's new 3604 is the first 4K design in real production. It dissipates only 60 μW/bit with the 3604-6 low stand-by power option. Yet 70 ns is guaranteed from 0-75° C, not just at 25° C. The new 2K and 4K designs offer three-state output options — 3622 and 3624. And the 3601-1, at 50 ns worst case access, is the world's fastest PROM. The ultimate in military PROMs is the M3601, with maximum access time of 90 ns from –55 to +125° C.

These PROMs all program easily, in less than a second, with high programming yields, using any of several standard programmers.

Most important, when polysilicon fuse is blown, it oxidizes completely. There is no conductive residue to short other parts of the circuit.

The very structure of an Intel PROM is inherently more reliable. You'll find no dissimilar metals, as you do in nichrome-aluminum interfaces, in our bipolar PROMs. The fuses are semiconductor material. And polysilicon is classically simple compared to blown junctions. Blown junctions miss the target, being complex, difficult to fabricate and requiring tight programming control. They also require high current programming pulses that may blow the wrong junction.





CELL SCHEMATIC

intel®

Schottky Bipolar **3301A**

HIGH SPEED FULLY DECODED 1024 BIT READ ONLY MEMORY

- **Fast Access Time -- 45 nsec Maximum over Temperature and Supply Voltage Variation.**
- **Low Power Dissipation -- 0.5 mW/bit typical.**
- **DTL and TTL Compatible -- Input Loading is .25 mA max. -- Outputs sink 15 mA.**
- **OR-Tie Capability -- Open Collector Outputs**
- **Simple Memory Expansion -- 2 Chip Select Input Leads.**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Standard Packaging -- 16 Pin Dual In-Line Lead Configuration.**

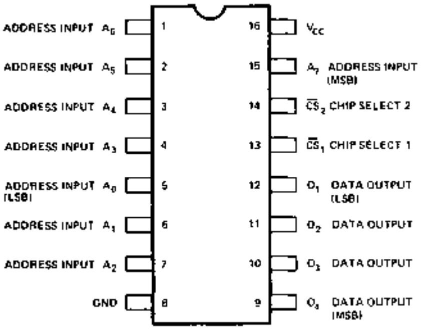
The 3301A is a fully decoded 1024 bit read only memory organized as 256 words by 4 bits. It is a higher speed version of the 3301 and is a direct pin for pin replacement of the 3301. Its performance is specified over the complete ambient temperature range of 0°C to 75°C and a V_{CC} supply voltage range of 5V ± 5%. The 3301A is programmed at the final step of processing which allows fast turnaround.

The OR tie capability and the 2 chip select inputs of the 3301A allow easy memory expansion into larger word and bit lengths.

The 3301A is mask programmed to customized patterns. It is also available in standard "off the shelf" configurations. Ideal applications are in microprogramming and table look up.

The 3301A is manufactured using Schottky barrier diode clamped transistors which allows higher switching speeds than those devices made with conventional gold diffusion process.

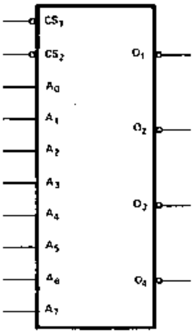
PIN CONFIGURATION



PIN NAMES

A_0–A_7	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$	CHIP SELECT INPUTS
$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS

LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	−65°to +125°C
Storage Temperature	−65°to +160°C
All Input, Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	−1.0 to 5.5V
Output Currents	100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

SYMBOL	PARAMETER	LIMITS MIN.	TYP.(1)	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT			−0.25	mA	V_{CC}= 5.25V, V_A = 0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT			−0.25	mA	V_{CC}= 5.25V, V_S = 0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			40	μA	V_{CC}= 5.25V, V_A = 5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE			−1.0	V	V_{CC}= 4.75V, I_A = −5.0mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE			−1.0	V	V_{CC}= 4.75V, I_S = −5.0mA
V_{OL}	OUTPUT LOW VOLTAGE			0.45	V	V_{CC}= 4.75V, I_{OL} = 15mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC}= 5.25V, V_{CE} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		90	125	mA	V_{CC}= 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V V_{S0} = V_{S1} = 0V
V_{IL}	INPUT "LOW" VOLTAGE			0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0			V	V_{CC} = 5.0V

Note 1: Typical values are at 25°C and at nominal voltage.

Switching Characteristics

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	LIMIT TYP.[1]	LIMIT MAX.	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	25	45	ns	Both C.S. lines must be at ground potential to activate the ROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	13	20	ns	

NOTE 1: Typical values are at 25°C and at nominal voltage.

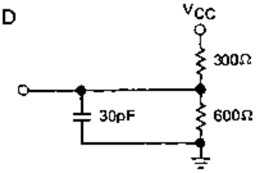
Capacitance[2] $T_A = 25°C$

SYMBOL	PARAMETER	LIMIT PLASTIC TYP.	LIMIT PLASTIC MAX.	LIMIT CERAMIC TYP.	LIMIT CERAMIC MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	5	8	6	10	pF	$V_{CC} = 5V$ $V_{INA} = 2.5V$
C_{INS}	Chip Select Input Capacitance	5	8	5	10	pF	$V_{CC} = 5V$ $V_{INS} = 2.5V$
C_{OUT}	Output Capacitance	7	10	8	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

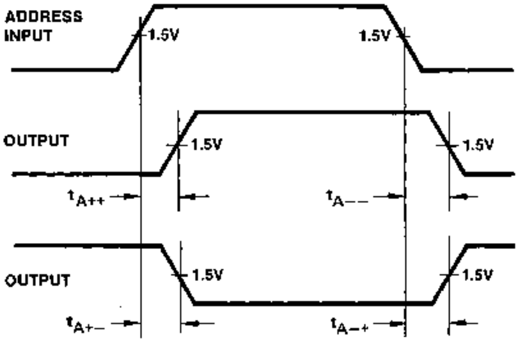
NOTE 2: This parameter is only periodically sampled and is not 100% tested.

Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

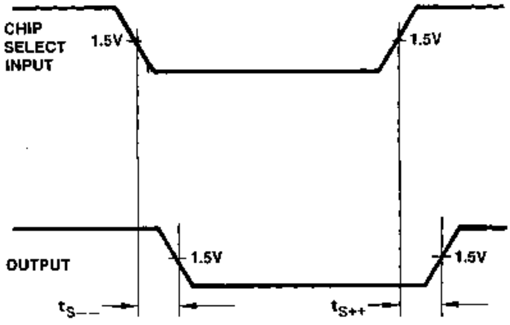
15 mA TEST LOAD



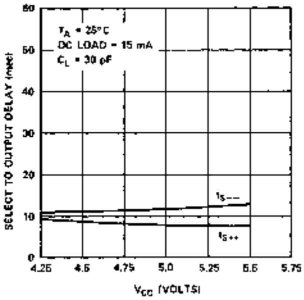
ADDRESS TO OUTPUT DELAY

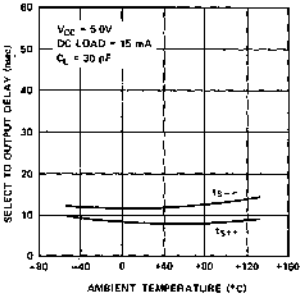


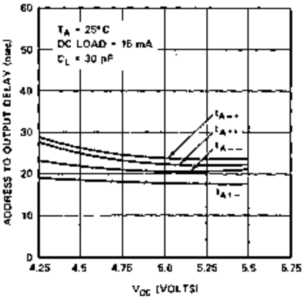
CHIP SELECT TO OUTPUT DELAY

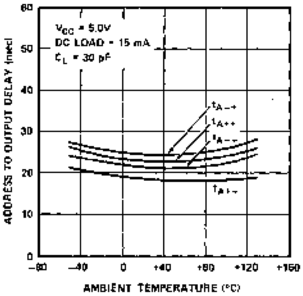


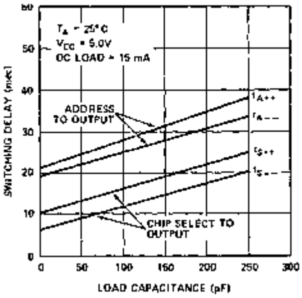
Typical A.C. Characteristics


SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE

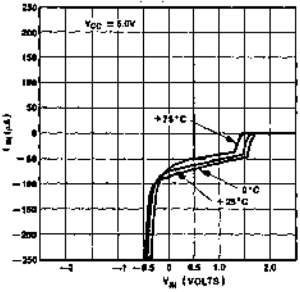

SELECT TO OUTPUT DELAY
VS. TEMPERATURE

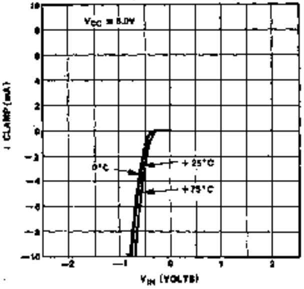

ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE

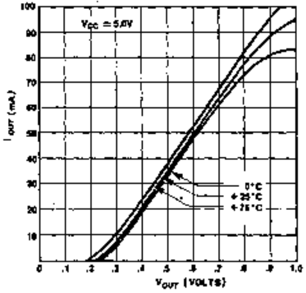

ADDRESS TO OUTPUT DELAY
VS. TEMPERATURE

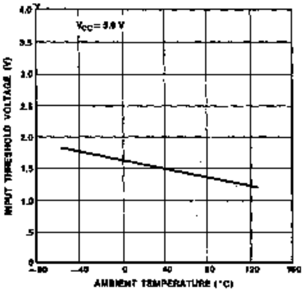

SWITCHING DELAY
VS. LOAD CAPACITANCE

Typical D.C. Characteristics


INPUT CURRENT
VS. INPUT VOLTAGE


INPUT CLAMP CURRENT
VS. INPUT VOLTAGE


OUTPUT CURRENT
VS. OUTPUT "LOW" VOLTAGE


INPUT THRESHOLD
VS. TEMPERATURE

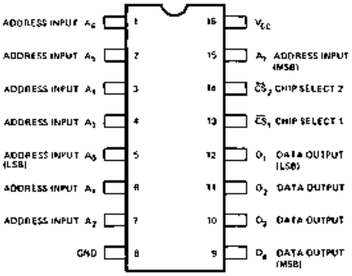
Schottky Bipolar **M3301A**

HIGH SPEED 1024 BIT READ ONLY MEMORY

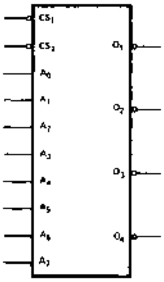
- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time—60 nsec Maximum**
- **OR-Tie Capability— Open Collector Outputs**
- **Standard Packaging—16 Pin Dual In-Line Lead Configuration**

The M3301A is a military temperature range ROM, organized as 256 words by 4-bits. It is mask programmed to customized patterns. Initial circuit prototyping can be performed before going into volume production by using the pin compatible M3601 PROM.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	−65°C to +150°C
Storage Temperature	−65°C to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	−1.2V to 5.5V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

All limits apply for V_{CC} = +5.0V ±5%, T_A = −55°C to +125°C, unless otherwise specified.

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		−0.7	−1.2	V	V_{CC} = 4.75V, I_A = −5.0mA
V_{CS}	Chip Select Input Clamp Voltage		−0.7	−1.2	V	V_{CC} = 4.75V, I_S = −5.0mA
V_{CS}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 10mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current		90	125	mA	V_{CC} = 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V, V_{CC} = 5.25V, V_{S0} = V_{S1} = 0V
V_{IL}	Input "Low" Voltage			0.80	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.1			V	V_{CC} = 5.0V

NOTE 1: Typical values are at 25°C and at nominal voltage.

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	ns	Both C.S. lines must be at ground potential to activate the ROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	30	ns	

Capacitance$^{(1)}$ $T_A = 25°C$

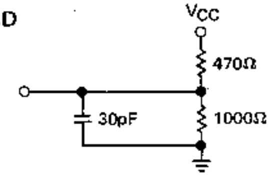
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

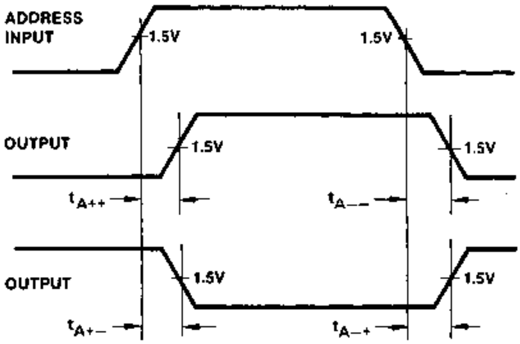
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

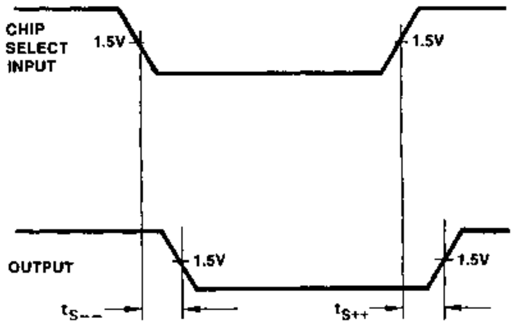


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



intel Schottky Bipolar **3601, 3601-1**

HIGH SPEED ELECTRICALLY PROGRAMMABLE 1024 BIT READ ONLY MEMORY

*50 nsec Max. Access Time

- **Fast Access Time -- 50 nsec (3601-1) and 70 nsec (3601) Maximum over Temperature and Supply Voltage Variation**
- **Fast Programming -- 1 ms/Bit Typically**
- **Polycrystalline Silicon Fuse**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Low Power Dissipation -- 0.5 mW/Bit Typical.**
- **DTL and TTL Compatible -- Input Loading is .25 mA max. -- Outputs sink 15 mA.**
- **OR-Tie Capability -- Open Collector Outputs**
- **Simple Memory Expansion -- 2 Chip Select Input Leads.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Standard Packaging -- 16 Pin Dual In-Line Lead Configuration.**

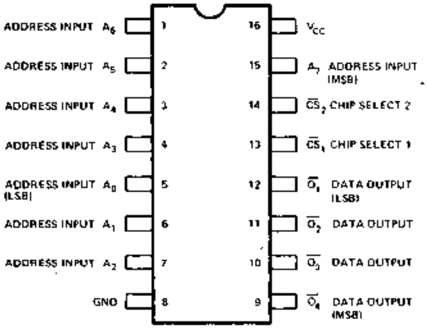
The Intel 3601, 3601-1 is a 1024 bit (256 word by 4-bit) electrically programmable ROM ideally suited for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROM is manufactured with all outputs low and logic high output levels can be electrically programmed in selected bit locations. The same address inputs are used for both programming and reading.

A higher system performance is achieved by using the 3601-1. The 3601-1 gives a 25% system speed improvement over the 3601.

The 3601, 3601-1 is pin compatible with the Intel metal mask 3301A ROM. The 3301A is ideal for large volume and lower cost production runs of systems initially using the PROM.

The 3601, 3601-1 is manufactured with the highly reliable polycrystalline silicon fuse and the fast switching Schottky barrier diode technology.

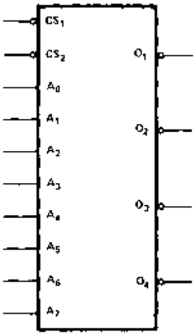
PIN CONFIGURATION



PIN NAMES

A_0–A_7	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$	CHIP SELECT INPUTS
$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS

LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	−1V to 5.5V
Output Currents	100mA
Programming Only:	
Output or V_{CC} Voltages	10.25V
CS_2 Voltage	15.5V
CS_2 Current	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.[1]	MAX.		
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.05	−0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.05	−0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−0.7	−1.0	V	V_{CC} = 4.75V, I_A = −5.0mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−0.7	−1.0	V	V_{CC} = 4.75V, I_S = −5.0mA
V_{OL}	OUTPUT LOW VOLTAGE		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		90	130	mA	V_{CC} = 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V V_{S0} = V_{S1} = 0V
V_{IL}	INPUT "LOW" VOLTAGE			0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0			V	V_{CC} = 5.0V

Note 1: Typical values are at 25°C and at nominal voltage.

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	MAXIMUM LIMITS			UNIT	CONDITIONS
		0°C	25°C	75°C		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay (3601)	70	60	70	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay (3601-1)	50	50	50	ns	
t_{S++}, t_{S--}	Chip Select to Output Delay	25	25	25	ns	

Capacitance$^{(1)}$ $T_A = 25°C$

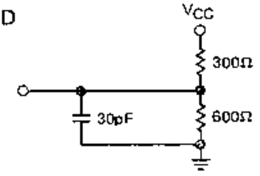
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

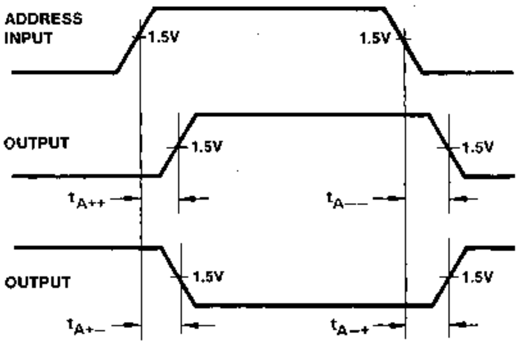
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

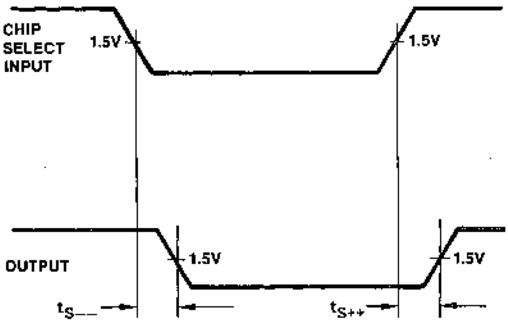


Waveforms

ADDRESS TO OUTPUT DELAY

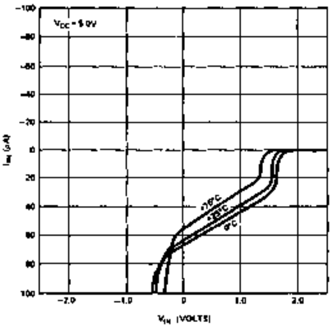


CHIP SELECT TO OUTPUT DELAY

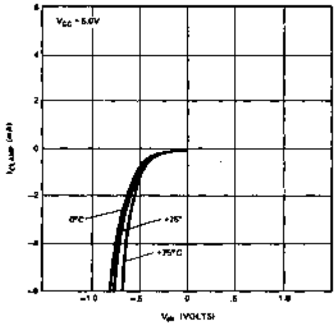


Typical D. C. Characteristics

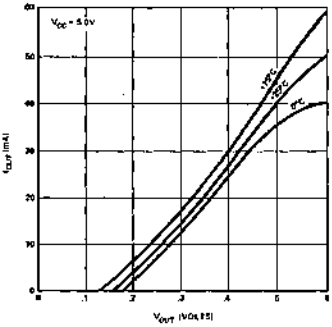
INPUT CURRENT
VS. INPUT VOLTAGE



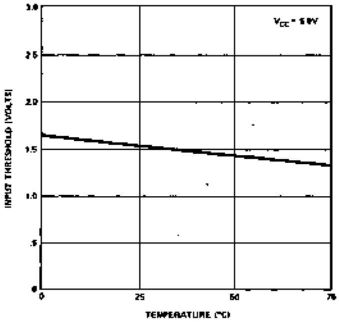
INPUT CLAMP CURRENT
VS. INPUT VOLTAGE



OUTPUT CURRENT
VS. OUTPUT "LOW" VOLTAGE

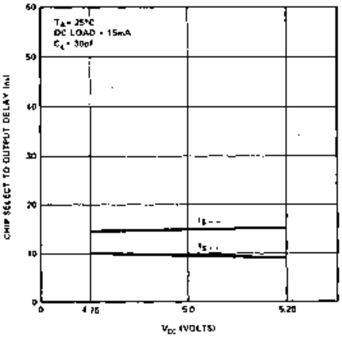


INPUT THRESHOLD
VS. TEMPERATURE

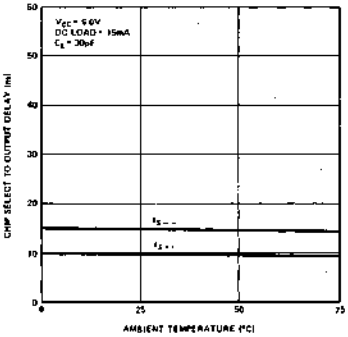


Typical A. C. Characteristics

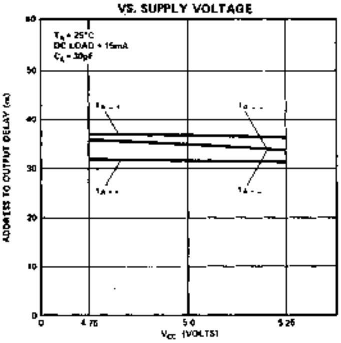
SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



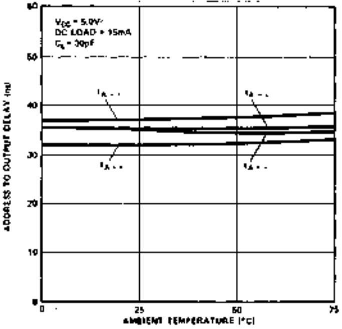
SELECT TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



ADDRESS TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



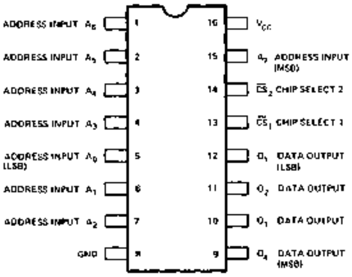
intel® Schottky Bipolar M3601

HIGH SPEED ELECTRICALLY PROGRAMMABLE 1024 BIT READ ONLY MEMORY

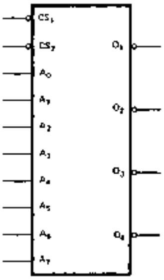
- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time — 90 nsec Maximum**
- **Fast Programming — 1 ms/bit Typically**
- **Standard Packaging — 16 Pin Dual In-Line Lead Configuration**

The M3601 is a military temperature range PROM, organized as 256 words by 4-bits. The PROM is manufactured with all outputs low and logic output high levels can be electrically programmed in selected bit locations. The M3601 is pin compatible with the Intel metal mask ROM M3301A.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +150°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.2V to 5.5V
Output Currents	100mA
Programming Only:	
Output or V_{CC} Voltages	10.25V
CS_2 Voltage	15.25V
V_{CC} Current	500mA
CS_2 Current	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

All limits apply for V_{CC} = +5.0V ±5%, T_A = -55°C to +125°C, unless otherwise specified.

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_A = -5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_S = -5.0mA
V_{CS}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 10mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V, V_{CE} = 5.25V V_{CC} = 5.25V,
I_{CC}	Power Supply Current		90	130	mA	$V_{A0} \rightarrow V_{A7}$ = 0V, V_{S0} = V_{S1} = 0V
V_{IL}	Input "Low" Voltage			0.80	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.1			V	V_{CC} = 5.0V

NOTE 1: Typical values are at 25°C and at nominal voltage.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = -55°C to +125°C

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	CONDITIONS
t_{A++} , t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	90	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	35	ns	

Capacitance[1] T_A = 25°C

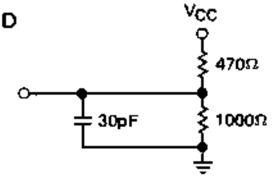
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

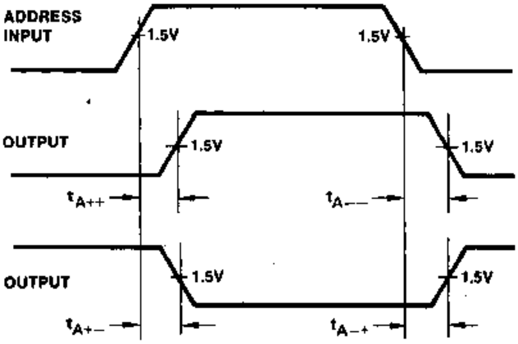
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

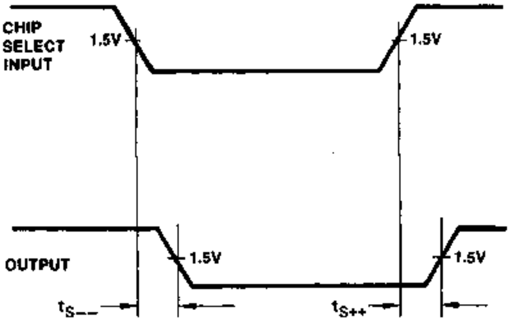


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



intel®

Schottky Bipolar 3302, 3302-4, 3302-6, 3322, 3322-4, 3322-6

HIGH SPEED 2048 BIT READ ONLY MEMORY

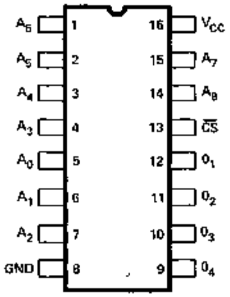
- **Fast Access Time—70 ns (3302, 3322) over Temperature and Supply Voltage Variation**
- **Low Standby Power Dissipation (3302-6, 3322-6)—100 μW/bit**
- **Fully Decoded—On Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Input Loading is 0.25 mA Max—Outputs Sink 15 mA**
- **Open Collector (3302, 3302-4, 3302-6) and Three State (3322, 3322-4, 3322-6) Outputs**
- **Standard Packaging—16 Pin Dual In-Line Lead Configuration**

The 3302 and 3322 device families are high density 2048 bit (512 words by 4-bit) ROMs. Electrical performance is specified over the complete ambient temperature range of 0°C to 75°C and V_{CC} supply voltage range of 5V ±5%. The 3302 and 3322 ROM families are pin compatible with the Intel 3602 and 3622 PROM families. Consequently initial circuit prototyping can be performed using the pin compatible PROMs.

The 3302-4 and 3322-4 are ideal for slower performance systems (>90 ns) where low system cost is a prime factor. For those systems requiring low power dissipation, one should consider the 3302-6 and 3322-6. Not only does the 3302-6 and 3322-6 dissipate 20% less active power than the 3302 and 3322 respectively, but it also has an added low standby power dissipation feature. Whenever the 3302-6 and 3322-6 is deselected, power dissipation is reduced by 70%.

The 3302 and 3322 devices are manufactured using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices made with gold diffusion process.

PIN CONFIGURATION

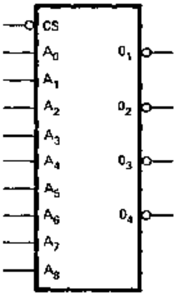


PIN NAMES

A_0-A_8	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT[1]
O_1-O_4	DATA OUTPUTS

[1] To select the ROM $\overline{CS}$ = Logic 0.

LOGIC SYMBOL



Schottky Bipolar 3602, 3602-4, 3602-6, 3622, 3622-4, 3622-6

HIGH SPEED ELECTRICALLY PROGRAMMABLE 2048 BIT READ ONLY MEMORY

- **Fast Access Time — 70ns (3602, 3622)**
- **Low Standby Power Dissipation (3602-6, 3622-6) — 100 μW/bit**
- **Open Collector (3602, 3602-4, 3602-6) or Three-State (3622, 3622-4, 3622-6) Outputs**
- **Fast Programming — 1 ms/bit Typically**
- **Polycrystalline Silicon Fuse**
- **Standard Packaging — 16 Pin Dual In-Line Configuration**

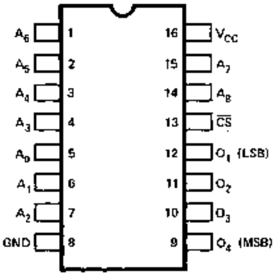
The 3602 and 3622 device families are high density 2048 bit (512 words by 4-bits) PROMs suitable for uses where fast turn-around and pattern experimentation are important such as in prototypes or in small production volume systems. For those systems requiring low power dissipation, one should consider the 3602-6 or 3622-6. Both the 3602-6 and 3622-6 have a low standby power dissipation feature. Whenever these two devices are deselected, power dissipation is reduced substantially over the active power dissipation. The 3602-4 and 3622-4 are ideal for slower performance systems (>90ns) where low system cost is a prime factor.

The PROMs are pin compatible with the Intel metal mask ROMs 3302, 3302-4, 3302-6, 3322, 3322-4 and 3322-6. The ROMs offer system cost savings over the PROMs when in large volume production.

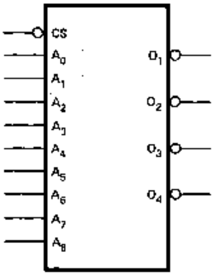
The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

The 3602 and 3622 device families are monolithic, high speed, Schottky clamped TTL arrays with polycrystalline silicon fuses. The Schottky barrier diode clamped transistors allow faster switching speeds than those devices made with the conventional gold diffusion processes.

PIN CONFIGURATION



LOGIC SYMBOL



intel® Schottky Bipolar 3304A, 3304A-4, 3304A-6, 3324A, 3324A-4

HIGH SPEED 4096 BIT READ ONLY MEMORY

- **Fast Access Time—70ns (3304A, 3324A) Over Temperature and Supply Voltage Variation**
- **Low Standby Power Dissipation (3304A-6)—60 μW/bit**
- **Fully Decoded—on Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Input Loading is 0.25 mA max—Output Sink is 15 mA**
- **Open Collector (3304A, 3304A-4, 3304A-6) and Three State (3324A, 3324A-4) Outputs**
- **Simple Memory Expansion—4 Chip Select Input Leads**
- **Standard Packaging—24 Pin Dual In-Line Lead Configuration**

The 3304A and 3324A device families are high density 4096 bit (512 words by 8-bit) ROMs. Electrical performance is specified over the complete ambient temperature range of 0°C to 75°C and V_{CC} supply voltage range of 5V ±5%. The 3304A and 3324A ROM families are pin compatible with the Intel 3604 and 3624 PROM families. Consequently initial circuit prototyping can be performed using the pin compatible PROMs.

The 3304A-4 and 3324A-4 are ideal for slower performance systems (>90 ns) where low system cost is a prime factor. For those systems requiring low power dissipation, one should consider the 3304A-6. Not only does the 3304A-6 dissipate 20% less active power than the 3304A, but it also has an added low standby power dissipation feature. Whenever the 3304A-6 is deselected, power dissipation is reduced by 70%.

The 3304A and 3324A device families are manufactured using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices mode with gold diffusion process.

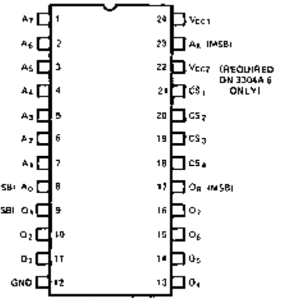
Mode/Pin Connection		Pin 22	Pin 24
Read:	3304A, 3304A-4, 3324A, 3324A-4	No Connect or 5V	5V
	3304A-6	+5V	No Connect
Standby Power:	3304A-6	Power dissipation is automatically reduced whenever the 3304A-6 is deselected.	

PIN NAMES

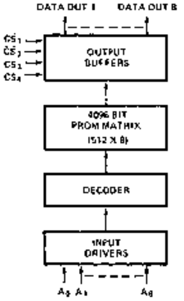
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$ CS_3–CS_4	CHIP SELECT INPUTS[1]
O_1–O_8	DATA OUTPUTS

[1] To select the ROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

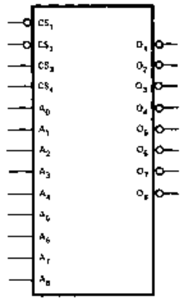
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



intel® Schottky Bipolar 3604, 3604-4, 3604-6

HIGH SPEED ELECTRICALLY PROGRAMMABLE 4096 BIT READ ONLY MEMORY

- **Fast Programming--1 ms/Bit Typically**
- **Fast Access Time--70 nsec (3604) Maximum over Temperature and Supply Voltage Variation**
- **Low Standby Power Dissipation (3604-6)--60 μW/bit Maximum**
- **Fully Decoded--on Chip Address Decode and Buffer**
- **DTL and TTL Compatible--Input Loading is .25 mA max--Outputs sink 15 mA**
- **OR-Tie Capability--Open Collector Outputs**
- **Simple Memory Expansion--4 Chip Select Input Leads**
- **Standard Packaging--24 Pin Dual In-Line Lead Configuration**

The 3604 family is a high density 4096 bit (512 word by 8-bit) electrically programmable ROMs suitable for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

The 3604 is pin compatible with the Intel 3304A metal mask ROM. The 3304A is ideal for large volume and lower cost production runs of systems initially using the 3604. The 3604-4 is ideal for slower performance systems where cost is a prime factor. The 3604-4 is pin compatible with the 3304A-4 metal mask ROM.

For those systems requiring low power dissipation, one should consider the 3604-6. Not only does the 3604-6 dissipate 20% less active power than the 3604, but it also has an added low standby power dissipation feature. Whenever the 3604-6 is deselected, power dissipation is reduced by 70%. The lower cost 3304A-6 metal mask ROM is also available for volume production usage.

The 3604 family is a monolithic, high speed, Schottky clamped TTL memory array with polycrystalline silicon fuses. The Schottky barrier diode clamped transistors allow faster switching speeds than those devices made with the conventional gold diffusion processes.

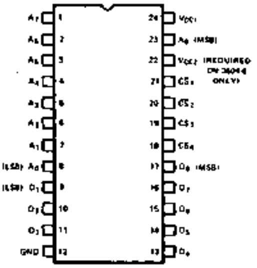
Mode/Pin Connection		Pin 22	Pin 24
Read:			
	3604, 3604-4	No Connect or 5V	5V
	3604-6	+5V	No Connect
Program:			
	3604, 3604-4	Pulsed 12V	Pulsed 12V
	3604-6	Pulsed 12V	Pulsed 12V
Standby Power:	3604-6	Power dissipation is automatically reduced whenever the 3604-6 is deselected.	

PIN NAMES

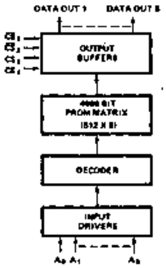
A_0–A_8	ADDRESS INPUTS
$\overline{CS_1}$–$\overline{CS_2}$ CS_3–CS_4	CHIP SELECT INPUTS[1]
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS_1} = \overline{CS_2} = 0$ and $CS_3 = CS_4 = 1$.

PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL

Absolute Maximum Ratings*

Temperature Under Bias	-65°C to +125°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1V to 5.5V
Output Currents	100mA
Programming Only:	
Output or V_{CC} Voltages	12.5V
CS_1 Voltage	15.5V
V_{CC} Current	600mA
CS_1 Current	150mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

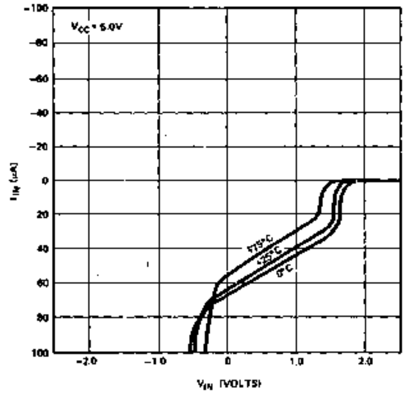
D. C. Characteristics: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.50	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 3.5V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.0	V	V_{CC} = 4.75V, I_A = -5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.0	V	V_{CC} = 4.75V, I_S = -5.0mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3604, 3604-4)			190	mA	$V_{CC\,1}$= 5.25V, V_{A0}→V_{A7} = 0V $\overline{CS_1}$ = $\overline{CS_2}$ = 0V CS_3 = CS_4 = 5.25V
I_{CC2}	Power Supply Current (3604-6)					V_{CC2} = 5.25V, V_{CC1} = Open
	Active			140	mA	Chip Selected
	Standby			45	mA	Chip Deselected, $\overline{CS_1}$=$\overline{CS_2}$=2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

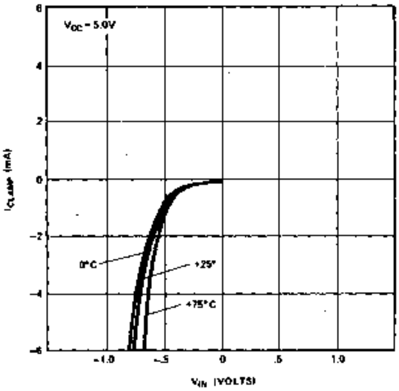
Note 1: Typical values are at 25°C and at nominal voltage.

Typical D. C. Characteristics

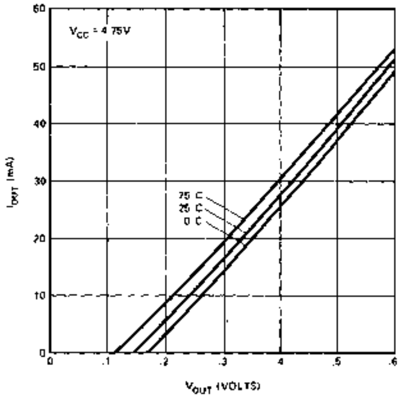
INPUT CURRENT VS. INPUT VOLTAGE



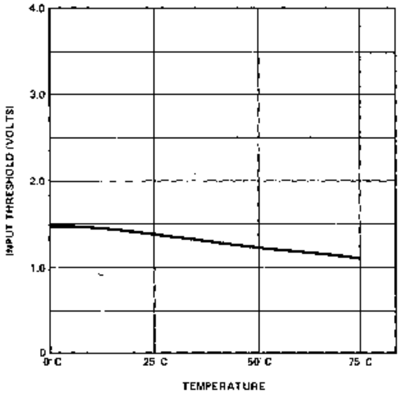
INPUT CLAMP CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT THRESHOLD VS. TEMPERATURE



A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter		Max. Limit	Unit	Conditions
t_{A++}, t_{A--}	Address to	3604	70	ns	$\overline{CS_1} = \overline{CS_2} = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to select the PROM.
t_{A+-}, t_{A-+}	Output Delay:	3604-4, 3604-6	90	ns	
t_{S++}	Chip Select to	3604, 3604-4	30	ns	
	Output Delay:	3604-6	30	ns	
t_{S--}	Chip Select to	3604, 3604-4	30	ns	
	Output Delay:	3604-6	120	ns	

Capacitance[1] $T_A = 25°C$

Symbol	Parameter	Limits		Unit	Test Conditions	
		Typ.	Max.			
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test:

Input pulse amplitudes - 2.5V

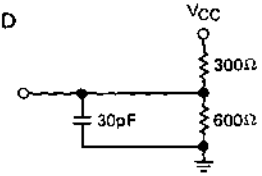
Input pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

Output loading is 15 mA and 30 pF

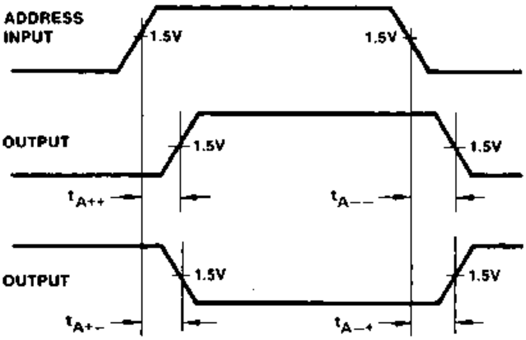
Frequency of test - 2.5 MHz

15 mA TEST LOAD

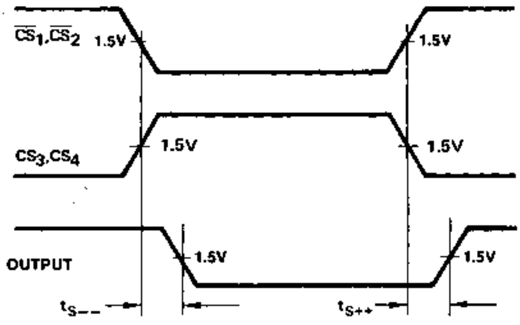


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



intel Schottky Bipolar 3624, 3624-4

HIGH SPEED ELECTRICALLY PROGRAMMABLE 4096 BIT READ ONLY MEMORY

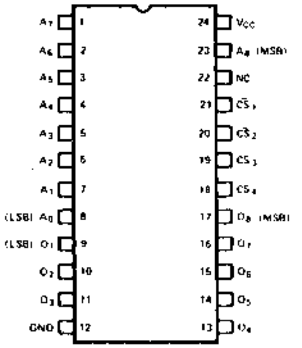
- **Fast Access Time—**
  70ns (3624)
  90ns (3624-4)
- **Three-State Outputs**
- **Fast Programming—1 ms/bit Typically**
- **Full Decoded—On Chip Address Decode and Buffer**
- **Polycrystalline Silicon Fuse**
- **Standard Packaging—24 Pin Dual In-Line Lead Configuration**

The 3624 and 3624-4 are high density 4096 bit (512 words by 8-bits) PROMs suitable for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

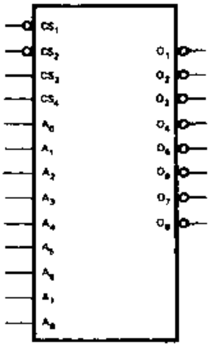
The 3624 and 3624-4 have pin compatible metal mask ROMs, the 3324A and 3324A-4 respectively. The ROMs are ideal for large volume and lower cost production runs of systems initially using the PROMs.

The 3624 and 3624-4 are monolithic, high speed, Schottky clamped TTL memory arrays with polycrystalline silicon fuses. The Schottky barrier diode clamped transistors allow faster switching speeds than those devices made with the conventional gold diffusion processes.

PIN CONFIGURATION



LOGIC SYMBOL



intel® ROM and PROM Programming Instructions

I. ROM and PROM Truth Table Format

Programming information should be sent in the form of computer punched cards or punched paper tape. When using the 7600C or MCS programmers, punched paper tape should be used. In all cases, a printout of the truth table should be accompanied with the order.

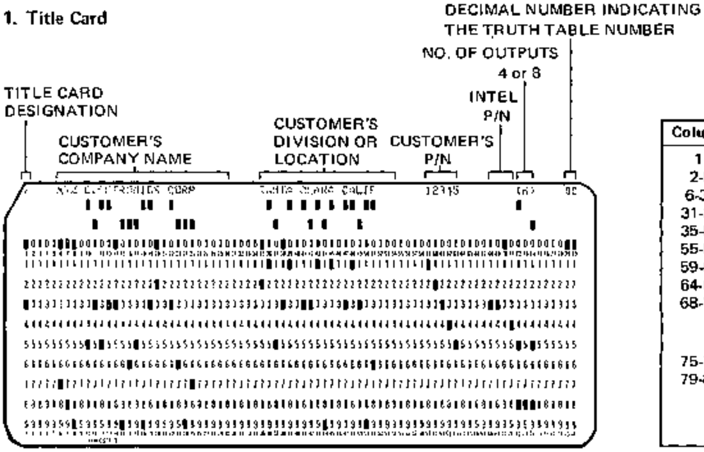
The following general format is applicable to the programming information sent to Intel:

1. A data field should start with the most significant bit and end with the least significant bit.
2. The data field should consist of P's and N's. A P is to indicate a high level output (most positive) and an N a low level output (most negative). If the programming information is sent on a punched paper tape, then a start character, B, and an end character, F, must be used in the data field.

A. Punched Card Format

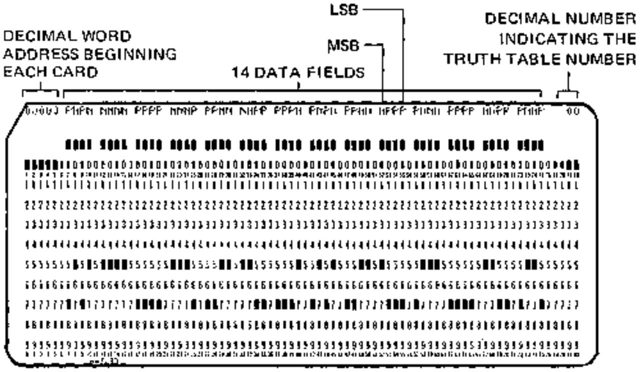
An 80 column Hollerith card (preferably interpreted) punched by an IBM 026 or 029 keypunch should be submitted. The first card will be a title card. The format is as follows:

1. Title Card



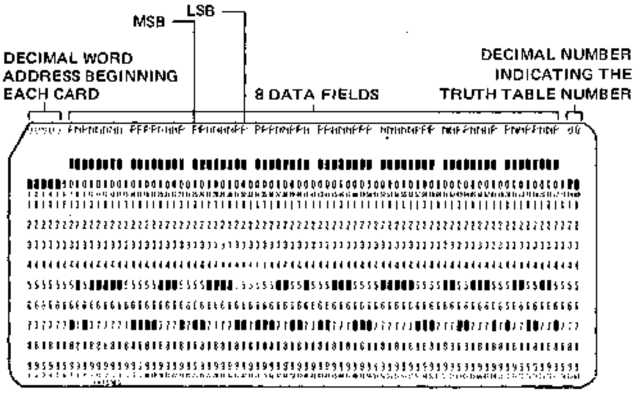
Column	Data
1	Punch a T
2-5	Blank
6-30	Customer Company Name
31-34	Blank
35-54	Customer's Company Division or location
55-58	Blank
59-63	Customer Part Number
64-67	Blank
68-74	Punch the Intel 4 digit basic part number and in () the number of output bits, e.g. 1702 (8) 3304 (8), 3301 (4), or 3601 (4).
75-78	Blank
79-80	Punch a 2 digit decimal number to identify the truth table number. The first truth table will be 00, second 01, third 03, etc.

2. For a N words x 4 bit organization only, cards 2 and the following cards should be punched as shown: Each card specifies the 4 bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00014, 00028, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

3. For a N words x 8 bit organization only, cards 2 and the following cards should be punched as shown. Each card specifies the 8 bit output of 8 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00008, 00016, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

B. Paper Tape Format

The paper tapes which should be used are the:

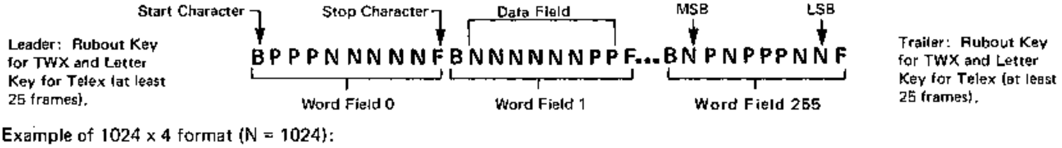
1. 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces, or the
2. 11/16" wide paper tape using 5 bit Baudot code, such as a Telex produces.

The format requirements are as follows:

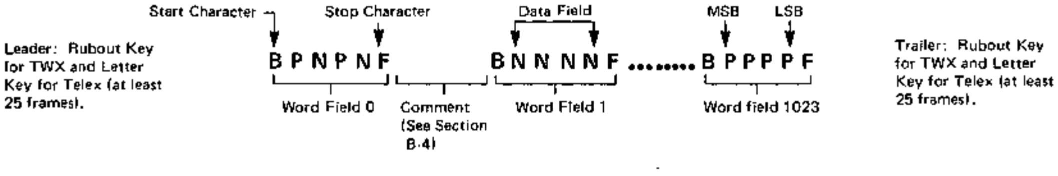
1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 or N x 4 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for the N x 8 or N x 4 organization respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of 256 x 8 format (N = 256):



Example of 1024 x 4 format (N = 1024):



II. Manually Programming the 3601 (or 3601-1)

The 3601 may be programmed using the basic circuit of Figure 1. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to V_{CC} through a 300Ω resistor. This will force the proper programming current (3-6mA) into the output when the V_{CC} supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V).

The programming pulse generator produces a series of pulses to the 3601 V_{CC} and $\overline{CS}_2$ leads. V_{CC} is pulsed from a low of 4.5 ± .25V to a high of 10 ± .25V, while $\overline{CS}_2$ is pulsed from a low of ground (TTL logic 0) to a high of 15 ± 0.5V. It is important to accurately maintain these voltage levels, otherwise, improper programming may result. The pulses applied must maintain a duty cycle of 50 ± 10% and start with an initial width of 1 (± 10%)μs, and increase linearly over a period of approximately 100ms to a maximum width of 8 (± 10%)μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, current to $\overline{CS}_2$ must be limited to 100mA. The output of the 3601 is sensed when $\overline{CS}_2$ is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the V_{CC} and $\overline{CS}_2$ pulse trains must be applied for another 100μs. One circuit which can be used to generate this pulse train is shown in Figure 2, while the characteristics of the pulse train are shown in Figure 3.

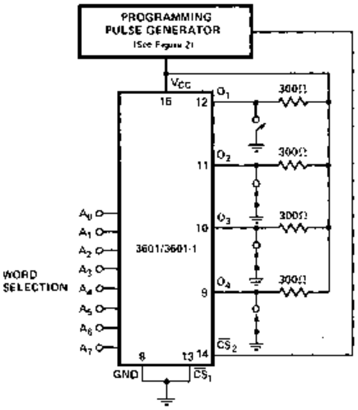
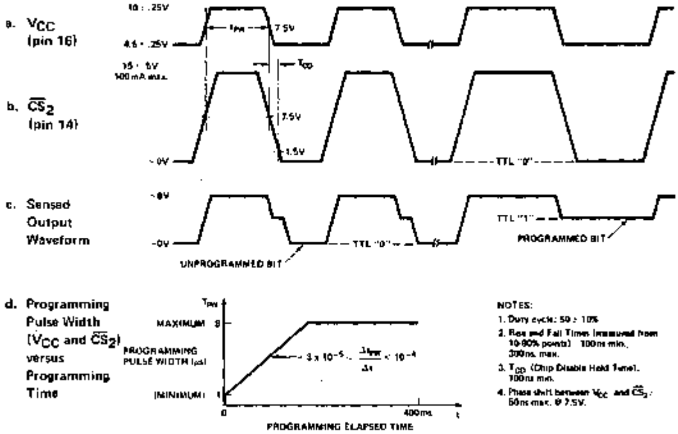


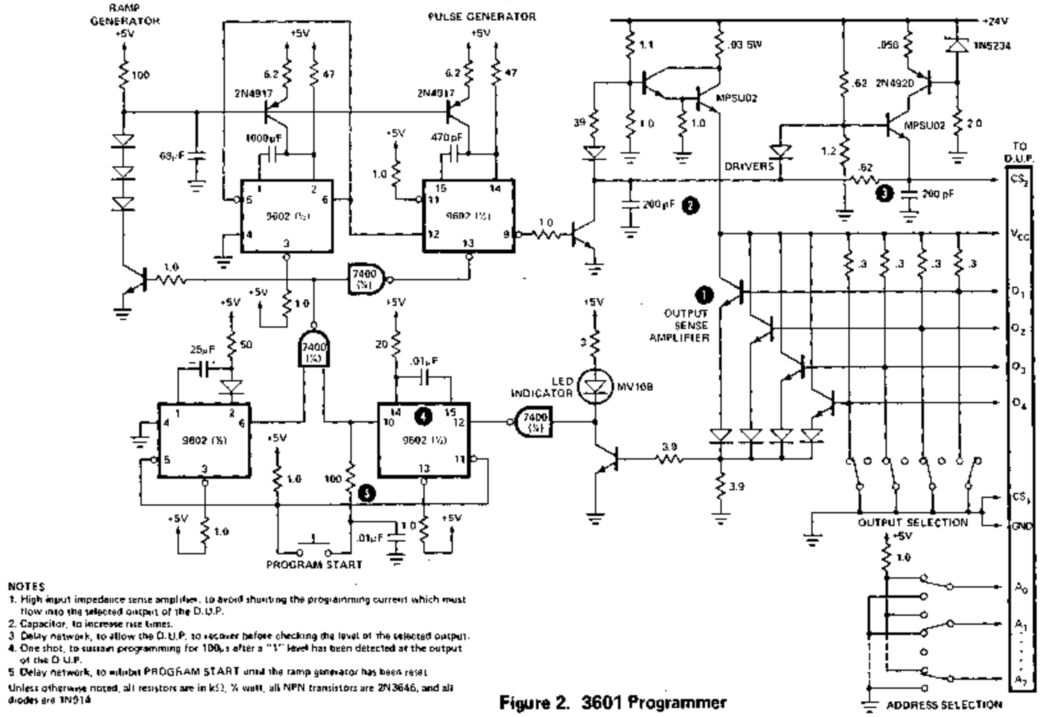
Figure 1. 3601 Programming



$3 \times 10^{-5} < \frac{\Delta t_{PW}}{\Delta t} < 10^{-4}$

NOTES:
1. Duty cycle: 50 ± 10%
2. Rise and Fall Times (measured from 10-90% points) 100ns min., 300ns. max.
3. T_{CD} (Chip Disable Hold Time). 100ns min.
4. Phase shift between V_{CC} and $\overline{CS}_2$: 50ns max. @ 7.5V.

Figure 3. Pulses During Programming



NOTES
1. High input impedance sense amplifier, to avoid shunting the programming current which must flow into the selected output of the D.U.P.
2. Capacitor, to increase rise times.
3. Delay network, to allow the D.U.P. to recover before checking the level of the selected output.
4. One shot, to sustain programming for 100μs after a "1" level has been detected at the output of the D.U.P.
5. Delay network, to inhibit PROGRAM START until the ramp generator has been reset.

Unless otherwise noted, all resistors are in kΩ, ¼ watt, all NPN transistors are 2N3646, and all diodes are 1N914.

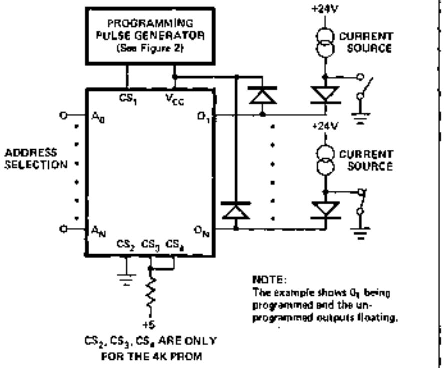
Figure 2. 3601 Programmer

ROM AND PROM PROGRAMMING INSTRUCTIONS

III. Manually Programming the 2K and 4K Bipolar PROMs

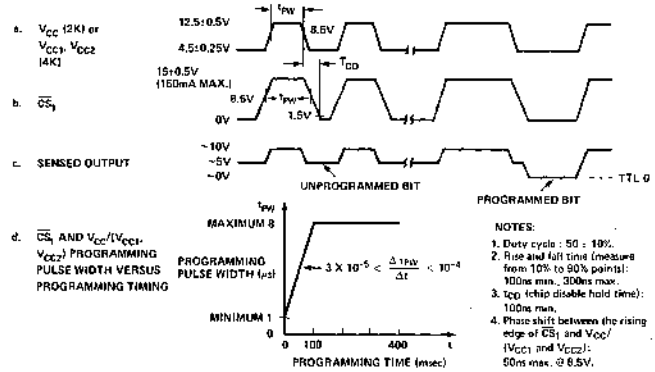
The Intel 2K and 4K bipolar PROMs may be programmed using the basic circuit of Figure 1. Initially all bits (either 2048 or 4096) are in a logic 1 (high) state. Only one output may be programmed at a time. The programming current (5mA ±10%) is forced into the output to be programmed by a current source. The current should be clamped to V_{CC} by a silicon diode. All other outputs must be allowed to float such that the outputs are allowed to rise one diode above V_{CC} (12.5V).

For simplicity of the programming description, reference will be made only to V_{CC}, however, this term includes both the V_{CC1} and V_{CC2} of the 4K PROM. There is only one V_{CC} for the 2K PROM. Programming pulses must be applied to both V_{CC} and CS. A series of pulses is applied to the V_{CC} and $\overline{CS}_1$ leads as shown in Figure 3a and 3b respectively. The pulse applied must maintain a duty cycle of 50 ±10% and start with an initial width of 1 (±10%) μs, and increase linearly over a period of approximately 100ms to a maximum of 8 (±10%) μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, the V_{CC} current must be limited to 600mA and the $\overline{CS}_1$ current to 150mA. A programmed bit will have a TTL low level. After a fuse is blown, the V_{CC} and $\overline{CS}_1$ pulse trains must be applied (the pulse width still linearly increasing to a maximum of 8μs) for another 100μs.



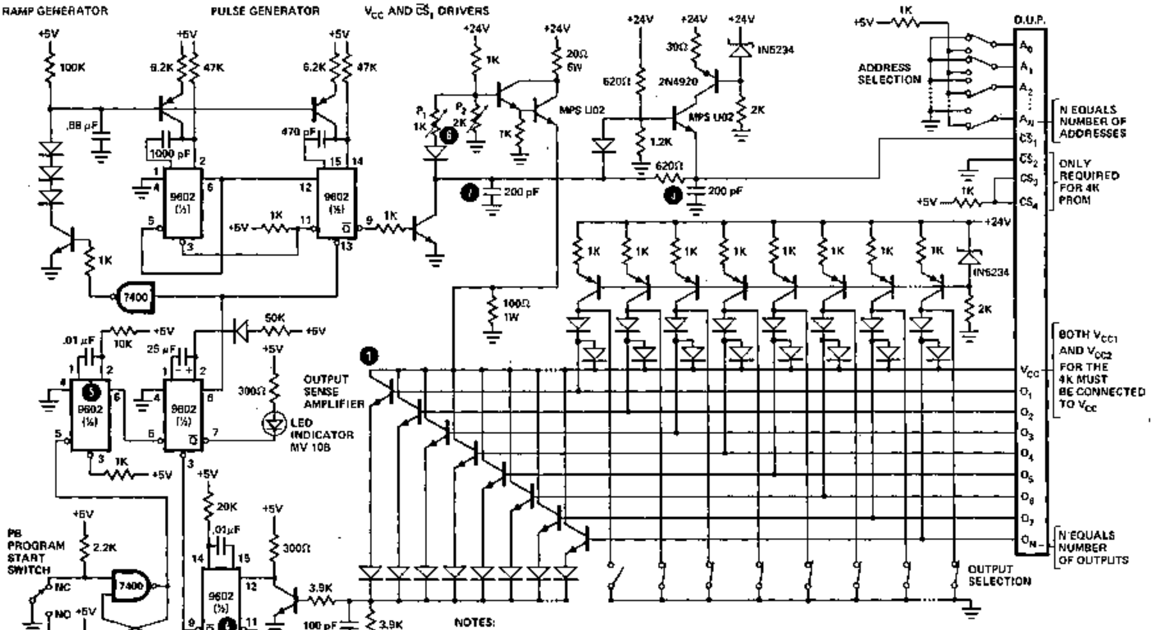
NOTE:
The example shows O_1 being programmed and the unprogrammed outputs floating.

Figure 1. 2K and 4K Bipolar PROM Programmer



NOTES:
1. Duty cycle : 50 ± 10%.
2. Rise and fall time (measure from 10% to 90% points): 100ns min., 300ns max.
3. t_{CD} (chip disable hold time): 100ns min.
4. Phase shift between the rising edge of $\overline{CS}_1$ and V_{CC}/(V_{CC1} and V_{CC2}): 50ns max. @ 8.5V.

Figure 3. Pulses During Programming

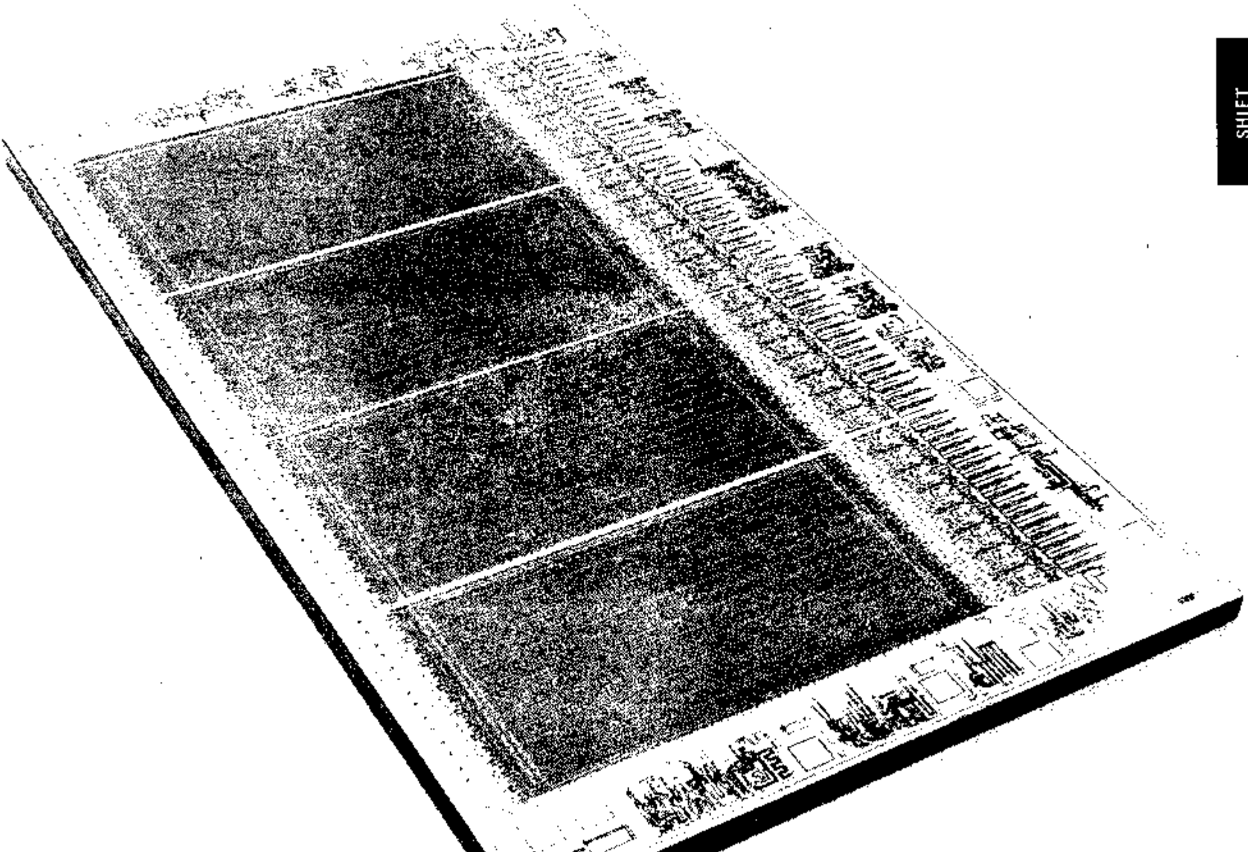


NOTES:
1. High impedance sense amplifier, to avoid shunting the programming current which must flow into the selected output of the D.U.P.
2. Capacitor, to adjust rise times.
3. Delay network, to allow the D.U.P. to recover before checking the level of the selected output.
4. One shot, to sustain programming for 100μs after a "0" level has been detected at the output of the D.U.P.
5. Delay network, to inhibit PROGRAM START until the ramp generator has been reset.
6. P_1 and P_2 adjusted for V_{CC} = 12.5V during programming and 4.5V during verify. Unless otherwise noted, all resistors are ¼ watt, all NPN transistors are 2N3646, all PNP transistors are 2N4917, and all diodes are IN914.

Figure 2. 2K and 4K Bipolar PROM Pulse Generator

4

SHIFT REGISTERS



SHIFT REGISTERS

	Type	No. of Bits	Description	Electrical Characteristics over Temperature						
				Data Rep. Rate		Power Dissipation Max.[1]	Input Output Levels	Clock Levels	Supplies [V]	Page No.
				Min.	Max.					
SILICON GATE MOS	1402A	1024	Quad 256-Bit Dynamic	10 kHz	5MHz	500 mW	TTL	MOS/TTL	5, −5 or 5, −9	4-3
	1403A	1024	Dual 512-Bit Dynamic	10 kHz	5MHz	500 mW	TTL	MOS/TTL	5, −5 or 5, −9	4-3
	1404A	1024	1024-Bit Dynamic	10 kHz	5MHz	500 mW	TTL	MOS/TTL	5, −5 or 5, −9	4-3
	1405A	512	Dynamic Recirculating	10 kHz	2MHz	400 mW	TTL	MOS/TTL	5, −5 or 5, −9	4-7
	1506[2]	200	Dual 100-Bit Dynamic	6 kHz	2MHz	110 mW	TTL	MOS	+5, −5	4-11
	1507[2]	200	Dual 100-Bit Dynamic (20 kΩ output)	6 kHz	2MHz	110 mW	TTL	MOS	+5, −5	4-11
	2401	2048	Dual 1024-Bit Dynamic Recirculating	25 kHz	1 MHz	350 mW	TTL	TTL	+5	4-15
	2405	1024	1024-Bit Dynamic Recirculating	25 kHz	1 MHz	350 mW	TTL	TTL	+5	4-15
	2416	16,384	CCD Serial Memory	125 kHz	2MHz	300 mW	TTL	MOS	+12, −5	4-19

Notes: 1. Power Dissipation calculated with maximum power supply current and nominal supply voltages.

2. The 1506 and 1507 are also available in military temperature range (−55° to +125°). To order specify 1406 or 1407, respectively.

intel® Silicon Gate MOS 1402A, 1403A, 1404A

1024 BIT DYNAMIC SHIFT REGISTER

- **Guaranteed 5 MHz Operation over Temperature Range**
- **Low Power Dissipation -- .1 mW/bit at 1 MHz**
- **DTL, TTL Compatible**
- **Low Clock Capacitance -- 140 pF**
- **Low Clock Leakage -- ≤ 1 μA**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- 8 Lead Metal Can, 16 Pin Ceramic Dual In-Line**
- **Three Standard Configurations -- Quad 256 Bit -- 1402A, Dual 512 Bit -- 1403A, Single 1024 Bit -- 1404A**

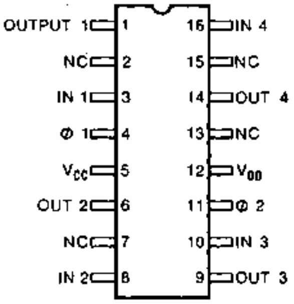
The 1402A/1403A/1404A are direct pin for pin replacements for the 1402/1403/1404. Due to "on chip" multiplexing the data rate is twice the clock rate. Data is shifted one bit on each clock pulse (both ϕ_1 and ϕ_2).

The 1402A/1403A/1404A family is ideally suited for usage in low cost serial memories or delay line applications. A high speed data rate of 5 MHz is easily obtained at the power supplies of +5V and −5V. The 1402A/3A/4A are capable of operating at the power supply voltages of +5V, −9V as well as +5V, −5V.

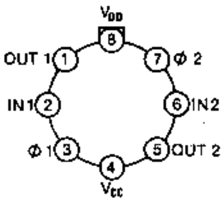
The input to the shift register can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The design of the output stage provides driving capability for both MOS and bipolar IC's.

Use of low threshold silicon gate technology allows high speed (5 MHz guaranteed) while reducing power dissipation by a factor of two and clock input capacitance by a factor of three compared to equivalent products manufactured by conventional technologies.

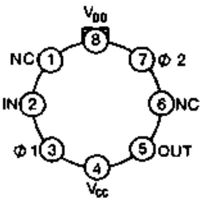
PIN CONFIGURATION



C1402A/P1402A



M1403A



M1404A

Absolute Maximum Ratings(1)

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
Power Dissipation (2)	1 Watt
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V

D.C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ±5% or −9V ±5%

SYMBOL	TEST	MIN.	TYP(3)	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current		<10	500	nA	T_A =25°C
I_{LO}	Output Leakage Current		<10	1000	nA	V_{OUT}=0.0V, T_A =25°C
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, T_A =25°C
V_{IL}	Input "Low" Voltage	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH}	Input "High" Voltage	$V_{CC}-1.5$		$V_{CC}+.3$	V	

V_{DD} = −5V ±5%

I_{DD1}	Power Supply Current		40	50	mA	T_A=25°C Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, $V_{ILC}=V_{CC}-17V$
I_{DD2}	Power Supply Current			56	mA	T_C=0°C
V_{ILC}	Clock Input Low Voltage	$V_{CC}-17$		$V_{CC}-15$	V	
V_{IHC}	Clock Input High Voltage	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}=−100 μA
V_{OH2}	Output High Voltage Driving MOS	$V_{CC}-1.4$	$V_{CC}-1$		V	R_{L2}=4.7K to V_{DD} (See p. 6 for connection)

V_{DD} = −9V ±5%

I_{DD3}	Power Supply Current		30	40	mA	T_A =25°C Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, $V_{ILC}=V_{CC}-14.7V$
I_{DD4}	Power Supply Current			45	mA	T_C =0°C
V_{ILC}	Clock Input Low Voltage	$V_{CC}-14.7$		$V_{CC}-12.6$	V	
V_{IHC}	Clock Input High Voltage	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1} =4.7K to V_{DD}, I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=4.7K to V_{DD}, I_{OH}=−100μA
V_{OH2}	Output High Voltage Driving MOS	$V_{CC}-1.4$	$V_{CC}-1$		V	R_{L2} =6.2K to V_{DD} R_{L3} =3.9K to V_{CC} (See p. 6 for connection)

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 3. When operating at V_{DD} = −5V±5% the maximum duty cycle is 33% and at V_{DD}=−9V+5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle= $[t_{\phi PW} + ½(t_R + t_F)]$x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A.C. Characteristics T_A = 0°C to 70°C; V_{CC} = +5V ±5%

SYMBOL	TEST	V_{DD} = −5V ±5% (Test Load 1)		V_{DD} = −9V ±5% (Test Load 2)		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	μsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE[2] V_{CC} = +5V ±5%, V_{DD} = −5V ±5% or −9V ±5%, T_A = 25°C

SYMBOL	TEST	TYP.	MAX.	CONDITIONS	
C_{IN}	Input Capacitance	5 pF	10 pF	$V_{IN} = V_{CC}$	f = 1 MHz
C_{OUT}	Output Capacitance	5 pF	10 pF	$V_{OUT} = V_{CC}$	
C_{ϕ}	Clock Capacitance	110 pF	140 pF	$V_{\phi} = V_{CC}$	
$C_{\phi 1 \phi 2}$	Clock to Clock Capacitance	11 pF	16 pF	$V_{\phi} = V_{CC}$	

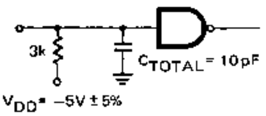
Note 1: See page 5 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

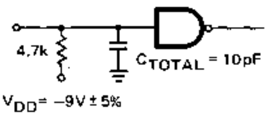
Conditions of Test

Input rise and fall times: 10 nsec
Output load is 1 TTL gate

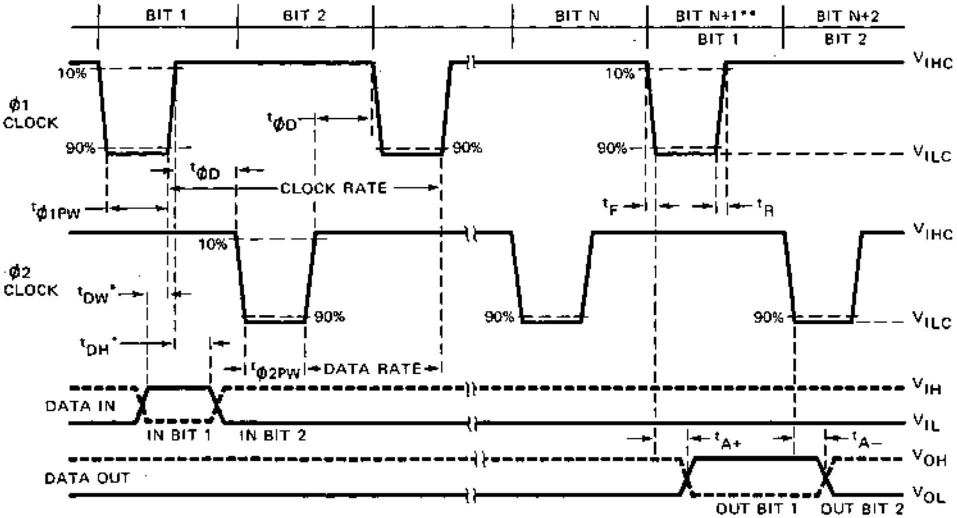
TEST LOAD 1



TEST LOAD 2



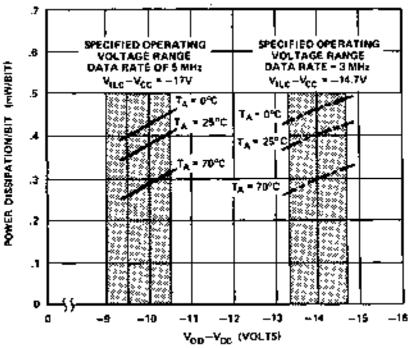
Timing Diagram



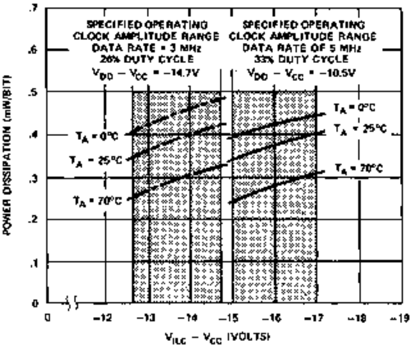
*t_{DW} and t_{DH} same for $t_{\phi 2}$ **N = 256 for 1402A, N = 512 for 1403A, N = 1024 for 1404A

Typical Characteristics

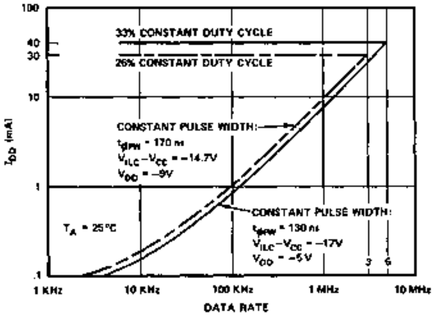
POWER DISSIPATION / BIT VS SUPPLY VOLTAGE



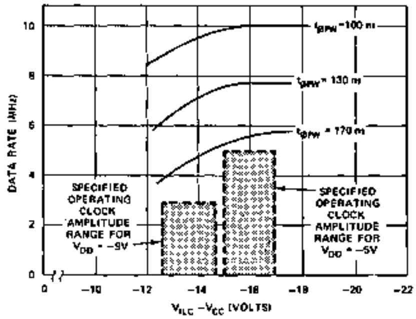
POWER DISSIPATION / BIT VS CLOCK AMPLITUDE



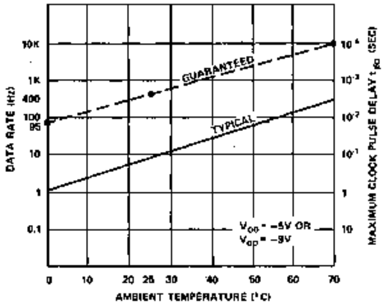
I_{DD} CURRENT VS DATA RATE



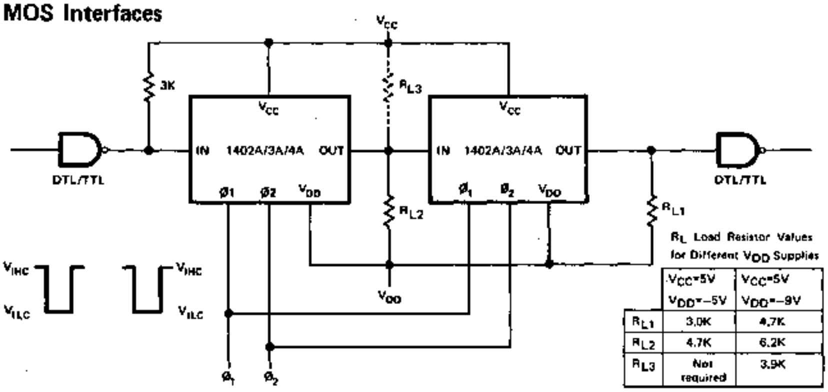
MAXIMUM DATA RATE VS CLOCK AMPLITUDE



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	$V_{CC}=5V$ $V_{DD}=-5V$	$V_{CC}=5V$ $V_{DD}=-9V$
R_{L1}	3.0K	4.7K
R_{L2}	4.7K	6.2K
R_{L3}	Not required	3.9K

intel®

Silicon Gate MOS **1405A**

512 BIT DYNAMIC RECIRCULATING SHIFT REGISTER

- **High Frequency Operation -- 2 MHz Guaranteed over Temperature.**
- **DTL, TTL Compatible**
- **Write/Recirculate and Read Controls Incorporated on the Chip**
- **Low Power Dissipation -- .3 mW/bit at 1 MHz**
- **Low Clock Capacitance -- 85 pF**
- **Low Clock Leakage -- ≤1 uA at −17 V**
- **Simple Two Dimensional Memory Matrix Organization -- 2 Chip Select Controls**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- 10 Lead Low Profile TO-99**

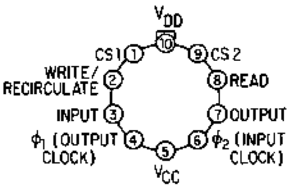
The 1405A is a 512 bit dynamic recirculating shift register and is a direct pin replacement for the 1405. The 1405A is capable of operating at power supply voltages of +5V, −9V as well as +5V, −5V. A high speed recirculating data rate of 2 MHz over the temperature is easily obtained at the +5, −5 power supplies.

Write/recirculate and read controls eliminate the need for external logic elements when recirculating data. In addition, any number of devices can be combined to form a multi-dimensional memory array. For this purpose two chip select controls have been provided.

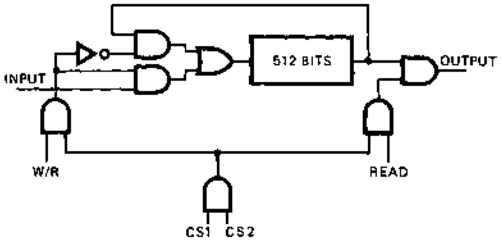
These registers can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for both MOS and bipolar IC's as well as OR-tieing of shift registers. The 1405A is ideally suited for usage in low cost memories or delay line applications.

Use of low threshold **silicon gate technology** allows high speed (2 MHz guaranteed) while reducing power dissipation by a factor of two and clock input capacitance by a factor of **three** over equivalent products manufactured by conventional technologies.

PIN CONFIGURATION



LOGIC DIAGRAM



PIN / MODE	W/R (2)	CS1 (1)	CS2 (9)	READ (8)
WRITE	1	1	1	1 or 0
RECIRCULATE(1)	1 or 0	1 or 0	1 or 0	1 or 0
READ	1 or 0	1	1	1

Note 1: Either W/R, CS1, or CS2 must be a "0" during Recirculation.

A logic 1 is defined as a high input and a logic 0 as a low input.

Maximum Guaranteed Ratings *

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +160°C
Power Dissipation (1)	600 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+.3V to −20V

* COMMENT:
Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified

$V_{DD} = -5V \pm 5\%$

SYMBOL	TEST	MIN.	TYP.(2)	MAX.	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	$V_{OUT} = 0.0V$
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC} = V_{CC} - 17V$
I_{DD1}	POWER SUPPLY CURRENT		25	40	mA	$T_A = 25°C$ Output at Logic "0", 2 MHz Data Rate, 40% Duty Cycle, Continuous Operation,
I_{DD2}	POWER SUPPLY CURRENT			45	mA	$T_C = 0°C$ $V_{ILC} = V_{CC} - 17V$
V_{ILC1}	CLOCK INPUT LOW VOLTAGE	$V_{CC} - 17$		$V_{CC} - 14.5$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC} - 1$		$V_{CC} + .3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC} - 10$		$V_{CC} - 4.2$	V	
V_{IH1}	INPUT "HIGH" VOLTAGE	$V_{CC} - 1.5$		$V_{CC} + .3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	$R_{L1} = 3K$ to V_{DD}, $I_{OL} = 1.6$ mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	$R_{L1} = 3K$ to V_{DD}, $I_{OH} = -100\ \mu A$
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC} - 1.4$	$V_{CC} - 1$		V	$R_{L2} = 5.6K$ to V_{DD} (see p. 6 for connection)

$V_{DD} = -9V \pm 5\%$

I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	$V_{OUT} = 0.0V$
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC} = V_{CC} - 14.7V$
I_{DD3}	POWER SUPPLY CURRENT		20	31	mA	$T_A = 25°C$ Output at Logic "0", 1.5 MHz Data Rate, 36% Duty Cycle, Continuous Operation,
I_{DD4}	POWER SUPPLY CURRENT			36	mA	$T_C = 0°C$ $V_{ILC} = V_{CC} - 14.7V$
V_{ILC2}	CLOCK INPUT LOW VOLTAGE	$V_{CC} - 14.7$		$V_{CC} - 12.6$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC} - 1$		$V_{CC} + .3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC} - 10$		$V_{CC} - 4.2$	V	
V_{IH2}	INPUT "HIGH" VOLTAGE	$V_{CC} - 1.5$		$V_{CC} + .3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	$R_{L1} = 5.6K$ to V_{DD} $I_{OL} = 1.6$ mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	$R_{L1} = 5.6K$ to V_{DD}, $I_{OH} = -100\ \mu A$
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC} - 1.4$	$V_{CC} - 1$		V	$R_{L2} = 6.2K$ to V_{DD} (See p. 6 for $R_{L3} = 3.9K$ to V_{CC} connection)

Note 1: For operating at elevated temperatures the device must be derated based as shown on page 3. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $(t_{\phi PW} + ½ (t_R + t_F))$ x clock rate.

Note 2: Typical values are at $T_A = 25°C$ and at nominal voltages.

A.C. Characteristics $T_A = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; $C_L = 20pF$; 1 TTL Load

SYMBOL	TEST	$V_{DD} = -5V \pm 5\%$ $V_{ILC} = V_{CC} - 14.5$ to $V_{CC} - 17$ $R_L = 3$ K		$V_{DD} = -9V \pm 5\%$ $V_{ILC} = V_{CC} - 12.6$ to $V_{CC} - 14.7$ $R_L = 5.6$ K		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	CLOCK DATA REP RATE	200 Hz @ 25°C[1]	2	200Hz @ 25°C[1]	1.5	MHz
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.200	10	.240	10	µsec
$t_{\phi D}$	CLOCK PULSE DELAY	30	Note 1	30	Note 1	nsec
Duty Cycle[2]	CLOCK DUTY CYCLE		40		36	%
t_R; t_F	CLOCK PULSE TRANSITION		1		1	µsec
t_{DW}	DATA WRITE (SETUP) TIME	100		100		nsec
t_{DH}	DATA TO CLOCK HOLD TIME	20		20		nsec
t_{A+}; t_{A-}	CLOCK TO DATA OUT DELAY		250		250	nsec
t_{R-}; t_{CS-}; t_{WR-}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec
t_{R+}; t_{CS+}; t_{WR+}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec

CAPACITANCE[3] $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ or $-9V \pm 5\%$, $T_A = 25°C$

SYMBOL	TEST	TYP.	MAX.	CONDITIONS	
C_{IN}	INPUT CAPACITANCE	3	5 pF	$V_{IN} = V_{CC}$	f = 1 MHz
C_{OUT}	OUTPUT CAPACITANCE	2	5 pF	$V_{OUT} = V_{CC}$	
C_{ϕ}	CLOCK CAPACITANCE	75	85 pF	$V_{\phi} = V_{CC}$	
$C_{\phi_1 \phi_2}$	CLOCK TO CLOCK CAPACITANCE	6	10 pF	$V_{\phi} = V_{CC}$	

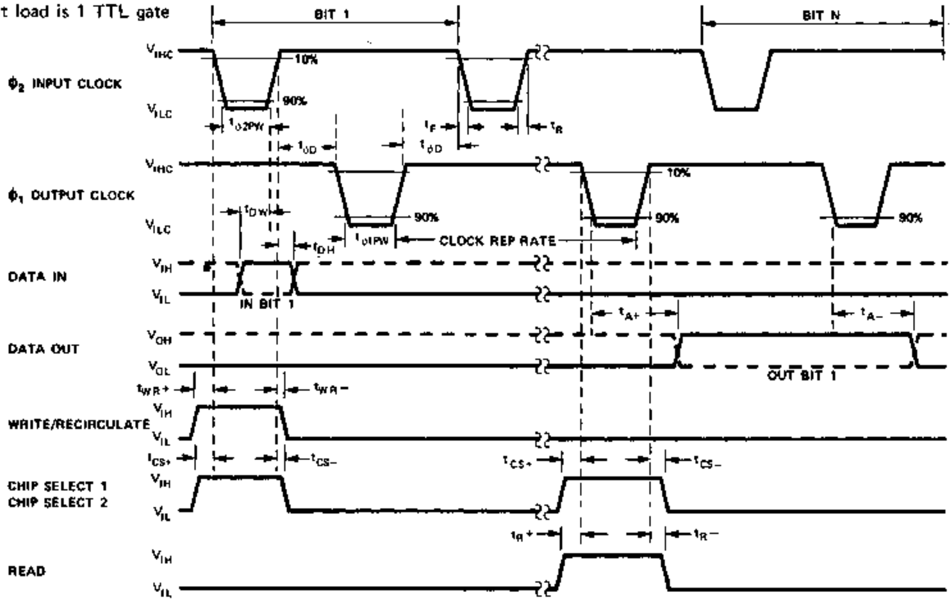
Note 1: See curve of Min Data Rate, and Max Clock Delay vs. Temp. on page 5. Note 2: Duty Cycle = $[t_{\phi PW} + ½(t_R + t_F)]$ x clock rate.
Note 3: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

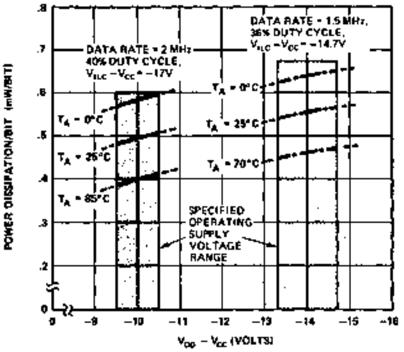
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

Timing Diagram

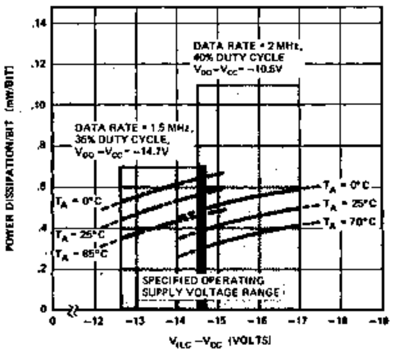


Typical Characteristics

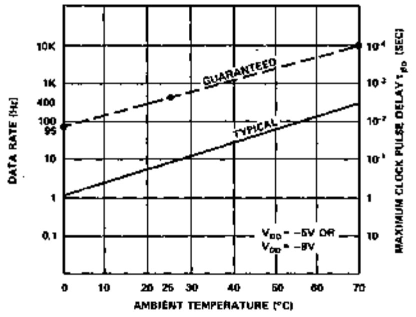
POWER DISSIPATION/BIT VS. SUPPLY VOLTAGE



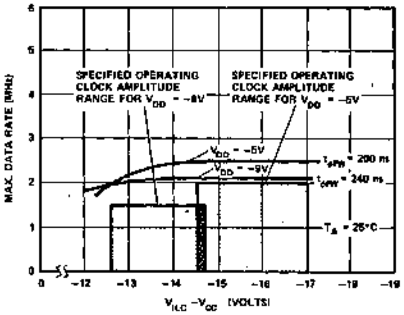
POWER DISSIPATION/BIT VS. CLOCK AMPLITUDE



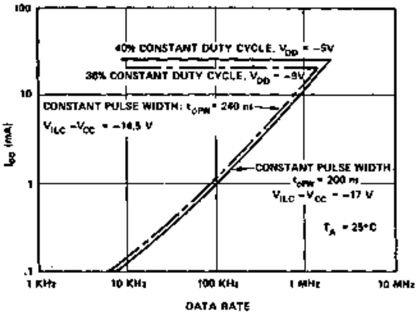
MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



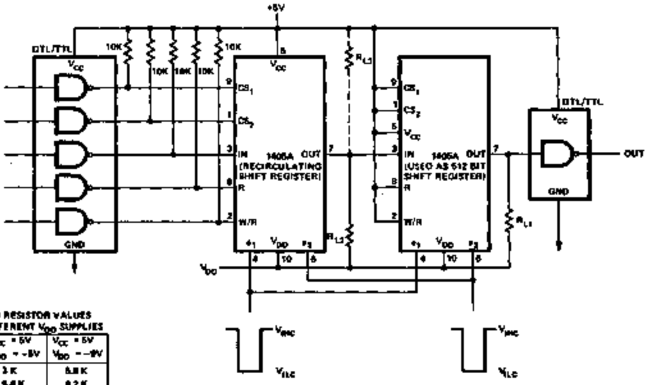
MAXIMUM DATA RATE VS. CLOCK AMPLITUDE



I_{DD} CURRENT VS. DATA RATE



DTL/TTL/MOS Interfaces



R_L LOAD RESISTOR VALUES FOR DIFFERENT V_{DD} SUPPLIES

	$V_{CC} = 5V$ $V_{DD} = -5V$	$V_{CC} = 5V$ $V_{DD} = -9V$
R_{L1}	3 K	6.8 K
R_{L2}	9.6 K	8.2 K
R_{L3}	not required	3.9 K

intel® Silicon Gate MOS **1406, 1506, 1407, 1507**

DUAL 100 BIT DYNAMIC SHIFT REGISTER

- **Low Power Dissipation--.4 mW/bit at 1 MHz**
- **High Frequency Operation -- 2 MHz Guaranteed over Temperature Range**
- **DTL, TTL Compatible**
- **Low Clock Capacitance -- 40 pF**
- **Low Clock Leakage -- ≤.5 μA at −18 V**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- Low Profile TO-5**
- **Military and Commercial Temperature Ranges**
- **Low Output Impedance -- 300Ω Typical**

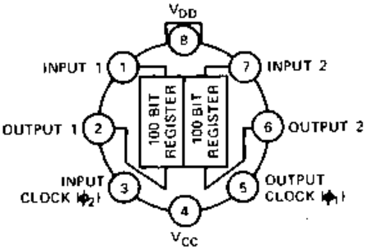
The Intel dual 100 bit dynamic shift register element consists of normally off P-channel MOS devices integrated on a monolithic array. It uses low voltage circuitry to minimize power dissipation and to facilitate interfacing with bipolar integrated circuits. It uses two clock phases only.

The dual 100 bit device can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for MOS or bipolar IC's.

Use of the low threshold **silicon gate technology** allows high speed (2 MHz guaranteed), while reducing power dissipation by a factor of 2 and reducing clock input capacitance by a factor of 3 compared to equivalent products manufactured by conventional MOS technologies.

This family is designed for low cost buffer applications. It is available in both military (—55°C to +125°C) and industrial (0°C to +70°C) grade. It is also available with or without an internal 20K pull-up resistor which may provide easier interfacing to other circuitry.

PIN CONFIGURATION



Configuration	Open Drain Output		20kΩ Output	
	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Dual 100 Bit	1406	1506	1407	1507

Absolute Maximum Ratings*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
Power Dissipation(1)	500 mW
Data and Clock Input Voltages with Respect to Most Positive Supply Voltage, V_{CC}	+.5 V to −25 V
Power Supply Voltage, V_{DD} with Respect to V_{CC}	+.5 V to −25 V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics

T_A= −55°C to +125°C (1406 and 1407)
T_A= 0°C to 70°C (1506 and 1507); V_{CC} = +5V ±5%, V_{DD}=−5V±5% unless otherwise noted.

SYMBOL	PARAMETER	LIMITS MIN.	TYP.(5)	MAX.	UNIT	CONDITION
I_{LI}	INPUT LOAD CURRENT (PIN 1)			500	nA	GND ON PINS 2, 3, 4, 5, 6, 7 PIN 1 = −18V, PIN 8 = −8V T_A = 25°C
I_{LI}	INPUT LOAD CURRENT (PIN 7)			500	nA	GND ON PINS 1, 2, 3, 4, 5, 6 PIN 7 = −18V, PIN 8 = −8V T_A = 25°C
I_{LO}(2, 3)	OUTPUT LEAKAGE CURRENT (PIN 2)			500	nA	GND ON PINS 1, 4, 6, 7, 8 PIN 2 = −18V, PINS 3, 5 = −8V T_A = 25°C
I_{LO}(2, 3)	OUTPUT LEAKAGE CURRENT (PIN 6)			500	nA	GND ON PINS 1, 2, 4, 7, 8 PIN 6 = −18V, PINS 3, 5 = −8V T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT (PIN 3 OR PIN 5)			500	nA	PIN 3, PIN 5 = −18V; PIN 8 = −10V ALL OTHERS AT GND T_A = 25°C
I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		10	17	mA	T_A = −55°C FREQ. = 1 MHz, 30% CLOCK DUTY CYCLE (SEE NOTE 4)
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}		6.0	13	mA	T_A = 0°C
I_{DD3}	POWER SUPPLY CURRENT, V_{DD}		5.0	11	mA	T_A = 25°C
V_{IL}	INPUT "LOW" VOLTAGE	−10	+0.2	+0.8	V	V_{DD} = −5V, V_{CC} = +5V
V_{IH}	INPUT "HIGH" VOLTAGE	+3.5		+5.3	V	V_{DD} = −5V, V_{CC} = +5V
V_{IHC}	CLOCK INPUT "HIGH" LEVEL	+4.0		+5.3	V	V_{DD} = −5V, V_{CC} = +5V
V_{ILC}	CLOCK INPUT "LOW" LEVEL	−13		−9.5	V	V_{DD} = −5V, V_{CC} = +5V
Z_{OUT}	OUTPUT IMPEDANCE		300	750	Ω	V_{DD} = −5V, V_{CC} = +5V I_{SOURCE} = 2.5mA
V_{OL}	OUTPUT "LOW" VOLTAGE		−1.8	0.4	V	I_{OL} = 1.6 mA SEE NOTE 6 FOR R_L
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.5	4		V	I_{OH} = −100 μA SEE NOTE 6 FOR R_L

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150° C/W junction to ambient. The full rating applies for ambient temperatures to +125°C for 1406, 1407 and +70°C for 1506, 1507.

Note 2: For 1407 and 1507 the output on pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 3, 4, and 8 at GND; pin 5 at −15V; pins 1, 7 open; measure pins 2 and 6. $25k\Omega \geq R_{OUT} \geq 15k\Omega$.

Note 3: Not for devices having internal resistors (1407 and 1507).

Note 4: In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle $=[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$ x clock rate.

Note 5: Typical values are at 25°C and at nominal voltage.

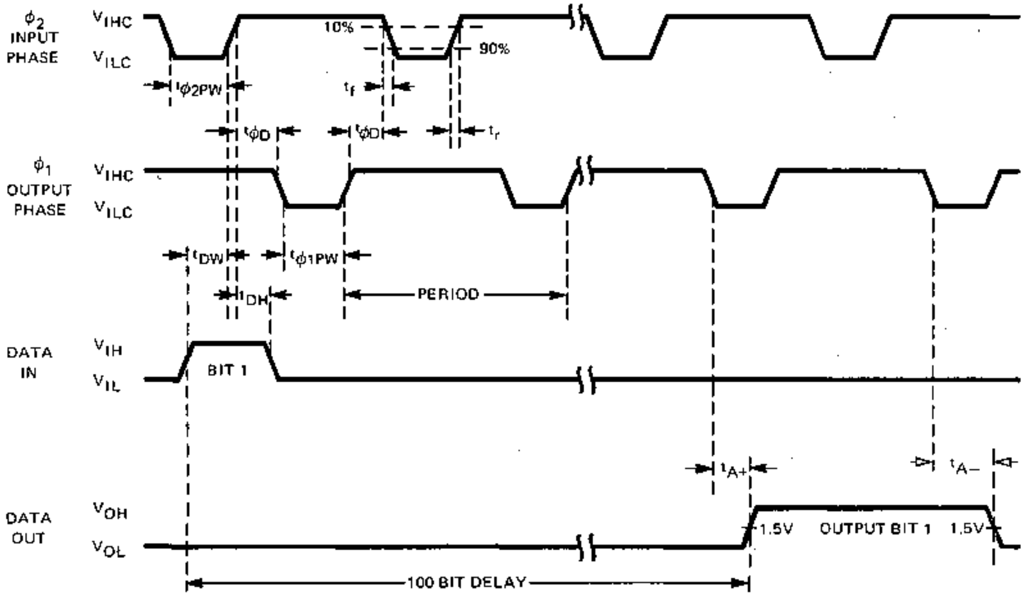
Note 6: For the 1406, 1506 R_L = 3.0K. For the 1407, 1507 R_L = 3.6K. R_L is tied from the output to −5V for a TTL compatible output.

Switching Characteristics

Conditions of Test

Data amplitude +.8 to +2.5V
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

Timing Diagram



A.C. Characteristics $V_{DD} = -5V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, 1 TTL Load, $C_{TOTAL} = 20$ pF.

	1406	1506	1407	1507
T_A	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
R_L	3K	3K	3.6K	3.6K

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	(NOTE 1)	2	MHz	
$t_{\phi 1PW}$	ϕ_1 CLOCK PULSE WIDTH	130		ns	
$t_{\phi 2PW}$	ϕ_2 CLOCK PULSE WIDTH	130		ns	
$t_{\phi D}$	CLOCK PULSE DELAY	100		ns	
t_r, t_f	CLOCK PULSE TRANSITION		50	ns	@ 1 MHz
t_{DW}	DATA WRITE TIME (SET UP)	100		ns	
t_{DH}	DATA TO CLOCK HOLD TIME	100		ns	
t_{A+}, t_{A-}	CLOCK TO DATA OUTPUT DELAY		100	ns	$V_{ILC} - V_{CC} = -16V$

Capacitance[(2)], $T_A = 25°C$

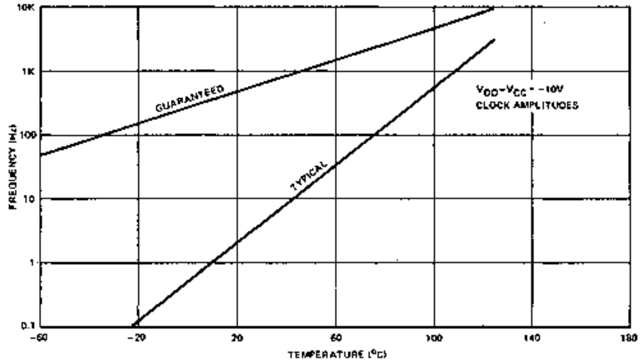
SYMBOL	PARAMETER	LIMIT TYP.	LIMIT MAX.	UNIT	CONDITION
C_{IN}	INPUT CAPACITANCE (PINS 1, 7)		4	pF	$V_{IN} = V_{CC}$
C_{ϕ}	CLOCK INPUT CAPACITANCE (PINS 3, 5)		40	pF	$V_{\phi} = V_{CC}$
C_{ϕ}	CLOCK INPUT CAPACITANCE (PINS 3, 5)		35	pF	$V_{\phi} = -20$ VOLT BIAS
$C_{\phi 1 \phi 2}$	CLOCK TO CLOCK CAPACITANCE	2	4	pF	$V_{\phi} = V_{CC}$
C_{OUT}	OUTPUT CAPACITANCE		5	pF	$V_{OUT} = V_{CC}$

Note 1: See page 6 for guaranteed curve

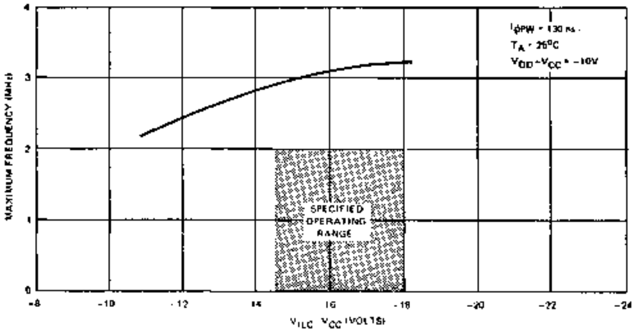
Note 2: This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

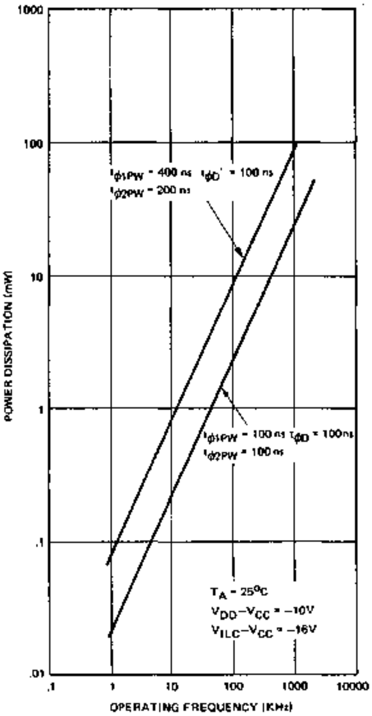
Minimum Operating Frequency



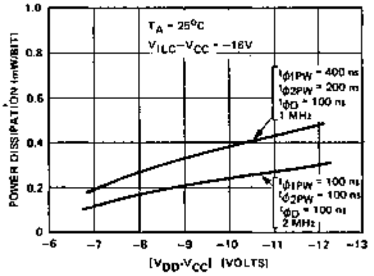
Clock Amplitude vs Maximum Frequency



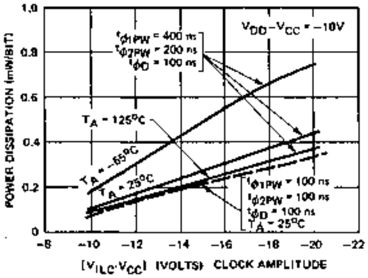
Power Dissipation vs Frequency



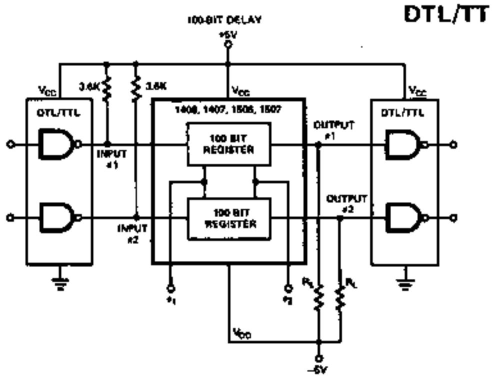
Power Dissipation/Bit vs Supply Voltage

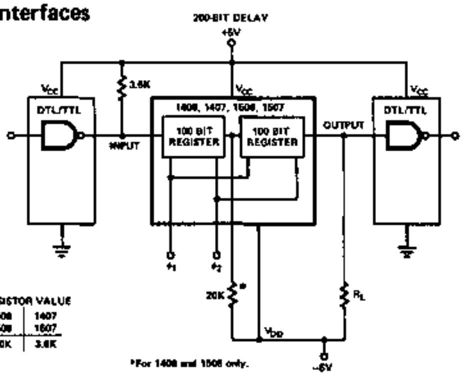


Power Dissipation/Bit vs Clock Amplitude



DTL/TTL MOS Interfaces





LOAD RESISTOR VALUE

	1406 1506	1407 1507
R_L	3.0K	3.6K

*For 1406 and 1506 only.

Silicon Gate MOS 2401, 2405

2048/1024 BIT DYNAMIC RECIRCULATING SHIFT REGISTERS

- **Single Supply Voltage -- +5 Volts**
- **Fully TTL Compatible -- Inputs, Outputs and Clock**
- **Single Phase Clock**
- **Guaranteed 1 MHz Operation with 100 pF Load, over Temperature Range**
- **Low Power Dissipation -- 120 μw/bit typically at 1 MHz**
- **Low Clock Capacitance -- 7 pF**
- **Write/Recirculate and Chip Select Logic Incorporated on Chip**
- **Standard Configurations -- Dual 1024 Bit -- 2401 Single 1024 Bit -- 2405**

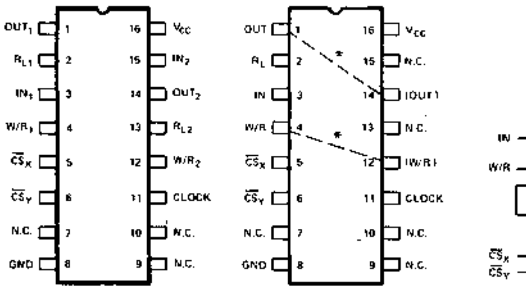
The 2401/2405 are 2048/1024 bit dynamic recirculating shift registers. They are directly TTL compatible in all respects: inputs, outputs, clock and a single +5 volt power supply.

Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

Two chip select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied". A separate internal "pullup" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

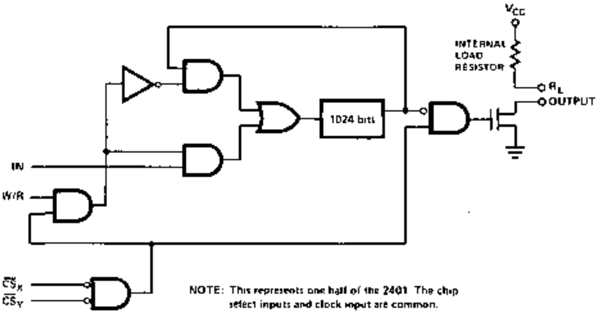
This Intel shift register family is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATIONS



* DASH LINES INDICATE NECESSARY EXTERNAL PRINTED CIRCUIT BOARD CONNECTIONS FOR PROPER OPERATION OF THE 2405. (SEE APPLICATION SECTION)

LOGIC DIAGRAM



NOTE: This represents one half of the 2401. The chip select inputs and clock input are common.

PIN NAMES

IN	DATA INPUT	OUT	DATA OUTPUT
W/R	WRITE/RECIRCULATE CONTROL	R_L	INTERNAL LOAD RESISTOR
$\overline{CS}_X$, $\overline{CS}_Y$	CHIP SELECT INPUT	N.C.	NO CONNECTION

TRUTH TABLE

FUNCTION	PIN SYMBOL W/R	$\overline{CS}_X$	$\overline{CS}_Y$
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level
X = Don't Care Condition

Absolute Maximum Ratings*

Ambient Temperature Under Bias:	0° C to 70° C
Storage Temperature:	−65° C to +150° C
Power Dissipation:	1W
Voltage on Any Pin with Respect to Ground:	−0.5V to +7V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

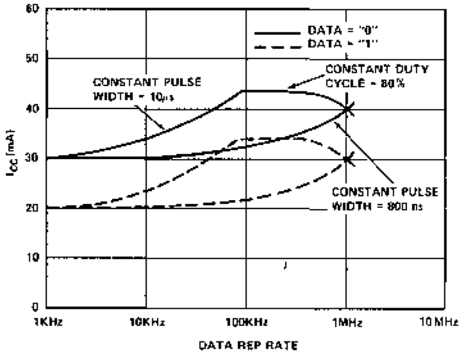
T_A = 0°to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.[1]	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{LI}	INPUT LEAKAGE			10	μA	V_{IN} = 5.25V
I_{LO}	OUTPUT LEAKAGE			100	μA	V_{OUT} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		45 50	70 80	mA mA	T_A = 25°C T_A = 0°C V_{CC} = 5.25V; 80% DUTY CYCLE
V_{IH}	INPUT HIGH LEVEL VOLTAGE (ALL INPUTS)	2.2		5.25	V	
V_{IL}	INPUT LOW LEVEL VOLTAGE (ALL INPUTS)	-0.3		0.65	V	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE	2.4		V_{CC}	V	I_{OH} = -1mA, R_L = 1.5K ± 5% ohms, external
V_{OL}	OUTPUT LOW LEVEL VOLTAGE	0		0.45	V	I_{OL} = 5.0mA, R_L = 1.5K ± 5% ohms, external[2]

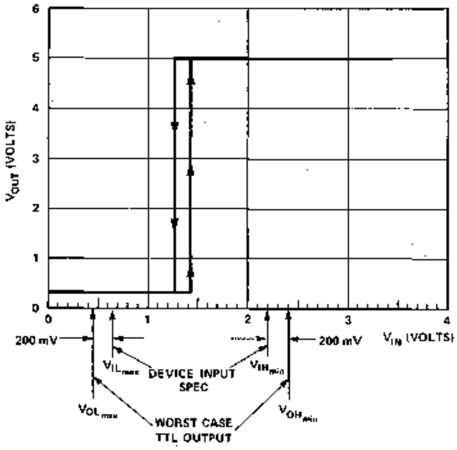
NOTES:
1. Typical values are at 25° C and at nominal voltage.
2. The following was used to calculate I_{OL}.

$$I_{OL} = \frac{V_{CC}\ (\text{max.}) - V_{OL}\ (\text{max.})}{R_L\ (\text{min.})} + I_{LI}\ (\text{TTL device}) = \frac{5.25 - 0.45}{1.425} + 1.6 = 4.97\text{mA.}$$

Also note that the internal load resistor, R_{LI}, has a value ranging from 500 ohms minimum to 2,200 ohms maximum. The internal load resistor can be used when driving from one 2401/2405 to another 2401/2405 or to other MOS inputs.



POWER SUPPLY CURRENT (I_{CC}) VS. DATA REP RATE



EFFECTIVE INPUT CHARACTERISTIC

A. C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.

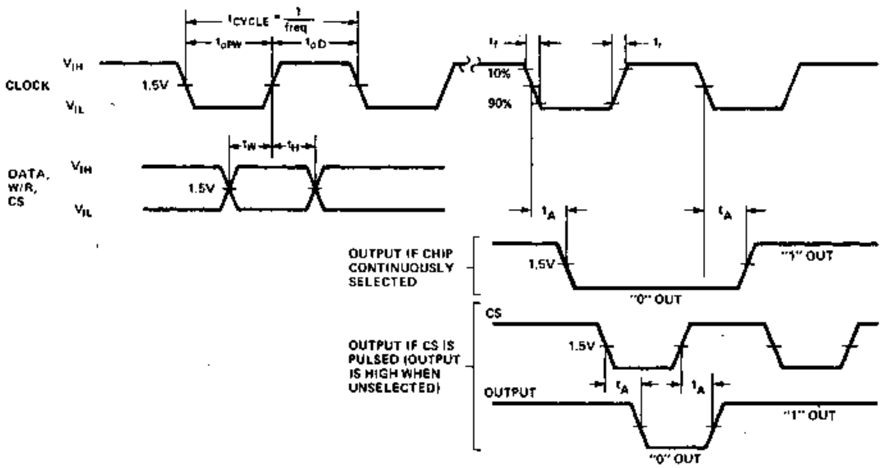
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
FREQ. MAX.	MAX. DATA REP. RATE			1	MHz	
FREQ. MIN.	MIN. DATA REP. RATE	1 25[1]			KHz KHz	$T_A = 25°C$ $T_A = 70°C$
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.80		10	µs	
$t_{\phi D}$	CLOCK PULSE DELAY	0.20 0.20		1000 40	µs µs	$T_A = 25°C$ $T_A = 70°C$
t_r , t_f	CLOCK RISE AND FALL TIME			50	ns	
t_W	WRITE TIME	200			ns	
t_H	HOLD TIME	150			ns	
t_A	ACCESS TIME FROM CLOCK OR CHIP SELECT		250	500	ns	$R_L = 1.5K \pm 5\%$ ohm, EXTERNAL $C_L = 100pF$ ONE TTL LOAD

NOTE: 1. 100 kHz in plastic (P) package.

Capacitance $T_A = 25°C$

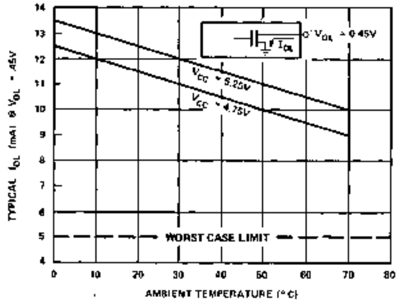
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	DATA, W/R & CS INPUT CAPACITANCE		4	7	pF	ALL PINS AT AC GROUND; 250 mV PEAK TO PEAK, 1 MHz
C_{OUT}	OUTPUT CAPACITANCE		10	14	pF	
C_ϕ	CLOCK CAPACITANCE		4	7	pF	

Waveforms

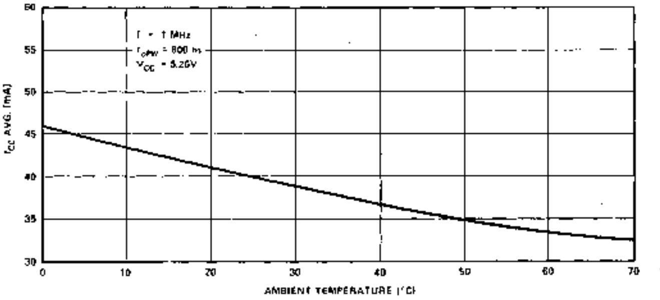


D. C. Characteristics

TEMPERATURE DEPENDENCE OF OUTPUT LOW LEVEL SINK CAPABILITY

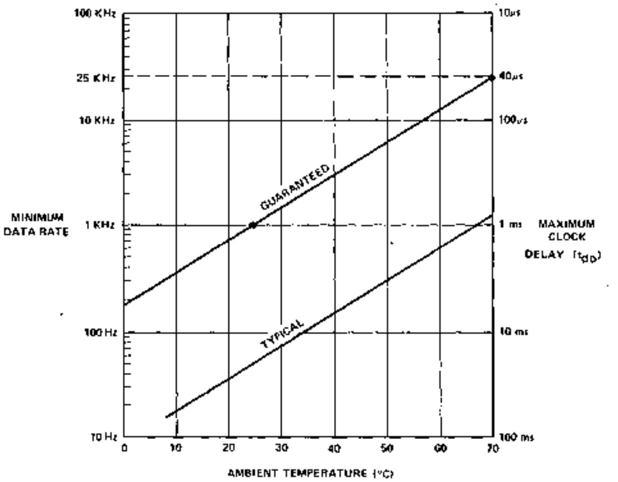


POWER SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE (°C)

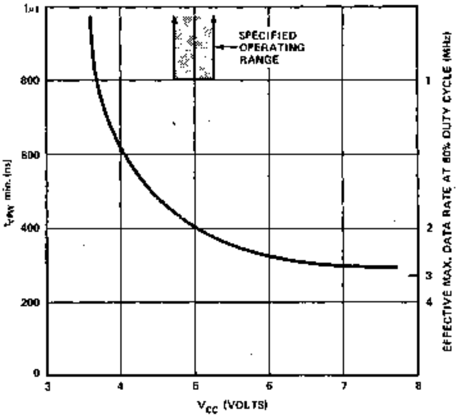


A. C. Characteristics

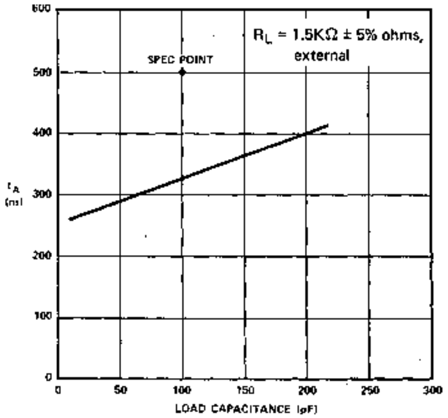
MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY VS. AMBIENT TEMPERATURE FOR CERAMIC (C) PACKAGE



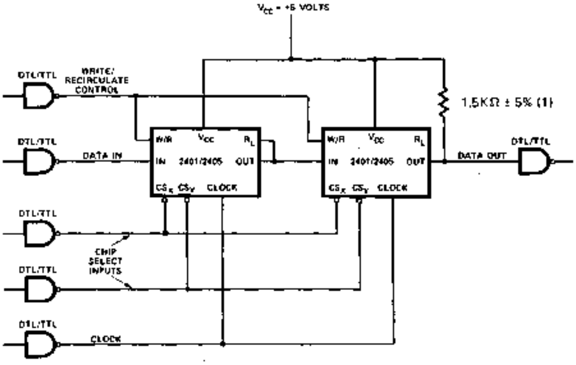
MINIMUM CLOCK PULSE WIDTH AND EFFECTIVE MAXIMUM DATA RATE AT 80% DUTY CYCLE VS. POWER SUPPLY VOLTAGE (V_{CC})



ACCESS TIME VS. LOAD CAPACITANCE



Typical Application Of TTL Compatible Shift Registers



NOTE (1): The 2401/2405 is directly compatible device to device. An external 1.5KΩ ± 5% load resistor is recommended for driving one TTL load with the 2401/2405 output.

intel® Charge Coupled Device **2416**

16,384 BIT CCD SERIAL MEMORY

- **Organization: 64 Recirculating Shift Registers of 256 Bits Each**

- **Avg. Latency Time Under 100 μs**
- **Max. Serial Data Transfer Rate —2 mega bits/sec.**
- **Address Registers Incorporated on Chip**
- **Standard Power Supplies— +12V, −5V**
- **Open Drain Output**
- **Combined Read/Write Cycles Allowed**

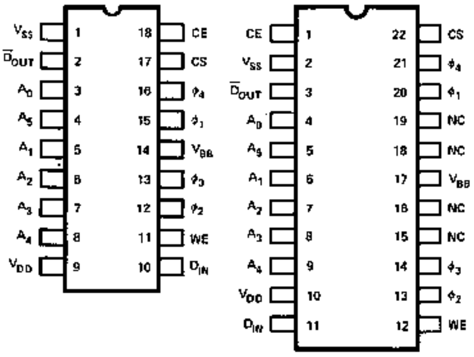
The Intel® 2416 is a 16,384 bit CCD serial memory designed for low-cost memory applications requiring average latency times under 100 μs. To achieve low latency time the memory was organized in the form of 64 independent recirculating shift registers of 256 bits each. Any one of the 64 shift registers can be accessed by applying an appropriate 6-bit address input.

The shift registers recirculate data automatically as long as the four-phase CCD clocks ($\phi_1 \ldots \phi_4$) are continuously applied and no write command is given. A one-bit shift is initiated in all 64 registers following a low-to-high transition of either ϕ_2 or ϕ_4. After the shift operation the contents of the 64 registers at the bit location involved are available for non-destructive reading, and/or for modification. I/O functions are accomplished in a manner similar to that of a 64-bit dynamic RAM. At the next shift cycle, the contents of the 64 accessible bits (whether modified or not) are transferred forward into the respective registers and the contents of the next bit of each register become accessible. No I/O function can be performed during the shift operation itself.

The Intel 2416 generates and uses an internal reference voltage which requires some time to stabilize after the power supplies and four phase clocks have been turned on. No I/O functions should be performed until the four-phase CCD clocks have executed at least 4000 shift cycles with power supplies at operating voltages. After this start-up period, no special action is needed to keep the internal reference voltage stable.

The 2416 is fabricated using Intel's advanced high voltage N-channel Silicon Gate MOS process.

PIN CONFIGURATIONS

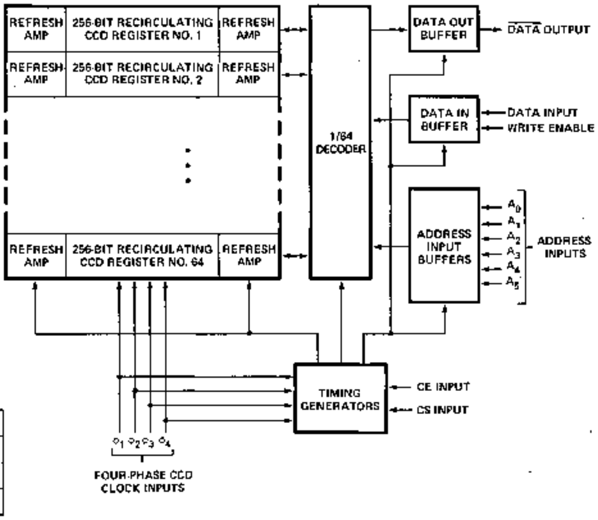

P2416

C2416

PIN NAMES

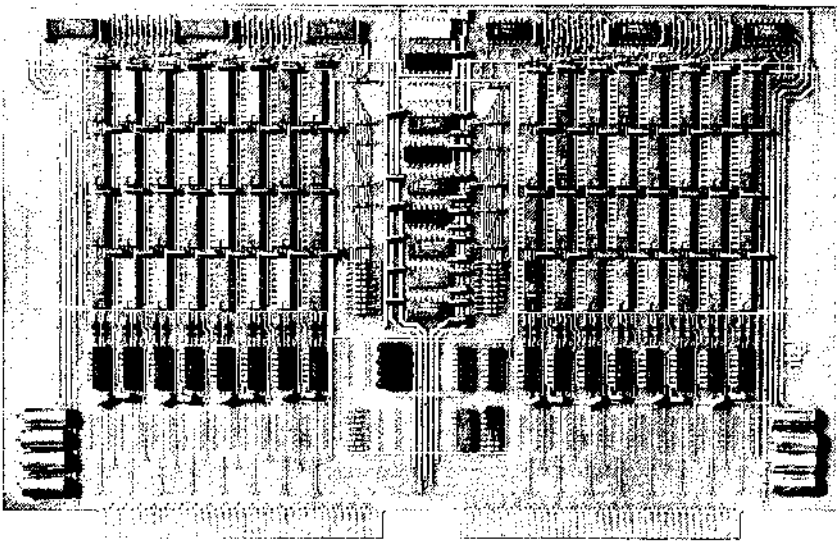
A_0-A_5	ADDRESS INPUTS	CE	CHIP ENABLE INPUT
D_{IN}	DATA INPUT	ϕ_1-ϕ_4	CCD CLOCK INPUTS
WE	WRITE ENABLE INPUT	V_{DD}, V_{SS}, V_{BB}	POWER SUPPLIES
CS	CHIP SELECT INPUT	$\overline{D}_{OUT}$	DATA OUTPUT

BLOCK DIAGRAM

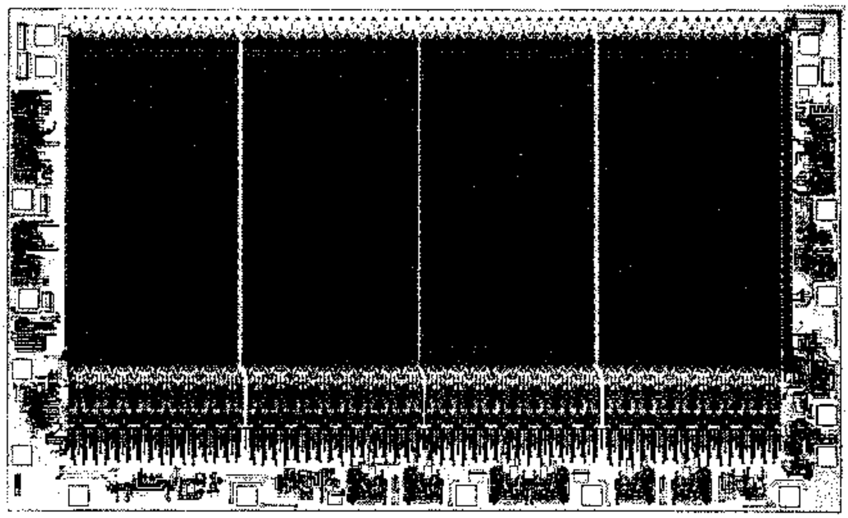


CHARGE COUPLED DEVICE 2416

Pictured below is a 1 million bit CCD Storage Card built with Intel's 2416 CCD Register. The card has an average latency time (access time to any bit) of less than 100 μs and a maximum data transfer rate of 16 million bits per second which may be increased to 64 million bits per second by using interleaved accesses.

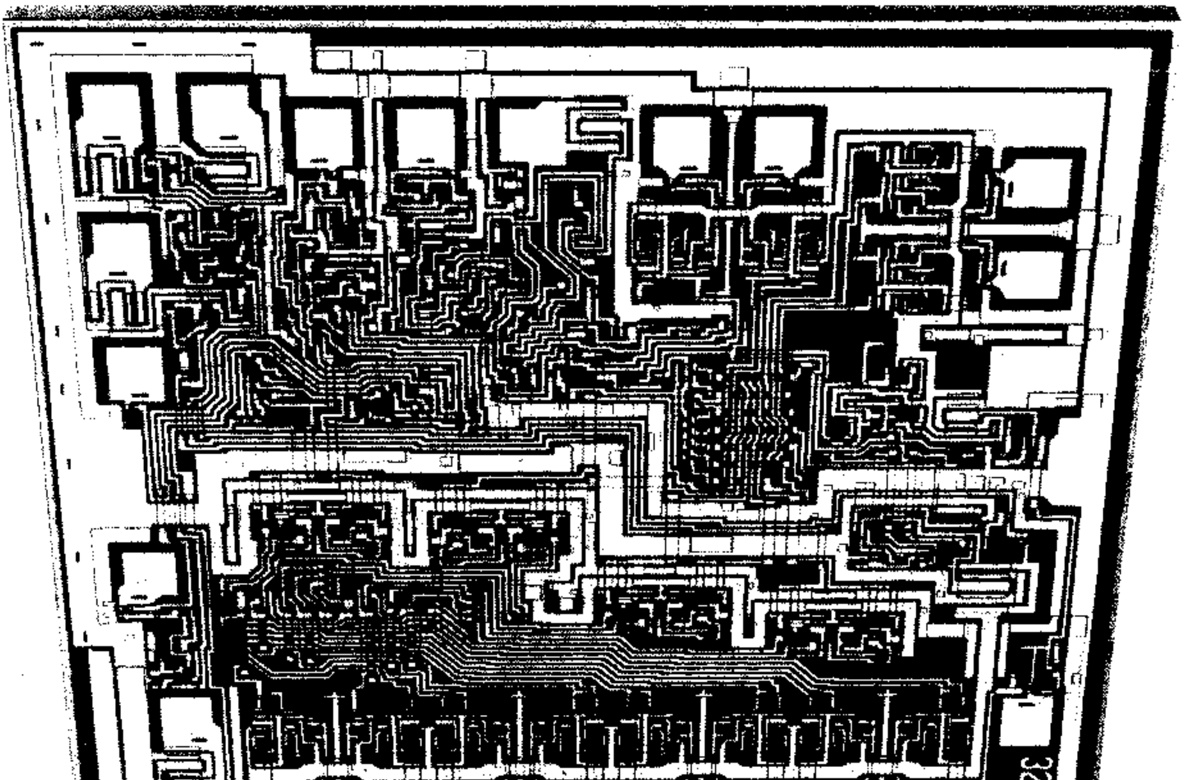


The photomicrograph below is of the 2416 16,384 bit CCD Register Chip.



5

MEMORY PERIPHERALS



MEMORY PERIPHERALS

	Type	Description	Electrical Characteristics over Temperature		Supplies [V]	Page No.
			Input to Output Delay Maximum	Power Dissipation[1] Maximum		
SCHOTTKY BIPOLAR	3205	1 of 8 Binary Decoder	18ns	350mW	+5	5-3
	3207A	Quad Bipolar to MOS Level Shifter and Driver	25ns	900mW	+5, +16, +19	5-7
	3207A-1	Quad Bipolar to MOS Level Shifter and Driver	25ns	1040mW	+5, +19, +22	5-11
	3208A	Hex Sense Amp for MOS Memories	20ns	600mW	+5	5-13
	3210	Single High Voltage Bipolar to MOS Level Shifter and Driver plus Quad Low Voltage Bipolar to MOS Level Shifter and Driver	40ns	570mW	+5, +12[2]	5-19
	3211	Single High Voltage ECL to MOS Level Shifter and Driver plus Quad Low Voltage ECL to MOS Level Shifter and Driver	45ns	705mW	+5, +12[2]	5-23
	3235	Quad Bipolar to MOS Level Shifter and Driver	32ns	690mW	+5, +12, +15	5-27
	3404	High Speed 6-Bit Latch	12ns	375mW	+5	5-3
	3408A	Hex Sense Amp and Latch for MOS Memories	25ns	625mW	+5	5-13

Notes: 1. Power Dissipation calculated with maximum power supply current and nominal power supply voltages.
2. One external PNP transistor is required.

3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER
3404 HIGH SPEED 6-BIT LATCH

- **18 ns max. Delay Over 0°C to 75°C Temperature -- 3205**
- **12 ns max. Data to Output Delay Over 0°C to 75°C Temperature -- 3404**
- **Directly Compatible with DTL and TTL Logic Circuits.**
- **Low Input Load Current -- .25 mA max., 1/6 Standard TTL Input Load.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Outputs Sink 10 mA min.**
- **16-Pin Dual In-Line Package.**
- **Simple Expansion -- Enable Inputs.**

3205

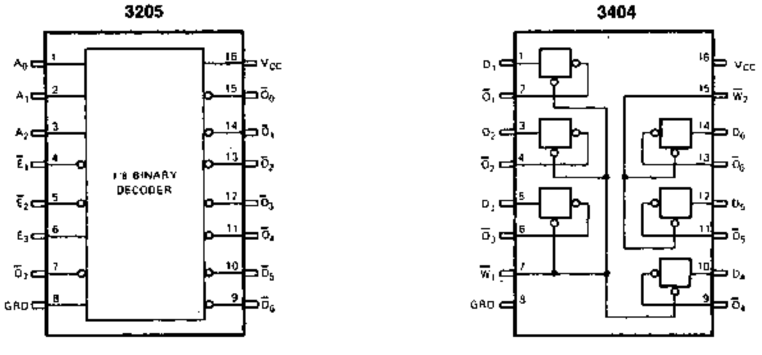
The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of it's eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION


3205

3404

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

3205, 3404

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	μA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA

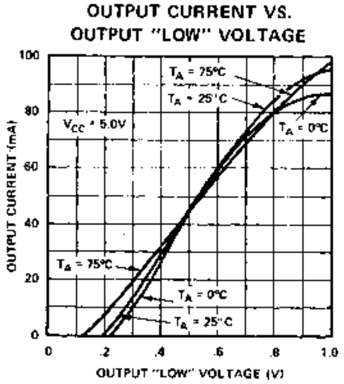
3205 ONLY

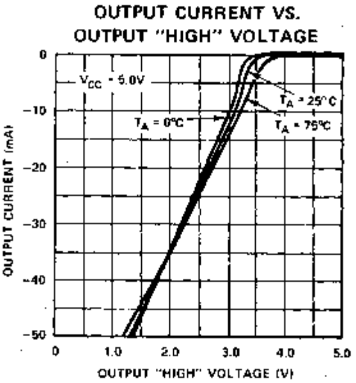
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V

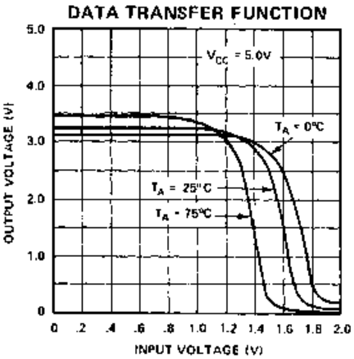
3404 ONLY

I_{CC}	POWER SUPPLY CURRENT		75	mA	V_{CC} =5.25V
I_{FW1}	WRITE ENABLE LOAD CURRENT PIN 7		−1.00	mA	V_{CC}=5.25V, V_W=0.45V
I_{FW2}	WRITE ENABLE LOAD CURRENT PIN 15		−0.50	mA	V_{CC}=5.25V, V_W=0.45V
I_{RW}	WRITE ENABLE LEAKAGE CURRENT		10	μA	V_R=5.25V

Typical Characteristics


OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE


OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE


DATA TRANSFER FUNCTION

3205-HIGH SPEED 1 OUT OF 8 BINARY DECODER

Switching Characteristics

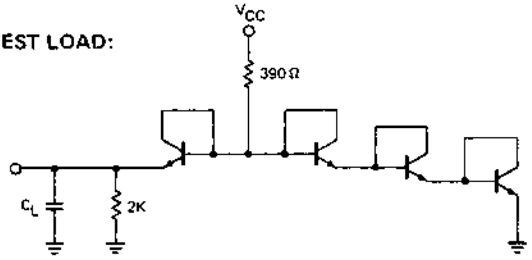
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

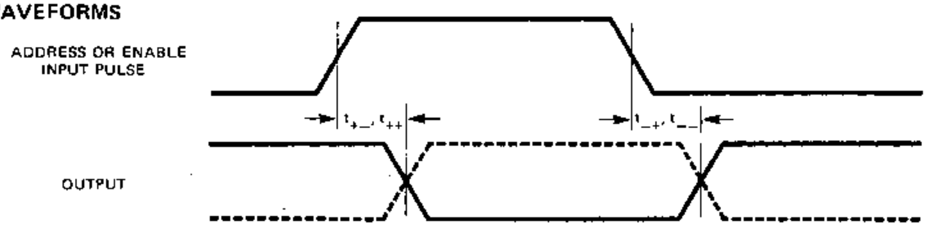
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



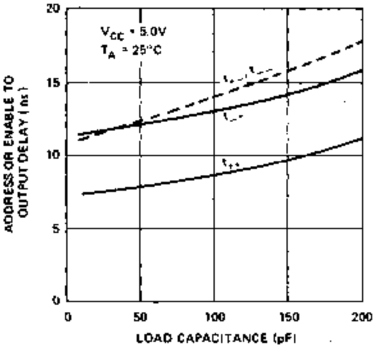
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} [1]	INPUT CAPACITANCE	P3205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C3205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

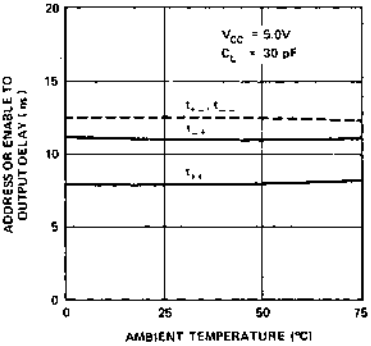
1. This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



3404 - 6-BIT LATCH

Switching Characteristics

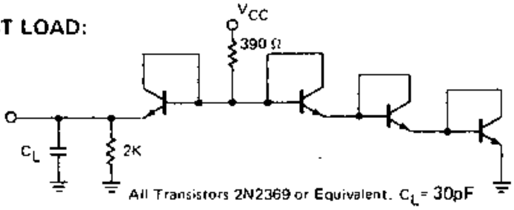
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

Measurements are made at 1.5V

TEST LOAD:

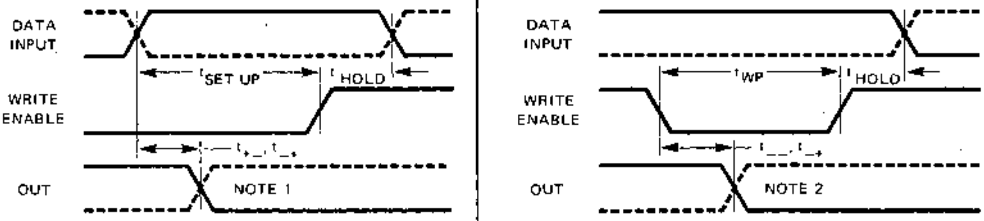


All Transistors 2N2369 or Equivalent. C_L = 30pF

TEST WAVEFORMS

MEASUREMENT FOR DATA DELAY

MEASUREMENT FOR WRITE ENABLE DELAY



NOTE 1: Output Data is valid after t_{+-}, t_{-+}

NOTE 2: Output Data is valid after t_{--}, t_{-+}

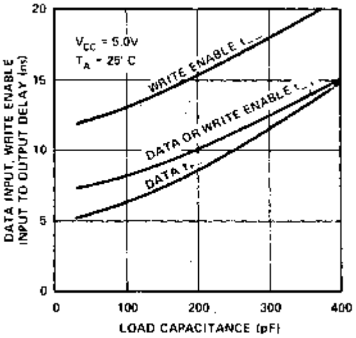
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER		LIMITS			UNIT	TEST CONDITIONS
			MIN.	TYP.	MAX.		
t_{+-}, t_{-+}	DATA TO OUTPUT DELAY				12	ns	
t_{--}, t_{-+}	WRITE ENABLE TO OUTPUT DELAY				17	ns	
$t_{SET\ UP}$	TIME DATA MUST BE PRESENT BEFORE RISING EDGE OF WRITE ENABLE		12			ns	
t_{HOLD}	TIME DATA MUST REMAIN AFTER RISING EDGE OF WRITE ENABLE		8			ns	
t_{WP}	WRITE ENABLE PULSE WIDTH		15			ns	
C_{IND}(3)	DATA INPUT CAPACITANCE	P3404		4		pF	f = 1 MHz, V_{CC} = 0V
		C3404		5		pF	V_{BIAS} = 2.0V, T_A = 25°C
C_{INW}(3)	WRITE ENABLE CAPACITANCE	P3404		7		pF	f = 1 MHz, V_{CC} = 0V
		C3404		8		pF	V_{BIAS} = 2.0V, T_A = 25°C

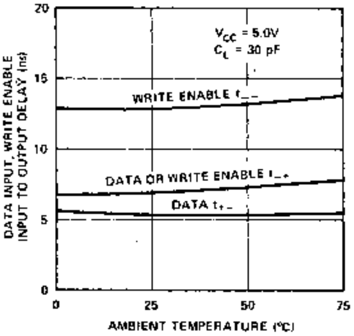
NOTE 3: This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

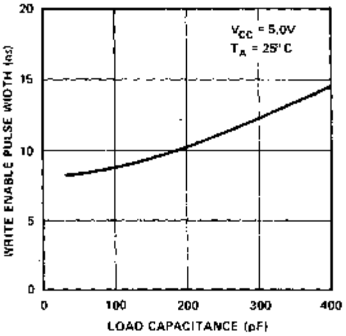
DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. LOAD CAPACITANCE



intel® Schottky Bipolar **3207A**

QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

- **High Speed, 45 nsec Max.-- Delay + Transition Time Over Temperature with 200 pF Load**
- **TTL & DTL Compatible Inputs**
- **1103 and 1103A Memory Compatible at Output**
- **Simplifies Design--Replaces Discrete Components**
- **Easy to Use--Operates from Standard Bipolar and MOS Supplies**
- **Minimum Line Reflection--Input and Output Clamp Diodes**
- **High Input Breakdown Voltage-- 19 Volts**
- **CerDIP Package--16 Pin DIP**

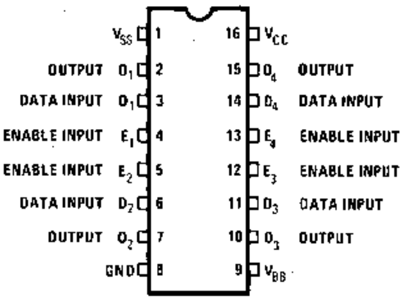
The 3207A is a Quad Bipolar-to-MOS level shifter and driver which accepts TTL and DTL input signals, and provides high output current and voltage suitable for driving MOS circuits. It is particularly suitable for driving the 1103 and 1103A memory chips. The circuit operates from a 5 volt TTL power supply, and V_{SS} and V_{BB} power supplies from the 1103 and 1103A.

The device features two common enable inputs per pair of devices which permits some logic to be done at their inputs, such as cenable and precharge decoding for the 1103 and 1103A.

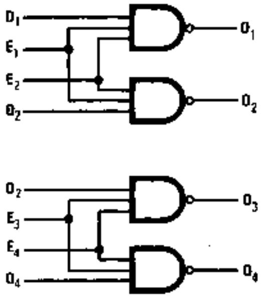
For the TTL inputs a logic "1" is V_{IH} and a logic "0" is V_{IL}. The 3207A outputs correspond to a logic "1" as V_{OL} and a logic "0" as V_{OH} for driving MOS inputs.

The 3207A is packaged in a hermetically sealed 16 pin ceramic dual-in-line package. The device performance is specified over the same temperature range as the 1103 and 1103A, i.e. from 0°C to +70°C.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias .... 0°C to +70°C
Storage Temperature........... –65°C to +160°C
All Input Voltages and V_{SS}.......... –1.0 to +21V
Supply Voltage V_{CC} .... –1.0 to +7V
All Outputs and Supply Voltage
V_{BB} with respect to GND .... –1.0 to +25V
Power Dissipation at 25°C............ 2 Watts (1)

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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(1) Refer to the graph of Junction Temperature versus Total Power Dissipation on page 5-10 for other temperatures.

D. C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT		UNIT	CONDITIONS
		MIN.	MAX.		
I_{FD}	DATA INPUT LOAD CURRENT		–0.25	mA	$V_D = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{FE}	ENABLE INPUT LOAD CURRENT		–0.50	mA	$V_E = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{OL}	OUTPUT "LOW" VOLTAGE		.8 .7 .6	V(0°C) V(25°C) V(70°C)	$I_{OL} = 500\mu A$, $V_{CC} = 4.75V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - .7$ $V_{SS} - .6$ $V_{SS} - .5$		V(0°C) V(25°C) V(70°C)	$I_{OH} = -500\mu A$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$, $V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	–100		mA	$V_O = V_{SS} - 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$ $V_{BB} = 19V$, $V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
C_{IN}	INPUT CAPACITANCE	8(Typical)		pF	$V_{BIAS} = 2.0V$, $V_{CC} = 0V$

POWER SUPPLY CURRENT DRAIN:

All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		21	mA	
P_{TOTAL}	Total Power Dissipation		900	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}	33	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Grounded
I_{SS}	Current from V_{SS}	250	μA	
I_{BB}	Current from V_{BB}	3	mA	
P_{TOTAL}	Total Power Dissipation	250	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}	0	mA	$V_{CC} = 0V$, $V_{SS} = 16.8V$, $V_{BB} = 16.8V$
I_{SS}	Current from V_{SS}	250	μA	
I_{BB}	Current from V_{BB}	250	μA	
P_{TOTAL}	Total Power Dissipation	10	mW	

Switching Characteristics

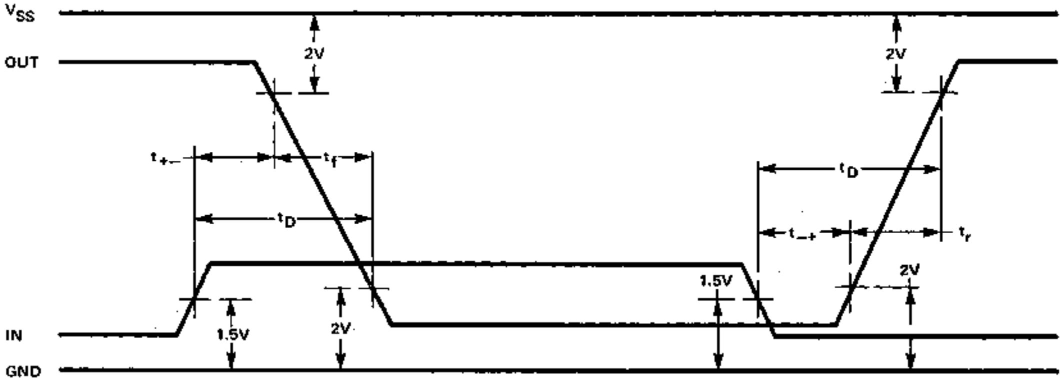
A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 16V \pm 5\%$, $V_{BB} = V_{SS} + 3$ to $4V$, f = 2 MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		C_L = 100 pF		C_L = 200 pF		DELAY DIFFERENTIAL(1) C_L = 200 pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	20	10	30	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

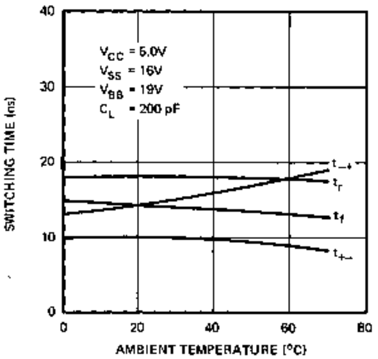
(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

Waveforms

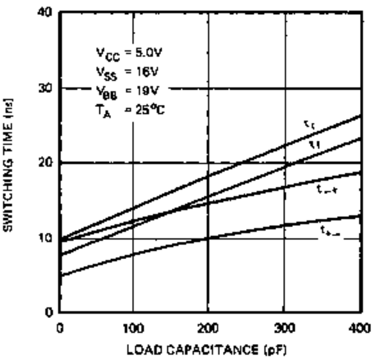


Typical Characteristics

SWITCHING TIME VS. AMBIENT TEMPERATURE

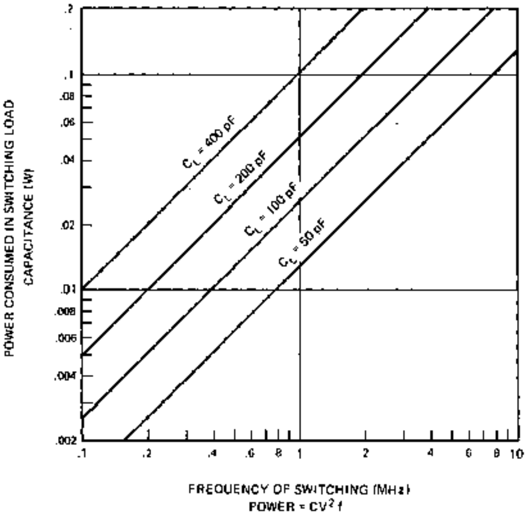


SWITCHING TIME VS. LOAD CAPACITANCE

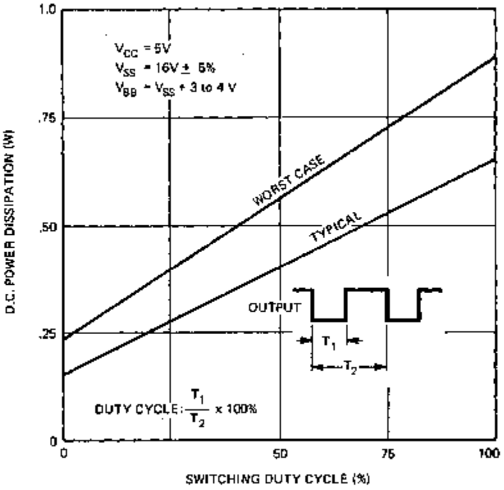


Power and Switching Characteristics

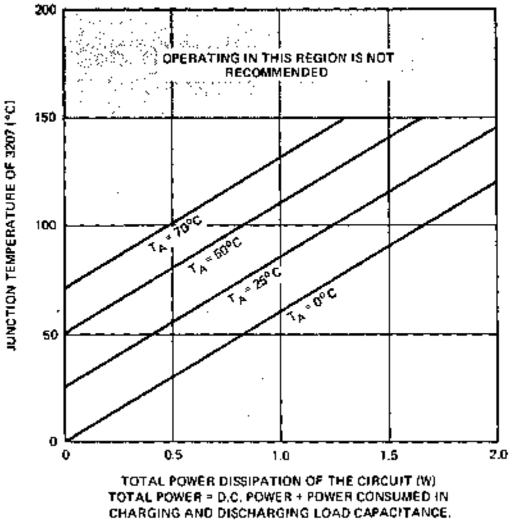
POWER CONSUMED IN CHARGING AND DISCHARGING LOAD CAPACITANCE OVER 0V TO 16V INTERVAL



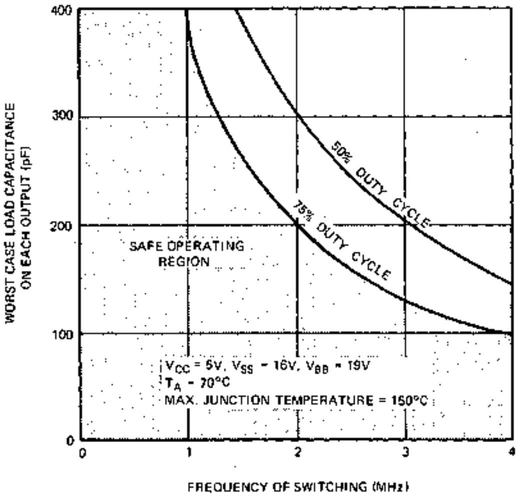
NO LOAD D.C. POWER DISSIPATION VS. OPERATING DUTY CYCLE



JUNCTION TEMPERATURE VS. TOTAL POWER DISSIPATION OF THE CIRCUIT



WORST CASELOAD CAPACITANCE ON EACH OUTPUT VS. FREQUENCY OF SWITCHING



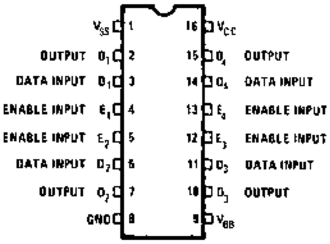
Schottky Bipolar **3207A-1**

QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

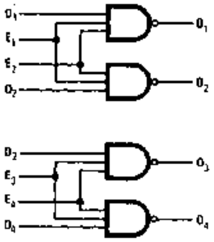
- **Power Supply Voltage Compatible with the High Voltage 1103-1**
- **1103-1 Memory Compatible at Output**

The Intel 3207A-1 is the high voltage version of the standard 3207A, and is compatible with the 1103-1. The 3207A-1 has all the same features as the standard 3207A. The absolute maximum ratings and pin configuration are repeated below for convenience, while the DC and AC characteristics appear below and on the next page.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +55°C
Storage Temperature	−65° C to +160°C
All Input Voltages	−1.0 to +21 Volts
Supply Voltage V_{CC}	−1.0 to +7.0 Volts
All Outputs and Supply Voltages V_{BB} and V_{SS} with respect to GND	−1.0 to +25 Volts
Power Dissipation at 25°C	2 Watts

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT		UNIT	CONDITIONS
		MIN.	MAX.		
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_D = .45V, V_{CC}= 5.25V, All Other Inputs at 5.25V, V_{SS} = 19V, V_{BB}= 23V
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	V_E = .45V, V_{CC}= 5.25V, All Other Inputs at 5.25V, V_{SS}= 19V, V_{BB}= 23V
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	V_D = 19V, V_{CC}= 5.0V, All Other Inputs Grounded, V_{SS} = 19V, V_{BB}= 23V
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	V_E = 19V, V_{CC}= 5.0V, All Other Inputs Grounded, V_{SS} = 19V, V_{BB}= 23V
V_{OL}	OUTPUT "LOW" VOLTAGE		0.8 0.7 0.6	V(0°C) V(25°C) V(55°C)	I_{OL} = 500μA, V_{CC}= 4.75V V_{SS} = 19V, V_{BB} = 23V All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	V_{SS} −0.7 V_{SS} −0.6 V_{SS} −0.5		V(0°C) V(25°C) V(55°C)	I_{OH} = −500μA, V_{CC} = 5.0V V_{SS} = 19V, V_{BB} = 23V All Inputs at 0.85V
V_{OH} (MAX.)			V_{SS} + 1.0	V	I_{OH} = 5mA, V_{CC} = 5.0V V_{SS} = 19V, V_{BB} = 23V
I_{OL}	OUTPUT SINK CURRENT	100		mA	V_O = 4V, V_{CC}= 5.0V, V_{SS} = 19V, V_{BB} = 23V, V_E = V_D = 2.0V
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	V_O = V_{SS} −4V, V_{CC}= 5.0V, V_{SS} = 19V V_{BB}= 23V, V_E = V_D = 0.85V
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	V_{CC}= 5.0V, V_{SS} = 19V, V_{BB}= 23V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC}= 5.0V, V_{SS} = 19V, V_{BB}= 23V
C_{IN}	INPUT CAPACITANCE	8(Typical)		pF	V_{BIAS}= 2.0V, V_{CC}= 0V

D.C. Characteristics (Continued) $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

POWER SUPPLY CURRENT DRAIN:

All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		25	mA	
P_{TOTAL}	Total Power Dissipation		1040	mW	

All Outputs "High"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		5	mA	
P_{TOTAL}	Total Power Dissipation		297	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 20V$, $V_{BB} = 20V$
I_{SS}	Current from V_{SS}		500	μA	
I_{BB}	Current from V_{BB}		500	μA	
P_{TOTAL}	Total Power Dissipation		15	mW	

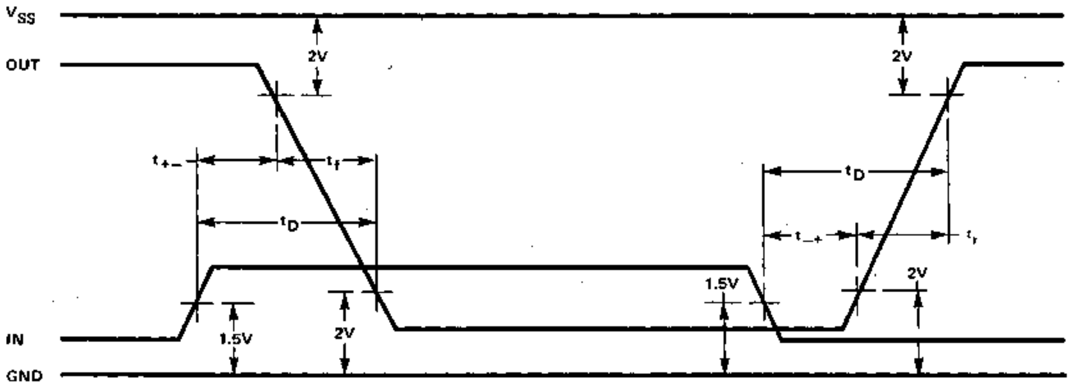
A.C. Characteristics

$T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} = V_{SS} + 3$ to $4V$, f = 2 MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		$C_L = 100$ pF		$C_L = 200$ pF		DELAY DIFFERENTIAL(1) $C_L = 200$ pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	25	10	35	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

Waveforms



intel Schottky Bipolar **3208A, 3408A**

HEX BIPOLAR SENSE AMPLIFIERS FOR MOS CIRCUITS

3208A HEX SENSE AMPLIFIER
3408A HEX SENSE AMPLIFIER WITH LATCHES

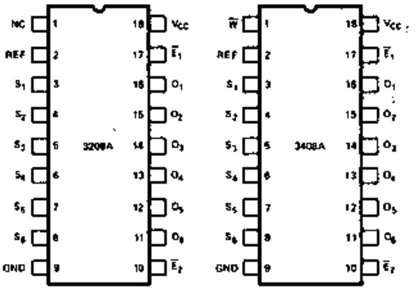
- **High Speed—20 nsec. max.**
- **Wire-OR Capability—**
  - **Open Collector Output ..3208A**
  - **Three-State Output 3408A**
- **Single 5 V Power Supply**
- **Input Level Compatible with 1103 Output**
- **Two Enable Inputs**
- **Minimum Line Reflection .... Low Voltage Diode Input Clamp**
- **Plastic 18 Pin Dual In-Line Package**
- **Schottky TTL**

The Intel 3208A is a high speed hex sense amplifier designed to sense the output signals of the 1103 memory. The device features two separate enable inputs each controlling the output state of three sense amplifiers, and a common voltage reference input. OR-tie capability is available with the 3208A open collector TTL compatible output.

The 3408A is a hex sense amplifier with a latch circuit connected to each amplifier. The sensed data may be stored in the latches through application of a write pulse. The 3408A has three-state TTL outputs, hence in the non-enabled state the outputs float allowing wire-OR memory expansion. The latches may be bypassed by grounding the write input pin. Under this condition, the 3408A functions as a hex sense amplifier.

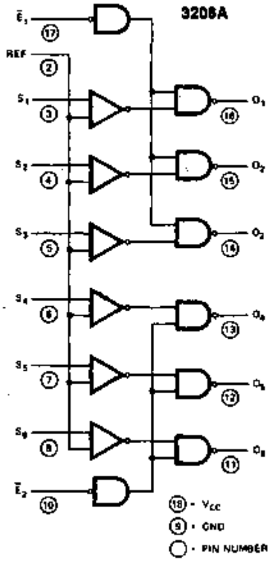
The 3208A and 3408A operate from a single +5 volt power supply. Device performance is specified over the complete ambient temperature range of 0°C to 70°C and over a V_{CC} supply voltage range of 5 volts ±5%. The 3208A and 3408A are packaged in an 18 pin plastic dual in-line package.

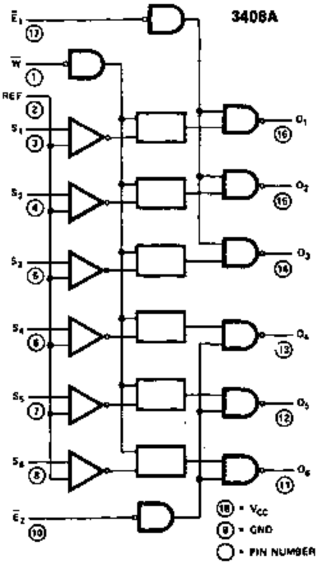
PIN CONFIGURATIONS



3208A 3408A

BLOCK DIAGRAMS





PIN NAMES

$S_1, S_2, S_3, S_4, S_5, S_6$	SENSE AMP INPUTS
$\bar{E}_1, \bar{E}_2$	ENABLE INPUTS
REF	REFERENCE INPUT
$O_1, O_2, O_3, O_4, O_5, O_6$	OUTPUTS (Non-inverting)
$\overline{W}$	WRITE INPUT (3408A only)

Absolute Maximum Ratings*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
All Outputs or Supply Voltage	−0.5 to +7 Volts
All TTL Input Voltages	−1 to +5.5 Volts
All Sense Input Voltages	−1 to +1 Volt
Output Currents Total	300mA
Input Current	125mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at this or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics for 3208A $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE INPUT	2.0			V	$V_{CC} = 5.0V$
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE INPUT			0.85	V	$V_{CC} = 5.0V$
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 10mA$
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	$V_{CC} = 5.25V$ $V_{CEX} = 5.25V$
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	$V_{CC} = 5.25V$ $V_{REF} = 100mV$
I_S	INPUT CURRENT ON SENSE AMP INPUT			−25	μA	$V_{CC} = 5.25V$ $V_S = 100mV$
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} -50	mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	$V_{CC} = 4.75$ to $5.25V$
I_{CC}	POWER SUPPLY CURRENT			120	mA	$V_{CC} = 5.25V$
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	$V_{CC} = 4.75V$ $I_C = -5.0mA$
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	$V_{CC} = 5.0V$ $I_D = 5.0mA$

3208A TRUTH TABLE

INPUTS Sense Amp	Enable	OUTPUT
$<V_{REF} -50mV$	L	L
$>V_{REF}$	L	H
X	H	H

X = Don't care

D. C. Characteristics for 3408A T_A = 0°C to +70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	V_{CC} = 5.25V V_F = 0.45V
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	V_{CC} = 4.75V V_R = 5.25V
I_{FW}	INPUT LOAD CURRENT ON WRITE INPUT			−0.25	mA	V_{CC} = 5.25V V_F = 0.45V
I_{RW}	INPUT LEAKAGE CURRENT ON WRITE INPUT			20	μA	V_{CC} = 4.75V V_R = 5.25V
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE AND WRITE INPUT	2.0			V	V_{CC} = 5.0V
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE AND WRITE INPUT			0.85	V	V_{CC} = 5.0V
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	V_{CC} = 4.75V I_{OL} = 10mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	V_{CC} = 4.75V I_{OH} = −1.5mA
$\|I_O\|$	OUTPUT LEAKAGE CURRENT FOR HIGH IMPEDANCE STATE			100	μA	V_{CC} = 5.25V V_O = 0.45V/5.25V
I_{SC}	OUTPUT SHORT CIRCUIT CURRENT	−40		−100	mA	V_{CC} = 5.0V V_O = 0V
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	V_{CC} = 5.25V V_{REF} = 100mV
I_S	INPUT CURRENT ON SENSE INPUT			−25	μA	V_{CC} = 5.25V V_S = 100mV
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	V_{CC} = 4.75 to 5.25V V_{REF} = 100 to 200mV
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} −60	mV	V_{CC} = 4.75 to 5.25V V_{REF} = 100 to 200mV
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	V_{CC} = 4.75 to 5.25V
I_{CC}	POWER SUPPLY CURRENT			125	mA	V_{CC} = 5.25V
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	V_{CC} = 4.75V I_C = −5.0V
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	V_{CC} = 5.0V I_D = 5.0mA

3408A TRUTH TABLE

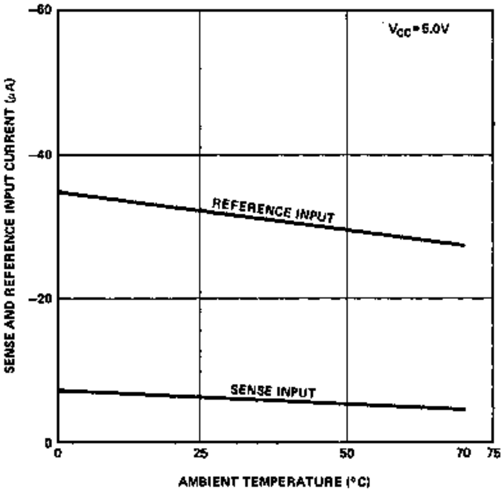
INPUTS Sense Amp	INPUTS Enable	INPUTS Write	OUTPUT
< V_{REF} −60mV	L	L	L
> V_{REF}	L	L	H
X	L	H	Previous Data Stored
X	H	X	High Z*

X = Don't care

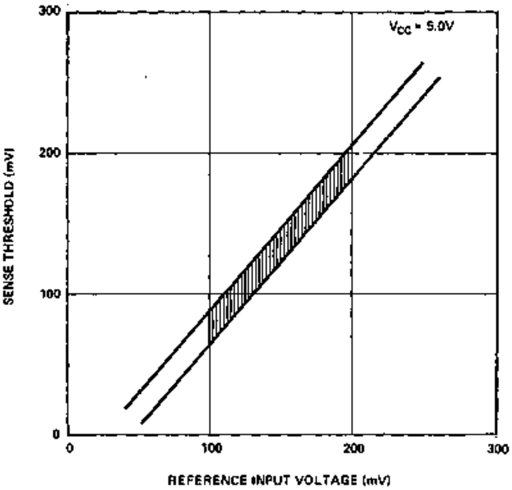
*The output of the 3408A is three-state, hence when not enabled the output is a high impedance.

Typical D. C. Characteristics for 3208A/3408A

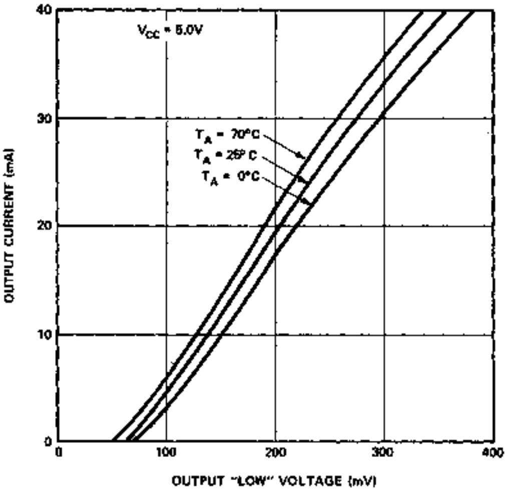
SENSE AND REFERENCE INPUT CURRENT VS. AMBIENT TEMPERATURE



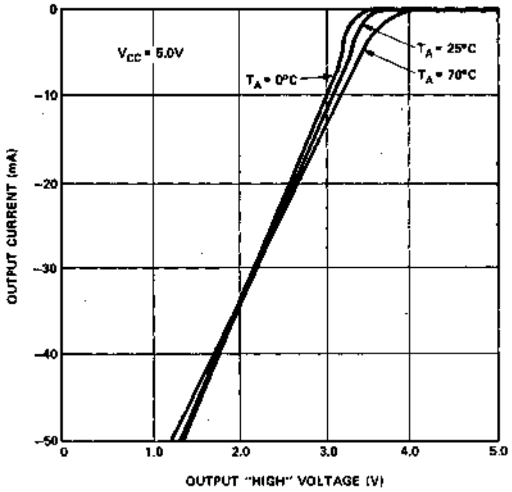
SENSE THRESHOLD VS. REFERENCE INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

3208A

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}				25		

3408A

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{WP}	WRITE PULSE WIDTH	30			ns	D.C. LOAD = 10mA C_L = 30pF
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			25	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "LOW"			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "HIGH"			25	ns	D.C. LOAD = 10mA C_L = 30 pF

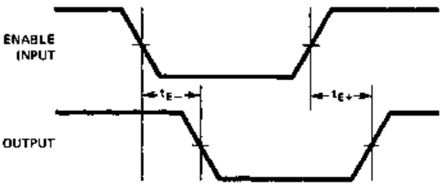
Capacitance[1] $T_A = 25°C$, f = 1 MHz

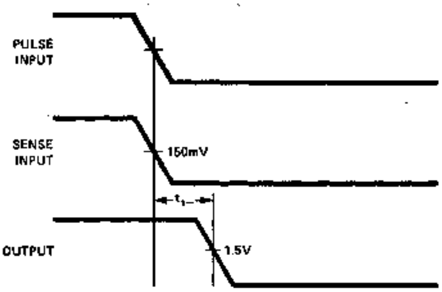
SYMBOL	TEST	LIMITS TYP.	LIMITS MAX.
C_O	$V_{CC} = 0V$, $V_{BIAS} = 2.0V$	8	12
C_{INE}	ENABLE INPUT $V_{CC} = 0V$, $V_{BIAS} = 2.0V$	6	10
C_{INS}	SENSE INPUT $V_{CC} = 0V$, $V_{BIAS} = 0V$	6	10

(1) This parameter is periodically sampled and is not 100% tested.

Waveforms

3208A/3408A

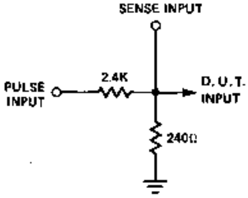




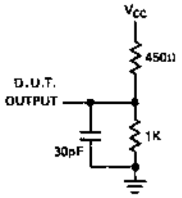
Switching Characteristics

CONDITIONS OF TEST

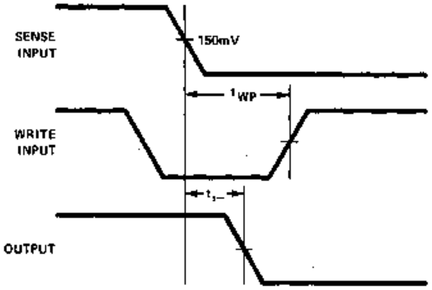
- Input Pulse amplitude: 2.5V for all TTL compatible inputs and 2.5V through a resistor network as shown below for sense input.
- Input Pulse rise and fall times: 5ns.
- Speed measurements are made at 1.5V for all TTL compatible inputs and outputs, and for sense input, see network and waveforms below. V_{REF} is set at 150mV.



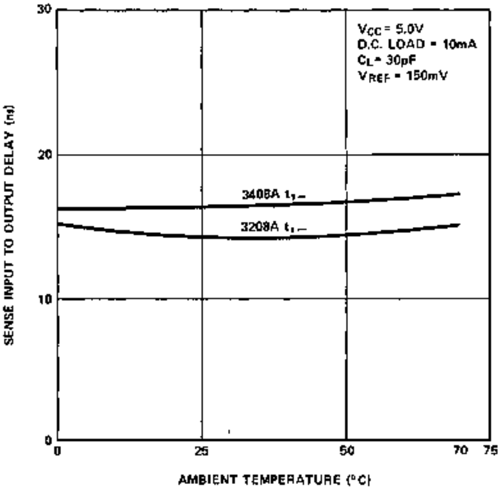
10mA TEST LOAD

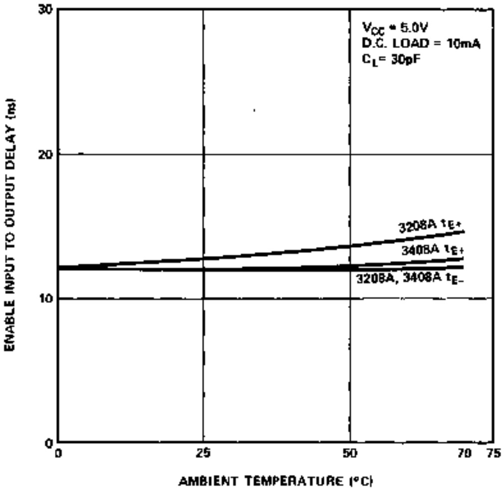


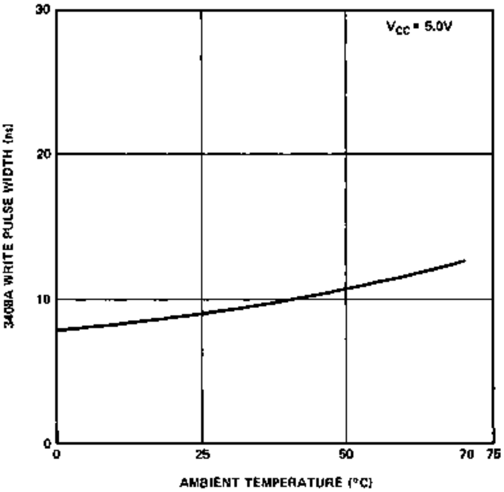
3408A ONLY

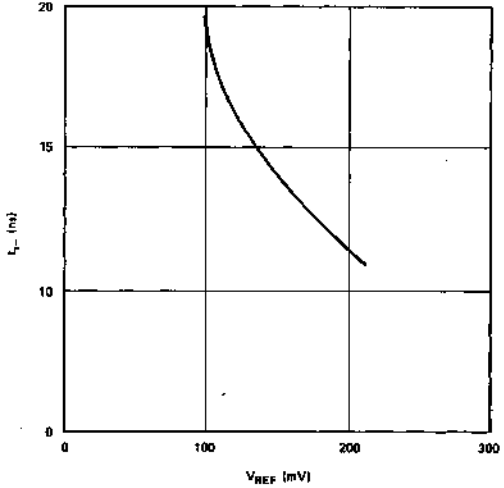


Typical A. C. Characteristics


SENSE INPUT TO OUTPUT DELAY VS. AMBIENT TEMPERATURE


ENABLE INPUT TO OUTPUT DELAY VS. AMBIENT TEMPERATURE


3408A WRITE PULSE WIDTH VS. AMBIENT TEMPERATURE


SENSE INPUT TO OUTPUT DELAY VS. REFERENCE INPUT VOLTAGE

intel® Schottky Bipolar **3210**

TTL-TO-MOS LEVEL SHIFTER AND HIGH VOLTAGE CLOCK DRIVER

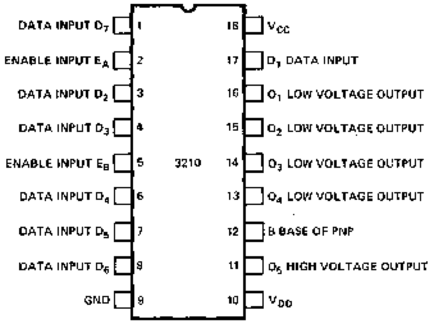
- **Four Low Voltage Drivers**
- **One High Voltage Driver**
- **TTL and DTL Compatible Inputs**
- **Outputs Compatible with 2105 and 2107 MOS Memories**
- **Operates from Standard TTL and MOS Power Supplies**
- **Maximum MOS Device Protection -- Output Clamp Diodes**

The Intel 3210 is a Bipolar-to-MOS level shifter and high voltage driver which accepts TTL and DTL inputs. It contains four (4) low voltage drivers and one high voltage driver, each with current driving capabilities suitable for driving N-channel MOS memory devices. The 3210 is particularly suitable for driving the 2105 and 2107 N-channel MOS memory chips. The 3210 operates from the 5 volt and 12 volt power supplies used to bias the memory devices.

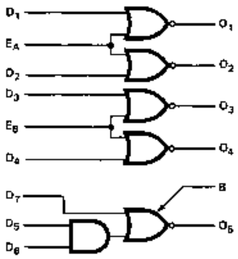
The four low voltage drivers feature two common enable inputs per pair of drivers which permits address or data decoding. The high voltage driver swings the 12 volts required to drive the chip enable (clock) input for the 2105 and 2107. In addition, the high voltage driver includes AND gate logic which can be used to implement refresh abort for the 2105 MOS memory.

The 3210 high voltage driver requires an externally connected PNP transistor. The PNP base is connected to pin 12, the collector to pin 11, and the emitter to pin 10 or V_{DD}. The use of a fast switching, high voltage, high current gain PNP, like the 2N5057 or 2N3546 is recommended.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	0°C to 75°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Supply Voltage, V_{DD}	−0.5 to +13V
All Input Voltages	−1.0 to +13V
Outputs for Low Voltage Drivers	−1.0 to +7V
Outputs for Clock Driver	−1.0 to +13V
Power Dissipation at 25°C	2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics $T_A = 0°C$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Data Input Load Current		−0.25	mA	$V_F = 0.45V$
I_{FE}	Enable Input Load Current		−0.50	mA	$V_F = 0.45V$
I_{RD}	Data Input Leakage Current		10	μA	$V_R = 12.6V$
I_{RE}	Enable Input Leakage Current		20	μA	$V_R = 12.6V$
V_{OL}	Output Low Voltage for all Drivers		0.45	V	$I_{OL} = 3mA$, $V_{IH} = 2V$
		−1.0		V	$I_{OL} = -5mA$
V_{OH1}	Output High Voltage for Low Voltage Drivers	$V_{CC} - 0.65$		V	$I_{OH} = -1mA$, $V_{IL} = 0.8V$
			V_{CC} +1.0	V	$I_{OH} = 5mA$
V_{OH2}	Output High Voltage for High Voltage Driver	V_{DD} −0.75		V	$I_{OH} = -1mA$, $V_{IL} = 0.8V$
			V_{DD}+1.0	V	$I_{OH} = 5mA$
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	
I_B	Base Drive to External PNP (Pin 12)	7	16	mA	$V_{IL} = 0.8V$, $V_B = V_{DD} - 0.8V$

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

All driver outputs are in the state indicated

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions -- Input states to ensure the following output states: All Low Voltage Outputs	Test Conditions -- Input states to ensure the following output states: High Voltage Output	Additional Test Conditions
I_{CC1}	Current from V_{CC}	27	32	mA	Low	Low	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$
I_{DD1}	Current from V_{DD}	12.5	16	mA			
P_{D1}	Power Dissipation	300	370	mW			
I_{CC2}	Current from V_{CC}	22	27	mA	Low	High	
I_{DD2}	Current from V_{DD}	28	34	mA			
P_{D2}	Power Dissipation	470	570	mW			
I_{CC3}	Current from V_{CC}	9	12	mA	High	Low	
I_{DD3}	Current from V_{DD}	9	11.5	mA			
P_{D3}	Power Dissipation	160	210	mW			
I_{CC4}	Current from V_{CC}	4.5	6	mA	High	High	
I_{DD4}	Current from V_{DD}	24	30	mA			
P_{D4}	Power Dissipation	325	410	mW			

A.C. Characteristics $T_A = 0°C$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
t_{LDR}	Delay Plus Rise Time for Low Voltage Drivers		17	25	ns	$C_L = 200pF$
t_{LDF}	Delay Plus Fall Time for Low Voltage Drivers		16	25	ns	$C_L = 200pF$
t_{H-+}	Input to Output Delay for High Voltage Driver	9	15		ns	$C_L = 175pF$
t_{HDR}	Delay Plus Rise Time for High Voltage Driver		27	40	ns	$C_L = 350pF$
t_{H+-}	Input to Output Delay for High Voltage Driver	4	8		ns	$C_L = 175pF$
t_{HDF}	Delay Plus Fall Time for High Voltage Driver		18	30	ns	$C_L = 350pF$
t_{DB}	Delay to Base Drive to External PNP (Pin 12)	4	8	17	ns	

Note 1: Typical values measured at $T_A = 25°C$.

Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.
C_{IN}	Input Capacitance, except D_7	5pF	10pF
C_{IN}	Input Capacitance, D_7	8pF	15pF

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

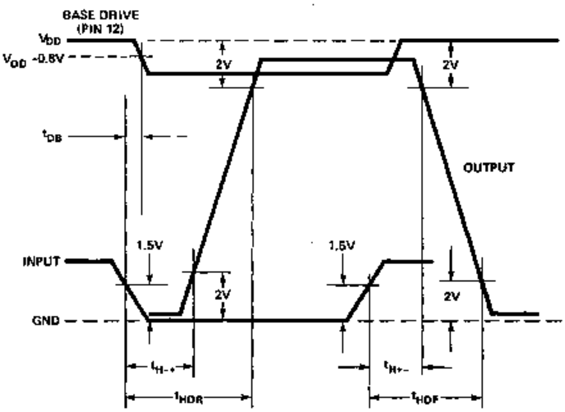
Input Pulse Amplitudes: 3.0V

Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts

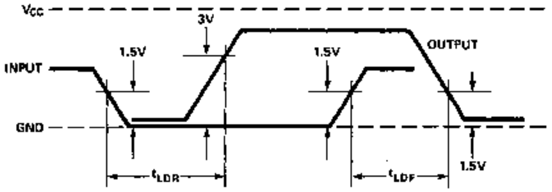
Measurement Points: See Waveforms

Waveforms

HIGH VOLTAGE DRIVER

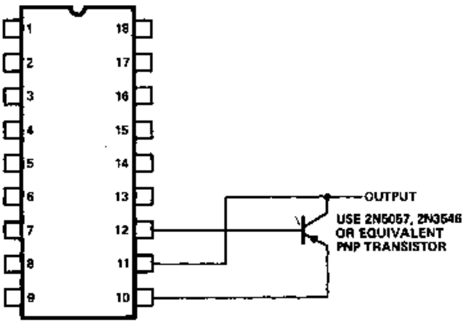


LOW VOLTAGE DRIVER



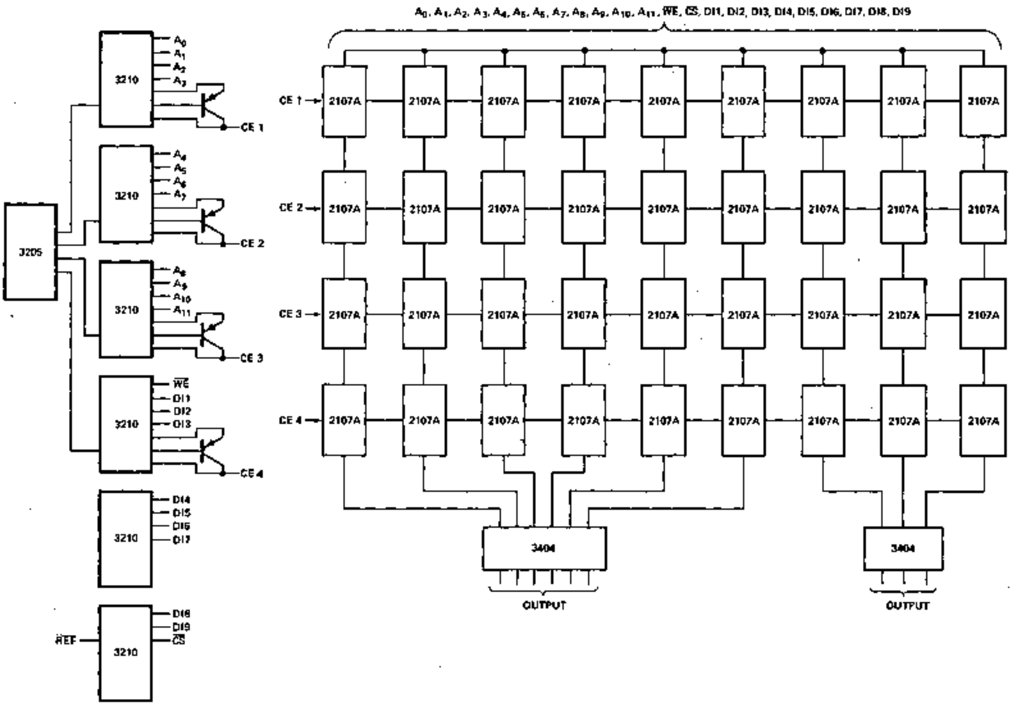
Application

HIGH VOLTAGE OUTPUT CONNECTIONS



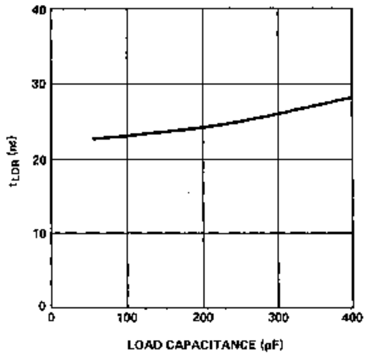
TYPICAL SYSTEMS

Below is an example of a 16K x 9 bit memory circuit employing the 3210 driver. Device decoding is done with the CE input. All devices are unselected during refresh with CS input. The 2107A, 3205 and 3404 are standard Intel products.

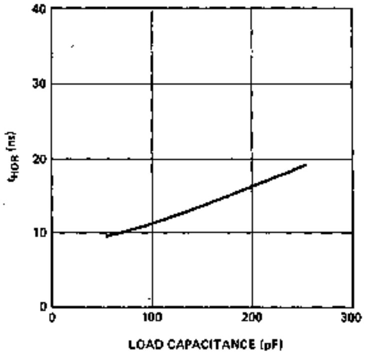


TYPICAL CHARACTERISTICS

t_{HDR} vs. LOAD CAPACITANCE



t_{LDR} vs. LOAD CAPACITANCE



ECL-TO-MOS LEVEL SHIFTER AND HIGH VOLTAGE CLOCK DRIVER

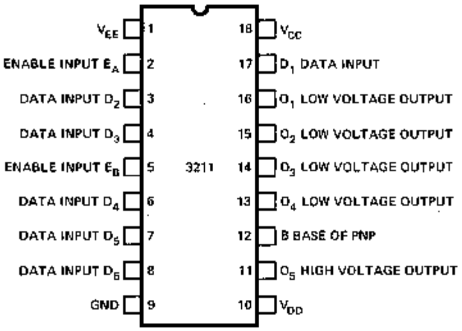
- **Four Low Voltage Drivers**
- **One High Voltage Driver**
- **10K Series ECL Compatible Inputs**
- **Outputs Compatible with 2105 and 2107 MOS Memories**
- **Operates from Standard TTL, ECL, and MOS Power Supplies**
- **Maximum MOS Device Protection-- Output Clamp Diodes**

The Intel 3211 is an ECL to MOS level shifter and N-channel MOS memory driver. Each package contains four (4) low voltage drivers and one high voltage driver. The 3211 is designed to have high performance when driving many RAM devices. It is compatible with the 2105 and 2107 N-channel MOS memory devices. The operating voltages are +5, +12, and -5.2V which are standard TTL, MOS and ECL power supply voltages.

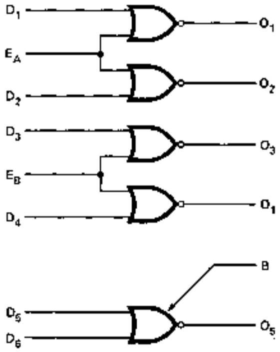
The four low voltage drivers feature two common enable inputs per pair of drivers which permits address or data decoding. The high voltage driver swings the 12 volts required to drive the chip enable (clock) input for the 2105 and 2107. The chip enable driver has two inputs to simplify logic design.

The 3211 high voltage driver requires an externally connected PNP transistor. The PNP base is connected to pin 12, the collector to pin 11, and the emitter to pin 10 or V_{DD}. The use of a fast switching, high voltage, high current gain PNP, like the 2N5057 or 2N3546 is recommended.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	0°C to 75°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Supply Voltage, V_{DD}	−0.5 to +13V
Supply Voltage, V_{EE}	+0.5 to −7V
All Input Voltages	0V to V_{EE}
Outputs for Low Voltage Drivers	−1.0 to +7V
Outputs for Clock Driver	−1.0 to +13V
Power Dissipation at 25°C	2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%, V_{EE} = -5.2V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Data Input Load Current		0.5	mA	$V_F = -0.8V$
I_{FE}	Enable Input Load Current		1.0	mA	$V_F = -0.8V$
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3mA, $V_{IH} = -1.025V$
	for all Drivers	−1.0		V	$I_{OL} = -5mA$
V_{OH1}	Output High Voltage	V_{CC} −0.65		V	$I_{OH} = -1mA$, $V_{IL} = -1.500V$
	for Low Voltage Drivers		V_{CC} +1.0	V	I_{OH} = 5mA
V_{OH2}	Output High Voltage	V_{DD} −0.75		V	$I_{OH} = -1mA$, $V_{IL} = -1.500V$
	for High Voltage Driver		V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs	−1.500V		V	
V_{IH}	Input High Voltage, All Inputs		−1.025V	V	
I_B	Base Drive to External PNP (Pin 12)	7	16	mA	$V_{IL} = -1.5V$ $V_B = V_{DD} - 0.8V$

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

All driver outputs are in the state indicated

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions -- Input states to ensure the following output states:		Additional Test Conditions
					All Low Voltage Outputs	High Voltage Output	
I_{CC1}	Current from V_{CC}	24.5	31	mA	Low	Low	V_{CC} = 5.25V, V_{DD} = 12.6V, $V_{EE} = -5.46V$
I_{EE1}	Current from V_{EE}	−24	−30	mA			
I_{DD1}	Current from V_{DD}	12.5	16.5	mA			
P_{D1}	Power Dissipation	415	535	mW			
I_{CC2}	Current from V_{CC}	20	26	mA	Low	High	
I_{EE2}	Current from V_{EE}	−21.5	−27	mA			
I_{DD2}	Current from V_{DD}	27	33.5	mA			
P_{D2}	Power Dissipation	560	705	mW			
I_{CC3}	Current from V_{CC}	11	16	mA	High	Low	
I_{EE3}	Current from V_{EE}	−19	−23.5	mA			
I_{DD3}	Current from V_{DD}	9	12	mA			
P_{D3}	Power Dissipation	275	365	mW			
I_{CC4}	Current from V_{CC}	6	10	mA	High	High	
I_{EE4}	Current from V_{EE}	−16	−20	mA			
I_{DD4}	Current from V_{DD}	23.5	27	mA			
P_{D4}	Power Dissipation	415	500	mW			

A.C. Characteristics T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%, V_{EE} = −5.2V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
t_{LDR}	Delay Plus Rise Time for Low Voltage Drivers		21	27	ns	C_L = 200pF
t_{LDF}	Delay Plus Fall Time for Low Voltage Drivers		22	32	ns	C_L = 200pF
t_{H-+}	Input to Output Delay for High Voltage Driver	14	20		ns	C_L = 175pF
t_{HDR}	Delay Plus Rise Time for High Voltage Driver		36	45	ns	C_L = 350pF
t_{H+-}	Input to Output Delay for High Voltage Driver	7	12		ns	C_L = 175pF
t_{HDF}	Delay Plus Fall Time for High Voltage Driver		27	40	ns	C_L = 350pF
t_{DB}	Delay to Base Drive to External PNP (Pin 12)	7	14	23	ns	

Note 1: Typical values measured at T_A = 25°C.

Capacitance* T_A = 25°C

Symbol	Test	Typ.	Max.
C_{IN}	Input Capacitance	4pF	8pF

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, V_{EE} = 0V, and T_A = 25°C.

A.C. CONDITIONS OF TEST

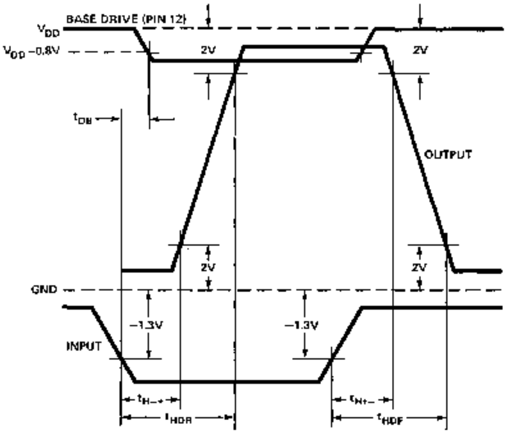
Input Pulse Amplitudes: −0.9V to −1.7V

Input Pulse Rise and Fall Times: 5ns (Between 10% and 90% points)

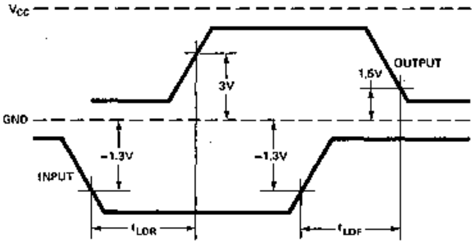
Measurement Points: See Waveforms

Waveforms

HIGH VOLTAGE DRIVER

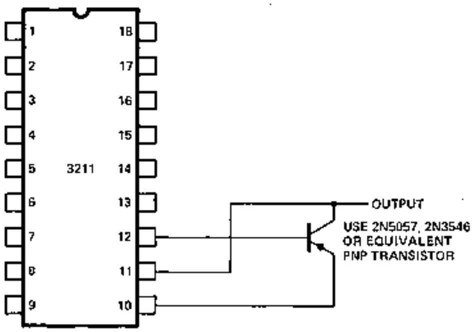


LOW VOLTAGE DRIVER



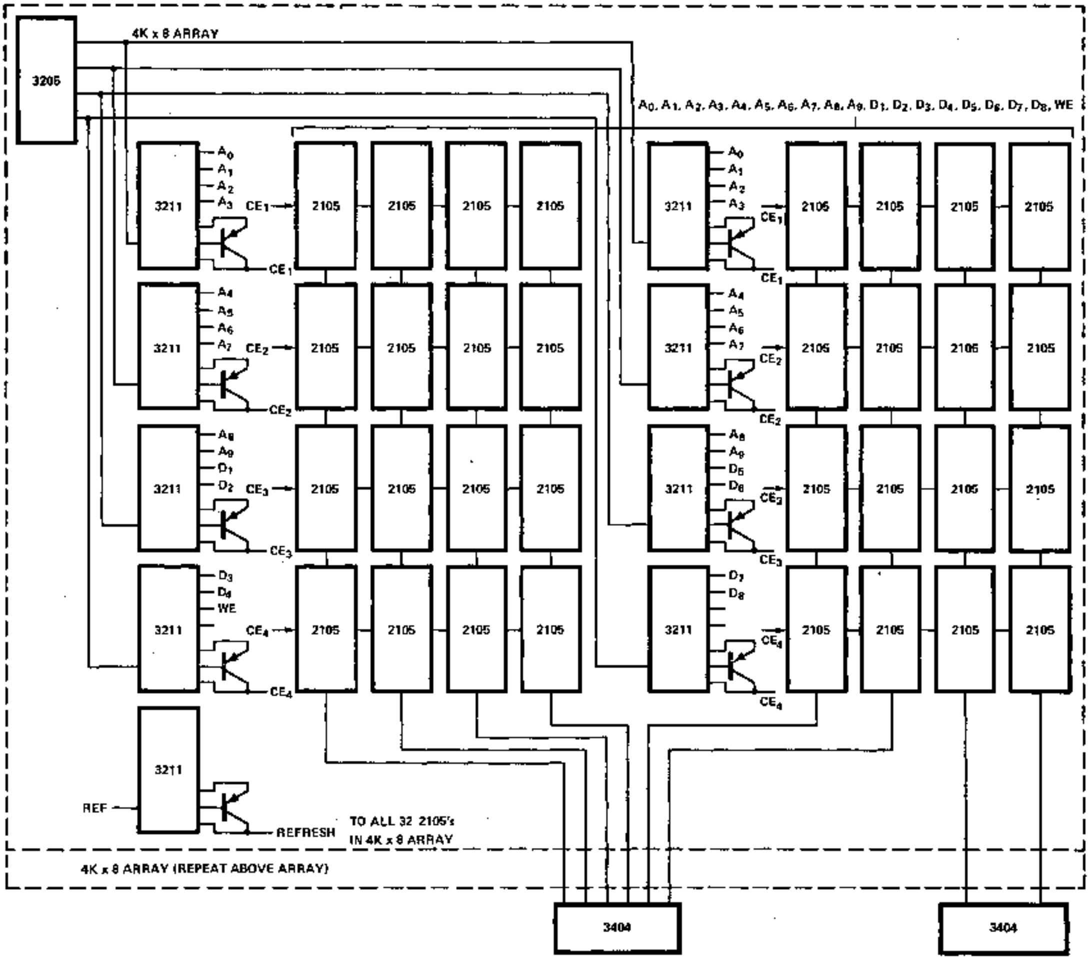
Application

HIGH VOLTAGE OUTPUT CONNECTIONS

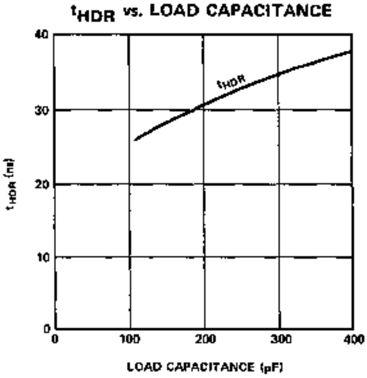


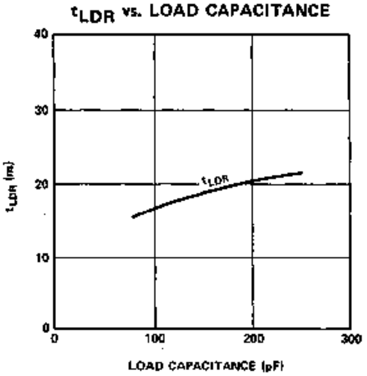
TYPICAL SYSTEM

Below is an example of an 8K x 8 bit memory circuit employing the 3211 driver. Device decoding is done with the CE input. The 2105, 3205 and 3404 are standard Intel products.



TYPICAL CHARACTERISTICS





QUAD BIPOLAR-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

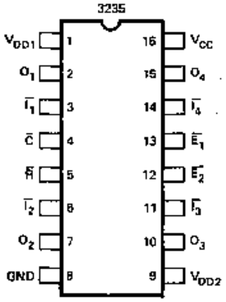
- **High Speed, 32 nsec Max.— Delay + Transition Time Over Temperature with 250 pF load**
- **High Density -- Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count and Eliminates Gating Delays**
- **TTL & DTL Compatible Inputs**
- **Minimum Line Reflection--Input and Output Clamp Diodes**
- **Safety Feature Protects 4 K RAMs if +5 V System Supply is Lost**
- **CerDIP Package--16 Pin DIP**

The Intel 3235 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107 or 2105. The circuit operates from three power supplies which are 5, 12, and 15 volts.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs.

A safety feature forces all outputs low if the V_{CC} power supply is lost. This protects 4K RAM's by putting them in the standby mode.

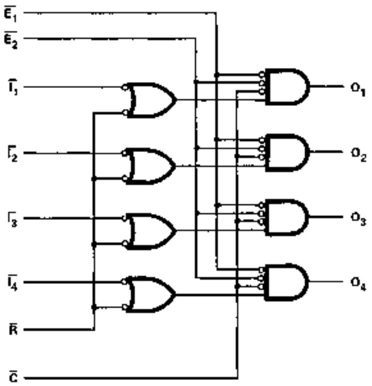
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}-\overline{I_4}$	DATA INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E_1}, \overline{E_2}$	ENABLE INPUTS	V_{CC}	+6V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD1}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	V_{DD2}	+15V POWER SUPPLY

LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 75°C
Storage Temperature . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . -0.5 to +7V
Supply Voltage, V_{DD1} . . . . -0.5 to +13V
Supply Voltage, V_{DD2} . . . . -0.5 to +16V
All Input Voltages . . . . -1.0 to V_{DD1}
Outputs for Clock Driver . . . . -1.0 to V_{DD1}+1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A=0°C to 75°C, V_{CC}=5.0V ±5%, V_{DD1} = 12V ±5%, V_{DD2} = V_{DD1} +(3V ±5%)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\bar{I}_1, \bar{I}_2, \bar{I}_3, \bar{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\bar{R}, \bar{C}, \bar{E}_1, \bar{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	µA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	µA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
V_{OH}	Output High Voltage	V_{DD1}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	21	32.0	mA	High	V_{CC} = 5.25V V_{DD1} = 12.6V V_{DD2} = 15.75V
I_{DD1}	Current from V_{DD1}	.2	2.0	mA		
I_{DD2}	Current from V_{DD2}	12.5	18.0	mA		
P_{D1}	Power Dissipation	310	477	mW		
	Power Per Driver	77	119	mW		
I_{CC}	Current from V_{CC}	36	46.0	mA	Low	
I_{DD1}	Current from V_{DD1}	2.1	3.0	mA		
I_{DD2}	Current from V_{DD2}	20	26.0	mA		
P_{D2}	Power Dissipation	530	689	mW		
	Power Per Driver	132	172	mW		

A.C. Characteristics T_A = 0° to 75°C, V_{CC} = 5.0V ± 5%, V_{DD1} = 12V ±5%, V_{DD2} = V_{DD1} +(3V ±5%)

Symbol	Parameter	Min.[1]	Typ.[2]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	
t_{DR}	Delay Plus Rise Time		20	32	ns	
t_{+-}	Input to Output Delay	3	8		ns	
t_{DF}	Delay Plus Fall Time		19	32	ns	

NOTES:
1. C_L = 150pF (minimum C_L for 9 4K RAMs).
2. C_L = 200pF (typical C_L for 9 4K RAMs). Typical values measured at T_A = 25°C.
3. C_L = 250pF (maximum C_L for 9 4K RAMs).

Capacitance* T_A = 25°C

Symbol	Test	Typ.	Max.
C_{IN}	Input Capacitance, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$	4.5pF	7
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$	8pF	12

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

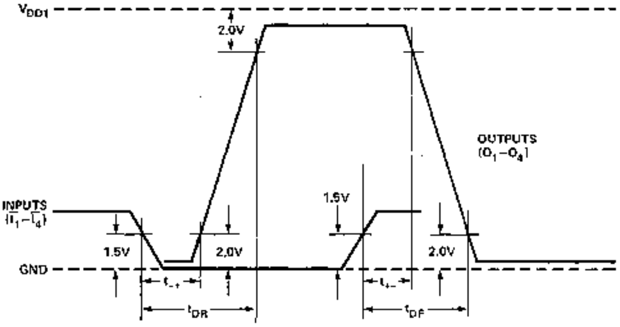
A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 3.0V

Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts

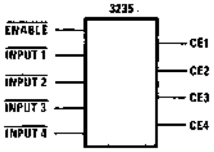
Measurement Points: See Waveforms

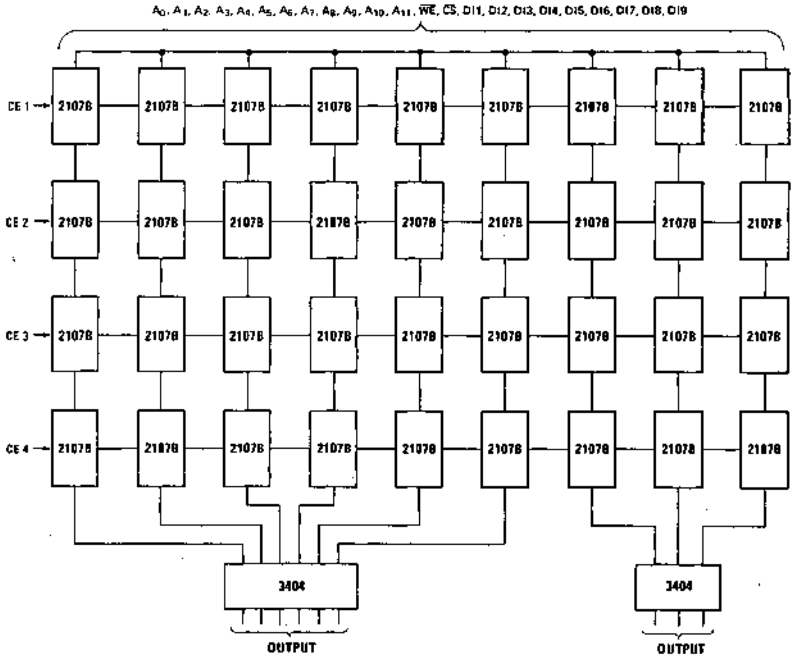
Waveforms



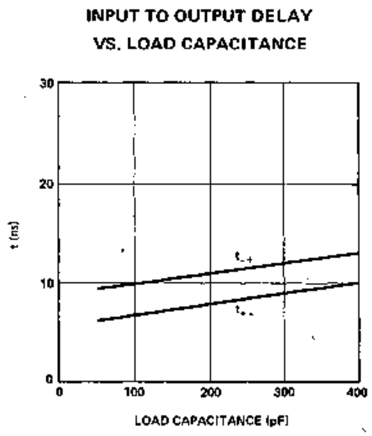
Typical System

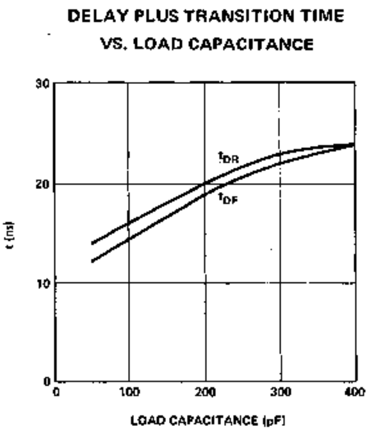
Below is an example of a 16K x 9 bit memory circuit employing the 3235 quad high voltage driver for the chip enable inputs. A single 3235 package will drive this 16K x 9 bit memory array.





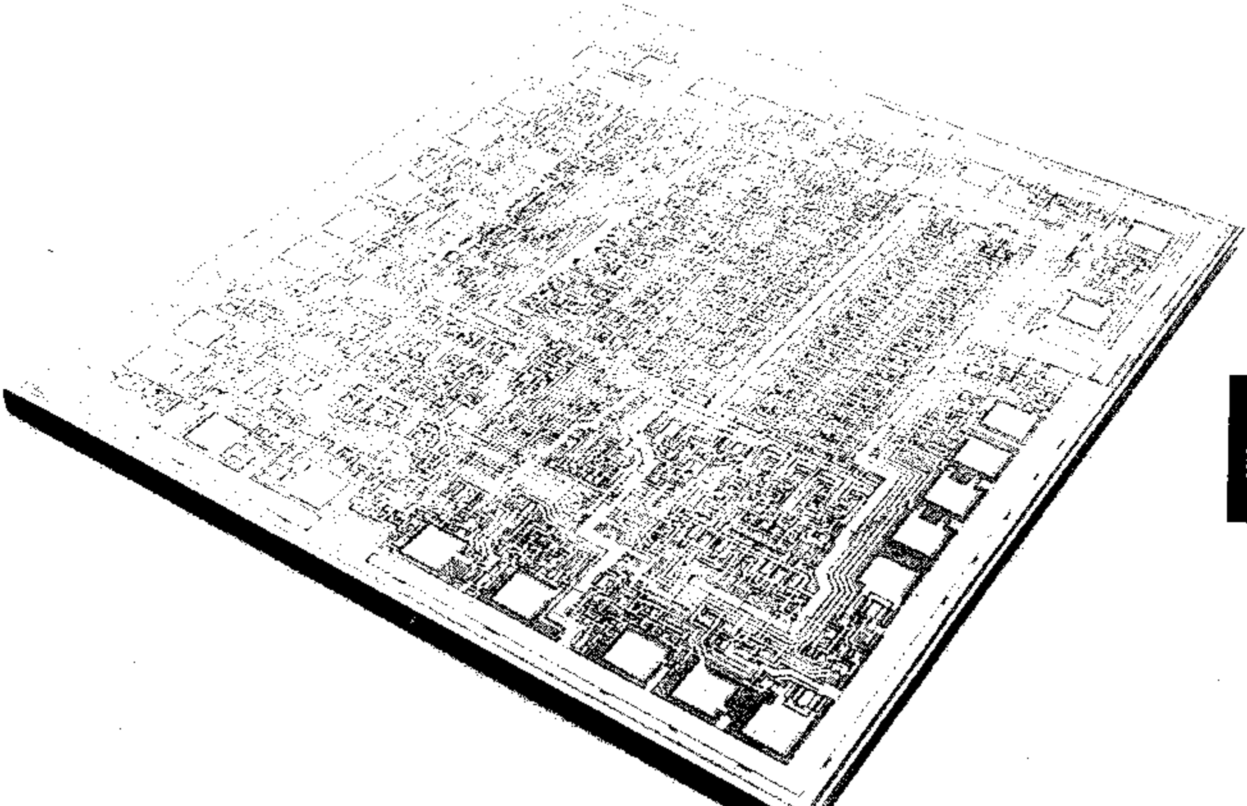
Typical Characteristics





MICROCOMPUTERS

6



INTEL® MICROCOMPUTER SYSTEMS

FIRST FROM THE BEGINNING IN MICROCOMPUTERS . . . .

Intel provides a broad range of CPUs, ROMs, PROMs, RAMs, I/O devices, and peripheral circuits which enable you to quickly put microcomputer systems to work for you.

Intel provides Intellec® program development systems complete with resident software, as well as cross product software for use on large scale computers. All cross product software is available world wide on time sharing computer services.

Intel also provides training courses and seminars, plus a complete line of documentation on all products. Field application engineers are also available to provide accurate, prompt technical information.

Put it all together and you have the broadest microcomputer systems capability and product support available anywhere.

Intel . . . . . . FIRST . . . . . . and FOREMOST . . . . . .

Page

WHY USE A MICROCOMPUTER?

INTRODUCTION

Since their inception, digital computers have continuously become more efficient, expanding into new applications with each major technological improvement. The advent of minicomputers enabled the inclusion of digital computers as a permanent part of various process control systems. Unfortunately, the size and cost of minicomputers in "dedicated" applications has limited their use. Another approach has been the use of custom built systems made up of "random logic" (i.e., logic gates, flip-flops, counters, etc.). However, the huge expense and development time involved in the design and debugging of these systems has restricted their use to large volume applications where the development costs could be spread over a large number of machines.

Today, Intel offers the systems designer a new alternative . . . . the microcomputer. Utilizing the technologies and experience gained in becoming the world's largest supplier of LSI memory components, Intel has made the power of the digital computer available at the integrated circuit level.

ECONOMICS OF USING MICROCOMPUTERS

Engineers are becoming more aware of the ways in which microcomputers can be applied to solve their problems. There are five basic reasons why many engineers have begun to use microcomputers. These are:

1. Manufacturing costs of products can be significantly reduced.
2. Products can get to the market faster providing a company with the opportunity to increase product sales and market share.
3. Product capability is enhanced allowing manufacturers to provide customers with better products which can frequently command a higher price in the market place.
4. Development costs and time are reduced.
5. Product reliability is increased which leads to a corresponding reduction in both service and warranty costs.

Microcomputers simplify almost every phase of product development. The first step, as in any product design program, is to identify the various functions that the end system is expected to perform. These functions are then implemented by encoding suitable sequences of instructions (programs) in the memory elements. Data and certain types of programs will be stored in RAM circuits, while the basic program will be stored in ROM circuits. The microprocessor performs all of the system's functions by fetching the instructions in memory, executing them and communicating the results via the microcomputer's I/O ports. A single-chip microprocessor, executing the programmed logic stored in a single ROM element, can perform the same logical functions that have previously required many logic gates.

REDUCING MANUFACTURING COSTS

If the burdened manufacturing cost of a digital electronic system is divided by the number of ICs, one generally finds that the system costs between $2 and $6 per IC to fabricate. The higher costs are generally associated with systems manufactured in volumes from 10 to 100 units annually. The table below presents a more detailed analysis of the source of these surprisingly high costs. The costs, themselves, are stated conservatively.

IC	.50
Incoming Inspection	.05
PC Card	.50
Fabrication	.05
Board Test and Rework	.10
Connector	.05
Discretes	.05
Wiring	.10
Power	.10
Cabinetry, Fans, Etc.	.10
	$1.60

Table I. System Manufacturing Costs Per IC

The ASP (average sale price) of an Integrated Circuit today is approximately 50¢. Incoming inspection and testing of these ICs costs the average company 5¢. However, many companies are now buying aged and tested circuits for their applications in order to increase system reliability. This adds about 15¢ to unit costs. Simple PC cards may cost as little as 25¢ an IC position, but the average cost in most applications for high quality cards is closer to 50¢. Sophisticated multilayer cards used in many high performance systems frequently cost *over a dollar a position*. When customers put ICs in sockets and then wire wrap cards, the cost per IC position quickly approaches $2. Customers with automatic IC insertion equipment and efficient flow soldering machines can fabricate a PC card for as low as 3¢ an IC position, though the average price is closer to 5¢. Board test and rework add another dime to system cost, while the cost of a connector divided by the number of ICs per printed circuit card frequently exceeds 5¢. In general, resistors, capacitors, power bus bars, etc., add a cost of 5¢ an IC position. Systems frequently average one wire or more per IC position and the wires put in with automatic equipment frequently cost over 10¢. Finally, the cost of power supplies and mechanical packaging add another 20¢ an IC position.

To determine the total savings in system manufacturing cost, the user must subtract the cost of implementing an equivalent system with a microcomputer. In moderate volumes, an MCS-40™ with 16,384 bits of ROM, a processor, and a minimal amount of RAM can be purchased for under $50. This system has the potential of displacing between $150 and $600 of system manufacturing cost.

How Memory Replaces Random Logic

It can be said that 8 to 16 bits of memory are the logical equivalent of a single gate. Assuming that the type IC used today contains on the order of 10 gates, then one can conclude that logic can be stored in memory in a very cost effective fashion. The following table indicates the number of IC's which are replaced by a single ROM (Read Only Memory). The table was derived by using the assumptions that 8 to 16 bits of ROM replace a gate and that on the average an IC contains 10 gates.

ROM Memory Size Bits	Gates Replaced	IC's Replaced
2048	128-256	13-25
4096	256-512	25-50
8192	512-1024	50-100
16384	1024-2048	100-200

Table II. Number of IC's Replaced with a ROM (Read Only Memory)

Reducing Development Time and Cost

Microcomputer systems simplify almost every phase of product development. Because of the extensive design aids and software support supplied by Intel it is relatively easy to develop application programs that tailor the device to the system. Development cycles can be cut by as long as six to twelve months. The table below tabulates a number of the steps in a development cycle and indicates how microcomputer systems can affect them. Surprisingly, product definition is frequently speeded up once the decision has been made to use a microcomputer. This is because the incremental cost for adding features to the system is usually small and can be easily estimated. For example, added features such as automatic tax computation for an electronic cash register may only require the addition of a single ROM. The addition of one LSI chip has a minimal effect on total system cost, power and packaging requirements. On the other hand, the same function implemented with IC logic might require two or three fairly large PC cards filled with MSI and SSI.

System and logic design time is also reduced. Programming is a faster way to design than using logic diagrams. PC card layout time is reduced simply because there are fewer cards to lay out. This reduction in hardware also reduces the load on the technical writers who must develop maintenance manuals. Parts lists become shorter, easing the task of transferring the product to manufacturing. Cooling, packaging, and power distribution problems frequently become trivial. Finally, engineering changes that are difficult to make and frequently tedious to document, become simple program changes. These can be made by changing the pattern in a ROM or PROM (Programmable Read Only Memory) such as Intel's 4702A.

Enhanced Product Capability

Product features can be easily added to microcomputer systems by simply adding more program storage. Examples of such easily added features are: putting automatic tax computations into a cash register by adding more ROM, adding automatic calibration features to instruments, and making traffic controllers that automatically sense traffic load and adjust the duration of the signals, etc.

Reduced Complexity

Because microcomputer systems eliminate many ICs and consequently the failures associated with these devices, it can significantly increase system reliability. Most of the failures in a digital system occur because an interconnect has failed. The use of a typical 16 pin IC will introduce approximately 36 interconnectors in a system. There are 16 interconnections from the chip to the lead frame, 16 from the lead frame to the PC card, and approximately 2 interconnections from the PC card to the back plane, and 2 interconnections from back plane point to back plane point per IC. If one ROM eliminates fifty ICs, then it eliminates approximately 1800 interconnections.

Development Steps	Conventional System	Programmed Logic
Product definition		Simplified because of ease of incorporating features
System and logic design	Done with logic diagrams	Can be programmed with design aids (compilers, assemblers, editors)
Debug	Done with conventional lab instrumentation	Software and hardware aids reduce time
PC card layout		Fewer cards to layout
Documentation		Less hardware to document
Cooling and packaging		Reduced system size and power consumption eases job
Power distribution		Less power to distribute
Engineering changes	Done with yellow wire	Change program in PROM

Table III. How Development Time and Cost are Reduced with Microcomputers

intel® Silicon Gate MOS 4004

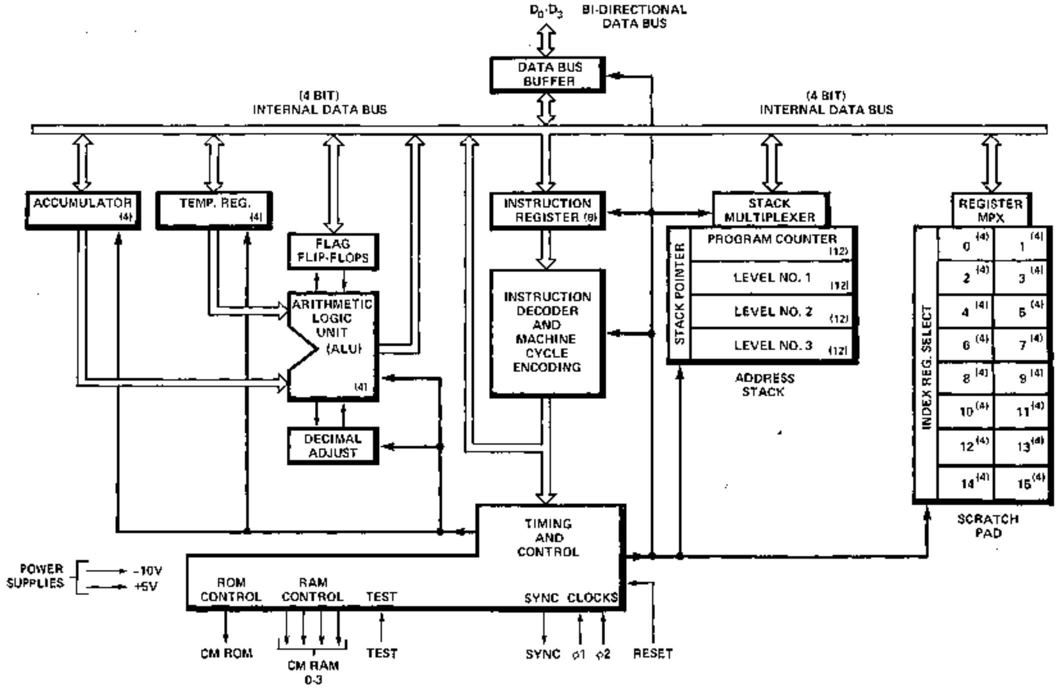
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **10.8 Microsecond Instruction Cycle**
- **CPU Directly Compatible With MCS-4 ROMs and RAMs**
- **Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM**
- **4-Bit Parallel CPU With 46 Instructions**
- **Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching**
- **Binary and Decimal Arithmetic Modes**

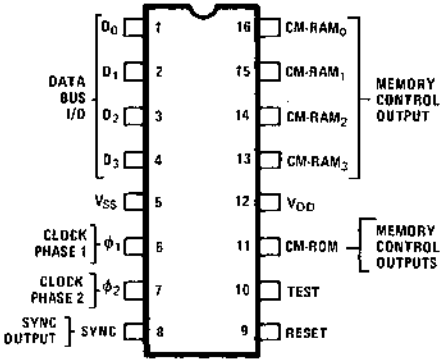
The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used in test systems, terminals, billing machines, process control and random logic replacement applications. The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



4004 FUNCTIONAL PIN DESCRIPTION



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

RESET

RESET input. A logic "1" level at this input clears all flags and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 64 clock cycles (8 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and set to the ROM and RAM chips. It indicates the beginning of an instruction cycle.

CM-ROM

CM-ROM output. This is the ROM selection signal sent out by the processor when data is required from program memory.

CM-RAM$_0$ – CM-RAM$_3$

CM-RAM outputs. These are the bank selection signals for the 4002 RAM chips in the system.

ϕ_1, ϕ_2

Two phase clock inputs.

V_{SS}

Ground reference — most positive voltage.

V_{DD}

-15 ±5% main supply voltage.

INSTRUCTION SET FORMAT

A. Machine Instructions

- 1 word instruction — 8-bits requiring 8 clock periods (instruction cycle).
- 2 word instruction — 16-bits requiring 16 clock periods (2 instruction cycles).

Each instruction is divided into two four-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

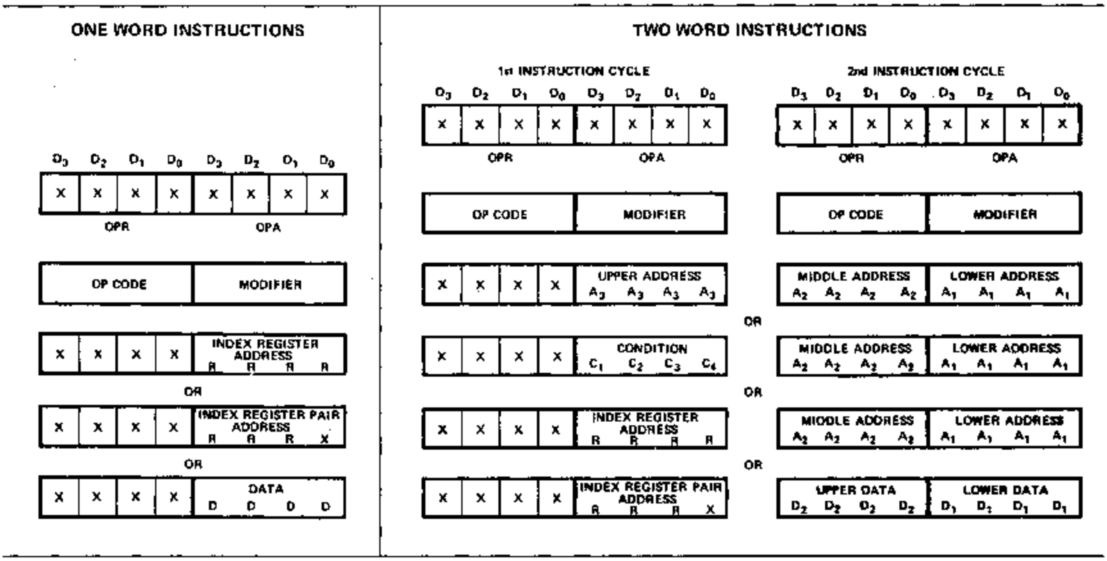


Table I. Machine Instruction Format

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

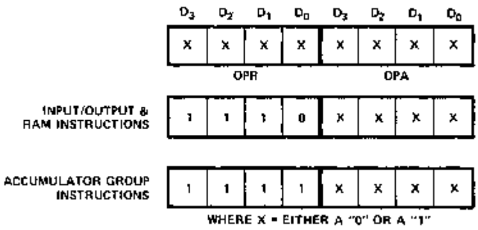


Table II. I/O and Accumulator Group Instruction Formats

MCS-4™ INSTRUCTION SET

(Those instructions preceded by an asterisk (*) are 2 word instructions that occupy 2 successive locations in ROM)

MACHINE INSTRUCTIONS (Logic 1 = Low Voltage = Negative Voltage; Logic 0 = High Voltage = Ground)

MNEMONIC	DESCRIPTION OF OPERATION	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$
NOP	No operation.	0 0 0 0	0 0 0 0
*JCN	Jump to ROM address $A_2\ A_2\ A_2\ A_2,\ A_1\ A_1\ A_1\ A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1\ C_2\ C_3\ C_4$[1] is true, otherwise skip (go to the next instruction in sequence).	0 0 0 1 $A_2\ A_2\ A_2\ A_2$	$C_1\ C_2\ C_3\ C_4$ $A_1\ A_1\ A_1\ A_1$
*FIM	Fetch immediate (direct) from ROM Data D_2, D_1 to index register pair location RRR.[2]	0 0 1 0 $D_2\ D_2\ D_2\ D_2$	R R R 0 $D_1\ D_1\ D_1\ D_1$
SRC	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the Instruction Cycle.	0 0 1 0	R R R 1
FIN	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.	0 0 1 1	R R R 0
JIN	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the Instruction Cycle.	0 0 1 1	R R R 1
*JUN	Jump unconditional to ROM address A_3, A_2, A_1	0 1 0 0 $A_2\ A_2\ A_2\ A_2$	$A_3\ A_3\ A_3\ A_3$ $A_1\ A_1\ A_1\ A_1$
*JMS	Jump to subroutine ROM address A_3, A_2, A_1, save old address. (Up 1 level in stack.)	0 1 0 1 $A_2\ A_2\ A_2\ A_2$	$A_3\ A_3\ A_3\ A_3$ $A_1\ A_1\ A_1\ A_1$
INC	Increment contents of register RRRR.[3]	0 1 1 0	R R R R
*ISZ	Increment contents of register RRRR. Go to ROM address A_2, A_1 (within the same ROM that contains this ISZ instruction) if result ≠ 0, otherwise skip (go to the next instruction in sequence).	0 1 1 1 $A_2\ A_2\ A_2\ A_2$	R R R R $A_1\ A_1\ A_1\ A_1$
ADD	Add contents of register RRRR to accumulator with carry.	1 0 0 0	R R R R
SUB	Subtract contents of register RRRR to accumulator with borrow.	1 0 0 1	R R R R
LD	Load contents of register RRRR to accumulator.	1 0 1 0	R R R R
XCH	Exchange contents of index register RRRR and accumulator.	1 0 1 1	R R R R
BBL	Branch back (down 1 level in stack) and load data DDDD to accumulator.	1 1 0 0	D D D D
LDM	Load data DDDD to accumulator.	1 1 0 1	D D D D

INPUT/OUTPUT AND RAM INSTRUCTIONS

(The RAM's and ROM's operated on in the I/O and RAM instructions have been previously selected by the last SRC instruction executed.)

MNEMONIC	DESCRIPTION OF OPERATION	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$
WRM	Write the contents of the accumulator into the previously selected RAM main memory character.	1 1 1 0	0 0 0 0
WMP	Write the contents of the accumulator into the previously selected RAM output port.	1 1 1 0	0 0 0 1
WRR	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)	1 1 1 0	0 0 1 0
WPM	Write the contents of the accumulator into the previously selected half byte of read/write program memory (for use with 4008/4009 only)	1 1 1 0	0 0 1 1
WRϕ[4]	Write the contents of the accumulator into the previously selected RAM status character 0	1 1 1 0	0 1 0 0
WR1[4]	Write the contents of the accumulator into the previously selected RAM status character 1	1 1 1 0	0 1 0 1
WR2[4]	Write the contents of the accumulator into the previously selected RAM status character 2	1 1 1 0	0 1 1 0
WR3[4]	Write the contents of the accumulator into the previously selected RAM status character 3	1 1 1 0	0 1 1 1
SBM	Subtract the previously selected RAM main memory character from accumulator with borrow	1 1 1 0	1 0 0 0
RDM	Read the previously selected RAM main memory character into the accumulator.	1 1 1 0	1 0 0 1
RDR	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)	1 1 1 0	1 0 1 0
ADM	Add the previously selected RAM main memory character to accumulator with carry	1 1 1 0	1 0 1 1
RDϕ[4]	Read the previously selected RAM status character 0 into accumulator	1 1 1 0	1 1 0 0
RD1[4]	Read the previously selected RAM status character 1 into accumulator.	1 1 1 0	1 1 0 1
RD2[4]	Read the previously selected RAM status character 2 into accumulator	1 1 1 0	1 1 1 0
RD3[4]	Read the previously selected RAM status character 3 into accumulator.	1 1 1 0	1 1 1 1

ACCUMULATOR GROUP INSTRUCTIONS

CLB	Clear both. (Accumulator and carry)	1 1 1 1	0 0 0 0
CLC	Clear carry.	1 1 1 1	0 0 0 1
IAC	Increment accumulator.	1 1 1 1	0 0 1 0
CMC	Complement carry.	1 1 1 1	0 0 1 1
CMA	Complement accumulator.	1 1 1 1	0 1 0 0
RAL	Rotate left. (Accumulator and carry)	1 1 1 1	0 1 0 1
RAR	Rotate right. (Accumulator and carry)	1 1 1 1	0 1 1 0
TCC	Transmit carry to accumulator and clear carry.	1 1 1 1	0 1 1 1
DAC	Decrement accumulator.	1 1 1 1	1 0 0 0
TCS	Transfer carry subtract and clear carry.	1 1 1 1	1 0 0 1
STC	Set carry.	1 1 1 1	1 0 1 0
DAA	Decimal adjust accumulator.	1 1 1 1	1 0 1 1
KBP	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.	1 1 1 1	1 1 0 0
DCL	Designate command line	1 1 1 1	1 1 0 1

NOTES [1] The condition code is assigned as follows:

$C_1 = 1$	Invert jump condition	$C_2 = 1$	Jump if accumulator is zero	$C_4 = 1$	Jump if test signal is a 0
$C_1 = 0$	Not invert jump condition	$C_3 = 1$	Jump if carry/link is a 1		

[2] RRR is the address of 1 of 8 index register pairs in the CPU.

[3] RRRR is the address of 1 of 16 index registers in the CPU.

[4] Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

intel®

Silicon Gate MOS **4040**

SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

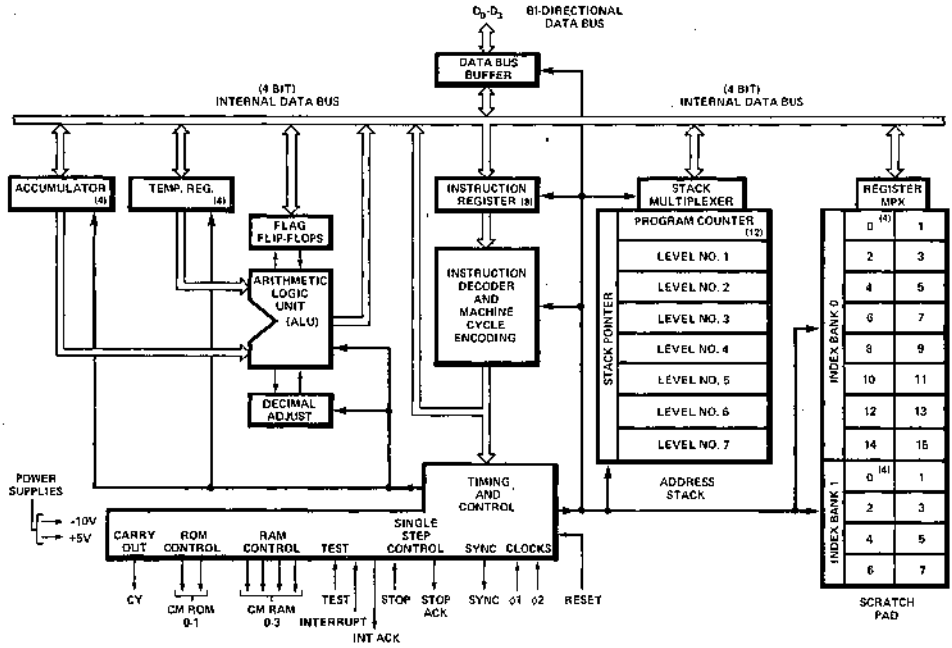
- **Functionally and Electrically Upward Compatible to 4004 CPU**
- **14 New Instructions (60 total) Including Logical Operations and Read Program Memory**
- **Interrupt Capability**
- **Single Step Operation**
- **8K Byte Memory Addressing Capability**
- **24 Index Registers**
- **Subroutine Nesting to 7 Levels**

The Intel® 4040 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used as a replacement for random logic design.

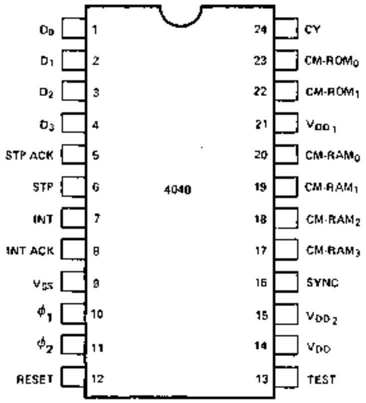
The CPU can directly address 4K eight bit instruction words or 8K with a bank switch. Seven levels of subroutine nesting, including interrupt, and 24 randomly accessable index registers (24x4) are provided as convenient facilities for the designer. The index registers may be used for addressing or for scratch pad memory for storing computation results. The interrupt feature permits a normal program sequence to be interrupted, with normal program execution continuing after the interrupt service routine is completed. Provisions have also been made to permit single-stepping the CPU using the STOP and ACKNOWLEDGE signals.

The 4040 is an enhanced version of the 4004 and as such retains all the functional capability of that device. It will execute all the 4004 instructions, and is also electrically compatible with the other members of the MCS-4 family (4001, 4002, 4003).

4040 CPU BLOCK DIAGRAM



4040 FUNCTIONAL PIN DEFINITION



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

STP

STOP input. A logic "1" level on this input causes the processor to enter the STOP mode.

STPA

STOP ACKNOWLEDGE output. This signal is present when the processor is in the stopped state. Output is "open drain" requiring pull-down resistor to V_{DD}.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

INTA

INTERRUPT ACKNOWLEDGE output. This signal acknowledges receipt of an INTERRUPT signal and prevents additional INTERRUPTS from entering the processor. It remains active until cleared by the execution of the new BRANCH BACK and SRC (BBS) instruction. The output is "open drain" requiring a pull-down resistor to V_{DD}.

RESET

RESET input. A logic "1" level at this input clears all flag and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 96 clock cycles (12 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and sent to ROM and RAM chips. It indicates the beginning of an instruction cycle.

CM-RAM_0 – CM-RAM_3

CM-RAM outputs. These are bank selection signals for the 4002 RAM chips in the system.

CM-ROM_0 – CM-ROM_1

CM-ROM outputs. These are bank selection signals for program ROM chips in the system.

CY

CARRY output. The state of the carry flip-flop is present on this output and updated each X_1 time. Output is "open-drain" requiring pull down resistor to V_{DD}.

ϕ_1, ϕ_2	Two phase clock inputs
V_{SS}	Ground reference – most positive voltage
V_{DD}	−15V ±5% – main supply voltage
*V_{DD_1}	−15V ±5% – Timing supply voltage
**V_{DD_2}	– Output buffer supply voltage

*For low power operation
**May vary depending on system interface

INSTRUCTION SET FORMAT

A. Machine Instructions

- 1 word instruction – 8-bits requiring 8 clock periods (1 instruction cycle)
- 2 word instruction – 16-bits requiring 16 clock periods (2 instruction cycles)

Each instruction is divided into two 4-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

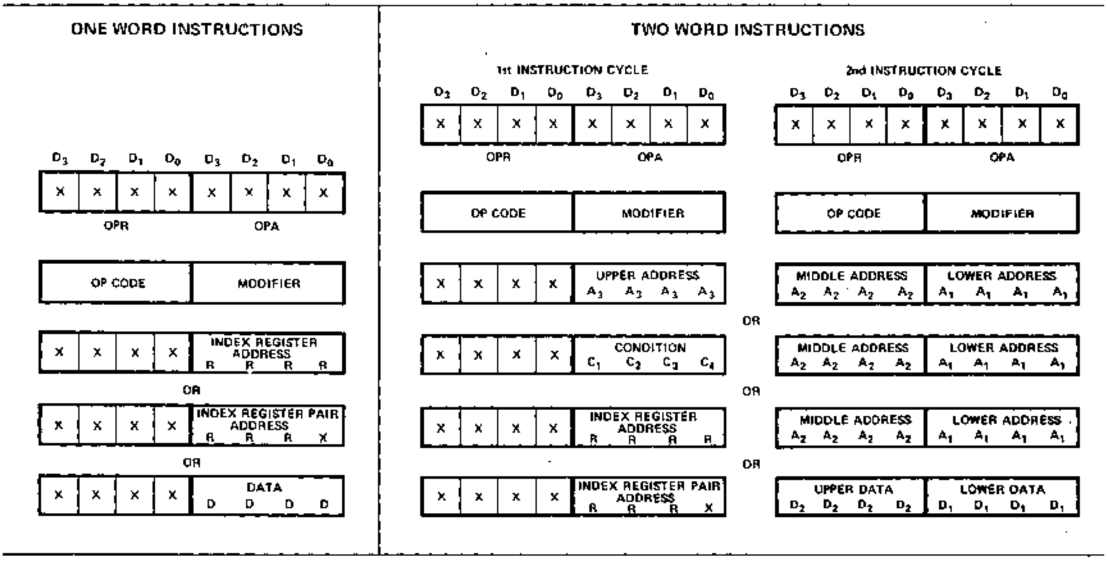


Table I. Machine Instruction Format.

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

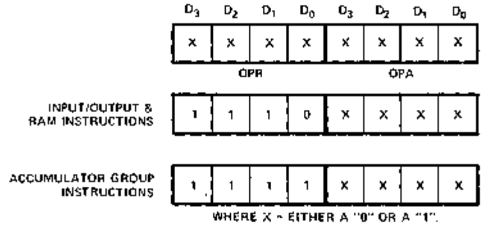


Table II. I/O and Accumulator Group Instruction Formats.

INSTRUCTION SET

Summary of Processor Instructions

*Two Cycle Instructions

		Instruction Code							
Mnemonic	Description	OPR				OPA			
		D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0
	MACHINE GROUP								
NOP	No Operation	0	0	0	0	0	0	0	0
HLT	Halt	0	0	0	0	0	0	0	1
BBS	Branch Back and SRC	0	0	0	0	0	0	1	0
LCR	Command Register to Accumulator	0	0	0	0	0	0	1	1
OR4	Logical OR, Index Register 4 and Accumulator	0	0	0	0	0	1	0	0
OR5	Logical OR, Index Register 5 and Accumulator	0	0	0	0	0	1	0	1
AN6	Logical AND, Index Register 6 and Accumulator	0	0	0	0	0	1	1	0
AN7	Logical AND, Index Register 7 and Accumulator	0	0	0	0	0	1	1	1
DB0	Designate ROM Bank 0	0	0	0	0	1	0	0	0
DB1	Designate ROM Bank 1	0	0	0	0	1	0	0	1
SB0	Select Index Register Bank 0	0	0	0	0	1	0	1	0
SB1	Select Index Register Bank 1	0	0	0	0	1	0	1	1
EIN	Enable Interrupt	0	0	0	0	1	1	0	0
DIN	Disable Interrupt	0	0	0	0	1	1	0	1
RPM	Read Program Memory, Half-Byte per Instruction	0	0	0	0	1	1	1	0
*JCN	Jump Conditional to Address $A_2A_2A_2A_2A_1A_1A_1A_1$ Condition Code, $C_1C_2C_3C_4$	0 A_2	0 A_2	0 A_2	1 A_2	C_1 A_1	C_2 A_1	C_3 A_1	C_4 A_1
*FIM	Fetch Immediate, ROM Data D_2D_1 to Index Register Pair RRR	0 D_2	0 D_2	1 D_2	0 D_2	R D_1	R D_1	R D_1	0 D_1
SRC	Send Register Control	0	0	1	0	R	R	R	1
FIN	Fetch Indirect, Data from ROM to Index Register Pair RRR	0	0	1	1	R	R	R	0
JIN	Jump Indirect to Address in Register Pair RRR	0	0	1	1	R	R	R	1
*JUN	Jump Unconditional to Address $A_3A_2A_1$	0 A_2	1 A_2	0 A_2	0 A_2	A_3 A_1	A_3 A_1	A_3 A_1	A_3 A_1
*JMS	Jump to Subroutine at Address $A_3A_2A_1$	0 A_2	1 A_2	0 A_2	1 A_2	A_3 A_1	A_3 A_1	A_3 A_1	A_3 A_1
INC	Increment Register RRRR	0	1	1	0	R	R	R	R
*ISZ	Increment Register RRRR. Go to Address A_2A_1 if result is not zero, otherwise go to next instruction	0 A_2	1 A_2	1 A_2	1 A_2	R A_1	R A_1	R A_1	R A_1
ADD	Add Register RRRR to Accumulator with Carry	1	0	0	0	R	R	R	R
SUB	Subtract Register RRRR from Accumulator with Borrow	1	0	0	1	R	R	R	R
LD	Load Contents of Register RRRR to Accumulator	1	0	1	0	R	R	R	R
XCH	Exchange Contents of Register RRRR and Accumulator	1	0	1	1	R	R	R	R
BBL	Branch Back and Load Data DDDD to Accumulator	1	1	0	0	D	D	D	D
LDM	Load Data DDDD to Accumulator	1	1	0	1	D	D	D	D

		Instruction Code							
Mnemonic	Description	OPR				OPA			
		D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0
	I/O and RAM GROUP								
WRM	Accumulator to Selected RAM Main Memory Character	1	1	1	0	0	0	0	0
WMP	Accumulator to Selected RAM Output Port	1	1	1	0	0	0	0	1
WRR	Accumulator to Selected ROM Output Port	1	1	1	0	0	0	1	0
WPM	Accumulator to Selected Half-Byte in Read/Write Program Memory	1	1	1	0	0	0	1	1
WR0	Accumulator to Selected RAM Status Character 0	1	1	1	0	0	1	0	0
WR1	Accumulator to Selected RAM Status Character 1	1	1	1	0	0	1	0	1
WR2	Accumulator to Selected RAM Status Character 2	1	1	1	0	0	1	1	0
WR3	Accumulator to Selected RAM Status Character 3	1	1	1	0	0	1	1	1
SBM	Subtract Selected RAM Main Memory Character from Accumulator with Borrow	1	1	1	0	1	0	0	0
RDM	Selected RAM Main Memory Character to Accumulator	1	1	1	0	1	0	0	1
RDR	Selected ROM Input Port to Accumulator	1	1	1	0	1	0	1	0
ADM	Add Selected RAM Main Memory Character to Accumulator with Carry	1	1	1	0	1	0	1	1
RD0	Selected RAM Status Character 0 to Accumulator	1	1	1	0	1	1	0	0
RD1	Selected RAM Status Character 1 to Accumulator	1	1	1	0	1	1	0	1
RD2	Selected RAM Status Character 2 to Accumulator	1	1	1	0	1	1	1	0
RD3	Selected RAM Status Character 3 to Accumulator	1	1	1	0	1	1	1	1
	ACCUMULATOR GROUP								
CLB	Clear Accumulator and Carry	1	1	1	1	0	0	0	0
CLC	Clear Carry	1	1	1	1	0	0	0	1
IAC	Increment Accumulator	1	1	1	1	0	0	1	0
CMC	Complement Carry	1	1	1	1	0	0	1	1
CMA	Complement Accumulator	1	1	1	1	0	1	0	0
RAL	Rotate Left, Accumulator and Carry	1	1	1	1	0	1	0	1
RAR	Rotate Right, Accumulator and Carry	1	1	1	1	0	1	1	0
TCC	Transmit Carry to Accumulator, Clear Carry	1	1	1	1	0	1	1	1
DAC	Decrement Accumulator	1	1	1	1	1	0	0	0
TCS	Transfer Carry Subtract and Clear Carry	1	1	1	1	1	0	0	1
STC	Set Carry	1	1	1	1	1	0	1	0
DAA	Decimal Adjust Accumulator	1	1	1	1	1	0	1	1
KBP	Keyboard Process	1	1	1	1	1	1	0	0
DCL	Designal Command Line	1	1	1	1	1	1	0	1

NOTES:

[1] The condition code is assigned as follows:

$C_1 = 1$ Invert jump condition
$C_1 = 0$ Not invert jump condition
$C_2 = 1$ Jump if accumulator is zero
$C_3 = 1$ Jump if carry/link is a 1
$C_4 = 1$ Jump if test signal is a 0

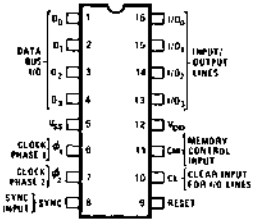
[2] RRR is the address of 1 of 8 index register pairs in the CPU.

[3] RRRR is the address of 1 of 16 index registers in the CPU.

[4] Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

4001

256 x 8-BIT MASK PROGRAMMABLE ROM and 4-BIT I/O PORT



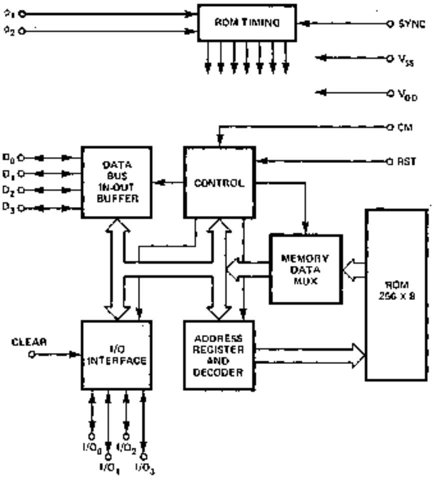
The 4001 is a 2048-bit metal mask programmable ROM providing custom microprogramming capability for the MCS-4™ micro computer set. It is organized as 256 x 8-bit word.

Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a SYNC signal supplied by the CPU. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command Line (CM) is also provided and its scope is to select a ROM bank (group of 16 ROM's).

During the two time periods (M_1 & M_2) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control Device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation.

Each I/O pin can be uniquely chosen as either an input or output port by metal option. Direct or inverted input or output is optional. An on-chip resistor at the input pins, connected to either V_{DD} or V_{SS} is also optional.



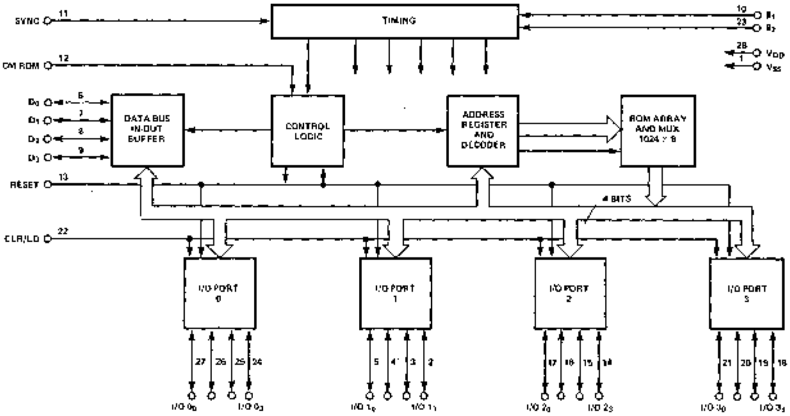
4308

8K MASK PROGRAMMABLE ROM

The 4308 ROM is organized as a 1024 x 8 word array. It is functionally identical to four 4001 ROMs, as well as electrically compatible to all existing MCS-40™ elements.

The 4308 also has 16 programmable I/O lines arranged in four 4-bit ports. Each line may be mask programmed as either an input or output line. The 4308 responds to the RDR, WRR, and SRC commands for I/O operations.

Chip select number is set by metal mask option.



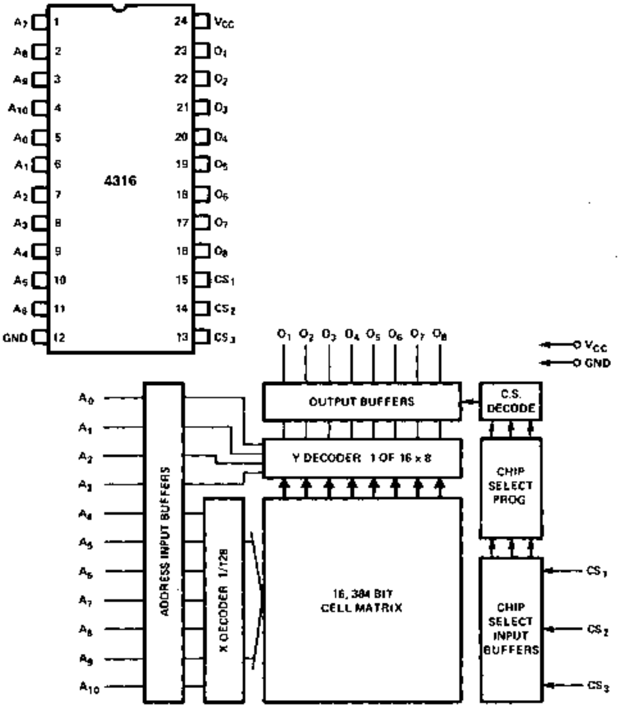
4316

16,384-BIT STATIC MOS ROM

The Intel®4316 is a 16,384 bit static MOS read only memory organized as 2048 words by 8-bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The 4316 access time is 2 μsec.

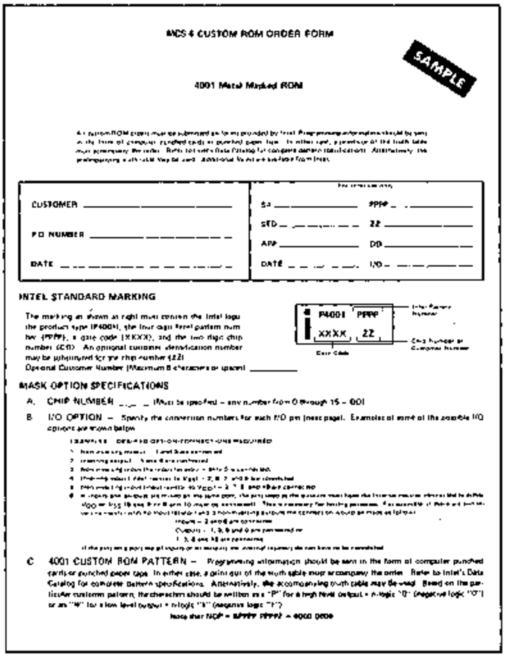
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.



MCS-40™

CUSTOM ROM GENERAL INFORMATION

All custom ROM orders must be submitted on forms provided by Intel. Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a print-out of the truth table must accompany the order.



MCS 4 CUSTOM ROM ORDER FORM

SAMPLE

4001 Metal Masked ROM

CUSTOMER ______	SA ______	PPPP ______
P.O. NUMBER ______	STD ______	ZZ ______
	APP ______	DD ______
DATE ______	DATE ______	I/O ______

INTEL STANDARD MARKING

The marking as shown at right must contain the Intel logo, the product type (P4001), the four digit Intel pattern number (PPPP), a date code (XXXX), and the two digit chip number (CN). An optional customer identification number may be substituted for the chip number (ZZ).

Optional Customer Number (Maximum 6 characters or spaces) ______

P4001 PPPP
XXXX ZZ

MASK OPTION SPECIFICATIONS

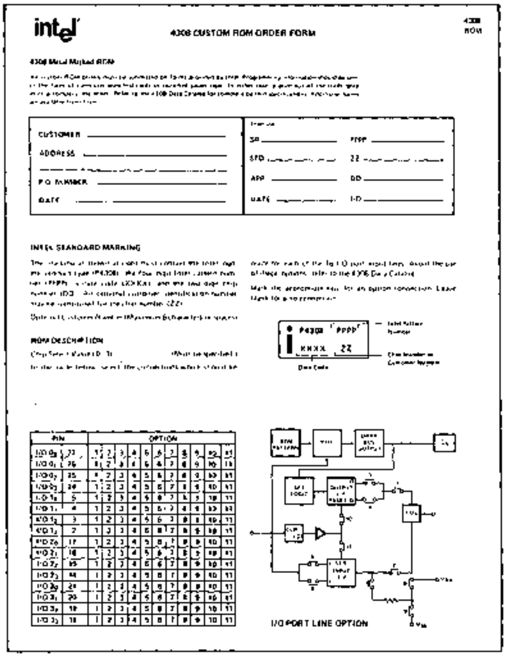
A. CHIP NUMBER ___ (Must be specified – any number from 0 through 15 – 00I)

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below.

C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a print out of the truth table must accompany the order. Refer to Intel's Data Catalog for complete pattern specifications. Alternatively, the accompanying truth table may be used. Based on the particular custom pattern, the character should be written as a "P" for a high level output = n-logic "0" (negative logic "0") or an "N" for a low level output = n-logic "1" (negative logic "1").

Note that NOP = PPPP PPPP = 0000 0000

4001 Custom ROM Order Form



intel

4308 CUSTOM ROM ORDER FORM

4308 ROM

4308 Metal Masked ROM

CUSTOMER ______	SA ______	PPPP ______
ADDRESS ______	STD ______	ZZ ______
P.O. NUMBER ______	APP ______	DD ______
DATE ______	DATE ______	I/O ______

INTEL STANDARD MARKING

P4308 PPPP
XXXX ZZ

ROM DESCRIPTION

4308 Custom ROM Order Form

4702A

2K REPROGRAMMABLE PROM

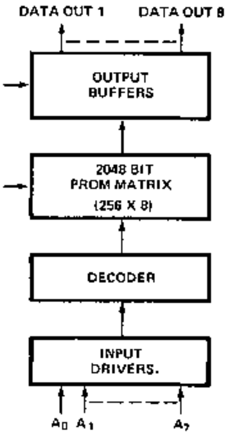
The 4702A is a 256 word by 8-bit electrically programmable ROM ideally-suited for microcomputer system development where a fast turn-around and pattern experimentation are important. The 4702A circuitry is entirely static; no clocks are required.

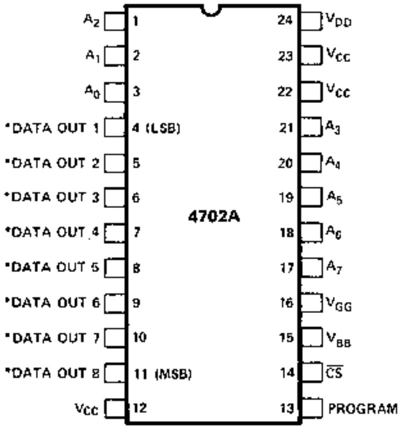
Access time is 1.7 µsec.

The 4702A is packaged in a 24 pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 4702A is designed for use with the MCS-40 CPU's.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs.

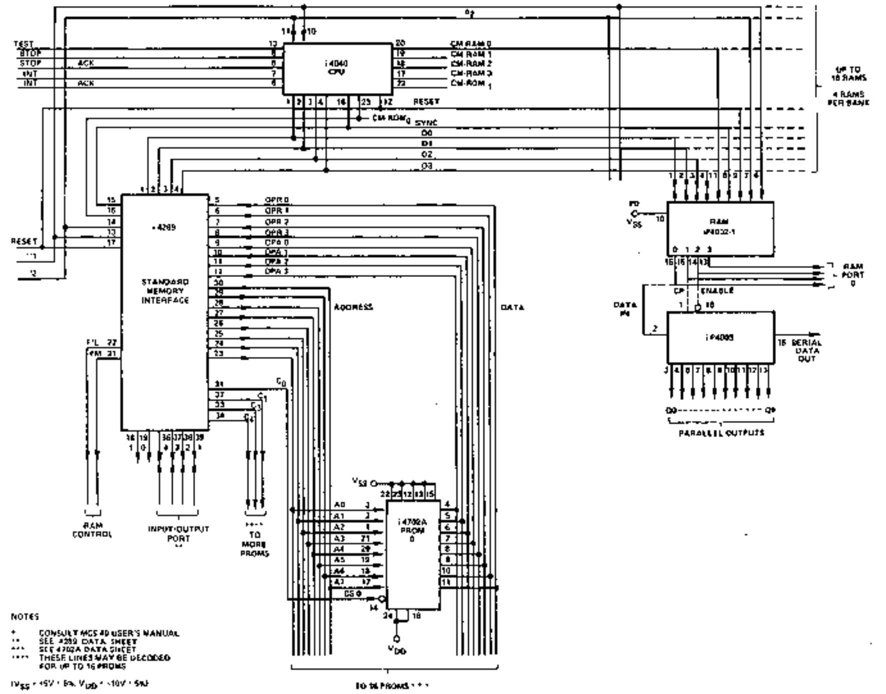




*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.

4040

SYSTEM INTERCONNECT



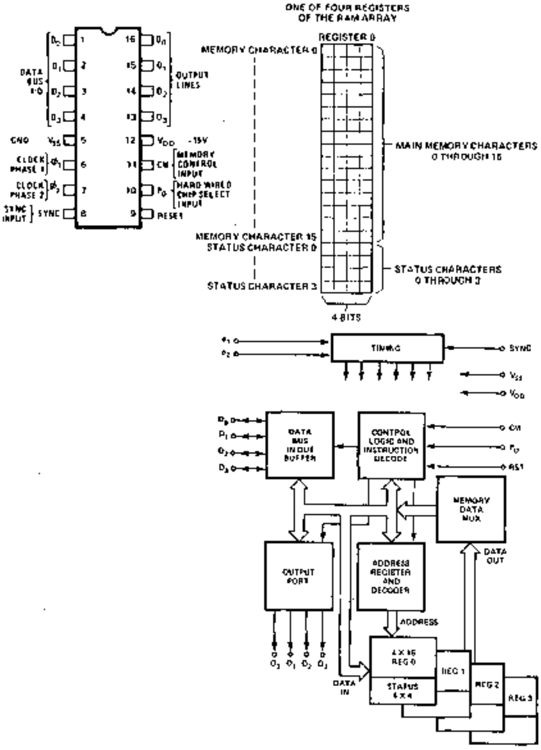
NOTES

* CONSULT MCS 40 USER'S MANUAL
** SEE 4289 DATA SHEET
*** SEE 4702A DATA SHEET
**** THESE LINES MAY BE DECODED FOR UP TO 16 PROMS

(V_{SS} = +5V ± 5%, V_{DD} = −10V ± 5%)

4002

320 BIT RAM and 4-BIT OUTPUT PORT



The 4002 performs two functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4-bit characters each (16 main memory characters and 4 status characters). It is provided with 4 output lines and associated control logic to perform output operations.

In the RAM mode, the operation is as follows: When the CPU executes an SRC instruction (see Basic Instruction Set) it will send out the contents of the designated index register pair during X_2 and X_3 as an address to the RAM, and will activate one CM-RAM line at X_2 for the previously selected RAM bank.

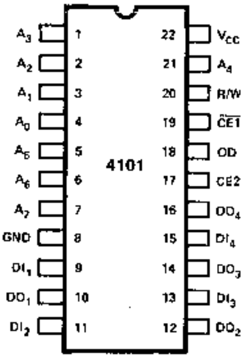
The status character locations (0 through 3) are selected by the OPA portion of one of the I/O and RAM Instructions.

For chip selection, the 4002 is available in two metal options, 4002-1 and 4002-2. An external pin, P_0 (which may be hard wired to either V_{DD} or V_{SS}) is also available for chip selection.

All communications with the system is through the data bus. The I/O port permits data out from the system. When the external RESET signal goes low, the memory and all static flip-flops (including the output registers) will be cleared. To fully clear the memory the RESET signal must be maintained for at least 32 memory cycles (32 x 8 clock periods).

4101

1024-BIT STATIC MOS RAM WITH SEPARATE I/O

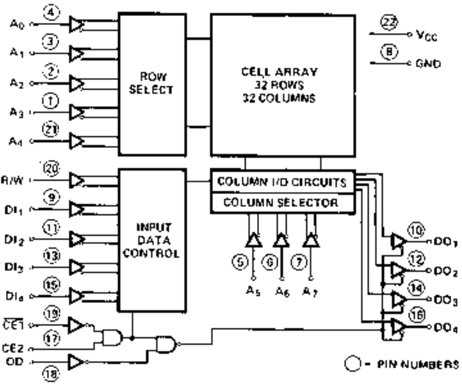


The Intel®4101 is a 256 word by 4-bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 4101 access time is 1 μs.

The 4101 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.



4003

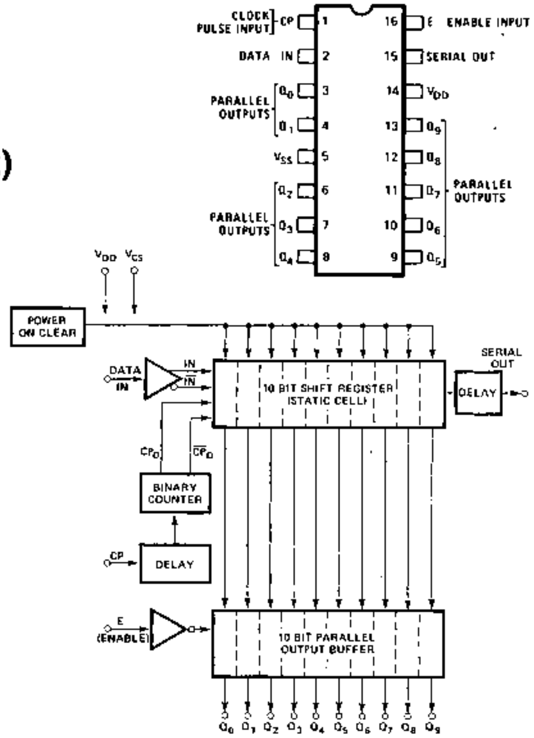
10-BIT SERIAL-IN/PARALLEL-OUT SERIAL-OUT SHIFT REGISTER (SR)

The 4003 is a 10-bit static shift register with serial-in, parallel-out and serial-out data. Its function is to increase the number of output lines to interface with I/O devices such as keyboards, displays, printers, teletypewriters, switches, readers, A-D converters, etc.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = low), the shift register contents is read out; when not enabled (E = high), the parallel-out lines are at V_{SS}. The serial-out line is not affected by the enable logic.

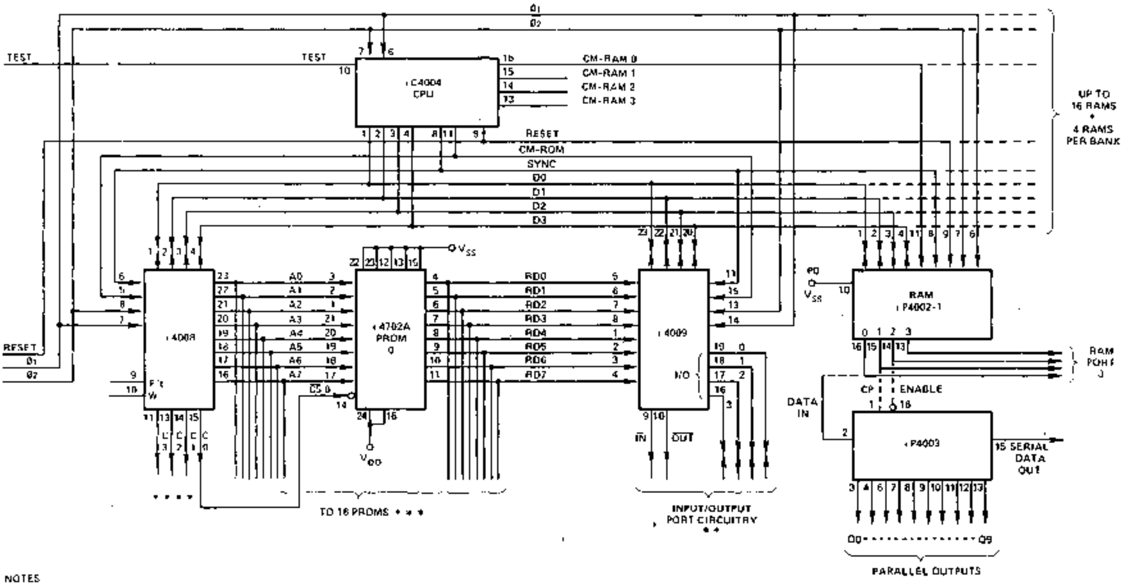
Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register (Q_i = V_{SS}) between the application of the supply voltage and the first CP signal.



4004

SYSTEM INTERCONNECT



NOTES
- * CONSULT MCS-4 USER'S MANUAL
- ** SEE 4008/4009 DATA SHEET
- *** SEE 4702A DATA SHEET
- **** THESE LINES MAY BE DECODED FOR UP TO 16 PROMS

(V_{SS} = +5V ±5%, V_{DD} = -10V ±5%)

4207, 4209, 4211

GENERAL PURPOSE I/O

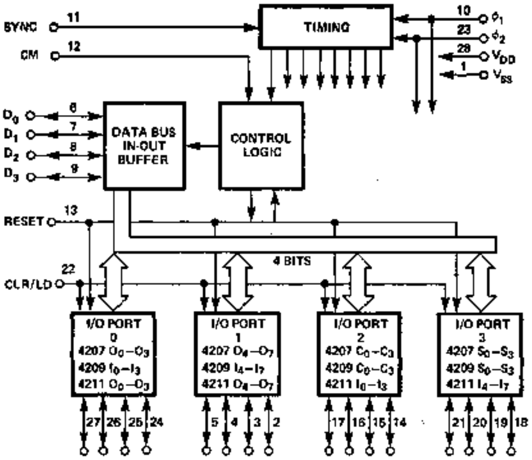
These three I/O devices expand MCS-40™ CPUs. Each device has four 4-bit ports designated as input or output. They respond to the SRC, RDR, and WRR commands, and Chip Select No. 3 (ROM pages 12-15).

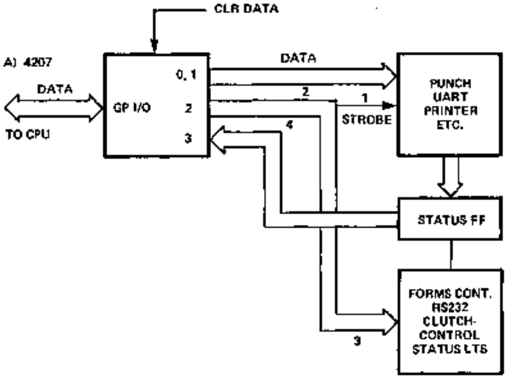
4207 Two 4-bit output ports loaded under program control. Contains the output data word(s). One 4-bit output port as a control source to steer data and control I/O device. One 4-bit input port for I/O status input data.

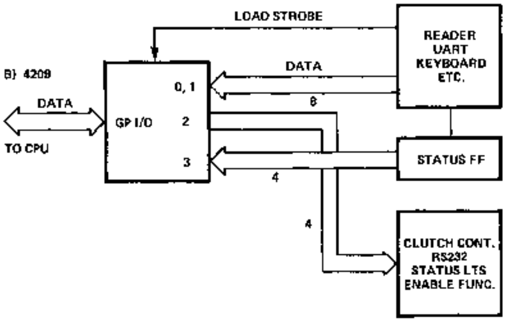
4209 Two 4-bit input ports for I/O input data. External strobe simultaneously loads input buffer. One 4-bit input port for I/O status input data. One 4-bit output port for I/O control data.

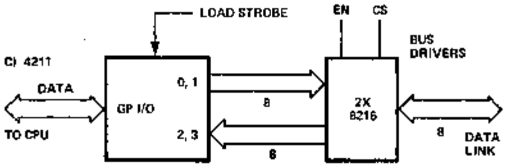
4211 Two 4-bit input ports. Two 4-bit output ports. This device is useful for byte transfers.

4207, 4209, 4211 FUNCTIONAL BLOCK DIAGRAM

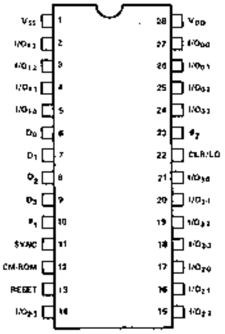








4207, 4209, 4211 PIN CONFIGURATION



4008/4009
STANDARD MEMORY AND I/O INTERFACE SET

The standard memory and I/O interface set (4008/4009) provides the complete control functions performed by the 4001 in MCS-4™ systems. The 4008/4009 are completely compatible with other members of the MCS-4 family. All activity is still under control of the 4004 CPU. One set of 4008/4009 and several TTL decoders is sufficient to interface to 4K words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

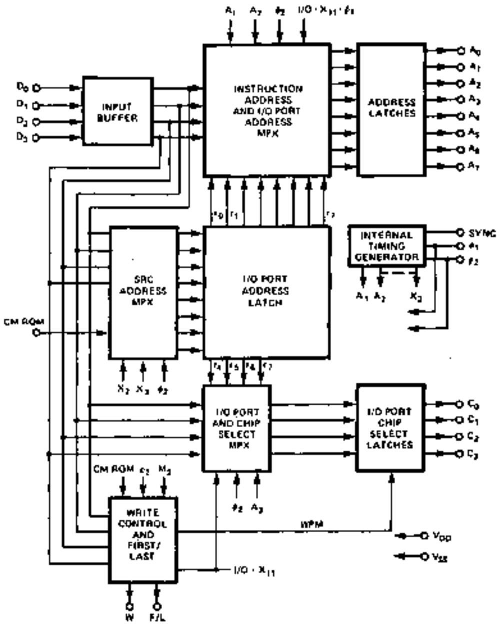
It should be noted that in any MCS-4 system the program memory is distinct from the read/write data storage (4002 RAM). Using the 4008/4009, programs can now be stored and executed from RAM memory, but this RAM memory is distinct from the 4002 read/write data storage. RAM program memory will be organized in eight bit words and 256 word pages, just like the memory array inside the 4001. Any combination of PROM, ROM, and RAM will be referred to as program memory. A formerly undefined instruction is now used in conjunction with the 4008/4009 to write data into the RAM program memory. This new instruction is called WPM (Write Program Memory – 1110 0011). When an instruction is to be stored in RAM program memory, it is written in two four-bit segments.

The 4008 is the address latch chip which interfaces the 4004 to standard PROMs, ROMs and RAMs used for program memory. The 4008 latches the eight bit program address sent out by the CPU during A1 and A2 time. During A3 time it latches the ROM chip number from the 4004. The eight bit program address is then presented at pins A0 through A7 and the four bit chip number (also referred to as page number) is presented at pins C0 through C3. These four bits must be decoded externally and one page of program memory is selected.

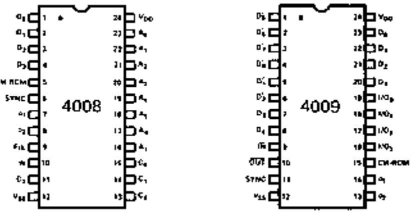
The 4009 then transfers the eight bit instruction from program memory to the 4004 four bits at a time at M1 and M2. The command signal sent by the CPU activates the 4009 and initiates this transfer.

When the CPU executes and SRC (Send Register Control) instruction, the 4008 responds by storing the I/O address in its eight bit SRC register. The content of this SRC register is always transferred to the address lines (A0 through A7) and the chip select lines (C0 through C3) at X1 time. The appropriate I/O port is then selected by decoding the chip select lines. The IN and OUT lines of the 4009 indicate whether an input or output operation will occur.

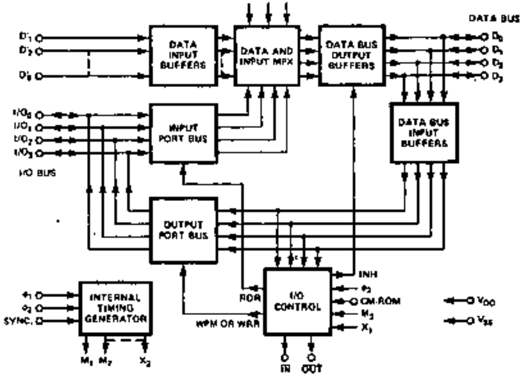
The 4009 is primarily an instruction and I/O transfer device. When the CPU executes an RDR (Read ROM Port) instruction, the 4009 will send an input strobe (pin 9) to enable the selected input port. It also enables I/O input buffers to transfer the input data from the I/O bus to the data bus. When the 4009 interprets a WRR (Write ROM Port) instruction, it tranfers output data from the CPU to the I/O bus and sends an output strobe (pin 10) to enable the selected output port.



4008 Block Diagram



Pin Configurations

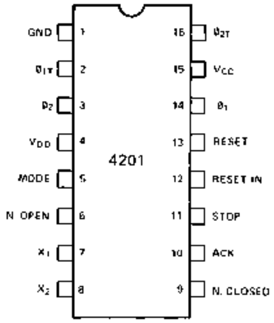


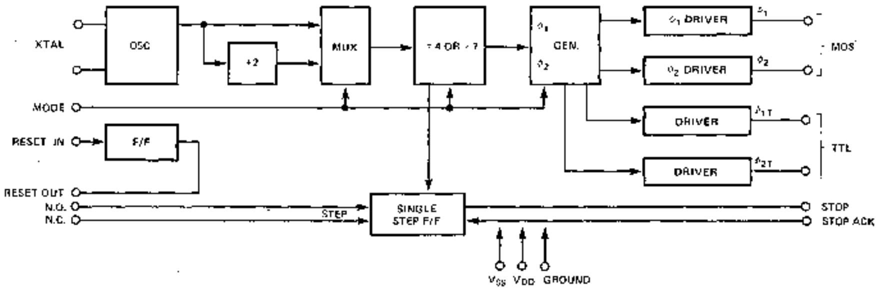
4009 Block Diagram

4201
CLOCK GENERATOR

The 4201 generates the two phase clock signals used by the MCS-40™ CPU's, ROMs, RAMs and I/O circuits. Both MOS and TTL level signals are available. Only an external crystal is required for the 4201. An internal divider selected by the MODE line divides the crystal frequency by seven or eight. A RESET signal generator is also provided for power-on or external reset requirements.

Switch inputs and the STOP and STOP/ACK signals provide the means to single step the 4040 CPU.



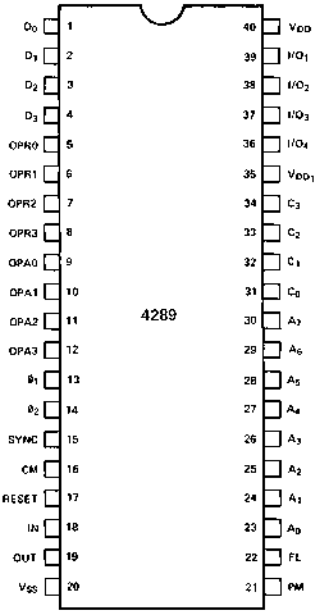


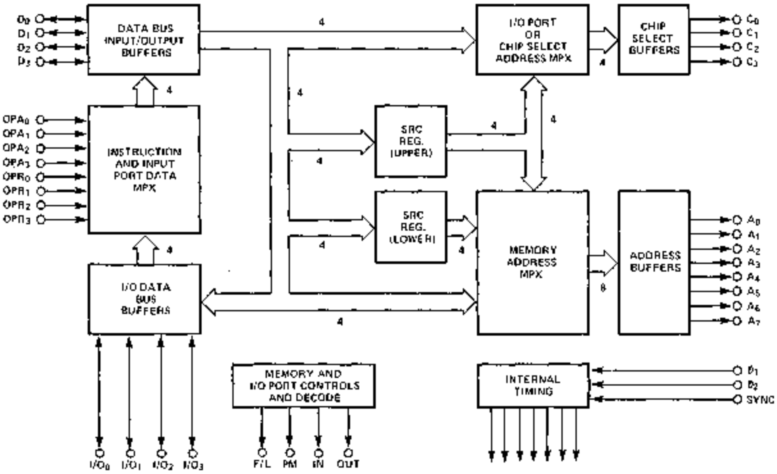
4289
STANDARD MEMORY INTERFACE

The 4289 enables the CPU devices to utilize standard memory components — PROMs, ROMs, RAMs, in a memory array to facilitate system program development.

The 4289 also contains an I/O bus enabling expansion of the ROM I/O ports, using the RDR and WRR commands. The READ PROGRAM MEMORY (RPM) and WRITE PROGRAM MEMORY (WPM) commands allow the user to store data and modify program memory.

The 4289 directly addresses 4K of program memory, and is a functional replacement for the 4008, 4009 pair of standard memory interface and I/O devices. Programs generated using the 4289 may be committed to ROM (4308 and 4001) with no software changes.





INTELLEC® 4 / MOD 4
MICROCOMPUTER DEVELOPMENT SYSTEM

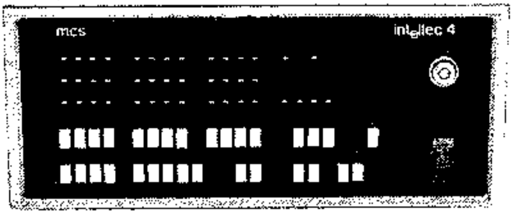
- **Complete hardware/software development system for the design and implementation of 4004 CPU based microcomputer systems.**
- **TTY interface, front panel designer's console, and high speed paper tape reader interface, in conjunction with PROM resident system monitor provide complete program loading, punching, monitoring, interrogation, and alteration capabilities.**
- **Program RAM (4K 8-bit bytes) provides a program development medium which lends itself to rapid and facile program monitoring and alteration.**
- **Data RAM (320 4-bit bytes expandable to 2560 bytes) provides data storage capacity.**
- **Program PROM (expandable to 4K 8-bit bytes) in conjunction with the resident PROM programmer provide capability of simulating final ROM resident program.**
- **PROM resident system monitor, RAM resident assembler.**
- **Includes program development features such as address search (and pass count), next instruction indication, program flow verification.**
- **I/O expandable to 16 4-bit input ports and 48 4-bit output ports (all TTL compatible) allowing simulation of entire user system (processor and peripheral devices).**
- **Modular design with expansion capability provided for up to eleven optional or user designed modules.**

The Intellec 4/MOD 4 (imm 4-40A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 4004 CPU based microcomputer systems. Its modular design provides the flexibility to adapt to any size user system and the resident software facilitates program development.

The basic Intellec 4/MOD 4 Microcomputer Development System consists of 4 microcomputer modules (CPU, RAM, and PROM PROGRAMMER), power supplies, I/O connectors, console, and displays. The heart of the system is the imm 4-42 central processor module built around Intel's 4-bit 4004 CPU. The imm 4-42 is a complete microcomputer system containing the system clock, 1K 8-bit bytes of PROM memory, 320 4-bit bytes of data RAM memory, 4 4-bit input ports and 8 4-bit output ports. The imm 6-28 program RAM memory module contains a 4K x 8 memory array composed of Intel 2102 static random access memory elements. The imm 6-76 PROM programmer module provides the capability of programming Intel 1702A PROMs in conjunction with the front panel PROM socket and system monitor. All I/O ports are TTL compatible and accessible from the back panel 37-pin connectors. The front panel designer's console provides a means of monitoring and controlling system operation.

The Intellec® modular design allows great design system flexibility. Program PROM can be expanded to 4K 8-bit bytes using imm 6-26 or imm 4-22 optional modules. Data RAM can be expanded to 2560 4-bit bytes using imm 4-24 modules. I/O capability can be expanded to 16 4-bit input and 48 4-bit output ports using optional imm 4-60 and 4-24 modules. The universal prototype card (imm 6-70) in conjunction with the eleven optional card sockets (which contain all essential system signals) provide the capability for interfacing custom designed modules.

Program interrogation and alteration can be accomplished by using any desired combination of the front panel designer's console, a teletype, the imm 4-90 high speed paper tape reader, and other Intellec compatible peripherals. The front panel designer's console provides the capability of manually writing data into memory and displaying memory contents, monitoring CPU bus contents during each processor subcycle, "freezing" system status after executing of a predefined instruction after a specified number of passes, and verifying program flow. The teletype and reader serve as vehicles to input and output paper tapes and execute the system monitor.



INTELLEC® 4/MOD 40 MICROCOMPUTER DEVELOPMENT SYSTEM

- **Complete hardware/software development system for the design and implementation of 4040 CPU based microcomputer systems.**
- **TTY interface, front panel designer's console, and high speed paper-tape reader interface, in conjunction with PROM resident system monitor provide complete program loading, punching, monitoring, interrogation, and alteration capabilities.**
- **Program RAM (4K 8-bit bytes) provides a program development medium which lends itself to rapid and facile program monitoring and alteration.**
- **Data RAM (320 4-bit bytes expandable to 2560 bytes) provides data storage capacity.**
- **Program PROM (expandable to 4K 8-bit bytes) in conjunction with the resident PROM programmer provide capability of simulating final ROM resident program.**
- **PROM resident system monitor, RAM resident assembler with edit feature included in standard systems software.**
- **Includes such standard program development features as program single step, address search (and pass count), next instruction indication, program flow verification.**
- **I/O expandable to 16 4-bit input ports and 48 4-bit output ports (all TTL compatible) allowing "hands-on" simulation of entire user system (processor and peripheral devices).**
- **RESET, STOP, INTERRUPT control signals available to user via back panel.**
- **Modular design with expansion capability provided for up to eleven optional or user designed modules.**

The Intellec 4/MOD 40 (imm 4-44A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 4040 CPU based microcomputer systems. Its modular design provides the flexibility to adapt to any size user system and the resident software facilitates program development.

The basic Intellec 4/MOD 40 Microcomputer Development System consists of 4 microcomputer modules (CPU, RAM, MEMORY CONTROL, and PROM PROGRAMMER), power supplies, I/O connectors, console, and displays. The heart of the system is the imm 4-43 central processor module built around Intel's high performance 4-bit 4040 CPU. The imm 4-43 is a complete microcomputer system containing the system clock, 1K 8-bit bytes of PROM memory, 320 4-bit bytes of data RAM memory, 3 4-bit input ports and 8 4-bit output ports. The imm 6-28 program RAM memory module contains a 4K x 8 memory array composed of Intel 2102 static random access memory elements. The imm 4-72 control module contains the circuitry required to interface the central processor module to the program RAM module. The imm 6-76 PROM programmer module provides the capability of programming Intel 1702A PROMs in conjunction with the front panel PROM socket and system monitor. All I/O ports are TTL compatible and accessible from the back panel 37-pin connectors. The front panel designer's console provides a means of monitoring and controlling system operation.

The Intellec® modular design allows great design system flexibility. Program PROM can be expanded to 4K 8-bit bytes using imm 6-26 or imm 4-22 optional modules. Data RAM can be expanded to 2560 4-bit bytes using imm 4-24 modules. I/O capability can be expanded to 16 4-bit input and 48 4-bit output ports using optional imm 4-60 and 4-24 modules. The universal prototype card (imm 6-70) in conjunction with the eleven optional card sockets (which contain all essential system signals) provide the capability for interfacing custom designed modules.

The user RESET IN/OUT, STOP/STOP ACKNOWLEDGE, and INTERRUPT/INTERRUPT ACKNOWLEDGE control signals are all available at the back panel. Hence, the user can interrupt, halt, and reset the resident CPU via his own interface.

Program interrogation and alteration can be accomplished by using any desired combination of the front panel designer's console, a teletype, the imm 4-90 high speed paper tape reader, and other Intellec compatible peripherals. The front panel designer's console provides the capability of manually writing data into memory and displaying memory contents, monitoring CPU bus contents during each processor subcycle, "freezing" system status after executing of a predefined instruction after a specified number of passes, single-stepping the program and verifying program flow. The teletype and reader serve as vehicles to input and output paper tapes and execute the system monitor.

imm4-90

INTELLEC® 4 HIGH SPEED PAPER TAPE READER

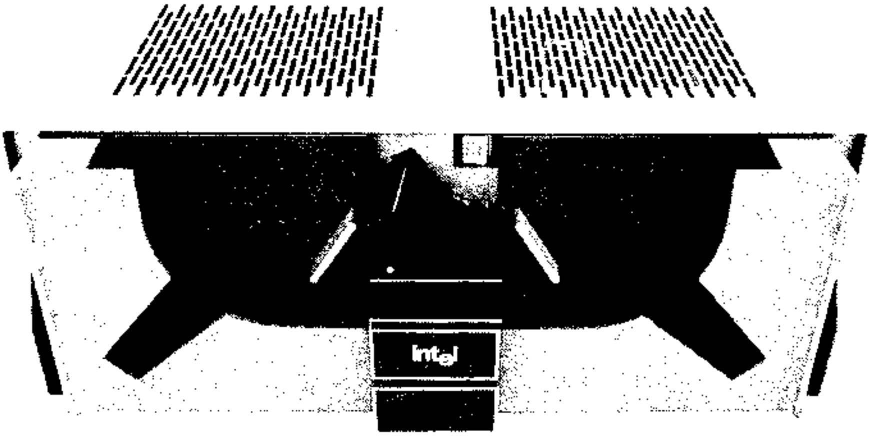
- **TAPE MOVEMENT**
  Tape Reading Speed:
  0 to 200 characters per second asynchronous
  Tape Stopping:
  Stops "On Character"
- **TAPE CHARACTERISTICS**
  Tapes must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.
  Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 57% (oiled buff paper tape).
  Tape loading: in line
  Tape width: 1 inch
- **ELECTRICAL CHARACTERISTICS**
  AC Power Requirement:
  3 wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.
- **EQUIPMENT SUPPLIED**
  Paper Tape Reader
  Reader Cable
  Reader Flat Cable
  Fanfold Tape Guide
  Fanfold Paper Tape
  Hardware Manual
  Installation and Operations Guide
  Fanfold Guide Installation Instructions

NOTE: Operation of the imm4-90 in conjunction with the Intellec 4/MOD 4 and Intellec 4/MOD 40 requires Version 2.0 software.

The imm4-90 high speed paper tape reader provides all Intellec 4 Microcomputer Development Systems with a high speed paper tape input that is twenty times faster than the standard ASR-33 teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.

The Intellec 4 monitor provides the capability of assigning the imm4-90 as an input device and contains the reader driver software. Tapes may be read in BNPF or hexadecimal format.

At least one optional imm4-60 Input/Output Module must be included in the Intellec system to provide the required reader input and output ports.



PA4-04 PROGRAM ANALYZER FOR MCS-4 DEVELOPMENT SYSTEM

The PA4-04 Program Analyzer is a compact (9" x 9" x 1.5") portable unit providing a powerful real-time analysis capability for MCS-4™ users. It was designed as an MCS-4 development tool and for convenient field service of microcomputer systems. Applications consist of software and system debugging, CPU data logging, program event detector, address comparator, binary display unit, and trouble shooting in the field.

The analyzer connects to the 4004 CPU via a 16 pin DIP-CLIP and displays all of the significant CPU parameters. LED displays thus latch and display the contents of the four bit data bus displaying the address sent out by the CPU, the instruction received back from ROM and the execution by the CPU. Displays also indicate which CM-RAM line is active and what the last RAM/ROM point is (SRC-instructions). In the free running mode this display is naturally changing as the program runs.

Provisions have been made for examining the contents of the data bus and the status of the CPU at selected points in the program. This is done by entering the selected instruction number into the SEARCH ADDRESS switches provided on the front panel. Now as the program runs the PA4-04 will latch the data at the selected instruction number. The display will hold until the reset button is hit (which also applies a reset pulse to the MCS-4 system being operated on).

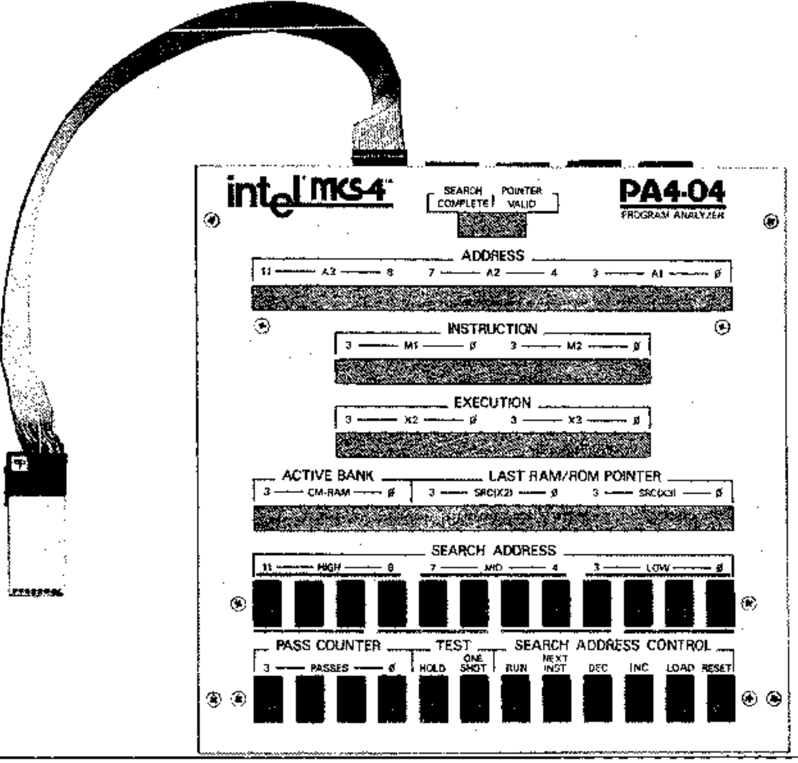
While the display of the search address is latched, the next instruction can be examined by hitting the NEXT INSTRUCTION switch. Pushing the INCREMENT button will increment the program one more count and this can be continued indefinitely. The previous instruction can be examined by using the DECREMENT switch in the same fashion.

A switch selectable pass counter provides interrogation of program loops by delaying the display until after a preset number of passes (1 to 15) have been made through the preset SEARCH ADDRESS.

SEARCH CONTROL and TEST switches provide additional features for easy program debugging.

All displayed parameters are also accessible in buffered TTL form via external 16 pin DIP sockets on the back panel. This allows for external monitoring needed for data logging applications.

The PA4-04 requires a single external power supply (+5V DC, 2.0A) which is connected to banana plug provided on the back panel.



intel® Silicon Gate MOS 8008, 8008-1

SINGLE CHIP EIGHT-BIT PARALLEL CENTRAL PROCESSOR UNIT

- **Instruction Cycle Time — 12.5 μs with 8008-1 or 20 μs with 8008**
- **Directly addresses 16K x 8 bits of memory (RAM, ROM, or S.R.)**
- **Interrupt Capability**
- **48 Instructions, Data Oriented**
- **Address stack contains eight 14-bit registers (including program counter) which permit nesting of subroutines up to seven levels**

The 8008 is a single chip MOS 8-bit parallel central processor unit for the MCS-8 microcomputer system.

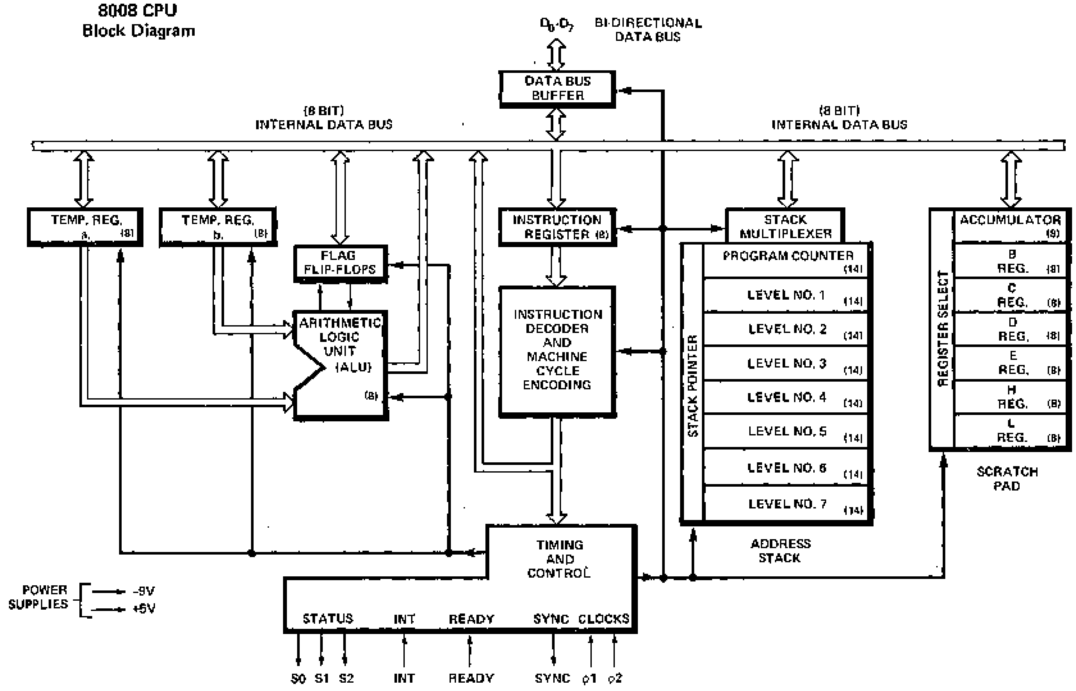
This CPU contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and seven 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM or S.R.).

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

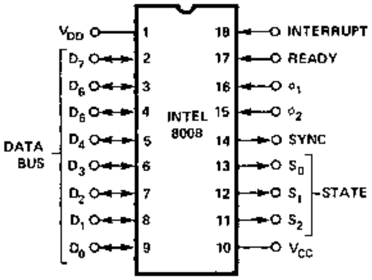
The normal program flow of the 8008 may be interrupted through the use of the INTERRUPT control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The READY command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

8008 CPU
Block Diagram



8008 FUNCTIONAL PIN DESCRIPTION



D_0-D_7

BI-DIRECTIONAL DATA BUS. All address and data communication between the processor and the program memory, data memory, and I/O devices occurs on these 8 lines. Cycle control information is also available.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

READY

READY input. This command line is used to synchronize the 8008 to the memory cycle allowing any speed memory to be used.

SYNC

SYNC output. Synchronization signal generated by the processor. It indicates the beginning of a machine cycle.

ϕ_1, ϕ_2

Two phase clock inputs.

S_0, S_1, S_2

MACHINE STATE OUTPUTS. The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals S_0, S_1, and S_2, along with SYNC inform the peripheral circuitry of the state of the processor.

V_{CC} +5V ±5%

V_{DD} -9V ±5%

BASIC INSTRUCTION SET

Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OP CODE	
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OPERAND	Immediate mode instructions
Three Byte Instructions		
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OP CODE	
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	LOW ADDRESS	JUMP or CALL instructions
X X $D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	HIGH ADDRESS*	

*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7\ D_6$	 $D_5\ D_4\ D_3$	 $D_2\ D_1\ D_0$	DESCRIPTION OF OPERATION
(1) MOV r_1, r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
MVI M	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

BASIC INSTRUCTION SET

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
ANA r	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
ANA M	(8)	1 0	1 0 0	1 1 1	
ANI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRA r	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRA M	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORA r	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator .
ORA M	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CMP r	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CMP M	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.

Program Counter and Stack Control Instructions

(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
JC, JZ JM, JPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
CALL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
CNC, CNZ, CP, CPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CC, CZ, CM, CPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ RM, RPE	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

Input/Output Instructions

IN	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).

Machine Instruction

HLT	(4) (4)	0 0 1 1	0 0 0 1 1 1	0 0 X 1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

(1) SSS = Source Index Register, DDD = Destination Index Register] These registers, r_i, are designated A(accumulator—000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

intel® Silicon Gate MOS 8080

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

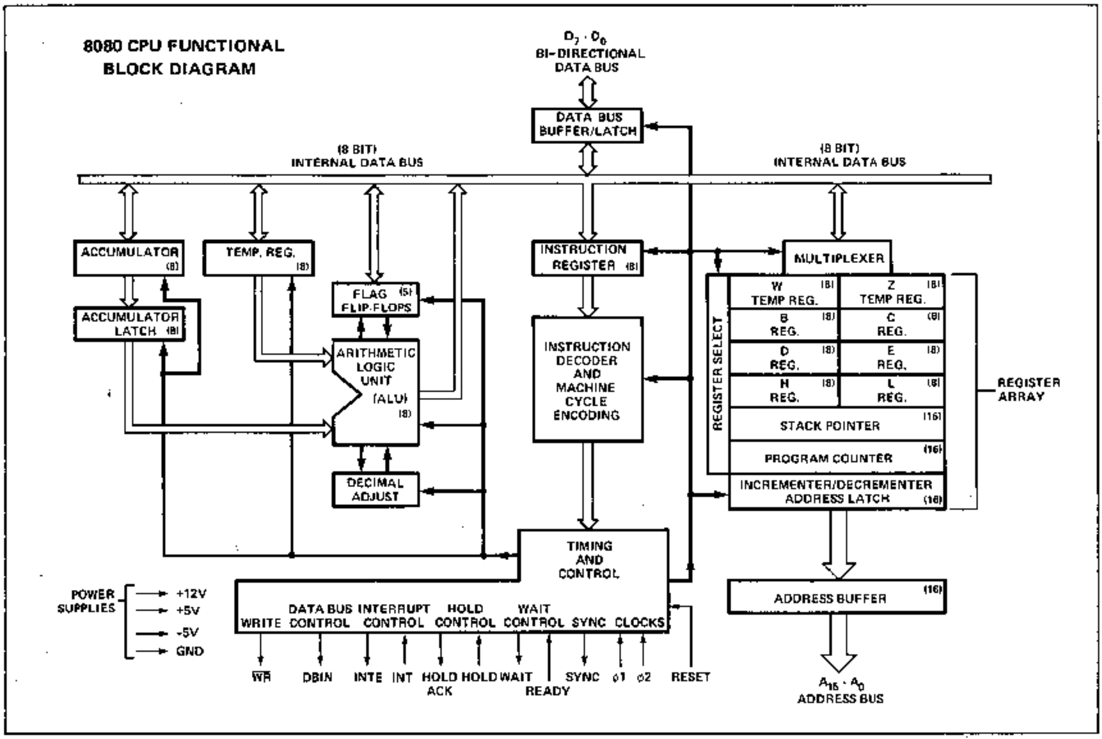
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

The Intel® 8080 is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080 contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080 has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080 the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microcoprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



8080 CPU FUNCTIONAL BLOCK DIAGRAM

8080 FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080 I/O pins. Several of the descriptions refer to internal timing periods.[1]

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bidirectional communication between the CPU, memory, and I/O devices for instructions and data transfers. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080 data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080 that valid memory or input data is available on the 8080 data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080 does not receive a READY input, the 8080 will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{\text{WR}}$ (output)
WRITE; the $\overline{\text{WR}}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{\text{WR}}$ signal is active low ($\overline{\text{WR}}$ = 0).

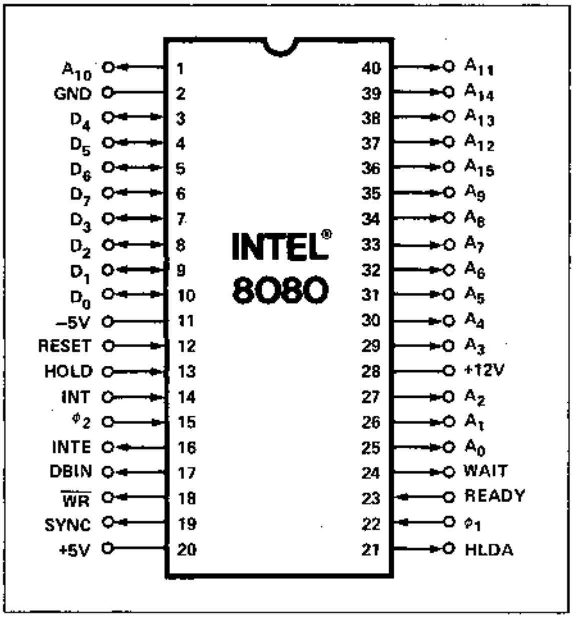
HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080 address and data bus as soon as the 8080 has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.



Pin Configuration

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input)[2]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{ss}	Ground Reference.
V_{dd}	+12 ± 5% Volts.
V_{cc}	+5 ± 5% Volts.
V_{bb}	−5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080 instruction set.

The following special instruction group completes the 8080 instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions
Two Byte Instructions		
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OP CODE	
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OPERAND	Immediate mode or I/O instructions
Three Byte Instructions		
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	OP CODE	Jump, call or direct load and store instructions
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	LOW ADDRESS OR OPERAND 1	
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	HIGH ADDRESS OR OPERAND 2	

For the 8080 a logic "1" is defined as a high level and a logic "0" is defined as a low level.

INSTRUCTION SET

Summary of Processor Instructions

				Instruction Code[1]						Clock[2]
Mnemonic	Description	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles
MOV $_{r1, r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M, r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11

				Instruction Code[1]						Clock[2]
Mnemonic	Description	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Compliment A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Compliment carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS — 000 B — 001 C — 010 D — 011 E — 100 H — 101 L — 110 Memory — 111 A.

2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

8308

8K STATIC MOS ROM

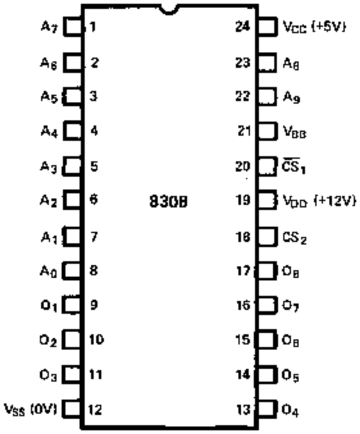
The Intel 8308 is an 8,192 bit static MOS Read Only Memory organized as 1024 words by 8-bits.

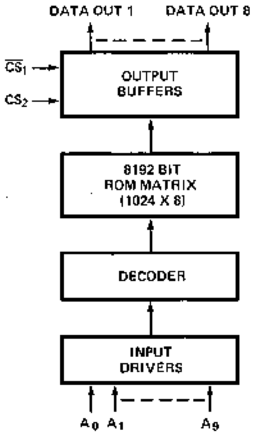
The access time is 450 nanoseconds.

This ROM is designed for 8080 microcomputer system applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible.

Three state outputs permit OR-tie capability. Two chip select inputs are provided for easy system memory expansion.





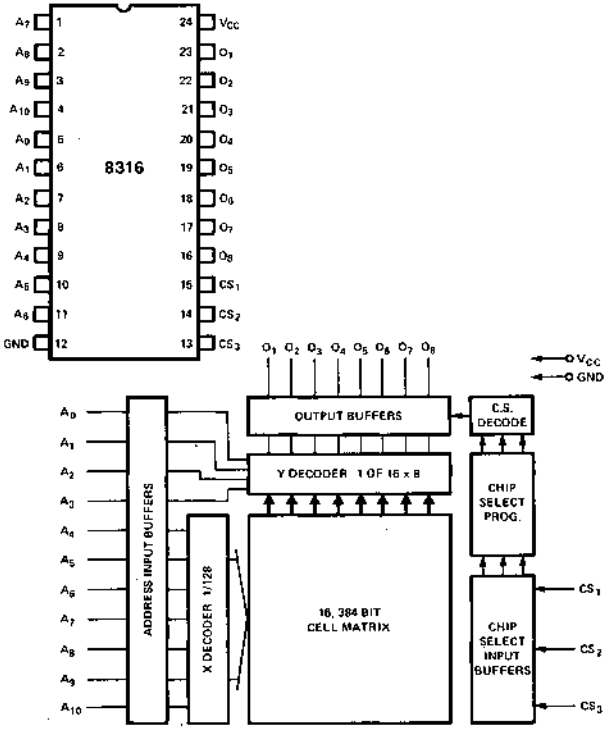
8316

16K STATIC MOS ROM

The Intel 8316 is a 16,384 bit static MOS read only memory organized as 2048 words by 8-bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The 8316 access time is 2 μsec.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.



PRELIMINARY

8604

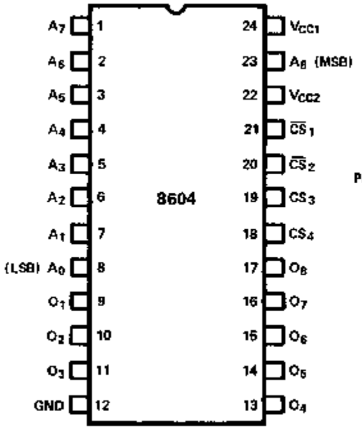
HIGH SPEED 4096 BIT ELECTRICALLY PROGRAMMABLE ROM

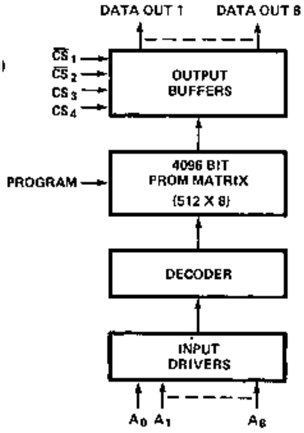
The 8604 is a 512 x 8 electrically programmable ROM ideally suited for high performance microcomputer systems where fast turnaround is important for system program development and for small volumes of identical programs in production systems.

The 8604 has an access time of 100 nanoseconds. It is fully decoded.

Chip select lines are available which permit easy system memory expansion.

The 8604 is a Schottky Bipolar device.





8702A, 8702A-4

2K REPROGRAMMABLE PROM

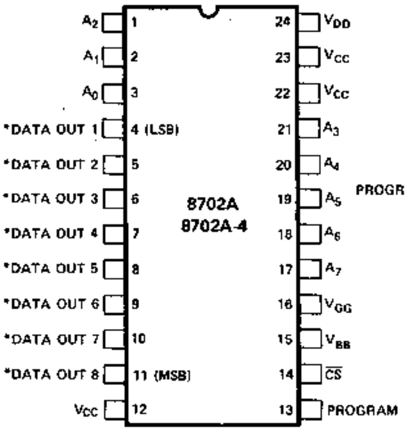
The 8702A is a 256 word by 8-bit electrically programmable ROM ideally suited for microcomputer system development where a fast turn-around and pattern experimentation are important. The 8702A circuitry is entirely static; no clocks are required.

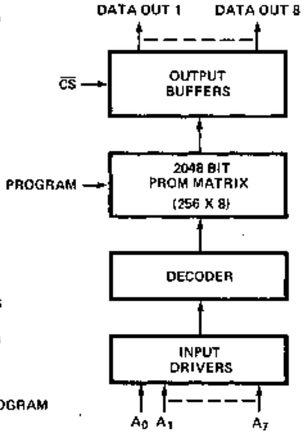
8702A access time is 1.3 μsec.

8702A-4 access time is 2.3 μsec.

The 8702A is packaged in a 24 pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

A pin-for-pin metal mask programmed ROM, the Intel 8302, is ideal for large volume production runs.





*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.

8101

1024 BIT (256 x 4) STATIC MOS RAM WITH SEPARATE I/O

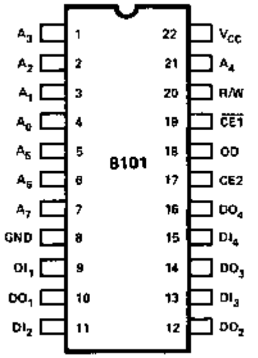
The Intel 8101 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices.

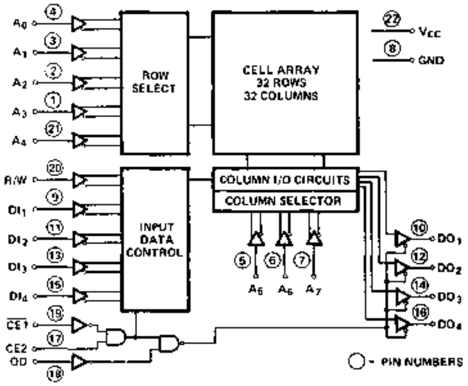
The 8101 access time is 850ns.

It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bidirectional logic.

The 8101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.





8111

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

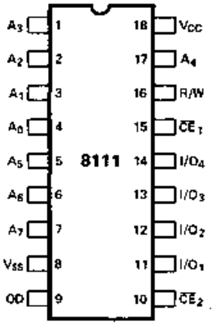
The Intel 8111 is a 256 word by 4 bit static random access memory element using normally off N-channel MOS devices.

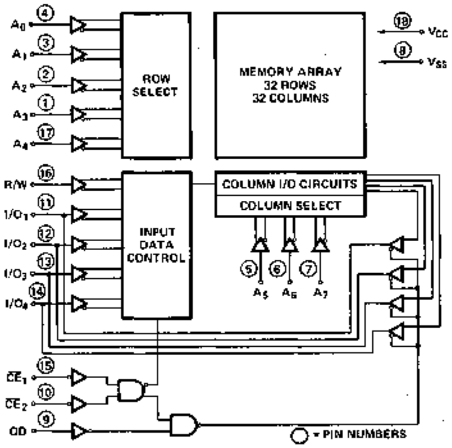
The 8111 access time is 850ns.

It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

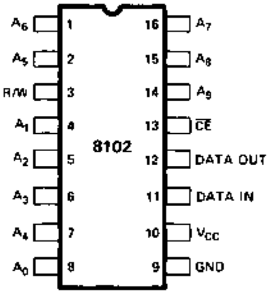
The 8111 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.





8102, 8102-2

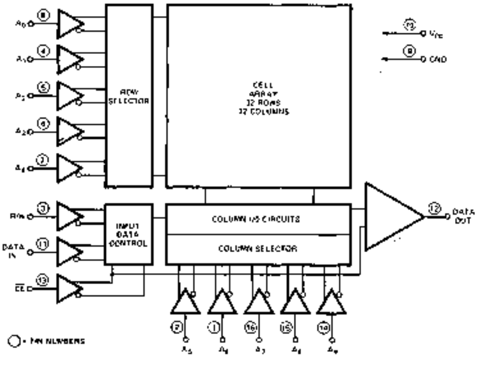
1024 BIT (1K x 1) STATIC MOS RAM



The 8102 is a 1024 word by 1 bit random access memory element with an access time of 1300ns.

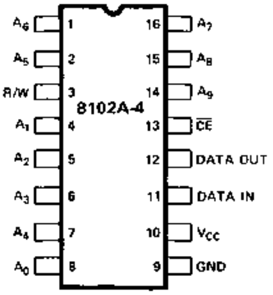
The 8102-2 has an access time of 850ns.

Both devices use DC stable (static) circuitry and require no clocks or refreshing to operate. Data is read out non-destructively and has the same polarity as the input data. They are designed for high performance, low cost microcomputer systems. They are TTL compatible in all respects. A separate chip enable ($\overline{CE}$) allows easy selection of packages when outputs are OR-tied.



8102A-4

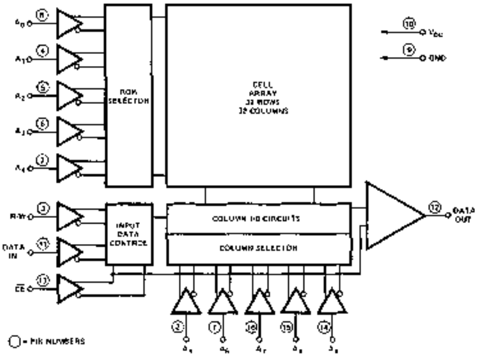
1024 BIT (1K x 1) STATIC MOS RAM



The 8102A-4 is a 1024 word by 1 bit random access memory element with an access time of 450ns.

The 8102A-4 may also be supplied in a power-down version with low standby power requirements.

The 8102A-4 uses DC stable (static) circuitry and requires no clocks or refreshing to operate. Data is read out non-destructively and has the same polarity as the input data. The device is TTL compatible in all respects. A separate chip enable ($\overline{CE}$) allows easy selection of packages when outputs are OR-tied.



8107A

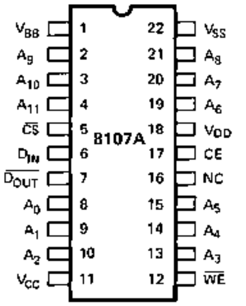
4096 BIT FULLY DECODED DYNAMIC RAM

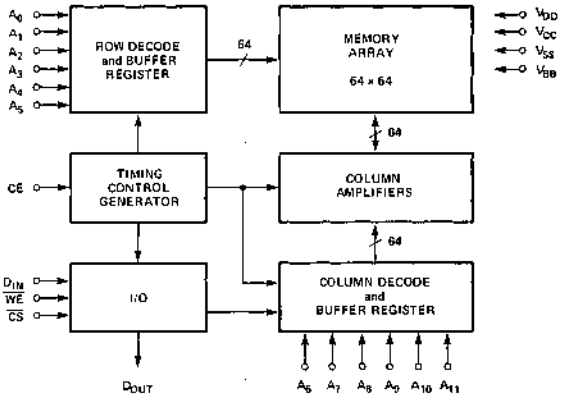
The Intel 8107A is a 4096 word by 1-bit dynamic n-channel MOS RAM.

The access time is 420 nanoseconds.

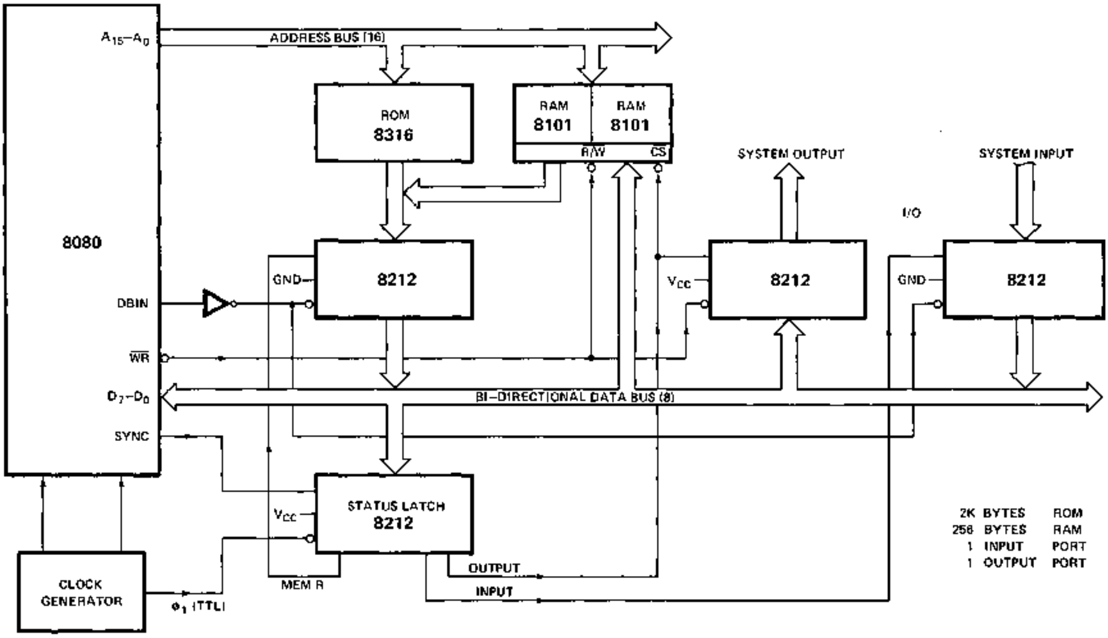
It was designed for memory applications where very low cost and large bit storage are important design objectives. The 8107A uses dynamic circuitry which reduces the operation and standby power dissipation.

Reading information from the memory is nondestructive. Refreshing is accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.





MINIMUM 8080 SYSTEM



8212

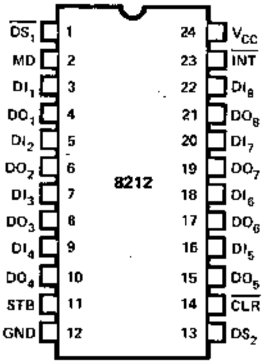
8-BIT INPUT/OUTPUT PORT

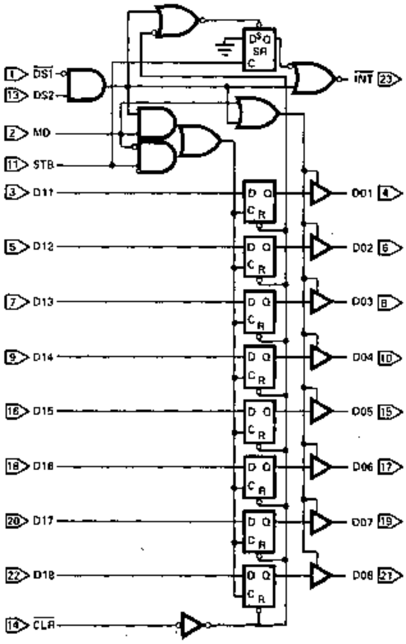
The 8212 input/output port consists of an 8-bit latch with tri-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

The 8212 requires only .25 μA input current, permitting direct connection to MOS data and address lines of Intel CPU's.

The high voltage (3.65V) output level provides direct interface with the 8008 or 8080 CPU.





8216

4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

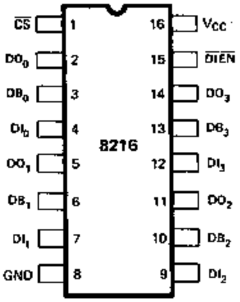
The 8216 is a 4-bit bi-directional bus driver/receiver.

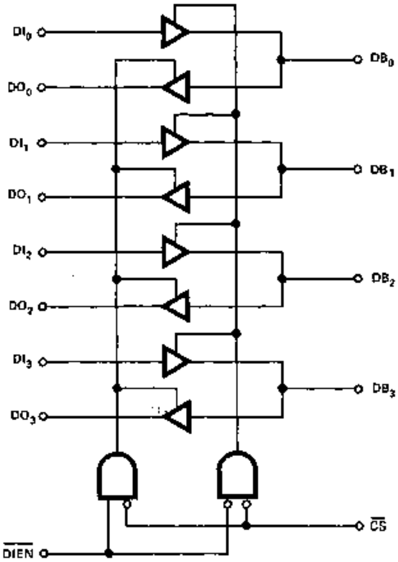
All inputs are low power TTL compatible.

For driving MOS, the DO outputs provide V_{OH} (3.65V), and for high capacitance terminated bus structures, the DB outputs provide a higher I_{OL} (50 mA) capability.

All outputs may be tri-stated.

The 8216 is ideal as the data bus buffer/driver for the 8080 CPU. It may also be used with other MCS CPUs.





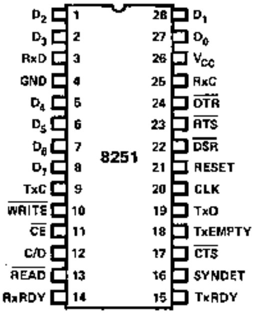
PRELIMINARY

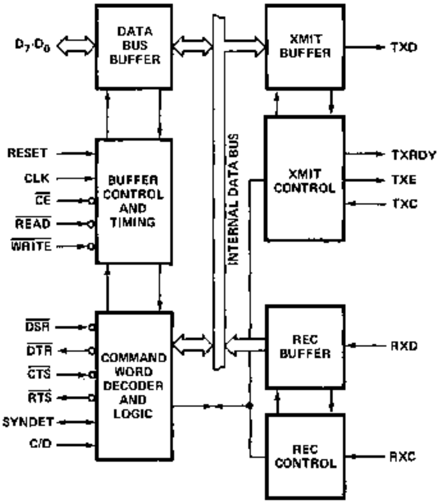
8251

UNIVERSAL COMMUNICATION INTERFACE

The 8251 is a Universal Synchronous/Asynchronous Transmitter/Receiver (USART) Chip that is designed for data communications in microcomputer systems. The USART is used as a peripheral device and it is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT.

The 8251 is fully compatible with the 8080 CPU and operates on a single +5V DC supply. It also requires only one TTL level clock. Error detection signals are supplied. Character synchronization and automatic SYNC insertion or deletion operating modes are possible.





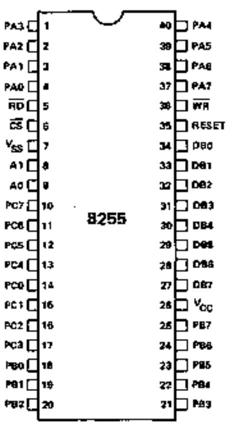
PRELIMINARY

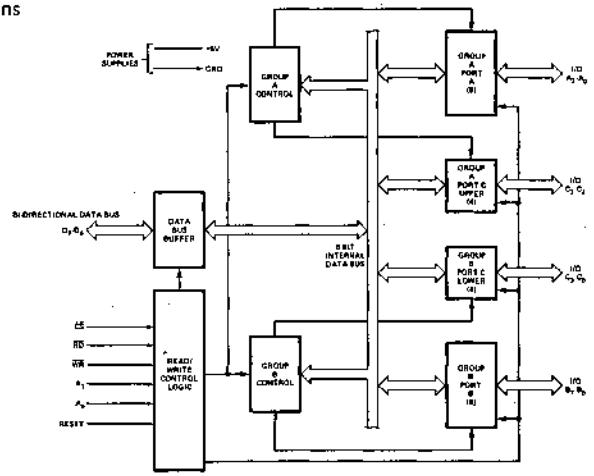
8255

PROGRAMMABLE PERIPHERAL INTERFACE

The 8255 is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255 include bit set and reset capability and the ability to source 1mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.





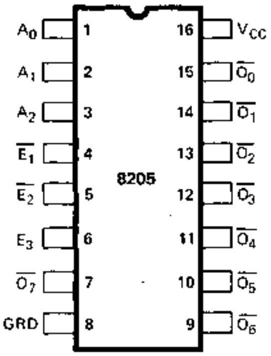
8205

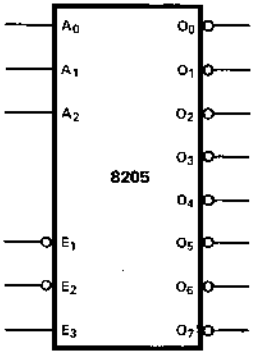
ONE OUT OF EIGHT DECODER

The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input.

When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory is selected. The 3 chip enable inputs on the 8205 allow easy system expansion.

For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.





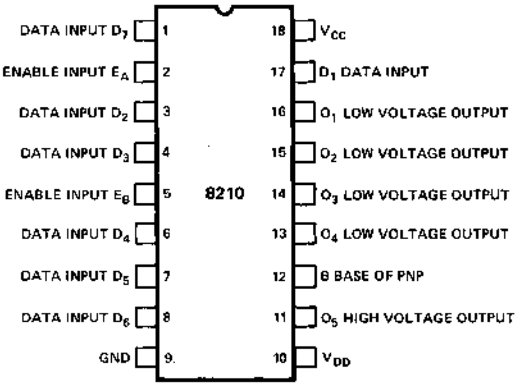
ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

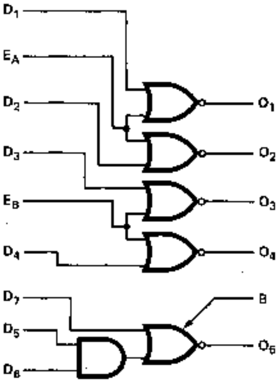
8210

TTL-TO-MOS LEVEL SHIFTER and HIGH VOLTAGE CLOCK DRIVER

The 8210 is a Bipolar-to-MOS level shifter and high voltage driver, each with current driving capabilities suitable for driving N-channel MOS memory devices. The 8210 is particularly suitable for driving the 8107A N-channel MOS memory chips. The 8210 operates from the 5 volt and 12 volt power supplies used to bias the memory devices. The four low voltage drivers feature two common enable inputs per pair of drivers which permits address or data decoding. The high voltage driver swings the 12 volts required to drive the chip enable (clock) input for the 8107A.

The 8210 high voltage driver requires an externally connected PNP transistor. The PNP base is connected to pin 12, the collector to pin 11, and the emitter to pin 10 or V_{DD}. The use of a fast switching, high voltage, high current gain PNP, like the 2N5057 is recommended.



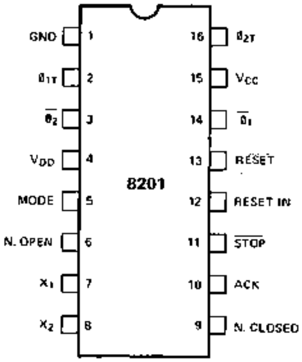


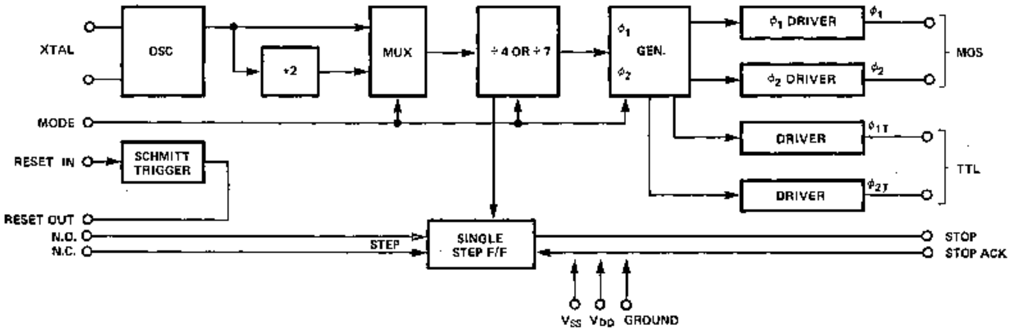
8201

CLOCK GENERATOR AND DRIVER FOR 8008 CPU

The 8201 generates the two phase clock signals used by the 8008 CPU. Both TTL and MOS level signals are available. Only an external crystal is required for the 8201.

A reset signal generator is also provided for power on or external reset requirements. The internal divider is selectable with the MODE line.





PRELIMINARY

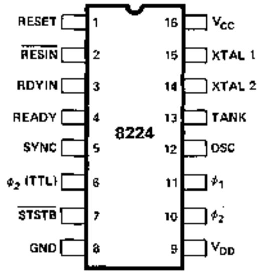
8224

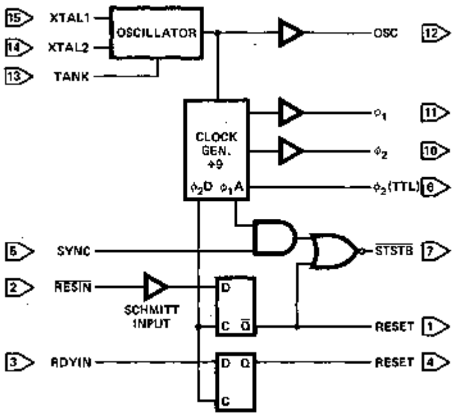
CLOCK GENERATOR AND DRIVER FOR 8080 CPU

The 8224 is a single chip clock generator/driver for the 8080 CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080.





8214

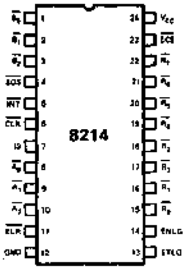
PRIORITY INTERRUPT CONTROL UNIT

The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

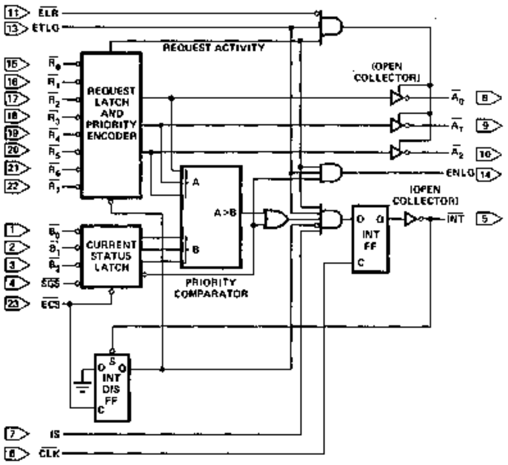
The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.



INPUTS	
$\overline{R_0\text{-}R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
$\overline{B_0\text{-}B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
IS	INTERRUPT STROBE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS:	
$\overline{A_0\text{-}A_2}$	REQUEST LEVELS } OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW) } OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP



8228

PRELIMINARY

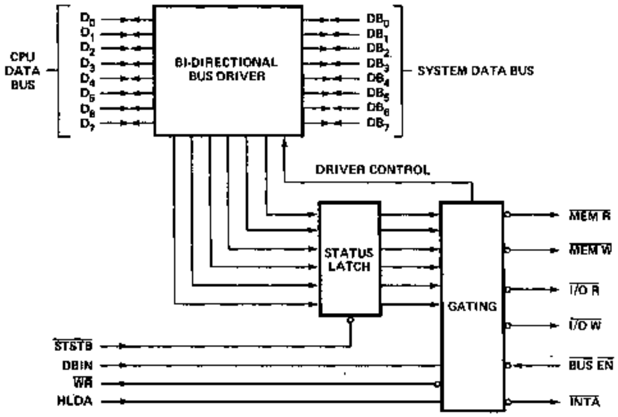
SYSTEM CONTROLLER AND BUS DRIVER FOR 8080 CPU

The 8228 is a single chip system controller and bus driver for MCS-80.™ It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of MCS-80 systems.



INTELLEC® 8 / MOD 8
MICROCOMPUTER DEVELOPMENT SYSTEM

- **Complete Hardware/Software Development System for the design and implementation of 8008 CPU based microcomputer systems.**
- **Front panel designer's console provides complete system control and monitoring functions.**
- **8K bytes of random access memory (RAM) expandable to 16K bytes.**
- **2K bytes of erasable and field programmable read only memory (PROM) expandable to 16K bytes.**
- **Self contained PROM programming facility with zero insertion force PROM socket.**
- **Four 8-bit input and four 8-bit output ports.**
- **Integral asynchronous serial data communications capability at 110, 1200, or 2400 baud.**
- **Discrete teletype interface (20mA current loop).**
- **Standard system software includes a PROM resident system monitor, RAM resident Macro-Assembler and RAM resident text editor.**
- **Expansion capability provided for up to 16 standard or custom designed microcomputer modules.**

The Intellec 8/MOD 8 (imm 8-80A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 8008 CPU based microcomputer systems. Its modular design facilitates the development of both large and small MCS-8 system.

The basic Intellec 8/MOD 8 consists of seven standard microcomputer modules (CPU, RAM, PROM, I/O, PROM Programmer, Front Panel Control) and power supplies enclosed in a finished table top cabinet. The heart of the system is the imm 8-82 central processor module built around Intel's 8008 p-channel 8-bit CPU on a single chip.

The Intellec® Development System directly supports up to 16K of memory, eight input ports, twenty-four output ports, and provides expansion capability for custom designed microcomputer modules within the system chassis.

The front panel designer's console provides an easy means of monitoring and controlling system operation, manually moving data to and from memory and input/output devices, setting hardware breakpoints, and executing or debugging programs.

The Intellec 8/MOD 8 has 10K bytes of memory in its basic configuration which can be expanded to 16K bytes within the system chassis. Of the basic 10K bytes of memory, 8K bytes are random access read/write memory located on two imm 6-28 RAM memory modules. This memory can be used for both data and program storage. The remaining 2K bytes of memory are located on the imm 6-26 PROM memory module and contain the Intellec 8/MOD 8 system monitor in eight Intel® 1702A erasable and field programmable read only memory chips. Eight additional sockets (2K bytes) are available on the imm 6-26 for expansion.

The PROM and RAM memory modules may be used in any combination to make up the 16K of directly addressable memory housed in the system chassis. Facilities are built into these modules so that combinations of RAM, ROM or PROM may be mixed in 256 byte increments.

The self-contained PROM programming module allows Intel® 1602A or 1702A PROMs to be programmed and verified directly from RAM or PROM memory.

INTELLEC® 8/MOD 80
MICROCOMPUTER DEVELOPMENT SYSTEM

- **Complete Hardware/Software Development System for the design and implementation of 8080 CPU based microcomputer systems.**
- **Front panel designer's console provides complete system control and monitoring functions.**
- **8K bytes of random access memory (RAM) expandable to 16K bytes.**
- **2K bytes of erasable and field programmable read only memory (PROM) expandable to 16K bytes.**
- **Self-contained PROM programming facility with zero insertion force PROM socket.**
- **Four 8-bit input and four 8-bit output ports.**
- **Integral asynchronous serial data communications capability at 110, 1200, or 2400 baud.**
- **Discrete teletype interface (20mA current loop).**
- **Standard system software includes a PROM resident system monitor, RAM resident macro-assembler and RAM resident text editor.**
- **Expansion capability provided for up to 16 standard or custom designed microcomputer modules.**

The Intellec 8/MOD 80 (imm 8-84A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 8080 CPU based microcomputer systems. Its modular design facilitates the development of both large and small MCS-80 systems.

The basic Intellec 8/MOD 8 consists of seven standard microcomputer modules (CPU, RAM, PROM, I/O, PROM Programmer, Front Panel Control) and power supplies enclosed in a finished table top cabinet. The heart of the system is the imm 8-83 central processor module built around Intel's 8080 high performance n-channel 8-bit CPU on a single chip.

The Intellec Development System directly supports up to 16K of memory, four to sixteen input ports, four to twenty-eight output ports, and provides expansion capability for custom designed microcomputer modules within the system chassis.

External expansion enclosures may be designed to support up to 64K of memory, 256 input ports and 256 output ports.

The front panel designer's console provides an easy means of monitoring and controlling system operation, manually moving data to and from memory and input/output devices, setting hardware breakpoints, and executing or debugging programs.

The Intellec 8/MOD 80 has 10K bytes of memory in its basic configuration which can be expanded to 16K bytes within the system chassis. Of the basic 10K bytes of memory, 8K bytes are random access read/write memory located on two imm 6-28 RAM memory modules. This memory can be used for both data and program storage. The remaining 2K bytes of memory are located on the imm 6-26 PROM memory module and contain the Intellec 8/MOD 80 system monitor in eight Intel 1702A erasable and field programmable read only memory chips. Eight additional sockets (2K bytes) are available on the imm 6-26 for expansion.

The PROM and RAM memory modules may be used in any combination to make up the 16K of directly addressable memory housed in the system chassis. Facilities are built into these modules so that combinations of RAM, ROM or PROM may be mixed in 256 byte increments.

The self-contained PROM programming module allows Intel® 1602A or 1702A PROMs to be programmed and verified directly from RAM or PROM memory.

imm8-90

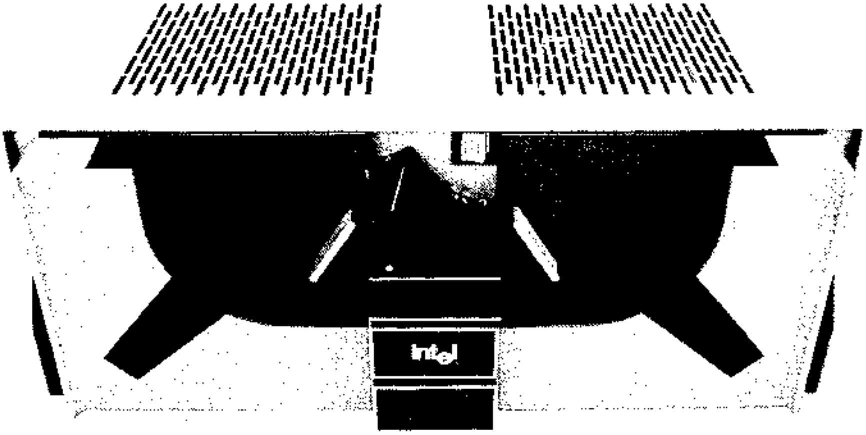
INTELLEC® 8 HIGH SPEED PAPER TAPE READER

- **TAPE MOVEMENT**
  Tape Reading Speed:
  0 to 200 characters per second asynchronous
  Tape Stopping:
  Stops "On Character"
- **TAPE CHARACTERISTICS**
  Tapes must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.
  Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 57% (oiled buff paper tape).
  Tape loading: in line
  Tape width: 1 inch
- **ELECTRICAL CHARACTERISTICS**
  AC Power Requirement:
  3 wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.
- **EQUIPMENT SUPPLIED**
  Paper Tape Reader
  Reader Cable
  Reader Flat Cable
  Fanfold Tape Guide
  Fanfold Paper Tape
  Hardware Manual
  Installation and Operations Guide
  Fanfold Guide Installation Instructions

NOTE: Version 2 software must be used when operating with Intellec® 8/Mod 8 Microcomputer Development System.

The imm8-90 high speed paper tape reader provides all Intellec 8 Microcomputer Development Systems with a high speed paper tape input that is over twenty times faster than the standard ASR-33 teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.

The Intellec 8 monitor software provides two key capabilities which significantly enhance the systems performance of the imm8-90. A general purpose paper tape reader driver is included in the Intellec 8 Monitor. It enables all systems software to utilize the high speed reader features and is callable by user written application programs. The monitor also provides dynamic I/O reconfiguration permitting instantaneous reassignment of physical devices to logical devices.



MICROCOMPUTER MODULES

MCS-4/40™

Modules may be ordered individually. All modules are 8" wide, 6.18" high and use standard 100-pin connectors.

imm4-42 Central Processor Module

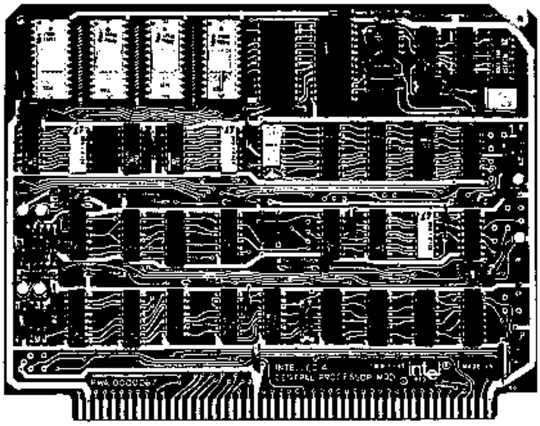
- This is a complete microcomputer system with the processor, program storage, data storage, and I/O in a single module.
- The heart of this module is Intel's 4004 single chip four-bit parallel processor — p-channel silicon gate MOS.
- Accumulator and sixteen working registers (4-bit).
- Subroutine nesting up to 3 levels.
- For development work, the CPU interfaces to standard semiconductor memory elements (provided by Intel's standard memory and I/O interface set 4008/4009).
- Sockets for 1K bytes of PROM (Intel 1702A PROM) are provided.
- 320 words (4-bit) of data storage (Intel 4002) are provided.
- Four 4-bit input ports and eight 4-bit output ports (includes TTY interface).
- Bus-oriented expansion of memory and I/O.
- Two phase crystal clock.

imm4-43 Central Processor Module

- Complete microcomputer system with Intel's high performance 4040 4-bit processor, program storage, data storage, I/O and system clock in a single module.
- 60 instructions including decimal arithmetic, register-to-register transfers, conditional branching, logical operations and I/O.
- Interrupt capability.
- Single step capability.
- 24 index registers.
- Subroutine nesting to 7 levels.
- Direct interface capability to all standard memories (i.e., TTL, NMOS, PMOS, CMOS) through Intel's 4289 Standard Memory Interface chip.
- Sockets for 1K x 8 bytes of program memory (Intel 4702A PROM) expandable to 4K x 8 using optional imm6-26 or imm4-24 modules.
- 320 4-bit bytes of data storage (Intel 4002) expandable to 2560 x 4 using optional imm4-22 or imm4-24 modules.
- Four 4-line input ports and eight 4-line output ports expandable to 16 input and 48 output ports using optional imm4-60, imm4-22 or imm4-24 modules.
- Two phase crystal clock.

imm4-22 Instruction/Data Storage Module

- This microcomputer module has memory capacity identical to the Central Processor Module and is used for expanding memory and I/O.
- Sockets for 1K bytes of PROM program storage are provided.
- 320 words (4-bit) of data storage are provided.
- Four 4-bit input ports and eight 4-bit output ports.



imm4-42 Central Processor Module

imm4-24 Data Storage Module

- This microcomputer module has capacity for sixteen Intel 4002 RAMS — 1280 words (4-bit) of data storage.
- 320 words (4-bit) of data storage are provided.
- A maximum Intellec 4 system may contain up to 2560 words of storage — decoding for this expansion is provided.
- A 4-bit output port is associated with each RAM on this microcomputer module providing sixteen 4-bit output ports on each module.
- All output ports are TTL compatible.

imm4-60 Input/Output Module

- This module provides input and output port expansion without additional memory.
- Eight 4-bit input ports and eight 4-bit output ports are provided.
- Ports on this module are TTL compatible.

MICROCOMPUTER MODULES

MCS-8™

imm8-82 Central Processor Module

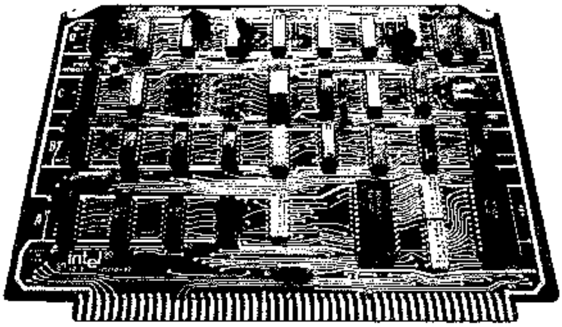
- Intel's 8080-1 eight-bit parallel single chip CPU — p-channel silicon gate MOS.
- Accumulator and six 8-bit working registers.
- Subroutine nesting up to seven levels.
- Interface to 16K 8-bit bytes of PROM, ROM, or RAM via the PROM Memory Module and RAM Memory Module.
- Interface for expansion to eight 8-bit input ports and twenty-four 8-bit output ports, via the I/O and Output Modules.
- Interrupt capability.
- Two phase crystal clock.
- All module interfaces are TTL compatible.

imm8-60 Input/Output Module

- Four 8-bit input ports (32 lines).
- Four 8-bit data latching output ports (32 lines).
- One pair of ports for TTY communication.
- All input and output ports are TTL compatible.

imm8-62 Output Module

- Eight 8-bit data latching output ports (64 lines).
- All output ports are TTL compatible.



imm8-82 Central Processor Module

MCS-80™

imm8-83 CPU Module

- Complete 8-bit parallel central processor module with system clocks, interface and control for memory, I/O ports, and real time interrupt.
- Utilizes Intel's high performance 8080 single chip n-channel microcomputer.
- 2.5 μsecond instruction execution time.
- 78 basic instructions including the entire 8008 instruction set.
- Direct addressing of up to 64K bytes of any speed ROM, PROM, or RAM memory.
- Unlimited subroutine nesting.
- Seven working registers — six 8-bit general purpose registers and an 8-bit accumulator.
- Separate 16-bit address bus, 8-bit output bus and 3 multiplexed 8-bit input busses for I/O input, memory input and interrupt data.
- Direct addressing of 256 input and 256 output ports.
- Multiple level real time interrupt capability.
- Direct memory access capability.
- All buses TTL compatible.

imm8-61 I/O Module

- Four 8-bit input and four 8-bit latching output ports.
- Directly compatible with imm8-83 central processor module.
- Integral asynchronous serial data communications capability and teletype interface.
- Jumper selectable transmission rates of 110, 1200 or 2400 baud.
- Crystal controlled clock.
- Capable of high speed serial communications to 9600 baud.
- TTL compatible.

imm8-63 Output Module

- Eight 8-bit latching output ports.
- Directly compatible with imm8-83 central processor module.
- Decoding provided for the selection of up to 256 individual output ports.
- TTL compatible.

MICROCOMPUTER MODULES

COMMON SYSTEM MODULES

imm6-26 PROM Memory Module

- Provides sockets for up to sixteen 1702A electrically programmable and erasable PROMs for a system's fixed program memory (maximum 4K bytes/module).
- For volume requirements, Intel 2048-bit mask programmed MOS ROMs (1302) may be substituted in the same module.

imm6-28 RAM Memory Module

- A 4K x 8 n-channel MOS memory system using Intel's 1024-bit Static RAM (2102).
- Address latching, data latching, and module select decoding are provided on the card.
- Provides program storage for up to 4K instructions.

imm6-70 Universal Prototype Module

- Accommodates 14, 16, 24, or 40 pin wire wrap sockets (maximum of 52 16-pin sockets).
- Provides breadboard capability for developing custom and specialized interface circuits.

imm6-72 Module Extender

- Extends Intellec modules out of card chassis for ease in test and system debugging.

imm6-76 PROM Programmer Module

- Provides all timing and level shifting circuitry for programming Intel's programmable and erasable 1702A PROMs.

CONVERSION KITS

imm4-88

The imm4-88 conversion kit provides an upgrade path for Intellec®4/MOD 4 microcomputer development systems. It includes all the hardware and software required to fully support 4040 CPU based microcomputer system development.

The conversion kit contains an imm4-43 CPU module, new memory controller, new front panel, and any software required.

NOTE: Due to necessary wiring changes, these conversions are done at the Intel factory. Contact local Intel salesmen or representatives for instructions.

imm8-88

The imm8-88 conversion kit provides an upgrade path for Intellec®8/MOD 8 microcomputer development systems. It includes all the hardware and software products required to fully support 8080 CPU based microcomputer system development. With the imm8-88 conversion kit installed in an Intellec 8/MOD 8, complete 8080 CPU hardware and software development capability is provided.

The conversion kit is installed by simply plugging in the three new hardware modules in the appropriate Intellec 8/MOD 8 chassis connectors and installing the new system monitor. The system can be quickly reconfigured to support 8080 CPU chip development by replacing the original boards and system monitor.

BAREBONES SYSTEMS

imm8-81 Barebones 8

- Complete 8008 CPU based microcomputer subsystem composed of Intel microcomputer modules which are housed in a card cage and interconnected by a printed circuit backplane with card sockets.
- Contains the following modules:*
  - imm8-82 Central Processor Module
  - imm6-26 PROM Memory Module
  - imm6-28 RAM Memory Module (4K Bytes)
  - imm8-60 I/O Module
- 12 additional sockets available for optional modules.
- Rack mountable chassis.

imm8-85 Barebones 80

Same as 8-81 except the following modules are used:*

imm8-83 Central Processor Module
imm6-26 PROM Memory Module
imm6-28 RAM Memory Module (4K Bytes)
imm8-61 I/O Module

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*See page 6-47 for module descriptions.

MCS PROTOTYPE SYSTEMS

Intel distributors are now stocking five new systems which enable even more companies to take advantage of the benefits of microcomputers at very low cost. The systems may be used to prototype products and will make low volume manufacturing more economical.

These prototype systems provide the designer with a wide range of price and performance choices . . . from lowest cost to highest performance. Additional prototype systems will be offered as newer microcomputer components are developed.

System Number	System Composition
MCS-80 System A	1 Model 8080 CPU 8 Model 8107A, 4096 x 1 Dynamic RAMs 8 Model 8212, Bipolar 8-bit I/O ports 1 Model 8702A, 256 x 8 PROM
MCS-80 System B	1 Model 8080 CPU 8 Model 8102-2, 1024 x 1 Static N-Channel RAMs 8 Model 8212, Bipolar 8-bit I/O ports 1 Model 8702A, 256 x 8 PROM
MCS-8 System A	1 Model 8008-1 CPU 8 Model 8102, 1024 x 1 Static RAMs 8 Model 8212, 8-bit I/O Latches 1 Model 8205, 1-Of-8 Decoder 1 Model 8702A-4, 256 x 8 PROM
MCS-40 System A	1 Model 4040 CPU 1 Model 4002-1, 320-bit RAM and 4-bit output port 1 Model 4003, Shift Register 1 Model 4289, Standard Memory and I/O Interface 1 Model 4702A, 2048-bit electrically Programmable ROM
MCS-4 System A	1 Model 4004 CPU 1 Model 4002-1, 320-bit RAM and 4-bit output port 1 Model 4003, Shift Register 1 Model 4008, Standard Memory and I/O Interface Set 1 Model 4009, Standard Memory and I/O Interface Set 1 Model 4702A, 2048-bit electrically Programmable ROM

CROSS PRODUCT SOFTWARE

The following support software is written in ANSI Standard FORTRAN IV and will execute on most large scale computer systems which have a FORTRAN IV Compiler and a minimum 32-bit integer format. The FORTRAN IV source code of each program is shipped on magnetic tape in the following format:

9 TRACK
800 BPI
80 Byte unblocked records
EBCDIC character code
unlabeled tape

These software products are also available on the following timesharing services:

Tymshare	U.S., U.K., France
General Electric	U.S., Canada
United Computing Systems	U.S.
Honeywell	Europe, Australia
Dentsu	Japan
Timesharing LTD.	U.K., Belgium

Contact each timesharing service for further information.

Product	Description
MCS-4	
MAC 4™	Macro Assembler – Translates symbolic assembly language into MCS-4 machine code.
SIM 4	Simulator – Simulates execution of the 4004 CPU including execution of all 46 instructions and I/O operations.
MCS-40	
MAC 4™	Macro Assembler – Translates symbolic assembly language into MCS-40 machine code.
MCS-8	
MAC 8™	Macro Assembler – Translates symbolic assembly language into MCS-8 machine code.
INTERP/8	Simulator – Simulates execution of the 8008 CPU including execution of all 48 instructions and I/O operations.
PL/M™8	High-level Systems Language Compiler – Translates a source program written in PL/M, Intel's systems programming language, into MCS-8 machine code.
MCS-80	
MAC 80™	Macro Assembler – Translates symbolic assembly language into MCS-80 machine code.
INTERP/80	Simulator – Simulates execution of the 8080 CPU including execution of all 78 instructions, I/O operations, the stack and interrupt systems.
PL/M™80	High-level Systems Language Compiler – Translates a source program written in PL/M, Intel's systems programming langauge, into MCS-80 machine code.

INTELLEC® RESIDENT SOFTWARE

System Monitor

- PROM resident for instant operation
- Manual or paper tape loading of programs
- Program Execution from RAM or PROM
- Alteration and display of RAM memory
- PROM programming and listing
- BNPF or HEX format paper tape
- Alteration and display of CPU registers (MOD 80 only)
- CPU breakpoint capability (MOD 80 only)

Assembler

The assembler translates symbolic assembly language into machine code:

- Built-in paper tape editor (MOD 4 and MOD 40)
- Provides source listing with address
- Error messages
- Hexadecimal output format
- 3 Pass assembler
- Full macro capability (MOD 8 and MOD 80 only)
- Conditional assembly capability (MOD 8 and MOD 80 only)
- Compatible with cross assemblers

Text Editor

The text editor provides powerful features for creation and correction of programs.

Editor includes following commands:

string search
substitution
insertion
deletion

Intellec	System Monitor	Assembler	Text Editor
4/MOD 4	X	X	
4/MOD 40	X	X	
8/MOD 8	X	X	X
8/MOD 80	X	X	X

MCS USER'S LIBRARY

Intel supports a Microcomputer User's Library for each of its 4004/4040 and 8008/8080 CPU's. Members of each library receive a manual containing documentation for each program in the library. Members also receive updates quarterly on new programs as they are received.

Each manual contains a program index, a brief description of each program, and a complete assembly language and hex code listing. All program documentation is supplied in the same format. User contributed programs are invited and submittal forms are available from Intel. Memberships are available free of charge to all accepted contributors. Contact Intel for full details.

A partial listing of programs already in these libraries is given below.

4004/4040

- Cross Assembler for PDP-8
- BNPF Tape Generator for PDP-8
- MCS-4 Simulator for PDP-8
- Chebyshev Approximation Functions
- Parity Checker/Generator
- Delay Subroutines
- Cross Assembler for NOVA
- Bit Manipulation Routine

8008/8080

- Floating Point Arithmetic Package
- Floating Point I/O Conversion Package
- 8-Bit Multiply
- 8-Bit Divide
- 16-Bit Multiply
- 16-Bit Divide
- Signed 16-Bit Multiply
- PROM Programming Routine
- 24-Bit Multiply
- Quicksort

BIPOLAR MICROPROCESSOR

A family architecture

To reduce component count as far as practical, a multi-chip LSI microcomputer set must be designed as a complete, compatible family of devices. The omission of a bus or a latch or the lack of drive current can multiply the number of miscellaneous SSI and MSI packages to a dismaying extent—witness the reputedly LSI minicomputers now being offered which need over a hundred extra TTL packages on their processor boards to support one or two custom LSI devices. Successful integration should result in a minimum of extra packages, and that includes the interrupt and the input/output systems.

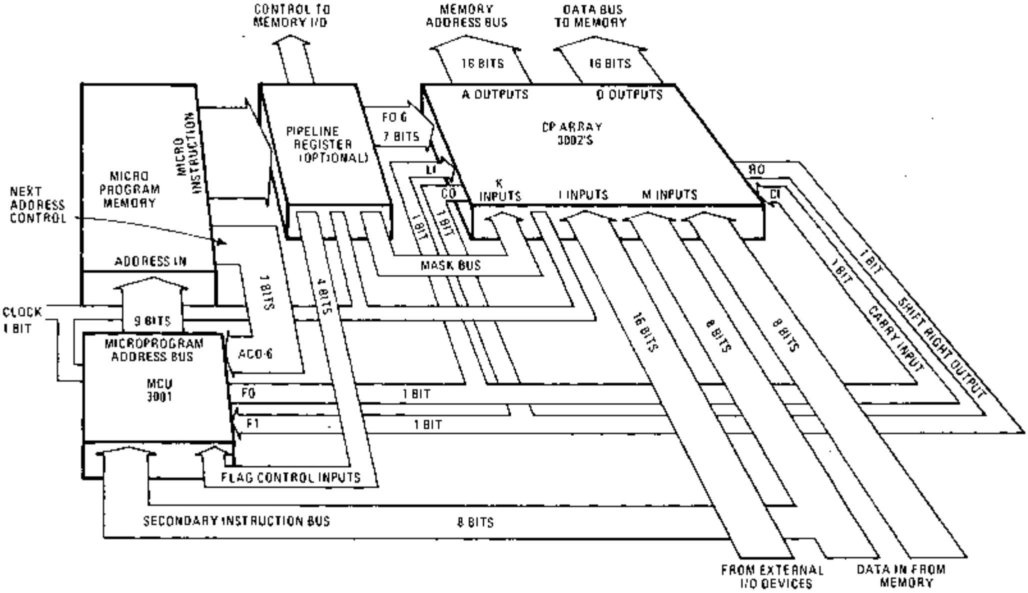
With this objective in mind, the Intel Schottky bipolar LSI microcomputer chip set was developed. Its two major components, the 3001 Microprogram Control Unit (MCU) and the 3002 Central Processing Element (CPE), may be combined by the digital designer with standard bipolar LSI memory to construct high-performance controller-processors (Fig. 1) with a minimum of ancillary logic.

Among the features that minimize package count and improve performance are: the multiple independent data and address busses that eliminate time multiplexing and the need for external latches; the three-state output buffers with high fanout that make bus drivers unnecessary except in the largest systems, and the separate output-enable logic that permits bidirectional busses to be formed simply by connecting inputs and outputs together.

Each CPE represents a complete two-bit slice through the data-processing section of a computer. Several CPEs may be arrayed in parallel to form a processor of any desired word length. The MCU, which together with the microprogram memory, controls the step-by-step operation of the processor, is itself a powerful microprogramed state sequencer.

Enhancing the performance and capabilities of these two components are a number of compatible computing elements. These include a fast look-ahead carry generator, a priority interrupt unit, and a multimode latch buffer. A complete summary of the first available members of this family of LSI computing elements and memories is given in the table on this page.

3001	Microprogram control unit
3002	Central processing element
3003	Look-ahead carry generator
3212	Multimode latch buffer
3214	Priority interrupt unit
3216	Noninverting bidirectional bus driver
3226	Inverting bidirectional bus driver
3601	256-by-4-bit programable read-only memory
3604	512-by-8-bit programable read-only memory
3301A	256-by-4-bit read-only memory
3304A	512-by-8-bit read-only memory



1. Bipolar microcomputer. Block diagram shows how to implement a typical 16-bit controller-processor with new family of bipolar computer elements. An array of eight central processing elements (CPEs) is governed by a microprogram control unit (MCU) through a separate read-only memory that carries the microinstructions for the various processing elements. This ROM may be a fast, off-the-shelf unit.

CPEs form a processor

Each CPE (Fig. 2) carries two bits of five independent busses. The three input busses can be used in several different ways. Typically, the K-bus is used for microprogram mask or literal (constant) value input, while the other two input busses, M and I, carry data from external memory or input/output devices. D-bus outputs are connected to the CPE accumulator; A-bus outputs are connected to the CPE memory address register. As the CPEs are wired together, all the data paths, registers, and busses expand accordingly.

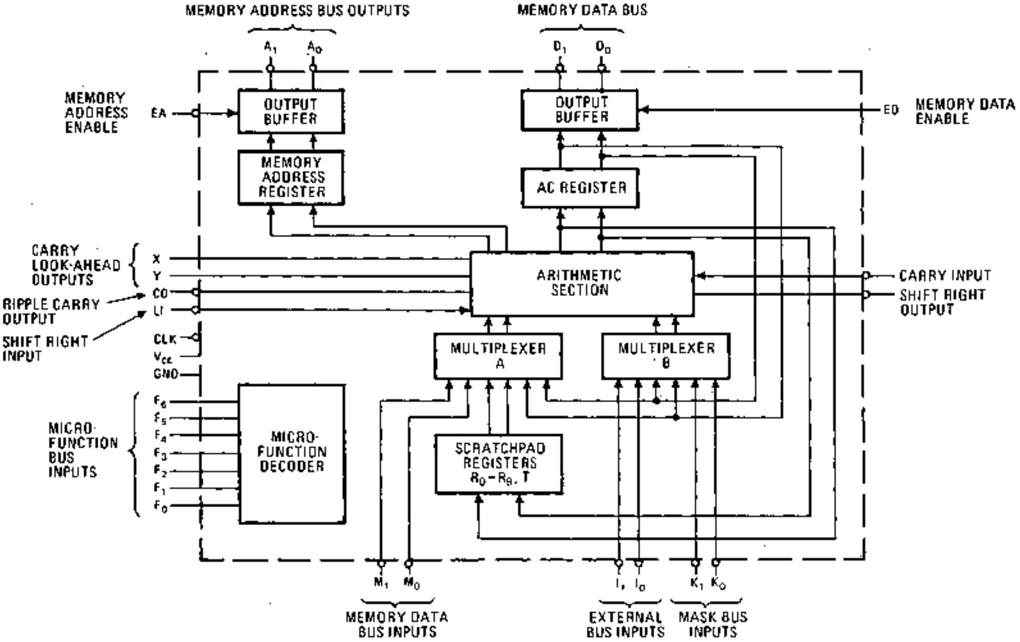
Certain data operations can be performed simply by connecting the busses in a particular fashion. For example, a byte exchange operation, often used in data-communications processors, may be carried out by wiring the D-bus outputs back to the I-bus inputs, exchanging the high-order outputs and low-order inputs. Several other discretionary shifts and rotates can be accomplished in this manner.

A sixth CPE bus, the seven-line microfunction bus, controls the internal operation of the CPE by selecting the operands and the operation to be performed. The arithmetic function section, under control of the microfunction bus decoder, performs over 40 Boolean and binary functions, including 2's complement arithmetic and logical AND, OR, NOT, and exclusive-NOR. It increments, decrements, shifts left or right, and tests for zero.

Unlike earlier MSI arithmetic-logic units, which contain many functions that are rarely used, the microfunction decoder selects only useful CPE operations. Standard carry look-ahead outputs, X and Y, are generated by the CPE for use with available look-ahead devices or the Intel 3003 Look-ahead Carry Generator. Independent carry input, carry output, shift input, and shift output lines are also available.

What's more, since the K-bus inputs are always ANDed with the B-multiplexer outputs into the arithmetic function section, a number of useful functions that in conventional MSI ALUs would require several cycles are generated in a single CPE microcycle. The type of bit masking frequently done in computer control systems can be performed with the mask supplied to the K-bus directly from the microinstruction.

Placing the K-bus in either the all-one or all-zero state will, in most cases, select or deselect the accumulator in the operation, respectively. This toggling effect of the K-bus on the accumulator nearly doubles the CPE's repertoire of microfunctions. For instance, with the K-bus in the all-zero state, the data on the M-bus may be complemented and loaded into the CPE's accumulator. The same function selected with the K-bus in the all-one state will exclusive-NOR the data on the M-bus with the accumulator contents.



2. Central processing element. This element contains all the circuits representing a two-bit-wide slice through a small computer's central processor. To build a processor of word width N, all that's necessary is to connect an array of N/2 CPEs together.

Three innovations

The power and versatility of the CPE are increased by three rather novel techniques. The first of these is the use of the carry lines and logic during non-arithmetic operations for bit testing and zero detection. The carry circuits during these operations perform a word-wide logical OR (ORing adjacent bits) of a selected result from the arithmetic section. The value of the OR, called the carry OR, is passed along the carry lines to be ORed with the result of an identical operation taking place simultaneously in the adjacent higher-order CPE.

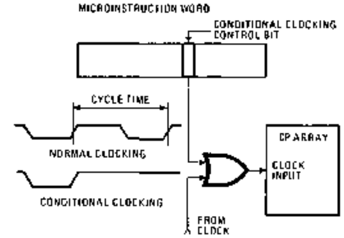
Obviously, the presence of at least one bit in the logical 1 state will result in a true carry output from the highest-order CPE. This output, as explained later, can be used by the MCU to determine which microprogram sequence to follow. With the ability to mask any desired bit, or set of bits, via the K-bus inputs included in the carry OR, a powerful bit-testing and zero-detection facility is realized.

The second novel CPE feature is the use of three-state outputs on the shift right output (RO) and carry output (CO) lines. During a right shift operation, the CO line is placed in the high-impedance (Z) state, and the shift data is active on the RO line. In all other CPE operations, the RO line is placed in the Z state, and the carry data is active on the CO line. This permits the CO and RO lines to be tied together and sent as a single rail input to the MCU for testing and branching. Left shift operations utilize the carry lines, rather than the shift lines, to propagate data.

The third novel CPE capability, called conditional clocking, saves microcode and microcycles by reducing the number of microinstructions required to perform a given test. One extra bit is used in the microinstruction to selectively control the gating of the clock pulse to the central processor (CP) array. Momentarily freezing the clock (Fig. 3) permits the CPE microfunction to be performed, but stops the results from being clocked into the specified registers. The carry or shift data that results from the operation is available because the arithmetic section is combinatorial, rather than sequential. The data can be used as a jump condition by the MCU and in this way permits a variety of nondestructive tests to be performed on register data.

Microprogram control

The classic form of microprogram control incorporates a next-address field in each microinstruction—any other approach would require some type of program counter. To simplify its logic, the MCU (Fig. 4) uses the classic approach and requires address control information from each microinstruction. This information is not, however, simply the next microprogram address. Rather, it is a highly encoded specification of the next address and one of a set of conditional tests on the MCU bus inputs and registers.



3. Conditional clock. This feature permits an extra bit in microinstruction to selectively control gating of clock pulse to CP array. Carry or shift data thus made available permits tests to be performed on data with fewer microinstructions.

The next-address logic and address control functions of the MCU are based on a unique scheme of memory addressing. Microprogram addresses are organized as a two-dimensional array or matrix. Unlike in ordinary memory, which has linearly sequenced addresses, each microinstruction is pinpointed by its row and column address in the matrix. The 9-bit microprogram address specifies the row address in the upper 5 bits and the column address in the lower 4 bits. The matrix can therefore contain up to 32 row addresses and 16 column addresses for a total of 512 microinstruction addresses.

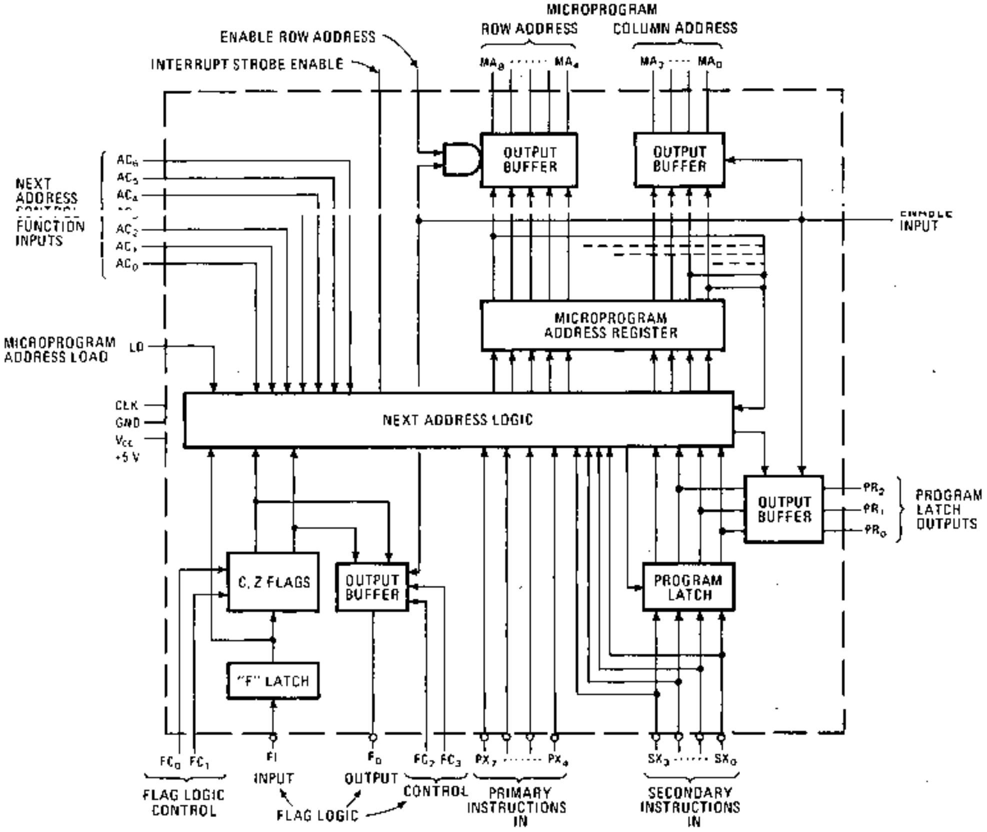
The next-address logic of the MCU makes extensive use of this addressing scheme. For example, from a particular row or column address, it is possible to jump either unconditionally to any other location in that row or column or conditionally to other specified locations, all in one operation. For a given location in the matrix there is a fixed subset of microprogram addresses that may be selected as the next address. These are referred to as a jump set, and each type of MCU address control jump function has a jump set associated with it.

Incorporating a jump operation in every microinstruction improves performance by allowing processing functions to be executed in parallel with program branches. Reductions in microcode are also obtained because common microprogram sequences can be shared without the time-space penalty usually incurred by conditional branching.

Independently controlled flag logic in the MCU is available for latching and controlling the value of the carry and shift inputs to the CP array. Two flags, called C and Z, are used to save the state of the flag input line. Under microprogram control, the flag logic simultaneously sets the state of the flag output line, forcing the line to logical 0, logical 1, or the value of the C or Z flag.

The jump decisions are made by the next-address logic on the basis of: the MCU's current microprogram address; the address control function on the accumulator inputs; and the data that's on the macroinstruction (X) bus or in the program latch or in the flags. Jump decisions may also be based on the instantaneous state of the flag input line without loading the value in one of the flags. This feature eliminates many extra microinstructions that would be required if only the flag flip-flop could be tested.

Microinstruction sequences are normally selected by the operation codes (op codes) supplied by the microinstructions, such as control commands or user instructions in main memory. The MCU decodes these commands by using their bit patterns to determine which is to be the next microprogram address. Each decoding results in a 16-way program branch to the desired microinstruction sequence.



4. **Microprogram control unit.** The MCU's two major control functions include controlling the sequence of microprograms fetched from the microprogram memory, and keeping track of the carry inputs and outputs of the CP array by means of the flag logic control.

Cracking the op codes

For instance, the MCU can be microprogramed to directly decode conventional 8-bit op codes. In these op codes the upper 4 bits specify one of up to 16 instruction classes or address modes, such as register, indirect, or indexed. The remaining bits specify the particular subclass such as ADD, SKIP IF ZERO, and so on. If a set of op codes is required to be in a different format, as may occur in a full emulation, an external pre-decoder, such as ROM, can be used in series with the X-bus to reformat the data for the MCU.

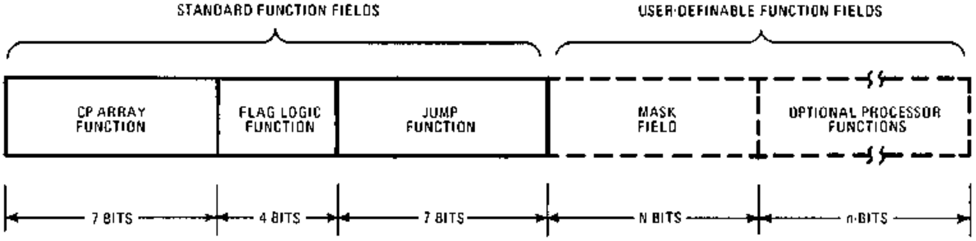
In rigorous decoding situations where speed or space is critical, the full 8-bit macroinstruction bus can be used for a single 256-way branch. Pulling down the load line of the MCU forces the 8 bits of data on the X-bus (typically generated by a predecoder) directly into the microprogram address register.

The data thus directly determines the next microprogram address which should be the start of the desired microprogram sequence. The load line may also be used by external logic to force the MCU, at power-up, into the system re-initialization sequence.

From time to time, a microprocessor must examine the state of its interrupt system to determine whether an interrupt is pending. If one is, the processor must suspend its normal execution sequence and enter an interrupt sequence in the microprogram. This requirement is handled by the MCU in a simple but elegant manner.

When the microprogram flows through address row 0 and column 15, the interrupt strobe enable line of the MCU is raised. The interrupt system, an Intel 3214 Interrupt Control Unit, responds by disabling the row address outputs of the MCU via the enable row address line, and by forcing the row entry address of the microprogram interrupt sequence onto the row address bus. The operation is normally performed just before the macroinstruction fetch cycle, so that a macroprogram is interrupted between, not during, macroinstructions.

The 9-bit microprogram address register and address bus of the MCU directly address 512 microinstructions. This is about twice as many as required by the typical 16-bit disk-controller or central processor.



5. Microinstruction format. Only a generalized microinstruction format can be shown since allocation of bits for the mask field and optional processor functions depends on the wishes of the designer and the tradeoffs he decides to make.

Moreover, multiple 512 microinstruction memory planes can easily be implemented simply by adding an extra address bit to the microinstruction each time the number of extra planes is doubled. Incidentally, as the number of bits in the microinstruction is increased, speed is not reduced. The additional planes also permit program jumps to take place in three address dimensions instead of two.

Because of the tremendous design flexibility offered by the Intel computing elements, it is impossible to describe every microinstruction format exactly. But generally speaking, the formats all derive from the one in Fig. 5. The minimum width is 18 bits: 7 bits for the address control functions, plus 4 bits for the flag logic control; plus 7 bits for the CPE microfunction control.

More bits can be added to the microinstruction format to provide such functions as mask field input to the CP array, external memory control, conditional clocking, and so on. Allocation of these bits is left to the designer who organizes the system. He is free to trade off memory costs, support logic, and microinstruction cycles to meet his cost/performance objectives.

Microprograming technology

- **Microprogram:** A type of program that directly controls the operation of each functional element in a microprocessor.
- **Microinstruction:** A bit pattern that is stored in a microprogram memory word and specifies the operation of the individual LSI computing elements and related subunits, such as main memory and input/output interfaces.
- **Microinstruction sequence:** The series of microinstructions that the microprogram control unit (MCU) selects from the microprogram to execute a single macroinstruction or control command. Microinstruction sequences can be shared by several macroinstructions.
- **Macroinstruction:** Either a conventional computer instruction (e.g. ADD MEMORY TO REGISTER, INCREMENT, and SKIP, etc.) or device controller command (e.g., SEEK, READ, etc.).

The cost/performance spectrum

The total flexibility of the Intel LSI computing elements is demonstrated by the broad cost/performance spectrum of the controllers and processors that can be constructed with them. These include:

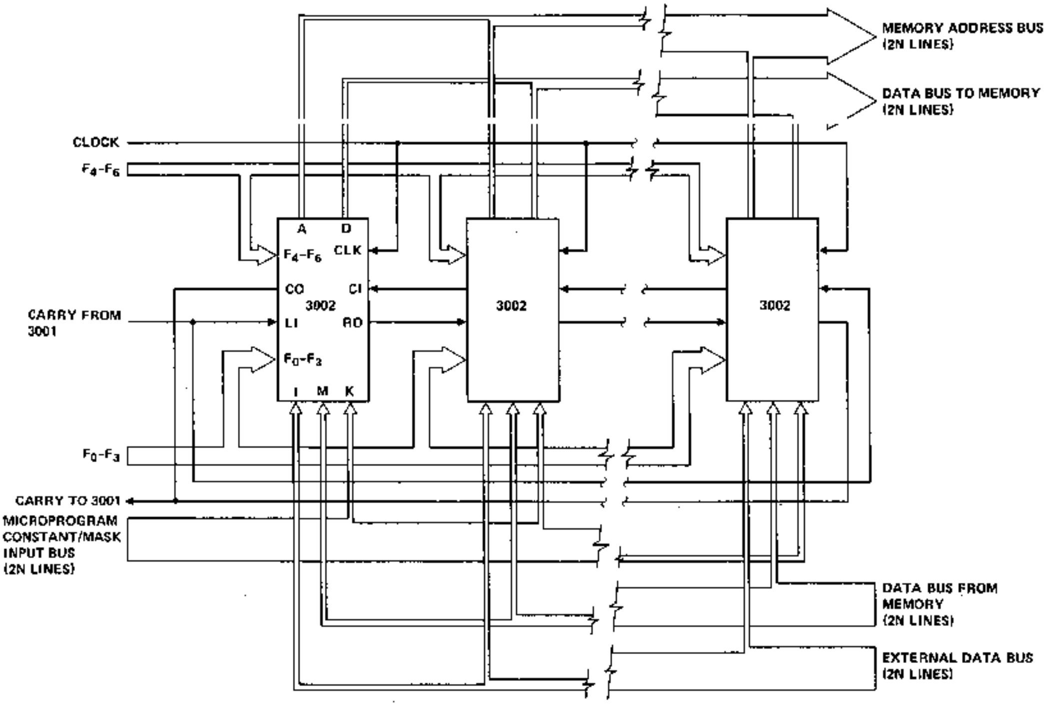
- High-speed controllers, built with a stand-alone ROM-MCU combination that sequences at up to 10 megahertz; it can be used without any CPEs as a system state controller.
- Pipelined look-ahead carry controller-processors, where the overlapped microinstruction fetch/execute cycles and fast-carry logic reduce the 16-bit add time to less than 125 nanoseconds.
- Ripple-carry controller processors (a 16-bit design adds the contents of two registers in 300 nanoseconds).
- Multiprocessors, or networks of any of the above controllers and processors, to provide computation, interrupt supervision, and peripheral control.

These configurations represent a range of microinstruction execution rates of from 3 million to 10 million instructions per second, or up to two orders of magnitude faster, for example, than p-channel microprocessors. Moreover, the increases in processor performance are achieved with relative simplicity. A ripple-carry 16-bit processor uses one MCU, eight CPEs, plus microprogram memory. One extra computing element, the 3003 Look-ahead Carry Generator, enhances the processor with fast carry. Increasing speed further by pipelining, the overlap of microinstruction fetch and execute cycles, requires a few D-type MSI flip-flops.

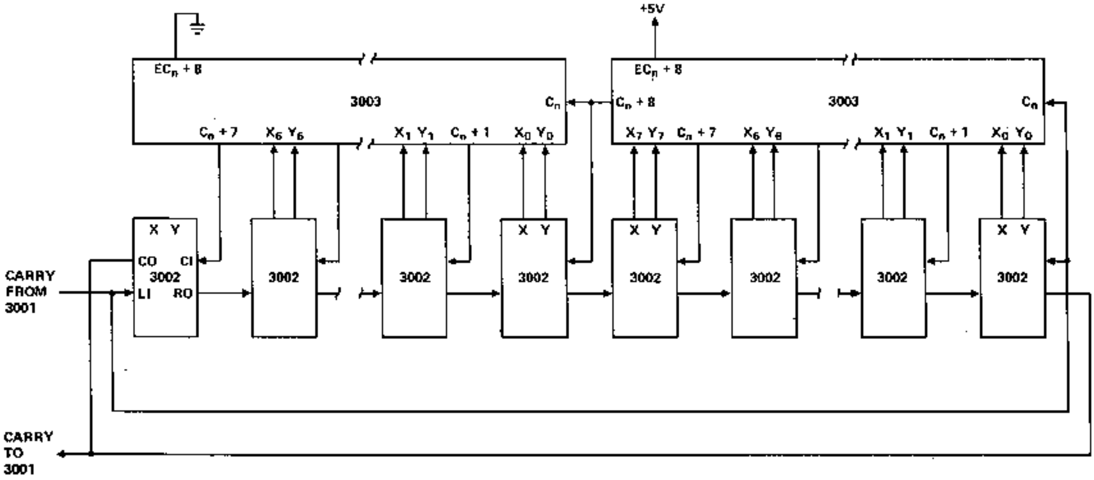
At the multiprocessor level, the microprogram memory, MCU, or CPE devices can be shared. A 16-bit processor, complete with bus control and microprogram memory, requires some 20 bipolar LSI packages and half that many small-scale ICs. In this configuration, it replaces an equivalent MSI TTL system having more than 200 packages.

Furthermore, systems built with this large-scale integrated circuitry are much smaller and less costly and consume less energy than equivalent designs using lower levels of transistor-transistor-logic integration. Even allowing for ancillary logic circuits, the new bipolar computing elements cut 60% to 80% off the package count in realizing most of today's designs made with small- or medium-scale-integrated TTL.

TYPICAL CONFIGURATIONS



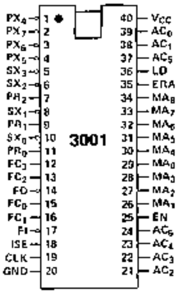
Ripple-Carry Configuration
(N 3002 CPE's)

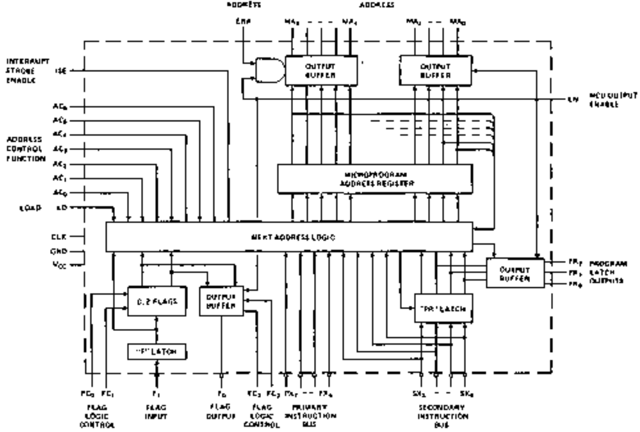


Carry Look-Ahead Configuration
With Ripple Through the Left Slice
(32 Bit Array)

3001

MICROPROGRAM CONTROL UNIT



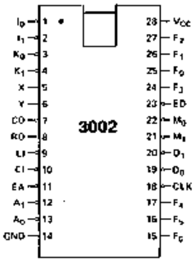


The Intel®3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.
- Selection of the next microinstruction based on the contents of the microprogram address register.
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.
- Saving and testing of carry output data from the central processor (CP) array.
- Control of carry/shift input data to the CP array.
- Control of microprogram interrupts.

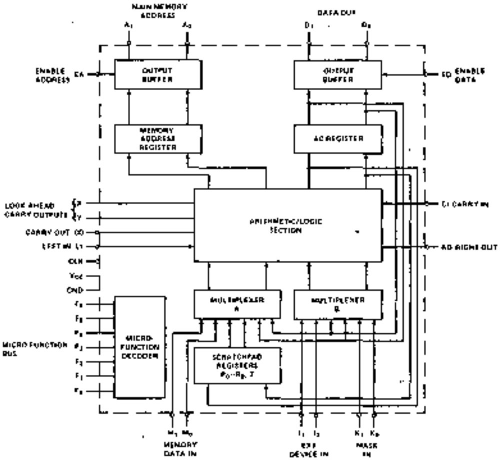
3002

CENTRAL PROCESSING ELEMENT



The Intel®3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPEs together. When wired together in such an array, a set of CPEs provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

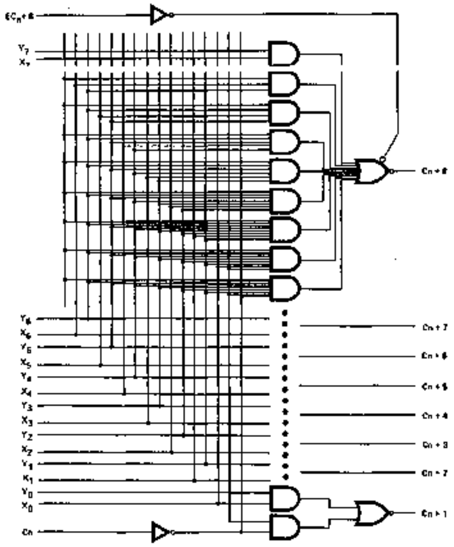


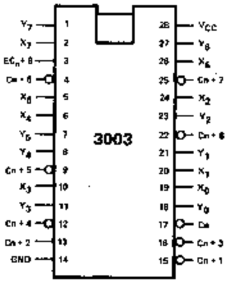
3003

LOOK-AHEAD CARRY GENERATOR

The Intel®3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16-bit 3002 Central Processing Array. When used with a larger 3002 CP Array multiple 3003 carry generators provide high speed carry look-ahead capability for any word length.

The LCG accepts eight pairs of active high cascade inputs (X, Y) and an active low carry input and generates active low carries for up to eight groups of binary adders.





3214

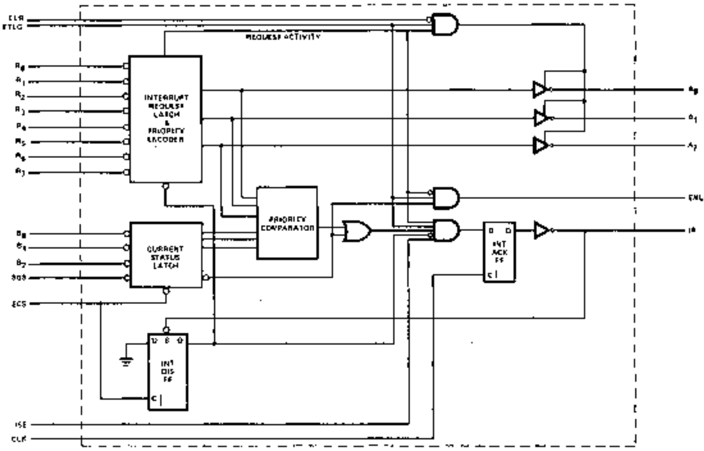
INTERRUPT CONTROL UNIT

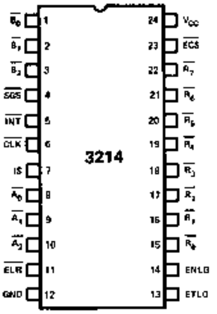
The Intel®3214 Interrupt Control Unit (ICU) implements multi-level interrupt capability for systems designed with Series 3000 computing elements.

The ICU accepts an asynchronous interrupt strobe from the 3001 Microprogram Control Unit or a bit in microprogram memory and generates a synchronous interrupt acknowledge and an interrupt vector which may be directed to the MCU or CP Array to uniquely identify the interrupt source.

The ICU is fully expandable in 8-level increments and provides the following system capabilities:

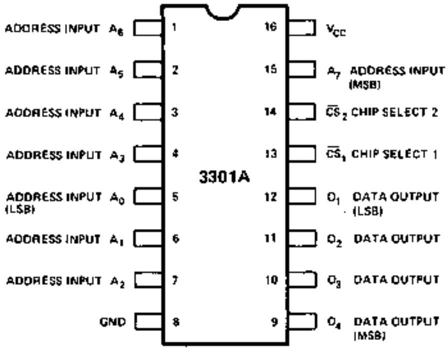
- 80 ns Cycle Time
  Eight unique priority levels per ICU
  Automatic Priority Determination
  Programmable Status
  N-level expansion capability
  Automatic interrupt vector generation





3301A

HIGH SPEED FULLY DECODED 1024 BIT READ ONLY MEMORY

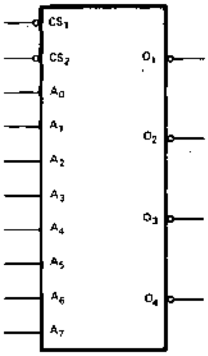


The 3301A is a fully decoded 1024 bit read only memory organized as 256 words by 4-bits. It is a higher speed version of the 3301 and is a direct pin for pin replacement of the 3301. Its performance is specified over the complete ambient temperature range of 0°C to 75°C and a V_{CC} supply voltage range of 5V ±5%. The 3301A is programmed at the final step of processing which allows fast turnaround.

Access time is 45 nanoseconds.

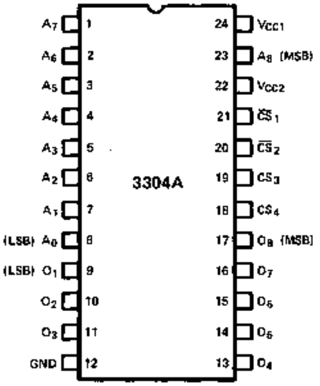
The OR-tie capability and the 2 chip select inputs of the 3301A allow easy memory expansion into larger word and bit lengths.

The 3301A is mask programmed to customized patterns. Ideal applications are in microprogramming and table look-up.



3304A

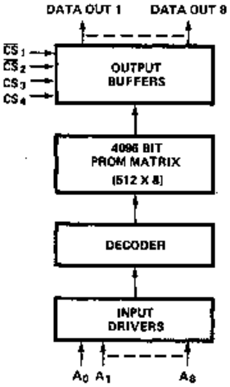
4096 BIT BIPOLAR READ ONLY MEMORY



The 3304A is a 4096 bit mask programmable read-only memory which is organized as 512 words by 8-bits. Electrical performance is specified over the complete ambient temperature range of 0°C to 75°C and V_{CC} supply voltage range of 5V ±5%.

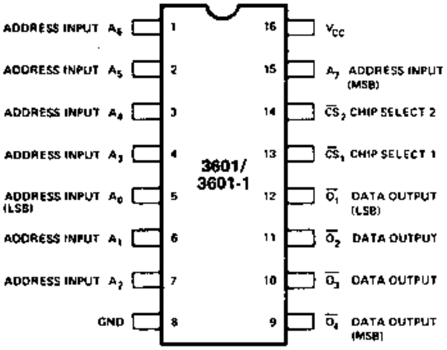
Access time is 70 nanoseconds.

The high bit density of the 3304A offers usage in applications in look-up tables, microporgramming, code conversion, logic function generation, or character generation.



3601, 3601-1

HIGH SPEED 1024 BIT PROM ELECTRICALLY PROGRAMMABLE



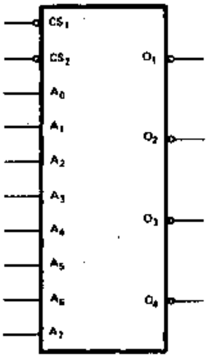
The Intel® 3601 and 3601-1 are 1024 bit (256 word by 4-bit) electrically programmable ROMs ideally suited for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROMs are manufactured with all outputs low and logic high output levels can be electrically programmed in selected bit locations. The same address inputs are used for both programming and reading.

The 3601 access time is 70 nanoseconds.

The 3601-1 access time is 50 nanoseconds.

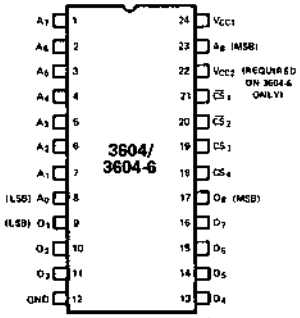
The 3601 and 3601-1 are pin compatible with the Intel® metal mask 3301A ROM. The 3301A is ideal for large volume and lower cost production runs of systems initially using the PROM.

The 3601 and 3601-1 are manufactured with the highly reliable polycrystalline silicon fuse and the fast switching Schottky barrier diode technology.



3604, 3604-6

HIGH SPEED 4096 BIT PROM ELECTRICALLY PROGRAMMABLE



The 3604 and 3604-6 are high density 4096 bit (512 word by 8-bit) electrically programmable ROMs suitable for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

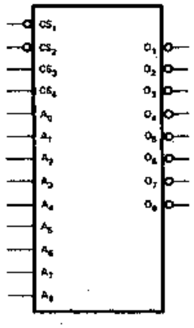
The 3604 access time is 70 nanoseconds.

The 3604-6 access time is 90 nanoseconds.

For those systems requiring low power dissipation, one should consider the 3604-6. Not only does the 3604-6 dissipate 20% less active power than the 3604, but it also has an added low standby power dissipation feature. Whenever the 3604-6 is deselected, power dissipation is reduced by 70%. The lower cost 3304A-6 metal mask ROM is also available for volume production usage.

The 3604 is pin compatible with the Intel® 3304A metal mask ROM. The 3304A is ideal for large volume and lower cost production runs of systems initially using the 3604.

The 3604 and 3604-6 are monolithic, high speed, Schottky clamped TTL memory arrays with polycrystalline silicon fuses.

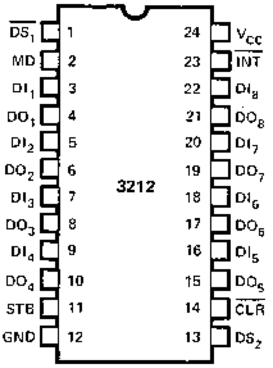


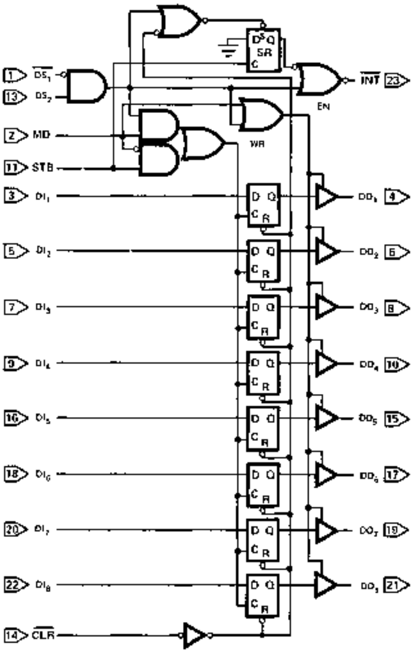
3212

MULTI-MODE LATCH BUFFER

The Intel®3212 Multi-Mode Latch Buffer is a versatile 8-bit latch with three-state output buffers and built-in device select logic. It also contains an independent service request flip-flop for the generation of central processor interrupts. Because of its multi-mode capabilities, one or more 3212's can be used to implement many types of interface and support systems for Series 3000 computing elements including:

- Simple data latches
- Gated data buffers
- Multiplexers
- Bi-directional bus drivers
- Interrupting input/output ports



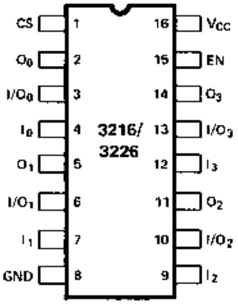


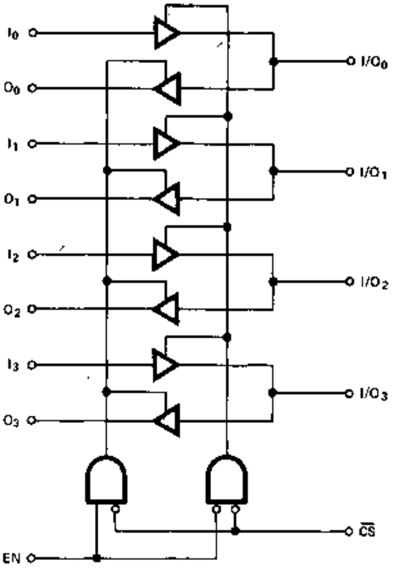
3216, 3226

4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

The Intel®3216/3226 are high speed 4-bit parallel, bi-directional bus drivers. The 3226 provides inverted I/O. The three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems.

The 3216/3226 driver and receiver gates have three-state outputs with PNP inputs. When the drivers or receivers are tri-stated the inputs are disabled, presenting a low current load, typically less than 40 µamps, to the system bus structure.





WF-3000
BIPOLAR SYSTEM DEVELOPMENT SET

The Intel WF-3000 Bipolar System Development Set contains the following members of the Schottky Bipolar LSI Microcomputer Set:

(2) 3001 Microprogram Control Units
(10) 3002 Central Processing Elements
(10) 3601 Bipolar PROMs (256 x 4)

Includes all Computing Elements and High Speed Memory required for the construction of 16, 18, or 20 bit processors and/or High Speed Controllers.

N-Bit Word Expandable.
Multi-bus Organization.
High Performance
  MCU Cycle Time – 700ns
  CPE Cycle Time – 100ns
  Total System Cycle Time – 150ns*

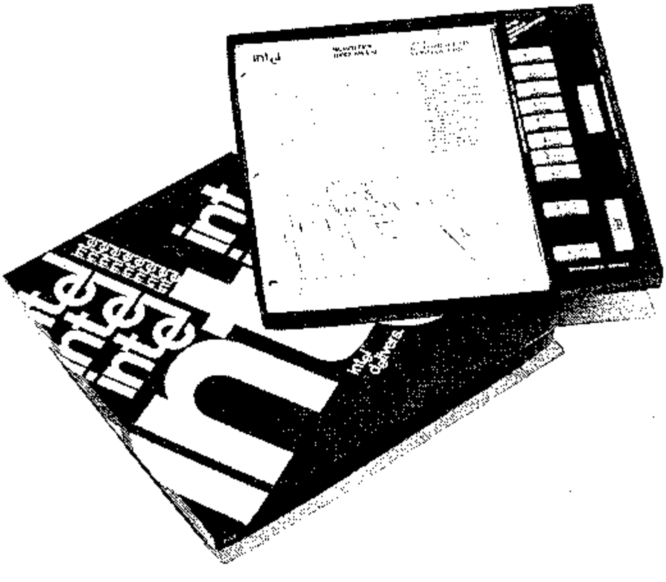
*Guaranteed worst case system cycle time for a 16-bit processor with a fast carry (3003) CP array, 3601-1 PROM Memory and a pipelined architecture.

A unique technology updating program insures that all set owners are kept abreast of Bipolar Microcomputer Set developments. This service includes priority mailings of additional design aids – application notes, specification sheets, user manuals – and free samples of new family members.

Upon receipt of the Bipolar system Development Registeration Card, free samples of the following computing elements will be sent to development set owners:

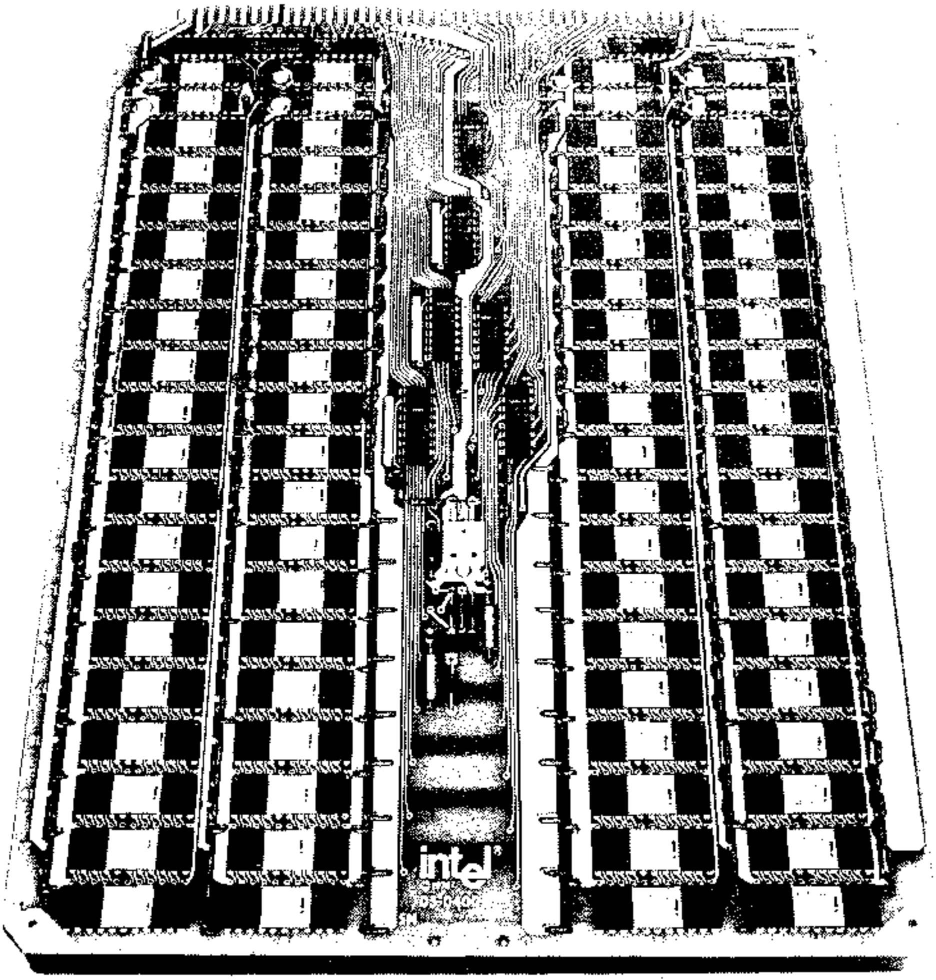
3003 Look-Ahead Carry Generator
3212 Multi-Mode Latch Buffer
3214 Interrupt Control Unit
3226 Inverting Bi-Directional Bus Driver

In addition, free samples of new computing elements will be provided as they are announced throughout 1975.

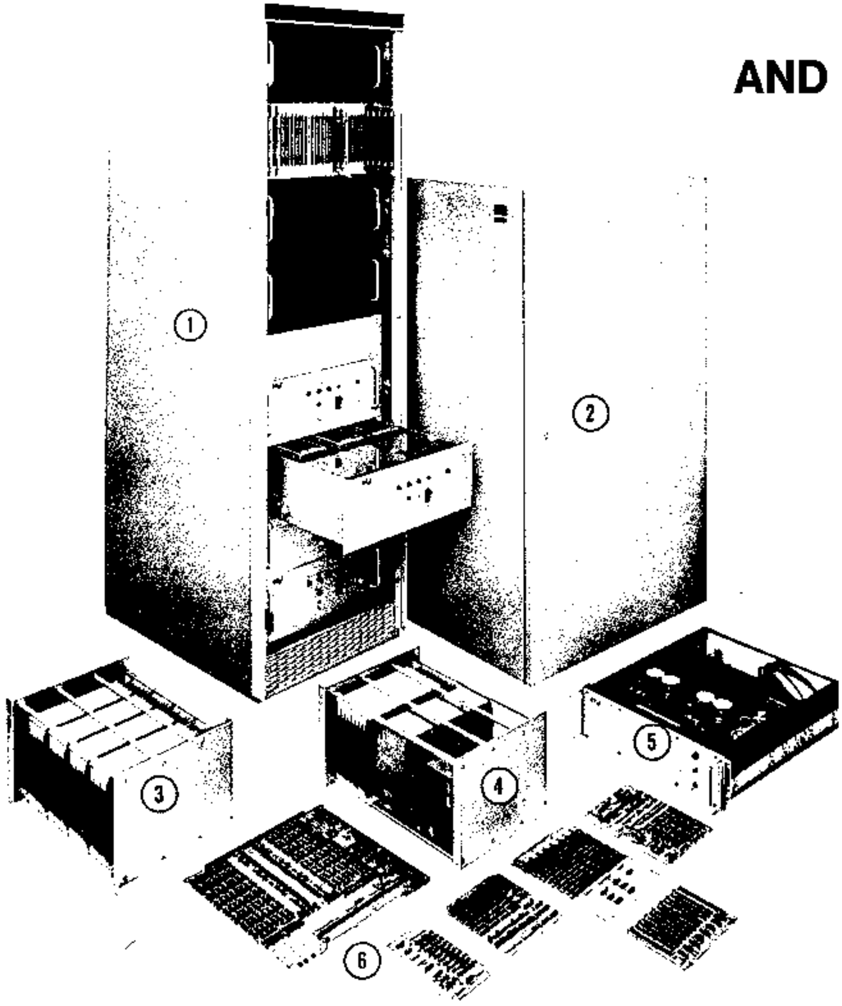


7

MEMORY SYSTEMS



INTEL SPECIALIZES IN CUSTOM MEMORY CARDS AND SYSTEMS



The above photograph features some of the memory systems that are available from Intel. These are shown as follows:

① 262k x 40 bit memory system – 600ns cycle time with battery backup as part of the power supply drawers.

② 65k x 144 bit memory system – with power supply and cabinet. Memory is mounted on hinges for access to either side.

③ 65k x 18 bit memory system mounted in a 19" relay rack – 450ns cycle time.

④ 32k x 18 bit memory system mounted in a 19" relay rack – 450ns cycle time.

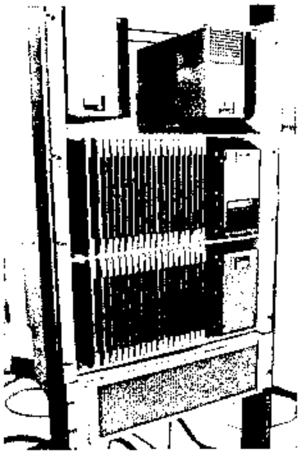
⑤ 19" relay rack mountable power supply for use with 65k x 18 memory system listed in #3.

⑥ Various memory cards are shown above that can be rack mounted in a number of configurations and physical sizes.

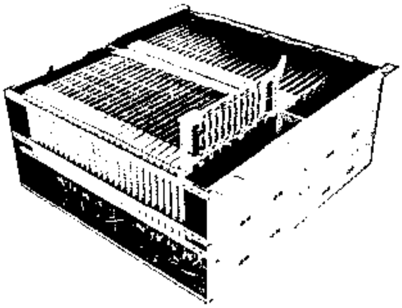
Contact your local Intel sales representative for further information on any of the above.

INTEL CUSTOM MEMORY SYSTEMS

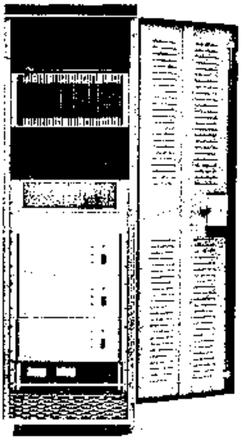
Intel specializes in the design and manufacture of custom memory systems for individual customer needs. Intel's memory cards are used as the basic building block in the design and manufacture of custom systems. These custom systems can vary in physical size, word length, storage capacity and speed. The following are examples of some of these systems.



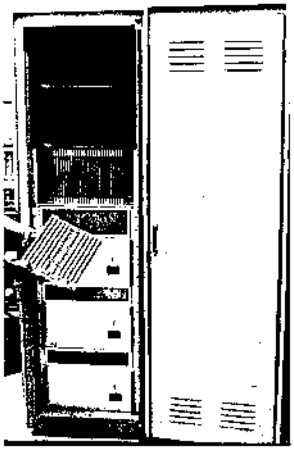
in-10 450ns system organized as 65k x 36 with battery backed up power supply and mounted in a 19" relay rack.



in-50 100ns system organized 1k x 520 bits with chassis for mounting in a 19" relay rack with fan assembly and power supply mounted below the unit.



in-12 650ns system organized as 128k x 63 bits in a free standing cabinet with power supplies and custom-designed interface. Air enters from bottom and is exited through top of unit. All units are modular and accessible from front and back sides.



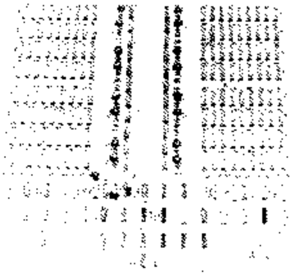
in-60A 1MHz system organized as 1,440,000 words by 10 bits in a free standing cabinet with power supply and cooling system located below the memory modules. This 14 million bit memory is one of the largest serial memory systems delivered to a customer.

CUSTOM MEMORY CARDS

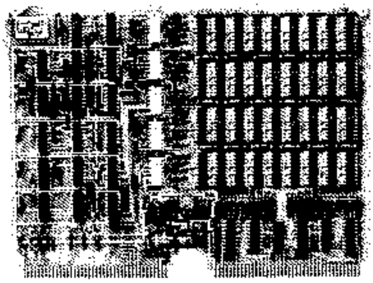
Featuring the Use of 1K Memory Components

Intel specializes in the design and manufacture of Custom Memory Cards for individual customer needs. Intel's application engineering experts design and build to your specification or work with you in the definition of one. The specification, once defined, will then be incorporated into a design that will match your card format, speed and timing considerations, and pin outs.

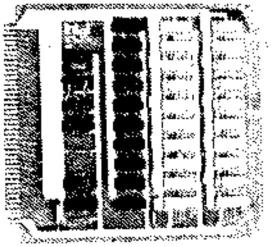
Intel will design and manufacture both shift register and random access memory applications. The following are examples of custom memory cards that have been designed to fulfull customer applications.



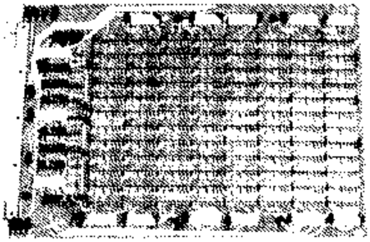
8k x 18 RAM Memory System designed especially for a mini-computer manufacturer, 700ns cycle time. Board size – 15" x 17".



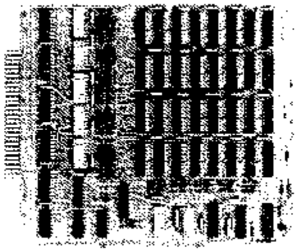
4k x 9 RAM Memory System designed especially for a small data communications user. Features 675ns speed and needs only two power supply voltages.



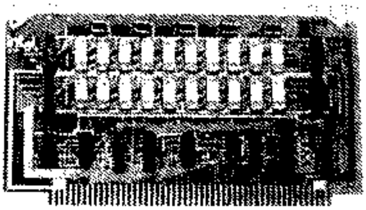
1k x 20 RAM Memory System designed to meet a customer's extended temperature ranges. Features a 1μs cycle time, needs only one power supply voltage.



8k x 12 RAM Memory System designed especially for a major computer manufacturer – 650ns cycle time, multi-layer card.



32k x 1 or 16k x 2 RAM Memory System designed to meet the needs of a customer's error correction logic system. 675ns cycle time.



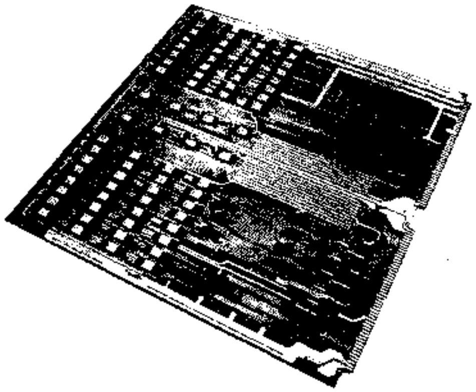
512k x 10 RAM Memory System designed especially for a major telephone company for use in special network monitoring. Features a small card size and 100ns cycle time.

CUSTOM MEMORY CARDS

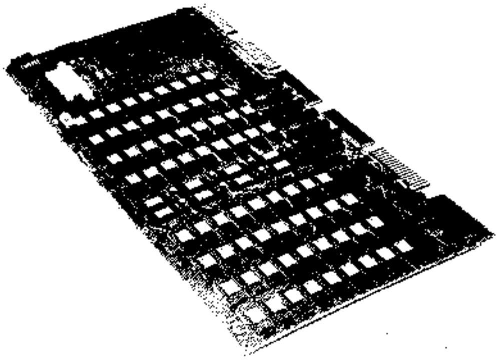
Featuring the Use of 4K Memory Components

As new components are developed by Intel, the Memory Systems Division is the first to evaluate and design around them at the system level. Design technique improvements are incorporated in both standard and custom memory designs. A custom memory system from Intel gives you GUARANTEED PRICE, GUARANTEED PERFORMANCE, and GUARANTEED DELIVERY.

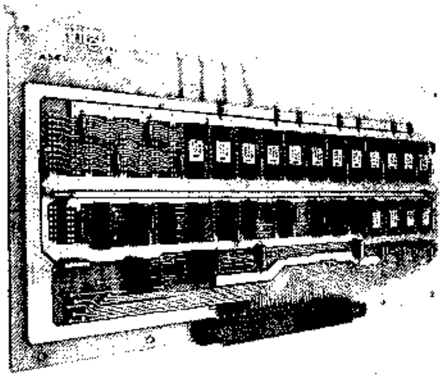
Rights to manufacture are extended after initial production and can be included in our packaged purchase plan. The memory systems below are typical of the type of designs we are manufacturing.



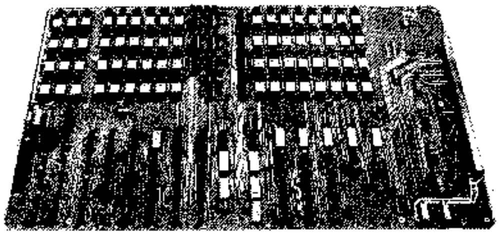
8K x 16 RAM Memory System. Another cost effective use of our 4K chip design for a serial (CRT) type application.



8K x 18 RAM Memory System designed to double the capacity and reduce the cost of the core memory that it is replacing in a major minicomputer.

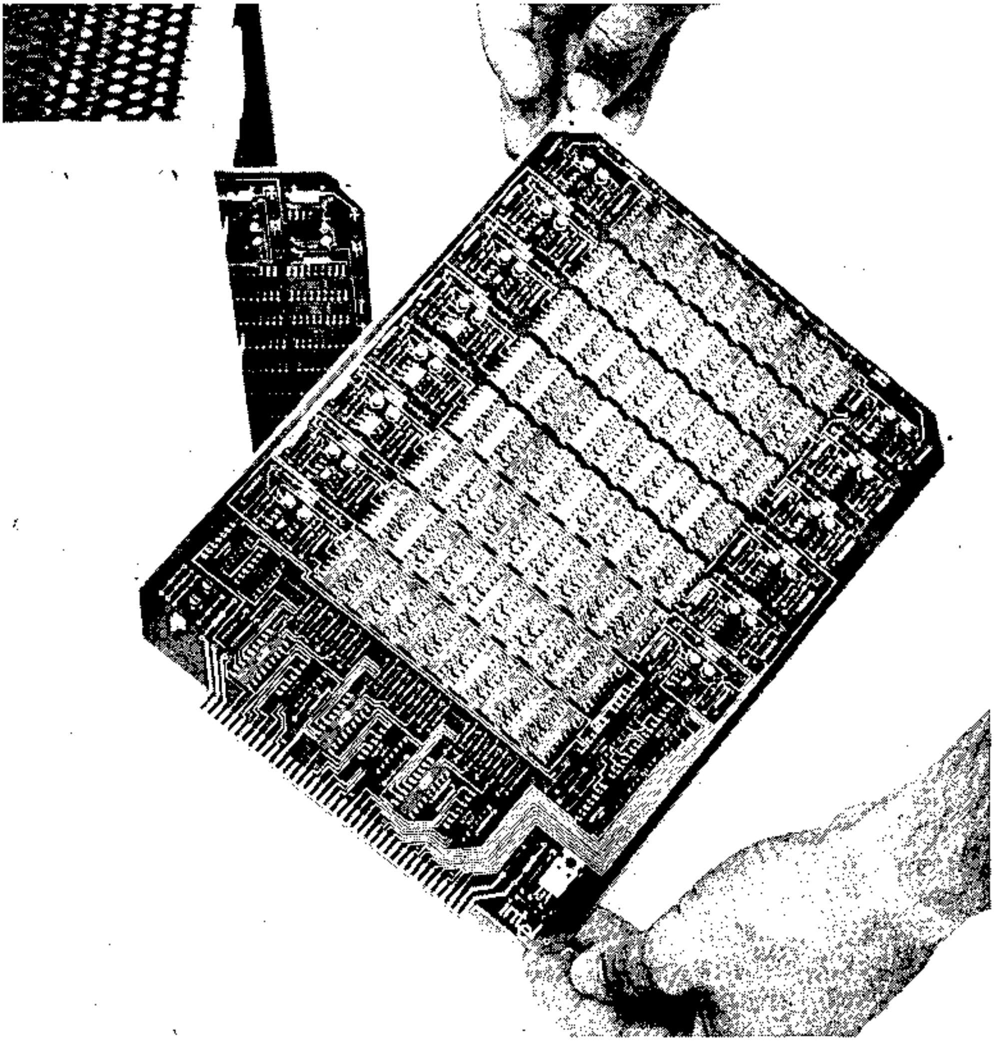


4K x 12 to 4K x 16 Serial RAM Memory System with external timing and control. Used to replace an expensive core memory in an intelligent terminal CRT display.



The in-473; 8K x 17 RAM Memory System used by a major industrial giant with stringent reliability requirements in the demanding environment of a numerical control application.

in-10 MEMORY SYSTEM



in-10 SERIES RAM MEMORY FEATURES:

- **Low Cost Memory**
- **High Reliability**
- **Modular Expandability**
- **Module Interchangeability**
- **Automatic Refresh**
- **Fast Cycle Time**
- **Low Power Requirements**
- **Compact Size**
- **Field Expandable**

The in-10 RAM Memory System is designed to meet the high reliability and low price requirements of large volume memory applications. The in-10 features the use of the Intel 1103 MOS chip. This memory system features a basic 4K x 18 or 8K x 9 configuration consisting of two plug-in boards: A memory board (MU) and a control board (CU). The control board is capable of operating up to 32K words x 18 bits or 65K words x 9 bits.

SYSTEM in-10 SPECIFICATIONS

Dimensions:

Memory Board:	8.175 Inches	High
(4K x 18 or 8K x 9)	10.5 Inches	Deep
	0.5 Inches	Wide

To expand to 32K x 18 add 0.5 inches per memory card. Only one control card (CU) is needed for systems up to 32K x 18 or 64K x 9.

Memory System:	8.175 Inches	High
(32K x 18)	10.5 Inches	Deep
	5.0 Inches	Wide

Capacity:

1024, 2048, 4096, 8192 words expandable in cards to 32,768 x 18 or 65,536 x 9 capacity.

Word Length:

8, 9, 10, 12, 16, or 18 bits in a single memory card. Longer word lengths can be accommodated by combining memory cards.

Cycle Time:

in-10A	450 Nanoseconds
in-10	450 Nanoseconds
in-12	675 Nanoseconds
in-14	850 Nanoseconds

Access Time:

in-10A	275 Nanoseconds
in-10	325 Nanoseconds
in-12	450 Nanoseconds
in-14	500 Nanoseconds

Operational Modes:

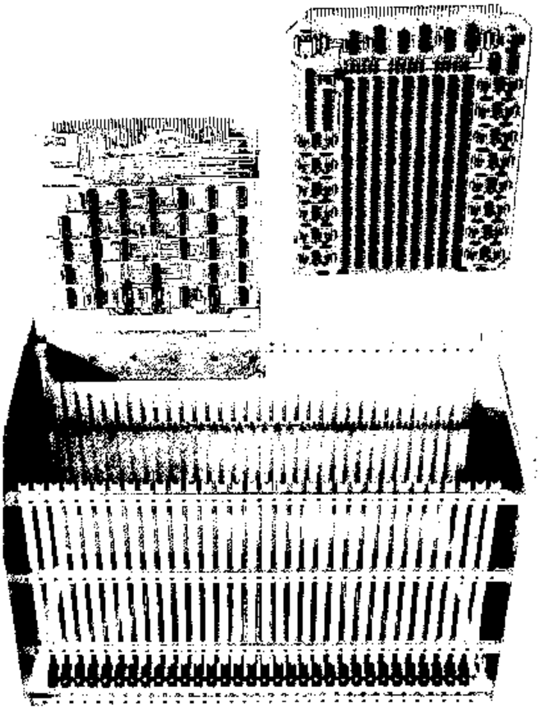
Read
Write
Read/Modify/Write (Optional)

Interface Characteristics:

- TTL Compatible
- Standard Input Lines:
  - Cycle Initiate
  - Byte Control
  - Read/Write
- Standard Output Lines:
  - Data Available
  - Memory Busy

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating



D.C. Power Requirement:

in-10:	Voltage	Regulation
	+3.5V (Stacked on 19.7V)	±10%
	+19.7	±5%
	+ 5	±5%

42 Watts (basic 4K x 18) (16 watts per additional 4K)

in-12 & 14:	Voltage	Regulation
	+3.5V (Stacked on 16.7V)	±10%
	+16.7	±5%
	+ 5	±5%

35 Watts (basic 4K x 18) (12 watts per additional 4K)

Features:

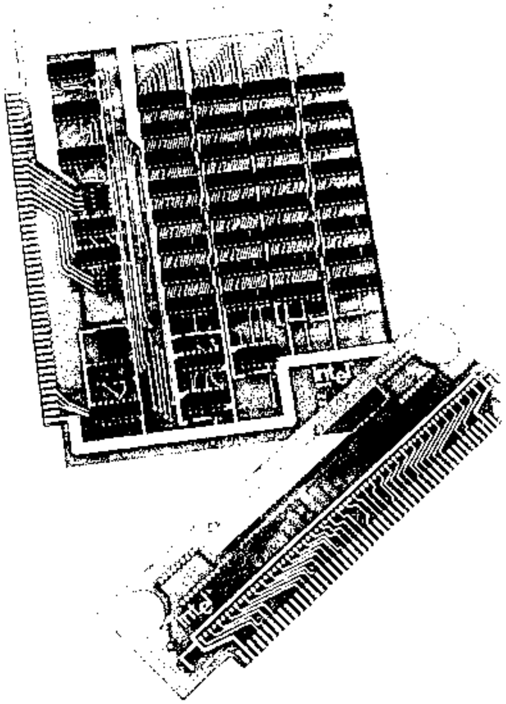
Byte Control (2 Zones Maximum)
Module Select
Address Register
Data Register (Optional)
Basic System Available As 4K x 18 or 8K x 9

Special Options:

INTEL also offers the in-10 mounted in a card chassis. This chassis is designed for mounting in 19" relay racks.

NEW OPTIONS

in-26 MEMORY SYSTEM



in-26 SERIES RAM MEMORY FEATURES

- Low Cost Memory
- High Reliability
- Modular Expandability
- Module Interchangeability
- Fast Cycle Time
- Low Power Requirements
- Compact Size
- Field Expandable
- 1 Power Supply Voltage

The in-26 RAM Memory System is designed to meet the high reliability and low cost requirements of random access buffer storage applications. The in-26 features a complete memory system on a single PC board. This memory system has a basic capacity of 4k x 10 and can be expanded to 16k x 10. It is also available in capacities as small as 1k x 10. The compact size of this system makes it ideal for use as a buffer main memory storage for various computer peripheral applications. This memory system is designed especially to interface with the MCS-4/MCS-8 series micro processors.

(Refer to SIM8-01/in-26 Application Note.)

SYSTEM in-26 SPECIFICATIONS

Dimensions:

Memory Board: (4k x 10)	8.175 Inches High 6.0 Inches Deep 0.5 Inches Wide

Capacity:

1024, 2048, and 4096 words expandable to 16k words by the addition of memory cards.

Word Length:

4, 6, 8, 9, 10 bits per card. Longer words can be made by adding additional memory cards.

Cycle Time:

in-26	900 Nanoseconds
in-26-1	600 Nanoseconds
in-26-2	475 Nanoseconds
in-26-3	375 Nanoseconds

Access Time:

in-26	900 Nanoseconds
in-26-1	600 Nanoseconds
in-26-2	475 Nanoseconds
in-26-3	375 Nanoseconds

Operational Modes:

- Read (NDRO)
- Write
- Read/Modify/Write

Interface Characteristics:

- TTL Compatible
- Standard Input Lines:
  - Cycle Initiate
  - Board Select
  - Read/Write
- Standard Output Lines:
  - Data Available
  - Memory Busy

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

DC Power Requirement:

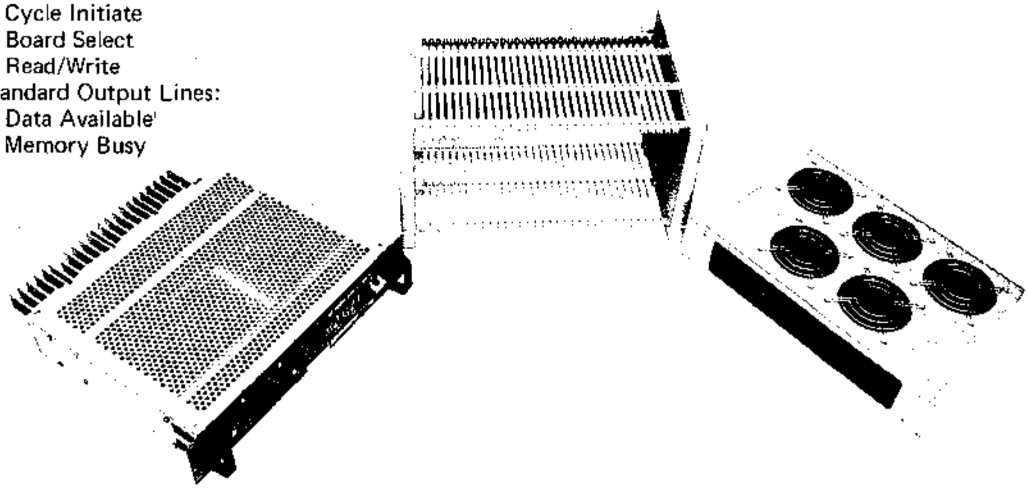
in-26	+5V ± 5%

Features:

- Board Select
- Address Register
- Low Power Standby Operation
- Single Board System
- One Connector Per System
- One Voltage

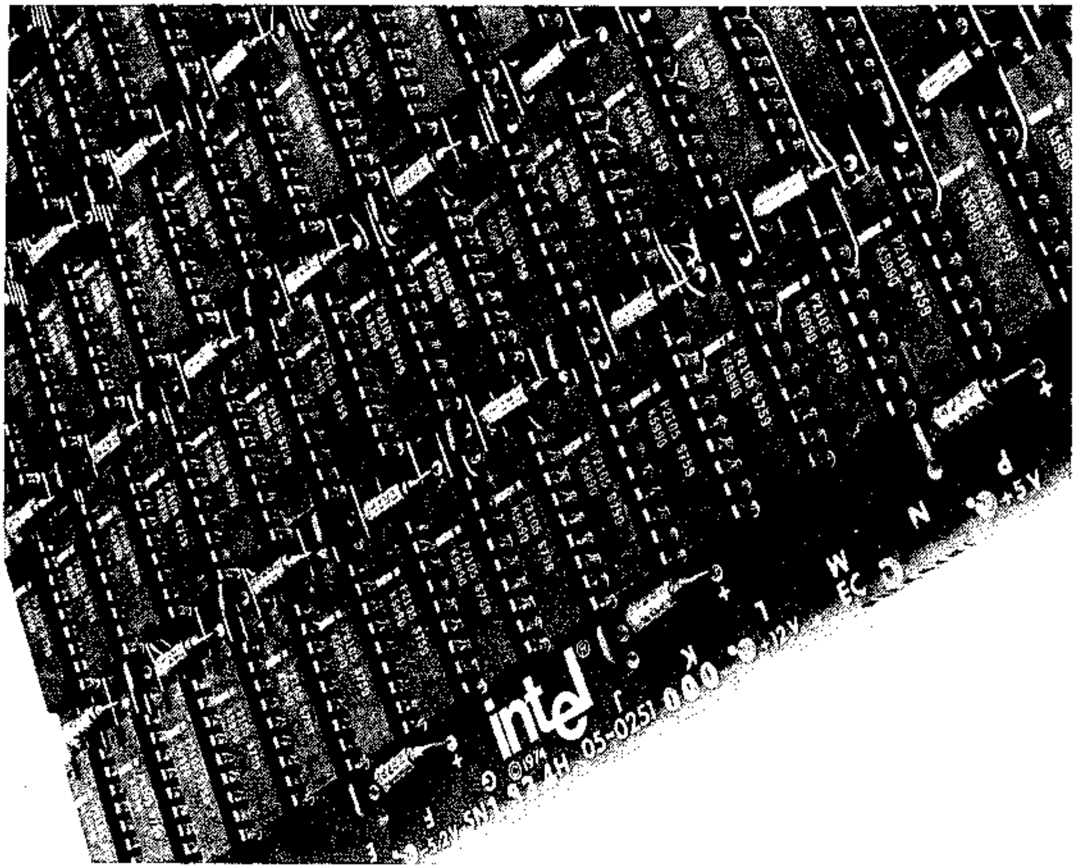
Special Options:

Intel also offers the in-26 mounted in a card chassis. This chassis is available in a variety of sizes and can be set up for future expansion of the memory without changing the basic chassis.



NEW

in-30 MEMORY SYSTEM



in-30 SERIES RAM MEMORY FEATURES:

- **Fastest MOS Memory**
- **High Reliability**
- **Modular Expandability**
- **Module Interchangeability**
- **Automatic Refresh**
- **Fast Cycle Time**
- **Low Power Requirements**
- **Compact Size**
- **Field Expandable**

The in-30 RAM Memory System is modular, built for standard expansion in off-the-shelf memory board (MU) increments of 4K x 18 or 8K x 9. A single control board (CU) is capable of operating up to 32K x 18 or 65K x 9. High speed access and cycle times offer maximum performance to price ratio. No adjustments are necessary with in-30 interchangeable modules. Chassis options include completely tested systems in custom configurations.

SYSTEM in-30 SPECIFICATIONS

Dimensions:

Memory Board: (4K x 18 or 8K x 9)	8.175 Inches	High
	10.5 Inches	Deep
	0.5 Inches	Wide

To expand to 32K x 18 add 0.5 inches per memory card. Only one control card (CU) is needed for systems up to 32K x 18 or 64K x 9.

Memory System: (32K x 18)	8.175 Inches	High
	10.5 Inches	Deep
	5.0 Inches	Wide

Capacity:

1024, 2048, 4096, 8192 words expandable in cards to 32,768 x 18 or 65,536 x 9 capacity.

Word Length:

8, 9, 10, 12, 16, or 18 bits in a single memory card. Longer word lengths can be accommodated by combining memory cards.

Cycle Time:

in-30	330 Nanoseconds

Access Time:

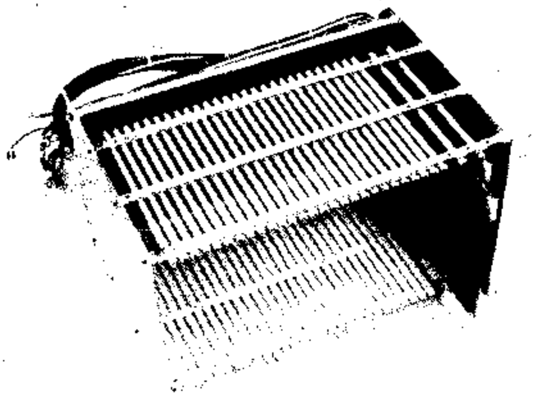
in-30	200 Nanoseconds

Operational Modes:

Read
Write
Read/Modify/Write (Optional)

Interface Characteristics:

- TTL Compatible
- Standard Input Lines:
  - Cycle Initiate
  - Byte Control
  - Read/Write
- Standard Output Lines:
  - Data Available
  - Memory Busy



Environment:

Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

D.C. Power Requirement:

in-30	Voltage	Regulation
	-5	±5%
	+12	±5%
	+5	±5%

50 Watts (basic 4K x 18) (26 watts per additional 4K)

Features:

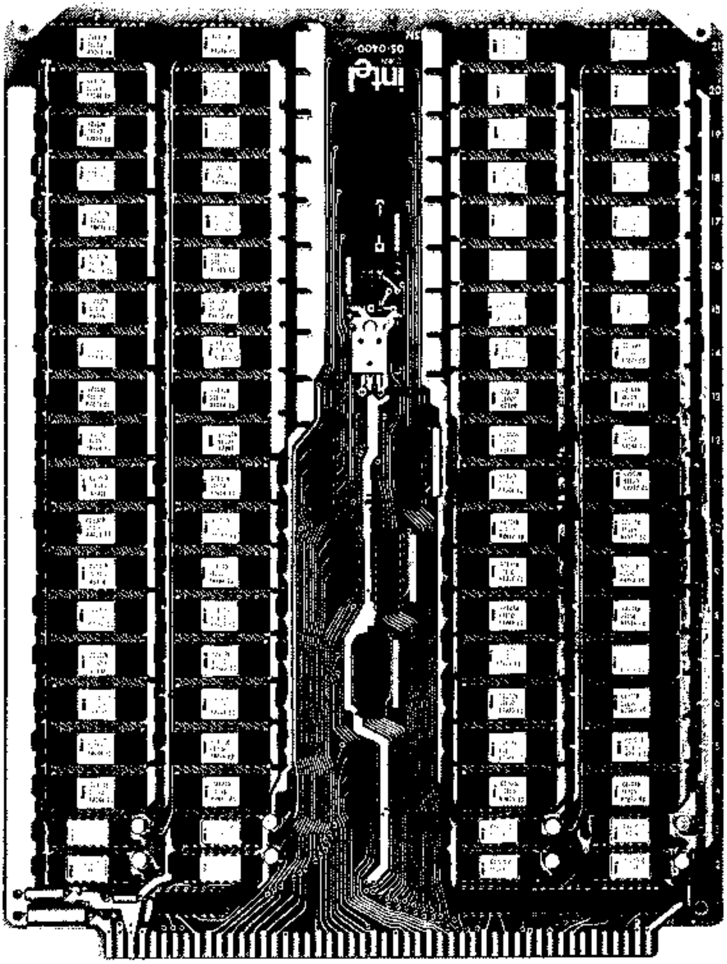
Byte Control (2 Zones Maximum)
Module Select
Address Register
Data Register (Optional)
Basic System Available As 4K x 18 or 8K x 9

Special Options:

INTEL also offers the in-30 mounted in card chassis designed for mounting in 19" and 24" relay racks. UT-30 socket cards allow easy wire wrapping of custom interfaces in the card chassis.

NEW

in-40 MEMORY SYSTEM



in-40 SERIES RAM MEMORY FEATURES:

- **Low Cost Memory**
- **High Reliability**
- **High Density**
- **Modular Expandability**
- **Module Interchangeability**
- **Automatic Refresh**
- **Fast Cycle Time**
- **Low Power Requirements**
- **Compact Size**
- **Field Expandable**

The in-40 RAM Memory System is perhaps the highest density memory now available. The interchangeable memory boards (MU) allow expansion in increments of 16K x 18 or 32K x 9 with no adjustments. A single control board (CU) handles up to 128K x 18 or 256K x 9 comprising our lowest cost-per-bit package available. Large and small chassis options include custom configurations with or without power supply and fan assemblies.

SYSTEM in-40 SPECIFICATIONS

Dimensions:

Memory Board:	8.175 Inches	High
(16K x 18 or 32K x 9)	10.5 Inches	Deep
	0.5 Inches	Wide

To expand to 128K x 18 add 0.5 inches per memory card. Only one control card (CU) is needed for systems up to 128K x 18 or 256K x 9.

Memory System:	8.175 Inches	High
(128K x 18)	10.5 Inches	Deep
	5.0 Inches	Wide

Capacity:

4096, 8192, 16,384, 32,768 words expandable in cards to 131,072 x 18 or 262,144 x 9 capacity.

Word Length:

8, 9, 10, 12, 16, or 18 bits in a single memory card. Longer word lengths can be accommodated by combining memory cards.

Cycle Time:

in-40	550 Nanoseconds
in-40-1	650 Nanoseconds

Access Time:

in-40	350 Nanoseconds
in-40-1	475 Nanoseconds

Operational Modes:

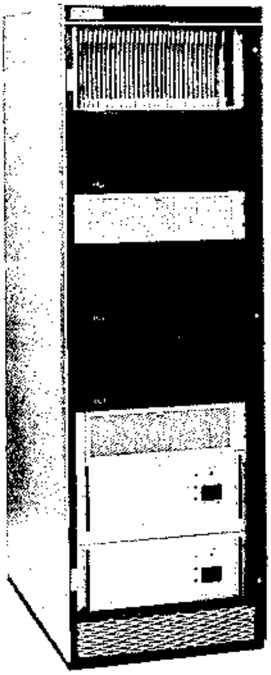
Read
Write

Interface Characteristics:

- TTL Compatible
- Standard Input Lines:
  - Cycle Initiate
  - Byte Control
  - Read/Write
- Standard Output Lines:
  - Data Available
  - Memory Busy

Environment:

Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating



D.C. Power Requirement:

MU-40:

Voltage	Current (Typical)	Regulation
+12V	1 Amp	±5%
+5V	1 Amp	±5%
-5V	<100 Milliamps	±5%

CU-40:

Voltage	Current (Typical)	Regulation
+5V	1.3 Amp	±5%

Features:

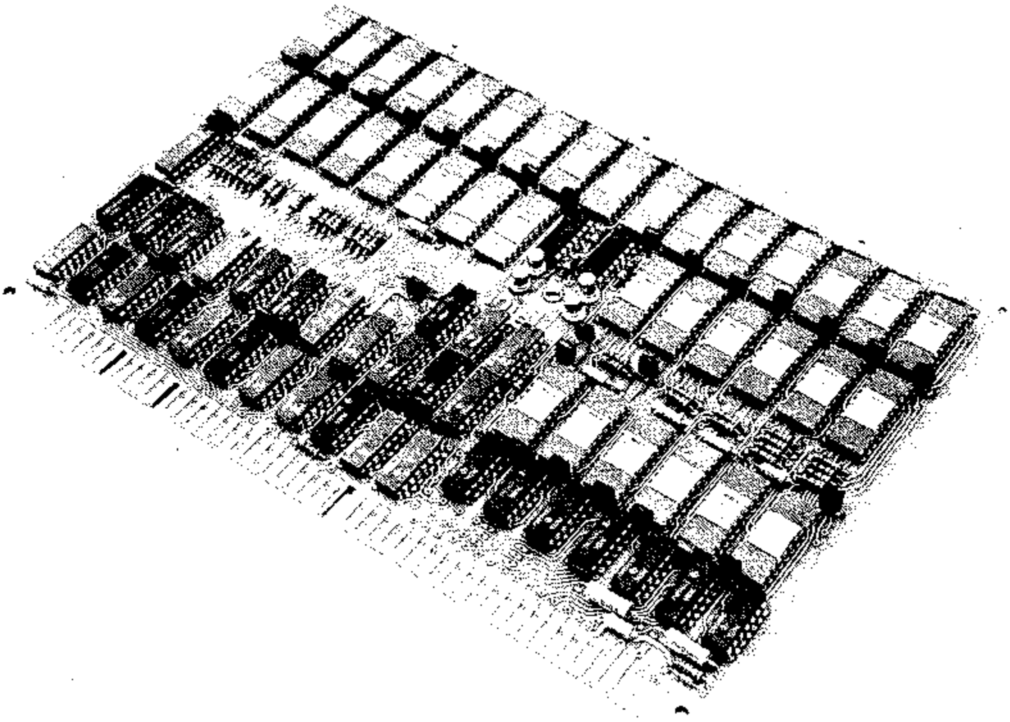
Byte Control (2 Zones Maximum)
Module Select
Address Register
Data Register (Optional)
Basic System Available As 16K x 18 or 32K x 9

Special Options:

INTEL also offers the in-40 mounted in card chassis designed for mounting in 19" and 24" relay racks. UT-40 socket cards allow easy wire wrapping of custom interfaces in the card chassis.

NEW

in-41E MEMORY SYSTEM
(Euroboard Format)



in-41E SERIES RAM MEMORY FEATURES:

- Low Cost Memory
- High Reliability
- Module Expandability
- Module Interchangeability
- Automatic Refresh
- Fast Cycle Time
- Low Power Requirements
- Compact Size
- Field Expandable
- Master/Slave Operation
- Complete Control on each Board
- Address and Data Registers

The in-41E RAM Memory System is perhaps the highest density memory now available on Euroboards. The interchangeable memory boards (MU) allow expansion in increments of 8K x 18 or 16K x 9 with no adjustments. A single control board (CU) handles up to 64K x 18 or 128K x 9 comprising our lowest cost-per-bit package available. This memory system features a fast access and cycle time, high density and the use of a 4K RAM as the storage device.

SYSTEM in-41E SPECIFICATIONS

Dimensions:

Memory Board:	160 mm	High
(8K x 18)	233.4 mm	Deep
	12.7 mm	Wide

To expand to 64K x 18, add 12.7 mm per memory card.

Capacity:

8,192 words expandable in cards to 65, 536 x 18 storage capacity or 128K x 9.

Word Length:

Up to 18 bits in a single memory card. Longer word length can be accommodated by combining memory cards.

Cycle Time:

in-41E	550 Nanoseconds
in-41E-1	650 Nanoseconds

Access Time:

in-41E	350 Nanoseconds
in-41E-1	475 Nanoseconds

Operational Modes:

Read (NDRO)
Write

Interface Characteristics:

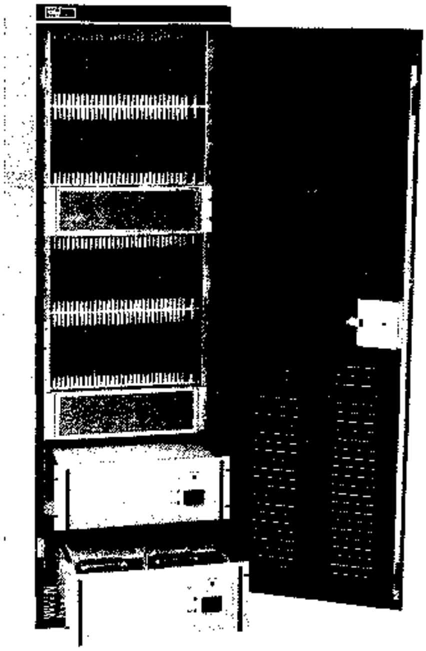
- TTL Compatible
- Standard Input Lines:
  - Cycle Initiate
  - Byte Control
  - Read/Write
- Standard Output Lines:
  - Data Available
  - Memory Busy

Address Input:

12 - 17 lines, binary, single ended.

Environment:

Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 15,000 feet non-operating



D.C. Power Requirements:

MU-41E: Selected

Voltage	Current (Typical)	Regulation
+12V	1.4 Amps	±5%
+5V	1.0 Amps	±5%
-5V	50 Milliamps	±5%

MU-41E: Unselected

Voltage	Current (Typical)	Regulation
+12V	0.142 Amps	±5%
+5V	1.0 Amps	±5%
-5V	50 Milliamps	±5%

CU-41E:

Voltage	Current (Typical)	Regulation
+5V	1.3 Amps	±5%

Features:

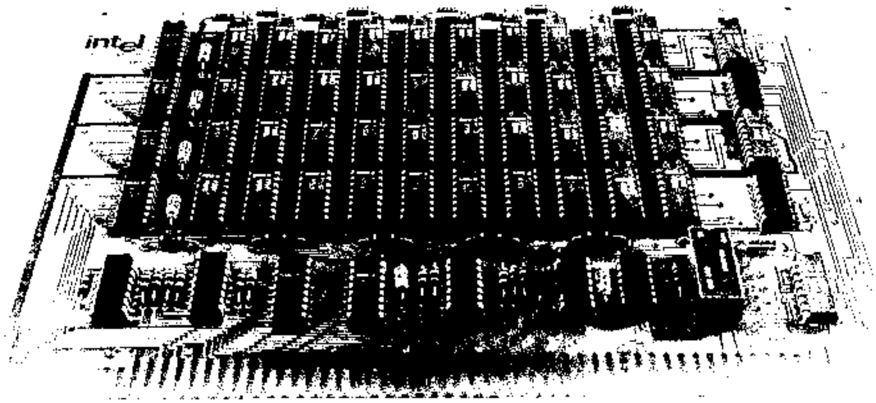
- Module Select
- Data Register (optional)
- Address Register
- Fast Cycle Time
- Byte Control (2 zones max)

Basic system available as 8K x 18 or 16K x 9.

Special Option:

Intel also offers the in-41E mounted in a card chassis either as a single or multiple card system.

in-50 MEMORY SYSTEM



in-50 SERIES RAM MEMORY FEATURES:

- **Low Cost Memory**
- **High Reliability**
- **Modular Expandability**
- **Module Interchangeability**
- **Fast Cycle Time**
- **Low Power Requirements**
- **Compact Size**
- **Field Expandable**
- **One Power Supply Voltage**
- **Fully Buffered System**

The in-50 RAM Memory System is designed to meet the needs of control memory, disk controllers, scratch pad and signal processing applications. This memory provides high reliability and performance at low costs through the use of all solid state integrated circuits. The in-50 utilizes Bipolar technology to achieve these fast cycle and access times.

This memory system features a basic size of 1024 words by 10 bits per memory card. This memory system can be expanded to any word or bit length by the use of additional memory cards. This system includes all address and data registers.

SYSTEM in-50 SPECIFICATIONS

Dimensions:

Memory Board:	8.175 Inches High
(1K X 10)	6.0 Inches Deep
	0.5 Inches Wide

Capacity:
256, 512 and 1024 words per memory card. Larger sizes are capable by the addition of memory cards.

Word Length:
2, 4, 6, 7, 8, 9, 10 bits per card. Longer words can be accomplished by the use of additional memory cards.

Cycle Time:

in-50	100 Nanoseconds
in-52	150 Nanoseconds

Access Time:

in-50	100 Nanoseconds
in-52	150 Nanoseconds

Operational Modes:
Read (NDRO)
Write

Interface Characteristics:
TTL Compatible
Standard Input Lines:
- Cycle Request
- Read/Write
- Write Data
- Address

Standard Output Lines:
- Data Available
- Read Data

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
	0 to 10,000 feet operating
Altitude:	Up to 50,000 feet non-operating

D.C. Power Requirement:

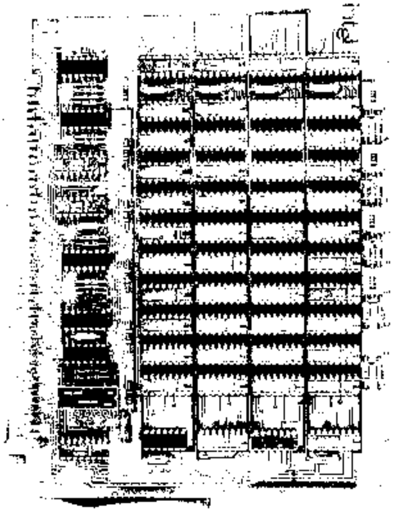
+5 Volts ±5%	5.5 Amps per memory card

Connector:

100 Pin, 125 mil centers	1 per memory card

Features:
- Module Select
- Address Registers
- Data Registers
- Single Board System
- Open Collector Outputs
- 1 Power Supply Voltage
- TTL Compatible
- Ease of Expansion

Inputs and Outputs are Buffered

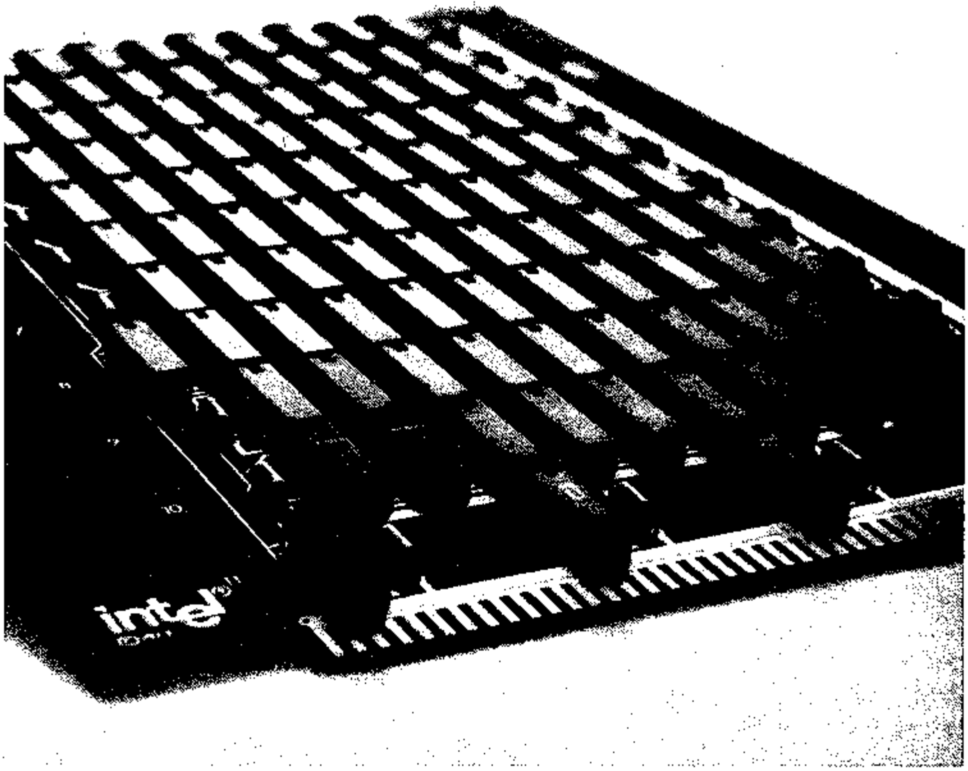


Special Features:
The in-50 is available in various word and bit lengths with card chassis completely wire wrapped with I/O connectors for mounting in 19" relay racks.

The in-50 can also be supplied with a power supply that is also mountable in a 19" relay rack.

Optional Features:
The standard in-50 has open collector outputs with pull-up resistors on the board.

in-60 MEMORY SYSTEM



in-60 SERIES SERIAL MEMORY FEATURES:

- **Low Cost Memory**
- **High Reliability**
- **Modular Expandability**
- **Module Interchangeability**
- **Field Expandable**
- **Only One Power Supply Voltage**
- **Compact Size**
- **Adjustable Clocking**
- **Fully Buffered**

The in-60 serial Memory System is designed to meet the high reliability and low cost requirements of large volume storage and CRT refresh applications. The in-60 features the use of a single voltage power supply and MOS N-channel silicon gate technology. This system is available as a self-contained 20,000 words by 10 bits memory unit. This system is expandable to virtually any size in either word or bit length by the use of additional memory cards. The in-60 features a compact size, high reliability and ease of expansion.

The in-60 is designed for the replacement of small flying head disks and for CRT refresh applications.

SYSTEM in-60 SPECIFICATIONS

Dimensions:

8.175 Inches High
10.5 Inches Deep
0.5 Inches Wide

Capacity:

Up to 20,000 words per memory card. Larger sizes are capable by the addition of memory cards.

Word Length:

6, 7, 8, 9, 10 bits per memory card. Longer words are made by combining memory cards.

Clock Rate:

in-60 1 megaHertz to 25 kiloHertz

Access Time:

in-60 500 Nanoseconds

Interface Characteristics:

TTL Compatible

Data Input:
Up to 10 lines, single ended

Data Output:
Up to 10 lines, single ended

Data Input Control:
1 line (clock), single ended

Environment:

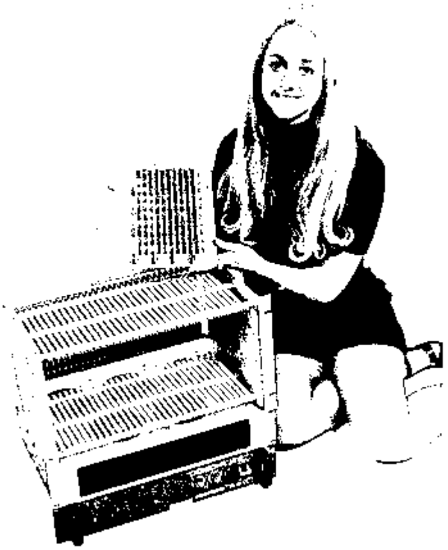
Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

D.C. Power Requirement:

+5.0 Volts ±5% at 7.0 Amps

Features:

TTL Compatible
1 Voltage Supply
Ease of Expansion
Single Board System
Adjustable Clocking
Single Phase Clocking
Fully Buffered System



Special Options:

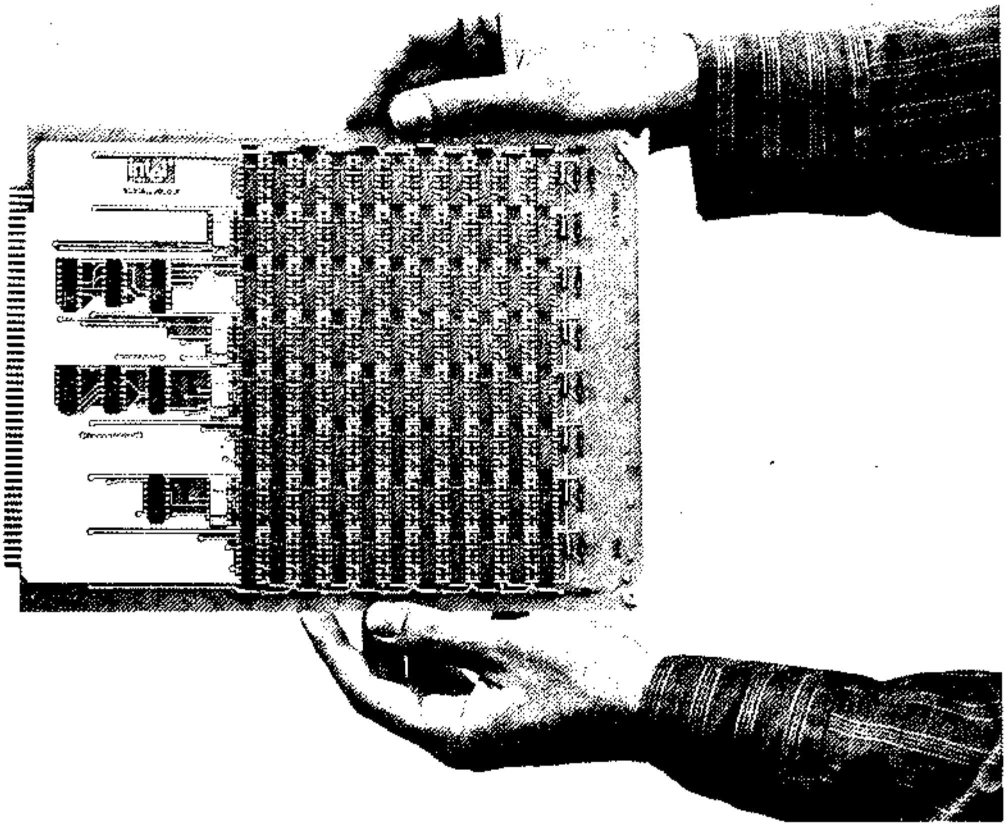
Intel also offers the in-60 mounted in a card chassis. This chassis will be wire-wrapped up to whatever size is ordered. This chassis will be able to be mounted in a 19" relay rack.

Intel will also supply a power supply for this system that mounts below the memory chassis. This supply is modular and can supply up to a full card chassis of memory.

A blower assembly is also available for this system. This blower can draw air from the front, back, or below for cooling the memory card chassis.

This is illustrated in the above photograph.

in-62 MEMORY SYSTEM



in-62 SERIES SERIAL MEMORY FEATURES:

- **Low Cost Memory**
- **High Reliability**
- **Modular Expandability**
- **Field Expandable**
- **Only One Power Supply Voltage**
- **Compact Size**
- **Adjustable Clocking**
- **Fully Buffered**

The in-62 serial Memory System is designed to meet the high reliability and low cost requirements of large volume storage and CRT refresh applications. The in-62 features the use of a single voltage power supply and MOS N-channel silicon gate technology. This system is available as a self-contained 88k words by 1 bit memory unit. This system is expandable to virtually any size in either word or bit length by the use of additional memory cards. The in-62 features a compact size, high reliability and ease of expansion.

SYSTEM in-62 SPECIFICATIONS

Dimensions:

8.175 Inches High
10.5 Inches Deep
0.5 Inches Wide

Capacity:

Up to 88,000 words per memory card. Larger sizes are capable by the addition of memory cards.

Word Length:

1 bit per memory card. Longer words are made by combining memory cards.

Clock Rate:

in-62 10MHz to 200kHz

Data Time:

in-62 10MHz to 200kHz

Interface Characteristics:

TTL Compatible
Data Input:
  1 line, single ended
Data Output:
  3 lines, single ended
  (Data Out, Data Out, Reg. Input)
Data Input Control:
  2 lines (clock), single ended
  (Collect/Recirculate, Clock)

Environment:

Temperature: 0°C to +50°C operating ambient
−40°C to +125°C non-operating
Relative Humidity: Up to 90%
with no condensation
Altitude: 0 to 10,000 feet operating
Up to 50,000 feet non-operating

DC Power Requirement:

+5.0 Volts ± 5% at 6.0 Amps

Features:

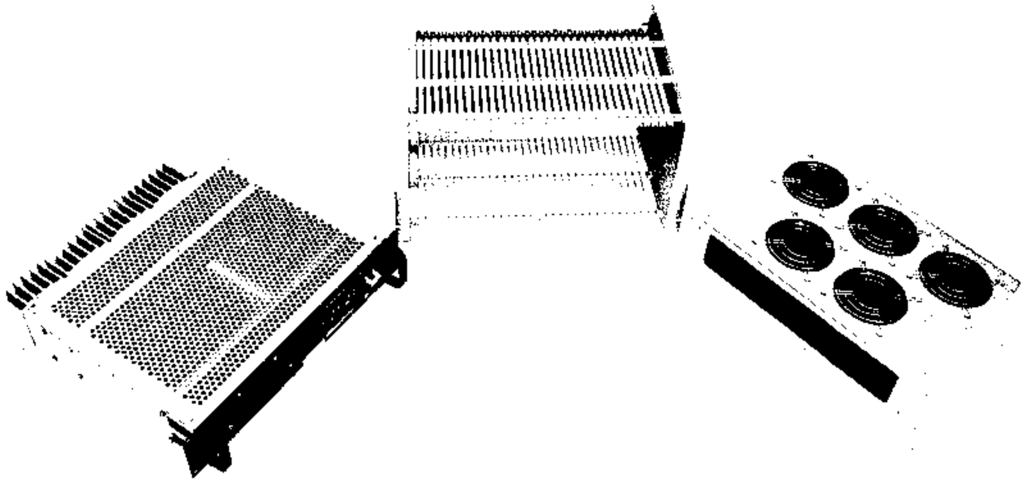
TTL Compatible
1 Voltage Supply
Ease of Expansion
Single Board System
Adjustable Clocking
Single Phase Clocking
Fully Buffered System

Special Options:

Intel also offers the in-62 mounted in a card chassis. This chassis will be wire-wrapped up to whatever size is ordered. This chassis will be able to be mounted in a 19" relay rack.

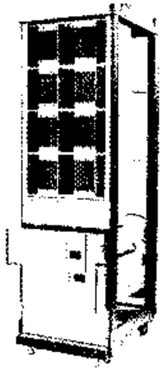
Intel will also supply a power supply for this system that mounts below the memory chassis. This supply is modular and can supply up to a full card chassis of memory.

A blower assembly is also available for this system. This blower can draw air from the front, back, or below for cooling the memory card chassis.



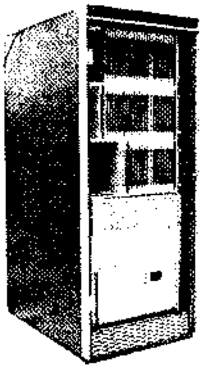
MEMORY CABINETS

The in-Series Memory Cards are available as individual units or as complete systems. Intel features a number of memory cabinets that can accommodate a variety of memory capacities. These cabinets are designed to allow customers maximum freedom in specifying memory configurations. These cabinets contain power supplies, cooling and interface connections. The following photographs show the various types that are available:

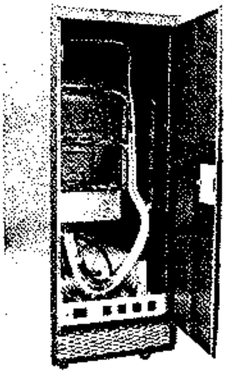


in-CAB-HB Memory Cabinet can accommodate up to 96 MU-10 series cards. This memory cabinet is 72" high, 19" wide and 30" deep. It is designed to be free-standing and contains room for cooling fans, power supplies and interface cabling. The memory size can vary from 48k x 144 to 512k x 18 bits. All power supplies are mounted on slides for easy access.

This shows the rear view of the in-CAB-HB memory cabinet. The memory chassis features PC back planes and is accessible from both front and back sides. Special power and interface connectors are mounted at the bottom of the cabinet for access through a false floor or rear.

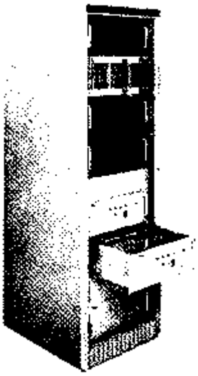


in-CAB-LB Memory Cabinet features a low profile with space for up to 32k x 128 bits of memory including power supplies and cooling. It is only 48" high x 30" deep and is 19" wide. It is free-standing and comes with casters for ease in moving the unit.



This shows the rear of the in-CAB-LB memory cabinet. All back planes, interface cables and power connections are easily accessible from the rear. There is also room for interface chassis to fit in the rear of the cabinet. All connections can go through the rear or bottom of this cabinet. A master circuit breaker is also available.

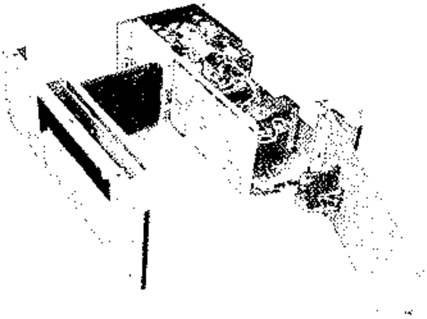
in-CAB-SHB Memory Cabinet features a capacity of up to 96k x 63 bits or 388k x 16 bits including power supplies and cooling. This cabinet is 70" high by 36" deep and is 19" wide. It is accessible from both front and rear. It is mounted on casters and has room in the rear for additional interface logic chassis.



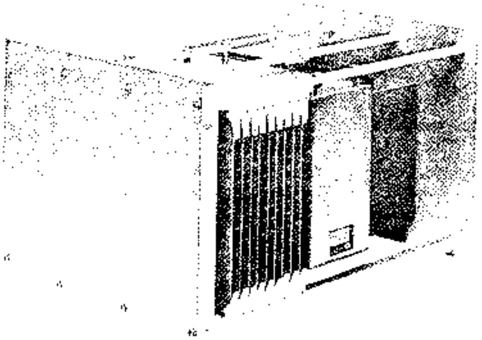
in-CAB-BHB Memory Cabinet features a capacity of up to 262k x 27 bits and includes space for power supplies with battery back-up capability including batteries for 1 hour back-up support. This cabinet is 80" high by 30" deep and is 19" wide. It is accessible from both the front and rear. It also contains its cooling fans and is free-standing with casters for ease of moving.

in-CHS CARD CHASSIS

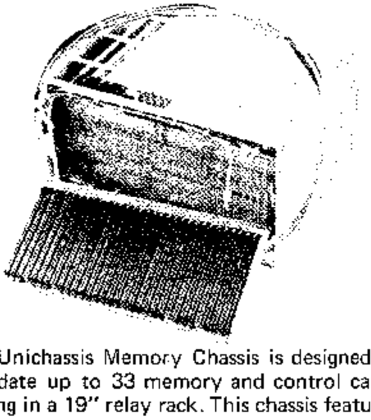
The in-Series Memory Systems are designed in modular form for ease in conversion into a variety of sizes and configurations. In order to accommodate customer applications, standard chassis were designed for use in fulfilling them. These are shown in the following photographs. See your local Intel sales representative for your particular application.



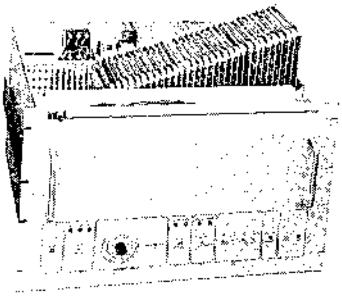
The in-Minichassis Memory Chassis is designed to accommodate up to 32k x 18 of memory. The memory cards are mounted horizontally with room for a control card and 1 UT-10 interface card. This mini-chassis is 7" high and includes power supplies and cooling fans. It is mounted on slides for ease of movement in and out. All connections are made from the rear of the unit and it is mountable in a 19" relay rack. A front panel is optional and includes a circuit breaker and indicator lights. This unit features the use of a PC back plane for all power and ground connections.



The in-Unichassis/OPS/BB Memory Chassis is designed to accommodate up to 32k x 18 of memory with battery back-up power supply and including a Gell cell battery. This chassis is mountable in a 19" relay rack. This chassis features a PC back plane for all power and ground connections. It is accessible from both front and rear. This chassis is 10.5" high and 12" deep.



The in-Unichassis Memory Chassis is designed to accommodate up to 33 memory and control cards for mounting in a 19" relay rack. This chassis features the use of a full PC back plane for power and ground. This chassis can be wired for a number of memory sizes and configurations. It can also be used in multiples for even larger memory configurations. It is 10.5" high, 12" deep, and can be used with in-CAB memory cabinet.



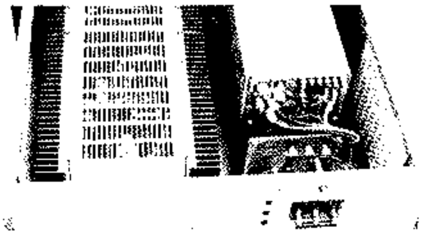
The in-Jumbochassis is designed for memory systems that may be mounted in a 24" cabinet. With integral power supplies and fan assemblies, it measures only 14"H x 24"W x 24"D. Forty-three card slots are available to house thousands of combinations of standard-sized Intel memory cards. This chassis has the capability of up to 10 megabits in 14". For instance, a 128k x 18 or 256k x 9 in-10 system or a 512k x 18 or 1024k x 9 in-40 system could be housed with seven I/O slots left over for address and data buffers or for other custom logic.

in-PS POWER SUPPLIES

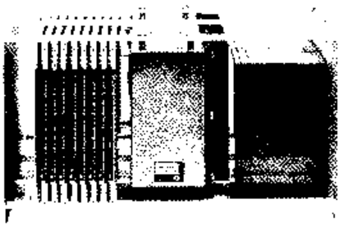
The in-Series Memory Systems are designed in modular form to allow conversion into a variety of sizes and configurations. In order to accommodate these various memory sizes, Intel has designed standard power supply modules for use in configuring these systems. The following photographs show standard power supply modules that are available. Contact your Intel Memory Systems representative for your particular application.

The in-OPS-3/BB Power Supply features a capacity to power up to 65k x 27 or 32k x 54 bits of Memory and has the capability of being powered by a battery in case of AC power failure. The battery back-up for a fully populated system is for a one hour period. This power supply is 8¾" high and is mountable in a 19" relay rack. It also has a circuit breaker switch and indicator light mounted on the front for easy use. It is recommended for use with the in-10 Series of memory.

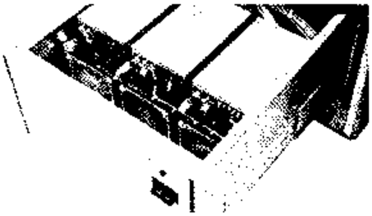
The in-DPS-3 Power Supply designed to provide voltage for up to 190k x 9 or 96k x 18 using individual supplies for each voltage level. This supply is 7" high and is 19" rack mountable. It features a circuit breaker and individual indicator lights mounted on the front. It also has its own internal cooling. It is recommended for use with the in-10 Series of memory.



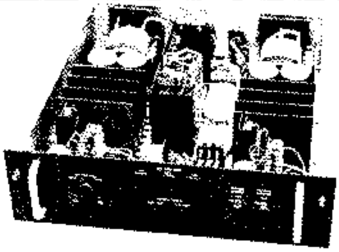
The in-DPS-5/2 Power Supply provides 1800 watts of power in two 8¾" drawers. Shown here are the V_{CC} + V_{SS} portion of the system. It is mountable in a 19" relay rack and has its own internal cooling. It is recommended for use with large in-10 Series memory systems.



The in-OPS-1 Power Supply is available in a 19" relay rack and it is shown mounted next to its memory and battery back-up. This power supply is capable of powering 32k x 18 or 65k x 9 (8 in-10) memory cards. This chassis with power supply is 10.5" high and 12" deep and includes memory system, power supply, and battery. It is recommended for use with the in-10 Series of memory.



The in-SPS-8 Power supply is a highly efficient power system designed to provide 1800 watts of power. This supply has +5.0V, –5.0V and +12.0V available and is contained in an 8¾" high chassis that is mountable in a 19" relay rack. It features its own internal cooling and is recommended for use with the in-60A memory systems.

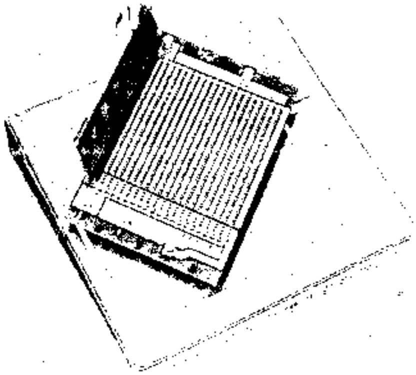


The in-DPS-U2 Power Supply features remote control options for power turn on and off, Voltage Margining, over-temperature sensing, and is only 5¼" high. Specially designed for use with the in-10 Series, it will power up to 65k x 18 of memory. All switches are located on the front of the unit for easy use. Mountable in a 19" relay rack.

The in-series is available in card chassis and with power supplies that are modular and can be mounted alongside, below, or behind the memory cards. Other accessories, like extender boards, interface boards and fan assemblies, are also available. Details on these are listed below.

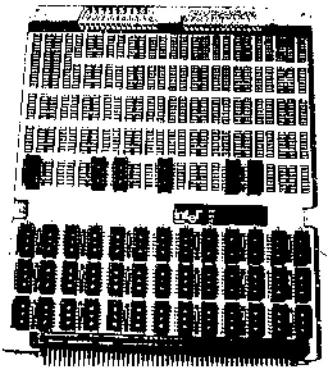
in-Series Interface Connector

This unique connector scheme is designed to provide inexpensive, yet reliable, interconnections to the in-Series memory systems. This connector fits over the in-Series back panel wire wrap pins and forms a tight interconnection. This connector is then fitted with flat cable for connection to other parts of the application with which it is being used.



in-10 Series Interface Board

This board is designed for use in assembling custom interfaces to use with in-10 series memory systems. This interface board can be used with I.C. sockets with up to 18 pins and can be wire-wrapped for quick interface connections. This I/O board plugs directly into the in-10 series connector slots. There are also 2 slots available for up to 40 pin sockets.

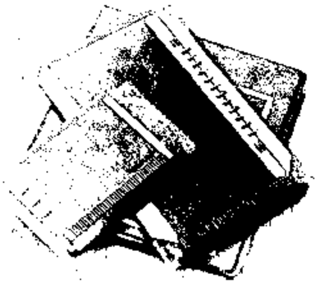


in-Series Fan Assembly

This fan assembly is designed for mounting in a 19" relay rack and is used for blowing air or sucking air upward through the in-series card chassis. This unit can receive air from the front, rear or underneath and send adequate air flow through up to 4 card chassis stacked upon each other.

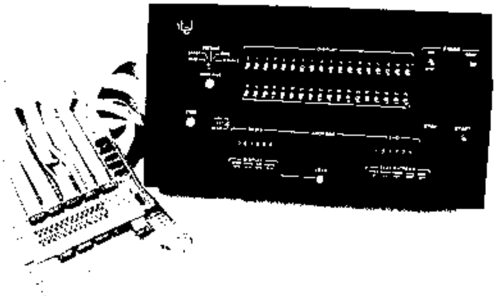
in-Series Extender Board

This extender board is designed to provide the user with full access to any in-series memory card. This extender board plugs directly into the back panel connector and allows full view of any of the in-series cards.

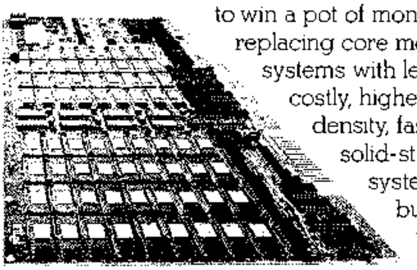


in-Series MT-10 System Exercisor

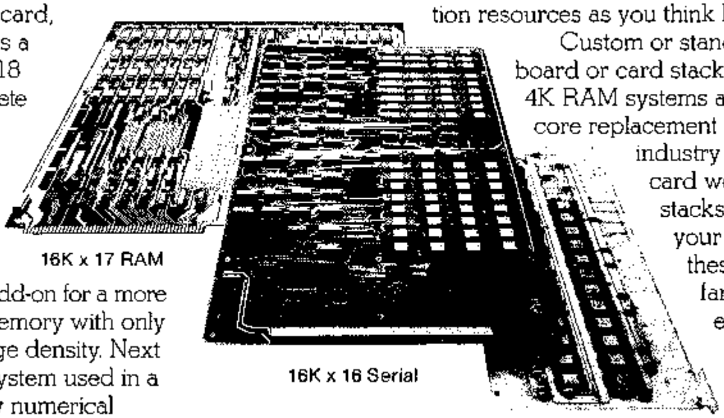
This system exercisor is designed to test up to 36 bits of information and address up to 262k words of memory. This tester is mountable on the front of the memory unit by use of self-contained magnetic devices and plugs directly into the memory system.



We stack the cards your way with 4K RAM systems.


16K x 18 RAM

Intel's know-how is all the ante you need to win a pot of money by replacing core memory systems with less costly, higher density, faster solid-state systems built with 4096-bit RAMs. Our know-how guarantees you price, performance and delivery right now.


16K x 17 RAM

16K x 16 Serial

4K x 16 Serial

Our first card, for example, is a custom 16Kx18 system, complete with control logic, that is now used in a popular minicomputer as a replacement add-on for a more costly core memory with only half the storage density. Next is a 16Kx17 system used in a high reliability numerical control system.

The center card is a custom 16Kx16 serial access RAM memory for a CRT display system. And the fourth operates in another display system as a 4Kx12 to 4Kx16 serial array It, too, replaces a bulkier, more costly core memory assembly.

For buyers of standard memory systems, our new ace in the hole is the *in-40*. One 8x10½-inch card stores up to 32 kilobytes in 4K RAMs, in your choice of word lengths, and accesses in only 350 nanoseconds. A universal control card allows expansion at any time to a 256 kilobyte capacity per control card. That stack is only 5 inches wide.

And here's another good deal. When you buy a custom memory system from Intel, you can get manufacturing rights after the initial production run. Use your production resources as you think best.

Custom or standard, single board or card stack, Intel's 4K RAM systems are the best core replacement deal in the industry today. Every card we make stacks the deal in your favor because these systems are far more cost-effective than core in density, performance and price.

Call or write Intel Memory Systems at 1302 North Mathilda, Sunnyvale, California 94086. (408) 734-8102.

Memory Options Unlimited

intel memory systems

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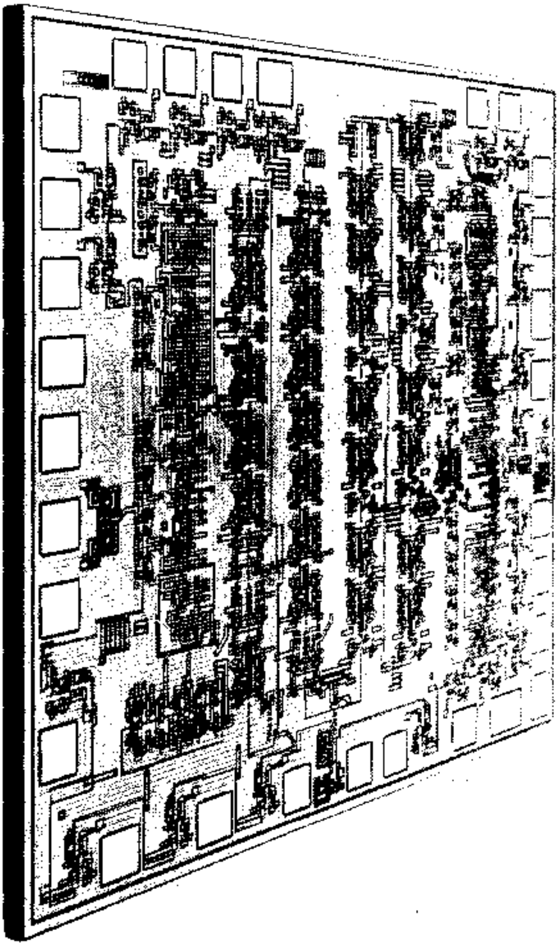
8

TIMEKEEPING CIRCUITS



CMOS TIMEKEEPING CIRCUITS

Type	Description	Display Type	Voltage Range	Page No.
5201	3 1/2 Digit Hours/Minutes/Seconds Decoder – Driver	D.S. LCD	10-15	8-3
5201-2	3 1/2 Digit Hours/Minutes/Seconds Decoder – Driver	F.E. LCD	6-10	8-3
5202	3 1/2 Digit Hours and Minutes Decoder – Driver	D.S. LCD	10-15	8-3
5202-2	3 1/2 Digit Hours and Minutes Decoder – Driver	F.E. LCD	6-10	8-3
5204	3 1/2 Digit Time/Seconds/Date Decoder – Driver	F.E. LCD	6-10	8-7
5801	32,768kHz Oscillator – Divider	N.A.	1.2-1.6	8-11

intel® Silicon Gate CMOS **5201, 5201-2, 5202, 5202-2**

LIQUID CRYSTAL DISPLAY DECODER-DRIVER

- **5201 and 5202 Drive Dynamic Scattering Displays**
- **5201-2 and 5202-2 Drive Field Effect Displays**
- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **5201 and 5201-2 Display Hours, Minutes and Seconds on Command**
- **5202 and 5202-2 Display Hours and Minutes**
- **Inputs Protected Against Static Discharge**

The 5201, 5201-2, 5202, and 5202-2 are low power 3½ digit liquid crystal display decoder/drivers intended for use in electronic timekeeping applications such as wristwatches and battery-operated clocks. The 5201 and 5202 are specified for operation over the supply voltage range 10 to 15 volts for use with dynamic scattering liquid crystal displays. The 5201-2 and 5202-2 are specified for operation from 6 to 10 volt supply voltages for use with field effect liquid crystal displays.

The 5201 and 5201-2 normally display hours and minutes. On activation of the seconds command switch, seconds are displayed in the minutes position and hours are blanked. Resetting of the seconds command switch restores the display mode to hours and minutes. The 5202 and 5202-2 display hours and minutes only. The colon is flashed at a 1 Hz rate on all four devices.

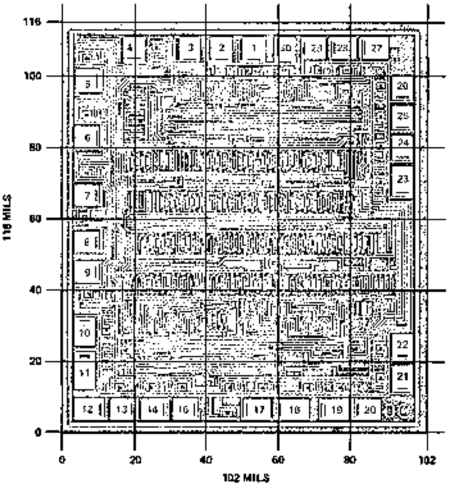
These decoder/drivers accept a 64 Hz input signal from which they count and decode hours and minutes (and seconds in the case of the 5201 and 5201-2). The decoded signals are used for driving the three 7-segment and one 2-segment display digits. A symmetrical 32 Hz signal is provided to drive the common back plate of the display. Segments to be energized are driven with a symmetrical 32 Hz signal that is out-of-phase with the common signal while unenergized segments are driven with a symmetrical 32 Hz signal in phase with the common signal.

Two inputs allow for time setting and resetting. (See page 8-5 for description of operation.)

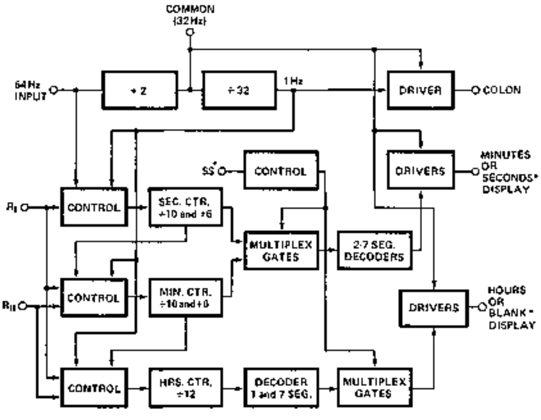
These devices are fabricated with complementary MOS silicon gate technology. This extremely low power technology is ideally suited for the manufacture of devices designed to operate from small batteries for long periods of time.

CHIP TOPOGRAPHY

(Numbers refer to package pin number.)



BLOCK DIAGRAM



(*5201 AND 5201-2 ONLY)

Absolute Maximum Ratings*

Temperature Under Bias . . . . −20°C to +70°C
Storage Temperature . . . . −40°C to +125°C
Supply Voltage V_{DD} with respect to GND . . . . −0.3V to +18.0V
Voltage on all Inputs or Outputs with respect to GND . . . . −0.3V to V_{DD} +0.3V
Power Dissipation 100mW

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics for 5201 and 5202

Dynamic Scattering Liquid Crystal Display Applications (T_A = 25°C; 10V ≤ V_{DD} ≤ 15V; f_{IN} = 64 Hz unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}(Avg.)	Average Operating Current			500	nA	V_{DD} = 15V; t_{pwc} = 25μs; t_f = 0.5μs; t_r = 35μs; outputs open
I_{DD}(Static)	Static Current			300	nA	V_{DD} = 15V; 64 Hz input open; outputs open
I_{IL}	Input Low Current	−5	−13	−28	μA	V_{DD} = 15V; V_{IN} = 1.2V
V_{IL}	Input Low Voltage	−0.3		1.2	V	V_{DD} = 15V
V_{IH}	Input High Voltage	14.0		15.3	V	V_{DD} = 15V
V_{OLC}	Output Low Voltage Common			0.1 0.1	V V	V_{DD} = 15V; I_{OLC} = 1.5μA V_{DD} = 10V; I_{OLC} = 1.0μA
V_{OHC}	Output High Voltage Common	14.9 9.9			V V	V_{DD} = 15V; I_{OHC} = −1.5μA V_{DD} = 10V; I_{OHC} = −1.0μA
V_{OLS}	Output Low Voltage Segments			0.1 0.1	V V	V_{DD} = 15V; I_{OLS} = 0.1μA V_{DD} = 10V; I_{OLS} = 0.06μA
V_{OHS}	Output High Voltage Segments	14.9 9.9			V V	V_{DD} = 15V; I_{OHS} = −0.1μA V_{DD} = 10V; I_{OHS} = −0.06μA

D.C. and Operating Characteristics for 5201-2 and 5202-2

Field Effect Display Applications (T_A = 25°C; 6V ≤ V_{DD} ≤ 10V; f_{IN} = 64 Hz unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{DD} (Avg.)	Average Operating Current			600	nA	V_{DD} = 10V; t_{pwc} = 25μs; t_f = 0.5μs; t_r = 75μs; outputs open
I_{DD} (Static)	Static Current			400	nA	V_{DD} = 10V; 64 Hz input open; outputs open
I_{IL}	Input Low Current	−0.5	−1.5		μA	V_{DD} = 6.0V; V_{IN} = 1.2V
V_{IL}	Input Low Voltage	−0.3		1.2	V	V_{DD} = 10V
V_{IH}	Input High Voltage	9.0		10.3	V	V_{DD} = 10V
V_{OLC}	Output Low Voltage Common			25 50	mV mV	V_{DD} = 10V; I_{OLC} = 0.15μA V_{DD} = 6V; I_{OLC} = 0.1μA
V_{OHC}	Output High Voltage Common	9.975 5.950			V V	V_{DD} = 10V; I_{OHC} = −0.15μA V_{DD} = 6V; I_{OHC} = −0.1μA
V_{OLS}	Output Low Voltage Segments			25 50	mV mV	V_{DD} = 10V; I_{OLS} = 10nA V_{DD} = 6V; I_{OLS} = 6nA
V_{OHS}	Output High Voltage Segments	9.975 5.950			V V	V_{DD} = 10V; I_{OHS} = −10nA V_{DD} = 6V; I_{OHS} = −6nA

A.C. Characteristics for 5201 and 5202 ($T_A = 25°C$; $f_{in} = 64Hz$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	Input Pulse Width	10	15	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time			0.5	μs	$V_{IL} = 1.2V$; $V_{IH} = 14V$; $V_{DD} = 15V$
t_r	Input Pulse Rise Time			35	μs	$V_{IL} = 1.2V$; $V_{IH} = 14V$; $V_{DD} = 15V$

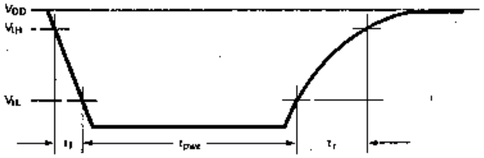
A.C. Characteristics for 5201-2 and 5202-2 ($T_A = 25°C$; $f_{in} = 64Hz$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	Input Pulse Width	10	15	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time			0.5	μs	$V_{IL} = 1.2V$; $V_{IH} = 14V$; $V_{DD} = 15V$
t_r	Input Pulse Rise Time			75	μs	$V_{IL} = 1.2V$; $V_{IH} = 9V$; $V_{DD} = 10V$

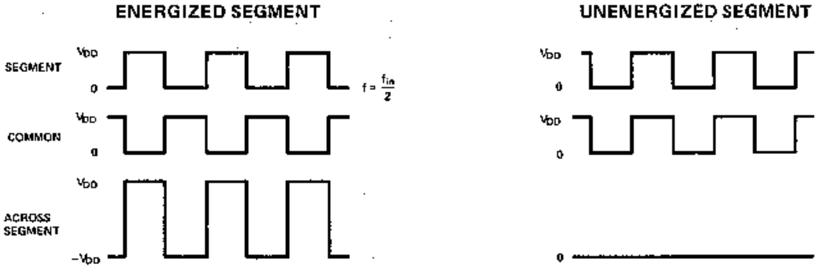
Capacitance ($T_A = 25°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		2.8	5	pF	Capacitances are measured in 30 lead flatpack with all pins except the test pin at ground, f = 1MHz.
C_{OUT_C}	Output Capacitance Common		8.5	15	pF	
C_{OUT_S}	Output Capacitance Segments		2.0	5	pF	

Input Waveform



Output Waveforms

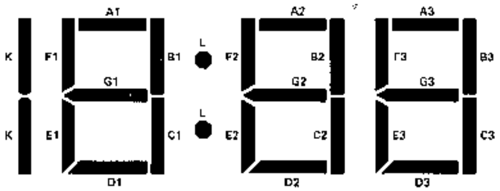


Time Setting

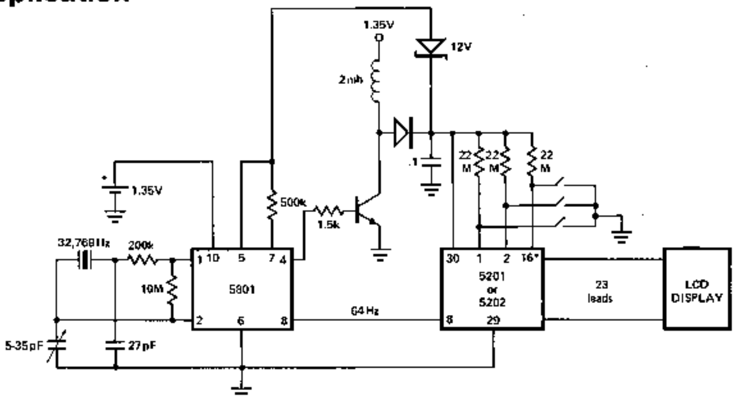
Two inputs (Reset I and Reset II) allow setting and synchronization of the time to a time standard. The operation of these two inputs is described by the following table:

State	Reset I	Reset II	Operation
B_1	V_{DD}	V_{DD}	Normal
B_2	V_{DD}	0	Clock Running, hours are advanced at 1Hz
B_3	0	0	Seconds counter is reset to 00 sec.; minutes are advanced at 1Hz rate; hours are incremented by 1 if minutes exceed 59, otherwise they are unaffected.
B_4	0	V_{DD}	Seconds counter reset to 00 sec.; minutes are held if state B_4 is entered directly from state B_3; hours are unaffected. Note: Minutes will be incremented by one if state B_4 is entered from state B_1 or B_2.

Display Segment Format

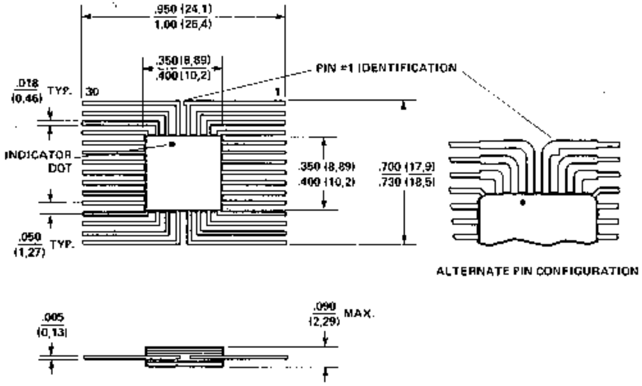


Typical Application



(*5201, 5201-2 ONLY)

Packaging Information



PIN ASSIGNMENT

Pin No.	Function	Pin No.	Function
1	Reset II	16	Seconds Switch*
2	Reset I	17	B3
3	Common	18	A3
4	K	19	F3
5	E1	20	G3
6	D1	21	B2
7	C1	22	A2 + D2
8	64Hz In	23	F2
9	L (Colon)	24	G2
10	E2	25	B1
11	C2	26	A1
12	E3	27	F1
13	D3	28	G1
14	C3	29	Ground
15	N/C	30	V_{DD}

*5201 and 5201-2 only

intel® Silicon Gate CMOS 5204

TIME/SECONDS/DATE LIQUID CRYSTAL DISPLAY DECODER-DRIVER

- **Displays Hours and Minutes or Seconds or Date**
- **Pin Compatible with Intel 5201 and 5202**
- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **Anti-Bounce Circuitry on Switch Inputs**
- **Drives 3½ Digit Field Effect Displays**
- **Inputs Protected Against Static Discharge**

The 5204 is a low power 3-½ digit liquid crystal display decoder driver intended for use in 12 hour timekeeping applications such as wristwatches and battery-operated clocks.

The 5204 accepts a 64 Hz input signal from which it counts and decodes Seconds, Minutes, Hours, and Date. The decoded signals are used for driving the three 7-segment and one 2-segment display digits. A symmetrical 32 Hz signal is provided to drive the common back plate of the display. Segments to be energized are driven with a symmetrical 32 Hz signal that is out-of-phase with the common signal while unenergized segments are driven with a 32 Hz signal in phase with the common signal.

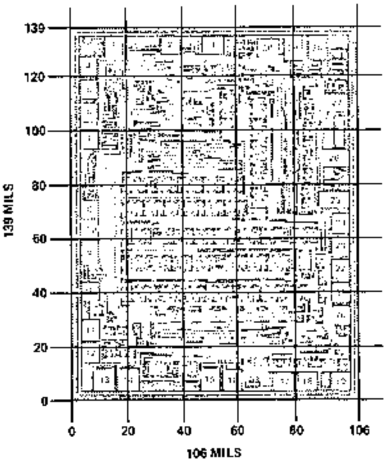
The 5204 will normally display Hours and Minutes. Depression of the D/C command switch will cause Seconds to be displayed in the Minutes position and the Hours will be blanked. A second depression of the D/C command switch will cause the Date to be displayed in the Minutes position and the Hours to be blanked. A third depression of the D/C command switch will cause a return to normal mode displaying Hours and Minutes. The colon is flashed at a 1 Hz rate in all three display modes. A separate switch is used for timesetting. Thus only two switches are required for operation of the watch. (See page 8-9 for description of operation.)

The 5204 is designed to operate in conjunction with the 5801 oscillator-divider circuit. For information on the 5801 see the 5801 data sheet.

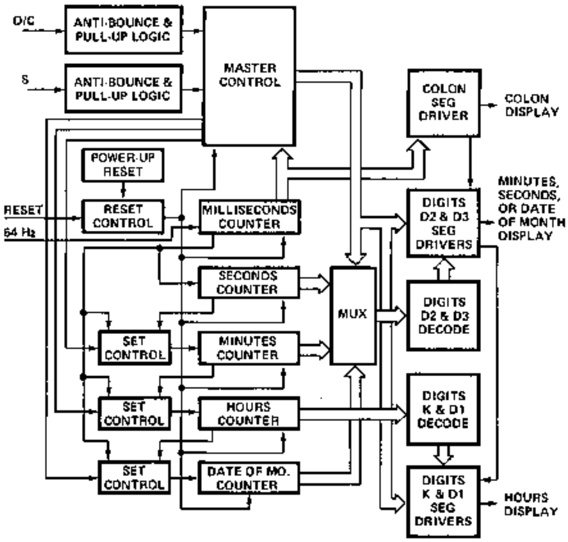
This device is fabricated with complementary MOS silicon gate technology. This extremely low power technology is ideally suited for the manufacture of devices designed to operate from small batteries for long periods of time.

CHIP TOPOGRAPHY

(Numbers refer to package pin number.)



BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−20°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{DD} with respect to GND	−0.3V to +18.0V
Voltage on all Inputs or Outputs with respect to GND	−0.3V to V_{DD} +0.3V
Power Dissipation	100mW

***COMMENT:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 25°C$; $6V \leqslant V_{DD} \leqslant 10V$; $f_{in} = 64$ Hz, Unless Otherwise Specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
I_{DD}	Total Average Internal Current		500	nA	$V_{DD} = 10V$; $t_{pwc} = 25\mu s$; $t_f = 0.5\mu s$; $t_r = 75\mu s$; Outputs Open
I_{ILC}	64 Hz Input Low Current (Clock)	2.0	-15	μA	$V_{DD} = 10V$; $V_{IN} = 1.2V$
I_{ILS}	Switch Input Low Current (D/C, S)	-1.0	-50	μA	$V_{DD} = 10V$; $V_{IN} = 1.2V$ 64 Hz Input Voltage = 0.0V Note 1
V_{IL}	Input Low Voltage	-0.3	1.2	V	
V_{OLC}	Output Low Voltage Common		25	mV	$V_{DD} = 10V$; $I_{OLC} = 1.0\mu A$
V_{OHC}	Output High Voltage Common	V_{DD}-.025		V	$V_{DD} = 10V$; $I_{OHC} = -1.0\mu A$
V_{OLS}	Output Low Voltage Segment		25	mV	$V_{DD} = 10V$; $I_{OLS} = 0.1\mu A$
V_{OHS}	Output High Voltage Segment	V_{DD}-.025		V	$V_{DD} = 10V$; $I_{OHS} = -0.1\mu A$
I_{ILR}	Reset Input Low Current	-1.0	-200	μA	$V_{DD} = 10V$

A.C. Characteristics

$T_A = 25°C$; $6V \leqslant V_{DD} \leqslant 10V$; $f_{in} = 64$ Hz, Unless Otherwise Specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{pwc}	Input Pulse Width (Clock)	10	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time		0.5	μs	$V_{DD} = 10V$; $V_{IL} = 1.2V$; $V_{IH} = 9V$
t_r	Input Pulse Rise Time		75	μs	$V_{DD} = 10V$; $V_{IL} = 1.2V$; $V_{IH} = 9V$
t_{sd}	Switch Delay	32	80	ms	Note 2

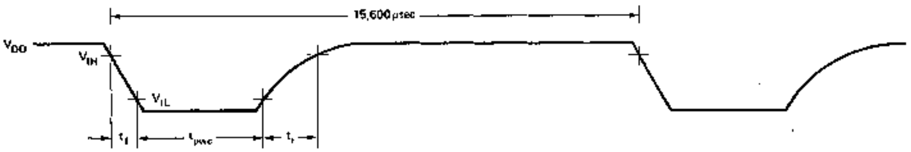
Capacitance ($T_A = 25°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		2.8	5	pF	Capacitances are measured in 30 lead flatpack with all pins except the test pin at ground, f = 1MHz.
C_{OUT_C}	Output Capacitance Common		8.5	15	pF	
C_{OUT_S}	Output Capacitance Segments		2.0	5	pF	

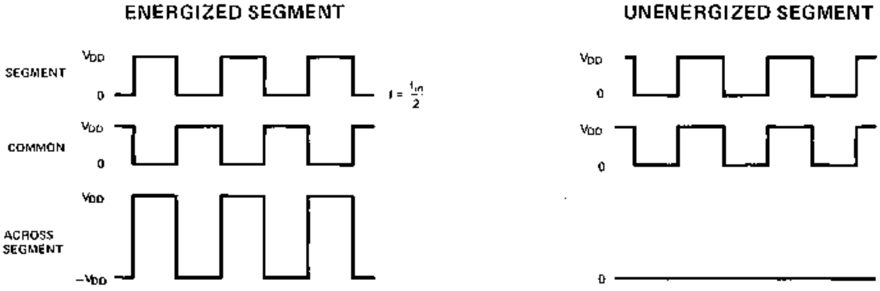
NOTES: 1. All switch inputs include dynamic pull-up circuitry which is clocked in synchronization with the 64 Hz input. The average current drawn by these inputs in the low state will be proportional to the duty cycle of the 64 Hz input. The value specified is for the case where the 64 Hz input is held low. (100% duty cycle).

2. The D/C and S switch inputs include anti-bounce circuitry. This circuitry requires that a switch input be stable for 2 consecutive 32 Hz clock periods in order to be recognized as a valid input. Switch delay is the time during which the antibounce circuitry is determining a valid, stable input.

Input Waveform

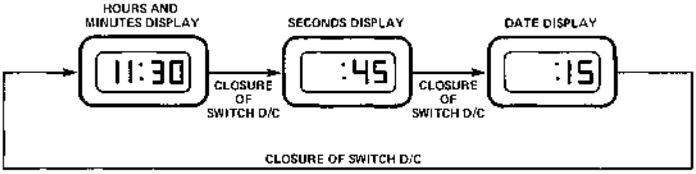


Output Waveforms



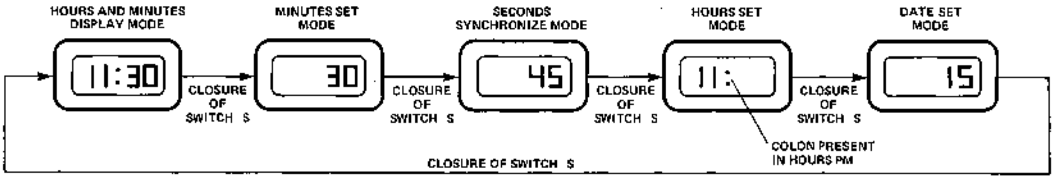
Time Display

Switch input D/C controls the time display modes. Each closure of switch D/C (D/C input = low) causes a change in the display mode in the sequence Hours and Minutes → Seconds → Date → Hours and Minutes. The following diagram illustrates this:



Time Setting

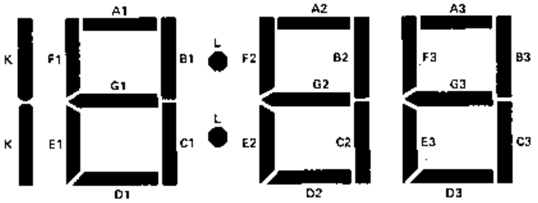
Switch input S controls the time setting modes. This switch input is active only when the circuit is in the Hours and Minutes display mode. Each closure of switch S (S input = low) causes a change in the time set modes in the sequence Hours and Minutes → Minutes → Seconds → Hours → Date → Hours and Minutes. *Closure of switch D/C when in the Minutes, Hours, or Date time set modes will cause that mode to be advanced at a 1 Hz rate. Closure of switch D/C in the Seconds synchronize mode will cause the Minutes to be advanced by one and the Seconds to be reset to zero and held until the D/C input is returned high.* The colon is displayed only in the Hours PM state in the time set mode. The following diagram illustrates this:



Reset

The reset input may be used to initialize all time counters to the zero state. All time counters are automatically reset to zero when voltage is initially applied to the circuit. The zero state is 12:00 AM, 00 Seconds, 0 Date.

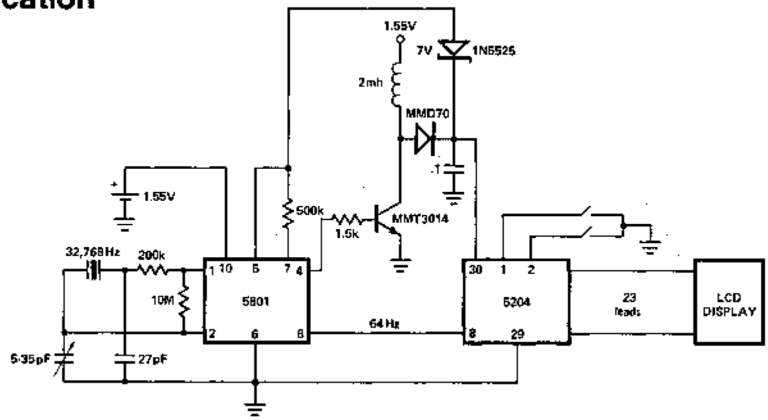
Display Segment Format



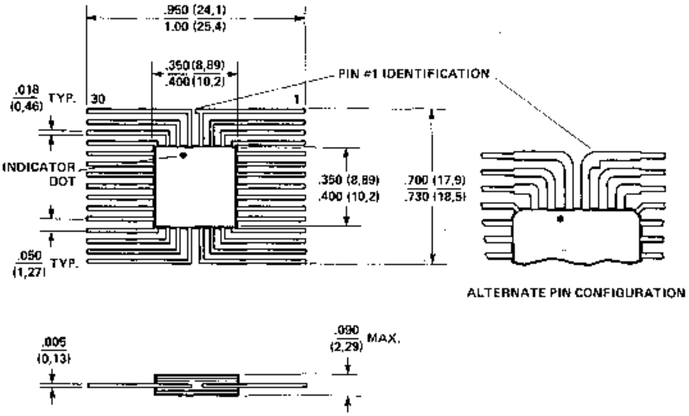
DIGITS D1, D2 AND D3 TRUTH TABLE

NUMBER	SEGMENTS						
	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Typical Application



Packaging Information



PIN ASSIGNMENT

Pin No.	Function	Pin No.	Function
1	D/C	16	N/C
2	S	17	B3
3	Common	18	A3
4	K	19	F3
5	E1	20	G3
6	D1	21	B2
7	C1	22	A2 + D2
8	64 Hz In	23	F2
9	L (Colon)	24	G2
10	E2	25	B1
11	C2	26	A1
12	E3	27	F1
13	D3	28	G1
14	C3	29	Ground
15	Reset	30	V_{DD}

intel Silicon Gate CMOS **5801**

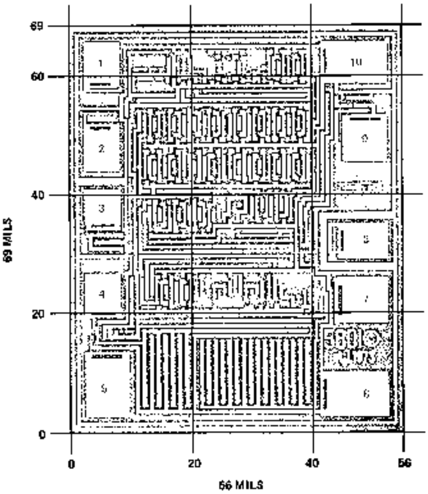
LOW POWER OSCILLATOR-DIVIDER

- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **On Chip Drive and Regulator Circuitry for Up-Converter**
- **Long Battery Life--Low Current Drain--5 μA max.**
- **Inputs Protected Against Static Discharge**

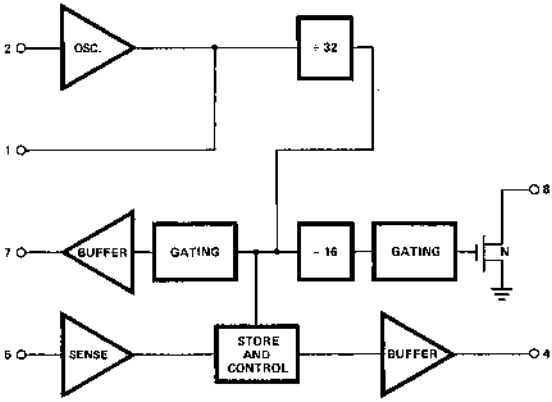
The 5801 is a low power oscillator and 2^9 divider ideally suited for use in battery powered timekeeping applications. The circuitry consists of an inverter stage designed to operate in conjunction with an external quartz crystal and feedback network to form an oscillator, a 9-stage binary ripple carry counter, and control logic. Two outputs are provided: A buffered drive output providing ½ cycle of the oscillator at a repetition rate equal to the frequency of the oscillator divided by 2^5 and an open drain output that is switched on for ½ cycle of the oscillator at a repetition rate of the oscillator divided by 2^9. The buffered drive output and associated control circuitry are designed for use with external components to implement a regulated voltage up-converter.

The 5801 is manufactured with complementary MOS silicon gate technology. Long term continuous operation from small batteries is made possible by use of this low power technology.

CHIP TOPOGRAPHY
(Numbers refer to package pin number.)



BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−20°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage (V_{DD})	−0.3V to +8.0V
Voltage on Output (pin 8) with respect to V_{SS}	−0.3V to +18.0V
Voltage on all other pins	−0.3V to V_{DD} +0.3V
Power Dissipation	80mW

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics ($T_A = 25°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{DD}	Average Supply Current		3.0	5.0	μA	V_{DD} = 1.4V, Note 1
V_{DDS}	Oscillation Start Voltage	1.2			V	Note 1
I_{OLC}	64 Hz N-Channel Open Drain Output Current	50			μA	V_{DD} = 1.2V; V_{OLC} = 1.2V
I_{OHD}	1024 Hz Drive P-Channel Output Current	−500			μA	V_{DD} = 1.2V; V_{OHD} = 0.7V
I_{OLD}	1024 Hz Drive N-Channel Output Current	200			μA	V_{DD} = 1.2V; V_{OLD} = 0.5V
I_{OLS}	1024 Hz Sample N-Channel Output Current	10			μA	V_{DD} = 1.2V; V_{OLS} = 0.15V
V_{IL}	Sense Low Input Voltage			0.4	V	V_{DD} = 1.2V
V_{IH}	Sense High Input Voltage	0.9			V	V_{DD} = 1.2V
V_{BDC}	64 Hz N-Channel Breakdown Voltage	15.0			V	V_{DD} = 1.2V; I_{BDC} = 1.0μA

Note 1. Frequency of oscillation = 32,768 Hz when connected as shown in Figure 1.

Test Circuit

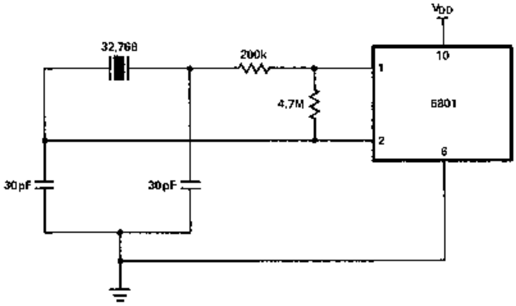


Figure 1.

A.C. Characteristics $T_A = 25°C$

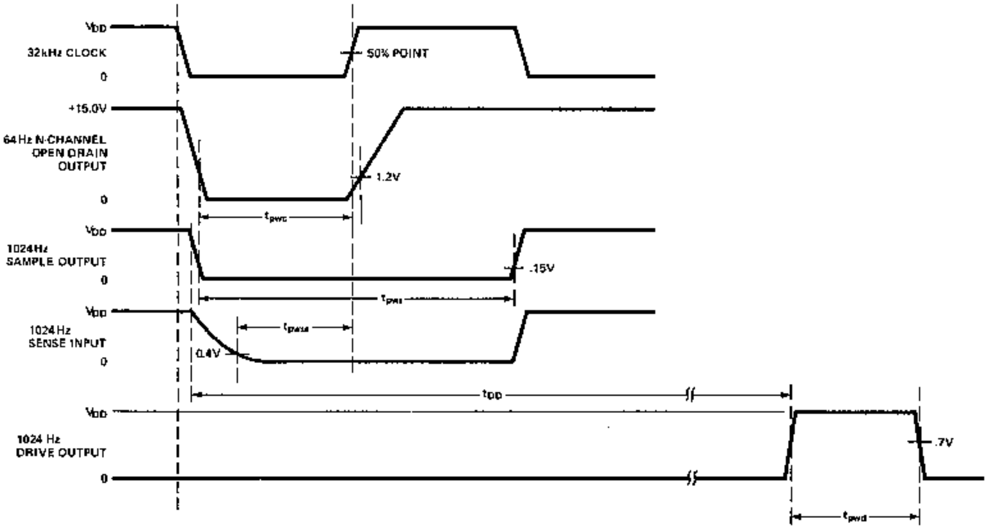
Symbol		Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	64Hz N-Channel Open Drain Output Pulse Width	10		25	μs	V_{DD} = 1.2V, 1.4V; 64Hz
t_{pws}	1024Hz Sample Output Pulse Width	25		35	μs	V_{DD} = 1.2V, 1.4V; 1024Hz
t_{pwd}	1024Hz Drive Output Pulse Width	13		17	μs	V_{DD} = 1.2V, 1.4V; 1024Hz
t_{dd}	1024Hz Sample Output to Drive Output Delay	485		520	μs	V_{DD} = 1.2V, 1.4V; 1024Hz
t_{pwse}	1024Hz Sense Input Pulse Width	5			μs	V_{DD} = 1.2V, 1.4V; 1024Hz

Capacitance

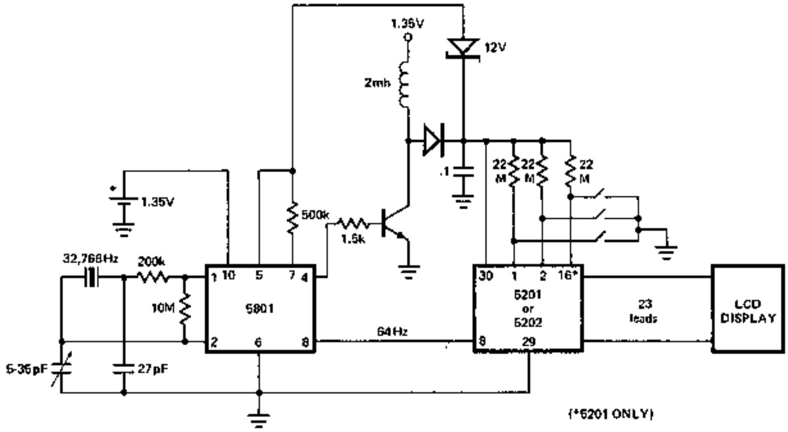
Symbol	Test	Typ.	Max.	Unit
C_{IN2}	Input Capacitance at pin 2 V_{IN} = 0V	3.2	8.0	pF
C_{IN5}	Input Capacitance at pin 5 V_{IN} = 0V	2.2	6.0	pF
C_{OUT1}	Output Capacitance at pin 1 V_{OUT} = 0V	3.0	8.0	pF
C_{OUT4}	Output Capacitance at pin 4 V_{OUT} = 0V	23	35	pF
$C_{OUT\ 7,8}$	Output Capacitance at pins 7,8; V_{OUT} = 0V	2.4	6.0	pF

Note: All capacitance values are measured in 10 lead flatpack with pins 6, 10 and all other untested pins tied to ground.

Timing Diagram

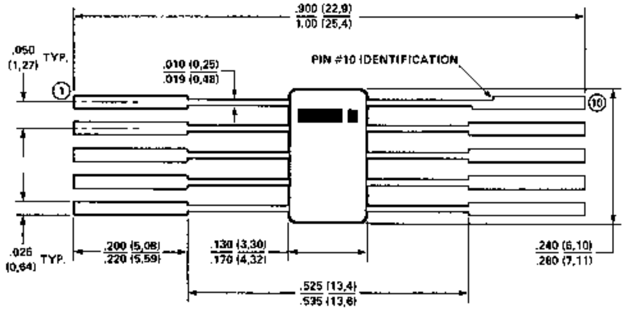


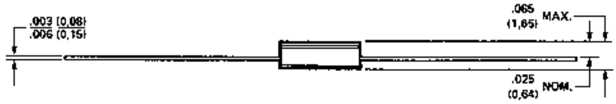
Typical Application



(*5201 ONLY)

Packaging Information





PIN ASSIGNMENT

Pin #	Function
1	OSC INV OUT
2	OSC INV IN
3	N/C
4	1024 Hz OUT (Drive)
5	1024 Hz IN (Sense)
6	GROUND
7	1024 Hz OUT (Sample)
8	64 Hz OUT (N-CH)
9	N/C
10	V_{DD}

TIMEKEEPING CIRCUITS

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