intel®

Microcomputer Memory — Silicon Gate MOS

4702A REPROGRAMMABLE 2K PROM

The 4702A is a 256 word by 8 bit electrically programmable ROM ideally suited for microcomputer system development where fast turn-around and pattern experimentation are important. The 4702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The 4702A is packaged in a 24 pin dual-in-line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

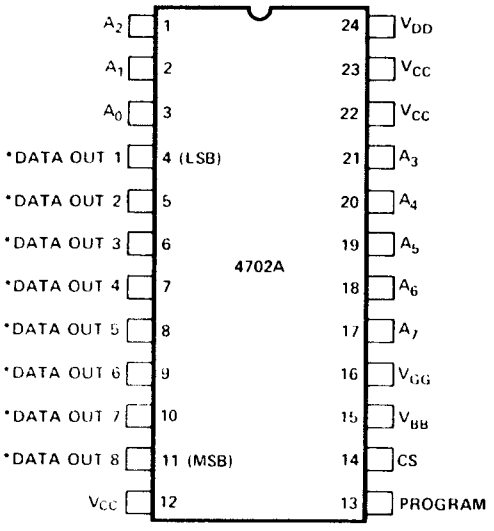
The circuitry of the 4702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302A, is ideal for large volume production runs of systems initially using the 4702A.

The 4702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

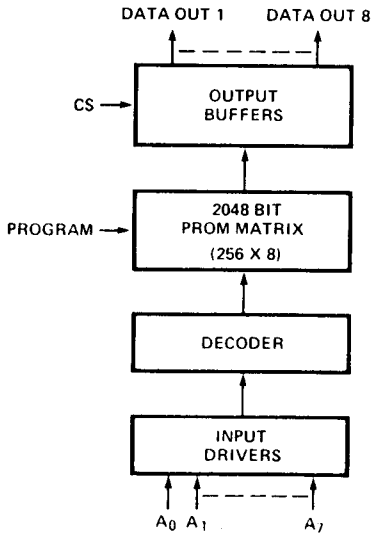
- **Access Time — 1.7 μsec Max.**
- **Fast Programming — 2 Minutes for all 2048 Bits**
- **Ultraviolet Erasable and Electronically Reprogrammable**
- **Fully Decoded, 256 x 8 Organization**
- **Static MOS — No Clocks Required**
- **Inputs and Outputs TTL Compatible**
- **Three State Output — OR-Tie Capability**
- **Simple Memory Expansion Chip Select Input Lead**

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.

BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
CS	CHIP SELECT INPUT
DO_1-DO_8	DATA OUTPUTS

PIN CONNECTIONS

The external lead connections to the 8702A differ, depending on whether the device is being programmed[1] or used in read mode. (See following table.)

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = -10V±5%, V_{GG}[2] = -10V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[3]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			10	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		6	14	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC} −2, I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		39	54	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		36	50	mA	$\overline{CS}$=0.0, I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		43	63	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
						Continuous Operation
I_{GG}	Gate Supply Current			10	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} 0.45V
V_{OL}	Output Low Voltage		7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −100 µA

Note 1: In the programming mode, the data inputs 1–8 are pins 4–11 respectively. $\overline{CS}$ = GND.
Note 2: V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle. (See p. 5)
Note 3: Typical values are at nominal voltages and T_A = 25°C.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = -10V±5%, V_{GG} = -10V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay			1.7	µs
t_{DVGG}	Clocked V_{GG} set up	1.0			µs
t_{CS}	Chip select delay			800	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	µs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

CAPACITANCE* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

* This parameter is periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

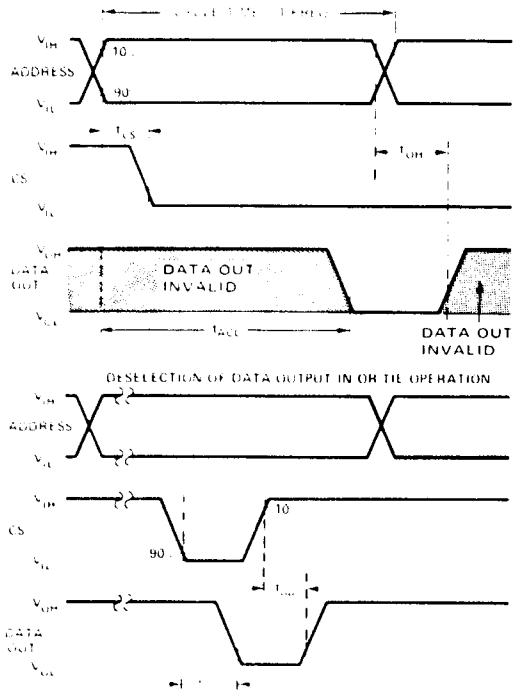
Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns.

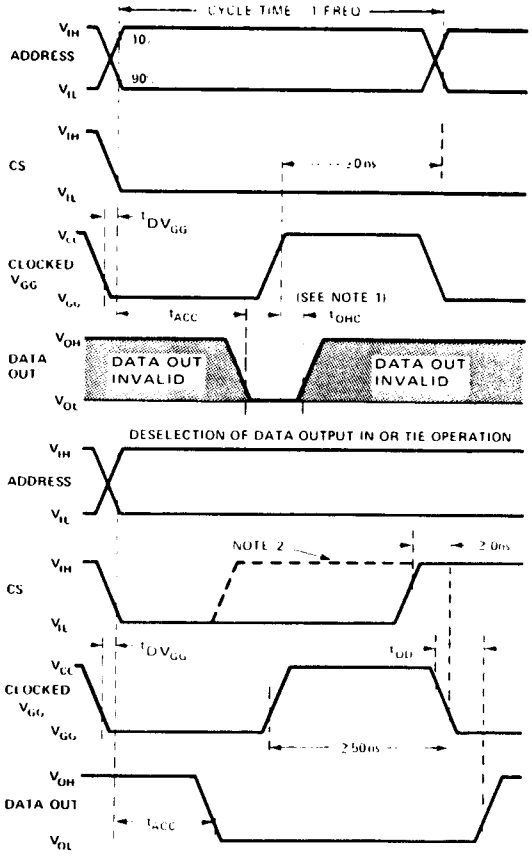
a) For output load = 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

b) For pure capacitive load of 75pf.

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation

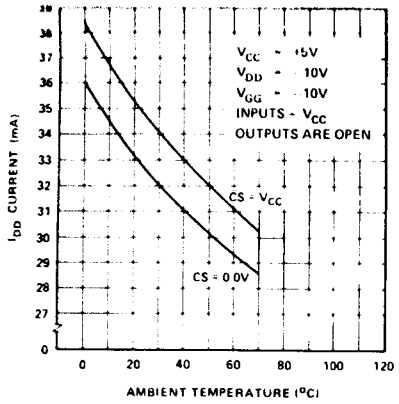


NOTE 1 The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

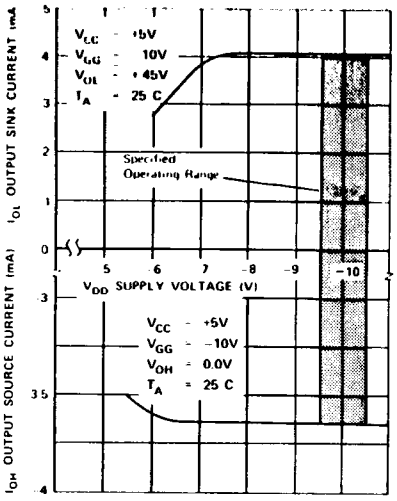
NOTE 2 If CS makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

TYPICAL CHARACTERISTICS

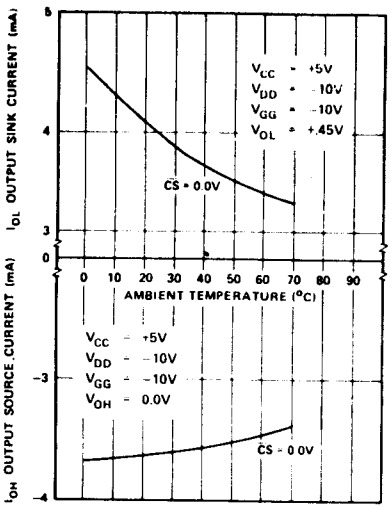
I_{DD} CURRENT VS. TEMPERATURE



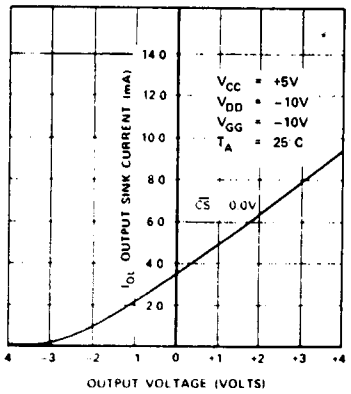
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



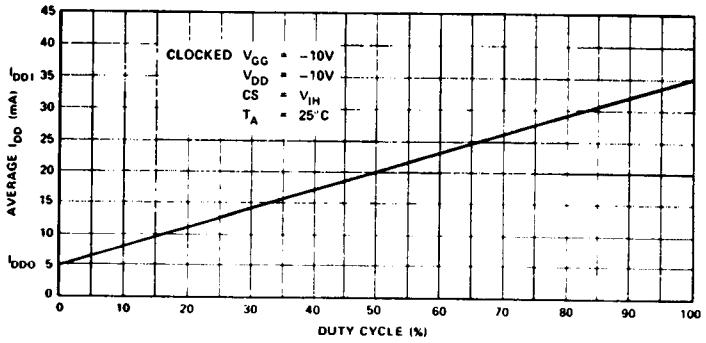
OUTPUT CURRENT VS. TEMPERATURE



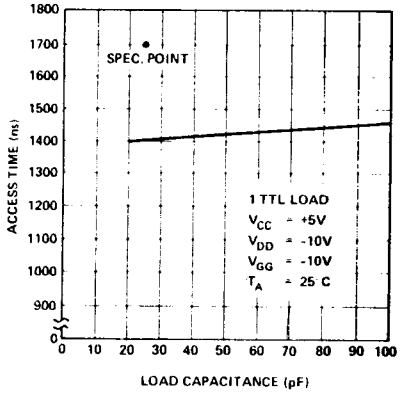
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



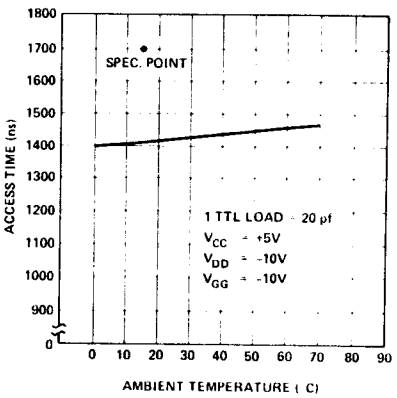
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



PROGRAMMING OPERATION

D.C. AND OPERATING CHARACTERISTICS FOR PROGRAMMING OPERATION

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current			10	mA	$V_{IN} = -48V$
I_{LI2P}	Program and V_{GG} Load Current			10	mA	$V_{IN} = -48V$
I_{BB}	V_{BB} Supply Load Current		.05		mA	
I_{DDP}(1)	Peak I_{DD} Supply Load Current		200		mA	$V_{DD} = V_{prog} = -48V$ $V_{GG} = -35V$
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−46		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−46		−48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 1: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

A.C. CHARACTERISTICS FOR PROGRAMMING OPERATION

$T_{AMBIENT} = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\varphi PW}$	Program Pulse Width			3	ms	$V_{GG} = -35V$, $V_{DD} = V_{prog} = -48V$
t_{DW}	Data Set Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW} (2)	Address Complement Set Up	25			μs	
t_{ACH} (2)	Address Complement Hold	25			μs	
t_{ATW}	Address True Set Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

Note 2. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0 through 255) must be programmed as shown in the timing diagram for a minimum of 32 times.

SWITCHING CHARACTERISTICS FOR PROGRAMMING OPERATION

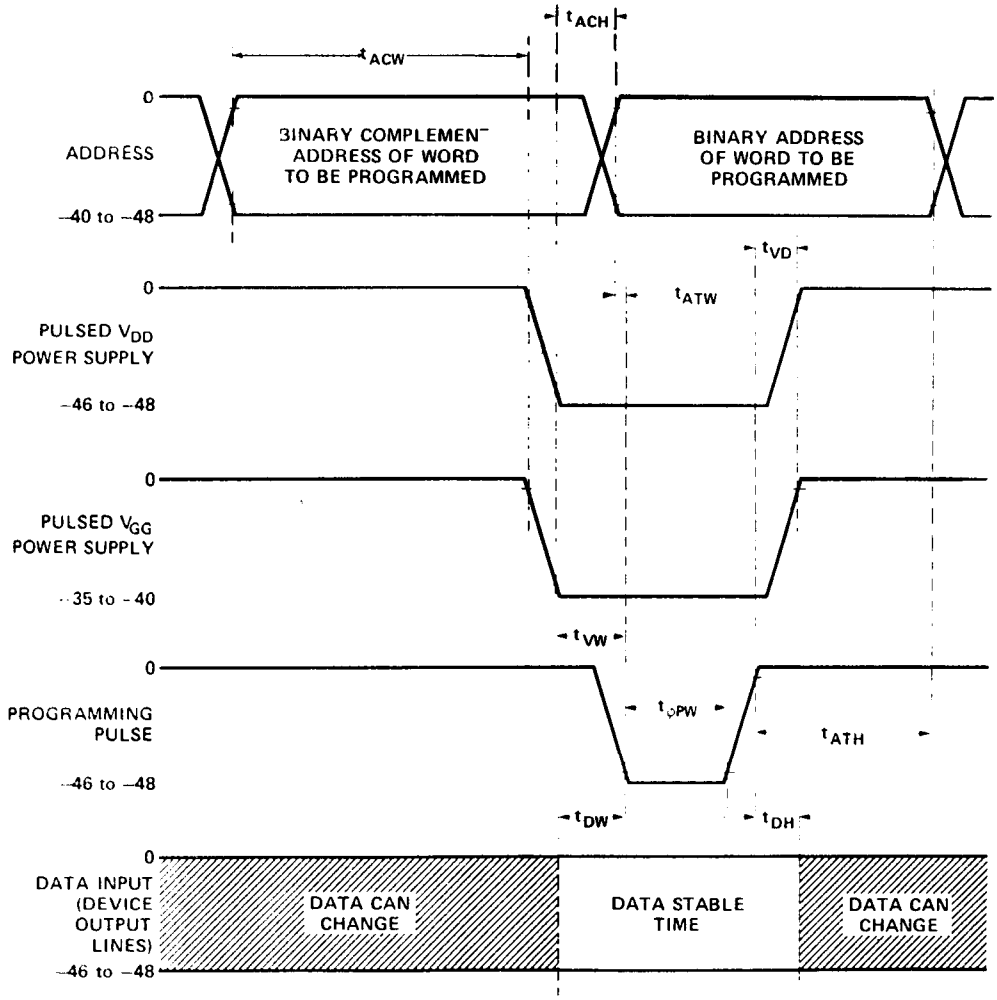
PROGRAM OPERATION

Conditions of Test:

Input pulse rise and fall times $\leq 1\mu sec$

$\overline{CS}$ = 0V

PROGRAM WAVEFORMS



PROGRAMMING OPERATION OF THE 4702A

When the Data Input for the Program Mode is:	Then the Data Output during the Read Mode is:
V_{ILP} = ~-48V pulsed	Logic 1 - V_{OH} = 'P' on tape
V_{IHP} = ~ 0V	Logic 0 - V_{OL} = 'N' on tape

WORD	ADDRESS A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|
255	1	1	1	1	1	1	1	1

Address Logic Level During Read Mode: Logic 0 = V_{IL} (~.3V) Logic 1 = V_{IH} (~3V)

Address Logic Level During Program Mode: Logic 0 = V_{IL2P} (~-40V) Logic 1 = V_{IHP} (~0V)

PROGRAMMING INSTRUCTIONS FOR THE 4702A

I. Operation of the 4702A in Program Mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table on page 6 for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25 μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10 μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (−48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 6). All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

II. Programming of the 4702A Using Intel Microcomputers

Intel provides low cost program development systems which may be used to program its electrically programmable ROMs. Note that the programming specifications that apply to the 4702A are identical to those for Intel's 1702A.

A. Intellec 4

The Intellec 4 program development system is used as a program development tool for the 4004 microprocessor. As such, it is equipped with a PROM programmer card and may be used to program Intel's electrically programmable and ultraviolet erasable ROMs.

An ASR-33 teletype terminal is used as the input device. Through use of the Intellec software system monitor, programs to be loaded into PROM may be typed in directly or loaded through the paper tape reader. The system monitor allows the program to be reviewed or altered at will prior to actually programming the PROM. For more complete information on this program development system, refer to the Intel Microcomputer Catalog or the Intellec Specifications.

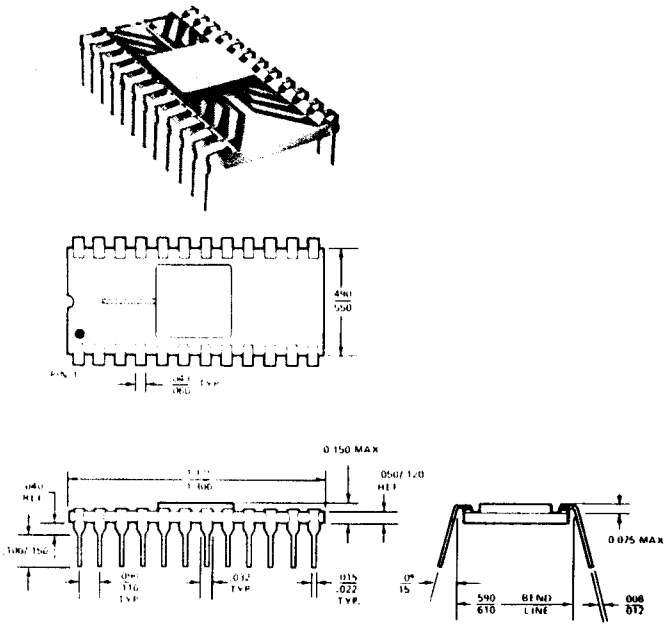
B. Users of the SIM4 microcomputer programming systems may also program the 4702A using the MP7-03 programmer card and the appropriate control ROMs:
SIM8 system—Control ROMs A0540, A0541 and A0543.

III. 4702A Erasing Procedure

The 4702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537A. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W-sec/cm^2. Examples of ultraviolet sources which can erase the 4702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the 4702A to be erased should be placed about one inch away from the lamp tubes.

PACKAGING INFORMATION

24-LEAD CERAMIC DUAL IN-LINE PACKAGE OUTLINE (C)



ORDERING INFORMATION

Intel Products may be ordered from either your local Intel sales office or stocking Intel distributor. To specify the desired package type, place the package letter designator in front of the part type.

C4702A Ceramic Package

Intel Corporation
3065 Bowers Avenue
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Tel: (408) 246-7501
TWX: 910-338-0026
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Tel: (714) 835-9642
TWX: 910-595-1114

Mid-America:
6350 L.B.J. Freeway
Suite 178
Dallas, Texas 75240
Tel: (214) 661-8829
TWX: 910-860-5487

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856 Union Rd.
Englewood, Ohio 45322
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2 Militia Drive
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Lexington, Massachusetts 02173
Tel: (617) 861-1136
TELEX: 92-3493

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30 S. Valley Rd.
Suite 108
Paoli, Pennsylvania 19301
Tel: (215) 647-2615
TWX: 510-668-7768

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