2048 BIT MASK PROGRAMMABLE READ ONLY MEMORY

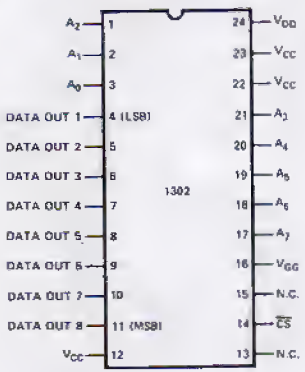
- Fully Decoded, 256x8 Organization
- Inputs and Outputs DTL and TTL Compatible
- Three-state Output -- OR-tie Capability
- Static MOS -- No Clocks Required
- Simple Memory Expansion -- Chip Select Input Lead
- 24-pin Dual-In-Line Hermetically Sealed Ceramic Package

The Intel®1302 is a fully decoded 256 word by 8-bit metal mask ROM. It is ideal for large volume production runs of systems initially using the 1702A erasable and electrically programmable ROM. The 1302 has the same pinning as the 1602A/1702A.

The 1302 is entirely static — no clocks are required. Inputs and outputs of the 1302 are DTL and TTL compatible. The output is three-state for OR-tie capability. A separate chip select input allows easy memory expansion. The 1302 is packaged in a 24 pin dual-in-line hermetically sealed ceramic package.

The 1302 is fabricated with p-channel silicon gate technology. This low threshold allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

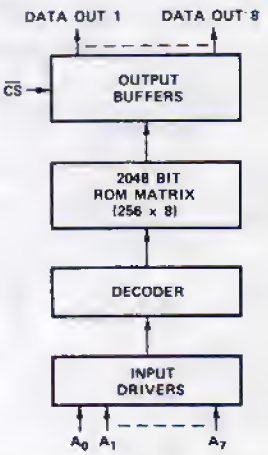
PIN CONFIGURATION



PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: LOGIC 1 AT INPUT AND OUTPUT IS A HIGH AND LOGIC 0 IS LOW.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, $V_{GG}^{(1)}$ = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.(2)	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC} −2 I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0 I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA , T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			1	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}−2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

Continuous Operation

Note 1. V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle.
Note 2. Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		.700	1	µs
t_{DVGG}	Clocked V_{GG} set up	1			µs
t_{CS}	Chip select delay			200	ns
t_{CO}	Output delay from $\overline{CS}$			500	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	µs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Capacitance* T_A = 25°C

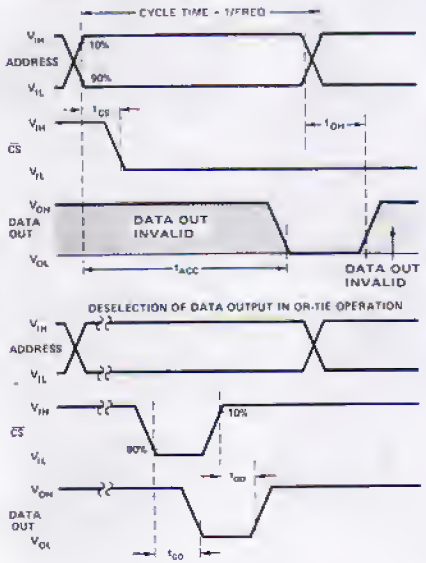
SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		5	10	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		5	10	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

*This parameter is periodically sampled and is not 100% tested.

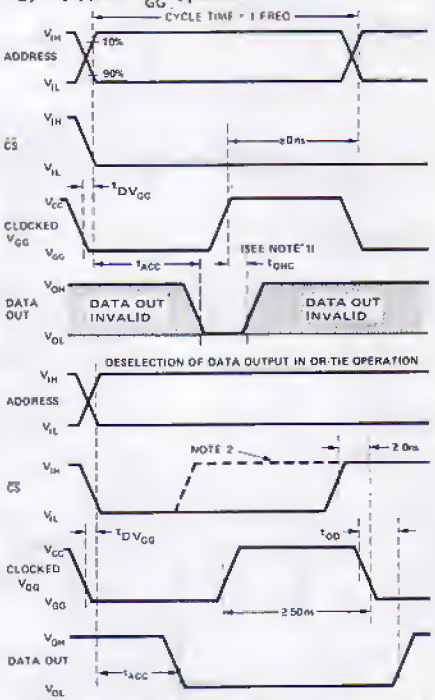
Switching Characteristics

Conditions of Test:
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation

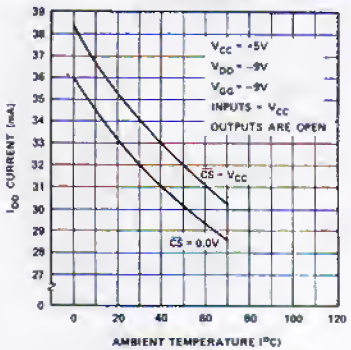


NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

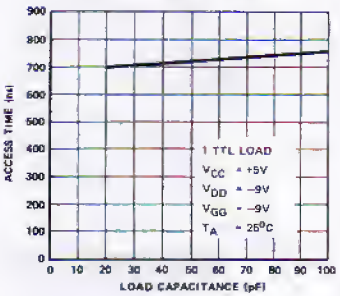
NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

Typical Characteristics

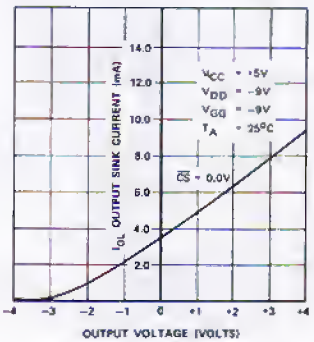
I_{DD} CURRENT VS. TEMPERATURE



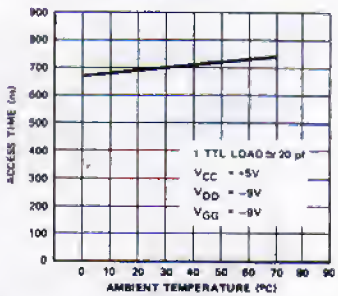
ACCESS TIME VS. LOAD CAPACITANCE



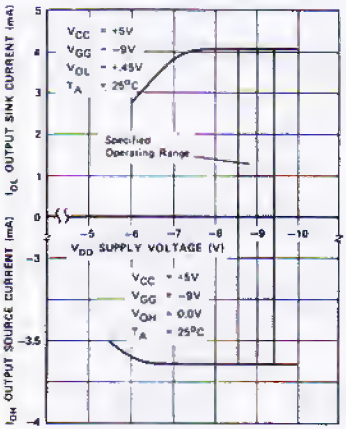
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



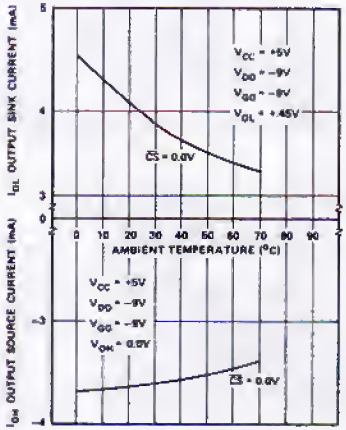
ACCESS TIME VS. TEMPERATURE



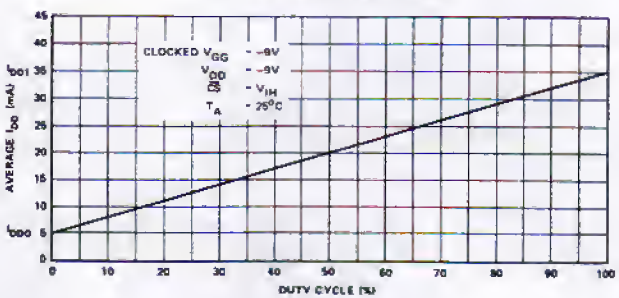
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



OUTPUT CURRENT VS. TEMPERATURE



AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

ROMs

- **Fast Access Time: Max. 650 ns (1702A–2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

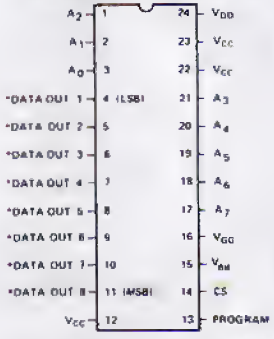
The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is also available for large volume production runs of systems initially using the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

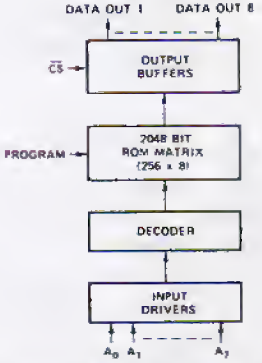


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming instructions section, pages 3-57.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to -20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . -48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG} = -9V ±5%, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

Note 1: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

Capacitance* T_A = 25°C

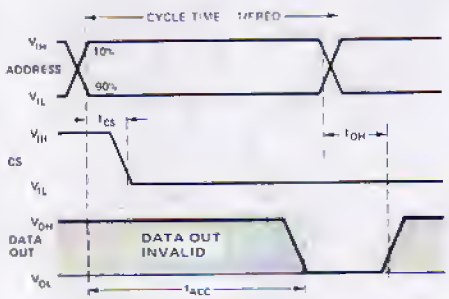
SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	

*This parameter is periodically sampled and is not 100% tested.

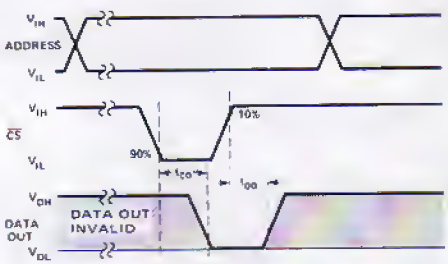
Switching Characteristics

Conditions of Test:
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION

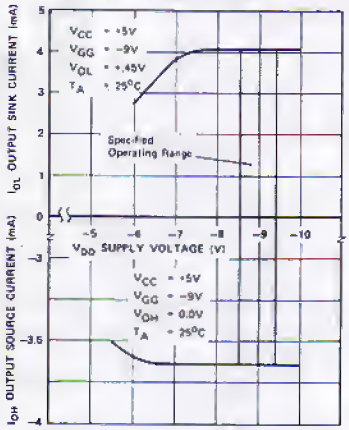


B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION

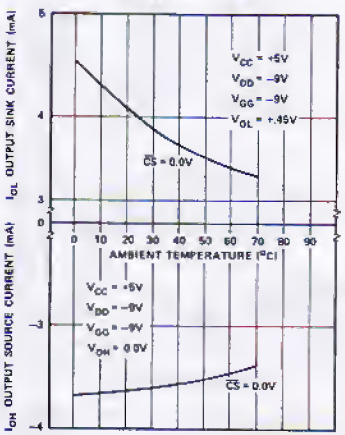


Typical Characteristics

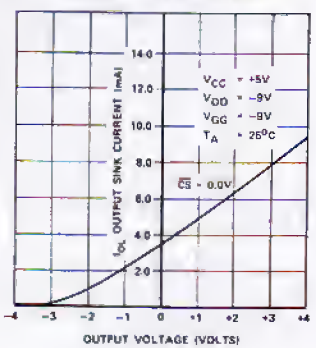
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



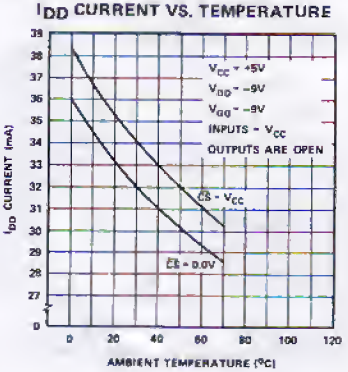
OUTPUT CURRENT VS. TEMPERATURE



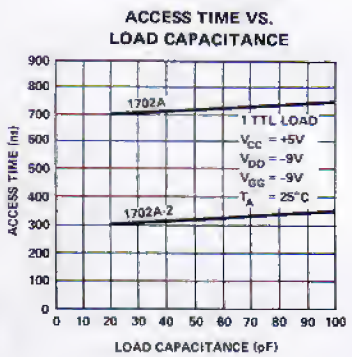
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE