

## INDEX

<ul> <li>MOS RAM</li> <li>MOS ROM</li> <li>MOS ROM</li> <li>MOS ROM</li> <li>MOS ROM</li> <li>MOS ROM</li> <li>MOS RAM</li> <li>Bipolar RAM</li> <li>Bipolar RAM</li> <li>Bipolar PROM</li> <li>PACKAGE INFORMATION</li> <li>RELIABILITY OF HITACHI IC MEMORIES</li> <li>PRECAUTIONS FOR HANDLING IC MEMORIES</li> <li>OUALITY ASSURANCE OF IC MEMORIES</li> <li>OUALITY ASSURANCE OF IC MEMORIES</li> <li>OUALITY ASSURANCE OF IC MEMORIES</li> <li>OUTLINE OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-31</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-31</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-31</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM4334P-31</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM4334P-41</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148P-61</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148P-55</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148P-35</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148H-75</li> <li>HO4-word x 4-bit RAM (CMOS)</li> <li>HM6147H-74</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-75</li> <li>4096-w</li></ul>	QUICK REFERENCE	GUIDE TO HITACHI IC MEMORIES 8
<ul> <li>MOS Memories of Wide Operating Temperature Range</li> <li>Bipolar RAM</li> <li>Bipolar PROM</li> <li>PACKAGE INFORMATION</li> <li>RELIABILITY OF HITACHI IC MEMORIES</li> <li>PRECAUTIONS FOR HANDLING IC MEMORIES</li> <li>OUALITY ASSURANCE OF IC MEMORIES</li> <li>OUTLINE OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming &amp; Erasing of EPROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM4334P-4</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P-6</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-15</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li></ul>	• MOS RAM	
<ul> <li>MOS Memories of Wide Operating Temperature Range</li> <li>Bipolar RAM</li> <li>Bipolar PROM</li> <li>PACKAGE INFORMATION</li> <li>RELIABILITY OF HITACHI IC MEMORIES</li> <li>PRECAUTIONS FOR HANDLING IC MEMORIES</li> <li>OUALITY ASSURANCE OF IC MEMORIES</li> <li>OUTLINE OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming &amp; Erasing of EPROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM4334P-4</li> <li>HO24-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P</li> <li>HM6148P-6</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-15</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li></ul>	• MOS ROM	
<ul> <li>Bipolar PROM</li> <li>PACKAGE INFORMATION</li> <li>RELIABILITY OF HITACHI IC MEMORIES</li> <li>PRECAUTIONS FOR HANDLING IC MEMORIES</li> <li>QUALITY ASSURANCE OF IC MEMORIES</li> <li>QUALITY OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>HM6148P-6</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-5</li> <li>HM6148P-5</li> <li>HM6148P-55</li> <li>HM6148H-55</li> <li>HM6148H-75</li> <li>HM6148H-75</li> <li>HM6148H-75</li> <li>HM6148H-73</li> <li>HM6148H-73</li> <li>HM6148H-74</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P</li> <li>HM6147P-3</li> <li>HM6147P-3</li> <li>HM6147H-4</li> <li>HM6147H-45</li> <li>HM6147H-45</li> <li>HM6147H-45</li> <li>HM6147H-75</li> <li>HM6147H-75</li> <li>HM6147H-75</li> <li>HM6147H-75</li> <li>HM6147H-74</li> <li>HM6147H-74</li> <li>HM6147H-74</li> <li>HM6147H-74</li> <li>HM6147H-75</li> <li>HM6147H-75</li> <li>HM6147H-7</li></ul>	<ul> <li>MOS Memories of W</li> </ul>	ide Operating Temperature Range
<ul> <li>PACKAGE INFORMATION.</li> <li>RELIABILITY OF HITACHI IC MEMORIES</li> <li>PRECAUTIONS FOR HANDLING IC MEMORIES</li> <li>QUALITY ASSURANCE OF IC MEMORIES</li> <li>OUTLINE OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming of Bipolar PROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334-4 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3L 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4L 1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148-6 1024-word x 4-bit RAM (CMOS)</li> <li>HM6148-7</li> <li>HM6147</li> <li>HM6147</li> <li>HM6147</li> <li>HM6147-1</li> <li< th=""><th></th><th></th></li<></ul>		
RELIABILITY OF HITACHI IC MEMORIES         PRECAUTIONS FOR HANDLING IC MEMORIES         QUALITY ASSURANCE OF IC MEMORIES         OUTLINE OF TESTING METHOD         APPLICATION OF DYNAMIC RAMS         PROGRAMMING & ERASING OF PROMS         • Programming of Bipolar PROM         • MASK ROM PROGRAMMING INSTRUCTION         DATA SHEETS         • MOS STATIC RAM         • HM4334-3       1024-word x 4-bit RAM (CMOS)         • HM4334-4       1024-word x 4-bit RAM (CMOS)         • HM4334P-3       1024-word x 4-bit RAM (CMOS)         • HM4334P-4       1024-word x 4-bit RAM (CMOS)         • HM6148       1024-word x 4-bit RAM (CMOS)         • HM6148       1024-word x 4-bit RAM (CMOS)         • HM6148P       1024-word x 4-bit RAM (CMOS)         • HM6148P       1024-word x 4-bit RAM (CMOS)         • HM6148P       1024-word x 4-bit RAM (CMOS)         • HM6148P-6       1024-word x 4-bit RAM (CMOS)         • HM6148P-5       1024-word x 4-bit RAM (CMOS)         • HM6148P-5       1024-word x 4-bit RAM (CMOS)         • HM6148P-5       1024-word x 4-bit RAM (CMOS)	• Bipolar PROM	
<ul> <li>PRECAUTIONS FOR HANDLING IC MEMORIES</li> <li>QUALITY ASSURANCE OF IC MEMORIES</li> <li>OUTLINE OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-5</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-5</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-75</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6147H-45</li> <li>4096</li></ul>		
QUALITY ASSURANCE OF IC MEMORIES         OUTLINE OF TESTING METHOD         APPLICATION OF DYNAMIC RAMS         PROGRAMMING & ERASING OF PROMS         Programming & Erasing of EPROM         MASK ROM PROGRAMMING INSTRUCTION         DATA SHEETS         MOS STATIC RAM         HM4334-3       1024-word x 4-bit RAM (CMOS)         HM4334-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3       1024-word x 4-bit RAM (CMOS)         HM4334P-3       1024-word x 4-bit RAM (CMOS)         HM4334P-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148-6       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS) <th></th> <th></th>		
<ul> <li>OUTLINE OF TESTING METHOD</li> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334-4 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3 1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4 1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>HM6148</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-45</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-45</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148HLP-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148HLP-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6147H-45</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-73</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-74</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-75</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-75</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-74</li> <li>H096</li></ul>		
<ul> <li>APPLICATION OF DYNAMIC RAMS</li> <li>PROGRAMMING &amp; ERASING OF PROMS</li> <li>Programming &amp; Erasing of EPROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-35</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-35</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-45</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6</li></ul>		
PROGRAMMING & ERASING OF PROMS           Programming & Erasing of EPROM           Programming & Erasing of EPROM           MASK ROM PROGRAMMING INSTRUCTION           DATA SHEETS           MOS STATIC RAM           HM4334-3           1024-word x 4-bit RAM (CMOS)           HM4334-4           HM4334P-3           1024-word x 4-bit RAM (CMOS)           HM4334P-3           HM4334P-4           1024-word x 4-bit RAM (CMOS)           HM4334P-3           HM4334P-4           HM4334P-4           HM4334P-3           HM4334P-4           HM6148           HM24-word x 4-bit RAM (CMOS)           HM6148           HM6148           HM6148P-6           HM6148HP-75           HM6148HP-75 </th <th></th> <th></th>		
<ul> <li>Programming &amp; Erasing of EPROM</li> <li>Programming of Bipolar PROM</li> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-35</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6147HP-3</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147HP-3</li></ul>		
<ul> <li>Programming of Bipolar PROM .</li> <li>MASK ROM PROGRAMMING INSTRUCTION .</li> <li>DATA SHEETS .</li> <li>MOS STATIC RAM .</li> <li>HM4334-3 1024-word x 4-bit RAM (CMOS) .</li> <li>HM4334-4 1024-word x 4-bit RAM (CMOS) .</li> <li>HM4334-3 1024-word x 4-bit RAM (CMOS) .</li> <li>HM4334P-3 1024-word x 4-bit RAM (CMOS) .</li> <li>HM4334P-4 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148P 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-5 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-75 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-75 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-P45 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-P5 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-P5 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-P35 1024-word x 4-bit RAM (CMOS) .</li> <li>HM6148H-P35 1024-word x 4-bit RAM (CMOS) .</li> <li>HM61471 4096-word x 1-bit RAM (CMOS) .</li> <li>HM61471-45 0096-word x 1-bit RAM (CMOS) .</li> <li>HM61471P 4096-word x 1-bit RAM (CMOS) .</li> <li>HM61471P 4096-word x 1-bit RAM (CMOS) .</li> <li>HM6147H-35 4096-word x 1-bit RAM (CMOS) .</li> <li>HM6147H-45 4096-word x 1-bit RAM (CMOS) .</li> <li>HM6147H-54 50</li></ul>	PROGRAMMING & EF	RASING OF PROMS 40
<ul> <li>MASK ROM PROGRAMMING INSTRUCTION</li> <li>DATA SHEETS</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4L</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-5</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HLP-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6147</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147P</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147LP</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147LP3</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-45</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-54</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-45</li> <li>4096-word x 1-bit RAM (CMOS)</li></ul>	<ul> <li>Programming &amp; Erasi</li> </ul>	ng of EPROM40
<ul> <li>DATA SHEETS.</li> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4L</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4L</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-45</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-45</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-45</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-45</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-55</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148HP-45</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6147HP-35</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6147P</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147P</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147P</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147LP</li> <li>4096-word x 1-bit RAM (CMOS)</li> <li>HM6147LP-3</li> <li>4096-word</li></ul>	<ul> <li>Programming of Bipc</li> </ul>	lar PROM
<ul> <li>MOS STATIC RAM</li> <li>HM4334-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334-4</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3L</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-3L</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM4334P-4L</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>1024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148P-6</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148LP-6</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-35</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-55</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-755</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-755</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6148H-755</li> <li>H024-word x 4-bit RAM (CMOS)</li> <li>HM6147H-73</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147P</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147P</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-73</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-745</li> <li>H096-word x 1-bit RAM (CMOS)</li> <li>HM6147H-75</li> <li>H096-word x 1-bit RAM (CMOS)<th></th><th></th></li></ul>		
HM4334-3       1024-word x 4-bit RAM (CMOS)         HM4334-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3       1024-word x 4-bit RAM (CMOS)         HM4334P-3       1024-word x 4-bit RAM (CMOS)         HM4334P-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H-755       1024-word x 4-bit RAM (CMOS)         HM6148H-755       1024-word x 4-bit RAM (CMOS)		
HM4334-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3       1024-word x 4-bit RAM (CMOS)         HM4334P-4       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148-6       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148LP-5       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)	<ul> <li>MOS STATIC RAM</li> </ul>	
HM4334P-3       1024-word x 4-bit RAM (CMOS)         HM4334P-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 1-bit RAM (CMOS) <th>HM4334-3</th> <th></th>	HM4334-3	
HM4334P-4       1024-word x 4-bit RAM (CMOS)         HM4334P-3L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148-6       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 1-bit RAM (CMOS)         HM6148H-55       1024-word x 1-bit RAM (CMOS)		
HM4334P-3L       1024-word x 4-bit RAM (CMOS)         HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP6       1024-word x 4-bit RAM (CMOS)         HM6148LP6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 1-bit RAM (CMOS)         HM6148HP-55       1024-word x 1-bit RAM (CMOS)         HM6147HP-35       1024-word x 1-bit RAM (CMOS)		
HM4334P-4L       1024-word x 4-bit RAM (CMOS)         HM6148       1024-word x 4-bit RAM (CMOS)         HM6148-6       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H LP-35       1024-word x 4-bit RAM (CMOS)         HM6148H LP-35       1024-word x 4-bit RAM (CMOS)         HM6147H 4096-word x 1-bit RAM (CMOS)       HM6147H         HM6147H 4096-word x 1-bit RAM (CMOS)       HM6147H		
HM6148       1024-word x 4-bit RAM (CMOS)         HM6148-6       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6147HP       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)		
HM6148-6       1024-word x 4-bit RAM (CMOS)         HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)57
HM6148P       1024-word x 4-bit RAM (CMOS)         HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148P-6       1024-word x 4-bit RAM (CMOS)         HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6147H       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148LP       1024-word x 4-bit RAM (CMOS)         HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148LP-6       1024-word x 4-bit RAM (CMOS)         HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148H-35       1024-word x 4-bit RAM (CMOS)         HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-45       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)     <		1024-word x 4-bit RAM (CMOS)
HM6148H-45       1024-word x 4-bit RAM (CMOS)         HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148H-55       1024-word x 4-bit RAM (CMOS)         HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		
HM6148HP-35       1024-word x 4-bit RAM (CMOS)         HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		
HM6148HP-45       1024-word x 4-bit RAM (CMOS)         HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)     <		
HM6148HP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-45       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM6147-3       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P.3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP.3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148HLP-35       1024-word x 4-bit RAM (CMOS)         HM6148HLP-45       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P.3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-45       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148HLP-45       1024-word x 4-bit RAM (CMOS)         HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM61477       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-45       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6148HLP-55       1024-word x 4-bit RAM (CMOS)         HM6147       4096-word x 1-bit RAM (CMOS)         HM61473       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		1024-word x 4-bit RAM (CMOS)
HM6147       4096-word x 1-bit RAM (CMOS)         HM6147-3       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		
HM6147-3       4096-word x 1-bit RAM (CMOS)         HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP3       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		4096-word x 1-bit RAM (CMOS)
HM6147P       4096-word x 1-bit RAM (CMOS)         HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)		4096-word x 1-bit RAM (CMOS)
HM6147P-3       4096-word x 1-bit RAM (CMOS)         HM6147LP       4096-word x 1-bit RAM (CMOS)         HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-45       4096-word x 1-bit RAM (CMOS)		4096-word x 1-bit RAM (CMOS)
HM6147LP         4096-word x 1-bit RAM (CMOS)           HM6147LP-3         4096-word x 1-bit RAM (CMOS)           HM6147H-35         4096-word x 1-bit RAM (CMOS)           HM6147H-45         4096-word x 1-bit RAM (CMOS)           HM6147H-55         4096-word x 1-bit RAM (CMOS)           HM6147HP-35         4096-word x 1-bit RAM (CMOS)           HM6147HP-35         4096-word x 1-bit RAM (CMOS)           HM6147HP-45         4096-word x 1-bit RAM (CMOS)	HM6147P-3	4096-word x 1-bit RAM (CMOS)
HM6147LP-3       4096-word x 1-bit RAM (CMOS)         HM6147H-35       4096-word x 1-bit RAM (CMOS)         HM6147H-45       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147H-55       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-35       4096-word x 1-bit RAM (CMOS)         HM6147HP-45       4096-word x 1-bit RAM (CMOS)	HM6147LP	4096-word x 1-bit RAM (CMOS)
HM6147H-35         4096-word x 1-bit RAM (CMOS)           HM6147H-45         4096-word x 1-bit RAM (CMOS)           HM6147H-55         4096-word x 1-bit RAM (CMOS)           HM6147H-35         4096-word x 1-bit RAM (CMOS)           HM6147HP-35         4096-word x 1-bit RAM (CMOS)           HM6147HP-45         4096-word x 1-bit RAM (CMOS)	HM6147LP-3	
HM6147H-45         4096-word x 1-bit RAM (CMOS)           HM6147H-55         4096-word x 1-bit RAM (CMOS)           HM6147HP-35         4096-word x 1-bit RAM (CMOS)           HM6147HP-45         4096-word x 1-bit RAM (CMOS)		4096-word x 1-bit RAM (CMOS)
HM6147H-55         4096-word x 1-bit RAM (CMOS)           HM6147HP-35         4096-word x 1-bit RAM (CMOS)           HM6147HP-45         4096-word x 1-bit RAM (CMOS)	HM6147H-45	4096-word x 1-bit RAM (CMOS)
HM6147HP-35 4096-word x 1-bit RAM (CMOS)	HM6147H-55	4096-word x 1-bit RAM (CMOS)
HM6147HP-45 4096-word x 1-bit RAM (CMOS)	HM6147HP-35	4096-word x 1-bit RAM (CMOS)
HM6147HP-55 4096-word x 1-bit RAM (CMOS)	HM6147HP-45	4096-word x 1-bit RAM (CMOS)
	HM6147HP-55	4096-word x 1-bit RAM (CMOS)



HM6147HLP-35	4096-word x 1-bit RAM (CMOS) 97
HM6147HLP-45	4096-word x 1-bit RAM (CMOS) 97
HM6147HLP-55	4096-word x 1-bit RAM (CMOS) 97
HM6116-2	2048-word x 8-bit RAM (CMOS)
HM6116-3	2048-word x 8-bit RAM (CMOS)
HM6116-4	2048-word x 8-bit RAM (CMOS)101
HM6116I-2	2048-word x 8-bit RAM (CMOS)
HM6116I-3	2048-word x 8-bit RAM (CMOS)
HM61161-4	2048-word x 8-bit RAM (CMOS) 107
HM6116P-2	2048-word x 8-bit RAM (CMOS)
HM6116P-3	2048-word x 8-bit RAM (CMOS)
HM6116P-4	2048-word x 8-bit RAM (CMOS) 101
HM6116PI-2	2048-word x 8-bit RAM (CMOS)
HM6116PI-3	2048-word x 8-bit RAM (CMOS)
HM6116PI-4	2048-word x 8-bit RAM (CMOS)
HM6116FP-2	2048-word x 8-bit RAM (CMOS)
HM6116FP-3	2048-word x 8-bit RAM (CMOS)
HM6116FP-4	2048-word x 8-bit RAM (CMOS)
HM6116CG-2	2048-word x 8-bit RAM (CMOS)120
HM6116CG-3	2048-word x 8-bit RAM (CMOS)
HM6116CG-4	2048-word x 8-bit RAM (CMOS)
HM6116L-2	2048-word x 8-bit RAM (CMOS) 124
HM6116L-3	2048-word x 8-bit RAM (CMOS) 124
HM6116L-4	2048-word x 8-bit RAM (CMOS)
HM6116LI-2	2048-word x 8-bit RAM (CMOS) 131
S81 HM6116LI-3	2048-word x 8-bit RAM (CMOS) 131
HM6116LI-4	2048-word x 8-bit RAM (CMOS) 131
HM6116LP-2	2048-word x 8-bit RAM (CMOS) 135
801 HM6116LP-3	2048-word x 8-bit RAM (CMOS) 135
HM6116LP-4	2048-word x 8-bit RAM (CMOS)
EOS HM6116LPI-2	2048-word x 8-bit RAM (CMOS) 142
HM6116LPI-3	2048-word x 8-bit RAM (CMOS) 142
HM6116LPI-4	2048-word x 8-bit RAM (CMOS) 142
101 HM6116LFP-2	2048-word x 8-bit RAM (CMOS) 146
HM6116LFP-3	2048-word x 8-bit RAM (CMOS)
HM6116LFP-4	2048-word x 8-bit RAM (CMOS)
HM6116K-3	2048-word x 8-bit RAM (CMOS) 150
HM6116K-4	2048-word x 8-bit RAM (CMOS)
HM6116AP-10	2048-word x 8-bit RAM (CMOS) 150
HM6116AP-12	2048-word x 8-bit RAM (CMOS) 154
HM6116AP-15	2048-word x 8-bit RAM (CMOS)
HM6116AP-20	2048-word x 8-bit RAM (CMOS) 154
HM6116ASP-10	2048-word x 8-bit RAM (CMOS) 154
M6116ASP-12	2048-word x 8-bit RAM (CMOS)
HM6116ASP-15	2048-word x 8-bit RAM (CMOS) 154
HM6116ASP-20	2048-word x 8-bit RAM (CMOS)
HM6116ALP-10	2048-word x 8-bit RAM (CMOS)
HM6116ALP-12	2048-word x 8-bit RAM (CMOS)
HM6116ALP-15	2048-word x 8-bit RAM (CMOS)
HM6116ALP-20	2048-word x 8-bit RAM (CMOS)
HM6116ALSP-10	THE PERSON NETWORK NAMES AND ADDRESS OF THE PERSON ADDRESS OF THE
HM6116ALSP-12	
HM6116ALSP-15	2048-word x 8-bit RAM (CMOS)
HM6116ALSP-20	2048-word x 8-bit RAM (CMOS)
TIMOTTOALSP-20	2010 WOID X O'DIT HAINI (UNIOS)

**HITACHI** 

HM6117P-3       2048-word x 8-bit RAM (CMOS)       162         HM6117P-3       2048-word x 8-bit RAM (CMOS)       167         HM6117FP-3       2048-word x 8-bit RAM (CMOS)       167         HM6117LP-3       2048-word x 8-bit RAM (CMOS)       172         HM6117LP-4       2048-word x 8-bit RAM (CMOS)       172         HM6117LP-4       2048-word x 8-bit RAM (CMOS)       172         HM61168H-55       4096-word x 4-bit RAM (CMOS)       178         HM6168H-55       4096-word x 4-bit RAM (CMOS)       184         HM6168H-55       4096-word x 4-bit RAM (CMOS)       185         HM6168H-54       4096-word x 4-bit RAM (CMOS)       185         HM6168H-55       4096-word x 4-bit RAM (CMOS)       185         HM6168H-57       4096-word x 4-bit RAM (CMOS)       186         HM6167H       16384-word x 1-bit RAM (CMOS)       186         HM6167F       16384-word x 1-bit RAM (CMOS)       186         HM6167F       16384-word x 1-bit RAM (CMOS)       186			
HM6117FP-3         2048-word x 8-bit RAM (CMOS)         167           HM6117LP-3         2048-word x 8-bit RAM (CMOS)         167           HM6117LP-3         2048-word x 8-bit RAM (CMOS)         172           HM6117LFP-4         2048-word x 8-bit RAM (CMOS)         172           HM6117LFP-4         2048-word x 8-bit RAM (CMOS)         178           HM6117LFP-4         2048-word x 4-bit RAM (CMOS)         178           HM6168H-45         4096-word x 4-bit RAM (CMOS)         184           HM6168H-54         4096-word x 4-bit RAM (CMOS)         184           HM6168H-75         4096-word x 4-bit RAM (CMOS)         184           HM6168H-74         4096-word x 4-bit RAM (CMOS)         184           HM6168H-74         4096-word x 4-bit RAM (CMOS)         185           HM6168H-74         4096-word x 4-bit RAM (CMOS)         185           HM6168H-75         4096-word x 4-bit RAM (CMOS)         185           HM6168H-74         4096-word x 4-bit RAM (CMOS)         186           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167P         16384-word x 1-bit RAM (CMOS)         186           HM6167P         16384-word x 1-bit RAM (CMOS)         192		HM6117P-3	2048-word x 8-bit RAM (CMOS)
HM6117FP-4         2048-word x 8-bit RAM (CMOS)         167           HM6117LP-3         2048-word x 8-bit RAM (CMOS)         172           HM6117LFP-3         2048-word x 8-bit RAM (CMOS)         178           HM6117LFP-4         2048-word x 8-bit RAM (CMOS)         178           HM6168H-55         4096-word x 4-bit RAM (CMOS)         184           HM6168H-55         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-75         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-75         4096-word x 4-bit RAM (CMOS)         185           HM6168H-P-70         4096-word x 4-bit RAM (CMOS)         185           HM6168H-P-70         4096-word x 4-bit RAM (CMOS)         185           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167-8         16384-word x 1-bit RAM (CMOS)         186           HM6167P-8         16384-word x 1-bit RAM (CMOS)         192           HM6167LP-8         16384-word x 1-bit RAM (CMOS)         192		HM6117P-4	2048-word x 8-bit RAM (CMOS)
HM6117FP-4         2048-word x 8-bit RAM (CMOS)         167           HM6117LP-3         2048-word x 8-bit RAM (CMOS)         172           HM6117LFP-3         2048-word x 8-bit RAM (CMOS)         178           HM6117LFP-4         2048-word x 8-bit RAM (CMOS)         178           HM6168H-55         4096-word x 4-bit RAM (CMOS)         184           HM6168H-55         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-75         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-75         4096-word x 4-bit RAM (CMOS)         185           HM6168H-P-70         4096-word x 4-bit RAM (CMOS)         185           HM6168H-P-70         4096-word x 4-bit RAM (CMOS)         185           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167-8         16384-word x 1-bit RAM (CMOS)         186           HM6167P-8         16384-word x 1-bit RAM (CMOS)         192           HM6167LP-8         16384-word x 1-bit RAM (CMOS)         192		HM6117FP-3	2048-word x 8-bit RAM (CMOS)
HM6117LP-3         2048-word x 8-bit RAM (CMOS)         172           HM6117LP-4         2048-word x 8-bit RAM (CMOS)         173           HM6117LFP-4         2048-word x 8-bit RAM (CMOS)         178           HM6168H-45         4096-word x 4-bit RAM (CMOS)         184           HM6168H-55         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168H-75         4096-word x 4-bit RAM (CMOS)         185           HM6168H-75         4096-word x 4-bit RAM (CMOS)         185           HM6168H-75         4096-word x 1-bit RAM (CMOS)         186           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM61678         16384-word x 1-bit RAM (CMOS)         186           HM6167P         16384-word x 1-bit RAM (CMOS)         186           HM6167P         16384-word x 1-bit RAM (CMOS)         192           HM6167P         16384-word x 1-bit RAM (CMOS)         192      <		HM6117FP-4	2048-word x 8-bit RAM (CMOS)
HM6117LFP-3       2048-word x 8-bit RAM (CMOS)       178         HM6117LFP-4       2048-word x 8-bit RAM (CMOS)       178         HM6168H-55       4096-word x 4-bit RAM (CMOS)       184         HM6168H-57       4096-word x 4-bit RAM (CMOS)       184         HM6168H-54       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-54       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-54       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS) <td< td=""><th></th><td>HM6117LP-3</td><td>2048-word x 8-bit RAM (CMOS)</td></td<>		HM6117LP-3	2048-word x 8-bit RAM (CMOS)
HM6117LFP-3       2048-word x 8-bit RAM (CMOS)       178         HM6117LFP-4       2048-word x 8-bit RAM (CMOS)       178         HM6168H-55       4096-word x 4-bit RAM (CMOS)       184         HM6168H-57       4096-word x 4-bit RAM (CMOS)       184         HM6168H-54       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-54       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-54       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS) <td< td=""><th></th><td>HM6117LP-4</td><td>2048-word x 8-bit RAM (CMOS) 172</td></td<>		HM6117LP-4	2048-word x 8-bit RAM (CMOS) 172
HM6117LFP-4       2048-word x 8-bit RAM (CMOS)       178         HM6168H-45       4096-word x 4-bit RAM (CMOS)       184         HM6168H-55       4096-word x 4-bit RAM (CMOS)       184         HM6168H-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 1-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       196         HM6167LP-55       16384-word x 1-bit RAM (CMOS)		HM6117LFP-3	2048-word x 8-bit RAM (CMOS)
HM6168H-55         4096-word x 4-bit RAM (CMOS)         184           HM6168H-70         4096-word x 4-bit RAM (CMOS)         184           HM6168HP-54         4096-word x 4-bit RAM (CMOS)         184           HM6168HP-57         4096-word x 4-bit RAM (CMOS)         184           HM6168HP-70         4096-word x 4-bit RAM (CMOS)         184           HM6168HP-70         4096-word x 4-bit RAM (CMOS)         185           HM6168HP-70         4096-word x 4-bit RAM (CMOS)         185           HM6168HP-70         4096-word x 4-bit RAM (CMOS)         185           HM6167         16384-word x 1-bit RAM (CMOS)         186           HM61677         16384-word x 1-bit RAM (CMOS)         186           HM61678         16384-word x 1-bit RAM (CMOS)         186           HM61679         16384-word x 1-bit RAM (CMOS)         186           HM6167P-8         16384-word x 1-bit RAM (CMOS)         192           HM6167LP-8         16384-word x 1-bit RAM (CMOS)         192           HM6167LP-85         16384-word x 1-bit RAM (CMOS)         196		HM6117LFP-4	
HM6168H-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-55       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677-8       16384-word x 1-bit RAM (CMOS)       186         HM61677-8       16384-word x 1-bit RAM (CMOS)       186         HM61671LP-8       16384-word x 1-bit RAM (CMOS)       192         HM61671H-55       16384-word x 1-bit RAM (CMOS)       196         HM61671H-745       16384-word x 1-bit RAM (CMOS) <th></th> <td>HM6168H-45</td> <td>4096-word x 4-bit RAM (CMOS) 184</td>		HM6168H-45	4096-word x 4-bit RAM (CMOS) 184
HM6168H-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-55       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677-8       16384-word x 1-bit RAM (CMOS)       186         HM61677-8       16384-word x 1-bit RAM (CMOS)       186         HM61671LP-8       16384-word x 1-bit RAM (CMOS)       192         HM61671H-55       16384-word x 1-bit RAM (CMOS)       196         HM61671H-745       16384-word x 1-bit RAM (CMOS) <th></th> <td>HM6168H-55</td> <td>4096-word x 4-bit RAM (CMOS)</td>		HM6168H-55	4096-word x 4-bit RAM (CMOS)
HM6168HP-45       4096-word x 4-bit RAM (CMOS)       184         HM6168HP-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-75       16384-word x 1-bit RAM (CMOS)       192         HM6167H-75       16384-word x 1-bit RAM (CMOS)       196         HM6167H-75       16384-word x 1-bit RAM (CMOS)       196         HM6167HC-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HC-45       16384-word x 1-bit RAM (CMOS)		HM6168H-70	
HM6168HP-55       4096-word x 4-bit RAM (CMOS)       184         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       184         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167-6       16384-word x 1-bit RAM (CMOS)       186         HM6167-78       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       189         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-5       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HC-45       16384-word x 1-bit RAM (CMOS)		HM6168HP-45	4096-word x 4-bit RAM (CMOS)
HM6168HP-70       4096-word x 4-bit RAM (CMOS)       184         HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-55       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM61677       16384-word x 1-bit RAM (CMOS)       186         HM616778       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167P-78       16384-word x 1-bit RAM (CMOS)       186         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       196         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLC-55       16384-word x 1-bit RAM (CMOS)		HM6168HP-55	4096-word x 4-bit RAM (CMOS) 184
HM6168HLP-45       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       186         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167-76       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       192         HM6167H-745       16384-word x 1-bit RAM (CMOS)       196         HM6167H-745       16384-word x 1-bit RAM (CMOS)       196         HM6167H-745       16384-word x 1-bit RAM (CMOS)       203         HM6167H-745       16384-word x 1-bit RAM (CMOS)       203         HM6167H-745       16384-word x 1-bit RAM (CMOS)       203         HM6167HC-55       16384-word x 1-bit RAM (CMOS)		HM6168HP-70	
HM6168HLP-55       4096-word x 4-bit RAM (CMOS)       185         HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167-6       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       192         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS) <th></th> <td>HM6168HLP-45</td> <td>4096-word x 4-bit RAM (CMOS)</td>		HM6168HLP-45	4096-word x 4-bit RAM (CMOS)
HM6168HLP-70       4096-word x 4-bit RAM (CMOS)       185         HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167-6       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)		HM6168HLP-55	4096-word x 4-bit RAM (CMOS)
HM6167       16384-word x 1-bit RAM (CMOS)       186         HM6167-6       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HC-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HC-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       211         HM6264P-10       8192-word x 8-bit RAM (CMOS)		HM6168HLP-70	4096-word x 4-bit RAM (CMOS)
HM6167-6       16384-word x 1-bit RAM (CMOS)       186         HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167P-76       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167H-65       16384-word x 1-bit RAM (CMOS)       196         HM6167H-65       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-16       192-word x 8-bit RAM (CMOS		HM6167	
HM6167-8       16384-word x 1-bit RAM (CMOS)       186         HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       192         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HC-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HC-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       201         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       211         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)<		HM6167-6	16384-word x 1-bit RAM (CMOS) 186
HM6167P       16384-word x 1-bit RAM (CMOS)       186         HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       211         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word x 8-bit RAM (CM		HM6167-8	16384-word x 1-bit RAM (CMOS) 186
HM6167P-6       16384-word x 1-bit RAM (CMOS)       186         HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       201         HM6264P-10       8192-word x 8-bit RAM (CMOS)       201         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM		HM6167P	16384-word x 1-bit RAM (CMOS) 186
HM6167P-8       16384-word x 1-bit RAM (CMOS)       186         HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       211         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM		HM6167P-6	16384-word x 1-bit RAM (CMOS) 186
HM6167LP       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       211         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 1-bit RAM (MOS)       222         HM4716A-1       16384-word x 1-bit R		HM6167P-8	16384-word x 1-bit RAM (CMOS) 186
HM6167LP-6       16384-word x 1-bit RAM (CMOS)       192         HM6167LP-8       16384-word x 1-bit RAM (CMOS)       192         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-11       8192-word x 1-bit RAM (MOS)       222         HM4716A-1       16384-word x 1-bit RAM (MOS)       222         HM4716A-2       16384-word x 1-bit RA		HM6167LP	16384-word x 1-bit RAM (CMOS) 192
HM6167LP-8       16384-word × 1-bit RAM (CMOS)       192         HM6167H-45       16384-word × 1-bit RAM (CMOS)       196         HM6167H-55       16384-word × 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word × 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word × 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word × 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word × 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word × 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word × 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word × 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word × 1-bit RAM (CMOS)       207         HM6264P-10       8192-word × 8-bit RAM (CMOS)       211         HM6264P-12       8192-word × 8-bit RAM (CMOS)       211         HM6264LP-13       8192-word × 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word × 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word × 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word × 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word × 1-bit RAM (NMOS)       222         HM4716A-1       16384-word × 1-bi		HM6167LP-6	16384-word x 1-bit RAM (CMOS) 192
HM6167H-45       16384-word x 1-bit RAM (CMOS)       196         HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       201         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word x 8-bit RAM (CMOS)       222         HM4716A-1       16384-word x 1-bit RAM (MOS)       222         HM4716A-1       16384-word x 1-bit		HM6167LP-8	16384-word x 1-bit RAM (CMOS) 192
HM6167H-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       201         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM (MMOS)       222         HM4716A-1       16384-word x 1-bit RAM (MMOS)       222         HM4716A-2       16384-word x 1-bit		HM6167H-45	16384-word x 1-bit RAM (CMOS) 196
HM6167HP-45       16384-word x 1-bit RAM (CMOS)       196         HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       201         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-16       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-17       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-18       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-19       8192-word x 1-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM (CMOS)       222         HM4716A-1       16384-word x 1-bit RAM (CMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit R		HM6167H-55	16384-word x 1-bit RAM (CMOS) 196
HM6167HP-55       16384-word x 1-bit RAM (CMOS)       196         HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 1-bit RAM (CMOS)       215         MOS DYNAMIC RAM       221       221       222         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM		HM6167HP-45	16384-word x 1-bit RAM (CMOS) 196
HM6167HCG-45       16384-word x 1-bit RAM (CMOS)       203         HM6167HCG-55       16384-word x 1-bit RAM (CMOS)       203         HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       201         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-11       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         MOS DYNAMIC RAM       221       221         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS) <td< td=""><th></th><td>HM6167HP-55</td><td>16384-word x 1-bit RAM (CMOS) 196</td></td<>		HM6167HP-55	16384-word x 1-bit RAM (CMOS) 196
HM6167HLP-45       16384-word x 1-bit RAM (CMOS)       207         HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264P-16       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-11       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 1-bit RAM (CMOS)       215         HM6264LP-17       8192-word x 1-bit RAM (CMOS)       222         HM4716A-1       16384-word x 1-bit RAM (CMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)<		HM6167HCG-45	16384-word x 1-bit RAM (CMOS) 203
HM6167HLP-55       16384-word x 1-bit RAM (CMOS)       207         HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-17       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-17       8192-word x 1-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 1-bit RAM (CMOS)       221         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS) </td <th></th> <td>HM6167HCG-55</td> <td>16384-word x 1-bit RAM (CMOS) 203</td>		HM6167HCG-55	16384-word x 1-bit RAM (CMOS) 203
HM6264P-10       8192-word x 8-bit RAM (CMOS)       211         HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-17       8192-word x 1-bit RAM (CMOS)       215         HM6264LP-16       8192-word x 1-bit RAM (CMOS)       221         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS) <th></th> <td>HM6167HLP-45</td> <td>16384-word x 1-bit RAM (CMOS) 207</td>		HM6167HLP-45	16384-word x 1-bit RAM (CMOS) 207
HM6264P-12       8192-word x 8-bit RAM (CMOS)       211         HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-13       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-14       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         MOS DYNAMIC RAM       221       215         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       223         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       233		HM6167HLP-55	16384-word x 1-bit RAM (CMOS) 207
HM6264P-15       8192-word x 8-bit RAM (CMOS)       211         HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         MOS DYNAMIC RAM       211         HM4716A-1       16384-word x 1-bit RAM (CMOS)       215         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233		HM6264P-10	8192-word x 8-bit RAM (CMOS) 211
HM6264LP-10       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         MOS DYNAMIC RAM       215         HM4716A-1       16384-word x 1-bit RAM (CMOS)       215         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-5       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233   <		HM6264P-12	8192-word x 8-bit RAM (CMOS) 211
HM6264LP-12       8192-word x 8-bit RAM (CMOS)       215         HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         MOS DYNAMIC RAM       221         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233		HM6264P-15	8192-word x 8-bit RAM (CMOS) 211
HM6264LP-15       8192-word x 8-bit RAM (CMOS)       215         MOS DYNAMIC RAM       221         HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233		HM6264LP-10	8192-word x 8-bit RAM (CMOS) 215
MOS DYNAMIC RAM         221           HM4716A-1         16384-word x 1-bit RAM (NMOS)         222           HM4716A-2         16384-word x 1-bit RAM (NMOS)         222           HM4716A-3         16384-word x 1-bit RAM (NMOS)         222           HM4716A-4         16384-word x 1-bit RAM (NMOS)         222           HM4716A-7         16384-word x 1-bit RAM (NMOS)         222           HM4716A-4         16384-word x 1-bit RAM (NMOS)         222           HM4716AP-1         16384-word x 1-bit RAM (NMOS)         222           HM4716AP-2         16384-word x 1-bit RAM (NMOS)         222           HM4716AP-3         16384-word x 1-bit RAM (NMOS)         222           HM4716AP-3         16384-word x 1-bit RAM (NMOS)         222           HM4716AP-4         16384-word x 1-bit RAM (NMOS)         222           HM4716AP-4         16384-word x 1-bit RAM (NMOS)         223           HM4816A-3         16384-word x 1-bit RAM (NMOS)         233           HM4816A-4         16384-word x 1-bit RAM (NMOS)         233           HM4816A-7         16384-word x 1-bit RAM (NMOS)         233		HM6264LP-12	8192-word x 8-bit RAM (CMOS)
HM4716A-1       16384-word x 1-bit RAM (NMOS)       222         HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-5       16384-word x 1-bit RAM (NMOS)       223         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233		HM6264LP-15	8192-word x 8-bit RAM (CMOS)
HM4716A-2       16384-word x 1-bit RAM (NMOS)       222         HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233	ľ		
HM4716A-3       16384-word x 1-bit RAM (NMOS)       222         HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233		HM4716A-1	16384-word x 1-bit RAM (NMOS)
HM4716A-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       223         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233		d la serie de la ser	16384-word x 1-bit RAM (NMOS) 222
HM4716AP-1       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-3E       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233			16384-word x 1-bit RAM (NMOS) 222
HM4716AP-2       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-3E       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233			16384-word x 1-bit RAM (NMOS) 222
HM4716AP-3       16384-word x 1-bit RAM (NMOS)       222         HM4716AP-4       16384-word x 1-bit RAM (NMOS)       222         HM4816A-3       16384-word x 1-bit RAM (NMOS)       233         HM4816A-3E       16384-word x 1-bit RAM (NMOS)       233         HM4816A-4       16384-word x 1-bit RAM (NMOS)       233         HM4816A-7       16384-word x 1-bit RAM (NMOS)       233			16384-word x 1-bit RAM (NMOS)
HM4716AP-4         16384-word x 1-bit RAM (NMOS)         222           HM4816A-3         16384-word x 1-bit RAM (NMOS)         233           HM4816A-3E         16384-word x 1-bit RAM (NMOS)         233           HM4816A-4         16384-word x 1-bit RAM (NMOS)         233           HM4816A-7         16384-word x 1-bit RAM (NMOS)         233			16384-word x 1-bit RAM (NMOS) 222
HM4816A-3         16384-word x 1-bit RAM (NMOS)         233           HM4816A-3E         16384-word x 1-bit RAM (NMOS)         233           HM4816A-4         16384-word x 1-bit RAM (NMOS)         233           HM4816A-7         16384-word x 1-bit RAM (NMOS)         233			
HM4816A-3E         16384-word x 1-bit RAM (NMOS)         233           HM4816A-4         16384-word x 1-bit RAM (NMOS)         233           HM4816A-7         16384-word x 1-bit RAM (NMOS)         233		61	
HM4816A-4         16384-word x 1-bit RAM (NMOS)         233           HM4816A-7         16384-word x 1-bit RAM (NMOS)         233			200
HM4816A-7 16384-word x 1-bit RAM (NMOS)			
HWI46 TOAP-3 T0384-WORD X T-DIT RAM (NMOS) 233			
		HM4816AP-3	10304-word x 1-bit HAM (NMOS) 233

() HITACHI

4

	HM4816AP-3E	16384-word x 1-bit RAM (NMOS)
	HM4816AP-4	16384-word x 1-bit RAM (NMOS)
	HM4816AP-7	16384-word x 1-bit RAM (NMOS) 233
	HM4864-2	65536-word x 1-bit RAM (NMOS) 241
	HM4864-3	65536-word x 1-bit RAM (NMOS) 241
	HM4864P-2	65536-word x 1-bit RAM (NMOS) 241
	HM4864P-3	65536-word x 1-bit RAM (NMOS) 241
	HM4864CC-2	65536-word x 1-bit RAM (NMOS) 251
	HM4864CC-3	65536-word x 1-bit RAM (NMOS) 251
	111140041-2	65536-word x 1-bit RAM (NMOS)
	HM48641-3	65536-word x 1-bit RAM (NMOS) 256
	HM4864K-2	65536-word x 1-bit RAM (NMOS) 256
	HM4864K-3	65536-word x 1-bit RAM (NMOS) 256
	HM4864A-12	65536-word x 1-bit RAM (NMOS) 260
	HM4864A-15	65536-word x 1-bit RAM (NMOS) 260
	HM4864A-20	65536-word x 1-bit RAM (NMOS) 260
	HM4864AP-12	65536-word x 1-bit RAM (NMOS) 260
	HM4864AP-15	65536-word x 1-bit RAM (NMOS) 260
	HM4864AP-20	65536-word x 1-bit RAM (NMOS)
	HM4864ACG-12	65536-word x 1-bit RAM (NMOS) 265
	HM4864ACG-15	65536-word x 1-bit RAM (NMOS) 265
	HM4864ACG-20	65536-word x 1-bit RAM (NMOS)
	HM4865AP-12	65536-word x 1-bit RAM (NMOS) 270
	HM4865AP-15	65536-word x 1-bit RAM (NMOS) 270
	HM4865AP-20	65536-word x 1-bit RAM (NMOS)
	HM50256-12	262144-word x 1-bit RAM (NMOS) 277
	HM50256-15	262144-word x 1-bit RAM (NMOS) 277
	HM50256-20	262144-word x 1-bit RAM (NMOS) 277
	HM50257-12	262144-word x 1-bit RAM (NMOS) 284
	HM50257-15	262144-word x 1-bit RAM (NMOS) 284
1072	HM50257-20	262144-word x 1-bit RAM (NMOS) 284
• N	IOS Mask ROM	291
	HN61364P	8192-word x 8-bit ROM (CMOS)
	HN61364FP	8192-word x 8-bit ROM (CMOS)
	HN61365P	8192-word x 8-bit ROM (CMOS) 294
	HN61366P	8192-word x 8-bit ROM (CMOS)
	HN43128P	16384-word x 8-bit or
	1000	32768-word x 4-bit ROM (CMOS)
	HN613128P	16384-word x 8-bit ROM (CMOS)
	HN613128FP HN61256P	16384-word x 8-bit ROM (CMOS)
	HIND1250P	32768-word x 8-bit or
	HN61256FP	65536-word x 4-bit ROM (CMOS)
	HING1250FP	
	HN613256P	05530-word x 4-bit ROW (CIVIOS)
	HN613256FP	
	HN62301P	32768-word x 8-bit ROM (CMOS)
	IOS PROM	
	HN462716	2048-word x 8-bit U.V. Erasable &
	HIN402710	FULL MAIL DE OTA MARCON BUNNED
	HN462716G	
	HIN402710G	
	HN462532	Electrically PROM (NMOS)
		Electrically PROM (NMOS)
		AUTION

() HITACHI

5

	HN462532G	4096-word x 8-bit U.V. Erasable &
	CSU.	Electrically PROM (NMOS) 314
	HN462732	4096-word x 8-bit U.V. Erasable &
	(20)	Electrically PROM (NMOS) 318
	HN462732G	4096-word x 8-bit U.V. Erasable &
	DO second and the	Electrically PROM (NMOS) 318
	HN462732G1	4096-word x 8-bit U.V. Erasable &
	0001	Electrically PROM (NMOS) 322
	HN482732AG-20	4096-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 325
	HN482732AG-25	4096-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 325
	HN482732AG-30	4096-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 325
	HN482764	8192-word x 8-bit U.V. Erasable &
280		Electrically PROM (NMOS) 328
280	HN482764-3	8192-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 328
200	HN482764-4	8192-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS)
	HN482764G	8192-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 328
270	HN482764G-3	8192-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 328
	HN482764G-4	8192-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS) 328
	HN4827128G-25	16384-word x 8-bit U.V. Erasable &
277		Electrically PROM (NMOS) 332
	HN4827128G-30	16384-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS)
	HN4827128G-45	16384-word x 8-bit U.V. Erasable &
		Electrically PROM (NMOS)
	HN48016P	2048-word x 8-bit Electrically Erasable &
292		PROM (NMOS)
	Bipolar RAM	341
296	HM10414	256-word x 1-bit RAM (ECL 10K) 342
	HM10414-1	256-word x 1-bit RAM (ECL 10K)
	HM2110	1024-word x 1-bit RAM (ECL 10K) 346
	HM2110-1	1024-word x 1-bit RAM (ECL 10K)
	HM2112	1024-word x 1-bit RAM (ECL 10K)
	HM2112-1	1024-word x 1-bit RAM (ECL 10K) 350
	HM10422	256-word x 4-bit RAM (ECL 10K) 355
	HIVI10422-7	256-word x 4-bit RAM (ECL 10K)
	HM10470	4096-word x 1-bit RAM (ECL 10K)
	HM10470-1	4096-word x 1-bit RAM (ECL 10K) 363
	HM10470F	4096-word x 1-bit RAM (ECL 10K) 363
	HM10470-15	4096-Word x 1-bit RAM (ECL 10K)
	HM2142	4096-word x 1-bit RAM (ECL 10K) 371
	HM10474	1024-word x 4-bit RAM (ECL 10K)
	HM10474-15	1024-word x 4-bit RAM (ECL 10K)
	HM10480	16384-word x 1-bit RAM (ECL 10K)
	HM10480F	16384-word x 1-bit RAM (ECL 10K)
	HM100415	1024-word x 1-bit RAM (ECL 100K)
	HM100415CC	1024-word x 1-bit RAM (ECL 100K) 382



	HM100422	256-word x 4-bit RAM (ECL 100K)
	HM100422F	256-word x 4-bit RAM (ECL 100K)
	HM100422CC	256-word x 4-bit RAM (ECL 100K)
	HM100470	4096-word x 1-bit RAM (ECL 100K)
	HM100470-15	4096-word x 1-bit RAM (ECL 100K)
	HM100474	1024-word x 4-bit RAM (ECL 100K)
	HM100474-15	1024-word x 4-bit RAM (ECL 100K)
	HM100474F	1024-word x 4-bit RAM (ECL 100K)
	HM100474F-15	1024-word x 4-bit RAM (ECL 100K)
	HM100480	16384-word x 1-bit RAM (ECL 100K)
	HM100480F	16384-word x 1-bit RAM (ECL 100K)
	HM2504	256-word x 1-bit RAM (TTL)
	HM2504-1	256-word x 1-bit RAM (TTL)
	HM2510	1024-word x 1-bit RAM (TTL)
	HM2510-1	1024-word x 1-bit RAM (TTL)
	HM2510-2	1024-wrod x 1-bit RAM (TTL)
	HM2511	1024-word x 1-bit RAM (TTL)
	HM2511-1	1024-word x 1-bit RAM (TTL)
	Bipolar PROM	£.85w2
	HN25044	1024-word x 4-bit PROM (TTL)
	HN25045	1024-word x 4-bit PROM (TTL)
	HN25084	2048-word x 4-bit PROM (TTL)
	HN25085	2048-word x 4-bit PROM (TTL)
	HN25084S	2048-word x 4-bit PROM (TTL)
	HN25085S	2048-word x 4-bit PROM (TTL)
	HN25088	1024-word x 8-bit PROM (TTL)
	HN25089	1024-word x 8-bit PROM (TTL)
	HN25088S	1024-word x 8-bit PROM (TTL)
	HN25089S	1024-word x 8-bit PROM (TTL)
	HN25088L	1024-word x 8-bit PROM (TTL)
	HN25089L	1024-word x 8-bit PROM (TTL)
	HN25168S	2048-word x 8-bit PROM (TTL)
	HN25169S	2048-word x 8-bit PROM (TTL)
	Memory Support Cir	cuits
	HD2912	Quadruple TTL-to-MOS Clock Drivers
	HD2916	Quadruple TTL-to-MOS Clock Drivers
	HD2923	Quadruple ECL-to-TTL Drivers
	8 9	

## NOTICE

The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied products. The company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

**HITACHI** 

# QUICK REFERENCE GUIDE TO HITACHI IC MEMORIES

MOS RAM

8

266-word x 4-bit 8AM (ECL 100K) . . 286-word x 4-bit 8AM (ECL 100K) . . .

	Total	88		Organi- zation	Access Time	Cycle Time	Supply Voltage	Power Dissi-	-	116	Pa	ckaş	te*	Replace-	Page		
Mode	Bit	Type No.	Process	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	(ns) max	(ns) min	(V)	(W)	Pin No.	CC	CG	G	P	FP	SP	ment	Pag
		HM4334-3	1.1	CAUTE	300	460		IT PATT	110.	1	1.94					HM-6514-9	52
		HM4334-4	1.19	CL 1001	450	640	x byo	10µ/20m		110	1.10						5
		HM4334-3L			300	460	x bro	H-1201	1.81	1753	1.45	101					5
		HM4334-4L	. (24	ECL 100	450	640	a brow	10µ/20m		1	13.0	00					5
		HM6148	. 128	EGL 101	70	70	C Bragan			190	BA					2148	6
		HM6148-6			85	85	1 8 33	0.1m/0.2								2148-6	6
		HM6148L		Sec. 54	70	70	1× 55	- 10 0			1-2	083					6
		HM6148L-6		1024×4	85	85	x bro	5µ/0.2			0	135					6
		HM6148H-35**		(JT	35	35	x.b.c.	1024-4	1		E-d	•					7
		HM6148H-45**			45	45	x bbr	0.1m/0.2			0.0					2148-45	7
		HM6148H-55**			55	55	x bee	1021-1			1					2148-55	7
1.0	4k-bit	HM6148HL-35**			35	35	or hear	1026.4	18		1.1	101					7
	4K-DIL	HM6148HL-45**			45	45		5µ/0.3	18	1	10	19		1751			7
		HM6148HL-55**		(STT	55	55	N Darry	1028-9			6.21	1.71					7
		HM6147		LATT	70	70	x buo	0.1m/75m			20					2147	8
		HM6147-3			55	55	w takes	0.1m//5m			2.0						8
		HM6147L			70	70		5µ/75m			30		•				8
		HM6147L-3		LITT	55	55	2 biot	3µ/73m									8
		HM6147H-35	1.1.1.1	4096×1	35	35		0.000			1	•	•			2147H-1	9
		HM6147H-45	100	4090 ~ 1	45	45		0.1m/0.15			19.62					2147H-2	9
Static		HM6147H-55	CMOS		55	55	+5	8-92.01			20						9
Juli		HM6147HL-35	CMOS	. (311	35	35		9-23-03			1930						9
		HM6147HL-45	1.53	1. 1311	45	45	× prev	5µ/0.15	1.2	1	100	103	•				9
		HM6147HL-55	1.24	. UTT	55	55	× 910	1024-8		1	1930	003	•				9
- 1		HM6116-2		- 1712	120	120	K (B)(D)	V-15507				•	•	•			10
		HM6116-3	120.00	- WILL	150	150		0.1m/0.18				•	•	•			10
		HM6116-4		- CLITE	200	200	× Back	2048.4		1	•	•	•	•			10
		HM6116L-2	-5.5	. 1171.	120	120	× 0101	2048-9		R	30	•	•	•			12
		HM6116L-3	1.1.1	in and	150	150		20µ/0.16	0	101	11.2		•	•	1		12
		HM6116L-4	119	onk Driv	200	200	T elos	Guedn			15	•	•	•			12
		HM6116A-10	178	oth Driv	100	100	FT slo.	Costra			-2	195	•		•		15
		HM6116A-12		210VT	120	120	pia Ed	0.1m/15m			5	195	•		•		15
	16k-bit	HM6116A-15	-	2048×8	150	150			24	-	_		•		•		15
1		HM6116A-20			200	200		_		_			•		•		15
		HM6116AL-10			100	100						_	•		•		15
		HM6116AL-12			120	120		5µ/10m		-			•		•	out 1	15
		HM6116AL-15	diaces	th other	150	150	00 00	nuonia be	ila	-	-	-	•		•		15
		HM6116AL-20	danabi		200	200	en bri	-	-	-	-	-	•				15
		HM6117-3	date	yns tot any	150	150		0.1m/0.2	140	_			•	•			16
		HM6117-4			200	200	General			-	-	1	•		1		16
		HM6117L-3	-	- THE PERSON A	150	150	-	10µ/0.18	1	-			•	•	100	15	172
		HM6117L-4			200	200		NUMBER OF STREET						•			172

(to be continued)

	Total	and the second second		Organi- zation	Access Time	Cycle Time	Supply Voltage	Power Dissipa-			Pac	kage	***			Replace-	
Mode	Bit	Type No.	Process	(word ×bit)	(ns) max	(ns) min	(V)	tion (W)	Pin No.	cc	CG	G	P	FP	SP	ment	Page
		HM6168H-45*		00	45	45	1 Land									2168	184
		HM6168H-55*	1-1-1-		55	55	1	0.1m/0.25									184
		HM6168H-70*			70	70	1										184
		HM6168HL-45*	1.00	4096×4	45	45	10.050		1		-			-			185
		HM6168HL-55*			55	55	1	5µ/0.25			-						185
		HM6168HL-70*	1		70	70	11.1869	0,0.20									185
		HM6167			70	70	1.5.6955	nuos l-								2167	186
		HM6167-6	82	Sec. 60	85	85	112 482	25m/0.15								2167-6	186
	16k-bit	HM6167-8	-		100	100	6.118855		20							2167-8	186
		HM6167L	100	1.1	70	70	+ - 102.02	-					0	-			192
		HM6167L-6	-	Sector.	85	85	8,6353	5µ/0.15			-	tie,	0	-			192
SRAM		HM6167L-8	CMOS	16384×1	100	100	+5	5,470.15		-	1.00	20		- 2	-		192
	611	HM6167H-45	100	222.3	45	45	10.000						•	-		IMS1400	192
	100000	HM6167H-45	-	Dia g	45	45	-	0.1m/0.2	-	-			•	-		10101400	190
		HM6167HL-45			45	45	-		-		-	-			-		207
	SUI	HM6167HL-45		6.785	45	45	-	$5\mu/0.2$		-	-	-	•	-	-		207
	L-AREP		1.65		1.2.2.1	1000	10.000		-	-	-	110					207
	1.1013	HM6264-10		10.210	100	100	-	0 1 /0 0	- 3	-	-	1	-	-	-		
	C-ADER	HM6264-12	-		120	120	-	0.1m/0.2				-	•	-	-		211
	64k-bit	HM6264-15	-	8182×8	150	150	-		28		-	-		-	-		211
	6-530	HM6264L-10	18	222.0	100	100	8-580			-	-	-		-	-		215
	1.101	HM6264L-12	1 21		120	120	-	10µ/0.2		-			•	_			215
825		HM6264L-15	-	-	150	150	-			-	-		•	-			215
		HM4716A-1			120	320	+12,			2.40		•	•	_	-		222
		HM4716A-2	19	0.25.0	150	320	+5,	20m/0.46	110	1.3	100	•	•	_		MK4116-2	222
		HM4716A-3	-		200	375	-5,		1.77	2.3	10	•	•	_		MK4116-3	222
	16k-bit	HM4716A-4	100	16384×1	250	410	1. 1. 1. 1.	a sub-w		-	1.1	•		_	-	MK4116-4	222
	and the second	HM4816A-3			100	235	-					•		_		2118-3	233
		HM4816A-3E	-		105	200	-	11m/0.15				•	•	_			233
		HM4816A-4			120	270	1					•	0			2118-4	233
		HM4816A-7			150	320						•	•			2118-7	233
		HM4864-2	1	BOW	150	270	<b>TEMPE</b>	20m/0.33	35	.0	101	•	•				241
		HM4864-3			200	335			-		-	.0	.0				241
DRAM		HM4864A-12	NMOS		120	230	1		16		0	•	•				260
11	64k-bit	HM4864A-15		65536×1	150	260		20m/0.275		21		•	•				260
	UTA DIL	HM4864A-20		00000771	200	330	+5					۰	•				260
		HM4865A-12**		1221	120	230	10						•				270
		HM4865A-15**			150	260		20m/0.275					•				270
	0.0	HM4865A-20**	1	144	200	330				-							270
	10 Q	HM50256-12**		655	120	220											277
	0.9	HM50256-15**		0.01	150	260		20m/0.35		1.161							277
	256k-bit	HM50256-20**		262144×1	200	330				101		•					277
	200K-DIL	HM50257-12**		202144 × 1	120	220					131/						284
Get		HM50257-15**		0.01	150	260		20m/0.35		10	1.00	0					284
-		HM50257-20**	0.0	-	200	330											284

Under development
 \*\* Preliminary △HM6116LP Series : 10µW
 \*\*\* The package codes of CC, CG, P, FP and SP are applied to the package materials as follows. CC : Side-brazed Ceramic Leadless Chip Carrier, CG : Glass-sealed Ceramic Leadless Chip Carrier, G : Cerdip, P : Plastic DIP, FP : Small Sized Plastic Flat Package(SOP), SP : Skinny Type Plastic DIP

**OHITACHI** 

Replace- Page	Total		Diseipa-	Organi- zation	Access Time	Supply Voltage	Power Dissi-	mail	Pac	kage	***	at l	Replace-	Page
Program	Bit	Type No.	Process	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	(ns) max	(V)	pation (W)	Pin No.	С	G	P	FP	ment	
184	1 13	HN61364	NE. Past.	2	250	100		28		001				292
	64k-bit	HN61365		8192×8	250	101	5µ/0.05			01				294
		HN61366	RT Busi		250	25		24			0	10 M.2		296
	128k-bit	HN43128		16384×8 32768×4	6500	01	3 m	28	1	1-1		Se Mile		298
Mask	LOOK DIL	HN613128	CMOS	16384×8	250	+5	5µ/0.05	28					1	300
	256k-bit	HN61256		32768×8 65536×4	3500	901	7.5m	28			•	•	- 118-201	302
		HN613256	21.00	32768×8	250		5µ/75m		-	1				304
	1M-bit	HN62301**		131072×8	350	Table 1	5m/60m	28		3-		1.561		306
100T 2042 19141	16k-bit	HN462716	1	2048×8	450	45	0.555	24			1	112	2716	310
		HN462532	2. (Var).	1	38	122	0.858				153	3348	TM S2532	314
	1	HN462732	5.04m2		450	4.5	0.788		•		100	(abc)	2732	318
	32k-bit	HN482732A-20	a ta tage	4096×8	200	82		24			10.5	800	2732A-2	325
	1.13	HN482732A-25	NMOS		250	1991	0.788				-	1	2732A	325
U. V. Erasable		HN482732A-30	Carl.	9	300	122			-				2732A-3	325
& Electrically		HN482764		-	250	+5	5162						2764	328
	64k-bit	HN482764-3	- C. T. MA	8192×8	300	051	0.555	28	•		1.1.1	1.1.1	2764-3	328
215		HN482764-4			450	0.81					200	350		328
		HN4827128-25**			250	0011					6.81	110		332
	128k-bit	HN4827128-30**	NMOS	16384×8	300	000	0.554	28			AdT	1.623		332
		HN4827128-45**			450	2005			1	•	8.37	2.263	1	332
Electrically Erasable	16k-bit	HN48016	NMOS	16384×8	350	+5	0.16	24		1		1	Sec. mill	336

\* Under development

Once development
 \*\* Preliminary
 \*\*\* The package codes of C, G, P and FP are applied to the package materials as follows.
 C : Side-brazed Ceramic DIP, G : Cerdip, P : Plastic DIP, FP : Plastic Flat Package

## MOS MEMORIES OF WIDE OPERATING TEMPERATURE RANGE

Mode	Total Bit	Type No.	Organization (word×bit)	Operating Temperature Range	Access Time (ns)	Power Dissipation	Packa	Page			
		6	STORAGE STORAGE	(°C)	max	(W)	Pin No.	Р	G	1	
0.98	10	HM6116I-2	tto Mast	130 180	120		TRANSPORT			107	
	1 0	HM6116I-3		alf off	150	0.1m/0.18	ALL LING			107	
		HM6116I-4		A1-1 107-2	200	1927				107	
	101.14	HM6116LI-2	2048×8	-40 to +85	120	18 **	Transf			131	
Static RAM	16k-bit	HM6116LI-3		088 005	150	20µ=/0.16	24		•	131	
		HM6116LI-4		1.220 . 1221	200	- 11 ····				131	
		HM6116K-3	28. Thuilt	080 080	150	1000			•	150	
285	1.1	HM6116K-4		-55 to +125	200	0.1m/0.18	SAN SEA ST			150	
		HM4864I-2			150	and the second	THE SPEC	1		256	
		HM4864I-3	another as a	-40 to +85	200	1 km 11 .9 .00	The sales	1.754	•	256	
Dynamic RAM	64k-bit	HM4864K-2	65536×1	Star Plane, DEP	150	- 15m/0.3	16	2.2		256	
		HM4864K-3		-55 to +85	200					256	
EPROM	32k-bit	HN 4627321	4096×8	-40 to +85	450	0.1/0.788	24		•	322	

△ HM6116LPI Series : 10µ ₩

	Total		Organi- zation		Access Time	Supply Voltage	Power Dissipa-	ł	Pack	age**			D
Level	Bit	Type No.	$\binom{word}{\times bit}$	Output	(ns) max	(V)	tion (mW/bit)	Pin No.	F	G	cc	Replacement	Page
1.25	256-bit	HM10414	256 - 1		10		2.8					F10414	342
114	200-DIL	HM10414-1	256×1		8		2.0	101		•			342
	481735	HM2110			35		0.5	16		•		F10415	346
		HM2110-1	1024×1		25		0.5			•		F10415A	346
	1k-bit	HM2112	1024 ^ 1	256	10		0.8	89.0E					350
123	1K-DIL	HM2112-1			8		0.8						350
ECL	35130	HM10422	256×4		10		0.8	24			1.5	F10422	355
ECL 10k	18181	HM10422-7	230 ^ 4		7	-5.2	1.0	24					360
IUN		HM10470		698	25		140					F10470	363
		HM10470-1	4096×1		15		0.2	18			1.14		363
	4k-bit	HM10470-15	4090×1	Open	15		10	18					368
	4K-DIT	HM2142		Emitter	10	P	0.3				10		371
101		HM10474	1004 - 4		25		1.0 0.0				-	F10474	374
		HM10474-15	1024×4	10 <b>0</b>	15		0.2	24			1.5		374
	16k-bit	HM10480	$16384 \times 1$		25	1.0.11.0.11.0.00	0.03	20				F10480	379
	1k-bit	HM100415	$1024 \times 1$	]	10		0.6	16				F100415	382
	1 K-DIL	HM100422	256  imes 4		10		0.8	24				F100422	385
Dat		HM100470	4096×1	1	25		0.0	18		0		F100470	388
ECL 100k	4k-bit	HM100470-15	4090 × 1		15	-4.5	0.2	18					388
1006	4 K-Dit	HM100474	1024×4	]	25		0.0					F100474	391
		HM100474-15	1024 ^ 4		15		0.2	24					391
	16k-bit	HM100480*	16384  imes 1		25		0.05	20				F100480	396
	256-bit	HM2504	256×1		55		1.0					93411	399
	200-Dit	HM2504-1	200 ~ 1		45		1.8			0		93411A	399
		HM2510		Open Collector	70					0			403
TTL		HM2510-1	1	Conector	45	+5	0.5	16				93415	403
	1k-bit	HM2510-2	1024×1		35							93415A	403
		HM2511		3-state	70		0.5						407
		HM2511-1		3-state	45		0.5					93425	407

\* Preliminary
 \*\* The package codes of F, G and CC are applied to the package material as follows.
 F : Flat Package, G : Cerdip, CC : Side-brazed Ceramic Leadless Chip Carrier

**OHITACHI** 

## BIPOLAR PROM

6

-12

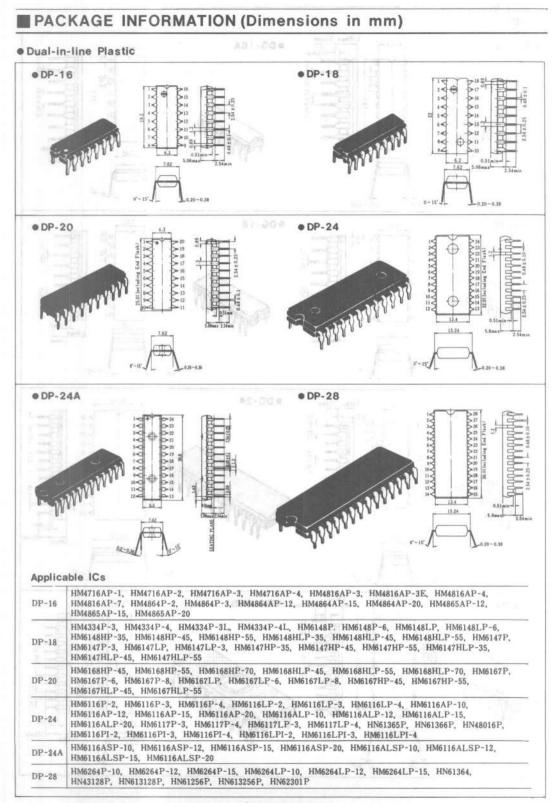
MAR PALICPUE

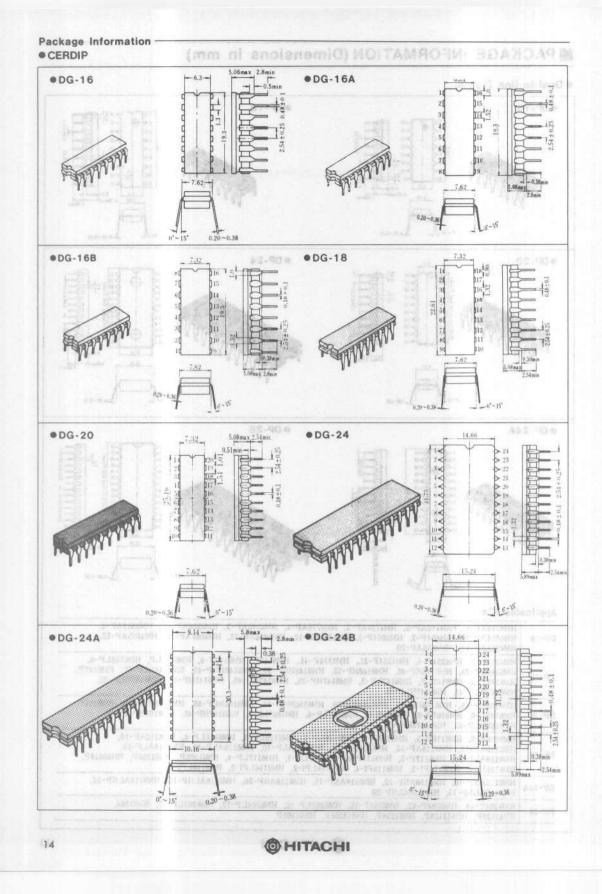
Total		Organi- zation	enff million	Access Time	Supply Voltage	and the second s		Pa	ckage*		Level .	
Bit	Type No.	$\begin{pmatrix} word \\ \times bit \end{pmatrix}$	Output	(ns) max	(V)	pation (mW)		- H	G	Р	Keplacement	Pag
FILLE	HN25044		0/C		A					114	82S136	414
4k-bit	HN25045	1024×4	3-s	50		500	18			o la co	82S137	414
215013	HN25084		0/C							2.01	82S184	419
.6214013	HN25085		3-s	60						00	82S185	419
	HN25084S	2048×4	0/C			550	18			1.53	in the last	423
	HN25085S		3-s	- 50					•	5.00		422
STADIS	HN25088		0/C	1				-	•	UN 1	82S180	425
8k-bit	HN25089		3-5	60	+5	-				1103	82S181	42
OLIOIN	HN25088S		0/C			600	-			11(0)		42
	HN25089S		3-s	50		1			•	16-9		42
1.	HN25088L		0/C			. Open			•	1.00		43
	HN25089L		3-s	100	1. 34	350		-		06		43
1.1000	HN25168S	-	0/C		C						82S190	43
16k-bit	HN25169S	2048×8	3-s	60	8 I.	600	24		•		82S191	43
ckage code of	G is applied to th	he material as fo	ollows.		25		D-SCHOLD		14844	141	Edex61	-
rdip	0 0											
	45											
									1-07472			
	1.11											
	Bit 4k-bit 8k-bit 16k-bit chage code of t	Total Bit HN25044 HN25045 HN25084 HN25084 HN25085 HN25085 HN25088 HN25089 HN2508 HN25089 HN2508 HN250 HN250 HN250 HN250 HN250 HN250 HN250 HN250 HN250 HN250 HN250	Total Bit     Type No.     zation (word) ×bit)       4k-bit     HN25044     1024×4       HN25085     1024×4       HN25085     2048×4       HN25085S     1024×4       HN25085S     1024×4       HN25088S     1024×4       HN25088S     1024×4       HN25088S     1024×8       HN25089S     1024×8       HN25089S     1024×8       HN25089L     1024×8 </td <td><math display="block"> \begin{array}{ c c c c c } \hline Total Bit \\ \hline Type No. \\ \hline &amp; \begin{array}{c} zation \\ (word) \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \begin{array}{c} 0 \\ \hline &amp; \end{array} \end{array} \begin{array}{c} Output \\ \hline &amp; \end{array} \end{array} </math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td> <td>Total Bit         Type No.         zation (word) (×bit)         Output bits         Time (ns) max         Voltage (V)         Dissi- pation (mW)         Pin No.         F         G         P         Replacement           4k-bit         HN25044         1024×4         O/C         3-s         50         18         0         225135           4k-bit         HN25085         2048×4         O/C         60         18         0         225137           4k-bit         HN25085         2048×4         O/C         60         +5         18         0         225136           8k-bit         HN25088         0/C         60         +5         600         24         0         825180           8k-bit         HN25088         1024×8         O/C         60         +5         600         24         0         825181           1024×8         O/C         3-s         100         350         0</td>	$ \begin{array}{ c c c c c } \hline Total Bit \\ \hline Type No. \\ \hline & \begin{array}{c} zation \\ (word) \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} word \\ \times bit \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \begin{array}{c} 0 \\ \hline & \end{array} \end{array} \begin{array}{c} Output \\ \hline & \end{array} \end{array} $	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Total Bit         Type No.         zation (word) (×bit)         Output bits         Time (ns) max         Voltage (V)         Dissi- pation (mW)         Pin No.         F         G         P         Replacement           4k-bit         HN25044         1024×4         O/C         3-s         50         18         0         225135           4k-bit         HN25085         2048×4         O/C         60         18         0         225137           4k-bit         HN25085         2048×4         O/C         60         +5         18         0         225136           8k-bit         HN25088         0/C         60         +5         600         24         0         825180           8k-bit         HN25088         1024×8         O/C         60         +5         600         24         0         825181           1024×8         O/C         3-s         100         350         0

manufactor of the

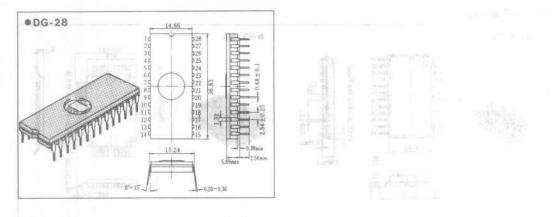
, we first as factoric reaching of a finite set  $30~{\rm ker}$  (  $3.3~{\rm k}$  ), where  $g_{\rm eff}$  (  $g_{\rm eff}$  ) is

**HITACHI** 





### Package Information

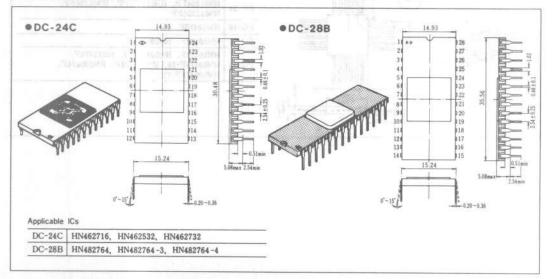


## Applicable ICs

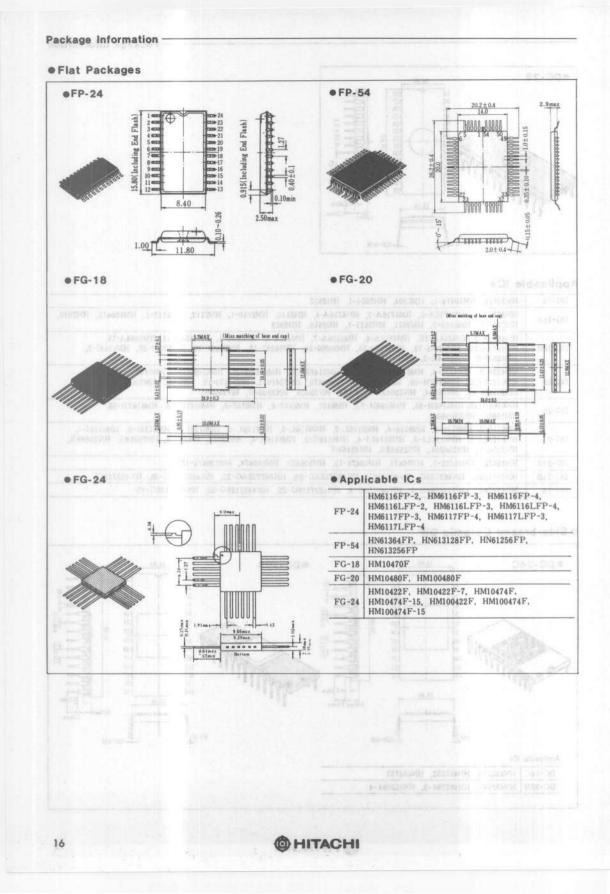
0.0-23.4

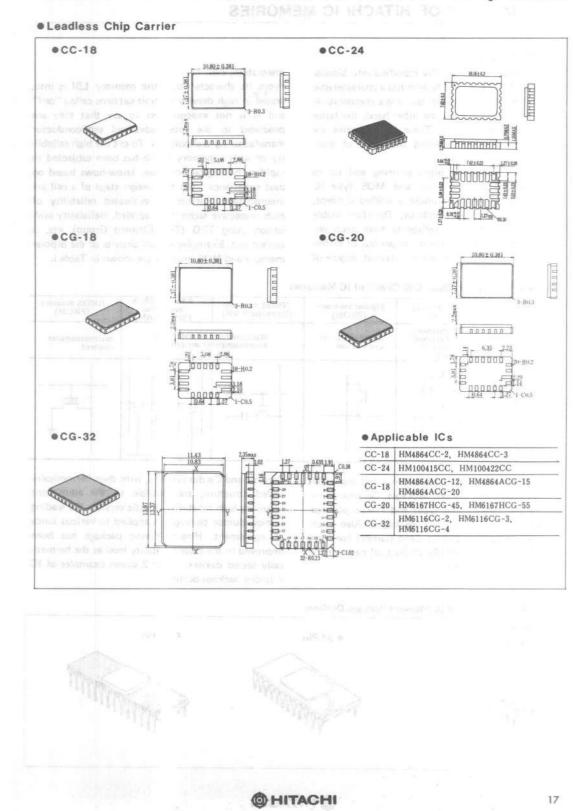
DG-16	HM10414, HM10414-1, HM2504, HM2504-1, HD2912
DG-16A	HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM2110, HM2110-1, HM2112, HM2112-1, HM100415, HM2510, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923
DG-16B	HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4864-2, HM4864-3, HM4864A-12, HM4864A-15, HM4864A-20, HM50256-12, HM50256-15, HM50256-20, HM50257-12, HM50257-15, HM50257-20, HM4864I-2, HM4864I-3, HM4864K-2, HM4864K-3
DG-18	HM4334-3, HM4334-4, HM6148, HM6148-6, HM6148H-35, HM6148H-45, HM6148H-55, HM6147, HM6147-3, HM6147H-35, HM6147H-45, HM6147H-55, HM10470, HM10470-1, HM10470-15, HM2142, HM100470, HM100470-15, HM25044, HN25085, HN25085, HN25084S, HN25085S
DG-20	HM6168H-45, HM6168H-55, HM6168H-70, HM6167, HM6167-6, HM6167-8, HM6167H-45, HM6167H-55, HM10480, HM100480
DG-24	HM6116-2, HM6116-3, HM6116-4, HM6116L-2, HM6116L-3, HM6116L-4, HM61161-2, HM61161-3, HM61161-4, HM6116L1-2, HM6116L1-3, HM6116L1-4, HM6116K-3, HM6116K-4, HN25088, HN25089, HN25088S, HN25089S, HN25088L, HN25088L, HN25168S, HN25169S
DG-24A	HM10422, HM10422-7, HM10474, HM10474-15, HM100422, HM100474, HM100474-15
DG-24B	HN462716G, HN462532G, HN462732G, HN482732AG-20, HN482732AG-25, HN482732AG-30, HN462732GI
DG-28	HN482764G, HN482764G-3, HN482764G-4, HN4827128G-25, HN4827128G-30, HN4827128G-45

### Side-brazed Ceramic DIP



15





## RELIABILITY OF HITACHI IC MEMORIES

### **1. STRUCTURE**

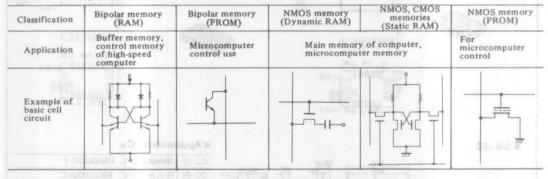
IC memories are structurally classified into bipolar type and MOS type. The former has a characteristic of an extremely high speed. But it is a comparatively small capacity and on the other hand, the latter features a large capacity. These IC memories are utilized by effectively taking the most of their respective characteristics.

Flows from designing, manufacturing and up to inspection for both Bipolar and MOS type IC memories are established under a unified concept, design and inspection standards. Therefore stable results concerning their reliability have been obtained with these IC memories, regardless of differences in the circuit design, pattern, layout, degree of integration, etc.

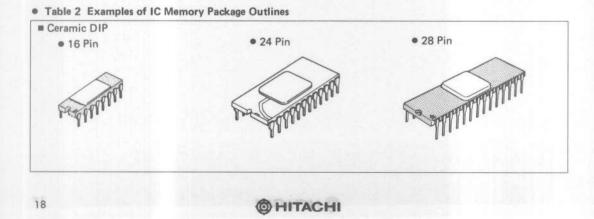
From its characteristics, the memory LSI is integrated in high density by unit patterns called "cell" and it is not exaggeration to say that they are produced in the most advanced semiconductor manufacturing technologies. To get the high reliability of such a memory which has been subjected to rapid technological advances, know-hows based on past experience from the design stage of a cell are incorporated. Farther to evaluated reliability of each respective technology applied. Reliability evaluation using TEG (Test Element Group), etc. is carried out. Examples of cell circuits of the Bipolar memory and MOS memory are shown in Table I.

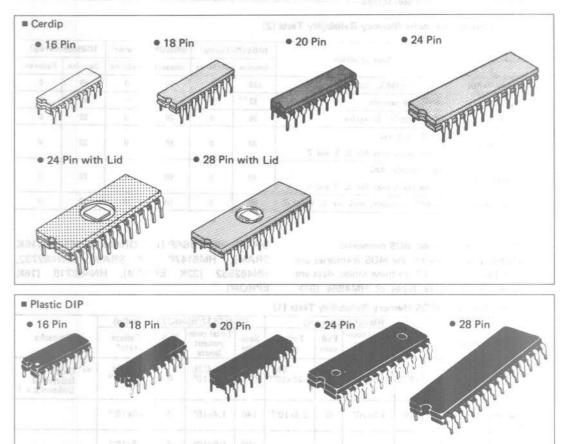
67-334

Table 1 Examples of Basic Cell Circuit of IC Memories



IC memory chips produced in the latest technologies are sealed in different packages. Ceramic package, Cerdip (glass-sealed type) and Plastic package are the current major IC packages. Also such packages as LCC (Leadless Chip Carrier) for high package density and SO (Small Outline) package are now under development. Ceramic and Cerdip versions, with their hermetically sealed structure, are suitable to the equipment requiring high reliability. Plastic version, the leading semiconductor package, is applied to various kinds of equipment. Hitachi Plastic package has been improved to the close reliability level as the hermetically sealed devices. Table 2 shows examples of IC memory package outlines.





## 2. RELIABILITY DATA Results of reliability tests are listed below.

## 2-1 Reliability test data on Bipolar memories The reliability test data on the Bipolar memories are shown in Tables 3 and 4. Since they are manufactured under the aforementioned standardized design

rules and quality control, there is no difference in reliability among various types. In addition, it can be said that the greater the capacity, the higher the reliability per bit.

	-483 F	HM10470 (Cerdip)				HM100422(Chip Carrier)				HN25089(Cerdip)			
Test item	Test condition	sam- ples	Total component hours	Fail- ures	Failure rate*	Sam- ples	Total component hours	Fail- ures	Failure rate*	Sam- ples	Total component hours	Fail- ures	Failure rate *
	<i>Ta</i> =125°C		C. H.		1/hr				-		С. Н.		1/hr
	$V_{EE} = -5.2V(\text{HM10470})$ $V_{cc} = 5.5V(\text{HN25089})$	125	4.0×10 <sup>5</sup>	0	2.3×10	2.0	ā -	104	1 20	36	3.6×10 <sup>4</sup>	0	2.6×10 <sup>-#</sup>
High- temperature (Operating)	$ \begin{array}{c} T_{a} \! = \! 150^{\circ} \mathbb{C} \\ V_{xx} \! = \! -5.2^{\circ} (\mathrm{HM10470}) \\ V_{xx} \! = \! -5.0^{\circ} (\mathrm{HM100422}) \\ V_{cc} \! = \! 5.5^{\circ} \mathrm{V} \\ t_{cr} \! = \! 1.\mu_{\mathrm{S}} \end{array} \! \left. \left( \mathrm{HN25089} \right) \right. $	80	2.7×10 <sup>s</sup>	0	3.4×10 <sup>-4</sup>	40	4×10*	0	2.3×10 <sup>-1</sup>	10	1.0×10*	0	9.2×10 <sup>-1</sup>
High- temperature - storage	Ta-200 °C	27	2.7×10 <sup>3</sup>	0	3.4×10 <sup>-5</sup>	40	4×10*	0	2.3×10 <sup>-5</sup>	15	1.5×10 <sup>4</sup>	0	6.1×10 <sup>-1</sup>
	Ta=295*C	20	2.0×10 <sup>5</sup>	0	4.6×10 <sup>-5</sup>	40	4×104	0	2.3×10 <sup>-5</sup>	15	1.5×10*	0	6.1×10 <sup>-1</sup>

Table 3 Results on Bipolar Memory Reliability Tests (1)

**OHITACHI** 

Reliability of Hitachi IC Memories

Table 4 Results on Bipolar Memory	Reliability	lests (2)	
-----------------------------------	-------------	-----------	--

1		HM10470	(Cerdip)	HM100422(0	hip carrier)	HN25089(Cerdip)	
Test item	Test condition	Samples	Failures	Samples	Failures	Samples	Failures
Temperature cycling	-65 °C~+150 °C, 10 cycles	120	0	40	0	45	0
Soldering heat	260 °C, 10 seconds	22	0	No. HS	-	22	0
Thermal shock	0°C~+100°C, 10 cycles	36	0	20	0	22	0
Mechanical shock	1500G, 0.5 ms, Three times each for X, Y and Z	30	0	60	0	22	0
Variable frequency	100~2000Hz, 20G Three times each for X, Y and Z	40	0	60	0	22	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	60	0	22	0

### 2-2 Reliability test data on MOS memories

The reliability test data on the MOS memories are shown in Tables 5, 6 and 7. In these tables, data are shown on representative types of HM4864 (64K DRAM), HM4716AP (16K DRAM), HM6116P (16K SRAM), HM6147P (4K SRAM), HN462732, HN462532 (32K EPROM), HN462716 (16K EPROM)

<ul> <li>Table 5 Results on MOS Memor</li> </ul>	y Reliability Tests (1)
--	-------------------------

	0 28 PG	1000	HM4864 (	(Ceran	nic)	HN	462532/HN	462732	2 (Cerdip)	0 10 Pin
Test item	Test condition	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Remarks
High- temperature dynamic operation	Ta=125°C V <sub>CC</sub> =5.5V t <sub>cyc</sub> =3μs	1872	C.H. 3.33×10 <sup>6</sup>	3*1	l/hr 1.25×10 <sup>-6</sup>	100	C.H. 1.0x10 <sup>5</sup>	0	l/hr 9.2×10⁻⁰	*1 Oxide failure × 2 Unknown × 1
High- temperature, storage	Ta=200° C	20	4.0×10 <sup>4</sup>	0	2.3×10 <sup>-5</sup>	140	1.4×10 <sup>s</sup>	0	6.6×10 <sup>-6</sup>	
High- temperature storage	Ta=259° C	-	-		-	100	5.0×104	0	1.8×10 <sup>-5</sup>	
High- temperature storage	Ta=295° C	-0.9	and A star	675	alus =	100	4.2×10 <sup>4</sup>	1*2	4.8×10 <sup>-5</sup>	*2 Data disappearance

\* Estimated failure rate with confidence level 60%

## Table 6 Results on MOS Memory Reliability Tests (2)

			HM4716A	P (Plas	stic)	H	M6116P/HM	16147P	(Plastic)	11 C
Test item	Test condition	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Sam- ples	Total com- ponent hours	Fail- ures	Failure rate*	Remarks
High- temperature dynamic operation	$\begin{array}{c} Ta=125^{\circ}C \\ V_{DD}=13.2V \\ (NMOS) \\ V_{CC}=5.5V \\ (CMOS) \\ t_{cyc}=3\mu s \end{array}$	2330	C.H. 3.46×10 <sup>6</sup>	6*1	1/hr 2.12×10 <sup>-6</sup>	1216	C.H. 1.90×10 <sup>-6</sup>	3*2	l/hr 2.19×10 <sup>-6</sup>	*1 Oxide failure × 6 *2 Oxide failure × 1 Electrostatic discharge ×1 Unknown × 1
High- temperature storage	Ta=150°C	45	4.5×10 <sup>4</sup>	0	2.0×10 <sup>-5</sup>	20	2.0×104	0	4.6×10 <sup>-5</sup>	
High- temperature and high- humidity bias	Ta=85°C, RH=85% VDD=12V (NMOS) VCC=5.5V (CMOS)	3081	6.2×10 <sup>6</sup>	19*3	3.1×10 <sup>-6</sup>	630	1.3×10 <sup>6</sup>	4*4	4.0×10 <sup>-6</sup>	<ul> <li>*3 Aluminium corrosion × 17 Unknown × 2</li> <li>*4 Aluminium corrosion × 3 Unknown × 1</li> </ul>

\* Estimated failure rate with confidence level 60%.

Table 7	Results on MOS	Memory	Reliability	Tests (3)
---------	----------------	--------	-------------	-----------

m !:.		HM4864 (Ceramic)		HM4864 (Cerdip)		EPROM (Cerdip)		HM4716AP		HM6116P/ HM6147P	
Test item	Test condition	Sam- ples	Fail- ures	Sam- ples	Fail- ures	Sam- ples	Fail- ures	Sam- ples	Fail- ures	Sam- ples	Fail ures
Temperature cycling	-65°C~RT~150°C 10 cycles	1208	0	260	0	50	0	-	-	-	-
Temperature cycling	-55°C~RT~150°C 10 cycles	-	-	-	-	310	0	7892	0	2080	0
Temperature cycling	-55°C ~ 150°C 1000 cycles	164	0	100	0	50	0	600	0	-	-
Thermal shock	-65°C ~ 150°C 15 cycles	22	0	60	0	72	0	190	0	-	-
Thermal shock	0°C ~ 100°C 15 cycles	-	-	-		197	0	138	0	60	0
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	128	0	60	0
Mechanical shock	1,500G, 0.5ms	22	0	38	0	38	0	- 1	-	1	<u></u>
Variable frequency	20~2,000Hz, 20G	22	0	38	0	38	0	-	-	<u>~</u>	-
Constant- acceleration	20,000G	22	0	38	0	38	0	-	-	-	-

### 2.3 Change of electrical characteristics under endurance test for IC memories

The degradation of  $I_{CBO}$  of the cell transistor, degradation of  $h_{FE}$ , etc., can be considered as main factors in the internal elements for reliability of Bipolar memories. In actual element designing,

however, it has been designed to operate in the range at which these degradations do not happen. Therefore changes of electrical characteristics including access time are not observed.

Time dependence in access time for HM10470 is shown in Fig. 1.

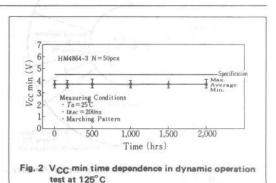
### Fig. 1 Example of Change in Bipolar Memory Characteristics

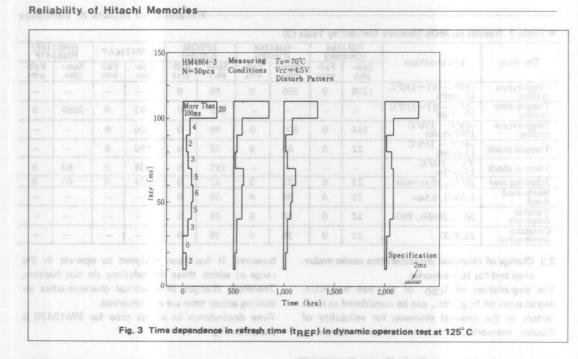
Example Example of time change in access time for Bipolar memory HM10470 Device name Test condition Ta=125°C, VEE=-5.2V Maximum Measuring Condition Average Failure criteria Minimum  $t_{AA} = 25 ns$ 35 Marching Pattern Failure mechanism Surface degradation 30 Results: taa (ns) Access time (tAA) is stabilized and is within the failure 25 criteria. 20 15 1,000 Time (hr)

**OHITACHI** 

 $V_{TH}$  is a basic parameter in the MOS memories, however, it has been confirmed there is not any shift in  $V_{TH}$  for practical usage because we have applied surface stabilizing technique, clean process, etc.

In case of dynamic RAM which needs refresh cycle, refresh time is also stabilized owing to the abovementioned process. Time dependence of Vcc min and  $t_{REF}$  characteristics for the 64K DRAM are shown in Fig. 2 and 3.





## 2.4 Classification of failure modes

Examples of failures happened in the field are shown in Fig. 4 and 5. Since memory LSIs generally require the most fine processing in semiconductor manufacturing technology, the percentage of failures resulting from pinholes, photoresist defects, foreign materials, etc., is tending to increase. To eliminate the latent defects which are generated in these manufacturing processes, we are constantly improving these processes, and performing burn-in screening under high temperature for all memories. In addition, since the analysis of failures in the field can result in important feedback to improve their design and manufacturing, we are always exerting our efforts to collect customer process data and field data with the aim of further establishing their high reliability.

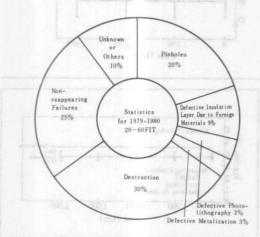


Fig. 4 Classification of Failure Modes of Bipolar Memory in the field

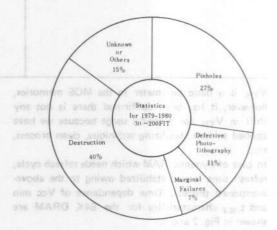


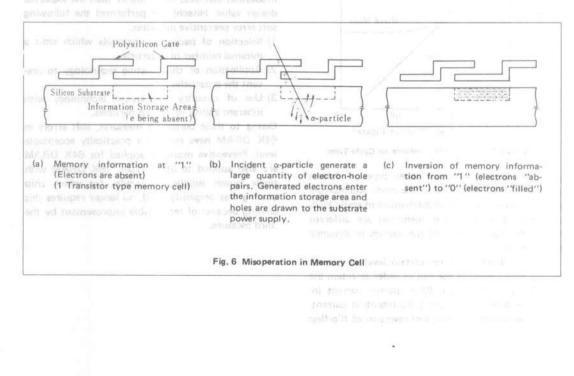
Fig. 5 Classification of Failure Modes of MOS Memory in the field

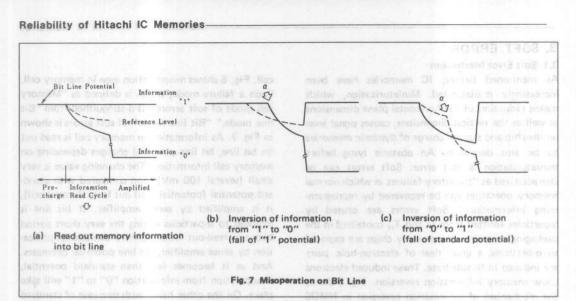
## 3. SOFT ERROR

### 3.1 Soft Error Mechanism

As mentioned before, IC memories have been increasingly miniaturized. Miniaturization, which means reduction of the horizontal plane dimensions as well as the vertical dimensions, causes signal level on the chip and storage charge of dynamic memories to be also decreased. An obstacle lying before miniaturization is soft error. Soft errors can be characterized as "transitory failures in which normal memory operation can be recovered by reprogramming information." Soft errors are caused by  $\alpha$ -particles emitted from U and T<sub>H</sub> contained in the packaging materials. As memory chips are exposed to α-particles, a great deal of electron-hole pairs are induced in Si substrate. These induced electrons cause memory information reversion. Fig. 6 shows the mechanism of information reversion in NMOS dynamic memory by *a*-particles. In case of NMOS dynamic memory, negative voltage is applied to the Si substrate. Therefore, positive holes are drawn by substrate, and only electrons cause information reversion (from information "1" to "0") of memory

cell. Fig. 6 shows misoperation seen in memory cell. Such a failure mode, which is defined as "Memory cell mode of soft errors," is distinguished from "Bit line mode." "Bit line mode" of soft errors is shown in Fig. 7. As information in memory cell is read out on bit line, bit line potential changes depending on memory cell information. The changing value is very small (several 100 mV), and compared with standard potential (potential read out from dummy cell). it is amplified by sense amplifier. If bit line is exposed to a-particles during the very short period between read-out from memory cell and amplification by sense amplifier, bit line potential decreases. And as it becomes less than standard potential, misoperation from information "0" to "1" will take place. On the other hand, with decrease of standard potential, misoperation from information "1" to "0" is seen. Both are called "Bit line mode" because errors appear at irradiation of  $\alpha$ -particles. Soft error dependence on cycle time is shown in Fig. 8.





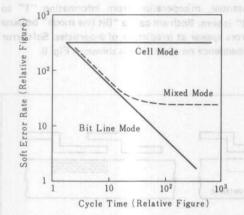


Fig. 8 Soft Error Rate's Dependence on Cycle Time

Actual products will have three types of failure modes, that is, cell mode, bit line mode and mixture of both modes. Soft error mechanism of static MOS memories and of bipolar memories are different from the above-mentioned mechanism in dynamic MOS memories.

In case of static memory, certain level of current always flows through the cell in order to retain the data in flip-flop circuit. When partial current induced by  $\alpha$ -particles exceeds the retention current, misoperation occurs because of reversion of flip-flop circuit.

### 3.2 Examples of soft error preventive measures in products

At the initial stage of the 64K DRAM development, its soft error rate was estimated from accelerated irradiation test data to be higher than the expected design value. Hitachi has performed the following soft error preventive measures.

- Selection of packaging materials which emit a minimal number of α-particles.
- Application of chip coating technology to prevent the α-particles.
- Use of circuitry and layout technology with inherent ability to resist α-particles.

Owing to these corrective measures, soft errors in 64K DRAM have reached a practically acceptable level. Preventive measures applied for 64K DRAM are also applied to other types. 16K DRAM with single power supply 5V family, for which chip coating was originally used, no longer requires this coating because of remarkable improvement by the third measure.

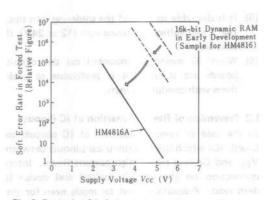


Fig. 9 Example of Soft Error Improvement on 16K-bit Dynamic RAM

3.3 Request for soft error preventative measures in system equipment

Thus our efforts to reduce soft errors have resulted in almost trouble-free memories. System reliability can be more improved by supplying some functions, that is, ECC device for lage memory system and parity bit for small one.

nene en role ann ann o ch der A beilgoup ar son ha AD syntrafic fion is for fun al spatloy yits - ch maar on in dham at s Montes Internety, The builded with to hourd-or valley of faces at Mourr and no one fioff. Same pressure from with regler.

An out-off frequency of an entropy appointed and an entropy and reacted for such essay, appoint 9.3 youd high frequency mode to put between 10;

10.3 to laws? "H" 4'4

(i) a most of ICs by interny by most as "H" level and minisparation in our int commostion, "H" and provided as V a proof and solution as V a proof and solution as Pages refer them.

one memory is 400mN to rectars in the case many met on dra board, mitural to reading. Therefore, ing with velocity higher

## 4. RELIABILITY CLASSIFICATION

In designing IC memories, Hitachi classifies memory reliability by their application and controls the flows of design, production and test. Reliability can be roughly classified as follows:

- For large scale computers and electronic exchangers
- (II) For important parts for auto-motive application
- (111) General communication-industrial use

In using our products, therefore, we would like you to consider the classification of the application. Especially, when you are going to apply our memories to any special equipment, please do not hesitate to consult our sales engineering staff.

eterge to contain them in our entry and them in with entry and the star is with entry and an entry. Shall of administration when the effect in the for a first and mathematical the star and an

A semination of the semination of t

If a part to prover the solution
 If a part to prover the solution

an annow be arrived to succeed the second se

**HITACHI** 

A variety of IC memories of high-spped, high-power and static lower power dissipation CMOS have been developed and commercially available, which allows an electronics designer to properly select the one best suited for a particular application. However, he must be familiar with the advantages and disadvantages of the devices to make the optimum selection and to prevent them from malfunctioning or, in the worst case, from breaking down. Precautions for handling IC memories given below will help the electronics designers to work out their optimum circuit designs.

## 1. BIPOLAR IC MEMORY

### 1.1 Prevention of static electricity

Bipolar memories have been considered to have high resistance to the static electricity than MOS ICs. However, the presently available high speed IC, represented by bipolar memories, must be provided with a suitable preventive measure against the static electricity. Because their diffused junctions have become thinner than the conventional types, in order to perform higher capability. Take note of the following points.

- (1) Keep all terminals of a device in the conductive mat during transportation and storage to keep them at the same potential. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specially stated, all HITACHI IC memories will be shipped in our conductive mats. Store them as they are.
- (2) When handling by hand IC memories for inspection or connection, his finger must be grounded as shown in Fig. 1. Do not forget to insert a 1M ohm resistor to protect him against an electric shock.

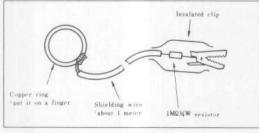


Fig. 1

- (3) It is advisable to control the ambient relative humidity at about 50 per cent to prevent the occurrence of static electricity.
- (4) It is also recommendable to wear cotton clothes instead of the ones made of synthetic fabrics to prevent the static electricity from occurring.

- (5) It is desirable to ground the soldering iron tips. Use a low voltage soldering iron (12 or 24V), if possible.
- (6) When IC memories mounted on the circuit boards are shipped, it is preferable to pack them with conductive mats.

## 1.2 Prevention of Reverse Insertion of IC Pinouts

In the case of reverse insertion of IC pinouts to board, ICs which have symmetrical pinouts between  $V_{EE}$  and Ground causes high current flown. Interconnection on the chip is melted and device is destroyed. Precaution must be made even for the ICs which do not have symmetrical pinouts between  $V_{EE}$  and Ground, because excess current flows and sometimes device is destroyed. On the device package, marking of No. 1 pin is stamped. Please watch this marking and insert ICs properly.

## 1.3 Mounting and Removal of ICs during Voltage is supplied

Usually, rather high current flows in regulator of bipolar memory. Therefore, if ICs are put in and pulled out to board during voltage is supplied, high voltage induced at current on/off destroys ICs. Mount and remove ICs after supply voltage is cut off. Same precaution must be made in measurement with tester.

### 1.4 Prevention of Oscillation

ECL bipolar memory has high cut-off frequency of transistor. Therefore, sometimes, oscillation is caused in relation with external circuit, and misoperation of ICs is occurred. In such cases, about 0.1  $\mu$ F of capacitor, which has good high frequency characteristics, is recommended to put between ICs and voltage supply line.

## 1.5 Precaution on Simple "H" Level of ECL Memory

In some cases, it is seen that input of ICs is directly connected to ground to fix input as "H" level. However, it sometimes causes misoperation in conjunction with internal circuit composition. "H" and "L" level of input are specified as  $V_{IL(min)}$  and  $V_{IH(max)}$  for ICs respectively. Please refer them and use ICs properly.

### 1.6 Cooling

Power dissipation of bipolar memory is 400mW to 1000mW depending on products. In the case many bipolar memories are mounted on the board, natural convention is insufficient for cooling. Therefore, please run forced air cooling with velocity higher



than 2.5m/s. In addition, by cooling, improvement of reliability can be expected as shown in Fig. 2. We recommend the junction temperature to be kept less than  $85^{\circ}$ C for high reliability use.

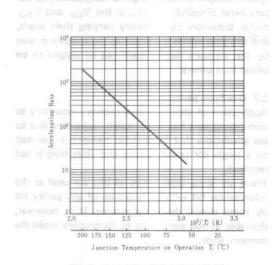


Fig. 2 Example of derating of ECL

### 1.7 Other Precautions

(1) Deforming of magazine and carrier

Since material of plastic magazine and carrier (for ECL flat package) is usually thermal plasticity, they deforms at temperature higher than 40 to 50°C and may not perform sufficiently. If burn-in is carried out at users, please use aluminum magazine or other metal fixtures.

### (2) Shock at transportation

Glass sealed type package is fragile. Usual handling and drop test (JIS C7021 A-8) on individual devices do not cause any problem. However, it devices packed in magazine receive strong shock such as drop shock, devices hit neighbouring devices and packages may be damaged. Therefore, at transportation or loading on/off, be careful not to drop them. Even after devices are mounted on board, IC packages may be damaged if strength of board is not enough and board receives strong deforming stress. Please be careful on strength of board and handling. If any questions rose at using Hitachi products, please feel free to contact closest Hitachi representatives or offices.

## 2. MOS IC MEMORY

2.1 Prevention of static electricity

Similar to bipolar IC memories, suitable preventive measures should be taken for MOS IC memories by referring to paragraph 1.1.

### 2.2 Absorption of power source noise

The source current level flowing in the dynamic memory during the time of access is considerably different from that of stand by. Although the current difference is quite effective to save the power consumption, the current spike may be developed into the power source noise. Since all MOS IC memories are, in general, accessed while being refreshed, it is recommended to insert large capacitors (a 10  $\mu$ F capacitor for every 9 pieces of 16K-bit HM4716A, for example) as well as a 0.1  $\mu$ F capacitor having good high-frequency characteristics for each memory. Needless to say, it is very important to reduce the power circuit impedance when designing.

#### 2.3 Current spike in VBB power

The V<sub>BB</sub> power is necessary for maintaining the IC memory function in the reverse bias and the current does not generally exceed the level of the reverse leakage current. However, in order to prevent an accidental current spike which is sharply formed in either positive or negative phase by the rise or fall clock pulse at the time of access, use a 0.1  $\mu$ F capacitor for every 2 or 3 memories for absorbing such noises.

### 2.4 Clock drive ICs

The TTL to MOS clock drive ICs have special designs so that they are capable of quick increase in the capacitive load. If a ground wire short-circuits either  $V_{DD}$  or  $V_{CC}$  which appear in the Pin No. 1 and No. 16 respectively, when the device is at high level, the device may be broken down. Carefully eliminate such possibility beforehand.

#### 2.5 Power application sequence

It is advisable to design the circuits so that power is applied in the sequence of V<sub>BB</sub>, V<sub>DD</sub> and V<sub>CC</sub> and interrupted in the reverse sequence, here the reverse bias V<sub>BB</sub> is applied first and interrupted last.

It may be impossible for some small-scaled systems to apply power in the above-mentioned sequence (for example, when the  $V_{BB}$  is supplied by a DC to DC converter). According to our experiments conducted in the under-mentioned test conditions, it



#### Precautions for Harding IC Memories

has been proved that such a small-scaled system as to consist of 200 to 300 memory devices is not affected by he power application sequence. Power application sequence test for N MOS IC

- Test method
   Ambient temperature: 25°C
- (1) Ambient temperature: 25 (
- (2) Power voltage: V<sub>DD</sub>=13.2V, V<sub>CC</sub>=5.0V,
- V<sub>IH</sub>=5.0V
   (3) Operation mode: AC operation ("0" to "16383" all bits scanning).
- $t_{cyc}=10 \ \mu s$ Read modify write oper-
- lis soni2 salon entro tion of eff offic hand web
- (4) V<sub>BB</sub> power: ON (1 min.) Floating
- (1 min.)
  - Here and the second sec
  - $\frac{1}{1} \frac{2}{2} \frac{3}{3} \frac{4}{4} \frac{5}{5}$   $\frac{1}{1} \frac{1}{1} \frac{$ 
    - anary humation in and in the law and descelly surgers the laws
- Type No.
   Number of cycles
   Number of sample
   Number of failures

   HM4716A
   2000 cycles
   50
   0
  - canacitor for every
  - CHARLES SHARE AND
  - The TTL to MOS doubeigns to that they are of the appartitive load. If a either Vipp or Vip who and Ho TB respectively, level, the davice may be efficience such possibility
  - 2.5 Power application set more in a detecte to design of all replied in the requestor V gas interrupted in the reletance of the biss V gas is applied first of the to apply power in the cover filter exercise when the original

drive ICs have special while of quick increase in uand wire short-cirruits expanse in the Pin No. 1 on the driving is at high broken down, Carefully creationd

2.) Test results

print districts so that power tarn V say V on and V oc at an equinos, here the tart rst of intercuted last, for one unall colled security he cola mentioned security

eventioned seed sequence a la supplied by a DC to a la supplied by a DC to b up a superiments onto in another seed strong in the seed strong set of the second in the second set of the second second in the second second second second second in the second second second second second second second in the second secon 2.6 Assessment of the memory system design It is quite effective to obtain the power margin curves (shmoo curve) for evaluating the memory system designs (timing margin or adaptability to the peripheral circuits). Investigate the  $V_{BB}$  and  $V_{DD}$ power behaviors by gradually varying their levels, and the ones which are closer to the margine shown by the memory device itself can be judged to be better than others.

### 2.7 Overhead parity bit

Application of MOS IC static memory especially to microcomputers has been rapidly increasing due to the advantages that MOS static memory is operated by a single 5V power source and refreshing is not required.

There are some cases where all bits are used as the information bit without inclusion of any parity bit by some circuit designing reasons. It is, however, desirable to add parity bits to thoroughly avoid the memory error.

fig. 2 . 6 . mapping of streaking of EOL

### .7 Other Pressuries:

- 1) Deforming of morecone and o
- Since material of plastle magazine and carrier (for ECL flat nackage) is temperature figher plasticity, they orforms at temperature figher then 48 to 50 ft and may not perform suffielently. If burned is carried out at owns, plaste
  - 2) Shock it transportation

Oless evalued true processes is fragilie, Usural marialing and or a test (JIS G2021 A-8) on extinuous devices do not cause any problem, how evich there is probled in mariatine monite any housing a strand problem may be any housing all tiens and problem may be obtained. Thereis an a strandportablem of loaddrive sevene evic mounted on beaud, HO and any the strandport of basic and stranger and basic testing of houring the not entropy and basic testing of houring on stranger and basic testing of houring housing kitsels produces, plane to any stranger and the stranger of testing of housing kitsels produces, plane to another the testing of the stranger of the strand through of the stranger of the stranger of the stranger of the stranger with the stranger of the stranger of the stranger of the stranger operates charger Mitachi representatives of



## 1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual users' purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality reuired by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize the quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality. In addition, quality required by users on semiconductor devices are going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

- Build the reliability in design at the stage of new product development.
- (2) Build the quality at the sources of manufacturing process.
- (3) Execute harder the inspection and reliability confirmation of final products.
- (4) Make quality level higher with field data feed back.
- (5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

## 2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

## 2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as wel as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

#### 2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely sude and execution of design standardization, device design (include process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishement of design rule, and standerdization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;

- Making clear about fundamental failure mode
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing
- 2 Effectiveness of evaluation by Test Site are as follows;
  - Common fundamental failure mode and failure mechanism in devices can be evaluated.
  - Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
  - Able to analyze relation between failure causes and manufacturing factors.
  - Easy to run tests.

etc.

#### 2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competition power of products, the major purpose of design review is to insure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even



for design changed products. Items discussed and determined at design review are as follows;

- Description of the products based on specified design documents.
- (2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub program of calculation, experiments, investigation, etc. will be carried out.
- (3) Determine contents of reliability and methods, etc. based on design document and drawing.
- (4) Check process ability of manufacturing line to achieve design goal.
- (5) Discussion about preparation for production.
- (6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
- (7) Reference of past failure experiences with similar devices, confirmation of method to provent them, and planning and execution of test program for confirmation of them. These study and decision are made using check lists made individually depending on the objects.

## 3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

### 3.1 Activity of Quality Assurance

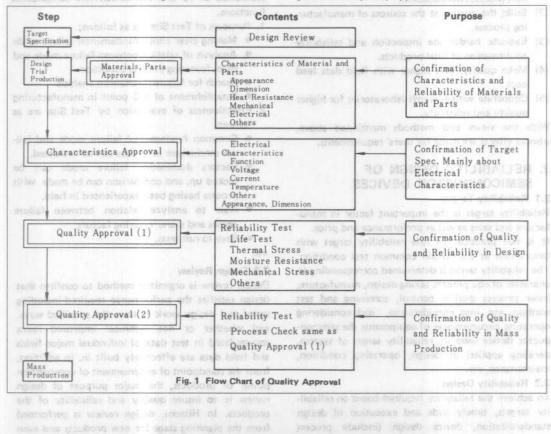
General views of overall quality assurance in Hitachi are as follows;

- Problems in individual process should be solved in the process. Therefore, at final product stage,
  - the potential failure factors have been already removed.
- (2) Feedback of information should be made to insure satisfied level of process ability.
- (3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

#### 3.2 Quality Approval

To insure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2. The views on quality approval are as follows;



**OHITACHI** 

 The third party executes approval objectively from the stand point of customers.

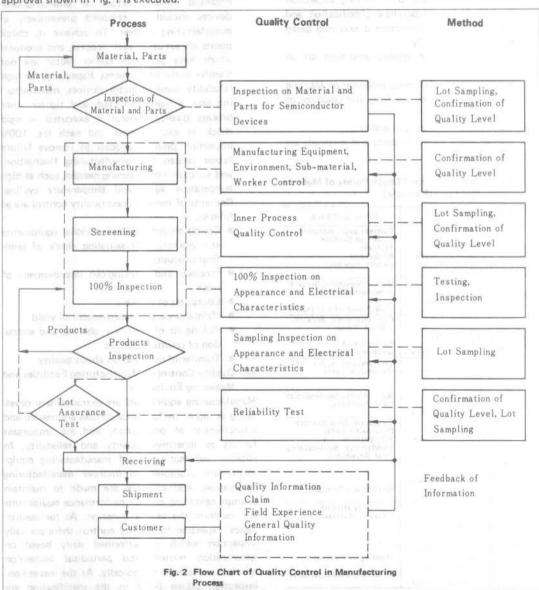
(2) Fully consider past failure experiences and information from field.

- (3) Approval is needed for design change and work change.
- (4) Intensive approval is executed on parts material and process.
- (5) Study process ability and fluctuation factor, and set up control points at mass production.

Considering the views mentioned above, quality approval shown in Fig. 1 is executed.

3.3 Quality and Reliability Control at Mass Producsensition and concernent according to the

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.



### 3.3.1 Quality Control of Parts and Material

As tendency toward higher performance and higher reliability of semiconductor devices, is going, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows;

- (1) Outside Vendor Technical Information Meeting
- (2) Approval on outside vendors, and guidance of outside vendors
- (3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

### Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance Dimension Sheet Resistance Defect Density Crystal Axis	Damage and Contamina- tion on Surface Flatness Resistance Defect Numbers
Mask	Appearance Dimension Resistoration Gradation	Defect Numbers, Scratch Dimension Level Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance Dimension Purity Elongation Ratio	Contamination, Scratch, Bend, Twist Purity Level Mechanical Strength
Frame	Appearance Dimension Processing Accuracy Plating Mounting Characteristics	Contamination, Scratch Dimension Level Bondability, Solderability Heat Resistance
Ceramic Package	Appearance Dimension Leak Resistance Plating Mounting Characteristics Electrical Characteristics Mechanical Strength	Contamination, Scratch Dimension Level Airtightness Bondability, Solderability Heat Resistance Mechanical Strength
Plastic	Composition Electrical Characteristics Thermal Characteristics Molding Performance Mounting Characteristics	Characteristics of Plastic Material Molding Performance Mounting Characteristics

#### 3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub materials. The manufacturing inner process quality control is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and tighter inner process quality control is executed - rigid check in each process and each lot, 100% inspection pointed process to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures
- Transfer of information about quality
- (2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipments are extraordinary developing as higher performance devices are needed and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain prompt operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection, which is performed periodically. At the inspection, inspection points listed in the specification are

## HITACHI

checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances – temperature, humidity, dust – and the control of submaterials – gas, pure water – used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

	Process	Contr	ol Point		Purpose of Control
	Y Purchase of Material				
Wafer-	1	Wafer	Characteri	stics, Appearance	Scratch, Removal of Crystal Defect Wafer
	Surface Oxidation	Oxidation			Assurance of Resistance
	Inspection on Surface Oxidation		Appearance Oxide Film	e, Thickness of	Pinhole, Scratch
	O Photo Resist	Photo Resist	-		
	Inspection on Photo Resist	Resist	Dimension,	Appearance	Dimension Level
	◇ PQC Level Check				Check of Photo Resist
	Diffusion	Diffusion	Diffusion D Resistance	epth, Sheet	Diffusion Status
	Inspection on Diffusion		Gate Width		Control of Basic Parameters
	◇ PQC Level Check		Characteri Breakdown	stics of Oxide Film Voltage	(Vтн, etc) Cleaness of surface Prior Check of Viн Breakdown Voltage Check
	Evaporation	Evapo- ration		of Vapor Film, ontamination	Assurance of Standard Thickness
	□ Inspection on Evaporation ◇ PQC Level Check		for a star ward		
	• Wafer Inspection	Wafer	tics	Vтн Characteris-	Prevention of Crack, Quality Assurance of Scribe
	hInspection on Chip Electrical Characteristics	Chip		Characteristics	
	OChip Scribe Inspection on Chip		Appearance	e of Chip	
	Appearance ◇PQC Lot Judgement				
Frame-	Assembling	Assaulting		(h. C).:-	Quality Charles ( Chin
	Assembling	Assembling	Bonding Appearance	e after Chip e after Wire	Quality Check of Chip Bonding Quality Check of Wire
	◇PQC Level Check			th, Compresion ar Strength	Bonding Prevention of Open and Short
	Inspection after Assembling			after Assembling	
2 5	◇PQC Lot Judgement		1.110		
Package	Sealing	Sealing	Appearance Outline, Di	e after Sealing	Guarantee of Appearance and Dimension
	◇PQC Level Check	Marking	Marking St		
	♦ Final Electrical Inspection ♦ Failure Analysis			Failures, Failure	Feedback of Analysis Infor-
	Anna Inneri		Mode, Mec	hanism	mation
	• Appearance Inspection Sampling Inspection on Products				
	O Receiving				
	Shipment				



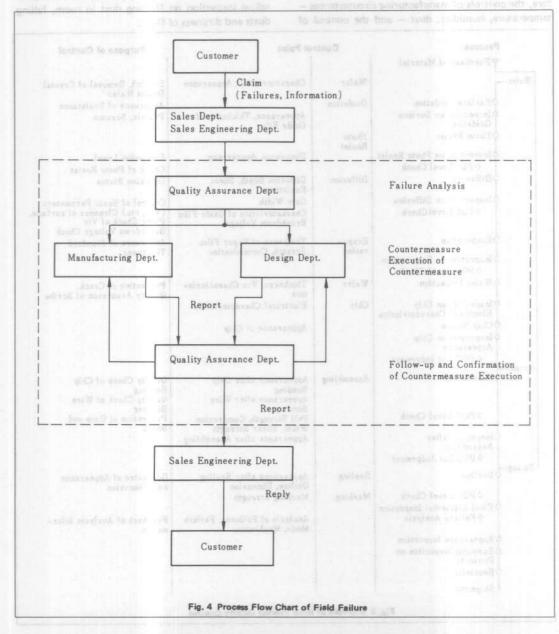
3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.



**OHITACHI** 

### OUTLINE OF TESTING METHOD

### 1. Inspection Method

Compared to conventional core memories, all peripheral circuits such as the decoder circuit, write circuit, read circuit, etc., are contained within the IC memories. As a result, all works of assembling the parts and performing electrical inspection, which had been carried out by core memory manufacturers in the past, have be come to be incorporated as works of IC manufacturers. Consequently, the electrical inspection of the memory IC has been faced to a more systematic inspection method and conventional IC inspection facilities have become completely useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a comparatively simple DC parameter facility. However, when the address input becomes multiplexed as in 16K memory, even the generation of the function test pattern becomes a serious problem. In the memory IC inspection, its guality cannot be judged by only inspecting DC characteristics related to external pins. This is because numbers of transistors, etc., related to the DC characteristics of the pins only amount to 1/1000 of all element numbers within IC memories. The following various address patterns are proposed to inspect whether or not the internal circuits are functioning correctly.

- (1) All "Low", all "High"
- (2) Checker flag
- (3) Stripe pattern
- (4) Marching
- (5) Galloping
- (6) Walking
- (7) Ping-pong

Although there are a lot of address patterns, only representative ones have been listed. These patterns are convenient for checking the mutual finter-ference of bits and sometimes are patterns with maximum power dissipation. Among the above-mentioned patterns, those of (1) to (4) are the socalled N patterns and these patterns are capable of checking IC memories of N bits with several sequences of N at most against the memory IC of N bits. Whereas, those of (5) to (7) are caled N<sup>2</sup> patterns and they need patterns several sequences of N<sup>2</sup>.

A serious problem arises in using the  $N^2$  patterns in a large-capacity memory, for example, a long period of about 30 minutes becomes necessary to perform inspection of the 16K memory with galloping pattern. Patterns from (1) (3) are comparatively simple and good methods, but they are not perfect against a failure in the decoder circuit. As the most simple pattern for inspecting the necessary memory function, there is a "Marching" pattern.

### 2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits written in "0"s. The addressing method will be explained for a simple 16 bit memory as an example.

- (1) Write "0" for all bits ..... Fig. 1(a)
- (2) Read "0" of 0th address and check that the read data is "0". Hereafter, the meaning of "Read" is "checking and judging the data".
- (3) Write "1" in the Oth address ..... Fig. I(b)
- (4) Read "0" of 1st address
- (5) Write "1" in 1st address
- (6) Read "0" of nth address
- (7) Write "1" in nth address ..... Fig. 1(c)
- (8) Repeat above procedures (6) and (7) up to the last. Finally, all data will become "1".
- (9) Since all data are "1"s in this condition, replace "0" and "1" after procedure (2) and repeat once more up to procedure (8).

It is understood that 5N address patterns are necessary for the N bit memory in this method.

		×		/ b				10						
0	0	0	0.	1	0	0	0	1	1	1	1			
0	0	0	0	0	0	0	0	1	I	1	1			
0	0	0	0	0	0	0	0	1	1	0	0			
0	0	0	0	0	0	0	0	0	0	Û	0			

Fig. 1 Addressing method for 16 bits memory in the Marching pattern

### 3. Generation of Marching Pattern

The method of generating the marching pattern and displaying failed bits of the memory on the Braun tube will be introduced. Fig. 2 shows the all block diagram. The address pattern is generated by using four synchronous 4 bit counters. All address patterns are shown in Fig. 4. This example, is for 16K bit memory, however, it can be easily understood that A14 which has a half frequency of the maximum address input A13 is the same as the data input.

The A15 signal together with the carrier signal of HD74161 is used to determinine the termination of the sequence.

As shown in Fig 2. In the read and write cycles after cleaning all bits addressing is twice the period of clearing. This switching is performed at the gate of



## **Outline of Testing Method-**

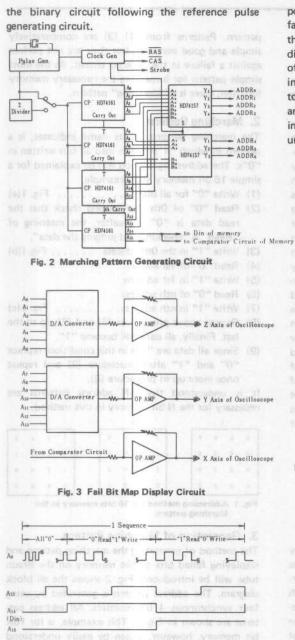
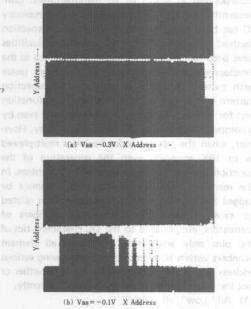


Fig. 4 Entire Pulse Relations

Input the output of HD74161 is input to the D/A converter and the output of D/A converter is connected to the oscilloscope to display  $\rightarrow$  X-Y matrix. The output of the comparator circuit is connected to the Z axis and performs luminous intensity modulation. In this way, the fail bit map can be displayed on the CRT. Fig. 5 shows an example checking a voltage margin. By changing the

power voltage  $V_{BB}$ , the increase and decrease of the failed bits can be well understood. The operation of the memory can be dynamically understood by displaying its operation on the CRT. The operation of the memory IC is extremely complicated differing from other TTLs, etc.. Its operation is not easy to understand by pulse waveform observation with an ordinary oscilloscope. The fail bit map as shown in Fig. 5 is extremely useful. It is capable of visually understanding the operation of memory IC.





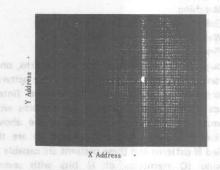


Fig. 6 Example of 1 bit solid fail

# 4. Failure Mode

Generally, failure  $70\% \sim 90\%$  of failures at users are of those called solid failure. This failure mode has no relation with access time, voltage margin and timing, and is not capable of reading from or writing to certain specified bits and is failure fixed to "0"



or "1". An example of single bit solid failure is shown in Fig. 6. The convenient checker, previously mentioned as simple tester, is sufficiently capable of detecting such failures. Therefore, with the exception of special cases, it can be considered that the necessity of performing high-precision measurements such as those made by memory IC manufacturers is rare.

In the inspection of memory IC at our company, full inspection under the worst conditions are performed so as to guarantee sufficient operations under all power voltage conditions and timing conditions listed in the data sheet.

An extremely accurate memory tester becomes necessary for performing high-precision inspection with 1ns accuracy. Our company is developing IC memory testers to supply memory ICs with excellent characteristics and quality to users and is establishing the system capable of developing further high-efficiency memory ICs.

Elimestate output with (a cutput is controlled by while CAS is fow, while a state when CAS is high, a cutous battomes is highvitic use as a common i/O

••• survivation to servitable of the createst accumulated to the createst accumulated device, and that y read or low and the service accumulated or an 846 bit, all bits rate be year only the service only the service only the the service of the cumulation of the

# Devision Guiper

troor of the compotion The tread fail auto the CAS signate in it. Sout returns to suite over the surfy write over increadurate one to over borrenat.

### SUSANA PARA

Incle up for the lask
 Increase cells f
 Increase and ware cells f
 Increase and Warehau
 Increase and Warehau
 Increase and Warehau
 Dimension RAMs i
 Dimension RAMs i
 Dimension RAMs i
 Dimension RAMs i
 Increase and certain William
 Increase and certain g
 Increase and certain g

() HITACHI

and a state when a substate of more state of the state of

A CONTRACTOR OF A CONTRACTOR

llen societaria anti il SAL' motore il more constanti

tente a dels a la cella del se Meta destato sere a concesa del concesa del sere

neta laveri glanace a company (1995) marchal EAS dent "read hini gallantadire- 1999 dgla paratan renovos see yee

# APPLICATION OF DYNAMIC RAMS

# 1. Power On

After turning on power to set the memory circuitry, hold for more than  $500\mu s$  and apply eight or more dummy loads before actuating the memory. The dynamic cycle may be either an ordinary memory cycle or a refresh cycle. When power is turned on, power-on current flows which varies with the rise time of V<sub>CC</sub> and clock conditions, as shown in Fig. 1. If the rise time is  $10\mu s$  or thereabout, the RAM does not operate dynamically and through-current passes to the internal inverter since the potential at the internal circuitry becomes unstable. Nevertheless, this through-current decreases as the operation of the internal circuitry becomes stable. With all this in mind, rise time of not shorter than  $100\mu s$  is recommended for power-up.

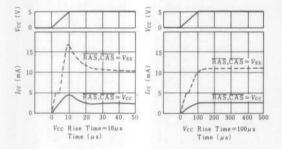


Fig. 1 Relationship between standard value of Icc and Vcc during power-up

## 2. Operation Modes (See Fig. 2)

(1) Read Cycle:

First, decide the X address of the memory cell chosen and start with trailing of  $\overline{RAS}$ . When the X address has been held by the internal circuitry, change it to Y address. Then, trail  $\overline{CAS}$  to take in the Y address. If the  $\overline{WE}$  pin is at high level, output will appear on the Dout pin after a certain time.

(2) Write Cycle:

The input at Din is written in the memory cell when  $\overline{\text{WE}}$  turns to low level before  $\overline{\text{CAS}}$ .

(3) Read/Modify/Write Cycle:

During this cycle,  $\overrightarrow{CAS}$  and, then,  $\overrightarrow{WE}$  are trailed down to low level so that data is read out from and written in the same address with in the same memory cycle.

(4) Page Mode Cycle:

In this cycle;  $\overrightarrow{CAS}$  is cyclically moved, after taking in the X address through  $\overrightarrow{RAS}$ , to scan only the Y address. This permits reading out and writing in only one column data at high speed.

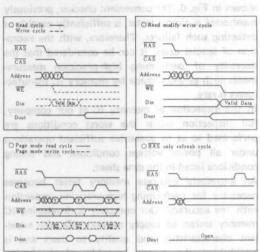


Fig. 2 Operating modes of Dynamic RAMs

# 2. Data Output

Dout is a TTL-compatible three-state output with two TTL-load fan outs. The output is controlled by the  $\overrightarrow{CAS}$  signals; it is held while  $\overrightarrow{CAS}$  is low, while Dout returns to a floating state when  $\overrightarrow{CAS}$  is high. In the early write cycle, the output becomes a highimpedance one to permit the use as a common I/O terminal.

# 3. Refreshing

Refreshing is a process of periodical rewriting to make up for the leakage of the charge accumulated in the memory cell. This operation is implemented in the RAS only refresh cycle, ordinary read cycle, and so on. Whether 16k- or 64k-bit, all bits can be refreshed by giving a 128-cycle scanning to only the X addresses between A0 and A6. To be more specific, each cycle refreshes 128 bits for the 16kbit Dynamic RAMs and 512 bits for the 64k-bit RAMs. Especially, the RAS only refresh cycle permits such a power-efficient refresh as calls for only approximately 75 percent of the current consumed by the read cycle. With CAS fixed at high level, the output is a high-impedance one. The HM4816A has a special function called the hidden refresh which enables holding the output by turning CAS to "low" while RAS only refresh is on. There are two methods of refreshing: concentrated and deconcentrated refreshing. The former gives a concentrated 128-cycle refresh after operating the memory for a period of 2ms maximum. In contrast, the latter repeats a refreshing cycle every 16µs following the initial 16µs (=2ms/128) memory operation. A



choice between the two modes calls for a careful consideration about the system's efficiency.

# 4. Operating Current for Dynamic RAMs

Fig. 3 shows the waveforms of the current applied in various operating modes (HM4864). The mean operating current in each mode equals the value obtained by dividing the integrated result of each waveform by the cycle time. The first peak current in each operating mode appears as a result of the circuit operation during the memory access time. On the other hand, the peak current during standby appear as a result of the precharging operation in each circuit. Having two circuitry operation modes - X and Y. Dynamic RAMs show different peak currents depending upon the operating timing of RAS and CAS. That is, the greatest peak current appears when both X and Y circuits operate simultaneously. The maximum peak current for the HM4864, for example, is approximately 100mA. The current consumed while the memory stands by on the board is expressed in terms of the cycle time dependency shown in Fig. 4. During standby, with a once-in-every 16µs refresh, the HM4864 consumes approximately 3mA of current.

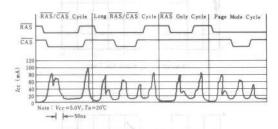
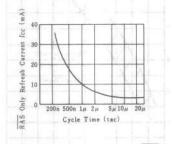
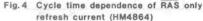


Fig. 3 Power supply voltage (HM4864)

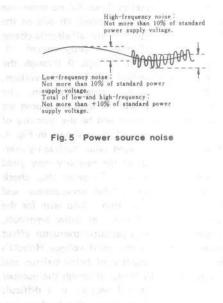




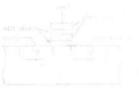
# 5. Noise

Broadly, noise can be classified into power source noise and input signal noise. With the latter, furthermore, whether it is an overshoot or undershoot must be considered. The overshoot should be

held below the highest input level specified. As to the undershoot, the input-undershoot-induced parasitic transistor effect in the input area is prevented by providing a -5V VBB to the three-way power source and a built-in bias circuit on the substrate. Normally, design should be such that the input undershoot does not exceed the minimum value specified for VIL, at worst. The power source noise can be further classed into low-frequency noise and high-frequency noise as shown in Fig. 5. To assure a stable memory operation, the peak-to-peak power supply voltage in the presence of low- or highfrequency noise should be held below 10 percent of its standard level. Overshoot and undershoot can be reduced by inserting a damping resistance of several tens of ohms in Dynamic RAM series. To prevent the power source noise, it is recommended to provide a condenser of 0,1µF or so to each one or two devices.



non and the second second



To stilled section & 013



# **PROGRAMMING & ERASING OF PROMS**

# 1. PROGRAMMING & ERASING OF EPROM

# 1.1 Programming the offer a problem of the

Information is programmed into the memory cell of an EPROM by applying a high voltage to its drain and gate (Fig. 1 and 2). The high voltage at the drain increases the energy of the electrons in the channel area. When the energy becomes high enough, the electrons become what are known as "hot electrons" that are capable of jumping across the oxide film. Pulled by the high voltage at the gate, the hot electrons are admitted into the floating gate. The electric charge entering the floating gate changes the threshold voltage in the memory element, whereby it is stored as new information. When reading out, voltage is applied as shown in Fig. 3, and "1" and "0" are identified by checking whether or not current flows. Since the drain voltage for read-out is set at about 3V, no erroneous writing takes place. When shipped, all bits of the EPROM are held at logic "1" with all electric charge released (with no information programmed in). By changing the logic 1 to logic 0 through the application of the specified waveform and voltage. the necessary information is programmed in. The higher the Vpp voltage and the longer the program pulse width tow, the more will be the quantity of electrons to be programmed in, as shown in Fig. 4. If the Vpp exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check Vpp overshoot by the PROM programmer and take all other possible caution. Also with for the negative-voltage-induced noise at other terminals, since it can touch off a parasitic transistor effect and apparently reduce the yield voltage Hitachi's EPROMs are usually capable of being written and erased more than 100 times, although the number of times is not guaranteed because it is difficult to give an exhaustive inspection prior to shipment. At any rate, 100 times is enough since the frequency of reprogramming in practical application rarely exceeds about 10 times.

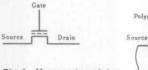
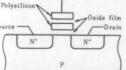


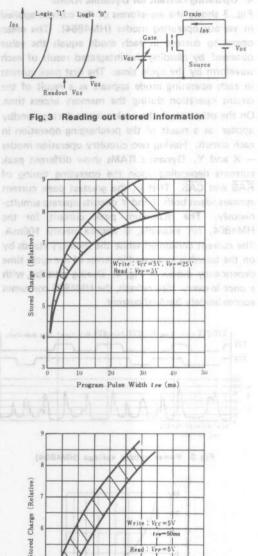
Fig. 1 Memory transistor circuit symbols

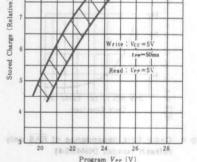


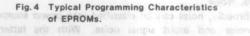
Gate

Fig. 2 Cross section of memory transistor

C HITACHI



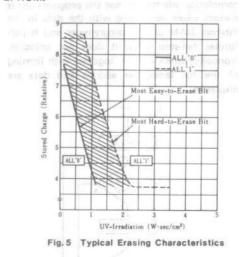






# 1.2 Erasing

Data strored in the EPROM is erased by releasing the electric charge from the floating gate through the exposure of the memory chip to ultraviolet light. Light has an energy that is inversely proportional to its wavelength. Receiving the energy of the ultraviolet light, the electrons in the floating gate are again turned into hot electrons, which jump across the oxide film into the control gate or substrate. As a result of this process, the stored information is erased. Accordingly, the stored information can not be erased by such lights whose wavelengths are too long to give adequate energy to jump over the barrier of the oxide film. For successful erasing, the wavelength and minimum exposure rate of ultraviolet light are specified as 2,537Å and 15W sec/cm<sup>2</sup> respectively. This condition is attained by exposing a device to an ultraviolet lamp of 12,000 $\mu$ W/cm<sup>2</sup> 1.2 ~ 3cm away for approximately 20 minutes. The ultraviolet light transmission rate of the transparent lid is about 70 percent. Any contamination or foreign material at the surface of the capsule lowers the transmission rate, prolonging the erasing time. So such contamination should be recovered by use of alcohol or other solvent that does not damage the package. Fig. 5 shows typical erasure characteristics for EPROM.



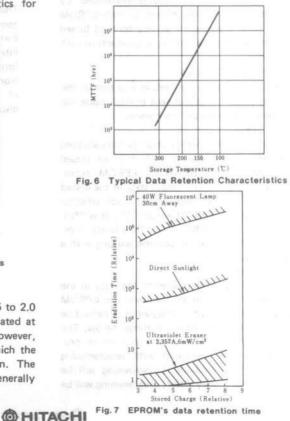
# 1.3 Data retention characteristic of EPROM

As a result of writing in, approximately 0.5 to 2.0  $\times 10^{-13}$  coulomb of electrons are accumulated at the floating gate. With the elapse of time, however, these electrons decrease, as a result of which the inversion of stored information can happen. The mechanism of electron dissipation is generally explained as follow:

(1) Data dissipation by heat

The accumulation of electrons at the floating gate is an unbalanced state, so the dissipation of thermally excited electron is unavoidable. Therefore, the data holding time has a close relationship with temperature. Fig. 6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

- (2) Data dissipation by ultraviolet light
  - Ultraviolet rays at a wavelength of not greater than  $3,000 \simeq 4,000$ Å is capable of releasing the electric charge stored in the memory of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet rays. so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Fig. 7 shows examples of the data retention time under an ultraviolet eraser, sunlight and fluorescent lighting. But it should be noted that the data for fluorescent light and sunlight are not definite because of their varying ultraviolet ray contents. The ultraviolet ray content in sunlight, for example, varies greatly with seasons, weather and the composition of the atmosphere.



### Programming & Erasing of PROMs

(3) Data dissipation by voltage

This type of data dissipation occurs while information is being written in. At other memory cells lying on the same word line or data line as the memory cell being programmed, high voltage can cause the dissipation of stored electric charge. Of course, such defects are removed at the factory by pre-shipment inspection. The programming voltage and pulse width should be always kept within the specified range for the same reason.

# 1.4 EPROM Programmer

The 16K EPROM Programmer stores the program in its internal RAM and writes the program in the EPROM. For this programming, the minimum of 3 functions, the Blank check function prior to programming, the programming function and the Verify function after programming are necessary. As shown in the drawing, there are also programmers provided with a reverse insertion checking function or pin contact checking function prior to the Blank Check. The outline of each block is as follows.

(a) Pin contact check

In the connection test of the ROM pin and the socket, normally checking is performed by detecting the forward current of each EPROM pin. Care is necessary as this forward biased resistance differs according to products of each company.

(b) Reverse insertion check

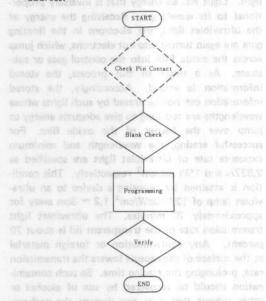
This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.

(c) Blank check

This check is performed prior to programming and checks whether or not it is an erased EPROM or for preventing EPROM reprogramming. Since the output data in the erased condition are "1" (high level), check whether or not data in EPROM are all "1". It willfailstop even when 1 bit of "0" (low level). Normally, it is designed to provide warning with a lamp or buzzer.

(d) Programming

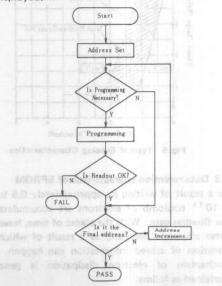
The function of programming the data in the internal RAM of the programmer into EPROM and will fail-stop when programming cannot be made. The normal flow is as shown below. The EPROM data will be read out prior to programming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, read out will be made again and compared with the programming data, and if they coincide, it will progress to the next address.



# (e) Verify

**OHITACHI** 

This function is for checking after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer and it performes fail-stop when it does not coincide. Normally, when it fails, together with lighting of the fail lamp, the address and data are displayed.



(f) How to input the program

There are the following methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and retypewriter input are options.

Method	Content				
Copy input	Input by copying the master ROM.				
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program				
Paper tape input	Read the paper tape furnished from the host system with the tape reader				
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.				

# 1.5 Handling EPROM

When brought in contact with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write marging setting that give a wrong impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges through the eradiation of ultraviolet rays for a short time. It is recommended to execute reprogramming after this eradiation since it reduces the electric charges in the floating gate, too. The basic cluntermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

- Establish a ground for the operator to handle EPROM. Avoid the use of gloves etc. that may develop a static charge.
- (2) Refrain from rubbing the glass window with plastics and other substances that may develop a charge.
- (3) Avoid the use of coolant sprays which contain some ions.
- (4) Use shielding labels (especially those containing conductive substances) that can evenly distribute the established charge.

# 1.6 Shielding label

When using an EPROM in an environment where ultraviolet exposure can occur, it is advisable to put a shielding label on its glass window to absorb ultraviolet light. Specially prepared shielding labels are marketed. Metal-loaded labels are particularly effective. In choosing a shielding label, the following points should be carefully checked.

(1) Adhesiveness (mechanical strength)

Avoid repeated attaching and dusting that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on the old one since peeling may develop a static charge.)

(2) Allowable temperature range

Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may come off easily. When it sticks too fast, the paste may remain on the window glass even after the label has been removed.

(3) Damp-proofness

Use the shielding label in an environment whose humidity falls within the specified allowable humidity range. Today there are few shielding labels that can meet all environmental requirements established for the EPROM. So a suitable one must be chosen for each specific application.

(a) A set of the se

 with press match institution of the environment of the institution of the belifterings as drawning instrument environe & the Princetille as a second of the Princetille as a second of the environe & the Princetille as a second of the Princetille as a second of the environe & the Princetille as a second of the Princetille as a second of the environe & the Princetille as a second of the Princetille as a second of the environe & the Princetille as a second of the environe & the Princetille as a second of the Prin



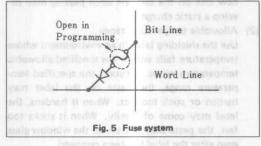
Programming & Erasing of PROMs-

# 2. PROGRAMMING OF BIPOLAR PROMS

## 2.1 Programming System

The storing system of the Bipolar PROM can be generally classified into 2 systems; the Blown diode system and fuse system.

The latter is a system in which the metal-made fuse is burned off by current (Fig. 5). In the former, Emitter-Base junction is short-circuited by AI, which has penetrated into Base because of current



### 2.2 Programming Method

Programming is executed by the conventional programming equipment (PROM writer) using a board suited to the product.

First, check if all bits are programmable (Blank check), next write the pattern you want to program one by one bit. At every application of current pulse, confirm that program is available by sensing output level. And when programming has been completed, apply additional pulse. This process should be performed for all bits into which you want to write, and as you have completed programming, check (Verify) if you have programmed in the same pattern as you intended. If you do not find any mistake, programming has been completed.

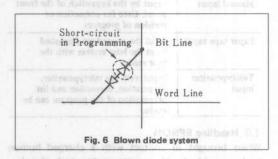
For Blank check, Sense and Verify whether output pin level is high (non-programmed) or low (programmed) is checked by sense current (Is). Vs - Ischaracteristic of normal series and S series is shown in Fig. 8 and 9, respectively. Specified value of sense current (Is) of both normal series and S series is 20 mA, and voltage reference level is 7.5 V.

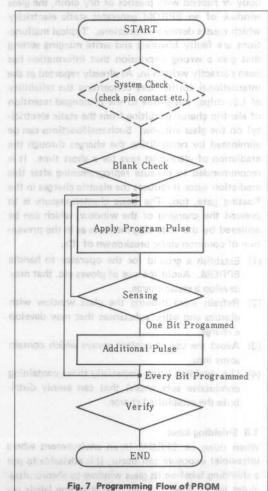
Fig. 10 and 11 show the relation between program current and program pulse number necessary for 1 bit to be written. With consideration of its influence on breakdown voltage, program current is specified as 130 mA in normal series and as 90 mA in S series.

**OHITACHI** 

### unational at a tridui da Masik

pulse applied to E-B junction (Fig. 6). Generally, the blown diode type is considered to be more reliable. A grow back phenomenon, that is, migration and recombination of the metal, is seen in fuse system. HITACHI devices use the blowin diode system.





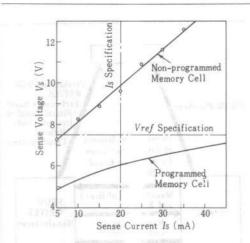


Fig. 8 Vs - Is Characteristic of Normal Series (HN25089)

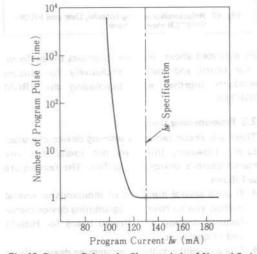


Fig. 10 Program Pulse – Iw Characteristic of Normal Series (HN25089)

2.3 Programming Characteristics of Hitachi Bipolar PROM

Small program current

130 mA for normal series, and 90 mA for S series are required for programming. Therefore, there are few bad effects caused by breakdown voltage degradation and parasitic effects.

Fast programming speed

As seen in Fig. 10 and 11, program pulse for 1 bit memory cell can be mostly written at one time Consequently, the program time per device is quite short. In case of 8K bit, for example, only 2 or 3 seconds at an average are required.

High programming yield

Unlike the MOS PROM, the Bipolar PROM cannot be rewritten, once it is written into the memory

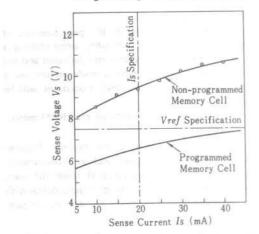


Fig. 9 Vs - Is Characteristic of S Series (HN25169S)

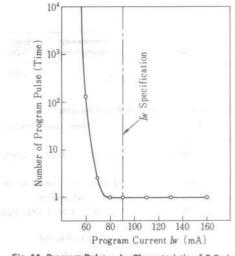


Fig. 11 Program Pulse – Iw Characteristic of S Series (HN25169S)

# cell.

Therefore, it does not allow programming and inspection of the product prior to delivery. Due to this, sometimes a defective product (which does not allow programming) might be delivered.

Generally, the programming efficiency percentage is 90~95% when programming is performed on the user's side. Special tests such as actually performing programming on the dummy cell in the chip, performing continuity test of all memory cells, etc., are made prior to delivery for minimizing the possibility to deliver defective products.



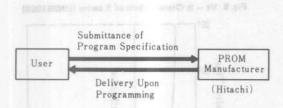
### Programming & Erasing of PROMs

# 2.4 Programming

There are two methods in the programming of PROM. That is, the method when programming is made by PROM manufacturer and delivered and the method when programming is made on the user's side. Both these methods and procedures will be explained below.

# 2.4.1 Programming performed by the PROM manufacturer

As shown in the drawing below, the manufacturer receives the program specification (specification designating the program pattern) from the user, performs writing (Programming) in accordance with the specification and performs delivery. In this case, a special writing fee is charged.



# 2.4.2 Programming performed by user

In this case, the following three items must be prepared by the user.

1 PROM WRITER (Main unit of programming equipment)

One capable of being used in common with equivalent products of other companies,

2 Performance board (Exclusive board designated by each manufacturer)

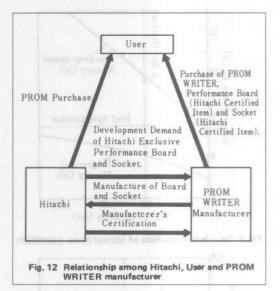
Minimum of 1 board for Hitachi PROM.

3 Sockets (sockets suited to product) Minimum of one socket per product. These sockets are purchased from the PROM WRITER manufacturer.

The relationship among PROM WRITER manufacturer, Hitachi and user is shown in Fig. 12.

at prior to delivery Due to prior to delivery Due to product (which does in be delivered.

Hing off clency percentage is name is perfectual on the such as seturally performing during cell in the chip, during cell in the chip, and of all memory cells, arc, inferty for minimizing the crive produces.



As indicated above, the user purchases the performance board and sockets exclusively for Hitachi products together with purchasing the PROM WRITER.

# 2.5 Programming Device

There are about ten programming device manufacturers. However, this does not mean that any manufacturer's device will suffice. The reasons are as follows.

- It costs several hundreds of thousands or several million yen to have a programming device manufacturer develop a dedicated board for Hitachi and to qualify it.
- The suitability of the programming device affects the programming efficiency. Therefore, it should be a device of a reliable manufacturer.
- The servicing setup for handling troubles should be consolidated. The setup should be one that judgement can be accurately made on whether it is a writing device trouble or PROM trouble.

Hitachi has prepared a list of recommended manufacturers which meet the above requirements. Please contact our sales engineering staff for information in this regard.

As even in Frig. 10 and 11, mogram obler for 1 bit memory cell can 14 mostly writeen as one time Consequently, the reogram time plat device is quite short, in cast of IN, bit, for exemple, only 2 or 3 mecond at an even to an required.

service MODE to MOV de Bipole ADD without the motion



# MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into the mask ROM is performed by the CAD system using a large-sized computer. You should submit the data of the ROM code in conformity with the specification explained below by either paper tape, EPROM or magnetic tape. In addition, enter your instructions such as the chip select, customer part number, etc., in the "ROM Specification Identification Sheet" and attach it to the ROM code data.

# 1. Overall Specification

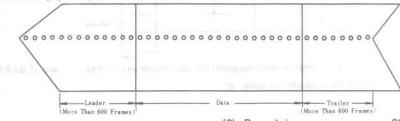
Since the submitted paper tape, card or magnetic

tape is fed into the large-size computer as it is, observe the following specifications.

# 1.1 Specification of Paper Tape

1.1.1 Any color paper tape may be used as long as it is a marketed 1 inch wide paper tape for computers. However, a black color paper tape is recommended.

1.1.2 Take more than 600 frames for the leader and trailer.



# 1.1.3 Parity mode

The presence and type of parity are clearly described in the "ROM Specification Identification Sheet".

There are following modes in the parity system.

(1)	With parity	
	Even parity	 EVEN
	Odd parity	 ODD

(2) Without parity

1.1.4 Use the 8 unit ASC11 code as the code.

# 1.2 Specification of Magnetic Tape

1.2.1 Use the following type of magnetic tape which can be netered in a magnetic tape device which is compatible with the IBM magnetic tape device.

- (1) Length .... 2,400 feet, 1,200 feet or 600 ffet
- (2) Width ...... 1/2 inch
- - ly state which it is in the "ROM Specification Indentification Sheet".)

1.2.2 Use the EBCDIC code as the use code.

1.2.3 Make the format of the magnetic tape as described below.

- (1) No leading tape mark
- (2) No label

- (3) Record size ...... 80 byte/1 record
- (4) Block size ..... 10 records/1 block
- (5) The end of the file should be indicated by 2 successive tape marks (TM).

1.2.4 Ensure that the magnetic tape becomes of 1 roll for each chip. Since extending the single-chip portion over several rools is impermissible, submit by compiling into the single-chip portion for each roll.

# 2. Data Mode

# 2.1 HMC\$6800 Load Module Mode

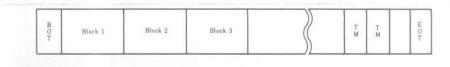
This mode is the object mode output from the assembler of HMCS6800.

2.1.1 Divide the 8 bit code into the upper and lower 4 bit codes and convert each into hexadecimal notation.

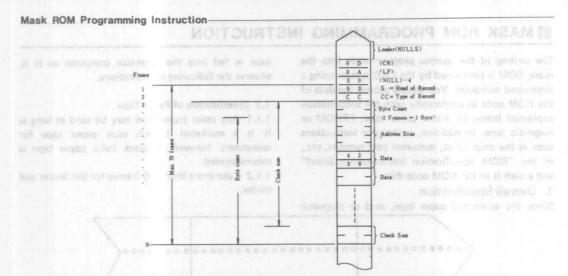
(Example) The code of 1100 0110 becomes as follows under binary notation.

(Upper 4 bits)	(Lower 4 bits)	Bit weight
D, D, D, D, D,	D, D, D, D, D,	(ROM output
1 1 0 0	0 1 1 0	equivalence)

2.1.2 The composition of the load module mode is shown below by taking the case of paper tape as the example. The numbers written in the tape are ASCII code hexadecimal numbers of the data.



C HITACHI



(Note) The check sum is a technique which disregards the complement on one of each bit sum of the 8 bits.

S

0

0 6

0000

48-H

44-D

52-R

1B (Check Su

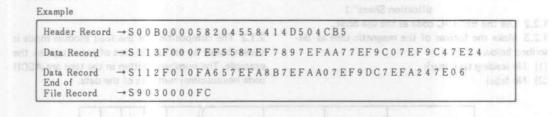
# 2.1.3 The actual load module mode becomes as shown below.

CC=30 Header record S vel betrouble Frame 1 Record Start 5 3 Record Type 3 0 3 0 Byte Count girlo-elonis edt points 3 6 3 0 findue eldisimus Address Size of the portion for each 3 0 3 0 3 4 3 8 Data 10 3 4 Data 3 4 3 5 3 2 Data 3 1 Check Sum 4 2

CC=1			= 39		
Data record		End	of record		
5 3	S	5	3	S	
3 1	1	3	9	9	
$\begin{array}{ccc} 3 & 1 \\ 3 & 6 \end{array}$	16		0 3	03	
3 1 3 1 3 0 3 0	1100	3 3 3 3	0 0 0	0000	
3 9 3 8	98	4	6 3	FC (Che Su	m }
3 0 3 2	0 2				
~					
4 1 3 8	Að (Check	Sum )			

S0 indicates the head of the file and S9 indicates the end of the file. The actual data enters following S1. It means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by

counting in increments of 1 byte of the data and checking whether it is sequential or not. In places where the address is skipped, the data of 00 or FF enters hexadecimally. The printed example of the paper tape of the HMCS6800 load module mode is as shown below.



2.1.4 The ROM code data are capable of handling the following 4 types of cases. A header recorder is required in front of the data recorder and an end of file recorder at the back of the data recorder.

 Case when the data reaches full capacity of ROM

The ROM recorder for 1 chip enters into the data recorder. Since the address of the address size of the



data recorder counts the data and checks whether or not it is in a sequential address, it becomes necessary that the address not be skipped. The ROM head address column of the "ROM Specification Identification Sheet" becomes 0.

(2) Case when data is input from en route of ROM



In this case, perform entry by decimal notation in the ROM head address column of the "ROM Specification Identification Sheet" on which ROM address you wish to input the data. The data 00 or FF will enter into the blank address by hexadecimal notation. (3) Case when data is input by skipping intermediate address



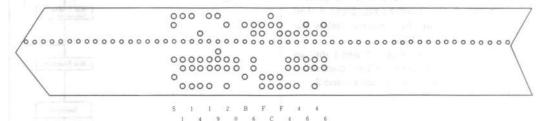
The address of the address size of the data recorder is counted in increments of 1 byte of the data, compared with the next address of the data recorder and checked whether or not it is sequential. The data 00 automatically enters by hexadecimal notation into the ROM code of the skipped address. Therefore, the writing of data as in the following drawing is also possible. In this case, perform entry into the "ROM Specification Identification Sheet" that the ROM head address enters from 0 address for data I and from which address it enters for data 11.

(4) Case when the data is less than the full capacity of ROM



In case the data volume is less than the total byte capacity of ROM LSI when the end of file recorder appears, it becomes written as the ROM code as shown in the following drawing.

(Example) Indicates the example of the paper tape when the data recorder is S1141920B6-FC ...



B

N

# 2.2 BNPF Mode

2.2.1 One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.

2.2.2 The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.

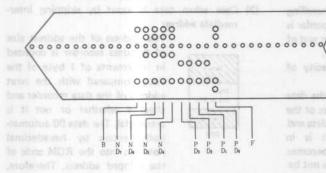
(Example) The code of OF by hexadecimal notation is symbolized as shown below (in case of paper tape)

2.2.3 It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specifica-

tion Identification Sheet" always becomes 0.

Indicates start of 1 word. Indicates "0" of 1 bit data. Indicates "1" of 1 bit data. Indicates end or 1 word.



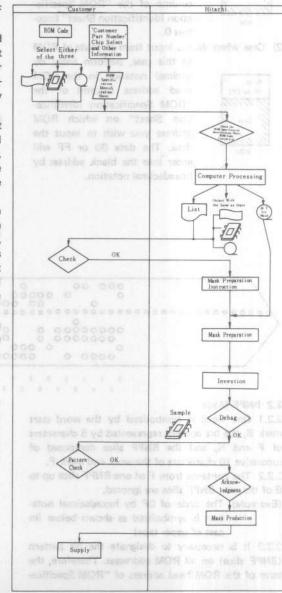


- Note 1) Sometimes X is used besides P and N in the display of the word content by the BNPF slice.
  - X means that the user is not concerned whether the bit is P or N. However, since it is necessary to decide the P or N for performing tests, Hitachi performs selection of P or N. The results are informed by making entry in the identification table.
- Note 2) The contents of the BNPF slice are not only those with the continuation of PN and the form of B\*nF can also be used. This means that the content of the slice existing just prior to this word will be repeated for n words from this word.

For example, when B\*4F exists at the 10th word, it means that the content of the 9th word will be repeated in the 10th, 11th, 12th and 13th words. (However, it does not necessarily follow that the X content of Note 1 above will be repeated.) n shall start from 1 and be a number below the total addresses of ROM.

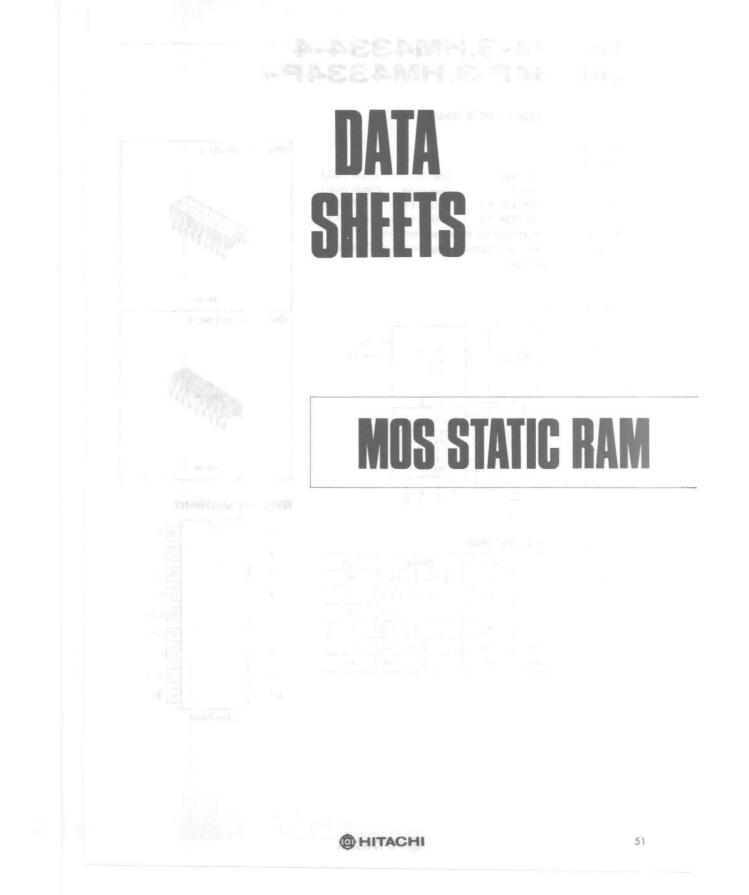
Note 3) When a certain block is not used (when an unused ROM address exists), disposition

# Mask ROM Development Flowchart



can be made by utilizing Notes 1 and 2.

**OHITACHI** 



# HM4334-3, HM4334-4 HM4334P-3, HM4334P-4

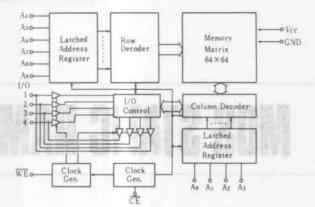
1024-word×4-bit Static CMOS RAM

# FEATURES

Single 5V Supp	bly		
Low Power Sta	andby and	Standby:	10μW (typ.)
Low Power Op	eration;	Operation:	20mW (typ.)
Access Time;	HM4334/P-3:	300 ns (max.)	(5V±5%)
	HM4334/P-4:	450 ns (max.)	(5V±10%)

- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

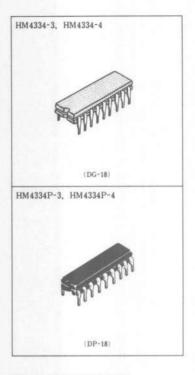
# BLOCK DIAGRAM



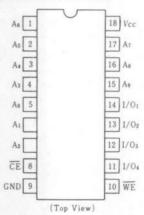
# BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin*	$V_7$	-0.3 to Vcc +0.5	V
Power Supply Voltage*	Vcc	-0.3 to +7.0	v
Power Dissipation	$P_{T}$	1.0	W
Operating Temperature	Tape	0 to +70	°C
Storage Temperature (Plastic)	Tete	-55 to +125	°C
Storage Temperature (Cerdip)	Tele	-65 to +150	°C

\* with respect to GND



# PIN ARRANGEMENT



Item	Symbol		HM4334/P-3			HM 4334 /P -4			
	Symbol	min	typ	max	min	typ	max	Unit	
	Vcc	4.75	5.0	5.25	4.5	5.0	5.5	V	
Supply Voltage	GND	0	0	0	0	0	0	V	
	VIII	2.4	-	Vcc+0.5	2.4	-	Vcc+0.5	V	
Input Voltage	VIL	-0.3	70,9410	0.8	-0.3	-	0.8	V	

# RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

# DC AND OPERATING CHARACTERISTICS

 $(T_a=0 \text{ to } +70^{\circ}\text{C}, \text{ GND}=0\text{V}, \text{HM}4334/\text{P}-3: V_{cc}=5\text{V}\pm5\%, \text{HM}4334/\text{P}-4: V_{cc}=5\text{V}\pm10\%)$ 

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$I_{LI}$	V <sub>IN</sub> =0 to V <sub>cc</sub>	-1.0	-	+1.0	μA
Output Leakage Current	$I_{L0}$	$\overline{CE} = V_{IH}, V_{ext} = 0$ to $V_{CC}$	-1.0	-	+1.0	μΑ
	Icci	$CE = 0V, V_{IN} = V_{CC}, I_{I \ge 0} = 0$	-	-	1.0	mA
Operating Power Supply Current	Iccz	$\overline{CE}=0.8V, V_{IN}=2.4V, I_{I < 0}=0$		2.5	5.0	mA
Average Operating Current	Icca	V <sub>IN</sub> =0 or V <sub>cc</sub> , f=1MHz, duty 50%, I <sub>1/0</sub> =0	-	4	7	mA
Standby Power Supply Current	Iccl	$CE \ge V_{cc} - 0.2V$		2	100	μΑ
-	Vol	$I_{oL} = 2.0 \text{mA}$		-	0.4	V
Output Voltage	Von	$I_{OH} = -1.0 \mathrm{mA}$	2.4		-	V

# **CAPACITANCE** $(Ta - 25^{\circ}C, f - 1MHz)$

Item	Symbol	Test Condition	min	typ	max	Unit
I/O Terminal Capacitance	Ciro	$V_{L>0} \rightarrow 0$ V	1-1	7	10	pF
Input Capacitance	<i>C</i> <sub><i>i</i></sub> ,	V.,=0V	-	3	5	pF

# AC CHARACTERISTICS

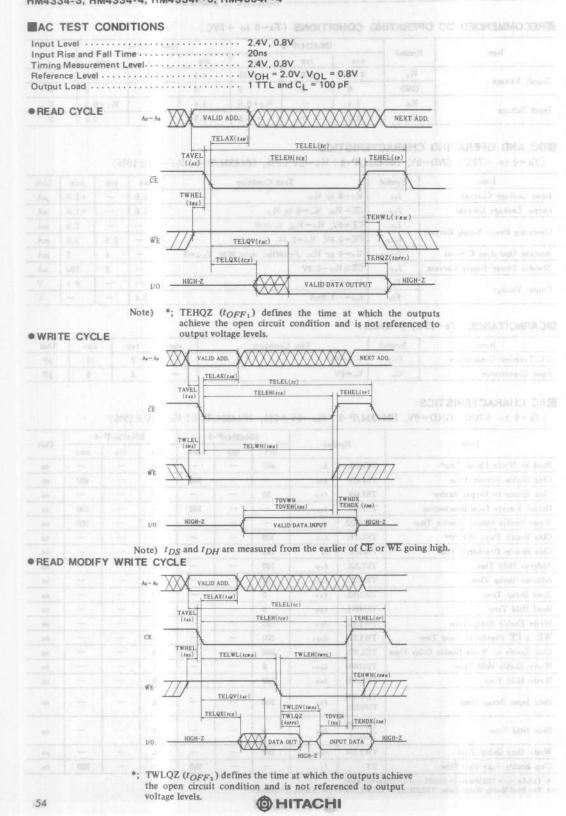
 $(T_a=0 \text{ to } +70^{\circ}\text{C}, \text{ GND}=0\text{V}, \text{ HM}4334/\text{P}-3 : V_{cc}=5\text{V}\pm5\%, \text{ HM}4334/\text{P}-4 : V_{cc}=5\text{V}\pm10\%)$ 

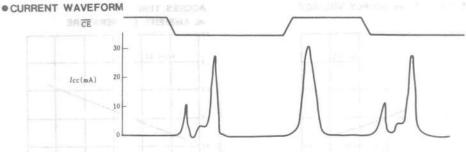
The second se	Symbol		HM 4334/P-3			HM 4334/P-4			Unit
Item	Syr	nbol	min	typ	max	min	typ	max	Uni
Read or Write Cycle Time*	TELEL.	tc	460	-	/	640	-	-	ns
Chip.Enable Access Time	TELQV	tAC			300	-		450	ns
Chip Enable to Output Active	TELQX	lcx	50	-		50	. <del></del>		ns
Output 3-state from Deselection	TEHQZ	torra	-	-	100			100	ns
Write Enable Output Disable Time	TWLQZ	toFFI		-	100			100	ns
Chip Enable Pulse Width**	TELEH	tcz	300	1-		450		-	ns
Chip Enable Precharge Time	TEHEL	t <sub>P</sub>	120	n ne <u></u> e - 1	—	150	-	-	ns
Address Hold Time	TELAX	t <sub>A H</sub>	100	-	- 3	100	-	-	ns
Address Setup Time	TAVEL	tAS	20	7-1	10-0	20	-		ns
Read Setup Time	TWHEL	LRS	0	-		0	-		ns
Read Hold Time	TEHWL	t <sub>RH</sub>	0		-	0	-	-	ns
Write Enable Setup Time	TWLEL	tws	-20	-		-20	-	-	ns
WE to CE Precharge Lead Time	TWLEH	IWPL	300	:=	1-	450			ns
Chip Enable to Write Enable Delay Time	TELWL	Lcwp	300	a training	-	450	-	-	ns
Write Enable Hold Time	TEHWH	t <sub>EWH</sub>	0	-		0	-		ns
Write Hold Time	TELWH	t wH	300		-	450	1. 1.	-	ns
Data Input Setup Time	TDVWH TDVEH	tos	200	22		350	-		ns
Data Hold Time	TWHDX TEHDX	ton	0		-	0	-		ns
Write Data Delay Time	TWLDV	twos	100	- 10	-	100	-	-	ns
Chip Enable Rise/Fall Time	TT	1.		-	300	-	-	300	ns

TELEL(t<sub>c</sub>) = TELEH(t<sub>ct</sub>) + TEHEL(t<sub>F</sub>) + t, (20ns) + t<sub>f</sub>(20ns) \*\* For Read Modify Write Cycle. TELEH(tcr) = TELWL(tcwp) + TWLEH(twpt) + t<sub>j</sub>(20ns)



# HM4334-3, HM4334-4, HM4334P-3, HM4334P-4





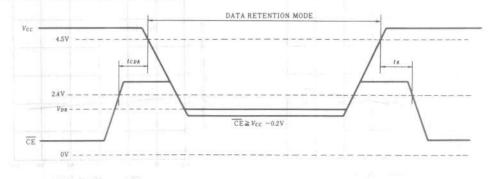
[NOTE]  $V_{CC} = 5.0V, T_a = 25^{\circ}C$ 

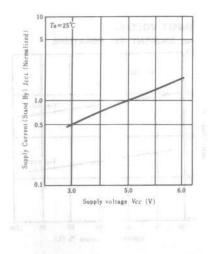
# **LOW Vcc DATA RETENTION CHARACTERISTICS** (Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{CE} \ge V_{cc} - 0.2V$	2.0	—	-	V
Data Retention Power Supply Current	ICCDR	$V_{DR} = 3.0 V$	-	0.5	50	μΑ
Chip Deselection to Data Retention Time	t <sub>CDR</sub>		0	-		ns
Operation Recovery Time	t <sub>R</sub>		trc*	-		ns

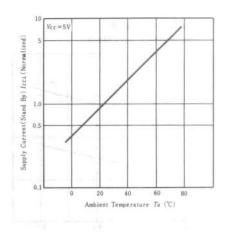
\* tsc-Read Cycle Time BRU (ARP) (148-1834) av

# . LOW Vcc DATA RETENTION TIMING





SUPPLY CURRENT VS. SUPPLY VOLTAGE SUPPLY CURRENT VS. AMBIENT TEMPERATURE



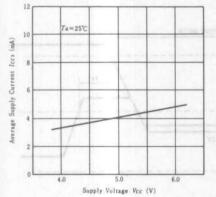
**OHITACHI** 

# HM4334-3, HM4334-4, HM4334P-3, HM4334P-4-

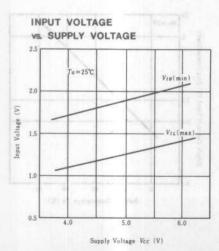
# ACCESS TIME vs. SUPPLY VOLTAGE

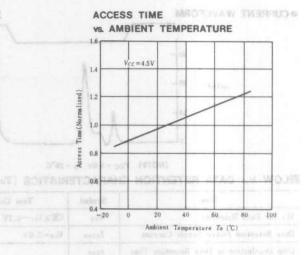




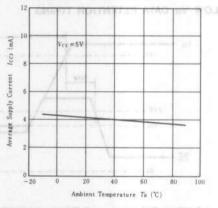


SUPPLY CURRENT AMERICAT TREMPERATURE

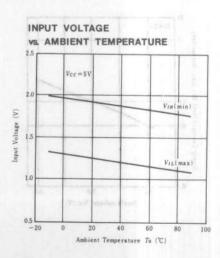




AVERAGE SUPPLY CURRENT







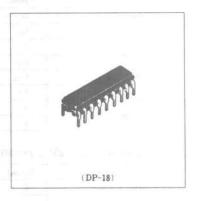
**HITACHI** 

# HM4334P-3L,HM4334P-4L

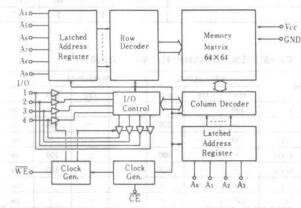
1024-word×4-bit Static CMOS RAM

# FEATURES

- Single 5V Supply
- Low Power Standby and Standby: 10μW (typ.) Low Power Operation; Operation: 20mW (typ.)
   Fast Access Time; HM4334P-3L: 300 ns (max.) (5V±5%) HM4334P-4L: 450 ns (max.) (5V±10%)
- HM4334P-4L: 450 ns (max.) • Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register







# **MABSOLUTE MAXIMUM RATINGS**

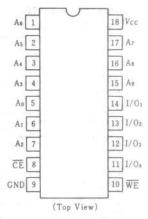
Item	Symbol	Rating	Unit
Voltage On Any Pin*	V <sub>7</sub>	-0.3 to Vcc+0.5	V
Power Supply Voltage*	Vcc	-0.3 to +7.0	V
Power Dissipation	Ρτ	1.0	W
Operating Temperature	Tepr	0 to +70	"C
Storage Temperature	Tris	-55 to +125	°C

\* with respect to GND

# **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to $+70^{\circ}$ C)

Item	Symbol						4 L.	Unit
Symbol	min	typ	max	min	typ	max	Unit	
6 31 V. 198	Vcc	4.75	5.0	5.25	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	0	0	0	V
r	VIN	2.4		Vcc+0.5	2.4	str13	Vcc+0.5	V
Input Voltage	V <sub>IL</sub>	-0.3		0.8	-0.3	-	0.8	V

# PIN ARRANGEMENT



HM4334P-3L, HM4334P-4L-

# DC AND OPERATING CHARACTERISTICS

(Ta=0 to +70°C, GND=0V, HM4334P-3L: Vcc=5V±5%, HM4334P-4L: Vcc=5V±10%)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	ILI	V <sub>IN</sub> =0 to V <sub>cc</sub>	-1.0		+1.0	μA
Output Leakage Current	ILO	$\overline{CE} = V_{lik}, V_{est} = 0$ to $V_{cc}$ =		violad	+1.0	μA
Operating Power Supply Current	Icci	$CE=0V, V_{IS}=V_{cc}, I_{I\times o}=0$	bost	Strad	1.0	mA
Operating Power Supply Current	Icci	CE-0.8V, VIN-2.4V, II-0-0	((10))	2.5	5.0	mA
Average Operating Current	Ices	$V_{lN} = 0$ or $V_{cc}$ , $f = 1$ MHz, duty 50%, $I_{lco} = 0$	Mis-	- 41	7	mA
Standby Power Supply Current	Iccl	CE≥Vcc−0.2V	-+0.54	2	20	μA
0	Vol	IoL=2.0mA antiquo bne atogni IA	oldis—a	102.1	0.4	V
Output Voltage	Von	Inn1.0mA 100 Helenmil price hoped	2.4	11.7814	0.0000	V

CAMP. E-9ACCAN

# **CAPACITANCE** (*Ta*=25°C, *f*=1MHz)

Item	Symbol	Test Condition	min	typ	max	Unit
1/O Terminal Capacitance	Ciro	V1>0-0V	-	7	10	pF
Input Capacitance	C.,	V <sub>in</sub> =0V	7. (=	3	5	pF

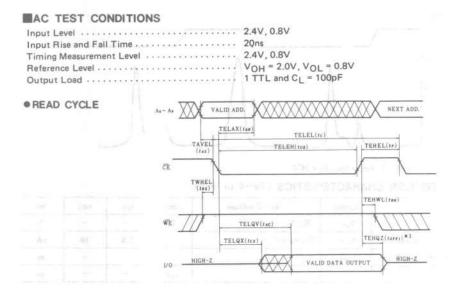
# **AC CHARACTERISTICS**

(Ta=0 to +70°C, GND=0V, HM4334P-3L: Vcc=5V±5%, HM4334P-4L: Vcc=5V±10%)

- AA	0			HM4334P-3L			M4334P-	4L	Unit
Item	Sym	ibol	min	typ	max	min	typ	max	Unst
Read or Write Cycle Time*	TELEL	te	460	-		640	-	1-2-1	ns
Chip Enable Access Time	TELQV	tAC	-	-	300			450	ns
Chip Enable to Output Active	TELQX	tex	50	and the		50	$\sim \sim$		ns
Output 3-state from Deselection	TEHQZ	lorri		11 3 12 -	100	-	-	100	ns
Write Enable Output Disable Time	TWLQZ	torri	-	-	100	A		100	ns
Chip Enable Pulse Width**	TELEH	ter	300	D-sh		450		1	ns
Chip Enable Precharge Time	TEHEL	t <sub>P</sub>	120	-	-	150	-		ns
Address Hold Time	TELAX	t <sub>AH</sub>	100	-	-	100	-		ns
Address Setup Time	TAVEL	tas	20	-	8.67741	20	01244	111	ns
Read Setup Time	TWHEL	tas	0	-	luces of	0	- 1	- 12.00	ns
Read Hold Time	TEHWL	t <sub>RH</sub>	0	1 1	-	0		-	ns
Write Enable Setup Time	TWLEL	tws	-20		-	-20	-	-	ns
WE to CE Precharge Lead Time	TWLEH	twpL	300	-		450		-	ns
Chip Enable to Write Enable Delay Time	TELWL	tewp	300	-		450		-	ns
Write Enable Hold Time	TEHWH	t <sub>EWH</sub>	0	-		0	1010 F	-	ns
Write Hold Time	TELWH	twn	300			450		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ns
Data Input Setup Time	TDVWH TDVEH	tos	200		CUATTA	350	-		ns
Data Hold Time	TWHDX TEHDX	IDH D	0	-	F.	0	-		ns
Write Data Delay Time	TWLDV	lwps	100			100	-	-	ns
Chip Enable Rise/Fall Time	TT	tT	2.0	22.0	300	<u>1</u> W.	-	300	ns

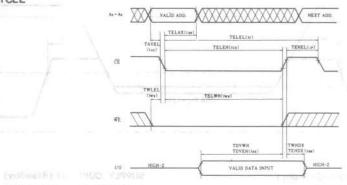
\* TELEL( $t_c$ ) = TELEH( $t_{c_E}$ ) + TEHEL( $t_P$ ) +  $t_r$ (20ns) +  $t_f$ (20ns)

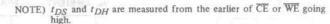
\*\* For Read Modify Write Cycle, TELEH(tcz)=TELWL(tcwp)+TWLEH(twrL)+t/(20ns)



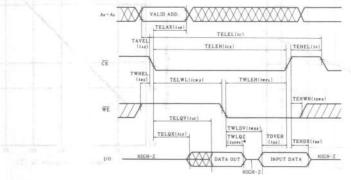
NOTE) \*: TEHQZ (t<sub>OFF1</sub>) defines the time at which the outputs achieve the open circuit condition and is not referenced to outputs voltage level.



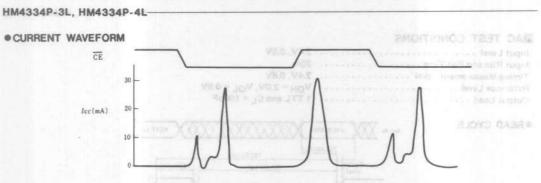








NOTE) \*: TWLQZ (t<sub>OFF2</sub>) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.



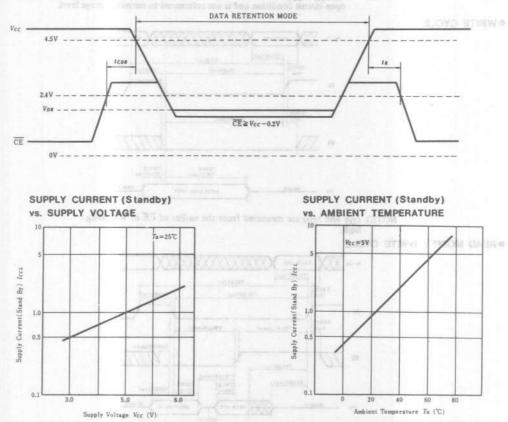
[NOTE] VCC = 5.0V, Ta = 25°C

# **ILOW Vcc DATA RETENTION CHARACTERISTICS** (Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{CE} \ge V_{cc} - 0.2V$	2.0	-	-	V
Data Retention Power Supply Current	ICCDR	V <sub>DR</sub> =3.0V	-	0.5	10	μA
Chip Deselection to Data Retention Time	lcor	in total in	0	-	-	ns
Operation Recovery Time	t <sub>R</sub>	1 11/00/	l RC*	-	-	ns

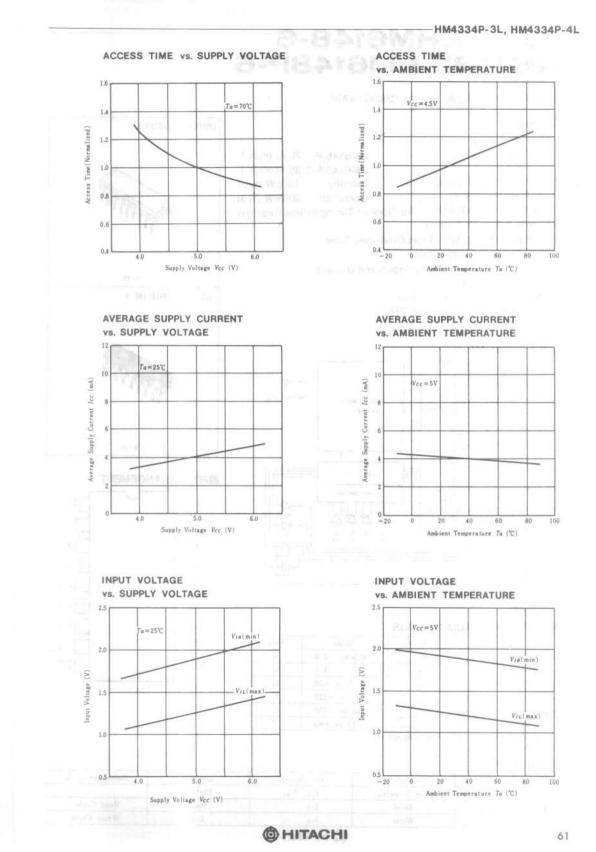
\* Isc-Read Cycle Time

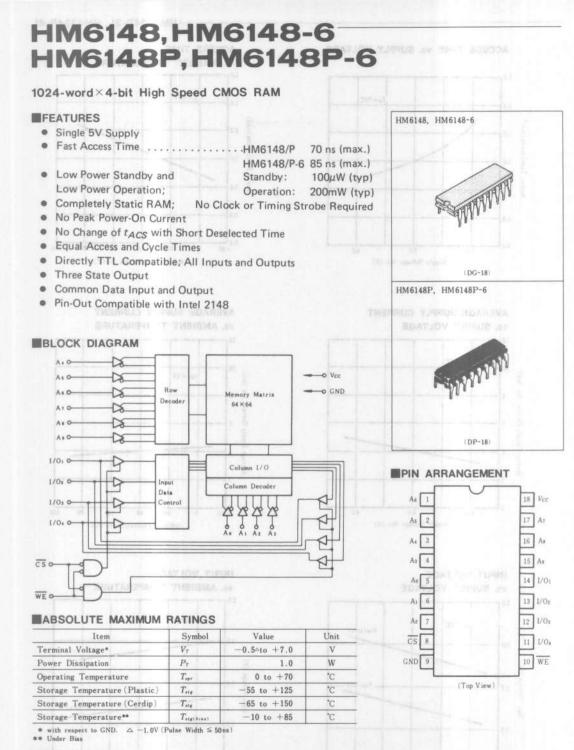
OLOW Vcc DATA RETENTION TIMING



(i) Figure (1997) (Copp.) defines the data at which the other are achieved in order change conditions and is not achieved to every coloring tracks.

**OHITACHI** 





# TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not Selected	IsB, IsBI	High Z	
L	Н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc	Din	Write Cycle

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
	VIH	2.4	3.5	6.0	V
Input Voltage	VIL	-0.3*		0.8	V

\*  $V_{lL}$  min = -1.0V (Pulse width  $\leq$  50ns)

# **DC AND OPERATING CHARACTERISTICS** (Vcc-5V±10%, GND-0V, Ta-0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5 V$ , $V_{is} = GND$ to $V_{cc}$		-	2.0	μA
Output Leakage Current	ILO	$\overline{CS} = V_{IH}$ , $V_{I/0} = GND$ to $V_{CC}$	-	-	2.0	μA
Orana in Real Connect	Icc	$\overline{\mathrm{CS}} = V_{lL}, \ I_{l \neq 0} = 0 \mathrm{mA}$	-	35	80	mA
Operating Power Supply Current -	Icci	$\overline{\text{CS}} = V_{IL}$ , Minimum Cycle, Duty = 100%, $I_{I > 0} = 0$ mA	-	40	80	mA
Average Operating Current	Icci**	Cycle=150ns, Duty=50%, I <sub>1/0</sub> =0mA		35	-	mA
C. II. D. C. I. C	Iso	$\overline{CS} = V_{IH}$	-	5	12	mA
Standby Power Supply Current	1381	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \ V_{i*} \le 0.2 \text{V} \text{ or } V_{i*} \ge V_{cc} - 0.2 \text{V}$	1000	20	800	μA
0	V <sub>o L</sub>	IoL=8mA	-	-	0.4	V
Output Voltage	V <sub>OH</sub>	$I_{OH} = -3.2 \mathrm{mA}$	2.4	-	-	V

Notes) \* Typical limits are at Voc=5.0V, Ta=25°C and specified loading. \*\* Reference only.

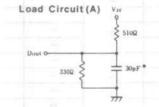
# **CAPACITANCE** (*Ta*=25°C, *f*=1MHz)

Item	C		min	max	Unit
Input Capacitance	C.,	V0V		5	pF
Input/Output Capacitance	$C_{I \times Q}$	V <sub>I × 0</sub> = 0V		12	pF

Note) This parameter is sampled and not 100% tested.

# **AC CHARACTERISTICS** (Vcc=5V±10%, Ta=0 to +70°C, unless otherwise noted) AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1





Vec

TT

₹5100

5pF

Load Circuit (B)

Fig. 1

\* includes probe and

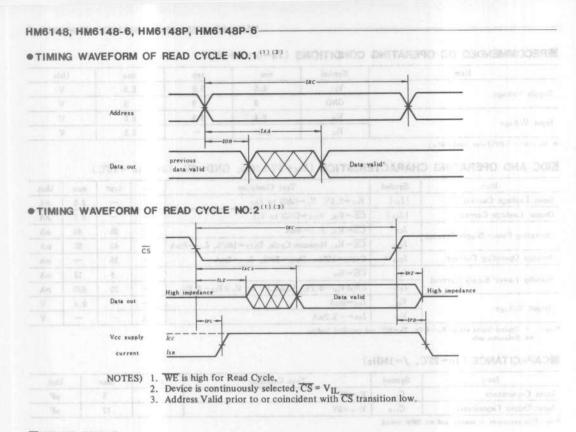
jig capacitance

# READ CYCLE

Parameter	Symbol	HM6	HM6148/P		HM6148/P-6	
	Symbol	min	max	min	max	Unit
Read Cycle Time	tRC	70	-	85	-	ns
Address Access Time	tax	-	70		85	ns
Chip Select Access Time	lacs	_	70	-	85	ns
Output Hold from Address Change	t on	5	-	5		ns
Chip Selection to Output in Low Z*	tLz	10	—	10	-	ns
Chip Deselection to Output in High Z*	1 <sub>HZ</sub>	0	40	0	40	ns
Chip Selection to Power Up Time	tru	0	1	0		ns
Chip Deselection to Power Down Time	tpp		40		40	ns

\* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.





# WRITE CYCLE

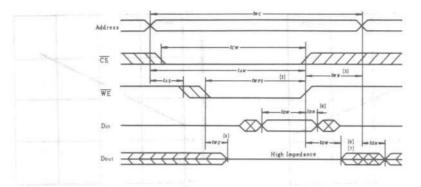
Parameter	Symbol	HM6	148/P	HM61	HM6148/P-6	
rarameter	Symbol	min	max	min	max	Unit
Write Cycle Time	twc	70		85	$-10 \div 104$	ns
Chip Selection to End of Write	tcw	50	• • • • • • • • • • • • • •	60	Parent Table	ns
Address Valid to End of Write	taw	65	-	80	-	ns
Address Setup Time	tas	15	-	15	01/01/ <u>0</u> /040	ns
W . D . Wills	twpi	50	-	60	-	ns
Write Pulse Width*	twp2	65	-	80	-	ns
Write Recovery Time	twa	5	-	5	-	ns
Data Valid to End of Write	tow	30	-	35	S 10.12	ns
Data Hold Time	t <sub>DH</sub>	5	-	5	-	ns
Write Enabled to Output in High Z**	twz	0	35	0	45	ns
Output Active from End of Write**	tow	0	-	0	- 3.73	ns

Notes) \* When the CS low transition occurs simultaneously with the WE low transition or after the WE transition. 1/O pins remain in a high impedance state. In this case twre, in the other case twre(-twrettaw).

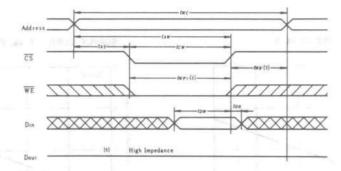
\*\* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.



● TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE CONTROLLED) (1)



• TIMING WAVEFORM OF WRITE CYCLE NO.2(CS CONTROLLED) (1)



Notes)

 CS and WE are paced in the WRITE state during low level period (t<sub>W</sub>).

2. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ .  $(t_{WP})$ 

 t<sub>WR</sub> is measured from the earlier of CS or WE going high to the end of write cycle.

During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

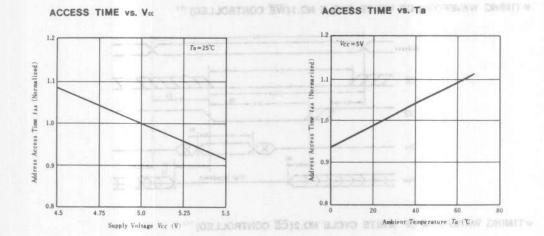
 If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain in a high impedance state.

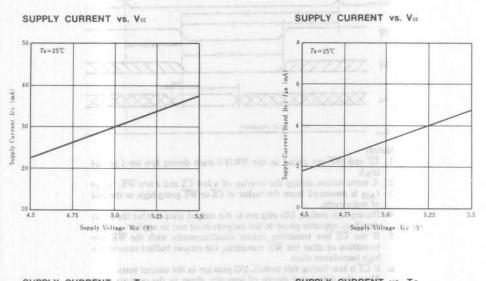
6. If CS is low during this period, I/O pins are in the output state.

Then the data input signals of opposite phase to the outputs must not be applied to them.

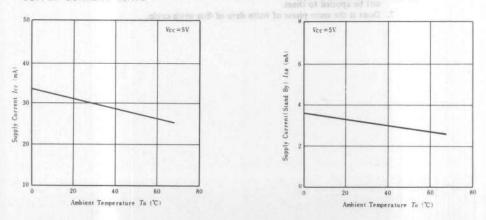
7. Dout is the same phase of write data of this write cycle.



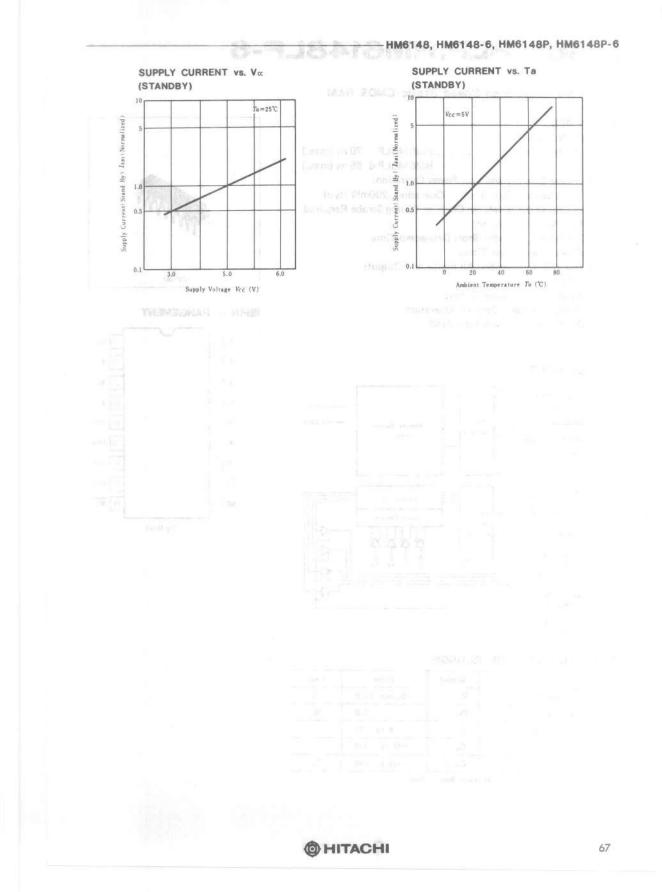












# HM6148LP, HM6148LP-6

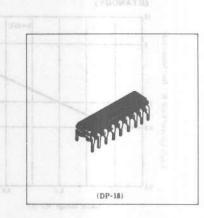
1024-word×4-bit High Speed Static CMOS RAM

# **FEATURES**

- Single 5V Supply
- Low Power Standby and Low Power Operation;

Standby: 5µW (typ) Operation: 200mW (typ)

- · Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t<sub>ACS</sub> with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Capability of Battery Back Up Operation
- Pin-Out Compatible with Intel 2148



# PIN ARRANGEMENT

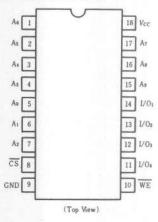
### BLOCK DIAGRAM A . 0-DX. -O Vec As O De Row A.O. De. - O GND Memory Matrix Decoder 64×64 X AT O Da As O D A . 0 1/0,0 Column 1,10 1/0: 0 D Input Column Decuder Data 1/01 0-5 Control 1/0.0 CS O WE O

# BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	$V_{\tau}$	-0.5≏to +7.0	v
Power Dissipation	PT	1.0	W
Operating Temperature	Terr	0 to +70	°C
Storage Temperature	Tere	-55 to +125	°C
Storage Temperature**	Tele (bias)	-10 to +85	°C

\* with respect to GND.  $\triangle -1.0V$  (Pulse Width  $\leq 50$  ns)

\*\* Under Bias



# TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not Selected	IsB, IsBi	High Z	
L	Н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc	Din	Write Cycle

# **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

Item	Syn	ibol min	typ	max	Unit
Supply Voltage	Vc	c 4.5	5.0	5.5	V
	GN	1D 0	0	0	V
	VII	2.4	3.5	6.0	V
Input Voltage	VI	-0.3*		0.8	V

\*  $V_{lL}$  min = -1.0V (Pulse width  $\leq$  50ns)

# **DC AND OPERATING CHARACTERISTICS** (Vcc-5V±10%, GND-0V, Ta-0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{L1} $	$V_{cc} = 5.5 V$ , $V_{cc} = GND$ to $V_{cc}$	-	-	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IN}, V_{LO} = \text{GND to } V_{CC}$	_	-	2.0	μA
Operating Power Supply Current	Icc	$\overline{\text{CS}} = V_{IL}, I_{LO} = 0 \text{mA}$	-	35	80	mA
A	Icci	$\overline{CS} = V_{IL}$ , Minimum Cycle, Duty=100%, $I_{LO} = 0$ mA		40	80	mA
Average Operating Current	Iccz**	Cycle=150ns, Duty=50%, I1.0=0mA		35		mA
C. I. D. C. I. C	Isa	$\overline{CS} = V_{IN}$		5	12	mA
Standby Power Supply Current	I 581	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{s} \le 0.2 \text{V} \text{ or } V_{s} \ge V_{cc} - 0.2 \text{V}$	-	1	100	μA
Outent Values	Vol	Io1. = 8mA		-	0.4	V
Output Voltage	V <sub>OH</sub>	Inn = -3.2mA	2.4	-	-	V

Notes) \* Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

\*\* Reference only.

# CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	C <sub>i</sub> ,	V0V	-	5	pF
Input/Output Capacitance	CLO	V1.0-0V		12	pF

Note) This parameter is sampled and not 100% tested.

# **AC CHARACTERISTICS** (Vcc=5V±10%, Ta=0 to +70°C, unless otherwise noted)

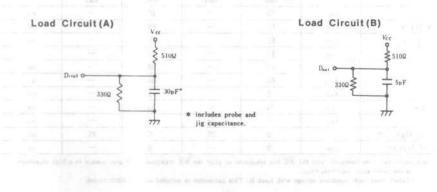
AC TEST CONDITIONS

 Input Pulse Levels
 GND to 3.0V

 Input Rise and Fall Times
 10ns

 Input and Output Timing Reference Levels
 1.5V

 Output Load
 See Figure



**OHITACHI** 

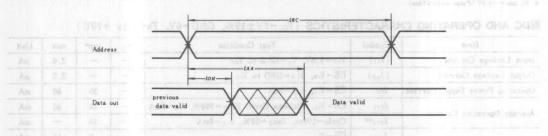
# HM6148LP, HM6148LP-6

# **READ CYCLE**

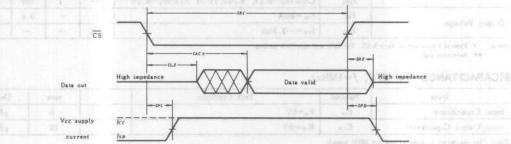
UO Pho Market Certa		HM6148LP		HM61	48LP-6	Unit
Parameter	Symbol	min	max	min	max	Unit
Read Cycle Time	trc	70	-	85	17	ns
Address Access Time	tAA	T	70	and W T	85	n5
Chip Select Access Time	tacs	-	70	-	85	ns
Output Hold from Address Change	ton	5		5	and Thende	ns
Chip Selection to Output in Low Z*	tiz	10	11000 <u>-</u> 000	10	Cold States	ns
Chip Deselection to Output in High Z*	tHZ	0	40	0	40	ns
Chip Selection to Power Up Time	tru	0	- 10	0	-	ns
Chip Deselection to Power Down Time	t <sub>PD</sub>	-	40	-	40	ns

\* Transition is measured ± 500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

# TIMING WAVEFORM OF READ CYCLE NO.1 (1) (2)



• TIMING WAVEFORM OF READ CYCLE NO.2(1)(3)



NOTES) 1. WE is high for Read Cycle.

2. Device is continuously selected,  $\overline{CS} = V_{IL}$ 

3. Address Valid prior to or coincident with CS transition low. BHOLDOHOD TEET DATE

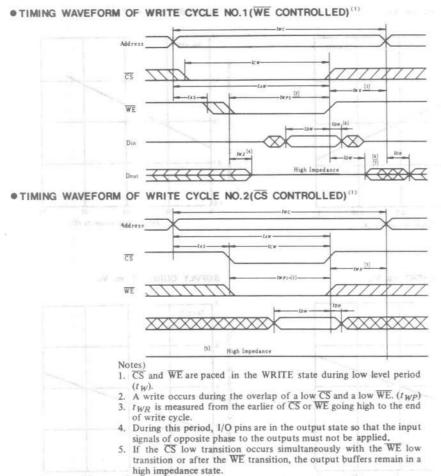
# **WRITE CYCLE**

Parameter	S	HM6148LP		HM6	II-it	
Farameter	Symbol	min	max	min	max	Unit
Write Cycle Time	twc	70		85	-	ns
Chip Selection to End of Write	tew	50	77	60	-(A) 1100210	ns
Address Valid to End of Write	taw	65	-	80	-	ns
Address Setup Time	tas	15	-	15	-	ns
Write Pulse Width*	twpi	50		60	-	ns
write Pulse width*	twpz	65		80	-	ns
Write Recovery Time	twe	5	-	5	Same-	ns
Data Valid to End of Write	tow	30	-	35	-	ns
Data Hold Time	t <sub>DH</sub>	5	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	5	-	ns
Write Enabled to Output in High Z**	twz	0	35	0	45	ns
Output Active from End of Write**	tow	0	-	0	_	ns

Notes) \* When the CS low transition occurs simultaneously with the WE low transition or after the WE transition, 1/0 pins remain in a high impedance state. In this case  $lw_{P1}$ , in the other case  $lw_{P2}(-lw_2+l_{DW})$ .

**OHITACHI** 

\*\* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.



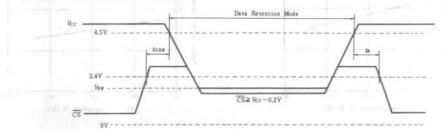
- If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
- 7. Dout is the same phase of write data of this write cycle.

**LOW Vcc DATA RETENTION CHARACTERISTICS** (Ta=0 to +70°C)

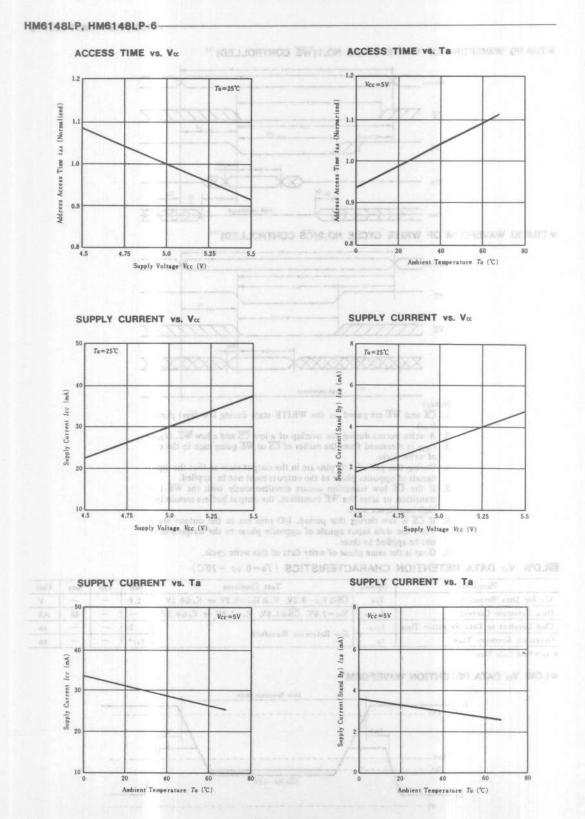
Parameter	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{CS} \ge V_{cc} - 0.2V$ , $V_{is} \ge V_{cc} - 0.2V$ or $V_{is} \le 0.2V$	2.0	1000	-	V
Data Retention Current	ICCDR	$V_{cc} = 2.0V$ , $\overline{CS} \ge 1.8V$ , $V_{cs} = 1.8V$ or $V_{cs} \le 0.2V$	-	-	40	μA
Chip Deselect to Data Retention Time	tear	C D W /	0	-	-	ns
Operation Recovery Time	t <sub>R</sub>	See Retention Waveform	t RC*	$\overline{a} \to \overline{a} \to \overline{a}$	-	ns

\* Isc-Read Cycle Time

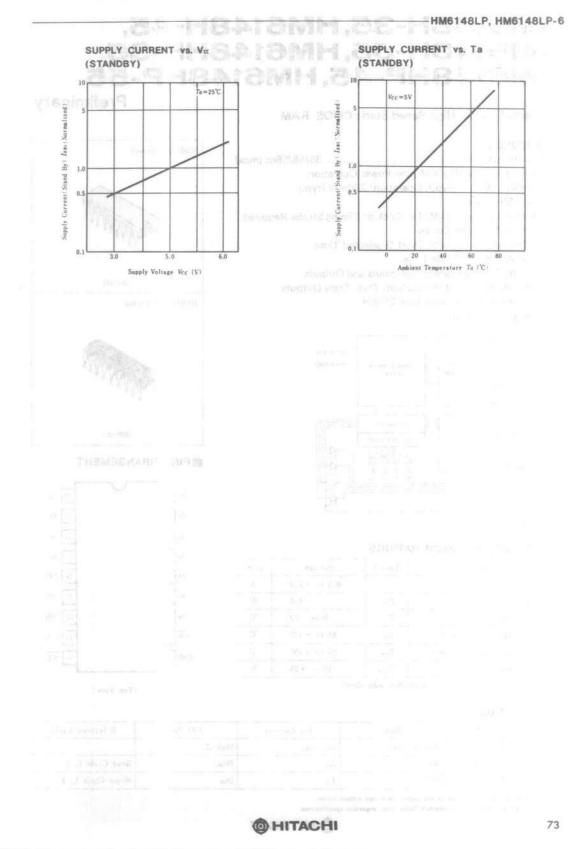
# . LOW Vcc DATA RETENTION WAVEFORM



**HITACHI** 



**HITACHI** 



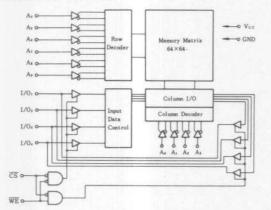
## HM6148H-35, HM6148H-45, HM6148H-55, HM6148HP-35, HM6148HP-45, HM6148HP-55 Preliminary

1024-word x 4-bit High Speed Static CMOS RAM

### **FEATURES**

- Low Power Standby and Low Power Operation; Standby: 100 μW (typ.), Operation: 200mW (typ.)
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t<sub>ACS</sub> with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Common Data Input and Output; Three-State Outputs
- Pin-Out Compatible with Intel 2148H

## BLOCK DIAGRAM



#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit	
Terminal Voltage*	VT	-0.5 to $+7.0$	V	
Power Dissipation	PT	1.0	W	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature (Plastic)	Tele	-55 to $+125$	"C	
Storage Temperature (Ceramic)	Tete	-65 to +150	°C	
Storage Temperature**	Thias	-10 to +85	°C	

\* with respect to GND. Vitain = -3.5V (Pulse width-20ns)

\*\* under bias

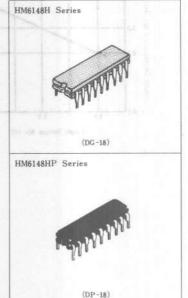
## TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not selected	IsB. IsBI	High Z	
L	Н	Read	Icc	Dout	Read Cycle 1, 2
L	L	Write	Icc	Din	Write Cycle 1, 2

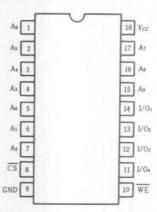
**OHITACHI** 

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.



#### PIN ARRANGEMENT



(Top View)

#### — HM6148H-35, HM6148H-45, HM6148H-55, HM6148HP-35, HM6148HP-45, HM6148HP-55

## ■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	v
	GND	0	0	0	V
Input Voltage	VIH	2.2		6.0	V
	VIL	-0.5*		0.8	V

\* -3.0V (Pulse width 20ns)

## **DC AND OPERATING CHARACTERISTICS[1]** (*Ta*=0~70°C, *Vcc*=5V±10%, GND=0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	$ I_{L1} $	Vcc-max, Via-GND to Vcc	-	-	2.0	μA	
Output Leakage Current	I_L0	$\overline{CS} = V_{IB}, V_{I \ge 0} = GND$ to $V_{CC}$	-	-	2.0	μA	
Operating Power Supply Current	Icc	$\overline{\mathrm{CS}} = V_{IL}, I_{I \ge 0} = 0 \mathrm{mA}$	-	35	80	mA	
Operating Power Supply Current: AC	Icci	min. cycle, $\overline{CS} = V_{lL}, I_{l \ge 0} = 0 \text{mA}$		50	100	mA	(2)
Standby Power Supply Current: DC	Isa	$\overline{CS} = V_{1H}$	-	5	20	mA	
Standby Power Supply Current(1): DC	I <sub>5.81</sub>	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{lN} \le 0.2 \text{V} \text{ or} \\ V_{lN} \ge V_{cc} - 0.2 \text{V}$	87 - <u></u> 8	20	800	μA	
Output Low Voltage	Vol	Io1-8mA	—	-	0.4	V	
Output High Voltage	VON	$I_{OH} = -4.0 \text{mA}$	2.4		_	V	

Notes) 1. Typical limits are at V<sub>cc</sub>-5.0V, Ta-+25°C and specified loading. 2. 120mA max. for HM6148HP-35

#### CAPACITANCE (Ta-25°C, f=1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	$V_{i_{\pi}} = 0 V$	3	5	pF
Input/Output Capacitance	C1 × 0	V1/0-0V	5	7	pF

Note) This parameter is sampled and not 100 % tested.

SOM STORE DAMAGE STORE AND STORE AND STORE

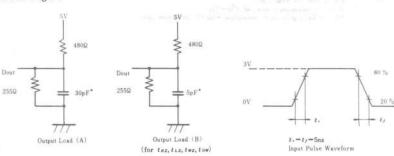
#### **AC CHARACTERISTICS** (Vcc=5V±10%, Ta=0 to +70°C)

### **ORISE FALL TIME**

Item	Symbol	min	typ	max	Unit
Input Rise Time	<i>t</i> ,		5	100	ns
Input Fall Time	ti	(	5	100	ns

#### **OAC TEST CONDITIONS**

Input pulse levels: GND to 3.0V Input rise and fall times: 5ns Input and Output timing reference levels: 1.5V Output load: See Figure



\* Including scope & jig.

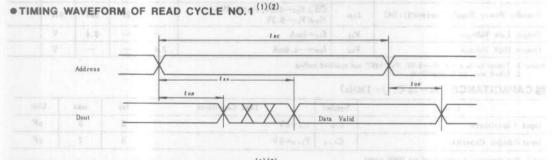
**HITACHI** 

#### HM6148H-35, HM6148H-45, HM6148H-55, -HM6148HP-35, HM6148HP-45, HM6148HP-55

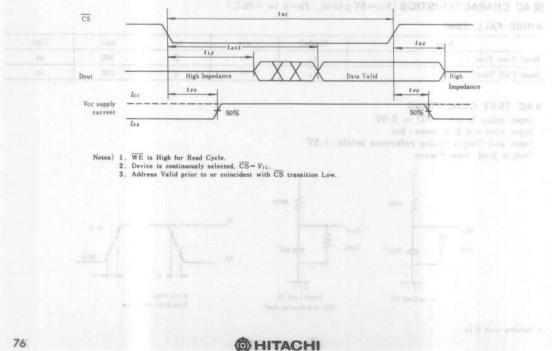
**EAC CHARACTERISTICS** (Ta=0 to 70°C,  $V_{cc}=5V\pm10\%$ , unless otherwise noted.) **• READ CYCLE** 

	0 1 1	HM614	8HP-35	HM6148HP-45		HM6148HP-55		Unit
Item	Symbol	min	max	min	max	mîn	max	Unit
Read Cycle Time	t <sub>RC</sub>	35	-	45	-	55	-	ns
Address Access Time	t <sub>AA</sub>	-,	35	-	45	-	55	ns
Chip Select Access Time	tACS	-	35	-	45	-	55	ns
Output Hold from Address Change	t <sub>on</sub>	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t <sub>LZ</sub> *	10	(c <u>31</u> ( c	10	<u></u>	10	ant <u>o</u> 01	ns
Chip Deselection to Output in High Z	t <sub>HZ</sub> *	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t <sub>PU</sub>	0	1240 - 127	0	-	0	1 1 <u>1</u> 2	ns
Chip Deselection to Power Down Time	t <sub>PD</sub>		30		30	-	30	ns

\* Transition is measured ±500 mV from high impedance voltage with Load(B). This parameter is sampled and not 100% tested. At any temperature and voltage condition tag max is less than the min.



• TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



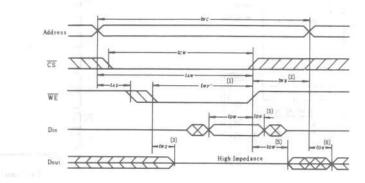
#### HM6148H-35, HM6148H-45, HM6148H-55, HM6148HP-35, HM6148HP-45, HM6148HP-55

## **WRITE CYCLE**

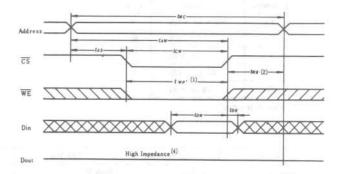
	0.11	HM614	18H/P-35	HM6148	8H/P-45	HM6148H/P-55		17-14	
Item	Symbol	min	max	min	max	min	max	Unit	
Write Cycle Time	twc	35	-	45	-	55	-	ns	
Chip Selection to End of Write	tcw	30	- Trans	40	and Take	50		ns	
Address Valid to End of Write	taw	30	-	40	1.1.20	50		ns	
Address Setup Time	tAS	0	1	0	i gebote	0	2-2	ns	
Write Pulse Width	twp	30	-	35	-	40	-	ns	
Write Recovery Time	twn	5	s nu <u>n</u> st	5	0.0 <u>0</u>	5	-	ns	
Data Valid to End of Write	t <sub>.DW</sub>	20		20		20		ns	
Data Hold Time	t <sub>DH</sub>	0	(ent) T	0	- 1 T	0	-	ns	
Write Enabled to Output in High Z*	twz	0	10	0	15	0	20	ns	
Output Active from End of Write*	tow	0	ini <del>n</del> i00	0	- 4 -	0	-	ns	

\* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO.2 (CS Controlled)



NOTES of Timing Waveform of Write

of liming Waveform of Write 1. A write occurs during the overlap of a low  $\overline{\text{CS}}$  and a low  $\overline{\text{WE}}$ .  $(t_{wP})$ 2. Twe is measured from the earlier of  $\overline{\text{CS}}$  or  $\overline{\text{WE}}$  going high to the end of write cycle. 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied. 4. If the  $\overline{\text{CS}}$  low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain

If the CS into cars simultaneously with the WE low transition or after the WE transition, the output outers remain a high impedance state.
 If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 Dout is the same phase of write data of this

write cycle.



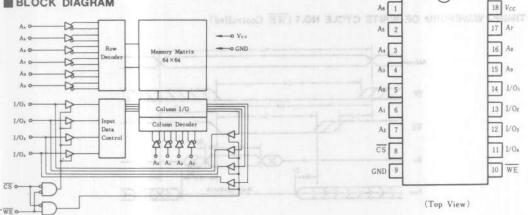
## HM6148HLP-35, HM6148HLP-45, HM6148HLP-55 Preliminary

1024-word × 4-bit High Speed Static CMOS RAM

## **FEATURES**

- Low Power Standby and Low Power Operation; Standby: 5µW (typ.), Operation: 300mW (typ.)
- Fast Access Time: 35/45/55ns (max)
- Capability of Battery Back Up Operation
- Single 5V Supply
- · Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of tacs with Short Deselected Time
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Three State Output
- Pin-Out Compatible with Intel 2148H





(DP-18)

PIN ARRANGEMENT

### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit	
Terminal Voltage*	Vr	-0.5 to $+7.0$	v	and a state of the
Power Dissipation	Pr	1.0	W	and the second s
Operating Temperature	Tepr	0 to +70	°C	
Storage Temperature	- Tela	-55 to +125	"C	
Storage Temperature **	Teres	-10 to +85	°C	111117 3

\* with respect to GND. V11 === = -3.5V (Pulse width = 20ns)

\* \* under bias.

#### TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Reference Cycle
Н	×	Not selected	IsB, IsB1	High Z	
L	Н	Read	Ice has No and	Dout	Read Cycle 1, 2
L	L	Write	Icc	Din	Write Cycle 1, 2

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.



Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	v
Input Voltage	VIH	2.2	22	6.0	v
	VIL	-0.5*	_	0.8	V

**RECOMMENDED DC OPERATING CONDITIONS**  $(T_a = 0 \text{ to } + 70^{\circ}\text{C})$ 

\* -3.0V (Pulse width 20ns)

## ■ DC AND OPERATING CHARACTERISTICS[1] (Ta=0~70°C, Vcc=5V±10%, GND=0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	I_{L1}	Vcc-max, Via-GND to Vcc	-	-	2.0	μA	
Output Leakage Current	I <sub>L0</sub>	$\overline{CS} = V_{IH}, V_{I \times 0} = GND$ to $V_{CC}$	-	-	2.0	μA	
Operating Power Supply Current: DC	Icc	$\overline{\text{CS}} = V_{lL}, I_{l\neq 0} = 0\text{mA}$		35	80	mA	
Operating Power Supply Current : AC	Icci	min. cycle, $\overline{CS} = V_{lL}, I_{l \ge 0} = 0 \text{mA}$	0.00-00-00	50	100	mA	[2]
Standby Power Supply Current : DC	IsB	$\overline{CS} = V_{IH}$		5	20	mA	
Standby Power Supply Current(1): DC	Isbi	$ \overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{lN} \le 0.2 \text{V} \text{ or } \\ V_{lN} \ge V_{cc} - 0.2 \text{V} $	CAN <u>H</u> P	1	50	μA	
Output Low Voltage	Vol	IoL=8mA		-	0.4	V	
Output High Voltage	VON	IOH=-4.0mA	2.4	_		V	

Notes) 1. Typical limits are at  $V_{cc}$  = 5.0V, Ta = +25°C and specified loading. 2. 120mA max. for HM6148HLP-35

## **CAPACITANCE** (*Ta*-25°C, *f*-1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	$V_{i_{n}} = 0$ V	3	5	pF
Input /Output Capacitance	C1.00	V1.0-0V	5	7	pF

Note) This parameter is sampled and not 100 % tested.

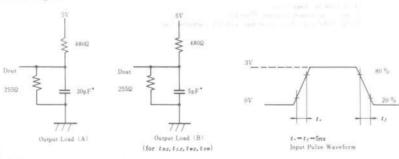
## **AC CHARACTERISTICS** (V<sub>cc</sub>=5V±10%, Ta=0 to +70°C)

### **ORISE FALL TIME**

Item	Symbol	min	typ	max	Unit
Input Rise Time	1,		5	100	ns
Input Fall Time	11		5	100	ns

## **OAC TEST CONDITIONS**

Input pulse levels : GND to 3.0V Input rise and fall times : 5ns Input and Output timing reference levels : 1.5V Output load : See Figure



\* Including scope & jig.



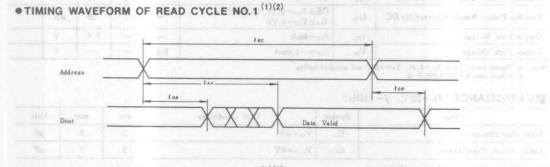
#### HM6148HLP-35, HM6148HLP-45, HM6148HLP-55-

## **EAC CHARACTERISTICS** (Ta=0 to 70°C, $V_{cc}=5V\pm10\%$ , unless otherwise noted.)

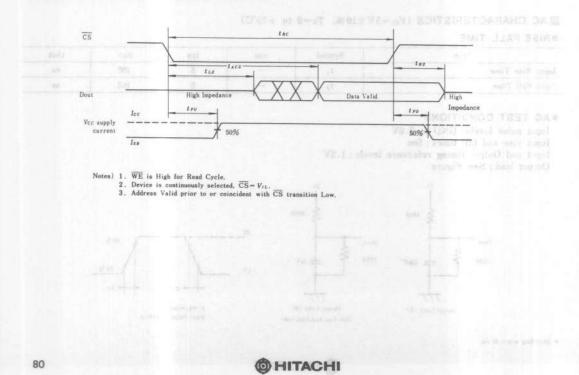
## **READ CYCLE**

Item	6.11	HM6148HLP-35		HM6148HLP-45		HM6148HLP-55		Their
	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	tRC	35	0."R	45	T	55	-	ns
Address Access Time	tAA	-	35		45	=	55	ns
Chip Select Access Time	tACS	-	35	-	45		55	ns
Output Hold from Address Change	toн	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t_Lz*	10	15 0715	10	相关区门	10	1912 QV	ns
Chip Deselection to Output in High Z	t <sub>HZ</sub> *	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t pu	0	A 40 - 13	0	-	0	1.1.1	ns
Chip Deselection to Power Down Time	tPD	100-	30	2	30		30	ns

\* Transition is measured ±500mV from high impedance voltage with Load(B). This parameter is sampled and not 100% tested. At any temperature and voltage condition t<sub>s2</sub> max is less than t<sub>15</sub> min.



• TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



## **WRITE CYCLE**

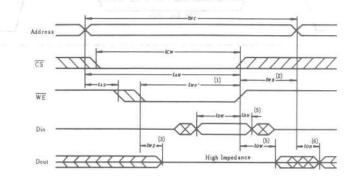
Item	Symbol	HM6148	HLP-35	HM6148HLP-45		HM6148	HLP-55	Unit
	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	35	85. <b>2</b> 07	45	-	55	-	ns
Chip Selection to End of Write	t av	30	20-21-2	40	-	50	-	ns
Address Valid to End of Write	t,w	30	1344	40		50		ns
Address Setup Time	tas	0		0	-	0	-	ns
Write Pulse Width	twp	30	-	35	-	40	-	ns
Write Recovery Time	twn	5	2-2	5	-	5	-	ns
Data Valid to End of Write	tow	20	-	20	-	20		ns
Data Hold Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Write Enabled to Output in High Z •	ťwz	0	10	0	15	0	20	ns
Output Active from End of Write •	tow	0	-	0		0	-	ns

\* Transition is measured ±500 mV from high impedance voltage with Load B.

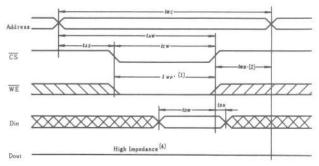
This parameter is sampled and not 100% tested.

All inputs  $t_r$ ,  $t_f$  (rise and fall time) are less than 100 ns.

## • TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO.2 (CS Controlled)

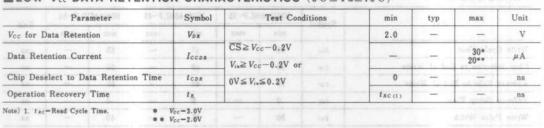


Notes of Timing Waveform of Write

Notes of Timing Waveform of Write : 1. A write occurs during the overlap<sup>2</sup> off  $\forall i$  low  $\overline{CS}$  and a low  $\overline{WE}$ . ( $t_{WP}$ ) 2.  $t_{WA}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle. 3. During this period, 1/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied. 4. If the  $\overline{CS}$  low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain in a high impedance state. 5. If  $\overline{CS}$  is low during this period, 1/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them. 6. Dout is the same phase of write data of this write cycle.

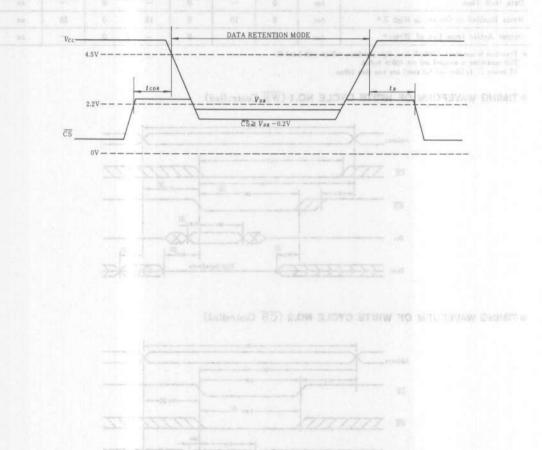


#### HM6148HLP-35, HM6148HLP-45, HM6148HLP-55 -



## **LOW** V<sub>cc</sub> DATA RETENTION CHARACTERISTICS $(0^{\circ}C \le Ta \le 70^{\circ}C)$

#### **OLOW Vcc DATA RETENTION WAVEFORM**



The second s

that TW and a bes 25 and any start of the transfer of the

I say to descend the two wates of 25 m WE going but is an ext of error speed. The to be presed, "10 mer over a 12 magin first as the data spectra makes of presence that we be add.

while continues that a realized to the second secon

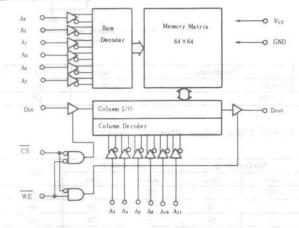
# HM6147, HM6147-3 HM6147P, HM6147P-3

4096-word×1-bit High Speed Static CMOS RAM

### FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby:100µW typ., Operation: 75mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power–On Current
- No Change of t<sub>ACS</sub> with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

#### BLOCK DIAGRAM



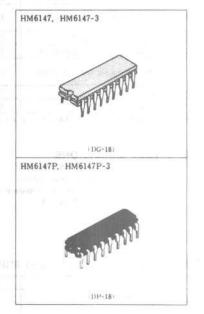
#### **ABSOLUTE MAXIMUM RATINGS**

Item 01	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	Vr	-0.5 to +7.0	V
Power Dissipation	$P_T$	1.0	W
Operating Temperature	T.,,	0 to +70	°C
Storage Temperature(Ceramic)	Tate	-65 to +150	°C
Storage Temperature(Plastic)	Telg	-55 to +125	°C

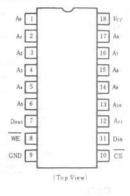
\*  $V_{IN} \min = -1.0 V$  (Pulse Width  $\leq 20 ns$ )

#### **RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
S I V K	Vcc	4.5	5.0	5.5	v
Supply Voltage	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	VIL	-0.3*	-	0.8	V



## PIN ARRANGEMENT





#### HM6147, HM6147-3, HM6147P, HM6147P-3 -

DC AND OPERATING CHARACTERIS	ICS $(0^{\circ}C \leq Ta \leq 70^{\circ}C)$ .	$V_{cc} = 5V \pm 10\%$ ,	GND-0V)
------------------------------	---	--------------------------	---------

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	ILI	Vcc=5.5V, GND to Vcc	-	-	2.0	μA	
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{out} = 0 \sim V_{CC}$	baller	2 (10)	2.0	μA	1.30
Operating Power Supply Current(1) DC	Icc	$\overline{CS} = V_{IL}$ , Output open		15	35	mA	
Operating Power Supply Current(2) DC	Icci	$\overline{\text{CS}} = V_{IL},  V_{IN} \le 0.2 \text{V or} \\ V_{IN} \ge V_{CC} - 0.2 \text{V}$	-	12	-	mA	(2)
Average Operating Current(3)	lecs	Cycle 150ns, duty 50%	-	14	-	mA	(2)
Standby Power Supply Current(1) DC	Isa	$\overline{CS} = V_{IH}$	-	5	12	mA	
Standby Power Supply Current(2) DC	I 5 81	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V},$ $V_{IN} \le 0.2\text{V or } V_{IN} \ge V_{cc} - 0.2\text{V}$	Citota a	20	800	μA	Stand
Output Low Voltage	Vol	$I_{oL} = 12 \text{mA}$		-	0.40	V	Man -
Output High Voltage	Von	$I_{OH} = -8.0 \text{mA}$	2.4	-	-	V	0.0825

Note) 1. Typical limits are at  $V_{cc} = 5.0V$ ,  $Ta = 25^{\circ}C$  and specified loading.

2. Reference only

#### AC TEST CONDITIONS

- Input pulse levels: GND to 3.5V
- Input rise and fall times: 10 ns
- Output load: See Figure 1



TALLES . PARCE

\* Including scope & jig capacitance Figure 1 Output Load

Ver

#### **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Conditions	max	Unit
Input Capacitance	<i>C</i> <sub>i</sub> ,	V=0V 5		pF
Output Capacitance	Cent	V <sub>mi</sub> -0V	7	pF

Note) This parameter is sampled and not 100% tested.

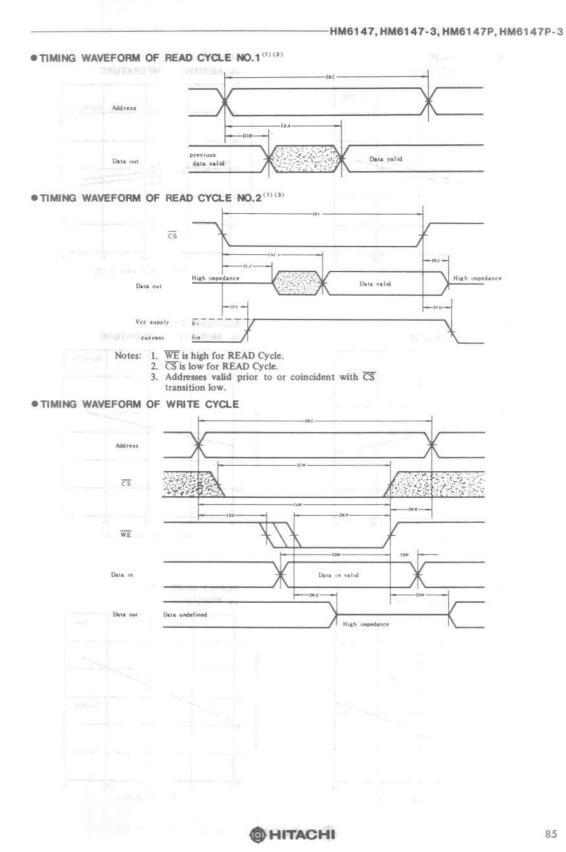
## **EAC CHARACTERISTICS** (Ta-0°C to 70°C, Vcc-5V±10%, unless otherwise noted.) ● READ CYCLE

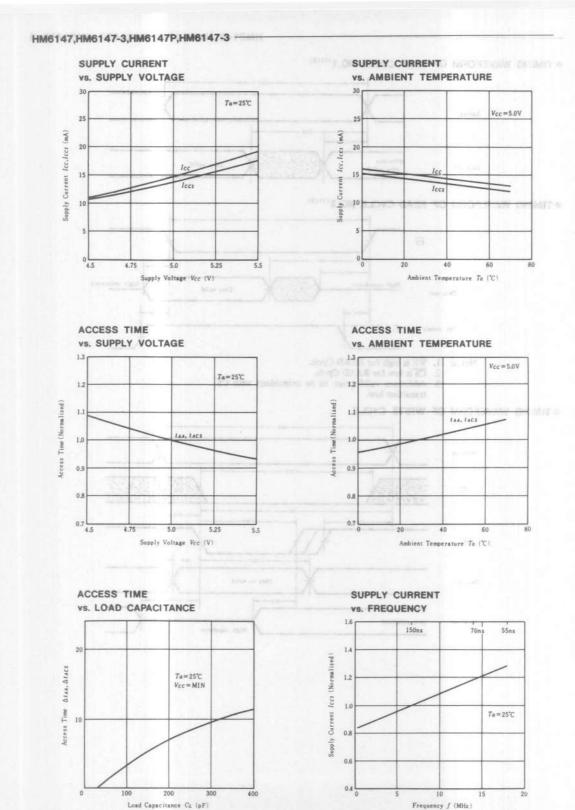
Parameter	C	HM614	17/P-3	HM6	147/P	Unit	
	Symbol	min	max	min	max	Unit	
Read Cycle Time	trc	55	-	70		ns	
Address Access Time	taa	-	55	9 6 9 9 9	70	ns	
Chip Select Access Time	lacs	-	55	-	70	ns	
Output Hold from Address Change	ton	5	-	5	-	ns	
Chip Selection to Output in Low Z	1LZ	10	-	10	NOTES IN STREET	ns	
Chip Deselection to Output in High Z	1 HZ	0	40	0	40	ns	
Chip Selection to Power Up Time	t <sub>PU</sub>	0	we day	0	Red to the shirts	ns	
Chip Deselection to Power Down Time	tpp	-	30		30	ns	

#### **WRITE CYCLE**

Parameter	Symbol	HM61	47/P-3	HM6147/P		Unit	
	Symbol	min	max	min	max	Unit	
Write Cycle Time	twc	55	-	70	-	n5	
Chip Selection to End of Write	tew	45	on names -	55	007908	ns	
Address Valid to End of Write	taw	45	Lookus 77	55	Trad	ns	
Address Setup Time	tas	0	-	0	-	ns	
Write Pulse Width	LWP	35	1	40	-	ns	
Write Recovery Time	twa	10	_	15		ns	
Data Valid to End of Write	tow	25		30	Constanting of the second	ns	
Data Hold Time	t <sub>DH</sub>	10		10	200 10 <u>27</u> 10 10 10	ns	
Write Enabled to Output in High Z	twz	0	30	0	35	ns	
Output Active from End of Write	tow	0	-	0	-	ns	

**OHITACHI** 





86

**OHITACHI** 

Frequency f (MHz)

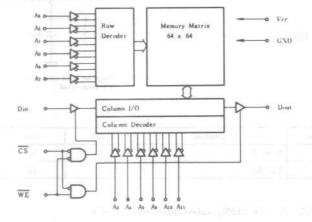
## HM6147LP, HM6147LP-3

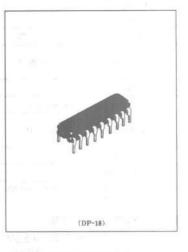
## 4096-word×1-bit High Speed Static CMOS RAM

### FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 5μW typ. Operation: 75mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t<sub>ACS</sub> with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Capability of Battery Back up Operation
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

## BLOCK DIAGRAM





#### PIN ARRANGEMENT

18 Vc
17 As
16 Ar
15 As
14 Aa
13 AH
12 Au
11 Di
10 C

#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	Vr	-0.5 to $+7.0$	V
Power Dissipation	Pr	1.0	W
Operating Temperature	Tapr	0 to +70	°C
Storage Temperature	Tele	-55 to +125	°C

\*  $V_{i\perp}$  min = -1.0V (Pulse Width  $\leq 20$  ns)

#### **RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	v
	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	VIL	-0.3*		0.8	V

\*  $V_{lL}$  min=-1.0V (Pulse width  $\leq 20$ ns)



#### HM6147LP,HM6147LP-3

DC AND OPERATING CHARACTERISTICS (0°C	$C \leq Ta \leq 70^{\circ}C$ ,	$V_{cc} = 5V \pm 10\%$ ,	GND=0V)
---------------------------------------	--------------------------------	--------------------------	---------

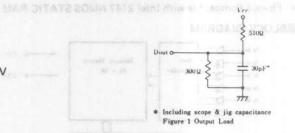
Parameter	Symbol	Test Condition	min	typ	max	Unit	Notes
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5V$ , GND to $V_{cc}$	-	-	2.0	μA	
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{ext} = 0 \sim V_{CC}$	-	-	2.0	μA	1013
Operating Power Supply Current(1) DC	Icc	$\overline{CS} = V_{lL}$ , Output open	N <u>D</u> eni	15	35	mA	Pute -
Operating Power Supply Current(2) DC	Icci	$\overline{CS} = V_{LL},  V_{LN} \le 0.2V \text{ or} \\ V_{LN} \ge V_{CC} = 0.2V$	Lotter P	12	1.142	mA	(2)
Average Operating Current(3)	Icci	Cycle 150ns, duty 50%	- 7/30	14	ind 3	mA	(2)
Standby Power Supply Current(1) DC	Isa	$\overline{CS} = V_{IH}$	-	5	12	mA	0.01
Standby Power Supply Current(2) DC	I <sub>SB1</sub>	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V},  V_{lN} \le 0.2 \text{V or} \\ V_{lN} \ge V_{cc} - 0.2 \text{V}$	nat Sinter (	1	100	μA	161
Output Low Voltage	Vol	$I_{0L} = 12 \text{mA}$	-		0.40	V	1.01
Output High Voltage	Von	Ion = -8.0mA	2.4	500	col To	v	56.5

LIN PIONNI, MINNIONNI

Note) 1. Typical limits are at Vcc-5.0V, Ta-25°C and specified loading. 2. Reference only.

AC TEST CONDITIONS

- Input pulse levels: GND to 3.5V
- Input rise and fall times: 10 ns
- Input and output timing reference levels: 1.5V
- Output load: See Figure 1



**CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Condition	max	Unit
Input Capacitance	C.,	<i>V<sub>IN</sub></i> =0V	5	pF
Output Capacitance	Cast	$V_{out} = 0 V$	7	pF

Note) This parameter is sampled and not 100% tested.

## **AC CHARACTERISTICS** (*Ta*-0°C to 70°C, *V<sub>cc</sub>*-5V±10%, unless otherwise noted.) • READ CYCLE

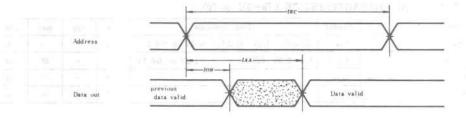
Parameter	Symbol	HM6147LP-3		HM6	Unit	
	Symbol	min	max	min	max	Unit
Read Cycle Time	tRC	55		70		ns
Address Access Time	taa	-	55	-	70	ns
Chip Select Access Time	tacs		55		70	ns
Output Hold from Address Change	ton	5		5	-	ns
Chip Selection to Output in Low Z	t_z	10		10	Sal important	ns
Chip Deselection to Output in High Z	tuz	0	40	0	40	ns
Chip Selection to Power Up Time	tru	0	-	0		ns
Chip Deselection to Power Down Time	1 PD		30	_	30	ns

**CHITACHI** 

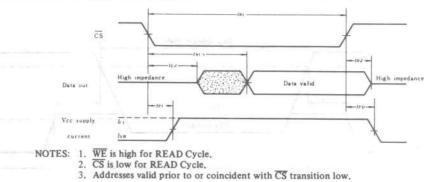
#### **WRITE CYCLE**

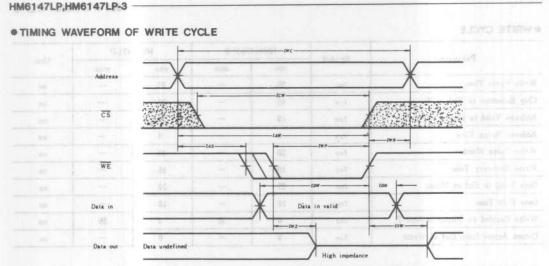
Parameter	C. hi	HM6147LP-3		HM6	147LP	Unit	
	Symbol	min	max	min	max	Unit	
Write Cycle Time	lwc	55		70	-	ns	
Chip Selection to End of Write	lcw	45	-	55	-	ns	
Address Valid to End of Write	LAW	45	- 2	55	-	ns	
Address Setup Time	tas	0		0	-	ns	
Write Pulse Width	twp	35	-	40		ns	
Write Recovery Time	l wR	10	/ -	15	-	ns	
Data Valid to End of Write	tow	25	-	30	-	ns	
Data Hold Time	LDH	10	-	10	—	ns	
Write Enabled to Output in High Z	lwz	0	30	0	35	ns	
Output Active from End of Write	Low	0		0		ns	

## TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



## TIMING WAVEFORM OF READ CYCLE NO.2 (1) (3)





ATTIMUS WAVEFOR'S OF READ OVOLE NO. 1000

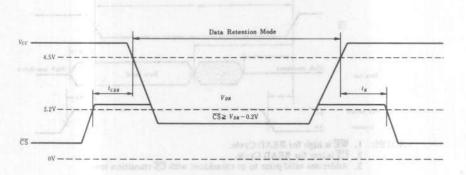
## LOW Vcc RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	VDR	$\widetilde{CS} \ge V_{cc} - 0.2V, V_{i*} \ge V_{cc} - 0.2V$ or $\le 0.2V$	2.0	-	-	V
Data Retention Current	Iccon	$V_{cc}$ =2.0V, $\overline{CS} \ge 1.8V$ , $V_{i} \ge 1.8V$ or $\le 0.2V$			40	μA
Chip Deselect to Data Retention Time	leon		0	-	-	ns
Operation Recovery Time	ta	A second state of the second	tRC*		-	ns

\* tac = Read Cycle Time

. LOW Vcc RETENTION CHARACTERISTICS

STAMING WAVES SHALL OF READ OVER 5 MO. 2"



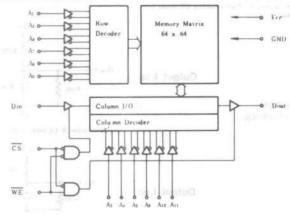
## HM6147H-35, HM6147H-45, HM6147H-55, HM6147HP-35, HM6147HP-45, HM6147HP-55

4096-word×1-bit High Speed Static CMOS RAM

## FEATURES

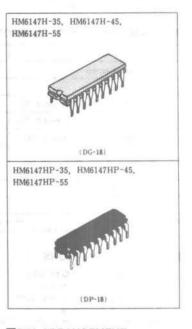
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns/55ns Max.
- Low Power Standby and Low Power Operation, Standby: 100µW typ., Operation: 150mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power-On Current
- No Change of t<sub>ACS</sub> with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM

## BLOCK DIAGRAM

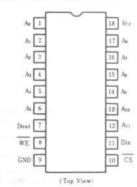


## **MABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	Vr	-3.5* to +7.0	V
DC Output Current	1.	20	mA
Power Dissipation	$P_{T}$	1.0	W
Operating Temperature	T.,,	0 to +70	°C
Storage Temperature (under bias)	Tete (bies)	-10 to +85	"C
Storage Temperature (Ceramic)	Tela	-65 to +150	°C
Storage Temperature (Plastic)	Teta	-55 to +125	"C



#### PIN ARRANGEMENT



■ Pulse Width 20ns, DC: -0.5V

**OHITACHI** 

## HM6147H-35,HM6147H-45,HM6147H-55,HM6147HP-35,HM6147HP-45,HM6147HP-55

## **RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (login 1) Voltage	VIH	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	VIL	-3.0*	1915 701945	0.8	V

\* Pulse Width 20ns, DC: -0.5V

## **DC AND OPERATING CHARACTERISTICS** ( $0^{\circ}C \le Ta \le 70^{\circ}C$ , $V_{cc} = 5V \pm 10\%$ , GND = 0V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{Ll} $	$V_{cc} = 5.5V$ , GND to $V_{cc}$	1903 - 1905	<u></u>	10	μA
Output Leakage Current	ILO	$\overline{\mathrm{CS}} = V_{IH_*}  V_{**t} = 0  \mathrm{V} \sim V_{CC}$			10	μA
Operating Power Supply Current(1) DC	Icc	$\overline{CS} = V_{IL}$ , Output open	-	30	80	mA
Operating Power Supply Current(2) DC	Icci	$\overline{\mathrm{CS}} = V_{l.t.}$ Minimum Cycle	+1977	40	80	mA
Standby Power Supply Current(1) DC	IsB	$\overline{\text{CS}} = V_{IH}, V_{CC} = \text{Min to Max}$	) <u>Suba</u> r (	8	20	mA
Standby Power Supply Current(2) DC	I <sub>581</sub>	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V},$ $V_{lN} \le 0.2\text{V or } V_{lN} \ge V_{cc} - 0.2\text{V}$	9001 164	20	800	μA
Output Low Voltage	Vol	IoL=8mA	ीक्षण ता	we attorn	0.40	V
Output High Voltage	Von	$I_{OH} = -4 \mathrm{mA}$	2.4	-	677	v

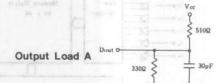
Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute. 2. Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

#### AC TEST CONDITIONS

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V

Output load: See Figure

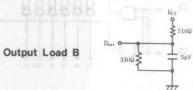
 Output timing reference levels: 1.5V (HM6147H/P-35) 0.8 to 2.0V (HM6147H/P-45/55)





th

5pF



#### **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Symbol Conditions		max	Unit
Input Capacitance	Cin	Via-OV	et.	The s Selected	pF
Output Capacitance	Cest	Vest-0V	h.	6	pF
Note) This parameter is sampled and not 100% t	ested.	0.001	1		internerit next
		28.4 mit 0.1		found retings and	anisated -passed
			The .	(alter i retic)	

**OHITACHI** 

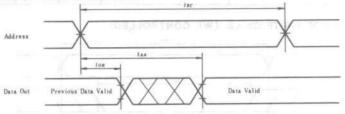
## HM6147H-35,HM6147H-45,HM6147H-55,HM6147HP-35,HM6147HP-45,HM6147HP-55

■ AC CHARACTERISTICS (Ta=0°C to 70°C, Vcc=5V±10%, unless otherwise noted.)

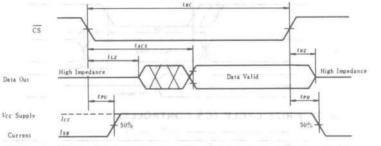
#### READ CYCLE

Parameter	Symbol	HM6147H/P-35		HM6147H/P-45		HM6147H/P-55		Unit	Notes
Farameter		min	max	min	max	min	max	Onit	INOLES
Read Cycle Time	t RC	35		45		55	2 — A	ns	(1)
Address Access Time	tAA	-	35		45	-	55	ns	
Chip Select Access Time	tACS	-	35	-	45	-	55	ns	
Output Hold from Address Change	t on	5	-	5	-	5	-	ns	
Chip Selection to Output in Low Z	t <sub>LZ</sub>	5		5	-	- 5	2	ns	(2), (3), (7)
Chip Deselection to Output in High Z	t <sub>HZ</sub>	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	t <sub>PU</sub>	0	-	0	_	0		ns	
Chip Deselection to Power Down Time	t <sub>PD</sub>	-	20		20		20	ns	
only besteretion to I ower Down Time	* PD		0		20		20	115	

TIMING WAVEFORM OF READ CYCLE NO.1 (4) (5)



## TIMING WAVEFORM OF READ CYCLE NO.2 (4) (8)



- Notes: 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
  - 2. At any given temperature and voltage condition,  $t_{HZ}$  max. is less than <sup>t</sup>LZ min. both for a given device and from device to device.
  - 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B. 4. WE is high for READ Cycle. 5. Device is continuously selected,  $\overline{CS}=V_{IL}$ . 6. Addresses valid prior to or coincident with  $\overline{CS}$  transition low.

  - - 7. This parameter is sampled and not 100% tested.

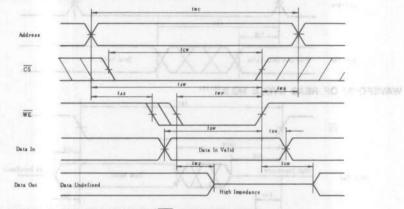


## HM6147H-35, HM6147H-45, HM6147H-55, HM6147HP-35, HM6147HP-45, HM6147HP-55-

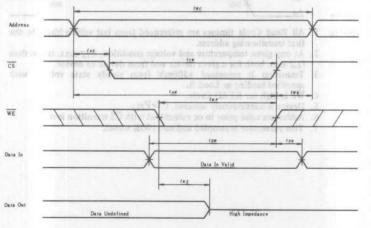
#### **WRITE CYCLE**

Parameter	Symbol -	HM6147H/P-35		HM6147H/P-45		HM6147H/P-55		11.10	Notes
Parameter		min	max	min	max	min	max	Unit	Notes
Write Cycle Time	twc	35	-	45		55		ns	(2)
Chip Selection to End of Write	tow	35		45	-	45	-	ns	100 David
Address Valid to End of Write	E.A.W	35		45	-	45	-	ns	
Address Setup Time	tAS	0		0		0	-	ns	
Write Pulse Width	twp	20		25		30	-	ns	
Write Recovery Time	twa	0		0	-	0		ns	
Data Valid to End of Write	tow	20		25	1 1	25		ns	
Data Hold Time	t <sub>DH</sub>	10		10		10	-	ns	
Write Enabled to Output in High Z	twz	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	tow	0	- 1911	0	10%9 0	0	MR9918	ns	(3), (4)

## . TIMING WAVEFORM OF WRITE CYCLE (WE CONTROLLED)



**•TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)** 



Note I CS or WE are High for Address Transition

Notes: 1. If CS goes high simultaneously with WE high, the output remains in a high impedance states. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 Transition is measured ±500mV from steady state voltage with specified loading in Load B.

4. This parameter is sampled and not 100% tested.

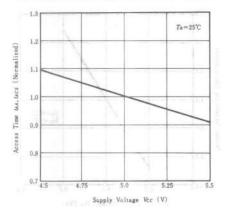
**OHITACHI** 

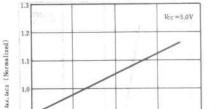
#### -HM6147H-35, HM6147H-45, HM6147H-55, HM6147HP-35, HM6147HP-45, HM6147HP-55

Access Time

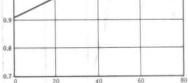
1.3

ACCESS TIME VS. SUPPLY VOLTAGE



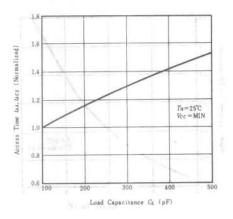


ACCESS TIME VS. AMBIENT TEMPERATURE



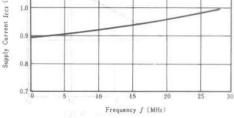
Ambient Temperature Ta (°C)

ACCESS TIME VS. LOAD CAPACITANCE

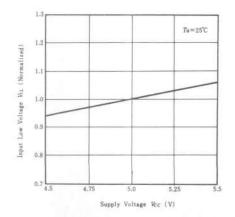




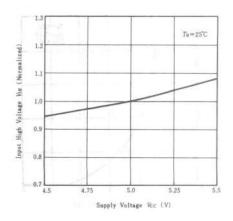
SUPPLY CURRENT VS. FREQUENCY



INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



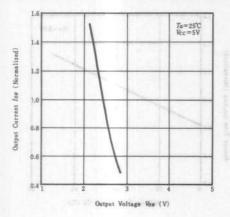


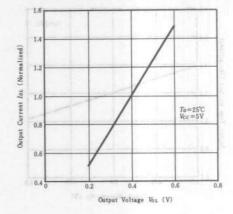


**HITACHI** 

#### HM6147H-35,HM6147H-45,HM6147H-55,HM6147HP-35,HM6147HP-45,HM6147HP-55

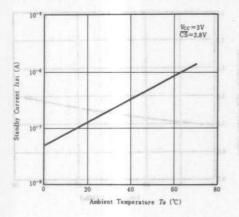
### OUTPUT CURRENT VS. OUTPUT VOLTAGE



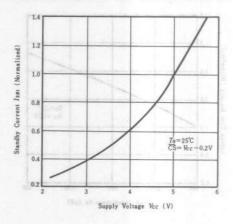


OUTPUT CURRENT VS. OUTPUT VOLTAGE

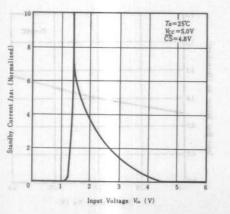
STANDBY CURRENT VS. AMBIENT TEMPERATURE



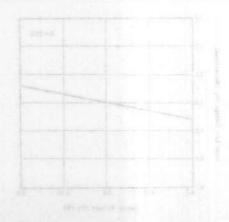
STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE



NPUT LOW VOLTAGE VE. SUPPLY VOLTAGE





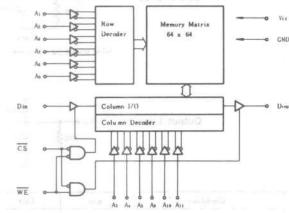
# HM6147HLP-35, HM6147HLP-45, HM6147HLP-55

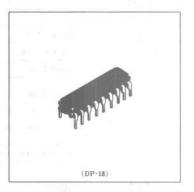
4096-word×1-bit High Speed Static CMOS RAM

## FEATURES

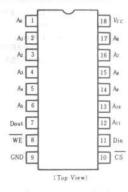
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns /55ns Max.
- Low Power Standby and Low Power Operation, Standby; 5μW typ., Operation: 150mW typ.
- Completely Static Memory No Clock nor Timing Strobe Required
- No Peak Power-On Current
- No Change of t<sub>ACS</sub> with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capable of Battery Back up Operation

## BLOCK DIAGRAM





### PIN ARRANGEMENT



## BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	VT .	-3.5* to +7.0	V
DC Output Current	Io	20	mA
Power Dissipation	PT	1.0	W
Operating Temperature	Tepr	0 to +70	°C
Storage Temperature (under bias)	Tate (hise)	-10 to +85	°C
Storage Temperature	Tstg	-55 to +125	°C

\* Pulse Width 20ns. DC: -0.5V

## **RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Parameter	Symbol	min	typ	max	Unit	
Supply Voltage	Vcc	4.5	5.0	5.5	V	
Supply Voltage	GND	0	0	0	v	
Input High (logic 1) Voltage	V <sub>tH</sub>	2.2	3.0	6.0	V	
Input Low (logic 0) Voltage	VIL	-0.5*	-	0.8	V	

\*  $V_{l\perp}$  min = -3V (Pulse width  $\leq 20ns$ )



#### HM6147HLP-35,HM6147HLP-45,HM6147HLP-55 ILT, CO-TATT AND ON THE

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5$ V, GND to $V_{cc}$	-	-	10	μA
Output Leakage Current	ILO	$\overline{\mathrm{CS}} = V_{IB}, V_{mi} = 0 \mathrm{V} \sim V_{CC}$	_	-	10	μA
Operating Power Supply Current(1) DC	Icc	$\overline{\mathrm{CS}} = V_{IL}$ , Output open	scattrides	30	80	mA
Operating Power Supply Current(2) DC	Icci	$\overline{\text{CS}} = V_{IL}$ , Minimum Cycle	-	40	80	mA
Standby Power Supply Current(1) DC	Ізв	$\overline{CS} = V_{IH}$ , $V_{CC} = Min$ to Max	1000000	5	15	mA
Standby Power Supply Current(2) DC	I <sub>\$81</sub>	$\overline{CS} \ge V_{cc} - 0.2V,$ $V_{lN} \le 0.2V \text{ or } V_{lN} \ge V_{cc} - 0.2V$	- <u>V</u> ior	eN 1	100	μA
Output Low Voltage	Vol	<i>I</i> <sub>0L</sub> = 8mA	3087	10-0-	0.40	V
Output High Voltage	V <sub>o H</sub>	$I_{OH} = -4.0 \text{mA}$	2.4	Rev + NA	to april	V

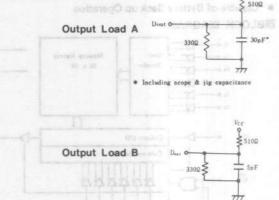
## ■DC AND OPERATING CHARACTERISTICS (0°C ≤ Ta≤70°C, Vcc=5V±10%, GND=0V)

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. TTO COMPANISHE - AN INSTRUM OF COMPANY 2. Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

#### **AC TEST CONDITIONS**

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147HLP-35)

0.8 to 2.0V (HM6147HLP-45/55)



w Cartale Data Inditi and Output Three State Output

MAR OITATE COMM HEAT had the standed and Link #

### **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Conditions	max	
Input Capacitance	<i>C</i> <sub>i*</sub>	V.,-0V	5	pF
Output Capacitance	Cint	Vest-OV 20M TAR	6	pF

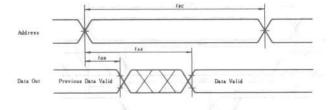
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (Ta=0°C to 70°C, Vcc=5V±10%, unless otherwise noted.) READ CYCLE

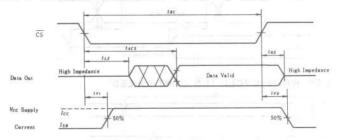
Parameter	Symbol -	HM6147HLP-35		HM6147HLP-45		HM6147HLP-55		Unit	Notes
Parameter		min	max	min	max	min	max	10.440.7	Notes
Read Cycle Time	tac	35	1 + 17 20-	45	-7-	55	- 44	ns	(1)
Address Access Time	1 AA	-	35	-	45	-	55	ns	the strength
Chip Select Access Time	LACS	R SHEAR	35	0177300	45	ARH O	55	ns	1003-1
Output Hold from Address Change	tон	5		5	-	5		ns	
Chip Selection to Output in Low Z	l LZ	5	-	5	-	5	-	ns	(2), (3), (7)
Chip Deselection to Output in High Z	Luz	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	1 PU	0	-	0	-	0	1 <u>1</u>	ns	digital street
Chip Deselection to Power Down Time	t PD		20		20	-	20	ns	the Lange

**HITACHI** 

TIMING WAVEFORM OF READ CYCLE NO.1 (4)(5)



#### TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)



Notes: 1. All Read Cycle timings are referenced from last valid address to the first transitionining address.

- 2. At any given temperature and voltage condition, tHZ max. is less than
- At any given temperature and voitage condition, 'HZ max. is less than <sup>t</sup>LZ min. both for a given device and from device to divice.
   Transition is measured ±500mV from steady state voltage with specified loading in Load B.
   WE is high for READ Cycle.
   Device is continuously selected, CS=V<sub>IL</sub>.
   Addresses valid prior to or coincident with CS transition low.

- 7. This parameter is sampled and not 100% tested.

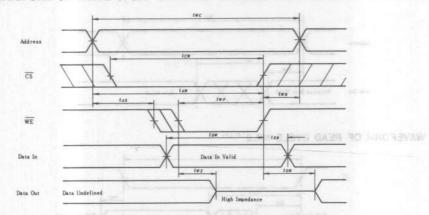
If there is the particular and		HM6147	HLP-35	HM6147HLP-45		HM6147HLP-55		Unit	N
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Write Cycle Time	twc	35	- <u>Son</u>	45	100 <u>0</u> 0	55		ns	[2]
Chip Selection to End of Write	1 cw	35	2000	45	1922	45	_	ns	
Address Valid to End of Write	t.sw	35	- بيارا	45		45	-	ns	
Address Setup Time	tas	0	_	0	-	0		ns	
Write Pulse Width	t wP	20	13-14	25	-	30	-	ns	
Write Recovery Time	t <sub>wn</sub>	0	-	0	-	0	-	ns	
Data Valid to End of Write	t <sub>DW</sub>	20		25	<u> </u>	25		ns	
Data Hold Time	t <sub>DH</sub>	10		10	-	10	-	ns	
Write Enable to Output in High Z	twz	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	tow	0	-	0	-	0		ns	[3], [4]

#### WRITE CYCLE

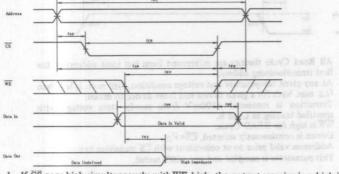


#### HM6147HLP-35,HM6147HLP-45,HM6147HLP-55

TIMING WAVEFORM OF WRITE CYCLE (WE CONTROLLED) 3.000 0438 10 00033 VAV 051000



TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)



Notes: 1. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance states. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 Transition is measured ±500mV from steady state voltage with specified loading in Load B.

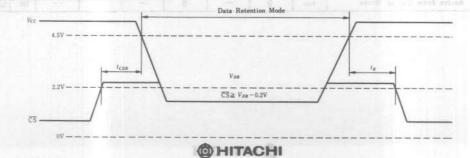
4. This parameter is sampled and not 100% tested.

**IDENTIFY and A RETENTION CHARACTERISTICS**  $(T_a=0^{\circ}C \text{ to } +70^{\circ}C)$ 

Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	V <sub>DR</sub>	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V}$ $V_{lN} \ge V_{cc} - 0.2\text{V or } V_{lN} \le 0.2\text{V}$	2.0	oav <u>R</u>	10 <u>0</u> 110	v
Data Retention Current	Iccor	$V_{CC} = 3.0V, \ \overline{CS} \ge 2.8V$ $V_{IN} \ge 2.8V \text{ or } V_{IN} \le 0.2V$	-	-	50	μA
Chip Deselect to Data Retention Time	tedr	2	0	-	to the se	ns
Operation Recovery Time	t.e.	See Retention Waveform	t RC*	-		ns

\* tac-Read Cycle Time.

**CLOW Vcc DATA RETENTION WAVEFORM** 



## HM6116-2, HM6116-3, HM6116-4 HM6116P-2, HM6116P-3, HM6116P-4

2048-word×8-bit High Speed Static CMOS RAM

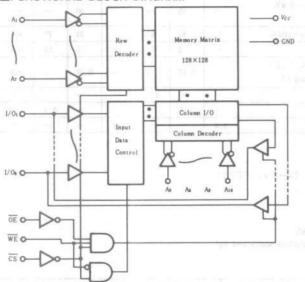
## FEATURES

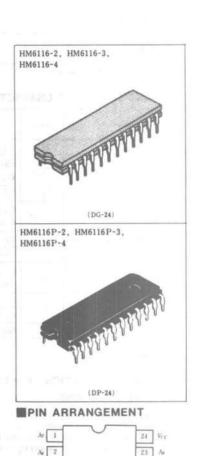
- Single 5V Supply and High Density 24 Pin Package
- 120ns/150ns/200ns (max.) High speed: Fast Access Time
- Low Power Standby and Standby: Low Power Operation
- Operation: 180mW (typ.) Completely Static RAM: No clock or Timing Strobe Required

100µW (typ.)

- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

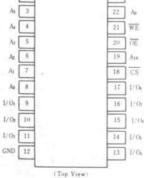
## **FUNCTIONAL BLOCK DIAGRAM**





## **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vr	-0.5* to +7.0	V
Operating Temperature	Tapr	0 to +70	°C
Storage Temperature (Plastic)	Teta CL	-55 to +125	°C
Storage Temperature (Ceramic)	Tele	-65 to +150	°C
Temperature Under Bias	Thin	-10 to +85	"C
Power Dissipation	$P_T$	1.0	W



Å

Ad

TRUTH TABLE

$\overline{\mathrm{CS}}$	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	I 3B, I 3B1	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3)
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	lcc	Din	Write Cycle (2)



## HM6116-2,HM6116-3,HM6116-4,HM6116P-2,HM6116P-3,HM6116P-4

Item	Symbol	min	typ	max	Unit
	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	1 Spe 0 St	0	V
	VIN	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	-	0.8	V

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

\* Pulse Width : 50ns, DC : Vit min = -0.3V

## **DC AND OPERATING CHARACTERISTICS** (Vcc-5V±10%, GND-0V, Ta=0 to +70°C)

Item	C 11	T + C - Pate	HM6116/P-2			HM6116/P-3/-4			Unit
	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	ILI	$V_{cc} = 5.5 V$ , $V_{in} = GND$ to $V_{cc}$	0.05	-	10	-	-	10	μA
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{L:0} = \text{GND to } V_{CC}$	-	-	10	ob <sub>H</sub> C	1.00-20	10	μA
	Icc	$\overline{\mathrm{CS}} = V_{tL}, \ I_{LO} = 0\mathrm{mA}$	-	40	80		35	70	mA
Operating Power Supply Current	Icc1 **	$V_{lH} = 3.5 V, V_{lL} = 0.6 V,$ $I_{l,0} = 0 m A$	-	35		-	30	-	mA
Average Operating Current	Iccz	Min. cycle, duty=100%	-	40	80	-	35	70	mA
Standby Power Supply Current Issu	$\overline{CS} = V_{IR}$	-	5	15		5	15	mA	
	I 5 B 1	$\overline{CS} \ge V_{CC} - 0.2V,  V_{i*} \ge V_{CC}$ $-0.2V \text{ or } V_{i*} \le 0.2V$	-	0.02	2	-	0.02	2	mA
	VoL 10L-4mA	0.4	1-1	T	-	V			
Output Voltage	VoL IoL=2.1mA		-		-	-		0.4	V
	Von	$I_{OH} = -1.0 \text{mA}$	2.4			2.4	-	-	V

\* Vcc-5V, Ta-25°C \*\* Reference Only

#### **EAC CHARACTERISTICS** (Vcc=5V±10%, Ta=0 to +70°C)

#### **AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

## • READ CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		
Item		min	max	mîn	max	min	max	Unit
Read Cycle Time	tac	120		150	-	200	-	ns
Address Access Time	t <sub>AA</sub>	-	120	<u> </u>	150		200	ns
Chip Select Access Time	tAcs	1 7 6	120	-	150	-	200	ns
Chip Selection to Output in Low Z	tclz	10	+	15	-	15	-	ns
Output Enable to Output Valid	tor	o - 11	80		100	Collector II	120	ns
Output Enable to Output in Low Z	totz	10	- n) <u>4</u> (-	15	-	15	tabeth res	ns
Chip Deselection to Output in High Z	tcHZ	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t <sub>onz</sub>	0	40	0	50	0	60	ns
Output Hold from Address Change	ton	10	-	15	-	15	100 000	ns

**OHITACHI** 

#### HM6116-2,HM6116-3,HM6116-4,HM6116P-2,HM6116P-3,HM6116P-4

#### **WRITE CYCLE**

	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
Item		min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	-	150	-	200	_	ns
Chip Selection to End of Write	tew	70	-	90	-	120		ns
Address Valid to End of Write	tAW	105	· · · · · ·	120	-	140	-	ns
Address Set Up Time	LAS	20	<u> </u>	20	-	20	12	ns
Write Pulse Width	twp	70	-	90	-	120	-	ns
Write Recovery Time	t w <sub>R</sub>	5	-	10	_	10		n5
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35		40.		60		ns
Data Hold from Write Time	t DH	5	-	10	-	10		ns
Output Active from End of Write	tow	5		10	-	10		n5

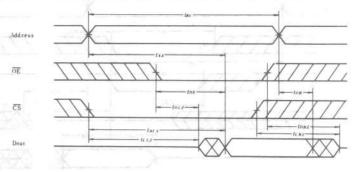
## **CAPACITANCE** (f-1MHz, Ta-25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	<i>C</i> <sub>1</sub> ,	V=0V	3	5	pF
Input/Output Capacitance	Cvo	$V_{LO} = 0 V$	5	7	pF

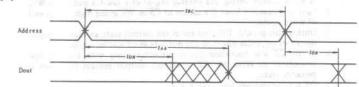
Note) This parameter is sampled and not 100% tested.

#### TIMING WAVEFORM

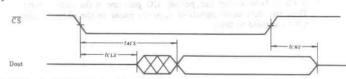
#### • READ CYCLE (1)



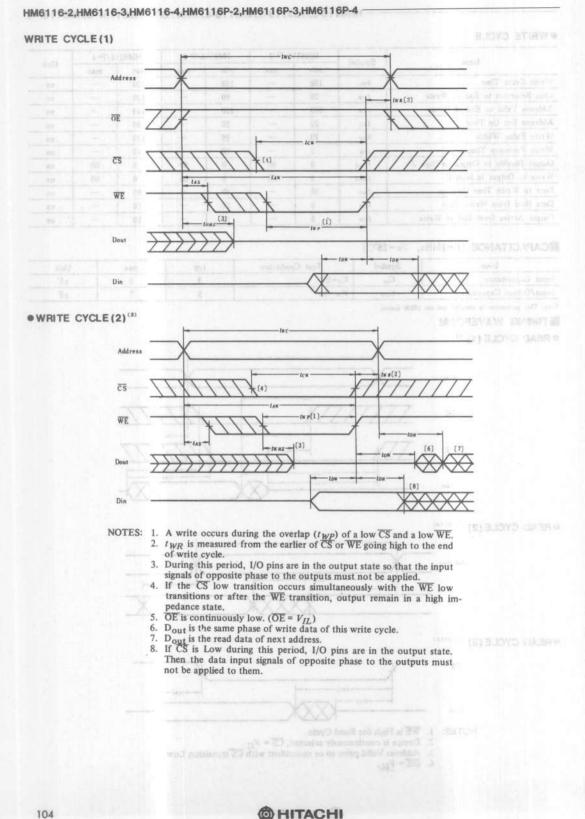


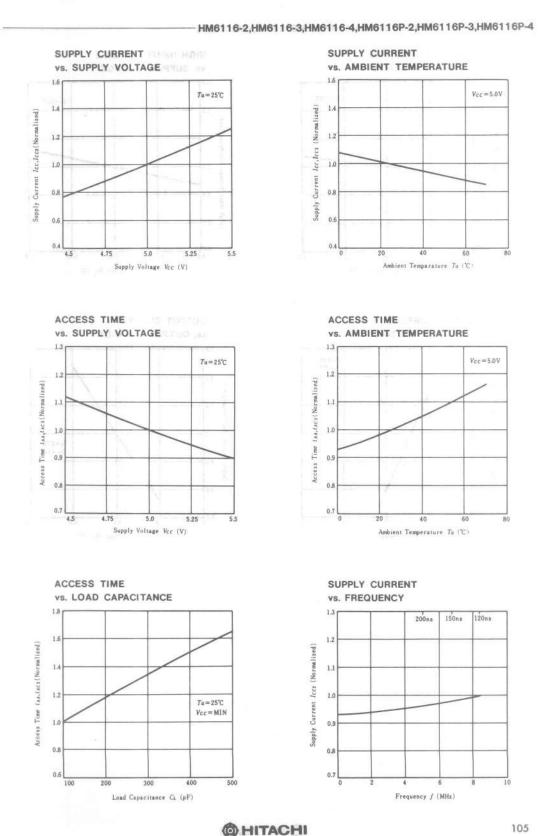


• READ CYCLE (3) (1) (3) (4)

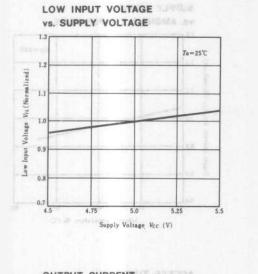


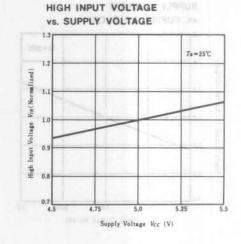
- NOTES: 1. WE is High for Read Cycle. 2. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low. 4.  $\overline{OE} = V_{IL}$ .



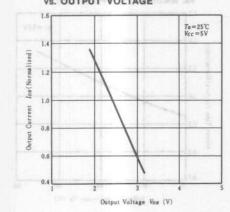








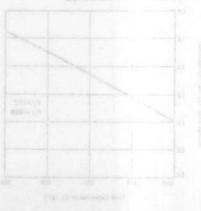
OUTPUT CURRENT



OUTPUT CURRENT

vs. OUTPUT VOLTAGE





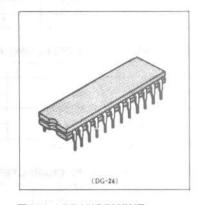
**OHITACHI** 

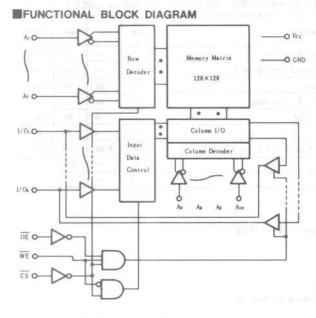
# HM6116I-2, HM6116I-3, HM6116I-4 — Wide Operating Temperature Range —

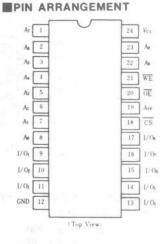
2048-word×8-bit High Speed Static CMOS RAM

## FEATURES

- Wide Operating Temperature Range ..... -40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
   Low Power Standby and Standby: 100µW (typ.)
  - Low Power Operation Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time







## BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vr	-0.5* to +7.0	V
Operating Temperature	$T_{**}$	- 40 to +85	"C
Storage Temperature	Tata	-65 to +150	°C
Power Dissipation	PT	1.0	W

\* Pulse Width 50ns : -1.5V



#### HM61161-2, HM61161-3, HM61161-4 -

TRUTH TABLE out a some pristand bill

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	ISB, ISBI	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

THE REPORT OF THE REPORT OF SCHOOL

#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=-40 to +85°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply voltage	GND	ND 0 0	0	V	
Non March 17 States and	VIH	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	NOT COMPANY	0.8	V

\* Pulse Width : 50ns. DC :  $V_{lL}$  min = -0.3V

EQUIT ACCESS MULTICACION DURING

#### **DC AND OPERATING CHARACTERISTICS** (Vec =5V±10%, GND=0V, Ta=-40 to +85°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	I_L	Vcc=5.5V, V.=GND to Vcc	-	-	10	μA
Output Leakage Current	11201	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ , $V_{LO} = GND$ to $V_{CC}$	-	-	10	μA
Operating Power Supply	Icc	$\overline{\text{CS}} = V_{IL},  I_{I,O} = 0 \text{mA}$	-	35	90	mA
Current	Ices **	$V_{IH} = 3.5 V, V_{IL} = 0.6 V, I_{LO} = 0 mA$	-	30	5-	mA
Average Operating Current	Ices	Min. cycle, duty=100%		35	90	mA
Standby Power Supply	Ism	CS = V <sub>IN</sub>	-	4	20	mA
Current	I 581	$\overline{CS} \ge V_{cc} - 0.2V, V_{i*} \ge V_{cc} - 0.2V \text{ or } V_{i*} \le 0.2V$	100	0.02	2	mA
Output Voltage	Voz	IoL=2.1mA	-	-	0.4	V
contract interes	VON	$I_{OH} = -1.0 \text{mA}$	2.4		10 10 90  90 20 2	V

Vcr = 5V, Tz= 25°C
\*\* Reference Only

and the second se

## **EAC CHARACTERISTICS** ( $V_{cc}=5V\pm10\%$ , $T_a=-40$ to $+85^{\circ}C$ )

#### **AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns Input and Output Timing Reference Levels: 1.5V Output Load: 1TTL Gate and CL = 100pF (including scope and jig)

#### READ CYCLE

ASSOLUTE MANUMUM ENDING

The second s	C	HM6116I-2		HM6116I-3		HM6116I-4		Unit	
Item	Symbol	min	max	min	max	min	max	Unit	
Read Cycle Time	t <sub>RC</sub>	120	02+ <u>at</u> 04	150		200	e verste <del>er</del> ginn	ns	
Address Access Time	laa	3-1	120	-	150	-	200	ns	
Chip Select Access Time	tacs	- n - 1	120		150	-	200	ns	
Chip Selection to Output in Low Z	ters	10		10	-	10	-	ns	
Output Enable to Output Valid	tor	-	80	-	100	-	120	ns	
Output Enable to Output in Low Z	toLZ	10	-	10	-	10	-	ns	
Chip Deselection to Output in High Z	t <sub>c HZ</sub>	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z.	tosz	0	40	0	50	0	60	ns	
Output Hold from Address Change	ton	10	-	10	-	10	-	ns	

#### **WRITE CYCLE**

	6 1 1	HM611	16 I-2	HM611	161-3	HM61	HM61161-4	
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	two	120		150		200	-	ns
Chip Selection to End of Write	low	70	-	90	-	120	-	ns
Address Valid to End of Write	taw	105		120	-	140	-	ns
Address Set Up Time	LAS	20	-	20	—	20	-	ns
Write Pulse Width	twp	70		90		120	-	ns
Write Recovery Time	twa	5	-//	10	-	10	-	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	Low	35		40	-	60	-	ns
Data Hold from Write Time	t <sub>DH</sub>	5	<u> </u>	10	-	10	-	ns
Output Active from End of Write	tow	5		10		10	-	ns

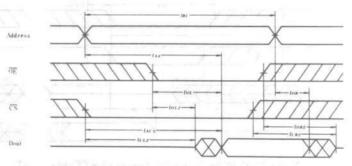
#### **CAPACITANCE** (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,.	$V_{in} = 0 V$	3	5	pF
Input/Output Capacitance	C1/0	V10 = 0V	5	7	pF

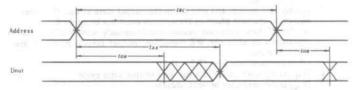
Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

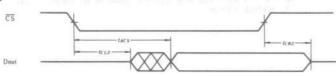
READ CYCLE (1) (1) (5)



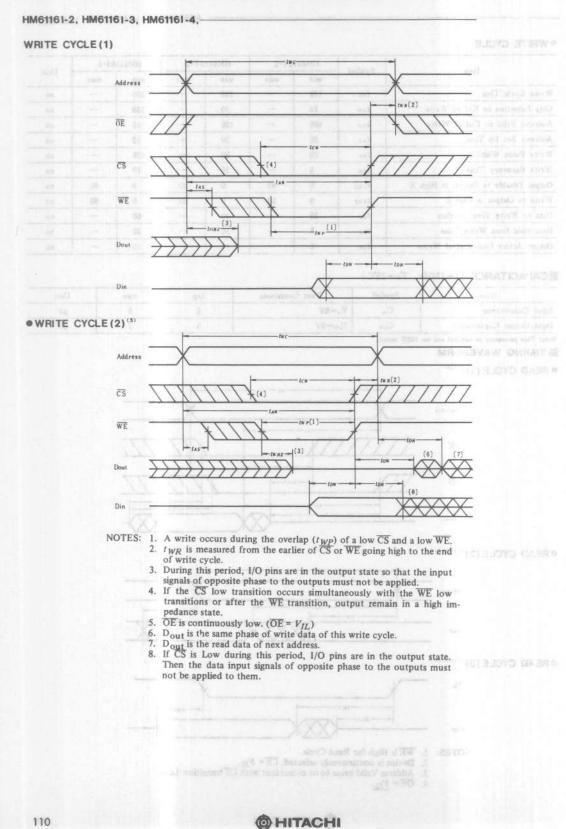
• READ CYCLE (2) (1) (2) (4)



• READ CYCLE (3) (1) (3) (4)



NOTES: 1. WE is High for Read Cycle. 2. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low. 4.  $\overline{OE} = \underline{V_{IL}}$ .

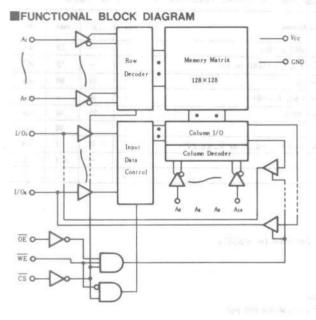


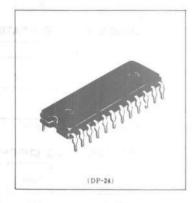
## HM6116PI-2, HM6116PI-3, HM6116PI-4 — Wide Operating Temperature Range —

#### 2048-word×8-bit High Speed Static CMOS RAM

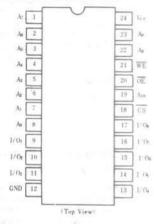
#### FEATURES

- Wide Operating Temperature Range ..... -40~+85°C
- Single 5V Supply and High Density 24 Pin Package
   High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and
   Standby: 100μW (typ.)
- Low Power Operation Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time





#### PIN ARRANGEMENT



#### **MABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vr	-0.5* to +7.0	V
Operating Temperature	T.,,	-40 to +85	°C
Storage Temperature	Tere	-55 to +125	"C
Power Dissipation	Pr	1.0	W
* Pulse Width 50ns : -1.5V	11	1.0	

#### HM6116PI-2, HM6116PI-3, HM6116PI-4-

#### TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	ISB, ISBI	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

## RECOMMENDED DC OPERATING CONDITIONS (Ta=-40 to +85°C)

Item	Symbol	min	typ	max	Unit
e 1 11 1	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	noi 0 - o 0	V
	VIN	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	on some and	0.8	v

\* Pulse Width: 50ns. DC: Vic min=-0.3V

### DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, GND=0V, Ta=-40 to +85°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	IL1	Vcc-5.5V, VGND to Vcc			10	μA
Output Leakage Current	1100	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ , $V_{LO} = GND$ to $V_{CC}$		- /	10	μA
Operating Power Supply	Icc	$\overline{CS} = V_{IL}, I_{I/0} = 0 \text{mA}$	-	35	90	mA
Current	Icci **	$V_{IN} = 3.5 V$ , $V_{IL} = 0.6 V$ , $I_{LO} = 0 mA$	-	30		mA
Average Operating Current	Iccz	Min. cycle, duty=100%	1-1-1	35	90	mA
Standby Power Supply	I <sub>5.0</sub>	CS-V <sub>IH</sub>	- 1	4	20	mA
Current	I <sub>SB1</sub>	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V},  V_{is} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{is} \le 0.2 \text{V}$	-	0.02	2	mA
Output Voltage	Vol	<i>I</i> <sub>0L</sub> = 2.1mA	11-	-	0.4	V
output ronage	Von	$I_{QH} = -1.0 \text{mA}$	2.4	-	10 10 90  90 20 2	V

cc=5V, Ta=250

\*\* Reference Only

### **EAC CHARACTERISTICS** (Vcc-5V±10%, Ta--40 to +85°C)

#### **AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

#### • READ CYCLE

Item	Symbol	HM61	16PI-2	HM61	16PI-3	HM6116PI-4		
	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	1 RC	120	+ 57 22-	150	-	200	-	ns
Address Access Time	taa	4 - 3	120	-	150	-	200	ns
Chip Select Access Time	lacs	-	120	-	150	- 5-	200	ns
Chip Selection to Output in Low Z	tell	10	-	10	-	10	-	ns
Output Enable to Output Valid	LOE	-	80	_	100	-	120	ns
Output Enable to Output in Low Z	losz	10	-	10	-	10	-	ns
Chip Deselection to Output in High Z	t <sub>c HZ</sub>	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	LOHZ	0	40	0	50	0	60	ns
Output Hold from Address Change	ton	10	-	10	-	10	_	ns



#### **WRITE CYCLE**

1	8 11	HM61	16PI-2	HM611	6PI-3	HM6116PI-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	lwc	120	-	150	140 <u>-</u>	200	-	ns
Chip Selection to End of Write	tew	70	-	90	-	120	-	ns
Address Valid to End of Write	t <sub>AW</sub>	105		120		140		ns
Address Set Up Time	LAS	20	-	20	-	20	-	ns
Write Pulse Width	twp	70	-	90	-	120	-	ns
Write Recovery Time	twa	5	-	10		10	-	ns
Output Disable to Output in High Z	LONZ	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	1 DW	35		40	-	60	-	ns
Data Hold from Write Time	ton	5	den /	10	-	10	-	ns
Output Active from End of Write	Low	5	-	10	-	10		ns

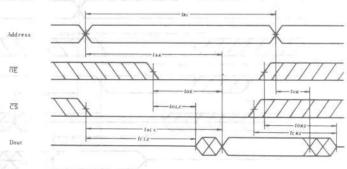
#### **CAPACITANCE** (f-1MHz, Ta-25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,,	$V_{i} = 0 V$	3	5	pF
Input/Output Capacitance	C10	$V_{l,o} = 0V$	5	7	pF

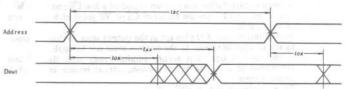
Note) This parameter is sampled and not 100% tested.

### TIMING WAVEFORM

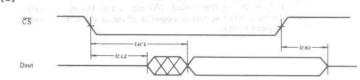
• READ CYCLE (1) (1)



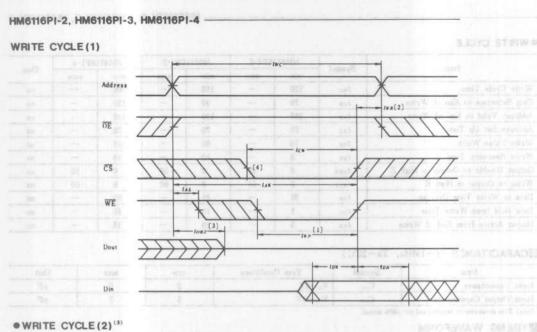
## READ CYCLE (2) (1) (2) (4)

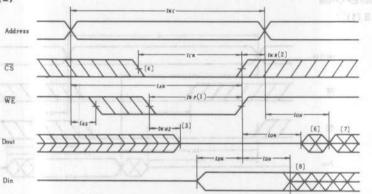


• READ CYCLE (3) (1) (3) (4)



- NOTES: 1. WE is High for Read Cycle. 2. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low. 4.  $\overline{OE} = V_{IL}$ .





NOTES: 1. A write occurs during the overlap  $(t_{WP})$  of a low  $\overline{CS}$  and a low  $\overline{WE}$ . 2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.

3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.

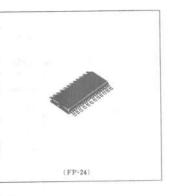
- OE is continuously low. (OE = V<sub>IL</sub>)
   D<sub>out</sub> is the same phase of write data of this write cycle.
- 7.
- Out is the read data of next address. If CS is Low during this period, I/O pins are in the output state. 8. Then the data input signals of opposite phase to the outputs must not be applied to them.

# HM6116FP-2, HM6116FP-3, HM6116FP-4

2048-word×8-bit High Speed Static CMOS RAM

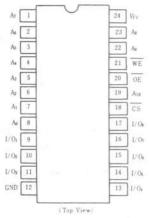
#### FEATURES

- High Density Small-Sized Package
- Projection Area Redueced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby
- Standby: 100µW (typ.)
- Low Power Operation;
- Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- FUNCTIONAL BLOCK DIAGRAM



#### -O Vec AL O Row Memory Matrix O GND Decoder . 128×128 AT C . . Column I/O 1/010 Input Column Decoder Data Control 1/0.0 ò As Âs. As Ave DE O-WE C CS O

### PIN ARRANGEMENT



### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	$V\tau$	-0.5* to +7.0	V
Operating Temperature	Top,	0 to +70	*C
Storage Temperature	Talg	-55 to +125	°C
Temperature Under Bias	There	-10 to +85	°C
Power Dissipation	Pr	1.0	W

\*  $V_{1S}$  min = -1.5V (Pulse Width  $\leq 50 \text{ ns}$ )

#### TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	158, 1581	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle(1)~(3
L.	Н	L.	Write	Icc	Din	Write Cycle(1)
L	L	L	Write	Icc	Din	Write Cycle(2)



#### HM6116FP-2,HM6116FP-3,HM6116FP-4

### RECOMMENDED DC OPERATING CONDITIONS (Ta-0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0 M SOREO STATE COROS RU	0 49 8	v	
	VIN	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*		0.8	v

\* Pulse Width: 50ns, DC: VIL min--0.3V

nou to shrink and of bacable as

TOHONT S-TRUCTION

#### **DC AND OPERATING CHARACTERISTICS** (Vcc-5V±10%, GND=0V, Ta=0 to +70°C)

10 m		T . C . Pris	Н	M6116FF	-2	H	M6116FP	-3/-4	11.1
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc}$ =5.5V, $V_{is}$ =GND to $V_{cc}$	ap <del>b</del> e.	-	10	-	100 me	10	μA
Output Leakage Current	IL0	$\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH}$ $V_{I,0} = \text{GND to } V_{CC}$	ni '-u	n sis <del>u</del> to	ol/10	164	121-6	10	μA
	Icc	$\overline{\mathrm{CS}} = V_{lL}, \ I_{L'0} = 0\mathrm{mA}$	-	40	80	T .Tou	35	70	mA
Operating Power Supply Current	Icci**	$V_{IR} = 3.5 V, V_{IL} = 0.6 V,$ $I_{LO} = 0 m A$	-	35	AS <u>D</u> A	a <u>x</u> r	30	иол	mA
Average Operating Current	Iccz	Min. cycle, duty=100%	-	40	80	-	35	70	mA
	I 5 B	$\overline{\text{CS}} = V_{IH}$		5	15	-	5	15	mA
Standby Power Supply Current	Isbi	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V},  V_{i*} \ge V_{cc}$ $-0.2 \text{V or } V_{i*} \le 0.2 \text{V}$	-	0.02	2		0.02	2	mA
1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Io1-4mA	-	-	0.4	-		-	V
Output Voltage	Vol	IoL=2.1mA	+ 1	-	-	-	-	0.4	V
	Von	I <sub>0H</sub> =-1.0mA	2.4	and the	-	2.4			V

♥ Vcc=5V, Ta=25°C

\*\* Reference Only

#### **EAC CHARACTERISTICS** ( $V_{cc}=5V\pm10\%$ , Ta=0 to $+70^{\circ}$ C)

#### AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

#### • READ CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM611	16FP-4	Unit	
Item	Symbol	mîn	max	min	max	min	max	Unit	
Read Cycle Time	tac	120	-	150	-	200	-	ns	
Address Access Time	t <sub>AA</sub>		120		150	-	200	ns	
Chip Select Access Time	lacs	-	120	-	150	-	200	ns	
Chip Selection to Output in Low Z	ICLZ	10	-	15	-	15	-	ns	
Output Enable to Output Valid	LOE	-	80	-	100	-	120	ns	
Output Enable to Output in Low Z	tolz	10	-	15	-	15	-	ns	
Chip Deselection to Output in High Z	t <sub>CHZ</sub>	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	ton	10	-	15	-	15		ns	

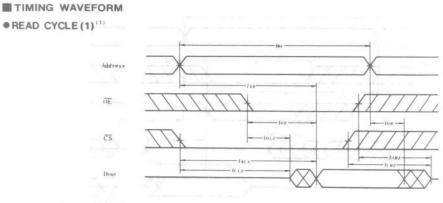
#### **WRITE CYCLE**

Terrer	0.11	HM61	16FP-2	HM61	16FP-3	HM6116FP-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	-	150	7	200	-	ns
Chip Selection to End of Write	tow	70		90		120	-	ns
Address Valid to End of Write	taw	105	-	120		140	-	ns
Address Set Up Time	tAS	20		20	-	20	-	ns
Write Pulse Width	twp	70		90	-	120	_	ns
Write Recovery Time	twR	5	- /	-10	-	10	-	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	/	40	-	60	-	ns
Data Hold from Write Time	t <sub>DH</sub>	5	- 4.	10	-	10	-	ns
Output Active from End of Write	tow	5		10		10		ns

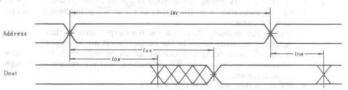
**CAPACITANCE** (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cis	$V_{in} = 0V$	3	5	pF
Input/Output Capacitance	$C_{L'^0}$	$V_{LO} = 0V$	5	7	pF

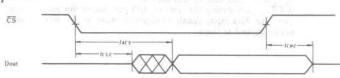
Note) This parameter is sampled and not 100% tested.



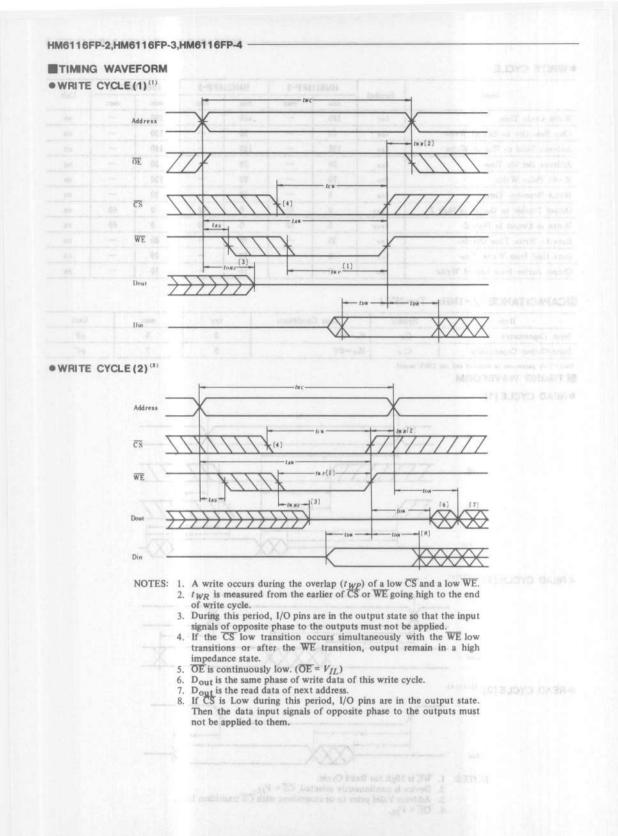
## • READ CYCLE (2) (1) (2) (4)

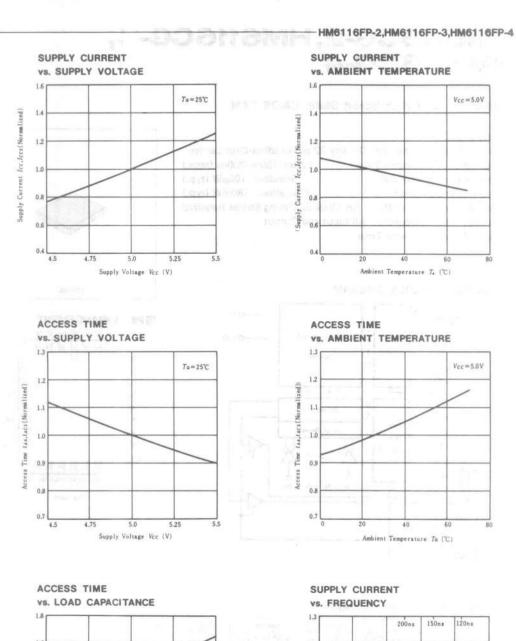


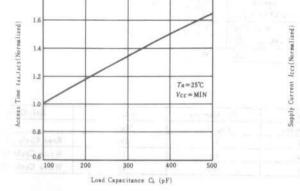
• READ CYCLE (3) (1) (3) (4)

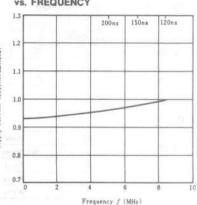


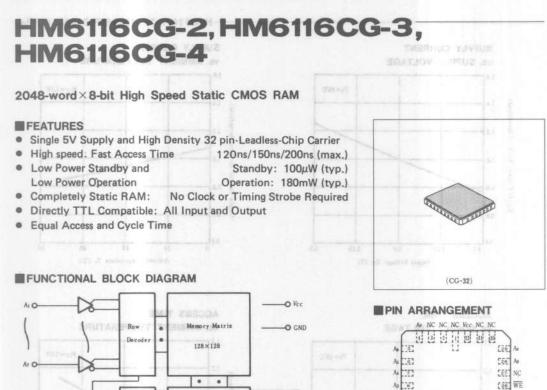
NOTES: 1. WE is High for Read Cycle. 2. Device is continuously selected,  $\overline{\text{CS}} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{\text{CS}}$  transition Low. 4.  $\overline{\text{OE}} = V_{IL}$ .











CZE OE

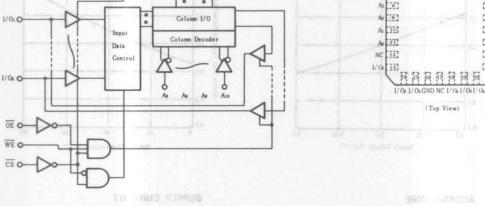
STE CS

(語)1/0

121 1/0:

A10

1241



#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	VT	-0.5* to +7.0	V	
Operating Temperature	Tape	0 to +70	°C	
Storage Temperature	Tete	-65 to +150	°C	
Power Dissipation	PT	1.0	W	

#### TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	ISB, ISBI	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)



#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
upply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
	VIH	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*		0.8	V

\* Pulse Width : 50ns, DC : Vit min=-0.3V

#### DC AND OPERATING CHARACTERISTICS (Vcc-5V±10%, GND=0V, Ta=0 to +70°C)

18 9		6 90 0	H	M6116CG	-2	HM	6116CG-	3/-4	The
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5V_*$ $V_{i*} = GND$ to $V_{cc}$	-	-	10	-	-	10	μA
Output Leakage Current	$ I_{L0} $	$\overline{CS} = V_{IN} \text{ or } \overline{OE} = V_{IN},$ $V_{I \circ O} = \text{GND to } V_{CC}$	-	-	10	-	-	10	μA
	Icc	$\overline{CS} = V_{IL}, I_{LO} = 0 \text{mA}$	-	40	80	-	35	70	mA
Operating Power Supply Current	Icci **	$V_{LH} = 3.5 V, V_{LL} = 0.6 V,$ $I_{1/2} = 0 \text{ mA}$	10=14	35	-	-	30		mA
Average Operating Current	Icci	Min. cycle, duty=100%	-	40	80	-	35	70	mA
	Isn	$\overline{CS} = V_{IH}$	-	5	15	-	5	15	mA
Standby Power Supply Current	I 5 81	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V},  V_{i*} \ge V_{CC}$ $-0.2 \text{V or } V_{i*} \le 0.2 \text{V}$	-	0.02	2	-	0.02	2	mA
		$I_{OL} = 4 \mathrm{mA}$		-	0.4	-	_		V
Output Voltage	VOL	/Io1.=2.1mA	-	-	-	-	-	0.4	V
	V <sub>o#</sub>	$I_{08} = -1.0 \text{mA}$	2.4	-	_	2.4			V

\*  $V_{CC} = 5V$ ,  $Ta = 25^{\circ}C$ 

\*\* Reference Only

#### **AC CHARACTERISTICS** (Vcc=5V±10%, Ta=0 to +70°C)

#### AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns Input and Output Timing Reference Levels: 1.5V Output Load: 1TTL Gate and CL = 100pF (including scope and jig)

#### • READ CYCLE

Item	0.1.1	HM61	HM6116CG-2		HM6116CG-3		16CG-4	Unit
Item	Symbol	min	max	mîn	max	min	max	Unit
Read Cycle Time	tRC	120	_	150	-	200		ns
Address Access Time	tAA	-V-V	120	-	150	-	200	ns
Chip Select Access Time	tacs		120	-	150		200	ns
Chip Selection to Output in Low Z	leiz	10	-	15	-	15		ns
Output Enable to Output Valid	tor	-	80		100		120	ns
Output Enable to Output in Low Z	torz	10	-	15	_	15		ns
Chip Deselection to Output in High Z	tenz	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	tonz	0	40	- 0	50	0	60	ns
Output Hold from Address Change	t <sub>on</sub>	10	(AEN)	15	-	15		ns

Town Route of Harther Lin

d mathematical affects, branker to writering bit investment

11.7



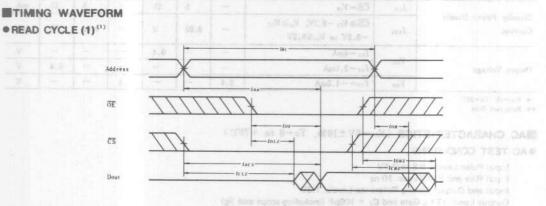
#### HM6116CG-2,HM6116CG-3,HM6116CG-4

#### **WRITE CYCLE**

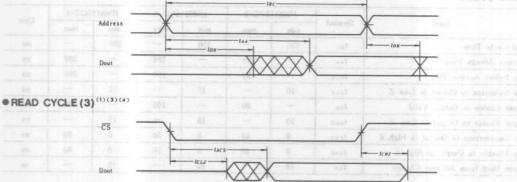
Item		HM6116CG-2		HM6116CG-3		HM6116CG-4		Unit	
Item	Symbol	min	max	min	max	min	max	Unit	
Write Cycle Time	lwc .	120	-	150	-	200	- 190	ns	
Chip Selection to End of Write	tew	70	-	90	-	120	-	ns	
Address Valid to End of Write	tAW	105		120	-	140	91	ns	
Address Set Up Time	las	20	-	20	-	20	-	ns	
Write Pulse Width	twp	70	-	90	- "	120	21	ns	
Write Recovery Time	twa	5	-	10	-	10	-	ns	
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Write to Output in High Z	twnz	0	50	0	60	0	60	ns	
Data to Write Time Overlap	4.DW	35	1000	40	-	60	mpri	ns	
Data Hold from Write Time	t <sub>DN</sub>	5		10		10		ns	
Output Active from End of Write	tow	5	-	10	-	10	-	ns	

#### **CAPACITANCE** (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	V.,-0V	3	5	pF
Input/Output Capacitance	Cuo	V1.0-0V	5	7	pF



• READ CYCLE (2) (1) (2) (4)



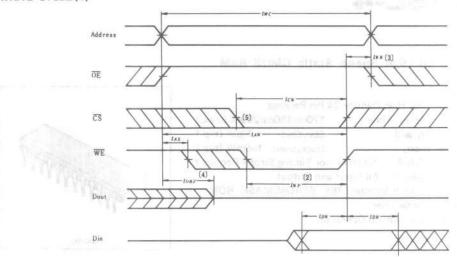
NOTES: 1. WE is High for Read Cycle.

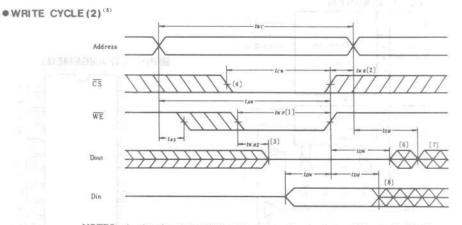
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low.

**OHITACHI** 

4.  $\overline{OE} = V_{IL}$ .







NOTES: 1. A write occurs during the overlap (t<sub>WP</sub>) of a low CS and a low WE.
2. t<sub>WR</sub> is measured from the earlier of CS or WE going high to the end of write cycle.

During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.

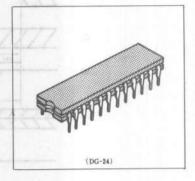
- 5. OE is continuously low. ( $\overline{OE} = V_{IL}$ ) 6. Dout is the same phase of write data of this write cycle. 7. D<sub>out</sub> is the read data of next address. 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

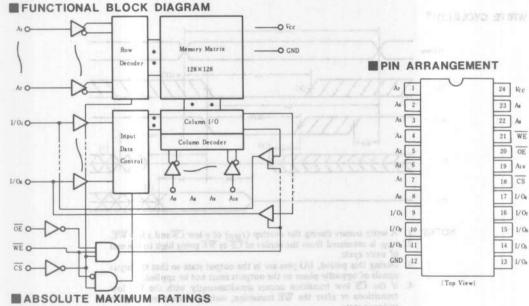
## HM6116L-2, HM6116L-3, HM6116L-4

2048-word×8-bit High Speed Static CMOS RAM

#### FEATURES

- Single 5V Supply and High Density 24 Pin Package
- 120ns/150ns/200ns (max.) High Speed: Fast Access Time Standby: 20µW (typ.) Low Power Standby and Operation: 160mW (typ.)
- Low Power Operation;
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation





#### Item Symbol Rating Unit VT -0.5\* to +7.0 V Voltage on Any Pin Relative to GND **Operating** Temperature Terr 0 to +70°C -65 to +150 °C Storage Temperature Tree Temperature Under Bias Think -10 to +85 °C Power Dissipation $P_T$ 1.0 W

\* Pulse Width 50ns : -1.5V

#### TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	Iso, Isoi	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)



#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
tan lin te-	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	v
	VIII	2.2	3.5	6.0	v
Input Voltage	VIL	-1.0*		0.8	V

Pulse Width: 50ns, DC: V/L min = -0.3V

#### DC AND OPERATING CHARACTERISTICS (Vcc=5V ±10%, GND=0V, Ta=0 to +70°C)

		Trat Conditions		6116L/F	2-2	HM6	116L/P-	3/-4	11.24
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	ILI	Vcc=5.5V, Vix=GND to Vcc	+	-	2	-	-	2	μA
Output Leakage Current	110	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I/0} = \text{GND to } V_{CC}$			2	-	-	2	μA
Oceanting Bound Supplu	Icc	$\overline{\mathrm{CS}} = V_{IL}, \ I_{I/0} = 0 \mathrm{mA}$		35	70		30	60	mA
Operating Power Supply Current	Icc1**	$V_{IN} = 3.5 V, V_{\ell L} = 0.6 V, I_{1 \neq 0} = 0 \text{mA}$	at the	30	-	-	25	-	mA
Average Operating Current	Icc :	min. cycle, duty=100%	-	35	70	-	30	60	mA
	Isb	$\overline{CS} = V_{IH}$	-	4	12	-	4	12	mA
Standby Power Supply Current	Ismi	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \ V_{is} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{is} \le 0.2 \text{V}$	-	4	100	-	4	100	μA
	Vol	101-4mA	-	-	0.4	-		-	v
Output Voltage	VOL	Io1=2.1mA	-	-		-	-	0.4	V
	VOH	<i>Iон</i> = -1.0mA	2.4	-	-	2.4	- 12		V

\* : Vcc=5V, Ta=25°C

\* \* : Reference Only

#### AC CHARACTERISTICS (Vcc=5V ±10%, Ta=0 to +70°C)

#### **e**AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns Input and Output Timing Reference Levels: 1.5V Output Load: 1TTL Gate and  $C_L$  = 100pF (including scope and jig)

#### READ CYCLE

Item	C. L.I	HM6116L-2		HM6116L-3		HM6116L-4		Unit	
item	Symbol	min	max	min	max	min	max	Unit	
Read Cycle Time	LRC	120	-	150	—	200	-	ns	
Address Access Time	LAA		120	-	150	-	200	ns	
Chip Select Access Time	LACS	1.7.7	120		150	-	200	ns	
Chip Selection to Output in Low Z	telz	10		15		15	-	n5	
Output Enable to Output Valid	tor	-	80	-	100	-	120	ns	
Output Enable to Output in Low Z	toiz	10	-	15	-	15	-	ns	
Chip deselection to Output in High Z	tenz	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	ton	10	-	15	-	15	-	ns	

store a long to the state of the state

CHARLEN AND AND ADDRESS AND ADDRESS AND ADDRESS ADDRES

second states contraction to or anti- print have pri-

ALC: NO. 1



#### HM6116L-2,HM6116L-3,HM6116L-4

#### **WRITE CYCLE**

1 July 184	Contat	HM61	16L-2	HM6116L-3		HM 61	16L-4	Unit	
Item	Symbol	min	max	min	max	min	max	Omt	
Write Cycle Time	twc	120	-	150	-	200	-	ns	
Chip Selection to End of Write	tew	70	-	90	-	120	_	ns	
Address Valid to End of Write	l AW	105		120	-	140	-	ns	
Address Set Up Time	tas	20	-	20	-	20		ns	
Write Pulse Width	twr	70	-	90		120	1.200	ns	
Write Recovery Time	twa	5	2.5.00	10	CATIO	10	0.000	ns	
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Write to Output in High Z	l whz	0	50	0	60	0	60	ns	
Data to Write Time Overlap	tow	35	-	40	-	60	-	ns	
Data Hold from Write Time	t DH	5	at ()=)	10	al - Var	10	1000 TTO 40	ns	
Output Active from End of Write	tow	5		10	25-	10	-	ns	

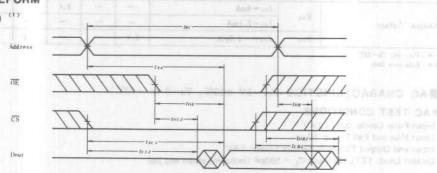
#### **CAPACITANCE** (f=1MHz, Ta=25°C)

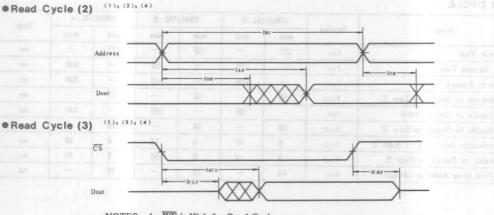
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cia	V0V	seb elses a 3	5	pF
Input/Output Capacitance	C1+0	$V_{I,e0} = 0V$	5	7	pF

Note) This parameter is sampled and not 100% tested.

TIMING WAVEFORM

•Read Cycle (1) (1)



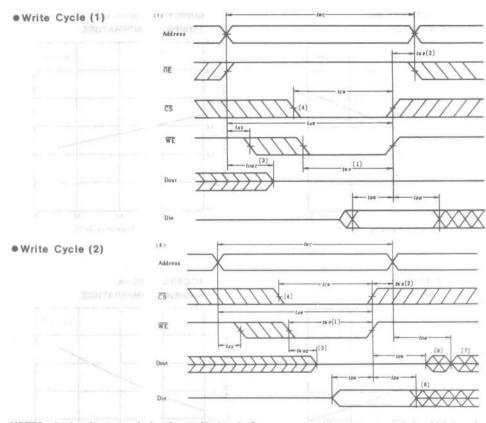


NOTES: 1. WE is High for Read Cycle.

- Device is continuously selected, CS = V<sub>IL</sub>.
   Address Valid prior to or coincident with CS transition Low.

**OHITACHI** 

4.  $\overline{OE} = V_{IL}$ .



NOTES: 1. A write occurs during the overlap  $(t_{WP})$  of a low CS and a low WE.

- 2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$ going high to the end of write cycle.3. During this period, I/O pins are in the output
- state so that the input signals of opposite
- state so that the input signals of opposite phase to the outputs must not be applied. 4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$

transition, output remain in a high impedance state.

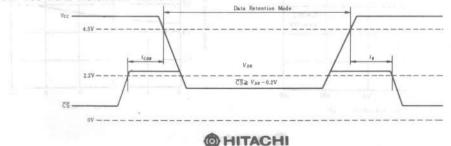
- 5.  $\overline{OE}$  is continuously low.  $(\overline{OE} = V_{IL})$ 6. D<sub>out</sub> is the same phase of write data of this write cycle.
- D<sub>out</sub> is the read data of next address.
   If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

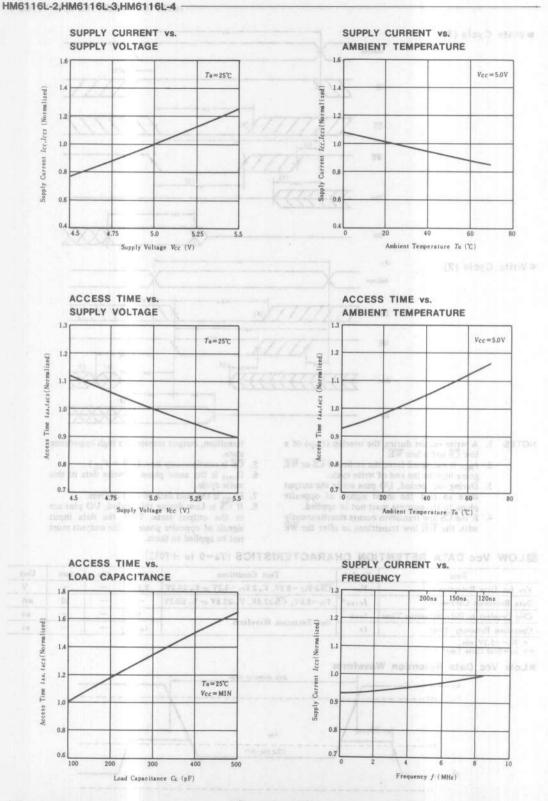
#### **LOW Vcc DATA RETENTION CHARACTERISTICS** (Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, V_{is} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{is} \le 0.2 \text{V}$	2.0		-	V
Data Retention Current	ICCDR*	$V_{cc} = 3.0 \text{ V}, \ \overline{\text{CS}} \ge 2.8 \text{ V}, \ V_{is} \ge 2.8 \text{ V} \text{ or } V_{is} \le 0.2 \text{ V}$	-		50	μA
Chip Deselect to Data Retention Time	tcon	C. D W. /	0		19 <u>-</u> 1	ns
Operation Recovery Time	t n	See Retention Waveform		-	-	ns

\* V<sub>11</sub>=-0.3V min.
\*\* t<sub>RC</sub>=Read Cycle Time.

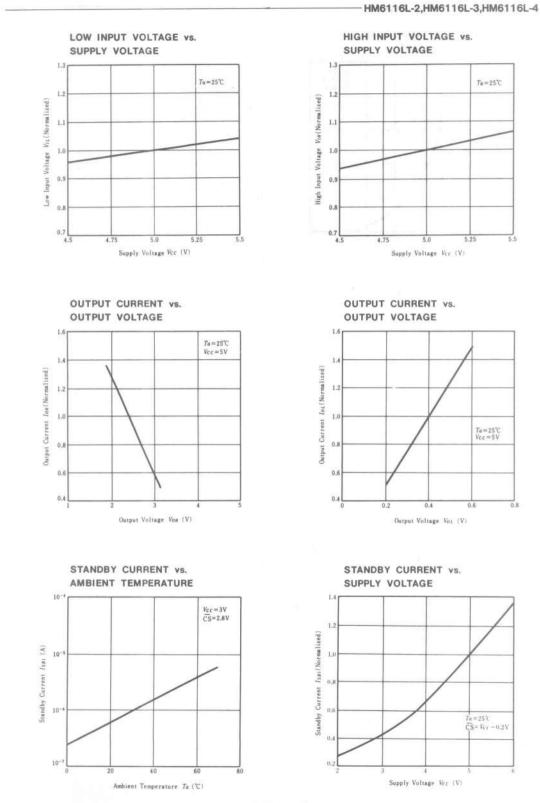
#### Low Vcc Data Retention Waveform





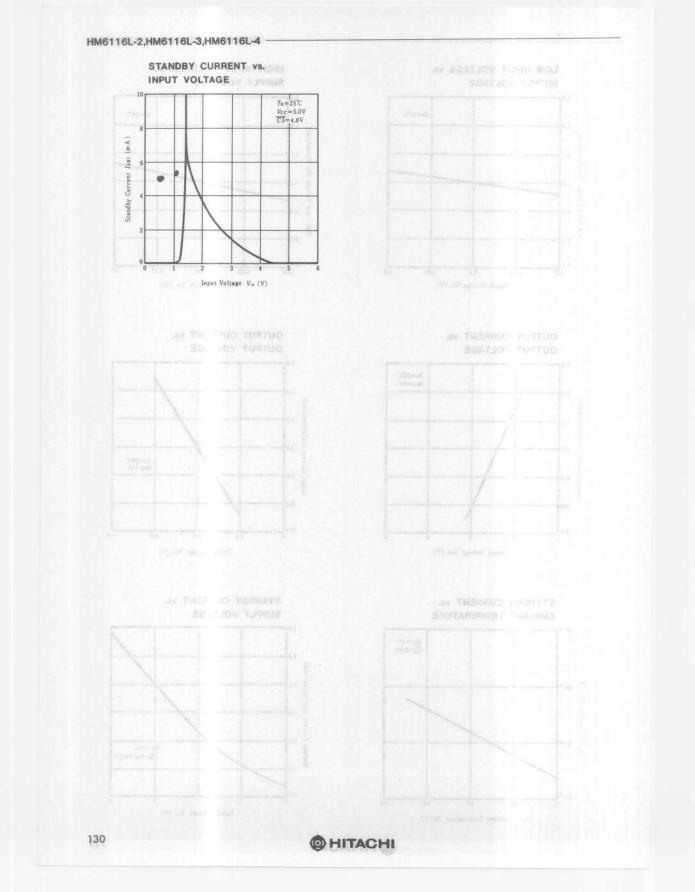
**HITACHI** 

128



**HITACHI** 

129



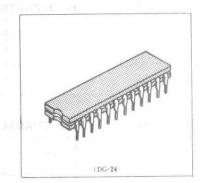
## HM6116LI-2, HM6116LI-3, HM6116LI-4 — Wide Operating Temperature Range –

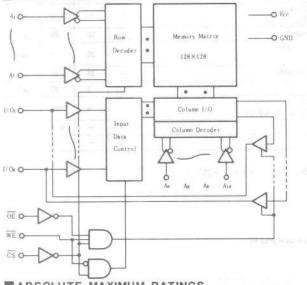
2048-word×8-bit High Speed Static CMOS RAM

#### FEATURES

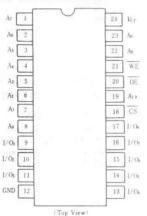
- Wide Operating Temperature Range ..... -40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 20μW (typ.)
   Low Power Operation; Operation: 160m W (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

FUNCTIONAL BLOCK DIAGRAM





## PIN ARRANGEMENT



#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	$V\tau$	-0.5* to +7.0	V
Operating Temperature	Topr	-40 to +85	*C
Storage Temperature	Tre	-65 to +150	°C
Power Dissipation	Pτ	1.0	W

\* Pulse Width 50ns : - 1.5 V

#### HM6116LI-2, HM6116LI-3, HM6116LI-4-

#### TRUTH TABLE

CS	OE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	Is8, Is81	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

### **RECOMMENDED DC OPERATING CONDITIONS** (*Ta* = -40 to +85°C)

Item	Symbol	min	typ	max	Unit	
Supply Voltage	Vcc	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input Voltage	VIH	2.2	3.5	6.0	V	
	VIL	-1.0*	his structs and	0.8	V	

Pulse Width: 50ns, DC: V/1 min = -0.3V

TLCCOLOMBING WHEN

#### **DC AND OPERATING CHARACTERISTICS** (Vcc=5V ±10%, GND=0V, Ta=-40 to +85°C)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input Leakage Current	141	$V_{cc} = 5.5$ V, $V_{is} = $ GND to $V_{cc}$	DIAGRAM	X041.	a =A	2	μA
Output Leakage Current	ILO	$\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH},$ $V_{I < 0} = \text{GND to } V_{CC}$		-		2	μA
0	Ice	$\overline{CS} = V_{IL},  I_{I>0} = 0 \text{mA}$	could protect	-	35	90	mA
Operating Power Supply Current	Icci**	$V_{IN} = 3.5 V, V_{IL} = 0.6 V, I_{I,0} = 0 mA$	egivert		30	2	mA
Average Operating Current	Icer	min. cycle, duty=100%		-	35	90	mA
C 11 D C 1	Isa	$\overline{CS} = V_{IR}$	Tr al	15	4	20	mA
Standby Power Supply Current	[581	$ \overline{CS} \ge V_{cc} - 0.2V, \\ V_{cs} \ge V_{cc} - 0.2V \text{ or } V_{cs} \le 0.2V $		-	4	2 2 90  90 20 200	μA
0	Vol	101=2.1mA	to fire second	1000	-	0.4	V
Output Voltage	Von	Ion = -1.0mA		2.4	- 1	1 -	V

\* : Vcc-5V, Ta-25°C \*\* : Reference Only

#### **AC CHARACTERISTICS** ( $V_{cc} = 5V \pm 10\%$ , Ta = -40 to $+85^{\circ}C$ )

#### **AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 \text{pF}$  (including scope and jig)

#### **READ CYCLE**

the second second	6.11	HM6116L1-2		HM6116L1-3		HM6116L.I-4		11-14	
Item	Symbol	min	max	mín	max	min	max	Unit	
Read Cycle Time	trc	120	1000	150	9 - G	200	-	ns	
Address Access Time	Las	3 <del>-</del> 3	120	-	150	-	200	ns	
Chip Select Access Time	lacs		120	-	150	-	200	ns	
Chip Selection to Output in Low Z	ters	10		10	1 -1	10		ns	
Output Enable to Output Valid	tor	-	80	-	100	-	120	ns	
Output Enable to Output in Low Z	torz	10	-	10	-	10	-	ns	
Chip deselection to Output in High Z	tenz	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	ton	10	-	10	-	10	-	ns	

#### **WRITE CYCLE**

1	C. L.I	HM61	16L1-2	HM6116L1-3		HM6116LI-4		Unit	
Item	Symbol	min	max	min	max	min	max	Unit	
Write Cycle Time	twc	120	-	150	-	200	-	ns	
Chip Selection to End of Write	t cw	70	-	90	-	120	-	ns	
Address Valid to End of Write	Law	105	-1.0	120	1 1 1 1 1 1 1	140	-	ns	
Address Set Up Time	tas	20	-	20		20		ns	
Write Pulse Width	Lwr	70		90	-	120	-	n5	
Write Recovery Time	twn	5	-	10	-	10		ns	
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Write to Output in High Z	twnz	0	50	0	60	0	60	ns	
Data to Write Time Overlap	tow	35	-	40		60		ns	
Data Hold from Write Time	t DH	5		10	100	10	-	ns	
Output Active from End of Write	tow	5	-	10		10	-	ns	

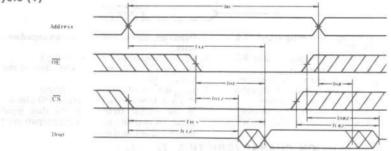
#### **CAPACITANCE** (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,.	V., = 0V	3	5	pF
Input/Output Capacitance	C1/0	V1.0-0V	5	7	pF

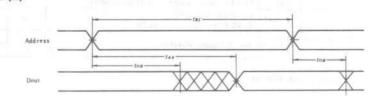
Note) This parameter is sampled and not 100% tested.

### TIMING WAVEFORM

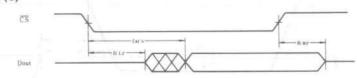
### • Read Cycle (1) (1), (5)



(1), (2), (4) •Read Cycle (2)



(1), (3), (4) Read Cycle (3)

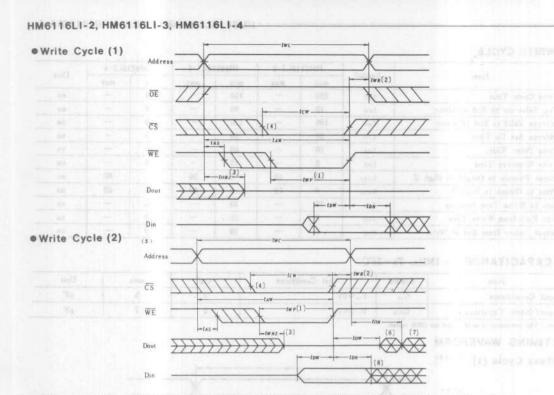


NOTES: 1. WE is High for Read Cycle.

2. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low.

4.  $\overline{OE} = V_{IL}$ .





- NOTES: 1. A write occurs during the overlap  $(t_{WP})$  of a low CS and a low WE.
  - 2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$ going high to the end of write cycle.
  - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  - 4. If the CS low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$

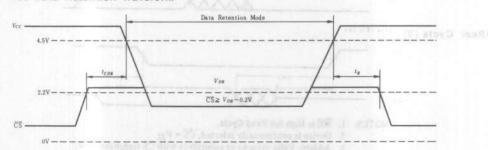
transition, output remain in a high impedance state.

- 5.  $\overline{OE}$  is continuously low. ( $\overline{OE} = V_{II}$ )
- 6. Dout is the same phase of write data of this write cycle.
- D<sub>out</sub> is the read data of next address.
   If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=-40 to +85°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{CS} \ge V_{cc} - 0.2V, V_{**} \ge V_{cc} - 0.2V \text{ or } V_{**} \le 0.2V$	2.0		-	V
Data Retention Current	Iccox*	$V_{cc} = 3.0V, \ \overline{CS} \ge 2.8V, V_{.*} \le 2.8V \text{ or } -0.3V \le V_{.*} \le 0.2V$	-		100	μA
Chip Deselect to Data Retention Time	tcos	6 D W	0	-	-	ns
Operation Recovery Time	1 R	See Retention Waveform	tac**	-	-	ns

Low Vcc Data Retention Waveform

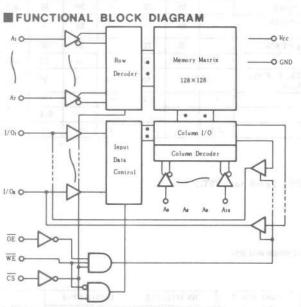


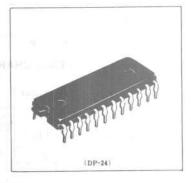
## HM6116LP-2, HM6116LP-3, HM6116LP-4

#### 2048-word×8-bit High Speed Static CMOS RAM

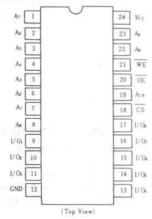
#### FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
   Low Power Standby and Standby: 10μW (typ.)
- Low Power Operation; Operation: 160mW (typ.) Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation





#### PIN ARRANGEMENT



#### BABSOLUTE MAXIMUM RATINGS

ltem	Symbol	Rating	Unit	
Voltage on Any Pin Relative to GND	V7	-0.5° to +7.0	V	
Operating Temperature	Ter.	0 to +70	°C	
Storage Temperature	Tere	-55 to +125	°C	
Temperature Under Bias	T	-10 to +85	°C	
Power Dissipation	Pr	1.0	W	

\* Pulse Width 50ns : -1.5V

### TRUTH TABLE

CS	ŌE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	Iso, Ison	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L ·	L	Write	Icc	Din	Write Cycle (2)



#### HM6116LP-2,HM6116LP-3,HM6116LP-4 ----

RECOMMENDED DC OFERATING CONDITIONO IN TO FOOT	RECOMMENDED DC	OPERATING	CONDITIONS	$(Ta=0 \text{ to } +70^{\circ}\text{C})$	
--	----------------	-----------	------------	--	--

Item	Symbol	min	typ	max	Unit	
Supply Voltage	Vee	4.5	5.0	5.5	V	
	GND	0	0	0	v	
Input Voltage	VIII	2.2	3.5	6.0	V	
	VIL	-1.0*	igh Denny 24	0.8	v	

Pulse Width: 50ns, DC: V/L min = -0.3V

#### **DC AND OPERATING CHARACTERISTICS** (Vcc-5V ±10%, GND-0V, Ta-0 to +70°C)

TAL STREETS		Ing Strong Required and	H	46116LP	-2	HM	6116LP-3	/-4	Unit
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit
Input Leakage Current	1101	$V_{cc}$ =5.5V, $V_{in}$ =GND to $V_{cc}$	12	or pra	2	- ·	1000200	2	μA
Output Leakage Current	110	$\overline{\text{CS}} = V_{IN} \text{ or } \overline{\text{OE}} = V_{IN}, \\ V_{I=0} = \text{GND to } V_{CC}$		Dante gG	2	-	nes Tra	2	μA
Operating Power Supply Current Vin	Icc	$\overline{CS} = V_{IL},  I_{I=0} = 0 \text{mA}$	-	35	70	-	30	60	mA
	$V_{IN} = 3.5V, V_{IL} = 0.6V, I_{I-0} = 0 \text{mA}$		30		-	25	-	mA	
Average Operating Current	Ice :	min. cycle, duty = 100%	-	35	70	-	30	60	mA
0. IL D. C. I	Isa	$\overline{CS} = V_{IH}$ and $O$		4	12		4	12	mA
Standby Power Supply	Ism	$\overline{CS} \ge V_{CC} - 0.2V, \ V_{i*} \ge V_{CC} - 0.2V \text{ or } V_{i*} \le 0.2V$	- 1	2	50	-	2	50	μA
2 2		Iot=4mA	-	-	0.4	-	- 30	-	0.0
Output Voltage	Vol	Io1=2.1mA	-	-	-		-	0.4	v
	Von	<i>I</i> on = -1.0mA	2.4		-	2.4	+1	-	v

≇ : Vec=5V, Ta=25℃

\* \* : Reference Only

### AC CHARACTERISTICS (Vcc=5V ±10%, Ta=0 to +70°C)

#### **•**AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

#### **READ CYCLE**

	0.11	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit	
Item	Symbol	min	max	min	max	min	max	12 Child	
Read Cycle Time	LAC	120	Tatles	150	-	200		ns	
Address Access Time	taa		120		150	at settisted	200	ns	
Chip Select Access Time	tacs	-11-	120	11	150	-	200	ns	
Chip Selection to Output in Low Z	lerz	10	42 <u>21</u> -	15	-	15		ns	
Output Enable to Output Valid	tor		80		100	-	120	ns	
Output Enable to Output in Low Z	torz	10	-	15		15		ns	
Chip Deselection to Output in High Z	lenz	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	ton	10	-	15	-	15	-	ns	

#### **WRITE CYCLE**

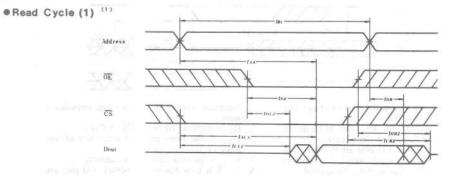
Terror Control of Cont	6 1.1	HM611	6LP-2	HM61	16LP-3	HM6116LP-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120		150		200	-	ns
Chip Selection to End of Write	tew	70	-	90		120	-	ns
Address Valid to End of Write	taw	105	-	120	-	140		ns
Address Set Up Time	tas	20	-	20	-	20	-	n5
Write Pulse Width	twp	70	1 C - C	90		120	-	ns
Write Recovery Time	twa	5	-	10	-	10	-	n5
Output Disable to Output in High Z	LOHZ	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	-	40		60	-	ns
Data Hold from Write Time	t DH	5		10	<u></u>	10	-	ns
Output Active from End of Write	tow	5		10	-	10	-	ns

### **CAPACITANCE** (f=1MHz, Ta=25°C)

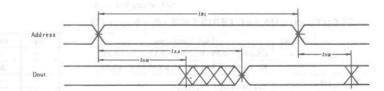
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	V0V	3	5	pF
Input/Output Capacitance	C1 o	$V_{I} = 0V$	5	7	pF

Note) This parameter is sampled and not 100% tested.

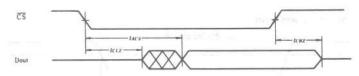
#### TIMING WAVEFORM



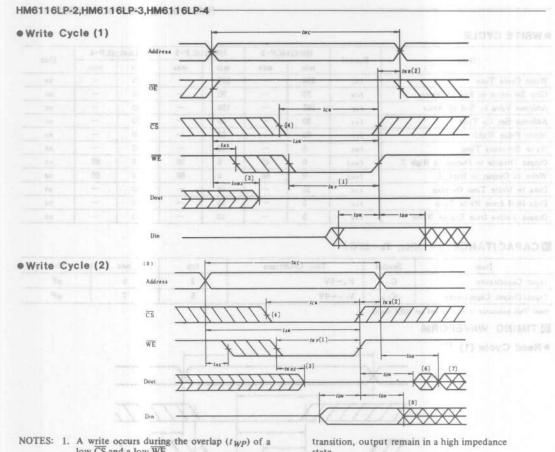
## •Read Cycle (2) (1), (2), (4)



Read Cycle (3) (1), (3), (4)



NOTES: 1. WE is High for Read Cycle.
2. Device is continuously selected, CS = V<sub>IL</sub>.
3. Address Valid prior to or coincident with CS transition Low. 4.  $\overline{OE} = V_{IL}$ .



- low CS and a low WE.
  - 2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$ going high to the end of write cycle.
  - 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  - 4. If the  $\overline{\text{CS}}$  low transition occurs simultaneously with the WE low transitions or after the WE

state.

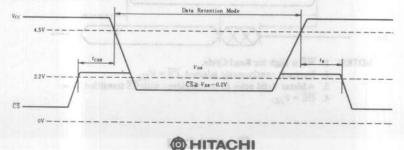
- 5.  $\overline{OE}$  is continuously low.  $\overline{OE} = V_{IL}$ ) 6. D<sub>out</sub> is the same phase of write data of this write cycle.
- Dout is the read data of next address.
   If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

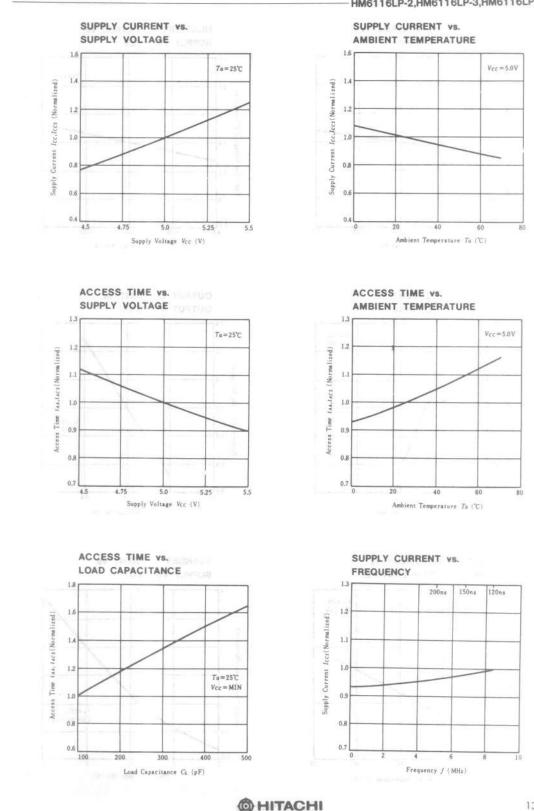
### LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	V.D.R	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \ V_{cc} \ge V_{cc} - 0.2 \text{V} \text{ or } V_{cc} \le 0.2 \text{V}$	2.0		-	V
Data Retention Current	Iccor*	$V_{cc} = 3.0 \text{V}, \ \overline{\text{CS}} \ge 2.8 \text{V}, \ V_{is} \ge 2.8 \text{V} \text{ or } V_{is} \le 0.2 \text{V}$	-		30	μA
Chip Deselect to Data Retention Time	lcon	C D	0	_	-	ns
Operation Recovery Time	t n	See Retention Waveform	tac**	-	-	ns

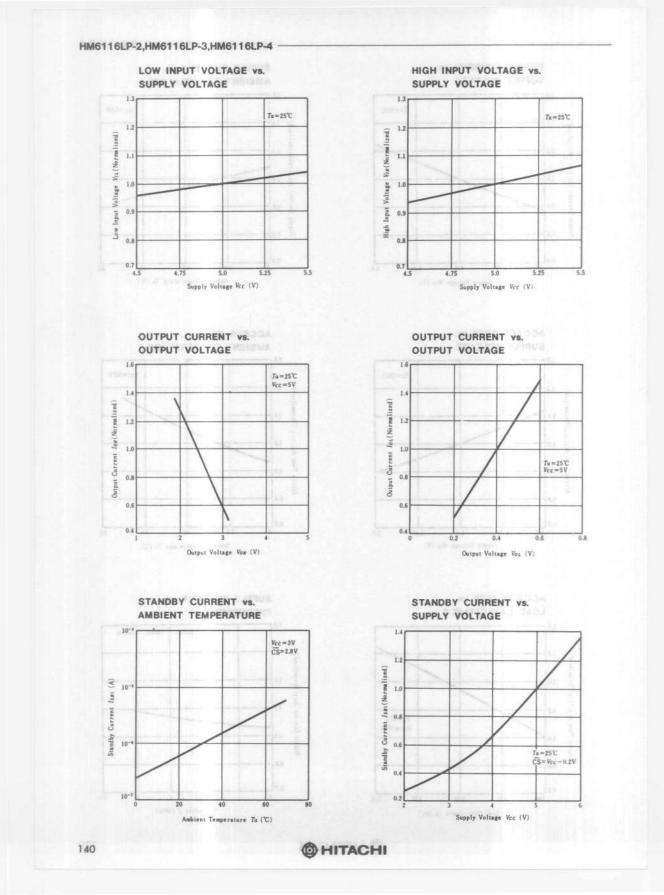
\*\* In: -Read Cycle Time.

#### Low Vcc Data Retention Waveform

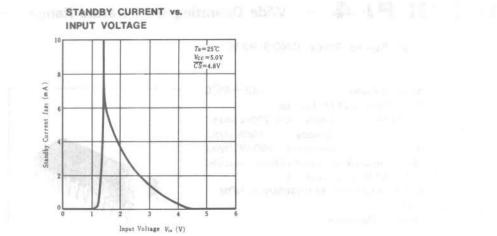




139









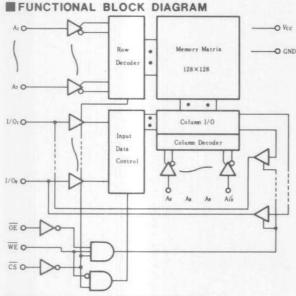


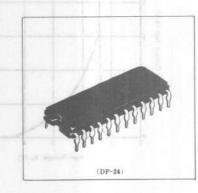
# HM6116LPI-2, HM6116LPI-3, HM6116LPI-4 — Wide Operating Temperature Range-

#### 2048-word×8-bit High Speed Static CMOS RAM

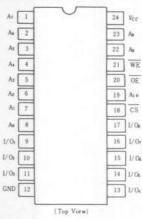
#### FEATURES

- Wide Operating Temperature Range ..... -40~+85°C
- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
   Low Power Standby and Standby: 10μW (typ.)
  - Low Power Operation; Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation





#### PIN ARRANGEMENT



#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	$V_T$	-0.5* to +7.0	V
Operating Temperature	Top.	-40 to +85	°C
Storage Temperature	Tele	-55 to +125	°C
Power Dissipation	PT	1.0	W

\* Pulse Width 50ns : -1.5 V

#### TRUTH TABLE

CS	OE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	Iso, Ison	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)

#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=-40 to +85°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
	Vin	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	- +	0.8	V

# Pulse Width: 50ns, DC: V/L min = -0.3V

#### ■ DC AND OPERATING CHARACTERISTICS (Vcc=5V ±10%, GND=0V, Ta=-40 to +85°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	ILt	Vcc=5.5V, V.s=GND to Vcc	-	-	2	μA
Output Leakage Current	120	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ , $V_{I+0} = GND$ to $V_{CC}$	-	- 77. V	2	μA
Operating Power Supply	Icc	$\overline{CS} = V_{IL},  I_{I/0} = 0 \text{mA}$		35	90	mA
Current	Ice1**	$V_{IH} = 3.5 V, V_{IL} = 0.6 V, I_{III} = 0 mA$	-	30		mA
Average Operating Current	Iccz	min. cycle, duty = 100%	-	35	90	mA
Standby Power Supply	I 5.8	$\overline{CS} = V_{IH}$		4	20	mA
Current	1 5.81	$\overline{\text{CS}} \ge V_{cc}$ -0.2V, $V_{is} \ge V_{cc}$ -0.2V or $V_{is} \le 0.2$ V	-	2	100	μA
Output Voltage	Vol	<i>Iot</i> = 2.1mA	-	-	0.4	V
Output voltage	Von	$I_{oH} = -1.0 \text{mA}$	2.4	_	-	V

\* : Vec=5V, Ta=25°C

\* \* : Reference Only

#### AC CHARACTERISTICS (Vcc=5V ±10%, Ta=-40 to +85°C)

#### **OAC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns Input and Output Timing Reference Levels: 1.5V Output Load: 1TTL Gate and  $C_L$  = 100pF (including scope and jig)

#### READ CYCLE

Item	Suchal	HM61	16LPI-2	HM6116LPI-3		HM6116LPI-4			
rtem	Symbol	min	max	min	max	min	max	Unit	
Read Cycle Time	trc	120	-	150	-	200		ns	
Address Access Time	- LAA	-	120	-	150	-	200	ns	
Chip Select Access Time	LACS	-	120	-	150	-	200	ns	
Chip Selection to Output in Low Z	leiz	10	-	10	-	10	-	ns	
Output Enable to Output Valid	toz	-	80		100	-	120	ns	
Output Enable to Output in Low Z	tors	10	-	10	-	10		ns	
Chip Deselection to Output in High Z	t c H Z	0	40	0	50	0	60	ns	
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns	
Output Hold from Address Change	ton	10	-	10	- T -	10	-	ns	



#### HM6116LPI-2,HM6116LPI-3,HM6116LPI-4 -

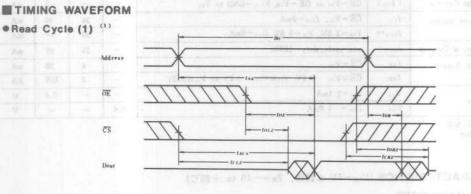
#### **WRITE CYCLE**

sheet Left Item	Symbol	HM61	16LP1-2	HM61	16LPI-3	HM61	HM6116LPI-4	
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	-	150	-	200	-	ns
Chip Selection to End of Write	tcw	70	-	90	-	120	1	n5
Address Valid to End of Write	LAW	105	-	120	-	140	-	ns
Address Set Up Time	tas	20	-	20	-	20	-	ns
Write Pulse Width	twp	70	TITIAN	90	ANTRO	120	1.71	ns
Write Recovery Time	twa	5	-	10		10	-	ns
Output Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Write to Output in High Z	twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	Low	35	1 - 0	40	-	60	-	ns
Data Hold from Write Time	ton	5	-	10	-	10	-	ns
Output Active from End of Write	Low	5	-	10	-	10	-	ns

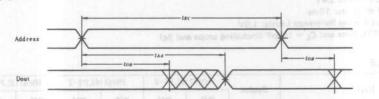
#### **CAPACITANCE** (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	V0V	3	5	pF
Input/Output Capacitance	C1-0	$V_{I \sim 0} = 0 V$	5	7	pF

Note) This parameter is sampled and not 100% tested.



• Read Cycle (2) (1), (2), (4)

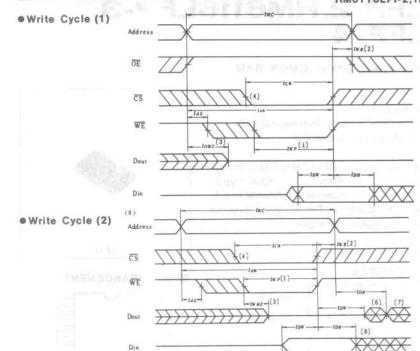


**OHITACHI** 

• Read Cycle (3) (1), (3), (4)

CS.	
Dout	
NC	TES: 1. WE is High for Read Cycle.
	<ol> <li>Device is continuously selected, CS = V<sub>IL</sub>.</li> <li>Address Valid prior to or coincident with CS transition Low.</li> </ol>

4.  $\overline{OE} = V_{IL}$ .



NOTES: 1. A write occurs during the overlap  $(t_{WP})$  of a low  $\overline{\text{CS}}$  and a low  $\overline{\text{WE}}$ .

- 2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$
- going high to the end of write cycle. 3. During this period, 1/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$

transition, output remain in a high impedance state.

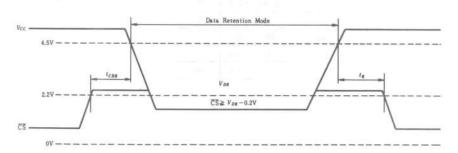
- 5.  $\overline{OE}$  is continuously low.  $\overline{OE} = V_{IL}$ ) 6. Dout is the same phase of write data of this write cycle.
- D<sub>out</sub> is the read data of next address.
   If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

LOW Vcc DATA	RETENTION	CHARACT	ERISTICS	(Ta = -40)	to +85°C)
--------------	-----------	---------	----------	------------	-----------

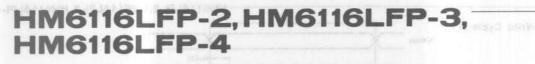
Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{CS} \ge V_{cc} - 0.2V, V_{.*} \ge V_{cc} - 0.2V \text{ or } V_{.*} \le 0.2V$	2.0	-	-	V
Data Retention Current	Iccos*	$V_{cc} = 3.0 \text{V}, \ \overline{\text{CS}} \ge 2.8 \text{V}, V_{cc} \ge 2.8 \text{V}, \text{ or } -0.3 \text{V} \le V_{cc} \le 0.2 \text{V}$	-	-	50	μA
Chip Deselect to Data Retention Time	tcor	C. D	0	-	-	ns
Operation Recovery Time	t n	See Retention Waveform	I RC **	-		ns

\* 10 µA max at Ta--40°C to +40°C V<sub>11</sub> min=-0.3V \*\* tsc-Read Cycle Time.

Low Vcc Data Retention Waveform



C HITACHI



2048-word×8-bit High Speed Static CMOS RAM

# FEATURES

- High Density Small-sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time
  Low Power Standby and

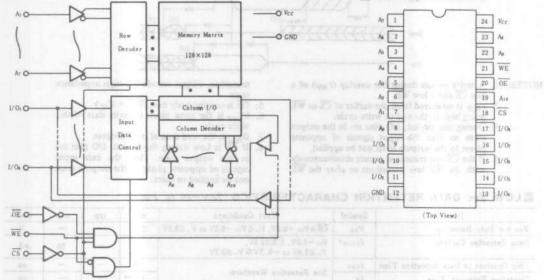
Low Power Operation;

- 120ns/150ns/200ns (max.) Standby: 10μW (typ.)
- Operation: 160mW (typ.)
- Completely Static RAM: No Clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation



#### PIN ARRANGEMENT

(FP-24)



#### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vτ	-0.5*to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tele	-55 to +125	"C
Temperature Under Bias	Thias	-10 to +85	°C
Power Dissipation	PT	1.0	W

Low Voo, Gale Hatension Waveform

\* V<sub>IN</sub> min = -1.5V (Pulse Width ≤ 50ns)

**OHITACHI** 

# TRUTH TABLE

CS	ŌE	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, ISB1	High Z	
L	- L 602	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	- H 031	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc Icc	Din	Write Cycle (2)

#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Secolar Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
	VIH	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	-	0.8	V

₱ Pulse Width: 50ns, DC: Vn, min=-0.3V.

#### **DC AND OPERATING CHARACTERISTICS** (Vcc=5V±10%, GND=0V, Ta=0 to +70°C)

	0.11	The Contraction	HM	46116LF	P-2	HM	HM6116LFP-3/-4			
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	Unit	
Input Leakage Current	ILI	Vcc=5.5V, V.,=GND to Vcc	-	-	2	-	-	2	μA	
Output Leakage Currnnt	IL0	$\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH},$ $V_{I=0} = \text{GND to } V_{CC}$	-	-	2	1-1	-	2	μÅ	
O	Icc	$\overline{CS} = V_{IL}, I_{I=0} = 0 \text{mA}$		35	70		30	60	mA	
Operating Power Supply Current	<i>Icc</i> 1**	$V_{IH} = 3.5 V, V_{IL} = 0.6 V,$ $I_{I_0} = 0 m A$	-	30	-	-	25	1	mA	
Average Operating Current	Icci	Min cycle, duty=100%	-	35	70	-	30	60	mA	
	Isa	$\overline{CS} = V_{IH}$	-	4	12	-	4	12	mA	
Standby Power Supply Current	Isai	$\overline{CS} \ge V_{CC} - 0.2V,  V_{in} \ge V_{CC}$ $-0.2V \text{ or } V_{in} \le 0.2V$	1.4	2	50	-	2	50	μA	
	17	Iot-4mA	-	-	0.4		-			
Output Voltage	VoL	$I_{OL} = 2.1 \text{mA}$	-				-	0.4	V	
	Vor	$I_{OH} = -1.0 \text{mA}$	2.4	-	_	2.4	_		V	

♦ : Vcc−5V, Ta−25'C

# # : Reference Only

# **AC CHARACTERISTICS** (Vcc=5V±10%, Ta=0 to +70°C)

# **OAC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L$  = 100pF (including scope and jig)

#### ●READ CYCLE

Item	Symbol	HM611	6LFP-2	HM611	6LFP-3	HM6116LFP-4		11.0
item	Symool	min	max	min	max	min	max	Unit
Read Cycle Time	1 RC	120	-	150	-	200		ns
Address Access Time	Lax.	- )	120	-	150		200	ns
Chip Select Access Time	lacs		120	-	150	-	200	ns
Chip Selection to Output in Low Z	terz	10	Date II sol	15	1 - 1	15	-	ns
Output Enable to Output Valid	tor	Date of the	80	2020	100	-	120	ns
Output Enable to Output in Low Z	lorz	10	2	15		15	-	ns
Chip deselection to Output in High Z	t <sub>cHZ</sub>	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	tonz	0	40	0	50	0	60	ns
Output Hold from Address Change	t.on	10	-	15	-	15	-	ns



#### HM6116LFP-2,HM6116LFP-3,HM6116LFP-4 -

#### **WRITE CYCLE**

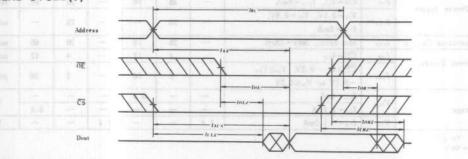
Item	0.11	HM611	6LFP-2	HM611	6LFP-3	HM6116LFP-4		Unit
Item	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	twc	120	-345	150		200	-	ns
Chip Selection to End of Write	tcw	70	-sin	90	-	120	-	ns
Address Valid to End of Write	taw	105	-211	120	-	140	-	ns
Address Set Up Time	tas	20	-	20	-	20	-	ns
Write Pulse Width	twp	70	19 min	90	neters	120	rice That	ns
Write Recovery Time	twa	5	-	10	-	10	-	ns
Output Disable to Output in High Z	Louz	0	40	0	50	0	60	ns
Write to Output in High Z	. twnz	0	50	0	60	0	60	ns
Data to Write Time Overlap	tow	35	- 18	40	-	60	-	ns
Data Hold from Write Time	ton	5	-	10	-	10		ns
Output Active from End of Write	tow	5	-	10	-	10	-	ns

#### **CAPACITANCE** (f-1MHz, Ta=25°C)

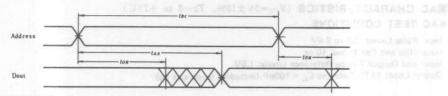
ltem	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	Vin=0V	3	5	pF
Input/Output Capacitance	C <sub>1</sub> o	$V_{I_0} = 0V$	5	7	pF

Note) This parameter is sampled and not 100% tested.

#### TIMING WAVEFORM •READ CYCLE(1)



# •READ CYCLE (3)(1)(3)(4)



#### •READ CYCLE (2)(1)(2)(4)

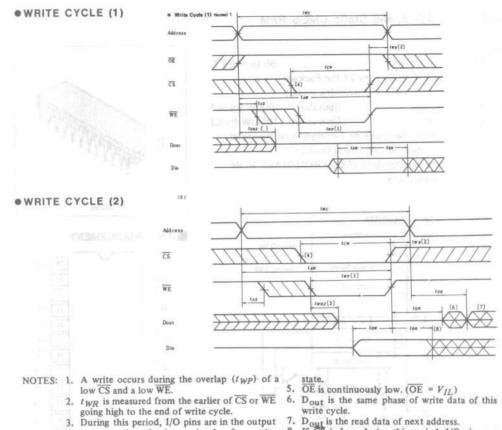
CS III	1	
	tacs	ti nz
Dout	luiz-	

NOTES: 1. WE is High for Read Cycle

- 2. Device is continuously selected,  $\overline{CS} = V_{IL}$ 3. Address Valid prior to or coincident with  $\overline{CS}$
- transition Low. 4.  $\overline{OE} = V_{IL}$ .

# **HITACHI**

#### HM6116LFP-2, HM6116LFP-3, HM6116LFP-4



- - buring this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied. while Cycle. 7. Dout is the read data of next address. 8. If CS is Low during this period, I/O pins are in the output state. Then the data input
- 4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$ transition, output remain in a high impedance

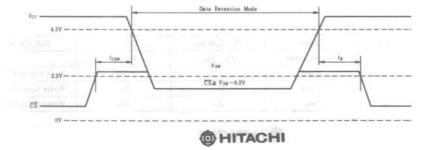
- signals of opposite phase to the outputs must not be applied to them.

<b>LOW Vcc DATA RETENTION CHARACTERISTICS</b> ( $Ta = 0$ to $+70$	LOW V	cc DATA	RETENTION	CHARACTERISTICS	(Ta=0 to	+70°C)
---	-------	---------	-----------	-----------------	----------	--------

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDR	$\overline{\text{CS}} \ge V_{cc} - 0.2\text{V}$ $V_{lN} \ge V_{cc} - 0.2\text{V or } V_{lN} \le 0.2\text{V}$	2.0	-	-	v
Data Retention Current	Iccon*	$V_{cc} = 3.0 \text{V}, \ \overline{\text{CS}} \ge 2.8 \text{V}$ $V_{lN} \ge 2.8 \text{V} \text{ or } V_{lN} \le 0.2 \text{V}$	-	-	30	μA
Chip Deselect to Data Retention Time	ICDR		0	-	-	ns
Operation Recovery Time	t <sub>R</sub>	- See Retention Waveform	**tRC	-		ns

\*  $V_{\ell \perp}$  min = -0.3V, 10  $\mu$ A max (at Ta=0 to +40°C) \* #  $t_{RC}$  = Read Cycle Time.

# **OLOW Vcc DATA RETENTION WAVEFORM**



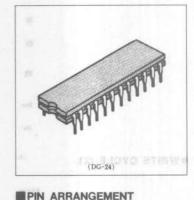
# HM6116K-3, HM6116K-4

2048-word × 8-bit High Speed Static CMOS RAM

#### FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (type.)
   Low Power Operation
   Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



#### -O Vec A: C Ar I 24 Vec Row Memory Matrix -O GND 23 A 2 Decode . 128×128 As At C 4 WE . . 20 0E 19 Ase Column 1/0 1/010 7 18 CS Input Column Decoder Data Ae 8 17 1/0. Control 1/01 9 16 1/07 1/0: 10 1/0.0 15 I/Os ó 1/01 11 A 14 1/05 A As An GND 12 13 1/0. OE O (Top View) WE SLOW V. DATA RETENTION CHARACTERISTICS (72-9 to + 79%) BARCOLUTE MAYIMUM DATINGS

ABSU	LUIE MAAIMUM RAI	INGS				
An	Item	Symbol	Rating	Unit	"hears"	Bros. Rel Milles Corcess
Voltage on	Any Pin Relative to GND	VT	-0.5* to +7.0	V	14423	
Operating	Temperature	Tapr	-55 to +125	°C	1	Operation Streets 11 th
Storage T	emperature	Tele	-65 to +150	°C	100	to as a with the same should be a marine of the
Power Dis	sipation	$P_T$	1.0	W		and Cycle Tree

\* Pulse Width 50ns : -1.5V

LOW YE DATA RETENTION WAVEFOR

#### TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	IsB, ISB1	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle(1)
L	L	L	Write	Icc	Din	Write Cycle(2)

**CHITACHI** 



-HM6116K-3, HM6116K-4

#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit	
	Vcc	4.5	5.0	5.5	V	
Supply Voltage	GND	0	0	0	v	
	VIN	2.2	3.5	6.0	v	
Input Voltage	VIL	-1.0*	_	0.8	v	

Pulse Width : 50ns, DC : Vit un=-0.3V

# DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, GND-0V, Ta=-55~+125°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	ILI	Vcc=5.5V, Via=GND to Vcc	-114		10	μA
Output Leakage Current	ILO	$\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH},$ $V_{I/0} = \text{GND to } V_{CC}$	an a	in the second	10	μA
	Icc	$\overline{\mathrm{CS}} = V_{IL_1}  I_{I \times 0} = 0 \mathrm{mA}$	-	35	90	mA
Operating Power Supply Current	<i>I</i> cc1**	$V_{IH} = 3.5 \text{V},  V_{IL} = 0.6 \text{V},$ $I_{I \neq 0} = 0 \text{mA}$	834-	30		mA
Average Operating Current	Iccz	Min. cycle, duty=100%	-	35	90	mA
	Isa	$\overline{CS} = V_{IH}$	-	4	20	mA
Standby Power Supply Current	I <sub>SB1</sub>	$CS \ge V_{cc} - 0.2V,  V_{is} \ge V_{cc}$ -0.2V or $V_{is} \le 0.2V$	-7.6	0.02	2	mA
0	Vol	IoL=2.1mA	-	(12.5	0.4	v
Output Voltage	VoH	I <sub>on</sub> =-1.0mA	2.4	-	-	V

\* Vcc-5V, Ta-25°C

#### \*\* Reference Only

# ■ AC CHARACTERISTICS (Vcc=5V±10%, Ta=-55 to +125°C)

# **AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 \text{pF}$  (including scope and jig)

### • READ CYCLE

Item	Symbol	HM61	16K-3	HM	6116K-4	Unit
Item	Symbol	min	max	mîn	max	Unit
Read Cycle Time	t RC	150	-	200	-	ns
Address Access Time	tAA		150	5	200	ns
Chip Select Access Time	tACS	7	150	-	200	ns
Chip Selection to Output in Low Z	telz	10	-	10		ns
Output Enable to Output Valid	t or	-	100	-	120	ns
Output Enable to Output in Low Z	tolz	10	-	10	LE (3)	ns
Chip Deselection to Output in High Z	t <sub>cHZ</sub>	0	50	0	60	ns
Chip Disable to Output in High Z	t ouz	0	50	0	60	ns
Output Hold from Address Change	t on	10		10	-	ns

Link M of Harth ( or M . 1 . 2.

Device di contratticitative enlocterit. C3

Address Vand melor tonic contraction to the Chevrolith I

**HITACHI** 

#### HM6116K-3,HM6116K-4

#### **WRITE CYCLE**

AL O ALAR DECIDING PARTIAL OF CARDENICS

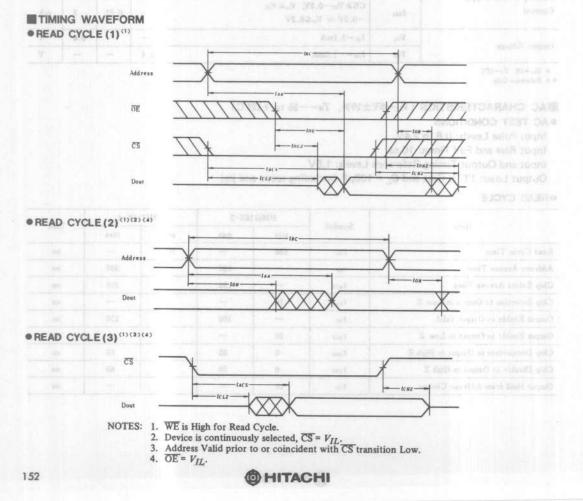
Item	Symbol	HM	5116K-3	HM61	16K-4	Unit
Item	Symbol	min	max	min	max	Unit
Write Cycle Time	twc	150	-	200		ns
Chip Selection to End of Write	tow	90		120	_	ns
Address Valid to End of Write	t AW	120	-	140	-	ns
Address Set Up Time	tAS	20		20	-	ns
Write Pulse Width	twp	90	-	120		ns
Write Recovery Time	twa	10	minimum	10	urra ann	ns
Output Disable to Output in High Z	tonz	0	50	0	60	ns
Write to Output in High Z	twhz	0	60	0	60	ns
Data to Write Time Overlap	tow	40	12.2-2	60	Current	ns
Data Hold from Write Time	t <sub>DH</sub>	10	1 (2 - 2 ) ( -	10	-	ns
Output Active from End of Write	tow	10	DD-12	10		ns

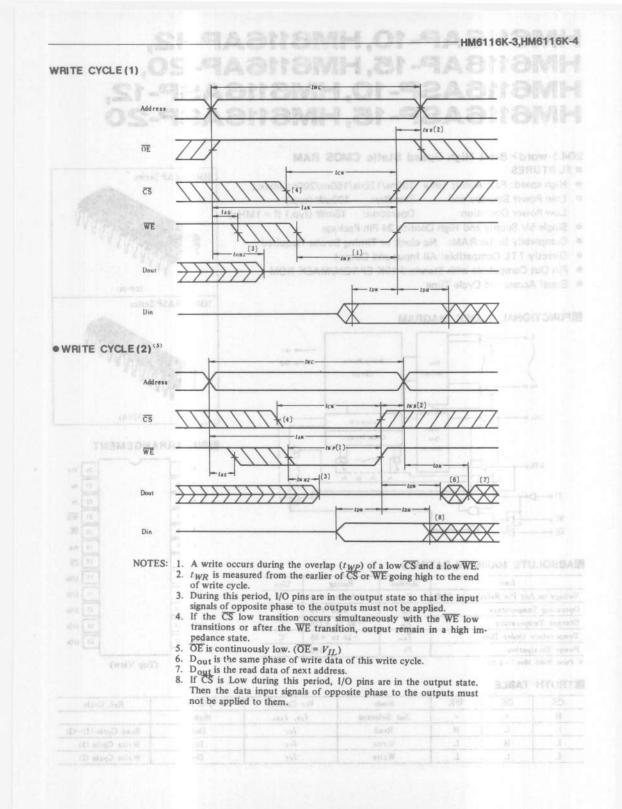
#### Kill - Kill - Bar - Bar

**CAPACITANCE** (f-1MHz, Ta-25°C)

COLORS, CRAMIT, THURSDAY,

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	V.,-0V	3	5	pF
Input/Output Capacitance	Cuo	V1.0-0V	5	7	pF



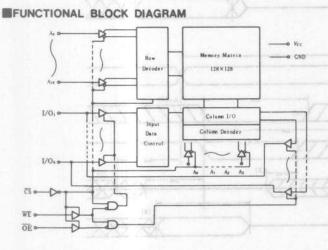


**HITACHI** 

# HM6116AP-10, HM6116AP-12, HM6116AP-15, HM6116AP-20, HM6116ASP-10, HM6116ASP-12, HM6116ASP-15, HM6116ASP-20

2048-word×8-bit High Speed Static CMOS RAM FURTURES

- High speed: Fast Access Time 100ns/120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 100µW (typ.) Low Power Operation Operation: 15mW (typ.) (f = 1MHz)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time



#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vr	-0.5° to +7.0	V
Operating Temperature	T.,,	0 to +70	°C
Storage Temperature	Trig	-55 to +125	.с
Temperature Under Bias	These	-10 to +85	ъ.
Power Dissipation	Pr	1.0	W

Pulse Width 50ns 1 -1.5%

# (DP-24) HM6116ASP Series Summun

(DP-24A)

HM6116AP Series

# PIN ARRANGEMENT

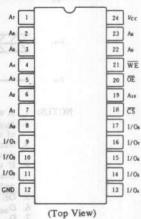
A

A.

Az

A

1/0



#### a if C2 is Low dorting this period, 1/O give are in the TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	1/0 Pin	Ref. Cycle
Н	×	×	Not Selected	Iso, Iso:	High Z	
L	L	н	Read	lee	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	lee	Din	Write Cycle (2)



#### HM6116AP-10,HM6116AP-12,HM6116AP-15,HM6116AP-20 HM6116ASP-10,HM6116ASP-12,HM6116ASP-15,HM6116ASP-20

Item	Symbol	min	typ	max	Unit
apply Voltage	Vcc	4.5	5.0	5.5	v
	GND	0	0	0	v
120 - 120 - 01	Vin	2.2	3.5	6.0	V
Input Voltage	VIL	-1.0*	WAL +	0.8	v

### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

\* Pulse Width : 50ns, DC : Vit min = 0.3V

#### **DC AND OPERATING CHARACTERISTICS** (Vcc-5V±10%, GND-0V, Ta=0 to +70°C)

m . 02 [		m . c . m	HM6	116AP//	SP-10	HM6	116AP//	SP-12	HM6	116AP//	SP-15	HM6	116 AP//	SP-20	
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	min	typ*	max	min	typ*	max	- Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}$ =5.5V, $V_{in}$ =GND to $V_{CC}$		-	2		-	2	-	-	2	d an	(1947) 2) 2947	2	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I/O} = \text{GND to } V_{CC}$	-	-	2	-	-	2	(-=_h)	38	2	-12	MĀT	2	μA
Operating Power	Icc	$\overline{CS} = V_{IL}, I_{I/O} = 0 \text{mA}$ $V_{in} = V_{IH} \text{ or } V_{IL}$	-	5	15	NoT VI	5	15	Sym.	5	15	-	5	15	mA
Supply Current	Icci	$\frac{V_{IH}=V_{CC}, V_{IL}=0V,}{\overline{CS}=V_{IL},}$ $I_{I/O}=0\text{mA}, f=1\text{MHz}$	-	3	6	¥8.	3	6	0 67 8	3	6			6	mA
Average Operating Current	I <sub>CC2</sub>	min. cycle, duty=100%	-	40	70	-	35	60	-	25	45	1934	20	35	mA
Standby Power	ISB	CS= V <sub>IH</sub>	-	1	4	-	1	4	-	1	4		1	4	mA
Supply Current	ISBI	$\overrightarrow{\text{CS}} \ge V_{CC} - 0.2 \text{V}$		0.02	2		0.02	2		0.02	2	-	0.02	2	mA
	VOL	I <sub>OL</sub> =4mA	1	-	0.4	-	-	0.4	-	391	0.4	-	-	0.4	V
Output Voltage	V <sub>OH</sub>	<i>I<sub>OH</sub></i> =-1.0mA	2.4	-		2.4	-	-	2.4	-	-	2.4		-	v

\* Vcc=5V, Ta=25°C

## AC CHARACTERISTICS (Vcc=5V±10%, Ta=0 to +70°C)

#### AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

#### READ CYCLE

Item	Symbol		116AP/ P-10		116AP/ SP-12		116AP/ IP-15		116AP/ P-20	Unit
		min	max	min	max	min	max	min	max	Oun
Read Cycle Time	IRC	100	- 1-	120	-	150	-	200	-	ns
Address Access Time	1 <sub>AA</sub>	1. AV	100	-	120	-	150	-	200	ns
Chip Select Access Time	TACS	_*	100	-	120	-	150	-	200	ns
Chip Selection to Output in Low Z	t <sub>CLZ</sub>	10	-	10	-	10		10	-	ns
Output Enable to Output Valid	tOE	-	50		55		60		70	ns
Output Enable to Output in Low Z	tolz	10	-	10	-	10	20_	10	-	ns
Chip Deselection to Output in High Z	<sup>t</sup> CHZ	0	40	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	toHZ	0	40	0	40	0	50	0	60	ns
Output Hold from Address Change	t <sub>OH</sub>	10	XeV	10	-	15	T LOOP	20	-	ns

1. WE is High for Read Own

stances 20 driw tablindies to or solid Site V areas at



#### HM6116AP-10.HM6116AP-12.HM6116AP-15.HM6116AP-20 HM6116ASP-10,HM6116ASP-12,HM6116ASP-15,HM6116ASP-20

#### WRITE CYCLE

Item	Symbol		16AP/ P-10		16AP/ P-12		116AP/ P-15		16 AP/ P-20	Unit
A COM	Bymoor	min	max	min	max	min	max	min	max	Unit
Write Cycle Time	twc	100	-	120	-	150	-	200	-	ns
Chip Selection to End of Write	tcw	65	-	70	-	90	-	120	-	ns
Address Valid to End of Write	tAW	80	-	105	-	120	-	140	-	ns
Address Set Up Time	TAS	0	-	0	-	0	-	0		ns
Write Pulse Width	twp	60	-	70	-	80	-	100	-	ns
Write Recovery Time	TWR	0	ant N	0	1.000	0	h mail	0	1000	ns
Output Disable to Output in High Z	tOHZ	0	40	0	40	0	50	0	60	ns
Write to Output in High Z	twHZ	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	tDW	30	-	35	-	40	-	50	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	10th De	0	-	0	-	ns
Output Active from End of Write	tow	10	-	10	-	10	10-	10	-	ns

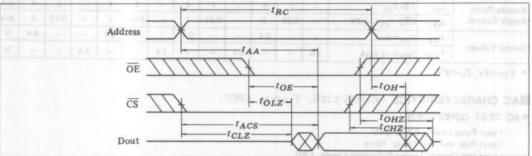
#### **CAPACITANCE** (f=1MHz, Ta=25°C)

CAPACITANCE (f=1MH	$z, Ta=25^{\circ}C$				
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	V0V	3	5	pF
Input/Output Capacitance	Cro	V1.0-0V	5	7	pF

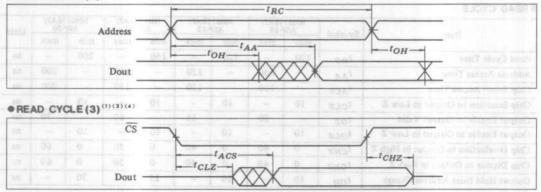
Note) This parameter is sampled and not 100% tested.

#### TIMING WAVEFORM

# • READ CYCLE (1) (1)



# • READ CYCLE (2) (1) (2) (4)



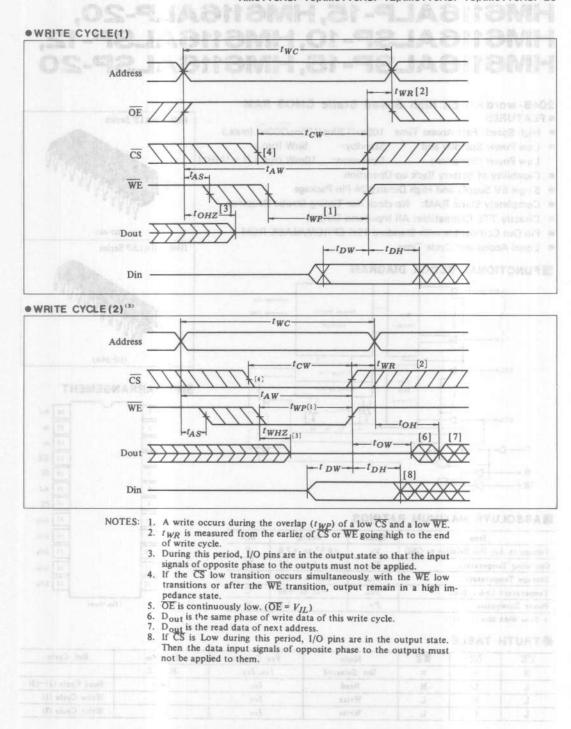
NOTES: 1. WE is High for Read Cycle.

2. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low.

**OHITACHI** 

4.  $\overline{OE} = V_{IL}$ .

HM6116AP-10,HM6116AP-12,HM6116AP-15,HM6116AP-20 HM6116ASP-10,HM6116ASP-12,HM6116ASP-15,HM6116ASP-20



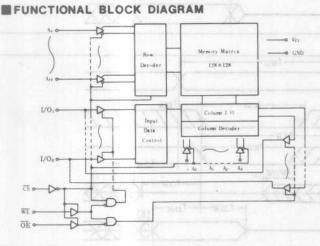
**HITACHI** 

157

# HM6116ALP-10, HM6116ALP-12, HM6116ALP-15, HM6116ALP-20, HM6116ALSP-10, HM6116ALSP-12, HM6116ALSP-15, HM6116ALSP-20

2048-word×8-bit High Speed Static CMOS RAM = FEATURES

- High Speed: Fast Access Time 100ns/120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 5μW (typ.)
   Low Power Operation; Operation: 10mW (typ.) (f = 1MHz)
- Capability of Battery Back up Operation
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time



#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vr	-0.5* to +7.0	V
Operating Temperature	T.p.	0 to +70	°C
Storage Temperature	Tere	-55 to +125	°C
Temperature Under Bias	T	-10 to +85	°C
Power Dissipation	Pτ	1.0	W

♥ Pulse Width 50ns : -1.5V

#### TRUTH TABLE

CS	ŌĒ	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
Н	×	×	Not Selected	Isa, Isai	High Z	
L	L	Н	Read	Icc	Dout	Read Cycle (1)~(3
L	Н	L	Write	Icc	Din	Write Cycle (1)
L	L	L	Write	Icc	Din	Write Cycle (2)



# PIN ARRANGEMENT

(DP-24A)



**OHITACHI** 

#### HM6116ALP-10,HM6116ALP-12,HM6116ALP-15,HM6116ALP-20 HM6116ALSP-10,HM6116ALSP-12,HM6116ALSP-15,HM6116ALSP-20

Item	Symbol	min	typ	max	Unit
en	Vcc	4.5	5.0	5.5	v
apply Voltage	GND	0	0	0	Notice V
Input Voltage	Vin	2.2	3.5	6.0	bilav v
	ViL	-1.0*	72.1 -	0.8	v

# **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to +70°C)

# DC AND OPERATING CHARACTERISTICS (Vcc=5V ±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	H	M6116A ALSP-1		H	M6116A ALSP-1		H	M6116A ALSP-1.		н	M6116A ALSP-2		Unit
Item	Symbol	Test Conditions	min	typ*	max	min	typ*	max	min	typ*	max	min	typ*	max	Onit
Input Leakage Current	I <sub>LI</sub>	$V_{CC}$ =5.5V, $V_{in}$ =GND to $V_{CC}$	-0	1	2	-	-	2	-	011×0	2	1,200	120	2	μÂ
Output Leakage Current	I <sub>LO</sub>	$\overline{\text{CS}} = V_{IH} \text{ or } \overline{\text{OE}} = V_{IH},$ $V_{I/O} = \text{GND to } V_{CC}$	-	-	2	-	-	2	- 27	ν <u>Έ</u> Ν.	2	3.04	AIN	2	μĀ
Operating Power	Icc	$\overline{\text{CS}} = V_{IL}, I_{I/O} = 0 \text{mA}$ $V_{in} = V_{IH} \text{ or } V_{IL}$	-	4	12	0 18 -	4	12	Tellan.	4	12	-	4	12	mA
Supply Current	Icci	$\frac{V_{IH}=V_{CC}, V_{IL}=0V,}{\overline{CS}=V_{IL}, I_{I/O}=0\text{mA}, f=1\text{MHz}}$	1	2	5	-	2	5		2	5	-	2	5	mA
Average Operating Current	I <sub>CC2</sub>	min. cycle, duty=100%	-	35	60	-	30	50	-	20	40	- Tro	15	30	mA
Standby Power	ISB	$\overline{\text{CS}} = V_{IH}$	-	0.5	3	-	0.5	3	-	0.5	3	17	0.5	3	mA
Supply Current	ISBI	$\overline{\text{CS}} \ge V_{CC} - 0.2 \text{V}$	-	1	50	1	1	50		1	50	-	1	50	μA
Output Voltage	VOL	I <sub>OL</sub> =4mA	-	-	0.4	-	-	0.4	-	-	0.4	215	-	0.4	V
Output + Oltage	VOH	I <sub>OH</sub> =-1.0mA	2.4	-	-	2.4	-	-	2.4	-	-	2.4	-	-	V

\*: V<sub>CC</sub>=5V, T<sub>a</sub>=25°C

AC CHARACTERISTICS (Vcc-5V ±10%, Ta-0 to +70°C)

#### **AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

#### **READ CYCLE**

Item	Symbol		6ALP/ P-10		16ALP/ P-12		6ALP/ P-15	HM611 ALS		Unit
1000	Symoor	min	max	min	max	min	max	min	max	Onn
Read Cycle Time	IRC	100	-	120	-	150	-	200	-	ns
Address Access Time	IAA	-	100	-	120		150	-	200	ns
Chip Select Access Time	TACS	-	100		120	-	150	-	200	ns
Chip Selection to Output in Low Z	t <sub>CLZ</sub>	10	(XeX)	10	-	10	-3.0	10	-	ns
Output Enable to Output Valid	tOE	-	50	-	55	-	60		70	ns
Output Enable to Output in Low Z	toLZ	10	-	10	-	10	-	10	0Y2 6	ns
Chip Deselection to Output in High Z	tCHZ	0	40	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	tOHZ	0	40	0	40	0	50	0	60	ns
Output Hold from Address Change	tOH	10		10	-	15	-	20	-	ns

#### HM6116ALP-10,HM6116ALP-12,HM6116ALP-15,HM6116ALP-20 HM6116ALSP-10,HM6116ALSP-12,HM6116ALSP-15,HM6116ALSP-20

#### **WRITE CYCLE**

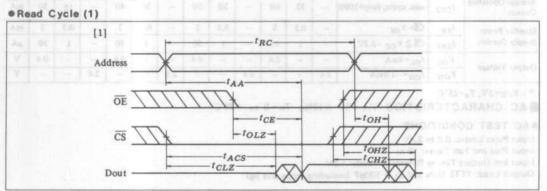
Item	Symbol		16ALP/ SP-10		16ALP/ IP-12		16ALP/ SP-15		IGALP/ P-20	Unit
A CONTRACTOR OF	Symoor	min	max	min	max	min	max	min	max	om
Write Cycle Time	twc	100	-	120	-	150	-	200		ns
Chip Selection to End of Write	1CW	65	-	70	+	90	-	120	-	ns
Address Valid to End of Write	TAW	80	-	105	+	120	-	140	-	ns
Address Set Up Time	tAS	0	-	0		0	-	0	100-20	ns
Write Pulse Width	twp	60	-	70	-	80	-	100	-	ns
Write Recovery Time	twR	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High Z	tOHZ	0	40	0	40	0	50	0	60	ns
Write to Output in High Z	IWHZ	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	1DW	30	- 11	35	-	40		50	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	tow	10	4	10	-	10	-	10	in states	ns

#### CAPACITANCE (f=1MHz, Ta=25°C)

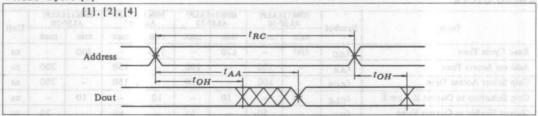
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C.,	V,0V	3	5	pF
Input/Output Capacitance	C1.0	V1 0-0V	5	7	pF

Note) This parameter is sampled and not 100% tested

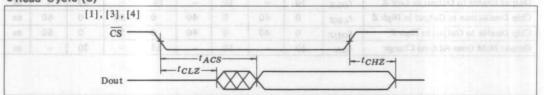
#### TIMING WAVEFORM







Read Cycle (3)



**OHITACHI** 

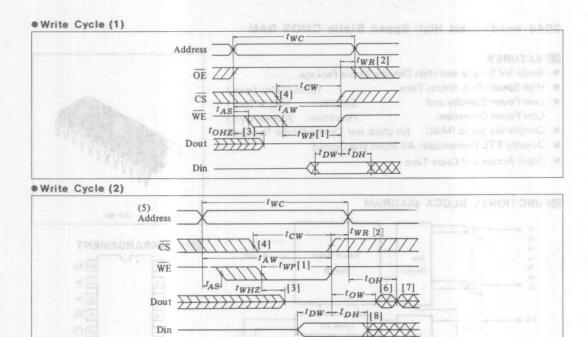
NOTES: 1. WE is High for Read Cycle.

2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .

3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low. 4.  $\overline{OE} = V_{IL}$ .

160

#### HM6116ALP-10,HM6116ALP-12,HM6116ALP-15,HM6116ALP-20 HM6116ALSP-10,HM6116ALSP-12,HM6116ALSP-15,HM6116ALSP-20



NOTES: 1. A write occurs during the overlap  $(t_{WP})$  of a low  $\overline{CS}$  and a low  $\overline{WE}$ .

- t<sub>WR</sub> is measured from the earlier of CS or WE going high to the end of write cycle.
- During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$

transition, output remain in a high impedance state.

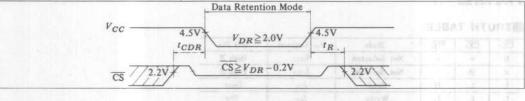
- 5.  $\overline{OE}$  is continuously low. ( $\overline{OE} = V_{IL}$ )
- 6. Dout is the same phase of write data of this
- write cycle.
- Dout is the read data of next address.
   If CS is Low during this period, I/O pins are
- in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

#### LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	VDA	CS≥Vcc -0.2V	2.0	-	1 -	V
Data Retention Current	Iccon*	Vcc = 3.0V, CS≥2.8V	CEISE-of a	100-01	30	μA
Chip Deselect to Data Retention Time	tcon		0	-	ini Latter	ns
Operation Recovery Time	t.e	See Retention Waveform	1 RC **	- sut	no the	ns

\*\* In. -Read Cycle Time.

#### Low Vcc Data Retention Waveform

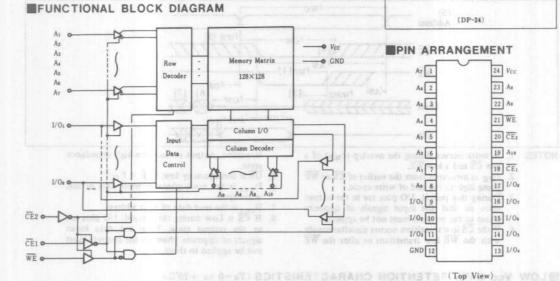


# HM6117P-3, HM6117P-4

2048-word×8-bit High Speed Static CMOS RAM

#### FEATURES

- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time
- Low Power Standby and Standby:
  - Low Power Operation: Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time



150ns/200ns (max.)

100µW (typ.)

#### **MABSOLUTE MAXIMUM RATINGS**

Symbol	Rating	Unit	
Vr	*-0.5 to +7.0	V	
Pr	1.0	W	
Tape	0 to +70	°C	
Teta	-55 to +125	°C	
Toins	-10 to +85	°C	
	VT PT Tspr Tsta	$V_T$ $\bullet -0.5 \text{ to} +7.0$ $P_T$ 1.0 $T_{spr}$ 0 to +70 $T_{stg}$ -55 to +125	$V_T$ *-0.5 to +7.0         V $P_T$ 1.0         W $T_{opr}$ 0 to +70         °C $T_{stg}$ -55 to +125         °C

Line Schmass Correct Cha Direter in Outs Hitestin Teel Operation Threets The Ref. as a Traff of the State

WWWWWWWW

\* Pulse width 50ns : -1.5V

#### TRUTH TABLE

I/O Pin	Vcc Current	Mode	WE	CE:	CEi
High Z	Iccli	Not Selected	×	×	Н
High Z	Iccus	Not Selected	×	Н	×
Dout	Icc	Read	H	L	L
Din	Icc	Write	L	L	L

HM6117P-3,HM6117P-4

# RECOMMENDED DC OPERATING CONDITIONS (0°C≤Ta≤70°C)

Item	Symbol	min	typ	max	- Unit	
	Vcc	4.5	5.0	5.5	v	
Supply Voltage	GND	0	0	0	V	
Input High (logic 1) Voltage	VIN	2.2	3.5	6.0	V	
Input Low (logic 0) Voltage	Vil	-1.0*	/4////	0.8	V	

Pulse width: 50ns, DC: Vilan = -0.3V

#### **DC AND OPERATING CHARACTERISTICS** (Ta=0°C to +70°C, Vcc-5V±10%, GND-0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	1_11	V.,-GND to Vcc	-	-	10	μA
Output Leakage Current	110	$\overline{CE}_{i} = V_{IH} \text{ or } \overline{CE}_{i} = V_{IH}$ $V_{I,a} = \text{GND to } V_{CC}$	ogen <u>1</u> 37	1 18 <u>1</u> 708	10	μA
Operating Power Supply Current: DC	Icc	$\overline{CE}_{1} = \overline{CE}_{2} = V_{IL},  I_{L,0} = 0 \text{mA}$		40	80	mA
Average Operating Current	Icci	$\frac{\text{Min cycle, duty}=100\%}{\overline{\text{CE}}_{1}-V_{11}, \overline{\text{CE}}_{2}=V_{11}}$	-	40	80	mA
Standby Power Supply Current (1): DC	IccLi®	$\frac{\overline{CE}_{i} \geq V_{cc} - 0.2V}{V_{iN} \geq V_{cc} - 0.2V}$ or $V_{iN} \leq 0.2V$	-	0.02	2	mA
Standby Power Supply Current (2): DC	Icc11*	$\overline{CE}_{z} \ge V_{cc} - 0.2V$		0.02	2	mA
Output low Voltage	Vol	Iot=2.1mA	-	-	0.4	V
Output High Voltage	Von	$I_{OH} = -1.0 \text{mA}$	2.4	-	-	V

Notes: 1) Typical limits are at  $V_{cc} = 5.0V$ ,  $Ta = +25^{\circ}C$ 

2) \* : Vitea -- 0.3V

#### **CAPACITANCE** (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	CIN	V <sub>IN</sub> =0V	3	5	pF
Input/Output Capacitance	Ciro	V1. 0-0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

#### **MAC CHARACTERISTICS** (Ta=0°C to +70°C, Vcc=5V±10% unless otherwise noted)

#### AC TEST CONDITIONS

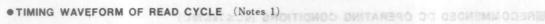
Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns Input and Output Timing Reference Levels: 1.5V Output Load: 1 TTL Gate and  $C_L$ =100pF (including scope and jig)

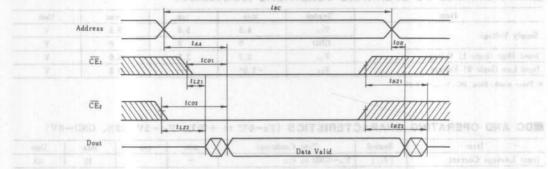
#### **•READ CYCLE**

[tem	Symbol	HM6117P-3		HM6117P-4		Unit	
Item	Symbol	min	max	mîn	max	Unit	
Read Cycle Time	trc	150	-	200	-	ns	
Address Access Time	las	inst T	150	b million	200	ns	
Chip Enable (CE1) to Output	teoi	916 -	150	10 (59:3)	200	ns	
Chip Enable (CE2) to Output	tcor	1803 <u>-</u>	150		200	ns	
Chip Enable $(\overline{CE}_1)$ to Output in Low Z	tizi	10	100 <u>- 10</u> 00	10	104	ns	
Chip Enable $(\overline{CE}_2)$ to Output in Low Z	lizz	10	-	10	1010	ns	
Chip Disable $(\overline{CE}_1)$ to Output in High Z	tHZI	0	70	0	80	ns	
Chip Disable $(\overline{CE}_2)$ to Output in High Z	tuzz	0	70	0	80	ns	
Output Hold from Address Change	ton	15	10/100	15	1000 C	ns	



#### HM6117P-3,HM6117P-4



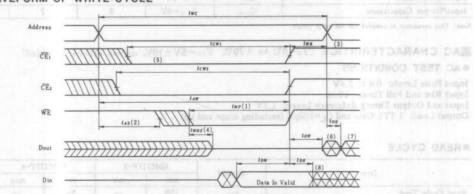


NOTES: 1. WE is High for Read Cycle.

#### **WRITE CYCLE**

Item	Symbol	HM6117P-3		HM6117P-4		Unit	
Item	Symbol	min	max	mîn	max	Uni	
Write Cycle Time	twc	150	H 332	200	-	ns	
Chip Enable (CE1) to End of Write	tem	100	6 4 4 v	120	all set of	ns	
Chip Enable (CE1) to End of Write	tews	110	-	130	-	ns	
Address Set Up Time	las	20	satt -	20	THICKS.	ns	
Address Valid to End of Write	LAW	130	-	150	-	ns	
Write Pulse Width	twp	100	100 L	120	- 344	ns	
Write Recovery Time	lwa	15	1999 <u>-</u>	15		ns	
Write to Output in High Z	lwnz	0	60	0	70	ns	
Data to Write Time Overlap	tow	50	-	60	-	ns	
Data Hold from Write Time	ton	20	-05.00 r	20	- Thurs	ns	
Output Active from End of Write	tow	10	-	10	-	ns	





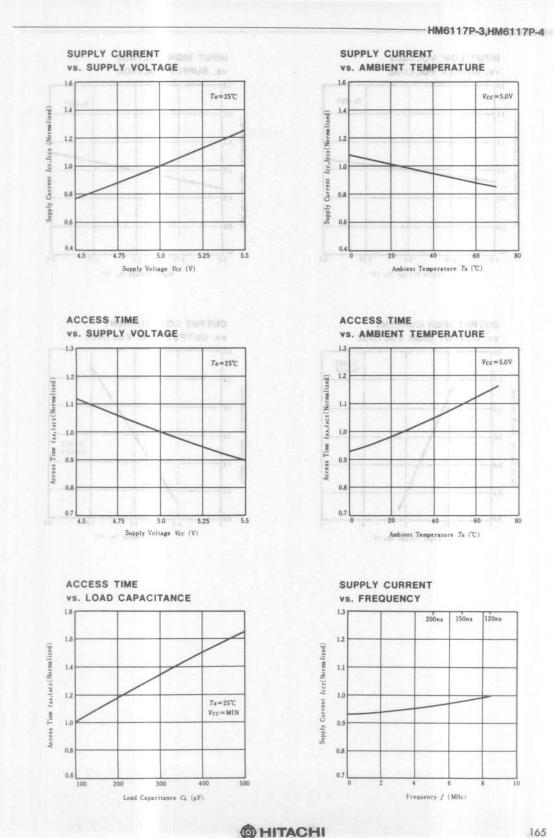
NOTES: 1 A write occurs during the overlap (twp) of low CE<sub>1</sub>, CE<sub>2</sub> and WE.
2. tAS is measured from the address changes to the biginning of the write.
3. twR is measured from the earlier of CE<sub>1</sub>, CE<sub>2</sub> or WE going high to the end/of write cycle.

 During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

5. If the  $\overline{CE}_1$  or  $\overline{CE}_2$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transitions, output remain in a high impedance state.

**OHITACHI** 

- Dout is the same phase of write data of this write cycle.
- Dout is the read data of next address.
- 8. If  $\overline{CE_1}$  and  $\overline{CE_2}$  are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

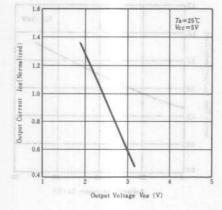






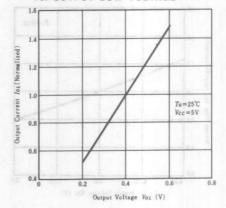
166



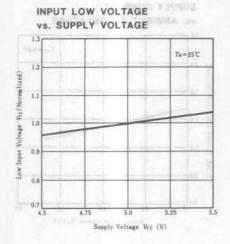


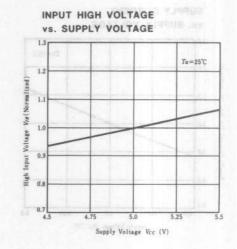
OUTPUT HIGH CURRENT

vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE





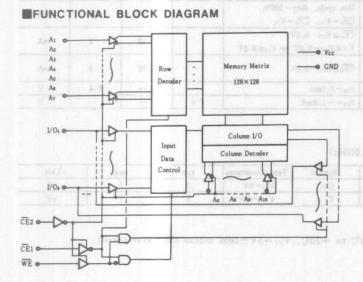
HM6117P-3,HM6117P-4 --



2048-word×8-bit High Speed Static CMOS RAM

#### FEATURES

- High Density Small Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (typ.)
   Low Power Operation: Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time





As 3 21 WE A. 4 20 CE: Aa 5 19 A10 Az 6 18 CE A1 7 17 L/Os 16 L/Or A. 8 I/01 9 15 1/0. 1/01 10 14 1/05 1/01 11 13 1/04 GND 12

# as 20- an apirary (Top View)

ENGINERAT CONCITIONS

WI CT I TOWAT DEPOSIT

and Representation of the second second

Gunnel Loud 1777 Gate and C. # 1000F

# BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	Vr	*-0.5 to +7.0	V
Power Dissipation	PT	1.0	W
Operating Temperature	Tepr	0 to +70	°C
Storage Temperature	Tele	-55 to +125	°C
Temperature Under Bias	There	-10 to +85	"С
Pulse width 50cs: -1.5V	150		443

#### TRUTH TABLE

<b>CE</b> <sub>1</sub>	CE:	WE	Mode	Vcc Current	I/O Pin
Н	×	×	Not Selected	IccLi	High Z
×	Н	×	Not Selected	IccLi	High Z
L	L	H	Read	Icc	Dout
L	L	L	Write	Icc	Din

Arm Ard No. ( Cycle Trino Add No. Arean Trin Chi Shake (C. ) to Daped in the Chi Shake (T. ) to Cated in the Chi Shake (T. ) to Cated in the



HM6117FP-3,HM6117FP-4

#### **RECOMMENDED DC OPERATING CONDITIONS** $(0^{\circ}C \le Ta \le 70^{\circ}C)$

Symbol	Of min ited	typ	max	Unit
Vcc	4.5	5.0	5.5	V
GND	0	0	0	V
VIN	- 2.2	3.5	6.0	V
VIL	-1.0*	to Orm. Third	0.8	V
	stidenti Dir	invited to that	Reduced to a	Thickness
	pin Package.	In Density 24		V3 stocks .
	Vcc GND Vin	Vcc         4.5           GND         0           Vin         2.2           Vin         -1.0*	Vcc         4.5         5.0           GND         0         0           Vin         2.2         3.5           Vin         -1.0*         -	Vcc         4.5         5.0         5.5           GND         0         0         0         0           Vin         2.2         3.5         6.0         6.0

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	V.,=GND to Vcc	Vo <del>cr</del> eak n	1000	10	μA
Output Leakage Current	110	$\overline{CE}_{1} = V_{IN} \text{ or } \overline{CE}_{t} = V_{IN}$ $V_{I \neq 0} = \text{GND to } V_{CC}$	ll (n <u>es</u> ut an a	A :si <u>di</u> osi Nele Tim	10	μA
Operating Power Supply Current : DC	Icc	$\overline{CE}_1 = \overline{CE}_2 = V_{IL},  I_{I=0} = 0 \text{mA}$	-	40	80	mA
Average Operating Current	Icei	$\frac{\text{Min cycle, duty}=100\%}{\overline{\text{CE}}_1 = V_{1L}, \ \overline{\text{CE}}_2 = V_{1L}}$	MAROM	40	80	mA
Standby Power Supply Current (1) : DC	Icc11*	$\overline{CE}_{i} \ge V_{cc} - 0.2V,$ $V_{is} \ge V_{cc} - 0.2V \text{ or } V_{is} \le 0.2V$	7-0	0.02	2	mA
Standby Power Supply Current (2): DC	Iccus*	$\overline{CE}_{t} \geq V_{cc} - 0.2V$	=	0.02	2	mA
Output low Voltage	Vol	IoL-2.1mA		-	0.4	V
Output High Voltage	VOR	Ion = -1.0mA	2.4	-		V

Notes : 1) Typical limits are at Vcc-5.0V, Ta-+25'C

2) ♥ : V<sub>ILare</sub> = −0.3V

## **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	CIN	$V_{IN} = 0V$	3	5	pF
Input/Output Capacitance	Ci o	V/ 0=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

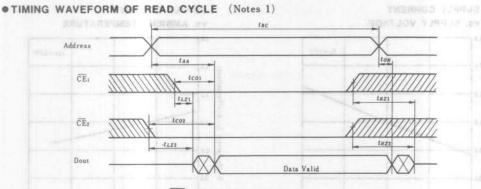
## ■AC CHARACTERISTICS (Ta=0°C to +70°C, Vcc=5V±10% unless otherwise noted)

#### AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V Input Rise and Fall Times: 10 ns Input and Output Timing Reference Levels: 1.5V Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

	0.5 10		AND OF THE	at Pas Rela		
Sumbal	HM6117P-3		HM6117P-4		Unit	
Symool	min	max	min	max	Onit	
1 tre 28 -	150		200	Units other	ns	
lan	-	150	-	200	ns	
tcoi	-	150		200	ns	
tcoz	-	150	-	200	EIS .	
tizi	10		10	1000	ns	
t 1.22	10	-	10	19.44	ns	
tHZI	0	70	0	80	ns	
tuzz	0	70	0	80	ns	
ton	15		15		ns	
	Symbol 1 KC 1 AA 1 CO1 1 CO2 1 L21 1 L22 1 M22 1 M22	Symbol         min           lnc         150           lAA         -           lcoi         -	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Symbol         HM6117P-3         HM61 $t_{AC}$ 150          200 $t_{AA}$ 150 $t_{CO1}$ 150 $t_{CO1}$ 150 $t_{CO1}$ 150 $t_{CO2}$ 150 $t_{CO2}$ 150 $t_{L21}$ 10          10 $t_{L22}$ 10          10 $t_{H21}$ 0         70         0	Symbol         HM6117P-3         HM6117P-4           min         max         min         max $t_{KC}$ 150          200 $t_{KA}$ 150          200 $t_{CO1}$ 150          200 $t_{CO1}$ 150          200          200          200          200          200          200          200          200          100          200          200          200          100          200          100          10           200          10           200          10           10           10           10           10           10          1         1          1         1          1         1         -	

BONTAR MUNIXAM BTUJO38A8

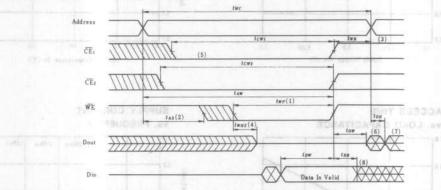


NOTES: 1. WE is High for Read Cycle.

#### **WRITE CYCLE**

Item	Symbol	HM61	17P-3	HM6	117P-4	Unit
item	Symuon	min	max	min	max	
Write Cycle Time	twc	150	-	200	-	ns
Chip Enable (CE1) to End of Write	tews	100	-	120	100455	ns
Chip Enable $(\overline{CE}_t)$ to End of Write	1 cwz	110	- 3	130	(1999)#R (18)	ns
Address Set Up Time	tAS	20		20		ns
Address Valid to End of Write	t.A.W.	130	- 19	150	-	ns
Write Pulse Width	twr	100	-	120		ns
Write Recovery Time	twn	15	-	15	-	ns
Write to Output in High Z	twnz	0	60	0	70	ns
Data to Write Time Overlap	tow	50	-	60	- 1	ns
Data Hold from Write Time	t <sub>DH</sub>	20	-	20		ns
Output Active from End of Write	tow	10	-	10	-	ns

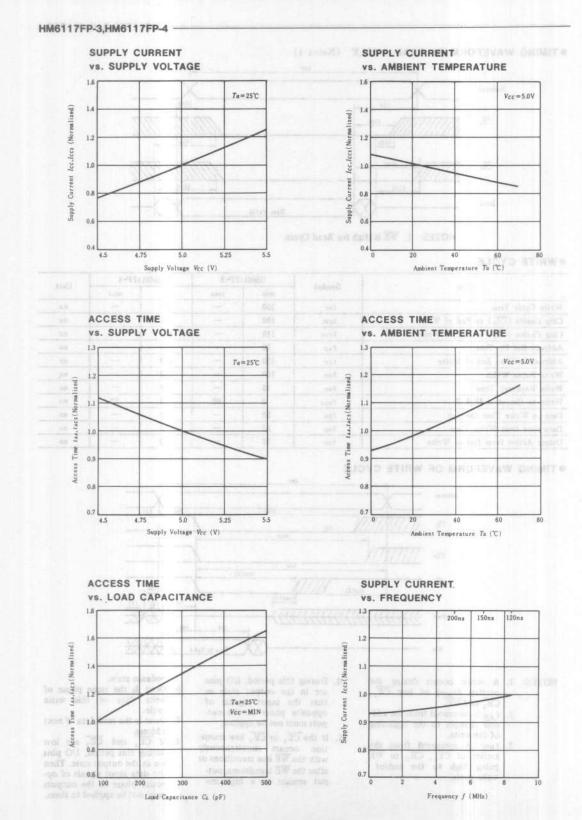
#### **TIMING WAVEFORM OF WRITE CYCLE**



- NOTES: 1. A write occurs during the overlap  $(t_W p)$  of low  $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{WE}$ .
  - 2.  $t_{AS}$  is measured from the address changes to the biginning of the write.
  - 3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}_1$ ,  $\overline{CE}_2$  or WE going high to the end/of write cycle.
- During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- 5. If the  $\overline{CE_1}$  or  $\overline{CE_2}$  low transition occurs simultaneously with the WE low transitions or after the WE transitions, output remain in a high im-

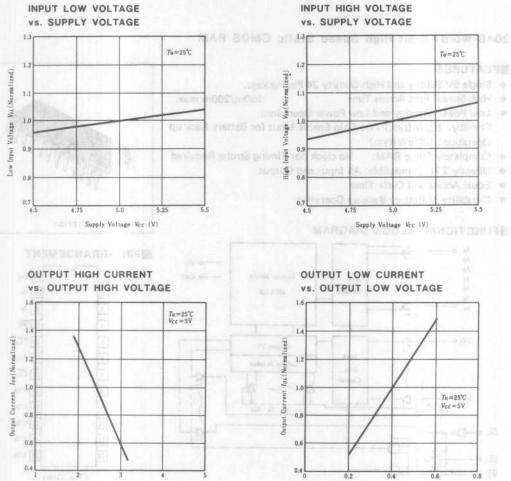
**OHITACHI** 

- pedance state.
- 6. Dout is the same phase of write data of this write cycle.
- Dout is the read data of next address.
- 8. If CE, and CE<sub>2</sub> are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.



170

( HITACHI



Output Voltage Von (V)

INPUT LOW VOLTAGE

Output Voltage Vol (V)

	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$

HM6117FP-3,HM6117FP-4

0.8

132-05

12

0.0

101.10

5.5

**OHITACHI** 

171

# HM6117LP-3, HM6117LP-4

ON NOR TRANS

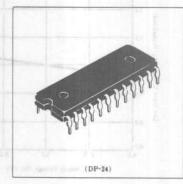
# NPUT LOW VOLTER

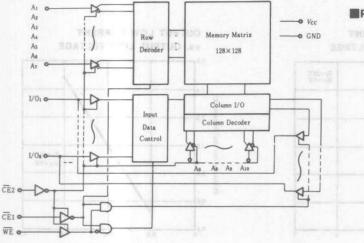
### 2048-word×8-bit High Speed Static CMOS RAM

#### FEATURES

- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation; Standby: 10µW (typ.) Two Chip Enable Input for Battery Back up Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

# FUNCTIONAL BLOCK DIAGRAM







#### **MABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	VT	*-0.5 to +7.0	V
Operating Temperature	$T_{spr}$	0 to +70	°C
Storage Temperature	Trie	-55 to +125	"C
Temperature Under Bias	T	-10 to +85	°C
Power Dissipation	Pr	1.0	·W

\* Pulse width 50ns : -1.5V

#### TRUTH TABLE

CE,	CE:	WE	Mode	Vcc Current	I/O Pin
Н	×	×	Not Selected	Iccli	High Z
×	Н	×	Not Selected	Iccus	High Z
L	L	Н	Read	Icc	Dout
L	L	L	Write	Icc	Din

#### HM6117LP-3,HM6117LP-4

Item	Symbol	min	typ	max	Unit
C	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High (logic 1) Voltage	Vin	2.2	3.5	6.0	V
Input low (logic 0) Voltage	VIL	-1.0*	-07400	0.8	V

RECOMMENDED DC OPERATING CONDITIONS (Ta-0°C to+70°C)

\* Pulse Width : 50ns, DC : Vilais = -0.3V.

#### **DC AND OPERATING CHARACTERISTICS** (Ta=0°C to +70°C, Vcc=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	Vin=GND to Vcc	-	-	2	μA
Output Leakage Current	ent $ I_{L0} $ $\frac{\overline{CE}_{i} - V_{IN} \text{ or } \overline{CE}_{i} - V_{IN}}{V_{I/0} = \text{GND to } V_{CC}}$		-	-	2	μA
Operating Power Supply Current : DC	Icc	$\overline{CE}_1 = \overline{CE}_2 = V_{IL},  I_{I \ge 0} = 0 \text{ mA}$	-	35	70	mA
Average Operating Current	Icci	Min cycle, duty = $100\%$ $\overline{CE}_1 = V_{1L}$ , $\overline{CE}_2 = V_{1L}$	-	35	70	mA
Standby Power Supply Current (1): DC	Iccu*	$\overline{CE}_{1} \ge V_{cc} - 0.2V$ $V_{IN} \ge V_{cc} - 0.2V \text{ or } V_{IN} \le 0.2V$	-	2	50	μA
Standby Power Supply Current (2): DC	Icc12*	$\overline{CE}_z \ge V_{cc} - 0.2V$	-	2	50	μA
Output low Voltage	Vol	IoL=2.1mA	-	- and	0.4	V
Output High Voltage	V on	$I_{OH} = -1.0 \text{mA}$	2.4	-	-	V

Notes: 1) Typical limits are at  $V_{cc} = 5.0V$ ,  $Ta = +25^{\circ}C$ 

2) \* :  $V_{Ilmin} = -0.3V$ 

#### **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	CIN	V1N=0V	3	5	pF
Input/Output Capacitance	Ciro	V100=0V	- 5	7	pF

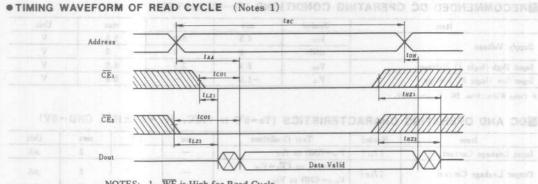
Note >1) This parameter is sampled and not 100% tested.

#### **BAC CHARACTERISTICS** ( $Ta=0^{\circ}C$ to $+70^{\circ}C$ , $V_{cc}=5V\pm10\%$ unless otherwise noted) •AC TEST CONDITIONS

#### READ CYCLE

Item	C. Li	HM61	17LP-3	HM61	17LP-4	
item	Symbol	min	max	min	max	Uni
Read Cycle Time	LAC	150	-	200	-	ns
Address Access Time	LAA		150		200	ns
Chip Enable $(\overline{CE}_1)$ to Output	tcoi	-	150	-	200	ns
Chip Enable (CE2) to Output	tcoz	Distant L	150	and the second	200	ns
Chip Enable (CE1) to Output in Low Z	tLZI	10	-	10	0.150	ns
Chip Enable (CEr) to Output in Low Z	tizz	10	-	10	100 H	ns
Chip Disable $(\overline{CE}_1)$ to Output in High Z	tHZI	0	70	0	80	ns
Chip Disable (CE:) to Output in High Z	tHZI	0	70	0	80	ns
Output Hold from Address Change	ton	15		15	-	ns

HM6117LP-3,HM6117LP-4

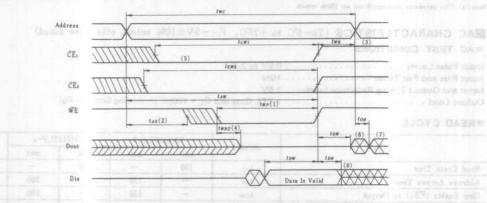


NOTES: 1. WE is High for Read Cycle.

#### **WRITE CYCLE**

Am Item	Sundal	HM61	17LP-3	HM61	17LP-4	Unit
Item	Symbol	min	max	mín	max	Unit
Write Cycle Time	twc	150	20 - CE.	200		ns
Chip Enable (CE1) to End of Write	tewi	100	147 <b>-</b>	120	- 100	ns
Chip Enable $(\overline{CE}_2)$ to End of Write	lows	110	-	130	rin <del>go</del> an	ns
Address Set Up Time	tas	20	-	20	- 30	ns
Address Valid to End of Write	LAW	130	103 - U	150		ns
Write Pulse Width	lwp	100	101 - 0	120	-100	ns
Write Recovery Time	lwa	15		15	· · · · · · · · · · · · · · · · · · ·	ns
Write to Output in High Z	lwnz	0	60	0	70	ns
Data to Write Time Overlap	Low	50	Contra To	60	anti-	ns
Data Hold from Write Time	l DH	20		20	a section of	ns
Output Active from End of Write	tow	10	-	10	11911	ns





NOTES:	1	A write occurs during the
		overlap $(t_W p)$ of low $\overline{CE}_1$ , $\overline{CE}_2$ , and $\overline{WE}_2$ .
81 83	2.	$t_{AS}$ is measured from the address changes to the bigin- ning of the write.
	3.	$t_{WR}$ is measured from the earlier of $\overline{CE}_1$ , $\overline{CE}_2$ or $\overline{WE}$ going high to the end/of

write cycle.

4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

5. If the  $\overline{CE}_1$  or  $\overline{CE}_2$  low transition occurs simultaneously with the WE low transitions or after the WE transitions, output remain in a high impedance state.

**OHITACHI** 

6. Dout is the same phase of write data of this write cycle.

7. Dout is the read data of next address.

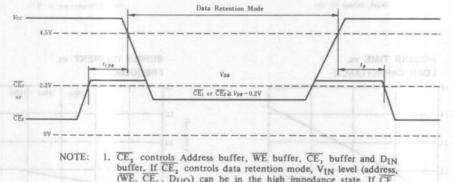
8. If  $\overline{CE_1}$  and  $\overline{CE_2}$  are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

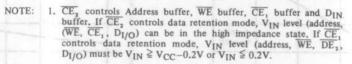
Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	V <sub>DR1</sub>	$\overline{\text{CE}}_{1} \ge V_{CC} - 0.2\text{V},$ $V_{IN} \ge V_{CC} - 0.2\text{V or } V_{IN} \le 0.2\text{V}$	2.0	-	-	v
Vcc for Data Retention	VOR2	$\overline{CE}_t \ge V_{cc} - 0.2V$	2.0	-	4	V
Data Retention Current	Iccons	$V_{CC} = 3.0 \text{V}, \ \overline{\text{CE}}_1 \ge 2.8 \text{V},$ $V_{IN} \ge 2.8 \text{V} \text{ or } V_{IN} \le 0.2 \text{V}$	-	-	30*	μA
Data Retention Current	ICCDRE	$V_{cc}=3.0V, \ \overline{CE}_{2} \ge V_{cc}=0.2V$	-	-	30*	μA
Chip Deselect to Data Retention Time	toos		0	-	-	ns
Operation Recovery Time	t <sub>R</sub>	See Retention Waveform	t RC**	-	-	ns

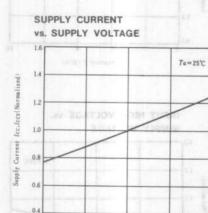
LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°Cto +70°C)

\*\* tac-Read Cycle Time

#### . LOW Vcc DATA RETENTION WAVEFORM







4.5

4.75

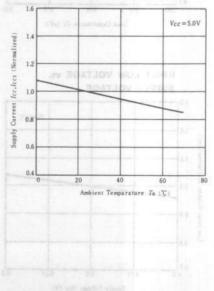
5.0

Supply Voltage Vcc (V)

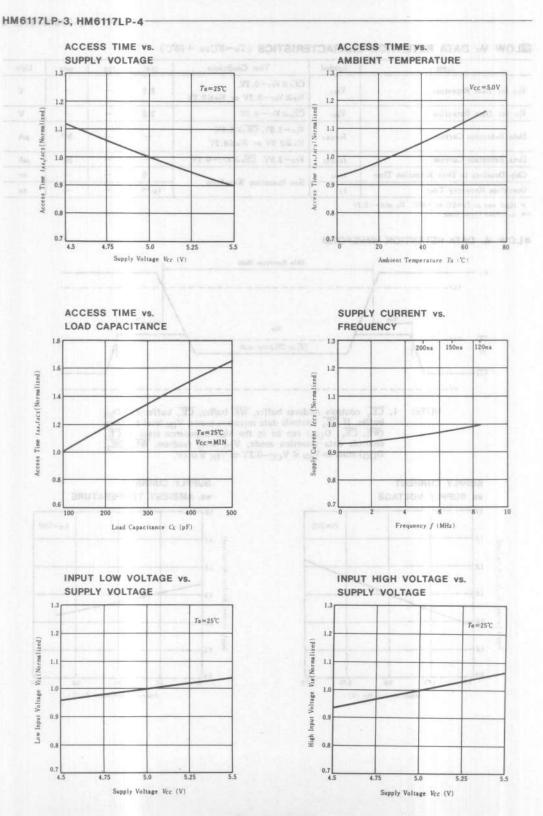
5.25

5.5

SUPPLY CURRENT vs. AMBIENT TEMPERATURE

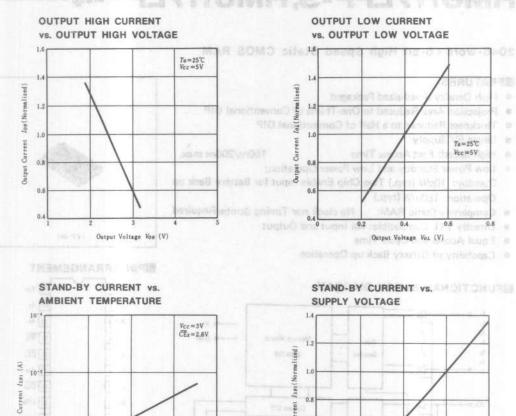


**OHITACHI** 



176

**HITACHI** 



0.8 ent

0.6 440

> 0.4 0.2

3



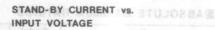
Ambient Temperature Ta ("C)

20

Standby

10-

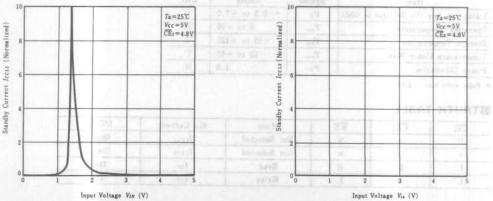
10-



Supply Voltage Vcc (V)

Ta=25'C CEa=Vec-0.2V

5



**OHITACHI** 

80

60

177

# HM6117LFP-3, HM6117LFP-4

#### 2048-word×8-bit High Speed Static CMOS RAM

#### FEATURES

Ai c Az

As

A

As

As Ar

1/0,0

1/0: 4

CE2 0

CEI O WE a

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- 150ns/200ns max. High Speed: Fast Access Time
- Low Power Standby and Low Power Operation; Standby: 10µW (typ.) Two Chip Enable Input for Battery Back up Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output

Row

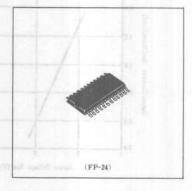
Decoder

Input

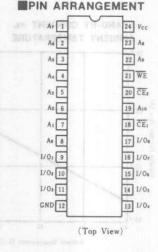
Data

Control

- Equal Access and Cycle Time
- Capability of Battery Back up Operation



#### **FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS** 

O Vcc

· GND

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	VT	*-0.5 to +7.0	V
Operating Temperature	Tapr	0 to +70	°C
Storage Temperature	Teta	-55 to +125	°C
Temperature Under Bias	Thins	-10 to +85	°C
Power Dissipation	PT	1.0	W

\* Pulse width

#### TRUTH TABLE

CE:	CE:	WE	Mode	Vcc Current	I/O Pin
Н	×	×	Not Selected	Iccus	High Z
×	Н	×	Not Selected	Iccus	High Z
L	L	Н	Read	Icc	Dout
L	L	L	Write	Icc	Din

Memory Matrix

128×128

Column I/O

Column Decoder

As As A10

An

23





#### HM6117LFP-3, HM6117LFP-4

#### **ERECOMMENDED DC OPERATING CONDITIONS** (Ta-0°C to+70°C)

Item	Symbol	min	typ	max	Unit
Sunda Valtage	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High (logic 1) Voltage	VIH	2.2	3.5	6.0	v
Input low (logic 0) Voltage	VIL	-1.0*	-907/4777	0.8	V

· Pulse Width : 50ns, DC : Vilan =-0.3V.

#### DC AND OPERATING CHARACTERISTICS (Ta-0°C to +70°C, Vcc-5V±10%, GND-0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	Vin-GND to Vcc	-	-	2	μA
Output Leakage Current	110	$\overline{CE}_{1} = V_{IH} \text{ or } \overline{CE}_{2} = V_{IH}$ $V_{I < 0} = \text{GND to } V_{CC}$	n 4.00 4.3	1 . T - 10 - 10	2	μA
Operating Power Supply Current: DC	Icc	$\overline{\mathrm{CE}}_1 = \overline{\mathrm{CE}}_2 = V_{IL},  I_{I+0} = 0 \mathrm{mA}$	-	35	70	mA
Average Operating Current	Icei	$\frac{\text{Min cycle, duty} = 100\%}{\overline{CE}_i - V_{1L},  \overline{CE}_2 - V_{1L}}$	-	35	70	mA
Standby Power Supply Current (1): DC	Iccui*	$\overline{CE}_{i} \ge V_{cc} = 0.2V$ $V_{1N} \ge V_{cc} = 0.2V \text{ or } V_{1N} \le 0.2V$	-	2	50	μA
Standby Power Supply Current (2): DC	Icc11*	$\overline{CE}_t \ge V_{cc} - 0.2V$	-	2	50	μA
Output low Voltage	Vol	Io1=2.1mA	-	Thin is	0.4	V
Output High Voltage	Von	$I_{ON} = -1.0 \text{mA}$	2.4	-		V

2) # : VILan = -0.3V

#### **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	CIN	V <sub>IN</sub> -0V	3	5	pF
Input/Output Capacitance	Ciro	V <sub>t</sub> o=0V	5	RO #7 1 43 M	pF

Note:1) This parameter is sampled and not 100% tested.

# **EAC CHARACTERISTICS** (Ta=0°C to +70°C, Vcc=5V±10% unless otherwise noted)

. AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V Input Rise and Fall Times ..... 10ns Input and Output Timing Reference Levels --- 1.5V Output Load ...... 1 TTL Gate and CL = 100pF (Including Scope & Jig)

#### **READ CYCLE**

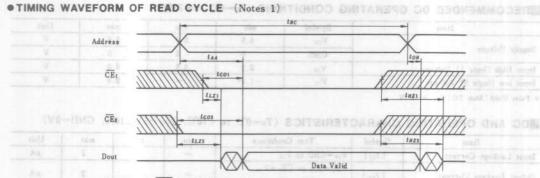
Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
Item		min	max	min	max	Unit
Read Cycle Time	IRC	150	-	200	-	ns
Address Access Time	· LAA	-	150	-	200	ns
Chip Enable (TE1) to Output	tcor	-	150	-	200	ns
Chip Enable (CE2) to Output	lcos	2013 2	150	101/220	200	ns
Chip Enable (TE1) to Output in Low Z	tizi	10	1973 TOOL 1	10	1010/AL_	ns
Chip Enable $(\overline{CE}_{2})$ to Output in Low Z	tLz:	10	in ward 1	10		ns
Chip Disable $(\overline{CE}_1)$ to Output in High Z	tuzi	0	70	0	80	ns
Chip Disable $(\overline{CE}_{\epsilon})$ to Output in High Z	tizi	0	70	0	80	ns
Output Hold from Address Change	ton	15	101 01 <u>0</u> 10_0	15	111-11	ns

most was be applied or floor

put remain in a high im-

**OHITACHI** 

HM6117LFP-3, HM6117LFP-4-

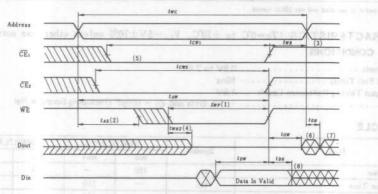


NOTES: 1. WE is High for Read Cycle.

#### **WRITE CYCLE**

Ace I Item	Symbol	HM6111	7LFP-3	HM611	7LFP-4	Unit
Item	Symbol.	min	max	min	max	Unit
Write Cycle Time	twc	150	35	200	in Similar	ns
Chip Enable $(\overline{CE}_1)$ to End of Write	lewi	100	$- v_{aa}$	120	- 30	ns
Chip Enable $(\overline{CE}_2)$ to End of Write	tcw2	110	-	130	ik <del>us</del> ik n	ns
Address Set Up Time	tas	20	-	20	- 30	ns
Address Valid to End of Write	LAW	130	ab = ab	150	-spath.	ns
Write Pulse Width	twp	100	nd - d	120	The de?	ns
Write Recovery Time	lwa	15	-3814-4	15	The sector in the sector	ns
Write to Output in High Z	twn2	0	60	0	70	ns
Data to Write Time Overlap	tow	50	-	60	-	ns
Data Hold from Write Time	t DH	20		20	11.02MAT	ns
Output Active from End of Write	tow	10	-	10	- 1000	ns

#### **TIMING WAVEFORM OF WRITE CYCLE**



NOTES: 1 A write occurs during the overlap  $(t_W p)$  of low  $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{WE}$ .

- 2.  $t_{AS}^{2}$  is measured from the address changes to the biginning of the write,
- 3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}_1$ ,  $\overline{CE}_2$  or  $\overline{WE}$  going high to the end/of write cycle.

 During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

 If the CE<sub>1</sub> or CE<sub>2</sub> low transition occurs simultaneously with the WE low transitions or after the WE transitions, output remain in a high im-

**OHITACHI** 

pedance state.

- Dout is the same phase of write data of this write cycle.
- Dout is the read data of next address.
- If CE<sub>1</sub> and CE<sub>2</sub> are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

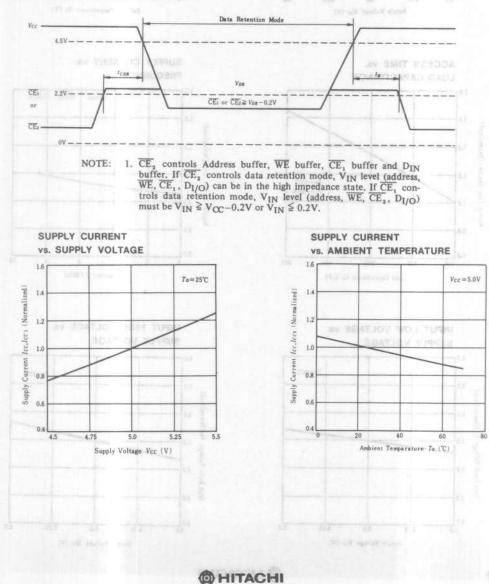
Item	Symbol	Test Condition	min	typ	max	Unit
Vcc for Data Retention	VDRI	$\overline{CE}_1 \ge V_{cc} - 0.2V,$ $V_{1N} \ge V_{cc} - 0.2V \text{ or } V_{1N} \le 0.2V$	2.0	-		v
Vcc for Data Retention	V <sub>DR2</sub>	$\overline{CE}_t \ge V_{cc} - 0.2V$	2.0	-	-	V
Data Retention Current	ICCDRI	$V_{CC} = 3.0V, \ \overline{CE_1} \ge 2.8V,$ $V_{IN} \ge 2.8V \text{ or } V_{IN} \le 0.2V$	-	>	30*	μA
Data Retention Current	ICCDR2	$V_{cc}=3.0V, \ \overline{CE}_t \ge V_{cc}=0.2V$		-	30*	μA
Chip Deselect to Data Retention Time	lcor	C. D. W. W.	0	-	-	ns
Operation Recovery Time	t <sub>R</sub>	See Retention Waveform				ns

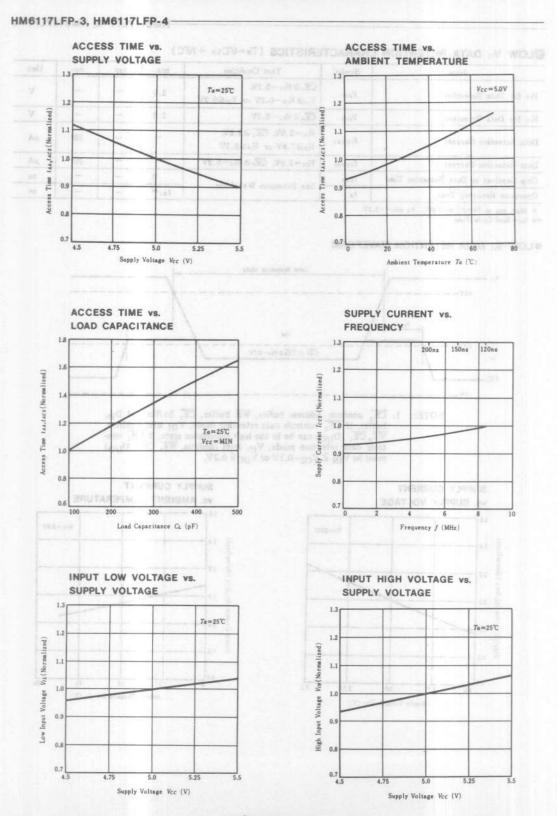


\*  $10\mu A$  max at Ta=0C to  $\pm 40C$ ,  $V_{IL}$  min=

\*\* tac=Read Cycle Time

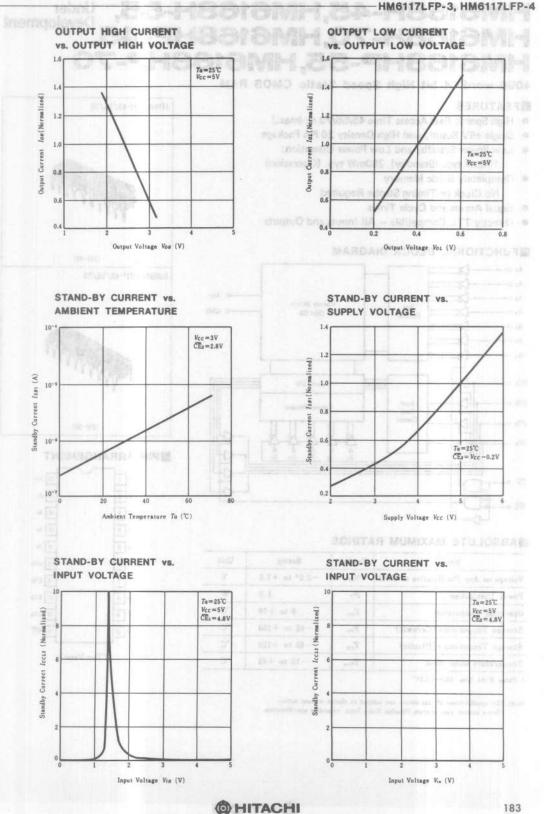
#### . LOW Vcc DATA RETENTION WAVEFORM

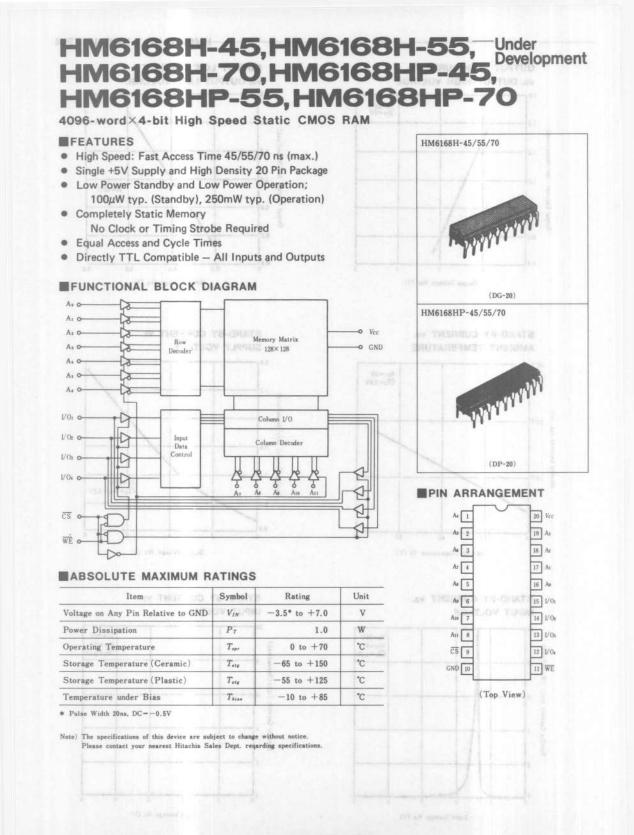




182

**OHITACHI** 





**HITACHI** 

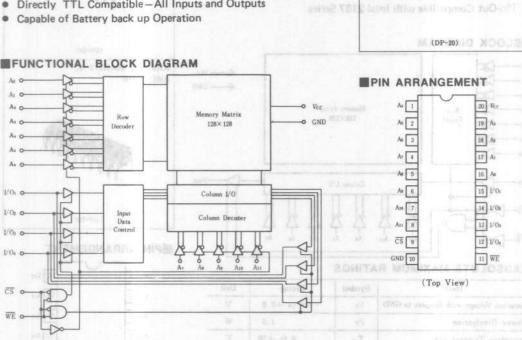
## HM6168HLP-45, HM6168HLP-55, HM6168HLP-70 **Under** Development

4096-word×4-bit High Speed Static CMOS RAM

I IIA - eldit -

## FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation; 5µW typ. (Standby), 250mW typ. (Operation)
- Completely Static Memory No Clock or Timing Strobe Required
- Equal Access and Cycle Times.
- Directly TTL Compatible All Inputs and Outputs
- .



#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit			Staroge Temperature Ceramini
Voltage on Any Pin Relative to GND	VIN	-3.5* to +7.0	v			
Power Dissipation	$P_{T}$	1.0	W			
Operating Temperature	Тарт	0 to +70	°C	- isan	TARRAD	
Storage Temperature	Tris	-55 to $+125$	"C			(6'C≤Ta≤70'01
Temperature under Bias	Thiss	-10 to +85	°C	-	Esturie 1	and
* Pulse Width 20ns, DC=-0.5V		V P.S	0.1	2.3		
				6.9		

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications

**OHITACHI** 

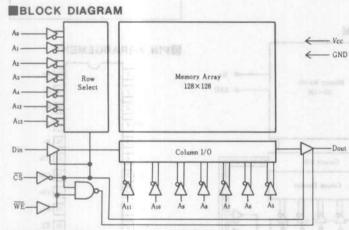
O S O A BI

# HM6167,HM6167-6,HM6167-8, HM6167P,HM6167P-6,HM6167P-8

16384-word×1-bit High Speed Static CMOS RAM

#### FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation Stand-by 25mW Typ, and Operating 150mW Typ.
- Completely Static Memory . . . . No Clock nor Refresh Required
- Fully TTL Compatible All Inputs and Output
- Separate Data Input and Output . . . . . . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series



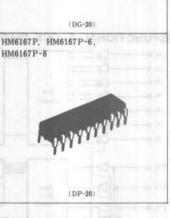
#### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	VT	-0.5 to $+7.0$	v
Power Dissipation	PT	1.0	w
Operating Temperature	Tope	0 to +70	°C
Storage Temperature(Plastic)	Tete	-55 to +125	°C
Storage Temperature(Ceramic)	Tete	-65 to +150	°C

## RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq Ta \leq 70^{\circ}C)$ 

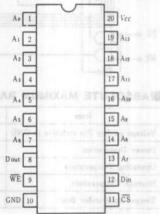
Item	Symbol	min	typ	max	Unit
e 1 V 1	Vcc	4.5	5.0	5.5	v
Supply Voltage	GND	0	0	0	v
Input High Voltage	Vin	2.2	-	6.0	v
Input Low Voltage	VIL	-0.5	-	0.8	v



HM6167, HM6167-6,

HM6167-8

#### **PIN ARRANGEMENT**



(Top View)



#### HM6167, HM6167-6, HM6167-8, HM6167P, HM6167P-6, HM6167P-8

WTIMING WAVEFORM OF READ CYCLE NO. 1 101

TIMENC WAVEFORM OF READ CYCLE NO 2 14.1

#### TRUTH TABLE

LOYO BERNIN

CS	WE	Mode	Vcc Current	Output Pin	Reference Cycle
Н	×	Not Selected	Isb. Isbi	High Z	
L	Н	Read	Icc	Dout	Read Cycle 1, 2
L	L	Write	Icc 85	High Z	Write Cycle 1, 2

## DC AND OPERATING CHARACTERISTICS (Vcc-5V±10%, Ta=0°C to +70°C)

Item	Symbol	Test Conditions	1	min	typ	max	Unit
Input Leakage Current	1411	$V_{cc} = 5.5 \text{ V},  V_{IN} = 0 \text{ V} \sim V_{cc}$		-	-	2	μA
Output Leakage Current	IL0	$\overline{\mathrm{CS}} = V_{IB}, V_{OUT} = 0 \mathrm{V} \sim V_{CC}$		-	seller/	2	μA
Operating Power Supply Current	Icc	$\overline{\mathrm{CS}} = V_{IL}$ , Output Open	10	-	30	60	mA
2.4 M M	Isa	$\overline{\mathrm{CS}} = V_{IH}$	1. 10	-2	5	20	mA
Standby Power Supply Current	Ism	$\overline{CS} = V_{cc} - 0.2 V$ $V_{is} \le 0.2 V \text{ or } \ge V_{cc} - 0.2 V$		n 19. ars Lisserthy	0.02	2	mA
Output Low Voltage	VOL	Io1-8mA	the start	CONTRACTOR	A Designation of	0.4	v
Output High Voltage	V <sub>OH</sub>	$I_{OH} = -4 \mathrm{mA}$		2.4	-	-	v

Note) Typical limits are at Vcc=5.0V. Ta=25°C and specified loading.

#### AC TEST CONDITIONS

**Output Load B Output Load A** Input pulse levels: GND to 3.0V ( for tHZ, tLZ, tWZ & tow) +5V Input rise and fall times: 5 ns 0 +5V Input timing reference levels: 1.5V 0 \$ 4800 Output reference levels: 1.5V ₹ 4800 Dout O-Output load: See Figure 30nF 2550 Dout O-5pF\* 2550 1 \* Including scope and jig.

## **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	CIN	5	pF	$V_{IN} = 0 V$
Output Capacitance	Cour	6	pF	$V_{0UT} = 0 V$

Note) This parameter is sampled and not 100% tested.

## **AC CHARACTERISTICS** (*Vcc*=5V±10%, *Ta*=0°C to 70°C, unless otherwise noted.) **•READ CYCLE**

Tanan	C 11	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit
Item	Symbol -	min	max	min	max	min	max	Unit
Read Cycle Time	tac	70	in the second	85	Those	100	-	ns
Address Access Time	tas	-	70	-	85	-	100	ns
Chip Select Access Time	tACS	-	70	-	85	-	100	ns
Output Hold from Address Change	ton	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	tiz	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	tHZ	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	tru	0	-	0	-	0	-	ns
Chip Deselection to Power Down Time	tpp	-	35	-	40		45	ns



#### HM6167, HM6167-6, HM6167-8, HM6167P, HM6167P-6, HM6167P-8-

#### **WRITE CYCLE**

stard men Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit	Notes
item S. a	Symbol	mîn	max	min	max	min	max	Unit	Ivotes
Write Cycle Time	d twc	70	Ten	85	-head	100	-11	ns	2
Chip Selection to End of Write	tcw	55		65	- and a	80	-	ns	
Address Valid to End of Write	tAW	55	-	65	-	80	-	ns	
Address Setup Time	tas	2010 V		0	ANT TAN	AHO0 DI	N CHARLEN	ns	A DOR
Write Pulse Width	twp	40	I have T the	45	1 Edm	55	-	ns	
Write Recovery Time	twa	0	-V5-N	0	-	0	-	ns	A. J. merel
Data Valid to End of Write	tow	30	10000	35	Tax	40	-	ns	T studet
Data Hold Time	t <sub>DH</sub>	0	and Inst	0		0	-	ns	
Write Enable to Output in High Z	twz	0	30	0	40	0	40	ns	3,4
Output Active from End of Write	tow	0	- 10	0	-	0	-	ns	3,4

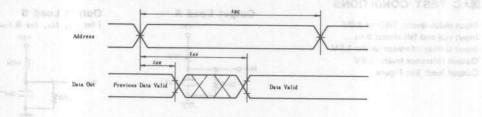
Notes) 1. If CS goes high simultaneouly with WE high, the output remains in a high impedance state. 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.

All write Cycle timings are referenced from the last valid address to the first transitioning address.
 Transition is measured ±500 mV from steady state voltage with specified loading in Load B.

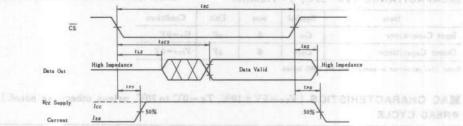
4. This parameter is sampled and not 100% tested.

ested. Astron Act





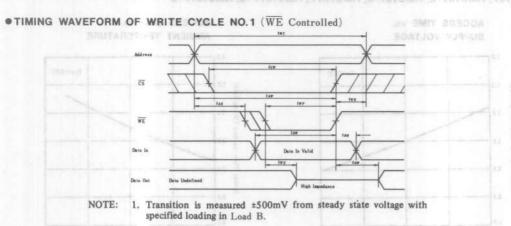
•TIMING WAVEFORM OF READ CYCLE NO.21,3)



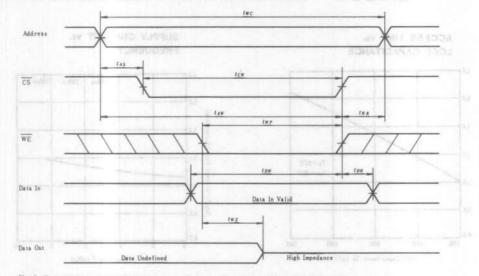
	NOTES:	2. Addr	high and Cesses valid p	prior to or	coincider	t with CS tra	ansition low.
		<ol> <li>Trans specification</li> </ol>	tition is maind	easured ±	500 mV fi	om steady s	state voltage with
		24		, an Loud L	-		
							Deput Huld Even Act and Owner
		0#					

**HITACHI** 

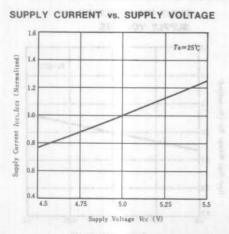
#### HM6167, HM6167-6, HM6167-8, HM6167P, HM6167P-6, HM6167P-8



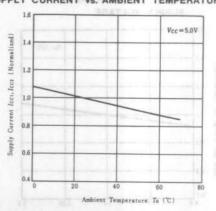
• TIMING WAVEFORM OF WRITE CYCLE No. 2 (CS Controlled)



Note) Transition is measured ±500mV from steady state voltage with specified loading in Load B.

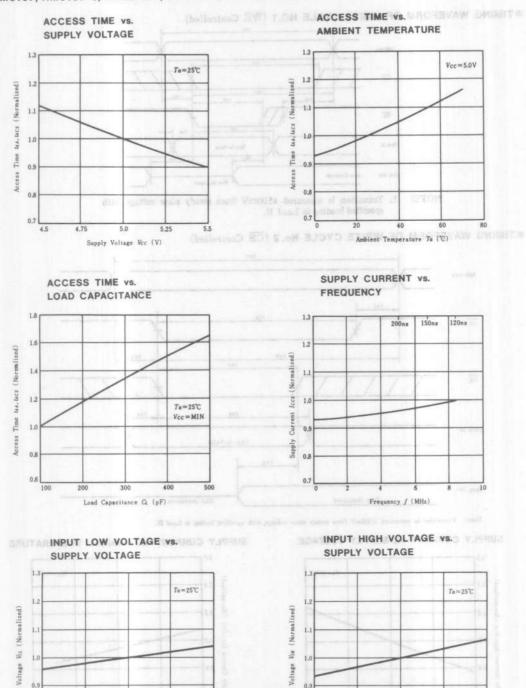






**OHITACHI** 

## HM6167, HM6167-6, HM6167-8, HM6167P, HM6167P-6, HM6167P-8-



190

0.5

ō,

0.7 4.5

4.75

5.0

Supply Voltage Vcc (V)

worl Input

**HITACHI** 

5.5

High Voltage

Input 0.8

0.9

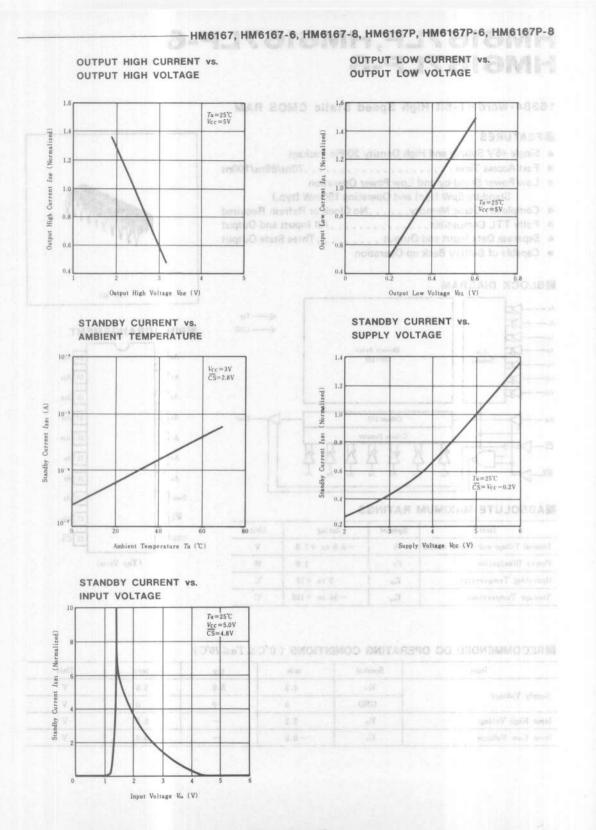
0.7 L 4,5

4.75

5.0

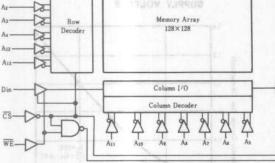
Supply Voltage Vcc (V)

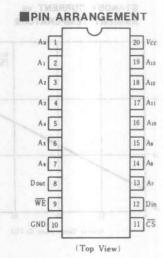
5.5



**HITACHI** 

## HM6167LP, HM6167LP-6, HM6167LP-8 16384-word×1-bit High Speed Static CMOS RAM FEATURES Single +5V Supply and High Density 20 Pin Package Low Power Stand-by and Low Power Operation Stand-by 5µW (typ) and Operating 150mW (typ.) A WAY THEY Completely Static Memory..... No Clock or Refresh Required Fully TTL Compatible . . . . . . . . . . . . . All Inputs and Output Separate Data Input and Output ..... Three State Output Capable of Battery Back up Operation BLOCK DIAGRAM (DP-20) X < - Vcc 2 - GND PIN ARRANGEMENT





## BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V7	-0.5 to +7.0	v
Power Dissipation	$P_{7}$	1.0	W
Operating Temperature	Tepr	0 to +70	°C
Storage Temperature	Tete	-55 to +125	*C

## ASATION PROPAGE

## **RECOMMENDED DC OPERATING CONDITIONS** ( $0 \degree C \leq Ta \leq 70\degree C$ )

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	v
	GND	0	0	0	v
Input High Voltage	Vin	2.2	-	6.0	v
Input Low Voltage	VIL	-0.5	-	0.8	v



#### -HM6167LP, HM6167LP-6, HM6167LP-8

#### TRUTH TABLE

OT MING WAYE ORM OF READ OVOLE NO. 1 "

CS	WE	Mode	Mode Vcc Current		Reference Cyc	
Н	×	Not Selected	I 5.B., I 5.B.1	High Z		
L	Н	Read	Icc	Dout	Read Cycle 1, 2	
L	L	Write	Icc	High Z	Write Cycle 1, 2	

## DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, Ta=0~+70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{cc} = 5.5 V V_{IN} = 0 V \sim V_{cc}$	-	-	2	μA
Output Leakage Current	IL0	$\overline{\mathrm{CS}} = V_{IH},  V_{out} = 0  \mathrm{V} \sim V_{CC}$		-	2	μA
Operating Power Supply Current	Icc	$\overline{CS} = V_{lL}$ , Output Open	-	30	60	mA
second of the	Isa	$\overline{\text{CS}} = V_{IH}$	-	5	20	mA
Standby Power Supply Current	Ism	$\overline{CS} = V_{cc} - 0.2V$ $V_{lN} \le 0.2V \text{ or } \ge V_{cc} - 0.2V$	-	1	50	μA
Output Low Voltage	Vol	<i>I</i> <sub>0L</sub> =8mA	-	-	0.4	v
Output High Voltage	Von	$I_{OH} = -4 \mathrm{mA}$	2.4	-	-	V

Note) Typical limits are at  $V_{cc}$  = 5.0V, Ta = 25°C and specified loading.

#### AC TEST CONDITIONS

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure		times: 5 ns		Output Load A	Output Load B (for tHz, tLz, tWZ & tow) +5V
		evels: 1.5V		Dout 0	₩ 480Ω
				2550 \$ = 30pF*	Dout O
				the second	2552 \$ 5pF
				* Including scope and jig.	where the second second second

## **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

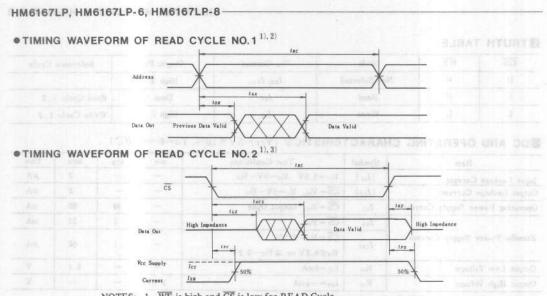
Item	Symbol	max	Unit	Conditions
Input Capacitance	CIN	5	pF	$V_{IN} = 0 V$
Output Capacitance	Cour	6	pF	Vour-0V

Note) This parameter is sampled and not 100% tested.

**EAC CHARACTERISTICS** ( $Ta=0^{\circ}C$  to  $+70^{\circ}C$ ,  $V_{cc}=5V\pm10\%$ , unless otherwise noted.) **•READ CYCLE** 

Item	Symbol -	HM6167LP		HM6167LP-6		HM6167LP-8		Unit
i tem		min	max	min	max	min	max	Unit
Read Cycle Time	tac	70	-	85	-	100	-	ns
Address Access Time	tax	-	70	-	85	- 100	100	ns
Chip Select Access Time	LACS	-	70	-	85	-	100	ns
Output Hold from Address Change	ton	5	-	5		5	-	ns
Chip Selection to Output in Low Z	t <sub>LZ</sub>	5		5		5	-	ns
Chip Deselection to Output in High Z	tuz	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	tru	0	/ - 1	0	-	0		ns
Chip Deselection to Power Down Time	tro	443	35	-	40	-	45	ns





NOTES: 1.  $\overline{\text{WE}}$  is high and  $\overline{\text{CS}}$  is low for READ Cycle.

- 2. Addresses valid prior to or coincident with  $\overline{\text{CS}}$  transition low.
- Transition is measured ±500mV from steady state voltage with specified loading B.

**WRITE CYCLE** 

Tanaolin Dal tinte dell'Internet

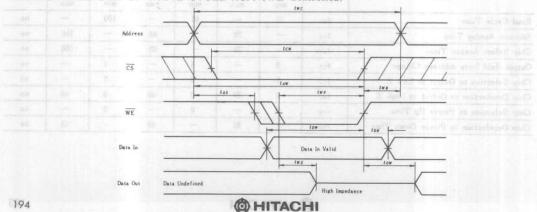
These	C. I.I	HM6167LP		HM6167LP-6		HM6167LP-8		Unit	Notes
Item	Symbol	min	max	min	max	min	max	Unit	ivotes
Write Cycle Time	twc	70	-	85	-	100	-	ns	2
Chip Selection to End of Write	tew	55	-	65	-	80	-	ns	
Address Valid to End of Write	t <sub>AW</sub>	55	000	65	-	80	-	ns	
Address Setup Time	tAS	0	-	0	-	0		ns	
Write Pulse Width	twp	40	-	45	10.7-1	55	7 30	ns	ICAPI
Write Recovery Time	twe	0	autores.	0	-	0	21-11	ns	
Data Valid to End of Write	t <sub>DW</sub>	30	-	35	-	40	-	ns	No.
Data Hold Time	t <sub>DH</sub>	0		0		0	-	ns	Dings (
Write Enable to Output in High Z	tw2	0	30	0	40	0	40	ns	3,4
Output Active from End of Write	low	0	-	0	-	0		ns	3,4

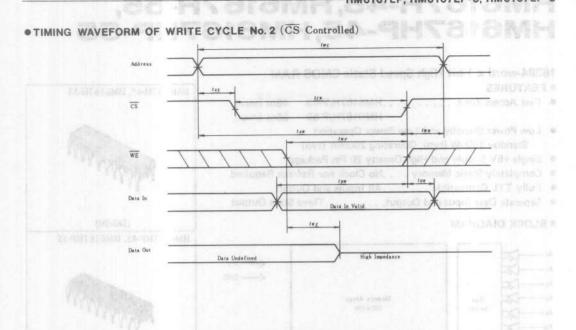
Notes) 1. If CS goes high simultaneouly with WE high, the output remains in a high impedance state.

2. All Write Cycle timings are referenced from the last valid address to the first transitioning address. 3. Transition is measured  $\pm$ 500mV from steady state voltage with specified loading in Load B.

4. This parameter is sampled and not 100% tested.





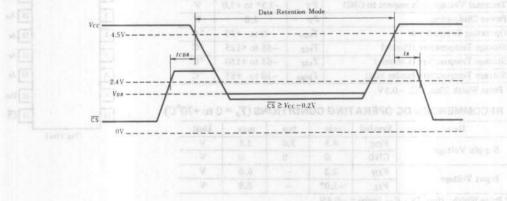


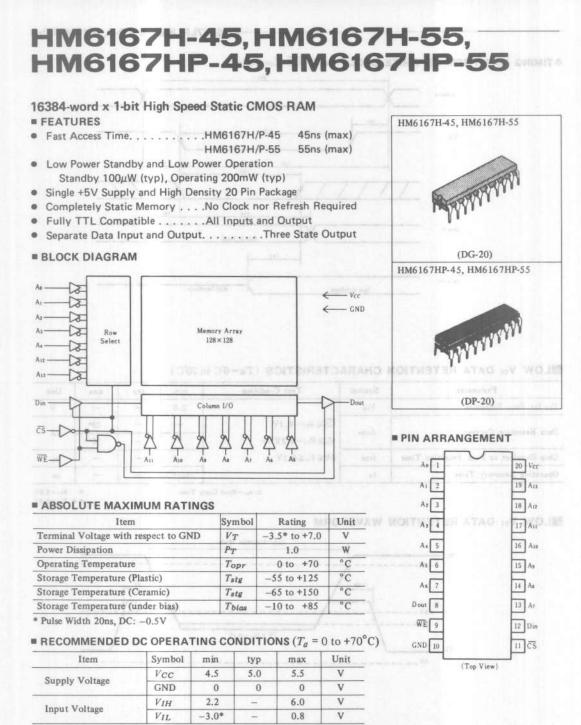
#### LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol Test Condition		min	typ	max	Unit
Vcc for Data Retention	VDR	av	2.0	-	-	V
Data Retention Current		$\overline{\mathrm{CS}} \ge V_{cc} - 0.2 \mathrm{V}$	-	-	20*	-
	ICCDR	$V_{i*} \ge V_{CC} = 0.2 \text{ V}$ or	1 7	15-1	30**	μA
Chip Deselect to Data Retention Time	İCDR	$0  \mathbb{V} \leq V_{i*} \leq 0.2  \mathbb{V}$	0	-	- 1	ns
Operation Recovery Time	t n		1 RC <sup>G</sup>	-	-	ns

\* Vec-2.0V \*\* Vcc=3.0V

## LOW Vcc DATA RETENTION WAVEFORM





\* Pulse Width: 20ns, DC:  $V_{II}$  (min) = -0.5V

#### -HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

CS	WE	Mode	Vcc Current	Dout Pin	Ref. Cycle
H	×	Not selected	Isn, Isni	High-Z	
L	Н	Read	Ice line	Dout	Read Cycle
L	en-L	Write	Ice	High-Z	Write Cycle

# BAC CHARACTERISTICS ( Wer-SV 110%, Te-07 to 200, alless of what the solar to TRUTH TABLE

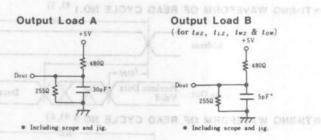
**DC AND OPERATING CHARACTERISTICS** ( $V_{cc} = 5V \pm 10\%$ ,  $T_a = 0^{\circ}$  to  $\pm 70^{\circ}$ )

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	$V_{cc} = 5.5 \text{V}, V_{IN} = 0 \text{V} \sim V_{cc}$	- 23	0.108_0.07	2	μA
Output Leakage Current	110	$\overline{\mathrm{CS}} = V_{IH},  V_{OUT} = 0  \mathrm{V} \sim V_{CC}$			2	μA
Operating Power Supply Current	Icc	$\overline{\text{CS}} = V_{lL}$ , Output Open		40	80	mA
	Isa	$\overline{CS} = V_{IH}$	-	10	20	mA
Standby Power Supply Current	Issi	$\overline{CS} \ge V_{cc} - 0.2V$ $V_{ts} \le 0.2V \text{ or } \ge V_{cc} - 0.2V$		0.02	2	mA
Output Low Voltage	Vol	<i>IoL</i> = 8mA	ENT CEUE	in The	0.4	V
Output High Voltage	V <sub>OH</sub>	$I_{GH} = -4 \mathrm{mA}$	2.4	all and a set	515 <u>0</u> -3	V

Note) Typical limits are at Vcc=5.0V. Ta=25℃ and specified loading.

#### **AC TEST CONDITIONS**

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure



#### **CAPACITANCE** (*Ta*=25°C, *f*=1.0MHz)

Item Strab	Symbol	typ	max	Unit	Conditions
Input Capacitance	CIN	3	5	pF	$V_{IN} = 0 V$
Output Capacitance	Cour	5	7	pF	Vour=0V

Note) This parameter is sampled and not 100% tested.

**HITACHI** 

#### HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

## **BAC CHARACTERISTICS** ( $V_{cc} = 5V \pm 10\%$ , $Ta = 0^{\circ}C$ to 70°C, unless otherwise noted.) **•READ CYCLE**

Item	Symbol	HM6167H/P-45		HM6167HP-55		Unit	Notes	
item	Symbol	min	max	min	max	Onit	Notes	
Read Cycle Time	IRC	45	-	55	-	ns	(1)	
Address Access Time	IAA	- 5	45	-	55	ns		
Chip Select Access Time	TACS	E[0] = E[T]	45	37,2494	55	ns	OKA DOD	
Output Hold from Address Change	toH	5	at 12	5	-	ns		
Chip Selection to Output in Low Z	ILZ	5		5	-	ns	(2) (3) (7)	
Chip Deselection to Output in High Z	tHZ	0	30	0	30	ns	(2)(3)(7)	
Chip Selection to Power Up Time	tPU	0	-	0	-	ns		
Chip Deselection to Power Down Time	IPD	-	30	-	30	ns	and the second	

NOTES: 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.

 At any given temperature and voltage condition, t<sub>HZ</sub> max, is less than t<sub>LZ</sub> min. both for a given device and from device to device.

3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

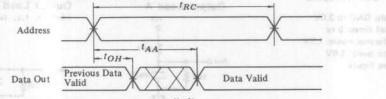
4. WE is High for READ cycle.

5. Device is continuously selected,  $\overline{CS} = V_{IL}$ .

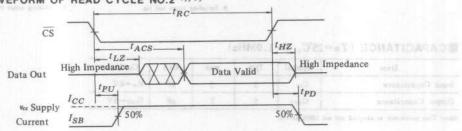
6. Addresses valid prior to or coincident with CS transition low.

7. This parameter is sampled and not 100% tested.

## • TIMING WAVEFORM OF READ CYCLE NO.1 4), 5)



TIMING WAVEFORM OF READ CYCLE NO.2 4), 6)



C HITACHI

#### HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

#### . WRITE CYCLE

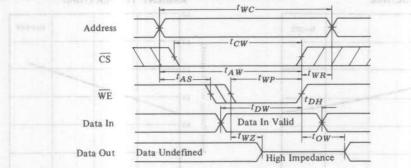
36014630 7	THE REPAIR	HM616	7H/P-45	HM616	HM6167H/P-55		
Item	Symbol	min	max	min	max	Unit	Notes
Write Cycle Time	IWC	45		55		ns	(2)
Chip Selection to End of Write	ICW	40	-	50	-	ns	1.1
Address Valid to End of Write	IAW	40		50		ns	1.5
Address Setup Time	IAS	0	-	0	-	ns	
Write Pulse Width	IWP	25	-	35	-	ns	1
Write Recovery Time	twR	0	-	0	-	ns	12.5
Data Valid to End of Write	IDW	25	-	25	-	ns	2
Data Hold Time	tDH .	0	-	0	-	ns	1.3
Write Enable to Output in High Z	twz	0	25	0	25	ns	(3) (4)
Output Active from End of Write	tow	0	-	0	-	ns	(3) (4)

NOTES: 1. If CS goes high simultaneously with WE high, the output remains in a high impedance states.

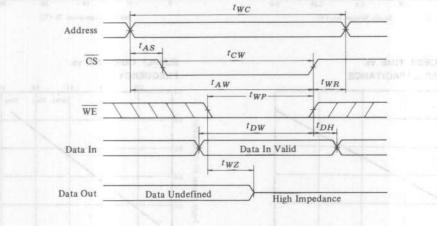
- All write cycle timings are referenced from the last valid address to the first transitioning address.
   Transition is measured ±500mV from steady state voltage with specified loading in Load B.

  - 4. This parameter is sampled and not 100% tested.

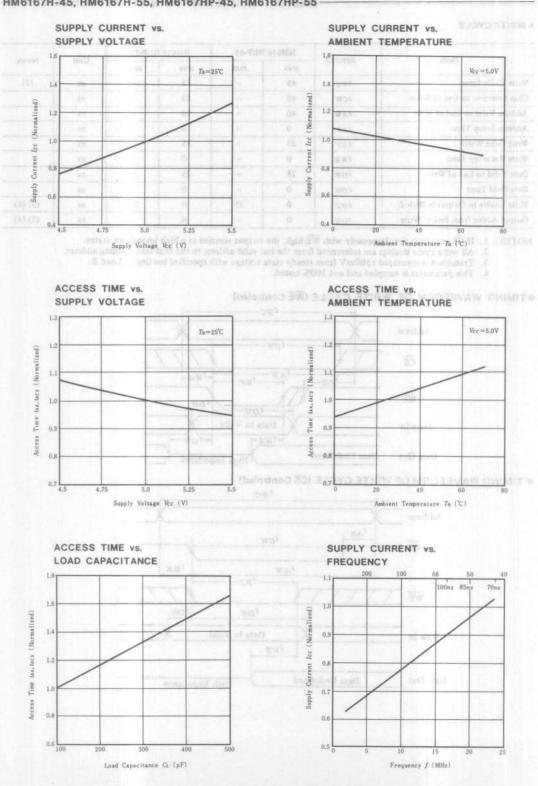




#### TIMING WAVEFORM OF WRITE CYCLE (CS Controled)

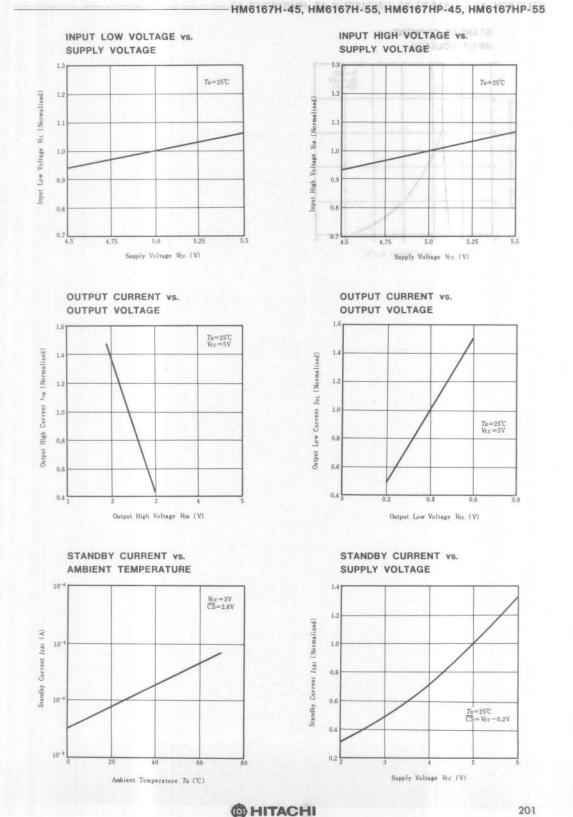


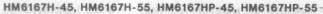


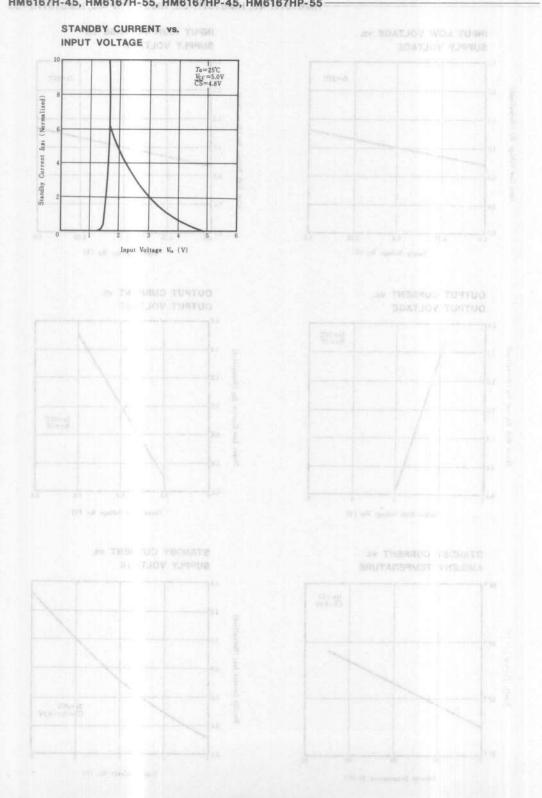


200

**OHITACHI** 







**OHITACHI** 

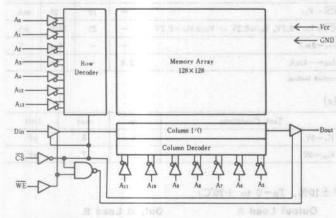
# HM6167HCG-45,HM6167HCG-55

16384-word×1-bit High Speed Static CMOS RAM

## FEATURES

- High Density 20 pin Leadless Chip Carrier
- High Speed: Fast Access Time 45/55ns Max.
- Low Power Standby and Low Power Operation Standby: 100µW typ., Operation: 200mW typ.
- Completely Static Memory;
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Output

#### BLOCK DIAGRAM



### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Voltage on Any Pin*	$V_{\tau}$	-0.5 to $+7.0$	v
Power Dissipation	P <sub>T</sub>	1.0	W
Operating Temperature	T.,,	0 to +70	.С
Storage Temperature	Tele	-65 to +150	°C
Temperature Under Bias	Think	-10 to +85	°C

BEAD CYCLE

3 A2

6 As

70 44

8 Dout

10

(CG-20)

PIN ARRANGEMENT

A12 18

Au 117

A10 16

As 115

A= 114

A: 113

19 20

ήň

Din CS GND WE (Bottom View)

#### # with respect to GND. Vin min=-3.5V (Pulse width 20ns)

#### TRUTH TABLE

CS	WE	Mode	Vcc Cur	rent	Dout Pin	Ref. Cycle
Н	×	Not selected	Isb, Is	81	High-Z	and second male and
L	Н	Read	Icc		Dout	Read Cycle
L	L	Write	Icc		High-Z	Write Cycle

the best Crown in the second of the base sets with the reach that the states where a set of the second set of t

**HITACHI** 

#### HM6167HCG-45, HM6167HCG-55-

#### **RECOMMENDED DC OPERATING CONDITIONS** (Ta=0 to $+70^{\circ}$ C)

Item	Symbol	OMOminited	betyp? dipl	max	Unit C
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V P
Input Voltage	VIH	2.2	ingless (2010) Can	6.0	V
	VIL	-0.5*	innetal amilia	0.8	V

\* -3.0V (Pulse width 20ns)

LON-OUTNOTON

## DC AND OPERATING CHARACTERISTICS (Vcc=5V ±10%, Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$\mid I_{LI} \mid$	$V_{cc}=5.5V$ , $V_{IN}=0V$ to $V_{cc}$	124100.01	10 T 11	2	μA
Output Leakage Current	ILO	$\overline{\text{CS}} = V_{IH}, V_{OUT} = 0V$ to $V_{CC}$	-	-	2	μA
Operating Power Supply Current	Ice	$\overline{CS} = V_{IL}$ , Output Open	-86	40	80	mA
	Iss	$\overline{\mathrm{CS}} = V_{IH}$	-	10	20	mA
Standby Power Supply Current	Isb1	$\overline{\text{CS}} \ge V_{cc} = 0.2 \text{V}, \ V_{lN} \le 0.2 \text{V} \text{ or } V_{lN} \ge V_{cc} = 0.2 \text{V}$	-	20	2000	μA
I ~ CRANGELIERT	Vol	IoL=8mA	-	-	0.4	V
Output Voltage	Von	Ion4mA	2.4	-	14	V

Note) \* : Typical limits are at Vcc=5.0V, Ta=25°C and specified loading.

#### **CAPACITANCE** ( $Ta = 25^{\circ}C$ , f = 1 MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cia	V0V	3	5	pF
Output Capacitance	Cast	$V_{ext} = 0V$	5	7	pF

Note) This parameter is sampled and not 100% tested.

Input Pulse Levels: GND to 3.0V

Input Rise and Fall Times: 5 ns

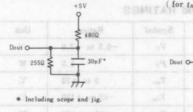
Output Reference Levels: 1.5V

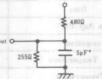
## **EAC CHARACTERISTICS** ( $V_{cc}=5V \pm 10\%$ , Ta=0 to $+70^{\circ}C$

## **AC TEST CONDITIONS**

## **Output Load A**

#### **Output Load B** (for thz, tiz, twz & tow)





+5V

**•READ CYCLE** 

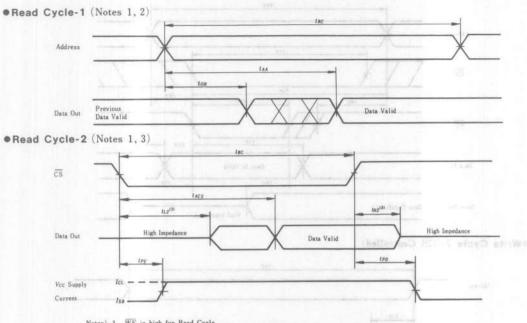
Item	0 1 1	HM6167HCG-45		HM6167HCG-55		Unit	Notes
item	Symbol	min	max	mîn	max	Unit	Notes
Read Cycle Time	tac	45	-	55	-	ns	1
Address Access Time	t <sub>AA</sub>	Periling Par	45	N	55	ns	2.0
Chip Select Access Time	tacs	101 mil	45	Distriction in	55	ns	1.0016
Output Hold from Address Change	Lo#	5	-	5		ns	
Chip Selection to Output in Low Z	tLZ	5	. <u>-</u> L.	5	-	ns	2, 3, 4
Chip Deselection to Output in High Z	t <sub>HZ</sub>	0	30	0	30	ns	2, 3, 4
Chip Selection to Power Up Time	tru	0	-	0		ns	
Chip Deselection to Power Down Time	tpp	-	30	-	30	ns	

Notes) 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.

2. At any given temperature and voltage condition,  $t_{nZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device. 3. Transition is measured  $\pm 500 \text{mV}$  from steady state voltage with specified loading in Load B.

4. This parameter is sampled and not 100% tested.





Notes) 1. WE is high for Read Cycle. 2. Address valid prior to or coincident with CS transition low. 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

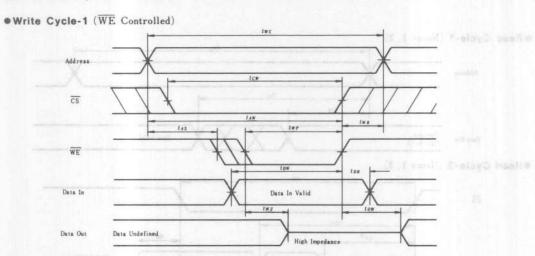
#### **WRITE CYCLE**

1. N.	Contal	HM6167	HCG-45	HM6167	HCG-55	The	Notes
Item	Symbol	min	max	min	max	Unit	Notes
Write Cycle Time	twc	45	-	55	-	ns	2
Chip Selection to End of Write	tcw	40	h	50		ns	
Address Valid to End of Write	taw	40		50	-	ns	
Address Setup Time	tAS	0	e)	0	-	ns	
Write Pulse Width	twp	25	-	35	-	ns	
Write Recovery Time	twa	0	-	0	- 600	ns	1.197
Data Valid to End of Write	t <sub>DW</sub>	25	-	25	-	ns	
Data Hold Time	t <sub>DH</sub>	0	-	0	-	ns	
Write Enable to Output in High Z	twz	0	25	0	25	ns	3,4
Output Active from End of Write	tow	0	-	0	-	ns	3,4

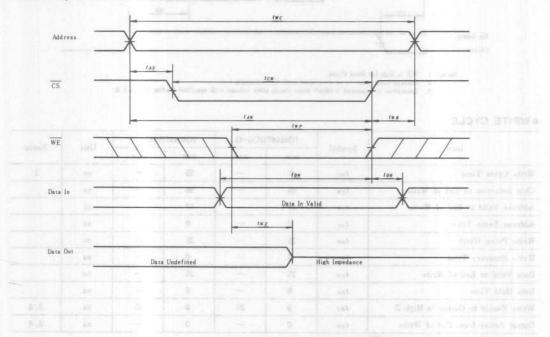
Notes) 1. If CS goes high simultaneouly with WE high, the output remains in a high impedance state.

 All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 Transition is measured ± 500mV from steady state voltage with specified loading in Load B.
 This parameter is sampled and not 100% tested.

## HM6167HCG-45, HM6167HCG-55-



• Write Cycle-2 (CS Controlled)



tion 1. I Gill you are continuedy with WE high the output transitions a bigs resolution stark

of total of principal participations with a section of the part of the section of the

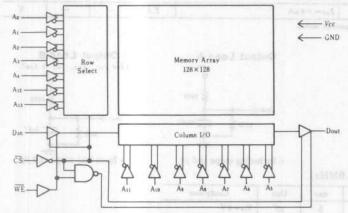
the start of the same type and prove and the start of the



16384-word x 1-bit High Speed Static CMOS RAM FEATURES

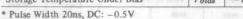
- 45ns (max) 55ns (max)
  - HM6167HLP-55
- Low Power Standby and Low Power Operation Standby 5µW (typ) and Operating 200mW (typ)
- Capable of Battery Back-up Operation
- Single +5V Supply and High Density 20 Pin Package
- Completely static Memory
- No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible . . . . All Inputs and Output

BLOCK DIAGRAM



#### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	VT	-3.5* to +7.0	V
Power Dissipation	PT	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C
Storage Temperature Under Bias	Thias	-10 to +85	°C



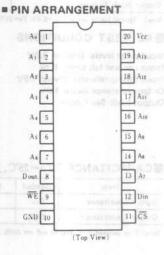
#### = RECOMMENDED DC OPERATING CONDITIONS ( $T_a = 0$ to $+70^{\circ}$ C)

Item	Symbol	min	typ	max	Unit
Councilly Malazza	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Innut Voltage	VIH	2.2	-	6.0	V
Input Voltage	VIL	-3.0*	-100	0.8	V

\* Pulse Width 20ns, DC:  $V_{IL}$  min = -0.5V

NHO BUILT FR

(DP-20)



TA CHARACT RISTICS ( Ta-

See.



#### HM6167HLP-45, HM6167HLP-55

#### TRUTH TABLE

CS	WE	Mode	Vcc Current	Dout Pin	Ref. Cycle
Н	×	Not selected	Isu, Isu	High-Z	TANT & BROWLEARD
L	н	Read	Icc	Dout	Read Cycle
L	L	Write	Icc	High-Z	Write Cycle

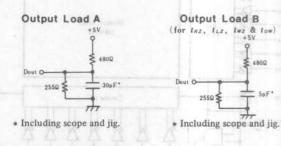
## DC AND OPERATING CHARACTERISTICS (Vcc-5V±10%, Ta=0~+70°C)

Symbol	Test Conditions	min	typ	max	Unit
ILI	$V_{cc} = 5.5 V V_{IN} = 0 V \sim V_{cc}$	the design of the st	100 2 000	2	μA
IL0	$\overline{CS} = V_{IH}, V_{wi} = 0 V - V_{cc}$	needer upper	one <u>V</u> iqu	2	μA
Icc	$\overline{CS} = V_{lL}$ , Output Open	-110	40	80	mA
Isa	$\overline{CS} = V_{IH}$		10	20	mA
I 5 81	$\overline{CS} = V_{CC} - 0.2V$ $V_{LN} \le 0.2V \text{ or } \ge V_{CC} - 0.2V$	P 100	1	50	μA
Vol	<i>I</i> <sub>0L</sub> = 8 mA	-	4.1	0.4	V
Von	$I_{ON} = -4 \mathrm{mA}$	2.4	-	+	V
	ILO   ICC ISB ISB1 VOL	$ I_{LI}  = \frac{V_{cc} - 5.5 V V_{IN} - 0 V - V_{cc}}{ I_{L0} }$ $ I_{L0}  = \frac{\overline{CS} - V_{IN}}{\overline{CS} - V_{IL}},  V_{ut} - 0 V - V_{cc}}$ $I_{cc} = \frac{\overline{CS} - V_{IL}}{\overline{CS} - V_{IL}},  Output Open$ $I_{SB} = \frac{\overline{CS} - V_{IN}}{\overline{CS} - V_{cc} - 0.2 V}$ $I_{SB1} = \frac{\overline{CS} - V_{cc} - 0.2 V}{V_{IN} \le 0.2 V \text{ or } \ge V_{cc} - 0.2 V}$ $V_{oL} = I_{oL} - 8 \text{mA}$	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $

Note) Typical limits are at Vcc-5.0V, Ta-25°C and specified loading.

#### **MAC TEST CONDITIONS**

Input pulse levels: GND to 3.0V Input rise and fall times: 5 ns Input timing reference levels: 1.5V Output reference levels: 1.5V Output load: See Figure



#### **CAPACITANCE** $(Ta=25^{\circ}C, f=1.0 \text{ MHz})$

Item	Symbol	typ.	max	Unit	Conditions	
Input Capacitance	CIN	3	5	pF	Vis-0V	
Output Capacitance	Cour	5	7	pF	Vour-OV 20MM	

Note) This parameter is sampled and not 100% tested.

## **EAC CHARACTERISTICS** ( $Ta=0^{\circ}C$ to $+70^{\circ}C$ , $V_{cc}=5V\pm10\%$ , unless otherwise noted.) **•READ CYCLE**

Item	Cumbel	HM6167HLP-45		HM616	HM6167HLP-55		Notes
Item	Symbol	min	max	min	max	Unit	Notes
Read Cycle Time	IRC	45	19050au	55	no sta on	ns	(1)
Address Access Time	t <sub>AA</sub>	1 1 - min	45		55	ns	
Chip Select Access Time	tACS	- 13	45		55	ns	
Output Hold from Address Change	toH	5	-	5	and a	ns	A Magua
Chip Selection to Output in Low Z	TLZ	5	-	5		ns	(2)(3)(7)
Chip Selection to Output in High Z	tHZ	0	30	0	30	ns	(2)(3)(7)
Chip Selection to Power Up Time	IPU	0	-	0	-	ns	
Chip Deselection to Power Down Time	IPD	-	30	-	30	ns	

NOTES: 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.

2. At any given temperature and voltage condition,  $t_{HZ}$  max. is less than  $t_{LZ}$  min. both for a given device and from device to device.

3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

4. WE is High for READ cycle.

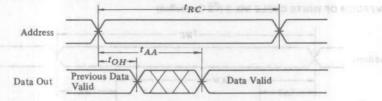
5. Device is continuously selected,  $\overline{CS} = V_{IL}$ . 6. Addresses valid prior to or coincident with  $\overline{CS}$  transition low.

7. This parameter is sampled and not 100% tested.

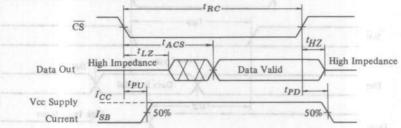


#### HM6167HLP-45, HM6167HLP-55

TIMING WAVEFORM OF READ CYCLE NO. 1 4) 5)



TIMING WAVEFORM OF READ CYCLE NO. 2 4) 6



. WRITE CYCLE

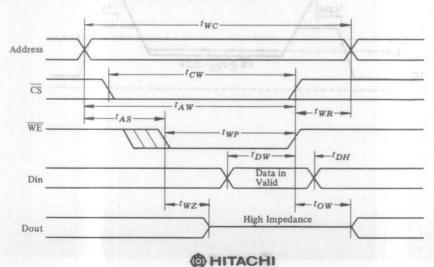
1	Cumhal	HM6167HLP-45		HM6167HLP-55		Unit	Martin
Item	Symbol	min	max	min	max	Onit	Notes
Write Cycle Time	twc	45	1437.36	55	AT 8 2157	ns	(2)
Chip Selection to End of Write	tcw	40	-	50	-	ns	
Address Valid to End of Write	tAW	40	-	50	-	ns	and and and
Address Setup Time	IAS	0	N 575	0	-	ns	
Write Pulse Width	tWP	25		35	-	ns	ato Donie
Write Recovery Time	twR	0	-	0	-	ns	
Data Valid to End of Write	tDW	25		25	Devis Sciences	ns	
Data Hold Time	tDH .	0	- :	0	-	ns	A BUILD CARD
Write Enable to Output in High Z	twz	0	25	0	25	ns	(3) (4)
Output Active from End of Write	tow	0	-	0	-	ns	(3) (4)

NOTES: 1. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance states.

All Write Cycle timings are referenced from the last valid address to the first transitions address.
 Transition is measured ±500mV from steady state voltage with specified loading in Load B.

4. This parameter is sampled and not 100% tested.

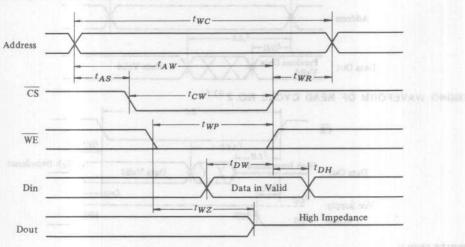
**TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE Controlled)** 



#### HM6167HLP-45, HM6167HLP-55-

ATTRACK WAVEFORM OF READ CYCLE NO. 1 ...

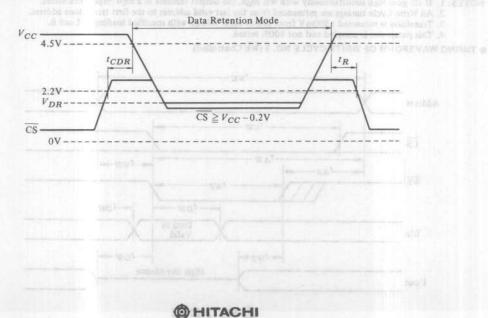
• TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS Controlled)

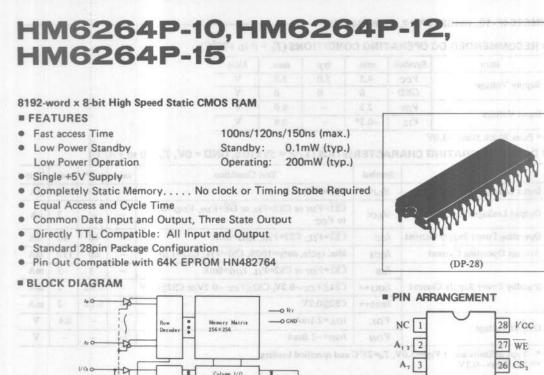


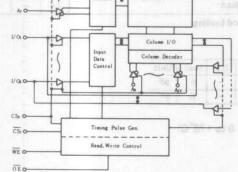
LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Symbol	Test Conditio	min	typ	max	Unit		
VDR	40	184.0	2.0	10192	ond <del>as</del> hits	V	
	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}$	8.4.5	-	-	20*	e investiga	
ICCDR	$V_{a} \ge V_{cc} = 0.2 V$ or	1011	-	-	30**	μA	
tcox	tcor	$0 V \le V_{i*} \le 0.2 V$	5.93	0			ns
t n		19401	IRC <sup>6</sup>	-	-	ns	
0.	2 A 1	-Read Cycl	e Time	The second		Vec = 2.0	
	Vor Iccor Iccar	$ \frac{V_{DR}}{I_{CCDR}} = \frac{\overline{CS} \ge V_{CC} - 0.2V}{V_{*} \ge V_{CC} - 0.2V} \text{ or} $ $ \frac{t_{CDR}}{t_{R}} = 0V \le V_{*} \le 0.2V $		$V_{DR}$ 2.0 $I_{CCDR}$ $\overline{CS} \ge V_{CC} - 0.2V$ $ V_{cab} \ge V_{CC} - 0.2V$ or $ V_{cab} \ge V_{cc} - 0.2V$ or $ t_{CDR}$ $0V \le V_{ca} \le 0.2V$ $0$	$V_{DR}$ 2.0         - $I_{CCDR}$ $\overline{CS} \ge V_{CC} - 0.2V$ -         - $V_{CR}$ $V_{CC} - 0.2V$ -         - $V_{CR}$ $V_{CC} - 0.2V$ or         -         - $V_{CR}$ $0V \le V_{CC} = 0.2V$ or         -         - $t_{RC}$ $0V \le V_{CC} = 0.2V$ or         -         - $t_{R}$ $0V \le V_{CC} = 0.2V$ or         -         -	$V_{0R}$ $2.0$ $ I_{CCDR}$ $\overline{CS} \ge V_{CC} - 0.2V$ $  I_{CCDR}$ $V_{**} \ge V_{CC} - 0.2V$ or $  20^{*}$ $t_{CDR}$ $0V \le V_{**} \le 0.2V$ $0$ $  t_R$ $0V \le V_{**} \le 0.2V$ $0$ $  t_R$ $t_{RC} = \text{Read Cycle Time}$ *	

**eLOW Vcc DATA RETENTION WAVEFORM** 









Item	Symbol	Rating	Unit
Terminal Voltage *	Vт	-0.5 ** to +7.0	v
Power Dissipation	Рт	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C
Storage Temperature (Under Bias)	Thias	-10 to +85	°C

\* With respect to GND. \*\* Pulse width 50ns: -3.0V

- TRUTH TARLE

WE	CS,	CS, CS, OE M		Mode	V <sub>CC</sub> Current	Note		
Х	H	X	X	Not Selected	High Z	ISB, ISB1		
X	X	L	X	(Power Down)	High Z	ISB, ISB2	127 BUSSIN	
Н	L	H	H	Output Disabled	High Z	ICC, ICC1		
H	L	H	L	Read	Dout	ICC, ICC1	ru -un arsteurs	
L	L	H	H	Write	Din	Icc, Icc1	Write Cycle (1)	
L	L	H	L	WINC	Din	ICC, ICC1	Write Cycle (2)	

× : Don't care.

(Top View)

NC 1	28 Vcc
A12 2	27 WE
A, 3	26 CS <sub>2</sub>
A <sub>6</sub> 4	25 A.
A 5	24 A,
A. 6	23 A <sub>11</sub>
A <sub>3</sub> 7	22 OE
A2 8	21 A <sub>10</sub>
A, 9	20 CS,
A. 10	19 I/O <sub>8</sub>
I/O, 11	18 I/O <sub>7</sub>
I/O2 12	17 I/O <sub>6</sub>
I/O <sub>3</sub> 13	16 I/O <sub>s</sub>
GND 14	15 I/O4

**OHITACHI** 

#### HM6264P-10, HM6264P-12, HM6264P-15

## ■ RECOMMENDED DC OPERATING CONDITIONS (T<sub>a</sub> = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
0	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
	VIH	2.2	-	6.0	V
Input Voltage	VIL	-0.3*	-	0.8	V

\* Pulse Width 50ns: -3.0V

## = DC AND OPERATING CHARACTERISTICS ( $V_{CC}$ = 5V±10%, GND = 0V, $T_a$ = 0 to +70°C)

1 Beer and the beer and				1	1	1
Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	ILI	Vin=GND to VCC	sNL-3	112 V	2	μA
Output Leakage Current	ILO	$\overline{\text{CS1}}=V_{IH}$ or $\text{CS2}=V_{IL}$ or $\overline{\text{OE}}=V_{IH}$ , $V_{I/O}=\text{GND}$ to $V_{CC}$	an <u>a</u> n	is sin stille		μA
Operating Power Supply Current	Icc	CS1=VIL, CS2=VIH, II/O=0mA	100 m		80	mA
Average Operating Current	Icc1	Min. cycle, duty=100%, CS1=VIL, CS2=VIH	60	110	mA	
verage Operating Current	ISB	CS1=VIH or CS2=VIL, II/O=0mA	-	1	3	mA
Standby Power Supply Current	ISB1**	$\overline{\text{CS1}} \ge V_{CC} - 0.2 \text{V}, \text{CS2} \ge V_{CC} - 0.2 \text{V} \text{ or } \text{CS2} \le 0.2 \text{V}$	1.10	0.02	2	mA
TN5MSBMARA M	ISB2**	CS2≦0.2V	32	0.02	2 2 80 110 3	mA
O THE REAL	VOL	IOL=2.1mA	+	-	0.4	V
Output Voltage	VOH	IOH=-1.0mA	2.4	-	2 80 110 3 2 2 2 0.4	V

8192 word a S-bit High Speed Statis Chit

PRINTAR MUNIXAM BYULIO2BA #

FEATURES
 Fast attest Time

\* Typical limits are at Vcc=5.0V, Ta=25°C and specified loading.

\*\* VIL min=-0.3V

#### **CAPACITANCE** (f = 1MHz, $T_a = 25^{\circ}$ C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0V$	1+1	6	pF
Input/Output Capacitance	C1/0	$V_{I/O} = 0V$	-	8	pF

Note) This parameter is sampled and not 100% tested.

#### = AC CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ , Ta = 0 to $+70^{\circ}$ C)

#### AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

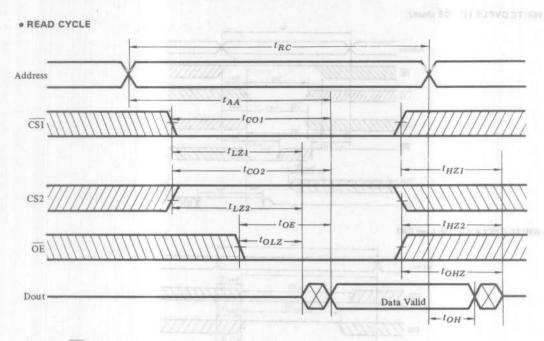
Output Load: 1TTL Gate and  $C_L$  = 100pF (including scope and jig)

#### READ CYCLE

Ton Fa	L'ON .		HM62	64P-10	HM62	64P-12	HM62	64P-15	
,ou be	- 40	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	Cillion .	IRC	100	11-21-53	120	10 -	150	ner single	ns
Address Access Time		tAA	1	100		120	a modern	150	ns
Chip Selection to Output	CS1	tco1	41	100	1 2000	120	1. C	150	ns
	CS2	tCO2	-	100	-	120	-	150	ns
Output Enable to Output Valid		toe	<u>a</u> g 0	50	-	60	-	70	ns
Chip Selection to	CS1	tLZ1	10		10	Selected	15	-	ns
Output in Low Z	CS2	ILZ2	10	-	10	fuel They	15	T	ns
Output Enable to Output in	Low Z	tolz	5	-	5	- b	5	14	ns
Chip Deselection to	CS1	tHZ1	0	35	0	40	0	50	ns
Output in High Z	CS2	tHZ2	0	35	0	40	0	50	ns
Output Disable to Output in	High Z	10HZ	0	35	0	40	0	50	ns
Output Hold from Address	Change	tOH	10	-	10	-	15	-	ns

NOTES: 1  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

2 At any given temperature and voltage condition, t<sub>HZ</sub> max is less than t<sub>LZ</sub> min both for a given device and from device to device.



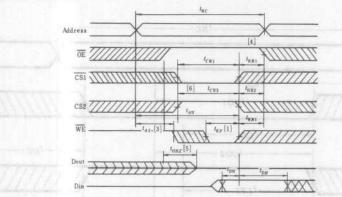
NOTE: 1) WE is high for Read Cycle

Thomas	Item		HM6264P-10		HM62	HM6264P-12		64P-15	Unit
Item		Symbol	min	max	min	max	min	max	Onn
Write Cycle Time		twc	100	ta deci o	120	d and	150	ni u <del>ni</del> ayo	ns
Chip Selection to End of Write		tċw	80	an and a	85	Coloradore	100	a light of the	ns
Address Setup Time		tAS	0	NOI STORES	0	d nite more	0	10-000	ns
Address Valid to End of Write		tAW	80	and Thir or	85	the silt of	100	1000 500 1001 100 4 10	ns
Write Pulse Width		twp	60	Sing 2011 (1	70	an adl un	90	$E = \frac{1}{2} $	ns
Write Recovery Time	CS1, WE	tWR1	5	ol ginda (	5	이 아이 아이 아이 아이	10	-	ns
white Recovery Tune	CS2	twR2	15	201 10 91 9	15	add <u>a</u> Od	15	aning (	ns
Write to Output in High 2	2	tWHZ	0	35	0	40	0	50	ns
Data to Write Time Overlap		tDW	40		50	-	60	1915 <u>- 1</u> 931 	ns
Data Hold from Write Time		t <sub>DH</sub>	0		0	n an l <del>i a</del> n rai	0	o indi	ns
OE to Output in High Z		tOHZ	0	35	0	40	0	50	ns
Output Active from End	of Write	tow	5	-	5	hellage se	10	n un <del>po</del> it	ns

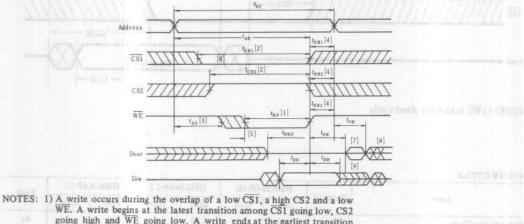
# () HITACHI

#### HM6264P-10, HM6264P-12, HM6264P-15





. WRITE CYCLE (2) (OE Low Fix)



WE. A write begins at the latest transition among CS1 going low, CS2 going high and WE going low. A write ends at the earliest transition among CS1 going high, CS2 going low and WE going high. twp is measured from the beginninng of write to the end of write.
2) t<sub>CW</sub> is measured from the later of CS1 going low or CS2 going high to

the end of write.

3)  $t_{AS}$  is measured from the address valid to the beginning of write. 4)  $t_{WR}$  is measured from the end of write to the address change.

 $t_{WR1}$  applies in case a write ends at CS1 or WE going high.  $t_{WR2}$  applies in case a write ends at CS2 going low.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If CS1 goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.

7) Dout is in the same phase of written data of this cycle.

8) Dout is the read data of the new address.

9) If CS1 is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

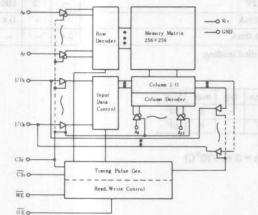
**OHITACHI** 

# HM6264LP-10, HM6264LP-12 HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

- **FEATURES**
- Fast access Time
- Low Power Standby Low Power Operation
- 100ns/120ns/150ns (max.) Standby: 0.01mW(typ.) Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory.... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

#### BLOCK DIAGRAM



# WWWWWWW (DP-28)

#### NC 1 28 VCC A12 2 27 WE A7 3 26 CS2 A. 4 25 A8 24 A. A. 5 A. 6 23 A11 A, 7 22 OE A2 8 21 A10 A, 9 20 CS. A. 10 19 I/O. 1/0, 11 18 I/O7 1/0, 12 17 I/O. 1/0,13 16 I/Os GND 14 15 I/O,

## ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Terminal Voltage *	VT	-0.5 ** to +7.0	V	
Power Dissipation	Рт	1.0	W	
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tstg	-55 to +125	°C	
Storage Temperature (Under Bias)	Toias	-10 to +85	°C	

\* With respect to GND. \*\* Pulse width 50ns: -3.0V

#### TRUTH TARLE

WE	CS <sub>1</sub>	CS,	OE	Mode	I/O Pin	V <sub>CC</sub> Current	Note
Х	H	X	X	Not Selected	High Z	/SB, /SB1	T and all
Χ′	X	L	X	(Power Down)	High Z	ISB, ISB2	-
Н	L	H	Н	Output Disabled	High Z	ICC, ICC1	The DO BE MORES
H	L	H	L	Read	Dout	ICC, ICC1	- m soussie
L	L	H	H	Write	Din	Icc, Icc1	Write Cycle (1)
L	L	H	L	WITTE	Din	ICC, ICC1	Write Cycle (2)

× : Don't care.

## PIN ARRANGEMENT

1	en no ne mones
	in nonesis.
	Write Cycle (1
	Write Cycle (2

(Top View)



#### HM6264LP-10, HM6264LP-12, HM6264LP-15-

# RECOMMENDED DC OPERATING CONDITIONS (T<sub>a</sub> = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Cumples Malters	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Inner Valence	VIH	2.2	-	6.0	V
Input Voltage	VIL	-0.3*	-	0.8	V

\* Pulse Width 50ns: -3.0V

# • DC AND OPERATING CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ , GND = 0V, $T_a = 0$ to $+70^{\circ}$ C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	ILI	Vin=GND to VCC	- 1	1002	2	μA
utput Leakage Current $ I_{LO} $ $\frac{\overline{CS1} = V_{IH} \text{ or } CS2 = V_{IL} \text{ or } \overline{OE} = V_{IH}, V_{I/O} = GND$ to $V_{CC}$		1	nctike	2	μA	
Operating Power Supply Current	Icc	CS1=VIL, CS2=VIH, II/O=0mA	1231	40	80	mA
Average Operating Current	Icc1	Min. cycle, duty=100%, $\overline{\text{CS1}}=V_{IL}$ , $\text{CS2}=V_{IH}$	5	60	110	mA
	ISB	$\overline{\text{CS1}}=V_{IH}$ or $\text{CS2}=V_{IL}$ , $I_{I/O}=0$ mA		1	3	mA
Standby Power Supply Current	ISB1**	$\overline{\text{CS1}} \ge V_{CC} - 0.2 \text{V}, \text{CS2} \ge V_{CC} - 0.2 \text{V} \text{ or } \text{CS2} \le 0.2 \text{V}$	-	2	100	μA
THREETRAGE	ISB2**	CS2≦0.2V	-	2	100	μA
Outrast Values	VOL	IOL=2.1mA	12	-	0.4	V
Output Voltage	VOH	<i>IOH</i> =-1.0mA	2.4	-	-	V

\* Typical limits are at Vcc=5.0V, Ta=25°C and specified loading.

\*\* VIL min=-0.3V

## **CAPACITANCE** (f = 1MHz, $T_a = 25^{\circ}$ C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	Cin	$V_{in} = 0V$	-	6	pF
Input/Output Capacitance	C1/0	$V_{I/O} = 0V$	-	8	pF

Note) This parameter is sampled and not 100% tested.

#### • AC CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ , Ta = 0 to $\pm 70^{\circ}$ C)

#### AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and  $C_L = 100 pF$  (including scope and jig)

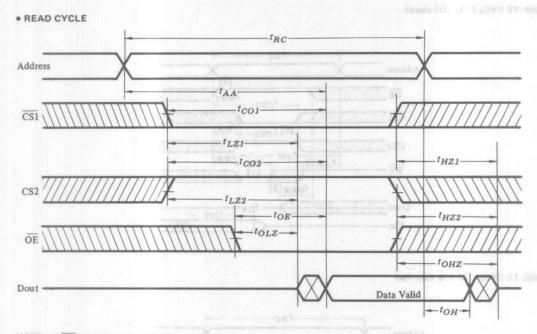
#### READ CYCLE

		Cumhal	HM620	64LP-10	HM626	64LP-12	HM626	64LP-15				
tem		Symbol	min	max	min	max	min	max	Unit			
	08	tRC	100	007010	120	-	150	and the state	ns			
ne	- CINID	IAA	-	100	-	120	-	150	ns			
	CS1	ICO1	-	100	_ 10	120	i m <u>ba</u> U	150	ns			
Jutput	CS2	1002	-	100	6 + <u>2</u> mic	120	- L	150	ns			
Output Enable to Output Valid			-	50	-	60	-	70	ns			
_	CS1	ILZ1	10	-	10	PONC	15	0	ns			
	CS2	tLZ2	10		10	AND STREET	15		ns			
Output in	Low Z	IOLZ	5	-	5	Hart True	5	-	ns			
0	CS1	tHZ1	0	35	0	40	0	50	ns			
With	CS2	tHZ2	0	35	0	40	0	50	ns			
Output Disable to Output in High Z			0	35	0	40	0	50	ns			
Output Hold from Address Change			10	-	10	-	15	-	ns			
	Output Va Output Va Output in Output in	ne CS1 CS2 Output Valid CS2 Output Valid CS1 CS2 Output in Low Z o CS1 CS2 Output in Hop Z Output in High Z	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	tem Symbol min tracestary for the symbol min symbol min symbol min symbol min symbol symbol symbol min symbol min symbol symbo	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Symbol         min         max         min           min         max         min         max         min           trac         100         -         120           ne         trac         min         max         min           trac         100         -           CS1         trac         50         -           CS1         trac         50         -           CS1         trac         5         -         5         -         5         -         5         -         5         -         5         -         5         -         5         -         5         -         5         -         5         -         5         -         5         - <th< td=""><td>Symbol         min         max         min         max           tRC         100         -         120         -           ne         tAA         -         120         -           Output         CS1         tCO1         -         100         -         120           Output         CS2         tCO2         -         100         -         100           Output Valid         tOE         CS1         tLZ2         10         -         60           CS1         tLZ2         10         -         10           CS1         tLZ2         10         -         10           CS1         tHZ1         0         35         0         40           CS1         tHZ2         0         35         0<td>Symbol         min         max         min         min         max         min         max         min         max         min         max         min         min         max         min                  <th colspan="2" min<<="" td=""><td>Symbol         min         max           trac         120         -         150           CS1         trac         100         -         100         -         150           CS2         trac         -         60         -         70           CS1         trac         -         5         -         5           CS1         trac         5         -         5           CS1         trac         5         -         5           CS1         trac          -         <th col<="" td=""></th></td></th></td></td></th<>	Symbol         min         max         min         max           tRC         100         -         120         -           ne         tAA         -         120         -           Output         CS1         tCO1         -         100         -         120           Output         CS2         tCO2         -         100         -         100           Output Valid         tOE         CS1         tLZ2         10         -         60           CS1         tLZ2         10         -         10           CS1         tLZ2         10         -         10           CS1         tHZ1         0         35         0         40           CS1         tHZ2         0         35         0 <td>Symbol         min         max         min         min         max         min         max         min         max         min         max         min         min         max         min                  <th colspan="2" min<<="" td=""><td>Symbol         min         max           trac         120         -         150           CS1         trac         100         -         100         -         150           CS2         trac         -         60         -         70           CS1         trac         -         5         -         5           CS1         trac         5         -         5           CS1         trac         5         -         5           CS1         trac          -         <th col<="" td=""></th></td></th></td>	Symbol         min         max         min         min         max         min         max         min         max         min         max         min         min         max         min         min <th colspan="2" min<<="" td=""><td>Symbol         min         max           trac         120         -         150           CS1         trac         100         -         100         -         150           CS2         trac         -         60         -         70           CS1         trac         -         5         -         5           CS1         trac         5         -         5           CS1         trac         5         -         5           CS1         trac          -         <th col<="" td=""></th></td></th>	<td>Symbol         min         max           trac         120         -         150           CS1         trac         100         -         100         -         150           CS2         trac         -         60         -         70           CS1         trac         -         5         -         5           CS1         trac         5         -         5           CS1         trac         5         -         5           CS1         trac          -         <th col<="" td=""></th></td>		Symbol         min         max           trac         120         -         150           CS1         trac         100         -         100         -         150           CS2         trac         -         60         -         70           CS1         trac         -         5         -         5           CS1         trac         5         -         5           CS1         trac         5         -         5           CS1         trac          - <th col<="" td=""></th>	

NOTES: 1  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

O HITACHI

2 At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.



NOTE : 1) WE is high for Read Cycle

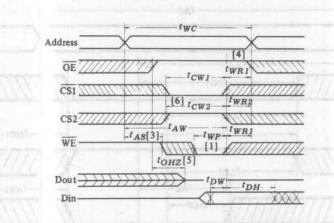
There	100000	Contraction (Contraction)	HM6264LP-10		HM6264LP-12		HM6264LP-15		TINIA
Item	Symbol	min	max	min	max	min	max	Unit	
Write Cycle Time		twc	100	-	120	-	150	-	ns
Chip Selection to End of Write		tcw	80	2 2.	85	TT-mol	100	-	ns
Address Setup Time		TAS	0	-	0	-	0	-	ns
Address Valid to End of Write		LAW	80	-	85	Dist_	100	-	ns
Write Pulse Width		tWP	60	-	70	-	90	-	пs
Write Recovery Time	CS1, WE	twR1	5	-	5	-	10	-	ns
while Recovery Thile	CS2	IWR2	15	-	15	-	15	-	ns
Write to Output in High 2	Z	twhz	0	35	0	40	0	50	ns
Data to Write Time Overlap		tDW	40	10.17000	50	of sets in	60		ns
Data Hold from Write Time		t DH	0	-	0	6. <u>–</u> 200	0	10000	ns
OE to Output in High Z		tohz	0	35	0	40	0	50	ns
Output Active from End of Write		tow	5		5	The Tax and	10	10012 1000	ns

(i) (i) a bit server of from the end-of write, to the address cherror, by g) internal to case a write ends at CS1 or OS going high from g update at case a write ends at CS2 going low.

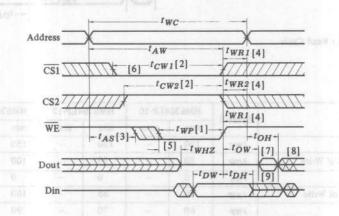


#### HM6264LP-10, HM6264LP-12, HM6264LP-15-

#### . WRITE CYCLE (1) (OE clock)



. WRITE CYCLE (2) (OE Low Fix)



- NOTES: 1) A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2 and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low and  $\overline{WE}$  going high,  $f_{WP}$  is measured from the beginning of write to the end of write.
  - t<sub>CW</sub> is measured from the later of CS1 going low or CS2 going high to the end of write.
  - 3)  $t_{AS}$  is measured from the address valid to the beginning of write.
  - 4) f<sub>WR</sub> is measured from the end of write to the address change. f<sub>WR1</sub> applies in case a write ends at CS1 or WE going high. f<sub>WR2</sub> applies in case a write ends at CS2 going low.
  - 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
  - 6) If CS1 goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.
  - 7) Dout is in the same phase of written data of this cycle.
  - 8) Dout is the read data of the new address.
  - 9) If CS1 is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.



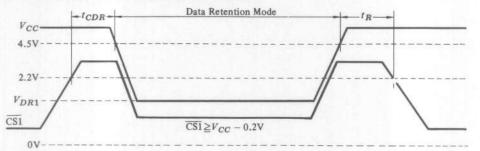
Item	Symbol	Test Condition	min	typ	max	Unit
V Co Data Detection	V <sub>DR1</sub>	$1 \qquad \overline{\text{CS1}} \ge V_{CC} - 0.2 \text{V}, \text{CS2} \ge V_{CC} - 0.2 \text{V} \text{ or } \text{CS2} \le 0.2 \text{V}$		-	-	V
$V_{CC}$ for Data Retention	V <sub>DR2</sub>	$CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I <sub>CCDR1</sub>	$\begin{array}{c} V_{CC} = 3.0 \text{V}, \overline{\text{CS1}} \geq V_{CC} - 0.2 \text{V}, \\ \text{CS2} \geq V_{CC} - 0.2 \text{V} \text{ or } \text{CS2} \leq 0.2 \text{V} \end{array}$		1	50*	μA
Data Retention Current	I <sub>CCDR2</sub>	$V_{CC} = 3.0$ V, CS2 $\leq 0.2$ V	-	1	50*	μA
Chip Deselect to Data Retention t <sub>CDR</sub>		See Retention Waveform	0	-	-	ns
Operation Recovery Time	tR		IRC**	-	-	ns

**LOW**  $V_{CC}$  DATA RETENTION CHARACTERISTICS ( $T_a = 0$  to +70 °C)

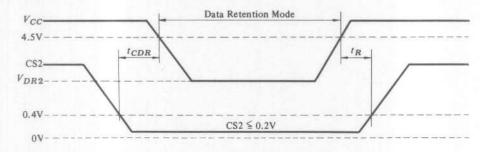
\*  $V_{IL}$  min = -0.3V

\*\* t<sub>RC</sub> = Read Cycle Time

LOW Vcc DATA RETENTION WAVEFORM (1) (CS1 Controlled)



#### • LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: CS<sub>2</sub> controls Address buffer,  $\overline{WE}$  buffer,  $\overline{CS}_1$  buffer and Din buffer. If CS<sub>2</sub> controls data retention mode, Vin level (Address,  $\overline{WE}$ ,  $\overline{CS}_1$ , I/O) can be in the high impedance state. If  $\overline{CS}_1$  controls data retention mode, CS<sub>2</sub> must be CS<sub>2</sub>  $\geq$  Vcc-0.2V or CS<sub>2</sub>  $\leq$  0.2V. The other inputs level (address,  $\overline{WE}$ , I/O) can be in the high impedance state.

**OHITACHI** 

HORIZGALP-10, HIMM: 11, P-12; HM6264LP-13

I LOW N.Y. BATA RETENTION CHARACTERIZTICS (T. + 0 10 + 10 °C)

	Call 2 Mr. 131 2 Frag 0.1V.			
<sup>7</sup> C2IK	See Xerenties Waveford			

VE.0 - + alm white

TT MTCHESS - DRIVE

LOW Ver DATA TETENTION WAREFORM (1) 1031 Controlled



(Bullowerd) SEG). (S) MROHEVAW MOTOSTER ATAG on WOU #



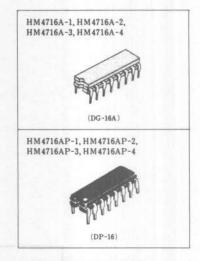
OTE: (3) Executed relation buffer, We buffer, CS, buffer and Din turbler, H (2), controls due remains more, Vits beal (Address, WE, CS, 100) can be in the high medianes area, if CS, controls data contribut much. (5), must be CS, given-0.2V or CS, (6).2V. The allor agains level (address, WE, 10) can be control with impedance state.

			HM4716A-1, HM4716A-	
		. flan	HM4716A-3, HM4716A	
	S	-9A	HM4716AP-1, HM4716/	
		AF	HM4716AP-3,HM4716	
1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1			18334-word + 1-bit Dynamic Random Access Memory The HM718A is 1 15,384 word by 1 bit MDS random actes memory clinat Limitated with HITACH1's double poly Mehaned silicon gete process for high performance and high functional detailty. The HM4/ I6A uses 3 single transistor dynamic storeg cell additionation ministry of a solitise high scred and low now discinstion. Multither detailing to active high scred and low now discinstion. Multither to active high scred and low now discinstion. Multither to active high scred and low now discinstion. Multither to the first the HM4716A to be and theorem the start and the off of 0.3 inch centers. This neckage the attact was method and the first the HM4716A to be acter modules from puter start and is compatible with white will be automated testing and insertion equipment. The HM4716A to detaged in a rate testing and insertion equipment. The HM4716A to prove the first output leach more personal the detain at the prove that output leach more personal to the securit 4K detain to produce (T6K R A-MM and RAM's This new generation of memory differed automated in the detain of the securit 4K detain produce (T6K R A-MM and the securit 5C detain and produce (T6K R A-MM and the securit active to personalize the first the conventional lateh, m produce the first the HM716A will remain valid from the access the high (T6K R A-MM and the securit AK detain to detain the first on the securit first. Data secure the HM716A will remain valid from the access the first on the the HM716A will remain valid from the access the first on the material first secure at the first on the secure first first. Data secure the HM716A will remain valid from the access the first on the first secure at the first on the secure test of the secure of the HM716A will remain valid from the access the first on the first secure first secure first secure first on the secure test of the first secure of the HM716A will remain valid from the access to the first secure of the HM716A will remain valid from the access test of the	
	Γ		<ul> <li>both (1) Movement suffy write evolve (W extremised End goest how), the data output will remain in the high impedance (open-</li> </ul>	
TREND	NPANO	211月11日		
			MUS UYNAMIC KAM	
	_	100	data in can be concerted directly to data-out-on a printed about	
			TCELOV until CE numero procharge.	
			<ol> <li>Two Methods (* Chip Selection)</li> </ol>	
			Brain CLI and/or FT, can be discuted for ship selection. Refinition	
			Refeating can be accorptioned every 2 ms by either of the two	
	weld			
			(1) normal read of write cycles on 128 addresses, A0 to Ait,	
			(2) P.E. unity cycles for 128 addinases, AD to AE, A write cycle with in truth stated data on all bits of the setucited row.	
			RE only infraction results in a substantial reduction in operating	

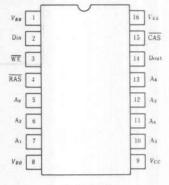
() HITACHI

#### 16384-word × 1-bit Dynamic Random Access Memory

The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe (CE). Data out of the HM4716A will remain valid from the access time from the Column Address Strobe until CE goes into precharge logic 1). However, in early write cycles (W active low before CE goes low), the data output will remain in the high impedance (opencircuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.



#### PIN ARRANGEMENT





Old	New	Definitions
A0 - A6	A0-A6	Address Inputs
CAS	CE	Column Address Strobe
Din	D	Data In
Dout	Q	Data Out
RAS	RE	Row Address Strobe
WRITE	W	Read/Write Input
VBB	VBB	Power (-5V)
Vcc	VCC	Power (+5V)
VDD	VDD	Power (+12V)
V35	VSS	Ground

#### 1. Common I/O Operation

If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.

2. Data Output Control

Data will remain valid at the output during a read cycle from TCELQV until  $\overline{CE}$  returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods of Chip Selection

Both  $\overline{CE}$  and/or  $\overline{RE}$  can be decoded for chip selection.

4. Refresh

Refreshing can be accomplished every 2 ms by either of the two following methods:

(1) normal read or write cycles on 128 addresses, A0 to A6.

(2) RE only cycles on 128 addresses, A0 to A6.

A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

 $\overline{\mathsf{RE}}$  only refreshes results in a substantial reduction in operating power.

5. Page Mode Operation

The HM4716A is designed for page mode operation.

# C HITACHI

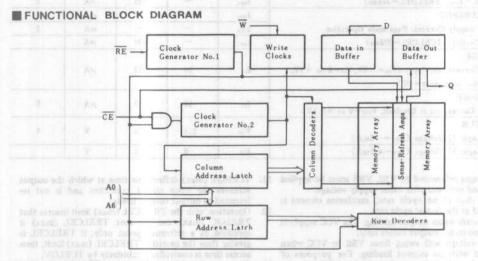
## FEATURES

- All Inputs Including Clocks TTL Compatible
- Input Latches for Address and Data in
- Three-State TTL Compatible Output
- Common I/O Capability
- Only 128 Refresh Cycles Required Every 2ms
- Standard Power Supplies +12V, +5V, -5V (All with 10% tolelance)

Maximum Access Time
HM4716A-1 120ns
HM4716A-2 150ns
HM4716A-3 200ns
HM4716A-4 250ns
Read or Write Cycle Time
HM4716A-1 320ns
HM4716A-2 320ns
HM4716A-3 375ns
HM4716A-4 410ns

BOC BLECTHONE CRARNOTERISTICS

i lort i .....



### ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to VBB0.5V to +20V	
Voltage on VDD, VCC Supplies Relative to VSS0.5V to +15V	
Voltage on Q Pin Relative to VSS0.5V to +10V	
Operating Temperature, TA (Ambient) · · · · · · · · · · · · · 0°C to +70°C	
Storage Temperature (Ambient)*	
Short-Circuit Output Current	
Power Dissipation 1W	
* In case of HM4716AP Series are -55°C to +125°C.	

# RECOMMENDED DC OPERATING CONDITIONS (TA-0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
	VDD	10.8	12.0	13.2	V	19.10
	VCC	4.5	5.0	5.5 0 -5.5	v	101
Supply Voltage	VSS	0	0		v	1 1
	VBB	-4.5	-5.0		v	
Input High (logic 1) Voltage RE, CE, W	VIHC	2.7	-	6.5	V	1
Input High (logic 1) Voltage All inputs except RE, CE, W	VIH	2.4	-	6.5	v	1
Input Low (logic 0) Voltage all inputs	VIL	-1.0	-	0.8	V	1



#### DC ELECTRICAL CHARACTERISTICS

(Ta=0 to +70°C, VDD=12)	$V \pm 10\%, V_{cc} = 5V \pm 10\%,$	$V_{BB} = -5V \pm 10\%, V_{SS} = 0V$
-------------------------	-------------------------------------	--------------------------------------

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT	IDD1	10(#)O	35	mA	2
Average Power Supply Operating Current	Icc1	-	V#in.	mA	3
(RE, CE Cycling; TRELREL=375ns)	IBBI	puited Even	300	μA	2
STANDBY CURRENT	IDDI	- N2+ V	1.5	mA	Sundar
Power Supply Standby Current	Iccz	-10	10	μA	5
$(\overline{\text{RE}} = \overline{\text{CE}} = V_{IBC})$	IBB2	-	100	/*A	
REFRESH CURRENT	IDD3	-	27	mA	2
Average Power Supply Current, Refresh Mode	leca	-10	10	μA	5
$(\overline{\text{RE}} \text{ Cycling}, \overline{\text{CE}} = V_{IRC}; \text{ TRELREL} = 375 \text{ ns})$	Івва	-	300	μA	2
PAGE MODE CURRENT	IDD4	MARE	27	mA	TOHUT
Average Power Supply Current, Page-mode Operation	Icc .	-	-	mA	3
$(\overline{\text{RE}} = V_{lL}, \overline{\text{CE}} \text{ Cycling}; \text{ TCELCEL}= 225 \text{ ns})$	IBB4	-	300	μA	
INPUT LEAKAGE	3 T	ST. Station	10		
Input Leakage Current, any Input ( $V_{BB} = -5V$ , $V_{IN} = 0$ to $+7V$ ,	Lin	-10	10	μA	
all other pins not under test = 0V)					
OUTPUT LEAKAGE	Int	-10	10	μA	5
Output Leakage Current (Q is Disabled, Vour=0 to +5.5V)	101	10	10	PA .	
OUTPUT LEVELS	Von	2.4	Vcc	v	4
Output High (Logic 1) Voltage (Iovr=-5mA)	YON	6.4	VCC		
Output Low (Logic 0) Voltage (Iour=4.2mA)	VoL	0	0.4	v	

**CHITACHI** 

NOTES

- 1. All voltages referenced to VSS, VBB must be applied 11. TCEHQZ (max) defines the time at which the output before and removed after other supply voltage.
- 2. Current depend on cycle rate: maximum current is measured at the fastest cycle rate.
- 3. ICC depends upon output loading. The VCC supply is connected to the output buffer only.
- 4. Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be 13. reduced to VSS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.
- 5. ICC2, ICC3 and IOL consists of leakage current only.
- 6. AC measurements assume TT = 5ns.
- 7. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VILS.
- 8. Assumes that TRELCEL = TRELCEL (max.) If TRELCEL is greater than the maximum recommended value shown in this table, TRELQV exceeds the value shown.
- 9. Assumes that TRELCEL = TRELCEL (max).
- Measured with a load circuit equivalent to 2TTL loads 16.  $\overline{CE} = VIHC$  to disable Q. 10. and 100pF (in case of HM4716A-2:1 TTL and 50pF). And VSS + 0.8V, VSS + 2.0V are the reference level for measuring timing of Q.

- achieves the open circuit condition and is not referenced to output voltage levels.
- 12. Operation with the TRELCEL (max) limit insures that TRELQC (max) can be met TRELCEL (max) is specified as a reference point only; if TRELCEL is greater than the specified TRELCEL (max) limit, then access time is controlled exclusively by TCELQV.
- These parameters are reference to CE leading edge in early write cycles and to W leading edge in delayed write or read-modify-write cycles.
- 14. TWLCEL, TCELWL and TRELWL are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if TWLCEL = TWLCEL (min), the cycle is an early write and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if TCELWL = TCELWL (min) and TRELWL will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

Capacitance measured with Boonton Meter or effec-15. tive capacitance measuring methods.)

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS #READ CYCLE

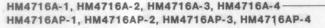
 $(T_a=0 \text{ to } +70^{\circ}\text{C}, V_{DD}=12\text{V}\pm10\%, V_{CC}=5\text{V}\pm10\%, V_{SS}=0\text{V}, V_{BB}=-5\text{V}\pm10\%)$ 

Parameter		Symbol	HM 47	716A-1	HM 4	716A-2	HM47	16A-3	HM4	716A-4	Unit	Notes
Tarameter	Old	New	min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t RC	TRELREL	320		320		375		410	-	ns	
Read-Write Cycle Time	trwc	TRELREL	320	-	320		375	-	515	-	ns	8
Page Mode Cycle Time	1 PC	TCELCEL	160	N	170	-	225	CHILDREN .	275	-	ns	
Access Time From RE	t RAC	TRELQV		120	-	150	-	200	-	250	ns	8,10
Access Time From CE	tere	TCELQV	-	80	-	100	-	135	-	165	ns	9, 10
Output Buffer Turn-off Delay	toff	TCEHQZ	0	35	0	50	0	60	0	70	ns	11
Transition Time (Rise and Fall)	t r	TT	3	35	3	35	3	50	3	50	ns	7
RE Precharge Time	LRP	TREHREL	100	-	100	-	120	W YE	150	in the	ns	180
RE Pulse Width	tRAS	TRELREH	120	10000	150	10000	200	10000	250	10000	ns	
RE Hold Time	trsh	TCELREH	80	-	100	-	135	-	165	-	ns	
CE Pulse Width	teas	TCELCEH	80	10000	100	10000	135	10000	165	10000	ns	
CE Hold Time	tesn	TRELCEH	120	-	150	-	200	-	250	-	ns	
RE to CE Delay Time	trco	TRELCEL	15	40	25	50	30	65	40	85	ns	12
CE to RE Precharge Time	lcrp	TCEHREL	0		-20	-	-20	-	-20	-	ns	1
Row Address Set-up Time	tASR	TAVREL	0	0.00	0	-	0	-	0	-	ns	
Row Address Hold Time	. trah	TRELAX	15	-	20	-	25	-	35		ns	
Column Address Set-up Time	tasc	TAVCEL	-5	120 <u>4</u> 33	-5	-	-5	-	-5	-	ns	
Column Address Hold Time	I CAH	TCELAX	40	-	45		55	-	75	-	ns	
Column Address Hold Time Reference to RE	tan	TRELAX	80	C 7/	95	100	120		160	-	ns	
Read Command Set-up Time	tres	TWHCEL	0	-	0	-	0	-	0	-	ns	
Read Command Hold Time	I ACH	TCEHWL	0	-	20	-	20	1 7	20	0-0	ns	-
Write Command Hold Time	twcn	TCELWH	40	-	45	-	55	-	75	-	ns	
Write Command Hold Time Reference RE	twcs	TRELWH	80	-	95	10 31	120	10.07/	160	313778	ns	9.96
Write Command Pulse Width	twp	TWLWH	40	()r	45	-	55		75	-	ns	
Write Command to RE Lead Time	t <sub>RWL</sub>	TWLREH	50	+	60	-	80	<u></u>	100	-	ns	
Write Command to $\overline{CE}$ Lead Time	t cw1	TWLCEH	50		60		80	12-	100	-	ns	
Data-in Set-up Time	tos	TDVCEL	0	-	0	× -3	0	-	0	-	ns	13
Data-in Hold Time	t <sub>DH</sub>	TCELDX	40	-	45		55	-	75	-	ns	13
Data-in Hold Time Referenced RE	t dhr	TRELDX	80	-	95	000	120	<u>1</u>	160	-	ns	
CE Precharge Time (for Page-mode Cycle Only)	tcp	TCEHCEL	60	- 2	60	-	80	2 2	100	-	ns	
Refresh Period	tREF	TRVRV	1	2	-	2	77777	2	-	2	ms	
W Command Set-up Time	twcs	TWLCEL	0	-	-20	-	-20	-	-20	-	ns	14
CE to RE Delay	tewp	TCELWL	60	-	70	-	95	NO DO	125	1.15	ns	14
RE to W Delay	l RWD	TRELWL	100	-	120	-	160	-	200	-	ns	14
RE Precharge to CE Hold Time	t RPC	TREHCEL	0	ger, -	0	-	0	-	0	-	ns	

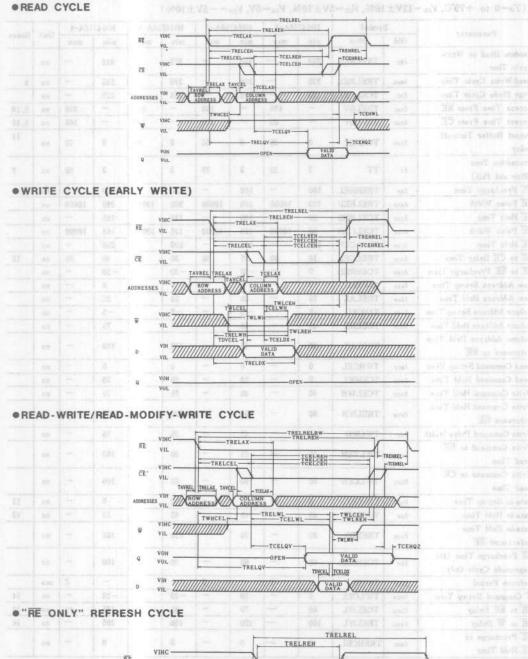
# AC ELECTRICAL CHARACTERISTICS

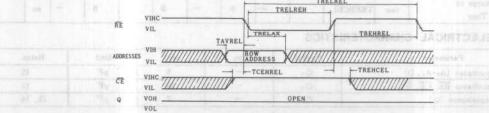
Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-Ac, D)	Cri	- 177	5	pF	15
Input Capacitance RE, CE, W	Cn	- /////	10	pF	15
Output Capacitance (Q)	Ce	-	7	pF	15, 16

**OHITACHI** 

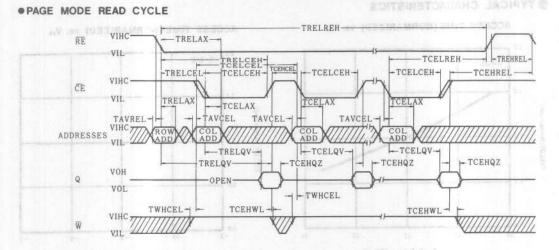


# TIMING WAVEFORMS **READ CYCLE**

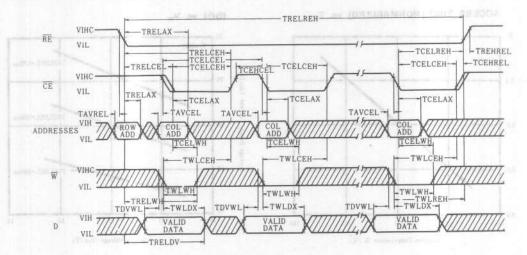


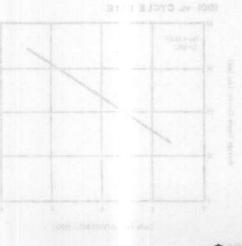


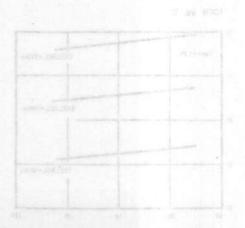
**OHITACHI** 



• PAGE MODE WRITE CYCLE

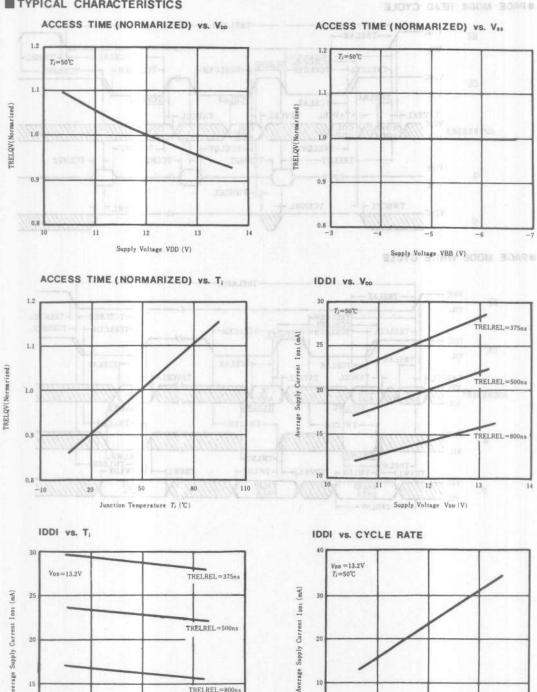






**OHITACHI** 

## TYPICAL CHARACTERISTICS



**OHITACHI** 

110

20

10

1

2

Cycle Rate (1/TRELREL) (MHz)

3

TRELREL=500ns

TRELREL=800ns

80

50

Junction Temperature Ti ('C)

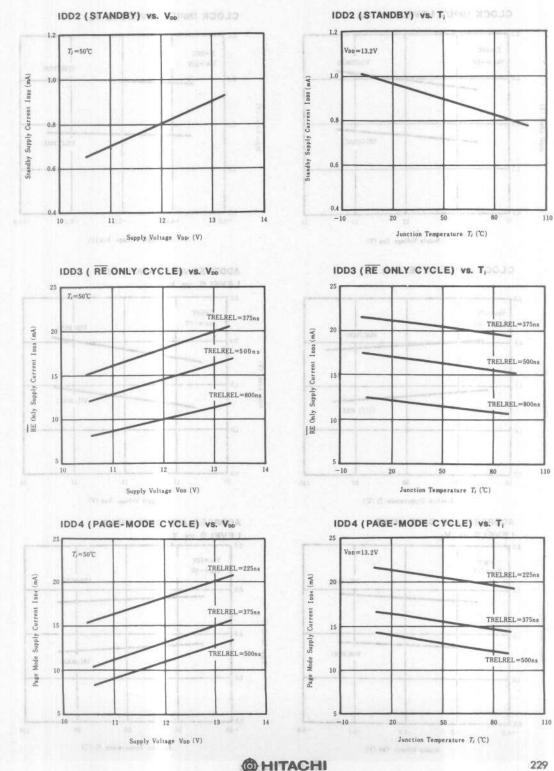
228

Average 15

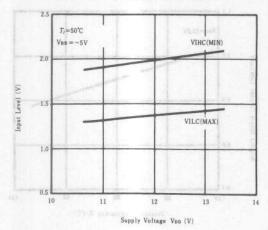
20

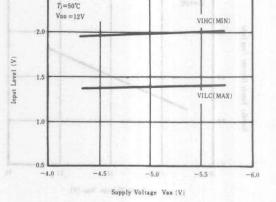
10

-10



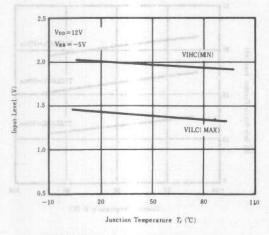
## CLOCK INPUT LEVELS vs. Voo

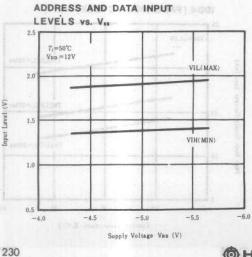




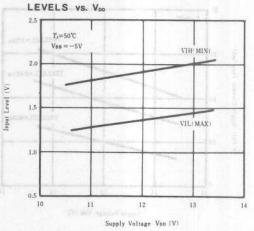
CLOCK INPUT LEVELS VS. Vas

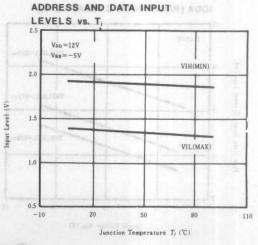
CLOCK INPUT LEVELS vs. T,





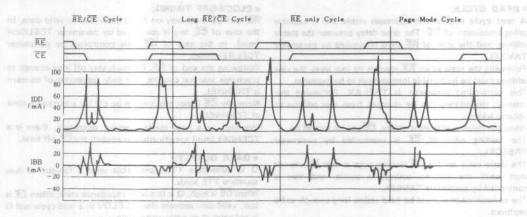






**OHITACHI** 

#### **CURRENT WAVEFORMS**



The odiettolong of treatter is TOELAX, New Jun-TREV, EL, levels, a not an operating their of the IMAY10A theory is specific on it fields on the deta severe the econics on them then TREVEL (new), the second treat run PE will be in the duty one time which TREVEEL and PE will be in the duty one time which TREVEEL

Following the time view CE evaluates to be level, and the sparse of time view CE evaluates to be level, and the sparse. This are restart in TELOV-section time from E. The action of MR STRELOV is the time the from efforts to varia CL. The minimum ratios of TRELOV is detend to the sum of TRELOEL(must) and TOULOV. The observed high, and the CD giv buschman high immediated intervent high, and the CD giv buschman high immediated. The preventions.

#### UT INTE OVCLE

A we receive a contranted by bringing W loss before on the

two militerent writes - circum be taffined and

Write evolve - Write altre are available at the beginning of over T.S. events that its write association starts at the header ming. In this most, O and W algorit course are not to any critical contrate draw motion or cle time.

Collowing the shoury when W reacting its low level. W more the relial status tong a 11-ph to be suptained. This W-an judge denation is suited TV. Wit.

ha i me nervined i ni spinere sector data in a latoh a dallara 1913-032

Finite cycle, is called an elevent

These Write spoke – This ovela marks as a read work, but as and as the Levice evolution to the sector and the sector and the minutes of Wissing 2 and behaved with after Q. This system is and as a "desired work". A "Read-modify-write system is a sector and this operation. In this mode, D and Wisseman and a construction for the armining system time.

## NOTE : VDD =13.2V, VBB = -4.5V, Ta = 25°C

Sons Sons Head and He

PAGE MODE:

Page mode operation of continues at munipia cocontinue with licenseed coeractine with licenseed coermentation of E. at a hopic titue normally require to dimensed, some and cycli common generation page.

mang minitive reasonable way as

and the second second second

white a true to be a beauties

way show an and the mainteet

we address into the abigured throughour all accousing OE any address is internet. As the robing is have new address in robing is note in the address and the robing on the destreased and the original factors.

#### APPLICATION INFORMATION

#### READ CYCLE;

A read cycle begins with addresses stable and a negative going transistion of  $\overline{RE}$ . The time delay between the stable address and the start of  $\overline{RE}$ -on is controlled by parameter TAVREL.

Following the time when RE reaches its low level, the row address must be held stable long enough to be captured.

This controlling parameter is TRELAX. Following this interval, the address can be changed from row address to column address.

When the column address is stable, CE can be turned on.

The leading edge of CE is controlled by parameter TRELCEL.

The basic limit on the  $\overline{CE}$  leading edge is that  $\overline{CE}$  cannot start until the column address is stable, and this is controlled by parameter TAVCEL.

The column address must be held stable long enough to be captured.

The controlling parameter is TCELAX. Note that TRELCEL(max) is not an operating limit of the HM4716A though its specification is listed on the data sheets. If CE becomes on later than TRELCEL(max), the access time from RE will be increased by the time which TRELCEL exceeds TRELCEL(max).

Following the time when  $\overline{CE}$  reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is TCELQV-access time from  $\overline{CE}$ . The access time from  $\overline{RE}$ -TRELQV is the time from  $\overline{RE}$ -on to valid Q. The minimum value of TRELQV is derived as the sum of TRELCEL(max) and TCELQV. The selected output data is held valid internally until  $\overline{CE}$  becomes high, and then Q pin becomes high impedance. This parameter is TECHQZ.

#### . WRITE CYCLE;

A write cycle is performed by bringing  $\overline{W}$  low before or during  $\overline{CE}$ -on.

Two different write cycles can be defined as;

Write cycle – Write data are available at the beginning of the  $\overline{CE}$ -on so that the write operation starts at the beginning. In this mode, D and W signal times are not in any critical path for determining cycle time.

Following the time when  $\overline{W}$  reaches its low level.  $\overline{W}$  must be held stable long enough to be captured. This  $\overline{W}$ -on pulse duration is called TWLWH.

The time required to capture write data in a latch is called TWLDX.

This cycle is called an "early write"

Read Write cycle – This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.  $\overline{W}$  and D are delayed until after O. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, D and  $\overline{W}$  become critical path signals for determining cycle time.

#### SMR0434AW (MSMMU)

#### CLOCK-OFF TIMING;

 $\overline{RE}$  and  $\overline{CE}$  must stay on for Q stabilized to valid data. In the case of  $\overline{CE}$ , this is controlled by parameter TCELCEH (min). In the case of  $\overline{RE}$ , this controlled by parameter TCELREH(min).

Following the end of  $\overline{RE}$ ,  $\overline{CE}$  must stay off long enough to precharge internal circuits. The only parameter of concern is TREHREL.

Normally CE is not required to be off for a minimum time of TCEHREL.

However, in a page mode memory operation, there is a TCEHCEL(min) specification to control the  $\overline{CE}$ -off time.

#### · DATA OUTPUT;

 $\ensuremath{\Omega}$  is three-state TTL compatible with a fan-out of two standard TTL loads.

When  $\overline{CE}$  is high, Q is in a high impedance state. When  $\overline{CE}$  is low, valid data appears after TCELQV at a read cycle and Q is not valid at an early-write cycle.

#### • REFRESH;

Refresh of the HM4716A is accomplished by performing A memory cycle at each of the 128 row addresses within each two millisecond time interval.

Any cycle in which RE signal occurs refreshes the entire selected row.

RE-only refresh results in substantial reduction in operating power.

This reduction in power is reflected in the IDD3 specification.

#### · PAGE MODE;

O HITACHI

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining  $\overline{RE}$  at a logic low throughout all successive  $\overline{CE}$  memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are reflected in the TCELQV, TCEHCEL, IDD4 specifications.

## 16384-word by 1-bit Dynamic Random Access Memory

The HM4816A is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816A (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power.

The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816A a truly superior RAM product. Multiplexed address inputs permits the HM4816A to be packaged in standard 16-pin DIP. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

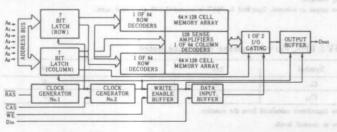
# FEATURES

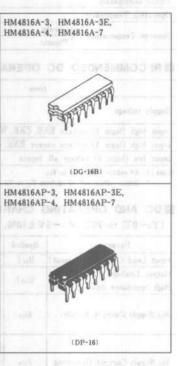
- Single 5V supply
  - Low power standby and operation
  - (Standby: 11mW max., operation: 150mW max.)
- Fast access time & cycle time

	HM4816A-3 HM4816AP-3	HM4816A-3E HM4816AP-3E		HM4816A-7 HM4816AP-7
Maximum Access Time (ns)	100	105	120	150
Read, Write Cycle (ns)	235	200	270	320
Read-Modify-Write Cycle (ns)	285	235	320	410

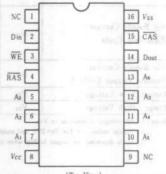
- Directly TTL compatible: All inputs & outputs
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary.
- Common I/O capability using "easy write" operation.
- Read modify write, RAS only refresh and page mode capability
- Only 128 refresh cycle required every 2ms
- Compatible with Intel 2118-3/-4/-7

#### BLOCK DIAGRAM





## PIN ARRANGEMENT



(Top View)



#### ABSOLUTE MAXIMUM RATINGS

Ite	m	Symbol	HM4816A or AP	Unit
Voltage on any pin rela	tive to GND	Vr	$-1.0 \sim +7.0$	v
Power supply voltage r	elative to GND	Vcc	$-0.5 \sim +7.0$	v
Short-circuit Output Current		Just	50	mA
Power Dissipation		Pr	1.0	W
Operating Temperature		Tept	$0 \sim +70$	°C
C	Cerdip	T	$-65 \sim +150$	ъ.
Storage Temperature	Plastic	Tete	$-55 \sim +125$	°C

a start and the second

# RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	Notes
empty webser	Vcc	4.5	5.0	5.5	v	1
Supply voltage	Vss	0	0	0	V	1, 2
Input high (logic 1) voltage RAS, CAS, WE	Vinc	2.4	1 A 15	7.0	V	1
Input high (logic 1) voltage except RAS, CAS, WE	VIN	2.4	-	7.0	V	1
Input low (logic 0) voltage all inputs	VIL	-2.0	-	0.8	V	1

Notes : 1. All voltage referenced to V<sub>53</sub>.

2. Output voltage will swing from Vis to Vcc when activated with no current loading.

### DC AND OPERATING CHARACTERISTICS (1)

 $(Ta=0^{\circ}C \text{ to } 70^{\circ}C, V_{cc}=5V\pm10\%, V_{ss}=0V, \text{ unless otherwise noted.})$ 

Parameter	Symbol	Test C	onditions	min	typ (2)	max	Unit	Notes
Input Load Current (any input)	$ I_{LI} $	$V_{IN} = V_{SS}$ to $V_{CC}$			0.1	10	μA	-
Output Leakage Current for High Impedance State	$ I_{LO} $	Chip Deselected; CAS a	at $V_{IH}$ , $V_{OUT}=0$ to 5.5V	aut i	0.1	10	μA	
Vcc Supply Current. Standby	Ices	Chip Deselected; $\overline{CAS}$ at $V_{i}$ $\overline{CAS}$ and $\overline{RAS}$ at $V_{iH}$ H	HM 4816AP-3, 4, 7 HM 4816A-3, 4, 7	-	1.2	2	mA	a chilas.M
		1	HM4816A, AP-3E	+	1.2	3	mA	
(0)-90		HM4816A, AP-3 $t_{RC} = t_R$	ICMIN <sup>DESE</sup>	-	23	27	mA	3
Input Load Current (any input) Output Leakage Current for High Impedance State Vcc Supply Current. Standby Vcc Supply Current. Operating Vcc Supply Current; RAS-Only Cycle Vcc Supply Current. Standby. Output Enabled Output Low Voltage		HM4816A, AP-3E tRC=	4	27	35	mA	3	
	Iccz	HM4816A, AP-4 trc= tr	+	21	25	mA	3	
		HM4816A, AP-7 $t_{RC} = t_R$	CMIN	-	19	23	mA	3
11 M	- Thore	HM4816A, AP-3 $t_{RC} = t_R$	CMIN	-	16	18	mA	3
Vcc Supply Current;		HM4816A, AP-3E tac=t	RCMIN		20	25	m.A	3
RAS-Only Cycle	Iccs	HM4816A, AP-4 $t_{RC} = t_R$	CMIN	and These	14	16	mA	3
and True	120	HM4816A, AP-7 tRC= tR	CMIN	-	12	14	mA	3
Vcc Supply Current. Standby. Output Enabled	Ices	CAS at VIL, RAS at	Vin maa baa dastaa	only i	3	6	m A	3
Output Low Voltage	VOL	$I_{OL} = 4.2 \mathrm{mA}$	star. Aleaa	0	90 BE //	0.4	v	anto a
Output High Voltage	- Von	$I_{OH} = -5 \mathrm{mA}$	13	2.4	15.1410	Vcc	v	1027 0

Notes : 1. All voltages referenced to Vss.

2. Typical values are for Ta=25°C and nominal supply voltages.

3. Icc is dependent on output loading when the devices output is selected. Specified Icc MAX is measured with the output open.

	CAPACITANCE	$(T_a=25^{\circ}C, V_{cc}=5V\pm 10\%)$	$V_{ss} = 0V$ , unless otherwise noted.)
--	-------------	--	--

Parameter	Symbol	typ	max	Unit
Address. Data In	Cri	3	5	pF
RAS, CAS, WE, Data Out	Ciz	4	7	pF

**OHITACHI** 

Notes : Capacitance measured with Boonton Meter or effective capacitance calculated from the equation :

 $C = \frac{I\Delta t}{\Delta V}$  with  $\Delta V$  equal to 3 volts and power supplies at nominal levels.

**AC CHARACTERISTICS** <sup>[1,2,3]</sup> ( $Ta=0^{\circ}$ C to 70°C,  $V_{cc}=5V\pm10\%$ ,  $V_{ss}=0V$ , unless otherwise noted.) • READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Parameter	Symbol	- Service and	HM 4816A-3 HM 4816AP-3		HM4816A-3E HM4816AP-3E		HM4816A-4 HM4816AP-4		HM4816A-7 HM4816AP-7		Notes
	Distant brist o	min	max	min	max	min	max	min	max	1287	31 40
Access Time From RAS	LRAC	1111	100	102227	105	-	120	0-11-0	150	ns	4, 5
Access Time From CAS	1 CAC	tore Third	55	-	60	1.000	65	-	80	ns	4, 5, 6
Time Between Refresh	Iner	CUSTA!	2	-	2	-	2	N98723	2	ms	ai ia
RAS Precharge Time	t <sub>RP</sub>	110	08 -	70	-	120	1.100	135	Sam	ns	R
CAS Precharge Time (non-page cycles)	1 <sub>CPN</sub>	50	- 000	50	-	55	-	70	-	ns	
CAS to RAS Precharge Time	tCRP	0	[sei] -	0	-	0	-	0	-	ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	25	45	25	45	25	55	25	70	ns	7
RAS Hold Time	t <sub>RSH</sub>	70	-	60	-	85	-	105	- 5 <del>.4</del> 0	ns	ADR
CAS Hold Time	t <sub>csn</sub>	100	1.04	105	-	120		165	-	ns	
Row Address Set-up Time	LASE	0	-	0	-	0	1275	0		ns	
Row Address Hold Time	LRAH .	15	-	15	-	15	- 1	15	100	ns	
Column Address Set-up Time	LASC	0	-	0	1.0	0		0	-	ns	
Column Address Hold Time	1 CAN	15	-	25	0	20	-	20		ns	
Column Address Hold Time to RAS	LAR	60	-	70	-	75	-	90		ns	
Transition Time (Rise and Fall)	l <sub>T</sub>	3	50	3	50	3	50	3	50	ns	8
Output Buffer Turn Off Delay	LOFF	0	45	0	50	0	50	0	60	ns	

## • READ AND REFRESH CYCLES

Random Read Cycle Time	t <sub>RC</sub>	235	-	200	2.10	270		320		ns	
RAS Pulse Width	tRAS	115	10000	105	10000	140	10000	175	10000	ns	
CAS Pulse Width	LCAS	55	10000	60	10000	65	10000	95	10000	ns	
Read Command Set-up Time	tRCS	0	-	0	-	0	-	0		ns	
Read Command Hold Time	t <sub>RCH</sub>	10		10	-	10	- 1	10		ns	

## **WRITE CYCLE**

Random Write Cycle Time	tac	235	-	200	-	270	-	320	11121	ns	THE OWNER
RAS Pulse Width	tras	115	10000	105	10000	140	10000	175	10000	ns	
CAS Pulse Width	teas	55	10000	60	10000	65	10000	95	10000	ns	
Write Command Set-up Time	twes	0	-	0	-	Ö	-	0	24	ns	9
Write Command Hold Time	twen	25		30	- 194	30		45	-	ns	
Write Command Hold Time to RAS	Lwca	70	-	75	19-	85	-3	115	-	ns	
Write Command Pulse Width	twp	25	-	30	-	30		50	1	ns	
Write Command to RAS Lead Time	t RWL	60	-	45	- 1	65	1	110		ns	
Write Command to CAS Lead Time	*tcwL	45	-	45	12-	50	1 10 - 3	100		ns	
Data-in Set-up Time	tos	0		0	-	0	-	0	-	ns	
Data-in Hold Time	LDH	25"	(8) -	30		30	-	45		ns	
Data-in Hold Time to RAS	t <sub>DHR</sub>	70	-	75	-	85	-	115	-	ns	

#### READ-MODIFY-WRITE CYCLE

Read-Modify-Write Cycle Time	t awc.	285	-	235	1-	320	-	410		ns	
RMW Cycle RAS Pulse Width	LRRW	165	10000	155	10000	190	10000	265	10000	ns	
RMW Cycle CAS Pulse Width	t <sub>CRW</sub>	105	10000	110	10000	120	10000	185	10000	ns	
RAS to WE Delay	t RWD	100	-	105	-	120	-	150	-	ns	9
CAS to WE Delay	tewn	55	-	60	-	65	-	80	-	ns	9

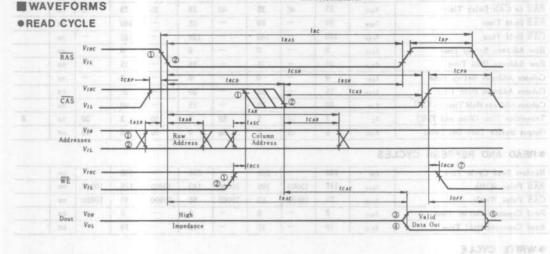
3.4  $^{60}OH$  here and  $^{6}OH$  at a  $\chi$  are definence levels for measuring times of DO(m) . So we areas well of  $O(m) < U_{EO}$  is  $L_{OE}$  with level  $\chi$  are defined to CAS or  $^{10}H_{\odot}$  with level  $\chi$ .

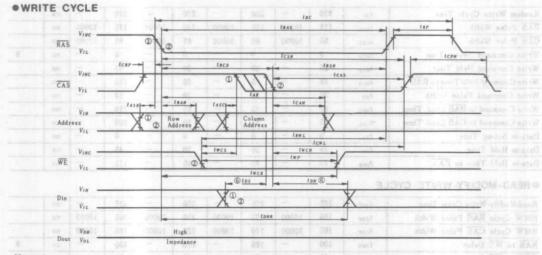


#### Notes:

- 1. All voltages referenced to VSS
- Eight cycles are required after power-up or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purposes.
- 3. AC Characteristics assume  $t_T$ =5ns
- 4. Assume that  $t_{RCD} \leq t_{RCD}$  (max.) If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.) then  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}$  (max.)
- 5. Load = 2 TTL Loads and 100pF
- 6. Assumes  $t_{RCD} \ge t_{RCD} (\max.)$

- 7.  $t_{RCD}$  (max.) is specified as a reference point only. If  $t_{RCD}$  is less than  $t_{RCD}$  (max.) access time is  $t_{RAC}$ . If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.) access time is  $t_{RCD} + t_{CAC}$ .
- 8.  $t_T$  is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.)
- 9.  $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are specified as reference points only. If  $t_{WCS} \ge t_{WCS}$  (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If  $t_{CWD} \ge t_{CWD}$  (min.) and  $t_{RWD} \ge t_{RWD}$  (min.), the cycle is a read-modifywrite cycle and the data out will contain the data read from the selected address if neither of the above conditions is satisfied, the condition on the data out is indeterminate.

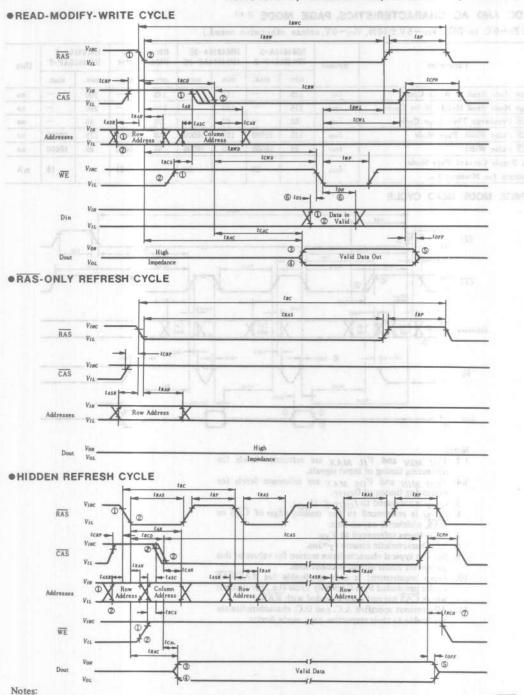




Notes:

- 1.2. V<sub>IH MIN</sub> and V<sub>IL MAX</sub> are reference levels for measuring timing of input signals.
- 3.4. VOH MIN and VOL MAX are reference levels for measuring timing of DOUT.
- 5. toFF is measured to IOUT <1 ILO 1.
- t<sub>DS</sub> and t<sub>DH</sub> are referenced to CAS or WE, whichever occurs last.
- 7. <u>tRCH</u> is referenced to the trailing edge of CAS or RAS, whichever occurs first.
- t<sub>CRP</sub> requirement is only applicable for RAS/CAS cycles preceeded by a CAS-only cycle (i.e., for system where CAS has not been decoded with RAS).





- Notes:
  1.2. V<sub>IH</sub> MIN and V<sub>IL</sub> MAX and reference levels for measuring timing of input signals.
  3.4. V<sub>OH</sub> MIN and V<sub>OL</sub> MAX are reference levels for measuring timing of D<sub>OUT</sub>.
  5. t<sub>OFF</sub> is measured to I<sub>OUT</sub> ≤ |I<sub>LO</sub>|
  6. t<sub>DS</sub> and t<sub>DH</sub> are referenced to CAS or WE, whichever reference levels for WE.

  - occurs last.
- t<sub>RCH</sub> is referenced to the trailing edge of CAS or RAS, whichever occurs first.
   t<sub>CRP</sub> requirement is only applicable for RAS/CAS cycles preceded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).

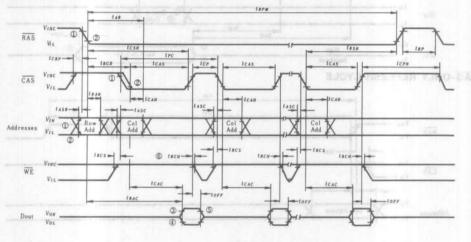


#### DC AND AC CHARACTERISTICS, PAGE MODE (7.8.)

(Ta=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.)

Parameter	Symbol	HM 48 HM 48	16A-3 16AP-3	HM 481 HM 481	6A-3E 6AP-3E	HM 481 HM 481	6A-4 6AP-4	HM 48 HM 48	16A-7 16AP-7	Unit
		min.	max.	min.	max.	min.	max.	min.	max.	Unit ns ns ns ns ms mA
Page Mode Read or Write Cycle	1 PC	125	-	130	(772-3	145	-	190	23-	ns
Page Mode Read Modify Write Cycle	L PCM	175	-	180		200	-	280	-	ns
CAS Precharge Time, Page Cycle	1cp	60	-	60	100	70	-	85	-	ns
RAS Pulse Width, Page Mode	t RPM	115	10000	105	10000	140	10000	175	10000	ns
CAS Pulse Width	leas	55	10000	60	10000	65	10000	95	10000	ns
VDD Supply Current Page Mode. Minimum tPC. Minimum tCAS	IDDA	-	23		23	No.	21	يبي.	18	mA

#### PAGE MODE READ CYCLE



## Notes:

- 1.2.  $V_{IH}$  MIN and  $V_{IL}$  MAX are reference levels for measuring timing of input signals.
- 3.4. V<sub>OH</sub> MIN and V<sub>OL</sub> MAX are reference levels for measuring timing of D<sub>OUT</sub>.
  5. t<sub>OFF</sub> is measured to I<sub>OUT</sub> ≤ |I<sub>LO</sub>|.
  6. t<sub>RCH</sub> is referenced to the trailing edge of CAS or RAS, whichever occurs first.

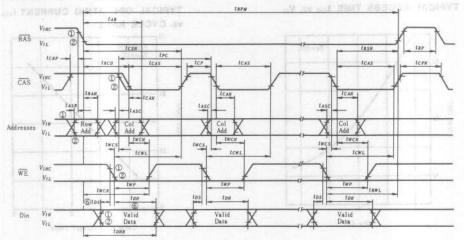
- 7. All voltages referenced to VSS.
- 8. AC Characteristic assume  $t_T$ =5ns.
- 9. See the typical characteristics section for values of this parameter under alternate conditions.
- 10.  $t_{CRP}$  requirement is only applicable for RAS/CAS cycles preceded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).
- 11. All previous specified A.C. and D.C. characteristics are applicable to their respective page mode device.

targe is releasant it
 targe is released in

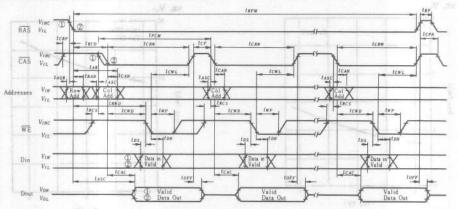
**OHITACHI** 

PREAD-MODIFY-WRITE CVOLE





## PAGE MODE READ-MODIFY-WRITE CYCLE

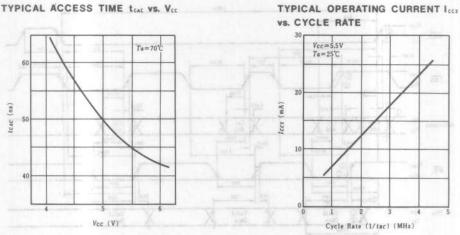


- 1.2. V<sub>IH MIN</sub> and V<sub>IL MAX</sub> are reference levels for measuring timing of input signals.
  - 3.4.  $V_{DH}$  MIN and  $V_{OL}$  MAX are reference levels for measuring timing of DOUT. 5.  $t_{OFF}$  is measured to  $I_{OUT} \leq |I_{LO}|$ . 6.  $t_{DS}$  and  $t_{DH}$  are referenced to CAS or WE, whichever

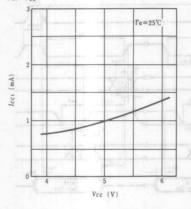
    - occurs last.
    - 7.  $t_{RCH}$  is referenced to the trailing edge of  $\overline{CAS}$  or RAS, whichever occurs first.
    - t<sub>CRP</sub> requirement is only applicable for RAS/CAS, cycles preceded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).

#### Typical Characteristics of HM4816A

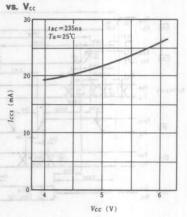
## TYPICAL ACCESS TIME tcat vs. Vcc



TYPICAL STANDBY CURRENT Icci VS. Vcc

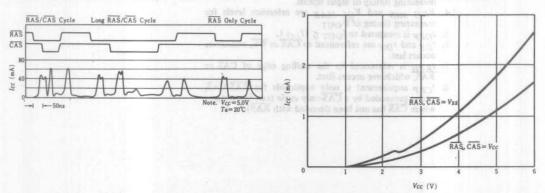






**TYPICAL SUPPLY CURRENT WAVEFORMS** 

TYPICAL Icc vs. Vcc DURING POWER UP



**OHITACHI** 

# HM4864-2, HM4864-3 HM4864P-2, HM4864P-3

## 65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

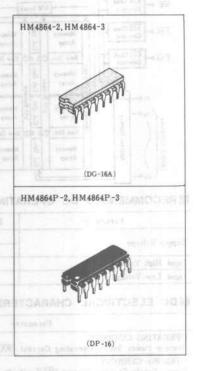
This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of  $\pm 5V$  with  $\pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and RAS-only refresh.

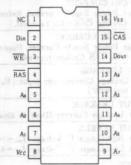
Proper control of the clock inputs (RAS, CAS, and WE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

## FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V±10% with a built-in V<sub>BB</sub> generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, and Page-mode capability
- 128 refresh cycle



#### PIN ARRANGEMENT



(Top View)

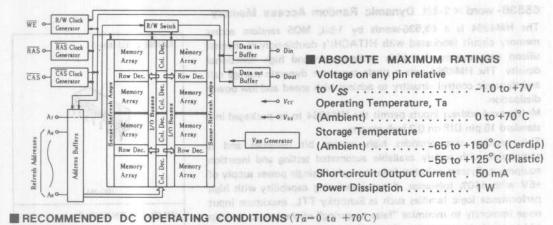
A A .	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
Ao-As	Refresh Address Input

qualit dipresent approaches accouch to varate rol



## HM4864-2, HM4864-3, HM4864P-2, HM4864P-3-

# FUNCTIONAL BLOCK DIAGRAM



Parameter	Symbol	min	typ	max	Unit	Notes
	Vcc	4.5	5.0	5.5	V	inconant
Supply Voltage	Vss	0	0	0	V	anner
Input High Voltage	VIH	2.4	-	6.5	v	1
Input Low Voltage	VIL	-1.0		0.8	V	1

# DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}, \overline{CAS}$ Cycling; $t_{sc} - \min$ .)	Icci	6 <u>1/0</u>	60	m A	2, 4
STANDBY-CURRENT Power Supply Standby Current ( $\overline{RAS} = V_{IH}$ , Dout = High Impedance)	Icc 2	-	3.5	m A	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, $\overline{CAS} = V_{IN}; t_{RC} = \min.)$	Iccs			mA	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation $(\overline{RAS} - V_{t_4} \overline{CAS} Cycling; t_{PC} - min.)$	Lean		45		2, 4
INPUT LEAKAGE Input Leakage Current, any Input ( $V_{in} = 0$ to $+6.5V_{in}$ all other pins not under test $= 0V$ )	Iμ	-10	10	μA	E sitt 4
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, V., (-0 to +5.5V)	ILO	-10	10	μA	and the second
OUTPUT LEVELS Output High (Logic 1) Voltage ( $I_{nt} = -5mA$ ) Output Low (Logic 0) Voltage ( $I_{nt} = 4.2mA$ )	Von Vot	2.4 0	<i>Vcc</i> 0.4	v v	Bry Bry Borner

NOTES

· Reat-Modily-Write, RAS-only refresh, and Page-mode republiky

1. All voltages referenced to VSS.

2. I<sub>CC</sub> depends on output loading condition when the device is selected. I<sub>CC</sub> max. is specified at the output open condition.

ILC consists of leakage current only.
 Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

#### AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-Ar, Din)	Cial	-	7	pF	1
Input Capacitance (RAS, CAS, WE)	Cinz	-	10	pF	1
Output Capacitance (Dout)	Court	-	7	pF	1, 2

NOTES

1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{CAS} = V_{IH}$  to disable DOUT.



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS 13, 22

	0.11	HM 486	4-2/P-2	HM 486	4-3/P-3		
Parameter	Symbol	min	max	min	max	Unit	Notes
Random Read or Write Cycle Time	1 <sub>RC</sub>	270	+	335	10 TTT	ns	
Read-Write Cycle Time	t <sub>RWC</sub>	270	-	335	-	ns	
Page Mode Cycle Time	1 <sub>PC</sub>	170	-	225	1.15	ns	
Access Time from RAS	1 RAC	-	150	-	200	ns	4,6
Access Time from CAS	ICAC.	1/-	100		135	ns	5,6
Output Buffer Turn-off Delay	forr.	0	40	0	50	ns	7
Transition Time (Rise and Fall)	tT	3	35	3	50	ns	3
RAS Precharge Time	1 <sub>RP</sub>	100	-	120	-	ns	
RAS Pulse Width	1 RAS	150	10000	200	10000	nŝ	
RAS Hold Time	t <sub>RSH</sub>	100	-	135	-	ns	
CAS Pulse Width	teas	100	-	135	-	ns	a 710 1/4
CAS Hold Time	t <sub>csH</sub>	150	-,	200	-	ns	
RAS to CAS Delay Time	1 RCD	20	50	25	65	ns	8
CAS to RAS Precharge Time	ICRP	-20	-	-20	·	ns	
Row Address Set-up Time	LASR	0		0	-	ns	
Row Address Hold Time	1 RAH	20	-	25	111-	ns	
Column Address Set-up Time	IASC	-10	-	-10	-	ns	
Column Address Hold Time	\$CAN	45	- Face Calif. and	55	-	ns	
Column Address Hold Time referenced to RAS	LAR	95	-	120	-	ns	
Read Command Set-up Time	IRCS	0	-	0	-	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	-	0	28 -	ns	
Write Command Hold Time	lwcн	45	-	55	-	ns	
Write Command Hold Time referenced to RAS	lwcn	95		120	-	ns	
Write Command Pulse Width	twp	45		55	010	ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	45	-	55	-	ns	
Write Command to CAS Lead Time	tcwi	45		55	-	ns	
Data-in Set-up Time	tps	0	-	0	-	ns	9
Data-in Hold Time	t <sub>DH</sub>	45	D BLEN	55	M-0/-	ns	9
Data-in Hold Time referenced to RAS	LDHR	95	-	120	-	ns	
CAS Precharge Time (for Page-mode Cycle Only)	lep	60	-	80	-	ns	
Refresh Period	t <sub>REF</sub>	-	2	-	2	ms	
Write Command Set-up Time	lwcs	-20		-20	-	ns	10
CAS to WE Delay	lewo	60	-	80	-	ns	10
RAS to WE Delay	t nw b	110		145	-	ns	10
RAS Precharge to CAS Hold Time	LRPC	0	-	0	-	ns	

 $(T_a=0 \text{ to } +70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$ 

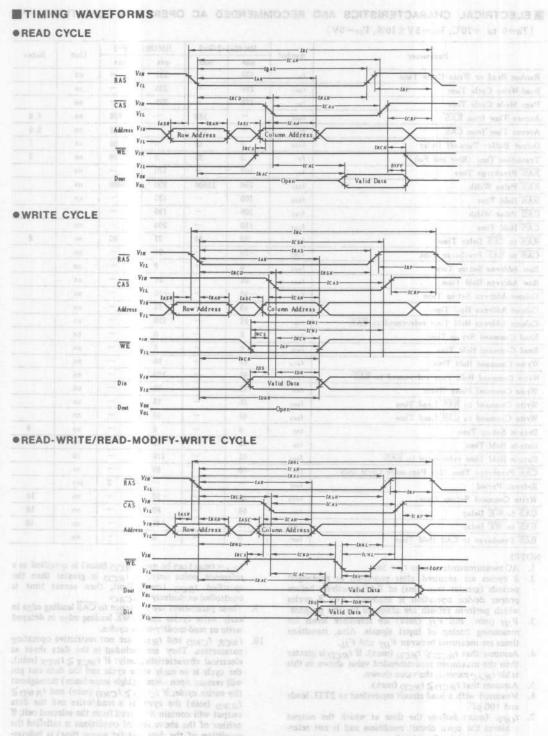
NOTES

- 1. AC measurements assume  $t_T = 5$ ns.
- 2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- 3.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 4. Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table  $t_{RAC}$  exceeds the value shown.
- 5. Assumes that  $t_{RCD} \ge t_{RCD}$  (max).
- Measured with a load circuit equivalent to 2TTL loads 6. and 100 pF.
- 7. t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 8. Operation with the  $t_{RCD}$  (max) limit insures that

 $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is

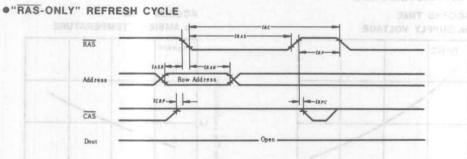
- controlled exclusively be t<sub>CAC</sub>.
  9. These parameters are reference to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
- 10. twcs. tcwp and tRwp are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge$  $t_{RWD}$  (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

#### HM4864-2, HM4864-3, HM4864P-2, HM4864P-3

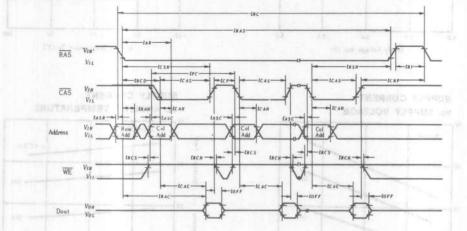


**OHITACHI** 

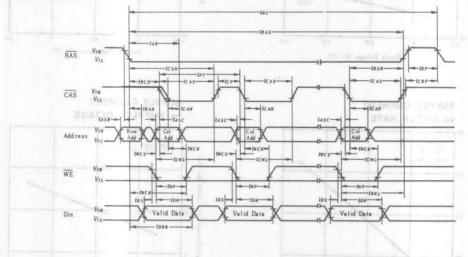
STYRICAL CHIRACTERISTICS





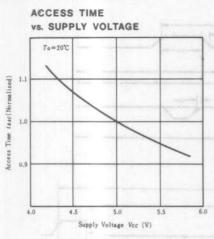


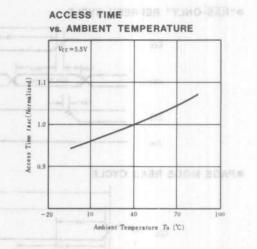


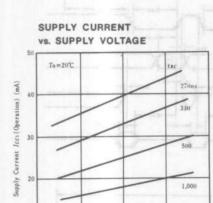


**OHITACHI** 

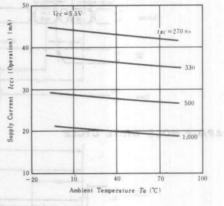


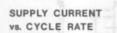












1

5(

40 (uo

30 Current

21

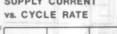
10 4

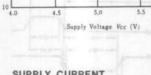
(WW)

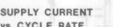
Icci(Operat

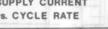
Supply (

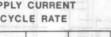
tap=100ns















2 Cycle Rate(1/tac) (MHz)

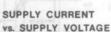


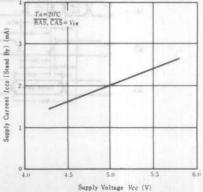




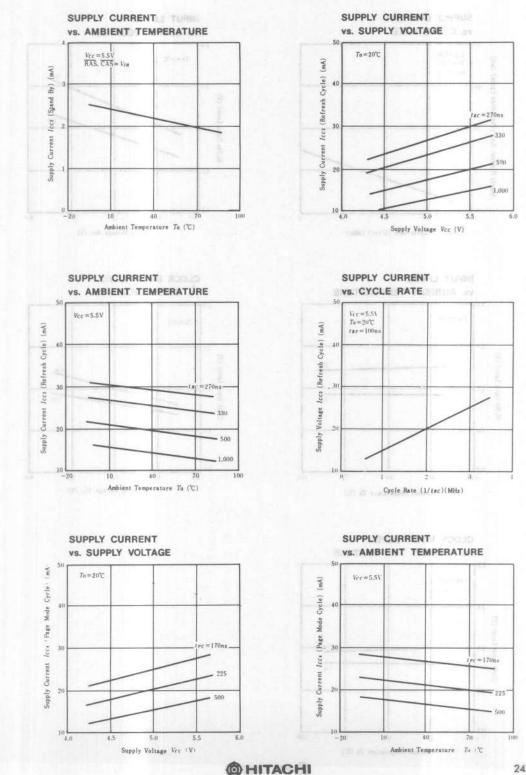
ent Cur

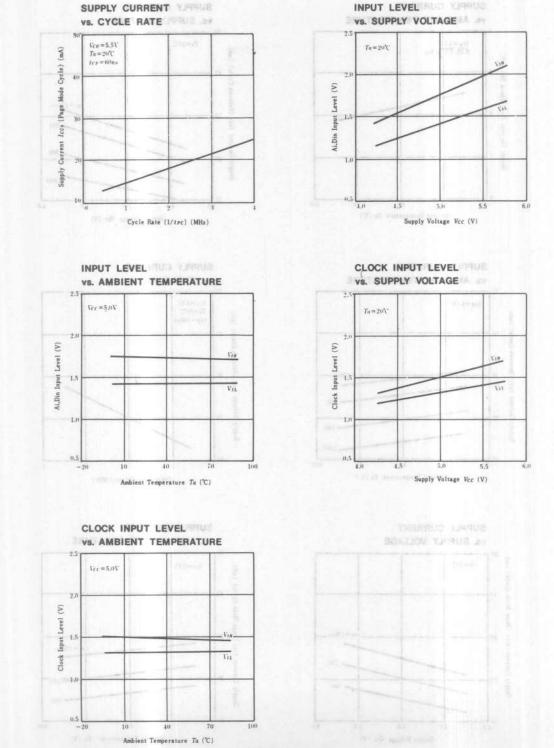
6.0





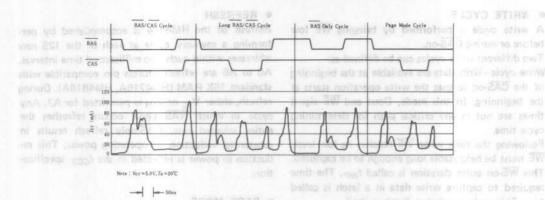






**OHITACHI** 

#### HM4864-2, HM4864-3, HM4864P-2, HM4864P-3



## APPLICATION INFORMATION

#### POWER ON

An initial pause of 500  $\mu$ s is required after power-up and a minimum of eight (8) initialization cycle, (any combination of cycles containing a RAS clock such as RAS-only refresh) must follow an initial pause.

The  $V_{CC}$  current ( $I_{CC}$ ) requirement of the HM4864 during power on is, however, dependent upon the input levels (RAS, CAS) and the rise time of  $V_{CC}$ , as shown in Fig. 1.

#### **READ CYCLE**

A read cycle begins with addresses stable and a negative going transition of  $\overline{RAS}$ . The time delay between the stable address and the start of  $\overline{RAS}$ -on is controlled by parameter  $t_{ASR}$ .

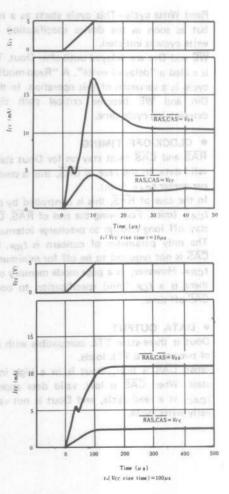
Following the time when  $\overline{RAS}$  reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is  $t_{RAH}$ . Following this interval, the address can be changed from row address to column address. When the column address is stable,  $\overline{CAS}$  can be turned on. The leading edge of  $\overline{CAS}$  is controlled by parameter  $t_{RCD}$ . The basic limit on the  $\overline{CAS}$  leading edge is that  $\overline{CAS}$  can not start until the column address is stable, and this is controlled by parameter  $t_{ASC}$ . The column address must be held stable long enough to be captured. The controlling parameter is  $t_{CAH}$ . Note that  $t_{RCD}$  (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If  $\overline{CAS}$  becomes on later than  $t_{RCD}$  (max), the access time from  $\overline{RAS}$  will be increased by the time which  $t_{RCD}$  exceeds  $t_{RCD}$  (max).

Following the time when  $\overline{CAS}$  reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is  $t_{CAC}$ -access time from  $\overline{CAS}$ .

The access time from  $\overline{RAS}-t_{RAC}$ -is the time from  $\overline{RAS}$ -on to valid Dout,

The minimum value of  $t_{RAC}$  is derived as the sum of  $t_{RCD}$  (max) and  $t_{CAC}$ .

The selected output data is held valid internally until  $\overline{CAS}$  becomes high, and then Dout pin becomes high impedance. This parameter is  $t_{OFF}$ .





HITACHI

#### HM4864-2, HM4864-3, HM4864P-2, HM4864P-3

#### WRITE CYCLE

A write cycle is performed by bringing WE low before or during CAS-on.

Two different write cycles can be defined as;

Write cycle—Write data are available at the beginning of the CAS-on so that the write operation starts at the beginning. In this mode, Dout and  $\overline{\text{WE}}$  signal times are not in any critical path for determining cycle time.

Following the time when  $\overline{WE}$  reaches its low level,  $\overline{WE}$  must be held stable long enough to be captured. This  $\overline{WE}$ -on pulse deration is called  $t_{WP}$ . The time required to capture write data in a latch is called  $t_{DH}$ . This cycle is called an "early write".

Read Write cycle—This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

WE and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and WE become critical path signals for determining cycle time.

### CLOCK-OFF TIMING

RAS and CAS must stay on for Dout stabilized to valid data. In the case of CAS, this is controlled by parameter  $t_{CAS}$  (min).

In the case of RAS, this is controlled by parameter  $t_{CAS}$  (min). Following the end of RAS, CAS must stay off long enough to precharge internal circuits. The only parameter of concern is  $t_{RP}$ . Normally CAS is not required to be off for minimum time of  $t_{CRP}$ . However, in a page mode memory operation, there is a  $t_{CP}$  (min) specification to control the CAS-off time.

#### DATA OUTPUT

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When  $\overrightarrow{CAS}$  is high, Dout is in a high impedance state. When  $\overrightarrow{CAS}$  is low, valid data appears after  $t_{CAC}$  at a read cycle, and Dout is not valid as an early-write cycle.

### REFRESH

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either  $V_{1L}$  or  $V_{1H}$  is permitted for A7. Any cycle in which RAS signal occurs refreshes the entire selected row. RAS-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the  $I_{CC3}$  specification.

#### PAGE MODE

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining RAS at a logic low throughout all successive CAS memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be descreaded and the operating power is reduced. These are specifications.

A new prote before with addresses stable and a negative field with a statement to real a state of the first doing before and the statement of the first doing before and the state of the first doing before the form the state of the formation of the state of the stat

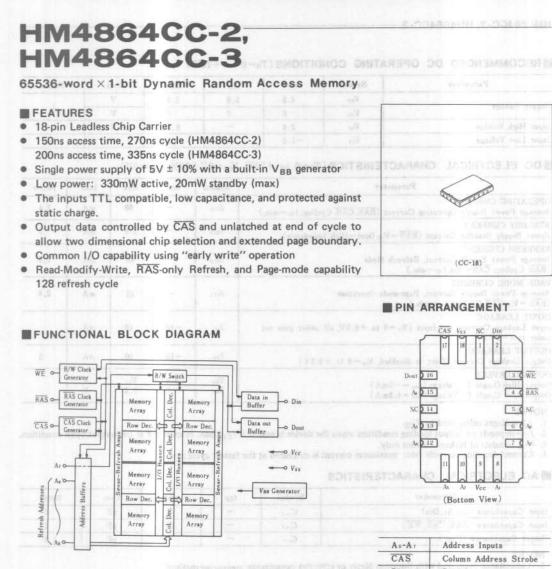
Following the time when CAS reaches its low level of deta-rot pin remains in a high impedance state undit a vaduta appears. This networks is four-rotain time from CAS. The access time from RAS-react-is the time from BAS, to well boot.

The minimum value of trace is derived in the sum of trace (mix) and trace.

The subset of the data is held valid internels, until C.A. Propries high, and dont Dout pin focomes high impediated The recommend of one

**OHITACHI** 





## ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative	
to V <sub>SS</sub>	-1.0 to +7V
Operating Temperature, Ta	
(Ambient)	0 to +70°C
Storage Temperature	
(Ambient)	-65 to +150°C
Short-circuit Output Current .	50 mA
Power Dissipation	1 W

A A7	Address Inputs					
CAS	Column Address Strobe					
Din	Data In					
Dout	Data Out					
RAS	Row Address Strobe					
WE	Read/Write Input					
Vcc	Power (+5V)					
Vss	Ground					
Ao-As	Refresh Address Input					

HITACHI

#### HM4864CC-2, HM4864CC-3-

#### RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
0 I WI	Vcc	4.5	5.0	5.5	v	
Supply Voltage	Vss	0	0	0	v e	ERUN AST B
Input High Voltage	VIH	2.4	-	6.5	V	1810187
Input Low Voltage	VIL	-1.0	12-00426888	0.8	v	0.00 - 1001

#### DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, Vcc -5V±10%, Vss=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling; t ac=min.)	Icci	NR, FOW	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current (RAS – V116, Dout – High Impedance)	Icca	845 <u></u> rd	3.5	mA	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, $\overline{CAS} = V_{IB}; t_{RC} = min.)$	Iccs	ni <u>ny</u> na	45	m A	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation (RAS - V <sub>IL</sub> CAS Cycling; t <sub>PC</sub> - min.)	Icc 4	-	45	mA	2,4
INPUT LEAKAGE Input Leakage Current, any Input ( $V_{i*}=0$ to $\pm 6.5V_{i*}$ all other pins not under test $\pm 0V$ )	Iu	-10	00.10	μA	SHUR
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, Var = 0 to +5.5V)	ILO	-10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage ( $I_{nt} = -5mA$ ) Output Low (Logic 0) Voltage ( $I_{nt} = 4.2mA$ )	Von Vol	2.4	Vcc 0.4	v v	
The second			Arrest Street		

#### NOTES

All voltages referenced to V<sub>SS</sub>.
 I<sub>CC</sub> depends on output loading condition when the device is selected. I<sub>CC</sub> max. is specified at the output open condition.

I<sub>LO</sub> consists of leakage current only.
 Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

#### AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-Ar, Din)	C 1	-	7	pF	1
Input Capacitance (RAS, CAS, WE)	Cinz	-	10	pF	1
Output Capacitance (Dout)	Cent		7	pF	1,2

#### NOTES

1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{CAS} = V_{IH}$  to disable DOUT.

SONTAR MUMINAM STUDCOSA #

Storage Temporenure

ELECTR	ICAL	CHARACTERISTICS	AND	RECOMMENDED	AC	OPERATING CONDITIONS 1). 3	3
(Ta=0 to	+70°C	$V_{cc} = 5V \pm 10\%, V_{ss} = 0$	V)				

Proventer	Sumbel	HM4864CC-2		HM486	4CC-3	Unit	Notes
Parameter	Symbol	min	max	min	max	Unit	Notes
Random Read or Write Cycle Time	tRC	270	=/	335	at BT	ns	
Read-Write Cycle Time	trwc	270	-	335	-	ns	
Page Mode Cycle Time	t <sub>PC</sub>	170		225	W 187	ns	
Access Time from RAS	tRAC		150	- about	200	ns	4,6
Access Time from CAS	LCAC .	12-	100	15	135	ns	5,6
Output Buffer Turn-off Delay	taFF	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t <sub>T</sub>	3	35	3	50	ns	3
RAS Precharge Time	t <sub>RP</sub>	100	-	120	3. 7	ns	
RAS Pulse Width	tras	150	10000	200	10000	ns	
RAS Hold Time	t <sub>RSH</sub>	100	-	135	-	ns	
CAS Pulse Width	teas	100	-	135	-	ns	STIPW
CAS Hold Time	t <sub>csH</sub>	150	-	200	-	ns	
RAS to CAS Delay Time	tRCD	20	50	25	65	ns	8
CAS to RAS Precharge Time	t <sub>CRP</sub>	-20		-20	11 11	ns	
Row Address Set-up Time	tASR	0	-	0		ns	
Row Address Hold Time	t <sub>RAH</sub>	20	-	25	11-	ns	
Column Address Set-up Time	LASC	-10		-10	-	ns	
Column Address Hold Time	LCAN	45	and the second	55	under -	ns	
Column Address Hold Time referenced to RAS	tAR	95	Ŧ	120	-	ns	
Read Command Set-up Time	LRCS	0	-	0	-	ns	
Read Command Hold Time	tRCH	0	-	0	- 12	ns	
Write Command Hold Time	twch	45	-	55	-	ns	
Write Command Hold Time referenced to RAS	twcr	95	-	120	-	ns	
Write Command Pulse Width	twp	45		55	-	ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	45	-	55	-	ns	
Write Command to CAS Lead Time	t <sub>CWL</sub>	45	-	55	-	ns	
Data-in Set-up Time	tos	0	-	0	-	ns	9
Data-in Hold Time	t <sub>DH</sub>	45	0.31299	55	00-01-02	ns	9
Data-in Hold Time referenced to RAS	t <sub>DHR</sub>	95	-	120	-	ns	
CAS Precharge Time (for Page-mode Cycle Only)	t <sub>CP</sub>	60	T	80	-	ns	
Refresh Period	l REF	ul <u>-</u> -	2	-	2	ms	
Write Command Set-up Time	twes	-20	+	-20	-	ns	10
CAS to WE Delay	town	60	<b>T</b>	80	-	ns	10
RAS to WE Delay	t RW D	110	-	145	-	ns	10
RAS Precharge to CAS Hold Time	1 RPC	0	+	0	-	ns	

NOTES

- 1. AC measurements assume  $t_T = 5$ ns.
- 8 cycles are required after power-on or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- 3.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 4. Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table  $t_{RAC}$  exceeds the value shown.
- 5. Assumes that  $t_{RCD} \ge t_{RCD}$  (max).
- Measured with a load circuit equivalent to 2TTL loads and 100 pF.
- t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 8. Operation with the  $t_{RCD}$  (max) limit insures that

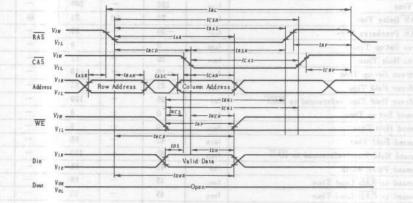
 $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively be  $t_{CAC}$ .

- controlled exclusively be t<sub>CAC</sub>.
  9. These parameters are reference to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
- 10.  $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge t_{RWD}$  (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

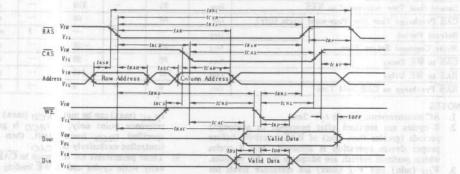


Row Address Column Address VIL tacs taca WE VIN . Vit--te at toFF --IN AC Vos Dout Open Valid Data Vol

**WRITE CYCLE** 



#### READ-WRITE/READ-MODIFY-WRITE CYCLE



mercurine there is input again. Also, transition the second obtained between  $V_{III}$  and  $V_{III}$ .

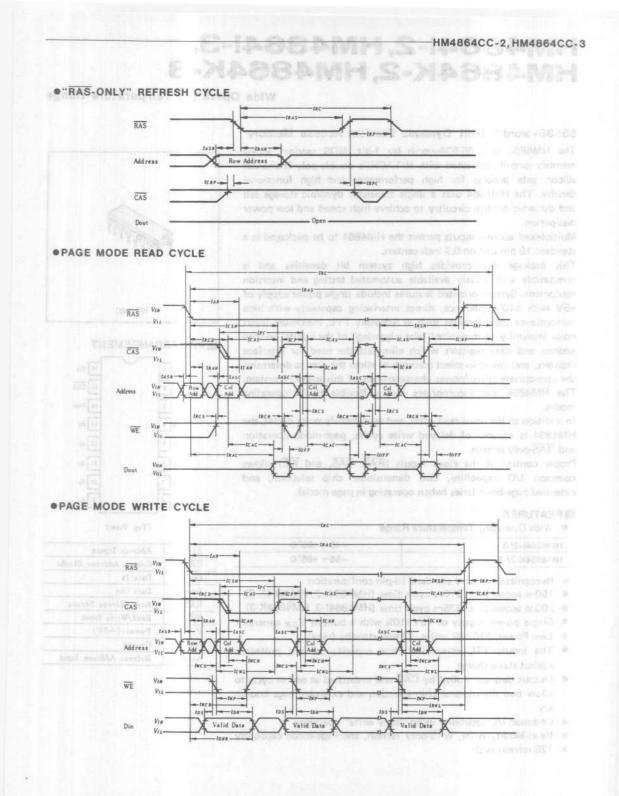
- Accurate that Inc., 1 April (MAN), Where beginning then the maximum according value above to the failly (page seconds the value above).
  - Augentian that (ACD 2 (Acm (Max).
- Missioned which is need directly represented to 21.23, longly such 100 pK.
- (j) set and the next the time at which the enquire enderer the open simple condition and it tilt white enced to optimit volume length.
- Operation with the research their lances that

while of molecuedity with twenty formers and spine 4 minimitation. They are interactional obstantiations: the grade is an early with well remain open carries the authors cyclics if form 3 with a surface cyclics if form 3 the authors of the stream is contigue of the stream is

ero (max) it specified as a acco is present than the gift, then access time in

al equa pribad 2 4 3 of 5 p bryalab al equa pribas 3

and periods well-litter (for as an iterating state with a useful (mini) growt) S growt is the ring two state sets bare slaves tourdgowalls (non-invente right S growp) bits (mina) growt is state with long slaveshers i is dise hermolies aff monthes with footbarte at monthes platebart is (writh seence sc



## HM4864I-2, HM4864I-3, HM4864K-2, HM4864K-3

Wide Operating Temperature Range

#### 65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of  $\pm 5V$  with  $\pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and RAS-only refresh.

Proper control of the clock inputs (RAS, CAS, and  $\overline{WE}$ ) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

#### FEATURES

Wide Operating Temperature Range

HM48641-2/-3	-40∼ +85°C
HM4864K-2/-3	-55∼ +85° C

Recognized industry standard 16-pin configuration

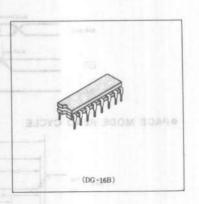
- 150ns access time, 270ns cycle time (HM4864I-2, HM4864K-2)
- 200ns access time, 335ns cycle time (HM4864I-3, HM4864K-3)

Single power supply of +5V±10% with a built-in V<sub>BB</sub> generator

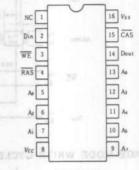
- Low Power; 330 mW active. 22 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation

Read-Modify-Write, RAS-only refresh, and Page-mode capability

128 refresh cycle



#### PIN ARRANGEMENT

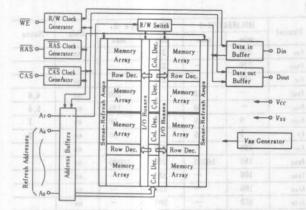


(T			

A A .	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
Ao-As	Refresh Address Input

HM48641-2, HM48641-3, HM4864K-2, HM4864K-3

#### FUNCTIONAL BLOCK DIAGRAM



#### ABSOLUTE MAXIMUM RATINGS Voltage on any pin relative Operating Temperature, Ta (Ambient) . . -40 to +85°C (HM48641 Series) -55 to +85°C (HM4864K Series) Storage Temperature (Ambient) . . . . . . . . . . . . -65 to +150°C Short-circuit Output Current . 50 mA Power Dissipation . . . . . . . . 1 W amil 168 37

#### RECOMMENDED DC OPERATING CONDITIONS (Ta=-40 to +85°C)

Parameter	Symbol	min	typ	max	Unit	Notes
	Vcc	4.5	5.0	5.5	v	and a sub
upply Voltage	Vss	0	0	0	V	otoma A fidvas
Input High Voltage	V <sub>IH</sub>	2.4	-	6.5	V	with a 1 meta
Input Low Voltage	VIL	-1.0	- 51	0.8	V	1

#### **DC** ELECTRICAL CHARACTERISTICS ( $T_a = -40$ to $+85^{\circ}C^{*}V_{cc} = 5V \pm 10\%, V_{ss} = 0V$ )

Parameter		Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling; tac=	min.)	Icci	of Neutron	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS} = V_{IK}$ Dout = High Impedance)	April 1	Iccz	<u>- 570</u>	4	mA	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS - Vin; t rc - min.)	Seat 1	lees	-	45	m A	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation (RAS = V <sub>1</sub> , CAS Cycling; t <sub>PC</sub> = min.)	Part Inge	Ice .	1 8.58 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	45	mA	2,4
INPUT LEAKAGE Input Leakage Current, any Input $(V_{s}=0 \text{ to } +6.5V, \text{ all other pin} \text{ under test} = 0V)$	s not	Iu	-10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, Veer=0 to +5.5V)	1 Level	ILO	-10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage (I <sub>est</sub> = -5mA) Output Low (Logic 0) Voltage (I <sub>est</sub> = 4.2mA)		Voin Vol	2.4	Vcc 0.4	V V	DIES ACR

#### NOTES

1. All voltages referenced to VSS.

2. I<sub>CC</sub> depends on output loading condition when the device is selected. I<sub>CC</sub> max. is specified at the output open condition.

3. ILO consists of leakage current only.

4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate. then are mean with between Pros

5. \*: HM4864K Series;  $T_{\rm B} = -55$  to +85°C

AC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Ta=25°C)

Parameter disso and als	Symbol	typ	max	Unit	Notes
Input Capacitance (Ao-Ar, Din)	Cast		7	pF	1
Input Capacitance (RAS, CAS, WE)	Cut	-	10	pF	001.1-1
Output Capacitance (Dout)	Ceel 1	etuo sett da	the is of it of	pF	1,2

NOTES

Capacitance measured with Boonton Meter or effective capacitance measuring method.
 CAS = V<sub>IH</sub> to disable D<sub>OUT</sub>.

2.  $\overline{CAS} = V_{IH}$  to disable D<sub>OUT</sub>.

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS 13, 23

Parameter	C. 1	HM 486	4I/K-2	HM4864I/K-3		
Farameter	Symbol	min	max	min	max	
Random Read or Write Cycle Time	tac	270		335	(mol-	
Read-Write Cycle Time	t <sub>RWC</sub>	270		335	-	
Page Mode Cycle Time	t <sub>PC</sub>	170		225	100 P 22	
Access Time from RAS	1 RAC	-	150	Non	200	
Access Time from CAS	LCAC	-	100	1.00	135	
Output Buffer Turn-off Delay	LOFF	0	40	0	50	
Transition Time (Rise and Fall)	l <sub>T</sub>	3	35	- 3	50	
RAS Precharge Time	tRP	100		120	Get in at	
RAS Pulse Width	tRAS	150	10000	200	10000	
RAS Hold Time	tRSH	100	4.4	135	1.11	
CAS Pulse Width	teas	100		135	-	

 $(T_a = -40 \text{ to } +85^{\circ}C^{*}V_{cc} = 5V \pm 10\%, V_{ss} = 0V)$ 

ns ns ns 200 ns 4.6 135 5.6 ns 50 ns 7 50 3 ns \_ ns 0000 ns ns ns CAS Hold Time 150 200 tesn ns RAS to CAS Delay Time 20 50 25 ns 8 trep 65 CAS to RAS Precharge Time 20 20 terp ns Row Address Set-up Time LASA 0 0 ns Row Address Hold Time 20 25 tRAH ns Column Address Set-up Time -5 - 5 tasc ns 45 55 Column Address Hold Time LCAN ns 95 120 Column Address Hold Time referenced to RAS LAR ns Read Command Set-up Time 0 0 tacs ns Read Command Hold Time 0 0 23 LACH ns Write Command Hold Time twen 45 55 ns Write Command Hold Time referenced to RAS 95 120 twee ns Write Command Pulse Width 45 120 55 twp \_ ns Write Command to RAS Lead Time 45 55 LRWL ns Write Command to CAS Lead Time 45 55 town \_ ns 0 0 9 Data-in Set-up Time Lps ns Data-in Hold Time 45 55 ns 9 ton 95 120 Data-in Hold Time referenced to RAS LONA DS. CAS Precharge Time (for Page-mode Cycle Only) 60 80 1 ter ns Refresh Period 2 2 ms LREF Write Command Set-up Time twes 10 -10 ns 10 CAS to WE Delay 60 80 10 tewp ns 110 RAS to WE Delay 145 10 tawn Ins RAS Precharge to CAS Hold Time 0 0 Lanc -ns

NOTES

- 1. AC measurements assume  $t_T = 5$ ns.
- 2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of RAS inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- 3.  $V_{IIH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 4. Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table  $t_{RAC}$  exceeds the value shown.
- 5. Assumes that  $t_{RCD} \ge t_{RCD}$  (max).
- 6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
- 7. toFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 8. Operation with the  $t_{RCD}$  (max) limit insures that

 $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively be  $t_{CAC}$ .

Unit

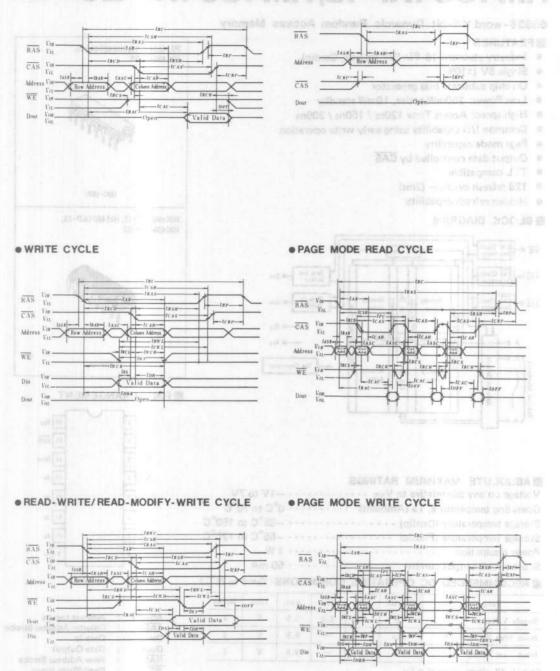
Notes

- 9 These parameters are reference to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
- twcs, tcwp and tRwp are not restrictive operating 10. parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge$  $t_{RWD}$  (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- 11. \*: HM4864K Series; T<sub>a</sub> = -55 to +85°C

### TIMING WAVEFORMS

READ CYCLE

#### . "RAS-ONLY" REFRESH CYCLE



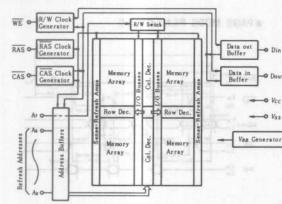
## HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

65536-word ×1-bit Dynamic Random Access Memory

#### FEATURES

- Industry standard 16- Pin DIP (plastic, Cerdip)
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120ns / 150ns / 200ns
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by CAS
- TTL compatible
- 128 refresh cycles (2ms)
- Hidden refresh capability

#### BLOCK DIAGRAM



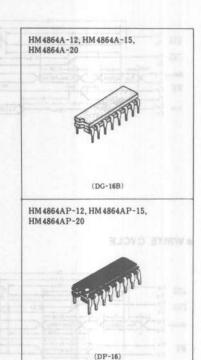
#### BABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to	Vss ·		 	<ul> <li>-1V to 7V</li> </ul>
Operating temperature, Ta (A	mbient	t) .	 	0°C to 70°C
Storage temperature (Cerdip)			 	-65°C to 150°C
Storage temperature (Plastic)			 	-55°C to 125°C
Power dissipation			 	• 1 W
Short circuit output current			 	50 mA

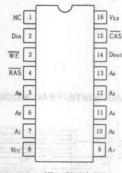
#### RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	mín.	typ.	max.	Unit	Notes
Supply Voltage	Vec	4.5	5.0	5.5	V	1
Input High Voltage	VIII	2.4	-	6.5	v	1
Input Low Voltage	Vit	-1.0	-	0.8.	V	1

Notes : 1. All voltages referenced to V >>>



#### PIN ARRANGEMENT



(Top View)

A0-A7	1	Address Inputs
CAS		Column Address Strobe
Din	- :	Data In
Dout	2	Data Output
RAS	-	Row Address Strobe
WE	3	Read/Write Input
Vcc	4	Power (+5V)
VSS	2	Ground
A0-A6	1	Refresh Address Inputs



#### HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

and the second se	0.11	HM4864A/P-12		HM4864A/P-15		HM4864A/P-20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	ma x	Unit	THOLES
Operating Current(RAS,CAS Cycling: tac-min)		-	55	.(0 <del></del> 36	50	11-1-1	44	mA	1,2
Standby Cnrrent(RAS = VIN, Dout = High Impedance)		11-104	3.5	1962	3.5	0.0410	3.5	mA	
Refresh Current(RAS Cycling, CAS = VIII, tRC=min)		-	42	-	38	-	33	mA	2
Standby Current(RAS-Vin, Dout Enable)		-	5.5	-	5.5	1,0771.5	5.5	mA	1
Page Mode Current(RAS - VIL, CAS Cycling; trc=min)	Iccs	1 -	38	-	35	-	31	mA	1,2
Input Leakage(0 < V <sub>est</sub> < 5.5V)		-10	10	-10	10	-10	10	μA	
Output Leakage(Dout is disabled, 0 < Vout < 5.5V)		-10	10	-10	10	-10	10	μA	6
Output Levels High(Int = -5mA)		2.4	Vcc	2.4	Vcc	2.4	Vec	V	1.
Output Levels Low(Int=4.2mA)		0	0.4	0	0.4	0	0.4	V	13

#### DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±10%, Vss=0V)

Notes) 1.  $I_{cc}$  depends on output loading condition when the device is selected.  $I_{\alpha}$  max, is specified at the output open condition. 2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate. **CAPACITANCE** ( $V_{cc} = 5V \pm 10\%$ ,  $Ta = 25^{\circ}C$ )

#### Notes Symbol Unit Parameter typ max pF C ... 1 -5 1 Ao~Ar, Din Input Capacitance pF RAS. CAS. WE Cist -10 1 1, 2 7 pF Cast Output Capacitance Dout ----

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{CAS} = V_{in}$  to disable Dout.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to 70°C, Vcc=5V±10%, Vss=0V)

Desembles	Symbol	HM 48	364A-12	HM4864A-15		HM4864A-20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Access Time From RAS	L RAC	-	120	-	150	-	200	ns	2,3
Access Time From CAS	t CAC		60	1 alter	75	-	100	ns	3,4
Output Buffer Turn-off Delay	torr	T.	35	1	40	-	50	ns	5
Transition Time (Rise and Fall)	1 <sub>T</sub>	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	1 RC	220	-	260	-	330	-	ns	
RAS Precharge Time	LAP	90	-	100	-	120	-	ns	
RAS Pulse Width	tRAS	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	LCAS	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	taco	25	60	25	75	30	100	ns	7
RAS Hold Time	trish	60	-	75	-	100	-	ns	
CAS Hold Time	tesn	120	-	150	-	200	-	ns	
CAS to RAS Precharge Time	temp	-10	-	-10	-	-10	-	ns	
Row Address Set-up Time	tasa	0	-	0	-	0	-	ns	
Row Address Hold Time	1 RAH	15		15	ISTH!	20	181 +1	ns	TIAN
Column Address Set-up Time	tasc	0	-	0	-	0	- 1	ns	
Column Address Hold Time	tCAH	20	-	25	-	30	-	ns	
Column Address Hold Time Referenced to RAS	LAR	80	-	100	- 1	130	-	ns	
WE Command Set-up Time	Iwes	0		0	-	0	-	ns	8
Write Command Hold Time	tw cH	40		45	-	55	-	ns	
Write Command Hold Time Referenced to RAS	twen	100	1 -	120	-	155	-	ns	-
Write Command Pulse Width	twp	40	-	45	-	55	-	ns	
Write Command to RAS Lead Time	tawi	40	-	45	-	55	-	ns	
Write Command to CAS Lead Time	tews	40	1/-	45	-	55	-	ns	-
Data-in Set-up Time	tos	0		0	A.A.	0	-	ns	9
Data-in Hold Time	1 DH	40	-	45	-	55	-	ns	9
Data-in Hold Time Referenced to RAS	Lour	100	-	120	-	155	-	ns	-
Read Command Set-up Time	tacs	0	- /	0	-	0	-	ns	
Read Command Hold Time Referenced to CAS	t RCH	0		0	-	0	-	ns	
Read Command Hold Time Referenced to RAS	t RRH	10		10		10	-	ns	
Refresh Period	tREF		2	-	2	-	2	ms	
Read-Write Cycle Time	L RW C	245	-	280	-	345	-	ns	
CAS to WE Delay	town	40		45	-	55		ns	8
RAS to WE Delay	t RW D	100	-	120	-	155	-	ns	
Page Mode Cycle Time	1 pc	120	-	145	-	190	-	ns	
CAS Precharge Time (for Page-mode Cycle Only)	lep	50	-	60	-	80	-	ns	
CAS Precharge Time	topy	30		35	-	45	-	ns	
RAS Precharge to CAS Hold Time	LAPC	0	-	0	-	0	-	ns	

#### HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

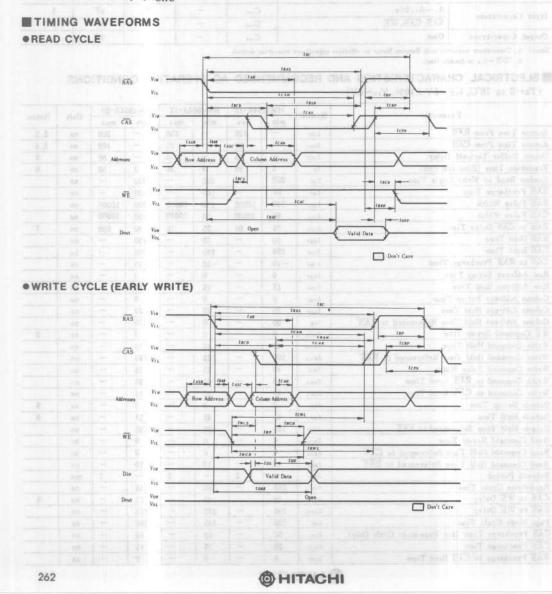
#### Notes

- 1. AC measurements assume  $t_T = 5$ ns.
- Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that  $t_{RCD} \ge t_{RCD}$  (max).
- t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 6.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 7. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .

 t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters.

They are included in the data sheet is electrical characteristics only; if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge t_{RWD}$  (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

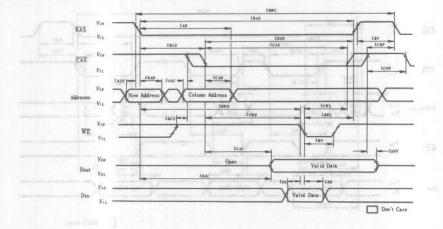
- There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- An initial pause of 100µs is required after power-up followed by a minimum of 8 initialization cycles.



#### 

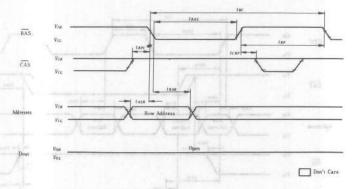
#### **• READ- WRITE/READ-MODIFY-WRITE CYCLE**

#### SJOVO BTLAM LOOM SDARE

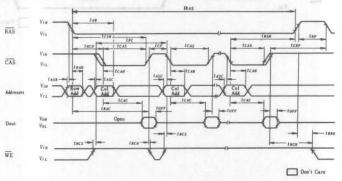


#### **• "RAS-ONLY" REFRESH CYCLE**

AND BEARING WEIGHT

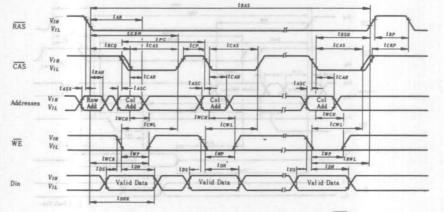


PAGE MODE READ CYCLE



#### HM4864A-12, HM4864A-15, HM4864A-20 HM4864AP-12, HM4864AP-15, HM4864AP-20

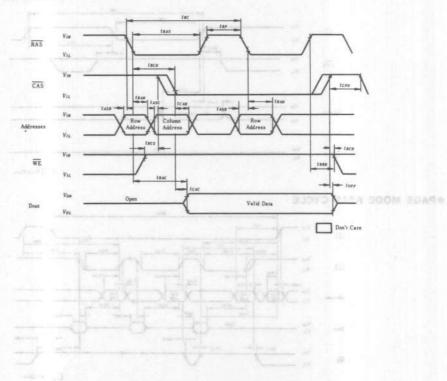
#### **OPAGE MODE WRITE CYCLE**



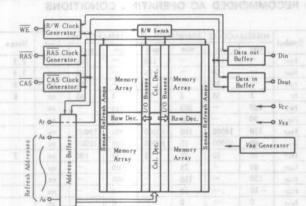
Don't Care

**HIDDEN REFRESH CYCLE** 

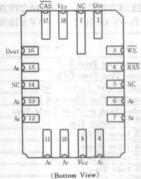












#### ■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V <sub>SS</sub>	-1V to +7V
Operating temperature, Ta (Ambient) 0°	C to +70°C
Storage temperature	to +150°C
Power Dissipation	
Short circuit output current	50mA

A0-A7	:	Address Inputs
CAS		Column Address Strobe
Din	4	Data In
Dout	:	Data Output
RAS	1	Row Address Strobe
WE	:	Read/Write Input
Vcc	:	Power (+5V)
VSS	-	Ground
A0-A6	Υ.	Refresh Address Inputs

#### ERECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	'typ.	max.	Unit	Notes
Supply Voltage	Vec	4.5	5.0	5.5	v	1
Input High Voltage	VIN	2.4		6.5	V	1
Input Low Voltage	VIL	-1.0	-	0.8	V	1

Notes : 1. All voltages referenced to Vas

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept, regarding specifications.



	0 11	HM4864ACG-12		HM4864ACG-15		HM4864ACG-20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	ma x	Unit	INOTES
Operating Current(RAS, CAS Cycling: tac=min)	Icci	-	55	-	50	-	44	mA	1,2
Standby Cnrrent(RAS - VIN, Dout - High Impedance)	Icci	100 700	3.5		3.5		3.5	mA	Contraction in
Refresh Current(RAS Cycling, CAS - VIN, tRC-min)	Icca	-	42	-	38	-	33	mA	2
Standby Current(RAS - VIN. Dout Enable)	Iccs	-	5.5	-	5.5	1. +	5.5	mA	1
Page Mode Current(RAS-VIL, CAS Cycling; tPc-min)	Icce	-	38	-	35	- 1	31	mA	1,2
Input Leakage(0 < Vast < 6.5V)	ILI	-10	10	-10	10	-10	10	μA	
Output Leakage(Dout is disabled, 0 < V rest < 5.5V)	ILO	-10	10	-10	10	-10	10	µA_	
Output Levels High(Int = -5mA)	VON	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	1921
Output Levels Low(Iest=4.2mA)	Vol	0	0.4	0	0.4	0	0.4	V	111

der.

#### DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±10%, Vss=0V)

Notes) 1. Icc depends on output loading condition when the device is selected, I<sub>0</sub> max, is specified at the output open condition. 2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

#### **EXAMPACITANCE** $(V_{cc}=5V\pm10\%, Ta=25^{\circ}C)$

	Symbol	typ	max	Unit	Notes		
	Ao~Ar, Din	Cial	-	5	pF	1	
Input Capacitance	RAS, CAS, WE	Cist	-	10	pF	1	
Output Capacitance	Dout	Cest	-	7	pF	1, 2	

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method. 2.  $\overline{CAS} = V_{ij}$  to disable Dout.

#### **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS** $(T_{a}=0 \text{ to } 70^{\circ}\text{C}, V_{cc}=5 \text{V} \pm 10\%, V_{ss}=0 \text{V})$

Parameter	Symbol	HM4864	ACG-12	HM4864ACG-15		HM4864ACG-20		Unit	Notes
Farameter	Symbol	min	max	min	max	min	max	-	TAOLE
Access Time From RAS	truc	-	120	-	150	-	200	ns	2,3
Access Time From CAS	teac		60	-	75	-	100	ns	3,4
Output Buffer Turn-off Delay	LOFF	1	35	-	40		50	ns	5
Transition Time (Rise and Fall)	17	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	LRC	220	-	260	-	330	-	ns	
RAS Precharge Time	LAP.	90	-	100	-	120		ns	
RAS Pulse Width	I RAS	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	I CAS	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	LACD	25	60	25	75	30	100	ns	7
RAS Hold Time	L RSH	60	-	75	-	100	-	ns	15
CAS Hold Time	lcs#	120	-	150	11 +1	200	-	ns	13
CAS to RAS Precharge Time	tCRP	-10	-	-10	1. 1. 1.	-10		ns	1.8
Row Address Set-up Time	LASR	0	-	0	15-00	0	1	ns	
Row Address Hold Time	LRAH	15	-	15	-	20	-	ns	
Column Address Set-up Time	LASC	0	-	0	017.53	0	YAR.	ns	12.03.8
Column Address Hold Time		20	-	25	-	30	-	ns	
Column Address Hold Time Referenced to RAS		80	-	100	-	130	-	ns	
WE Command Set-up Time		0		0	There is a	0	-	ns	8
Write Command Hold Time	twen	40		45		55	0(1)(22)(0	ns	00.010
Write Command Hold Time Referenced to RAS	twee	100		120	-	155	. 1750	ns	1 366
Write Command Pulse Width	twp	40	-	45	-	55	0.0.00	ns	10 100
Write Command to RAS Lead Time	t RW L	40	-	45	-	55	-	ns	
Write Command to CAS Lead Time	tcw1	40	-	45	-	55	-	ns	
Data-in Set-up Time	tos	0	-	0	-	0	-	ns	9
Data-in Hold Time	t DH	40	1 T INCEN	45	1100	55	-	ns	9
Data-in Hold Time Referenced to RAS	tour	100	-	120	-	155	-	ns	
Read Command Set-up Time	tacs	0		0		0		ns	
Read Command Hold Time Referenced to CAS	LRCH	0	- 40	0	-	0	-	ns	1.1.25
Read Command Hold Time Referenced to RAS	LRRH	10	-	10	-	10	-	n's	121 years
Refresh Period	LREF	-	2	-	2	-	2	ms	
Read-Write Cycle Time	LRWC	245	-	280	-	345	-	ns	
CAS to WE Delay	1 CW D	40	-	45	-	55		ns	8
RAS to WE Delay	L RW D	100	-	120	-	155	-	ns	
Page Mode Cycle Time	tre	120	1000	145		190	100	ns	1 1 2 2
CAS Precharge Time (for Page-mode Cycle Only)	ter	50	4	60	-	80	-	ns	
CAS Precharge Time	topn	30	-	35	-	45	-	ns	
RAS Precharge to CAS Hold Time	LAPC	0	-	0	-	0	-	ns	

Notes

- 1. AC measurements assume  $t_T = 5$ ns.
- 2. Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
- 3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that  $t_{RCD} \ge t_{RCD}$  (max). 5.  $t_{OFF}$  (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 6.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 7. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by tCAC.

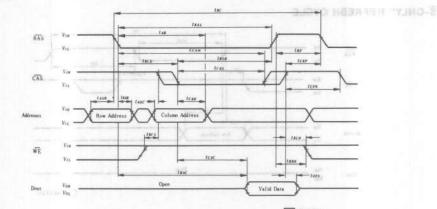
#### TIMING WAVEFORMS

#### **OREAD CYCLE**

8. twcs, tcwp and tRwp are not restrictive operating parameters.

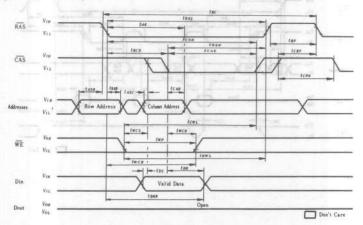
They are included in the data sheet is electrical characteristics only; if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge t_{RWD}$  (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate,

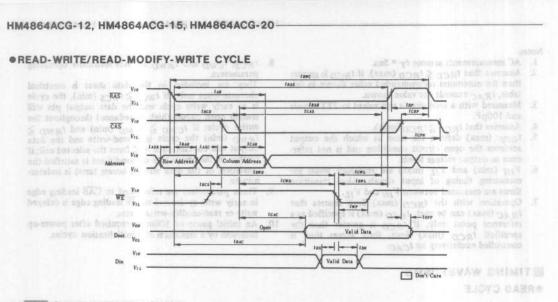
- 9. There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- 10. An initial pause of 100µs is required after power-up followed by a minimum of 8 initialization cycles.



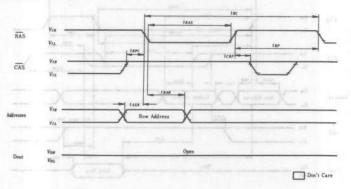
Don't Care BLOYD DATH BOOM BDAG+

#### **WRITE CYCLE (EARLY WRITE)**

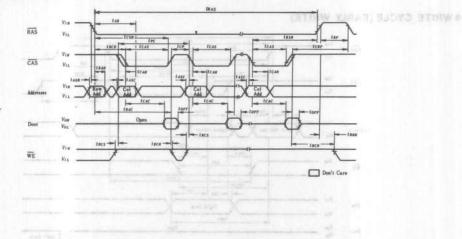




**• "RAS-ONLY" REFRESH CYCLE** 







HM4864ACG-12, HM4864ACG-15, HM4864ACG-20

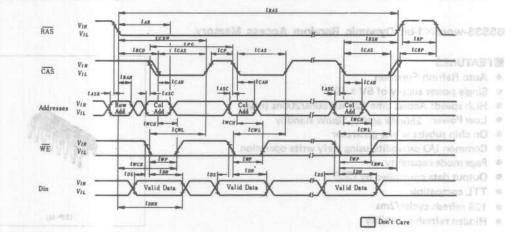
10.0

RABAM

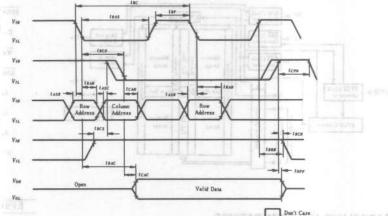
#### **@PAGE MODE WRITE CYCLE**

Strate Strate

1 (A) (C)



#### HIDDEN REFRESH CYCLE



#### Don't Care

		Power Divarpation
	wit .	

#### BRECOMMENDUD DO OPERATING CONDITIONS (Ta-0 to + 70°C)

alae		
	1.8	

# RAS

CAS Addresses WE Doot

Panker [ FEV]

## HM4865AP-12, HM4865AP-15 HM4865AP-20

65536-word×1-bit Dynamic Random Access Memory

#### FEATURES

- Auto Refresh Function
- Single power supply of 5V ± 10%
- High speed: Access time 120ns/150ns/200ns (max.)
- Low Power: 250mW active, 18mW standby
- On chip substrate bias generator
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by CAS
- TTL compatible
- 128 refresh cycles/2ms
- Hidden refresh capability

#### BLOCK DIAGRAM



Din

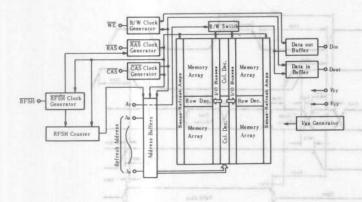
WE

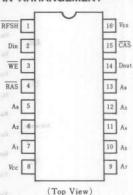
Ae

As

Vcc

(DP-16)





#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit
Voltage on any pin	VT	-1.0 to +7.0	V
Supply Voltage	Vcc	-1.0 to +7.0	v
Short Circuit Output Current	Int	50	mA
Power Dissipation	Pr	1.0	W
Operating Temperature	Tapt	0 to +70	°C
Storage Temperature	Tate	-55 to +125	°C

RFSH	Refresh
A.~A.	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
Ao~As	Refresh Address Inputs

with respect to Vas

#### **RECOMMENDED DC OPERATING CONDITIONS** (*Ta*=0 to +70°C)

Item	Symbol	min	typ	max	Unit
S 1 1/1	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	v
1	VIH	2.4	-	6.5	V
Input Voltage	VIL	-1.0	-	0.8	v

**OHITACHI** 

Note) All voltages referenced to Vas-

File Hus Ekill Otob - 47-21	8 11	HM4865A/P-12		HM4865A/P-15		HM4865A/P-20		Unit	Notes
Parameter	Symbol	min	max	min	max	min	ma x	Unit	Hores
Operating Current(RAS,CAS Cycling: tRc=min)	Icci		55	-	50	-	44	mA	1,2
Standby Cnrrent(RAS = VIH, Dout = High Impedance)	Icci	-	3.5	-	3.5	-	3.5	mA	
Refresh Current(RAS Cycling, CAS = VIH, tRC = min)	Icca	-	42	-	38	-	33	mA	2
Standby Current(RAS = VIN, Dout Enable)	Iccs	1000	5.5	-	5.5	- 22	5.5	mA	1
Page Mode Current(RAS-VIL, CAS Cycling; tPC=min)	Iccs	-	38	0 mail	35	00 -	31	mA	1,2
Auto Refresh Current ( $\overline{\text{RFSH}}$ - Cycle, $\overline{\text{RAS}}$ - $V_{IH}$ )	Icci		44	-	40	-	35	mA	
Input Leakage(0 < V at < 6.5V)	ILI	-10	10	-10	10	-10	10	μA	
Output Leakage(Dout is disabled, 0 < Vant < 5.5V)	ILO	-10	10	-10	10	-10	10	μA	
Output Levels High(I <sub>sat</sub> =-5mA)	VOH	2.4	Vcc	2.4	Vcc	2.4	Vcc	v	34
Output Levels Low(Int=4.2mA)	Vol	0	0.4	0	0.4	0	0.4	V	43 27

DC ELECTRICAL	CHARACTERISTICS	Ta=0 to 70	$^{\circ}C$ , $V_{cc} = 5V$	$\pm 10\%, V_{ss} = 0V$
---------------	-----------------	------------	-----------------------------	-------------------------

Notes) 1. Icc depends on output loading condition when the device is selected, Icc max is specified at the output open condition. 2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

#### **CAPACITANCE** ( $V_{cc} = 5V \pm 10\%$ , $Ta = 25^{\circ}C$ )

	Parameter	Symbol	typ	max	Unit	Notes
	A <sub>0</sub> ~A <sub>7</sub> , Din	Cint	-	5	pF	1
Input Capacitance	RAS, CAS, WE	Cinz	-	10	pF	1
Output Capacitance	Dout	Cout	-	7	pF	1. 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS - VIH to disable Dout.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS $(T_a=0 \text{ to } 70^{\circ}\text{C}, V_{cc}=5 \text{V} \pm 10\%, V_{ss}=0 \text{V})$

**EAC CHARACTERISTICS** (Vcc=5V±10%, Vss=0V, Ta=0 to +70°C)<sup>13,23</sup>

Martinen entern - of gine series in this table		HM4865AP-12		HM486	5AP-15	HM486	5AP-20	Unit	Notes
Item	Symbol	min	max	min	max	min	max	Unit	Note
Random Read or Write Cycle Time	t <sub>RC</sub>	220	-	260	11 (C.20)	330	14102 900	ns	
Read-Write Cycle Time	L RNC	245	a and an	280	smit un	345	1.50	ns	
Page Mode Cycle Time	t <sub>PC</sub>	120	-	145		190	partie + ka	ns	
Access Time from RAS	t RAC	81 <u>10</u> 0	120	iloni <u>t (</u> a	150	n ad Ein	200	ns	4, 6
Access Time from CAS	t CAC	Ser PERI	60	These is	75	CONT.	100	ns	5, 6
Output Buffer Turn-off Delay	LOFF	in and	35	1 01 200	40	10 100	50	ns	1
Transition Time(Rise and Fall)	t T	3	35	3	35	3	50	ns	1
RAS Precharge Time	t <sub>RP</sub>	90	10 6700	100	12 200 _QV	120	CF7721	ns	
RAS Pulse Width	tRAS	120	10000	150	10000	200	10000	ns	
RAS Hold Time	l RSH	60	conc-	75	un un	100	s notice	ns	
CAS Pulse Width	teas	60	10000	75	10000	100	10000	ns	
CAS Hold Time	t <sub>csn</sub>	120	-	150	-	200	-	ns	
RAS to CAS Delay Time	t RCD	25	60	25	75	30	100	ns	
CAS to RAS Precharge Time	t CRP	-10	-	-10	-	-10	-	ns	
Row Address Set-up Time	LASR	0	-	0	-	0	-	nis	
Row Address Hold Time	t RAH	15	-	15	-	20	-	ns	
Column Address Set-up Time	LASC	0		0	-	0	-	ns	
Column Address Hold Time	t CAH	20	-	25	-	30	-	ns	
Column Address Hold Time referenced to RAS	LAR	80	-	100	-	130	-	ns	
Read Command Set-up Time	trcs	0	-	0	-	0	-	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	-	0	-	0	-	ns	
Write Command Hold Time	t wCN	40	-	45	-	55	-	ns	
Write Command Hold Time referenced to RAS	twcr	100	-	120	-	155	-	ns	
Write Command Pulse Width	t wp	40	-	45	-	55	-	ns	
Write Command to RAS Lead Time	t RWL	40	-	45	-	55	-	ns	



#### HM4865AP-12, HM4865AP-15, HM4865AP-20

Item Start				HM4865AP-15		HM4865AP-20		Unit	Notes	
Item	Symbol	min	max	min	max	min	ınax	Unit	Notes	
Write Command to CAS Lead Time	t <sub>CWL</sub>	40	-	45	-	55	-	ns		
Data-in Set-up Time	tos	0	-	0	na tr <u>sen</u> th	0	2.44	ns	9	
Data-in Hold Time	t DH	40		45	1000 1000 1000 1000 1000 1000 1000 100	55		ns	9	
Data-in Hold Time referenced to RAS	t <sub>DHR</sub>	100	-	120	1.1.1	155	2751	ns	San P	
CAS Precharge Time(for Page-mode Cycle Only)	tcp	50	<u>(in</u> )	60	-	80	11	ns	16 200	
Refresh Period	tREF	<u> </u>	2	Coller.	2	0- <u>T</u> 6.	2	ns	port inter	
Write Command Set-up Time	twes	0	-	0	1	0	-	ns	10	
CAS to WE Delay	t <sub>CWD</sub>	40	-	45	-	55	1752)	ns	10	
RAS to WE Delay	t RWD	100	-	120	-	155	1 - <del>1 -</del> -	ns	Designed	
RAS Precharge to CAS Hold Time	L RPC	0	-	0	_	0		ns	. Carto	
Read-modify-write Hold Time	t RRH	10	7.	10	20.00	10	1 20	ns		
CAS Precharge Time	topn	30	-	35	-	45		ns		
RFSH Set-up Time	LFSR	90	-	100		120	-	ns		
RAS to RFSH Delay Time	t RFD	90	-	100	15-31	120	-	ns	n na	
RFSH Cycle Time	1 FC	220	-	260	-	330	-	ns		
RFSH Pulse Width	1 FP	120	5000	150	5000	200	5000	ns	1 60	
RFSH Precharge Time	t <sub>FT</sub>	90	-	100	-	120	و تقصر المحاد	ns	13	

Notes) 1. AC measurements assume  $t_T = 5ns$ .

2. An initial pause of 100µs is required after power-up followed by a minimum of 8 initialization of cycles.

 V<sub>IH</sub>(min) and V<sub>IL</sub>(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.

 Assumes that t<sub>RCD</sub> = t<sub>RCD</sub>(max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> exceeds the value shown.

5. Assumes that t<sub>RCD</sub>-t<sub>RCD</sub>(max).

6. Measured with a load circuit equivalent to 2TTL loads and 100pF.

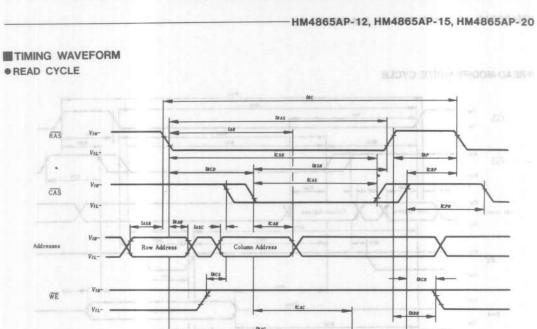
 t<sub>OFF</sub>(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

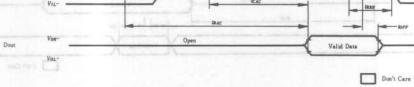
 Operation with the t<sub>RCD</sub>(max) limit insures that t<sub>RAC</sub>(max) can be met, t<sub>RCD</sub> (max) is specified as a reference point only, if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub>(max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.

 These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.

10. t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t<sub>WCS</sub> = t<sub>WCS</sub>(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t<sub>CWD</sub> = t<sub>CWD</sub>(min) and t<sub>RWD</sub>(min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

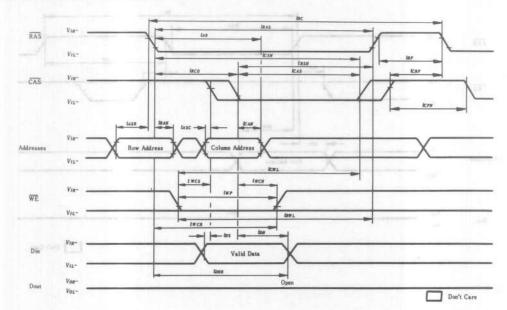
	0			
				Calmen Address Set on Trees
			- 48	Ciline Astroit Edd T as referenced to EAS
10				
1.110.				
	88	-88		







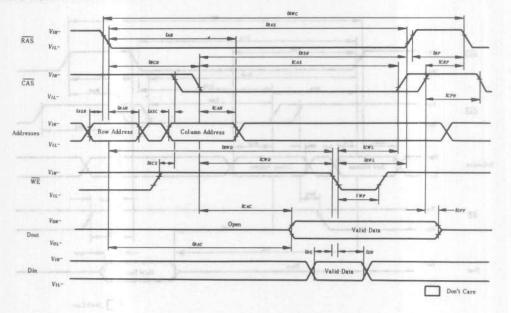
\*RAS CHEV REFRIGH CYCL



273

HM4865AP-12, HM4865AP-15, HM4865AP-20-

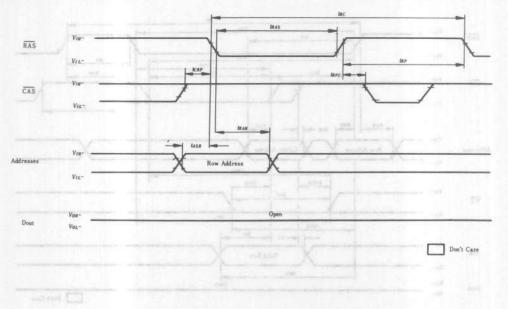




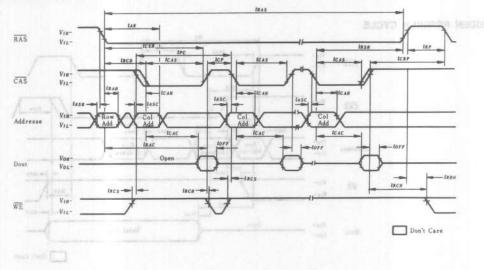


(温脂(熱液、大口) (名) ヨロの古の 田山和林市

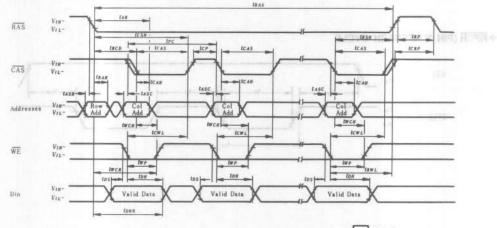
MROTEVAW SMEARING IN



#### PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



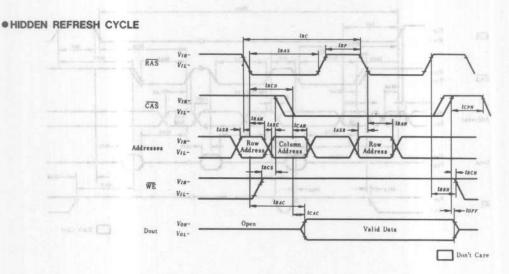
Don't Care

**OHITACHI** 

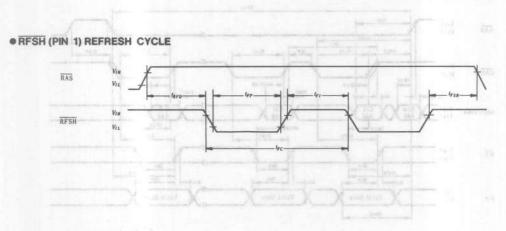
275

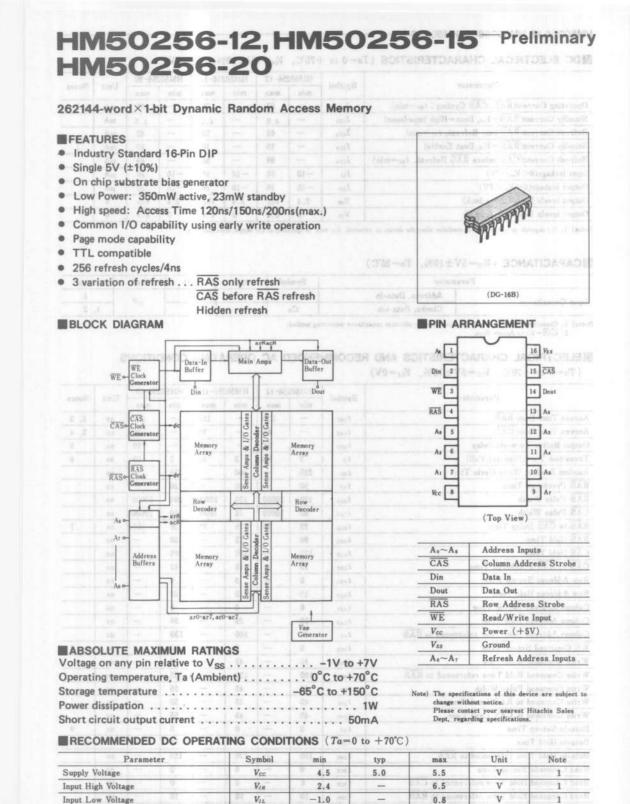


· PAGE NODE READ CYCLE



BIOYD BICHW BOOM BOARD





Note) 1. All voltages referenced to Vas



277

#### HM50256-12, HM50256-15, HM50256-20-

DC ELECTRICAL CHARACTERISTICS	(Ta=0 to +70°C,	$V_{cc} = 5V \pm 10\%$ ,	$V_{SS}=0V$ )	COMP. R. R. L.
-------------------------------	-----------------	--------------------------	---------------	----------------

	0.11	HM50	256-12	HM50	256-15	HM50	256-20	Unit	Notes
Parameter	Symbol	min	max	min	max	mîn	max	Unit	ivotes
Operating Current(RAS, CAS Cycling: t ac-min)	Icci	28.7713	83		70		55	mA	1
Standby Current(RAS = VIR, Dout = High Impedance)	Icca	-	4.5	-	4.5	-	4.5	mA	
Refresh Current(RAS only Refresh, tRC=min)	1 CC3	-	62	-	53	-	42	mA	
Standby Current( $\overline{RAS} = V_{IB}$ , Dout Enable)	Iccs	-	10	-	10		10	mA	1
Refresh Current(CAS before $\overline{RAS}$ Refresh, $t_{BC} = \min$ )	Icco	-	69	-	58		45	mA	
Input leakage(0< Vest<7V)	Iu	-10	10	-10	10	-10	10	μA	and a
Output leakage(0 < V sal < 7V)	ILO	-10	10	-10	10	-10	10	μA	
Output levels High(I <sub>est</sub> =-5mA)	Von	2.4	Vcc	2.4	Vec	2.4	Vcc	V	10.0
Output levels Low(Int-4.2mA)	Vol.	0	0.4	0	0.4	0	0.4	V	U.S. isa

MM X-06100

Notes) 1. Icc depends on output loading condition when the device is selected. Icc max is specified at the output open condition.

· TTL compatible

· Rage mode capability

286 refrects cycles. Ans

#### **CAPACITANCE** ( $V_{cc}=5V\pm10\%$ , $Ta=25^{\circ}C$ )

	Parameter	Symbol	typ	max	Unit	Notes
(BL-06)	Address, Data-in	Cn	A ambad	5	-F	1
Input Capacitance	Clocks, Data-out	Ca	damite v mo	7	pr	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method. 2.  $\overrightarrow{CAS} = V_{iii}$  to disable Dout.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

and set	Cumbel	HM50	256-12	HM50	256-15	HM50	256-20	Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	INOTES
Access Time from RAS	1 RAC	-	120	-	150	-	200	ns	2, 3
Access Time from CAS	t CAC.	-	60		75	-	100	ns	3, 4
Output Buffer Turn-off Delay	torr	10-00	30		40	-	50	ns	5
Transition Time(Rise and Fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t ac	220		260	-	330	-	ns	
RAS Precharge Time	t RP	90	-	100	-	120	1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-	ns	
RAS Pulse Width	I RAS	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	I CAS	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	t RCD	25	60	25	75	30	100	ns	7
RAS Hold Time	t <sub>RSH</sub>	60	-	75	-	100	-	ns	
CAS Hold Time	t <sub>csn</sub>	120	-	150		200		ns	
CAS to RAS Precharge Time	t CRP	10	-	10	1000	10	-	ns	
Row Address Set-up Time	tASR	0	-	0	-	0	-	ns	
Row Address Hold Time	t RAH	15	-	15	-	20	-	ns	
Column Address Set-up Time	1 ASC	0	-	0		0	-	ns	
Column Address Hold Time	t CAH	20	-	25	104.75 <u>0-</u> 08	30	-	ns	
Column Address Hold Time referenced to RAS	t <sub>AR</sub>	80	-	100	-	130	-	ns	
WE Command Set-up Time	twcs	0	-	0	ARTAS	0	1.1.55	ns	8
Write Command Hold Time	- Awen	40	-	45	00 V-03	55	1	ns	apaste.
Write Command Hold Time referenced to RAS	Twee C	100	-	120	Anothe	155	1.76 100	ns	Distant.
Write Command Pulse Width	twp	40	-	45	-	55	1000	ns	and the
Write Command to RAS Lead Time	t RWL	40	-	45	-	55		ns	
Write Command to CAS Lead Time	1 CWL	40	-	45	-	55		ns	
Data-in Set-up Time	tos	0	-	0	-	0	-	ns	9
Data-in Hold Time	t DH	40	(10:40)	45	11823	55	0340	ns	8, 9
Data-in Hold Time referenced to RAS	t DHR	100	(There	120	-	155	-	ns	
Read Command Set-up Time	t acs	0	-	0	-	0	-	ns	
Read Command Hold Time referenced to CAS	t RCH	0	-	0	-	0	-	ns	
Read Command Hold Time referenced to RAS	t RRH	10	-	10	-	10	-	ns	3 10
Refresh Period	LREF	-	4	-	4	-	4	ms	

**CHITACHI** 



#### HM50256-12, HM50256-15, HM50256-20

Parameter	Symbol	HM50	HM50256-12		HM50256-15		256-20	Unit	Notes
rarameter	Symbol	min	max	min	max	min	max	Unit	inotes
Read-Write Cycle Time	t awc	265	-	310	-	390	-	ns	
CAS to WE Delay	t cwp	60	-	75		100	-	ns	8
RAS to WE Delay	t RWD	120	-	150		200		ns	
CAS Precharge Time	tepn	50	-	60	- 2	80		ns	
CAS Setup Time	tesn	10		10	-	10		ns	
CAS Hold Time (CAS before RAS Refresh)	t <sub>CHR</sub>	120	-	150	-	200	-	ns	
RAS Precharge to CAS Hold Time	t RPC	0	A	0	-	0	-	ns	

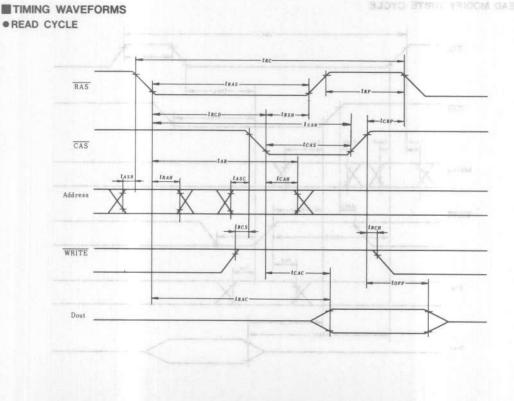
Notes

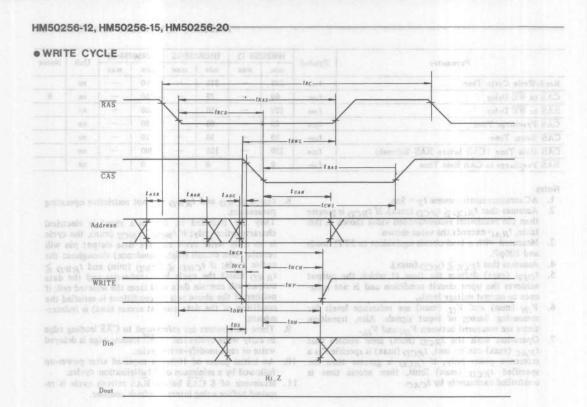
- 1. AC measurements assume  $t_T = 5$ ns.
- 2. Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that  $t_{RCD} \ge t_{RCD}$  (max).
- t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 6.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 7. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .

#### twcs, tcwp and tRwp are not restrictive operating parameters.

They are included in the data sheet is electrical characteristics only; if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge t_{RWD}$  (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

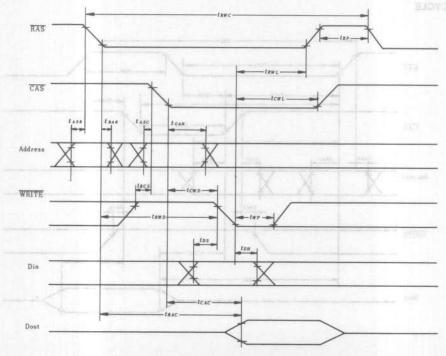
- There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- An initial pause of 100µs is required after power-up followed by a minimum of 8 initialization cycles.
- 11. Minimum of 8 CAS before RAS refresh cycle is required before using internal refresh counter.





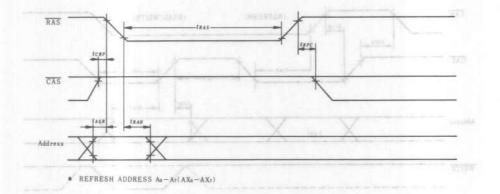




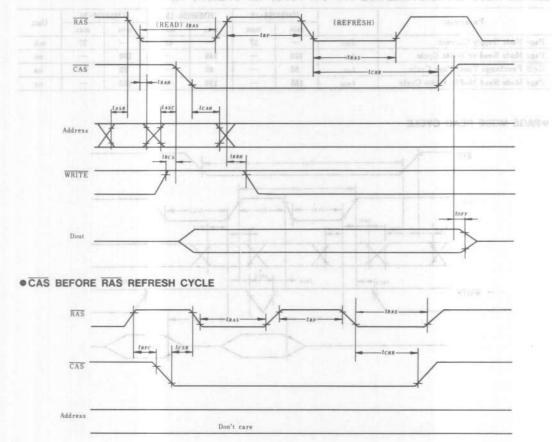


#### • RAS ONLY REFRESH CYCLE

· COUNTER TEST



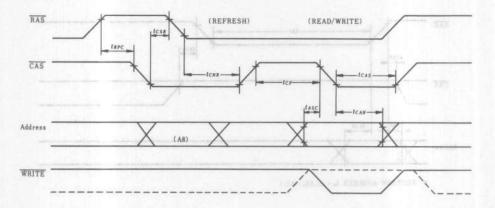




#### HM50256-12, HM50256-15, HM50256-20-

#### ● COUNTER TEST

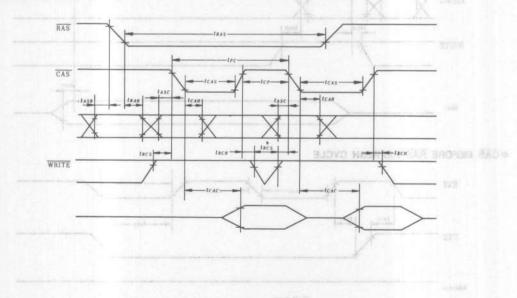
WAS CHUY REPRESS CYCL



■PAGE MODE CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±10%, Vss=0V)

Guild	HM50256-12			256-15	HM50	Unit	
Symbol	min	max	min	max	min	max	Unit
Icci	-	57		48	1 -	37	mA
1 PC	120	-	145	-	190	-	ns
tcp	50	-	60	1-	80	#3	ns
t PCM	165	-	195		250	-	ns
	t <sub>PC</sub> t <sub>CP</sub>	Symbol         min           Iccr         -           trc         120           tcp         50	Symbol         min         max           Iccr         -         57           trc         120         -           tcp         50         -	Symbol         min         max         min           Icer         -         57         -           trc         120         -         145           tcp         50         -         60	Symbol         min         max         min         max           Iccr         -         57         -         48           t <sub>PC</sub> 120         -         145         -           t <sub>CP</sub> 50         -         60         -	Symbol         min         max         min         max         min           I_{ccr}         -         57         -         48         -           t_{PC}         120         -         145         -         190           t_{CP}         50         -         60         -         80	Symbol         min         max         min         max         min         max           I_{ccr}         -         57         -         48         -         37           t_{PC}         120         -         145         -         190         -           t_{CP}         50         -         60         -         80         -

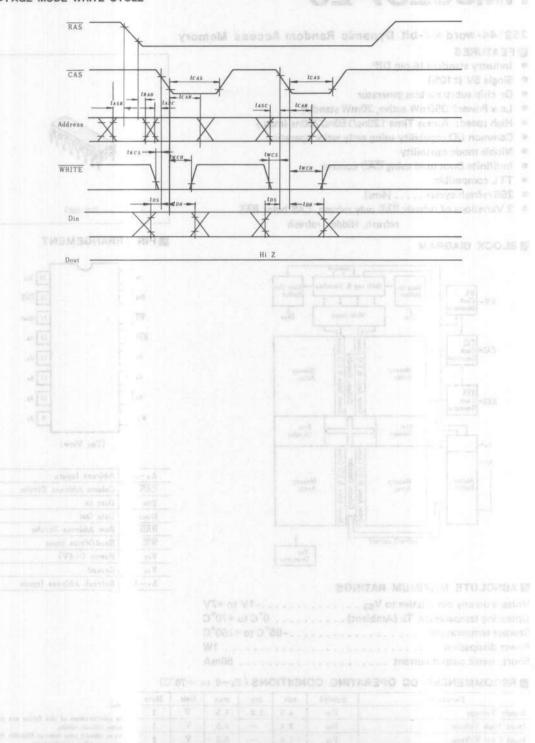
● PAGE MODE READ CYCLE



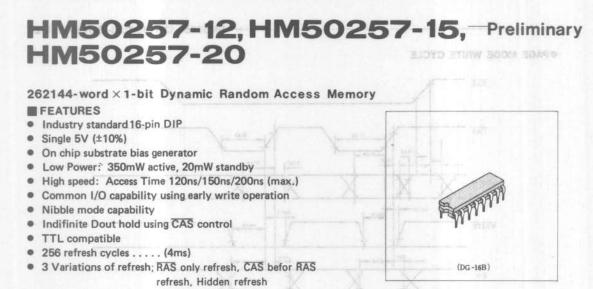
#### • PAGE MODE WRITE CYCLE

Vignmers

10513



SESOENH,



BLOCK DIAGRAM

PIN ARRANGEMENT

As 1

Din 2

WE 3

RAS 4

Ao 5

AI

Vec 8

Ao~Aa

CAS

Din

Dout

WE

Vcc

Vss

Ao~A+

Az 6

16 Vss

15 CAS

14 Dout

13 As

12 A:

11 A.

10 As

9 A1

(Top View)

Address Inputs

Data In

Ground

Note)

Data Out

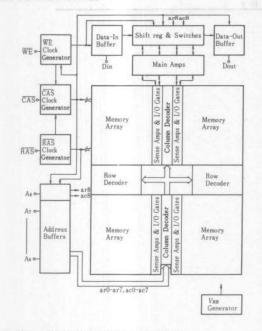
Column Address Strobe

Row Address Strobe

Refresh Address Inputs

Read/Write Input

Power (+5V)



#### **ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to	0 V <sub>SS</sub> 1V to +7V
Operating temperature, Ta (A	Ambient) $0^{\circ}$ C to $+70^{\circ}$ C
Storage temperature	65°C to +150°C
	1W
Short circuit output current	

#### ■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	mîn	typ	max	Unit	Note
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Input High Voltage	Vtu	2.4	-	6.5	V	1
Input Low Voltage	VIL	-1.0		0.8	V	1

**OHITACHI** 

The specifications of this device are subject to change without notice. Please contact your nearest Hitachin Sales Dept, regarding specifications.

Note 1) All voltages referenced to Vas.

the set of the set	G 1.1	HM50	257-12	HM50	257-15	HM50	257-20	Unit	Notes
Parameter	Symbol	mîn	max	mîn	max	min	max	Unit	Hotes
Operating Current (RAS, CAS Cycling: tRc=min)	Icci	0.0.7	83	-	70	-	55	mA	1
Stand by Current ( $\overline{RAS} = V_{IH}$ , Dout = High Impedance)	Icci	1000	4.5	-	4.5	+	4.5	mA	L EAR
Refresh Current (RAS only Refresh, t <sub>RC</sub> =min) -	Iccs	· · · · ·	62	-	53	-	42	mA	4 2/10
Standby Current (RAS = VIH, Dout Enable)	Iccs	9 H 2	10	-	10	-	10	mA	1
Refresh Current ( $\overline{CAS}$ before $\overline{RAS}$ Refresh, $t_{RC}$ =min)	Iccs	1xst	69	(1000)	58	100000	45	mA	6.170
Input leakage (0 <v<sub>mit&lt;7V)</v<sub>	ILI	-10	10	-10	10	-10	10	μA	1.273
Output leakage (0 < V <sub>mt</sub> < 7V)	ILO	-10	10	-10	10	-10	10	μA	
Output levels High (I <sub>sut</sub> =-5mA)	Von	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	4510k
Output levels Low (Int = 4.2mA)	Vol		0.4	0	0.4	0	0.4	V	2 6

#### **DC ELECTRICAL CHARACTERISTICS** (*Ta*=0 to +70°C, *Vcc*=5V±10%, *Vss*=0V)

Notes) 1. Icc depends on output loading condition when the device is selected Icc max, is specified at the output open condition. **CAPACITANCE** ( $V_{cc}$ =5V±10%, Ta=25°C)

S many lass (card) o	Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-In	Cri	fold <u>e</u> the	5	ins) (din	3801 -2
	Clocks, Data-Out	C11	pers pourt	7	pr	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method. 2. CAS-V<sub>III</sub> to disable Dout.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, V_{cc}=5\text{V}\pm10\%, V_{ss}=0\text{V})$ 

ter a minime of 5 telligibles as the	Symbol	HM50	257-12	HM50	257-15	HM50	257-20	Unit	Notes
Parameter	Symbol	min	max	min	max	min	max	Unit	Notes
Access Time from RAS	tRAC	-	120	-	150	-	200	ns	2,3
Access Time from CAS	teac	-	60	-	75	-	100	ns	3,4
Output Buffer Turn-off Delay	torr	-	30	-	40	NAO	50	ns	5
Transition Time (Rise and Fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	tRC	220	-	260	-	330	-	ns	
RAS Precharge Time	tap	90	-	100	-	120		ns	
RAS Pulse Width	tRAS	120	10000	150	10000	200	10000	ns	
RAS Pulse Width	ICAS	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	IRCD	25	60	25	75	30	100	ns	7
RAS Hold Time	tRSH	60	-	75	-	100	-	ns	
CAS Hold Time	tesu	120	-	150	-	200	-	ns	
CAS to RAS Precharge Time	terp	10	-	10	-	10	-	ns	
Row Address Set-up Time	LASE	0	-	0	-	0	-	ns	
Row Address Hold Time	t <sub>RAH</sub>	15	- 111-	15	-	20		ns	
Column Address Set-up Time	LASC	0	-	0	-	0		ns	
Column Address Hold Time	LCAH	20		25		30		ns	
Column Address Hold Time referenced to RAS	LAR	80	X -	100	-	130	-	ns	
WE Command Set-up Time	lwcs	0	-	0	-	0	-	ns	8
Write Command Hold Time	twcn	40	-	45		55	-	ns	
Write Command Hold Time referenced to RAS	twca	100	-	120	-	155	-	ns	
Write Command Pulse Width	twp	40	-	45	-	55		ns	
Write Command to RAS Lead Time	1 RWL	40	\	45	-	55		ns	
Write Command to CAS Lead Time	town	40	-	45	-	55	-	ns	
Data-in Set-up Time	tos	0	-	0	-	0	-	ns	9
Data-in Hold Time	ton	40	-	45	-	55	-	ns	8,9
Data-in Hold Time referenced to RAS	town	100	-	120	-	155		ns	
Read Command Set-up Time	tacs	0	-	0	-	0	-	ns	
Read Command Hold Time referenced to CAS	tRCH	0	-	0	-	0	-	ns	
Read Command Hold Time referenced to RAS	tRRH	10	-	10	-	10	-	ns	1
Refresh Period	LREF	-	4		4	-	4	ns	

(to be continued )



#### HM50257-12, HM50257-15, HM50257-20

B	1.4.6	1.13	14	C 11	HM50257-12		HM50257-15		HM50257-20		11.11	Notes
Parameter				Symbol	min	max	min	max	min	max	Unit	Notes
Read-Write Cycle Time	8-1L	elter	102	tRWC	265	-	310	-	390	-	ns	
CAS to WE Delay	12	-	- 20	tewp	60		75	niis —	100	123-0	ns	8
RAS to WE Delay	1		8.4	tRWD	120	(	150	1- (-1)	200	10/200	ns	bhaid
CAS Precharge Time	1.1		- 28	tCPN	50	- 1	60	$(dz \rightarrow b)$	80	222-2	ns	Ref de R
CAS Setup Time	18	-	10.	tesk	10	-	10	en Hans	10	611-30	ns	Shoute
CAS Hold Time (CAS before RAS	S Ref	resh)	-65-	tenn	120	(0	150	19 <u>44</u>	200	88.24	ns	and a start
RAS Precharge-to CAS Hold Tin	ne	03~	1.01	tape	0	-	0	-	0	1.201	ns	C Inquid

Notes

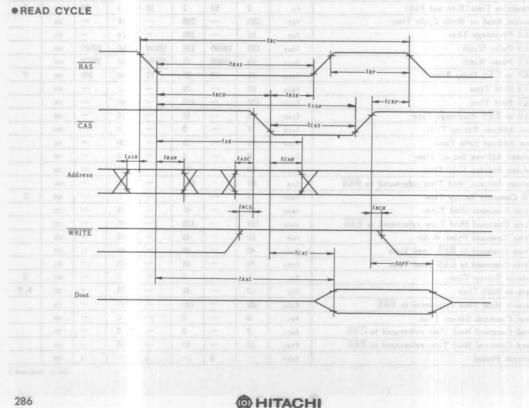
1. AC measurements assume  $t_T = 5$ ns.

- 2. Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 4. Assumes that  $t_{RCD} \ge t_{RCD}$  (max).
- t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 6.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 7. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .

 t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters.

They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge t_{RWD}$  (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

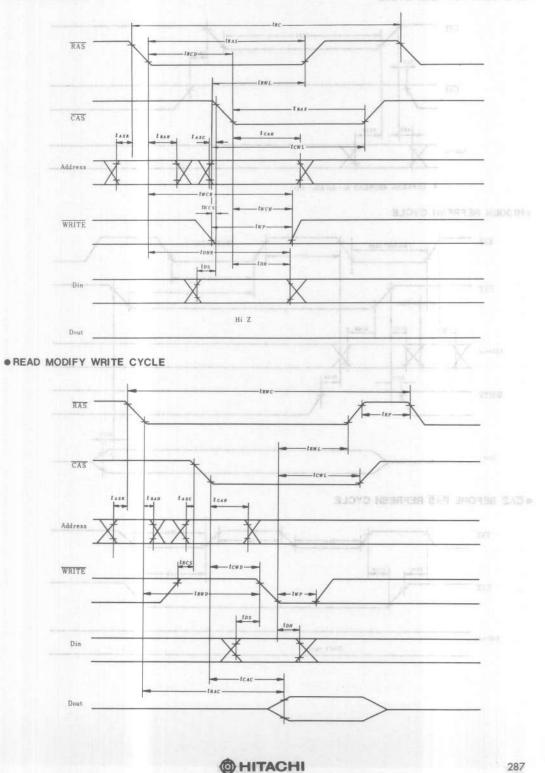
- There parameters are referenced to CAS leading edge in early write cycles and to WE leading edge is delayed write or read-modify-write cycles.
- An initial pause of 100µs is required after power-up followed by a minimum of 8 initialization cycles.
- 11. Minimum of 8 CAS before RAS refresh cycle is required before using internal refresh counter.

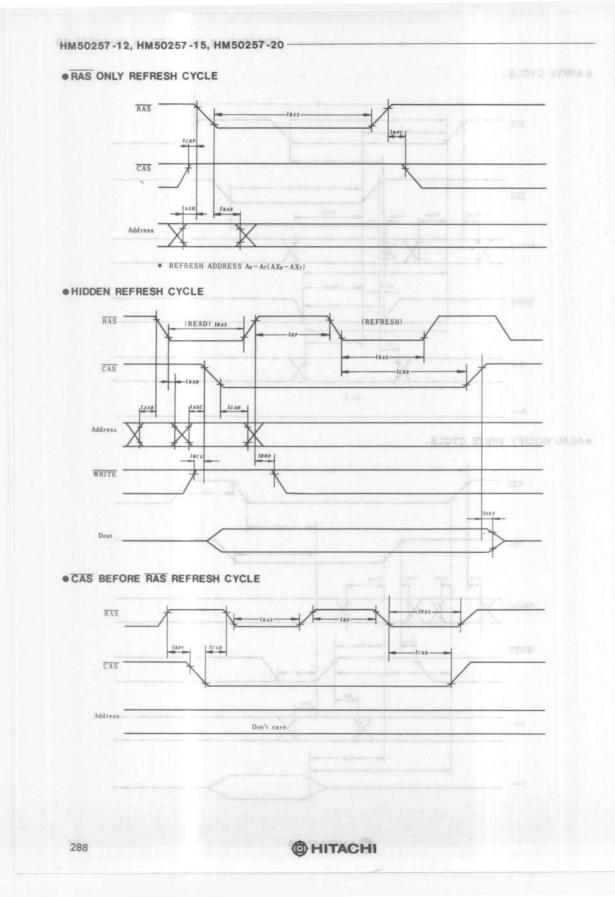


#### TIMING WAVEFORMS

**WRITE CYCLE** 

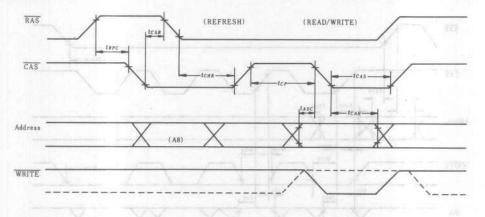
EXPO MASS FOR YOR 2/9





• COUNTER TEST

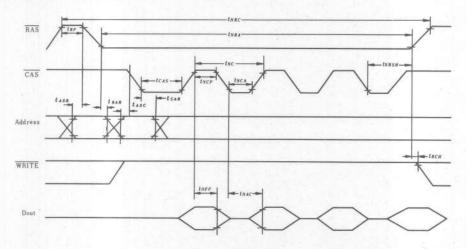
A HIRELE MOUT WRITE CYCLE



### **NIBBLE MODE CHARACTERISTICS** (*Ta*=0 to +70°C, *V*<sub>cc</sub>=5V±10%, *V*<sub>ss</sub>=0V)

Parameter	S-1-1	HM50257-12		HM50257-15		HM50257-20		Unit
Farameter	Symbol	min	max	min	max	min	max	Unit
Nibble Mode Supply Current	Iccs	-	57	-	48	-	37	mA
Nibble Mode Access Time	t NAC	-	20		25	-	35	ns
Nibble Mode RAS Cycle Time	t NRC	390	-	460	-	590	-	ns
Nibble Mode RAS Pulse Width	t <sub>NRA</sub>	290	-	350	-	460	-	ns
Nibble Mode Cycle Time	tNC	50	-	60	-	80	-	ns
Nibble Mode CAS Precharge Time	INCP	20	-	25	-	35	-	ns
Nibble Mode CAS Pulse Width	t NCA	20	-	25	-	35	-	ns
Nibble Mode RAS Hold Time	tNRSH.	40	-	45	-	55	-	ns

#### . NIBBLE MODE READ CYCLE

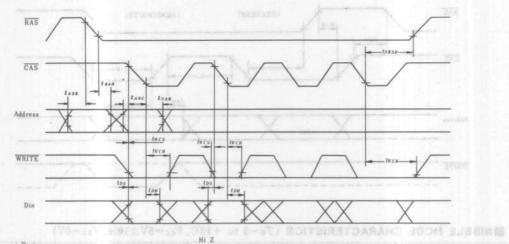


**HITACHI** 

#### HM50257-12, HM50257-15, HM50257-20

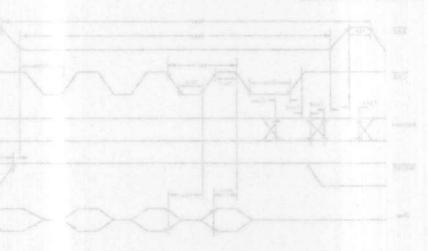






trout		Dout				11-12-10	COMP.	- Continue Da	
							Paradaster		
							Mildle Mode RAS (Sec)+ Time		
							tilble Made HAE Mold Case		

BUDYD GAIN BOOM BUBBING



290

### HNG1364P, HNG1364F

- 6 Stocke vSV Rower Scoply a Those votre Data Octuat for OR-data



V		
	-20.10 +85	

VI			

















### HN61364P, HN61364FP

#### 8192-word x 8-bit Mask Programmable Read Only Memory

### The HN61364P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

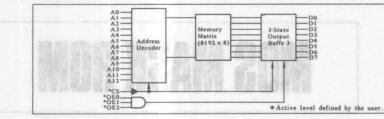
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS,  $OE_0 \sim OE_2$  inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

#### **FEATURES**

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5µW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

#### BLOCK DIAGRAM



#### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	
Supply Voltage*	Vcc	-0.3 to +7.0	v	
Input Voltage*	Vin	-0.3 to +7.0	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-55 to +125	°C	
Bias Storage Temperature	Tbias	-20 to +85	°C	

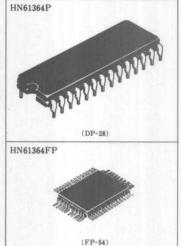
\* with respect to  $V_{SS}$ 

#### RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage *	Vcc	4.5	5.0	5.5	V
Input Voltage*	VIL	-0.3	-	0.8	V
	VIH	2.2	-	Vcc	V
Operating Temperature	Topr	-20	-	75	°C

O HITACHI

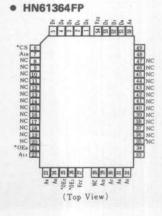
\* with respect to Vss



#### PIN ARRANGEMENT

HN61364P

NCI	28 Vcc
A12 2	27 OE
A7 3	26 OE2
A6 4	25 A8
Ass	24 A9
A4 6	23 A <sub>11</sub>
A3 7	22 OE.
A2 8	21 A10
A1 9	20 CS*
A <sub>0</sub> [10	19 D <sub>7</sub>
D <sub>0</sub> 11	18 D <sub>6</sub>
D112	17 D <sub>5</sub>
D <sub>2</sub> 13	16 D4
V <sub>SS</sub> 14	15 D3
(Top	View)



Item		Symbol	Test Condition	min	typ	max	Unit
Input High-level	Voltage	VIH		2.2	-	Vcc	V
Input Low-level	Voltage	VIL	political president bake "sugerumento"	-0.3	-	0.8	V
Output High-leve	el Voltage	VOH	I <sub>OH</sub> =-205µА	2.4	-	ten Test t	v
Output Low-leve	l Voltage	VOL	<i>I<sub>OL</sub></i> =3.2mA	-	C. Gen	0.4	V
Input Leakage Current		Iin	Vin=0 to 5.5V		- YA	2.5	μA
Output High-level Leakage Current		ILOH	Vout=2.4V, CS=0.8V, CS=2.2V		0.00 <u>0</u> 0.5	10	μA
Output Low-leve	l Leakage Current	ILOL	Vout=0.4V, CS=0.8V, CS=2.2V	SO_910		10	μA
Supply Current	Active	Icc *	V <sub>CC</sub> =5.5V, I <sub>out</sub> =0mA	die 75. p.r.	10	25	mA
Supply Cullent Standby	Standby	I <sub>SB</sub>	$V_{CC}$ =5.5V, $\overline{CS} \ge V_{CC}$ -0.2V, $CS \le 0.2V$	10000	1	30	μA
Input Capacitance Output Capacitance		Cin	$V_{in}=0V, f=1MHz, T_a=25^{\circ}C$	-	-	10	pF
		Cout	, IN-01, J-IMIL, 1 a-25 C	-	-	15	pF

### ■ ELECTRICAL CHARAGTERISTICS (V<sub>CC</sub> = 5V±10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = -20 to +75°C

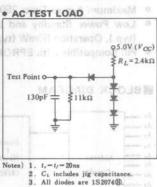
\* steady state current

#### RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

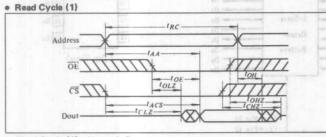
 $(V_{cc}=5V\pm10\%, V_{ss}=0V, Ta=-20 \text{ to } +75^{\circ}\text{C}, t_r=t_f=20 \text{ ns})$ 

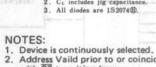
Item	Symbol	min	max	Unit
Read Cycle Time	t <sub>RC</sub>	250	-	ns
Address Access Time	t <sub>AA</sub>	-	250	ns
Chip Select Access Time	tACS	-	250	ns
Chip Selection to Output in Low Z	t <sub>CLZ</sub>	10	noitiinag	ns
Output Enable to Output Valid	t <sub>OE</sub>	-	100	ns
Output Enable to Output in Low Z	tolz	10	-	ns
Chip Deselection to Output in High Z	t <sub>CHZ</sub>	0	100	ns
Chip Disable to Output in High Z	toHZ	0	1.00	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	ns

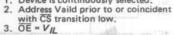




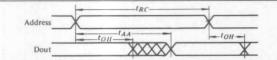
TIMING WAVEFORM



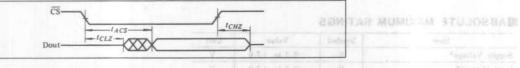




e Read Cycle (2) Notes 1, 3



• Read Cycle (3) Notes 2, 3





Storages Temperstates

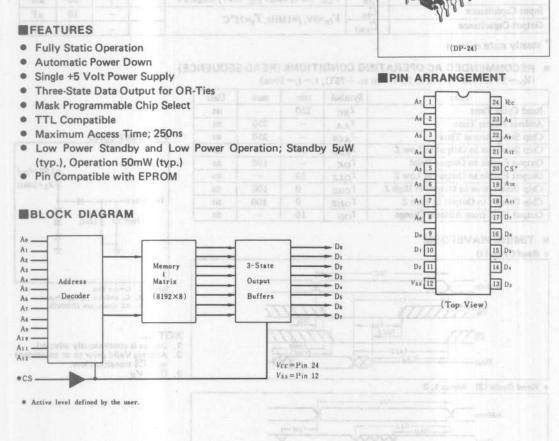
# HN61365P

#### 8192-word×8-bit Mask Programmable Read Only Memory

The HN61365P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS input and the memory content are defined by the user. The chip select input deselects the output and puts the chip in a power-down mode.



#### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to $+7.0$	V
Input Voltage*	Vin	-0.3 to +7.0	V
Operating Temperature	Tope	-20 to +75	°C
Storage Temperature	Teta	-55 to +125	*C
Storage Temperature (under bias)	Thins	-20 to +85	°C

\* with respect to Vss

**OHITACHI** 

#### RECOMMENDED DC OPERATING CONDITIONS

Symbol	no R min dan	typ	max	Unit
Vcc	4.5	5.0	5.5	V
VIL	-0.3		0.8	V
VIN	2.2	CELEBORYS DEGI	Vcc	v
Tepr	-20	thu say odo	75	°C
	Vcc VIL VIN	$     \frac{V_{cc}}{V_{IL}} = -0.3 \\     \hline     V_{IN} = 2.2   $	$     \frac{V_{cc}}{V_{IL}} = \frac{4.5}{-0.3} = \frac{5.0}{-0.3}     \frac{V_{IL}}{V_{IN}} = \frac{2.2}{-0.3} = \frac{1}{-0.3}     \frac{1}{-0.3} = \frac{1}{-0.3} = \frac{1}{-0.3}     \frac{1}{-0.3} = \frac{1}{-0.3} $	$     \begin{array}{c cccccccccccccccccccccccccccccccc$

\* With respect to Van

#### ELECTRICAL CHARACTERISTICS (Vcc=5V ±10%, Vss=0V, Ta=-20 to +75°C)

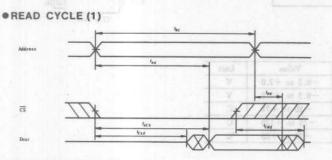
Item	Symbol	Test Condit	tions	min	typ	max	Unit
Input Voltage	VIH			2.2	-	Vcc	V
	VIL			-0.3	-	0.8	v
Output Voltage	Von	$I_{0H} = -205 \mu A$		2.4	Noite as	Sheid O	v
	VOL	101=3.2mA		- 95	NO. TRODE	0.4	V
Input Leakage Current	ILI	V <sub>IN</sub> =0~5.5V		10.1077	esute un	2.5	μA
Output Leakage Current	ILOH	CS-0.8V, CS-2.2V	Vest=2.4V	all states	0.00	10	μA
Output Leakage Current	ILOL	CS-0.0V, CS-2.2V	$V_{sut}=0.4V$	-		10	μA
Active Supply Current	Icc*	Vcc=5.5V, Ipour=0mA		ard)77	10	25	mA
Stand by Supply Current	Isb	$\overline{\text{CS}} \ge V_{cc} - 0.2 \text{V}, \text{ CS} \le 0$	$0.2V, V_{cc} = 5.5V$	Non Star	1	30	μA
Input Capacitance	Cin	− V <sub>ia</sub> =0V, f=1MHz, Ta=25°C		11500	- 17	10	pF
Output Capacitance	Coul			-	-	15	pF

\* Steady state current

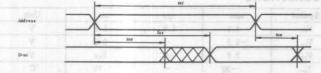
#### RECOMMENDED AC OPERATING CHARACTERISTICS

•READ SEQUENCE (Vcc=5V±10%, Vss=0V, Ta=-20 to +75°C, tr=tr=20ns)

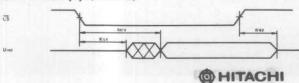
Item	Symbol	min	max	Unit
Read Cycle Time	trc	250		ns
Address Access Time	LAA	-	250	ns
Chip Select Access Time	tACS	—	250	ns
Chip Selection to Output in Low Z	telz	10	-	ns
Chip deselection to Output in High Z	t <sub>CHZ</sub>	0	100	ns
Output Hold from Address Change	ton	10	-	ns



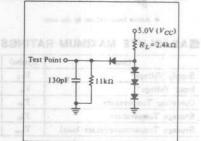
#### • READ CYCLE (2) (Notes 1)



• READ CYCLE (3) (Notes 2)







# Notes) 1. t,-t,-20ns. 2. CL includes jig capacitance. 3. All diodes are 1S2074⊕.

Summer Voltage



Notes)

1. Device is continuously selected 2. Address Valid prior to or coincident with  $\overline{\rm CS}$ 

transition low.

# HN61366P

INTERNET DC OPERATING CONDITIONS

#### 8192-word×8-bit Mask Programmable Read Only Memory

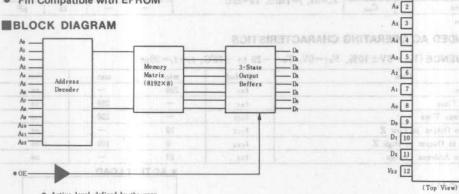
The HN61366P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has

compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the OE input and the memory content are defined by the user.

#### FEATURES

- Fully Static Operation
- Single +5V power supply
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Operation; 50mW (typ.)
- Pin Compatible with EPROM



\* Active level defined by the user.

#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit		
Supply Voltage*	Vcc	-0.3 to +7.0	V		
Input Voltage*	Via	-0.3 to $+7.0$	V		
Operating Temperature	T.pr	-20 to +75	°C		. 47
Storage Temperature	Teta	-55 to +125	°C	2	
Storage Temperature(under bias)	Thies	-20 to $+85$	°C	Nor many Street	

\* With respect to Vas

#### RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	Vcc	4.5	5.0	5.5	V
	VIL	-0.3		0.8	V
Input Voltage*	VIII	2.2	CXX <del>X</del>	Vcc	V
Operating Temprature	Tape	-20	-	75	°C

\* With respect to Vss

PREAD CYCLE (II) Disker 2)

WREAD CYCLE (2) (Notes 1)



(DP-24)

### IPIN ARRANGEMENT

A1 1

14 D4 13 D2

24 Vec

23 As 22 As

19 A10

17 D7

16 De

15 Ds

21 A12

20 OE

18 Au

View) VO O

max

Vcc

0.8

Unit

V

V

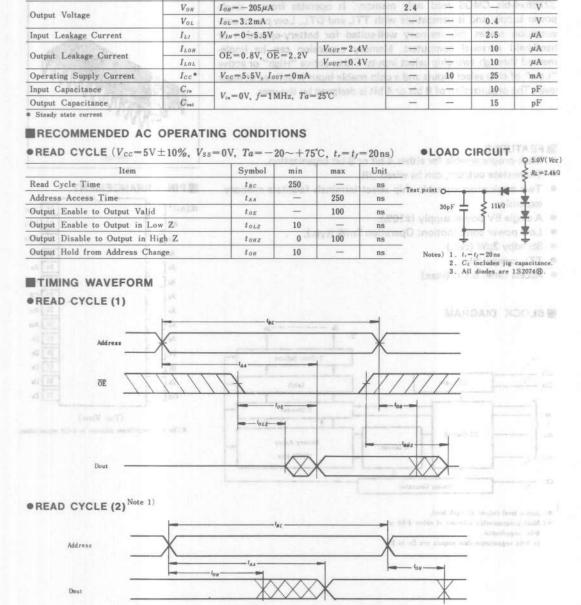
min

2.2

-0.3

typ

\_



**ELECTRICAL CHARACTERISTICS** (Vcc-5V±10%, Vss-0V, Ta=-20 to +75°C)

Test Conditions

Symbol

VIH

ViL

Note) 1.  $\overline{\text{OE}} = V_{\text{FL}}$ 

Item

Input Voltage

### HN43128P

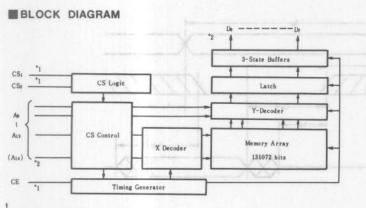
16384 × 8-bit or 32768 × 4-bit CMOS Mask Programmable Read Only Memory

The Hitachi HN43128P is a mask programmable, 16384x8-bit or 32786x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL and DTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through two chip select inputs. Either active "High" or active "Low" of chip select inputs and a chip enable input is defined at mask level. The organization of 8 bit or 4 bit is designed by the user.

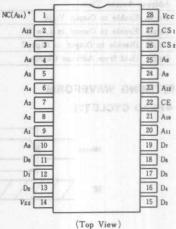


FEATURES

- Mask-programmable for either 4-bit or 8-bit organization.
- Three-state outputs, can be wired-OR.
- Two mask programmable chip select terminals facilitate memory expansion.
- A single 5V power supply (±10%).
- Low power consumption: Operation 3mW (typ.),
- Standby 3µW (typ.)
- TTL compatible
- Access time: 6.5µs (max)



PIN ARRANGEMENT



\*The most significant address in 4-bit organization.

#1 Active level defined at mask level.

#2 Mask programmable selection of either 4-bit or 8-bit organization.

In 4-bit organization, data outputs are Da to Da.

298

#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit	10384-word×8-bit Mask F
Supply Voltage*	Vcc	-0.3~+7.0	V	TO E W 53 SECTOREME, edg
Input Voltage*	Via	-0.3~+7.0		and all and for the basis
Operating Temperature Range	T.p.	-20~+75	.C.	the device operation from a singl
Storage Temperature	Teta	-55~+125	°C	widt TTL, and requires no doold
Bias Storage Temperatore	Thins	-20~+85	. °C	retion. The antive toyal of the C

Note : \* Referenced to Vzz.

output and publities the thick power down mode.

#### ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Vss=0V, Ta=-20~+75°C)

I	em	Symbol	Test	Condition	min	typ	max	Unit
Input "High" Level	Voltage	V <sub>IH</sub>			2.4	homen	Vcc	V
Input "Low" Level	Voltage	VIL		8 5 M 1	0	NAME IS	0.8	V
Output "High" Leve	el Voltage	V <sub>OH</sub>	$I_{OH} = -100 \mu \text{A}$		2.4	12 HEREN	tiov-2+	V
Output "Low" Leve	l Voltage	Vol	IoL = 1.6 m A		20 101	uota Vatou	0.4	V
Input Leakage Curi	ent	Iin	$V_{in} = 0 \sim 5.5 V$		o Salact	40 T	2.5	μA
Output "High" Leve	l Leakage Current	ILON	CE-0.8V	V = 2.4 V	-		5	μA
Output "Low" Leve	l Leakage Current	ILOL	$\overline{CE} = 2.4V$	V = 0.4 V	and ac		5	μA
	In stand-by	Isb	$ \overline{CS} \ge V_{cc} - 0.2V \\ CS \ge V_{ss} + 0.2V $	U - F FV	and war at	1	30	μA
Supply Current	In operation	Icc *	$t_{RC} = 7.5 \mu s$	$-V_{\rm cc}=5.5V$	02405	0.6	1.5	mA
Input Capacitance		<i>C</i> <sub>i</sub> ,	$V_{a} = 0V_{b}f = 1 \text{ MHz} T_{a} = 25 \text{ C}$		Hanton .		10	pF
		Cost			-	-	12.5	pF

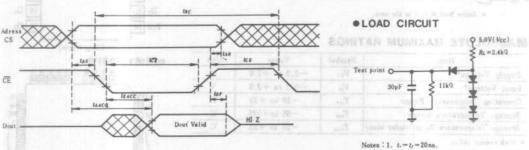
\* Steady state current

#### AC OPERATING CHARACTERISTICS

#### HAHEMARD NOOLIS []]

READ SEQUENCE	$(V_{cc} = 5V \pm 10\%)$	$V_{SS}=0V,$	Ta = -20 to	$+75^{\circ}C, t_r = t_f = 20 ns$	)
---------------	--------------------------	--------------	-------------	-----------------------------------	---

Item		Symbol	min	max	Unit
Read Cycle Time	3.0	t <sub>RC</sub>	7.5	1000	μs
Address Access Time		LAACC		6.5	μs
Chip Enable Access Time	300	LEACC	-	6.0	μs
Data Hold Time from Address	1997	t <sub>DF</sub>	0.05	0.5	μs
Address Set-up Time	1.1.10	LAS	0.5	+	μs
Address Hold Time	2.19	LAH	0	-	μs
Chip Enable ON Time	As D	$t_{\overline{c}\overline{e}}$	6.0	-	μs
Chip Enable OFF Time	1 00	tcz	1.0	- +	μs



2. Ct includes jig capacitance. 3. All diodes are 1S2074 (B.

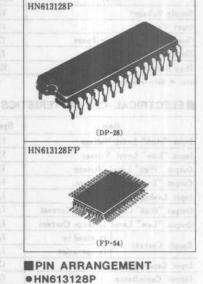
Daix			iner]
			- Service T ariters



### HN613128P, HN613128FP

#### 16384-word×8-bit Mask Programmable Read Only Memory

The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE<sub>0</sub>, OE<sub>1</sub> input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.



28 Vcc

27 OE1 \*

26 A13

25 As

24 A9

23 A11

21 A10

20 CS \*

19 D7

18 De

17 Ds

16 D4

15 D3

22 OE0 \*

Pin	Com	patible	with	EPROM
-----	-----	---------	------	-------



**TTL** Compatible

FEATURES

.

.

. .

. .

0

0

.

**Fully Static Operation** 

Automatic Power Down

Single +5-Volt Power Supply

Maximum Access Time; 250ns

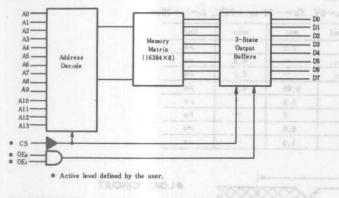
Standby:

**Operation:** 

Three-State Data Output for OR-Ties

Mask Programmable Chip Select, Output Enable

Low Power Standby and Low Power Operation;



5µW (typ.)

50mW (typ.)



Item	Symbol	Value	Unit
Supply Voltage*	Vcc	-0.3 to $+7.0$	V
Input Voltage*	Via	-0.3 to $+7.0$	v
Operating Temperature Range	Tepr	-20 to $+75$	°C
Storage Temperature Range	Tele	-55 to +125	°C
Storage Temperature Range (under bias)	Thies	-20 to +85	°C

\* With respect to V ##.

#### RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage *	Vcc	4.5	5.0	5.5	V
	VIL	-0.3	-	0.8	V
Input Voltage*	Vin	2.2	-	Vcc	V
Operating Temperature	Tape	-20	-	75	°C

\* With respect to Vas.





NC

A7

As 4

As 5

A2

Ao 10

Do 11

D1 12

D2 13

Vss 14

A4 6

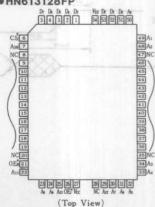
7 As

8

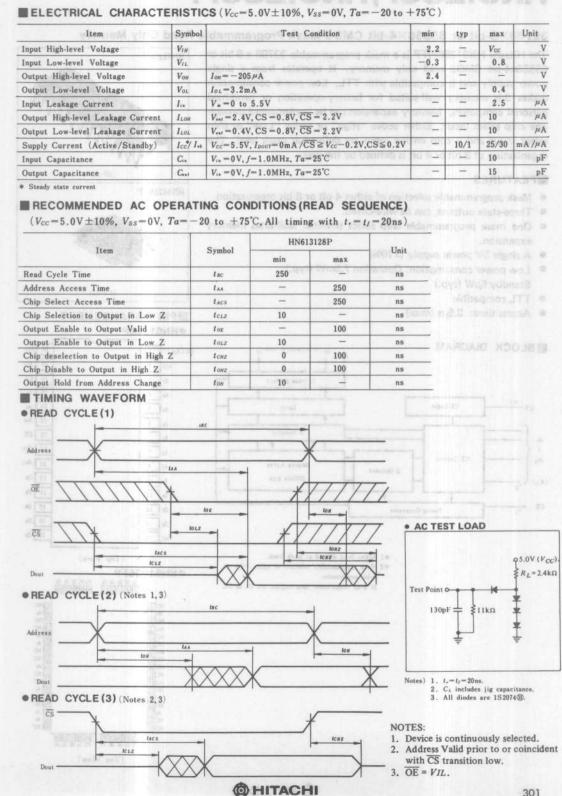
9 Aı

2 A12

3



HN613128FP



301

### HN61256P, HN61256FP

#### 32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

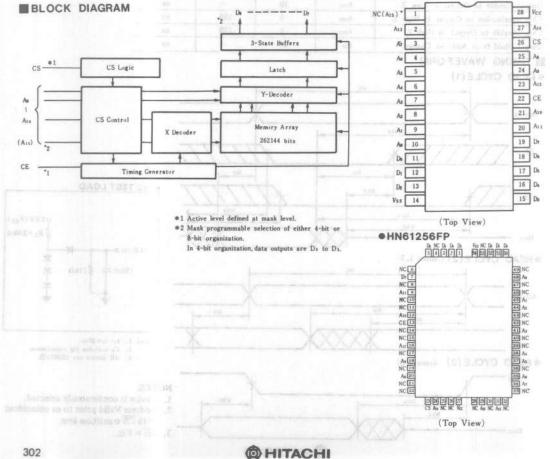
The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

#### FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%)
- Low power consumption: Operation 7.5mW (typ.), . Standby 5µW (typ.)
- TTL compatible
- Access time: 3.5µs (max)

HN61256P (DP-28) HN61256FP (FP-54)

#### PIN ARRANGEMENT HN61256P



#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	Vcc	-0.3~+7.0	V
Input Voltage*	Via	-0.3~+7.0	V
Operating Temperature Range	Tope	$0 \sim +75$	°C
Storage Temperature Range	Tere	$-55 \sim +125$	°C
Bias Storage Temperature Range	Thiar	-20~+85	°C

The HH6122566/IFF is a mark through by designed for use in but org mission To facilitate use, the device operate compatibility with TTL, and the

Note : \* Referenced to Vss.

#### active level of the US and UE Induit, and the memodefined by the user. The Chile Select local develocation

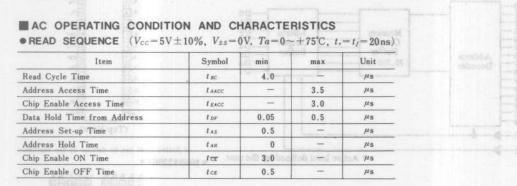
#### **ELECTRICAL CHARACTERISTICS** $(V_{cc}=5V\pm10\%, V_{ss}=0V, Ta=0\sim+75^{\circ}C)$

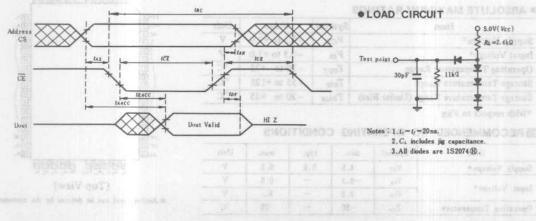
it purs the chip in a power-down mode.

It	em	Symbol	Test C	Condition	min	typ	max	Unit
Input "High" Level	Voltage	VIH			2.4		Vcc	V
Input "Low" Level Voltage		VIL			0	-	0.8	V
Output "High" Level Voltage		Von	$I_{OH} = -100\mu\mathrm{A}$		2.4	-		V
Output "Low" Level Voltage		VoL	$I_{OL} = 1.6 \mathrm{mA}$			ado zera	0.4	V
Input Leakage Curr	ent	La	$V_{cs} = 0 - 5.5 V$		a toallee e	an Tas	2.5	μA
Output "High" Leve	el Leakage Current	ILOH	CE = 0.8V	$V_{out} = 2.4 \text{ V}$	-	- 3	5	μA
Output "Low" Leve	l Leakage Current	ILOL	CE = 2.4V	$V_{est} = 0.4 \text{ V}$	RUPIGY:	1911/12/11	5	μA
Supply Current	In stand-by	IsB	$ \begin{array}{c} \overline{\text{CS}} \geq V_{cc} = 0.2 \text{ V}, \\ \overline{\text{CS}} \geq V_{ss} + 0.2 \text{ V}. \end{array} $	$V_{cc} = 5.5 V$	A MOT DA	5 VO1	30	μA
Supply Current	In operation	Icc *	$t_{RC} = 4.0 \mu s$	Vcc-3.5V	CE notress	1.5	3.0	mA
Input Capacitance	The second	<i>C</i> .,	$V_{ix} = 0$ V, $f = 1$ MHz, $Ta = 25$ °C		(HCH)	역전 (특징성)	10	pF
Output Capacitance	1	Cont			-	-	12.5	pF

acost romm.

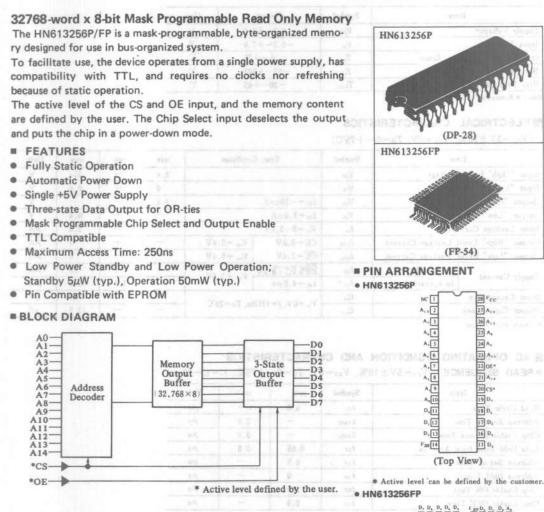
\* Steady state current





**OHITACHI** 

### HN613256P, HN613256FP



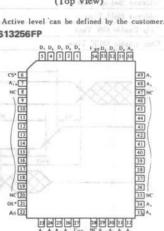
#### ABSOLUTE MAXIMUM RATINGS

-		Unit
VCC	-0.3 to +7.0	V
Vin	-0.3 to +7.0	V
Topr	-20 to +75	°C
Tstg	-55 to +125	°C
Thias	-20 to +85	°C
	Vin Topr Tstg	Vin         -0.3 to +7.0           Topr         -20 to +75           Tstg         -55 to +125

\*With respect to VSS

#### RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage *	Vcc	4.5	5.0	5.5	V
	VIL	-0.3	-	0.8	V
Input Voltage*	Vin	2.2	-	Vcc	V
Operating Temperature	Tepr	-20	-	75	°C



(Top View)

\* Active level can be defined by the customer.

\* With respect to Vzs.



#### Preliminary

	ELECTRICAL	CHARACTERISTICS	0	CC=	5.0V±10%,	VSS	= 01	$T_{a}$	= -20 ~	~+75 °	C)	
--	------------	-----------------	---	-----	-----------	-----	------	---------	---------	--------	----	--

It	em	Symbol	Test Co	ondition	min	typ	max	Unit
X		VIH	To facilitate use the	anatara batintato o	2.2		Vcc	V
Input Voltage		VIL	iso validitaomoo and vidous rewoo slonia		-0.3	ottes	0,8	V
Outeret Valterer		VOH	$I_{OH} = -205 \ \mu \text{A}$		2.4	1.5	10.7%	V
Output Voltage		VOL	$I_{OL} = 3.2  \text{mA}$			100	0.4	V
Input Leakage C	urrent	Iin	$V_{in} = 0 \sim 5.5 \text{V}$		a 1173		2.5	μA
Output Leakage	Current	I <sub>LOH</sub>	$CS = 0.8V, \overline{CS} = 2.2V$ $V_{out} = 2.4V$			100	10	μA
Output Leakage	current	ILOL		$V_{out} = 0.4$ V	-	-	10	μA
Supply Current	Active	Icc*	$V_{CC} = 5.5 \text{V}, I_{out} = 0 \text{ m}$	A	-	10	30	mA
Supply Current	Standby	ISB	$V_{CC} = 5.5 \text{V}, \overline{\text{CS}} \ge V_{CC}$	$c = 0.2$ V, CS $\leq 0.2$ V	The	1	30	Au o
Input Capacitan	ce	Cin	$V_{in} = 0$ V, $f = 1$ MHz, $T_a = 25$ °C		0	-	10	pF
Output Capacita	nce	Cout				-	15	pF

\* Steady state current

area-State Dated Consultation OR-Tis

#### RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

 $(V_{cc}=5V\pm10\%, V_{ss}=0V, Ta=-20\sim+75^{\circ}C, t_r=t_f=20ns)$ 

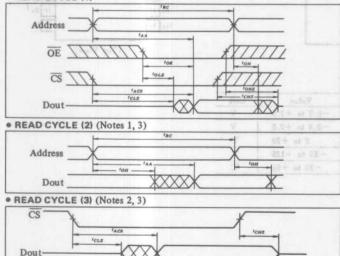
Item	Symbol	min	max	Unit	
Read Cycle Time	tRC	250	-	ns	
Address Access Time	IAA	-	250	ns	
Chip Select Access Time	IACS	-	250	ns	
Chip Selection to Output in Low Z	tCLZ	10	-	ns	
Output Enable to Output Valid	toe	-	100	ns	
Output Enable to Output in Low Z	tolz	10	-	ns	
Chip Deselection to Output in High Z	ICHZ	0	100	ns	
Chip Disable to Output in High Z	tOHZ	0	100	ns	
Output Hold from Address Change	tOH	10	-	ns	

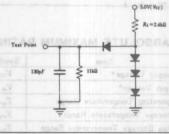


MARDAID NOOJEW



### TIMING WAVEFORM READ CYCLE (1)





Notes : 1. t.-t/= 20 ns 2. CL includes jig capacitance 3. All diodes are 1S2074®

3. All glodes are

**LOAD CIRCUIT** 

NOTES:

 Device is continuously selected.
 Address Valid prior to or coincident with CS transition low.

3.  $\overline{OE} = VIL$ .

**OHITACHI** 

### HN62301P

### Preliminary-

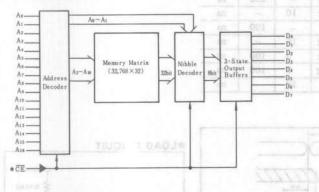
#### 131,072-word×8-bit Mask Programmable Read Only Memory

The HN62301P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The Chip Enable and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

#### FEATURES

- Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time-350ns
- Lower Power Standby and Low Power Operation; Standby: 2mW (typ.), Operation: 75mW (typ.)

#### BLOCK DIAGRAM



Symbol

Vcc

Vis

Tapr

Tels

Thiss

Value

-0.3 to +7.0

-0.3 to +7.0

-55 to +125

-20 to +85

0 to +70

Unit

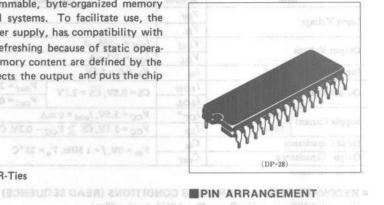
V

V

°C

°C

°C



Ais 1

A12 2

28 Vcc

27 A14



# epotit h



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales Dept, regarding specifications.

ABSOLUTE MAXIMUM RATINGS

Item

**Operating Temperature Range** 

Bias Storage Temperature Range

Storage Temperature Range

Supply Voltage\*

\* With respect to Vas

Input Voltage\*

### **OHITACHI**

HN62301P

#### **RECOMMENDED DC OPERATING CONDITIONS** (*Ta*=0 to 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage*	Vcc	4.5	5.0	5.5	V
	VIL	-0.3	V4	0.8	v
Input Voltage*	Vin	2.2		Vcc	v

\* with respect Vss

#### ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Vss=0V, Ta=0 to +70°C)

Item	Symbol			min	typ	max	Unit
Normal Operating Current	Icci *	$t_{RC1} = \min, V_{CC} = 5.5 \text{V}, I_{out} = 0 \text{mA}$		-	15	50**	mA
Nibble Operating Current	Iccz *	$t_{RC2} = \min, V_{CC} = 5.5 \text{V}, I_{mt} = 0 \text{mA}$		$\overline{\tau}$	15	50**	mA
Stand by Current	Iss	$\overline{CE} \ge V_{cc} - 0.2V, V_{cc} = 5.5V$		-	0.4	10	mA
Input Leakage Current	TLI	V <sub>IN</sub> =0 to 5.5V, other 0V		-10	-	10	μĂ
0	ILON	$\overline{CE} = 2.2V$	Vest=2.4V	-	-	10	μA
Output Leakage Current	ILOL	CE=2.2V V <sub>est</sub> =0.4V		1.5	-	10	μA
0	Von	$I_{out} = -205 \mu A$		2.4	-	-	V
Output Voltage	Vol	I <sub>mat</sub> =3.2mA	I <sub>est</sub> =3.2mA		-	0.4	V

\* Steady state current
\* TBD

#### **CAPACITANCE** (*Vcc*=5V±10%, *Ta*=25°C, 1MHz, *V*<sub>in</sub>=0V)

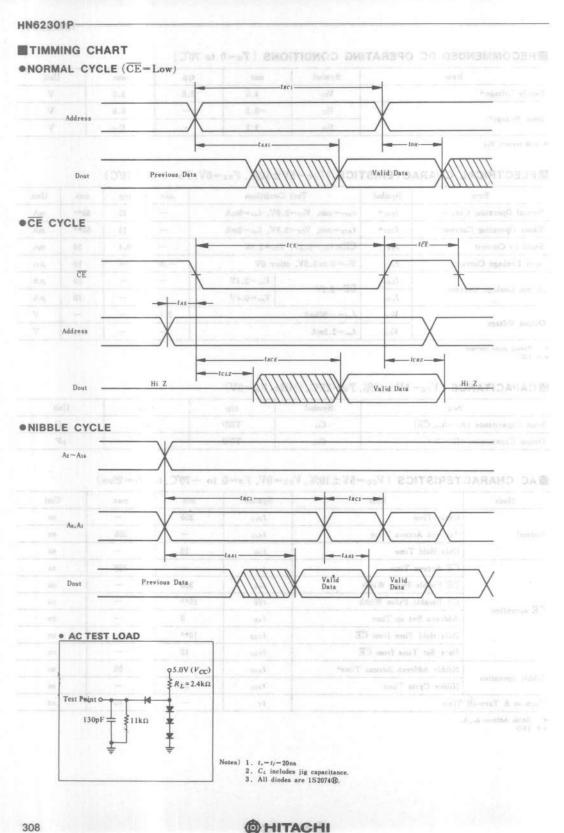
Item	Symbol	typ	max	Unit
Input Capacitance $(A_0 \sim A_{16}, \overline{CE})$	Cis	TBD	10	pF
Output Capacitance (D <sub>0</sub> ~D <sub>7</sub> )	Cest	TBD	15	pF

#### **EAC CHARACTERISTICS** ( $V_{cc}=5V\pm10\%$ , $V_{ss}=0V$ , Ta=0 to $+70^{\circ}C$ , $t_r=t_f=20ns$ )

Mode	Item	Symbol	min	max	ι	Jnit
	Cycle Time	tRCI	350	-		ns
Normal	Address Access Time	t <sub>AA1</sub>	- A	350		ns
	Data Hold Time	ton	-	1	ns	
1.5	CE Access Time	LACE		350		ns
	CE Enable Pulse Width		350		and i	ns
755	CE Disable Pulse Width	ICE	15**	-		ns
CE operation	Address Set up Time	tAS	0	-		ns
	Data Hold Time from $\overline{CE}$	t <sub>CHZ</sub>	10**	0.405 7827	3A -	ns
	Data Set Time from CE	lcLZ	10	-		ns
NULL	Nibble Address Access Time*	LAAZ	120 11 -0.29	50		ns
Nibble operation	Nibble Cycle Time	tRCI	50	-		ns
Turn-on & Turn-of	f Time	t <sub>T</sub>		40	State 1	ns

\* Nibble Address As, As

\* \* TBD



### HN462716, HN4627166

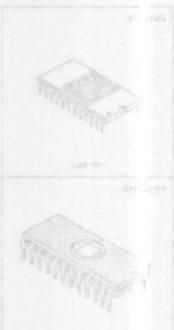
- Sincle Rover Supply ---- +5/r ±5%
- - Colu Power Dissidation -- REBmW Max, Active Power
    - · Three State Outlett ..... OR- The Capability



Outputs (9-(1-3-17)		-47 (15)		
				Deprisent
S (SPH				
			Pair of Wayne Star	
	4+			Program Verify

#### GARSOLUTE MAXIMUM RATINGS

Specific Temperature Range		
Starting Trappedators I wage		
"angerfo" ingent her negel for	14 61 6.0-	
	87 + 02 E.O-	V.







**OHITACHI** 

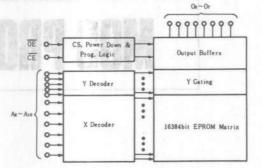
### HN462716, HN462716G

### 2048-word × 8-bit U.V. Erasable and Electrically Programmable Read Only Memory

The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-inline package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

- Single Power Supply · · · · +5V ±5%
- Simple Programming · · · · Program Voltage: +25V DC Programs with One 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time · · · · · · 450ns Max.
- Low Power Dissipation · · 555mW Max. Active Power 161mW Max. Standby Power
- Three State Output · · · · · OR- Tie Capability
- Interchangeable with Intel 2716

#### BLOCK DIAGRAM



#### PROGRAMMING OPERATION

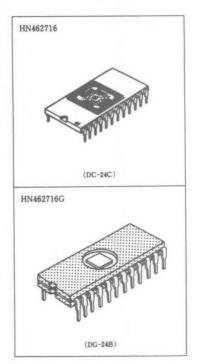
Pins	CE (18)	0E (20)	V <sub>PP</sub> (21)	Vcc (24)	Outputs (9~11, 13~17)
Read	VIL	VIL	+5	+5	Dout
Deselect	Don't Care	Vin	+5	+5	High Z
Power Down	Vin	Don't Care	+5	+5	High Z
Program	Pulsed VIL to VIH	Vin	+25	+5	Din
Program Verify	VIL	VIL	+25	+5	Dout
Program Inhibit	VIL	Vin	+25	+5	High Z

#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit	
Operating Temperature Range	Tape	0 to +70	°C °C	
Storage Temperature Range	Tete	-65 to +125		
All Input and Output Voltages*	Vr	-0.3 to $+7$	V	
VPP Supply Voltage*	VPP	-0.3 to $+28$	V	

**HITACHI** 

\* With respect to Ground



#### PIN ARRANGEMENT

	~~~	
A7 1		24 Vcc
34 2		23 As
As 3		22 As
A. 4		21 Vpp
Aa 5		20 OE
Az 6		19 A18
A1 7		18 CE
Aa 8		17 07
06 9		16 Os
Q1 10		15 05
O2 11		14 0.
GND 12		13 03
	_	

(Top View)

#### READ OPERATION

OTVRICAL CHARACTERISTICS

• DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±5%, VPP=Vcc±0.6V)

Item	Symbol	Test Condition	min.	typ.	max,	Unit
Input Leakage Current	Iu	VIN=5.25V	-	-	10	μA
Output Leakage Current	ILO	Vour=5.25V/0.4V	-		10	μA
VPP Current	IPP1	V <sub>PP</sub> =5.85V		-	5	mA
Vcc Current (Standby)	Icei	$\overline{\text{CE}} = V_{IH}, \overline{\text{OE}} = V_{IL}$	-	13	25	mA
Vcc Current (Active)	Icc:	$\overline{\text{OE}} = \overline{\text{CE}} = V_{IL}$		56	100	mA
Input Low Voltage	VIL		-0.1	-	0.8	V
Input High Voltage	VIH		2.0	-	Vcc+1	V
Output Low Voltage	VoL	Iou = 2.1 mA	-	-	0.4	v
Output High Voltage	Von	Ion = -400 µA	2.4	-		V

Note : Vcc must be applied simultaneously or before VPP and removed simultaneously or after VPP.

#### • AC CHARACTERISTICS ( $T_a=0$ to $\pm 70^{\circ}$ C, $V_{cc}=5V\pm5\%$ , $V_{PP}=V_{cc}\pm0.6V$ )

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address to Output Delay	LACC	$\overline{\text{OE}} = \overline{\text{CE}} = V_{IL}$	-	+	450	ns
CE to Output Delay	tce	$\overline{\text{OE}} = V_{lL}$	-	+	450	ns
OE to Output Delay	tor	$\overline{\text{CE}} = V_{IL}$		+-+-+	120	ns
OE High to Output Float*	tor	$\overline{\text{CE}} = V_{IL}$	0		100	ns
Address to Output Hold	t on	$\overline{OE} = \overline{CE} = V_{IL}$	0	1 - 1	+	ns

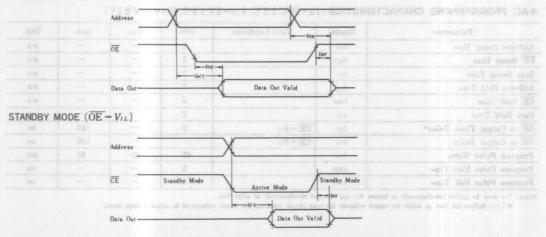
\* : tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

#### • CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C.,	V <sub>IN</sub> =0V	-	6	pF
Output Capacitance	Cres	Vour=0V	DARATICS	12	pF

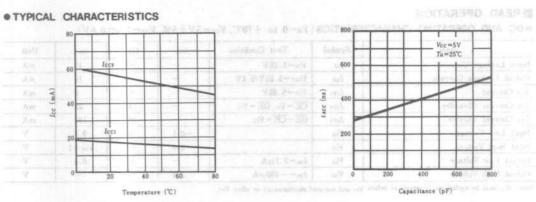
SWITCHING CHARACTERISTICS		
Test Conditions		Ispet Lealings Correct
A Input Pulse Levels:	0.8V to 2.2V	
Input Rise and Fall Times:	≤ 20 ns	New Sociale Courtes Divising Program
Output Load:	1TTL Gate + 100 pF	
Reference Level for Measuring Timing		Invest Low Lawed
	Outputs 0.8V and 2V	

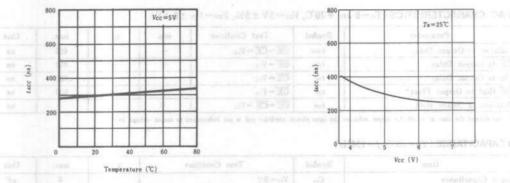
#### READ MODE $(\overline{CE} - V_{IL})$





#### HN462716, HN462716G-





#### • DC PROGRAMMING CHARACTERISTICS ( $Ta=25^{\circ}C\pm 5^{\circ}C$ , $V_{cc}=5V\pm 5\%$ , $V_{PP}=25V\pm 1V$ )

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	VIN=5.25V	-	-	10	μA
VPP Supply Current	IPPS	CE-VIL VSCOIVE.0			5	mA
VPP Supply Current During Programming	IPP1	$\overline{\text{CE}} = V_{IH}$ $\longrightarrow$ $OE >$	-	ANNAL IN	30	mA
Vcc Supply Current	Icc	40.001 + 4160 74.11		<u> </u>	100	mA
Input Low Level	VIL	VIL DICE VIE LEVIDIO	-0.1	11.10E-240 CO	0.8	V
Input High Level	VIH	AT DOM & CO. MUCHEC	2.0	-	$V_{cc}+1$	V

#### • AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=5V±5%, VPP=25V±1V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	las		2		1.11	μs
OE Setup Time	toes	· · · · · · · · · · · · · · · · · · ·	2	-	-	μs
Data Setup Time	tos		2		-	μs
Address Hold Time	-tan	www.wo.wol	2		_	μs
OE Hold Time	toeн	and the second second second	5	-	-	μs
Data Hold Time	t DH		2		- 301-300	ι.v.μs.
OE to Output Float Delay*	t DF	$\overline{CE} = V_{IL}$	0	_	120	ns
OE to Output Delay	tos	$\overline{\text{CE}} = V_{IL}$	-	-	120	ns
Program Pulse Width	t pw	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	45	50	55	ms
Program Pulse Rise Time	L PRT		5	-	-	ns
Program Pulse Fall Time	L PFT	V	5	- 1		ns

Notes : Vcc must be applied simultaneously or before Vrr and removed simultaneously or after Vrr.

# : tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

#### HN462716, HN462716G

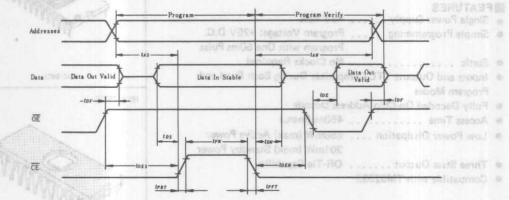
#### SWITCHING CHARACTERISTICS

#### **Test Conditions**

Input Pulse Level: 0.8V to 2.2V Reference Level for Measuring Timing: Inputs; 1V and 2V, Outputs; 0.8V and 2V

4096-word X 8-bit U. V. Emassillo and Programmable The HN462532 is a 4036 word by 8 bit preside and electrically Input Rise and Fall Times: <20 ns Output Load: 1 TTL Gate + 100 pF a new pattern can then be written into the device.

#### PROGRAMMING WAVEFORMS



#### *ERASE*

Erasure of HN462716 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm<sup>2</sup> DEVICE OPERATION

#### READ MODE

Dataout is available 450ns (t'ACC) from addresses with OE low or 120ns (t OE) from OE with addresses stable.

#### DESELECT MODE

The outputs may be OR-tied together with the other HN462716s. When HN462716s are deselected, the OE inputs must be at high TTL level.

#### POWER DOWN MODE

Power down is achieved with CE high TTL level. In this mode the outputs are in a high impedance state.

#### PROGRAMMING

Initially, and after each erasure, all bits of the HN462716 are in the "High" state (Output High). Data is introduced by selectively programming "low" into the desired bit locations. In the programming mode, Vpp power supply is at 25V and OE input is at high TTL level. Data to be programmed are presented 8-bits in parallel, to the data output lines (00 to 07).

The addresses and inputs are at TTL levels.

After the address and data setup, a 50 ms, active high program pulse is applied to the CE input. The CE is at TTL level.

The HN462716 must not be programmed with a DC signal applied to the CE input.

#### PROGRAM VERIFY

The HN462716 has a program verify mode. A verify should be performed on the programmed bits to determine that they were correctly programmed. In this mode Vpp is at 25V.

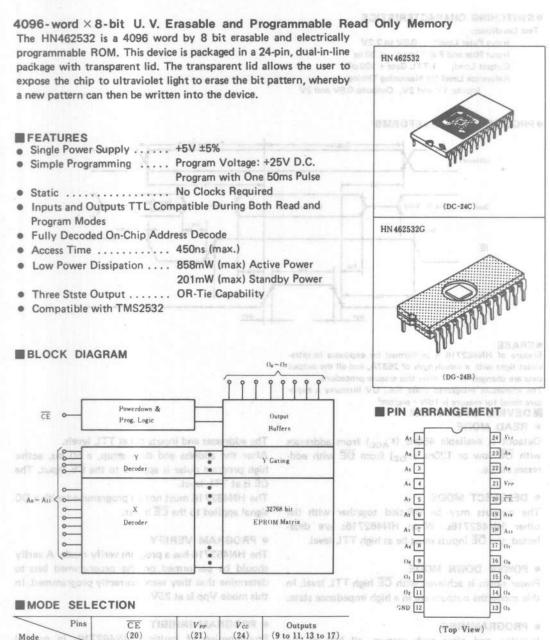
#### PROGRAM INHIBIT

Programming of multiple HN462716s in parallel with different data is easily accomplished by using this mode. Except for CE, all like inputs of the parallel HN462716s may be common.

A TTL program pulse applied to a HN462716's CE input will program that HN462716. A low level CE inhibits the other HN462716s from being programmed.



### HN462532, HN462532G



High Z High Z

Stand by VIN +5+5Program Pulsed Vin to Vil +25+5Program Inhibit VIN +25 +5

VIL

+5

+5

C HITACHI

Dout

Din

Read

#### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*	V <sub>T</sub>	-0.3 to +7	v
VPP Voltage*	V <sub>PP</sub>	-0.3 to +28	V
Operating Temperature Range	Tup	0 to +70	°C
Storage Temperature Range	Ting	-65 to +125	°C
* With respect to GND.		1	

#### READ OPERATION

#### • DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±5%, VPP=Vcc±0.6V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	V., =5.25 V	-1 Smb		10	μA
Output Leakage Current	ILO	Vout = 5.25 V /0.4 V	- 1	-	10	μA
VPP Current	IPPI	$V_{PP} = 5.85 V$	-	-	12	m A
Vcc Current (Standby)	Icci	$\overline{\text{CE}} = V_{IH}$	- 1 in	-	25	m A
Vcc Current (Active)	Iccz	$\overline{\text{CE}} = V_{lL}$	- 1	-	150	m A
Input Low Voltage	VIL		-0.1	-	0.8	V
Input High Voltage	Vin		2.0		Vcc+1	V
Output Low Voltage	VoL	$I_{OL} = 2.1 \mathrm{mA}$	-	-	0.4	V
Output High Voltage	Von	$I_{OH} = -400 \mu \text{A}$	2.4	-	10 10	V

Note I Ver must be applied simultaneously or before Vir and removed simultaneously or after Vir.

#### • AC CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±5%, Vpp=Vcc±0.6V)

Parameter	Symbol	Test Condition	min	typ	max	Uhit
Address to Output Delay	LACC	$\overline{CE} = V_{IL}$	801+219	BTO <del>R</del> CA	450	ns
CE to Output Delay	tce		-	-	450	ns
CE High to Output Float *	tor	V 5.2 07 V 6.0	0	- 1	100	ns
Address to Output Hold	toн	$\overline{CE} - V_{IL}$	0	_	boi_adfi	ns

\* : tow defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

#### Contractive O.S.V. and 2.V.

#### SWITCHING CHARACTERISTICS

#### Test Conditions Input Pulse Levels: 0.8V to 2.2V Input Rise and Fall Times: < 20 ns 1TTL Gate + 100pF Output Load: Reference Level for Measuring Timing: Inputs; 1V and 2V, Outputs; 0.8V and 2V Address CE Standby Mode Active Mode Standby Mode LOF

• CAPACITANCE ( $Ta=25^{\circ}C, f=1MHz$ )

Data Out

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C.a	V., = 0 V	-	-	6	pF
Output Capacitance	Crat	$V_{ext} = 0 V$	-	-	12	pF

LEE

Data Out Valid



#### HN462532, HN462532G

#### PROGRAMMING OPERATION

EABSOLUTE MACIMUM RATINGS

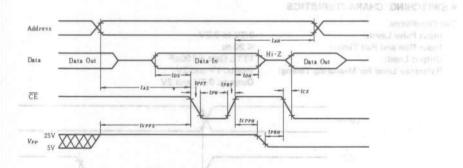
• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=5V±5%, VPP=25V±1V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	Via = 5.25 V /0.4 V	-	-	10	μA
VPP Supply Current During Programming	IPPI	$\overline{CE} = V_{IL}$	-	08410	30	mA
Vcc Supply Current	Icc	A second second	-		150	mA
Input Low Level	VIL		-0.1	-	0.8	V
Input High Level-	VIR		2.0	14813	Vcc+1	V

• AC PROGRAMMING CHARACTERISTICS ( $Ta=25^{\circ}C\pm5^{\circ}C$ ,  $V_{cc}=5V\pm5\%$ ,  $V_{PP}=25V\pm1V$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	tas	Va 0. 28 V /0. 4 V	2	-' 105	No. Stand	μs
Data Setup Time	tos	V02.2-44	2	-		μs
Address Hold Time	t <sub>AH</sub>	14-351	2		lisent) h	μs
Data Hold Time	t <sub>DH</sub>	1 - CE = 10	2	-	alista a	μs
Setup Time from VPP	lypps		0	-	Voltage	ns
Program Pulse Hold Time	t PRH		0	-	Softwork -	ns
VPP Hold Time	t vpph	Am - Solar A	0	-	AUDDER V	ns
Program Pulse Width	t pw	A.o. 901 - au	45	50	55	ms
Program Pulse Time	tPRT	N role is derrichten fermer bie	5	i nationali		ns
Program Pulse Time	<b>L</b> PFT		5	-	-	ns

SWITCHING CHARACTERISTICS			
Test Conditions		412	
Input Pulse Level:	0.8V to 2.2V		Ch. Mush to Output. Floar?"
Input Rise and Fall Times: Output Load:	< 20 ns 1TTL Gate + 100pF	nik	Unit improves an and the Links
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V	s esperado comine to	



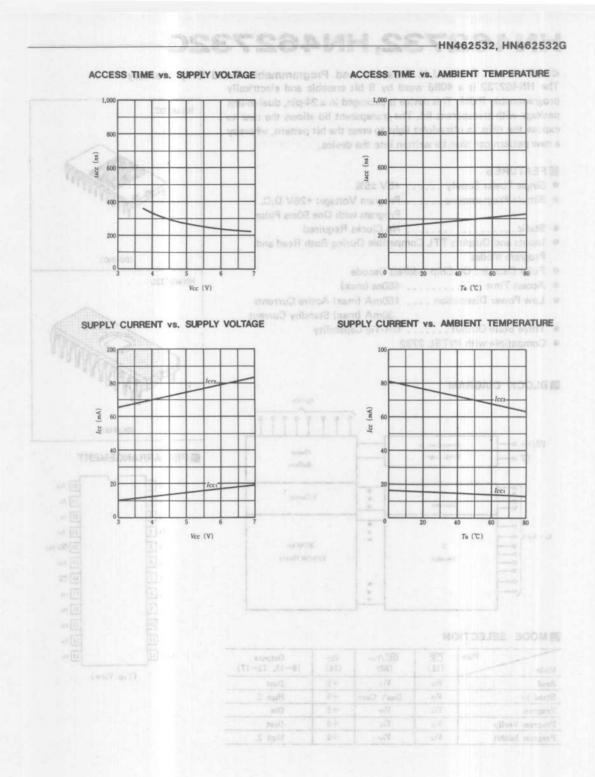
#### ERASE

Erasure of HN462532 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated close (i.e., UV intensity x exposure time) for erasure is  $15W \cdot sec/cm^2$ .

	States and a state of the

		Text Couldness		an in manufic
			- C M	Inco. Countinees

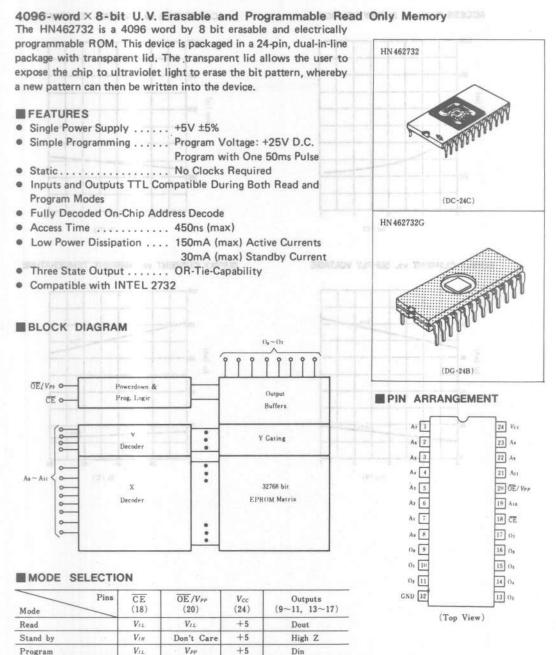
**HITACHI** 



**OHITACHI** 

317

# HN462732, HN462732G



Dout

High Z

**Program Verify** 

**Program** Inhibit

Vit

 $V_{IH}$ 

ViL

VPP

+5

+5

Item	7-31 (V) 3 V BE	Symbol		Value		Unit		
Operating Temperature Range	- 1 + 510C	N Intell	T <sub>opr</sub>	0 to +70 °C				
Storage Temperature Range	78.0			-65 to +125		20	-	
All Input and Output Voltage*		Amilia	VT	-0.3 to +7		V		
VPP Voltage*	1.1.1.1.1	1.504	OE /VPP	-0.3 to +28		V	11 100	
With respect to GND READ OPERATION DC AND OPERATING CH/ Parameter		i ( <i>Ta=</i>	0 to +70°C, Vcc=5	V±5%, V <sub>PF</sub>	$= V_{cc} \pm typ.$	0.6V)	Unit	
Input Leakage Current (Except C		Iun	V <sub>IN</sub> =5.25V	-	-	10	μA	
OE /Vrp Input Leakage Current	(BITH)	Ius	$V_{IN} = 5.25 V$		-	10	μA	
Output Leakage Current	100 050 0800	ILO	$V_{ent} = 5.25 \text{V}$	-	197 - 197	10	μA	
Vcc Current (Standby)		Icci	$\overline{\text{CE}} = V_{IH}, \overline{\text{OE}} = V_{IL}$	-	-	30	mA	
Vcc Current (Active)	5	Icca	$\overline{OE} = \overline{CE} = V_{IL}$	-	-	150	mA	
Input Low Voltage	5	VIL	-	-0.1	-	0.8	V	
Input High Voltage	6	Vin		2.0	-	Vcc+1	V	
Output Low Voltage	2	Vol	Ioc=2.1mA	-	-	0.45	V	
Output High Voltage	4	Von	$I_{OH} = -400 \mu \text{A}$	2.4		-	V	
AC CHARACTERISTICS	<i>Ta</i> =0 to +70°C,	$V_{cc} = 5$	$V\pm5\%, V_{PP}=V_{cc}\pm0$	0.6V) *cale	1 2007 1	THE AT ME	an Taga	
Parameter	23	Symbol	Test Condition	min	typ	max	Unit	
Address to Output Delay	50	1 ACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	minuterence	S NUT W	450	ns	
CE to Output Delay -	2	t <sub>CE</sub>	$\overline{OE} = V_{IL}$	-	-	450	ns	
Output Enable to Output Delay		1000	and the second s			100		
output isnable to output Delay	regular acquerit in press	tor	$CE = V_{IL}$	dr a contra longe	A DECTOR	120	+ 85	
		tor	$\frac{CE = V_{IL}}{CE = V_{IL}}$	0	- 100 Tay -	120	+ ns	
Output Enable High to Output Flo Address to Output Hold <i>tar</i> defines the time at which the output <b>SWITCHING CHARACTER</b> Test Condition	at *	tor ton it condition	$\overline{CE} = V_{IL}$ $\overline{CE} = \overline{OE} = V_{IL}$ a and is not referenced to our	0 htput voltage level		100 Control of the second seco	ns Thins tegal tugal	
Output Enable High to Output Flo Address to Output Hold * tor defines the time at which the output <b>SWITCHING CHARACTER</b> Test Condition Input Pulse Levels: Input Rise and Fall Times: Output Load: Reference Level for Measurin Address	t achieves the open circu ISTICS 0.8 ≤ 2 1T ng Timing: Inp	I DF I ON it condition V to 2.2 20ns TL Gate uuts 1V i tputs 0.1	$CE - V_{IL}$ $CE - OE = V_{IL}$ and is not referenced to out $2V$ $+ 100pF$ and 2V $8V \text{ and } 2V$ $6ode$ $cz - for -$	0 ttput voltage level	- TTD4110 a. contT is contT is contM to	100 Control of the second seco	ns Ins Ingel	
Dutput Enable High to Output Flo Address to Output Hold to reference Levels: Input Rise and Fall Times: Output Load: Reference Level for Measurin Address OE OE Data Out CCAPACITANCE (Ta-25°C, J Parameter	t achieves the open circu ISTICS 0.8 ≤ 2 1T ng Timing: 0u tandby Mode	Lop Lon it condition V to 2.2 20ns TL Gate uuts 1V : tputs 0.1 Active M	$CE - V_{IL}$ $CE - OE - V_{IL}$ a and is not referenced to out $2V$ $+ 100pF$ and 2V $BV and 2V$ $BV and 2V$ $bode$ $ce$ $toz - toz$	0 ttput voltage level	- TTD4110 a. contT is contT is contM to	100	ns ns definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition definition defin	
Output Enable High to Output Flo Address to Output Hold * tor defines the time at which the output SWITCHING CHARACTER Test Condition Input Pulse Levels: Input Rise and Fall Times: Output Load: Reference Level for Measurin Address CE S OE Data Out - CAPACITANCE (Ta-25°C, J	t achieves the open circu ISTICS 0.8 ≤ 2 1T ng Timing: 0u tandby Mode	I DF I ON it condition V to 2.2 20ns TL Gate nuts 1V it tputs 0.1 Active M	$CE = V_{IL}$ $CE = OE = V_{IL}$ a and is not referenced to out $2V$ $+ 100pF$ and 2V $BV and 2V$ $BV and 2V$ $bode$ $ce$ $-toz$ $-toz$ $Data Out Valid$	tput voltage level		001 010 010 010 010 010 010 010	ns Ins Ins Ins Ins Ins Ins Ins Ins Ins I	

**HITACHI** 

#### HN462732, HN462732G

#### **PROGRAMMING OPERATION**

BARSOLUTE MAX-MOM PATINGS

SAN TOHING CHARACTERISTICS

CAPACITARCE (The 26°C, J=1 MHa)

• DC PROGRAMMING CHARACTERISTICS ( $V_{cc} = 5V \pm 5\%$ ,  $V_{PP} = 25V \pm 1V$ ,  $Ta = 25^{\circ}C \pm 5^{\circ}C$ )

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	VIN=5.25V/0.4V	-	0.57ic 8 .	10	#A
Output Low Voltage During Verify	VoL	Io1 = 2.1 mA	-	* 191 <del>0 -</del> 17 - 1	0.4	V
Output High Voltage During Verify	Von	Ion=-400 µA	2.4	-		V
Vcc Supply Current	Icc		-	-	150	mA
Input Low Level	VIL		-0.1	- Kenth	0.8	V
Input High Level (All Input Except $\overline{\mathrm{OE}}/V_{PP})$	VIN	RISTICS (Ter-1 to	2.0	D DESTA	Vcc+1	V
VPP Supply Current	IPP	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{PP}$	-		30	mA

• AC PROGRAMMING CHARACTERISTICS ( $V_{cc} = 5V \pm 5\%$ ,  $V_{PP} = 25V \pm 1V$ ,  $Ta = 25^{\circ}C \pm 5^{\circ}C$ )

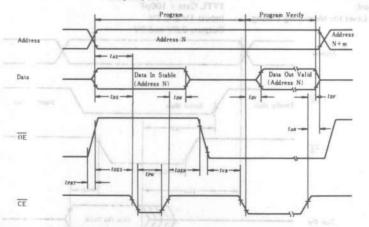
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	tas	- 13 I I I I	2	- 10	Constant In	μs
OE Setup Time	loss	- 100 Long	2	-	m. Dervo	μs
Data Setup Time	tos	262	2	-	N. TEV	μs
Address Hold Time	t AH	No.	0	-	Distantin V	μs
OE Hold Time	LOEN	Mr. See-	2	-	and a	μs
Data Hold Time	ton	Part I fee	2	-	an toy da	μs
Chip Enable to Output Float Delay*	tor	ALL TRACK MANAGER	0		120	ns
Data Valid from CE	tov	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{IL}$	-		1	μs
CE Pulse Width During Programming	t <sub>Pw</sub>	locinical .	45	50	55	ms
OE Pulse Rise Time During Programming	L PRT	ter O	50	- Lie	trand a	ns
VPP Recovery Time	t vk	- 315 ml -	2	-	(dell-page	μs

\* tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

#### SWITCHING CHARACTERISTICS

#### **Test Conditions**

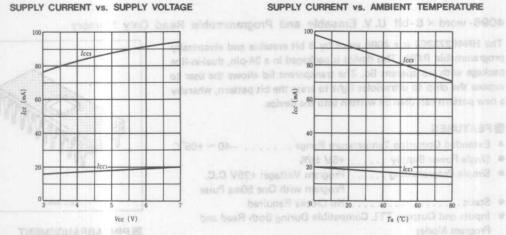
Input Pulse Level: Input Rise and Fall Times: Output Load: Reference Level for Measuring Timing: 0.8V to 2.2V ≤ 20ns 1TTL Gate + 100pF Inputs; 1V and 2V, Outputs; 0.8V and 2V

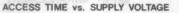


#### • ERASE

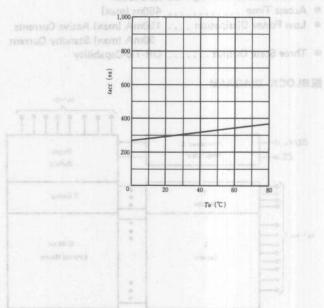
Erasure of HN462732 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this prosedure. The minimum integrated close (i.e., UV intensity x expo-

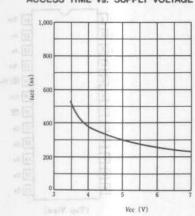
sure time) for erasure is 15W • sec/cm<sup>2</sup>.











		08.96		
(11-11 12-17)				
	24		112	

NOTIOBLER BELECTION

**HITACHI** 

### HN462732G

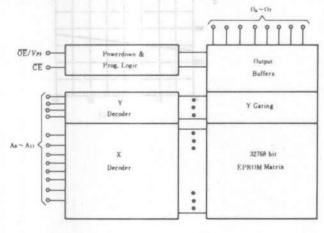
4096-word × 8-bit U.V. Erasable and Programmable Read Only Memory

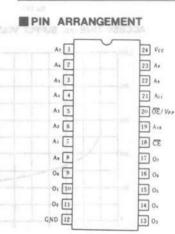
The HN462732GI is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

#### FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +25V D.C. Program with One 50ms Pulse
- Static . . . . . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time ...... 450ns (max)
- Low Power Dissipation .... 150mA (max) Active Currents 30mA (max) Standby Current
- Three State Output ..... OR-Tie-Capability





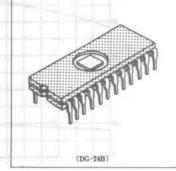


(Top View)

#### MODE SELECTION

Pins	CE (18)	0E /V <sub>PP</sub> (20)	Vcc (24)	Outputs (9~11, 13~17)
Read	VIL	VIL	+5	Dout
Stand by	VIN	Don't Care	+5	High Z
Program	VIL	V <sub>PP</sub>	+5	Din
Program Verify	VIL	VIL	+5	Dout
Program Inhibit	VIN	VPP	+5	High Z

**OHITACHI** 



#### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit
Operating Temperature Range	Tayr	-40 to +85	°C
Storage Temperature Range	Tete	-65 to +125	С.
All Input and Output Voltage*	Vr	-0.3 to +7	V
VPP Voltage*	OE /VPP	-0.3 to +28	and such a V and sugar
With respect to GND	An 000	direct as	and analisi will report
READ OPERATION			
DC AND OPERATING CHARACTERIST	ICS $(Ta = -40 \text{ to } + 85^{\circ}C)$	V <sub>CC</sub> =5V ±5%,)	

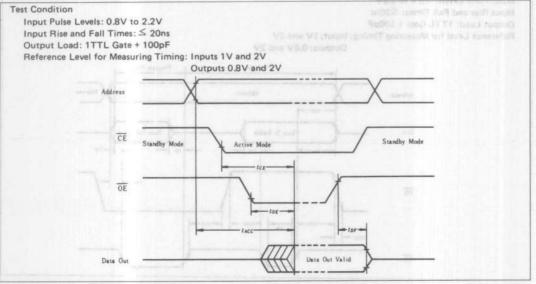
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current (Except OE /VPP)	I <sub>U1</sub>	$V_{IN} = 5.25 V$	-	-	10	μA
OE /VPP Input Leakage Current	Iui	$V_{IN} = 5.25 V$	-	-	10	μA
Output Leakage Current	ILO	Vout = 5.25V/0.45V	0120-00	10.76	10	μA
Vcc Current (Standby)	Icc1	$\overline{\text{CE}} = V_{IH}, \overline{\text{OE}} = V_{IL}$	-	-	30	mA
Vcc Current (Active)	Icc 2	$\overline{\text{OE}} = \overline{\text{CE}} = V_{IL}$	-	-	150	mA
Input Low Voltage	VIL		-0.1	-	0.8	V
Input High Voltage	Vin		2.0	-	Vcc+1	v
Output Low Voltage	VoL.	$I_{OL} = 2.1 \mathrm{mA}$	-	-	0.45	V
Output High Voltage	Von	Iон 400 µА	2.4	-	-	V

• AC CHARACTERISTICS ( $Ta = -40 \text{ to } + 85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ )

Parameter	Symbol	Test Condition	HN462732GI			Unit
			min.	typ.	max.	Unit
Address to Output Delay	IACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	- 1800		450	ns
CE to Output Delay	1 <sub>CE</sub>	$\overline{OE} = V_{IL}$	E-Thomas I	- 10 - 10 - 10 - 10 - 10 - 10 - 10 - 10	450	ns
Output Enable to Output Delay	LOE	$\overline{\text{CE}} = V_{IL}$	-	-	150	ns
Output Enable High to Output Float*	tDF	$\overline{CE} = V_{IL}$	0	the the second	130	ns
Address to Output Hold	toH	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	-	ns

\* tar defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.





#### • CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance (Except OE/VPP)	Gm	V <sub>IN</sub> -0V	antras auto	199 T 20 1 1 1	6	pF
OE /Vpp Input Capacitance	Cinz	$V_{IN} = 0 V$		-	20	pF
Output Capacitance	Cest	V <sub>sat</sub> = 0 V	Farmer and	WITT	12	pF



WARSOLUTE MAXIMUM RATING

# **PROGRAMMING OPERATION**

• DC PROGRAMMING CHARACTERISTICS ( $V_{cc} = 5V \pm 5\%$ ,  $V_{PP} = 25V \pm 1V$ ,  $Ta = 25^{\circ}C \pm 5^{\circ}C$ )

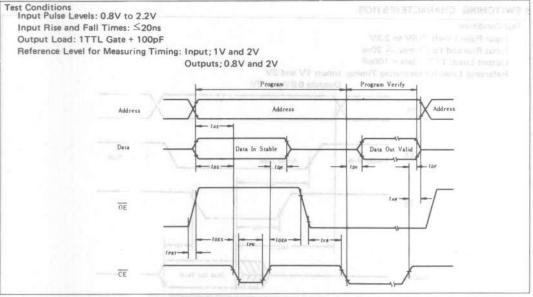
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	VIN=5.25V/0.4V	-	10000007	10	μA
Output Low Voltage During Verify	Vol	Io1 = 2.1 mA	-	-	0.4	V
Output High Voltage During Verify	Von	$I_{OH} = -400\mu\mathrm{A}$	2.4	-	0.00	v
Vcc Supply Current	Icc		-	144017	150	mA
Input Low Level	VIL	ang 1103 (14= -40.0	-0.1	0.0400	0.8	V.
Input High Level (All Input Except $\overline{\operatorname{OE}}/V_{PP})$	VIN	Symbol	2.0	11157011	Vcc+1	V
VPP Supply Current	Ipp	$\overline{\text{CE}} = V_{IL}, \overline{\text{OE}} = V_{PP}$	(1. N. T.)		30	mA

# • AC PROGRAMMING CHARACTERISTICS ( $V_{cc} = 5V \pm 5\%$ , $V_{PP} = 25V \pm 1V$ , $Ta = 25^{\circ}C \pm 5^{\circ}C$ )

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	tas	an ing	2	-	Lattola h	μs
OE Setup Time	toes		2	-	00(6 <u>35</u> 0V)	μs
Data Setup Time	tos		2	-	1997	μs
Address Hold Time	t <sub>AH</sub>	A A	0	-	raatt <u>eV</u> =	μs
OE Hold Time	t oen	New John	2	-	14/11/22 14	μs
Data Hold Time	t <sub>DH</sub>	1 + W2 = 0.0 4 (2 128 + 01	2	1804181	137.0450	μs
Chip Enable to Output Float Delay*	tor		0	-	120	ns
Data Valid from CE	tov	$\overline{\text{CE}} = V_{lL}, \overline{\text{OE}} = V_{lL}$	-		1	μs
CE Pulse Width During Programming	L PW	1×30×33 1 33%	45	50	55	ms
OE Pulse Rise Time During Programming	1 PRT	16# 1 QL+ VIL	50	-	Visio (Helico)	ns
VPP Recovery Time	t vn	108 CE+ Pr	2	200-001	10 a - 14	μs

# tar defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

# SWITCHING CHARACTERISTICS



# • ERASE

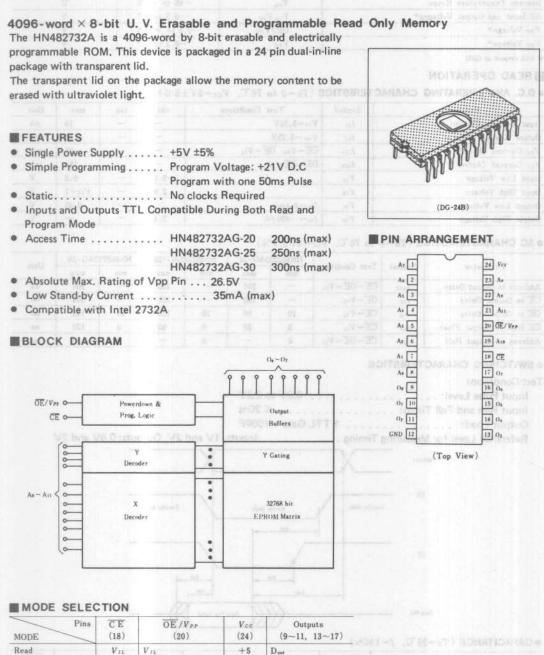
Erasure of HN462732 is performed by exposure to Ultraviolet light of 2537A, and all the output data are changed to "1" after this prosedure.

The minimum integrated close (i.e., UV intensity x exposure time) for erasure is  $15W \cdot sec/cm^3$ 

reau Ganesterre Diness (1874) OF 70% Ingen Capatitien Deper Capatitien

**© HITACHI** 

# HN482732AG-20, HN482732AG-25, HN482732AG-30



HITACHI

High Z

Dis

Dour

High Z

+5

+5

+5

+5

Don't Care

Vpp

VIL

VPP

VIN

VIL

VIL

VIH

Stand by

Program

Program Verify

Program Inhibit

# HN482732AG-20, HN482732AG-25, HN482732AG-30-

# BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tate	-65 to +125	°C
All Input and Output Voltages*	Vis, Vest	-0.3 to +7	V
VPP Voltage *	OE/Vpp	-0.3 to +26.5	v
Vcc Voltage*	Vcc	-0.3 to $+7$	V

\* with respect to GND

bill the transformed differences and

# READ OPERATION

COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPANY OF A COMPA

D.C. AND OPERATING	CHARACTERISTICS (Ta=	0 to 70°C.	$V_{cc} = 5V \pm 5\%$	
--------------------	----------------------	------------	-----------------------	--

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	Iu	V18-5.25V	-	-	10	μA
Output Leakage Current	ILO	$V_{vut} = 5.25 V$	-		10	μA
Vcc Current (Standby)	Icci	$\overline{\text{CE}} = V_{IH}, \ \overline{\text{OE}} = V_{IL}$	12+	37/0 0	35	mA
Vcc Current (Active)	Iccz	$\overline{\text{OE}} = \overline{\text{CE}} = V_{lL}$	- Pres		150	mA
Input Low Voltage	VIL	which ambit uses three must	-0.1		0.8	V
Input High Voltage	VIN	hadring to produce	2.0	-	Vcc+1	V
Output Low Voltage	V OL	Io1-2.1mA	1		0.45	V
Output High Voltage	Vou	<i>Iон</i> =-400 <i>µ</i> А	2.4		-	V

# • AC CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±5%)

Parameter Symbol	Conclust	Test Conditions	HN482732AG-20		HN482732AG -25		HN482732AG-30		Unit	
	Symbol	Test Conditions	min	max	min	max	min	max	Unit	
Address to Output Delay	LACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	200	-	250	12-12-16-1	300	ns	
CE to Output Delay	tcE	$\overline{OE} = V_{IL}$	-	200	00-	250	100	300	ns	
OE to Output Delay	t OE	$\overline{\text{CE}} = V_{IL}$	10	90	10	100	10	150	ns	
OE High to Output Float	tor	$\overline{\text{CE}} = V_{IL}$	0	80	0	90	0	130	ns	
Address to Output Hold	ton	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	-	0	348 1	ns	

# • SWITCHING CHARACTERISTICS

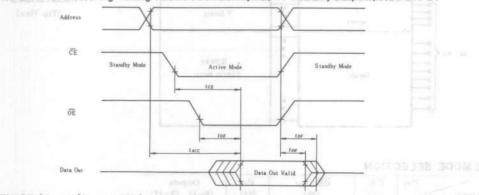
**Test Conditions** 

Input Pulse Level: .		0.8V to 2.2V
----------------------	--	--------------

Input Rise and Fall Times: . . . . . . . . . . . . . . . .  $\leq$  20ns

Output Load: ..... 1 TTL Gate + 100PF

Reference Level for Measuring Timing . . . . . . . . . Inputs, 1V and 2V, Outputs; 0.8V and 2V



# • CAPACITANCE (Ta=25°C, f=1 MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance (Except OE / VPP)	C <sub>IN1</sub>	$V_{IN}=0$ V		-	6	pF
OE / VPP Input Capacitance	Cint	V1N=0V	-	-	20	pF
Output Capacitance	Cest	$V_{out} = 0 V$		-	12	pF

# PROGRAMMING OPERATION

●DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=5V±5%, Vpp=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	VIN-VIL OF VIH	-	-	10	μA
Output Low Voltage During Verify	Vol	IoL=2.1mA	9943-V	JU 4id	0.4	V
Output High Voltage During Verify	Von	Iou=-400 #A	2.4	(C12+0)	1011	V
Vcc Supply Current	Icc	reactions in a 20 pills that in	d maistable	shift M	150	mA
Input Low Level	VIL	and with one fail tree management a	-0.1	Institut	0.8	V
Input High Level (All Inputs Except $\overline{OE}/V_{PP}$ )	VIH	month and about the shifter bigan	2.0	ALC: THE .	Vcc+1	V
V <sub>PP</sub> Supply Current	IPP	$\overline{\rm CE} = V_{IL_{\rm f}} \ \overline{\rm OE} = V_{PP}$	-	-	30	mA

RUYAGHI

# • AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=5V±5%, Vpp=21V±0.5V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Address Setup Time	tas	states and the userably	2	-	-	μs
OE Setup Time	toes	STRUE ENDERT ON Y COMPANY	2		1.1-1.5	μs
Data Setup Time	tos	pur usey unde quirnis alons	2	I I KIND	LAU DESE	μ5
Address Hold Time	t AH		0	-	<u>, el</u> . o h	μs
OE Hold Time	t OEH	HIMAEL MARG	2		<u>-</u>	μs
Data Hold Time	t <sub>DH</sub>	HM482781/6-1 3000	2	-	-	μs
Chip Enable to Output Float Delay*	tor	HN482784/G-4 455x4	0	-	130	ns
Data Valid from CE	tov	$\overline{\text{CE}} = V_{1L}, \ \overline{\text{OE}} = V_{1L}$	enimis	1001-001	1	223
CE Pulse Width During Programming	t <sub>PW</sub>	Am28	45	50	55	ms
OE Pulse Rise Time During Programming	t PRT		50	C laboration of	Hw attales	ns
VPP Recovery Time	t vn		2	-	-	μ5

\* IDF defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

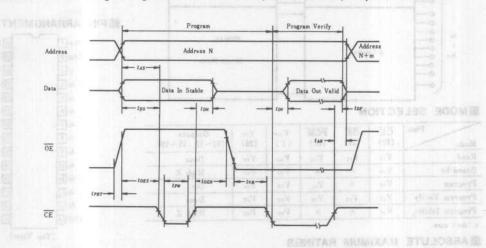
# SWITCHING CHARACTERISTICS

# **Test Condition**

Input Pulse Level ..... 0.8V to 2.2V

Input Rise and Fall Time ..... ≦ 20ns

Reference Level for Measuring Timing: ..... Inputs 1V and 2V; Outputs 0.8V and 2V



#### ERASE

Erasure of HN482732A is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm<sup>2</sup>.



# HN482764, HN482764-3, HN482764-4, HN482764G, HN482764G-3, HN482764G-4

8192-word × 8-bit U. V. Erasable and Programmable Read Only Memory The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line HN482764, HN482764-3, HN482764-4 package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light. FEATURES Simple Programming ..... Program Voltage: +21V D.C. Program with one 50ms Pulse ..... No Clocks Required • Static . . . . Inputs and Outputs TTL Compatible During Both Read and Program Mode. . HN482764/G 250ns max (DC-28B) Access Time HN482764/G-3 300ns max HN482764G, HN482764G-3. HN482764/G-4 450ns max HN482764G-4 High Performance Programming Available 35mA max. . . . . . . . . . . . Compatible with Intel 2764 UB-01 BLOCK DIAGRAM 0 0 9 PGM Power Down Output ŌĒ 0 Prog. Logic CE Buffers 0 (DG-28) Y-Gating Y-Decoder 0 PIN ARRANGMENT 0 0 As 65536 bit 28 Vcc VPP 1 0 27 PGM X-Decode A12 2 A11 0 Memory Matrix 26 NC A1 3 0 0 25 As As 4 0 24 As As 5 23 Au A4 6 MODE SELECTION 22 OE As 7 Pins CE OE PGM VPP Vcc Outputs 21 Ase Az 8 (97) (1) (28) (11~12 15~10 (20) (22) 20 CE A1 9 19 07 Ae 10

Mode	(20)	(22)	(27)	(1)	(28)	(11~13, 15~19)
Read	VIL	$V_{IL}$	Vin	Vcc	Vcc	Dout
Stand-by	VIN	×	×	Vcc	Vcc	High Z
Program	VIL	×	VIL	VPP	Vcc	Din
Program Verify	VIL	VIL	VIH	$V_{PP}$	Vcc	Dout
Program Inhibit	Vin	×	×	VPP	Vcc	High Z

× : don't care

#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value 01 0	Unit
Operating Temperature Range	Tape	0 to +70	°C
Storage Temperature Range	Tere	-65 to +125	°C
All Input and Output Voltage*	V <sub>T</sub>	-0.3 to +7	V
VPP Voltage	VPP	-0.3 to $+26.5$	V

\* : with respect to GND

328

18 04

17 05

16 04

15 01

01 13

GND 14

# (Top View)

# — HN482764, HN482764-3, HN482764-4, HN482764G, HN482764G-3, HN482764G-4

# READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to  $+70^{\circ}$ C,  $V_{cc}=5V\pm5\%$ ,  $V_{PP}=V_{cc}\pm0.6V$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	V <sub>cc</sub> =5.25V, V., =5.25V	-	-	10	μA
Output Leakage Current	ILO	$V_{cc} = 5.25 \text{ V}, V_{aut} = 5.25 \text{ V} / 0.4 \text{ V}$	1		10	μA
VPP Current	I <sub>PP1</sub>	$V_{PP} = V_{CC} + 0.6 \mathrm{V}$	20	-	15	mA
Vcc Current (Standby)	Icci	$\overline{CE} = V_{IH}$	-	-	35	mA
Vcc Current (Active)	Icci	$\overline{CE} = \overline{OE} = V_{IL}$	-	100	150	mA
Input Low Voltage	VIL		-0.1	-	0.8	V
Input High Voltage	Vin		2.0	-	Vcc+1	V
Output Low Voltage	Vol	Io4 = 2.1 mA	-	-	0.45	V
Output High Voltage	VOR	$I_{ON} = -400 \mu \text{A}$	2.4	10 20	NAS <u>E</u> DON	V

# • AC CHARACTERISTICS (Ta=0 to $+70^{\circ}$ C, $V_{cc}=5V\pm5\%$ , $V_{PP}=V_{cc}\pm0.6V$ )

Parameter	Symbol	Test Conditions	HN482764/G		HN482764/G-3		HN482764/G-4		Unit
Parameter			min	max	min	max	min	max	Unit
Address to Output Delay	tACC	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	250	-	300	-	450	ns
CE to Output Delay	t <sub>CE</sub>	$\overline{OE} = V_{IL}$		250	-	300		450	ns
OE to Output Delay	tor	$\overline{\text{CE}} = V_{IL}$	10	100	10	150	10	150	ns
OE High to Output Float	tpp	$\overline{\text{CE}} = V_{TL}$	0	90	0	130	0	130	ns
Address to Output Hold	tou	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	-	0	-	0		ns

Note: Iar defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels

as before the these of a black the mount of the error sources whether our to not bedressen in a mount set on the state

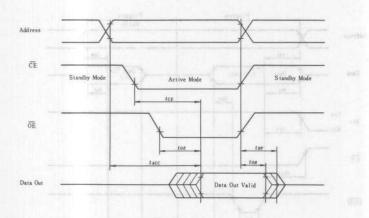
# SWITCHING CHARACTERISTICS Test Condition

Input Pulse Levels: Input Rise and Fall Time: Output Load: Reference Level for Measuring Timing: 0.8V to 2.2V ≤ 20ns 1TTL Gate + 100pF Inputs; 1V and 2V Output; 0.8V and 2.0V

Inna Pute Level: Inna: Pute ind Put

SWITCHING CHARACTERISTICS





#### • CAPACITANCE $(T_a - 25^{\circ}C, f - 1 MHz)$

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C.,	$V_{in} = 0 V$	-	4	6	pF
Output Capacitance	Cest	Vest - 0 V	of the other	8	12	pF

and the state of the second second state the second sec



# HN482764, HN482764-3, HN482764-4, HN482764G, HN482764G-3, HN482764G-4

#### PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, Vcc=5V±5%, Vpp=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	ILI	V., = 5.25 V	-		10	μA
Output Low Voltage During Verify	VoL	$I_{oL}=2.1\mathrm{mA}$	-	-	0.45	V
Output High Voltage During Verify	Von	$I_{OH} = -400 \ \mu \text{A}$	2.4	-	-	V
Vcc Current (Active)	Icca		-	-	150	mA
Input Low Level	VIL	N = S(0 = 3.)	-0.1	-	0.8	V
Input High Level	VIH		2.0	—	$V_{cc} + 1$	V
VPP Supply Current	IPP	$\overline{\text{CE}} = \overline{\text{PGM}} = V_{lL}$	-		30	mA

# • AC PROGRAMMING CHARACTERISTICS ( $T_a = 25\% \pm 5\%$ , $V_{cc} = 5V \pm 5\%$ , $V_{PP} = 21V \pm 0.5V$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	tas	A DE LE COMPANY	2	de Tare	TTTON	μs
OE Setup Time	toes		2	-	-	μs
Data Setup Time	tos	cities the later	2			μs
Address Hold Time	LAH		0	-	-	μs
Data Hold Time	t <sub>DH</sub>	1 - 10 - 10 - 11	2	TE	- MARTER &	μs
OE to Output Float Delay	tor	Per 1020 104	0	-	130	ns
VPP Setup Time	tvs	14-39 M	2	-	1. (m 2. c)	μ5
PGM Pulse Width During Programming	tpw	(V = 10, +4	45	50	55	ms
CE Setup Time	tces	VA = 30 - 125 ( 0.0	2		100242	μs
Data Valid from OE	tor	support sector radi su es	and the second	so entre es	150	ns

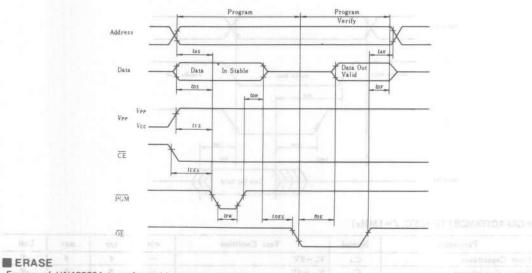
Note: Inr defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:

Input Rise and Fall Time: Reference Level for Measuring Timing: 0.8V to 2.2V ≤ 20 ns Input; 1V and 2V Output; 0.8V and 2V ter ut Polas Linera erunt Rias and Fait Phile Dropes Londi Philemene Land Pai Missione T



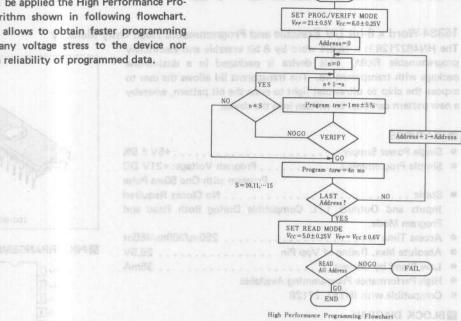
Erasure of HN482764 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W + sec/cm<sup>2</sup>

# HN482764, HN482764-3, HN482764-4, HN482784G, HN482764G-3, HN482764G-4

START

#### HIGH PERFOMANCE PROGRAMMING

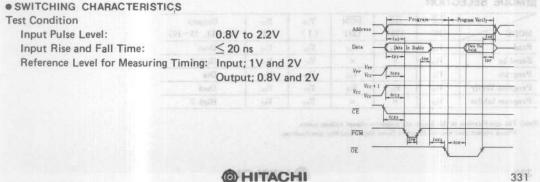
This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

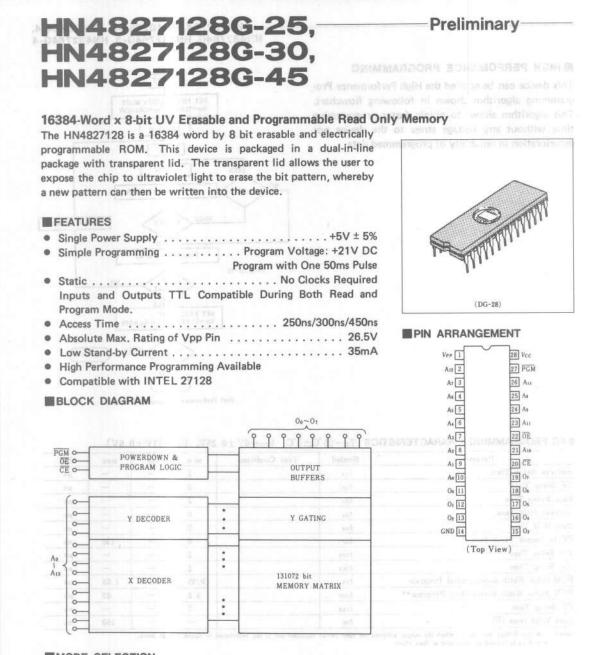


# • AC PROGRAMMING CHARACTERISTICS $(T_a - 25 \degree C \pm 5 \degree C, V_{cc} = 6V \pm 0.25V, V_{PP} = 21V \pm 0.5V)$

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	tas	Taile .	2	-	-	μs
OE Setup Time	toes		2	-	-	μs
Data Setup Time	tos	and the second second second	2	-	-	μs
Address Hold Time	t <sub>AH</sub>	TAG Y	0	lanes Treat	-	μs
Data Hold Time	t <sub>DN</sub>		2	-	-	μs
OE to Output Float Delay*	tor	Sector Contraction	0	-	130	ns
VPP Setup Time	typs		2	-	-	μs
V <sub>cc</sub> Setup Time	tvcs		2	-	-	μs
PGM Pulse Width during Initial Program	t pw.	Manual Manual States	0.95	1.0	1.05	ms
PGM Pulse Width during Over Program **	t opw		3.8	-	63	ms
CE Setup Time	lces		2	-	—	μs
Data Valid from OE	toe		-	-	150	ns

Notes) \* tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. \*\* turn is defined as mentioned in flort chart.





#### MODE SELECTION

Pins	CE (20)	0E (22)	PGM (27)	V <sub>PP</sub> (1)	V <sub>cc</sub> (28)	Outputs (11~13, 15~19)	
Read	VIL	VIL	VIB	Vcc	Vcc	Dout	
Stand by	VIN	×	×	Vcc	Vcc	High Z	
Program	$V_{IL}$	×	VIL	Vpp	Vcc	Din	
Program Verify	VIL	VIL	VIN	$V_{PP}$	Vcc	Dout	
Program Inhibit	VIH	×	×	VPP	Vcc	High Z	

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

# HN4827128G-25, HN4827128G-30, HN4827128G-45

#### BABSOLUTE MAXIMUM RATINGS

#### BPROGRAMMANO CPERATION

Item	Symbol	Value	Unit
Operating Temperature Range	Tapr	0 to +70	°C
Storage Temperature Range	Tate	-65 to +125	C
All Input and Output Voltages*	VIN, Vout	-0.3 to +7	Contract V. Voltage
V <sub>PP</sub> Voltage*	V <sub>PP</sub>	-0.3 to +26.5	Charles VV Voltagen
Vcc Voltage*	Vcc	-0.3 to +7	V

READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, Vcc=5V±5%, VPP=Vcc±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	ILI	V <sub>cc</sub> =5.25V, V <sub>IN</sub> =5.25V	-	10.77070	10	μA
Output Leakage Current	ILO	V <sub>cc</sub> =5.25V, V <sub>est</sub> =5.25V/0.4V	-	-	10	μA
VPP Current	I <sub>PP1</sub>	$V_{PP} = V_{CC} + 0.6 V$	-	-	5	mA
Vcc Current (Standby)	Icc1	$\overline{\text{CE}} = V_{IH}$	-	-	35	mA
Vcc Current (Active)	Iccz	$\overline{CE} = \overline{OE} = V_{lL}$	-	60	100	mA
Input Low Voltage	VIL	1	-0.1		0.8	V
Input High Voltage	VIH	Lee .	2.0	1.0	Vcc+1	V
Output Low Voltage	Vol.	$I_{0L}=2.1 \text{mA}$	-		0.45	V
Output High Voltage	Von	$I_{on} = -400 \mu A$	2.4	1.00	1077 0000	V

# • AC CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±5%, Vpp=Vcc±0.6V)

Parameter	Symbol	Test Condition	HN4827	HN4827128G-25		HN4827128G-30		HN4827128G-45	
rarameter	Symbol	Test Condition	min	max	min	max	min	max	Unit
Address to Output Delay	t ACC	$\overline{CE} = \overline{OE} = V_{IL}$	-	250	-	300	- 1	450	ns
CE to Output Delay	tcz	$\overline{\text{OE}} = V_{IL}$	11/末の	250	-	300	11075.1	450	ns
OE to Output Delay	tor	$\overline{CE} = V_{IL}$	1. 1 N	100	-	120	-	150	ns
OE High to Output Float	tor	$\overline{CE} = V_{IL}$	0	85	0	105	0	130	ns
Address to Output Hold	t oH	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	-	0	-	ns

# tor defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

#### SWITCHING CHARACTERISTICS

# **Test Condition**

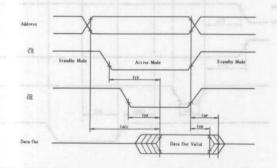
Output Load:

Input Pulse Levels: Input Rise and Fall Time:

	0.8V to 2.2V	
	$\leq 20 \text{ ns}$	
	1 TTL Gate + 100 pF	
g:	Inputs; 1V and 2V	

Reference Level for Measuring Timing:

Outputs; 0.8V and 2.0V



• CAPACITANCE (Ta=25°C, f= 1 MHz)

Parameter Symbol Test Condition mîn Unit typ max Input Capacitance Cin V.,-0V 6 pF 4 **Output** Capacitance Vest-0V Cust \_ 8 12 pF



# HN4827128G-25, HN4827128G-30, HN4827128G-45

#### PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS ( $Ta=25^{\circ}C\pm5^{\circ}C$ ,  $V_{cc}=5V\pm5\%$ ,  $V_{PP}=21V\pm0.5V$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	14	V <sub>IN</sub> =5.25V		2 <del></del>	10	μΑ
Output Low Voltage During Verify	Vol	IoL=2.1mA	* <del></del>	11-	0.45	V
Output High Voltage During Verify	- Vон	$I_{OH} = -400 \mu A$	2.4	-	1.45	V
Vcc Current (Active)	Icca	-W			100	mA
Input Low Level	VIL		-0.1		0.8	V
Input High Level	VIH		2.0		Vcc+1	V
VPP Supply Current	IPP	$\overline{CE} = \overline{PGM} = V_{IL}$	_	14	30	mA

BENGAR MURRAN STUDDERA

# • AC PROGRAMMING CHARACTERISTICS ( $Ta=25^{\circ}C\pm5^{\circ}C$ , $V_{cc}=5V\pm5\%$ , $V_{PP}=21V\pm0.5V$ )

Parameter	Symbol	Test Condition	k	min	typ	max	Unit
Address Setup Time	t <sub>A5</sub>	Prese taski Waltered	- Nel	2		11-4	μs
OE Setup Time	toes	Service and the	and K	2	-		μs
Data Setup Time	t <sub>DS</sub>	10 mm	- Au	2	<u>-4</u> 600	123-11-21	μs
Address Hold Time	t <sub>AH</sub>	1-30-20		0		0.15-691	μs
Data Hold Time	t DH		18	2	-	office in	μs
OE to Output Float Delay	t DF		- 61	0	-	130	ns
V <sub>PP</sub> Setup Time	t vs	Kos = 2, 1 mA		2		1267_26.	μs
PGM Pulse Width During Programming	t pw	1 mm	100	45	50	55	ms
CE Setup Time	tces		1	2		-	μs
Data Valid from OE	tor	NC. REWEYS. R.	a) 0-43	1 22 1	31-211	150	ns

Note : tar defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

# **SWITCHING CHARACTERISTICS**

# **Test Condition**

- Input Pulse Level:
- Input Rise and Fall Time:

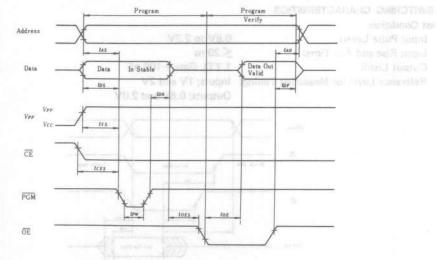
Reference Level for Measuring Timing: Input; 1V and 2V

# Output; 0.8V and 2V

 $\leq$  20 ns

0.8V to 2.2V





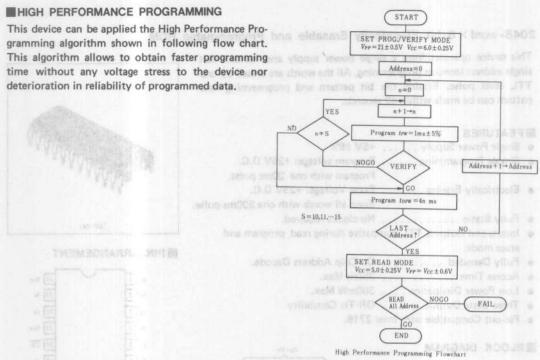
C HITACHI

# ERASE

Erasure of HN4827128 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W-sec/cm<sup>2</sup>.

334

# HN4827128G-25, HN4827128G-30, HN4827128G-45

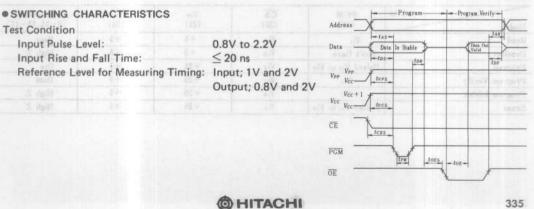


# ● AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=6V±0.25V, VpP=21V±0.5V)

Parameter	Symbol	Test Cond	lition	min	typ	max	Unit
Address Setup Time	tAS	want wear		2	-		μs
OE Setup Time	t oes			2	-		μs
Data Setup Time	tos	and the second second		2	-	-	μs
Address Hold Time	t <sub>AR</sub>		1.5	0	-	+	μs
Data Hold Time	t <sub>DH</sub>	and a second second	1	2	- 1	124	μs
OE to Output Float Delay*	t DF			0	-	130	ns
V <sub>PP</sub> Setup Time	t vps		1.1	2	-		μs
Vcc Setup Time	t vcs	you (within)		2	-	-at	μs
PGM Pulse Width during Initial Program	t <sub>PW</sub>	NAME ADDRESS	- 1 - E	0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	torw			3.8	-	63	ms
CE Setup Time	tces			2	-	100-	μs
Data Valid from OE	tos			-		150	ns

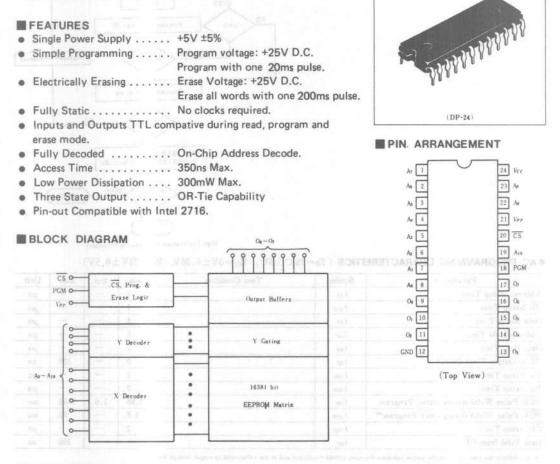
\* tor defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.

\*\* topw is defined as mentioned in flow chart.





single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new pattern can be made within 42 seconds.



# MODE SELECTION

Pins	PGM (18)	CS (20)	V <sub>PP</sub> 80 (21)	(24)	Outputs (8~11,13~17)
Read	VIL	VIL	+5	+5	Dout
Deselect	Don't Care	Vin	+5	+5	High Z
Program	Pulsed Vit to Vin	Vin	+25	+5	Din
Program Verify	Vil	$V_{\ell L}$	+25	+5	Dout
Program Inhibit	VIL	Vin	+25	+5	High Z
Erase	Pulsed Vil to Vin	Vil	+25	+5	High Z

#### **ABSOLUTE MAXIMUM RATINGS**

MUNIARSKAM OPERATION

Item	Symbol	Symbol Rating		
All Input and Output Voltage	VIN+ Voul -	$-0.3$ to $V_{CC}$ +0.3 or $V_{PP}$ +0.3	V	
Vcc Voltage	Vcc	-0.3 to +7.0	V	
VPP Voltage	V <sub>PP</sub>	-0.3 to +28	V	
Operating Temperature Range	Tepr	0 to +70	°C	
Storage Temperature Range	Tue	-55 to +125	*С	

# READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Vcc=5V±5%, Vpp=Vcc±0.6V,\* Ta=0 to +70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	Iu	V <sub>IN</sub> =5.25V	-	-	10	μA
Output Leakage Current	ILO	Vour-5.25V	-	-	10	μA
Vcc Current	Icci	$\overline{\mathrm{CS}} = V_{IH} / V_{IL}$	-	32	50	mA
VPP Current	IPP1	$V_{PP} = 5.85 \text{ V}$	-	4	7	mA
	VIL	1 6-4 1	-0.1	-	0.8	V
Input Voltage	Vin	100	2.0	-		V
0 N. h	VoL	IoL = 1.6 m A	100-	on Reality	0.4	V
Output Voltage	Von	$I_{OH} = -100 \ \mu \text{A}$	2.4	2014 m	10 11 10	V

\* The tolerance of 0.6V allows the use of a driver circuit for switching the  $V_{ee}$  supply pin from  $V_{cc}$  in read to 25V for programming.

# • AC CHARACTERISTICS ( $V_{cc}=5V\pm5\%$ , $V_{PP}=V_{cc}\pm0.6V$ , Ta=0 to $\pm70^{\circ}C$ )

Address

CS

Output

High Z

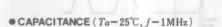
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address to Output Delay	LACC	$PGM = \overline{CS} = V_{IL}$	-	200	350	ns
Chip Select to Output Delay	lco	$PGM = V_{lk}$	-	70	150	ns
Chip Deselect to Output Float	t <sub>DF</sub>	a the same of the second se	0	40	100	ns
Address to Output Hold	ton	$PGM = \overline{CS} = V_{IL}$	10	-	-	ns

# • TEST CONDITION

Input pulse levels: Input rise and fall time: Output load: Reference level for Measuring Timing: 0.8V to 2.0V ≦ 20ns 1TTL Gate + 100 pF Inputs 1V and 1.8V Outputs 0.8V and 2.0V



Selenence level for Manualine Triffing:



Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C.,	$V_{i*} = 0 V$	-	7.5	pF
Output Capacitance	Cent	V <sub>sst</sub> - 0 V	-	15	pF

tco

Data Out Valid

tor

High Z



# HN48016P-

# PROGRAM OPERATION

ABSOLUTE: MALLANER MALE

● DC PROGRAMMING CHARACTERISTICS (Vcc=5V±5%, Vpp=25V±1V, Ta=0 to +70℃)

Parameter	Symbol	Test , Condition	min	typ	max	Unit
Input Leakage Current	Iu	VIN=5.25 V	-		10	μA
Vcc Supply Current	Icc2	1. Pre- 1	-	32	50	mA
VPP Supply Current	IPPZ	dia and a set	-	10	20	mA
0.0	VIL	Tes	-0.1	الاعتبار ال	0.8	V
Input Voltage	VIH		2.0	-	-	V

● AC PROGRAMMING CHARACTERISTICS (Vcc=5V±5%, VPP=25V±1V, Ta=0 to +70℃)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setap Time	tas	VIE SHOW IN THE	2	- 195	100 To.	μs
CS Setup Time	tess	Ve could all	2	-		μs
Data Setup Time	tos	A. REALS	2	-	-	μs
Address Hold Time	tan	And No. of Street, 187	2*	-	- 2019	μs
CS Hold Time	1csH		7	-	-	μs
Data Hold Time	t <sub>DN</sub>		2	-	-	μs
Chip Deselect to Output Float Delay	tor	Val. 1 Auril 1 av	0	40	100	ns
Chip Select to Output Delay	tco	AN 601 - MAR - 23	-	70	150	ns
Program Pulse Width	trw	at all printer of same	15	20	25	ms
Program Pulse Rise Time	t <sub>PRT</sub>		5	-	-	ns
Program Pulse Fall Time	LPFT		5		-	ns
VPP Setup Time	1 tes	LESS Row Keel 0.8	10	हर्ज जात	TO BULL	μs
V <sub>PP</sub> Hold Time	t <sub>PH</sub>		10	-	-	μs
CS to Program Mode Time	lvs		10	-	-	μs
V <sub>PP</sub> Read Mode Time	l vn	14 - 57 - 1621   Syst	10		The Part of	μs

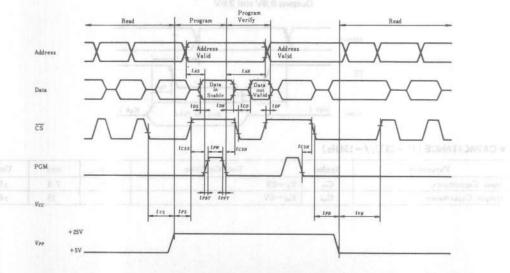
\* If the mode changes from program mode to program verify mode sequentially (in the same address),  $t_{abt}$  must be larger than  $t_{CBt} + t_{CO}$ .

# • TEST CONDITION

**Test Condition** 

Input pulse levels: Input rise and fall time: Reference level for Measuring Timing: 0.8V to 2.0V 20ns (10% to 90%) Input; 1V and 1.8V Output: 0.8V and 2.0V TEST CONNETCH
 Test columnst
 Test columnst
 Test columnst

minus? gain most see boah appears



#### **ERASE OPERATION**

●DC ERASING CHARACTERISTICS (Vcc=5V±5%, Vpp=25V±1V, Ta= 0 to +70℃)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	Iu	VIN=5.25V		-	10	μA
Vcc Supply Current	Icca		-	32	50	mA
VPP Supply Current	Ірра	and provide a		10	20	mA
	VIL	a manual and a second	-0.1		0.8	V
Input Voltage	Vin		2.0	-	-	V

#### ● AC ERASING CHARACTERISTICS (V<sub>cc</sub>-5V±5%, V<sub>PP</sub>-25V±1V, Ta= 0 to +70℃)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
CS Setup Time	tecss		2	-	-	μs
PGM to Output Delay	teo		7	-	-	μs
Erase Pulse Width	ter		190	200	210	ms
Erase Pulse Rise Time	t ert		5	-	-	ns
Erase Pulse Fall Time	t eft		5	-	-	ns
VPP Setup Time	tes	APPN ANA AR	10	122.00	101-1010	μs
VPP Hold Time	ten	estray alando	10	N 994 Vo	S (14106)	μs
Erase Program Time t <sub>EP</sub>	t <sub>EP</sub>	davn, keep the	10	i lon <del>a</del> na c	1.6421.001	μs
Program Enase Time tre	t PE	but patore and	10	1.6 10- 10	2.1 ° - 768	μs

TEST CONDITION

**Test Condition** 

Input pulse levels: Input rise and fall time: Reference level for Measuring Timing: 0.8V to 2.0V 20ns (10% to 90%) Input; 1V and 1.8V Output; 0.8V and 2.0V

#### POWER SUPPLY SEQUENCE PRECAUTIONS

To protect the written data, power supply to the HN48016P should be turned on and off in the following order:

Power On-Off Order and Input Level Limitation for CS and PGM Terminals

Table 1 shows the relationship between the order in which power supply for the HN48016P should be turned on and off and the input levels of the CS and PGM terminals.

- (1) For the 5V Vpp and Vcc, there is no limitation as to the order in which power is turned on and off the state of the input terminals CS and PGM.
- (2) When turning on and off power supply for the 25V Vpp, keep Vcc at between 4.5V and 7V. and PGM at "Low."
- 5V V<sub>CC</sub> while V<sub>PP</sub> equals 25V ± 1V (this being a rare case for the HN48016P), make sure to keep PGM at "Low."

turned on and off.

• Table	Table 1. Power On-Off Order for HN48016P							
Input	Level	Powe	r On-Off					
PGM	CS	5V-VPP-Vcc	25 V- V <sub>PP</sub>					
VIL	VIL	Sed Vil of eaV	Possible only when					
VIL	Vin	Possible	$V_{cc} = 4.5 \sim 7 V^{*2}$					
VIH	VIL	Possible	impossible <sup>#2</sup>					
Vin	VIH	rossible	impossible					

Note 1. If Power for the 25V Vpp were turned on or off while V<sub>CC</sub> = -0.3V to +4.5V, the data holding characteristic would probably deteriorate.

Note 2. If the 25V Vpp were operated to choose a "write" or "erase" mode while PGM = "VIH," contents of ROM would probably change.

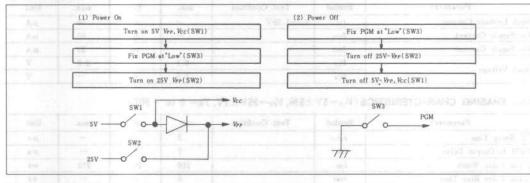
(3) When turning on and off power supply for the

# Fig. 1 shows the timing order in which power is

#### HN48016P-

#### Example of Standard Power Supply Sequence

The following is an example of standard power supply sequence:



**OHITACHI** 

#### Inter-mode Timing

The HN48016P has six operating modes, 5V Vpp readout, non-selected, 25V Vpp write, write check, write inhibit, and erase. To protect the written data, keep the terminal PGM at "Low" for a period of  $10\mu$ s before and after turning the terminal Vpp from 5V to 25V and vice versa.



#### ● Readout → Write → Readout

Before turning the terminal V<sub>PP</sub> to 25V, keep the terminal PGM at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>VS</sub>). After the terminal V<sub>PP</sub> has been turned to 25V, keep the terminal  $\overline{CS}$  at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>PS</sub>). Before turning the terminal V<sub>PP</sub> to 5V, keep the terminal  $\overline{CS}$  at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>PS</sub>). After the terminal V<sub>PP</sub> has been turned to 5V, keep the terminal V<sub>PP</sub> has been turned to 5V, keep the terminal PGM at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>PH</sub>).

# Readout→Erase→Readout

This timing sequence is shown in Fig. 3. After turning the terminal V<sub>PP</sub> to 25V, keep the terminal PGM at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>ES</sub>). Keep the terminal PGM at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>EH</sub>) before turning the terminal V<sub>PP</sub> to 5V, as well.

#### ● Erase → Write → Erase

This timing sequence is shown in Fig. 4. Before turning the terminal  $\overline{CS}$  to "High (write mode)," keep the terminal.

PGM at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>EP</sub>). Before turning from "write" to "erase," keep the terminal  $\overline{CS}$  at "Low" for a period of 10 $\mu$ s minimum (as indicated by t<sub>PE</sub>).

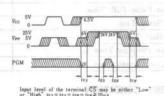
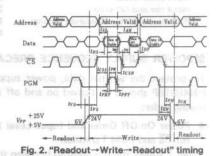
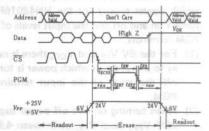
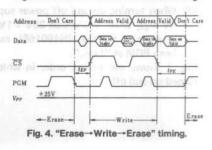


Fig. 1. Power on-off timing sequence.









# HMIO414, HMIO414-1

256+word × 1-bit Fully Decodud Random Access Mamory

The MM10414-ta ECL 10K compatible, 255-word x 1-bit, read write, random eccess memory developed for High speed systems such as seniotor ped and control/buffer storages.

no nacination process uses the Mitamir's low especitance, addisolation method with double metallication.

he HellDelA is e creaulated in onder-Tépin package, compatible rel Faircolid's F10416.

Fully compatible with 10K BCL level

Additional address birned Hitel 64.14c 10ea (a

HR10014-1: 866 (mix)

Linimi and criticise value winty

ania taske gifts servir a

(testinis nago) 10-ismiss or eldenistics sugar a









1

BARSOLUTE MAXIMUM RATINGS

will visite a

**OHITACHI** 

341

# HM10414, HM10414-1

# 256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.) HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



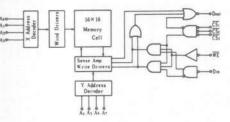
# PIN ARRANGEMENT

# TRUTH TABLE

Input				0	Mode
CS		WE	Din	Output	
any or	ne H	×	×	L	Not Selected
all	L	L	L	L	Write "0"
all	L	L	Н	L	Write "1"
all	L	Н	×	Dout *	Read

\* : Read out non-inverted

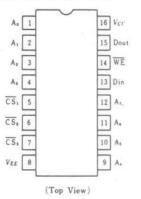
# BLOCK DIAGRAM



# BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Vis	$\pm 0.5$ to $V_{EE}$	V
Output Current	Iver	-30	mA
Storage Temperature	Tua	-65 to +150	°C
Storage Temperature	T., (Bias)*	-55 to +125	°C

\* Under Bias



# ELECTRICAL CHARACTERISTICS

Item	Symbol	Test Conditio	n	min (B)	typ	max (A)	Unit
			0°C	-1000	-	-840	
	Von		+25°C	-960	-	-810	
			+75°C	- 900	patrice and	-720	
Output Voltage	100	$V_{IN} = V_{IHA}$ or $V_{ILB}$	0°C	-1870		-1665	mV
	VoL	The Res	+25°C	-1850	-	-1650	
		12	+75°C	-1830	- 1	-1625	
Har bet	1000		0*C	-1020		-	
	Vouc		+25*C	- 980	-	-	
Output Threshold Voltage			+75°C	-920	-		
		$V_{IN} = V_{IHB}$ or $V_{ILA}$	0°C		- 80	-1645	mV
	Volc	Lines	+25°C	1.000	- 20	-1630	
		A CALL AND A CALL AND A	+75°C	-	-	-1605	
	1000		0°C	-1145	- /	-840	
	Vin	Guaranteed Input Voltage	+25°C	-1105	-	-810	
		High for All Inputs	+75*C	-1045		-720	
Input Voltage			0°C	-1870	-		mV
	Vil	Guaranteed Input Voltage	+25°C	-1850	-	-1475	
		Low for All Inputs	+75°C	-1830	-	-1450	
	Im	$V_{IN} = V_{IHA}$	0 to +75°C	-	-	220	
Input Current		CS		0.5	-	170	μA
	In	$\frac{0.0}{\text{Other}} V_{IN} = V_{FLB}$	0 to +75°C	-50		1.04	
		All Input and Output Open,	+75°C	/-	-130	8 -	
Supply Current	IEE	Test Pin 8	0°C	-180	-140	-	mA

# • DC CHARACTERISTICS ( $V_{ee} = -5.2V$ , $R_L = 50 \Omega$ to -2.0V, $T_a = 0$ to $+75^{\circ}C$ , air flow exceeding 2m/sec)

# • AC CHARACTERISTICS

 $(V_{EE} = -5.2 \text{V} \pm 5\%, Ta = 0 \text{ to } +75^{\circ}\text{C}, \text{air flow exceeding } 2\text{m/sec, see test circuit and waveforms})$ 1. READ MODE

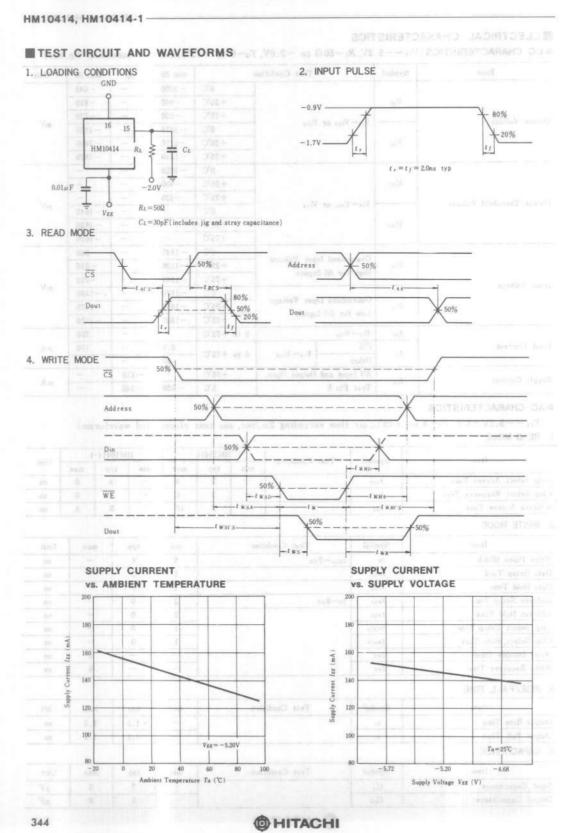
Item	Symbol	Test Condition	HM10414			ŀ	Unit		
Item			min	typ	max	min	typ	max	Unit
Chip Select Access Time	LACR	A State	-	3	6	-	3	6	ns
Chip Select Recovery Time	IRCS	1	21.00	3	6	-	3	6	ns
Address Access Time	IAA	1		7	10		6	8	ns

2. WRITE MODE

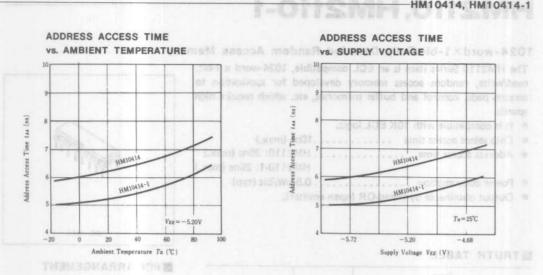
Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	$t_{WSA} = 2 \mathrm{ns}$	6	4	-	ns
Data Setup Time	twso		1	0	100	ns
Data Hold Time	twho	1	1	0	10.12	ns
Address Setup Time	twsa	1w=6ns	2	0	-	ns
Address Hold Time	twna		2	0	-	ns
Chip Select Setup Time	twscs		1	0	-	ns
Chip Select, Hold Time	twncs		1	0	-	ns
Write Disable Time	tws		-	-	5	ns
Write Recovery Time	twa		1		5	ns

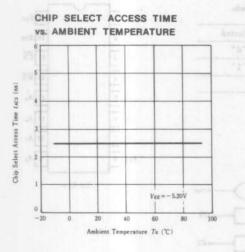
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t,		-	1.5	2.5	ns
Output Fall Time	tj			1.5	2.5	ns
4. CAPACITANCE						
4. CAPACITANCE Item	Symbol	Test Condition	min	typ	max	Unit
	Symbol Cin	Test Condition	1	typ 3	max 5	Unit



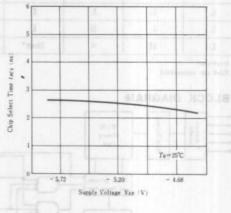


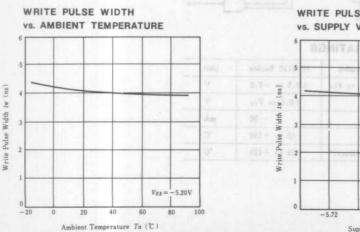
@mina

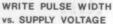


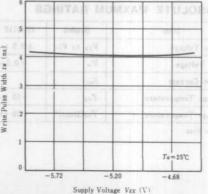












345

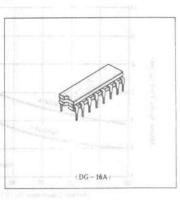
# HM2110, HM2110-1

# 1024-word×1-bit Fully Decoded Random Access Memory

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time .....10ns (max.)

- Output obtainable by Wired-OR (open emitter).



PIN ARRANGEMENT

16 Vcc

15 Din

14 CS

13 WE

12 A,

Dout 1

A<sub>1</sub>

A. 2

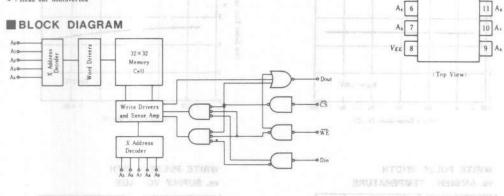
3

5

# TRUTH TABLE

	Input	0	Mode		
CS	WE	Din	Output		
Н	× 32	- 10x 219	0.03 JE	Not Selected	
L	L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout*	Read	

\* : Read out noninverted



# ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	v
Input Voltage	Via	$+0.5$ to $V_{EE}$	v
Output Current	Int	-30	mA
Storage Temperature	Trig	-65 to +150	°C
Storage Temperature	Telg (Bias)*	-55 to +125	°C

346

DC CHARACTERISTIC	$S(V_{EE} =$	$-5.2$ V, $R_L = 50\Omega$ to $-2.0$	V, $Ta=0$ to	+75°C, ai	r flow e	exceeding	2m/sec
Item	Symbol	Test Conditio	n	min(B)	typ	max(A)	Unit
431			0°C	-1000	-	-840	el 1 que
	Von		+25°C	-960	-	-810	
			+75°C	-900	-	-720	
Output Voltage	19.	$V_{IN} = V_{IHA}$ or $V_{ILB}$	0°C	-1870	-	-1665	mV
44	Vol		+25°C	-1850	-	-1650	
34 1			+75°C	-1830	-	-1625	
			0°C	-1020	-	-	
Output Threshold Voltage -	Vonc		+25°C	- 980	ante-	and were	15311
		BELLINE THREE ST	+75°C	-920	-20	03802.3480	ilolo i
		$V_{1N} = V_{1HB}$ or $V_{1LA}$		-	-	-1645	mV
1	Volc	N	+25"C	-	-	-1630	
		America .	+75°C	-	-	-1605	
Steel.			0°C	-1145	-	-840	
and an	VIH	Guaranteed Input Voltage	+25°C	-1105	4	-810	
5 · · · 1/ 1/		High for All Inputs	+75°C	-1045	304	-720	
Input Voltage			0°C	-1870	+	-1490	mV
	VIL.	Guaranteed Input Voltage Low for All Inputs	_ +25"C	-1850	-	-1475	
		Low for All Inputs	+75°C	-1830	-	-1450	a durch
	Іін	$V_{IN} = V_{IHA}$	0 to +75°C	-	-	220	-
Input Current	1.	$\overline{CS}$ $V_{IN} = V_{ILB}$	0 to +75°C	0.5		170	μA
	IIL	Other VIN = VILB	0 10 +750	-50	-	-	
Suindly Connect		All Input and Output Open,	$0 \leq Ta < 25^{\circ}C$	-150	-100	3000	COLOR
Supply Current	IEE	Test Pin 8	$T_a \ge 25^{\circ}C$	-125	- 90	1	mA

# **•**AC CHARACTERISTICS

 $(V_{EE} = -5.2V \pm 5\%, Ta = 0$  to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms) 1. READ MODE

Test Pin 8

Item	Symbol	Test Condition	HM2110				Date		
Item			min	typ	max	min	typ	max	Unit
Chip Select Access Time	lacs		-	7	10	-	7	10	ns
Chip Select Recovery Time	tres			7	10	/-	7	10	ns
Address Access Time	E.A.A		-	20	35	-	15	25	ns

Ta≥25°C

-125

-90

2. WRITE MODE

Item	Symbol	Test Condition		HM2110			HM2110 ~1			
Item	Symbol		min	typ	max	min	typ	max	Unit	
Write Pulse Width	t w	twsa=8ns	25	-	-	25	-	-	ns	
Data Setup Time	twsp		5	-		5	-	-	ns	
Data Hold Time	t wHD	- wat- a	5	-	-	5	-	1	ns	
Address Setup Time	twax	tw=25ns	8		-	8	-	-	ns	
Address Hold Time	l wHA	- A A	2	-		2	-	-	ns	
Chip Select Setup Time	twscs	1.12.25	5	-	-	5	-	-	ns	
Chip Select Hold Time	twncs	144 miles	5	-	-	5	-	-	ns	
Write Disable Time	tws		-	-	10		-	10	ns	
Write Recovery Time	twe		-	-	10	-	-	10	ns	



# HM2110, HM2110-1-

3. RISE/FALL TIME

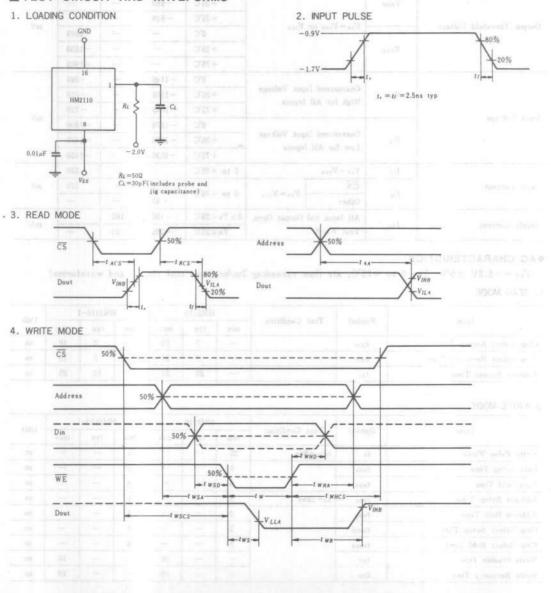
ELECTRICAL CRARACTERIET

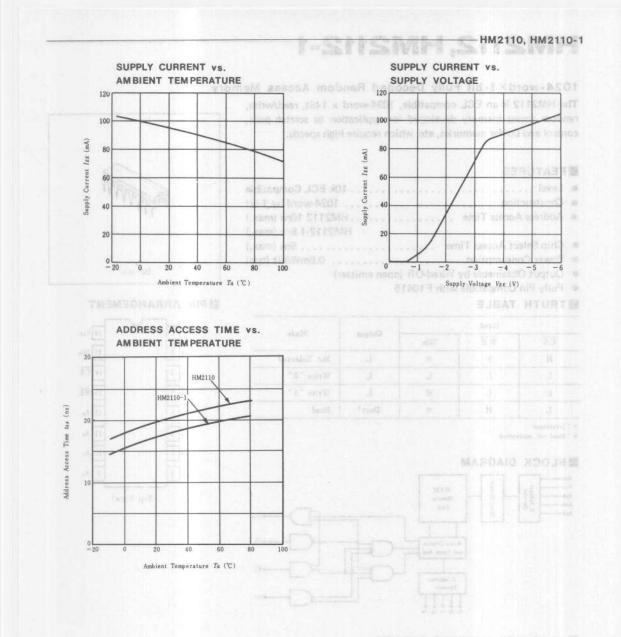
Item	Symbol	- Test Condition	mîn	typ 200	max	Unit
Output Rise Time	. t.	Tett Caudition	-	5	-	ns
Output Fall Time	11			5	_	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	(2t -	-	4	5	pF
Output Capacitance	Cent	(BY )	-	7	8	pF

# TEST CIRCUIT AND WAVEFORMS





#### WARSOLUTE MAXHIUM RATINGS

	Trac (Black	

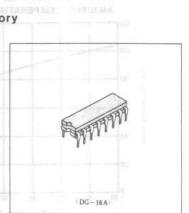
w. thefire first

# HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- FEATURES
- Level ..... ..... 10k ECL Compatible
- Construction ...... 1024-word by 1-bit
- HM2112-1 8ns (max.)
- Power Consumption ...... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

# TRUTH TABLE



# PIN ARRANGEMENT

A. 6

A. 7

16 Ver 15 Din

14 CS

13 WE 12 A,

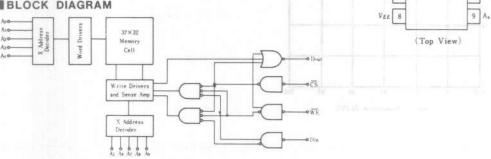
11 A.

10 A.

D D	Mode	0		Input	
SAUTARS	Mode	Output	Din	WE	CS
1	Not Selected	L	×	×	Н
1.11000	Write "0"	L	L	L	L
	Write "1"	L	Н	L	L
	Read	Dout*	×	Н	L

× : Irrelevant \* : Read out noniverted





# **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	HM2112	Unit
Supply Voltage	$V_{EE}$ to $V_{CC}$	$\pm 0.5$ to $-7.0$	V
Input Voltage	V.,	$+0.5$ to $V_{EE}$	V
Output Current	I.m.	- 30	mA
Storage Temperature	T <sub>*te</sub>	-65 to $+150$	*C
Storage Temperature	Tate (Bias)*	-55 to +125	°C

\* Under Bias

# ELECTRICAL CHARACTERISTICS

 $(V_{EE} = -5.2V, R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+75^{\circ}C$ , air flow exceeding 2m/sec)

DC CHARACTERISTIC	S							
Item	Symbol	0.8	Test Condition	1	min(B)	typ	max(A)	Unit
				0*C	-1000	-	-840	
	Von			+25°C	-960	-	-810	
Tield near Unit		dia	Continos	+75°C	-900	-	-720	
Output Voltage	1	$V_{IN} = V_{IHA}  0$	or VILB	0*C	-1870	-	-1665	mV
74 8	VOL	8		+25°C	-1850	-	-1650	
				+75°C	-1830	-	-1625	
				0°C	-1020	24 21	10 HI 2	14-21 2
	Vonc	ALENT POLLE		+25°C	- 980	40	00802-3	
				+75°C	-920	-	-	
Output Threshold Voltage		$V_{IN} = V_{IHB}$ or $V_{ILA}$	0°C	-	-	-1645	mV	
111 4	Volc	Themes		+25°C	-		-1630	-
		-		+75°C	-	-	-1605	
				0°C	-1145	-	-840	
	VIH	Guaranteed High for Al	Input Voltage	+25°C	-1105	-	-810	
1		righ for Al	II Inputs	+75°C	-1045	-	-720	mV
Input Voltage				0°C	-1870	-	-1490	mv
	VIL	Guaranteed Low for Al	Input Voltage	+25*C	-1850	-	-1475	
		LOW IOF AI	i inputs	+75°C	-1830	- 4.1	-1450	
	In	$V_{IN} = V_{INA}$	Thereits	0 to +75°C	and a start of the start of the	-	220	
Input Current		CS	$V_{IN} = V_{ILB}$	0 to +75°C	0.5	-	170	μA
	IIL	Other	VIN - VILB	0 to +75C	-50	-	-	
Sunda Connect	Ιεε	All Input an	nd Output Open,	<i>Ta</i> =0*C	-200	-	-	mA
Supply Current	ILE	Test Pin 8		Ta=75°C	-170	-	-	mA

# **AC CHARACTERISTICS**

 $(V_{EE} = -5.2V \pm 5\%, Ta = 0$  to  $\pm 75^{\circ}$ C, air flow exceeding 2m/sec, see test circuit and waveforms) 1. READ MODE

Item	Symbol	Test Condition	- 1	HM2112-	1	1	HM2112	-	Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs		1	3	5	1	3	5	ns
Chip Select Recovery Time	tres		1	3	5	1	3	5	ns
Address Access Time	taa		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Same	Test Condition	- second	HM2112-	1		HM2112		Unit
Item	Symbol	lest Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	tw	twsA=3ns	6	2		6	2		ns
Data Setup Time	twsp	appel and a second	1	0	-	1	0		ns
Data Hold Time	I WHD		1	0		1	0	-	ns
Address Setup Time	lwsa	$t_w = 6 ns$	3	0	-	3	0	-	ns
Address Hold Time	t with A	/	2	0	-	2	0	-	ns
Chip Select Setup Time	twscs		1	0	-	1	0	-	ns
Chip Select Hold Time	twncs		1	0	-	1	0	-	ns
Write Disable Time	tws		1	3	5	1	3	5	ns
Write Recovery Time	t wn		1	3	5	1	3	5	ns

# HM2112, HM2112-1-

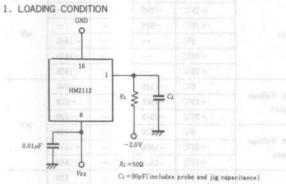
3. RISE/FALL TIME

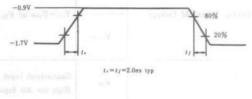
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.		0.8	1.5	2.5	ns
Output Fall Time	11		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin		1	3	5	pF
Output Capacitance	Cast		3	5	8	pF

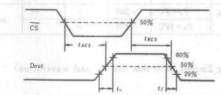
# **TEST CIRCUIT AND WAVEFORMS**

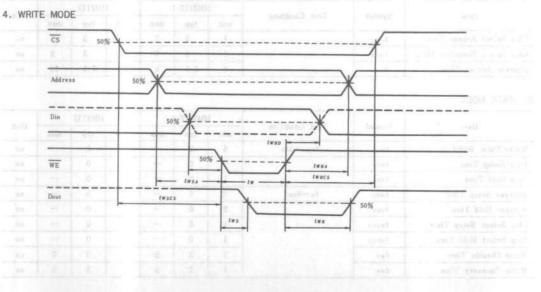




2. INPUT PULSE

3. READ MODE





**HITACHI** 

Address

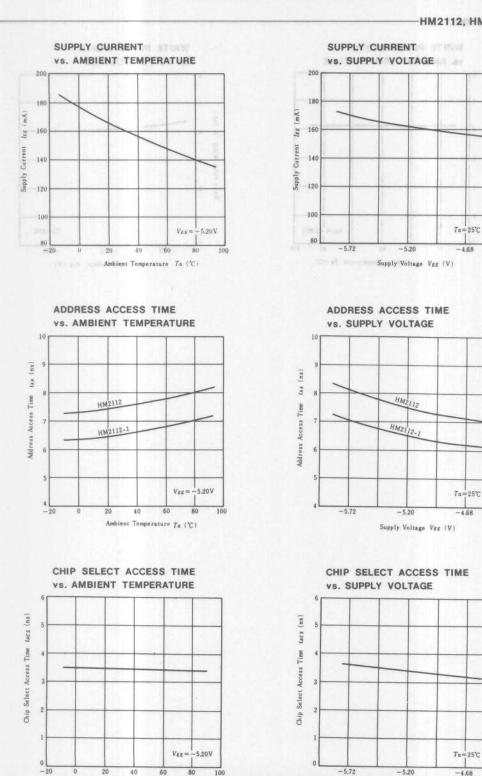
Dout

50%

tan

50%





**HITACHI** 

0

40

60

Ambient Temperature Ta (°C)

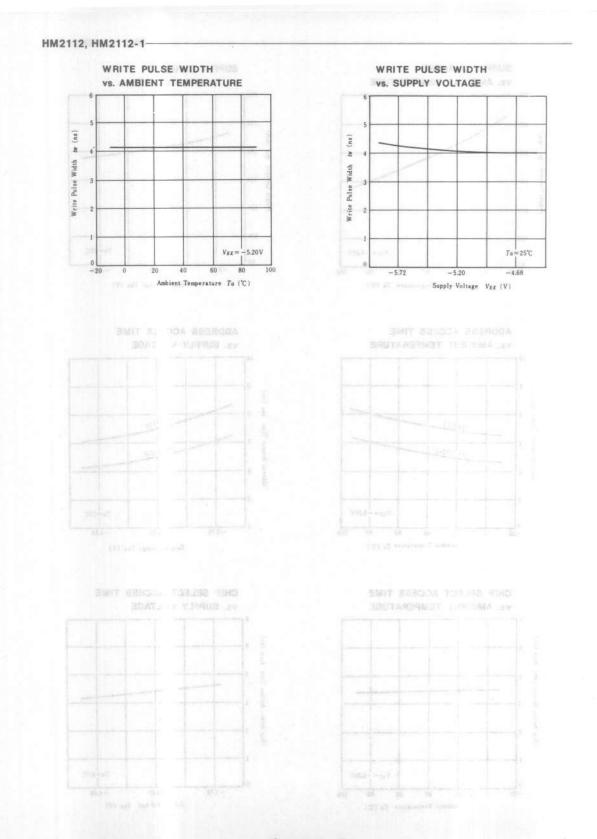
80

100

353

-4.68

Supply Voltage  $V_{EE}$  (V)



354

# HM10422

256-word × 4-bit Fully Decoded Random Access Memory The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

- FEATURES
- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

# TRUTH TABLE

# : Read out noninvert

BLOCK DIAGRAM

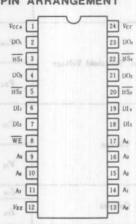
Input			0	
BS		Output	Mode	
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

Ai

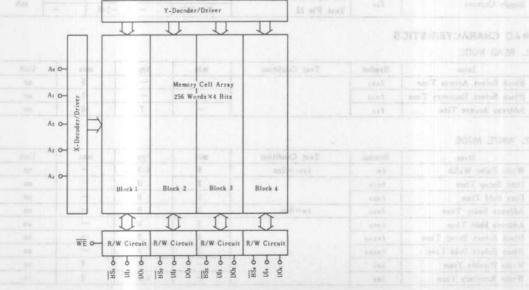
0

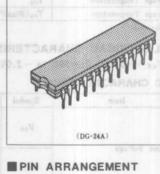
A

1.



(Top View)





# 222000MM

# HM10422-

# **MABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Via	+0.5 to Ver	V
Output Current	Int	-30	mA
Storage Temperature	Tele	-65 to +150	°C
Storage Temperature	T <sub>sta</sub> (Bias)*	-55 to +125	°C

2.50 World X 4: 501 Fully December 2 The Hittbld22 is ECL TDK comparible, 265 miniorm sectors memory developed for bit inmitch pads and control buffer storages. Four notive Low Bloch, wheet lines are proodependently.

\* Under Bias

# ELECTRICAL CHARACTERISTICS

The Devication proves is the Hilashi's in

 $(V_{EE} = -5.2V, R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+75^{\circ}C$ , air flow exceeding 2m/sec)

# ODC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	Von		0°C	-1000		-840	mV
			+25*C	-960		-810	
		$V_{IN} = V_{INA}$	+75°C	-900	-	-720	
	Vol	OT VILB	0°C	-1870	101-10	-1665	
			+25°C	-1850	0.000	-1650	
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			+75°C	-1830	1910-01	-1625	
	1089		0°C	-1020	nt 1 - 200	17 11 CH 11 12 CT	Chinkers and
00 10	Vonc	13	+25°C	-980	W 90 <u>3</u> 17	editado a	
	356		+75°C	-920	-		
Output Threshold Voltage	1.00	- VIN-VINB OF VILA	0°C	-		-1645	mV
	Volc		+25*C	-		-1630	
李团		Made	+75°C		-	-1605	
10 m	VIH		0°C	-1145	-	-840	21
100 (10)		Guaranteed Input Voltage	+25*C	-1105	-	-810	
THE REAL		High for All Inputs	+75°C	-1045	-	-720	
nput Voltage	VIL	1 83671	0°C	-1870		-1490	mV
		Guaranteed Input Voltage	+25*C	-1850	-	-1475	
		Low for All Inputs	+75°C	-1830	-	-1450	
A 11	Im	$V_{IN} = V_{IHA}$	0 to +75°C	-	-	220	
nput Current	IIL	BS		0.5	MOTO:	170	μA
		$V_{IN} = V_{ILB}$	0 to +75°C	-50	-	-	
(HVA-102)		All Input and Output Open,	Ta = 0°C	-200	-160		
Supply Current	Ιεε	Test Pin 12	Ta=75°C	e —	-145		mA

# **AC CHARACTERISTICS**

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	LABS		and the should	—	5	ns
Block Select Recovery Time	tras		and the second second	-	5	ns
Address Access Time	tax		-	7	10	ns

# 2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	twsa=2ns	6	4.5	<u> </u>	ns
Data Setup Time	twsp	Y-date 1	2	0		ns
Data Hold Time	t who		2	0	-	ns
Address Setup Time	twsx	$t_w = 6 ns$	2	0		ns
Address Hold Time	t wHA		2	0	_	ns
Block Select Setup Time	twsbs	and the second second second	2	0		ns
Block Select Hold Time	twnus		2	0	-	ns
Write Disable Time	tws	0000	6 c 6 . c	2 4 0	5	ns
Write Recovery Time	tws	13 2 2 3	2 IL 2 1	4.5	9	ns

**OHITACHI** 

HM10422

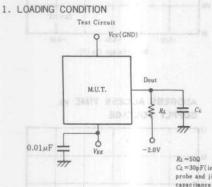
3. RISE/FALL TIME

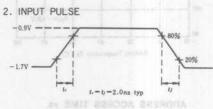
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.	18	- 1	2	-	ns
Output Fall Time	t/		-	2	-	ns

4. CAPACITANCE

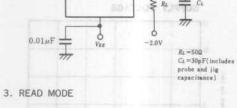
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C in		-	4	-	pF
Output Capacitance	Cent		-	7		pF

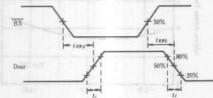
# TEST CIRCUIT AND WAVEFORMS

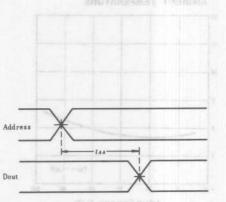




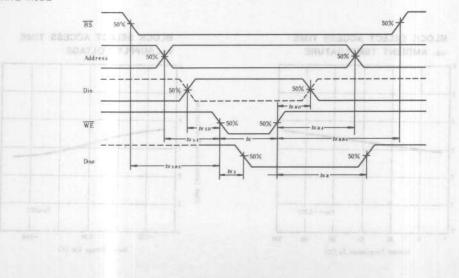






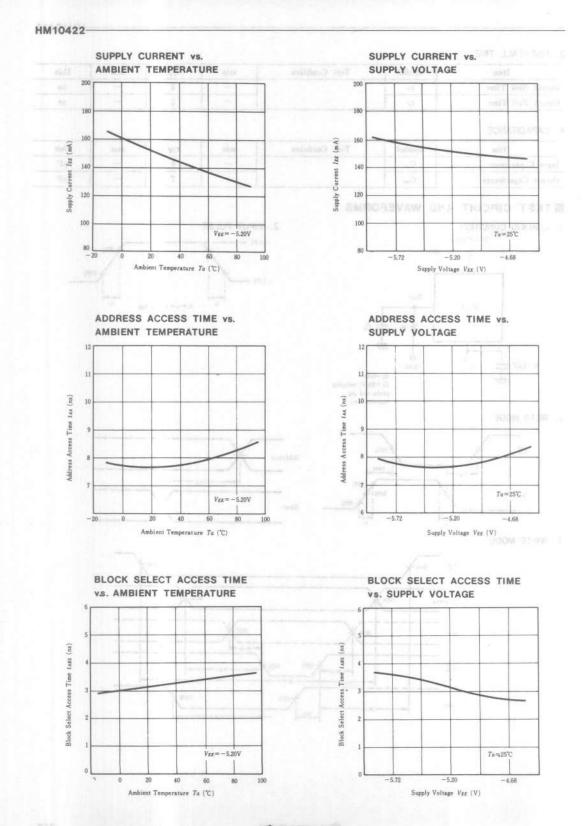


4. WRITE MODE



**HITACHI** 

357

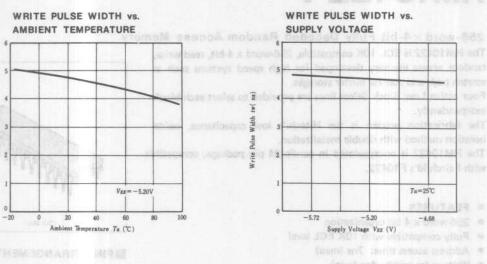


358

-HM10422

indepe

S out

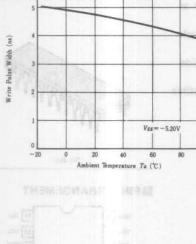


· Write pulse width: 4as finin)

" Lind				











## HM10422-7

#### RAA REAL AND ALL AND A

## 256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

FEATURES

3

- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

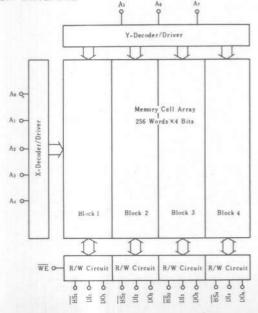
## TRUTH TABLE

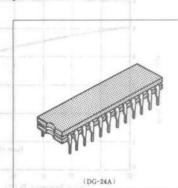
	Input		0	Mode
BS	WE	Din		
Н	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant

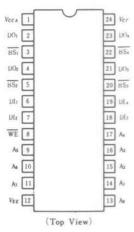
\* : Read out noninvert

## BLOCK DIAGRAM





#### PIN ARRANGEMENT





**OHITACHI** 

### BABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
VEE to Vcc	+0.5 to -7.0	V
Via	$+0.5$ to $V_{EE}$	V
Int	- 30	mA
Tetg.	-65 to +150	°C
Tete (Bias)*	-55 to +125	°C
	VEE         to         Vcc           Via         Iout         Tail         Tail	$V_{EE}$ to $V_{cc}$ +0.5 to -7.0 $V_{is}$ +0.5 to $V_{EE}$ $I_{ret}$ -30 $\mathcal{T}_{sig}$ -65 to +150

\* Under Bias

## ELECTRICAL CHARACTERISTICS

 $(V_{EE} = -5.2V, R_L = 50\Omega \text{ to } -2.0V, Ta = 0 \text{ to } +75^{\circ}C, \text{ air flow exceeding } 2m/sec)$ 

#### OC CHARACTERISTICS

SMADEVAN GRA TIUGALS TEATH

Item	Symbol	Test Con	ndition	min(B)	typ	max(A)	Unit
and the second se			0°C	-1000	-	-840	
	Von		+25°C	-960	- <del>-</del> -	-810	
/		$V_{IN} = V_{INA}$	+75°C	-900	-	-720	
Output Voltage		or VILB	0°C	-1870	-	-1665	mV
44	Vol	+25°C	-1850	-	-1650		
	1 11-1		+75°C	-1830	-	-1625	
			0°C	-1020	-	-	
Output Threshold Voltage	Vonc		+25°C	-980	-		mV
			+75°C	-920	-	-	
		$V_{IN} = V_{IHB}$ or $V_{ILA}$	0°C	9	-0	-1645	
	Volc		+25°C	-	-	-1630	
	11		+75°C	-	-	-1605	
			0°C	-1145	-	-840	mV
	VIN	Guaranteed Input Volt	age + 25°C	-1105	-	-810	
	1.52	High for All Inputs	+75*C	-1045	-	-720	
Input Voltage		121/12	0°C	-1870	-	-1490	
	VIL	Guaranteed Input Volt	age +25°C	-1850	-	-1475	
		Low for All Inputs	+75°C	-1830	-	-1450	
	Im	VIN-VIHA	0 to +75°C	-	31-	220	
Input Current	1	BS	a Janto	0.5	- 11	170	μA
	IIL	$V_{IN} = V_{IN}$	0 to +75°C	-50	-		
	1	All Input and Output (	Open, Ta=0°C	-240	-200	-	
Supply Current	IEE	Test Pin 12	$Ta = 75^{\circ}C$	-	-180	-	mA

### **AC CHARACTERISTICS**

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	LABS			-	5	ns
Block Select Recovery Time	tres				5	ns
Address Access Time	LAA	A.	Net and Alexandre	4	7	ns

#### 2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	twsa,=2ns	4	3	-	ns
Data Setup Time	twsp	- marker of a	- 1 -		-	ns
Data Hold Time	t wHD		1		-	ns
Address Setup Time	twsa	$t_w = 4  \mathrm{ns}$	2		-	ns
Address Hold Time	t wira		1		—	ns
Block Select Setup Time	twsss		1		-	ns
Block Select Hold Time	twnbs		1		-	ns
Write Disable Time	tws		-	3	5	ns
Write Recovery Time	t wR		-	3	5	ns



	HM	104	22-	7
--	----	-----	-----	---

Output Capacitance

3. RISE/FALL TIME Item Symbol Test Condition min typ max -\_ Output Rise Time t. 2 Output Fall Time -2 \_ ti 4. CAPACITANCE Item Symbol Test Condition min typ max Input Capacitance Cin -3 -

-

5

\_

Unit

ns

ns

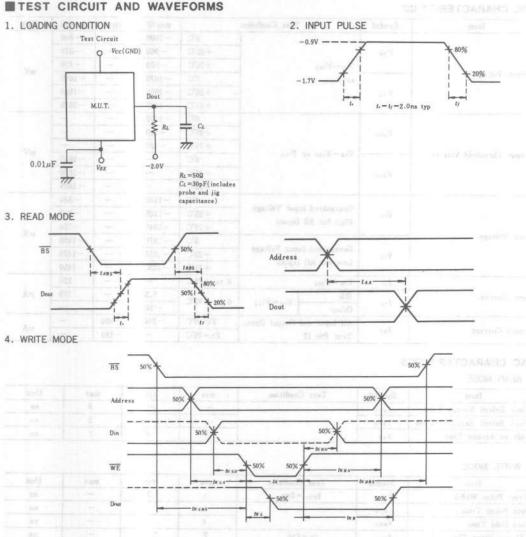
Unit

pF

pF

TEST CIRCUIT AND WAVEFORMS	T CIRCUIT AND WAVEF	ORMS	
----------------------------	---------------------	------	--

Cast



**HITACHI** 

## HM10470, HM10470-1, HM10470F

4096-word x 1-bit Fully Decoded Random Access Memory The HM10470/F is ECL 10K compatible, 4096-words x 1-bit, read write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

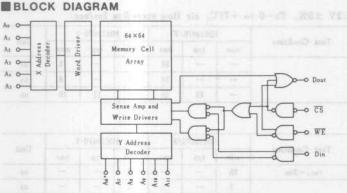
The HM10470/F is encapsulated in cerdip-18 pin and Flat-18 pin package, compatible with Fairchild's F10470.

- FEATURES
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10740/F 25ns (max) HM10470-1 15ns (max)
   Write pulse width: HM10470/F 25ns (min) HM10470-1 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

## TRUTH TABLE

	Input		0	Mode		
CS	WE Din		WE Din		Output	Mode
Н	×	×	Cont - Loo o	Not Selected		
L	L	L	L	Write "0"		
L	L	Н	-0-L	Write "1"		
L	Н	×	Dout*	Read		

Notes) × : Irrelevant \* : Read Out Noninvert

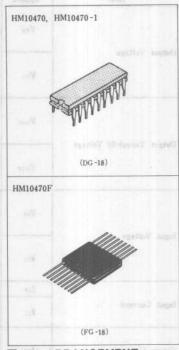


#### ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to $-7.0$	V
Input Voltage	Vie	$+0.5$ to $V_{EE}$	V
Output Current	Inst	-30	mA
Storage Temperature	Tala	-65 to +150	<b>'</b> C
Storage Temperature	Tete (Bias)*	-55 to +125	°C

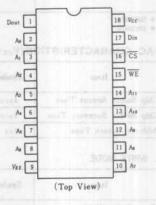
C HITACHI

\* Under Bias



## PIN ARRANGEMENT

------





# HM10470, HM10470-1, HM10470F-

## **TEST CIRCUIT AND WAVEFORMS**

•DC CHARACTERISTICS (V<sub>EE</sub> = -5.2V, R<sub>L</sub>=50Ω to -2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Provinger, of working

104701

18

Item	Symbol	Test Condition	ettole, 4008	min(B)	typ	max(A)	Unit	
5-0390	0.01000	speed systems such	0°C	-1000	0.015-00-00	-840	toni stri	
	Von	1.000	+25°C	- 960	Jonnag	-810	robutos	
		eitance, oxida isola-	+75°C	-900	1.15.304200	-720	ni fubria	
Output Voltage		$V_{IN} = V_{IHA}$ or $V_{ILB}$	0°C	-1870	nc, 6)d <u></u> 81	-1665	mV	
	Vol	nig 81-selfi bris nig	+25°C	- 1850	ideou=s	-1650	n Hult	
			+75°C	-1830	4 (UN 9 <u>1</u> 9)	-1625	1.200-2	
A WORSE			0°C	-1020	-	-		
	Vonc		+25°C	-980	-	83760	TABS	
		VIN = VINB OF VILA		- 920	hayno <del>H</del> id	1 x true	mV	
Output Threshold Voltage				JOH HOL	( Thesi	-1645		
	Volc	(2115h) 21	+25°C	MH =	1 33 <del>#</del> 8	-1630	a-567.	
	1.04.04.7E2	(x6m) at	+75°C	- HIM	-	- 1605		
		(nim) a	0°C	-1145	)	-840	atove	
		Guaranteed Input Voltage	+25°C	-1105	-	-810		
		High for All Inputs	+75°C	-1045	triolitical	-720	-V	
Input Voltage			0°C	-1870	W V 20	-1490	mV	
	VIL	Guaranteed Input Voltage	+25°C	-1850	-	-1475		
		Low for All Inputs	+75*C	-1830		-1450	1000	
and the second	Іли	VIN=VINA	0 to +75°C	-		220	-	
Input Current		CS	A	0.5		170	μA	
	In	$V_{IN} = V_{ILB}$	0 to +75°C	-50				
00-00		10 H H H H H H H H H H H H H H H H H H H		-200*	-160*			
Supply Current	Ise	All Input and Output Open,	<i>Ta</i> = 0°C	-280**	-200**	+	mA	
Calify Calify A 3 9 N A 1		Test Pin 9	Ta=75°C	-	-145			

\*\* HM10470-1

and set work in w

AC CH	<b>IARACTERISTICS</b>	$V_{EE} = -5.2 \mathrm{V}$	±5%,	Ta=0 to	+75°C,	air	flow exceeding 2m/sec)	
-------	-----------------------	----------------------------	------	---------	--------	-----	------------------------	--

Tre III Item	HM10470/F		)/F	HM10470-1			Unit			
	Symbol Test Condition	min	typ	max	min	typ	max	Unit		
Chip Select Access Time	tACS	unt son all	-	-	10	10112	-	8	n5	
Chip Select Recovery Time	tres			- •		10	-	-	8	ns
Address Access Time	- 2		-	15	25	-	12	15	ns	

2. WRITE MODE

364

Terrer	Symbol	Test Condition		HM10470	)/F	ecces yH	M10470-	1	11.24
Item a V apr	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	Iwsa=3ns	25	-	- 0	15	-	-	ns
Data Setup Time	twsp		2	-	2-11	2	-	-	ns
Data Hold Time	t wn D		2	150		2	-		ns
Address Setup Time	twsa	tw=tw min	3	-	120	3	-	-	ns
Address Hold Time	t wha	1964	2	-	1 <u>eris</u> tati	2		1997	ns
Chip Select Setup Time	twscs		2	10 m	107-51	2		4.547	ns
Chip Select Hold Time	twncs	V I	2	-	-	2	-		ns
Write Disable Time	tws		-		10	-	-	8	ns
Write Recovery Time	twn		-	-	10	-1-		8	ns

**OHITACHI** 

-HM10470, HM10470-1, HM10470F

3. RISE/FALL TIME THE AND THE AUT

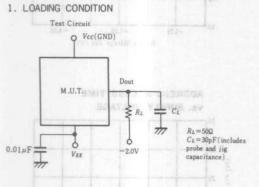
PPLY CURRENT VS.

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.		-	2	-	ns
Output Fall Time	1/		-	2	-	ns

#### 4. CAPACITANCE

	Item	Symbol	Test Condition	min	typ	max	Unit
Input	Capacitance	C.s		-	3		pF
Outpu	t Capacitance	Cest		-	5	-	pF



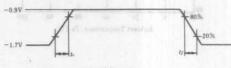


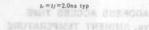
-tacs-

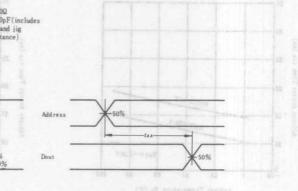
50%

-lacs-







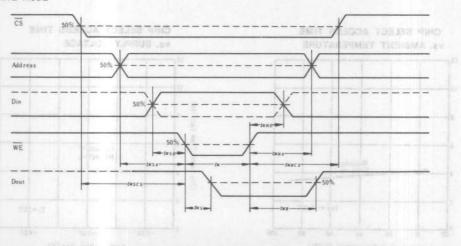


4. WRITE MODE

3. READ MODE

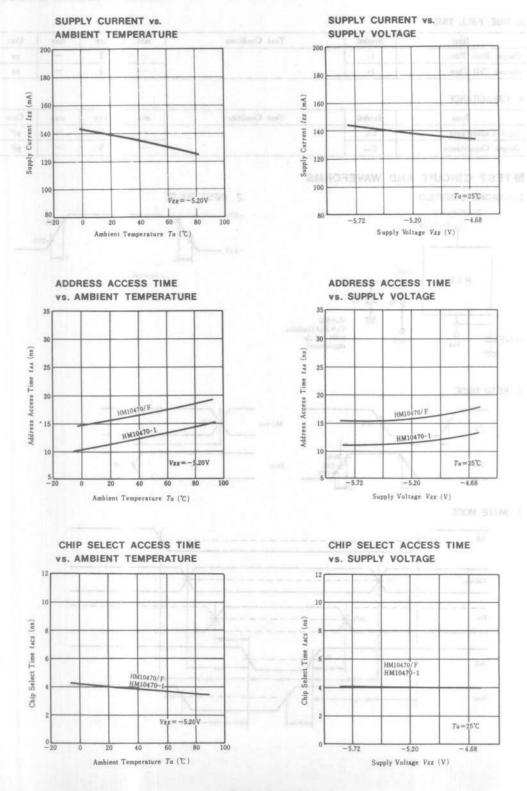
cs

Dout

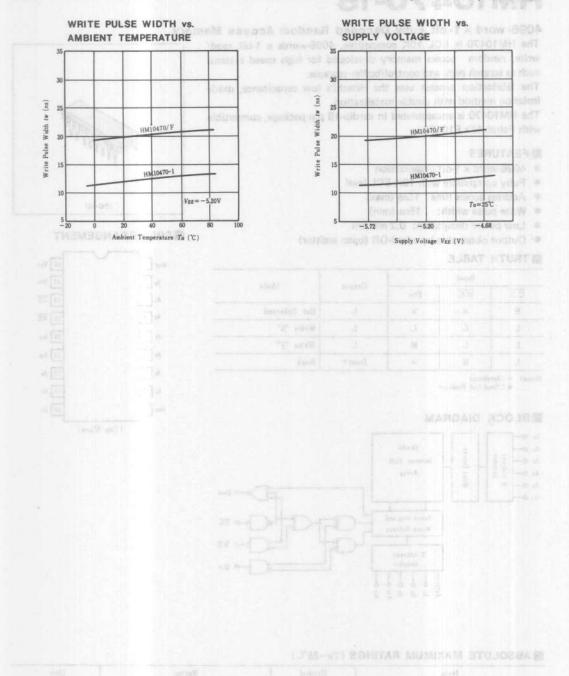


**HITACHI** 

#### HM10470, HM10470-1, HM10470F



**OHITACHI** 



**HITACHI** 

## HM10470-15

 4096-word × 1-bit Fully Decoded Random Access Memory

 The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/

 write, random access memory developed for high speed systems

 such as scratch pads and control/buffer storages.

 The fabrication process uses the Hitachi's low capacitance, oxide

isolation method with double metalization. The HM10470 is encapsulated in cerdip-18 pin package, compatible

with Fairchild's F10470.

## **FEATURES**

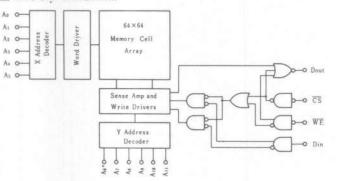
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 15ns (max)
- Write pulse width: 15ns (min)
- Low power dissipation: 0.2 mW/bit
- Output obtainable by wired-OR (open emitter)

## TRUTH TABLE

	Input		Output	Mode	
CS	WE	Din	Output		
Н	×	×	L	Not Selected	
L	L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout *	Read	

Notes) × : Irrelevant \* : Read Out Nonivert

## BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS (Ta-25°C)

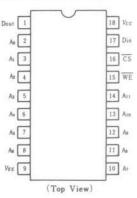
Symbol	Rating	Unit
VEE to Vcc	+0.5 to $-7.0$	V
Vix	$+0.5$ to $V_{EE}$	V
Iest	-30	mA
Tate	-65 to $+150$	°C
Trig (Bias)=	-55 to +125	°C
	VEE to Vcc           Vis           Irst           Tste	$V_{EE}$ to $V_{cc}$ $+0.5$ to $-7.0$ $V_{ix}$ $+0.5$ to $V_{EE}$ $I_{rat}$ $-30$ $T_{ste}$ $-65$ to $+150$

\* Under Bias

368

## (DG-18)

### PIN ARRANGEMENT



() HITACHI

-HM10470-15

1007 11005 SOL

	Item		Symbol	Test Condition	1	min (B)	typ	max(A)	Unit
2.0	1200				0°C	-1000		-840	s a number
			Von		+25°C	-960	-	-810	
					+75°C	-900	-	-720	
Output V	oltage		win .	$V_{IN} = V_{INA}$ or $V_{ILB}$	0°C	-1870	-	-1665	mV
			Vol		+25°C	-1850		-1650	and the
			- 1		+75°C	-1830	-	-1625	stgar Cs
					0°C	-1020	-	-	
Output Threshold Voltage		Vonc		+25°C	- 980	nav Ti	and the	TEBT	
			2. INPOT PULS	+75°C	-920	RU	10407.9	mV	
			VIN=VINB OF VILA	0°C	-	-	-1645		
		Volc	1	+25°C	-	01410	-1630		
				1 August	+75°C	-	-	-1605	-
	hand			deed	0°C	-1145	+	-840	
			Vin	Guaranteed Input Voltage High for All Inputs	+25*C	-1105	-	-810	mV
. 17				riign for All Inputs	+75°C	-1045	-	-720	
nput Vo	Itage				0°C	-1870	+	-1490	
			VIL	Guaranteed Input Voltage Low for All Inputs	+25°C	-1850	-	-1475	
			Low for All inputs	+75°C	-1830		-1450		
			Im	$V_{IN} = V_{IHA}$	0 to +75°C	-	-	220	de la
nput Cu	rrent			$\overline{CS}$ $V_{IN} = V_{ILB}$	0	0.5	-	170	μA
			IIL	Other VIN = VILB	0 to +75°C	-50	-	-	
				All Input and Output Open,	<i>Ta</i> =0°C	-200	-160	-	
Supply Current		IEE	Test Pin 12	Ta-75°C		-145	1-	mA	

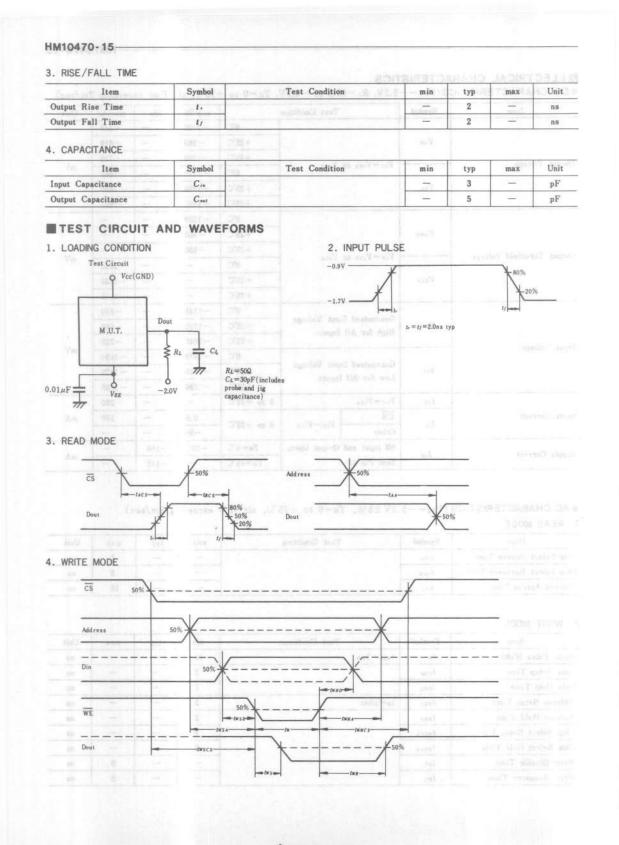
## • AC CHARACTERISTICS ( $V_{EE} = -5.2 \text{V} \pm 5\%$ , Ta = 0 to +75 °C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs		-	-	8	ns
Chip Select Recovery Time	tres		-	-	8	ns
Address Access Time	EAA				15	ns

2. WRITE MODE

L. WHITE MODE		You and a second second second			u. step	1.1.1
Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	twsx=3ns	15 -			ns
Data Setup Time	twso	*	2	-	-	ns
Data Hold Time	twHD		2	-	-	ns
Address Setup Time	LWSA	tw=15ns	3	-	-	ns
Address Hold Time	₿ <sub>₩HA</sub>	harmon francisco	2	-	-	ns
Chip Select Setup Time	twscs		2	-	-	ns
Chip Select Hold Time	twhcs	ale and a second second	2		-	ns
Write Disable Time	tws		-	-	8	ns
Write Recovery Time	twn	hamman particul	-	-	8	ns



370

**OHITACHI** 

## HM2142

4096-words × 1-bit Very High Speed Random Access Memory

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.

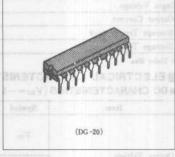
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM2142 is encapsulated in cerdip-20 pin package.

## **FEATURES**

- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

## TRUTH TABLE



## PIN ARRANGEMENT

	Input		0	-	Mode		-		
CS	WE	Din	Output	-	Mode		NC 1	20 Vec.4	
Н	×	×	L	Ne	ot Selected		Dout 2	19 Vcc	
L	L	L	L	W	rīte "0"		As 3	18 Din	
L	L	Н	L	W	rite "1"		At 4	17 CS	
L	Н	×	Dout •	R	ead		Az 5	16 WE	
Notes) × : Irr * : Re	relevant ad Out Nonive	ert			Ourseineren Input Falsage Rick for All Inputs		As 6	15 A11	
							A+ 7	14 Au	
BLOCK		AM					As 8	13 As	
A= 0-		-	-162				A6 9	12 Aa	
A1 0-		64 × 64	1.17.81+				Vee 10	11 A7	
V V V	Word Driver	Memory Cell Array	- Jata wa				(T	Top View)	
As 0 ×	3	-940	1 2 2 - 13 V		Dout Dout	n1			
		Sense Amp an Write Driver		7				AC CHARACTERI	
				+	La poo WE				
		Y Address Decoder			Din Din				
	ð. 1	TIT							
		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0						Chip Soleer Responses 7	
1. 100-1			<		+				

BOOM STIRW 3

			Barn Stald Than

**OHITACHI** 

#### HM2142-

5. 35 J 5. 1971 / 7

ABSOLUTE MAXIMUM RATING	$(Ta=25^{\circ}C)$	
-------------------------	--------------------	--

Item	Symbol	Rating	Unit	
Supply Voltage	VEE to Vcc	+0.5 to $-7.0$	V	
Input Voltage	Via	$+0.5$ to $V_{EE}$	V	
Output Current	Iout	-30	mA	
Storage Temperature	Tele	-65 to $+150$	°C	
Storage Temperature	Trig (Bias)*	-55 to +125	D.	

\* Under Bias

## ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V<sub>EE</sub> = -5.2V, R<sub>L</sub>=50Ω to -2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	Contraction in the	min(B)	typ	max(A)	Unit
		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0°C	-1000	-	-840	
	V OH		+25°C	- 980	E 101 - 200	-810	
			+75°C	-950	12/10/00/0	-720	POW/OR
Output Voltage		$V_{IH} = V_{IRA}$ or $V_{ILB}$	0°C	-1870	M-2070	-1665	mV
THEMEDMAR	VOL		+25°C	-1850	- 3	-1650	
			+75°C	-1830	-	-1625	
0 5	18	Made	0°C	-1020			
	Vonc		+25°C	-980		-	
		$V_{IR} = V_{IRB}$ or $V_{ILA}$	+75°C	- 920	-		mV
Output Threshold Voltage			0°C	-	- 1	-1645	
	VOLC	12° at	+25°C	-	- T	-1630	
			+75°C		+	-1605	
		C	0°C	-1165	· · · ·	-880	mV
	VIH	Guaranteed Input Voltage	+25°C	-1165	-	-880	
No.		High for All Inputs	+75°C	-1165	-	-880	
Input Voltage		Contract I have William	0°C	-1810	-	-1560	
12	VIL	Guaranteed Input Voltage	+25°C	-1810	1440	-1560	
1 M (E)		Low for All Inputs	+75°C	-1810		-1560	
A 15 10 10 10 10	Inn	$V_{IN} = V_{IHA}$	0 to +75°C		-	220	in the second
Input Current	In	$\overline{CS}$ $V_{IN} = V_{ILR}$	0 to +75°C	0.5	-	170	μA
	LIL	Others VIN= VILB	0 10 +15 C	-50	-	- 1	Eler
Sumly Courses	Ise	All Input and Output Open.	<i>Ta</i> -0°C	-270	-240	-	mA
Supply Current	1 EE	An input and Output Open.	Ta-75°C		-220		an M

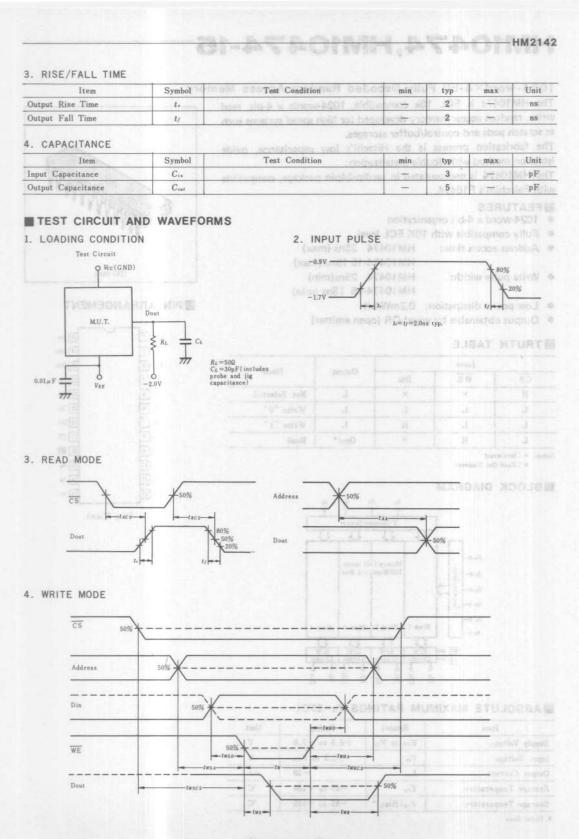
## • AC CHARACTERISTICS (V<sub>EE</sub>=-5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs	the second s		1-	6	ns
Chip Select Recovery Time	tRCS		3 <u>4</u> 0	1 6 <u>1</u>	6	ns
Address Access Time	t AA		1 L L L L		10	ns

#### 2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	1 <sub>WSA</sub> =3ns	10		-	ns
Data Setup Time	twsp		1		-	ns
Data Hold Time	twHD		1	-	-	ns
Address Setup Time	twsa	tw=10ns	3	-	-	ns
Address Hold Time	t wHA		2	-	-	ns
Chip Select Setup Time	twscs		1	-	-	n5
Chip Select Hold Time	twncs		1	-	-	ns
Write Disable Time	tws		_		6	ns
Write Recovery Time	twn		-	-	6	ns



**OHITACHI** 

## HM10474, HM10474-15

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

## FEATURES

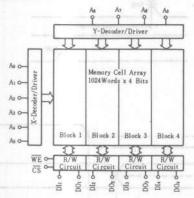
- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474 25ns (max) HM10474-15 15ns (max)
   Write pulse width: HM10474 25ns(min)
- HM10474 250s(min) HM10474-15 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

### TRUTH TABLE

	Input			Mode
CS	WE	Din	Output	Mode
Н	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant \* : Read Out Nonivert

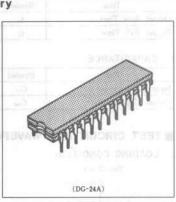
#### BLOCK DIAGRAM



## **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Via	+0.5 to VEE	v
Output Current	Inst	-30	mA
Storage Temperature	Tag	-65 to +150	°C
Storage Temperature	Tre (Bias)*	-55 to +125	°C

\* Under Bias



### PIN ARRANGEMENT

Vccs 1	24 Vec
DOs 2	23 DO2
DO <sub>4</sub> 3	22 DO1
An 4	21 DI.
A1 5	20 DIa
Ag 6	19 DI1
As 7	18. DI1
A4 8	17 CS
As 9	16 WE
NC 10	15 As
Ae 11	14 Aa
VEE 12	13 Az

HOOM BITIS

**OHITACHI** 

## ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS ( $V_{EE} = -5.2V$ ,  $R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+75^{\circ}C$ , air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
H. C. S. L. R.			0°C	-1000	-	-840	5. H.R.
	Von	The second second	+25°C	-960	-	-810	
			+75°C	-900	-	-720	CNEA
Output Voltage	nut (	$V_{IN} = V_{INA}$ or $V_{ILB}$	0°C	-1870	-	-1665	mV
30	Vol		+25°C	-1850	-	-1650	
79 - 7			+75°C	-1830	-	- 1625	
			0°C	-1020	-	-	
	Vonc		+25*C	-980	NCV 71	0895	
		E.UA TUAN IS	+75°C	-920	40	10102-01	mV
Output Threshold Voltage		VIN = VIHB OF VILA	0°C	-	-	-1645	
1	Volc	*	+25°C	-	((142))	-1630	
				-	-	-1605	
the second second		N	0°C	-1145	-	-840	mV
	Vin	Guaranteed Input Voltage	+25°C	-1105	- Eng	-810	
part of the second		High for All Inputs	+75°C	-1045	-	-720	
Input Voltage			0°C	-1870	5. 17	-1490	
	VIL	Guaranteed Input Voltage	+25°C	-1850	-	-1475	
		Low for All Inputs	+75*C	-1830	2 -	-1450	
	Іт	$V_{IN} = V_{IHA}$	0 to +75°C	- 0.	-	220	-
Input Current		CS		0.5	-	170	μA
	In	$V_{IN} = V_{ILB}$	0 to +75°C	-50	-	-	
		All Input and Output Open,	<i>Ta</i> =0°C	-200	-160		(LAH)
upply Current	IEE	Test Pin 12	Ta = 75°C		-145	1	mA

## •AC CHARACTERISTICS ( $V_{EE} = -5.2V \pm 5\%$ , Ta = 0 to $+75^{\circ}C$ , air flow exceeding 2m/sec)

1. 1						
4.4	EX-	-n	<i>u</i>	145.	$\mathcal{O}\mathcal{O}$	·

Item	Symbol Test Condition	HM10474			Н	Unit			
Item		lest Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	tACS		-	-	10	-	-	8	ns
Chip Select Recovery Time	t <sub>RCS</sub>		-	-	10	-	-	8	ns
Address Access Time	LAA		-	15	25		Æ	15	ns

2. WRITE MODE

Item	Cali	Test Condition	HM10474			HM10474-15			Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	tw	twsa=3ns	25	15		15	-		ns
Data Setup Time	f with	1 Acres	2	-	14-	2	-	1000 ( <u>1000</u> )	ns
Data Hold Time	t wird	Contraction of the second s	2	-	-	2	-	-	ns
Address Setup Time	t was	tw-twais	3	1-	-	3	-	-	ns
Address Hold Time	t wha	- William - New	2	-		2	-	110	ns
Chip Select Setup Time	t wscs	and the second second	2	-	-	2	-	-	ns
Chip Select Hold Time	t whos		2	-	-	2	-	-	ns
Write Disable Time	tws		-		10		-	8	ns
Write Recovery Time	ž wn	design of the second	-	-	10	-	-	8	ns

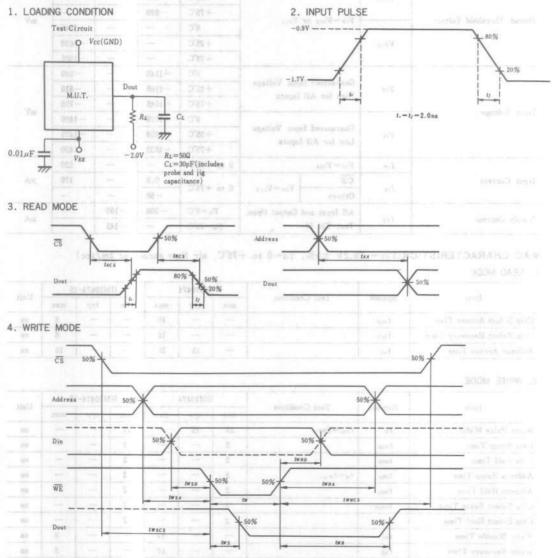


HM10474, HM10474-15 3. RISE/FALL TIME

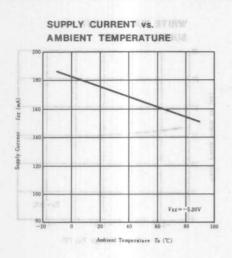
Symbol	Test Condition	2.8 min 3	typ	max	Unit
inte 1	Two Conditions	Latare P	2	(1110)	ns
tr.		-	2	-	ns
	Symbol t. t/	Symbol Test Condition	Symbol     Test Condition     min       tr	Symbol         Test Condition         min         typ           t.	Symbol         Test Condition         min         typ         max           t.        2        2

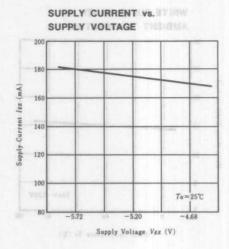
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cia		100	4		pF
Output Capacitance	Cast		_	7		pF

## **TEST CIRCUIT AND WAVEFORMS**

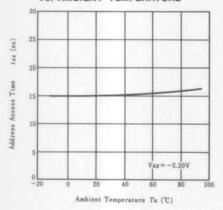


HITACHI

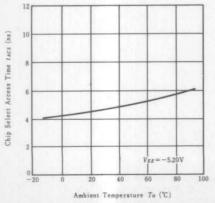




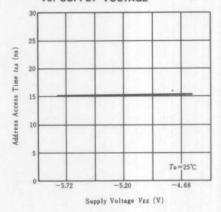
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



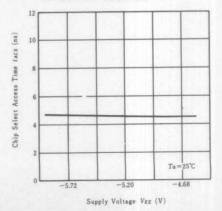




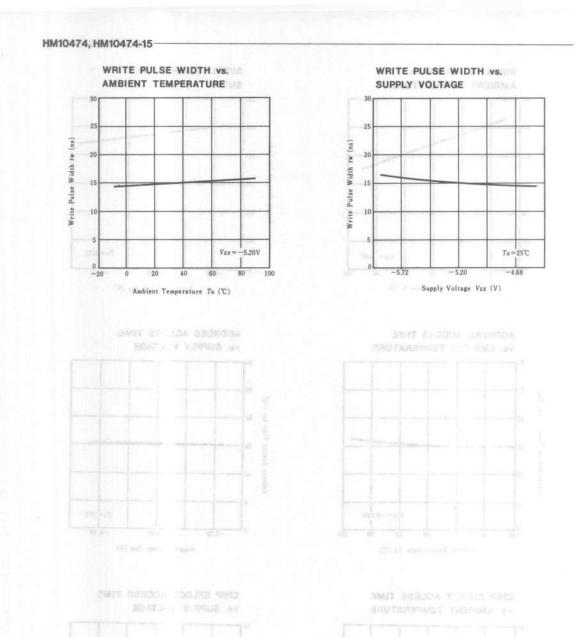
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE

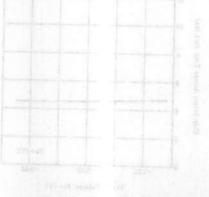


CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



**HITACHI** 

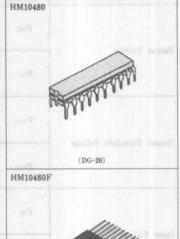




**HITACHI** 

## HM10480, HM10480F

## 16,384-words × 1-bit Fully Decoded Random Access Memory The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages. The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization. The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.



## FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

## TRUTH TABLE

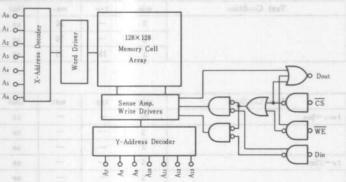
Mode	Output		Input	
Mode	Output	Din	WE	CS
Not Selected	Leo I	×	×	Н
Write "0"	L	L	L	L
Write "1"	L	Н	L	L
Read	Dout*	×	H	L

PIN ARRANGEMENT

(FG-20)

Notes) × : Irrelevant \* : Read Out Noninvert

#### BLOCK DIAGRAM



#### 20 Vcc Dout 1 19 Din Ao 2 18 CS A1 3 17 WE Az 4 16 A13 Az 5 15 Au A 6 As 7 14 Au As 8 13 A10 12 As A7 9 VEE 10 11 Aa

## (Top View)



## **BABSOLUTE MAXIMUM RATINGS** (*Ta*=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Via	$+0.5$ to $V_{EE}$	V
Output Current	Ieut	-30	mA
Storage Temperature	Teta	-65 to +150	°C
Storage Temperature	Tate (Bias)*	-55 to +125	°C

\* Uniter Bias



## HM10480, HM10480F-

## ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS ( $V_{EE} = -5.2V$ ,  $R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+75^{\circ}$ C, air flow exceeding 2m/sec)

MID480, MM0480F

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
	0010-000	being doct bid her	0°C	-1000	enoter a	-840	CONTRACTOR
	Von		+25°C	-960	L.Q. (1996)	-810	e umos.
		sepsoitanos, oxide	+75'C	-900	11.250	-720	rdat jir
Output Voltage		$V_{IN} = V_{IHA}$ or $V_{ILB}$	0'C	-1870	uol mie	-1665	mV
Real	Vol	nig-OS rall bos n	+25°C	-1850	Dod ( See 9	-1650	Table 1
11785			+75°C	-1830	(10) You Yo	-1625	1925/3
1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.			0°C	-1020	1.00	-	
Output Threshold Voltage	Vonc		+25°C	-980			1
			+75'C	-920	-	-	T/mV
		VIN = VIHB OF VILA	0*C	-	-	-1645	
	Volc		+25°C	THE R. L. L.	0.110-1-2	-1630	
			+75°C			-1605	14140-1 1-1-1-12
	VIH		0*C	-1145	-	-840	mV
		Guaranteed Input Voltage	+25*C	-1105	2001	-810	
and the second		High for All Inputs	+75°C	-1045	1.11.27.10	-720	
nput Voltage			0"C	-1870	-	-1490	
	VIL	Guaranteed Input Voltage	+25*C	-1850	-	-1475	
	2	Low for All Inputs	+75°C	-1830	-	-1450	
	Іт	$V_{IN} = V_{IHA}$	0 to +75*C		109	220	100
nput Current		CS	0	0.5		170	μA
	IIL	$V_{IN} = V_{ILB}$	0 to +75°C	-50	-	-	
04.020		All Input and Output Open,	<i>Ta</i> =0°C	-170	-140	-	
Supply Current	Ιεε	Test Pin 10	Ta - 75°C	-	-130	-	mA

## •AC CHARACTERISTICS ( $V_{\mathcal{E}\mathcal{E}} = -5.2V \pm 5\%$ , Ta=0 to $+75^{\circ}$ C, air flow exceeding 2m/sec) 1. READ MODE

						272.9%	NUMBER /	- U-202-I
Item	Symbol	Tes	t Condition	-	min	typ	max	Unit
Chip Select Access Time	tacs				2	- 1	10	ns
Chip Select Recovery Time	tres				2	-	10	ns
Address Access Time	1 4 4				3	15	25	ns
2. WRITE MODE								and a
Item	Symbol	Tes	t Condition		min	typ	max	Unit
Write Pulse Width	t w	twss=5ns	and -	-	25		-	ns
Data Setup Time	twsp	3110	1201		5	-		ns
Data Hold Time	t who	5		- 19	5		-	ns
Address Setup Time	twsn	tw=25ns	3	6	5	3 -	-	ns
Address Hold Time	t wn a		5	1	5	1	-	ns
Chip Select Setup Time	twscs				5	-	-	ns
Chip Select Hold Time	twncs			) (2)	5	MR 42007	5	ns
Write Disable Time	tws	and			al is <del>T</del>	-	10	ns
Write Recovery Time	t wn	1			Ve <del>rt</del> o Si		10	ns
		. V	251 of 1.04		15		20	dill have

HITACHI

HM10480, HM10480F

3. RISE/FALL TIME

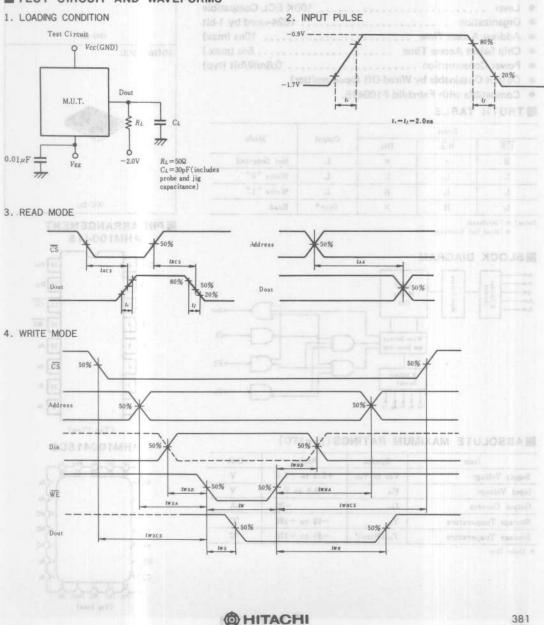
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t,	Hit, mulhorita strokow ussess	Note the	2	1 377-00	ns
Output Fall Time	t,		noites las	2	de Tigor	ns

JUSTROOMMH, BTP

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cin	anorgaulated in emotion (	(doment) of	4	M.(7_3)(0	pF
Output Capacitance	Cui		-	7	-	pF

## TEST CIRCUIT AND WAVEFORMS



## HM100415,HM100415CC

### 1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

### FEATURES

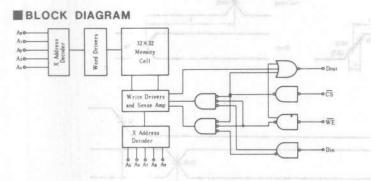
- Level ..... 100K ECL Compatible

- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

## TRUTH TABLE

	Input		0	Mode
CS	WE	Din	Output	Mode
Н	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant \* : Read Out Noninvert

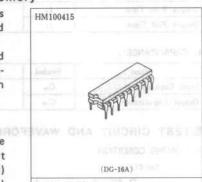


## **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

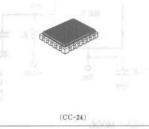
Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Via	$+0.5$ to $V_{EE}$	V
Output Current	Int	-30	mA
Storage Temperature	Tata	-65 to +150	°C
Storage Temperature	Tere (Bias)*	-55 to +125	°C

**OHITACHI** 

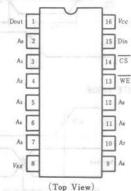
\* Under Bias



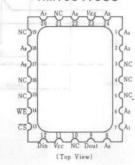
HM100415CC



PIN ARRANGEMENT HM100415



●HM100415CC



## ELECTRICAL CHARACTERISTICS

MROHEVAN GWA TIUDAID TSET

• DC CHARACTERISTICS ( $V_{EE} = -4.5V$ ,  $R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+85^{\circ}$ C, air flow exceeding 2m/sec)

Item	Symbol	T	est Condition	min(B)	typ	max(A)	Unit
	Von			-1025	-955	0-880	mV
Output Voltage	Vol	$-V_{in}=V_{IHA}$ or $V$	11.8	-1810	-1715	-1620	mV
o	Vonc				-	-	mV
Output Threshold Voltage	Volc	$V_{in} = V_{IHB}$ or $V_{ILA}$				-1610	mV
* ***	Vin	Guaranteed Input Voltage High/Low for All Inputs		-1165	-	-880	mV
Input Voltage	VIL			-1810	-	-1475	mV
	Im	$V_{is} = V_{IHA}$		-6	-	220	μA
Input Current			CS		-	170	
	In	$I_{IL}$ $V_{in} = V_{ILB}$	Others	-50	-	-	μA
Supply Current	IEE	All Inputs and	Outputs Open	-200	-150	-	mA

## •AC CHARACTERISTICS ( $V_{EE} = -4.5V \pm 5\%$ , Ta=0 to $+85^{\circ}$ C, air flow exceeding 2m/sec)

## 1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	tacs	ant (8	-	3	5	ns
Chip Select Recovery Time	tres		-	3	5	ns
Address Access Time	taa		-	7	10	ns

#### 2. WRITE MODE

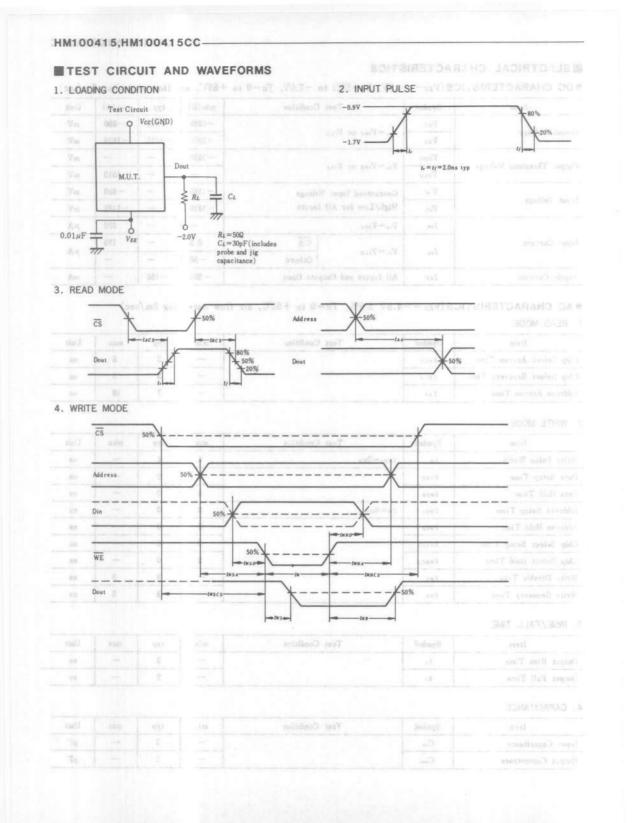
Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t w	twsA = 2ns	6	4	-	ns
Data Setup Time	twso	*	2	0		ns
Data Hold Time	t who		2	0	-	ns
Address Setup Time	twsa	tw-6ns	2	0	-	ns
Address Hold Time	t wax		2	0	-	ns
Chip Select Setup Time	twscs	the second second	2	0		ns
Chip Select Hold Time	twncs	have been been been	2	0		ns
Write Disable Time	tws	The second se		3	5	ns
Write Recovery Time	twe	General and here		3	5	ns

### 3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	<i>t</i> ,		-	2	-	ns
Output Fall Time	t/		-	2	-	ns

### 4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	Cia			3	-	pF
Output Capacitance	Cent		-	5	-	pF



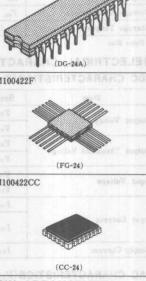
**OHITACHI** 

# HM100422,HM100422F HM100422CC

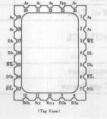
256-word×4-bit Fully Decoded Random Access Memory

The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages. Four active Low Block Select lines are provided to select each block independently. (DG-24A) The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization. HM100422F The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422. FEATURES 256-word x 4-bit organization Fully compatible with 100K ECL level (FG-24) Address access time: 10ns (max.) HM100422CC Minimum write pulse width: 6ns (min.) Low power dissipation: 0.8mW/bit Output obtainable by wired-OR (open emitter) TRUTH TABLE (CC-24) Input Output Mode BS WE Din PIN ARRANGEMENT н × L Not Selected ●HM100422 × Vet+ 14 Vec 11 UQs L L L L Write "0" UG1 2 L L Н L Write "1" H5. 1 22 154 DO: 4 H × 21 005 L Dout\* Read HS# 5 20 1154 Notes) × : Irrelevant Ul: 4 Ul: 7 19 UL. 18 UL # : Read Out Noninvert WE I 17 A BLOCK DIAGRAM As A<sub>4</sub> A: 4 9 16 A 0 An 10 Ar 11 15 A 14 4 Y-Decoder/Driver Vex 12 13 A Top View) ●HM100422F ññ ññ As O-Memory Cell Array AE WK AI O-256 Words ×4 Bits 06 100 100 UL.C HS.C BSe der/ Az O-DO-F JUG X-De As O (Top View) ●HM100422CC AI O Block I Block 2 Block 3 Block 4 R/W Circuit R/W Circuit R/W Circuit R/W Circuit WE O-85. P 7 9 6 P 9 2 6 9 6 6 6 U01 Uls Uls BSa Ub 50 DI.

**OHITACHI** 



HM100422





## HM100422,HM100422F,HM100422CC-

## **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V
Input Voltage	Via	$+0.5$ to $V_{EE}$	v
Output Current	Ient	-30	mA
Storage Temperature	Tela	-65 to +150	•с
Storage Temperature	T <sub>stg</sub> (Bias)*	-55 to $+125$	°C

256 word X 4-bit Fully Decoded R The HM109422 is EQL 100K comparible, 2 while, random access memory developed for Four addies Low Block Select fines are pro-

\* Under Bias

ELECTRICAL CHARACTERISTICS

Item	Symbol	Te September 1	est Condition	min(B)	typ	max(A)	Unit
0	Von	Vis = VIHA OF VILB		-1025	- 955	-880	mV
Output Voltage	Voi.			-1810	-1715	-1620	mV
Output Threshold Voltage	Vonc	W _ W W		-1035	sine <b>g</b> <del>es</del> i	id-Nie <del>t</del> ni	mV
	Volc	Via=VINB or VILA		104 800	l neri <del>ne</del> u	-1610	mV
	VIII Guaran	Guaranteed Inpu	Guaranteed Input Voltage		101 J.+#1	-880	mV
Input Voltage	VIL	High/Low for A	All Inputs	-1810	pinti sittid	-1475	mV
	Іт	$V_{in} = V_{IHA}$		RAWIE .	particular d	220	μA
Input Current			BS (Matsime nec	0.5	iw ye <u>n</u> a	170	include in a
	IIL	$V_{ix} = V_{ILB}$	Others	-50		-	μA
Supply Current	IEE	All Inputs and	Outputs Open	-200	-165	ABAL 1	mA

•DC CHARACTERISTICS (V<sub>EE</sub> = -4.5V, R<sub>L</sub>=50Ω to -2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

## •AC CHARACTERISTICS ( $V_{EE} = -4.5V \pm 5\%$ , Ta=0 to $+85^{\circ}$ C, air flow exceeding 2m/sec) 1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	tABS	0 Stell		-	5	ns
Block Select Recovery Time	tres				5	ns
Address Access Time	tan	lized* liced	-	7	10	ns

#### 2. WRITE MODE

Item	Symbol	Te	st Condition	min	typ	max	Unit
Write Pulse Width	tw	twsx=2ns		6	4.5	-	ns
Data Setup Time	twsp		winderstand and the second sec	2	0		ns
Data Hold Time	t who	-	L III L	2	0	-	ns
Address Setup Time CO	tws A	tw=6ns		2	0	-	ns
Address Hold Time	t wha			2	0	-	ns
Block Select Setup Time	twsbs	]		2	0	121	ns
Block Select Hold Time	twnss		Bener Coll James	2	0	-	ns
Write Disable Time	tws		AND DE MONTON		4	5	ns
Write Recovery Time	twe			-	4.5	9	ns

## 3. RISE/FALL TIME

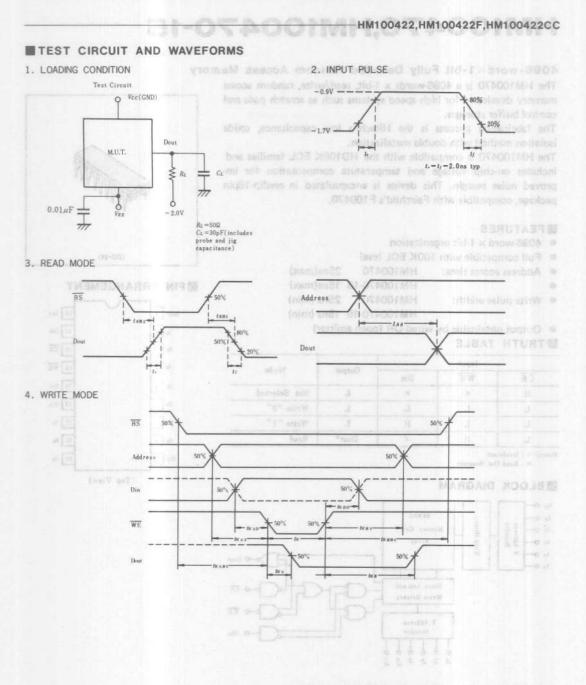
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.			2		ns
Output Fall Time	11	1 2010 1 2000 1 3	4 m P _ 1 m	2	-	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C.,.	and the second s	-	4	-	pF
Output Capacitance	Cast		2. 4 2 - 2 1	7	-	pF

386

## **HITACHI**



#### ELESSOLUTE MAXAMUM RATINGS IL-ST

		Sugar Voltage
	*(aa16)75	

**HITACHI** 

## HM100470,HM100470-15

## 4096-word × 1-bit Fully Decoded Random Access Memory The HM100470 is a 4096-words x 1-bit, read/write, random access

memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.

## FEATURES

- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: HM100470 25ns(max)
- Write pulse width:
- HM100470-15 15ns(max) HM100470 25ns (min) HM100470-15 15ns (min)
- Output obtainable by wired-OR (open emitter)

## TRUTH TABLE

Input			0	Mode
CS	WE	Dín	Output	Mode
Н	×	x	L	Not Selected
L	L	L	L	Write "0"
L	L	Н	L	Write "1"
L	Н	×	Dout*	Read

Notes) × : Irrelevant \* : Read Out Nonivert

An O

AI O-

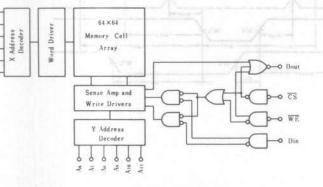
Ai o-

As o-

A. 0-

As O

### BLOCK DIAGRAM



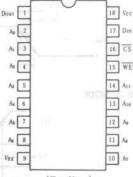
### BABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vee to Vcc	+0.5 to -7.0	V
Input Voltage	V	$+0.5$ to $V_{EE}$	V
Output Current	I est	-30	mA
Storage Temperature	Tela	-65 to +150	°C
Storage Temperature	Tere (Bias)*	-55 to +125	•C

\* Under Bias

(DG-18)





(Top View)

388

## **OHITACHI**

### HM100470, HM100470-15

## ELECTRICAL CHARACTERISTICS

BTEST CINCUIT AND WAVEFORMS

• DC CHARACTERISTICS ( $V_{EE} = -4.5V$ ,  $R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+85^{\circ}C$ , air flow exceeding 2m/sec)

Item	Symbol	Т	est Condition	min(B)	typ	max(A)	Unit
	Von			-1025	-955	-880	mV
Output Voltage	Vol	$V_{in} = V_{IHA}$ or $V$	ILB	-1810	-1715	-1620	mV
	Vonc				-	-	mV
Output Threshold Voltage	Volc	$V_{i*} = V_{IHB}$ or $V_{i}$	LA	-	-	-1610	mV
	VIN	Vin Guaranteed Input Voltage	ut Voltage	-1165	-	-880	mV
Input Voltage	VIL	High/Low for All Inputs		-1810		-1475	mV
	Іт	$V_{in} = V_{IHA}$	0.0-3	-	0 -	220	μA
Input Current			CS	0.5	-	170	
	In	$V_{in} = V_{ILB}$ Others		-50	-	-	μA
Supply Current	IEE	All Inputs and	Outputs Open	-200	-165	SCIEN	mA

## •AC CHARACTERISTICS ( $V_{EE} = -4.5V \pm 5\%$ , Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	-	Н	M100470-	-15	K	HM10047	0	Unit
	Symbol	Test Condition	min	typ	max	min	typ	max	Ont
Chip Select Access Time	tACS		-	-	8		-	10	ns
Chip Select Recovery Time	tres		-	-	8	-	-	10	ns
Address Access Time	LAA		-	-	15	-	-	25	ns

#### 2. WRITE MODE

Item	0.11	Test Condition	H	IM100470-	-15		HM10047	0	Unit
Item	Symbol	Test Condition	min	typ	max	min	typ max	Unit	
Write Pulse Width	t w	twsa=3ns	15	-	-	25	-	-	ns
Data Setup Time	twsp		2		Je-	2	-	-	ns
Data Hold Time	t who		2	-	1-	2	-		ns
Address Setup Time	t wsx	tw=twmin	3		-	3	-	-	ns
Address Hold Time	t wha	1	2	7-	-	2	-	-10	ns
Chip Select Setup Time	twscs		2			2	-	-	ns
Chip Select Hold Time	t whos		2	-		2	-		ns
Write Disable Time	t ws		-4	-	8	-	-	10	ns
Write Recovery Time	t wn			-	8	-		10	ns

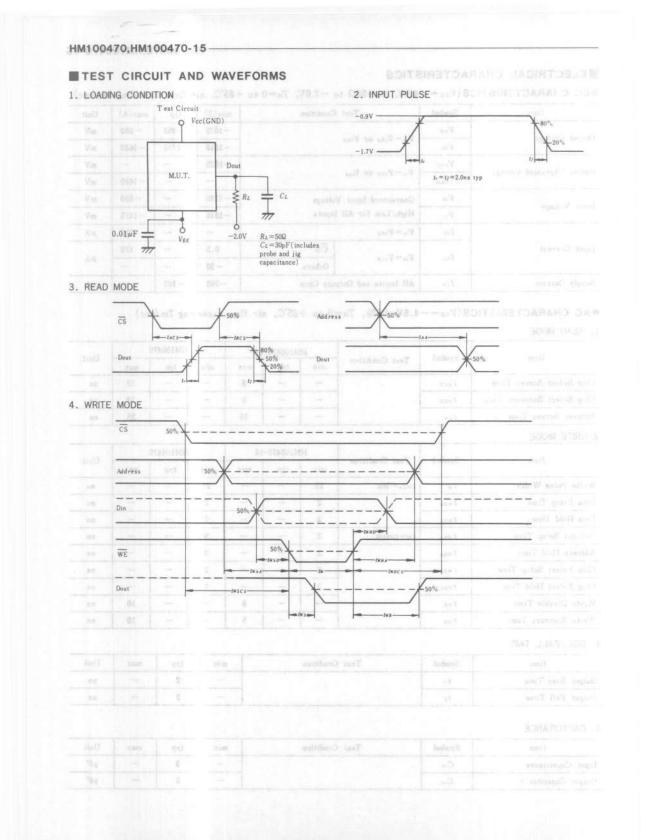
## 3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t.		-	2	-	ns
Output Fall Time	tj		-	2	-	ns

#### 4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C in		-	3	-	pF
Output Capacitance	Cent		-	5	-	pF





**CHITACHI** 



## 1024-word×4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

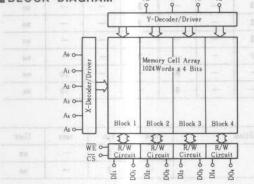
- FEATURES
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474/F 25ns(max)
- Write pulse width:
- HM100474/F-15 15ns(max) dth: HM100474/F 25ns(min) HM100474/F-15 15ns(min)
- Output obtainble by wired-OR (open emitter)

### TRUTH TABLE

	Input	t Output		Mode
CS	WE	Din	Output	Mode
Н	×	×	L	Not Selected
L	Liter	Kit L	$= L(\mathcal{M})$	Write "0"
L	L con	Н	L get	Write "1"
L	Н	×	Dout*	Read

\* : Read Out Nonivert

## BLOCK DIAGRAM

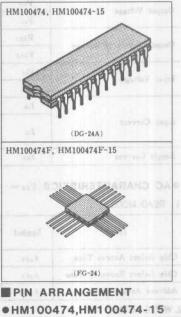


#### **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	VEE to Vcc	+0.5 to -7.0	v
Input Voltage	Vin	+0.5 to VEE	V
Output Current	Iout	-30	mA
Storage Temperature	Tria	-65 to $+150$	°C
Storage Temperature	T <sub>sig</sub> (Bias)*	-55 to +125	*C

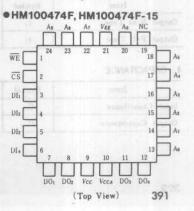
**OHITACHI** 

\* Under Bias





(Top View)



## HM100474,HM100474-15,HM100474F,HM100474F-15-

## ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS ( $V_{EE} = -4.5$ V,  $R_L = 50\Omega$  to -2.0V, Ta = 0 to  $+85^{\circ}$ C, air flow exceeding 2m/sec)

Item	Symbol	Tes Memor	est Condition	min(B)	typ	max(A)	Unit
	Vos	4-bit, readimite, landon acces		1020	-955	-880	mV
Output Voltage	Vol	$-V_{in}=V_{iHA}$ or $V$	ILB CONTRACTOR ACTIV	-1810	- 1715	-1620	mV
	Vonc	$-V_{is} = V_{IRS}$ or $V_{ILS}$ diverges well and the		-1035	1.000000	n nolfica	mV
Output Threshold Voltage	Volc	$V_{is} = V_{IHB}$ or $V$	7LA		tuab thi	-1610	mV
1 Marson	Vin	Guaranteed Inp	-1165	nda ↔	-880	mV	
Input Voltage	VIL	High/Low for	-1810	10112-01	-1475	mV	
	Im	$V_{in} = V_{IHA}$	sectarias in conditional	North R R POOL	a san <u>L</u> a	220	μA
Input Current			CS	0.5	Tort in the	170	
	IIL	$V_{in} = V_{ILB}$	Others	-50	-	8.949	μA
Supply Current	Ιεε	All Inputs and	Outputs Open	-200	- 165	LA R MO	mA

•AC CHARACTERISTICS ( $V_{EE} = -4.5V \pm 5\%$ , Ta = 0 to  $+85^{\circ}$ C, air flow exceeding 2m/sec)

1. READ MODE

						M100474/		Unit ns ns ns
Symbol	Test Condition	min	typ	max	min	typ	max	
tACS		-	-	8	-		10	ns
tRCS		-	-	8	-	-	10	ns
LAA 9		× -	<u>L</u> eno	15		15	25	ns
	tacs tres	tacs tacs	min t.xcs - t.xcs -	min typ tAcs – – tAcs – –	min         typ         max           tAcs         -         -         8           tAcs         -         -         8	min         typ         max         min           tAcs         -         -         8         -           tAcs         -         -         8         -	min         typ         max         min         typ           tAcs         -         -         8         -         -           tAcs         -         -         8         -         -	min         typ         max         min         typ         max           tAcs         -         -         8         -         -         10           tAcs         -         -         8         -         -         10

Item	Symbol	Test Condition	HM	1100474/F	-15	- F	IM100474.	/F	Unit
Tem	Symbol	Test Condition	min	typ	max	min	typ	max	Univ
Write Pulse Width	t w	$t_{ws,s} = 3$ ns	15	201	-	25	15	-	ns
Data Setup Time	twsp		2	-	-	2			ns
Data Hold Time	t whd		2	-	-	2		Sector 1	ns
Address Setup Time	twsa	tw=twmin	3	-		3	-		ns
Address Hold Time	t wha		2	-	1110 <u>1-</u> 4	2	-	-	ns
Chip Select Setup Time	twiscs	]	2	-	-	2	-	-	ns
Chip Select Hold Time	twacs		2	-	and The s	2	-		ns
Write Disable Time	tws	]	-	-	8	-	-	10	ns
Write Recovery Time	t wn		-	-	8	-	1-13	10	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	<i>t</i> ,	Well Street		2	-	ns
Output Fall Time	1/		1 1 1	2	-	ns

4. CAPACITANCE

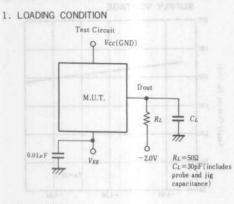
IN ASSOLUTE MALLMUM RATINGS(Tem 201)

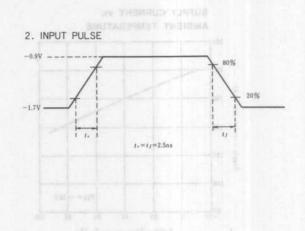
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C.,	A Bran de gran	104 10 Hole	4		pF
Output Capacitance	Cout			7	-	pF

**OHITACHI** 

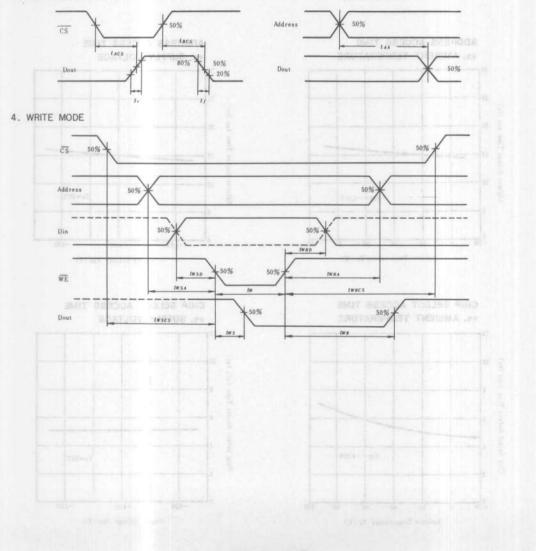
## HM100474,HM100474-15,HM100474F,HM100474F-15

## TEST CIRCUIT AND WAVEFORMS





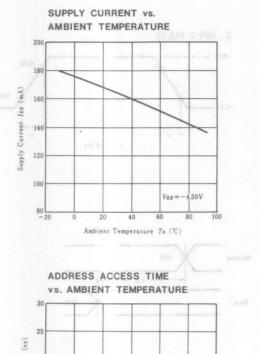
3. READ MODE

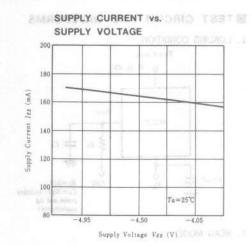


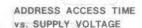
**HITACHI** 

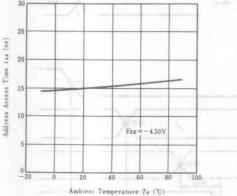
.

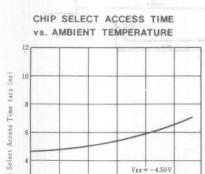
## HM100474,HM100474-15,HM100474F,HM100474F-15











20

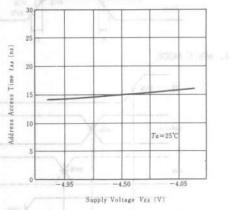
40

Ambient Temperature To ("C)

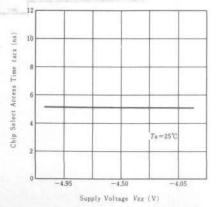
60

80

100

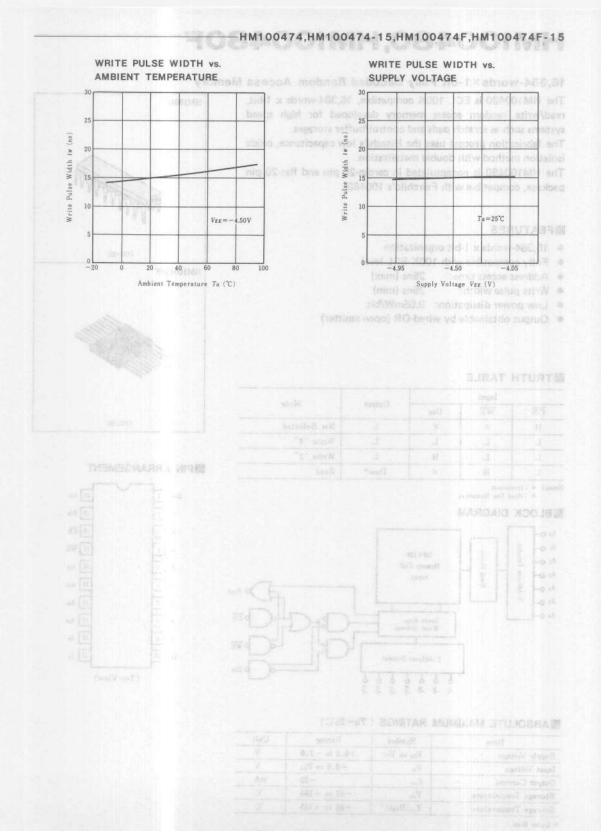


CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



Chip

0L -20



**HITACHI** 

# HM100480, HM100480F

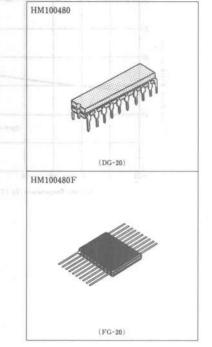
# 16,384-words×1-bit Fully Decoded Random Access Memory

The HM100480 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages. The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100480 is encapsulated in cerdip-20 pin and flat-20 pin package, compatible with Fairchild's 100480.

#### FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns (min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

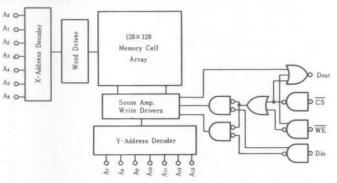


## TRUTH TABLE

	Input		0		
CS	WE	Din	Output	Mod	
Н	×	×	L	Not Selected	
L	L	L	L	Write "0"	
L	L	Н	L	Write "1"	
L	Н	×	Dout*	Read	

Notes) × : irrelevant \* : Read Out Noninvert

#### BLOCK DIAGRAM



#### PIN ARRANGEMENT



#### **ABSOLUTE MAXIMUM RATINGS** (*Ta*=25°C)

Item	Symbol	Rating	Unit	
Supply Voltage	V <sub>EE</sub> to V <sub>cc</sub>	+0.5 to -7.0	v	
Input Voltage	Via	$+0.5$ to $V_{EE}$	v	
Output Current	Inut	-30	mA	
Storage Temperature	Teta	-65 to +150	°C	
Storage Temperature	Tata (Bias)*	-55 to +125	*C	

\* Under Bias

396

**OHITACHI** 

#### -HM100480, HM100480F

THAT I A SUMMAR

#### **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

Item	Symbol	Rating	Unit		
Supply Voltage	VEE to Vcc	+0.5 to -7.0	V.	45	
Input Voltage	Via	$+0.5$ to $V_{EE}$	v		
Output Current	Int	-30	mA		
Storage Temperature	Tete	-65 to +150	°C		
Storage Temperature	T <sub>st</sub> (Bias)*	-55 to $+125$	°C		
Under Bias					

# ELECTRICAL CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
0	V <sub>OH</sub>			-1025	-955	- 880	mV
Output Voltage	Vol	$-V_{is}=V_{IHA}$ or $V$	11.8	-1810	-1715	-1620	mV
	Vonc	$-V_{in}=V_{IHB}$ or $V_{ILA}$		-1035	-	-	mV
Output Threshold Voltage	Volc			-	100	-1610	mV
Input Voltage	VIII	Guaranteed Inp	-1165	-	- 880	mV	
	VIL	High/Low for All Input		-1810	- 1	-1475	mV
	IIH	$V_{in} = V_{IHA}$			-	220	μA
Input Current			ĈŜ	0.5	1945	170	=
	$I_{IL}$	$V_{in} = V_{ILB}$	Others	-50	-	-	μA
Supply Current	IEE	All Inputs and Outputs Open		-200	-165	-	mA

# •AC CHARACTERISTICS ( $V_{EE} = -4.5V \pm 5\%$ , Ta = 0 to $+85^{\circ}$ C, air flow exceeding 2m/sec)

### 1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	FACS		2	×-	10	ns
Chip Select Recovery Time	tres		2	4	10	ns
Address Access Time	dress Access Time tAA		3	1000	25	ns

#### 2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	tw	Iwsa=5ns	25	-	-	ns
Data Setup Time	twsp	Y	5	-	-	ns
Data Hold Time	twnd		5			ns
Address Setup Time	twsx	$t_w = t_w \min$	5			ns
Address Hold Time	t wha		5	-	-	ns
Chip Select Setup Time	twscs	( the second sec	5	-	-	ns
Chip Select Hold Time	twncs		-	-	5	ns
Write Disable Time	tws	the state of the s			10	ns
Write Recovery Time	twa	N	-	-	10	ns

( HITACHI

HM100480, HM100480F-

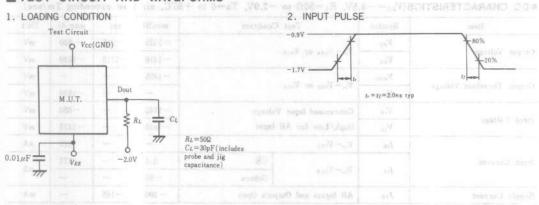
3. RISE/FALL TIME

SOLUTE MAXIMUM RATINGS (To+28%)

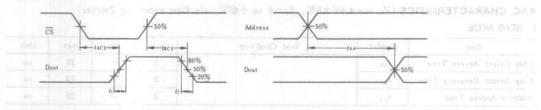
Item	Symbol	Unie	Test Condition	( interv	min	typ	max	Unit
Output Rise Time	t.,	V	0.3 - M 8.0 V	set of a	3 -	2	- could	ns
Output Fall Time	tj	14	10.201		a T	2	-	ns
4. CAPACITANCE								
Item	Symbol	2	Test Condition		min	typ	max	Unit
Input Capacitance	C.,	0	847 × 00 60-	Toursenants		3	a ut <u>er</u> eques	pF
Output Capacitance	Cust				-	5	-	pF

#### TEST CIRCUIT AND WAVEFORMS

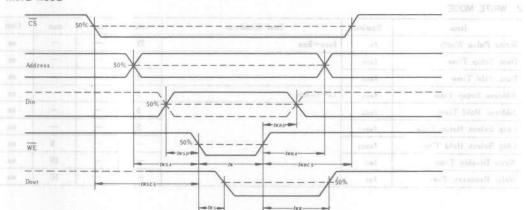
BELECTRICAL CHARACTERISTIC



3. READ MODE







**OHITACHI** 

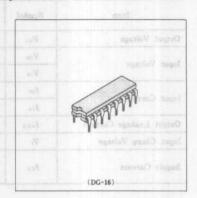
# HM2504, HM2504-1

ODC CHARACTERISTICS (Red

## 256-word×1-bit Fully Decoded Random Access Memory The HM2504 Series item is a TTL compatible, 256-word x 1-bit, read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. This is a fully decoded, read/write random access memory perfectly compatible with the TTL logic family, designed as an open collector output type for simplicity of expansion.

Construction	
Read access time HM2504: 55ns (max)	
HM2504-1: 45ns (max.	.)
Chip select access time 30ns (max.)	

Power consumption ..... 1.8mW/bit (typ) Output ..... Open collector

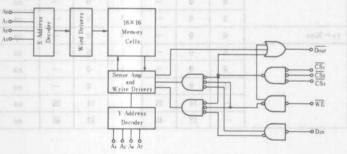


		PIN	ARRANGEMENT
	A STATE SIGNAL		

1	And	Inputs	Output		
CS	-	WE	Din	Open Collector	Mode
any one	H	×	×	Н	Not Selected
dl	L	L	L	H	Write "0"
11	L	L	Н	Н	Write "1"
all	L	Н	×	Dout *	Read

Not \* : Read out inverted

# BLOCK DIAGRAM



#### 16 Vcc A, I A1 2 15 A., CS, 3 14 Ar CS, 4 13 Din 12 WE CS, 5 6 A. A., 7 10 A. GND 8 9 A.,

	Weigh Russer's Thirt

(Top View)

#### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2504, HM2504-1	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	Via 3	-0.5 to +5.5	V
Input Current	In	-12 to $+5.0$	mA
Output Voltage (Output High)	Vest	-0.5 to $+5.5$	V
Output Voltage (DC Output Low)	Inut	+20	mA
Storage Temperature	Tata	-65 to +150	°C
Storage Temperature	Tate (Bias)*	-55 to +125	"C

\* Under Bias



## HM2504, HM2504-1

#### ELECTRICAL CHARACTERISTICS

•DC CHARACTERISTICS (Vcc=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol		Condition	H	M2504 Ser	ies	Unit	
Item	Symbol	lest of no her do	Condition	min	typ	max	Unit	
Output Voltage	Vol	Vcc=4.75V, IoL=	September	0.3	0.45	v		
	Vin Guaranteed Input Voltage		Voltage High	2.0	1.6	ap Allin	v	
Input Voltage	VIL	Guaranteed Input	10 1961 200	1.5	0.85	v		
	In	Vcc-5.25V, V.,-	4.5V	-	0	20	μA	
Input Current	In	Vcc=5.25V, Vis=		-530	-800	μA		
Output Leakage Current	Icex	Vcc=5.25V, Ver	4.5V		0	50	μA	
Input Clamp Voltage	Vi	$V_i = V_{cc} = 5.25 \text{V}, I_{i*} = -10 \text{mA}$		$V_{cc} = 5.25 V, I_{is} = -10 m A$	-	-1.0	-1.5	V
		Vcc-5.25V	0< Ta<25°C		-	135	mA	
Supply Current	Icc	All input GND	<i>Ta</i> ≥25°C	-	-	130	mA	

MME AOBSMH

# AC CHARACTERISTICS

( $V_{cc}$ =5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/s, see test circuit and waveforms) 1. READ MODE

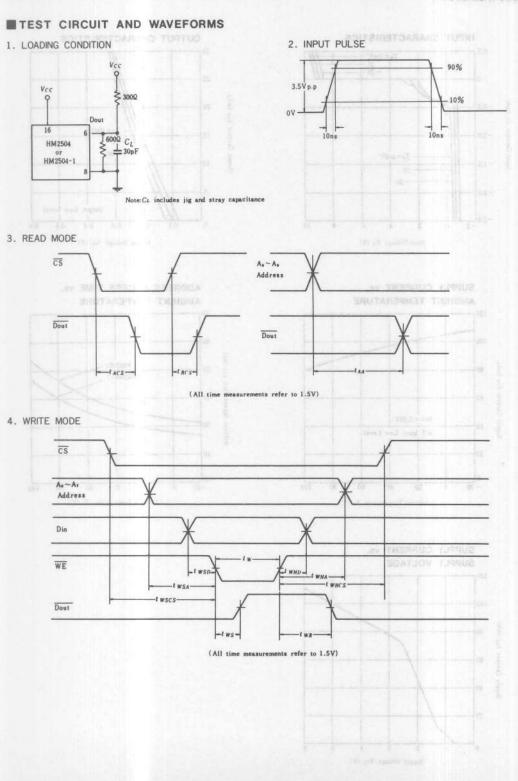
A B			HM2504			1	USTR		
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Chip Select Access Time	LACS	Stede .	-	12	30	-	12	30	ns
Chip Select Recovery Time	tres		-	18	25	-	18	25	ns
Address Access Time	t A A		-	35	55		30	45	ns

#### 2. WRITE MODE

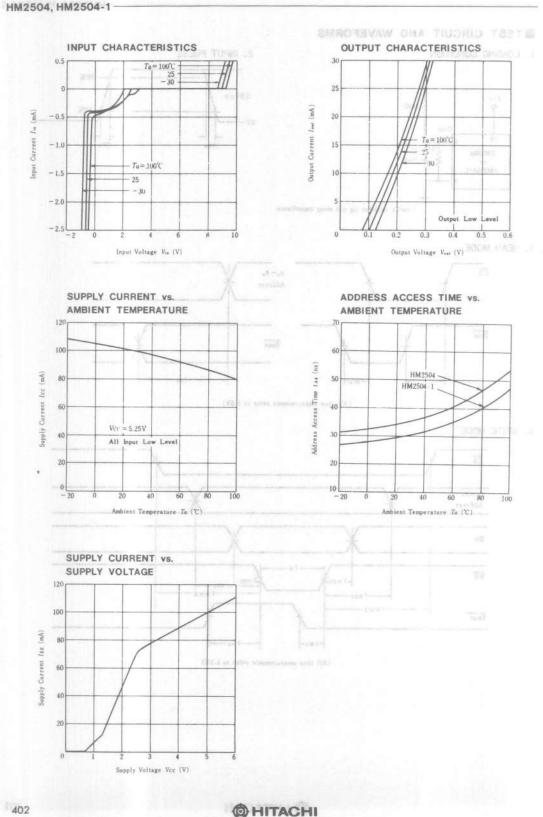
Item	Symbol	Test Condition		HM2504		1	1	Unit	
Item	Symbol	Test Condition	min	typ	max	min	typ	max	Unit
Write Pulse Width	t w	$t_{wsA} = 0$ ns	30	8	-	30	8		ns
Data Setup Time	twsp		0	0	-	0	0	-	ns
Data Hold Time	t whd		5	0	-	5	0	- 1	ns
Address Setup Time	twsx	tw=30ns	0	0	-	0	0	-1	ns
Address Hold Time	t wha	CE CE	5	0	1 -	5	0	1 4	ns
Chip Select Setup Time	twscs	Rent	0	0	-	0	0	-	ns
Chip Select Hold Time	lwncs	and the second s	5	0	-	5	0		ns
Write Disable Time	tws	Warmed Dr.	-	14	35	-	14	35	ns
Write Recovery Time	twn		_	12	40	-	12	40	ns

#### 3. CAPACITANCE

Item	Symbol	Test Condition	HM2504			ALC: NO	Unit		
			min	typ	max	min	typ	max	Unit
Input Capacitance	Cin	V		3	5	-	3	5	pF
Output Capacitance	Cour		- 1	6	8	-	6	8	pF



**HITACHI** 



									cess Me		Y			
								and the second s	ite random memories,		N		egatio (	lingi
									is a fully					
									compatible					
									utput type					
or simp	lcity of	expan	sion.									1	>	
Level					7	TL co	mpa	tible	81 - 1	(Biles)		100	R	
							Sec. and	x 1 bit				BARN	- sector	
Read	access	time .	• • • • •	•••••	9765 B			70ns (m	2002 C	NTR		Y!		
								45ns (1 35ns (1	max)					
Chin	elact a	ccess t						40ns (m						
omp :	Scieur a	100033 L	ine .					30ns (r		1		(DG-16A)		
								25ns (r	max.)	L				-
Power	consu	mption	1		0	).5mW	/bit		AND AND AN			RRANGEN	ENT	
Outpu					0	)pen c	ollec	tor					Valuer	
			*								CS	1	16 Vcc	
											Aa	2	15 Din	
											A.	3	14 WE	
TRUT	H TA	BLE									and a	Cornel	P	
V	8.1-	Inputs	1-1		T		T	An.91	A // M. 8-		A,	4		
CS	121	WE	-	Din		Output		M	ode		A,	5	12 A.	
Н	1.10	×		×		Н		Not Sel	ected		A.	6	11 A,	
L		L	-	L	-	Н		Write "			Dout	7	10 A.	
L		L		Н	-	Н	-	Write "	- AL		GND	erealere 8	9 As	
L		Н		×	-	Dout*		Read			0.40	-		
otes) × : D		on-inverted	1 3.00	10.000	100		ACR S	lain	et Condition			(Top View	est.	
	icau out u		01											
BLOG	K DI	AGRA	M											
As • A1 •	ē.,	Driwes	32×	32										
A2 = A3 =	X Address Decoder	Wand Dr	Mem Cell	ory				5						
Aro			4	100		F	-	P	- Dout					
			Senze				- 537	-0	• CS					
			WriteB	rivers	TC	J.	1.02	7						
			Y Add		40			-7-	WE		1091			
			Decod		4		1	0	P Dia					
	- 0		As As As	As As		-		2	• Din					
					-						11041			
								1-1						

**HITACHI** 

#### HM2510, HM2510-1, HM2510-2-

#### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	HM2510 Series	Unit
Supply Voltage	Vec	-0.5 to $+7.0$	V
Input Voltage	Via	-0.5 to +5.5	v
Input Current	In	-12 to $+5.0$	mA
Output Voltage (Output High)	Vout	-0.5 to +5.5	V
Output Voltage (DC Output Low)	Int	+20	mA
Storage Temperature	Tete	-65 to $+150$	.С
Storage Temperature	Tete (Bias)*	-55 to +125	*C

T-OIGSMI

\* Under Bias

# nou surran

# ELECTRICAL CHARACTERISTICS

# •DC CHARACTERISTICS (Vcc=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Sunkal	Test	Condition	H	M2510 Ser	ies	Uni
Item	Symbol	lest	Condition	min	typ	max	Um
Output Voltage	Vol	$V_{oL}$ $V_{cc} = 4.75 V, I_{oL} = 16 mA$			0.3	0.45	v
put Voltage		Guaranteed Input \	2.1	1.6	-	V	
Input voltage	VIL	Guaranteed Input	-	1.5	0.80	ν	
	Ііна	Vcc=5.25V, Via=	4.5V	-	0	40	μA
Input Current	Ілна	Vcc=5.25V, Vin=	-	0	1.0	mA	
	In	Vcc=5.25V, Vis=	-	-250	-400	μA	
Output Leakage Current	Icex	Vcc=5.25V, Vout=	4.5V	-	0	100	μA
Input Clamp Voltage	VI	Vcc=5.25V, Iin=	-10mA	-	-1.1	-1.5	V
S 1 S 1		Vcc=5.25V	0< Ta<25°C	-	-	155	mA
Supply Current	Icc	All input GND	<i>Ta</i> ≧25°C	-	95	130	mA

# •AC CHARACTERISTICS (Vcc=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

In Street V and	Symbol	Test Condition	HM2510		HM2510-1			HM2510-2			Unit	
Item	Symbol Test Condition	min	typ	max	min	typ	max	min	typ	max	Unit	
Chip Select Access Time	tACS		-	15	40	-	~	30	-	15	25	ns
Chip Select Recovery Time	tres		-	25	40	-	-	30	1.00	17	25	ns
Address Access Time	taa		-	40	70	-	35	45	-	25	35	ns

#### 2. WRITE MODE

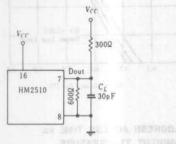
Item	Symbol	Test Condition	E	HM2510	0	H	M2510	-1	HM2510-2			Unit
Item	Symbol	Test Condition	min	typ	max	min	typ	max	min	typ	max	Unit
Write Pulse Width	tw	tws. = min	50	10	-	35	10		25	10	-	ns
Data Setup Time	twsp	18	5	0	-	5	-	-	5	0	-	ns
Data Hold Time	t wh D		5	0	-	5		-	5	0	-	ns
Address Setup Time	twsa	tw=min	15	0	-	5	-	-	5	0	-	ns
Address Hold Time	t wha		5	0	-	5	-10.0	-	5	0	-	ns
Chip Select Setup Time	twscs	]	5	0	-	5		-	5	0	-	ns
Chip Select Hold Time	twncs	1	5	0	-	5	-	-	5	0	-	ns
Write Disable Time	tws	1	-	20	40	-	20	35		15	25	ns
Write Recovery Time	twa		-	30	55	-	30	45	-	15	25	ns

3. CAPACITANCE

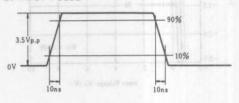
Item	Symbol	Test Condition	H	These		
		lest Condition	min	typ	max	Unit
Input Capacitance	Cin		-	3	5	pF
Output Capacitance	Cont		-	6	8	pF

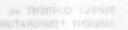
### TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

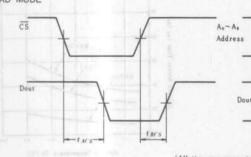


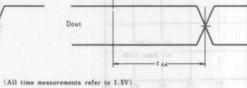
2. INPUT PULSE



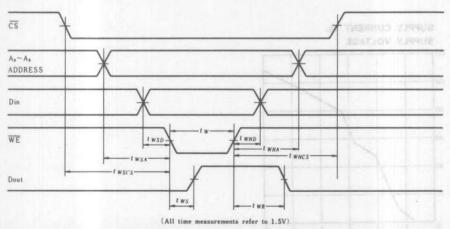


3. READ MODE

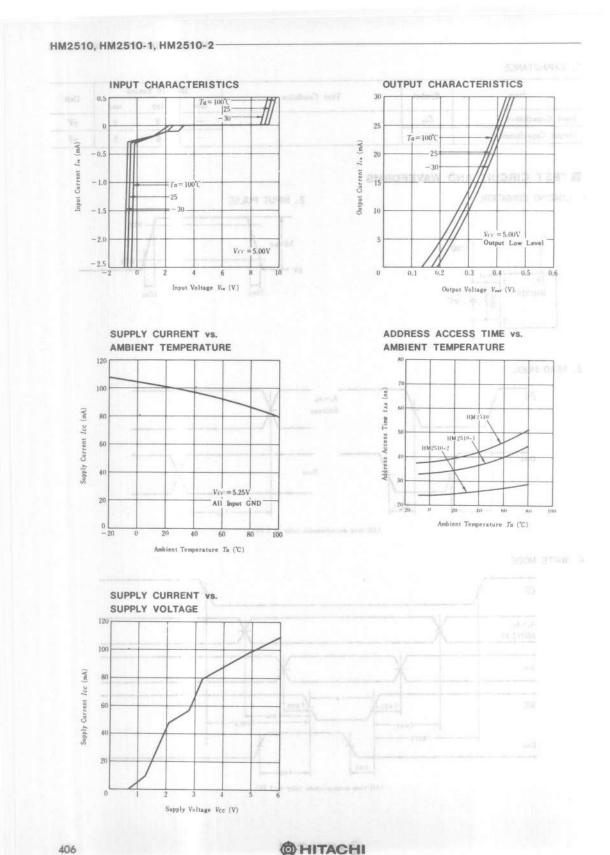




4. WRITE MODE



**OHITACHI** 

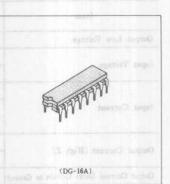


# HM2511, HM2511-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2511 Series item is a 1024-word x 1-bit read/write random access memory with three-state output developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with TTL logic families.

- Level ..... TTL compatible Read access time ..... HM2511: 70ns (max) HM2511-1: 45ns (max) . Chip select access time ..... HM2511: 40ns (max) HM2511-1: 30ns (max)
- Power consumption ..... 0.5mW/bit
- Output ..... three-state



	-	~ ~			
CS	1	0	16	Vcc	
As	2		15	Din	
A,	3	inato/	14	WE	-

PIN ARRANGEMENT

	-		-		
A2	4		13	A,	
- A1	5		12	A	
A.	6		11	A,	
Dout	7	2 8	10	As	
GND	8		9	As	

TRUTH TABLE

	Input		0	Mode		
CS	CS WE Di		Output	Mode		
Н	×	×	High Z	Not Selected		
L	L	L	High Z	Write "0"		
tint) L	L	Н	High Z	Write "1"		
L	Н	×	Dout*	Read		

\* : Read out noninverted

### BLOCK DIAGRAM

40 N. Address Decider  $32 \times 32$ World Drive 310-Memory Cell 1.0-3.0 Sense Amp And Write Drivers o WF Y Address Decoder O Dir è 0 0

#### (Top View) 2. WRITE MODE

# **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	HM2511 Series	Unit				
Supply Voltage	Vcc	-0.5 to +7.0	v	- 111			
Input Voltage	Vin	-0.5 to $+5.5$	v				
Input Current	In	-12 to $+5.0$	mA	-			
Output Voltage (Output High)	Vour	-0.5 to +5.5	v	Industri			
Output Voltage (DC Output Low)	Inst	+20	mA	-			
Storage Temperature	Tera	-65 to +150	°C	and 1			
Storage Temperature	T <sub>ets</sub> (Bias)*	-55 to +125	°C	- 6.0			
	Construction of the second sec						

\* Under Bias



HM	251	1	HM	251	1-1	-

#### ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (Vcc=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

	e		Tid-1 x bron-1	Н	M2511 Ser	ies	Unit
Item	Symbol	lest C	ondition	min	typ	max	Unit
Output Low Voltage	Vol	Vcc=4.75V, IoL=	- 16mA		0.3	0.45	V
1	VIH	Guaranteed Input	Voltage High	2.1	1.6		v
Input Voltage	VIL	Guaranteed Input	Voltage Low		1.5	0.8	V.
110 march	I 1H 1	Vcc=5.25V, Vis=	4.5V	1 a 1 T	0	40	μA
Input Current	I 1H 2	Vcc=5.25V, V=		0	1.0	mA	
	In	Vcc=5.25V, Vis=	0.4V	-	-250	-400	μA
	I OFF 1	Vcc=5.25V, Vest=	-2.4V	-	-	50	μA
Output Current (High Z)	I OFF 2	Vcc=5.25V, Vmt=0.5V		-	1,000	-50	μA
Output Current Short Circuit to Ground	Ios	Vcc=5.25V,	mercente			-100	mA
Output High Voltage	Von	$I_{ON} = -10.3 \text{mA}, V$	/cc=5.0V ±5%	2.4	-	-	V
Input Clamp Voltage	Vi	Vcc-5.25V, I	-10mA	-	-1.0	-1.5	V
		Vcc-5.25V	0≤ <i>Ta</i> <25℃	-	17.1	155	mA
Supply Current	Icc	All input GND	Ta≥25*C		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	130	mA

# •AC CHARACTERISTICS (Vcc=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Sumbal	ymbol Test Condition	HM2511			HM2511-1			Unit
	Symbol		min	typ	max	min	typ	max	Unit
Chip Select Access Time	tacs	here's	-	15	40	-		30	ns
Chip Select to High Z	tznes		-	20	40		Traine	30	ns
Address Access Time	taa		-	40	70	-	35	45	ns

#### 2. WRITE MODE

Item	Symbol	Test Condition	HM2511			HM2511-1			Unit
Item	Symbol	lest Condition	min	typ	max	min	typ	max	Unit
Wrjte Pulse Width	tw	twsa=min	50	25	-	35	10	-	ns
Data Setup Time	twsp	La Del	5	0		5	(-)	-	ns
Data Hold Time	t wn D		5	0		5	-	-	ns
Address Setup Time	t ws a	tw=min	15	0	-	5	-	-	ns
Address Hold Time	t wha	Carlo Carlos	5	0		5		-	ns
Chip Select Setup Time	twacs		5	0	-	5	_	-	ns
Chip Select Hold Time	twncs		5	0	TER	5	1.12	T T I O	ns
Write Disable to High Z	lzws	ators aslend 11	-	20	40		20	35	ns
Write Recovery Time	twn	and another th	-	42	55		30	45	ns

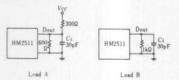
3. CAPACITANCE

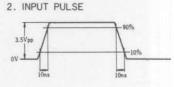
Item	Symbol Test Condition	Test Condition	Н	Date		
		min	typ	max	Unit	
Input Capacitance	Cin		-	3	5	pF
Output Capacitance	Cent		-	9	11	pF



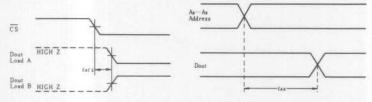
#### TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



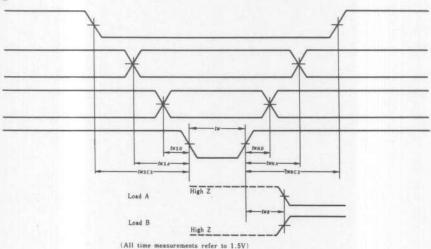


3. READ MODE

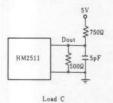


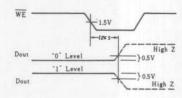
(All time measurements refer to 1.5V)

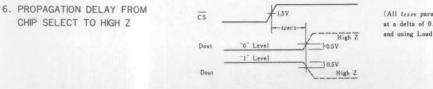
4. WRITE MODE



5. WRITE ENABLE TO HIGH Z DELAY



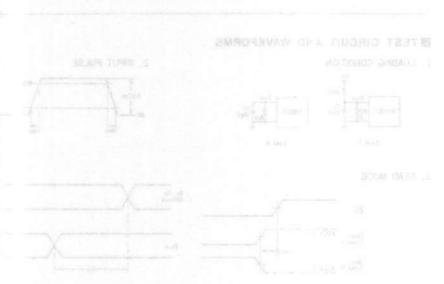




(All Izzzz parameters are measured at a delta of 0.5V from the logic level and using Load C)

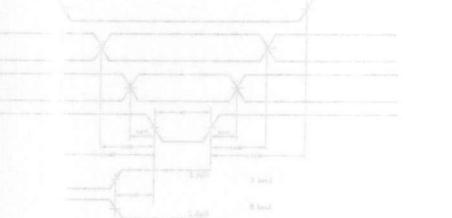
**OHITACHI** 







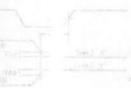


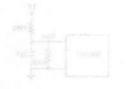




**HITACHI** 







eners data



PRL/PAGATION DE CONTRACTOR DE

#### HOITAN TO INT DRIMMARDORES

liado fe experientement EL a Emitrar autorative and programming plan method analime ELpher programministing and factor programming rise reverse and PRD Mr. Not the Righter reflection.

and a state powering of the hyperbolic Country of the powering more and integration of the powering of the powering of the powering the settle system and the powering of the state of the powering of the pow

To move that the element is programmed proposity as with terms but programming when we up the immediately elements when internet on a statement of the programmed term programming pales and the the track with the programmed with an elements abortion on a state bits. The programmed with, with an elements abortion of the track statement with a statement with a statement of the statement of the programmed with.

Ina arctit new add new extre realized of har offic pairs additional sealars avait the (in PROM etc), allow biggered bottoy auting 1.00 NC and propressing the neutral factor for offic and and multiply provide webting constituted the testeries completened and expression of drawell in archive granemate high propresentables.

EMORALES ESCHO, LISS SECTION)

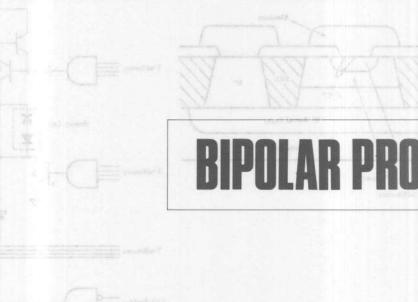
The efforts in manufactured will be all sensingle adds, Toy Winter beams and the descent in allest a states. Tob presences is allest a state. Tob presences is allest a state and the interval bit for a state and the interval bit for the state states. Here, a state of the states may be states and the states and the states of the states and the states are states and the states are states and the states and the states and the states and the states are states and the states are states and the states are states are states and the states are states and the states are states ar

TERMAL PROCEAMING

("even" signt addition! with even it is they industries a tarting it wants guilding a set state production is

In constraint we need to an event of the second of the second sec

Endow 2 weige printer analysis 11 or of the showing printer with all the print a fit frameway and stand it are also printed, to endoge 15 ft



#### PROGRAMMING INFORMATION

Hitachi's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time ordinary PROMs, for the highest reliability.

Fast programming time of typically 7.5µs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Hitachi advanced technology allows very high programmability.

To assure that the element is programmed properly an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed (one programming pulse: Series) bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell.

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and eliability.

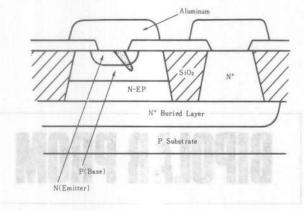


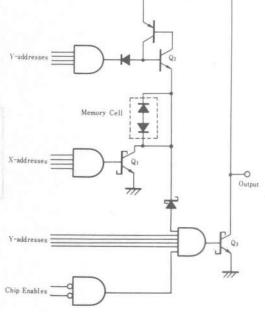
The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using ten address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic in state.

An additional 4 programming pulses (1 programming pulse: S-series) are required to ensure that the bit is fully programmed, and to achieve high reliability. One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at time.

INTERNAL PROGRAMMING CIRCUIT

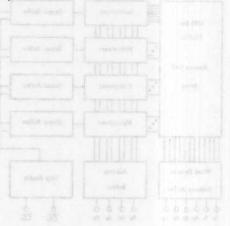




Memory Size	Organization	Output	N-Series	S-Series		
	11.544	0.C.	HN25044 (50ns max)	NITACHI-H28004 and I		
4k	1k×4	3 S	HN25045 (50ns max)	roominable univ decoded		
		0.C.	HN25084 (60ns max)	HN25084S(50ns max)		
	2k×4	3 S	HN25085 (60ns max)	HN25085S(50ns max)		
8k			0.C.	HN25088 (60ns max)	HN25088S(50ns max)	
OK	1k×8	0.0.	HN25088L(100ns max)			
	IK×8	35	HN25089 (60ns max)	HN25089S(50ns max)		
		55	HN25089L(100ns max)	111200030(0013 11118)		
16k	2k×8	0.C.	(or (fully decorded)	HN25168S(60ns max)		
TOK	68.48	3 S	- stutzu	HN25169S(60ns max)		
Pi	rogramming Curren	t	130mA(typ)	90mA(typ)		

Note) O.C. : Open Collector Output 3 S : Three State Output

Hitachi's PROM has two families in accordance with the program specifications. They are usually discriminated by the suffix of the model name. For the S-series PROM, the production technique established for the N-series PROM is further improved to attain very small memory cell area and chip area as well as high performance.



CPUCSMM, PROCEMI

BASSOLUTE VAXIMUM RATINGS (Te-25C)

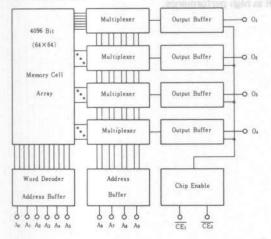
8.2 - 41 8.9-	

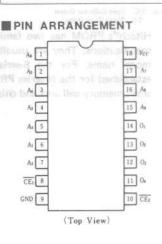
# HN25044, HN25045

1024-word × 4-bit Programmable Read Only Memory The HITACHI HN25044 and HN25045 are high speed electrically programmable, fully decoded TTL Bipolar 4096 bit read only memories organized at 1024 words by 4 bits with on-chip address decoding and two chip enable inputs. The HN25044 and HN25045 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

- FEATURES
- 1024 words x 4 bits organization (fully decoded)
- TTL Compatible inputs and outputs
- Fast read access time; 30 ns typ. (50 ns max.)
- Medium power consumption; 500 mW typ.
- · Two Chip enable inputs for memory expansion
- Open collector outputs (HN25044)/Three-state outputs (HN25045)
- Standard cerdip 18-pin package

#### BLOCK DIAGRAM





(DG+18)

### **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to $+7.0$	V
Input Voltage	V.a.	-0.5 to +5.5	V
Output Voltage	Veut	-0.5 to $+5.5$	V
Output Current	Int	50	mA
Operating Temperature	$T_{ept}$	-25 to +75	°C
Storage Temperature	Tatg	-65 to +150	°C



Item	e 1.1	Symbol Test Condition			HN2504	4 distant	Cherry of	HN2504	5	Unit
Item	Symbol	Test Conditio	n	min	typ	max	min	typ	max	Unit
	Vin			2.0	-	-	2.0	-	-	V
Input Voltage	Vit	132-146	1		-	0.8	-	-	0.8	v
o	Von	$I_{OH} = -2mA$		-	-	-	2.4		-	V
Output Leakage Current	Vol	10L=16mA		-	-	0.45	-	-	0.45	V
Input Current	Im	VIII = 2.7V		-	-	40	-	-	40	μA
	In	V11 = 0.4V		-	-	-0.4	-	-	-0.4	mA
		V <sub>est</sub> =5.5V		-	-	100	-	-	100	
nput Current Dutput Leakage Current nput Clamp Voltage	Ιοικ	$V_{eet} = 0.4 V$		-	-	40	-	-	40	μA
Input Clamp Voltage	Vi	1 = 18mA	churgh	44	(1) <u>(1</u> )	-1.2		ocusted	-1.2	v
Power Supply Current	Icc	Input Either Open or at	Ground	-	100	130	-	100	130	mA
Output Short-circuit Current	Ios	$V_{out} = 0 V$	-	-	1100	mint	15	30	60	mA
Input Capacitance	Cia	$V_{is} = 2V, V_{cc} = 0V$	- animala		5	10		5	. 10	pF
Output Capacitance	Cent	Vevt=0V, Vcc=0V		-	7	12		7	12	pF

DC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to +75°C) TACHEORIE

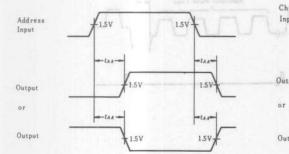
AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

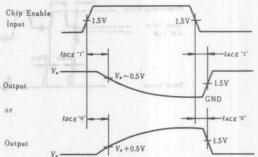
Item	Symbol	min	typ	max	Unit
Address Access Time	t x x	-	35	50	ns
Chip Enable Access Time	TACE	-	20	30	ns
Chip Enable Disable Time	toce	-	20	30	ns

Notes: 1. Typ. value is at  $V_{CC}$ =5.0 V and  $T_a = 25^{\circ}$  C

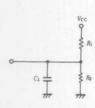
2. Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a  $\Delta V$  of 0.5 V from the active output level.

#### SWITCHING WAVEFORMS





### SWITCHING TIME TEST CONDITIONS



	HN25044		HN25045			
$R_1$	R:	CL	<b>R</b> 1	R:	C <sub>L</sub>	
<b>300Ω</b>	600Ω	30pF	300Ω	600Ω	30pF	
-	-	-	00	600Ω	10pF	
300 Ω	600Ω	10pF	300Ω	600Ω	10pF	
-	-	-	00	600Ω	30pF	
300Ω	600Ω	30pF	300Ω	600Ω	30pF	
	300Ω  300Ω 	R₁         R₂           300Ω         600Ω               300Ω         600Ω	300Ω         600Ω         30pF           -         -         -           300Ω         600Ω         10pF           -         -         -	R1         R2         CL         R1           3000         6000         30pF         3000           -         -         -         ∞           3000         6000         10pF         3000           -         -         -         ∞	R <sub>1</sub> R <sub>2</sub> C <sub>L</sub> R <sub>1</sub> R <sub>2</sub> 300Ω         600Ω         30pF         300Ω         600Ω           -         -         -         ∞         600Ω           300Ω         600Ω         10pF         300Ω         600Ω           -         -         -         ∞         600Ω           -         -         -         ∞         600Ω	

Amplitude - 0V to 3V

Rise and Fall time - 5ns from 1V to 2V

Frequency - 1MHz

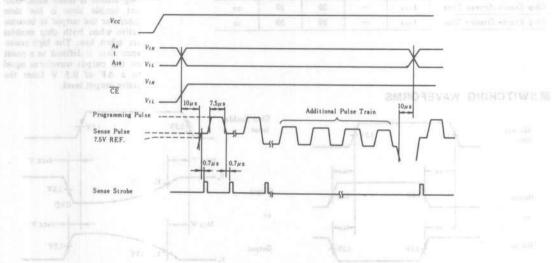
**HITACHI** 

#### HN25044, HN25045-

	Chara	cteristic				Limit	Unit	Notes
Ambient Temperature	Birt	1310	961			25±5	°C	
Programming Pulse	0.5	1		W.B.			140	spot-7 as
Amplitude						$130 \pm 5\%$	mA	
Clamp Voltage						20+0%-2%	v	
Ramp Rate						70max	V/µs	man and a series
Pulse Width						7.5±5%	μs	10V point/150Ω load
Duty Cycle					-	70% min	Ere :	
Sense Current		1.0-	-	1		Vie Con at	fri.	
Amplitude						20±0.5	mA	
Clamp Voltage						20+0%-2%	V	and standing and standing of the standing of t
Ramp Rate						70max	V/µs	10V point/150Ω load
Sense current interr	uption	before a	nd after	address	s change	10min	μs	spatioV uses, 7 fir
Programming Vcc	-	107	1001	-	heavil	5.0+5%-0%	56 V	Paratal (1998) in
Maximum Sensed Volta	ge for	program	nmed "1	•		7.5±0.1	v	oper Stamping Courses
Delay from trailing edg output voltage	e of pr	ogrammi	ing puls	e before	sensing	0.7min	μs	and States
Programming Time All	ocation	/Bit	at all a			100max	ms	
Additional Programming	g Pulse	Number	r	C-94		4-1	Time	CONTOSEMUS D

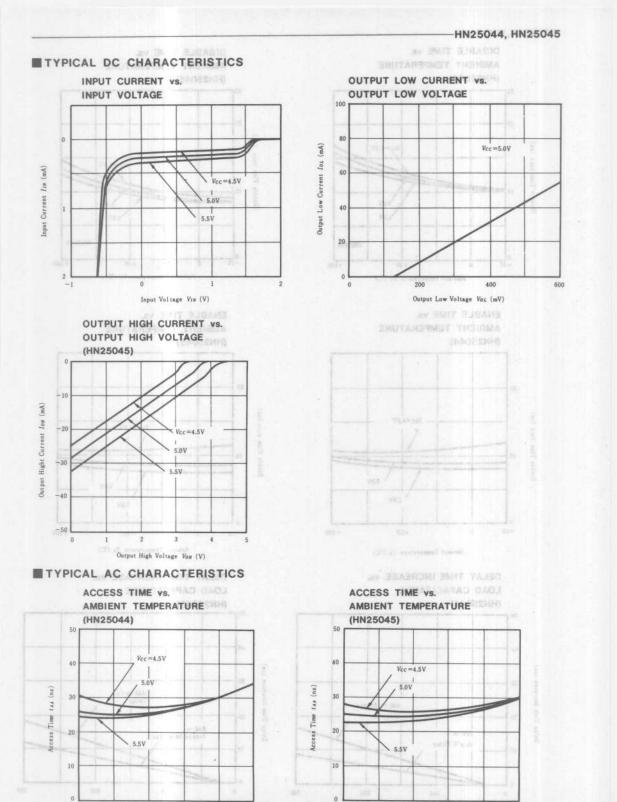
PROGRAMMING SPECIFICATION

TYPICAL WAVEFORMS



			WITCHING
china			
		50013	

**HITACHI** 





+100

-25 0 +50

Ambient Temperature To ('C)

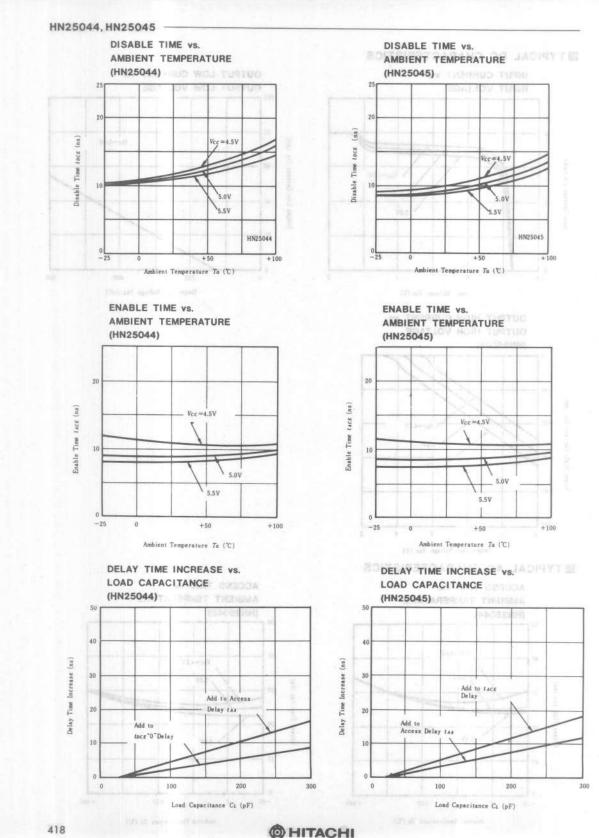
-25 0

+50

Ambient Temperature Ta (°C)

417

+100



# HN25084, HN25085

2048-word × 4-bit Programmable Read Only Memories The HITACHI HN25084 and HN25085 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 word by 4 bit with on-chip address decoding and one chip enable input. The HN25084 and HN25085 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

#### FEATURES

- 2048 word x 4 bit organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084)/Three-state outputs (HN25085)
- Standard cerdip 18-pin dual in-line package

#### OPERATION

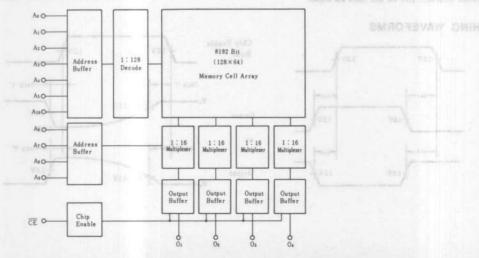
Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing  $\overline{CE}$  to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

#### • Reading

To read the memory the device is enabled by bringing  $\overline{CE}$  to a logic "zero". The outputs then correspond to the data programmed in the selected word.

#### LOGIC DIAGRAM



**OHITACHI** 

(DG-18)

#### PIN ARRANGEMENT



(Top View)

Decelo unit con l'anti-

#### HN25084, HN25085-

ONNEL PRODUCEMEN

#### **BABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	Vin	-0.5 to +5.5	v
Output Voltage	Vaut	-0.5 to $+5.5$	v
Output Current	I out	50	mA
Operating Temperature	Tapr	-25 to +75	°C
Storage Temperature	Tela	-65 to +150	°C

#### **DC CHARACTERISTICS** ( $V_{cc}=4.75$ to 5.25V, Ta=0 to 75°C)

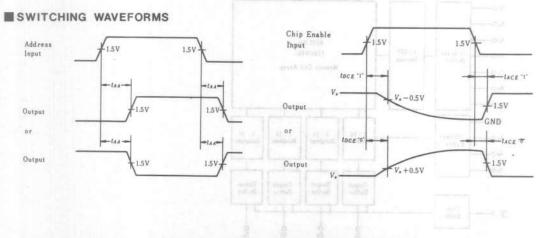
Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	VIN	ets.	2.0	(arueri e	ditesen o	V
Input Low Voltage	VIL	(80 m mas)	101/1-201	the reasons.	0.8	v
Input High Current	I IH	V1-2.7V	ing ruon	0000000	40	μA
Input Low Current	-In	V1=0.4V		-	0.40	mA
Output Low Voltage	Vol	<i>I</i> <sub>0L</sub> =16mA	-	-	0.45	V
Output Leakage Current	I OLK 1	V_0=5.25V 1000000000	ni o <del>ri</del> an	h nue 1	100	μA
Output Leakage Current	I OLK 2	Vo=0.4V	-		40	μA
Input Clamp Voltage	Vi	$I_l = -18 \text{mA}$	-	-	-1.2	N OP N
Power Supply Current	Icc	Inputs Either Open or at Ground	Volume.	110	150	mA
Output High Voltage*	VOH	$I_o = -2 \mathrm{mA}$	2.4	-		V
Output Short Circuit Current*	-Ios	Vo-OV	15	Section and	60	mA

**AC CHARACTERISTICS** (Vcc-4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max 🔛	Unit
Address Access Time	t AA	led by bringing CE to a logit	hina n <u>so</u> iraí	40	60	ns
Chip Enable Access Time	tACE	19 TH DOLENN GO 10 10 10 10 10	N DRUGE_TEX.	25	35	ns
Chip Enable Disable Time	t dce			25	35	ns

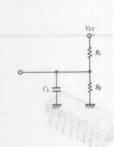
Note) 1. Output Load: See Test Circúit. 2. Measurement Reference: 1.5V for both inputs and outputs.

ELOGIC DIAGR



HITACHI

#### SWITCHING TIME TEST CONDITIONS



SWITCHING	HINON	N25084		iff ald	HN25085	
PARAMETER	Ri	R	CL	Ri	R:	CL
taa	300Ω	600Ω	30pF	300Ω	600Ω	.30pF
tace "1"	01112 <u>15</u> 1	103:20	10102-0	00	600Ω	10pF
tace "0"	300 D	600Ω	10pF	300Ω	600Ω	10pF
toce "1"	nol Exc	1110	and The	00	600Ω	30pF
toce "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

**IFEATURES** 

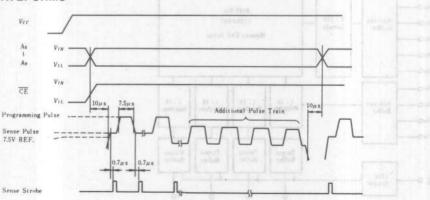
Amplitude-0V to 3V Rise and Fall time-5ns from 1V to 2V Frequency-1MHz

### PROGRAMMING SPECIFICATION

Faul ried social films: 26 ht typ. (60 nt mail)
 Medium power consumption: 660 mW typ.

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	*C	©pan contrator outp
Programming Pulse Amplitude Clamp Voltage Ramp Rate Pulse Width Duty Cycle	70.01	mA V V/μs μs	10V point/150Ω load
Sense Current Amplitude Clamp Voltage Ramp Rate Sense Current Interruption before and after address change	20±0.5 20±2% 70max 10min	mA V V/μs μs	golphins vid betrieb
Programming Vcc	5.0+5%-0%	V	hing tencentoge the girefa
Maximum Sensed Voltage for programmed "1"	7.5±0.1	V	To read the memory t
Delay from trailing edge of programming pulse before sensing output voltage	0.7min	μs	<sup>d</sup> zero <sup>d</sup> . The outputs the
Programming Pulse Number	100max	ms	
Additional Programming Pulse Number	4	Time	MARDAID DIDOUS





**HITACHI** 

# HN25084S, HN25085S

#### OLLINGO 1531 3411 DEHOLINS I

# 2048-word×4-bit Programmable Read Only Memories

The HITACHI HN25084S and HN25085S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 words by 4 bits with on-chip address decoding and one chip enable input. The HN25084S and HN25085S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

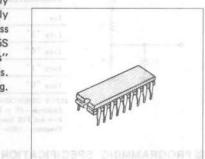
#### FEATURES

- 2048 words x 4 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084S)/Three-state outputs (HN25085S)
- Standard cerdip 18-pin dual in-line package.
- OPERATION
- Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing  $\overline{CE}$  to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

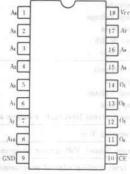
#### Reading

To read the memory the device is enabled by bringing  $\overline{CE}$  to a logic "zero". The outputs then correspond to the data programmed in the selected word.



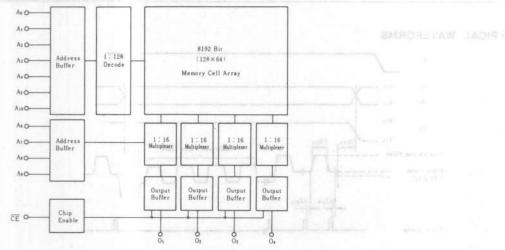
#### PIN ARRANGEMENT

(DG-18)



(Top View)

#### LOGIC DIAGRAM



**OHITACHI** 

#### BABSOLUTE MAXIMUM RATINGS

SWITCHING THAT TEST CONDITION

Item	Symbol	Rating	Unit	
Supply Voltage	Vcc	-0.5 to +7.0	V	PERAMETER
Input Voltage	Vis	-0.5 to +5.5	V	
Output Voltage	Vint	-0.5 to +5.5	v	"1" and
Output Current	Int	50	mA	-0" stel
Operating Temperature	Tope	-25 to +75	°C	"I" zai)
Storage Temperature	Tue	-65 to +150	°C	-0" and

#### DC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Tes	Condition:	5	min	typ	max	Unit
Input High Voltage	VIN			INC.	2.0	1995 D	externa ex	v
Input Low Voltage	VIL	THE STATE			-	and the second s	0.8	v
Input High Current	Ітя	V1-2.7V			-	-	40	μA
Input Low Current	$-I_{IL}$	V1=0.4V			-		0.40	mA
Output Low Voltage	Vol	I				-	0.45	v
Output Leakage Current	IOLKI	Vo=5.25V	28	10	-		100	μA
Output Leakage Current	IOLKI	Vo-0.4V	点,能	49. j.	-	-	40	μA
Input Clamp Voltage	V,	$I_{I} = -18 \text{mA}$	1.0	Sec. 1	-	-	-1.2	v
Power Supply Current	Icc	Inputs Either Og	oen or at G	round	-	110	160	mA
Output High Voltage*	Von	I2mA			2.4	-	200	O anV
Output Short Circuit Current*	$-I_{os}$	Vo-OV	19.1		15	_	60	mA

\* Note: Applicable to HN25089 only.

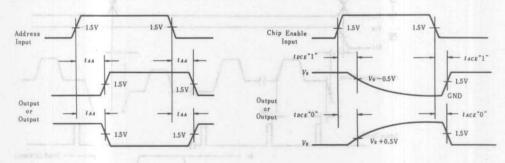
#### AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	taa	1.2	-	25	50	ns
Chip Enable Access Time	IACE.		-	20	35	ns
Chip Enable Disable Time	toce			15	35	ns

Note) 1. Output Load: See Test Circuit.

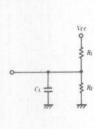
2. Measurement Reference: 1.5V for both inputs and outputs.

#### SWITCHING WAVEFORMS



#### HN25084S, HN25085S-

## SWITCHING TIME TEST CONDITIONS



SWITCHING	1	HN25084	5	1	HN25085	5	
PARAMETER	<i>R</i> <sub>1</sub>	R <sub>2</sub>	CL	<i>R</i> <sub>1</sub>	Ra	CL	
1.**	300Ω	600Ω	30pF	300Ω	600Ω	30pF	
tace "1"	÷	-	21.4	00	600Ω	10pF	
tace "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF	
1 DCE "1"	- <u></u>	- 3	tie o <del>g</del> eli	00	600Ω	30pF	
t DCE "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF	which the part of the second

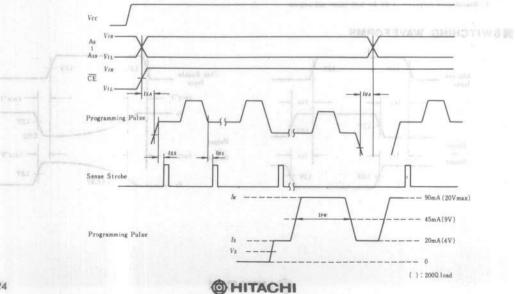
INPUT CONDITIONS

Amplitude - 0V to 3V Rise and Fall time - 5ns from 1V to 2V

Frequency-1MHz

#### **PROGRAMMING SPECIFICATION**

PARAMI	ETER		Symbol	min	typ	max	Unit	Note
Ambient Temperature			Ta	20	25	30	*C	Toplates Ship addi
Programming Vcc		-	Vec	4.75	5.0	5.25	v	and the second
Programming Pulse Amplitude	-	-	Iw	88	90	92	mA	imple takey writte
Clamp Voltage Ramp Rate Pulse Width			Vw t pw	19.0 10 7.1	19.5 	20.0 70 7.9	V V/µs µs	9V point/200Ω load
Duty Cycle	201	-	hunor	70	noiti nin	l = ssl	%	Passes Stuppe Corners
Sense Current Amplitude Sense Voltage Clamp Voltage Ramp Rate	-	3.2 6)	Is Vs	19 7.4 19.0 70	20 7.5 19.5 —	21 7.6 20.0	mA V V V/µs	Ourput High Vallage* (Saget Reim Frecalt Co Nov. Instantion 1711) 8 AGC CHARACT
Address Setup Time Address Hold Time Sense Setup Time Sense Hold Time	(1) (1)	da 	t 5A t HA t 55 t HS	10 10 0.7 0.7	er		μs μs μs μs	Chevro Charles (1997) Chevro Accese View
Additional Programmin	g Pulse			1	1	1.1	time	Chip Scattle Access Ten-
Programming Pulse N	umber p	er bit	n	-	-	10000	time	etti sunno suces der-



# HN25088, HN25089

1024-word × 8-bit Programmable Read Only Memories The HITACHI HN25088 and HN25089 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088 and HN25089 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

#### FEATURES

- 1024 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 40 ns (typ), 60 ns (max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088)/Three-state outputs (HN25089)
- Standard cerdip 24-pin dual in-line package

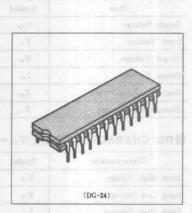
### OPERATION

#### Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing  $\overline{CE1}$  and/or  $\overline{CE2}$  to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

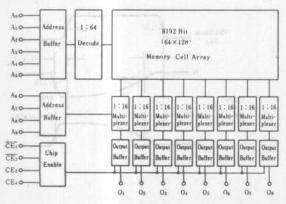
To read the memory the device is enabled by bringing  $\overline{CE1}$  and  $\overline{CE2}$  to a logic "zero". CE3 and CE4 to a logic "one". The outputs them correspond to the data programmed in the selected word.

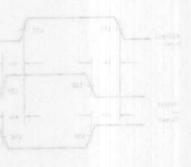






#### LOGIC DIAGRAM





**OHITACHI** 

#### HN25088, HN25089-

The lot of the second s

# **MABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	Vin	-0.5 to +5.5	v
Output Voltage	Vest	-0.5 to +5.5	v
Output Current	I out	50	mA
Operating Temperature	$T_{epr}$	-25 to +75	°C
Storage Temperature	Tere	-65 to +150	°C

# DC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to +75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	VIH	2110	2.0	guq <del>ro</del> o	tdiase <del>rs</del> ed	V
Input Low Voltage	VIL	), 60 ns (max)	148)-an (	b second s	0.8	V
Input High Current	IIN	V1-2.7V	1000	0001200	40	μA
Input Low Current	-In	V1-0.4V	0.00 000	-	0.40	mA
Output Low Voltage	Vol	<i>I</i> <sub>04</sub> = 16 m A	-	-	0.45	V
Output Leakage Current	IOLKI	V_o=5.25V	ll-reiten)	elu=3	100	μA
Output Leakage Current	IOLKS	Va=0.4V	-	-	40	μA
Input Clamp Voltage	Vi	$I_l = -18 \text{mA}$	-	-	-1.2	V
Power Supply Current	Icc	Inputs Either Open or at Ground	-	120	160	mA
Output High Voltage*	Voн	$I_{OH} = -2 \mathrm{m} \mathrm{A}$	2.4	00000-00	1180 8110	V
Output Short Circuit Current*	-Ios	Vo-OV	15	-	60	mA

\* Note: Applicable to HN25089 only.

# AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

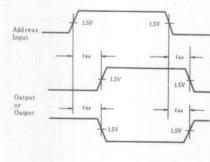
Characteristic	Symbol	Test Conditions	otoo min to	typ	max	Unit
Address Access Time	t A A	biquote el	unig 'pr <del>ig</del> de	40	60	ns
Chip Enable Access Time	tACE			20	35	ns
Chip Enable Disable Time	toce	ed by bringing GE1 and CE	10800 11 <u>10</u> 010 11	20	35	ns

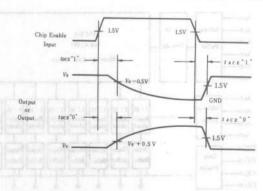
Note) 1. Output Load: See Test Circuit.

SWITCHING WAVEFORMS

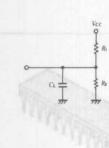
2. Measurement Reference: 1.5V for both inputs and outputs.

MARDAID DIAGRAM





# SWITCHING TIME TEST CONDITIONS



SWITCHING	tomet	HN25088		P etd	HN25089			
PARAMETER	<i>R</i> <sub>1</sub>	Rı	CL	<b>R</b> 1	Rı	CL		
LAA	300Ω	600Ω	30pF	300 M	600Ω	30pF		
tace "1"	200	a the	-	00	600Ω	10pF		
tace "0"	300 D	600Ω	10pF	300Ω	600Ω	10pF		
t de "1"	betted		ni ten	00	600Ω	30pF		
toce "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF		

INPUT CONDITIONS

Amplitude - 0V to 3V

Rise and Fall time-5ns from 1V to 2V Frequency-1MHz

3 3 33 1 T A 3 3 4

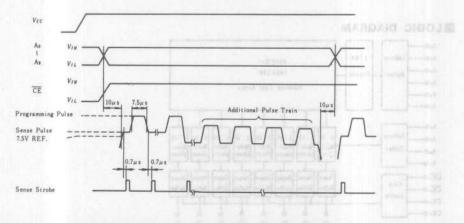
\$024 words x 8 bits organization ffully decede

PROGRAMMING SPECIFICATION

TTL competicle inputs and purparts

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	<ul> <li>Four dito enablis int</li> </ul>
Programming Pulse	SS/Three-state out	ins (8742508	· Doen collector sure
Amplitude	$130\pm5\%$	mA	(299021044)
Clamp Voltage	$20\pm2\%$	V	<ul> <li>Standard cerdip 24</li> </ul>
Ramp Rate	70max	V/µs	The second conversion of
Pulse Width	$7.5 \pm 5\%$	μs	10V point/150Ω load
Duty Cycle	70% min		四 OPERATION
Sense Current			a recipantoury
Amplitude	20±0.5	mA	A logic one case to a
Clamp Voltage	20±2%	V	loeston by using prop
Ramp Rate	70max	V/µs	selected by this win
Sense Current Interruption before and after address change	10min	µs 1	disabled by bringing
Programming Vcc	5.0+5%-0%	v	sad/or CE4 to s 40
Maximum Sensed Voltage for programmed "1"	7.5±0.1	v	a sarind Bulanue Bold
Delay from trailing edge of programming pulse before sensing output voltage	0.7min	belle µs	en achtilomat pulse to i
Programming Pulse Number	100max	ms	European of
Additional Programming Pulse Number	4	Time	to a louis "and" CE

brow testaste and in formmanion while and to broothings



# HN25088S, HN25089S

1024-word × 8-bit Programmable Read Only Memories The HITACHI HN25088S and HN25089S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit-read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088S and HN25089S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

#### FEATURES

- 1024 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088S)/Three-state outputs (HN25089S)
- Standard cerdip 24-pin dual in-line package

# OPERATION

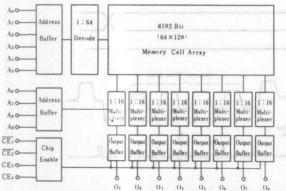
#### Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing  $\overline{CE1}$  and/or  $\overline{CE2}$  to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory the device is enabled by bringing  $\overline{CE1}$  and  $\overline{CE2}$  to a logic "zero", CE3 and CE4 to a logic "one". The outputs then correspond to the data programmed in the selected word.

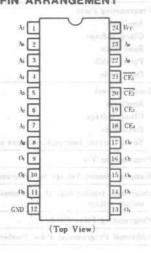


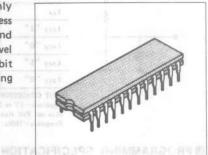


**MITACHI** 

PIN ARRANGEMENT

(DG-24)





#### -HN25088S, HN25089S

#### **BABSOLUTE MAXIMUM RATINGS**

SWITCHING THE TEST CONDITIONS

Item	Symbol	Rating	Unit	
Supply Voltage	Vcc	-0.5 to +7.0	v	ABAMETER
Input Voltage	V 000	-0.5 to +5.5	v	
Output Voltage	Vest	-0.5 to +5.5	v	*1* av
Output Current	Int	C2004 19401 50 4	mA	"Q" 10
Operating Temperature	Ter.	-25 to +75	°C	11.00
Storage Temperature	Tere	-65 to +150	"C	"0" sa

#### DC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to +75°C)

Characteristic	Symbol	Test Conditions			min	typ	max	Unit
Input High Voltage	VIH	1		MC	2.0	2.0 -	10Mittan	DO V
Input Low Voltage	VIL	100	ala a	Lune	-	17.12	-0.8	v
Input High Current	Im	V1 = 2.7V	100		-	<u> </u>	40	μA
Input Low Current	-In	V/=0.4V		- the	-	-	0.40	mA
Output Low Voltage	Vol	<i>I</i> ot 16 m A				-	0.45	v
Output Leakage Current	IOLKI	Vo-5.25V	.28	18	-	-	100	μA
Output Leakage Current	IOLK :	Vo=0.4V	1979E	100	-	-	40	μA
Input Clamp Voltage	Vi	I1 = -18mA	2.1	web.	-	-	-1.2	v
Power Supply Current	Icc	Inputs Either O	pen or at G	round	-	120	160	mA
Output High Voltage*	Von	$I_{OH} = -2 \mathrm{m} \mathrm{A}$	1		2.4	-	2010/01/2	v
Output Short Circuit Current*	-Ios	Vo=0V			15	-	60	mA

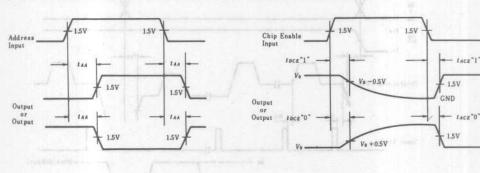
# AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t AA	- 10 m	-	25	50	ns
Chip Enable Access Time	LACE	1 1.		20	35	ns
Chip Enable Disable Time	LDCE		-136 -	15	35	ns

Note) 1. Output Load : See Test Circuit.

2. Measurement Reference: 1.5V for both inputs and outputs.

# SWITCHING WAVEFORMS

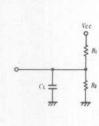


**OHITACHI** 

# HN25088S, HN25089S-

### SWITCHING TIME TEST CONDITIONS

Ra

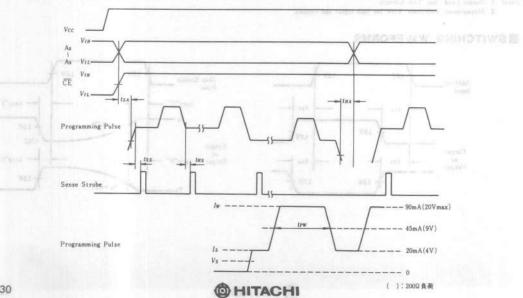


SWITCHING	and I	IN 250883	3	I	IN 25089 S	S	
PARAMETER	Ri	R:	CL	Rı	Rz	CL	
taa	300 D	Ω00a	30pF	300Ω	600Ω	30pF	tapik Voltage
tace "1"	-	-	$(-\tau)$	00	600Ω	10pF	
tace "0"	300 D	600Ω	10pF	300Ω	600Ω	10pF	
toce "1"	-	-	1.1 1	00	600Ω	30pF	
1 DCE "0"	300 D	600Ω	30pF	300Ω	£000	30pF	

INPUT CONDITIONS

Amplitude-0V to 3V Rise and Fall time-5ns from 1V to 2V Frequency-1MHz

ON						
Symbol	min	typ	max	Unit	Note	
Ta	20	25	30	*C	and the Conversion	
Vcc	4.75	5.0	5.25	v	MATHC	
		A.#37*	103		Output Love Voltage	
Iw	88	90	92	mA	(avoid states) input)	
Vw	19.0	19.5	20.0	V	Cutput Ludage Correct	
	10	-	70	V/µs	the case officient radius	
t pw	7.1	7.5	7.9	μs	9V point/200Ω load	
5.0	70	I welling an		%	Person Structure Connect	
		Aust -			Control Malti Ported	
Is	19	20	21	mA		
Vs	7.4	7.5	7.6	v	Origina Share Create Co-	
	19.0	19.5	20.0	V	Martin Applements of Records	
	70	-	-	V/µs		
tsx	10	0.52 1 20 3	0.0-70	μs	BAC CHARACTE	
t HA	10	-		μs	Character contactor	
tss	0.7	-		μs	La Line Constante.	
t HS	0.7	-	- 111	μs	mit T tesaste surifici	
	1	1	1	time	and internet when a light	
п	-	-	10000	time	Celo Cable Dealer 7 p	
	Ta Ta Vcc Iw Vw trw trw tss tss tss tss tss tss tss tss	Symbol         min           Tα         20           Vcc         4.75           Iw         88           Vw         19.0           10         10           trw         7.1           70         70           Is         19           Vs         7.4           19.0         70           tss         10           tss         0.7           tss         0.7           tss         0.7           1         1	$\begin{tabular}{ c c c c c } \hline Symbol & min & typ \\ \hline Ta & 20 & 25 \\ \hline Vcc & 4.75 & 5.0 \\ \hline Iw & 88 & 90 \\ \hline Vw & 19.0 & 19.5 \\ 10 & - \\ t_{PW} & 7.1 & 7.5 \\ \hline 70 & - \\ \hline Is & 19 & 20 \\ \hline Vs & 7.4 & 7.5 \\ \hline 19.0 & 19.5 \\ \hline 70 & - \\ \hline Is & 19 & 20 \\ \hline Vs & 7.4 & 7.5 \\ \hline 19.0 & 19.5 \\ \hline 70 & - \\ \hline t_{ss} & 10 & - \\ t_{ss} & 10 & - \\ t_{ss} & 0.7 & - \\ \hline t_{ns} & 0.7 & - \\ \hline 1 & 1 \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c c c } \hline Symbol & min & typ & max \\ \hline Ta & 20 & 25 & 30 \\ \hline Vcc & 4.75 & 5.0 & 5.25 \\ \hline Iw & 88 & 90 & 92 \\ Vw & 19.0 & 19.5 & 20.0 \\ & 10 & - & 70 \\ t_{Fw} & 7.1 & 7.5 & 7.9 \\ \hline 70 & - & - \\ \hline Is & 19 & 20 & 21 \\ Vs & 7.4 & 7.5 & 7.6 \\ \hline 19.0 & 19.5 & 20.0 \\ \hline 70 & - & - \\ \hline Is & 10 & - & - \\ \hline Is & 10 & - & - \\ \hline Is & 10 & - & - \\ \hline Is & 0.7 & - & - \\ \hline Is & 0.7 & - & - \\ \hline 1 & 1 & 1 \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	



# HN25088L, HN25089L

#### 1024-word × 8-bit Programmable Read Only Memories

The HITACHI HN25088L and HN25089L are low power and high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 1024 words by 8 bits with onchip address decoding and four chip enable inputs.

The HN25088L and HN25089L are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

#### FEATURES

- 1024 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 60ns typ. (100ns max.)
- Low power consumption: 350mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088L)/Three-state outputs (HN25089L)



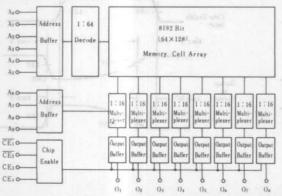
#### Programming

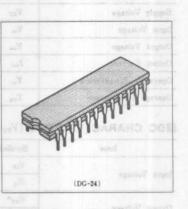
A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing  $\overline{CE1}$  and/or  $\overline{CE2}$  to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

#### Reading

To read the memory the device is enabled by bringing CE1 and CE2 to a logic "zero", CE3 and CE4 to a logic "one". The outputs then correspond to the data programmed in the selected word.





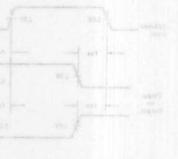


#### PIN ARRANGEMENT



(Top View)

25WITCHING WAVEFORMS



#### HN25088L, HN25089L

#### **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to $+7.0$	v
Input Voltage	Via	-0.5 to +5.5	V
Output Voltage	Vout	-0.5 to +5.5	V V
Output Current	Imi	50	mA
Operating Temperature	Tapr	-25 to $+75$	.c
Storage Temperature	Teta	-65 to $+150$	°C

#### **DC CHARACTERISTICS** ( $V_{cc}$ =4.75 to 5.25V, Ta=0 to +75°C)

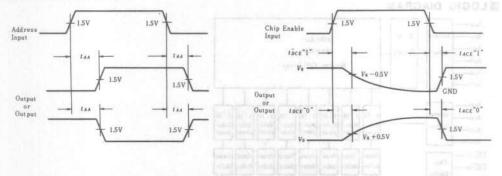
and the second second second		typ	max	Unit
	2.0	an Tre	-Ormania	v
(Jaoim 2001) .	6 at 53	times	0.8	v
$V_{OH} = -2 \mathrm{mA}$ GVO V	2.4	ojn <del>a-</del> arv	NOS 1 <del>03</del> 101	v
loL=16mA	011561_10	din <u>1.</u> 4.9	0.45	v
V <sub>1</sub> =2.7V	ana) _200	200-0	40	μA
$V_t = 0.4 V$	-	-	0.4	mA
Vo=5.25V	-	-	100	
V_a=0.4V	-		40	μA
nputs Either Open or at Ground	-	70	100	mA
<i>V<sub>0</sub></i> =0V	8	175 <u>-</u> 16	30	mA
$T_{I} = -18 \mathrm{mA}$	ante <u>E</u> uru		-1.2	V
1				

#### AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to +75°C)

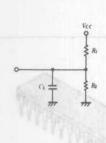
Item	Symbol	min	typ	max	Unit
Address Access Time	taa	Tergota	60	100	ns h
Chip Enable Access Time	tACE	-	40	70	ns
Chip Enable Disable Time	toce	by beinging f	40	70 70	ns

Notes) 1. Output Load: See Test Circuit 2. Measurement Reference: 1.5V for both inputs and outputs

#### SWITCHING WAVEFORMS



#### SWITCHING TIME TEST CONDITIONS



SWITCHING	home	IN250881	O bas	HN25089L		
PARAMETER	<i>R</i> <sub>1</sub>	R:	CL	R <sub>1</sub>	Rı	CL
tAA	300Ω	600Ω	30pF	300Ω	600Ω	30pF
tACE "1"	1000	900 <u>2-</u> 01		00	600Ω	10pF
tace "0"	300 Ω	600Ω	10pF	300Ω	600Ω	10pF
t DCE "1"	1 1.5	ales Del	est Type	00	600Ω	30pF
toce "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS

Amplitude-0V to 3V

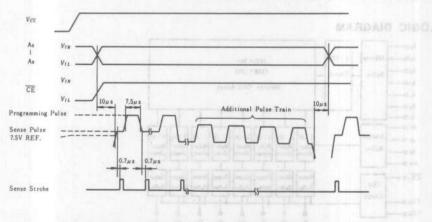
Rise and Fall time-5ns from 1V to 2V Frequency-1MHz

23RUTABR

#### PROGRAMMING SPECIFICATION

Limit Unit Notes Characteristic  $25\pm5$ °C Ambient Temperature 1.0 **Programming** Pulse Amplitude 130±5% mA Clamp Voltage  $20 \pm 2\%$ V · Standard oard o Ramp Rate V/µs 70max Pulse Width 7.5±5% 10V point/150Ω load #s Duty Cycle 70% min Sense Current 20±0.5 Amplitude mA Clamp Voltage 20±2% V Ramp Rate 70max V/us Sense Current Interruption before and after address change 10min µs. V Programming Vcc 5.0+5%-0% Maximum Sensed Voltage for programmed "1" V  $7.5 \pm 0.1$ Delay from trailing edge of programming pulse before sensing 0.7min µs output voltage Programming Pulse Number 100max ms 4 Time Additional Programming Pulse Number

concernation of the data programment in the selection word



# HN25168S, HN25169S

2048-word × 8-bit Programmable Read Only Memories The HITACHI HN25168S and HN25169S are high speed electrically programmable, fully decoded TTL Bipolar 16384 bit read only memories organized as 2048 words by 8 bits with on-chip address decoding and three chip enable inputs. The HN25168S and HN25166S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

#### FEATURES

- 2048 words x 8 bits organization (fully decoded)
- TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 600 mW typ.
- Three chip enable inputs for memory expansion.
- Open collector outputs (HN25168S)/Three-state outputs (HN25169S)
- Standard cerdip 24-pin dual in-line package

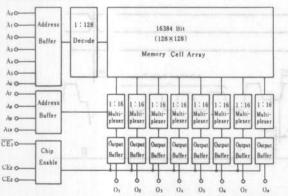
## OPERATION Programming

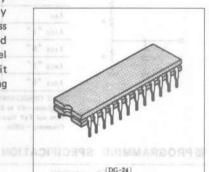
A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired world is selected by the eleven address inputs in TTL level. The device is disabled by bringing CE1 to as logic "one" or CE2 and/or CE3 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse is applied, then is stopped.

#### Reading

To read the memory the device is enabled by bringing  $\overline{CE1}$  to a logic "zero", CE2 and CE3 to a logic "one". The outputs then correspond to the data programmed in the selected word.







#### PIN ARRANGEMENT

A7 1	$\cup$	24 Vee
A 2		23 Au
AL 3		22 40
Au 4		21 Ato
Au 5		20 CE1
A 6		19 CE:
Ai 7		18 CEa
30 11		17 04
01 9		16 0;
Or 10		15 04
O <sub>1</sub> 11		14 01
ND 12		13 0,

#### BABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	
Supply Voltage	Vcc	-0.5 to +7.0	v	RETRIESS
Input Voltage	Vin	-0.5 to +5.5	v	
Output Voltage	Veer	-0.5 to +5.5	v	1. 1. 1
Output Current	I aut	50	mA	101 -
Operating Temperature	$T_{spr}$	-25 to +75	•С	111
Storage Temperature	Tete	-65 to +150	°C	1.181.2

#### DC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to +75°C)

Characteristic	Symbol	Tes	t Conditions		min	typ	max	Unit
Input High Voltage	VIN			ИСП	2.0	IGTSP	NAME OF	V
Input Low Voltage	Vil			T in a	-	5.	0.8	v
Input High Current	Іт	V1-2.7V	20		-	-	40	μA
Input Low Current	-114	V1-0.4V			-	-	0.40	mA
Output Low Voltage	Vol	$I_{0L} = 16 \mathrm{mA}$			-	-	0.45	v
Output Leakage Current	IOLKI	Vo=5.25V	15	a3 -	-	-	100	μA
Output Leakage Current	IOLKI	Vo-0.4V	9.95	45	-	-	40	μA
Input Clamp Voltage	V <sub>1</sub>	I/=-18mA	1.5	web	-	-	-1.2	v
Power Supply Current	Icc	Inputs Either O	pen or at G	round	-	120	170	mA
Output High Voltage*	Von	$I_{OH} = -2 \mathrm{m} \mathrm{A}$			2.4	-	- <u>1-1</u> 2/17	v
Output Short Circuit Current*	-los	Vo-OV	100	1	15	-	60	mA

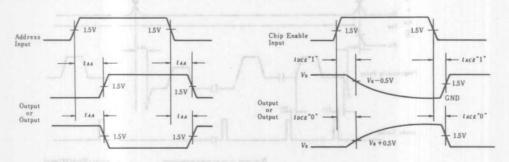
\* Note: Applicable to HN25169S only.

#### AC CHARACTERISTICS (Vcc=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	- In		1999-132-1610	Unit
Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	taa	- 5.4	-	40	60	ns
Chip Enable Access Time	LACE		-	20	35	ns
Chip Enable Disable Time	t DCE			20	35	ns

Note) 1. Output Load: See Test Circuit. 2. Measurement Reference: 1.5V for both inputs and outputs.

#### SWITCHING WAVEFORMS



#### SWITCHING TIME TEST CONDITIONS

		Vec
		Î RI
-	-	1
	$a \neq$	₹ R2
	777	

SWITCHING	ł	IN251685	5	ł	IN251698	5	
PARAMETER	R <sub>1</sub>	Rı	CL	R <sub>1</sub>	Rı	C <sub>L</sub>	
taa	300 D	600Ω	30pF	300Ω	600Ω	30pF	
tace "1"	+	-	$(\overline{c}, \overline{c}) \in [0, 1]$	00	600Ω	10pF	
tACE "0"	300 <i>Ω</i>	600Ω	10pF	300Ω	600Ω	10pF	
toce "1"	-	-	1	00	600Ω	30pF	
t DCE "0"	300Ω	600Ω	30pF	300Ω	600£	30pF	warmon Temperature

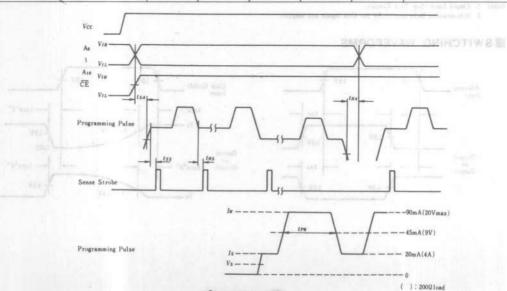
INPUT CONDITIONS

Amplitude - 0V to 3V

Rise and Fall time-5ns from 1V to 2V Frequency-1MHz

#### **PROGRAMMING SPECIFICATION**

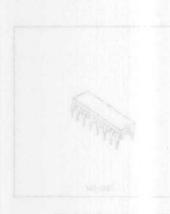
PARAMETER			Symbol	min	typ	max	Unit	Note
Ambient Temperature			Ta	20	25	30	°C	control of the state of the
Programming Vcc			Vcc	4.75	5.0	5.25	v	NOR CONCERNENT INCOME
Programming Pulse	-	1			A Starty of			shows per many
Amplitude			Iw	88	90	92	mA	Griper Letters Correct
Clamp Voltage			Vw	19.0	19.5	20.0	V	Orque Lookage Carried
Ramp Rate				10	-	70	V/µs	
Pulse Width			t pw	7.1	7.5	7.9	μs	9V point/200Ω load
Duty Cycle			. Deste	70	2-1940	- 1	%	Parer Sugir Carren
Sense Current		1.2		_	1.05-1			Control Martin Control
Amplitude			Is	19	20	21	mA	
Sense Voltage			Vs	7.4	7.5	7.6	V	Output Slagt Cleant Co
Clamp Voltage				19.0	19.5	20.0	V	Networkships of the State
Ramp Rate				70	-	-	V/µs	
Address Setup Time			t sx	10	Vep.8_63	271-55.01	μs	CIGARARO DAS
Address Hold Time			t HA	10	- Te.	Tratera	μs	a remember of
Sense Setup Time			tss	0.7	-		μs	
Sense Hold Time			t n š	0.7	-		μs	filters Access Line
Additional Programmin	ng Pulse			1	1	1	time	Obje Roable Active Ture
Programming Pulse N	umber per	r bit	п	-	-	10000	time	Obje Explice Oracida Visio



The HD2012, a cloth driver for the MOS memory, has basically the NARO function. Its input is a TTL level and its output becomes and N WOS clock input level. It contrates on two power supplies –  $V_{CO}$  (SV) and  $V_{CO}$  (12V). It anticipates telefog as its load a maximum of two units of 4K bit N MOS memories and can drive a load capacity of 400 pF at high speed.

- Tituatis terrevisios Invit 20M-111
  - Usam) in 03 tank politerive .
- Losd capacity driveoler 600gF
  - \* Mountad with 4 circuits
- Applicable temps stars: 0 to 70°C

#### LADSOLUTE MATIMUM RATINGS



 Item
 Symbol
 MD391I
 Unit
 Image
 <th

# **MEMORY SUPPORT CIRCUITS**

			ent.
			Liquit - Voltage
		0	

#### 顧客LECTRICAL CHARACTERISTICS Torrelle + TOC, M--5V 1586, M. - 11V -

		$V_{11} = 2V_{11} I_{111} = 0$ , $k_{20} h_{1}$	
Infus Gersent			
	S all		

**OHITACHI** 

15	

# HD2912

#### Quadruple TTL-to-MOS Clock Drivers

The HD2912, a clock driver for the MOS memory, has basically the NAND function. Its input is a TTL level and its output becomes and N MOS clock input level. It operates on two power supplies - Vcc (5V) and VDD (12V). It anticipates taking as its load a maximum of ten units of 4K-bit N MOS memories and can drive a load capacity of 400 pF at high speed.

- TTL-MOS level converter circuit
- Switching time: 50 ns (max.)
- Load capacity drivable: 600pF
- Mounted with 4 circuits
- Applicable temperature: 0 to 70°C

#### **MABSOLUTE MAXIMUM RATINGS**

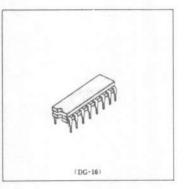
Item	Symbol	HD2912	Unit
	Vcc*	7.0	v
Supply Voltage	V <sub>DD</sub> *	18.0	V
Input Voltage	Vin *	5.5	v
Load Capacitance	C **	600	pF
Power Dissipation	Pr***	800	mW
Operating Temperature	Tepr	0 to +70	"C
Storage Temperature	Tata	-65 to +150	°C

\*\* per circuit

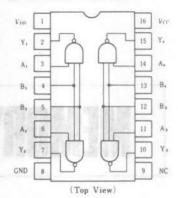
\*\*\* per package

#### RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
C 1 11 1	Vcc	4.75	5.0	5.25	V
Supply Voltage	VDD	11.4	12	12.6	V
Operating Temperature	Tapr	0	25	70	°C
Load Capacitance	C <sub>L</sub>	100		600	pF
Damping Resistance	Ro	10	-	-	Ω



#### PIN ARRANGEMENT



#### **ELECTRICAL CHARACTERISTICS** $(Ta=0 \text{ to } +70^{\circ}\text{C}, V_{cc}=5V \pm 5\%, V_{bb}=12V \pm 5\%)$

Item		Symbol	Test Condition	min	typ*	max	Unit
I		Viz		2.0	-	-	V
Input Voltage		VIN		-	-	0.8	V
Output Values		Vol	Via=2V, Iot=0.1mA		0.45	0.6	V
Output Voltage		Von	$V_{in} = 0.8 V, I_{OH} = -0.1 m A$	V <sub>DD</sub> -0.9	11.5	-	V
	A	In	$V_{ix} = 2V, I_{0L} = 0.1 \text{mA}$ $V_{ix} = 0.8V, I_{0H} = -0.1 \text{mA}$ $V_{ix} = 0.4V$ $V_{ix} = 0.4V$ $V_{ix} = 2.4V$ $V_{ix} = 5.5V$ $V_{ix} = 0V$	-	-1	-1.6	mA
	В	In			-2	-3.2	mA
Input Current	A	Іін	V - 9 4V	-	-	40	μA
	В	IIN	V = 2.4 V	-	-	80	μA
		$I_l$	V.,=5.5V	-	-	1	mA
		Ірри	V., -0V	-	16	24	mA
Power Supply Current		IDDL	V=5V	-	-	0.5	mA
rower Supply Current		Iccn	V., -0V	-	12	18	mA
	0.31	Icci	V., -5V	-	67	100	mA
Input Clamp Voltage		Vi	$I_{12} = -12 \text{mA}$	-	-	-1.5	V

**HITACHI** 

\* Vcc=5V, Vpp=12V

438

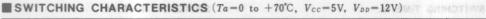
Unit

ns

ns

ns

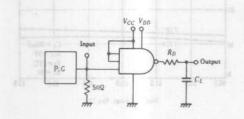
ns

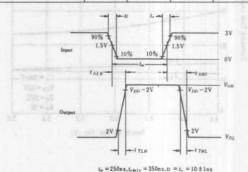


Test Condition

Item	Symbol	NAME S
Rising Delay Time	t dlh	1
Falling Delay Time	t DHL	C300pF
Rise Time	t TLH	$R_D = 0\Omega$
Fall Time	t THL	

#### . TEST CIRCUIT AND WAVEFORMS





min

-

-

-

typ

35

25

12

12

max

50

45

25

25

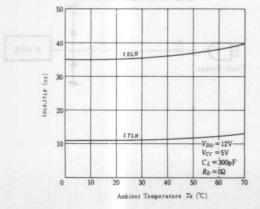
 $t_{\mu} = 250 n_{\pi}, t_{eW} t_{\pi} = 350 n_{\pi}, t_{\ell} = t_{\pi} = 10 \pm 1 n_{\pi}$ 

FALLING DELAY TIME vs. LOAD CAPACITANCE (1) 50 40 Tugni Bo CONL. 30 oibil a Basi ert ni sare å 20 Falling webs V00=12V 10 Vcc=5V Ta=25'C 040 0 100 200 300 400 500 600

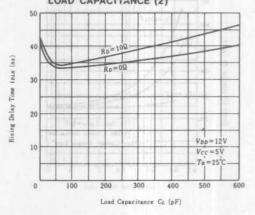
Load Capacitance Cr (pF)

When mounting this content, it is receivered to

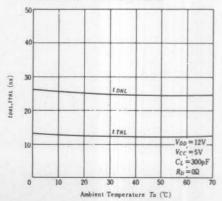


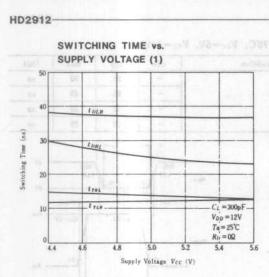




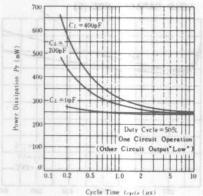


FALL TIME AND FALLING DELAY TIME vs. AMBIENT TEMPERATURE

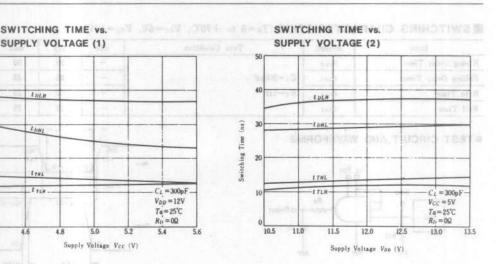




#### POWER DISSIPATION vs. CYCLE TIME



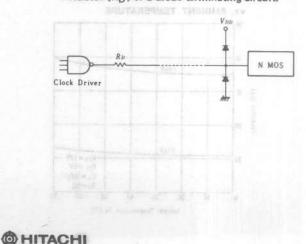




#### **ITEMS REQUIRING CARE WHEN USING** THE HD2912

When measuring or mounting the HD2912, consider the following.

- 1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
- 2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.
- 3. If its load capacity is less than a certainalue (100pF), sometimes this element cannot fully provide its function. Take note of this fact when designing a system.
- 4. When mounting this element, it is recommended providing the output terminal with a damping resistor (RD) or a diode terminating circuit.



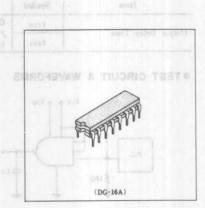
# HD2916

#### Quadruple TTL-to-NMOS Clock Drivers

The HD2916, a clock driver for the MOS memory, basically possesses a NAND function. Its Input is a TTL level and its output becomes N MOS clock input level. It operates on two power supplies –  $V_{CC}$  (5V) and  $V_{DD}$  (12V). Assuming that a maximum of five units of 4K-bit N MOS memories may be connected, it is designed to drive a load capacity of 200pF at high speeds.

#### FEATURES

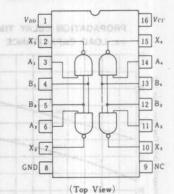
- TTL-MOS level converter
- Switching time: 50 ns (max.)
- Average power consumption: 600mW (max.)
- Load capacity drivable: 300pF
- Mounted with 4 circuits
- Applicable temperature: 10 to 65°C



#### PIN ARRANGEMENT

#### ABSOLUTE MAXIMUM RATINGS

Item UTA9391	Symbol	HD2916	Unit
C 1 11 1	Vcc*	-0.5 to +7	V
Supply Voltage	VDD*	-0.5 to +15	v
Input Terminal Voltage	Vin*	-0.5 to $+5.5$	v
Output Load Capacitance	C**	300	pF
Power Dissipation	Pr***	700	mW
Operating Temperature	Tepr	0 to +70	°C
Storage Temperature	Tate	-50 to +150	°C
+ With and the CMD			



\* With respect to GND

\*\* Per circuit
\*\*\* Per package

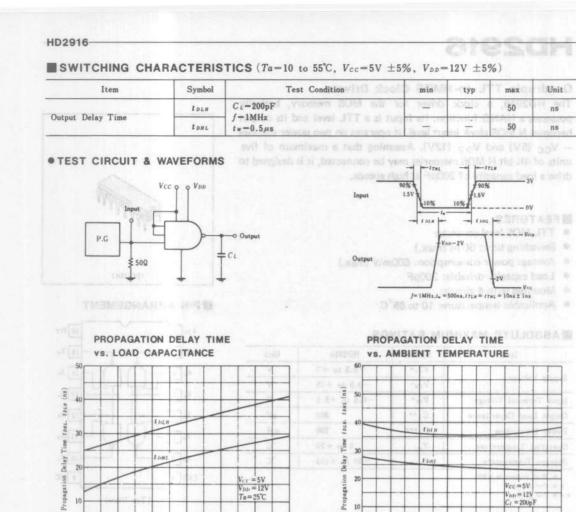
#### RECOMMENDED OPERATING CONDITION

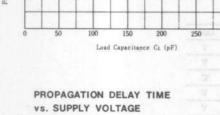
Item	Symbol	min	typ	max	Unit
C I VI	Vcc	4.75	5.0	5.25	v
Supply Voltage	VDD	11.4	12.0	12.6	V
Operating Temperature	Tepr	10	25	55	°C
	Vin	2.0	-	5.5	V
Input Voltage Level	VIL	-0.5		0.8	V

#### ELECTRICAL CHARACTERISTICS (Ta=10 to 55°C, $V_{cc}=5V \pm 5\%$ , $V_{pp}=12V \pm 5\%$ )

Item		Symbol	Test Condition	min	typ*	max	Unit
		Im	V <sub>IN</sub> =2.4V	-	-	40	μA
	A	In	$V_{IN} = 0.4V$		-1	-2	mA
Input Current		Im	$V_{IN} = 2.4 V$	-		80	μA
	в	In	V <sub>IN</sub> =0.4V	-	-2	-4	mA
B IIL VIN-0.4V Von VIN-0.8V, Ion Von VIN-0.8V, Ion		$V_{IN} = 0.8 V, I_{OB} = -50 \mu A$	V <sub>DD</sub> -0.7	V0.4	-	V	
itput Voltage		Vol	$V_{IN} = 2.0 V, I_{OL} = 50 \mu A$	-	0.3	0.45	V
utput voitage		Ідон	$V_{IN} = 0 V$	-	13	20	mA
Sand Change		Іссн	$V_{IN} = 0 V$	-	13	40	mA
Supply Current	1. 1.1	IDDL	V <sub>IN</sub> =5V	-	-	39	mA
		Icer	V <sub>IN</sub> =5V	<u> </u>	40	60	mA
Average Power Dissipatio	n	Рта	$C_L=300 \text{pF}, f=1 \text{MHz}$ $t_W=0.5 \mu \text{s}, \text{ one circuit operation}$	the state	300	600	mW

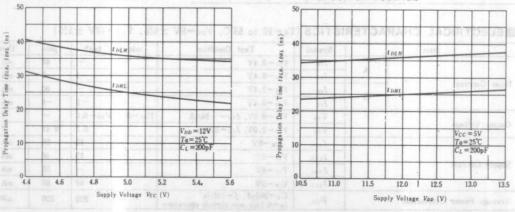
**HITACHI** 

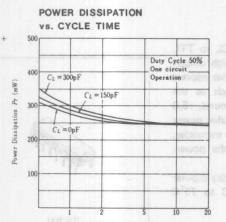






Ambient Temperature Ta("C)





10 20 more that lected, th

# THE HD2916

When measuring or mounting the HD2916, consider the following:

- At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
- When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.

FEATURES

10K EEE Company and monthly 101 (a)

CONTRACTOR OF THE PARTY OF THE PARTY OF THE

CARCOLETE MAXIMUM RATEROS

#### ERECOMMENDED OPERATING CONDITIONS



supply heline algebra at supply.

SJEAT HT. TABLE

# HD2923

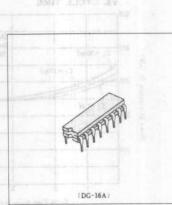
DWIGH WEHN BAA - OWINDORR SMETTE

## Quadruple ECL to TTL Drivers

NORTANISSIC REWOR

# The HD2923 is a monolithic, high speed Quadruple ECL to TTL Driver which accepts ECL input signals. It provides high output current suitable for driving the TTL clock inputs or other address multiplexing inputs of N-channel MOS memories such as the HM4816A of MK4116.Power supply requirements are ground, +5.0 Volts and -5.2 Volts. The HD2923 requires no particular power supply sequencing in order to assure standby mode of memories, because the outputs are always "high" at applying the power. Propagation delay is 10ns MAX.

The HD2923 is fabricated by means of HITACHI's Schottky Bipolar technology to assure high performance over the  $0^{\circ}$ C to  $75^{\circ}$ C ambient temperature range.



#### FEATURES

- High Speed ..... t<sub>pd</sub> = 10ns MAX. (50% to 2.2V dc out or to +1.0V dc out, 200pF Load)
- Low Power ..... 250mW typ. (DC)
- 10K ECL Compatible Inputs
- Pin Compatibility ...... MC10125 or HD10125

#### BABSOLUTE MAXIMUM RATINGS

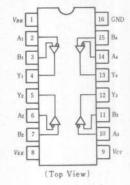
Item	Symbol	Value	Unit
	Vcc	-0.5 to +7	v
Supply Voltage	VEE	-7 to +0.5	v
Input Voltage	Vis	$V_{EE}$ to $\pm 0.5$	V
Output Voltage	Vest	-1.0 to Vcc+1	v
Power Dissipation	Рт	1.0	W
Operating Temperature*	Tser	-10 to +85	°C
Storage Temperature	Tota	-65 to +150	°C

\* under bias

#### RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
~	Vcc	4.75	5.0	5.25	v
Supply Voltage	VEE	-5.46	-5.2	-4.94	v
	V <sub>IH</sub>	-1.025	-	-	V
Input Voltage	VIL.	-	-	-1.520	V
Operating Temperature	Topr	0	-	75	°C

#### PIN ARRANGEMENT



The  $V_{BB}$  reference voltage is available on pin 1 for use in single ended input biasing

#### TRUTH TABLE

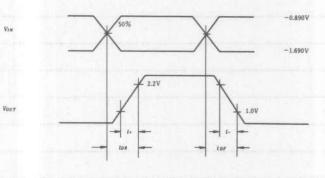
Inj	out	Output
А	В	Y
Н	V <sub>BB</sub>	L
L	$V_{BB}$	Н
Н	L	L
L	Н	Н
VBB	Н	Н
VBB	L	L
Open	Open	Н

#### DC CHARACTERISTICS

Item	Symbol	Test Condition	mîn	typ	max	Unit	
NO COUNTERNOL OF THE OFF	$-I_{EE}$		-	22	27	mA	
Power Supply Drain Current	Іссн	$V_{\mathcal{E}\mathcal{E}} = -5.2 \text{V}, V_{\text{c}\mathcal{C}} = 5.0 \text{V}$	-	23.5	29	mA	
	Iccl		-	34.5	42	mA	
Input Current	I in H	$V_{IN} = -0.81 V$	-	-	115	μA	
Input Leakage Current	Ісво	$V_{IN} = -5.2 V$	-	-	1.0	μA	
0 · · · · · · · ·	Von	$I_{on} = -1.0 \text{mA}$	2.7	-	-	V	
Output Voltage	Vol	IoL=5.0mA		-	0.5	v	
	VORA	$V_{IH} = -1.1 V, I_{OH} = -1.0 mA$	2.7	-	-	V	
Threshold Voltage	VOLA	$V_{LL} = -1.48$ V, $I_{OL} = 5.0$ mA	-	-	0.5	V	
Indeterminate Input	Vons	All inputs = $V_{EE}$	2.7	-			
Protection Tests	Vons	All inputs - Open	2.7	-	-	v	
Reference Voltage	VBB		-1.420	-	-1.150	V	
		$V_{INH} = 0.300 \text{V}, V_{INL} = -0.825 \text{V}$	2.7	-	-	v	
	Vonc	$V_{INH} = -1.890 \text{V}, V_{INL} = -2.890 \text{V}$	2.7		-	v	
Common Mode Rejection Tests	V	$V_{INH} = 0.300 \text{V}, V_{INL} = -0.825 \text{V}$		-	0.5		
	Volc	$V_{INH} = -1.890 V, V_{INL} = -2.890 V$	-	-	0.5	v	

#### **MAC CHARACTERISTICS**

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t DR	50% to +2.2V, C <sub>L</sub> =200pF	-	-	10	ns
	t df	50% to +1.0V, C <sub>L</sub> -200pF	-	-	10	ns
Rise Time	t+	+1.0V to +2.2V, C <sub>L</sub> =200pF			5	ns
Fall Time	1-	+2.2V to +1.0V, C <sub>L</sub> =200pF	-	-	5	ns



IVI	EMO	)						
				•••••				 
								 Q. straf. class?
						Aller Constraints		 
64						12.2		treesed spates I a
			1.1					 
					••••••			 
					2.22.2-1.1			 
						Contract DA.		
			118			All Inputse - 0	press, V. v.	
				78		700.0		 
							A CONTRACTOR	
	61							 
	2							

( HITACHI