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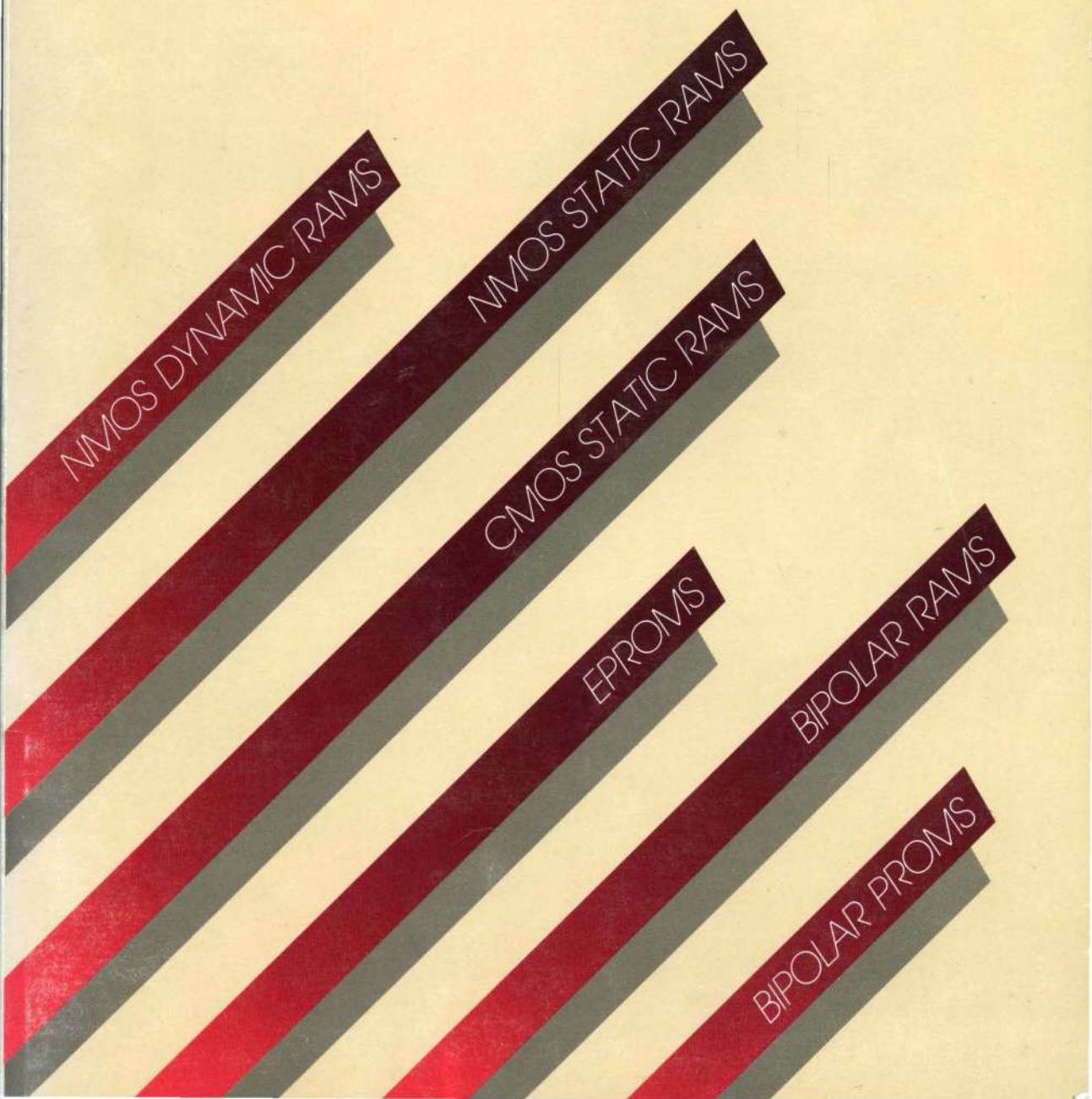
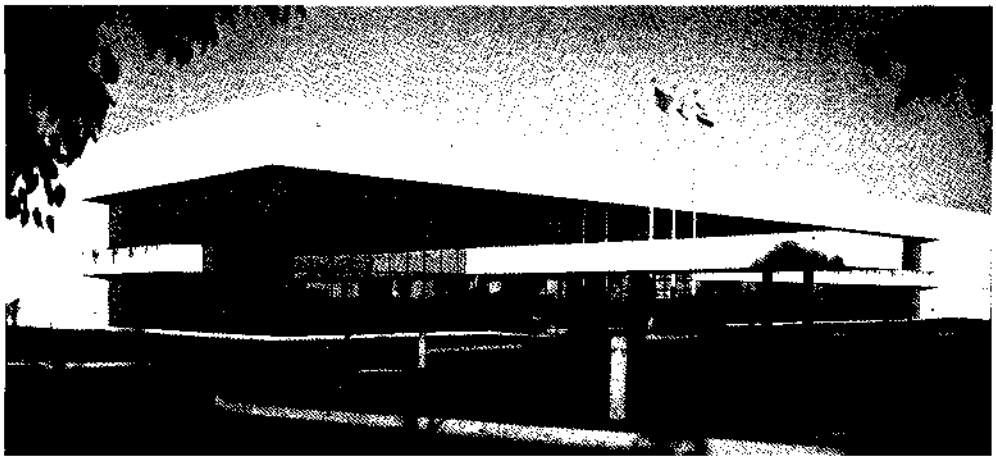
MEMORY DATA BOOK 1982





Fujitsu Microelectronics' manufacturing facility in San Diego, California

FUJITSU MICROELECTRONICS, INC.— A U.S. ORGANIZATION

Fujitsu Microelectronics Inc. (FMI) is a U.S. subsidiary of Fujitsu Limited of Tokyo. A California Corporation, FMI is responsible for the marketing and sales of all semiconductor products in North, Central and South America.

Fujitsu Limited manufactures and markets advanced data processing and telecommunications systems, semiconductors and electronic components on a worldwide scale. Fujitsu Limited is ranked as Japan's number one computer manufacturer with sales in the $2 billion range.

A LEADER IN ICs

Fujitsu is one of the world's largest electronic companies with development and manufacturing capabilities utilizing the most modern and innovative technical skills. Fujitsu Microelectronics remains at the leading edge of semiconductor technology as exemplified by its offering of the world's first mass-produced 64K-bit MOS RAM. Process technologies include both MOS and bipolar; products include static and dynamic memories, RAMs, EPROMs and PROMs; as well as LSI logic including microprocessors and gate arrays.

ABOUT FUJITSU MICROELECTRONICS

Fujitsu Microelectronics has completed a new assembly and test facility in order to better service our North American customers. The 66,000 square-foot facility is located in Kearny Mesa Industrial Park near downtown San Diego. The building was dedicated in June 1981 and is now fully operational.

ABOUT FUJITSU MIKROELEKTRONIK GmbH

Fujitsu Mikroelektronik GmbH was formed in June 1980 as a wholly owned subsidiary of Fujitsu Limited of Tokyo. From headquarters in Frankfort, West Germany, it supervises the sales and marketing of Fujitsu semiconductor products throughout Western Europe. Fujitsu plans to construct a factory in Ireland to further increase its ability to provide high quality semiconductor devices to its European customers.

FUJITSU
MICROELECTRONICS

MEMORY DATA BOOK

APRIL 1982

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FUJITSU MICROELECTRONICS' CROSS REFERENCE GUIDE

AMD	FMI
AM2716	MBM2716
AM2732	MBM2732
AM9016	MB8116
AM9147	MBM2147
AM27S28	MB7123
AM27S29	MB7124
AM27S32	MB7121
AM27S33	MB7122
AM27S180	MB7131
AM27S181C	MB7132
AM27S185C	MB7128
AM27S191C	MB7138

ELECTRONIC ARRAYS	FMI
EA2716	MBM2716

FAIRCHILD	FMI
F2764	MBM2764
F4116	MB8116
F4164	MB8264
F10415	MBM10415
F10422	MBM10422
F10470	MBM10470A
F10474	MBM10474
F93419	MBM93419
F93450	MB7131
F93451	MB7132
F93452	MB7121
F93453	MB7122
F93511	MB7138
F98510	MB7137
F100422	MBM100422
F100470	MBM100470

HARRIS	FMI
HM7642	MB7121
HM7643	MB7122
HM7648	MB7123
HM7649	MB7124
HM7680	MB7131
HM7681	MB7132
HM7684	MB7127
HM7685	MB7128
HM76160	MB7137
HM76161	MB7138
HM76321	MB7142

HITACHI	FMI
HM4716A	MB8116
HM4816	MB8118
HM4847	MBM2147
HM4864	MB8264
HM6116L	MB8416
HM6147	MBM2147
HN25044	MB7121
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HN25169	MB7138
HN462716	MBM2716
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INMOS	FMI
IMS1400	MB8167
IMS1420	MB8168
IMS2600	MB8264
IMS2600	MB8266A

INTEL	FMI
2117	MB8116
2118	MB8118
2147	MBM2147
2148	MBM2148
2149	MBM2149
2164	MB8264
2167	MB8167
2168	MB8168
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2732A	MBM2732A
2764	MBM2764
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3632	MB7142
3636-1	MB7138

INTERSIL	FMI
IM5626	MB7122

MITSUBISHI	FMI
M5L2716	MBM2716
M5L2732K	MBM2732
M5K4116	MB8116
M5K4164NS	MB8264
M5K4164S	MB8265
M58725	MB8128

MONOLITHIC MEMORIES	FMI
6352	MB7121
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6380	MB7131
6381-1	MB7132
63100	MB7127
63101	MB7128
63S1681	MB7138

MOSTEK	FMI
MK2147	MBM2147
MK2716	MBM2716
MK4116	MB8116
MK4164	MB8265
MK4167	MB8167
MK4516	MB8117
MK4564	MB8264
MK4802	MB8128

MOTOROLA	FMI
MCM2147	MBM2147
MCM2167	MBM8167
MCM2716	MBM2716
MCM4016	MB8128
MCM4116	MB8116

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MOTOROLA (Cont'd)	FMI
MCM4516	MB8117
MCM4517	MB8118
MCM6664	MB8265
MCM6665	MB8264
MCM7642	MB7121
MCM7643	MB7122
MCM7681	MB7132
MCM7685	MB7128
MCM10146	MBM10415
MCM65116	MB8416

NATIONAL	FMI
DM10415	MBM10415
DM74S472	MB7124
DM74S473	MB7123
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DM74S573	MB7122
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DM87S184	MB7127
DM87S185	MB7128
DM87S190	MB7137
DM87S191	MB7138
MM2147	MBM2147
MM5290	MB8116
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NMC27C32	MBM27C32
NMC4164	MB8264
NMC5295	MB8118

NEC	FMI
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μPD2147	MBM2147
μPD2167	MB8167
μPD2716	MBM2716
μPD2732	MBM2732
μPD4164	MB8264

OKI	FMI
MSM2128	MB8128
MSM2716	MBM2716
MSM2732	MBM2764
MSM2764	MBM2764
MSM3764	MB8264
MSM5128	MB8416

PANASONIC	FMI
MN2716	MBM2716

RAYTHEON	FMI
29631	MB7132
29641	MB7122
29650	MB7127
29651	MB7128
29653	MB7128
29681	MB7138

SIGNETICS	FMI
2716	MBM2716
10415	MBM10415
10422	MBM10422
10470	MBM10470
10474	MBM10474
100422	MBM100422
100470	MBM100470
82S137	MB7122
82S147	MB7124
82S180	MB7131
82S181	MB7132
82S184	MB7127
82S185	MB7128
82S190	MB7138
82S191	MB7138
82S321	MB7142

SUPERTEX	FMI
SM82S180	MB7131
SM82S181	MB7132
SM82S191	MB7138

SYNERTEK	FMI
SY2128	MB8128
SY2716	MBM2716

TI	FMI
TBP24S41	MB7122
TBP24S81	MB7128
TBP28S42	MB7124
TBP28S86	MB7132
TBP28S166	MB7138
TMS2147H	MBM2147H
TMS2149	MBM2149
TMS2716	MBM2716
TMS4016	MB8128
TMS4116	MB8116
TMS4164	MB8264

TOSHIBA	FMI
TC5516	MB8417
TC5517	MB8416
TC5518	MB8418
TMM315D	MBM2147
TMM323C	MBM2716
TMM416	MB8116
TMM2016	MB8128
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UNIVERSAL	FMI
UM2147	MBM2147

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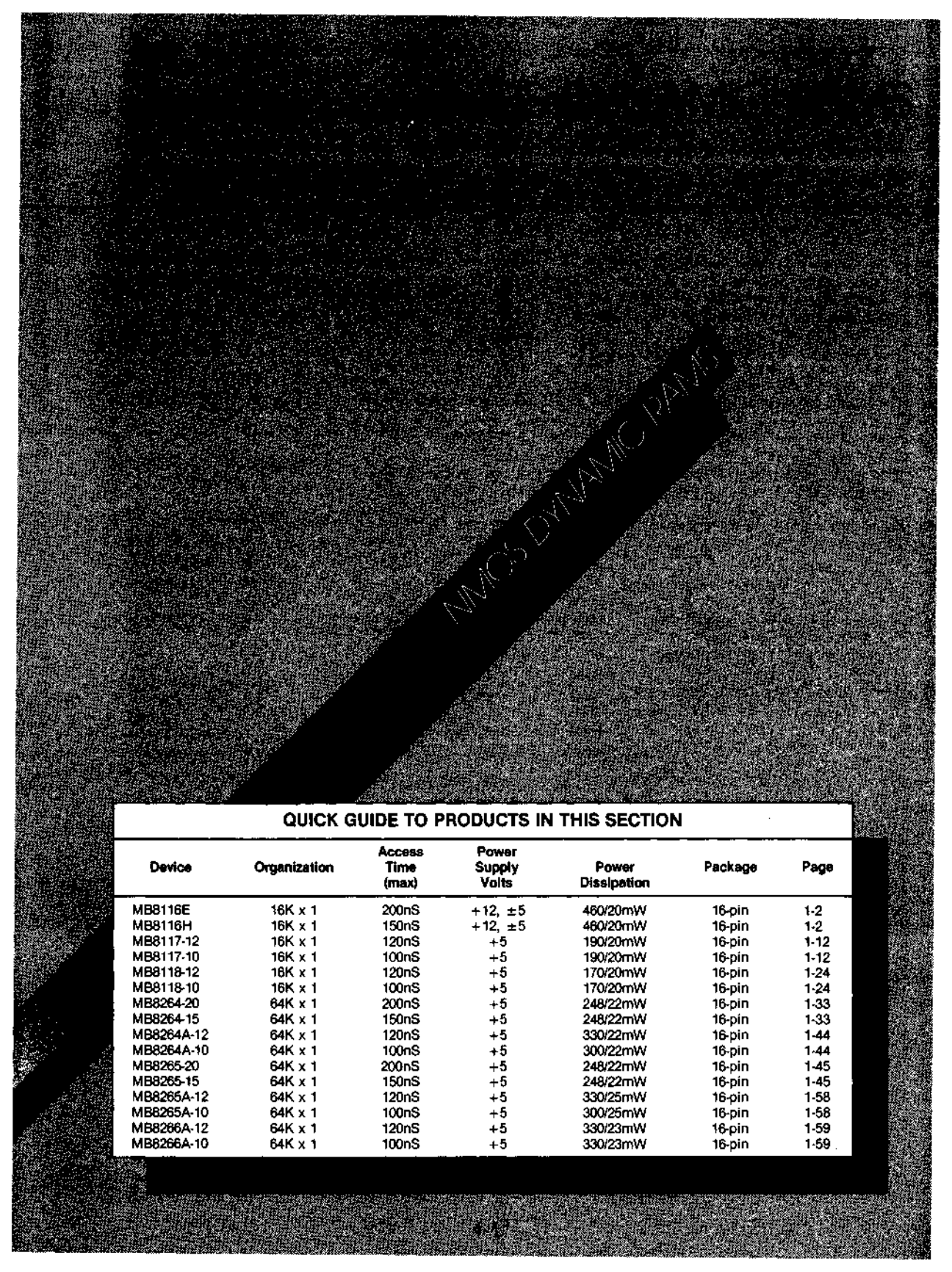


QUICK GUIDE TO PRODUCTS IN THIS SECTION

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB8116E	16K x 1	200nS	+12, ±5	460/20mW	16-pin	1-2
MB8116H	16K x 1	150nS	+12, ±5	460/20mW	16-pin	1-2
MB8117-12	16K x 1	120nS	+5	190/20mW	16-pin	1-12
MB8117-10	16K x 1	100nS	+5	190/20mW	16-pin	1-12
MB8118-12	16K x 1	120nS	+5	170/20mW	16-pin	1-24
MB8118-10	16K x 1	100nS	+5	170/20mW	16-pin	1-24
MB8264-20	64K x 1	200nS	+5	248/22mW	16-pin	1-33
MB8264-15	64K x 1	150nS	+5	248/22mW	16-pin	1-33
MB8264A-12	64K x 1	120nS	+5	330/22mW	16-pin	1-44
MB8264A-10	64K x 1	100nS	+5	300/22mW	16-pin	1-44
MB8265-20	64K x 1	200nS	+5	248/22mW	16-pin	1-45
MB8265-15	64K x 1	150nS	+5	248/22mW	16-pin	1-45
MB8265A-12	64K x 1	120nS	+5	330/25mW	16-pin	1-58
MB8265A-10	64K x 1	100nS	+5	300/25mW	16-pin	1-58
MB8266A-12	64K x 1	120nS	+5	330/23mW	16-pin	1-59
MB8266A-10	64K x 1	100nS	+5	330/23mW	16-pin	1-59

FUJITSU
MICROELECTRONICS

MB8116E
MB8116H

MOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MB8116 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

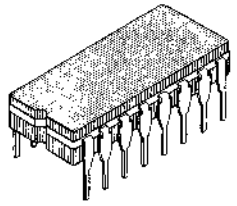
Multiplexed row and column address inputs permit the MB8116 to be housed in a standard 16-pin DIP. Pin-outs conform to the accepted industry standard.

The MB8116 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

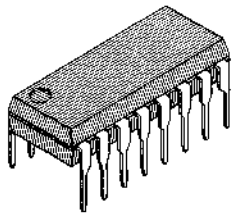
Clock timing requirements are non-critical, and power supply tolerances are 10%. All inputs are TTL compatible; the output is three-state TTL.

FEATURES

- **16,384 x 1 RAM, 16 pin package**
- **Silicon-gate, double-poly NMOS, single transistor cell**
- **Row access time:**
  200 ns max. (MB8116E)
  150 ns max. (MB8116H)
- **Cycle time:**
  375 ns min.
- **Low power**
  462mW active,
  20 mW standby (max.)
- **±10% tolerance on +12V, ±5V supplies**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-In**
- **Compatible with MK4116**

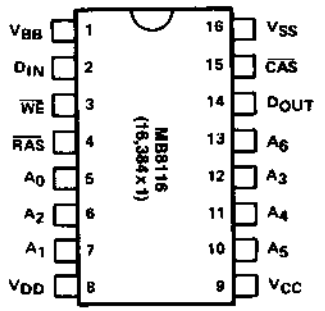


CERDIP PACKAGE
DIP-16C-C03



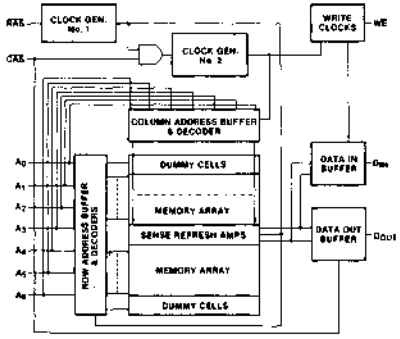
PLASTIC PACKAGE
DIP-16P-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8116 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (see Note)

Rating		Symbol	Value	Unit
Voltage of any pin relative to V_{BB}		V_{IN}, V_{OUT}	−0.5 to +20	V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}		V_{DD}, V_{CC}	−0.5 to +15	V
V_{BB}-V_{SS} (V_{DD}-V_{SS} > 0V)		—	0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−40 to +125	
Power Dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	NOTES	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	1	V_{DD}	10.8	12.0	13.2	V	0°C to +70°C
	1 2	V_{CC}	4.5	5.0	5.5	V	
	1	V_{SS}	0	0	0	V	
	1	V_{BB}	−4.5	−5.0	−5.5	V	
Input High Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IHC}	2.7	—	6.5	V	
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V_{IL}	−1.0	—	0.8	V	

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	Min	Max	Units
OPERATING CURRENT Average power supply current $\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)		I_{DD1} I_{BB1}	—	35 300	mA µA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IHC})		I_{DD2} I_{BB2}	—	1.5 100	mA µA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = min)		I_{DD3} I_{BB3}	— —	25 300	mA µA
PAGE MODE CURRENT Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225ns)		I_{DD4} I_{BB4}	— —	27 300	mA µA
V_{CC} POWER SUPPLY CURRENT (Data out is disabled)	3	I_{CC}	−10	10	µA
INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ 7V, all other pins not under test = 0V)		I_{IL}	−10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	µA
OUTPUT LEVELS Output high voltage (I_{OH} = −5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4	 0.4	V V

Notes: 1. All voltages are reference to V_{SS}.

2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH}(min) specification is not guaranteed in this mode.

3. When Data out is enabled, V_{CC} power supply current depends upon output loading; V_{CC} is connected to the output buffer only.

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 ~ A_6, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	10	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

DYNAMIC CHARACTERISTICS [NOTES 4, 5, 6]

(Recommended Operating Conditions unless otherwise noted.)

Parameter [NOTES]	Symbol	MB8116E		MB8116H		Units
		Min	Max	Min	Max	
Time between Refresh	t_{REF}	—	2	—	2	ms
Random Read/Write Cycle Time	t_{RC}	375	—	375	—	ns
Read-Write Cycle Time	t_{RWC}	375	—	375	—	ns
Page Mode Cycle Time	t_{PC}	225	—	170	—	ns
Access Time from $\overline{RAS}$ [7] [9]	t_{RAC}	—	200	—	150	ns
Access Time from $\overline{CAS}$ [8] [9]	t_{CAC}	—	135	—	100	ns
Output Buffer Turn Off Delay	t_{OFF}	0	50	0	50	ns
Transition Time	t_T	3	50	3	35	ns
$\overline{RAS}$ Precharge Time	t_{RP}	120	—	100	—	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	200	32000	150	32000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	135	—	100	—	ns
$\overline{CAS}$ Precharge Time	t_{CP}	80	—	60	—	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	135	10000	100	10000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	200	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time [10]	t_{RCD}	30	65	25	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20	—	−20	—	ns
Row Address Set Up Time	t_{ASR}	0	—	0	—	ns
Row Address Hold Time	t_{RAH}	25	—	20	—	ns
Column Address Set Up Time	t_{ASC}	−5	—	−5	—	ns
Column Address Hold Time	t_{CAH}	55	—	45	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120	—	95	—	ns
Read Command Set Up Time	t_{RCS}	0	—	0	—	ns
Read Command Hold Time	t_{RCH}	10	—	10	—	ns
Write Command Set Up Time [11]	t_{WCS}	−10	—	−10	—	ns
Write Command Hold Time	t_{WCH}	55	—	45	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120	—	95	—	ns
Write Command Pulse Width	t_{WP}	55	—	45	—	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	80	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	80	—	60	—	ns
Data In Set Up Time	t_{DS}	0	—	0	—	ns
Data In Hold Time	t_{DH}	55	—	45	—	ns
Data In Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120	—	95	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay [11]	t_{CWD}	95	—	70	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay [11]	t_{RWD}	160	—	120	—	ns

Notes: 4. Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Dynamic measurements assume t_T = 5ns.

6. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

7. Assumes that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

8. Assumes that $t_{RCD} \geq t_{RCD}$(max).

9. Measured with a load equivalent to 2 TTL loads and 100pF.

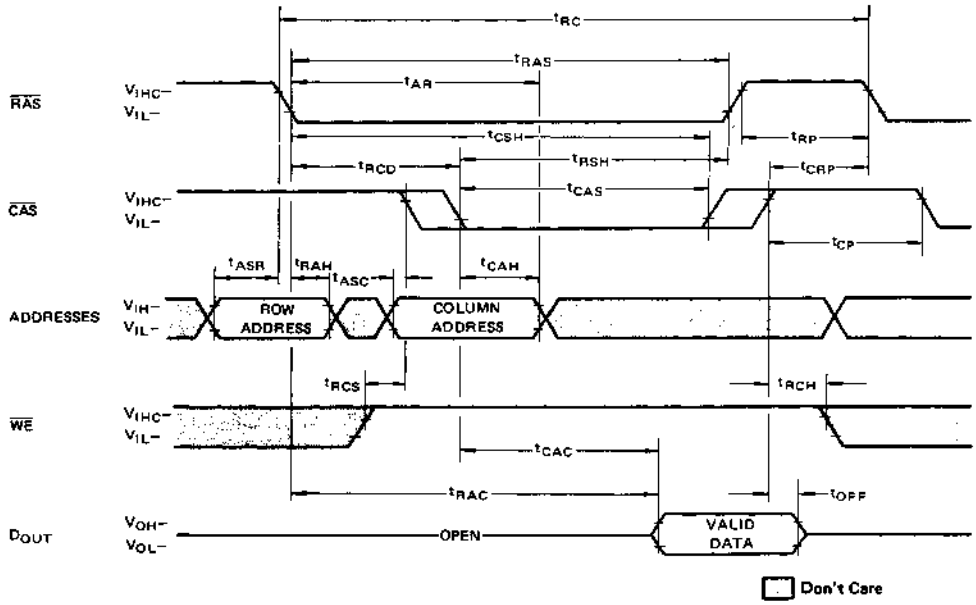
10. Operation within the t_{RCD}(max) limit insures that t_{RCD}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

11. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.

If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

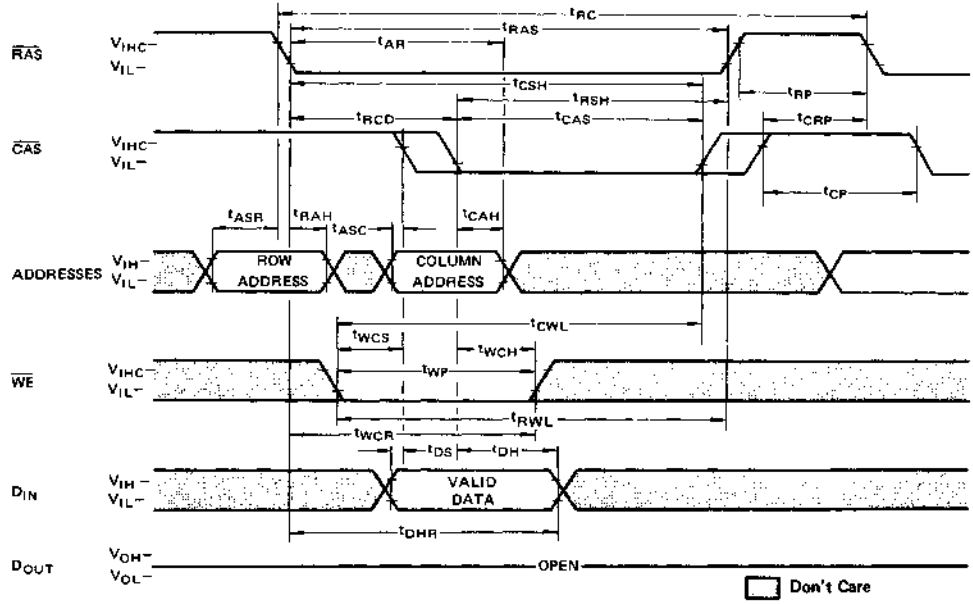
TIMING DIAGRAMS

READ CYCLE

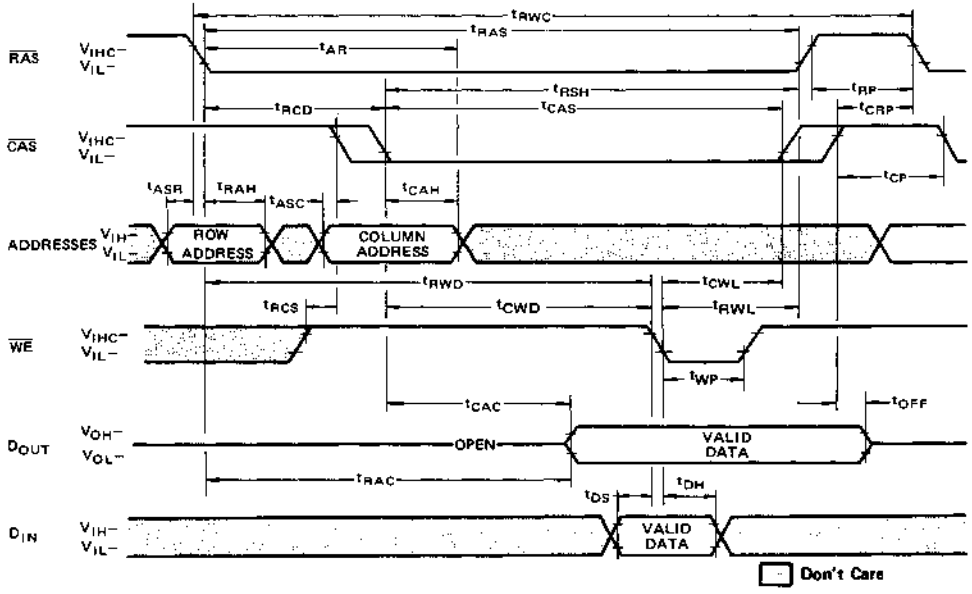


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



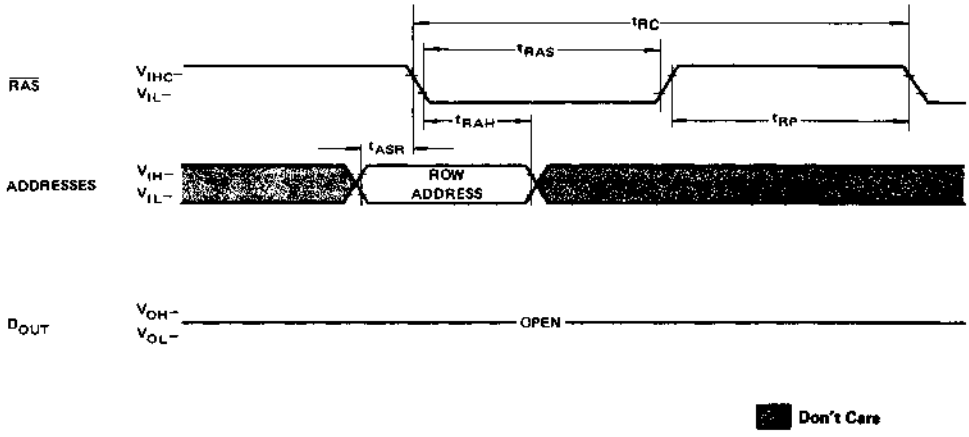
READ-WRITE/READ-MODIFY-WRITE CYCLE



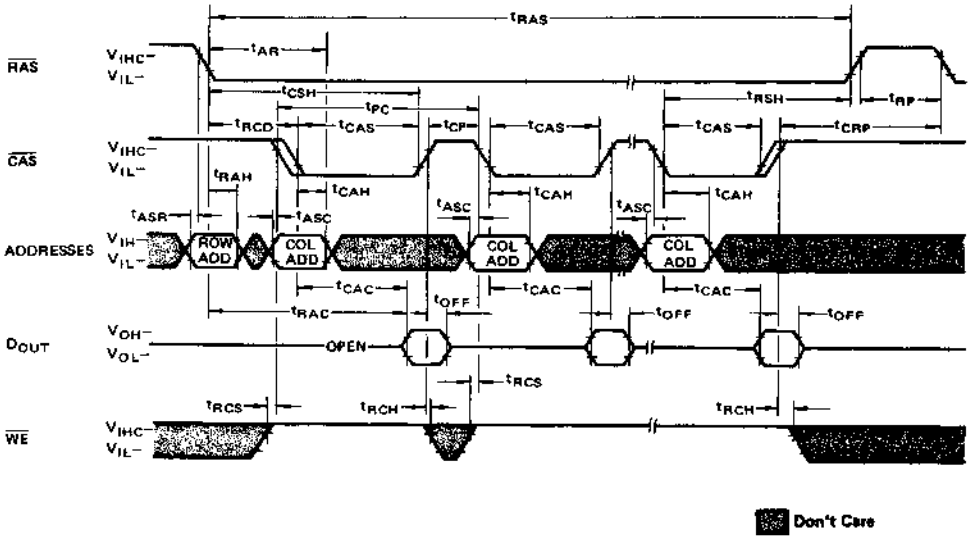
TIMING DIAGRAMS (Continued)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = Don't Care

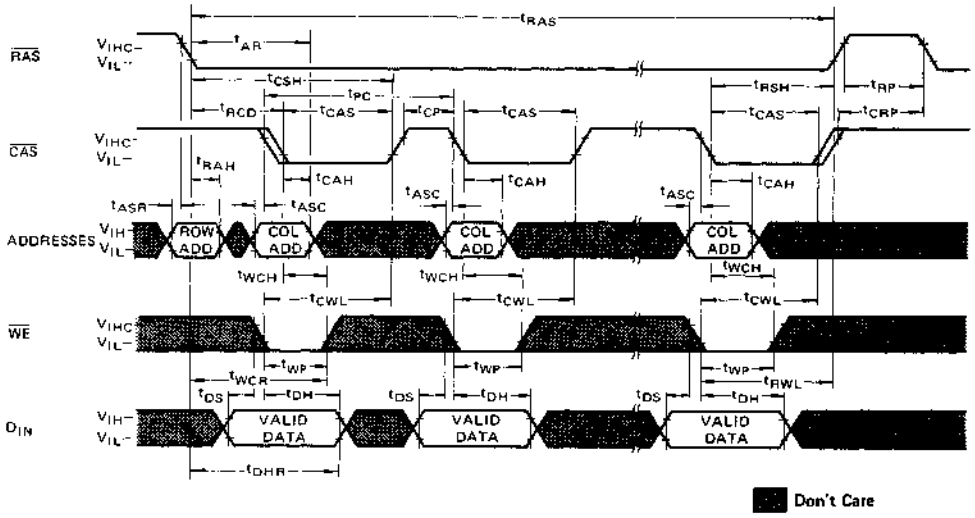


PAGE-MODE READ CYCLE



TIMING DIAGRAMS (Continued)

PAGE-MODE WRITE CYCLE



DESCRIPTION

Address Inputs:

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8116. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). The seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data Input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:

Data is written into the MB8116 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode:

Page-mode operation permits strobing the row-address into the MB8116 while maintaining RAS at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus the power dissipated by the negative going edge of RAS is saved. Futher, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-address at least every two milli-seconds. Any operation in which $\overline{RAS}$ transits accomplishes refresh. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substanial reduction in power dissipation.

Power Considerations:

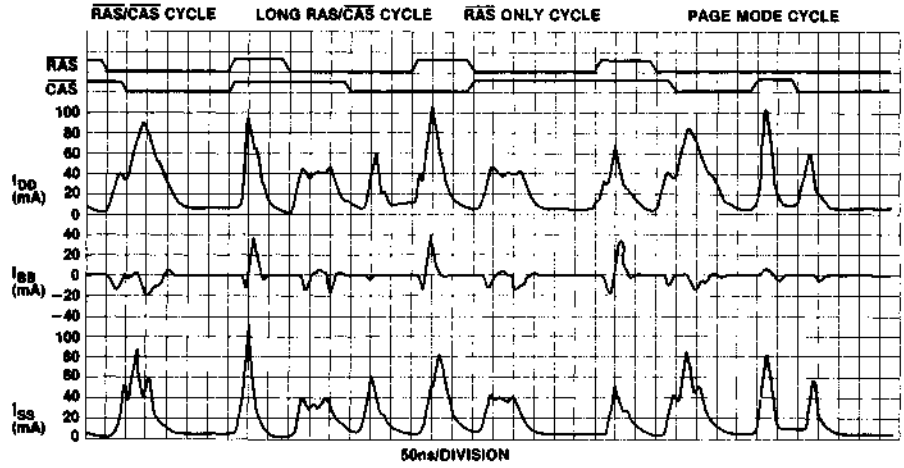
The output buffer of the MB8116 can be powered via V_{CC} from the supply voltage (normally 5 volts) to which the memory is interfaced. In standby operation, V_{CC} may be removed without affecting refresh. Thus standby power is conserved because all the power supplies for the peripheral circuitry with the exception of $\overline{RAS}$ timing and refresh address is turned off. Most of the MB8116 circuitry, including sense amplifiers, is dynamic, and most of the power drain comes from an address strobe ($\overline{RAS}$ or $\overline{CAS}$) edge. Thus, dynamic power dissipation depends mostly on operating frequency.

Power Up:

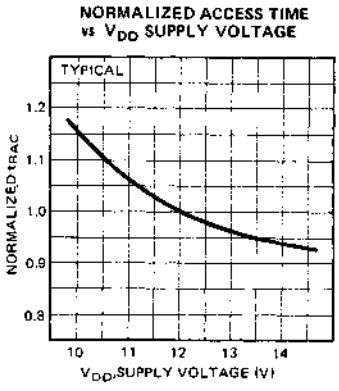
No particular supply sequencing is required for the MB8116. However, absolute maximum ratings must be adhered to. Thus, V_{BB} should be turned on first and turned off last, and V_{DD} is turned on. After power is applied, several cycles are required before proper operation is assured. About eight refresh cycles should be sufficient to accomplish this.

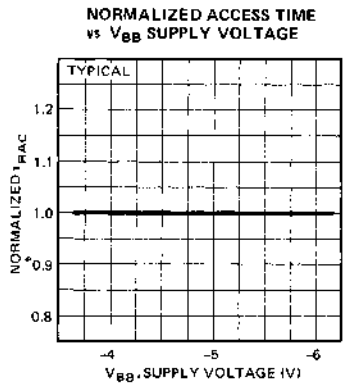
Current Waveforms

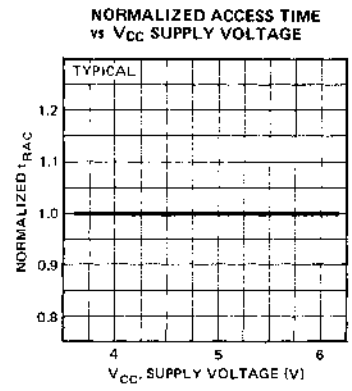
NOTE: V_{DD} = 13.2V, V_{BB} = −4.5V, T_A = 25°C



TYPICAL CHARACTERISTICS CURVES

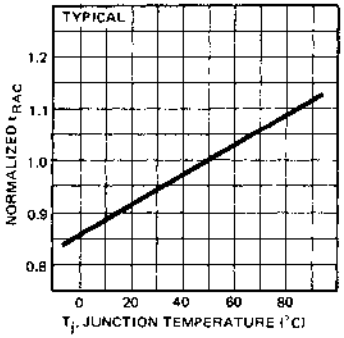




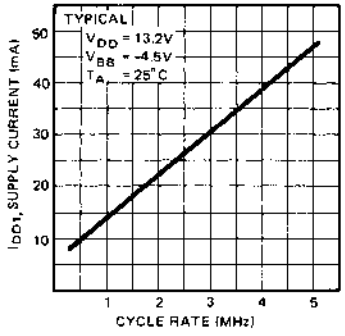


TYPICAL CHARACTERISTICS CURVES (Continued)

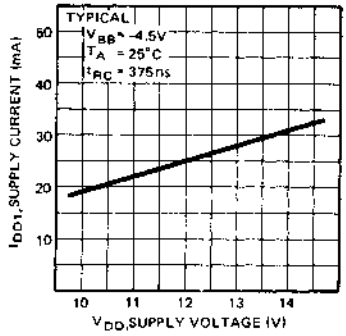
NORMALIZED ACCESS TIME vs T_j JUNCTION TEMPERATURE



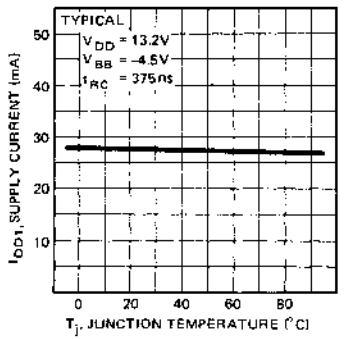
I_{DD1} (AVERAGE) vs CYCLE RATE



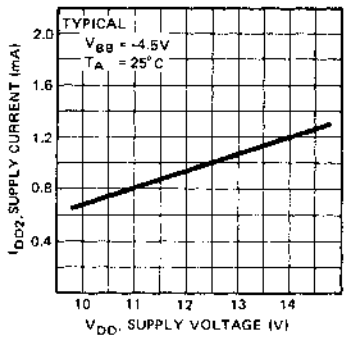
I_{DD1} (AVERAGE) vs V_{DD} SUPPLY VOLTAGE



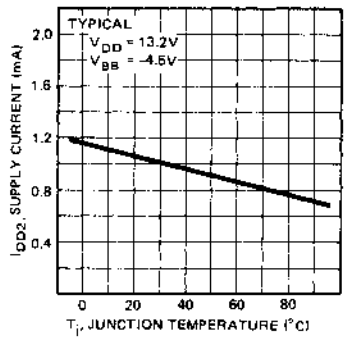
I_{DD1} (AVERAGE) vs T_j JUNCTION TEMPERATURE



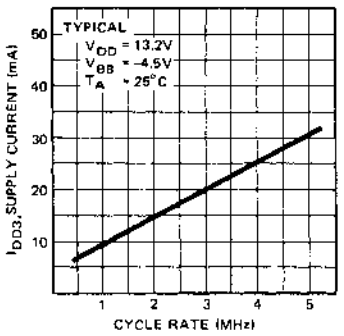
I_{DD2} (STANDBY) vs V_{DD} SUPPLY VOLTAGE



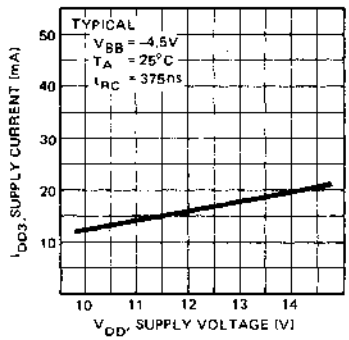
I_{DD2} (STANDBY) vs T_j JUNCTION TEMPERATURE



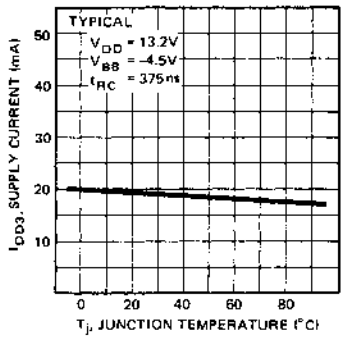
I_{DD3} ($\overline{RAS}$–ONLY) vs CYCLE RATE



I_{DD3} ($\overline{RAS}$–ONLY) vs V_{DD} SUPPLY VOLTAGE

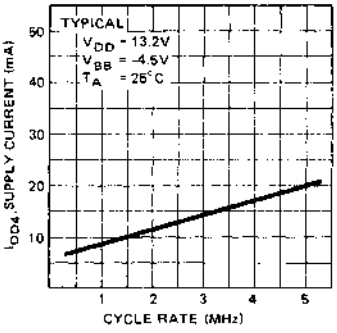


I_{DD3} ($\overline{RAS}$–ONLY) vs T_j JUNCTION TEMPERATURE

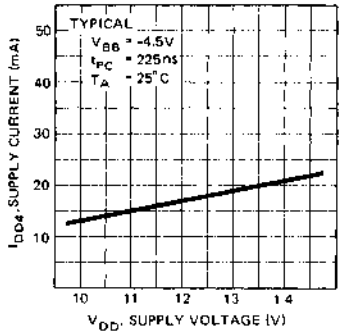


TYPICAL CHARACTERISTICS CURVES (Continued)

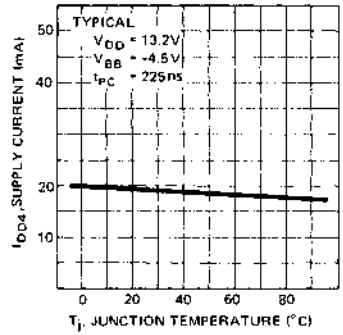
I_{DD4} (PAGE–MODE) vs CYCLE RATE



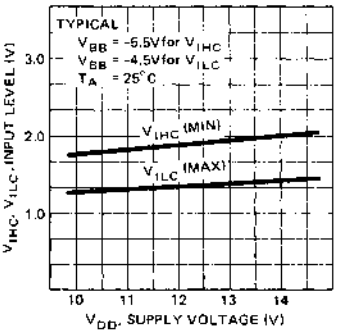
I_{DD4} (PAGE–MODE) vs V_{DD} SUPPLY VOLTAGE



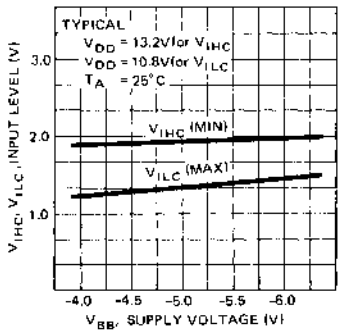
I_{DD4} (PAGE–MODE) vs T_j JUNCTION TEMPERATURE



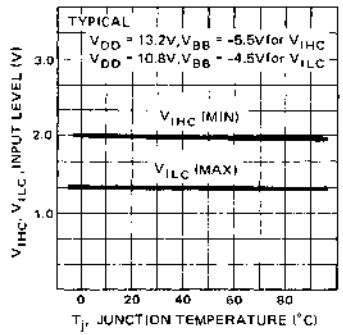
V_{IHC}, V_{ILC} INPUT LEVELS vs V_{DD} SUPPLY VOLTAGE



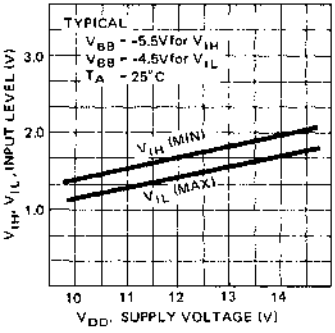
V_{IHC}, V_{ILC} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE



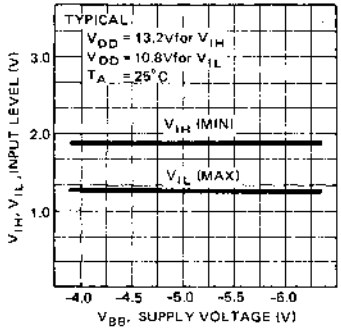
V_{IHC}, V_{ILC} INPUT LEVELS vs T_j JUNCTION TEMPERATURE



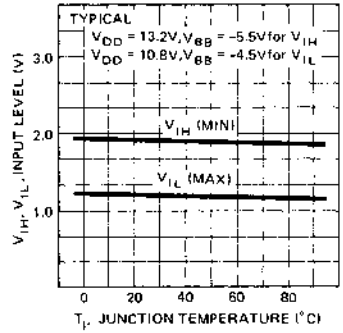
V_{IH}, V_{IL} INPUT LEVLES vs V_{DD} SUPPLY VOLTAGE



V_{IH}, V_{IL} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE



V_{IH}, V_{IL} INPUT LEVELS vs T_j JUNCTION TEMPERATURE



FUJITSU
MICROELECTRONICS

MB8117-10
MB8117-12

NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MB8117 is a fully decoded, dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8117 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

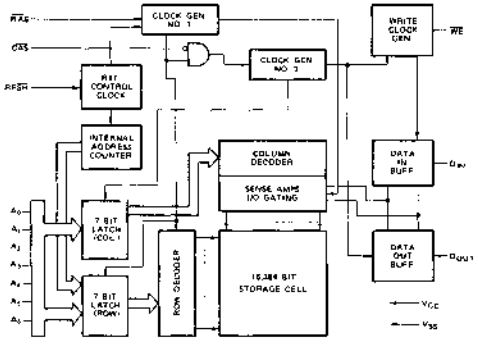
The MB8117 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

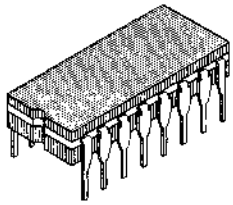
Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.

FEATURES

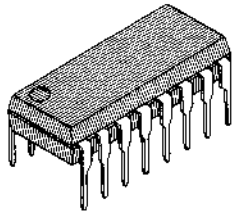
- **16,384 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS single-transistor cell**
- **Address access time**
  - **100 ns max (MB8117-10)**
  - **120 ns max (MB8117-12)**
- **Cycle time,**
  - **235 ns min (MB8117-10)**
  - **270 ns min (MB8117-12)**
- **Low power:**
  - **182 mW max (MB8117-10)**
  - **160 mW max (MB8117-12)**
  - **19.5 mW max (Standby)**
- **+5V single power supply, ±10% tolerance**
- **On-chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Pin 1 auto refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Address and Data-in**
- **Offers two variations of hidden refresh**
- **Pin compatible with MK4516 and MCM4516**

MB8117 BLOCK DIAGRAM



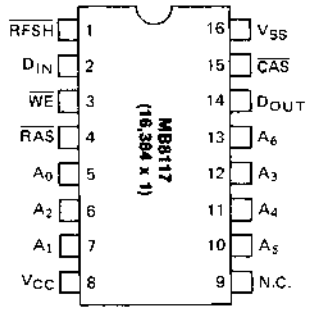


CERDIP PACKAGE
DIP-16C-C03



PLASTIC PACKAGE
DIP-16P-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage high than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} pin relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−40 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operational should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 – A_6, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{IN2}	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

STATIC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB8117-10 Min	MB8117-10 Max	MB8117-12 Min	MB8117-12 Max	Unit
OPERATING CURRENT Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min)	1	I_{CC1}	—	33	—	29	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		I_{CC2}	—	3.5	—	3.5	mA
REFRESH CURRENT 1 Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min)	1	I_{CC3}	—	25	—	22	mA
PAGE MODE CURRENT Average Power Supply Current[1] ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min)	1	I_{CC4}	—	25	—	22	mA
REFRESH CURRENT 2 Average Power Supply Current ($\overline{RFSH}$ cycling, $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}; t_{FC} = Min)	1	I_{CC5}	—	28	—	25	mA
INPUT LEAKAGE CURRENT Current, any input (0V ≤ V_{IN} ≤ 5.5V) Input pins not under test = 0V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V		I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V < V_{OUT} < 5.5V		I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	—	2.4	—	V

Notes: 1 I_{CC} is dependent on output loading. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS [NOTES 1, 2, 3]

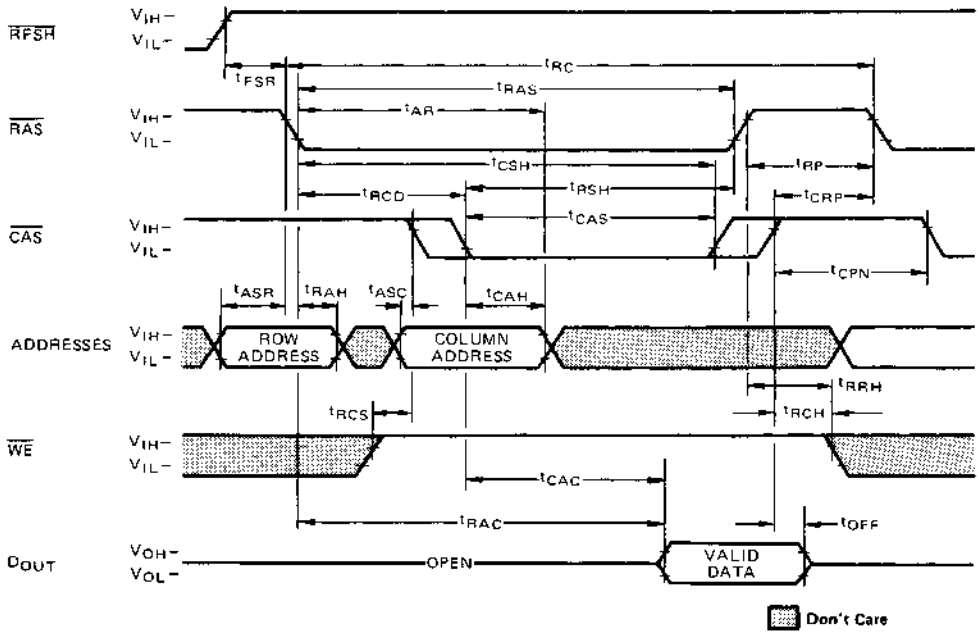
(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 8117-10		MB 8117-12		Unit
			Min	Max	Min	Max	
Time Between Refresh		t_{REF}	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	235	—	270	—	ns
Read-Write Cycle Time		t_{RWC}	285	—	320	—	ns
Page Mode Cycle Time		t_{PC}	125	—	145	—	ns
Access Time from $\overline{RAS}$	4 5	t_{RAC}	—	100	—	120	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	55	—	65	ns
Output Buffer Turn Off Delay		t_{OFF}	0	45	0	50	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	110	—	120	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	115	10000	140	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	70	—	85	--	ns
$\overline{CAS}$ Prechange Time (all cycles except page mode)		t_{CPN}	50	—	55	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	60	—	70	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	10000	65	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100	—	120	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	25	45	25	55	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	15	—	15	—	ns
Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	15	—	15	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	60	—	70	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
Read Command Hold Time		t_{RCH}	0	—	0	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	30	—	35	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	75	—	90	—	ns
Write Command Pulse Width		t_{WP}	30	—	35	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	60	—	65	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	45	—	50	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	ns
Data In Hold Time		t_{DH}	30	—	35	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	75	—	90	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	55	—	65	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	100	—	120	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	20	—	25	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{RAS}$		t_{FSR}	110	—	120	—	ns
RAS to $\overline{RFSH}$ Delay		t_{RFD}	110	—	120	—	ns
$\overline{RFSH}$ Cycle Time		t_{FC}	235	—	270	—	ns
$\overline{RFSH}$ Pulse Width		t_{FP}	100	—	120	—	ns
$\overline{RFSH}$ Hold Time Referenced to $\overline{RAS}$	10	t_{FHR}	0	—	0	—	ns
$\overline{RFSH}$ Precharge Time		t_{FI}	110	—	120	—	ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	10	t_{FRD}	55	—	65	—	ns

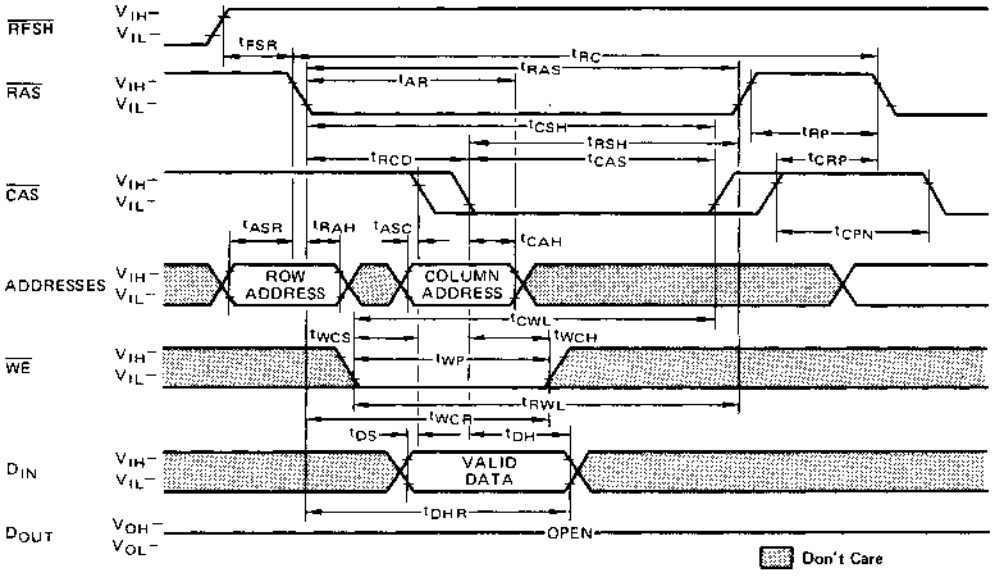
Notes:

1. An initial pause of 200μs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
   If internal refresh counter is to be effective, a minimum of 64 active $\overline{RFSH}$ initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2 ms if the $\overline{RFSH}$ refresh function is used.
   Besides $\overline{RFSH}$ must be held high even if the $\overline{RFSH}$ refresh function is not used.
2. Dynamic measurements assume $t_T = 5ns$.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} > t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. $t_{RAC}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} > t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Test mode write cycle only.

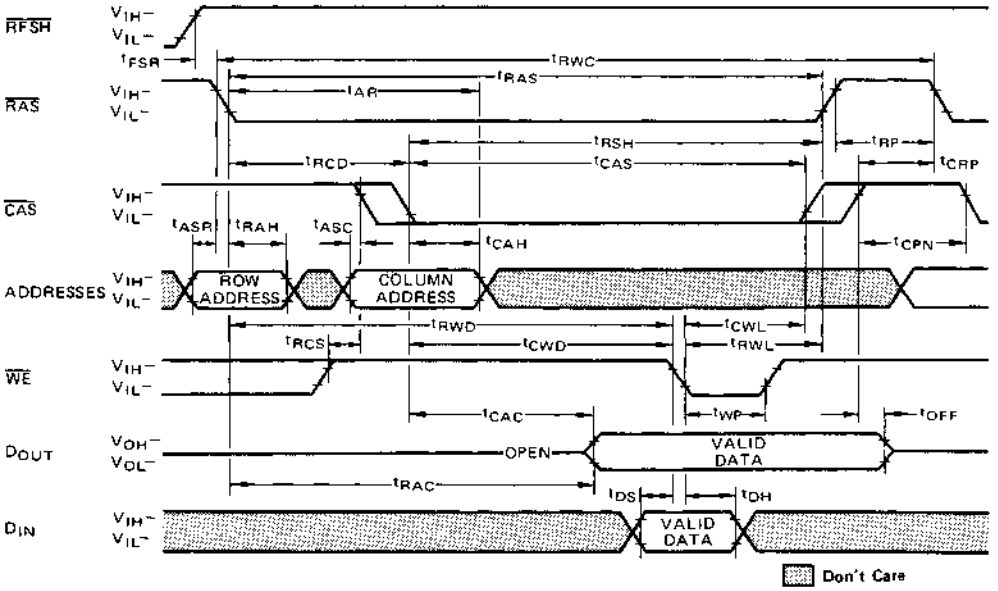
READ CYCLE



WRITE CYCLE (EARLY WRITE)

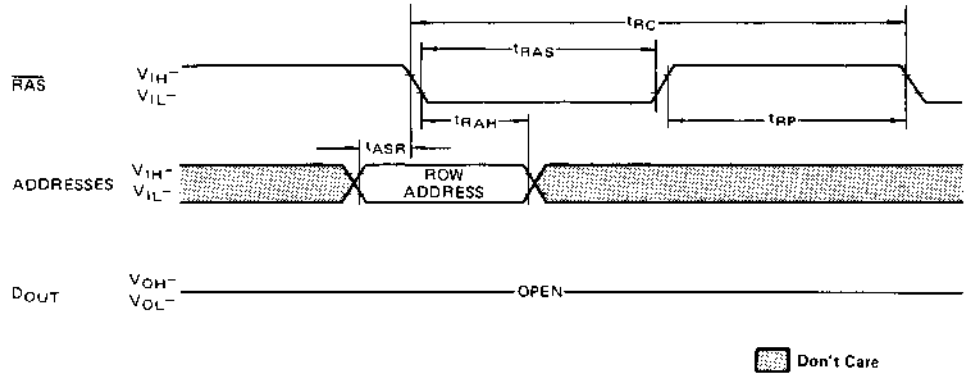


READ-WRITE/READ-MODIFY-WRITE CYCLE

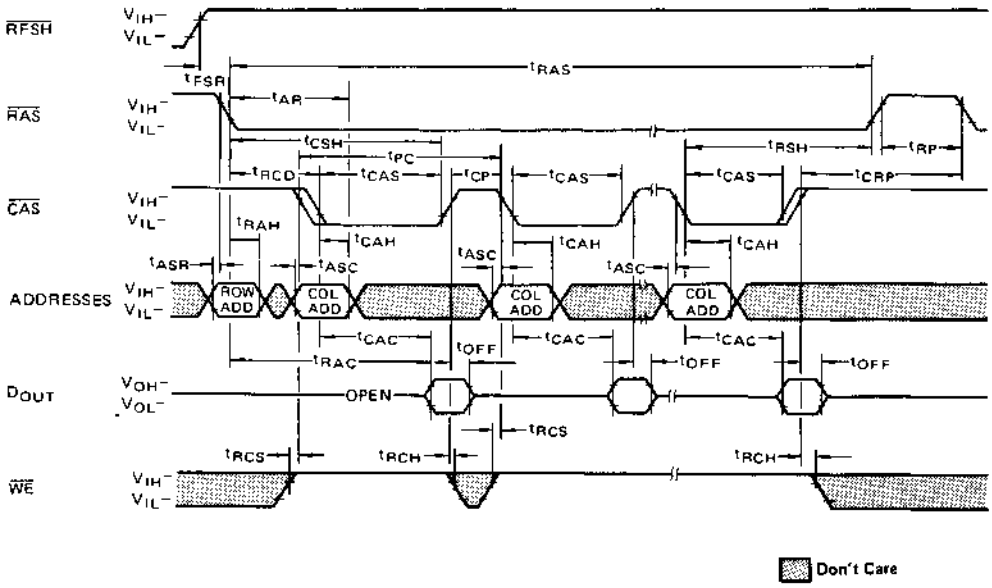


RAS-ONLY REFRESH CYCLE

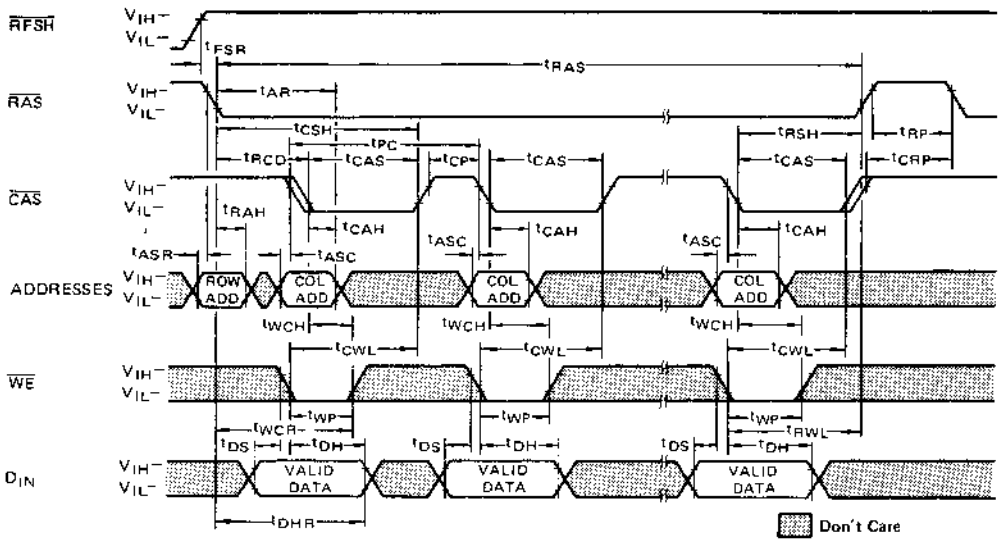
Note: $\overline{RFSH}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't Care



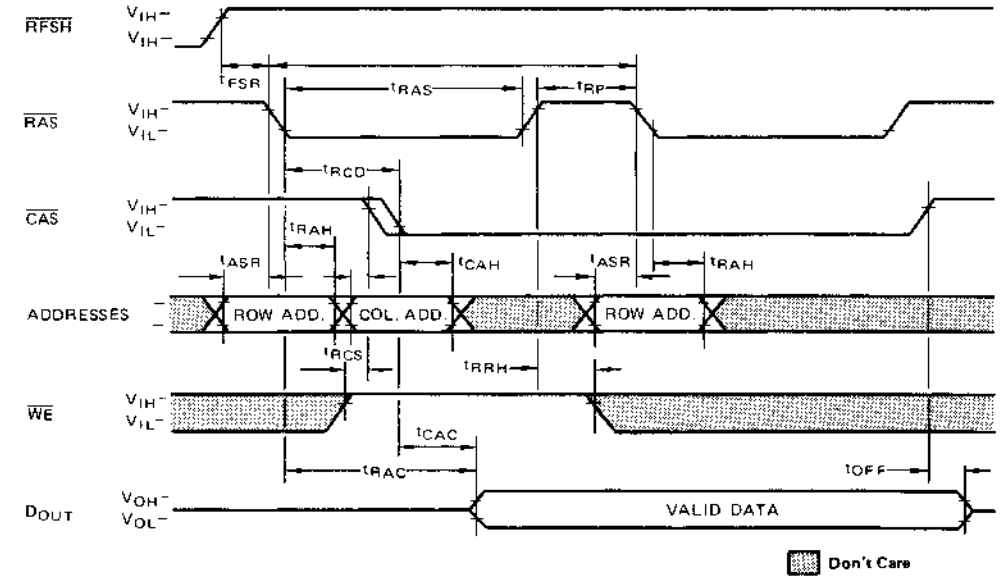
PAGE-MODE READ CYCLE



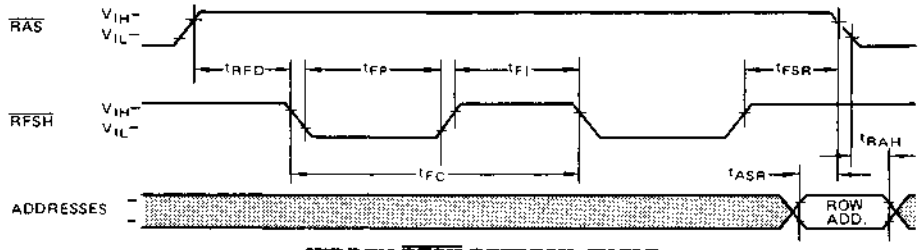
PAGE-MODE WRITE CYCLE



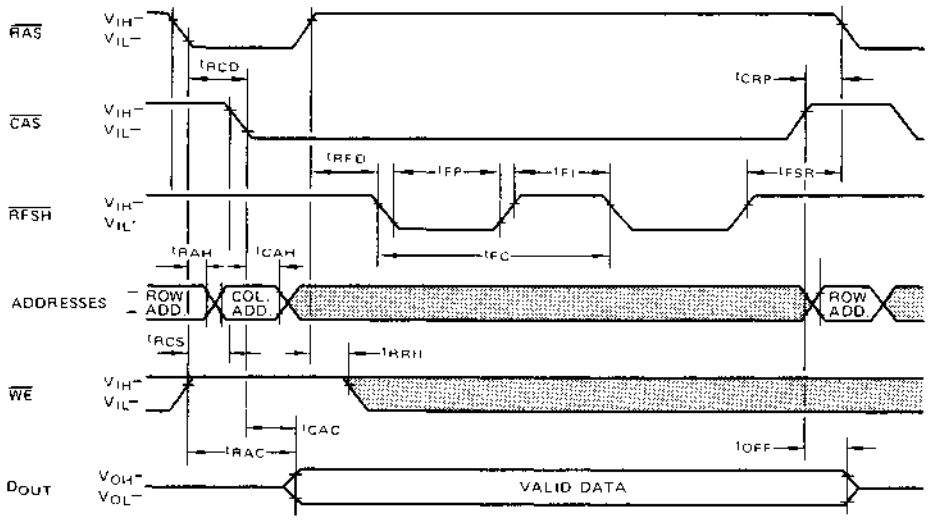
HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE



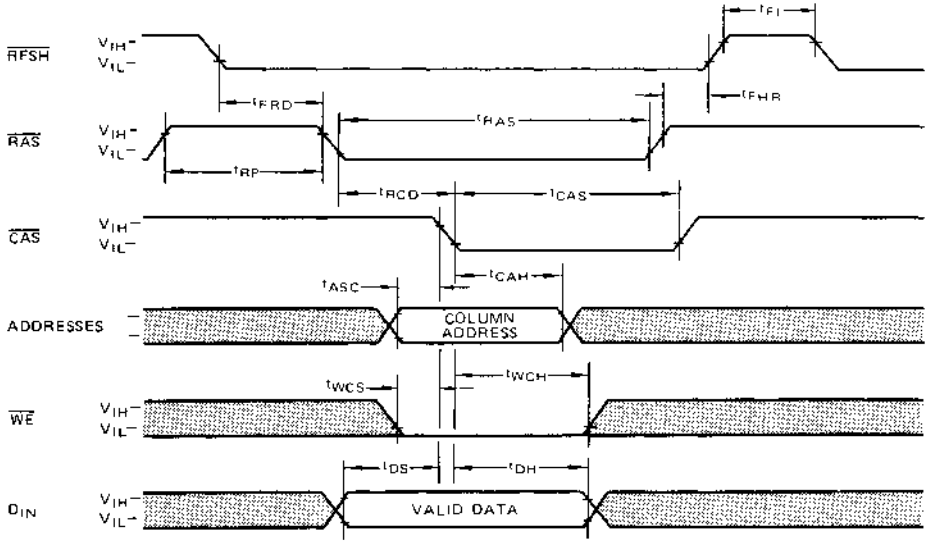
$\overline{RFSH}$ REFRESH CYCLE



HIDDEN $\overline{RFSH}$ REFRESH CYCLE



$\overline{RFSH}$ COUNTER TEST WRITE CYCLE



Don't Care

DESCRIPTION

Address Inputs

A total of fourteen binary input address bits are required to decode any 1 of 16,384 storage cell locations within the MB8117. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). Then seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input

Data written into the MB8117 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8117 while maintaining $\overline{RAS}$ at a logic "low" throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cell is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{RFSH}$ Refresh

$\overline{RFSH}$ type refreshing available on the MB8117 offers an alternate refresh method. When $\overline{RFSH}$ (Pin 1) is brought low and $\overline{RAS}$ is inactive, on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place. When $\overline{RFSH}$ is brought high (inactive) the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ cycle. Only $\overline{RFSH}$ activated cycles affect the internal refresh address counter. The use of $\overline{RFSH}$ type refreshing eliminates the need of providing additional external devices to generate refresh addresses.

Hidden Refresh

Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle.

The MB8117 offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-Only Refresh and Hidden $\overline{RFSH}$ Refresh.

1) Hidden $\overline{RAS}$-Only Refresh
Hidden $\overline{RAS}$-Only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing "$\overline{RAS}$-Only" refresh, but with $\overline{CAS}$ held low. $\overline{RFSH}$ has to be held at V_{IH}.

2) Hidden $\overline{RFSH}$ Refresh
Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.

A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

$\overline{RFSH}$ (PIN 1) TEST CYCLE

A special timing sequence using the PIN 1 counter test cycle provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

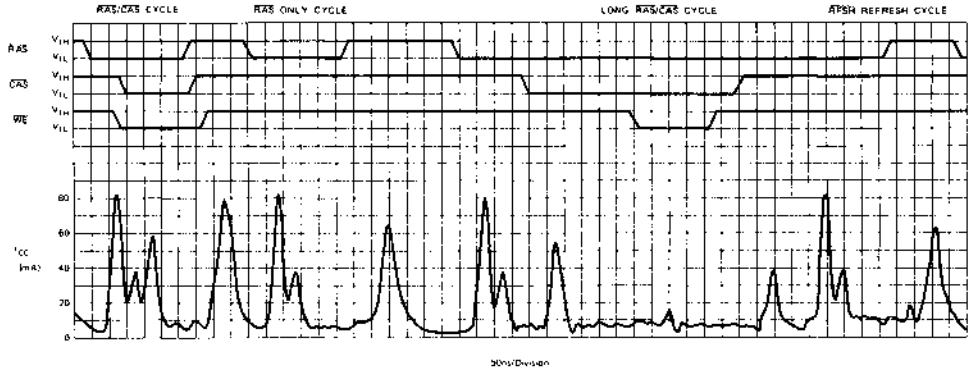
When $\overline{RFSH}$ is activated prior to and remains valid through a normal write cycle, the D_{IN} is written into the memory location defined by the current contents of the on-chip refresh counter and the column address present at the external address pins during the high-to-low transition of $\overline{CAS}$. (See PIN 1 counter test write timing diagram.)

The following test procedure may be used to verify the functionality of the internal refresh counter. There are a multitude of patterns and sequences which may also be used to verify the $\overline{RFSH}$ feature. This test should be performed after it has been confirmed that the device can uniquely address all 16,384 storage locations.

SUGGESTED $\overline{RFSH}$ COUNTER TEST PROCEDURE

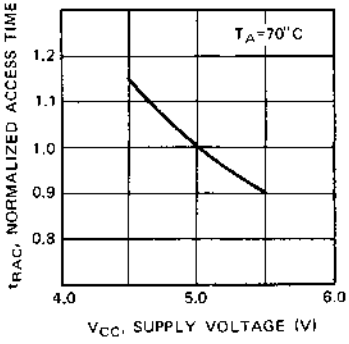
1. Initialize the on-chip refresh counter. 64 cycles are adequate for this purpose.
2. Write a test pattern of zeroes into the memory at a single column address and all row addresses by using 128 $\overline{RFSH}$ (pin 1) refresh counter test write cycles.
3. Verify the data written into the RAM by using the column address used in step 2 and sequence through all row address combinations by using conventional read cycles.
4. Compliment the test pattern and repeat steps 2 and 3.

CURRENT WAVEFORMS (V_{CC} = 5.0V, T_A = 25°C)

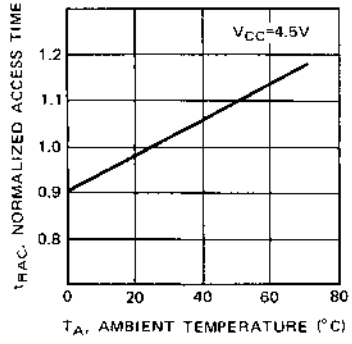


TYPICAL CHARACTERISTICS CURVES

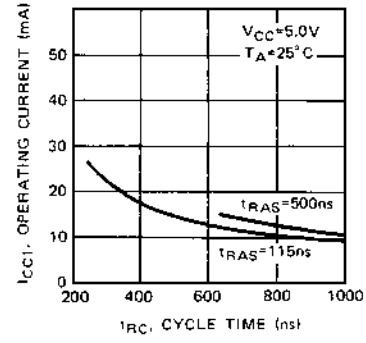
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



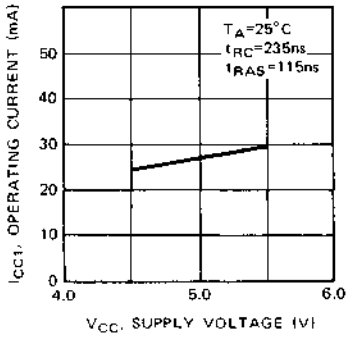
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



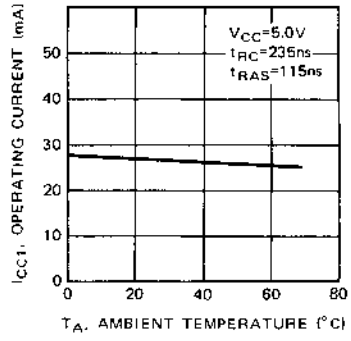
OPERATING CURRENT (TYPICAL) vs CYCLE TIME



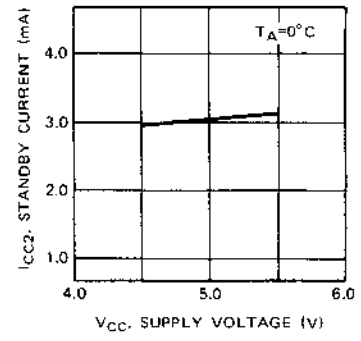
OPERATING CURRENT (TYPICAL) vs SUPPLY VOLTAGE



OPERATING CURRENT (TYPICAL) vs AMBIENT TEMPERATURE

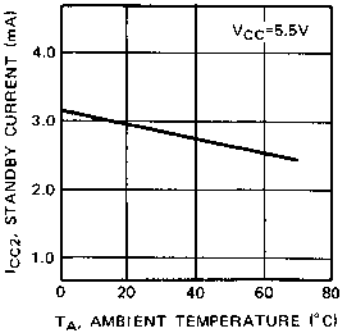


STANDBY CURRENT (TYPICAL) vs SUPPLY VOLTAGE

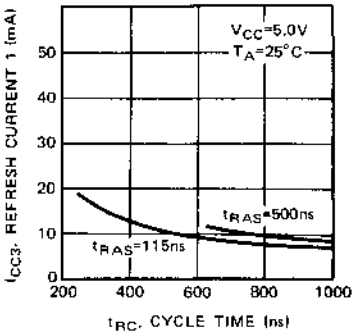


TYPICAL CHARACTERISTICS CURVES, (Continued)

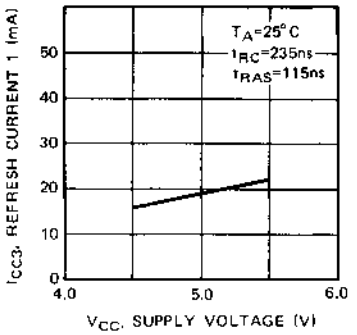
STANDBY CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



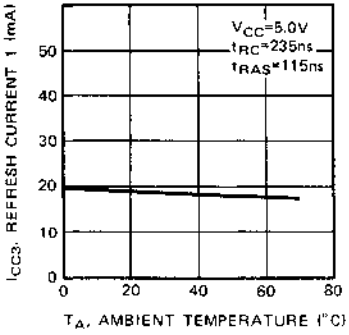
REFRESH CURRENT 1 (TYPICAL) vs CYCLE TIME



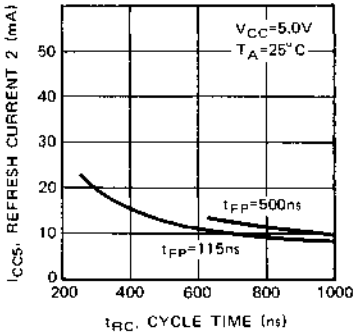
REFRESH CURRENT 1 (TYPICAL) vs SUPPLY VOLTAGE



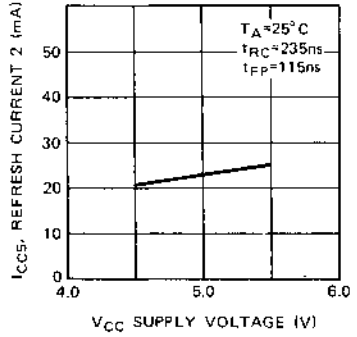
REFRESH CURRENT 1 (TYPICAL) vs AMBIENT TEMPERATURE



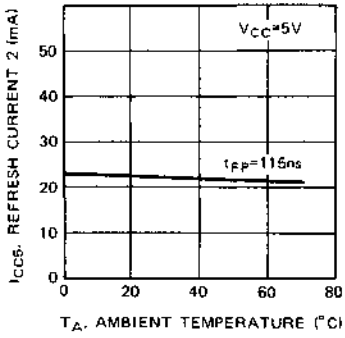
REFRESH CURRENT 2 (TYPICAL) vs CYCLE TIME



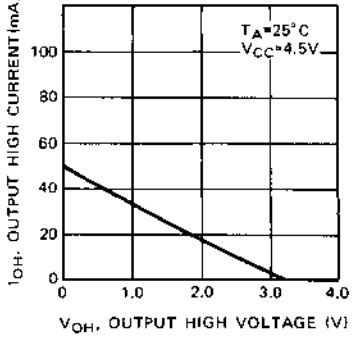
REFRESH CURRENT 2 (TYPICAL) vs SUPPLY VOLTAGE



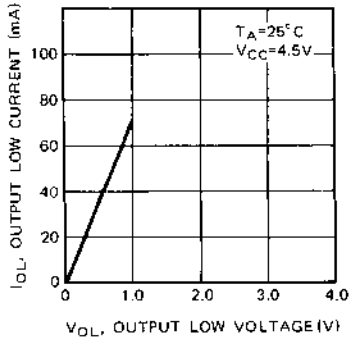
REFRESH CURRENT 2 (TYPICAL) vs AMBIENT TEMPERATURE



OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

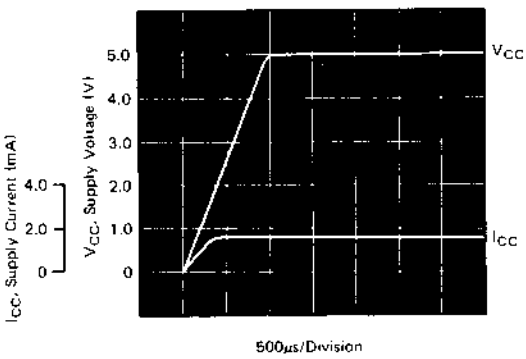


OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE

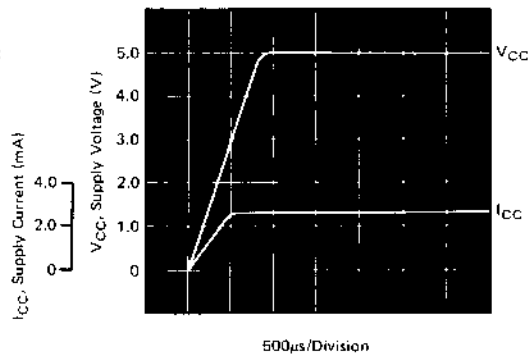


TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1) $\overline{RAS} = V_{IL}$, $\overline{CAS} = V_{IL}$



2) $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IH}$



FUJITSU
MICROELECTRONICS

MB8118-10
MB8118-12

NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

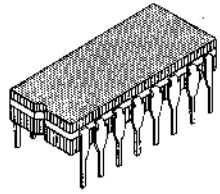
DESCRIPTION

The Fujitsu MB8118 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

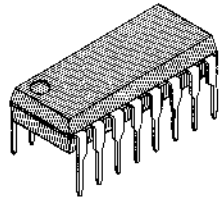
Multiplexed row and column address inputs permit the MB8118 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

The MB8118 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.



CERDIP PACKAGE
DIP-16C-C03

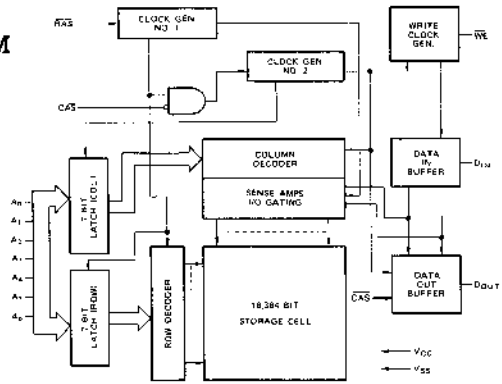


PLASTIC PACKAGE
DIP-16P-M01

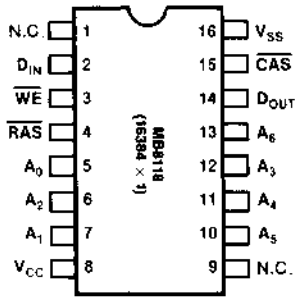
FEATURES

- **16,384 × 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Address access time:**
  100 ns max (MB8118-10)
  120 ns max (MB8118-12)
- **Cycle time:**
  235 ns min (MB8118-10)
  270 ns min (MB8118-12)
- **Low power:**
  182mW max (MB8118-10)
  160mW max (MB8118-12)
  16.5mW max (Standby)
- **+5V single power supply, ± 10% tolerance**
- **On chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Hidden refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Pin compatible with Intel 2118 and MCM4517**

MB8118 BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} pin relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Cerdip	T_{STG}	−55 to +150	°C
	Plastic		−40 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_6, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10		MB8118-12		Unit
			Min	Max	Min	Max	
OPERATING CURRENT Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min)	[1]	I_{CC1}	—	33	—	29	mA
STANDBY CURRENT Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} − High Impedance)		I_{CC2}	—	3.0	—	3.0	mA
REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min)	[1]	I_{CC3}	—	25	—	22	mA
PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min)	[1]	I_{CC4}	—	25	—	22	mA
INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 5.5) Input pins not under test = 0V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V		I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	—	2.4	—	V

Note: [1] I_{CC} is dependent on output loading. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS NOTES 1,2,3

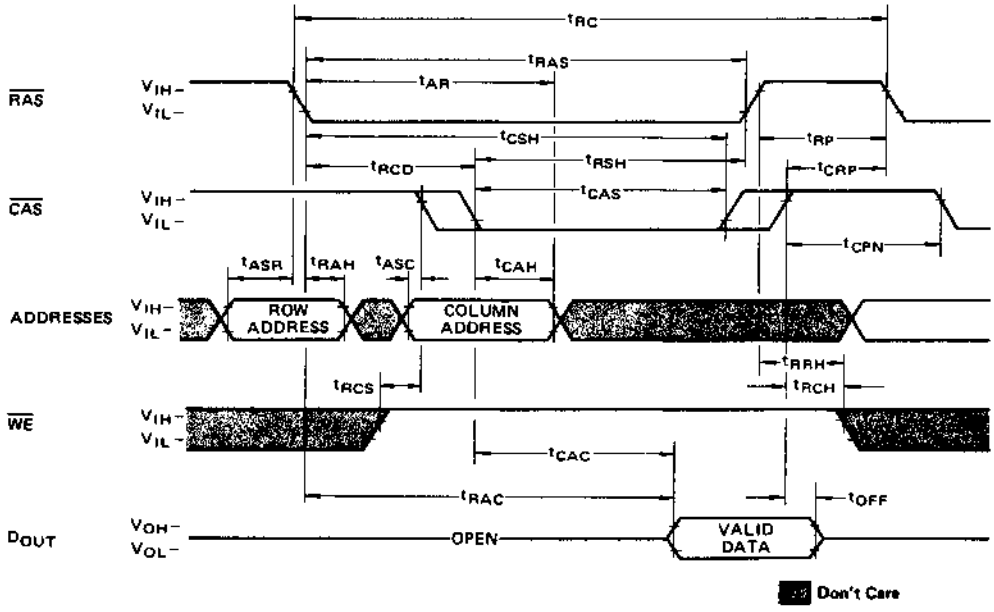
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10			MB8118-12			Unit
			Min	Typ	Max	Min	Typ	Max	
Time Between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	235	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	285	—	—	320	—	—	ns
Page Mode Cycle Time		t_{PC}	125	—	—	145	—	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	—	100	—	—	120	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	—	55	—	—	65	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	45	0	—	50	ns
Transition Time		t_T	3	—	50	3	—	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	110	—	—	120	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	115	—	10000	140	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	70	—	—	85	—	—	ns
$\overline{CAS}$ Prechange Time (all cycles except page mode)		t_{CPN}	50	—	—	55	—	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	60	—	—	70	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	—	10000	65	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100	—	—	120	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	25	—	45	25	—	55	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	15	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	15	—	—	15	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	60	—	—	70	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time		t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	—	0	—	—	ns
Write Command Hold Time		t_{WCH}	30	—	—	35	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	75	—	—	90	—	—	ns
Write Command Pulse Width		t_{WP}	30	—	—	35	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	60	—	—	65	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	45	—	—	50	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	30	—	—	35	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	75	—	—	90	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	55	—	—	65	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	100	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	20	—	—	25	—	—	ns

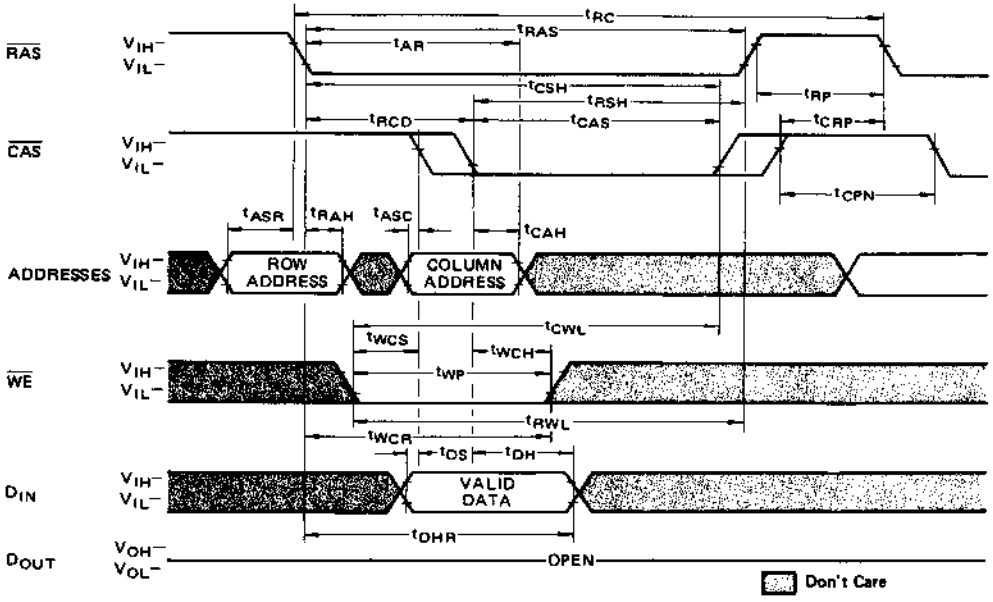
Notes:

1. An initial pause of 200μs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. Dynamic measurements assume t_T=5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RCD} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. $t_{RCD}(min) = t_{RAH}(min) + 2t_T(t_T = 5ns) + t_{ASC}(min)$.
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

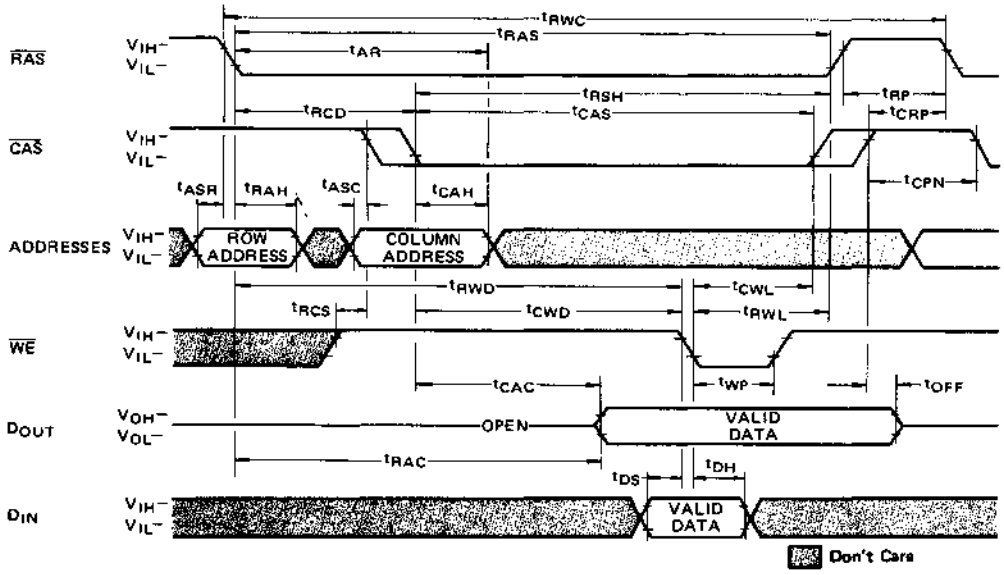
READ CYCLE



WRITE CYCLE (EARLY WRITE)

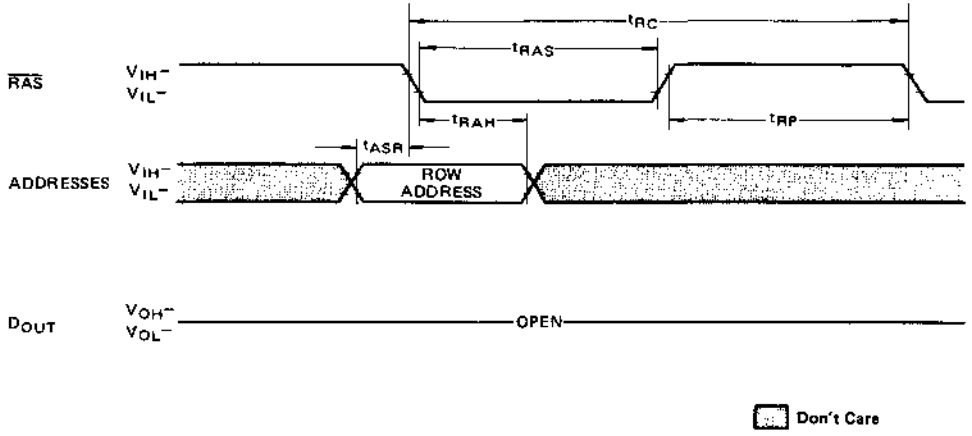


READ-WRITE/READ-MODIFY-WRITE CYCLE

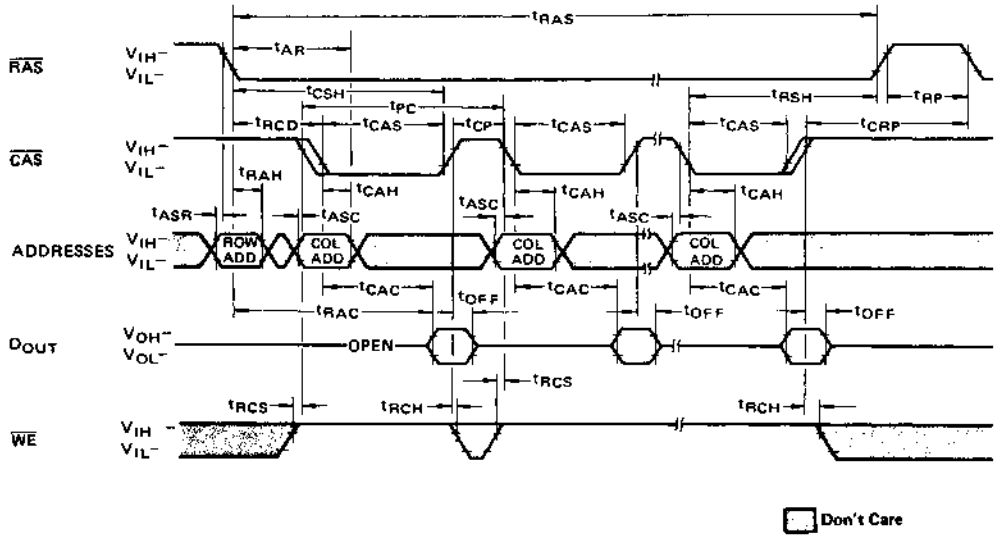


"RAS-ONLY" REFRESH CYCLE

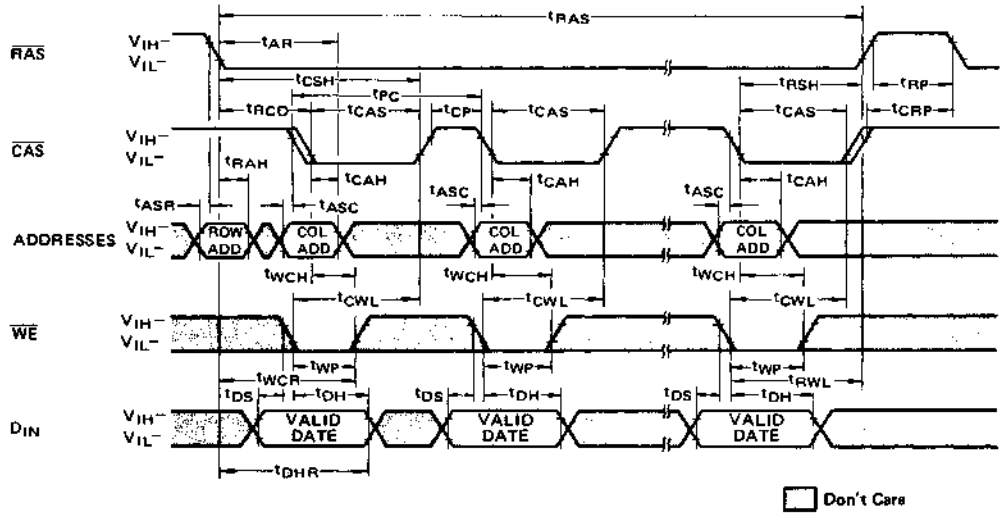
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care



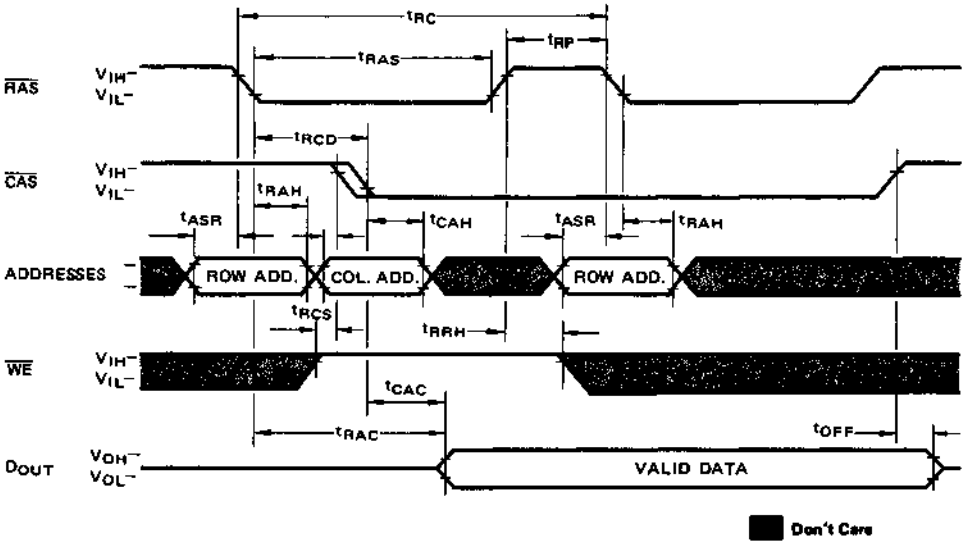
PAGE-MODE READ CYCLE



PAGE-MODE WRITE CYCLE



HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8118. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). Seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:

Data is written into the MB8118 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of RAS when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits latching the row-address into the MB8118 and maintaining $\overline{RAS}$ at a logic "low" throughout all successive memory operations in which the row-address doesn't change. This saves the power required by a $\overline{RAS}$ cycle. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{RAS}$-only refresh prevents any output during refresh because the output buffer is in the high impedance state since $\overline{CAS}$ is at V_{IH}. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in the memory to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle. (See Figure 1 below)

FIG. 1 HIDDEN REFRESH

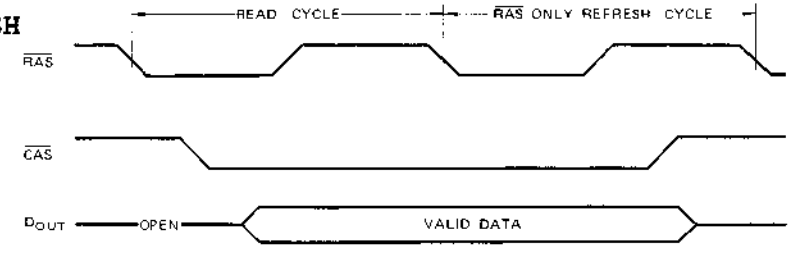
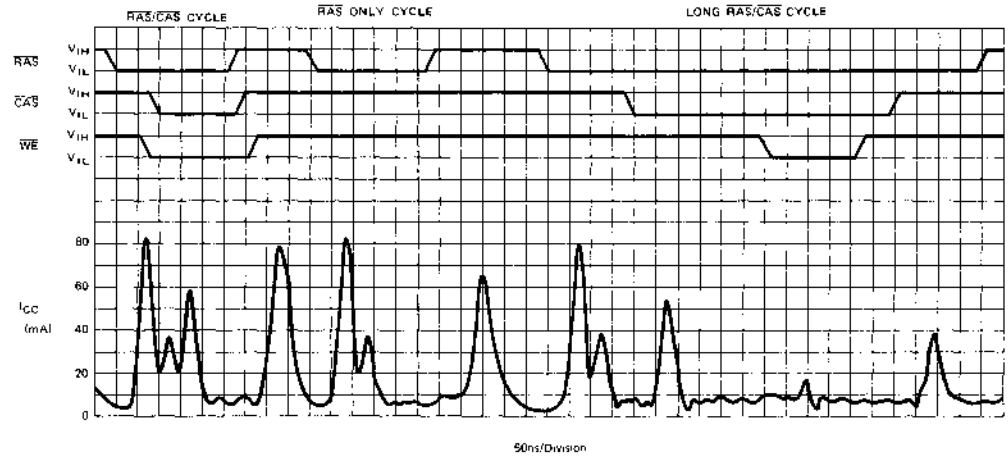
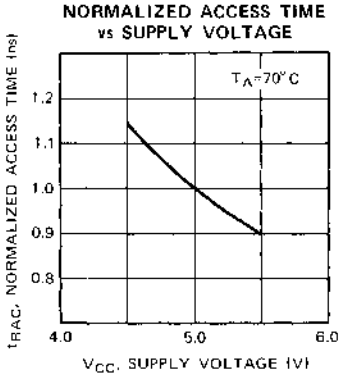
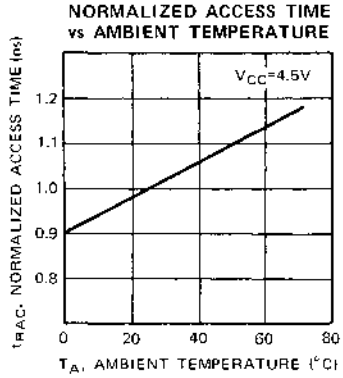


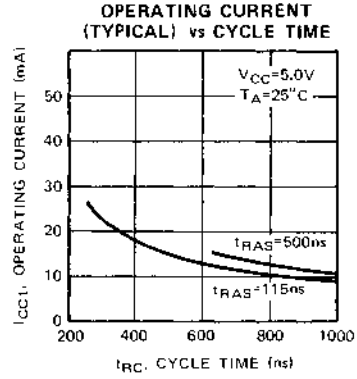
FIG. 2 — CURRENT WAVEFORMS (V_{CC} = 5.0V, T_A = 25°C)

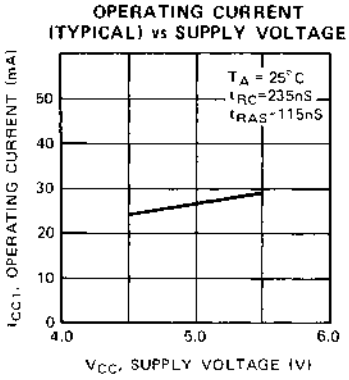


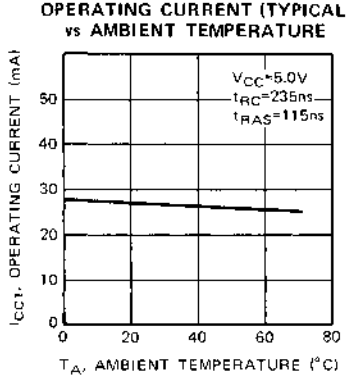
TYPICAL CHARACTERISTICS CURVES

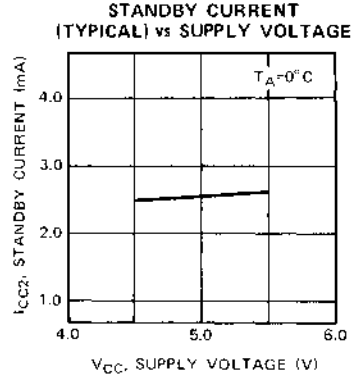






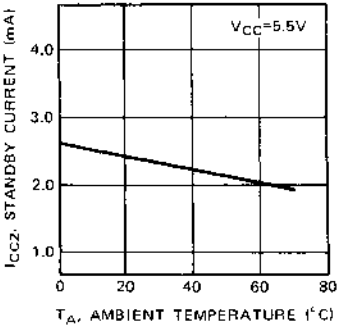




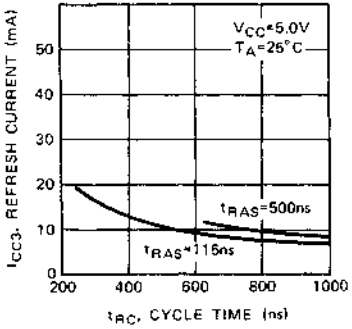


TYPICAL CHARACTERISTICS CURVES (continued)

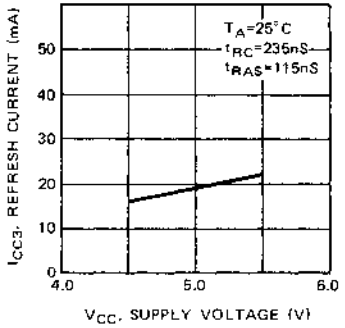
STANDBY CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



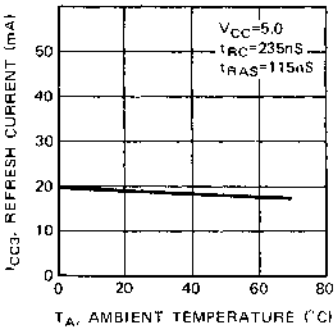
REFRESH CURRENT (TYPICAL) vs CYCLE TIME



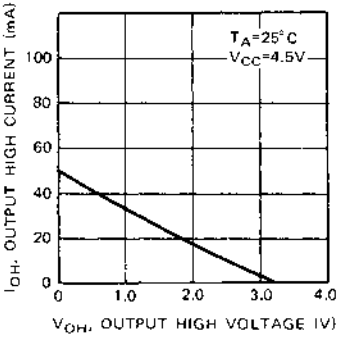
REFRESH CURRENT (TYPICAL) vs SUPPLY VOLTAGE



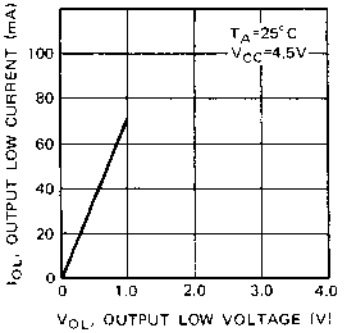
REFRESH CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

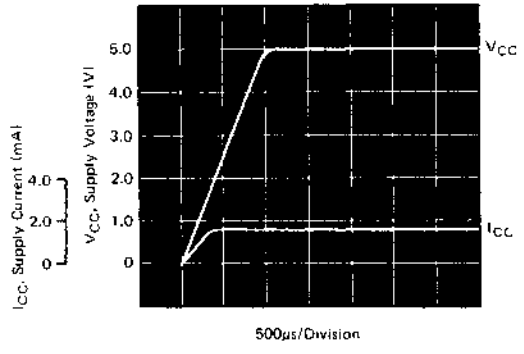


OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE

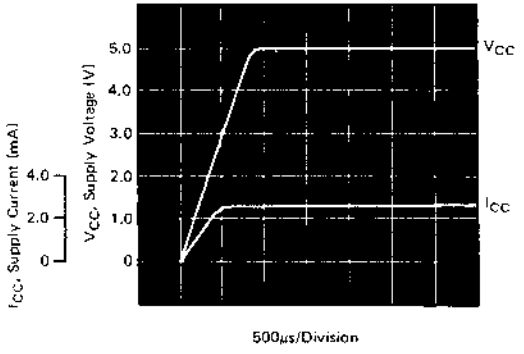


TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1) $\overline{RAS}$=V_{CC}, $\overline{CAS}$=V_{CC}



2) $\overline{RAS}$=V_{SS}, $\overline{CAS}$=V_{SS}



MB8264-15
MB8264-20

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

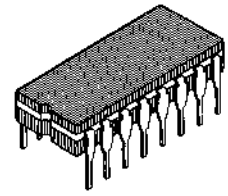
DESCRIPTION

The Fujitsu MB8264 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8264 to be housed in a standard 16-pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8264 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is ±10%. All inputs/outputs are TTL compatible.

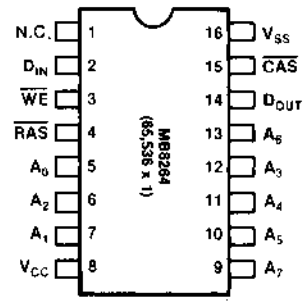


CERDIP PACKAGE
DIP-16C-C04

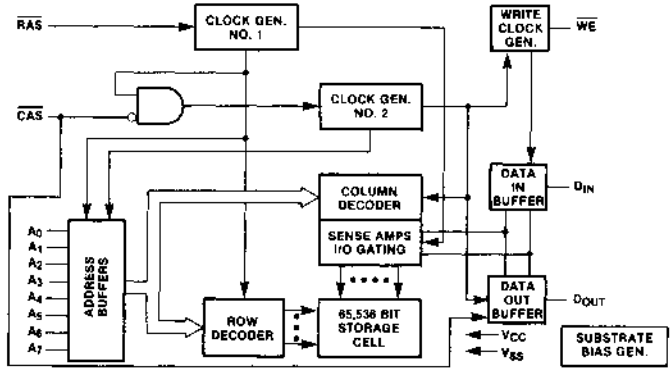
FEATURES

- **65,536 x 1 RAM, 16-pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  150ns Max (MB8264-15)
  200ns Max (MB8264-20)
- **Cycle time:**
  270ns Min (MB8264-15)
  330ns Min (MB8264-20)
- **Low power:**
  22 mW Max Standby
  275 mW Max Active (MB8264-15)
  248 mW Max Active (MB8264-20)
- **±10% tolerance on +5V Supply**
- **On-chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-In**
- **Hidden Refresh Capability**
- **Pin compatible with HM4864, MK4164, TMS4164, MCM6665, μPD4164 and IMS2600**

PIN ASSIGNMENT



MB8264 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT*	MB8264-20	I_{CC1}		45	mA
Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8264-15		—	50	mA
STANDBY CURRENT					
Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	4	mA
REFRESH CURRENT*	MB8264-20	I_{CC3}		36	mA
Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min)	MB8264-15		—	42	mA
PAGE MODE CURRENT*					
Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)		I_{CC4}	—	34	mA
INPUT LEAKAGE CURRENT					
Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V)		I_{IL}	−10	10	μA
Input pins not under test = 0V, V_{CC} = 5.5V, V_{SS} = 0V					
OUTPUT LEAKAGE CURRENT					
(Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
OUTPUT LEVEL					
Output low voltage (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V
OUTPUT LEVEL					
Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS Notes [1,2,3]

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8264-20			MB8264-15			Unit
			Min	Typ	Max	Min	Typ	Max	
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	[4] [6]	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	[5] [6]	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_T	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time (Page Mode Only)		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)		t_{CPN}	30	—	—	25	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	[7] [8]	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time	[10]	t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	[9]	t_{WCS}	−10	—	—	−10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Reference to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[9]	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[9]	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	[10]	t_{RRH}	25	—	—	20	—	—	ns

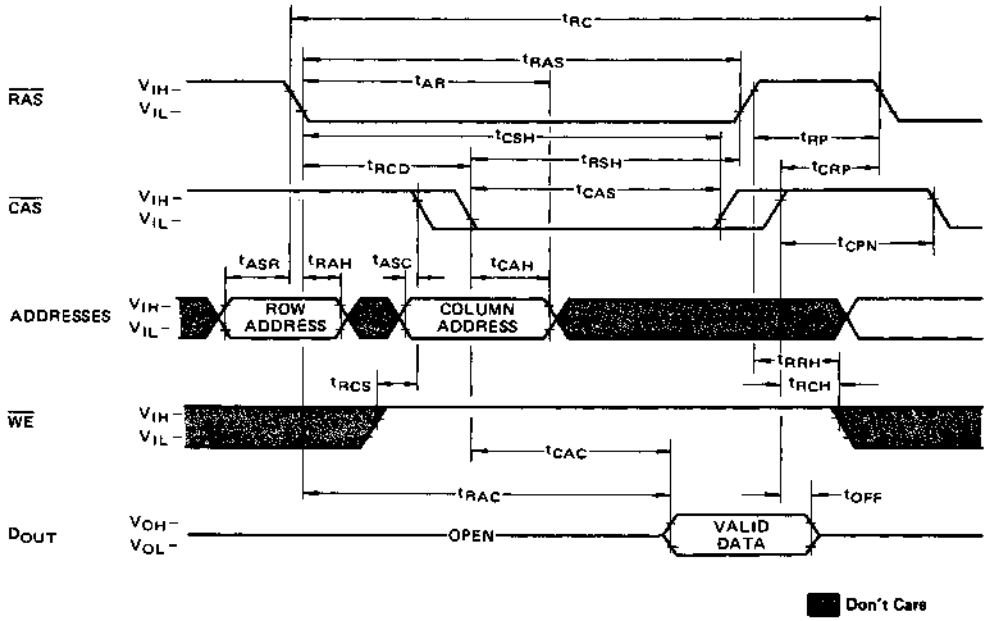
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. $t_{RCD}(min) = t_{RAH}(min) + 2t_T(t_T = 5ns) + t_{ASC}(min)$.
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

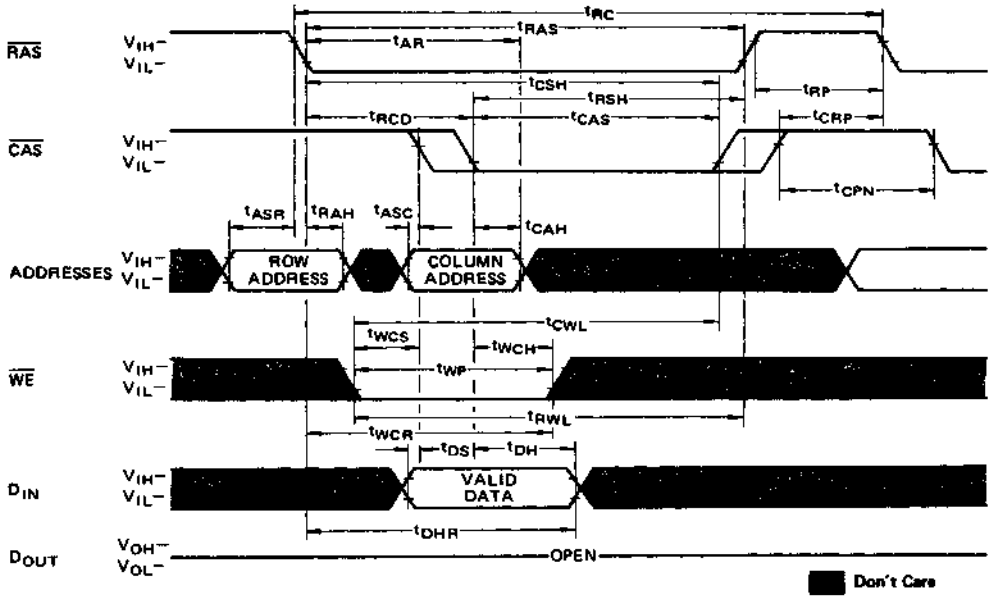
   If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

TIMING DIAGRAMS

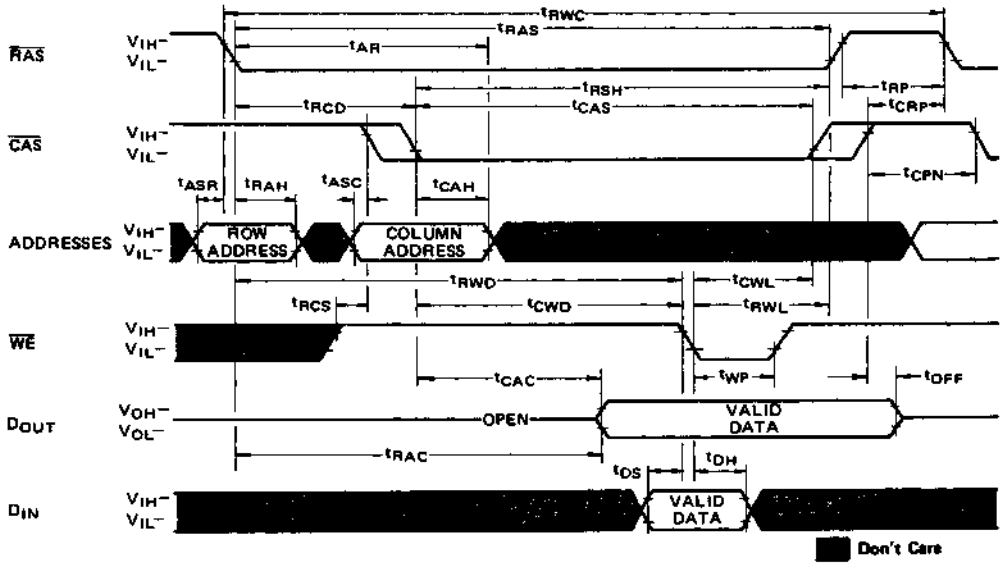
READ CYCLE



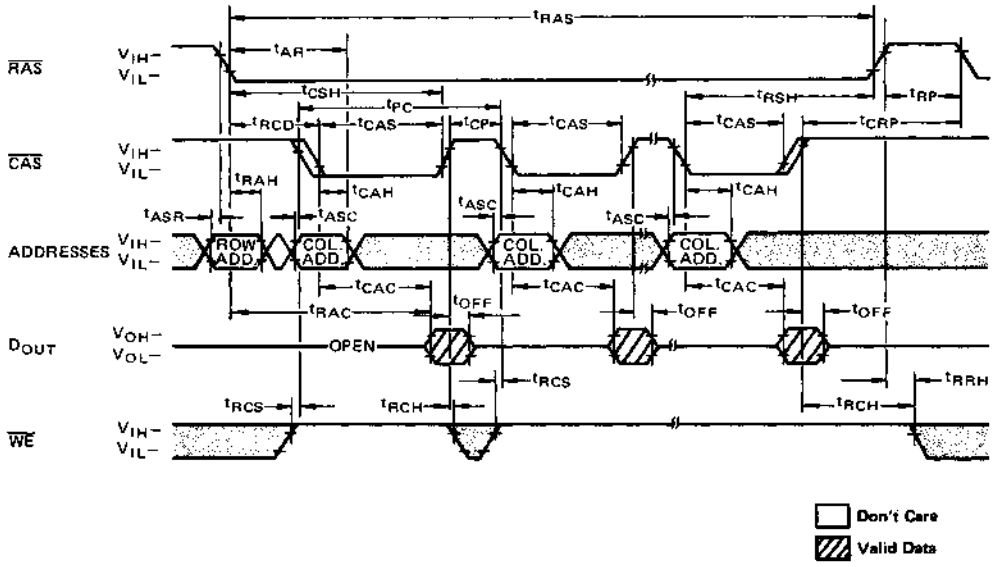
WRITE CYCLE (EARLY WRITE)



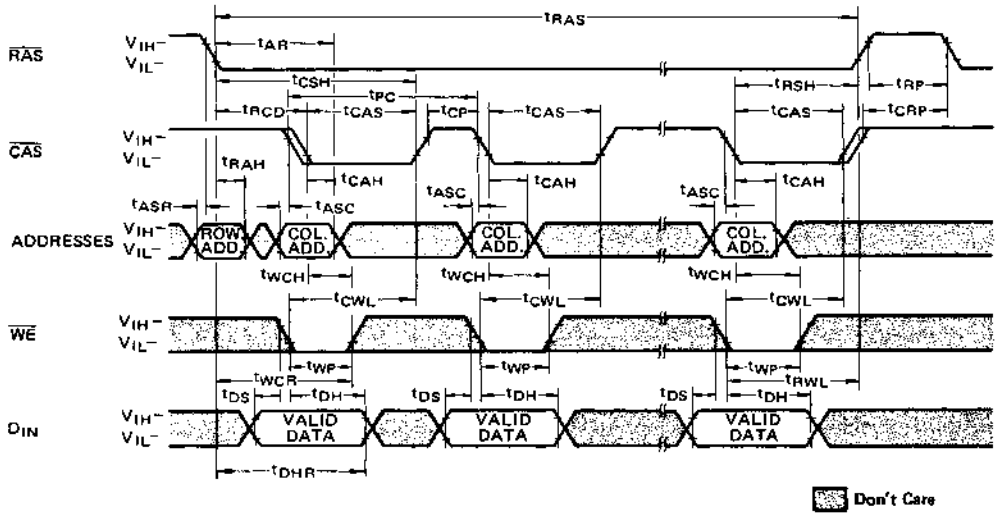
READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

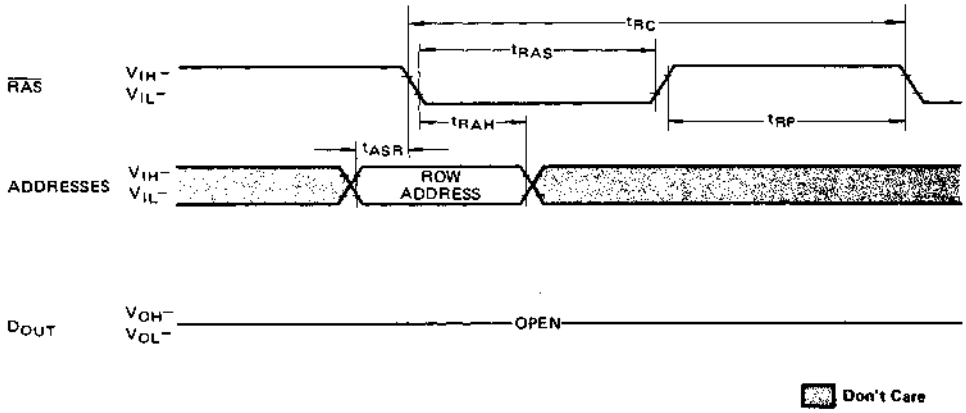


PAGE-MODE WRITE CYCLE

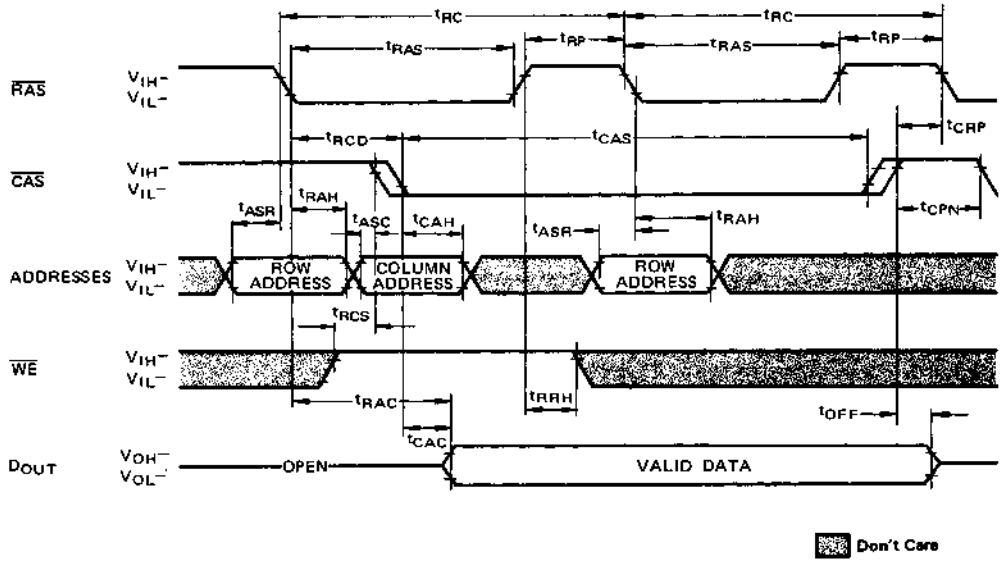


"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care



HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8264. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). Then eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8264 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

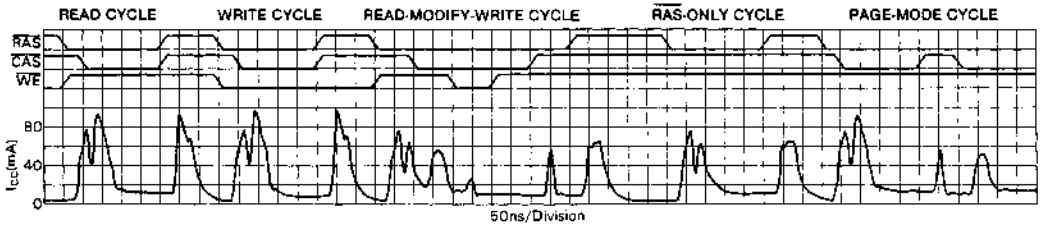
Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

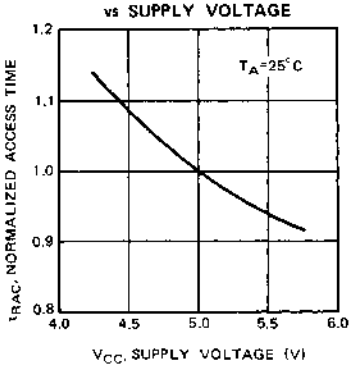
$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25 °C)

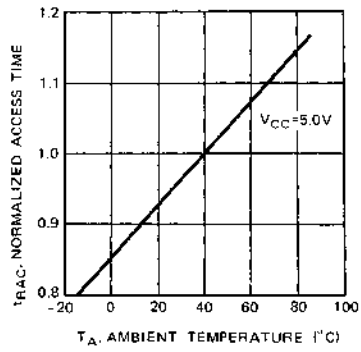


TYPICAL CHARACTERISTICS CURVES

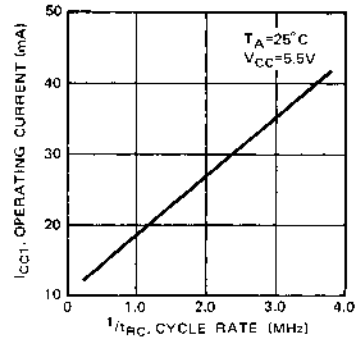
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



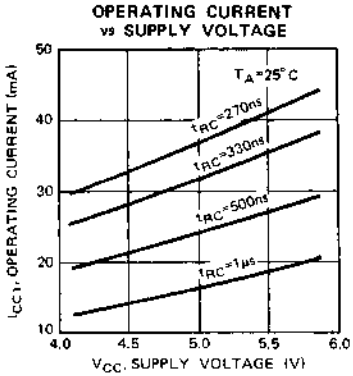
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



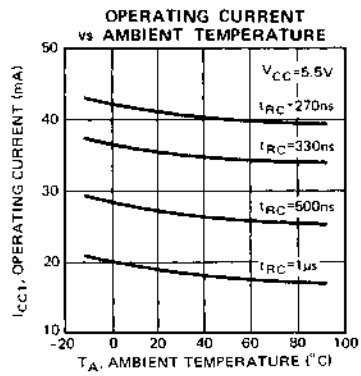
OPERATING CURRENT vs CYCLE RATE



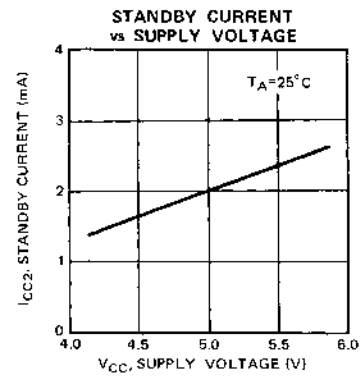
OPERATING CURRENT vs SUPPLY VOLTAGE



OPERATING CURRENT vs AMBIENT TEMPERATURE

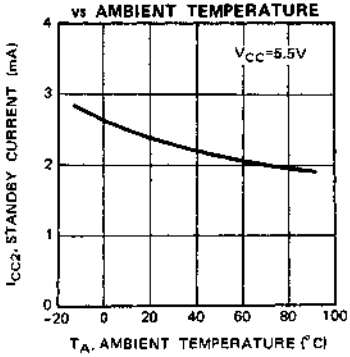


STANDBY CURRENT vs SUPPLY VOLTAGE

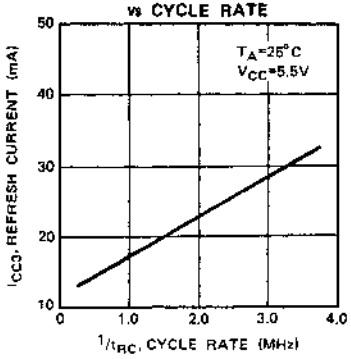


TYPICAL CHARACTERISTICS CURVES (Continued)

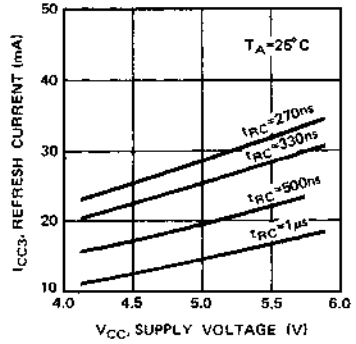
STANDBY CURRENT vs AMBIENT TEMPERATURE



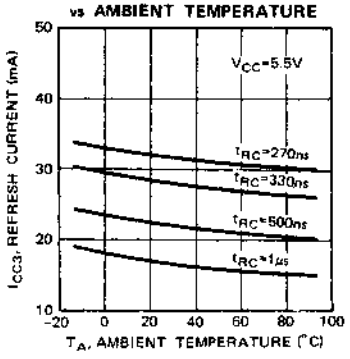
REFRESH CURRENT vs CYCLE RATE



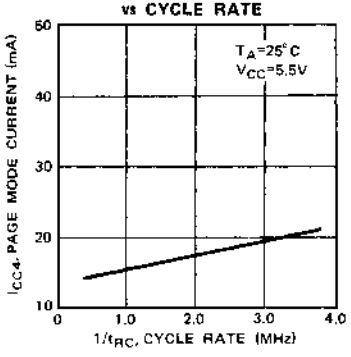
REFRESH CURRENT vs SUPPLY VOLTAGE



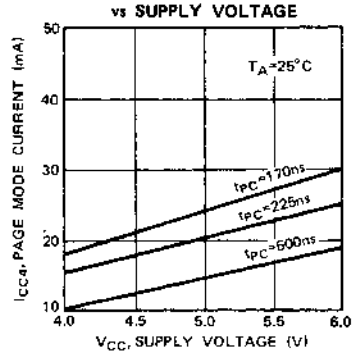
REFRESH CURRENT vs AMBIENT TEMPERATURE



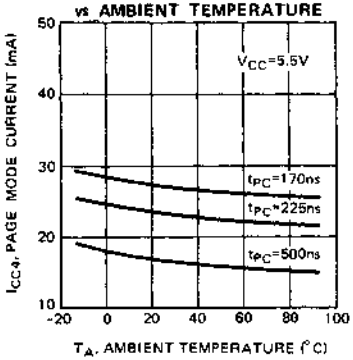
PAGE MODE CURRENT vs CYCLE RATE



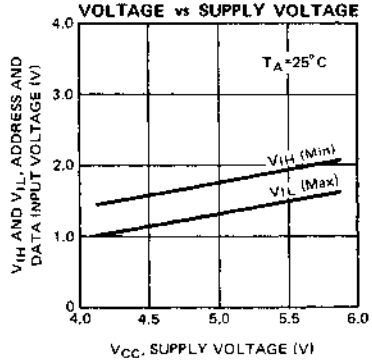
PAGE MODE CURRENT vs SUPPLY VOLTAGE



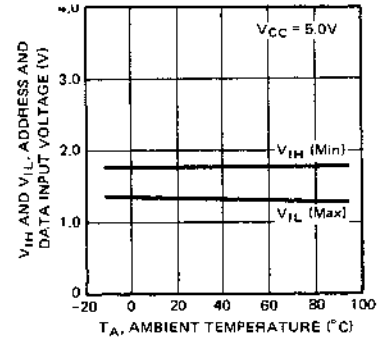
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

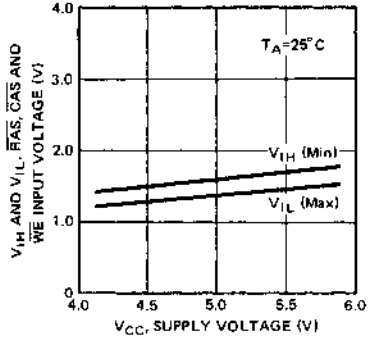


ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

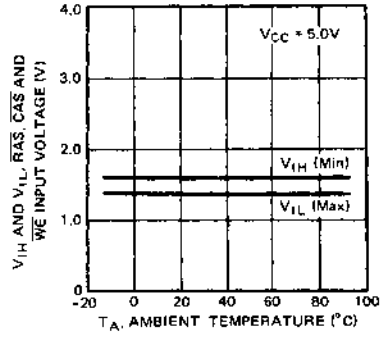


TYPICAL CHARACTERISTICS CURVES (Continued)

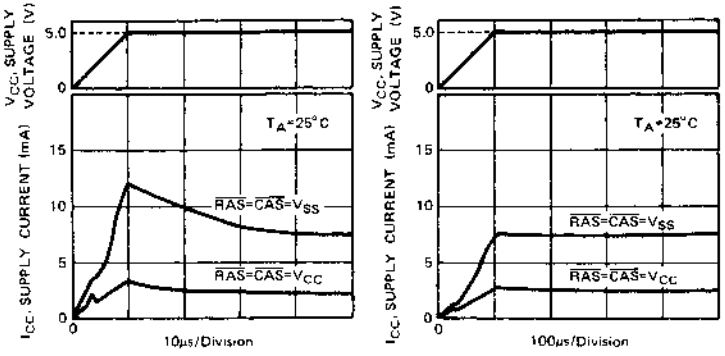
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE



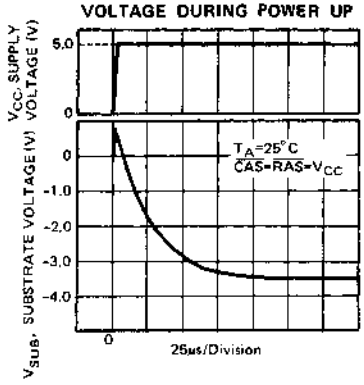
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE



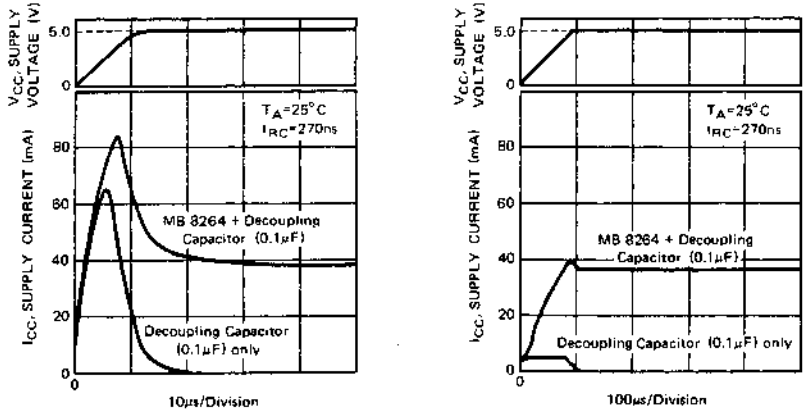
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP



SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE DURING POWER UP



SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP (ON MEMORY BOARD)



FUJITSU
MICROELECTRONICS

MB8264A-10
MB8264A-12

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

ADVANCE INFORMATION

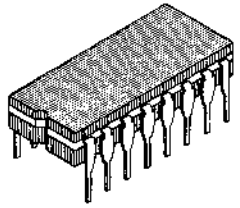
DESCRIPTION

The Fujitsu MB8264A is a fully decoded, dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB8264A to be housed in a standard 16 pin DIP. Pinouts conform to the JEDEC approved pin out.

The MB8264A is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is ±10%. All inputs/outputs are TTL compatible.

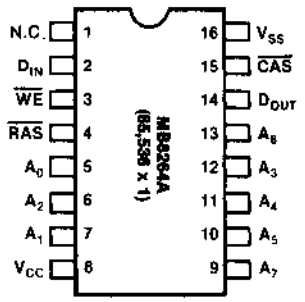


CERDIP PACKAGE
DIP-16C-C04

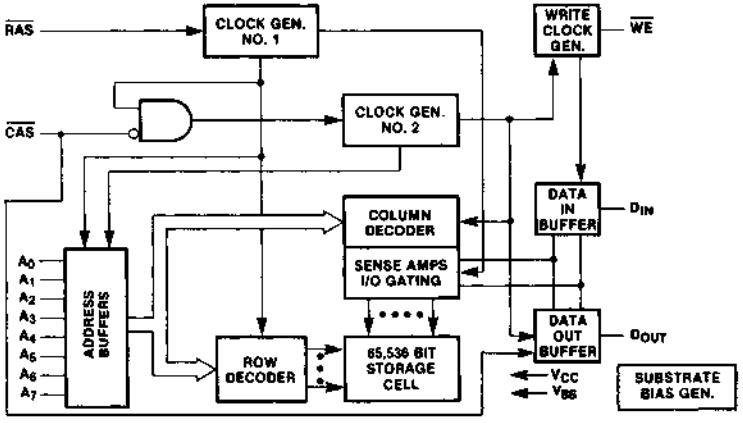
FEATURES

- **65,536 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  - **MB8264A-10 100 ns Max**
  - **MB8264A-12 120 ns Max**
- **Cycle time:**
  - **MB8264A-10 200 ns Min**
  - **MB8264A-12 230 ns Min**
- **Low power:**
  - **MB8264A-10 330mW Max (Active)**
  - **MB8264A-12 300mW Max (Active) 22mW Max (Standby)**
- **±10% tolerance on +5 volt supply**
- **On-chip substrate bias generator**
- **All inputs/outputs TTL compatible, low capacitive load**
- **Three-state output**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, hidden refresh and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**

PIN ASSIGNMENT



MB8264A BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8265-15
MB8265-20

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

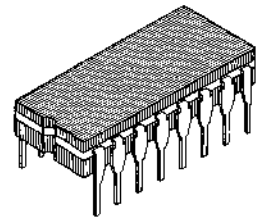
DESCRIPTION

The Fujitsu MB8265 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8265 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8265 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

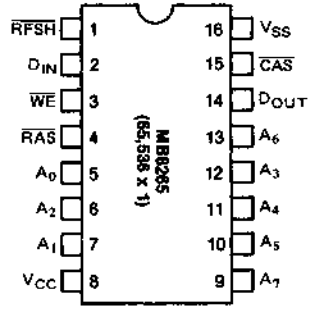


CERDIP PACKAGE
DIP-16C-C04

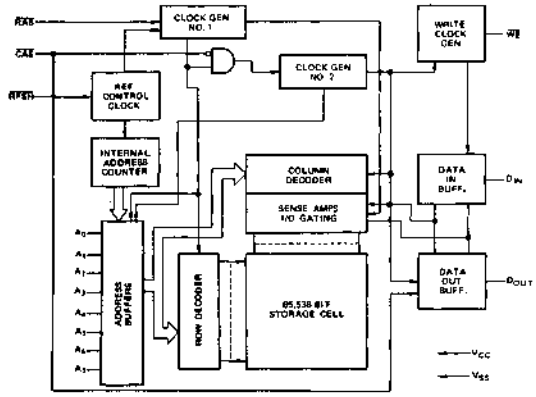
FEATURES

- **65,536 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  150ns Max (MB8265-15)
  200ns Max (MB8265-20)
- **Cycle time:**
  270ns Min (MB8265-15)
  330ns Min (MB8265-20)
- **Low power:**
  275 mW Active, (MB8265-15)
  248 mW Active, (MB8265-20)
  28 mW Standby (Max)
- **+5V Supply, ±10% tolerance**
- **On chip substrate bias generator for high performance**
- **Three-state TTL compatible output**
- **All inputs TTL compatible, low capacitive load**
- **"Gated" CAS**
- **128 refresh cycles**
- **Pin 1 Refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, RAS-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-In**
- **Offers two variations of hidden refresh**

PIN ASSIGNMENT



MB8265 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circut Output Current	I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8265-20	I_{CC1}		45	mA
	MB8265-15		—	50	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH})		I_{CC2}	—	5	mA
REFRESH CURRENT 1 Average power current ($\overline{RAS}$ cycling $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH}; t_{RC} = min)	MB8265-20	I_{CC3}	—	36	mA
	MB8265-15			42	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)		I_{CC4}	—	34	mA
REFRESH CURRENT 2 Average power supply current ($\overline{RFSH}$ cycling; $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, t_{FC} = min)		I_{CC5}	—	46	mA
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V) Input pins not under test = 0V, V_{CC} = 5.5V, V_{SS} = 0V		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
OUTPUT LEVEL Output low voltage (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V
OUTPUT LEVEL Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS Notes [1, 2, 3]

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8265-20 Min	MB8265-20 Typ	MB8265-20 Max	MB8265-15 Min	MB8265-15 Typ	MB8265-15 Max	Unit
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	[4] [6]	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	[5] [6]	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_T	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time (Page Mode Only)		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)		t_{CPN}	30	—	—	25	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to CAS Delay Time	[7] [8]	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time	[10]	t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	[9]	t_{WCS}	−10	—	—	−10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[9]	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[9]	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	[10]	t_{RRH}	25	—	—	20	—	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{RAS}$		t_{FSR}	120	—	—	100	—	—	ns
$\overline{RAS}$ to $\overline{RFSH}$ Delay		t_{RFD}	120	—	—	100	—	—	ns
$\overline{RFSH}$ Cycle Time		t_{FC}	330	—	—	270	—	—	ns
$\overline{RFSH}$ Pulse Width		t_{FP}	200	—	—	150	—	—	ns
$\overline{RFSH}$ Inactive Time		t_{FI}	120	—	—	100	—	—	ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	[11]	t_{FRD}	50	—	—	40	—	—	ns
$\overline{RFSH}$ Hold Time	[11]	t_{FSH}	20	—	—	15	—	—	ns
$\overline{RFSH}$ Address Set Up Time	[11]	t_{ASF}	0	—	—	0	—	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{CAS}$	[11]	t_{FSC}	50	—	—	40	—	—	ns

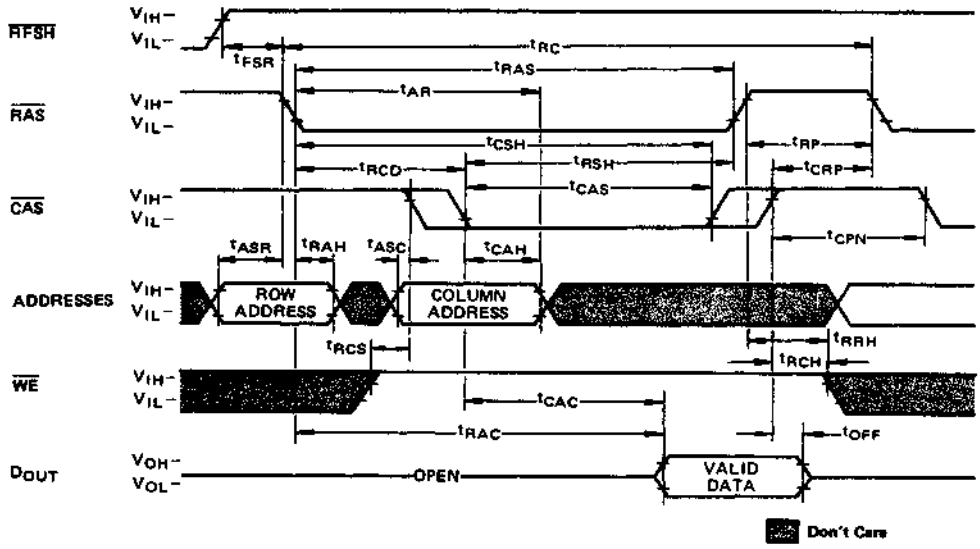
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 active $\overline{RFSH}$ initialization cycles required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the $\overline{RFSH}$ refresh function is used. The $\overline{RFSH}$ must be held at V_{IH} if the $\overline{RFSH}$ function is not used.
2. Dynamic measurements assume $t_T = 5ns$.
3. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}(min)$ and $V_{IL}(max)$.
4. Assumes that $t_{RCD} \leq t_{RCD}(max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
8. $t_{RCD}(min) = t_{RAH}(min) + 2t_T (t_T = 5ns) + t_{ASC}(min)$.
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.

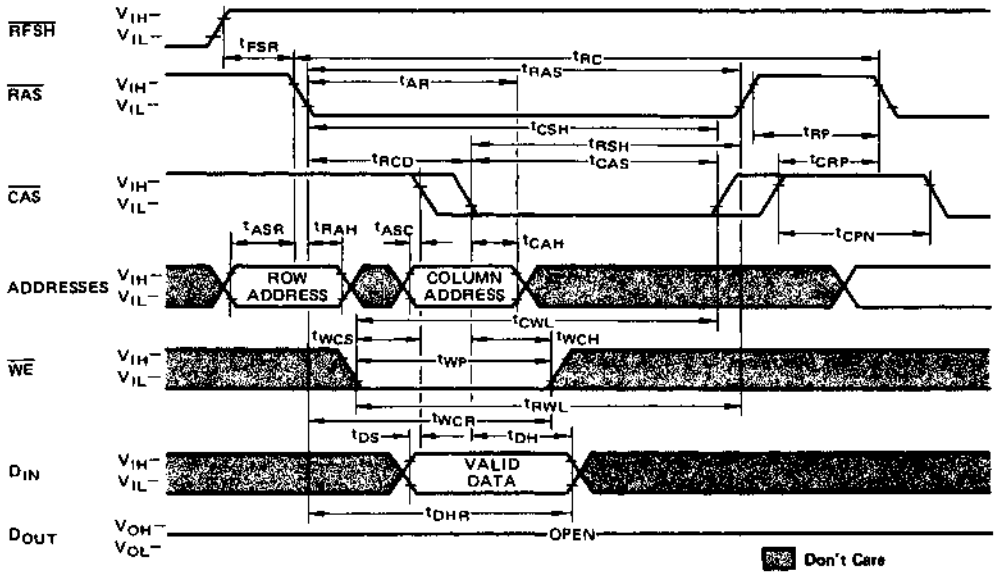
   If $t_{CWD} \geq t_{CWD}(min)$ and $t_{RWD} \geq t_{RWD}(min)$, the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{RFSH}$ counter test read/write cycle only.

TIMING DIAGRAMS

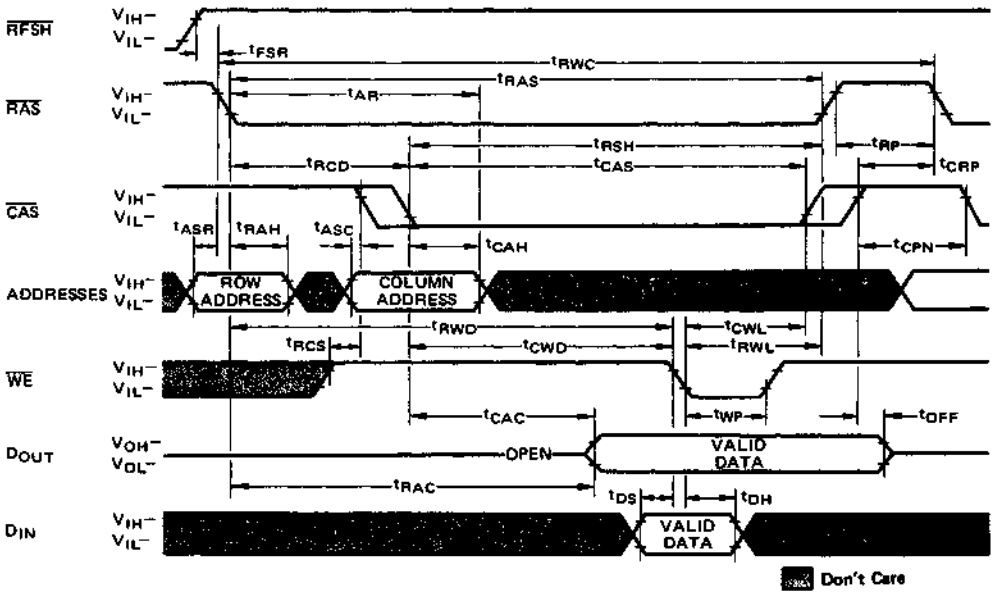
READ CYCLE



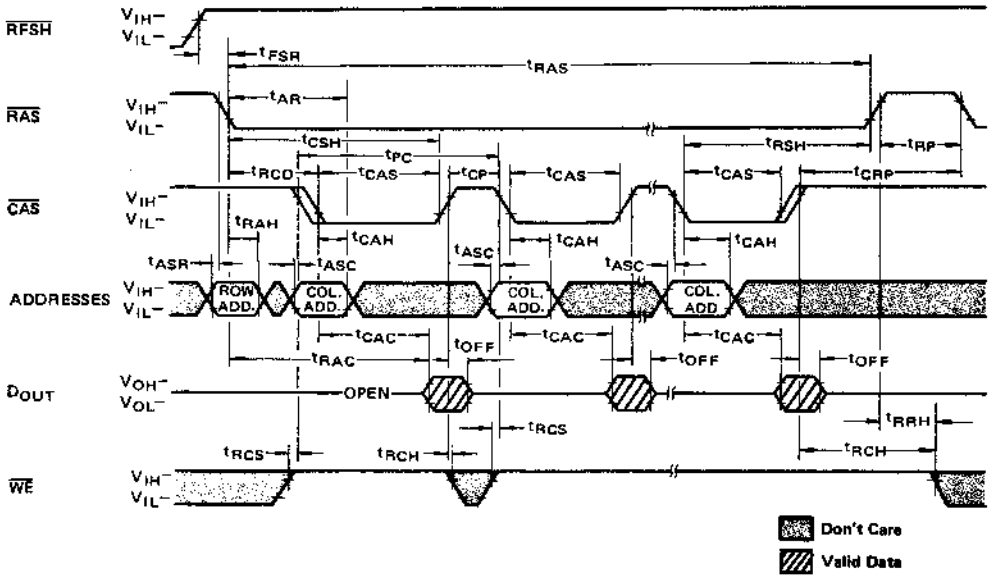
WRITE CYCLE (EARLY WRITE)



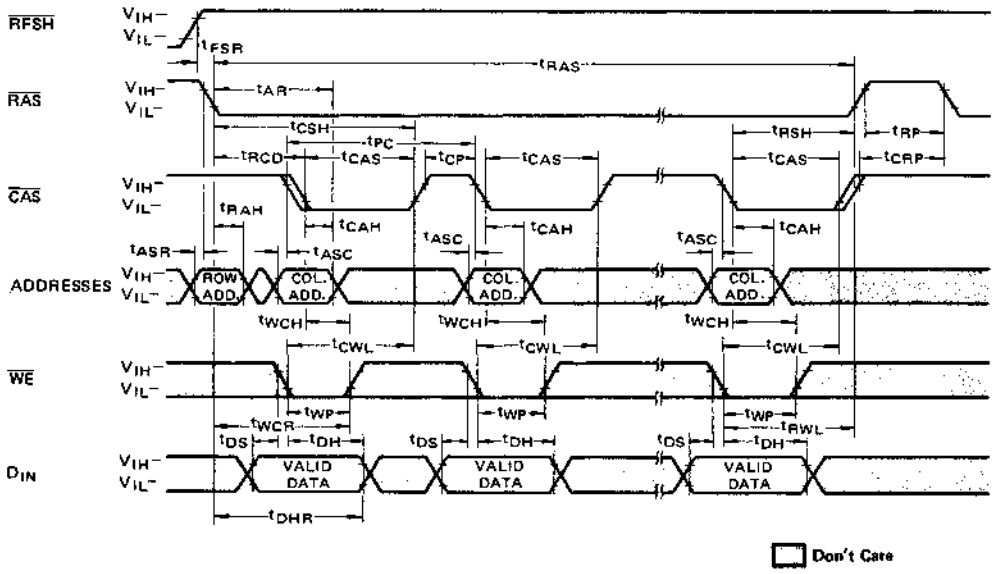
READ-WRITE / READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

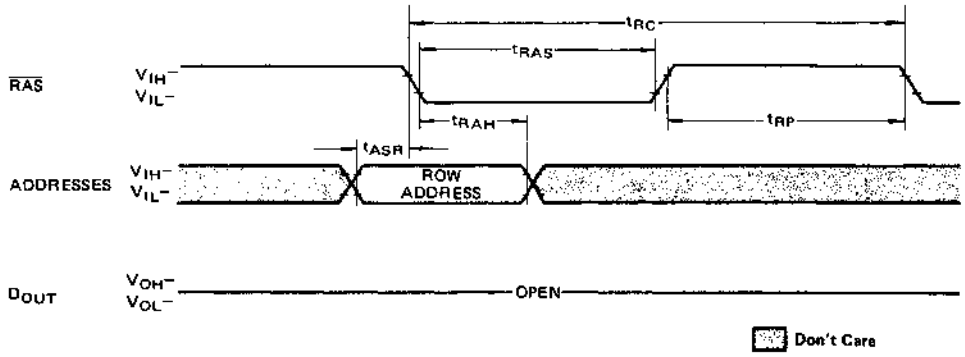


PAGE-MODE WRITE CYCLE



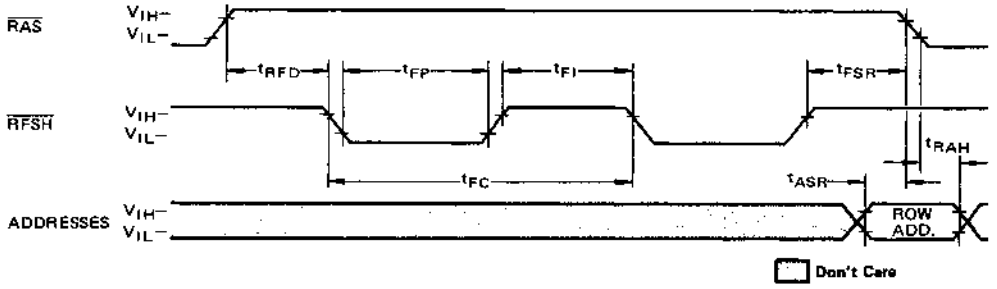
"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{RFSH}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't Care

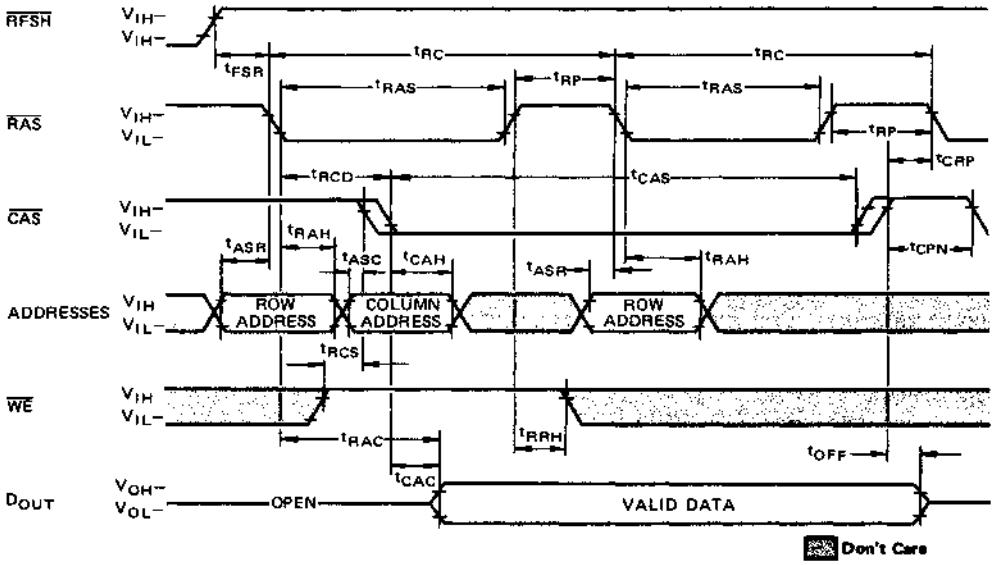


$\overline{RFSH}$ REFRESH CYCLE

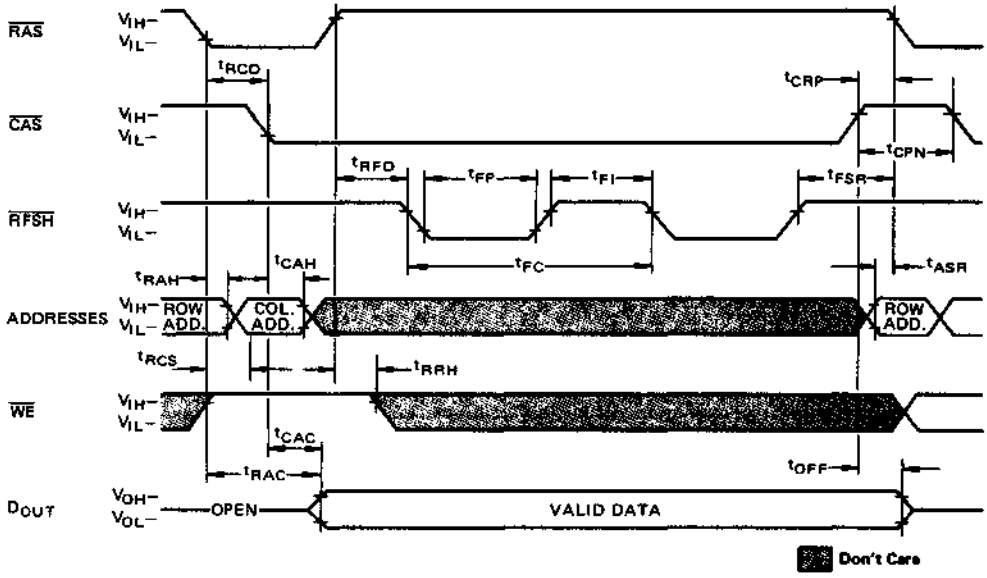
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't Care



HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE

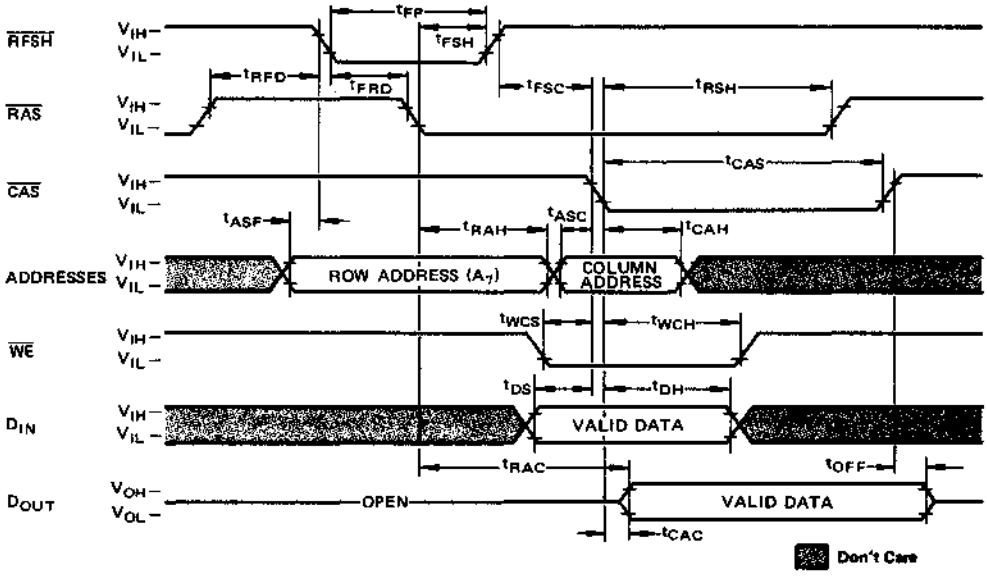


HIDDEN $\overline{RFSH}$ REFRESH CYCLE



$\overline{RFSH}$ COUNTER TEST READ/WRITE CYCLE

Note: D_{OUT} is the waveform in Read-Modify-Write Cycles



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8265. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data written into the MB8265 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to ahigh level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8265 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{RFSH}$ Refresh

$\overline{RFSH}$ type refreshing available on the MB8265 offers an alternate refresh method: (1) When $\overline{RFSH}$ (pin 1) is brought low (active) during $\overline{RAS}$ (Pin 4) is high (inactive), on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place. (2) When $\overline{RFSH}$ is brought high (inactive), the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ refresh cycle. Only $\overline{RFSH}$ activated cycles affect the internal refresh address counter.
The use of $\overline{RFSH}$ type refreshing eliminates the need of providing additional external devices to generate refresh addresses.

Hidden Refresh

Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle.

The MB8265 offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-Only Refresh and Hidden $\overline{RFSH}$ Refresh.

1) Hidden $\overline{RAS}$-Only Refresh
Hidden $\overline{RAS}$-Only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing "$\overline{RAS}$-Only" refresh, but with $\overline{CAS}$ held low. $\overline{RFSH}$ has to be held at V_{IH}.

2) Hidden $\overline{RFSH}$ Refresh
Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.

A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

Refresh Counter Test Cycle

A special timing sequence provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

(A) $\overline{RFSH}$ Test Read/Write Cycle

When $\overline{RFSH}$ is given a signal in timing as shown in timing diagram of $\overline{RFSH}$ counter Test Read/Write Cycle, Read/Write Operation is enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed can be defined as follows:

* A ROW ADDRESS — Bits $A_0 \sim A_8$ are defined when contents of the internal address counter are latched. The other bit A_7 is defined by latching a level on A_7 pin during $\overline{RFSH}$ = "L" and $\overline{RAS}$ = "H" (t_{RFD}).
* A COLUMN ADDRESS — All the bits $A_0 \sim A_7$ are defined by latching levels on $A_0 \sim A_7$ pins in a high-to-low transition of $\overline{CAS}$.

DESCRIPTION (Continued)

By using a 16-bit address latched into the on-chip address buffers by means of the above operation, any of 64K memory cells can be read/written into/from.

(B) $\overline{RFSH}$ Test Read-Modify-Write Cycle

Also, Read-Modify-Write Operation (not only the above normal Read/Write Operations) can be used in this $\overline{RFSH}$ Counter Test Cycle.

(C) Example of Refresh Counter Test Procedure

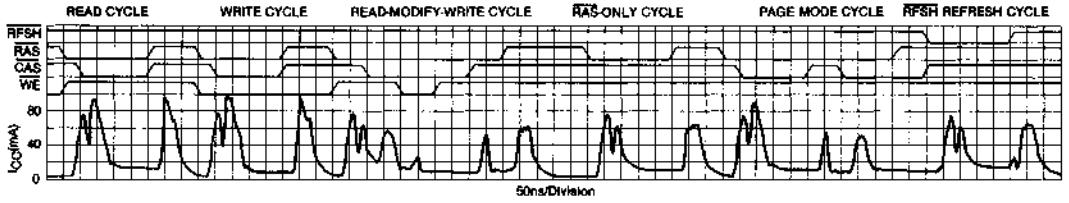
(1) Initialize the internal refresh counter. For this operation, 8 $\overline{RFSH}$ cycles are required.

(2) Write a test pattern of "0"s into the memory cells at a single column address and 128 row addresses by using 128 RFSH Test Write Cycle or RFSH Test Read-Modify-Write Cycle. (At this time, A_7 (row) must be fixed at "H" or "L".).

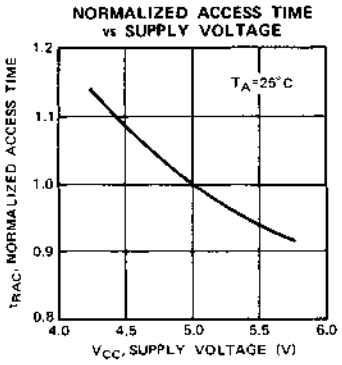
(3) Verify the data written into the memory cells in the above step (2) by using the column address used in step (2) and sequence through 128 row address combinations ($A_0 \sim A_6$) by means of normal Read Cycle. (At this time, A_7 (row) must be fixed at the same level as the above step (3).)

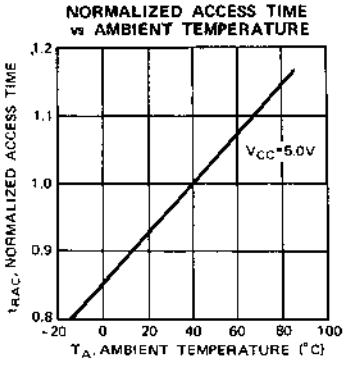
(4) Compliment the test pattern and repeat steps (2) and (3).

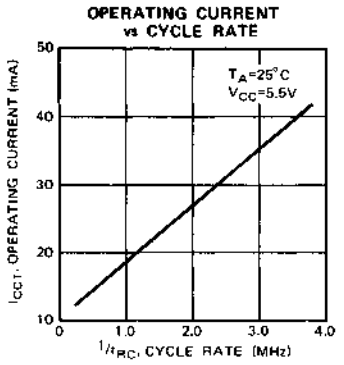
CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

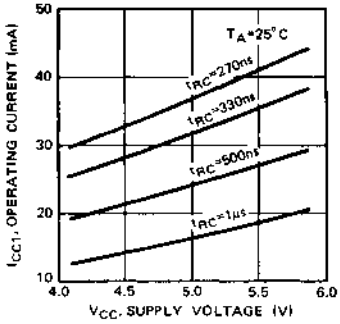




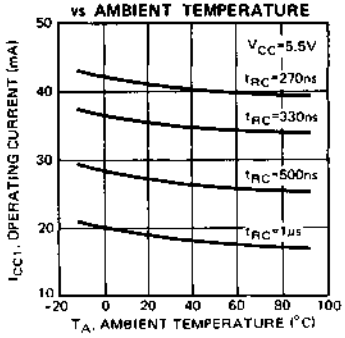


TYPICAL CHARACTERISTICS CURVES (Continued)

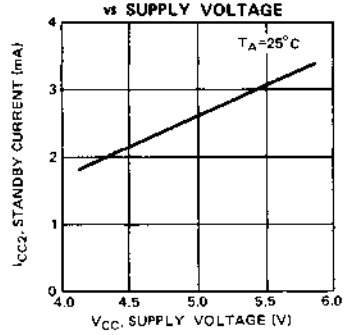
OPERATING CURRENT vs SUPPLY VOLTAGE



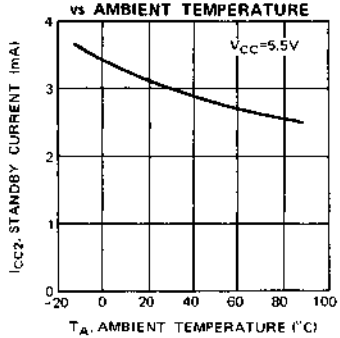
OPERATING CURRENT vs AMBIENT TEMPERATURE



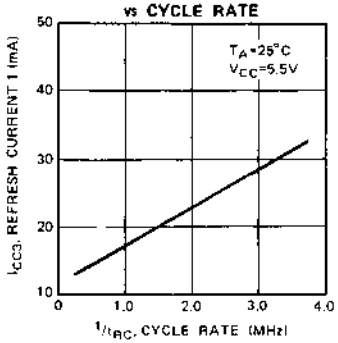
STANDBY CURRENT vs SUPPLY VOLTAGE



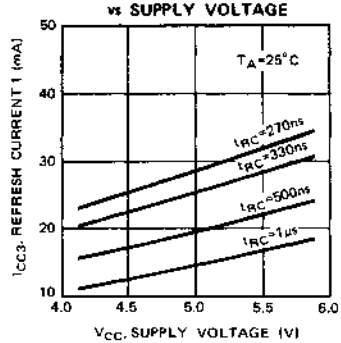
STANDBY CURRENT vs AMBIENT TEMPERATURE



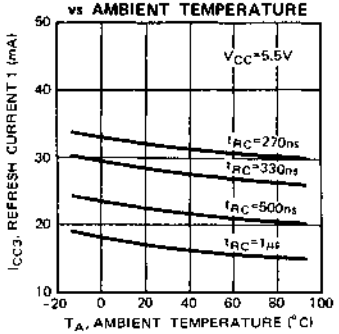
REFRESH CURRENT 1 vs CYCLE RATE



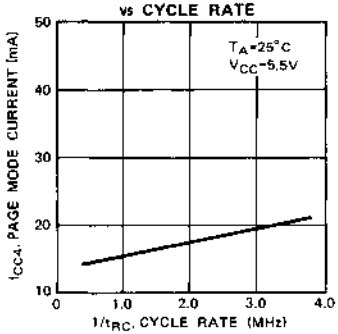
REFRESH CURRENT 1 vs SUPPLY VOLTAGE



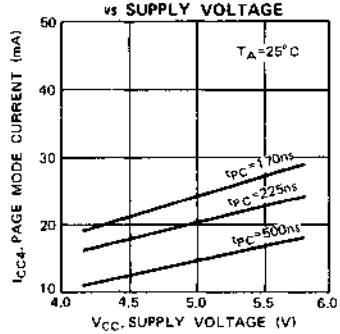
REFRESH CURRENT 1 vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

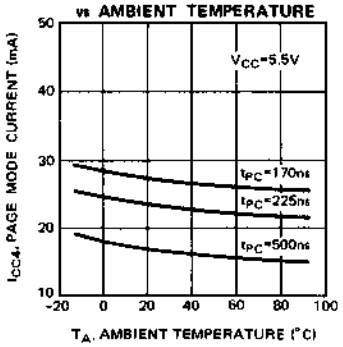


PAGE MODE CURRENT vs SUPPLY VOLTAGE

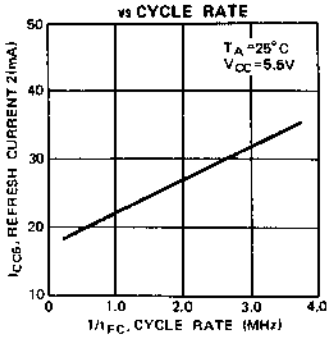


TYPICAL CHARACTERISTICS CURVES (Continued)

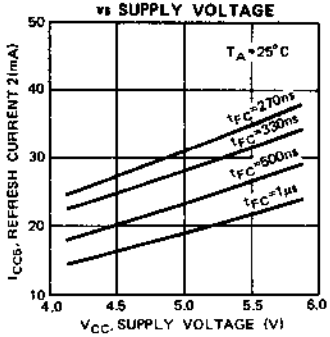
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



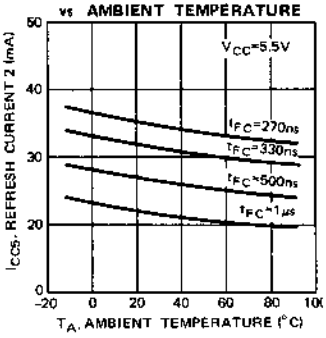
REFRESH CURRENT 2 vs CYCLE RATE



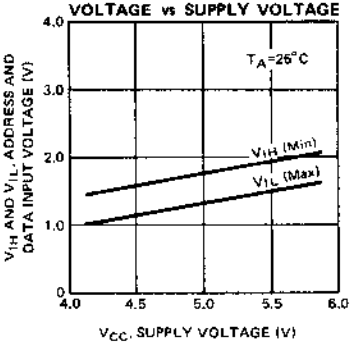
REFRESH CURRENT 2 vs SUPPLY VOLTAGE



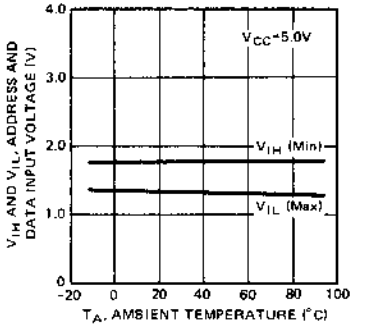
REFRESH CURRENT 2 vs AMBIENT TEMPERATURE



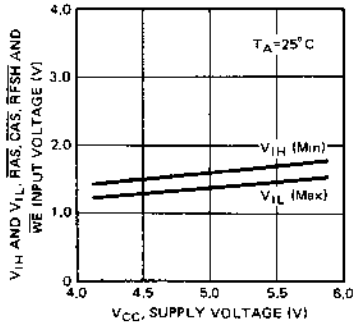
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



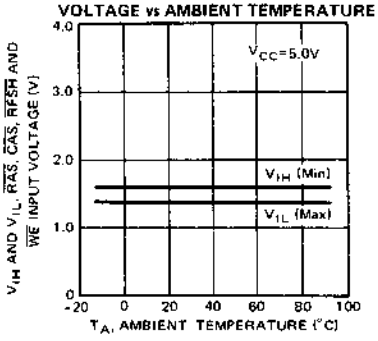
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

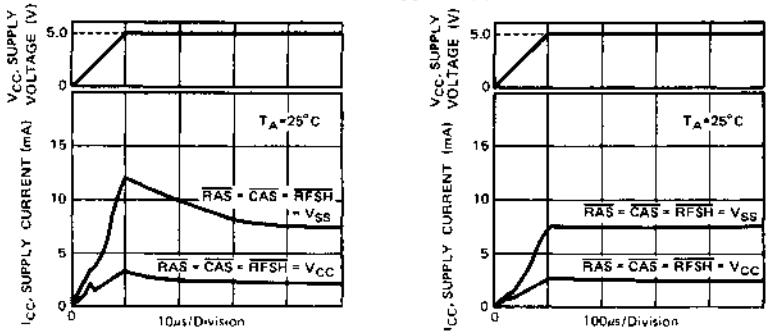


$\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

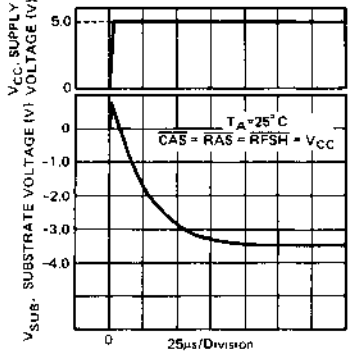


TYPICAL CHARACTERISTICS CURVES (Continued)

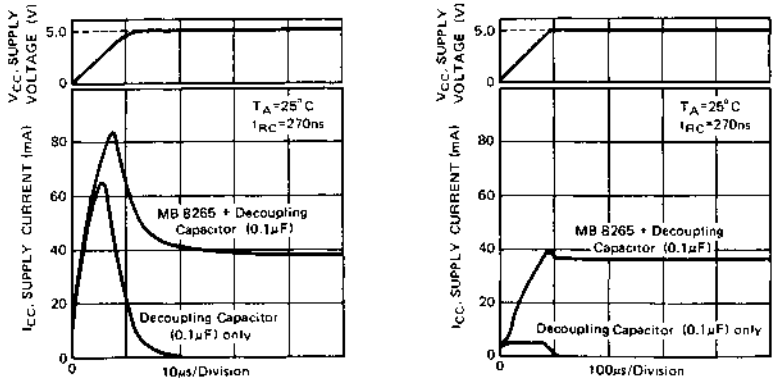
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP



SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE DURING POWER UP



SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP (ON MEMORY BOARD)



FUJITSU
MICROELECTRONICS

MB8265A-10
MB8265A-12

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

ADVANCE INFORMATION

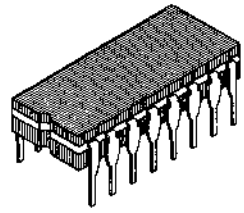
DESCRIPTON

The Fujitsu MB8265A is a fully decoded, dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8265A to be housed in a standard 16-pin DIP. Pinouts conform to the JEDEC approved pin out.

The MB8265A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is ±10%. All inputs/outputs are TTL compatible.

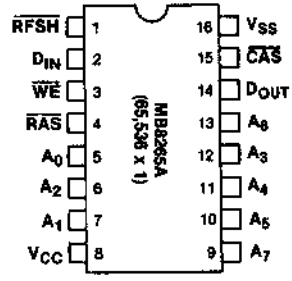


CERDIP PACKAGE
DIP-16C-C04

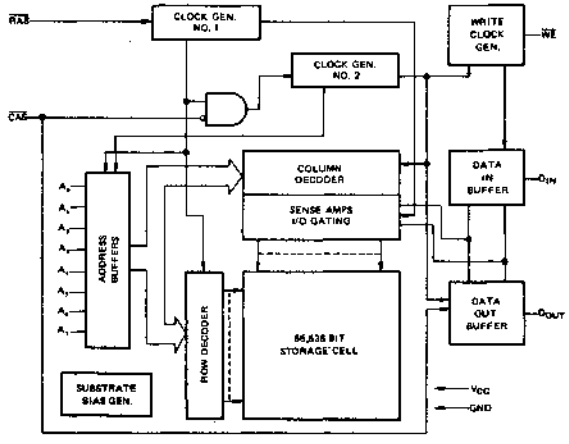
FEATURES

- **Organized as 65,536 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS single transitor cell**
- **Row Access Time:**
  - **MB8265A-10 100ns Max.**
  - **MB8265A-12 120ns Max.**
- **Cycle Time:**
  - **MB8265A-10 200 ns Min.**
  - **MB8265A-12 230 ns Min.**
- **Low Power:**
  - **MB8265A-10 330mW Max. (Active)**
  - **MB8265A-12 300mW Max. (Active)**
  - **25mW Max (Standby)**
- **±10% tolerance on a +5 volt supply**
- **On-chip substrate bias generator**
- **All inputs/outputs TTL compatible, low capacitive load**
- **Three-state output**
- **"Gated" $\overline{CAS}$**
- **Pin 1 refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh capability**
- **Page-Mode capability**
- **On-chip latches for addresses and Data-in**
- **Offers two variations of hidden refresh**

PIN ASSIGNMENT



MB8265A BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU
MICROELECTRONICS

MB8266A-10
MB8266A-12

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

ADVANCE INFORMATION

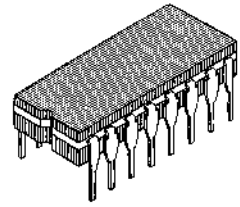
DESCRIPTION

The Fujitsu MB8266A is a fully decoded dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8266A to be housed in a standard 16-pin dual in-line package. The MB8266A offers new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before $\overline{RAS}$ refresh provides an on-chip refresh capability that is acceptable upward to 256K dynamic RAMs as pin 1 is left as a no connect. The MB8266A also features "nibble mode" which allows high speed serial access to up to 4-bits of data.

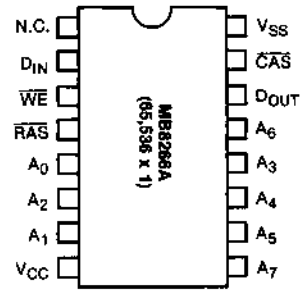
The MB8266A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.



CERDIP PACKAGE
DIP-16C-C04

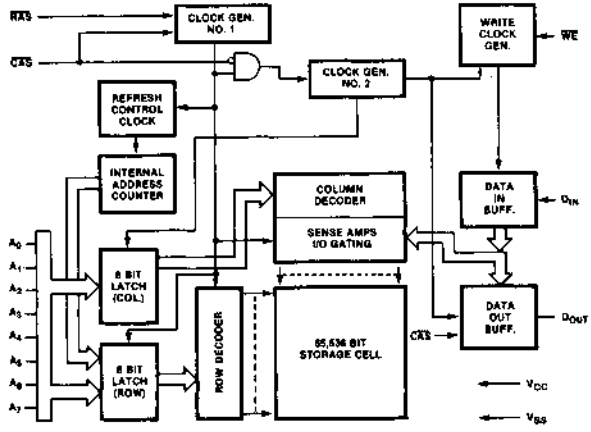
PIN ASSIGNMENT



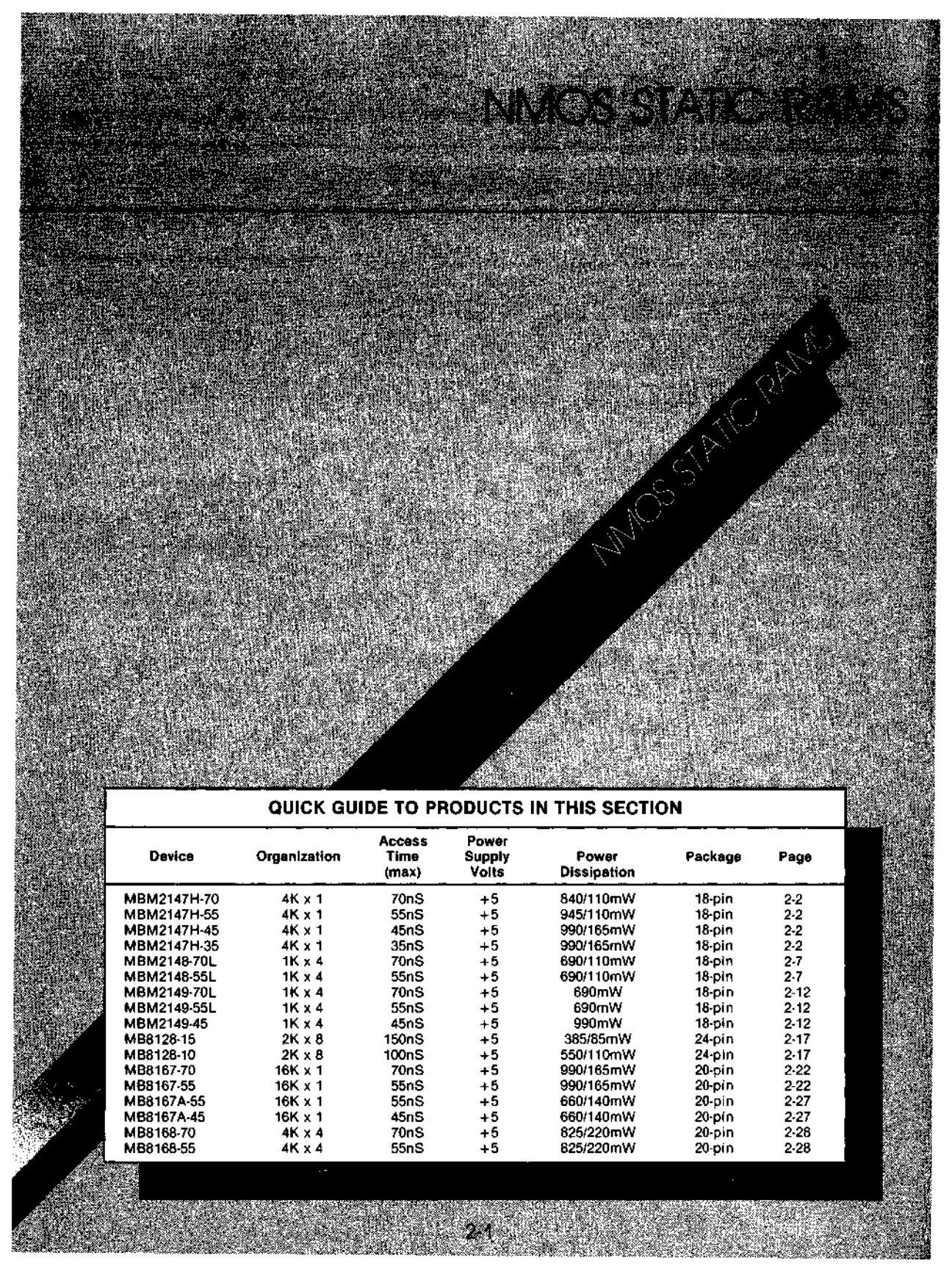
FEATURES

- **Organized as 65,536 x 1, 16-pin package, JEDEC approved pin-out**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row Access Time:**
  MB8266A-10 100ns max.
  MB8266A-12 120ns max.
- **Cycle Time:**
  MB8266A-10 200 ns min.
  MB8266A-12 230 ns min.
- **Low Power:**
  330mW max (Active)
  23mW max (Standby)
- **±10% tolerance on a +5V supply**
- **On-chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state output**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **Nibble mode capability**
- **Read-Modify-Write, $\overline{RAS}$-only refresh capability**
- **On-chip latches for addresses and D_{IN}**
- **Offers "$\overline{CAS}$-before-$\overline{RAS}$" hidden refresh**

MB8266A BLOCK DIAGRAM



NMOS STATIC RAMS



QUICK GUIDE TO PRODUCTS IN THIS SECTION

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MBM2147H-70	4K x 1	70nS	+5	840/110mW	18-pin	2-2
MBM2147H-55	4K x 1	55nS	+5	945/110mW	18-pin	2-2
MBM2147H-45	4K x 1	45nS	+5	990/165mW	18-pin	2-2
MBM2147H-35	4K x 1	35nS	+5	990/165mW	18-pin	2-2
MBM2148-70L	1K x 4	70nS	+5	690/110mW	18-pin	2-7
MBM2148-55L	1K x 4	55nS	+5	690/110mW	18-pin	2-7
MBM2149-70L	1K x 4	70nS	+5	690mW	18-pin	2-12
MBM2149-55L	1K x 4	55nS	+5	690mW	18-pin	2-12
MBM2149-45	1K x 4	45nS	+5	990mW	18-pin	2-12
MB8128-15	2K x 8	150nS	+5	385/85mW	24-pin	2-17
MB8128-10	2K x 8	100nS	+5	550/110mW	24-pin	2-17
MB8167-70	16K x 1	70nS	+5	990/165mW	20-pin	2-22
MB8167-55	16K x 1	55nS	+5	990/165mW	20-pin	2-22
MB8167A-55	16K x 1	55nS	+5	660/140mW	20-pin	2-27
MB8167A-45	16K x 1	45nS	+5	660/140mW	20-pin	2-27
MB8168-70	4K x 4	70nS	+5	825/220mW	20-pin	2-26
MB8168-55	4K x 4	55nS	+5	825/220mW	20-pin	2-28

FUJITSU
MICROELECTRONICS

MOS 4096-BIT STATIC RANDOM ACCESS MEMORY

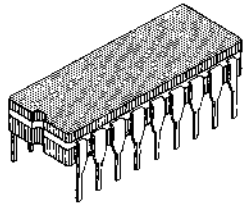
MBM2147H-70
MBM2147H-55
MBM2147H-45
MBM2147H-35

DESCRIPTION

The Fujitsu MBM2147H is a 4096 words by 1 bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatabile with TTL logic families in all respects: inputs, outputs and the use of a single +5V DC supply. For ease of use, chip select ($\overline{CS}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MBM2147H. All devices offer the advantage of low power dissipation, low cost and high performance.

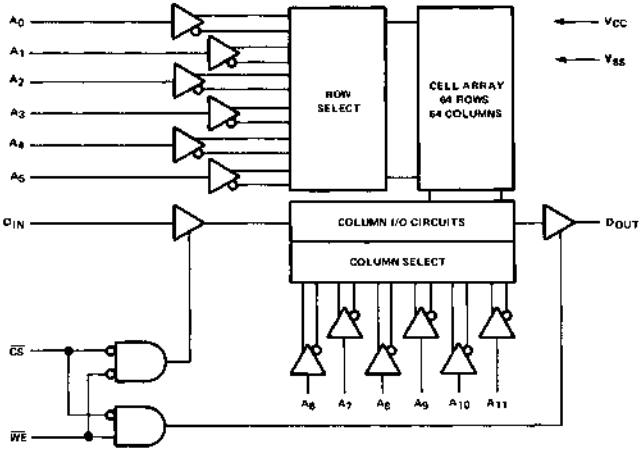
FEATURES

- **Organization: 4096 words X 1 bit**
- **Static operation, no clocks or refresh required**
- **Fast Access Time:**
  - **MBM2147H-70: 70 ns Max**
  - **MBM2147H-55: 55 ns Max**
  - **MBM2147H-45: 45 ns Max**
  - **MBM2147H-35: 35 ns Max**
- **Single +5V DC supply voltage**
- **TTL compatible input/output**
- **3-state output with OR-tie capability**
- **Chip select with automatic power down**
- **Standard 18 pin DIP package**
- **Pin compatible with Intel 2147/2147H**

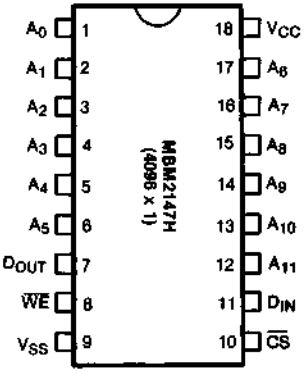


CERDIP PACKAGE
DIP-18C-C01

MBM2147H BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
DC Output Current	I_O	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

CAPACITANCE

(T_A = 25°C; f = 1MHz

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	6	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max		I_{LI}	—	10	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}, V_{CC} = Max.)		I_{LO}	—	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	H-70	I_{CC}	—	160	mA
	H-55/H-45/H-35		—	180	
Output Low Voltage (I_{OL} = 8mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)		V_{OH}	2.4	—	V
Standby Current, (V_{CC} = Max, $\overline{CS}$ = V_{IH}, I_{OUT} = 0mA)	H-70	I_{SB}	—	20	mA
	H-55/H-45/H-35		—	30	
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CS}$ = Lower of V_{CC} or V_{IN} Min.)	H-70	I_{DO}	—	50	mA
	H-55/H-45/H-35			70	
Output Short Circuit Current		I_{OS}	−200	+200	mA

AC CHARACTERISTICS

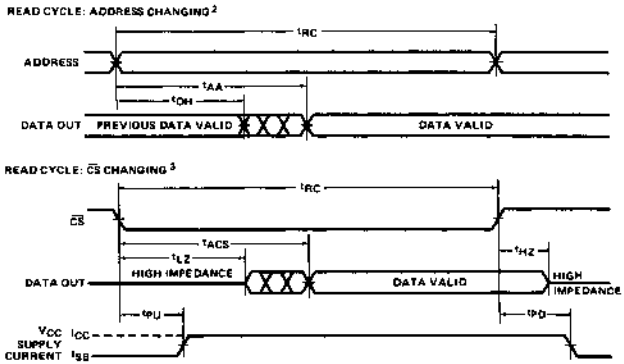
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Note	Symbol	MBM2147H-70		MBM2147H-55		MBM2147H-45		MBM2147H-35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time		t_{RC}	70	—	55	—	45	—	35	—	ns
Address Access Time		t_{AA}	—	70	—	55	—	45	—	35	ns
Chip Select Access Time	1	t_{ACS1}	—	70	—	55	—	45	—	35	ns
Chip Select Access Time	2	t_{ACS2}	—	80	—	65		45	—	35	ns
Previous Read Data Valid After Change of Address		t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Select to Power Up		t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Select to Output Active		t_{LZ}	10	—	10	—	5	—	5	—	ns
Chip Select to Output Three-Stated		t_{HZ}	0	40	0	40	0	30	0	30	ns
Chip Select to Power Down		t_{PD}	—	30	—	30	—	20	—	20	ns

Notes: 1) Chip deselected for greater than 55 ns prior to selection.
2) Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle: Address Changing.)

READ CYCLE[1]

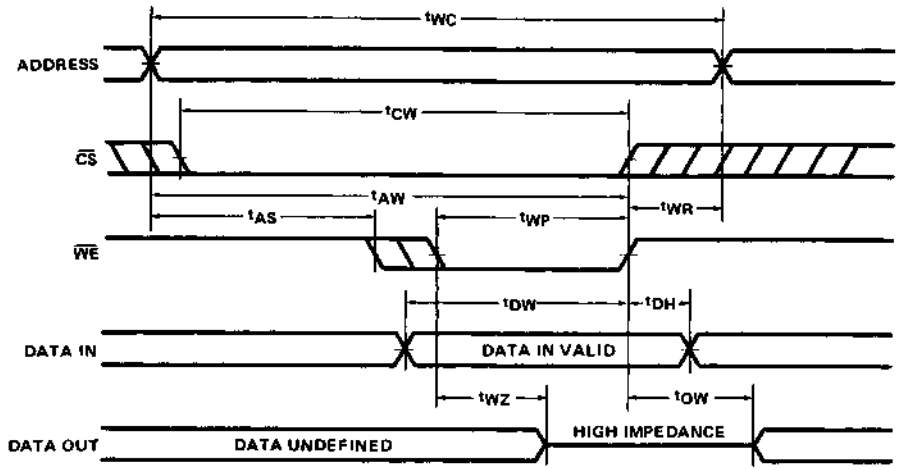


Notes: 1) $\overline{WE}$ is high for read cycle.
2) Device is continuously selected, $\overline{CS}$ = V_{IL}.
3) Addresses valid prior to or coincident with $\overline{CS}$ low transition.

WRITE CYCLE

Parameter	Symbol	MBM2147H-70		MBM2147H-55		MBM2147H-45		MBM2147H-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70	—	55	—	45	—	35	—	ns
Address Valid to End of Write	t_{AW}	55	—	45	—	45	—	35	—	ns
Chip Select to End of Write	t_{CW}	55	—	45	—	45	—	35	—	ns
Data Valid to End of Write	t_{DW}	30	—	25	—	25	—	20	—	ns
Data Hold Time	t_{DH}	10	—	10	—	10	—	10	—	ns
Write Pulse Width	t_{WP}	40	—	35	—	25	—	20	—	ns
Write Recovery Time	t_{WR}	15	—	10	—	0	—	0	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	0	—	ns
Output Active From End of Write	t_{OW}	0	—	0	—	0	—	0	—	ns
Write Enabled to Output Three-State	t_{WZ}	0	35	0	30	0	25	0	20	ns

WRITE CYCLE

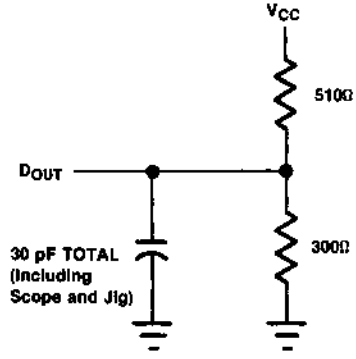


MBM2147H AC TEST CONDITIONS

MBM2147H-70/MBM2147H-55

Input Pulse Levels:	0V to 3.5V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 0.8V to 2.0V

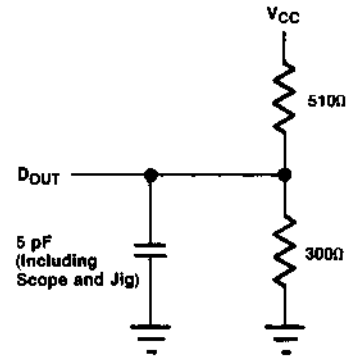
OUTPUT LOAD



MBM2147H-45

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 0.8 to 2.0V

OUTPUT LOAD
FOR t_{HZ}, t_{LZ}, t_{WZ} and t_{OW}



MBM2147H-35

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 1.5V

DESCRIPTION

The MBM2147 family from Fujitsu are high performance parts. They are designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MBM2147's chip select (active low). The MBM2147 automatically enters standby (drawing only I_{SB}) whenever the chip select is high.

Upon activation of chip select ($\overline{CS}$ = LOW) the MBM2147 automatically powers up and draws I_{CC}.

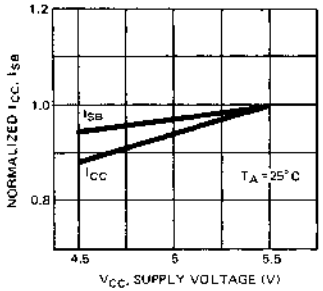
This automatic power up/down is an extremely useful feature. However, care must be used as proper decoupling and PC board layout is required to minimize power line glitches.

PC board layout with proper V_{CC} decoupling will minimize power line glitches.

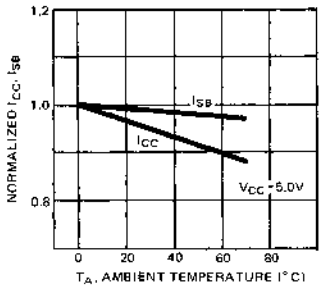
Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

TYPICAL CHARACTERISTICS CURVES

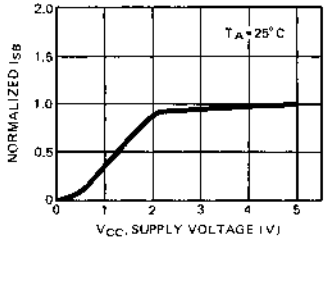
SUPPLY CURRENT vs SUPPLY VOLTAGE



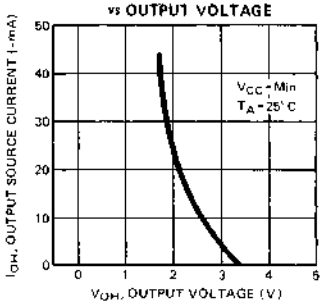
SUPPLY CURRENT vs AMBIENT TEMPERATURE



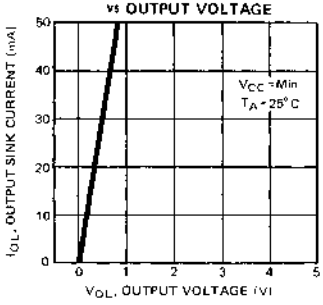
TYPICAL POWER-ON CURRENT vs SUPPLY VOLTAGE



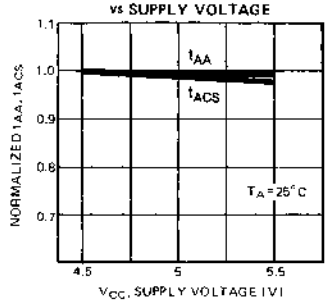
OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE



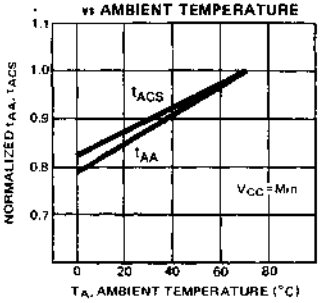
OUTPUT SINK CURRENT vs OUTPUT VOLTAGE



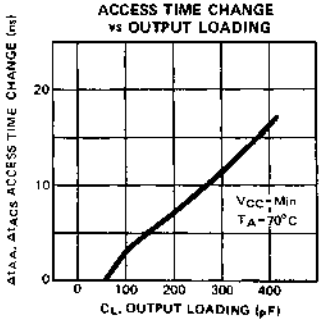
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



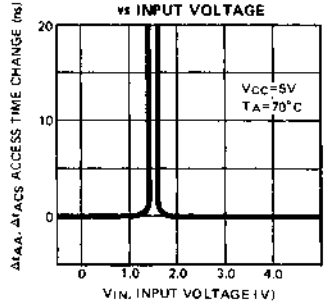
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



ACCESS TIME CHANGE vs OUTPUT LOADING



ACCESS TIME CHANGE vs INPUT VOLTAGE



FUJITSU
MICROELECTRONICS

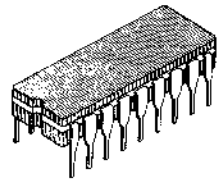
MBM2148-55L
MBM2148-70L

MOS 4096-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM2148L is a 1024 word by 4 bit static random access memory with automatic power down. It is fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}$ the other deselected packages automatically power down. Fujitsu's MBM2148L offers the advantages of low power dissipation, low cost and high performance.

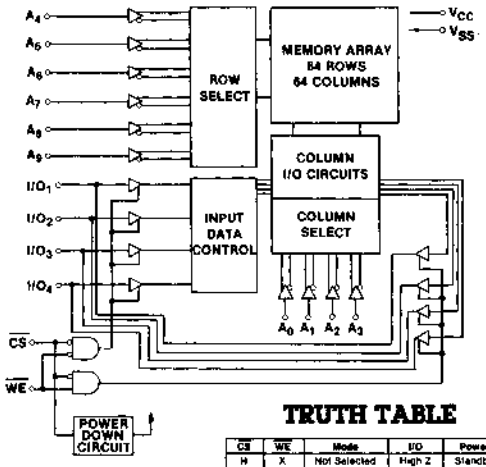


CERDIP PACKAGE
DIP-18C-C01

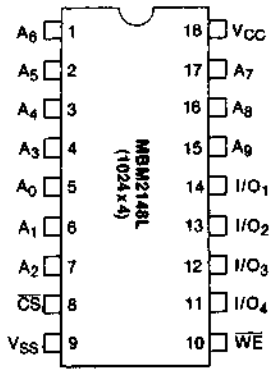
FEATURES

- **Organization: 1024 words x 4 bits**
- **Static operation; no clock or timing strobe required**
- **Fast access time:**
  MBM2148-55L: 55 ns max.
  MBM2148-70L: 70 ns max.
- **Low power consumption:**
  I_{CC} = 125mA max.
  I_{SB} = 20mA max.
- **Single +5V DC supply voltage (±10% tolerance)**
- **Common data input/output**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power down**
- **Standard 18-pin DIP package**
- **Pin compatible with Intel 2148**

MBM2148 BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not Selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Short Circuit Output Current	—	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE[1]

(T_A = 25°C; f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Address/Control Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Input/Output Capacitance (V_{OUT} = 0V)	$C_{I/O}$	—	7	pF

NOTE: 1) This parameter is sampled and not 100% tested.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.1	—	6.0	V	

NOTE: 1. The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	125	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	20	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC}, Min $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min)	I_{PO}	—	30	mA
Output Short Circuit Current (V_{OUT} = V_{SS} to V_{CC})	I_{OS}	−200	200	mA

AC CHARACTERISTICS

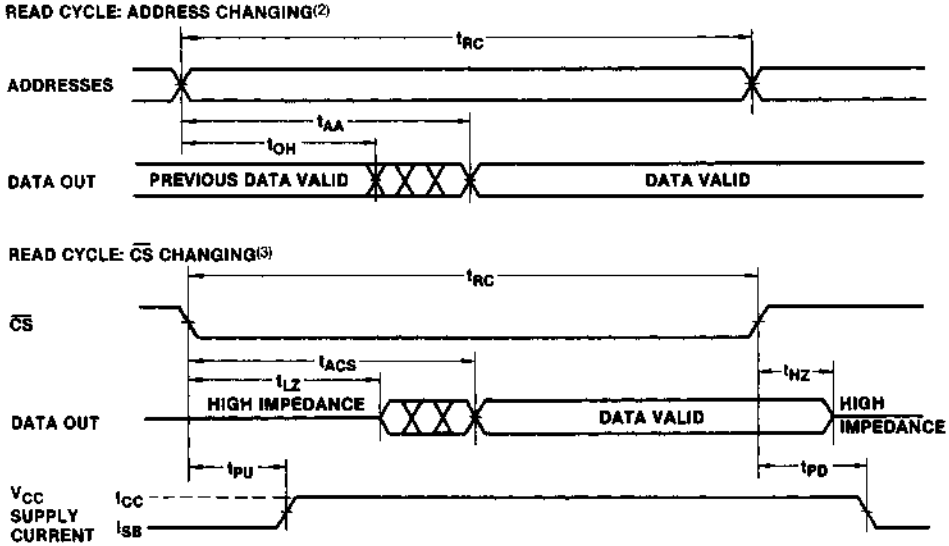
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	NOTES	Symbol	MBM2148-55L			MBM2148-70L			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		t_{RC}	55	—	—	70	—	—	ns
Address Access Time		t_{AA}	—	—	55	—	—	70	ns
Chip Select Access Time	1	t_{ACS1}	—	—	55	—	—	70	ns
Chip Select Access Time	2	t_{ACS2}	—	—	65	—	—	80	ns
Previous Read Data Valid After Change of Address		t_{OH}	5	—	—	5	—	—	ns
Chip Select to Power Up		t_{PU}	0	—	—	0	—	—	ns
Chip Select to Output Active	3	t_{LZ}	20	—	—	20	—	—	ns
Chip Select to Output Three-State	3	t_{HZ}	0	—	20	0	—	20	ns
Chip Select to Power Down		t_{PD}	—	—	30	—	—	30	ns

NOTE: 1. Chip deselected for greater than 55 ns prior to selection
2. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle: Address Changing.)
3. Transition is measured ±500 mV from high impedance voltage with LOAD B. This parameter is sampled and not 100% tested.

READ CYCLE (1)



NOTE: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincindent with $\overline{CS}$ low transition.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

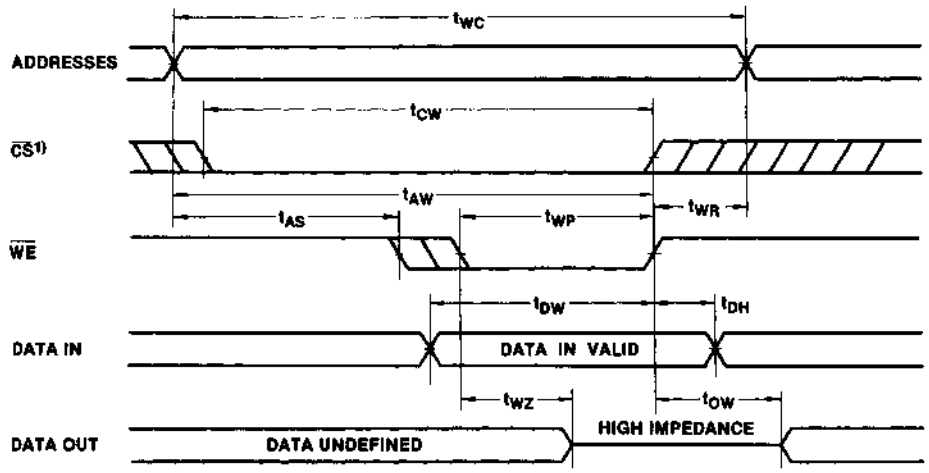
WRITE CYCLE

Parameter	NOTES	Symbol	MBM2148-55L			MBM2148-70L			Unit
			Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t_{WC}	55	—	—	70	—	—	ns
Address Valid to End of Write		t_{AW}	50	—	—	65	—	—	ns
Chip Select to End of Write		t_{CW}	50	—	—	65	—	—	ns
Data Valid to End of Write		t_{DW}	20	—	—	25	—	—	ns
Data Hold Time		t_{DH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WP}	40	—	—	50	—	—	ns
Write Recovery Time		t_{WR}	5	—	—	5	—	—	ns
Address Setup Time		t_{AS}	0	—	—	0	—	—	ns
Output Active From End of Write	1	t_{OW}	0	—	—	0	—	—	ns
Write Enabled to Output Three-State	1	t_{WZ}	0	—	20	0	—	25	ns

NOTE: 1. Transition is measured ±500 mV from high impedance voltage with LOAD B. This parameter is sampled and not 100% tested.

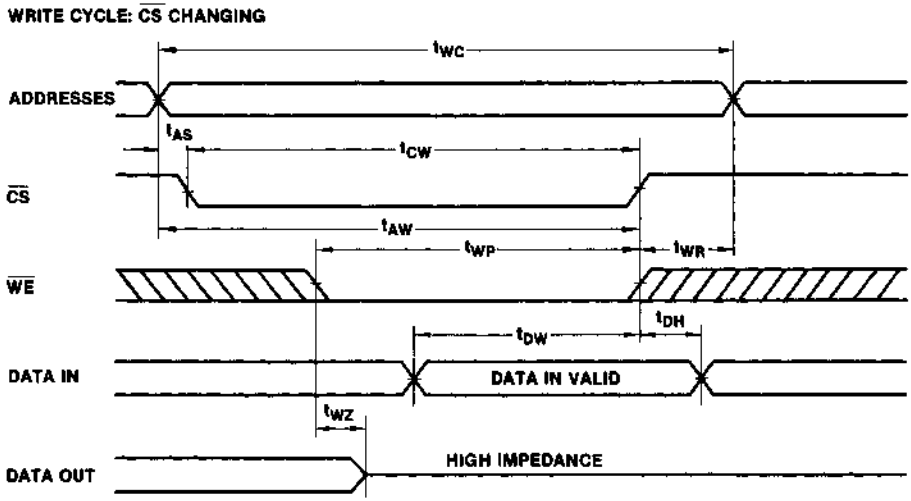
WRITE CYCLE

WRITE CYCLE: $\overline{WE}$ CHANGING



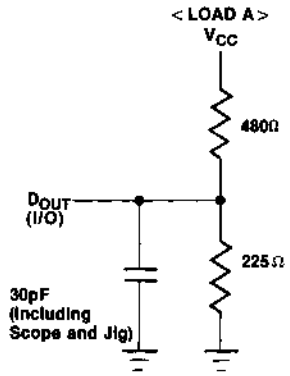
NOTE: 1. If $\overline{CS}$ goes high simulataneously with $\overline{WE}$ high, the output remains in a high impedance state.

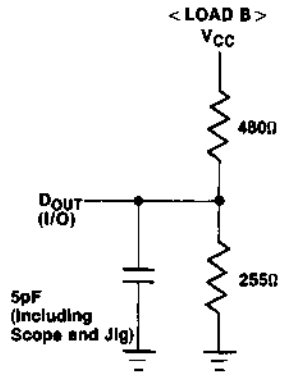
WRITE CYCLE



AC TEST CONDITIONS

Input Pulse Level:	0V to 3.0V
Input Pulse Rise and Fall Times:	5ns
Timing Measurement Reference Levels:	Inputs: 1.5V
	Outputs: 1.5V





OVERVIEW

The MBM2148 family from Fujitsu are high performance parts. They are designed for high speed and low power system requirements.

The high speed is obtained by advanced NMOS processing. The low power system requirements are achieved by the use of the MBM2148's chip select (active low). The MBM2148 automatically enters stand-by (drawing only I_{SB}) whenever the chip select is high. Upon activation of chip select ($\overline{CS}$ = LOW) the MBM2148 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address line. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

FUJITSU
MICROELECTRONICS

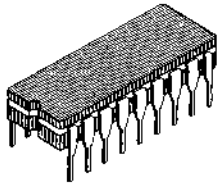
MBM2149-45
MBM2149-55L
MBM2149-70L

MOS 4096-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM2149 is a 1024 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied. Fujitsu's MBM2149 offers the advantages of low power dissipation, low cost and high performance.

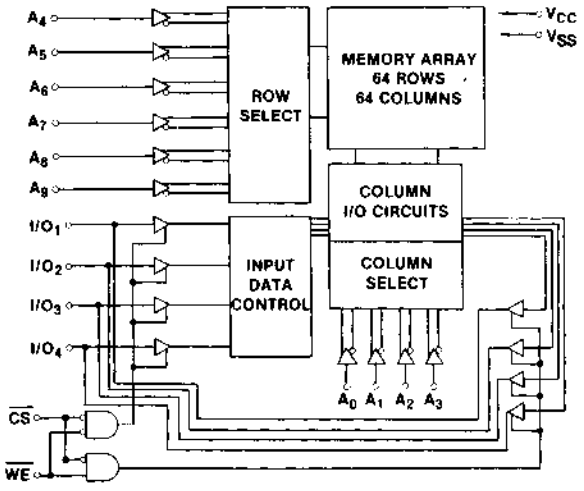


CERDIP PACKAGE
DIP-18C-C01

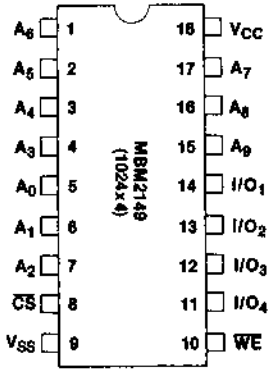
FEATURES

- **Organization: 1024 words x 4 bits**
- **Static operation; no clocks or timing strobe required**
- **Address Access Time:**
  MBM2149-45: 45 ns max.
  MBM2149-55L: 55 ns max.
  MBM2149-70L: 70 ns max.
- **Chip Select Access Time:**
  MBM2149-45: 20 ns max.
  MBM2149-55L: 25 ns max.
  MBM2149-70L: 30 ns max.
- **Low Power Consumption:**
  MBM2149-45: 160mA
  MBM2149-55L/-70L: 125mA
- **Single +5V DC supply voltage (±10% tolerance)**
- **Common data input/output**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Chip select for simplified memory expansion**
- **Standard 18-pin DIP package**
- **Pin compatible with Intel 2149**

MBM2149 BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O
H	X	Not Selected	High Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Short Circuit Output Current	—	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE(1)

(T_A = 25°C; f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Address/Control Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Input/Output Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	7	pF

NOTE: 1. This parameter is sampled and not 100% tested.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient(1) Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.1	—	6.0	V	

NOTE: 1. The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)		I_{LI}	−10	10	μA
Input/Output Leakage Current ($\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to 4.5V, V_{CC} = Max)		I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	MBM2149-45	I_{CC}	—	180	mA
	MBM2149-55L / -70L	I_{CC}	—	125	mA
Output Low Voltage (I_{OL} = 8mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)		V_{OH}	2.4	—	V
Output Short Circuit Current (V_{OUT} = V_{SS} to V_{CC})		I_{OS}	—	±200	mA

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

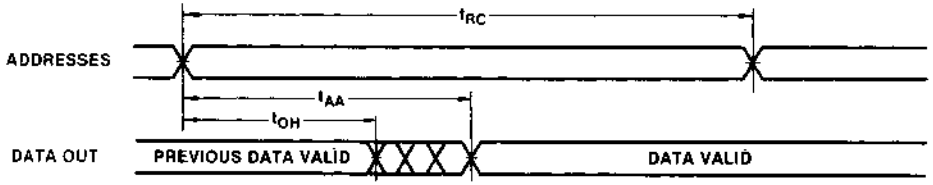
READ CYCLE

Parameter	NOTES	Symbol	MBM2149-45		MBM2149-55L		MBM2149-70L		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time		t_{RC}	45	—	55	—	70	—	ns
Address Access Time		t_{AA}	—	45	—	55	—	70	ns
Chip Select Access Time		t_{ACS}	—	20	—	25	—	30	ns
Previous Read Data Valid After Change of Address		t_{OH}	5	—	5	—	5	—	ns
Chip Select to Output Active	1	t_{LZ}	5	—	5	—	5	—	ns
Chip Select to Output Three-State	1	t_{HZ}	0	15	0	15	0	15	ns

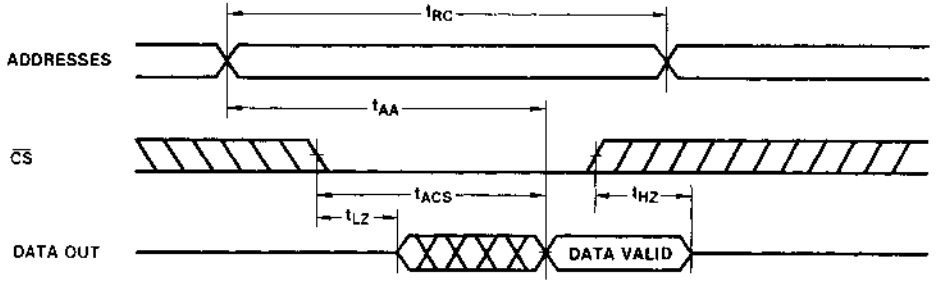
NOTE: 1. Transition is measured ±500 mV from high impedance voltage with LOAD B. This parameter is sampled and not 100% tested.

READ CYCLE (1)

READ CYCLE: ADDRESS CHANGING(2)



READ CYCLE: $\overline{CS}$ CHANGING



Note: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.

AC CHARACTERISTICS

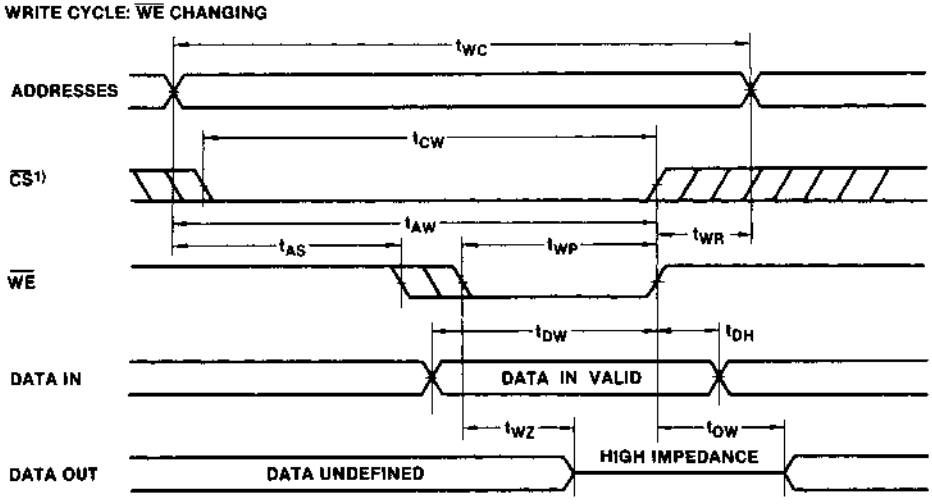
(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE

Parameter	NOTES	Symbol	MBM2149-45		MBM2149-55L		MBM2149-70L		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time		t_{WC}	45	—	55	—	70	—	ns
Address Valid to End of Write		t_{AW}	40	—	50	—	65	—	ns
Chip Select to End of Write		t_{CW}	40	—	50	—	65	—	ns
Data Valid to End of Write		t_{DW}	20	—	20	—	25	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	35	—	40	—	50	—	ns
Write Recovery Time		t_{WR}	5	—	5	—	5	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Output Active From End of Write	1	t_{OW}	0	—	0	—	0	—	ns
Write Enabled to Output Three-State	1	t_{WZ}	0	15	0	20	0	25	ns

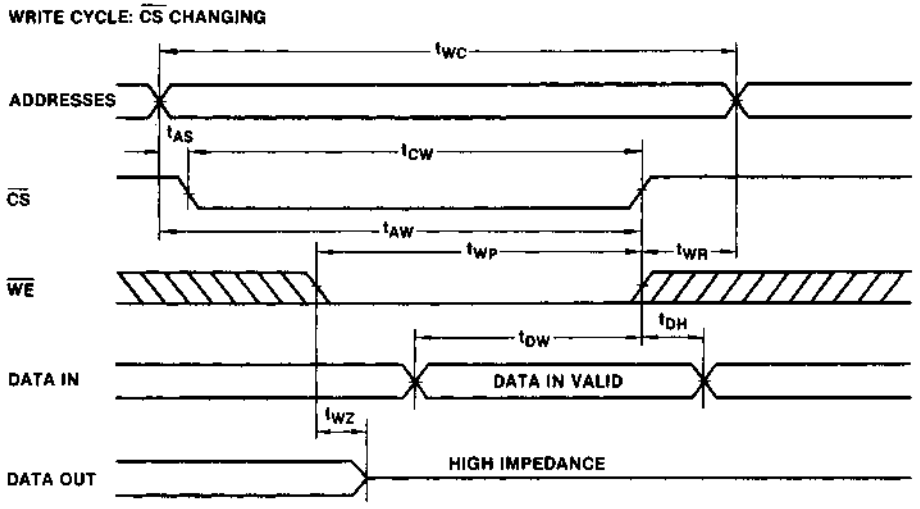
NOTE: 1. Transition is measured ±500 mV from high impedance voltage with LOAD B. This parameter is sampled and not 100% tested.

WRITE CYCLE



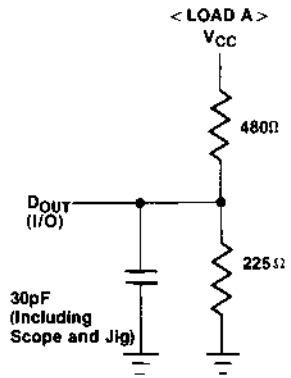
NOTE: 1. If $\overline{CS}$ goes high simulataneously with $\overline{WE}$ high, the output remains in a high impedance state.

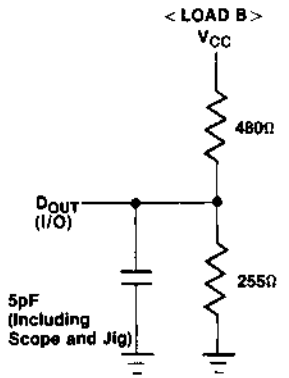
WRITE CYCLE



AC TEST CONDITIONS

Input Pulse Level:	0V to 3.0V	
Input Pulse Rise and Fall Times:	5ns	
Timing Measurement Reference Levels:	Inputs:	1.5V
	Outputs:	1.5V





OVERVIEW

The MBM2149 family from Fujitsu are high performance parts. They are designed for high speed and low power system requirements. The high speed is obtained by advanced NMOS processing.

Input and data bus lines are an area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address line. Careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

MB8128-10
MB8128-15

NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

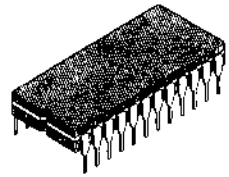
DESCRIPTION

The MB8128 is fabricated using N-channel silicon gate MOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

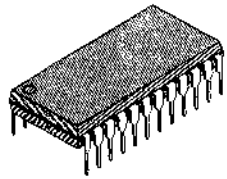
MB8128 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. The MB8128 is compatible with TTL logic families in all respects; inputs, outputs and a single +5V supply.

FEATURES

- 2048 words x 8-bit organization
- Static operation: no clocks or refresh required
- Fast access time:
  MB8128-10 100 ns Max.
  MB8128-15 150 ns Max.
- Single +5V supply voltage
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Three-state output with OR-tie capability
- Chip Enable for simplified memory expansion
- Automatic power down
- Industry standard 24-pin DIP package
- Pin compatible with MB8416 (CMOS Static RAM) and MBM2716 (EPROM)

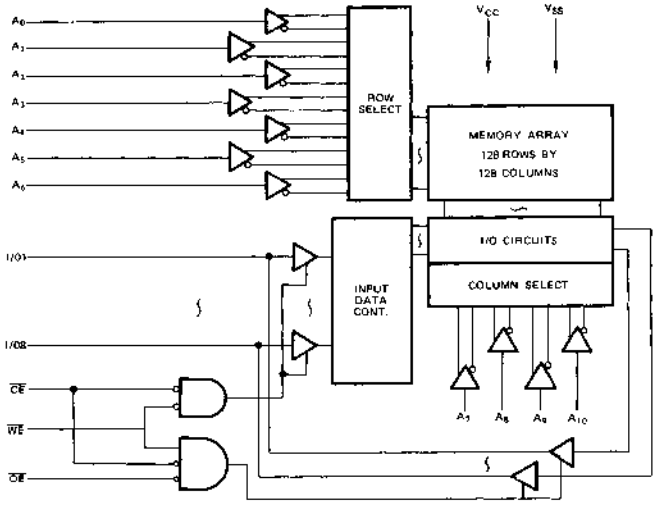


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

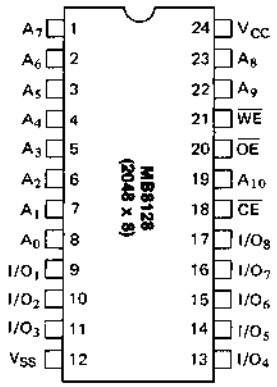
MB8128 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH Z
L	H	H	D_{OUT} DISABLE	I_{CC}	HIGH Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on Any Pin With Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient (1) Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.2	—	6.0	V	

NOTE: 1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter			Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)			I_{LI}	−10	—	10	μA
Input/Output Leakage Current ($\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}, V_{CC} = Max)			I_{LO}	−10	—	10	μA
Power Supply Current (V_{CC} = Max, $\overline{CE}$ = V_{IL}, Data I/O = Open)	T_A = 25 °C	MB8128-10	I_{CC}	—	70	—	mA
		MB8128-15		—	50	—	
	T_A = 0 °C	MB8128-10		—	—	100	
		MB8128-15		—	—	70	
Output Low Voltage (I_{OL} = 2.1 mA)			V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1 mA)			V_{OH}	2.4	—	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CE}$ = V_{IH})		MB8128-10	I_{SB}	—	8	20	mA
		MB8128-15		—	6	15	
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min)		MB8128-10	I_{PO}	—	—	20	mA
		MB8128-15		—	—	15	

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

READ CYCLE

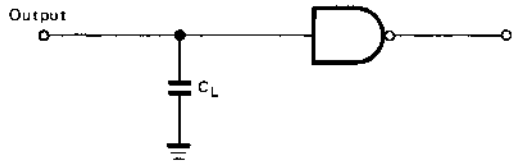
Parameter	Symbol	MB8128-10			MB8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle Time	t_{RC}	100	—	—	150	—	—	ns
Address Access Time	t_{AA}	—	—	100	—	—	150	ns
Chip Enable Access Time	t_{ACE}	—	—	100	—	—	150	ns
Output Hold from Address Change	t_{OH}	15	—	—	20	—	—	ns
Chip Enable to Output Active	t_{LZ}	0	—	—	0	—	—	ns
Chip Enable to Output in High Z	t_{HZ}	—	—	40	—	—	60	ns
Output Enable to Output Valid	t_{OE}	—	—	50	—	—	60	ns
Output Enable to Output Active	t_{OLZ}	10	—	—	10	—	—	ns
Output Enable to Output in High Z	t_{OHZ}	—	—	40	—	—	60	ns
Chip Enable to Power Up Time	t_{PU}	0	—	—	0	—	—	ns
Chip Enable to Power Down Time	t_{PD}	—	—	40	—	—	60	ns

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Input/Output Capacitance (V_{OUT} = 0V)	$C_{I/O}$	—	7	pF

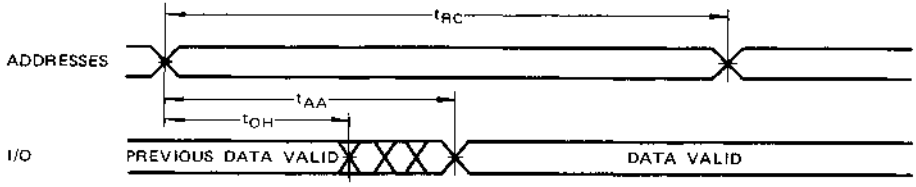
AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.4V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 1.5V
Output Load :	1 TTL Gate and C_L = 100 pF

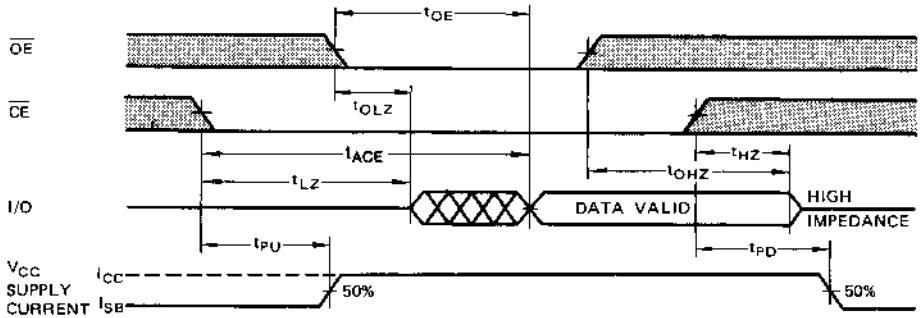


READ CYCLE [1]

READ CYCLE: ADDRESS CONTROLLED[2]



READ CYCLE: $\overline{CE}$/$\overline{OE}$ CONTROLLED[3]



: Don't Care

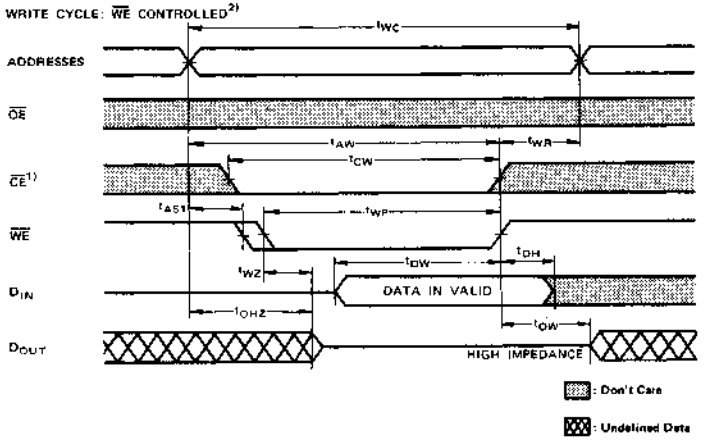
: Undefined Data

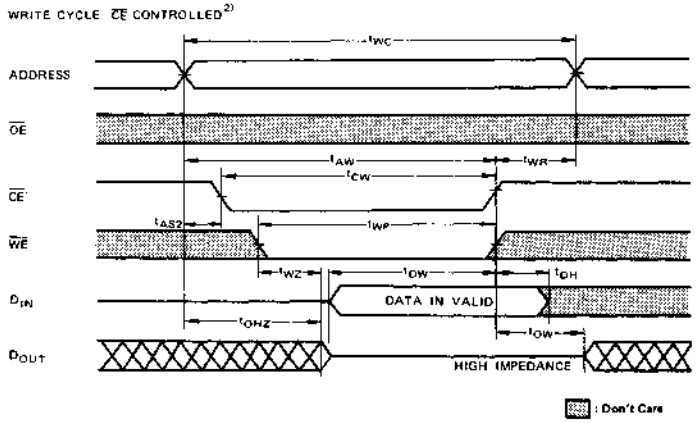
Note: 1) $\overline{WE}$ is high for Read Cycle.
2) Device is continuously selected, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}.
3) Addresses valid prior to or coincident with $\overline{CE}$ transition low.

WRITE CYCLE

Parameter	Symbol	MB8128-10			MB8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	t_{WC}	100	—	—	150	—	—	ns
Address Valid to End of Write	t_{AW}	95	—	—	140	—	—	ns
Chip Select to End of Write	t_{CW}	95	—	—	140	—	—	ns
Data Valid to End of Write	t_{DW}	40	—	—	60	—	—	ns
Data Hold Time	t_{DH}	5	—	—	5	—	—	ns
Write Pulse Width	t_{WP}	85	—	—	130	—	—	ns
Write Recovery Time	t_{WR}	5	—	—	10	—	—	ns
Address Setup Time	t_{AS1}	0	—	—	0	—	—	ns
	t_{AS2}	0	—	—	0	—	—	ns
Output Active From End of Write	t_{OW}	10	—	—	10	—	—	ns
Write Enable to Output in High Z	t_{WZ}	—	—	40	—	—	60	ns

WRITE CYCLE





Note: 1) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ low, the outputs remain in a high impedance state.
2) $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

OVERVIEW

The MB8128 from Fujitsu is a high performance part, designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MB8128 chip enable (active low). The MB8128 automatically enters standby operation drawing only I_{SB} whenever the chip enable is high. Upon activation of chip enable ($\overline{CE}$ = LOW) the MB8128 automatically powers up. This automatic power up/down is an extremely useful feature. Care must be used as proper decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

FUJITSU
MICROELECTRONICS

MB8167-55
MB8167-70

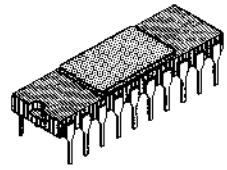
NMOS 16,384 BIT STATIC RANDOM ACCESS MEMORY

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MB8167A-55/MB8167A-45.

DESCRIPTION

The Fujitsu MB8167 is a 16384 words by 1 bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output and the use of a single +5V DC supply.

For ease of use, chip enable ($\overline{CE}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB8167. This device offers the advantages of low power dissipation, low cost, and high performance.

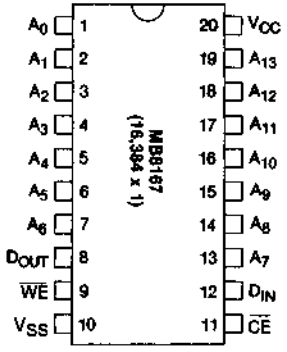


CERAMIC PACKAGE (METAL SEAL) DIP-20C-A01

FEATURES

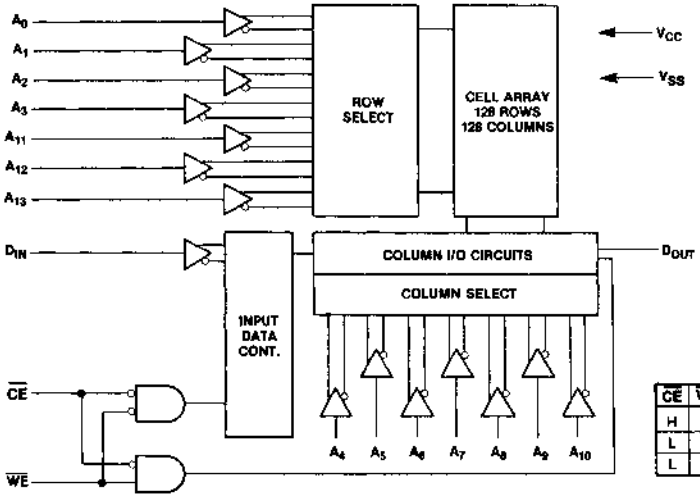
- **Organized as 16384 words X 1 Bit**
- **Static operation: no clocks or refresh required**
- **Fast Access Time:**
  MB8167-55 55 ns Max.
  MB8167-70 70 ns Max.
- **Single +5V DC supply voltage**
- **Separate data input and output**
- **TTL compatible inputs and output**
- **Three-state output with OR-tie capability**
- **Chip enable for simplified memory expansion and automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2167**

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8167 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

NOTE: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	6	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)		I_{LI}	−10	10	μA
Output Leakage Current ($\overline{CE}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC} Min, V_{CC} = Max)		I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA)	T_A = 25°C	I_{CC}	—	170	mA
	T_A = 0°C		—	180	
Output Low Voltage (I_{OL} = 8mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)		V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}		I_{SB}	—	30	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min)		I_{PO}	—	30	mA

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MB8167A-55/MB8167A-45.

AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.2V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Inputs: 1.5V
	Output: 1.5V

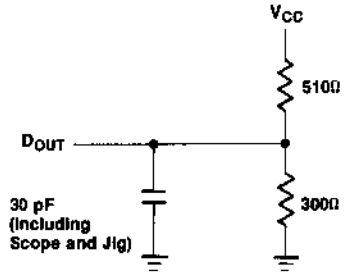


Fig. 1: OUTPUT LOAD

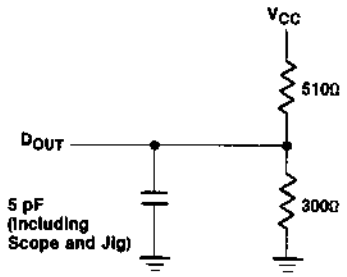


Fig. 2: OUTPUT LOAD for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

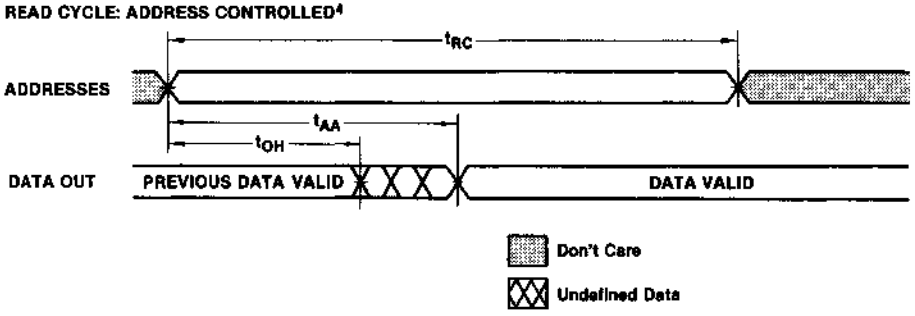
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

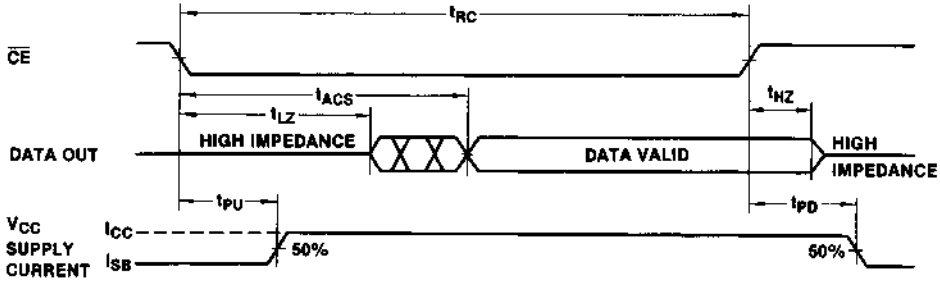
Parameter	NOTES	Symbol	MB8167-55			MB8167-70			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		t_{RC}	55	—	—	70	—	—	ns
Address Access Time		t_{AA}	—	—	55	—	—	70	ns
Chip Enable Access Time		t_{ACS}	—	—	55	—	—	70	ns
Output Hold from Address Change		t_{OH}	5	—	—	5	—	—	ns
Chip Enable to Output Active	1 2	t_{LZ}	10	—	—	10	—	—	ns
Chip Enable to Output in High Z	1 2	t_{HZ}	0	—	30	0	—	40	ns
Chip Enable to Power Up Time		t_{PU}	0	—	—	0	—	—	ns
Chip Enable to Power Down Time		t_{PD}	—	—	30	—	—	35	ns

READ CYCLE[3]



READ CYCLE[3] (Cont'd)

READ CYCLE: $\overline{CE}$ CONTROLLED[5]



Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig.2.
3. $\overline{WE}$ is high for Read Cycle.
4. Device is continuously selected, $\overline{CE}$ = V_{IL}.
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low.

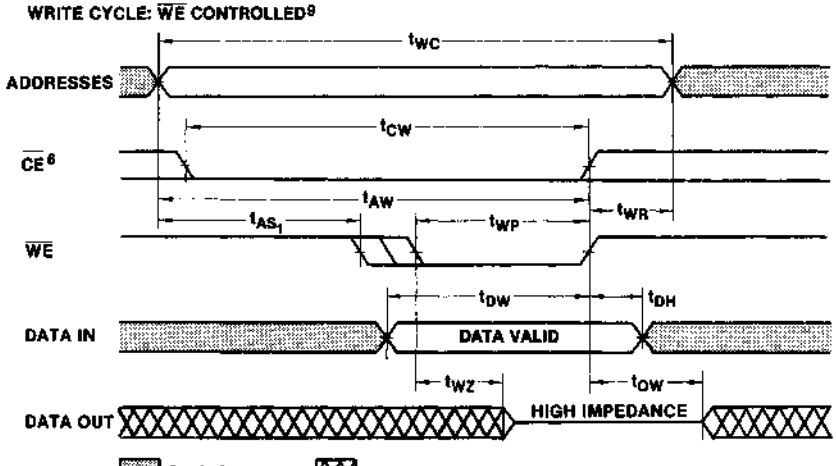
Undefined Data

WRITE CYCLE

Parameter	NOTES	Symbol	MB8167-55 Min	MB8167-55 Typ	MB8167-55 Max	MB8167-70 Min	MB8167-70 Typ	MB8167-70 Max	Unit
Write Cycle		t_{WC}	55	—	—	70	—	—	ns
Address Valid to End of Write		t_{AW}	45	—	—	50	—	—	ns
Chip Enable to End of Write		t_{CW}	50	—	—	60	—	—	ns
Data Valid to End of Write		t_{DW}	35	—	—	45	—	—	ns
Data Hold Time		t_{DH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WP}	35	—	—	45	—	—	ns
Write Recovery Time		t_{WR}	5	—	—	10	—	—	ns
Address Setup Time		t_{AS1}	5	—	—	10	—	—	ns
		t_{AS2}	0	—	—	0	—	—	
Output Active From End of Write	7 8	t_{OW}	0	—	—	0	—	—	ns
Write Enable to Output in High Z	7 8	t_{WZ}	0	—	30	0	—	35	ns

WRITE CYCLE

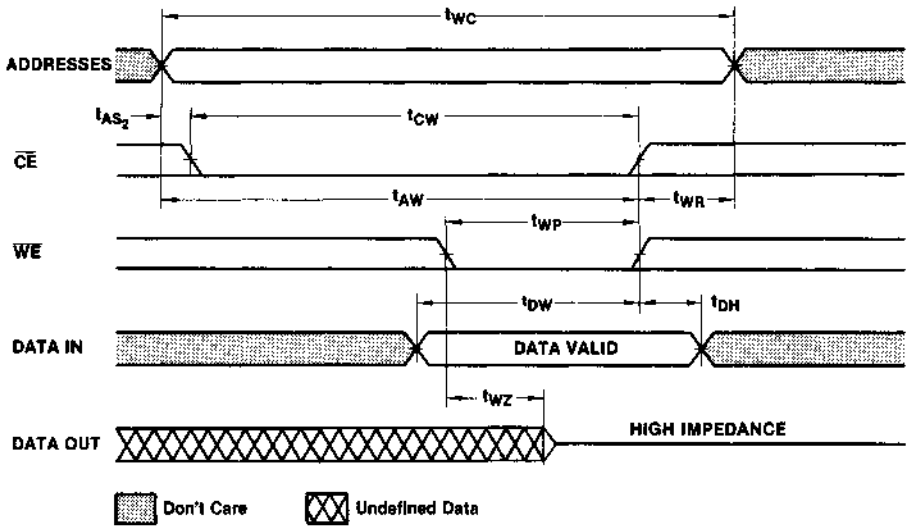
WRITE CYCLE: $\overline{WE}$ CONTROLLED[9]



Don't Care Undefined Data

WRITE CYCLE (Cont'd)

WRITE CYCLE: $\overline{CE}$ CONTROLLED[9]



Notes: 6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

DESCRIPTION

The MB8167 from Fujitsu is a high performance part. It is designed for high speed and low power system requirements.

The high speed is obtained by advanced NMOS processing. The power requirements are achieved by the use of MB8167 chip enable (active low). The MB8167 automatically enters standby drawing only I_{SB} whenever the chip enable is high. Upon activation of chip enable ($\overline{CE}$ = LOW) the MB8167 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

FUJITSU
MICROELECTRONICS

Sec- 8/67

MB8167A-45
MB8167A-55

NMOS 16,384 BIT STATIC RANDOM ACCESS MEMORY

ADVANCE INFORMATION

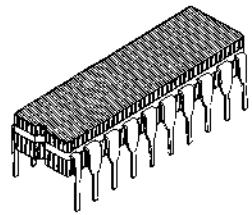
DESCRIPTION

The Fujitsu MB8167A is a 16,384 words by 1-bit static random access memory fabrication using N-channel silicon gate MOS technology. Separate Input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output and the use of a single +5V DC supply.

For ease of use, chip enable ($\overline{CE}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB8167A. This device offers the advantages of low power dissipation, low cost, and high performance.

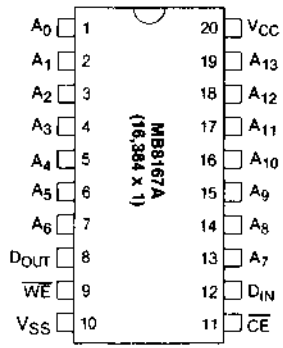
FEATURES

- **Organized as 16,384 words x 1 Bit**
- **Static operation: no clocks or refresh required**
- **Fast Access Time:**
  MB8167A-45: 45ns Max.
  MB8167A-55: 55ns Max.
- **Separate data input and output**
- **TTL compatible inputs and output**
- **Single +5V DC supply voltage**
- **Three-state output with OR-tie capability**
- **Chip enable for simplified memory expansion and automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2167**

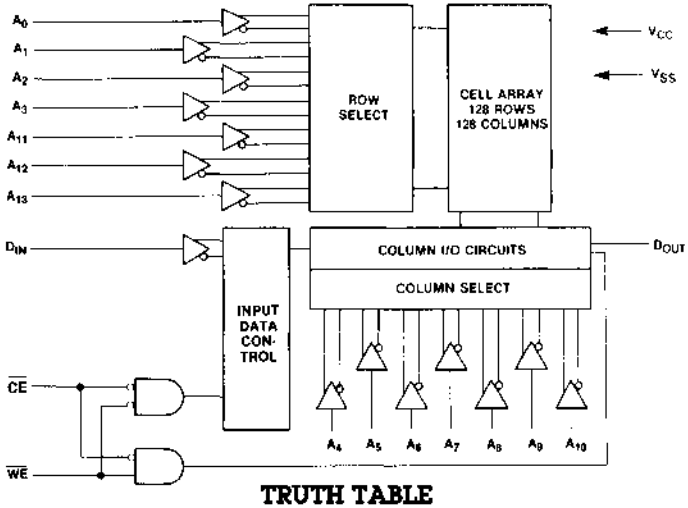


CERDIP PACKAGE
DIP-20C-C03

PIN ASSIGNMENT



MB8167A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU
MICROELECTRONICS

MB8168-55
MB8168-70

NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

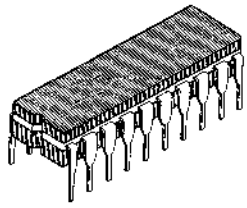
ADVANCE INFORMATION

DESCRIPTION

The Fujitsu MB8168 is a 4096 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{CS}$, the other deselected packages automatically power down.

All Fujitsu devices offer the advantages of low power dissipation, low cost and high performance.

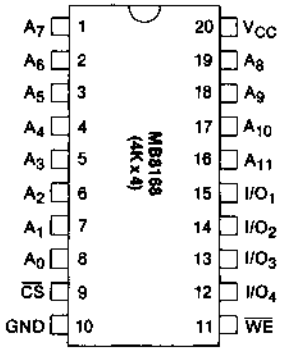


CERDIP PACKAGE
DIP-20C-C03

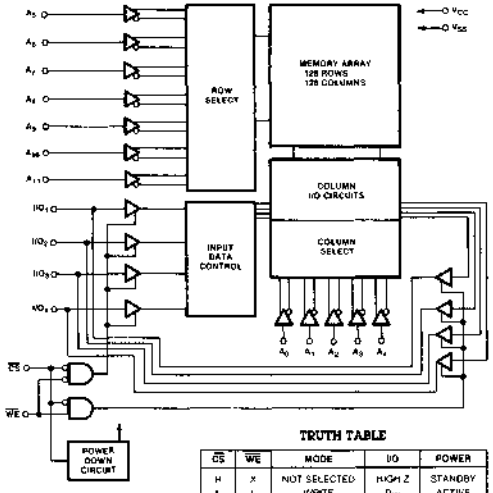
FEATURES

- **Organized as 4096 x 4**
- **Fully Static Operation, no clocks or timing strobe required**
- **Fast Access Time:**
  MB8168-55 55 ns Max.
  MB8168-70 70 ns Max.
- **Low Power Consumption:**
  I_{CC} = 150mA Max. (Active)
  I_{SB} = 40mA Max. (Standby)
- **Single +5V DC Supply Voltage, ±10% tolerance**
- **Common data input and output**
- **Three-state output with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power-down**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2168**

PIN ASSIGNMENT



MB8168 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Short Circuit Output Current	—	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient 1) Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

NOTE: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

CAPACITANCE (T_A = 25°C, f = 1 MHz, this parameter is sampled, not 100% tested.)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address, $\overline{WE}$: V_{IN} = 0V	C_{IN}	—	7	pF
Input Capacitance	$\overline{CS}$: V_{IN} = 0V	$C_{\overline{CS}}$	—	8	pF
Output Capacitance	Data I/O, V_{OUT} = 0V	C_{OUT}	—	8	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	150	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	40	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min)	I_{PO}	—	50	mA
Output Short Circuit Current (V_{OUT} = V_{SS} to V_{CC})	I_{OS}	−200	200	mA

AC TEST CONDITIONS

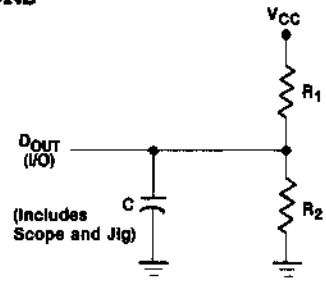
Input Conditions:

Input Pulse Levels:	**0V to 3.0V**
Input Pulse Rise/Fall Times:	**5 ns**
Input Timing Reference Level:	**1.5V**

Output Conditions:

Output Timing Reference Level:	**0.8V to 2.0V**
Output Load:	

	R_1	R_2	C	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ} and t_{OW}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}



OUTPUT LOAD

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

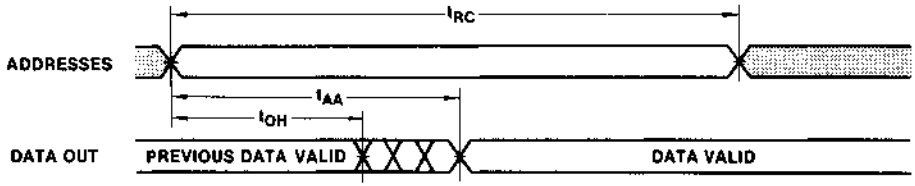
READ CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Read Cycle Time		t_{RC}	55	—	—	70	—	—	ns
Address Access Time		t_{AA}	—	—	55	—	—	70	ns
Chip Select Access Time		t_{ACS}	—	—	55	—	—	70	ns
Output Hold from Address Change		t_{OH}	5	—	—	5	—	—	ns
Chip Select to Output Active	1 2	t_{LZ}	10	—	—	10	—	—	ns
Chip Select to Output in High Z	1 2	t_{HZ}	0	—	30	0	—	40	ns
Chip Select to Power Up Time		t_{PU}	0	—	—	0	—	—	ns
Chip Select to Power Down Time		t_{PD}	—	—	55	—	—	70	ns

Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig. 2. This parameter is sampled and not 100% tested.

READ CYCLE 3

READ CYCLE: ADDRESS CHANGING 4



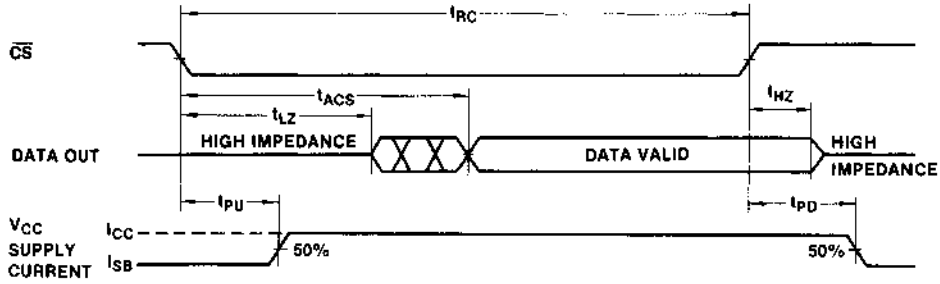
Notes: 3. $\overline{WE}$ is high for Read Cycle.
4. Device is continuously selected. $\overline{CS} = V_{IL}$.

Don't Care

Undefined Data

READ CYCLE [3] (Cont'd)

READ CYCLE: $\overline{CS}$ CHANGING[5]



Notes: 3. $\overline{WE}$ is high for Read Cycle.
4. Device is continuously selected. $\overline{CS} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

Undefined Data

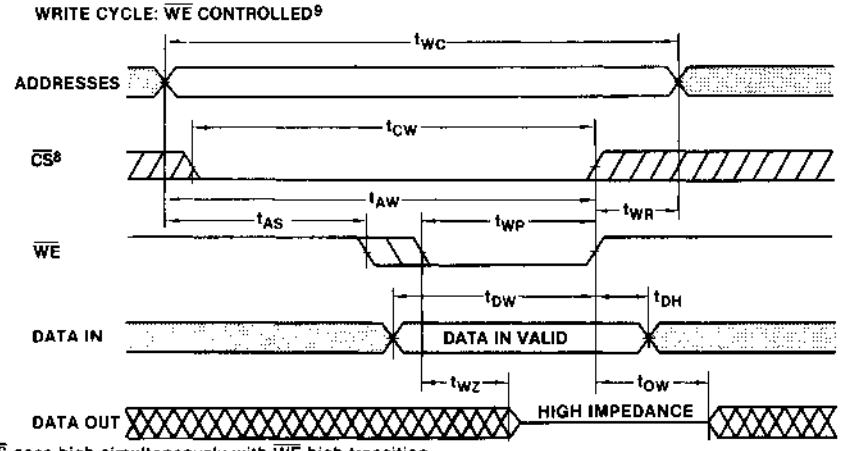
WRITE CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Write Cycle Time		t_{WC}	55	—	—	70	—	—	ns
Address Valid to End of Write		t_{AW}	55	—	—	70	—	—	ns
Chip Select to End of Write		t_{CW}	55	—	—	70	—	—	ns
Data Valid to End of Write		t_{DW}	25	—	—	30	—	—	ns
Data Hold Time		t_{DH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WP}	55	—	—	70	—	—	ns
Write Recovery Time		t_{WR}	0	—	—	0	—	—	ns
Address Setup Time		t_{AS}	0	—	—	0	—	—	ns
Output Active From End of Write	[6] [7]	t_{OW}	0	—	—	0	—	—	ns
Write Enable to Output in High Z	[6] [7]	t_{WZ}	0	—	30	0	—	40	ns

Notes: 6. Transition is measured at the point of +500mV from steady state voltage.
7. This parameter is measured with specified loading in Fig. 2.

WRITE CYCLE

WRITE CYCLE: $\overline{WE}$ CONTROLLED[9]

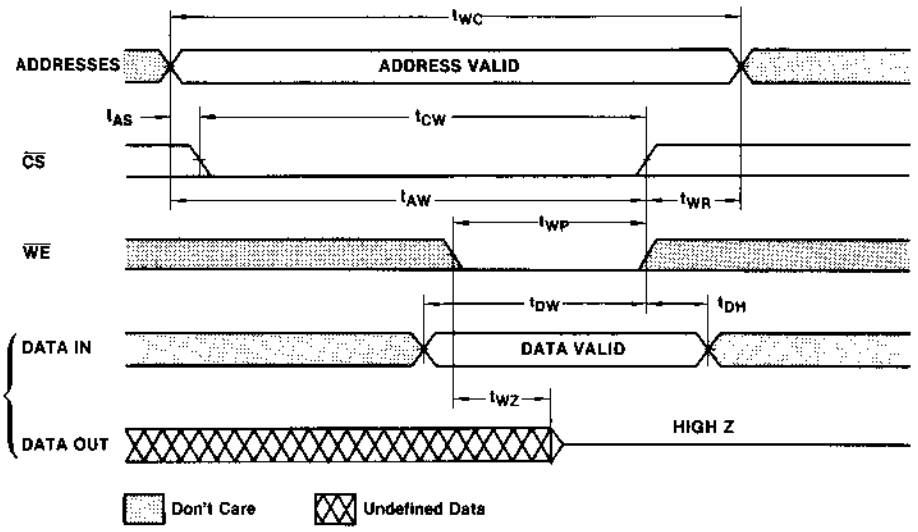


Note: *If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high transition, DATA OUT remains in a high impedance state.

Don't Care Undefined Data

WRITE CYCLE (Cont'd)

WRITE CYCLE: $\overline{CS}$ CHANGING[9]



Notes: 6. Transition is measureed at the point of ±500 mV from steady state voltage.
7. This parameter is measured with specified loading in Fig. 2.
8. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
9. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

DESCRIPTION

The MB8168 from Fujitsu is a high performance part. It is designed for high speed and low power system requirements.

The high speed is obtained by advanced NMOS processing. The power requirements are achieved by the use of MB8168 chip select (active low). The MB8168 automatically enters standby drawing only I_{SB} whenever the chip select is high. Upon activation of chip select ($\overline{CS}$ = LOW) the MB8168 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

CMOS STATIC RAMS

QUICK GUIDE TO PRODUCTS IN THIS SECTION

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB8416	2K x 8	200nS	+5	330mW/55μW	24-pin	3-2
MB8416-X	2K x 8	200nS	+5	330mW/55μW	24-pin	3-2
MB8416A-15	2K x 8	150nS	+5	330mW/11mW	24-pin	3-8
MB8416A-12	2K x 8	120nS	+5	330mW/11mW	24-pin	3-8
MB8417	2K x 8	200nS	+5	330mW/55μW	24-pin	3-9
MB8417-X	2K x 8	200nS	+5	330mW/55μW	24-pin	3-9
MB8417A-15	2K x 8	150nS	+5	330mW/11mW	24-pin	3-15
MB8417A-12	2K x 8	120nS	+5	330mW/11mW	24-pin	3-15
MB8418	2K x 8	200nS	+5	330mW/55μW	24-pin	3-16
MB8418-X	2K x 8	200nS	+5	330mW/55μW	24-pin	3-16
MB8418A-15	2K x 8	150nS	+5	330mW/11mW	24-pin	3-21
MB8418A-12	2K x 8	120nS	+5	330mW/11mW	24-pin	3-21

MB8416
MB8416-X

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

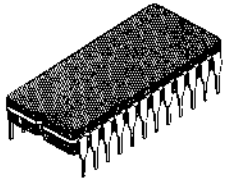
The Fujitsu MB8416/MB8416-X is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

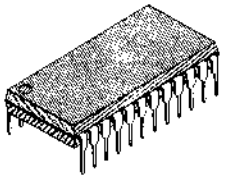
The MB8416/MB8416-X can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Output Enable ($\overline{OE}$) input permits the disable of all outputs when outputs are OR-tied. The MB8416/MB8416-X is packaged in an industry standard 24-pin dual in-line package.

FEATURES

- **Organized as 2048 words by 8 bits**
- **Fast Access Time: 200ns Max.**
- **Low Power: 55μW Max. Standby**
- **Completely Static Operation, no clocks required**
- **Extended temperature range (MB8416-X): −40°C to +85°C**
- **Single +5 Volt Power Supply, +10% tolerance**
- **TTL compatible Inputs/Outputs**
- **Low Voltage Data Retention: 2.0V Min.**
- **MB8416 is pin compatible with HM6116, TC5517, μPD446**

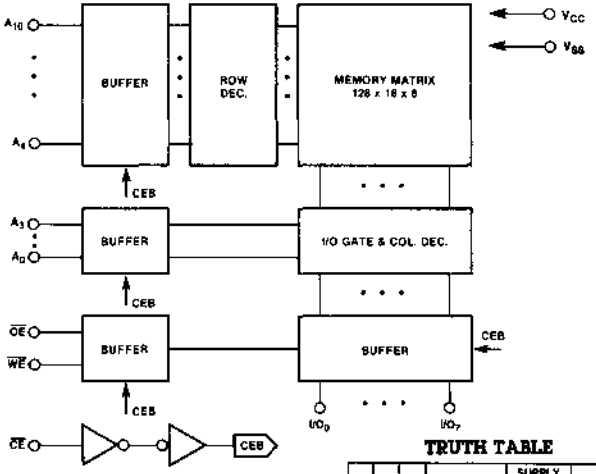


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

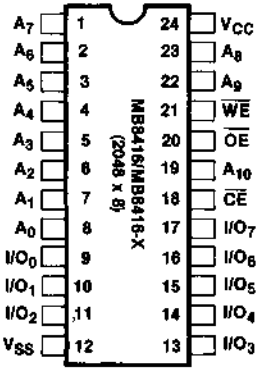
MB8416/MB8416-X BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Ceramic	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = GND)

Parameter	Symbol	MB8416			MB8416-X			Unit
		Min	Typ	Max	Min	Typ	Max	
Ambient Temperature	T_A	0	—	+70	−40	—	+85	°C
Supply Voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

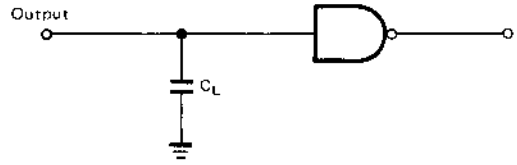
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Units
Standby Supply Current	$\overline{CE}$ = V_{CC} − 0.2 to V_{CC} +0.2V V_{IN} = −0.2V to V_{CC} +0.2V	I_{SB1}	—	10	μA
Standby Supply Current	$\overline{CE}$ = V_{IH} V_{IN} = −0.2V to V_{CC} +0.2V	I_{SB2}	—	2	mA
Active Supply Current	$\overline{CE}$ = V_{IL} V_{IN} = V_{IL} or V_{IH}; I_{OUT} = 0	I_{CC1}	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I_{OUT} = 0	I_{CC2}	—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{CE}$ = V_{IH}	I_{LO}	−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}	—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and C_L = 100 pF**



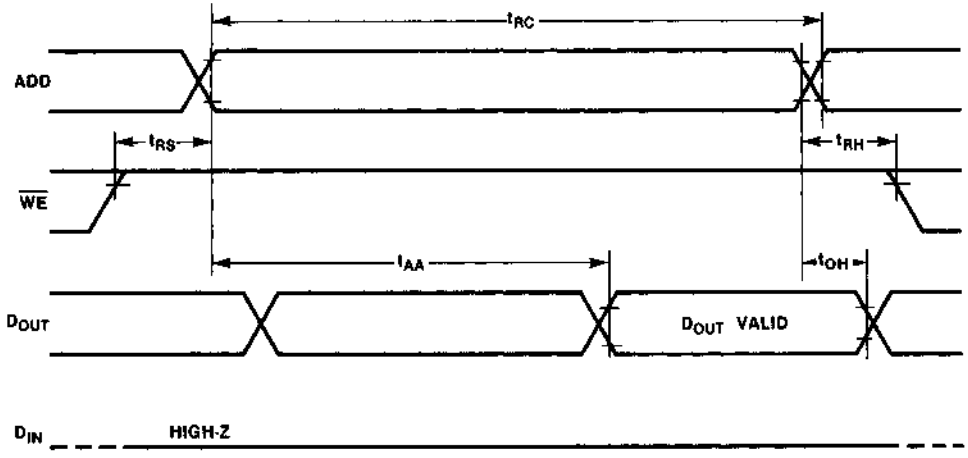
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Write Cycle Time	t_{WC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
Chip Enable Access Time	t_{ACE}	—	200	ns
Output Hold from Address Change	t_{OH}	15	—	ns
Output Low Z from $\overline{CE}$	t_{CLZ}	15	—	ns
Output High Z from $\overline{CE}$	t_{CHZ}	—	60	ns
Output Low Z from $\overline{OE}$	t_{OLZ}	15	—	ns
Output High Z from $\overline{OE}$	t_{OHZ}	—	60	ns
Output Low Z from $\overline{WE}$	t_{WLZ}	15	—	ns
Output High Z from $\overline{WE}$	t_{WHZ}	—	60	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Address Set Up Time	t_{AS}	0	—	ns
Read Set Up Time	t_{RS}	0	—	ns
Read Hold Time	t_{RH}	0	—	ns
Write Set Up Time	t_{WS}	0	—	ns
Write Hold Time	t_{WH}	0	—	ns
Address Valid to End of Write	t_{AW}	160	—	ns
Chip Enable to End of Write	t_{CEW}	160	—	ns
Write Pulse Width	t_{WP}	140	—	ns
Write Recovery Time	t_{WR}	10	—	ns
Data Set Up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DH}	0	—	ns

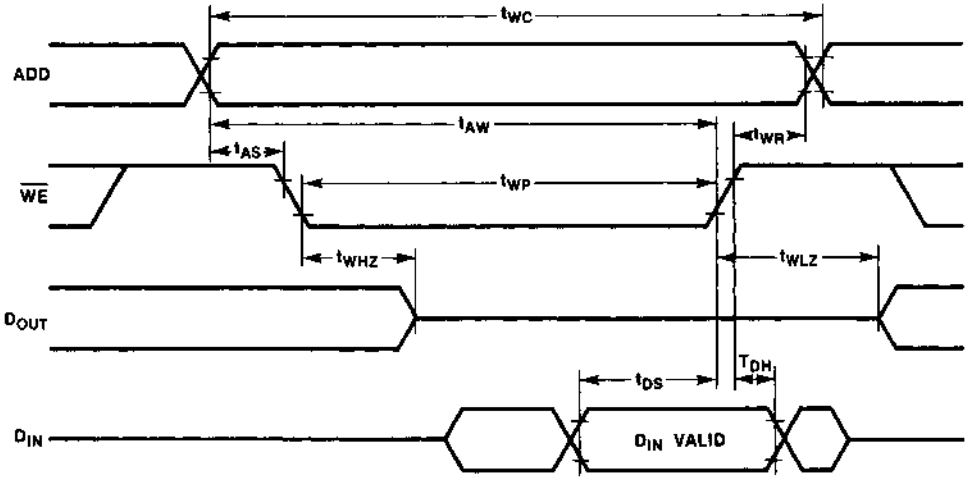
WAVEFORMS

MODE 1. $\overline{WE}$ Controlled. ($\overline{CE}$ = Low, $\overline{OE}$ = Low)

Read Cycle



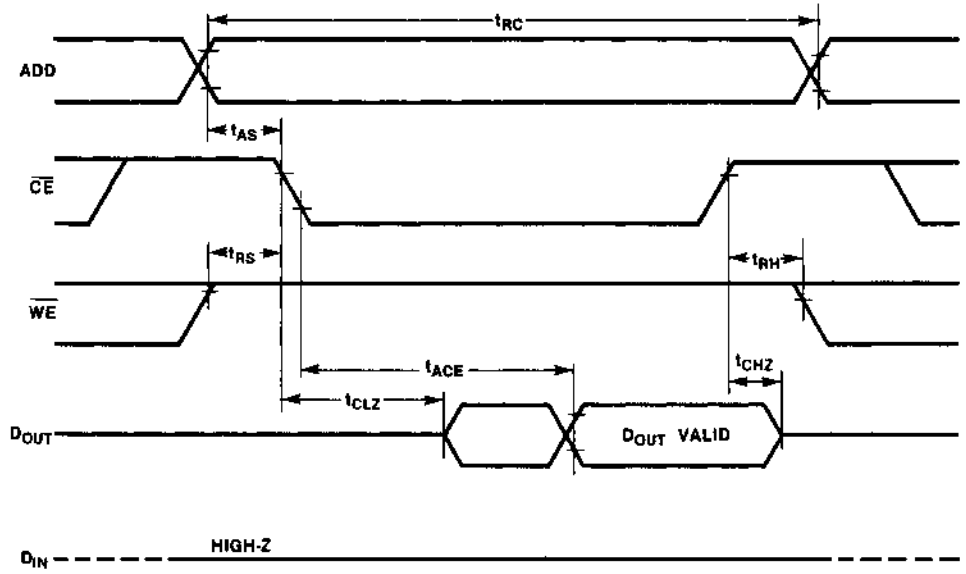
Write Cycle



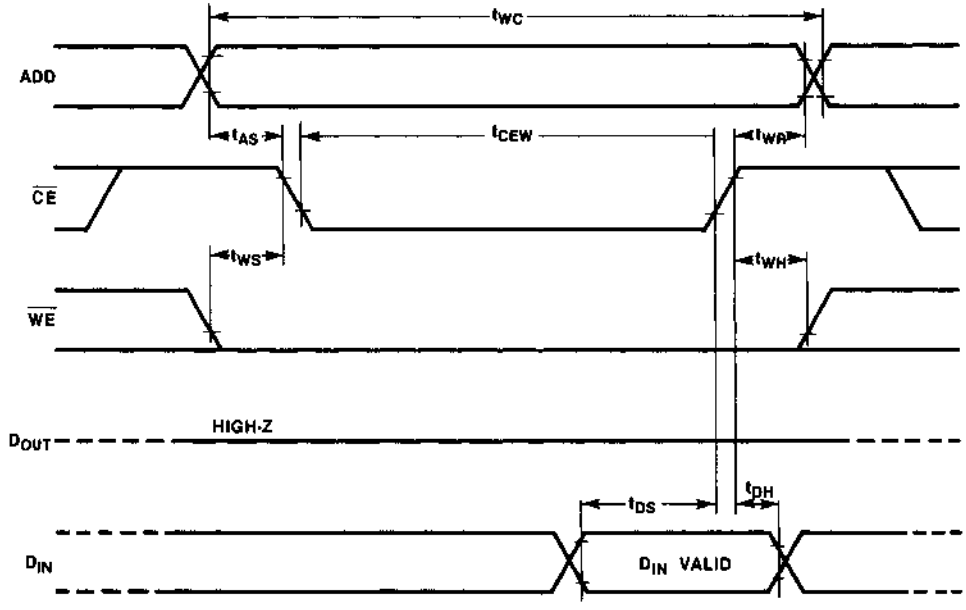
WAVEFORMS (Continued)

MODE 2. $\overline{CE}$ Controlled, ($\overline{OE}$ = Low)

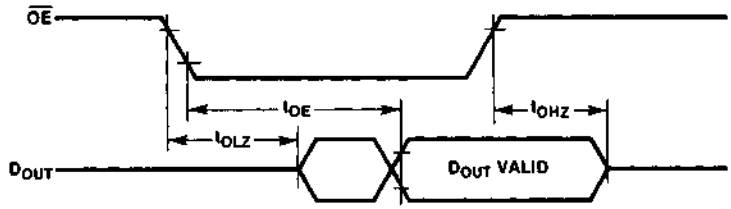
Read Cycle



Write Cycle



WAVEFORMS (Continued)
Enable/Disable $\overline{OE}$ Controlled; ($\overline{CE}$ = Low, $\overline{WE}$ = High)



DYNAMIC CHARACTERISTICS

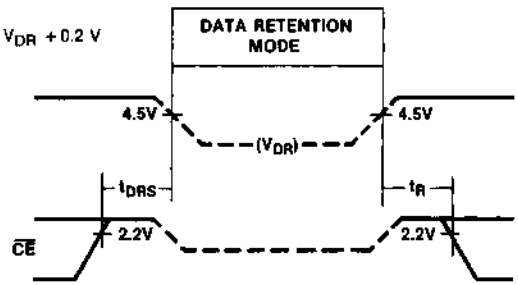
Data Retention Characteristics, Notes [1,2]

Parameter	Notes	Symbol	Min	Max	Unit
Data Retention Supply Voltage	[1]	V_{DR}	2.0	5.5	V
Data Retention Supply Current	[2]	I_{DR}	—	10	μA
Data Retention Set Up Time		t_{DRS}	60	—	ns
Recovery Time		t_R	60	—	ns

NOTES:

[1.] $V_{CC} = V_{DR}$, $\overline{CE} = V_{DR} - 0.2$ V to $V_{DR} + 0.2$ V, $V_{IN} = -0.2$ V to $V_{DR} + 0.2$ V

[2.] When V_{DR} = 2.5V to 5.5V,
$\overline{CE}$ = 2.2V to V_{DR} + 0.3V
When V_{DR} = 2.0V to 2.5V
$\overline{CE} = V_{DR} - 0.3$V to $V_{DR} + 0.3$V



FUJITSU
MICROELECTRONICS

MB8416A-12
MB8416A-15

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

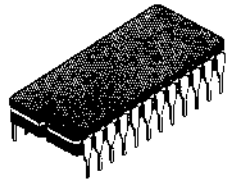
ADVANCE INFORMATION

DESCRIPTION

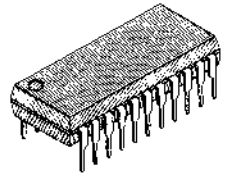
The Fujitsu MB8416A is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

The MB8416A can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Output Enable ($\overline{OE}$) input permits the disable of all outputs when outputs are OR-tied. The MB8416A is packaged in an industry standard 24-pin dual in-line package.



CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24C-M01

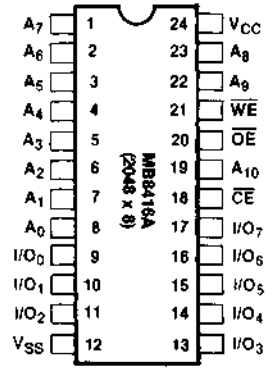
FEATURES

- **Organized as 2048 words by 8-bits**
- **Address Access Time:**
  MB8416A-12 120ns Max.
  MB8416A-15 150ns Max.
- **Low Power Dissipation:**
  I_{CC} (Active) = 60mA Max.
  I_{SB} (Standby) = 4mA Max.
  I_{DR} (Data Retention) = 2mA Max.
- **Completely static operation, no clocks required**
- **Single +5 Volt Power Supply, ±10% tolerance**
- **TTL compatible inputs/outputs**
- **Data Retention: 2.0V Min.**
- **Equal Access and Cycle Times**
- **Output timing reference levels: 0.8V to 2.2V**
- **Plug-in compatible with 16K EPROMs**
- **Pin compatible with HM6116, TC5517, μPD446**

TRUTH TABLE

DEVICE NUMBER	MB8416A				
PIN NUMBER	18	20	21	24	9-11 13-17
PIN NAME / MODE	CE	OE	WE	SUPPLY CURRENT	I/O
WRITE	L	X	L	I_{CC}	D_{IN}
READ	L	L	H	I_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	H	I_{CC}	HIGH Z
STANDBY	H	X	X	I_{SB}	HIGH Z

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU
MICROELECTRONICS

MB8417
MB8417-X

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

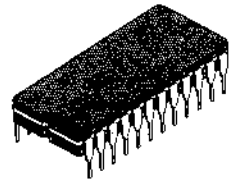
The Fujitsu MB8417/MB8417-X is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

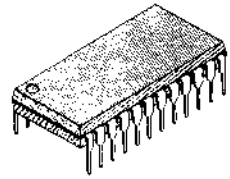
The MB8417/MB8417-X can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Chip Select ($\overline{CS}$) permits fast access time. The device is packaged in an industry standard 24-pin dual in-line package.

FEATURES

- **Organized as 2048 words by 8-bits**
- **Fast Access Time:**
  200 ns Max. ($\overline{CE}$ Controlled)
  100 ns Max. ($\overline{CS}$ Controlled)
- **Low Power: 55 μW Max.**
  Standby
- **Completely Static Operation, no clocks required**
- **Extended temperature range (MB8417-X): −40° to +85°C**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention**
  2.0V Min.
- **MB8417 is pin compatible with TC5516, μPD447**

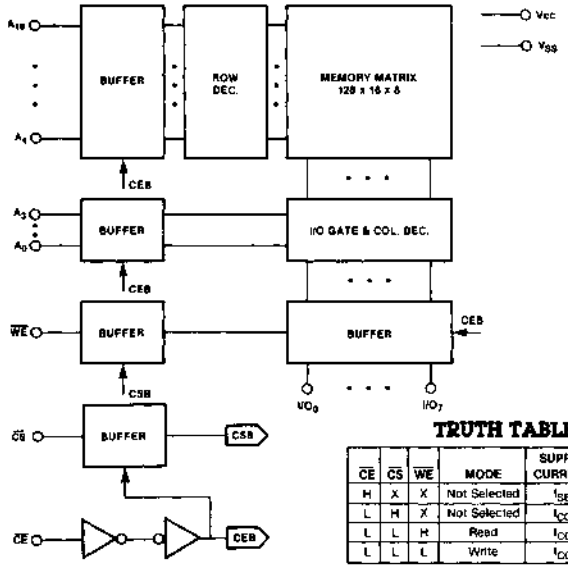


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

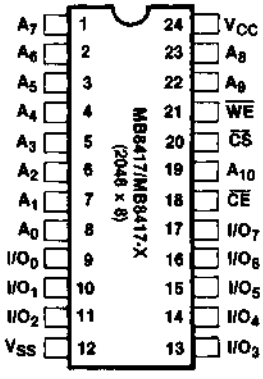
MB8417/MB8417-X BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{CS}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	X	Not Selected	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Ceramic	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, V_{SS} = GND

Parameter	Symbol	MB8417			MB8417-X			Unit
		Min	Typ	Max	Min	Typ	Max	
Ambient Temperature	T_A	0	—	+70	−40	—	+85	°C
Supply Voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

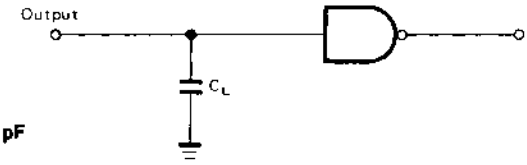
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Units
Standby Supply Current	$\overline{CE}$ = V_{CC} − 0.2V to V_{CC} + 0.2V V_{IN} = −0.2V to V_{CC} + 0.2V	I_{SB1}	—	10	μA
Standby Supply Current	$\overline{CE}$ = V_{IH} V_{IN} = −0.2V to V_{CC} + 0.2V	I_{SB2}	—	2	mA
Active Supply Current	$\overline{CE}$ = V_{IL} V_{IN} = V_{IL} or V_{IH}; I_{OUT} = 0	I_{CC1}	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I_{OUT} = 0	I_{CC2}	—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{CE}$ = V_{IH}	I_{LO}	−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}	—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and C_L = 100 pF**



DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Write Cycle Time	t_{WC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
Chip Enable Access Time	t_{ACE}	—	200	ns
Chip Select Access Time	t_{ACS}	—	100	ns
Output Hold from Address Change	t_{OH}	15	—	ns
Output Low Z from $\overline{CE}$ or $\overline{CS}$	t_{CLZ}	15	—	ns
Output High Z from $\overline{CE}$ or $\overline{CS}$	t_{CHZ}	—	60	ns
Output Low Z from $\overline{WE}$	t_{WLZ}	15	—	ns
Output High Z from $\overline{WE}$	t_{WHZ}	—	60	ns
Address Set Up Time	t_{AS}	0	—	ns
Read Set Up Time	t_{RS}	0	—	ns
Read Hold Time	t_{RH}	0	—	ns
Write Set Up Time	t_{WS}	0	—	ns
Write Hold Time	t_{WH}	0	—	ns
Address Valid to End of Write	t_{AW}	160	—	ns
Chip Enable to End of Write	t_{CEW}	160	—	ns
Chip Selection to End of Write	t_{CSW}	100	—	ns
Write Pulse Width	t_{WP}	140	—	ns
Write Recovery Time	t_{WR}	10	—	ns
Data Set Up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DH}	0	—	ns

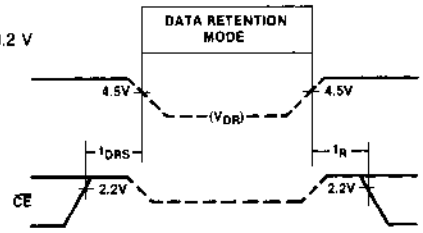
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, Notes [1,2]

Parameter	Notes	Symbol	Min	Max	Unit
Data Retention Supply Voltage	[1]	V_{DR}	2.0	5.5	V
Data Retention Supply Current	[2]	I_{DR}	—	10	μA
Data Retention Set Up Time		t_{DRS}	60	—	ns
Recovery Time		t_R	60	—	ns

NOTES:

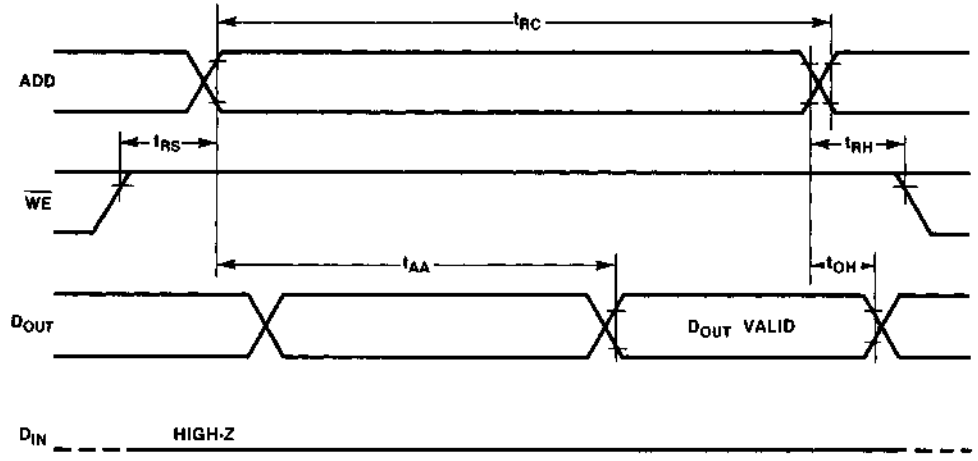
1. $V_{CC} = V_{DR}$, $\overline{CE} = V_{DR} - 0.2$ V to $V_{DR} + 0.2$ V, $V_{IN} = -0.2$ V to $V_{DR} + 0.2$ V
2. When V_{DR} = 2.5V to 5.5V,
   $\overline{CE}$ = 2.2V to V_{DR} + 0.3V
   When V_{DR} = 2.0V to 2.5V
   $\overline{CE} = V_{DR} - 0.3$V to $V_{DR} + 0.3$V



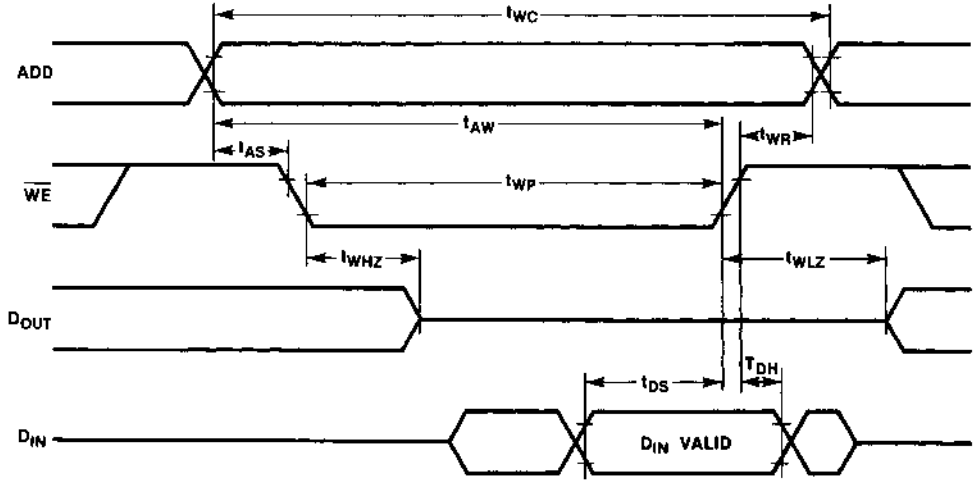
WAVEFORMS

MODE 1. $\overline{WE}$ Controlled: ($\overline{CE}$ = Low, $\overline{CS}$ = Low)

Read Cycle



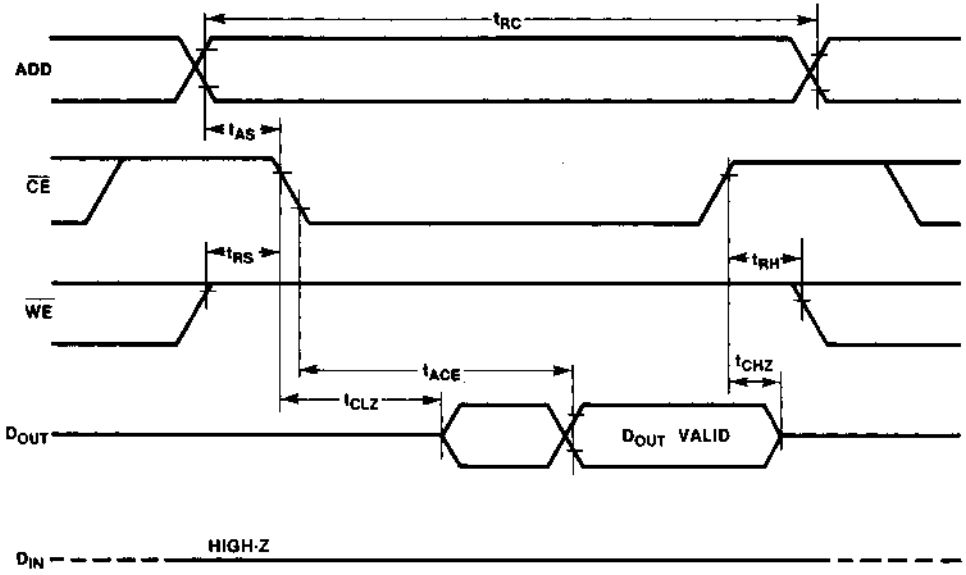
Write Cycle



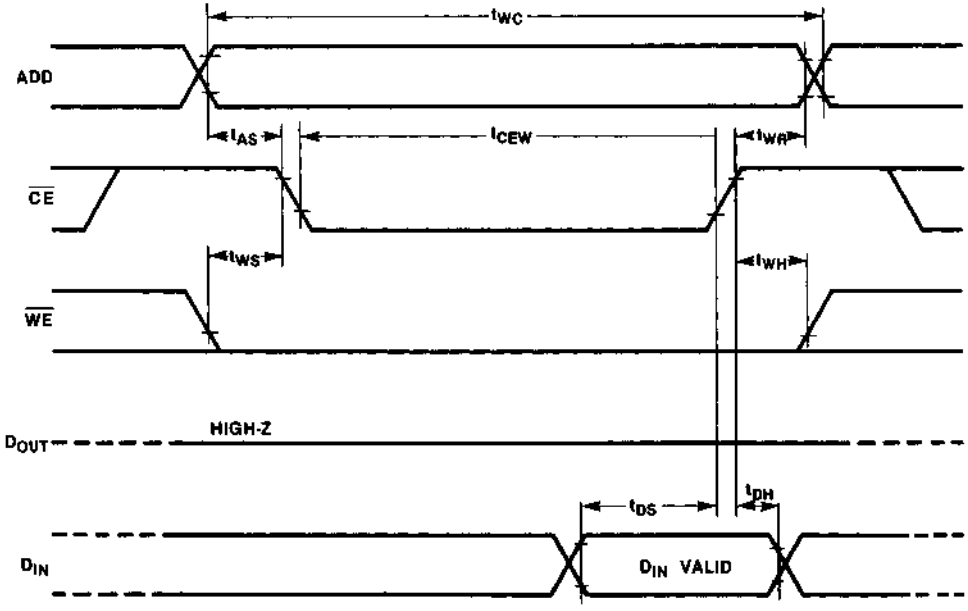
WAVEFORMS (Continued)

MODE 2. $\overline{CE}$ Controlled, ($\overline{CS}$ = Low)

Read Cycle



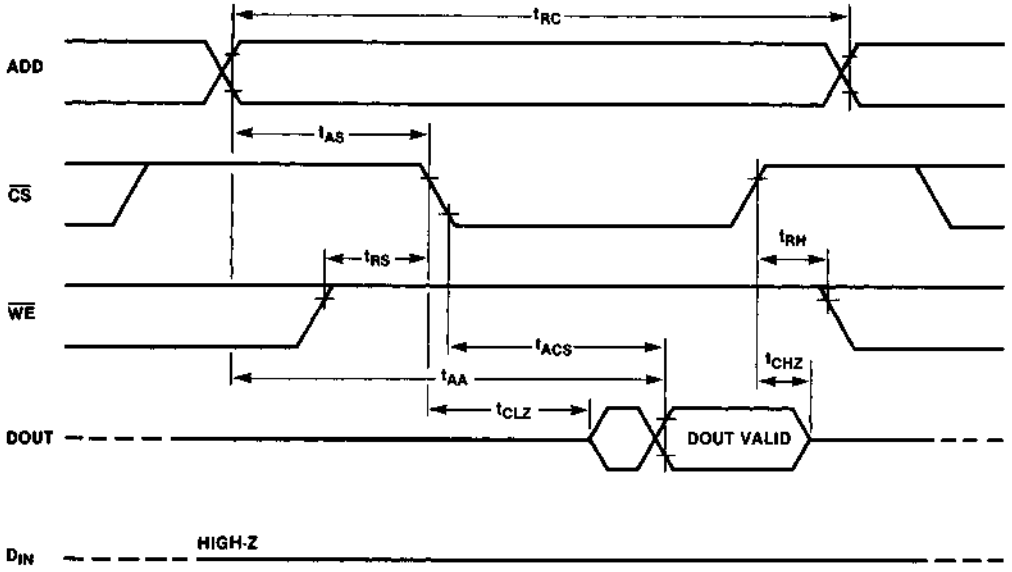
Write Cycle



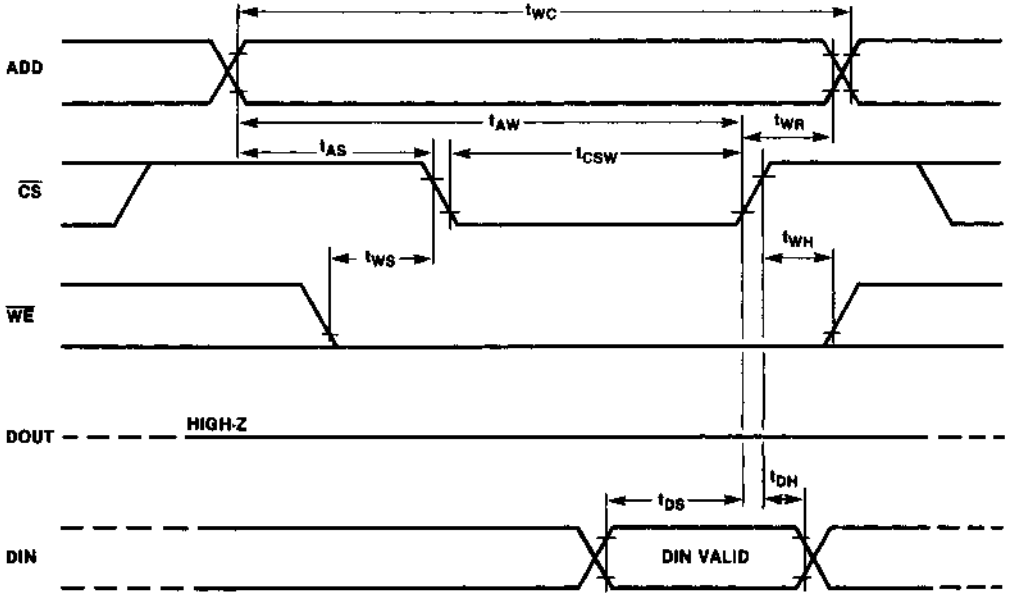
WAVEFORMS (Continued)

MODE 3: $\overline{CS}$ Controlled, ($\overline{CE}$ = Low)

Read Cycle



Write Cycle



FUJITSU
MICROELECTRONICS

MB8417A-12
MB8417A-15

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

ADVANCE INFORMATION

DESCRIPTION

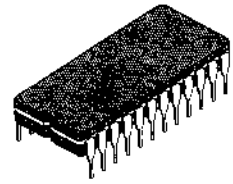
The Fujitsu MB8417A is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

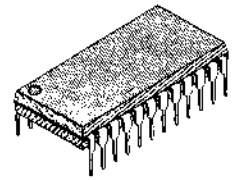
The MB8417A can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Chip Selects ($\overline{CS}$) permits fast access time. The MB8417A is packaged in an industry standard 24-pin dual in-line package.

FEATURES

- **Organized as 2048 words by 8-bits**
- **Address Access Time:**
  MB8417A-12 120ns Max.
  MB8417A-15 150ns Max.
- **Low Power Dissipation:**
  I_{CC} (Active) = 60mA Max.
  I_{SB} (Standby) = 4mA Max.
  I_{DR} (Data Retention) = 2mA Max.
- **Completely Static Operation, no clocks required**
- **Single +5 V Power Supply, ±10% tolerance**
- **TTL Compatible Inputs/Outputs**
- **Data Retention 2.0V Min.**
- **Equal Access and Cycle Times**
- **Output Timing reference levels: 0.8V to 2.2V**
- **Pin compatible with TC5516, μPD447**

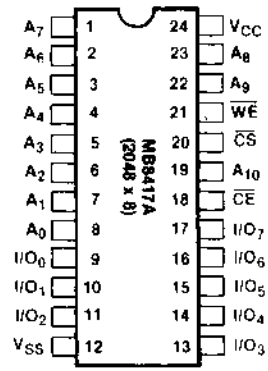


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24C-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

TRUTH TABLE

DEVICE NUMBER	MB8417A				
PIN NUMBER	18	20	21	24	9-11, 13-17
PIN NAME / MODE	$\overline{CE}$	$\overline{CS}$	$\overline{WE}$	SUPPLY CURRENT	I/O
WRITE	L	L	L	I_{CC}	D_{IN}
READ	L	L	H	I_{CC}	D_{OUT}
CHIP DESELECT	L	H	X	I_{CC}	HIGH Z
STANDBY 2	H	X	X	I_{SB}	HIGH Z

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

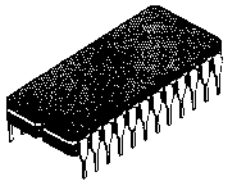
The Fujitsu MB8418/MB8418-X is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

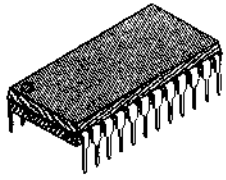
The MB8418/MB8418-X can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Two chip selects ($\overline{CE}_2$ and $\overline{CE}_1$) permit the selection of an individual package when outputs are OR-tied, and the device automatically powers down. The MB8418/MB8418-X is packaged in an industry standard 24-pin dual in-line package.

FEATURES

- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200ns Max.**
- **Low Power: 55μW Max. Standby**
- **Completely Static Operation, no clocks required**
- **Extended Temperature Range (MB8418-X): −40°C to +85°C**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **MB8418 is compatible with TC5518**

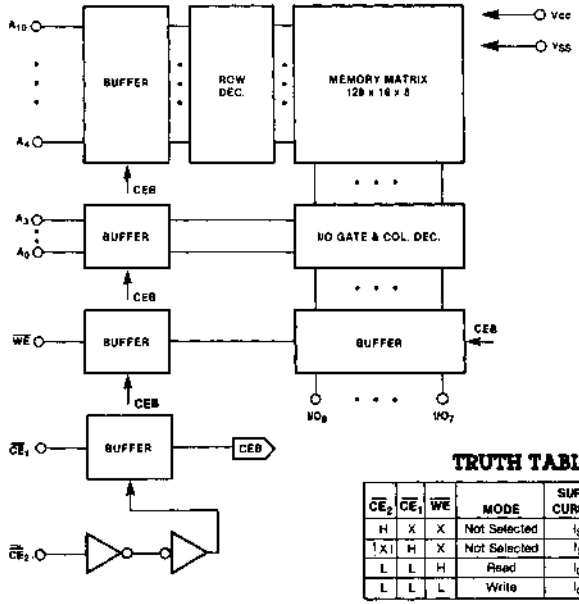


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

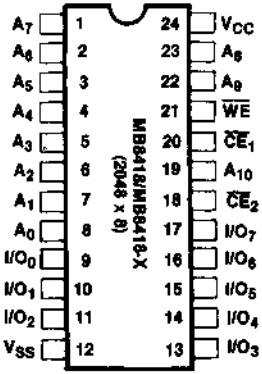
MB8418/MB8418-X BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}_2$	$\overline{CE}_1$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Ceramic	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, (Referenced to V_{SS} = GND)

Parameter	Symbol	MB8418			MB8418-X			Unit
		Min	Typ	Max	Min	Typ	Max	
Ambient Temperature	T_A	0	—	+70	−40	—	+85	°C
Supply Voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	−0.3	—	0.8	V

CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

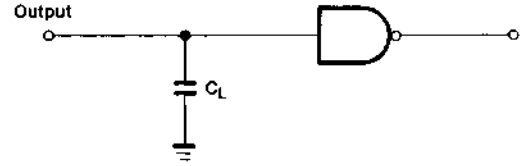
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Units
Standby Supply Current	$\overline{CE}$ = V_{CC} − 0.2V to V_{CC} + 0.2V V_{IN} = −0.2V to V_{CC} + 0.2V	I_{SB1}	—	10	μA
Standby Supply Current	$\overline{CE}$ = V_{IH} V_{IN} = −0.2V to V_{CC} +0.2V	I_{SB2}	—	2	mA
Active Supply Current	$\overline{CE}$ = V_{IL} V_{IN} = V_{IL} or V_{IH}; I_{OUT} = 0	I_{CC1}	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I_{OUT} = 0	I_{CC2}	—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{CE_1}$ or $\overline{CE_2}$ = V_{IH}	I_{LO}	−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}	—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns (Between 0.8V to 2.2V)**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and C_L = 100 pF**



DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Write Cycle Time	t_{WC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
Chip Enable Access Time	t_{ACE}	—	200	ns
Output Hold from Address Change	t_{OH}	15	—	ns
Output Low Z from $\overline{CE}_2$ or $\overline{CE}_1$	t_{CLZ}	15	—	ns
Output High Z from $\overline{CE}_2$ or $\overline{CE}_1$	t_{CHZ}	—	60	ns
Output Low Z from $\overline{WE}$	t_{WLZ}	15	—	ns
Output High Z from $\overline{WE}$	t_{WHZ}	—	60	ns
Address Set Up Time	t_{AS}	0	—	ns
Read Set Up Time	t_{RS}	0	—	ns
Read Hold Time	t_{RH}	0	—	ns
Write Set Up Time	t_{WS}	0	—	ns
Write Hold Time	t_{WH}	0	—	ns
Address Valid to End of Write	t_{AW}	160	—	ns
Chip Enable to End of Write	t_{CEW}	160	—	ns
Write Pulse Width	t_{WP}	140	—	ns
Write Recovery Time	t_{WR}	10	—	ns
Data Set Up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DH}	0	—	ns

DYNAMIC CHARACTERISTICS

Data Retention Characteristics, Notes [1,2]

Parameter	Notes	Symbol	Min	Max	Unit
Data Retention Supply Voltage	[2]	V_{DR}	2.0	5.5	V
Data Retention Supply Current	[1]	I_{DR}	—	10	μA
Data Retention Set Up Time		t_{DRS}	60	—	ns
Recovery Time		t_R	60	—	ns

NOTES:

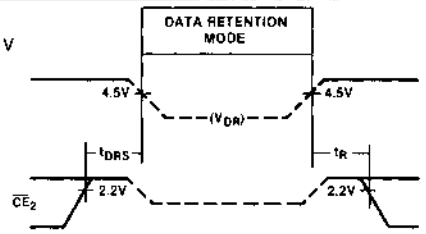
[1.] $V_{CC} = V_{DR}$, $\overline{CE}_2 = V_{DR} - 0.2$ V to $V_{DR} + 0.2$ V, $V_{IN} = -0.2$ V to $V_{DR} + 0.2$ V

[2.] When V_{DR} = 2.5V to 5.5V,

($\overline{CE}_1$) $\overline{CE}_2$ = 2.2V to V_{DR} + 0.3V

When V_{DR} = 2.0V to 2.5V

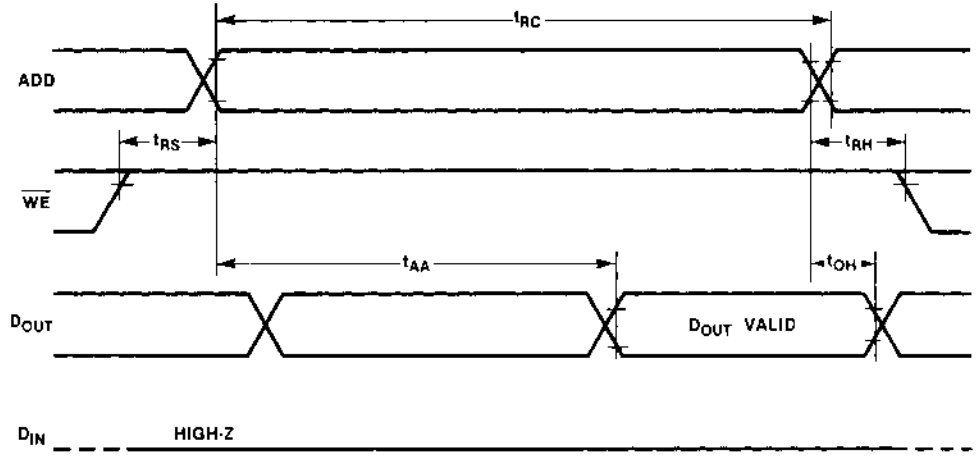
($\overline{CE}_1$) $\overline{CE}_2$ = V_{DR} − 0.3V to V_{DR} + 0.3V



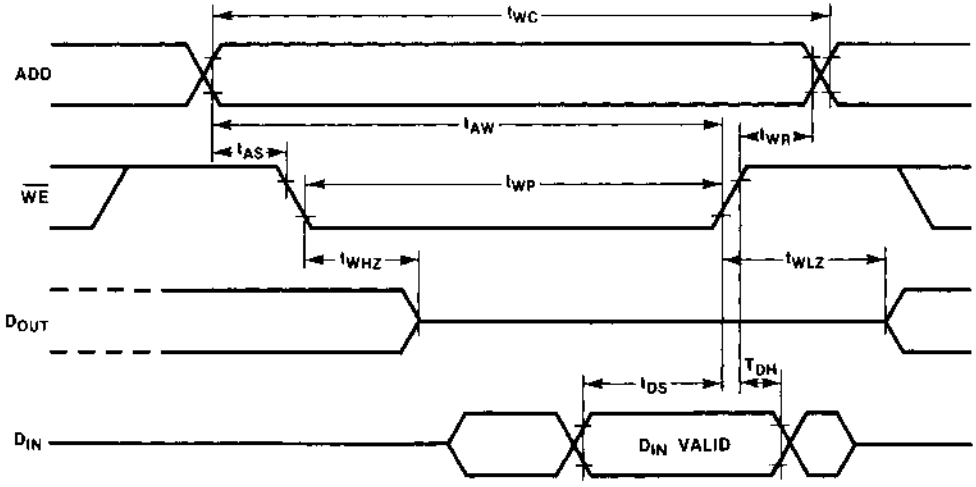
WAVEFORMS

MODE 1: $\overline{WE}$ Controlled: ($\overline{CE_2}$ = LOW, $\overline{CE_1}$ = LOW)

Read Cycle



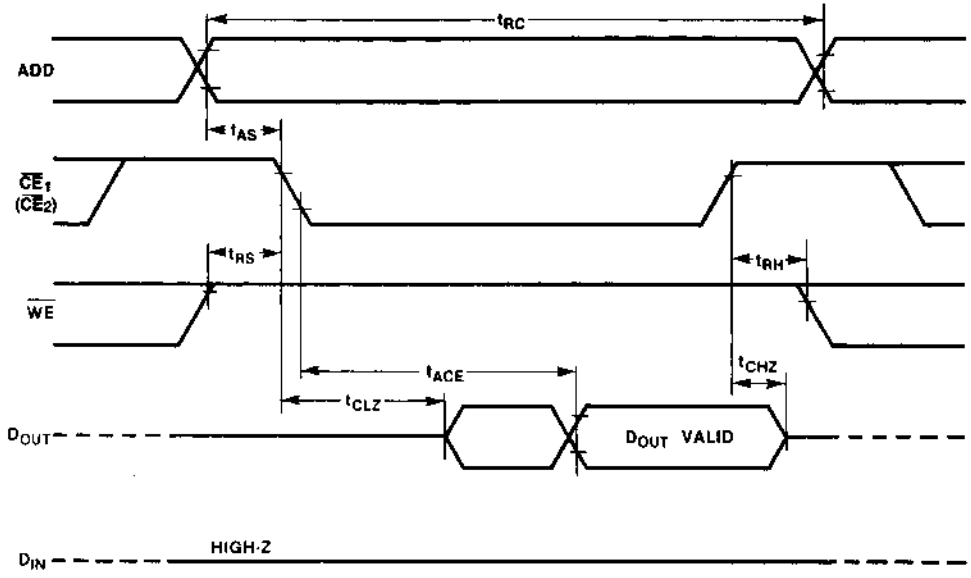
Write Cycle



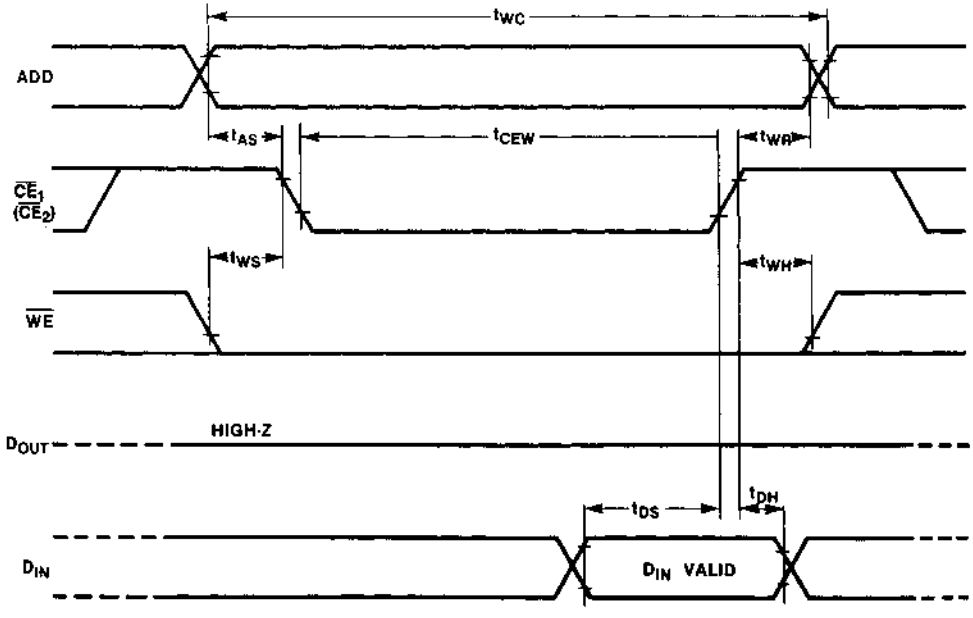
WAVEFORMS (Continued)

MODE 2: $\overline{CE_1}$ or $\overline{CE_2}$ Controlled, ($\overline{CE_2}$ = LOW or $\overline{CE_1}$ = LOW)

Read Cycle



Write Cycle



FUJITSU
MICROELECTRONICS

MB8418A-12
MB8418A-15

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

ADVANCE INFORMATION

DESCRIPTION

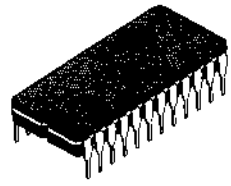
The Fujitsu MB8418A is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

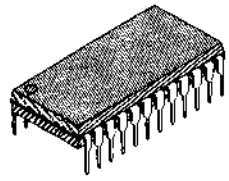
The MB8418A can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Two chip selects ($\overline{CE}_2$ and $\overline{CE}_1$) permit the selection of an individual package when outputs are OR-tied, and the device automatically powers down. The MB8418A is packaged in an industry standard 24-pin dual in-line package.

FEATURES

- **Organized as 2048 words by 8-bits**
- **Address Access Time:**
  MB8418A-12 120ns Max.
  MB8418A-15 150ns Max.
- **Low Power Dissipation:**
  I_{CC} (Active) = 60mA Max.
  I_{SB} (Standby) = 4mA Max.
  I_{DR} (Data Retention) = 2mA Min.
- **Completely static operation, no clocks required**
- **Single +5V Power Supply, ±10% tolerance**
- **TTL compatible inputs/outputs**
- **Data Retention: 2.0V Min.**
- **Equal Access and Cycle Times**
- **Output timing reference levels: 0.8V to 2.2V**
- **Both $\overline{CE}_2$ and $\overline{CE}_1$ (Pins 18 and 20) provide power-down capability**
- **Pin compatible with TC5518**

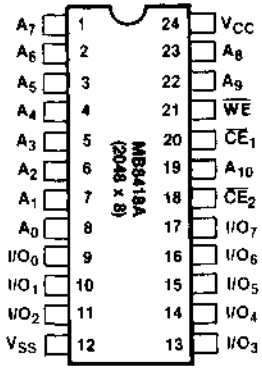


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24C-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

TRUTH TABLE

DEVICE NUMBER	MB8418A				
PIN NUMBER	18	20	21	24	9-11 13-17
PIN NAME / MODE	$\overline{CE}_2$	$\overline{CE}_1$	$\overline{WE}$	SUPPLY CURRENT	I/O
WRITE	L	L	L	I_{CC}	D_{IN}
READ	L	L	H	I	D_{OUT}
OUTPUT DISABLE	—	—		—	—
CHIP SELECT	—	—	—	—	—
STANDBY 1	X	H	X	I_{SB}	HIGH Z
STANDBY 2	H	X	X	I_{SB}	HIGH Z

NMOS AND CMOS EPROMS

EPROMS

QUICK GUIDE TO PRODUCTS IN THIS SECTION

Device	Technology	Organization	Access Time (max)	Power Supply Volts	Power Dissipation Active	Power Dissipation Standby	Package	Page
MBM2716	NMOS	2K x 8	450nS	+5	525	132mW	24-pin	4-2
MBM2716H	NMOS	2K x 8	350nS	+5	550	138mW	24-pin	4-2
MBM2716-X	NMOS	2K x 8	450nS	+5	525	132mW	24-pin	4-2
MBM2732-45	NMOS	4K x 8	450nS	+5	788	158mW	24-pin	4-7
MBM2732-35	NMOS	4K x 8	350nS	+5	825	165mW	24-pin	4-7
MBM2732A-35	NMOS	4K x 8	350nS	+5	825	165mW	24-pin	4-14
MBM2732A-35X	NMOS	4K x 8	350nS	+5	825	165mW	24-pin	4-14
MBM2732A-30	NMOS	4K x 8	300nS	+5	788	184mW	24-pin	4-14
MBM2732A-25	NMOS	4K x 8	250nS	+5	788	184mW	24-pin	4-14
MBM2732A-20	NMOS	4K x 8	200nS	+5	788	184mW	24-pin	4-14
MBM27C32-25	CMOS	4K x 8	250nS	+5	40mW/MHz		24-pin	4-20
MBM27C32-30	CMOS	4K x 8	300nS	+5	40mW/MHz		24-pin	4-20
MBM2764-30	NMOS	8K x 8	300nS	+5	788	184mW	28-pin	4-21
MBM2764-30X	NMOS	8K x 8	300nS	+5	788	184mW	24-pin	4-21
MBM2764-25	NMOS	8K x 8	250nS	+5	788	184mW	28-pin	4-21
MBM2764-20	NMOS	8K x 8	200nS	+5	788	184mW	28-pin	4-21
MBM27C64-30	CMOS	8K x 8	300nS	+5	40mW/MHz		28-pin	4-28
MBM27C64-25	CMOS	8K x 8	250nS	+5	40mW/MHz		28-pin	4-28

FUJITSU
MICROELECTRONICS

MBM2716
MBM2716H
MBM2716-X

UV ERASABLE 16,384-BIT READ ONLY MEMORY

DESCRIPTION

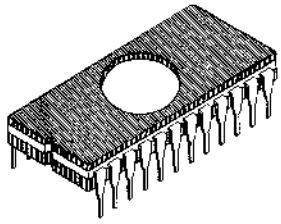
The Fujitsu MBM2716 is a high speed 16,384-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 24-pin dual in-line package with a transparent lid is used to package the MBM2716. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2716 is fabricated using N-channel double polysilicon gate technology with single transitor stacked gate cells. It is organized as 2048 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

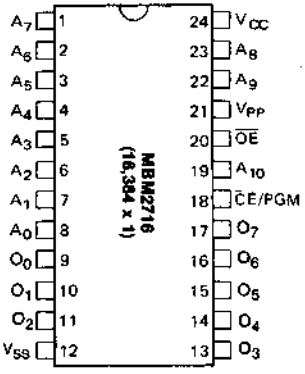
FEATURES

- **Organized as 2048 words by 8-bits, fully decoded**
- **Fast Access Time:**
  MBM2716 450ns Max.
  MBM2716H 350ns Max.
  MBM2716-X 450ns Max.
- **MBM2716-X: Extended temperature range**
  −40°C to +85°C
- **Fast programmming:**
  100 sec. for all 16,384 bits
- **Low power requirement:**
  525 mW Active
  132 mW Standby
- **No clocks required, fully static operation**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-TIE capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion and bus control**
- **Single +5V Operation**
- **Standard 24-pin DIP package**
- **MBM2716/MBM2716H are compatible with Intel 2716**
- **MBM2716-X is compatible with Intel I2716**



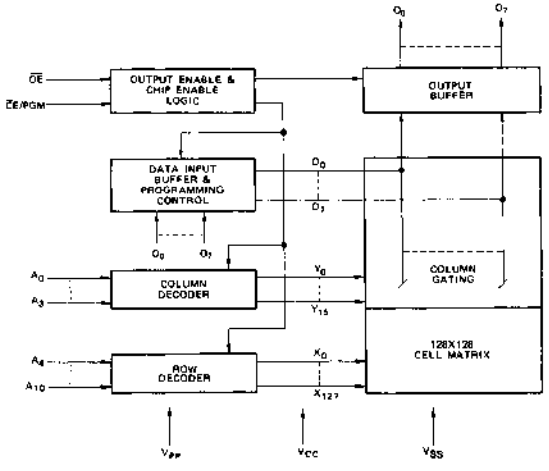
CERDIP PACKAGE
DIP-24C-C02

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MBM2716 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (see Note)

Rating		Symbol	Value	Unit
Temperature Under Bias	MBM2716/MBM2716H	T_A	−25 to +85	°C
	MBM2716-X		−50 to +95	°C
Storage Temperature		T_{stg}	−65 to +125	°C
Inputs/Outputs (Except V_{PP}) with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.3 to +7	V
Program Input with Respect to V_{SS}		V_{PP}	−0.3 to +26.5	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.3 to +7	V
Power Dissipation		P_D	1.6	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter		Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage(1)	MBM2716 MBM2716-X	V_{CC}	4.75	5.0	5.25	V	MBM2716/MBM2716H 0°C to +70°C
	MBM2716H		4.5	5.0	5.5		
Supply Voltage		V_{SS}	—	GND	—	V	
V_{PP} Power Supply(2)		V_{PP}	0.0	5.0	V_{CC} +0.6	V	MBM2716-X −40°C to +85°C
Input High Voltage		V_{IH}	2.0	—	V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1	—	0.8	V	

Note: (1) V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
(2) During read operation, V_{PP} may be connected either to V_{CC} or V_{SS}.
When connected to V_{CC}, V_{CC} current would be the sum of I_{CC} and I_{PP1}.

FUNCTIONS AND PIN CONNECTIONS $V_{CC}(24)$ = +5V, $V_{SS}(12)$ = GND

Function (Pin No.) / Mode	Address Input (1 – 8, 19, 22, 23)	Data I/O (9 – 11, 13 – 17)	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} Supply (21)	I_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5	I_{CC2}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	+5	I_{CC2}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	+5	I_{CC1}
Program	A_{IN}	D_{IN}	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	I_{CC2}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+25	I_{CC2}
Program Inhibit	Don't Care	High Z	V_{IL}	V_{IH}	+25	I_{CC2}

CAPACITANCE (T_A = 25°C; f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

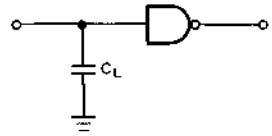
Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current (V_{PP} = 5.85V)	I_{PP1}	—	—	5	mA
V_{CC} Supply Current (Standby)	I_{CC1}	—	—	25	mA
V_{CC} Supply Current (Active)	I_{CC2}	—	—	100	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤ 20nS

Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs

Output Load: 1 TTL gate and C_L = 100pF

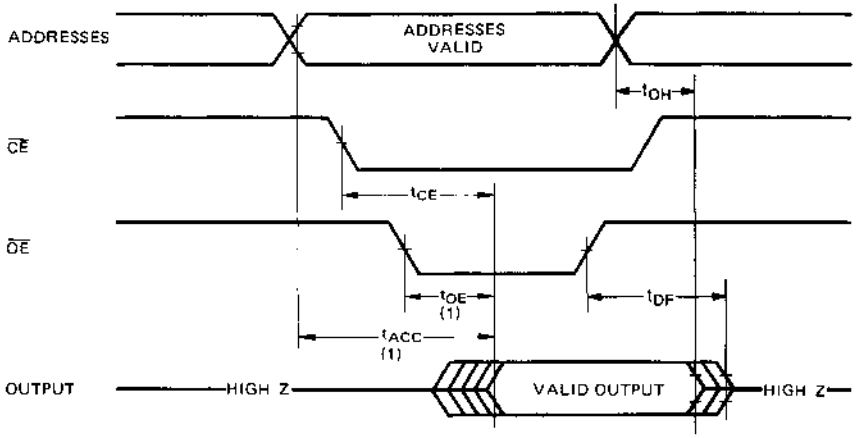


AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	MBM2716		MBM2716H		MBM2716-X		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}	—	450	—	350	—	450	ns
Chip Enable to Output Delay	t_{CE}	—	450	—	350	—	450	ns
Output Enable to Output Delay	t_{OE}	—	120	—	120	—	150	ns
Address to Output Hold	t_{OH}	0	—	0	—	0	—	ns
Output Enable High to Output Float	t_{DF}	0	100	0	100	0	130	ns

OPERATION TIMING DIAGRAM



Note: (1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM2716 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and top select gate (see Fig. 14). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 15). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{THO}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 15.

Fig. 14 — MEMORY CELL

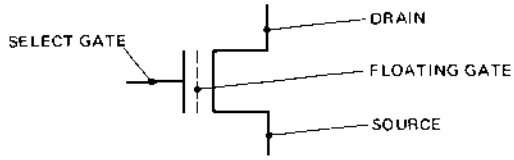
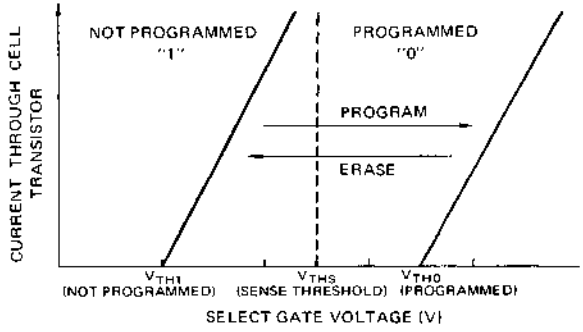


Fig. 15 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2716 has all 16,384 bits in the "1", or high, state. "0's" are loaded into the MBM2716 through the procedure of programming.

The programming mode is entered when +25V is applied to the V_{PP} pin and when $\overline{OE}$ is at V_{IH}. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data outputs pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL High-level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2716 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM2716. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM2716 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2716 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM2716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING INFORMATION (Continued)

DC CHARACTERISTICS

(T_A = 25°C, V_{CC}(1) = 5V ±5%, V_{PP}(1,2) = 25V ±1V, V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Current (V_{IN} = 5.25V/0.45V)	I_{IL}	—	—	10	μA
V_{PP} Supply Current ($\overline{CE}$/PGM = V_{IL})	I_{PP1}	—	—	5	mA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$/PGM = V_H)	I_{PP2}	—	—	30	mA
V_{CC} Supply Current	I_{CC2}	—	—	100	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IL}	2.0	—	V_{CC} + 1	V

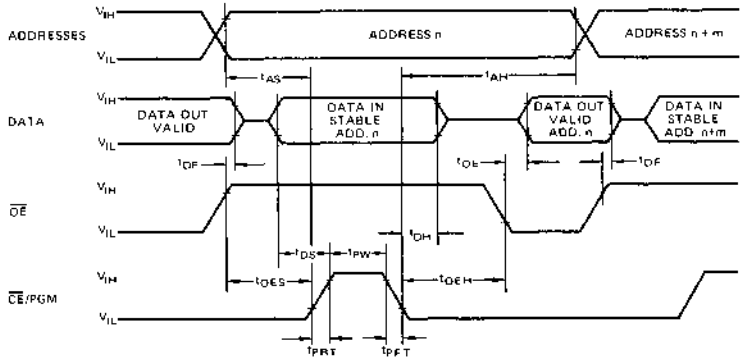
Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out or put into a socket remaining V_{PP} = 25 volts. Also, during $\overline{OE}$ = $\overline{CE}$/PGM = V_{IH}, V_{PP} must not be switched from 5 volts to 25 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
Output Enable Setup Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	2	—	—	μs
Output Enable Hold Time	t_{OEH}	2	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Output Disable to Output Float Delay ($\overline{CE}$/PGM = V_{IL})	t_{DF}	0	—	120	ns
Output Enable to Output Delay ($\overline{CE}$/PGM = V_{IL})	t_{OE}	—	—	120	ns
Program Pulse Width	t_{PW}	45	50	55	ms
Program Rise Pulse Time	t_{PRT}	5	—	—	ns
Program Pulse Fall Time	t_{PFT}	5	—	—	ns

PROGRAMMING WAVEFORMS



FUJITSU
MICROELECTRONICS

MBM2732-35
MBM2732-45

UV ERASABLE 32,768-BIT READ ONLY MEMORY

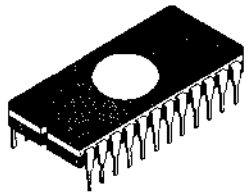
NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MBM2732A.

DESCRIPTION

The Fujitsu MBM2732 is a high speed 32,768-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

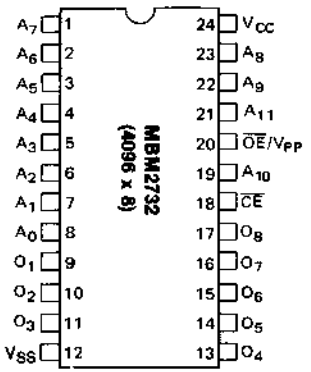
A 24-pin dual-in-line package with a transparent lid is used to package the MBM2732. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2732 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 4096 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERDIP PACKAGE
DIP-24C-C02

PIN ASSIGNMENT

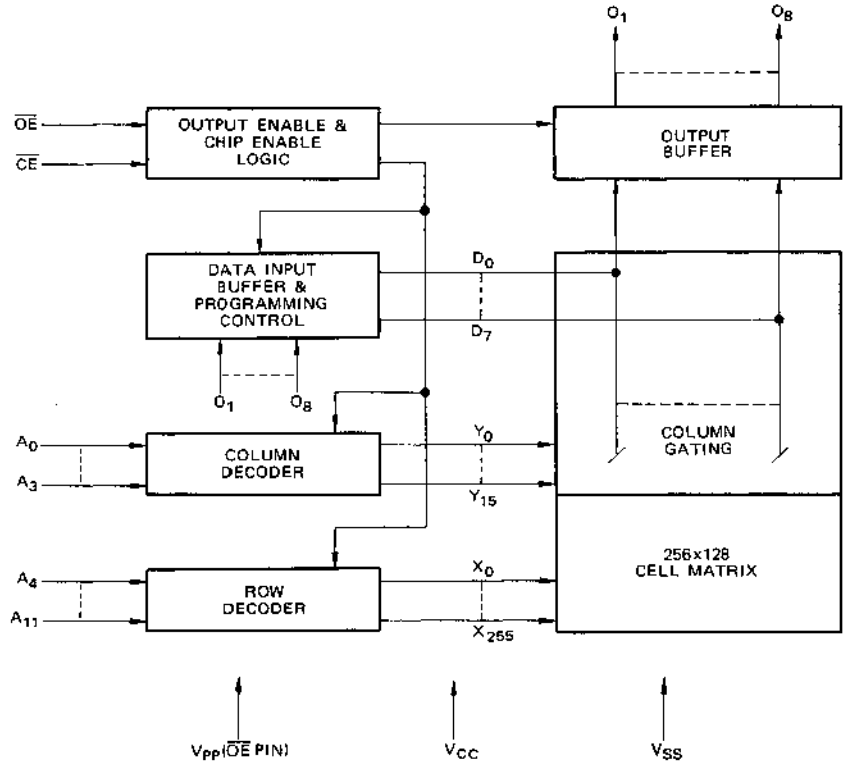


FEATURES

- **4096 words by 8-bits organization, fully decoded**
- **Simple programming requirements**
- **Single location programming**
- **Programs with one 50ms pulse**
- **Low power requirement:**
  825mW max (active)
  165mW max (standby)
- **No clocks required (fully static operation)**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Fast access time:**
  MBM2732-35 350ns
  MBM2732-45 450ns
- **Single +5V operation**
- **Standard 24-pin DIP package**
- **Pin compatible with Intel 2732**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MBM2732 BLOCK DIAGRAM



CAPACITANCE

(T_A = 25°C; f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$, V_{IN} = 0V)	C_{IN1}	—	4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0V)	C_{IN2}	—	14	20	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs (Except $\overline{OE}/V_{PP}$) with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.3 to +7	V
Output Enable/Program Input with Respect to V_{SS}	$\overline{OE}/V_{PP}$	−0.3 to +26.5	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.3 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONS AND PIN CONNECTIONS $V_{CC}(24) = +5$, $V_{SS}(12) = GND$

Mode \ Function (Pin No.)	Address Input (1 ~ 8, 19, 21 ~ 23)	Data I/O (9 ~ 11, 13 ~ 17)	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	I_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	I_{CC2}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	I_{CC1}
Program	A_{IN}	D_{IN}	V_{IL}	V_{PP}	I_{CC2}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	I_{CC2}
Program Inhibit	Don't Care	High Z	V_{IH}	V_{PP}	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter		Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage(1)	MBM2732-35	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	MBM2732-45		4.75	5.0	5.25		
Supply Voltage		V_{SS}	—	GND	—	V	
Input High Voltage		V_{IH}	2.0	—	V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1	—	0.8	V	

Note: (1) V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

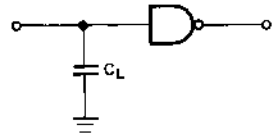
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}	—	—	10	μA
V_{CC} Supply Current (Standby)	I_{CC1}	—	—	30	mA
V_{CC} Supply Current (Active)	I_{CC2}	—	—	150	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Fig. 2 — AC TEST CONDITIONS (Including Programming)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF

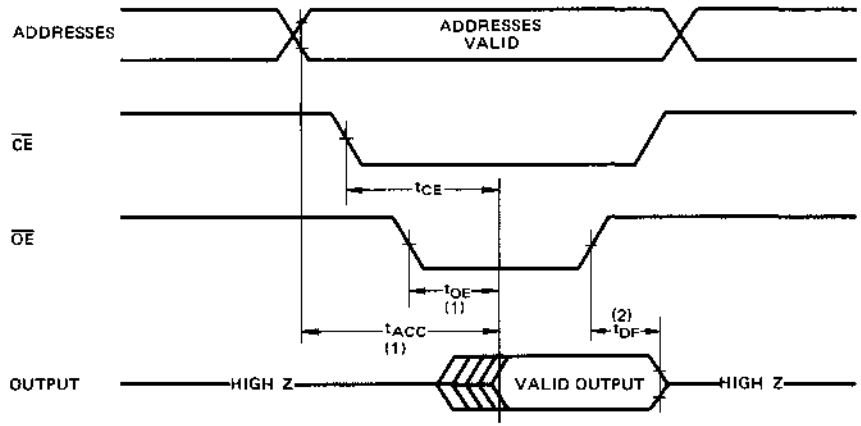


AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM2732-35			MBM2732-45			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{ACC}	—	—	350	—	—	450	ns
Chip Enable to Output Delay	t_{CE}	—	—	350	—	—	450	ns
Output Enable to Output Delay	t_{OE}	—	—	120	—	—	120	ns
Address to Output Hold	t_{OH}	0	—	—	0	—	—	ns
Output Enable High to Output Float	t_{DF}	0	—	100	0	—	100	ns

READ OPERATION TIMING DIAGRAM



Note: (1) $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING/ERASING INFORMATION

Memory Cell Description

The MBM2732 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 14). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 15). In the initial state the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 15.

Fig. 14 — MEMORY CELL

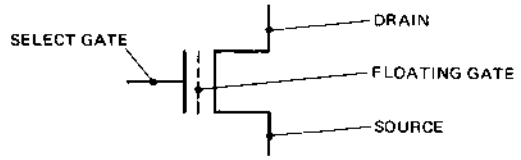
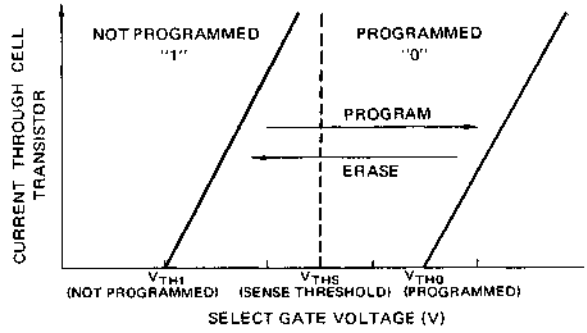


Fig. 15 — MEMORY CELL THRESHOLD SHIFT



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2732 has all 32,768 bits in the "1", or high state. "0's" are loaded into the MBM2732 through the procedure of programming.

The programming mode is entered when +25V is applied to the $\overline{OE}/V_{PP}$ pin. A 0.1μF capacitor between $\overline{OE}/V_{PP}$ and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{CE}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied for each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{CE}$ input is prohibited when programming.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 2732 to an ultraviolet light source. A dosage of 15 W-second/cm² is required to completely erase an MBM2732. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 20 minutes. The MBM2732 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2732 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM2732, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

PROGRAMMING / ERASING INFORMATION (continued)

DC Characteristics

(T_A = 25°C, V_{CC}(1) = 5V ±5%, V_{PP}(1,2) = 25V ± 1V, V_{SS} = GND

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}	—	—	10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{PP})	I_{PP}	—	—	30	mA
V_{CC} Supply Current	I_{CC2}	—	—	150	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IH}	2.0	—	V_{CC} +1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

(2) V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket when V_{PP} = 25 volts. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from V_{IL} to 25 volts or vise-versa.

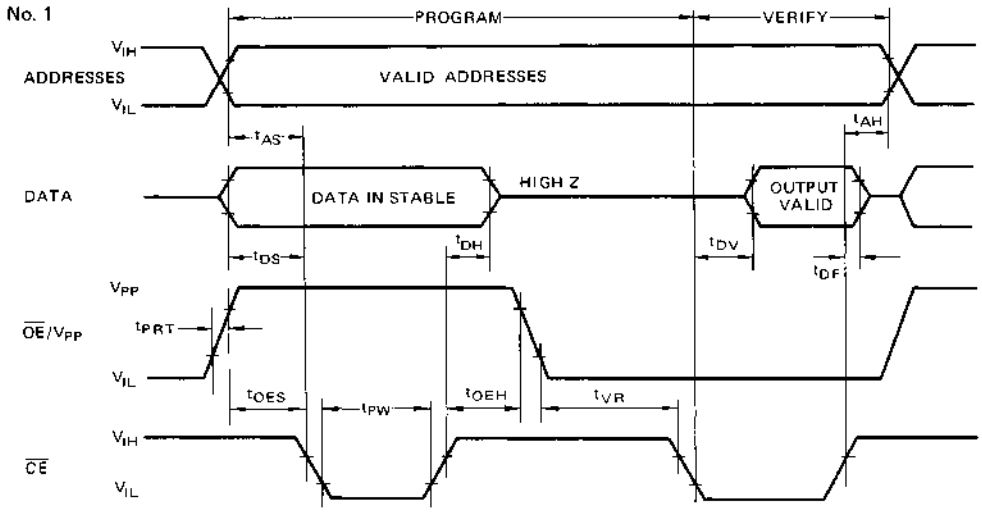
AC Characteristics

(T_A = 25°C)

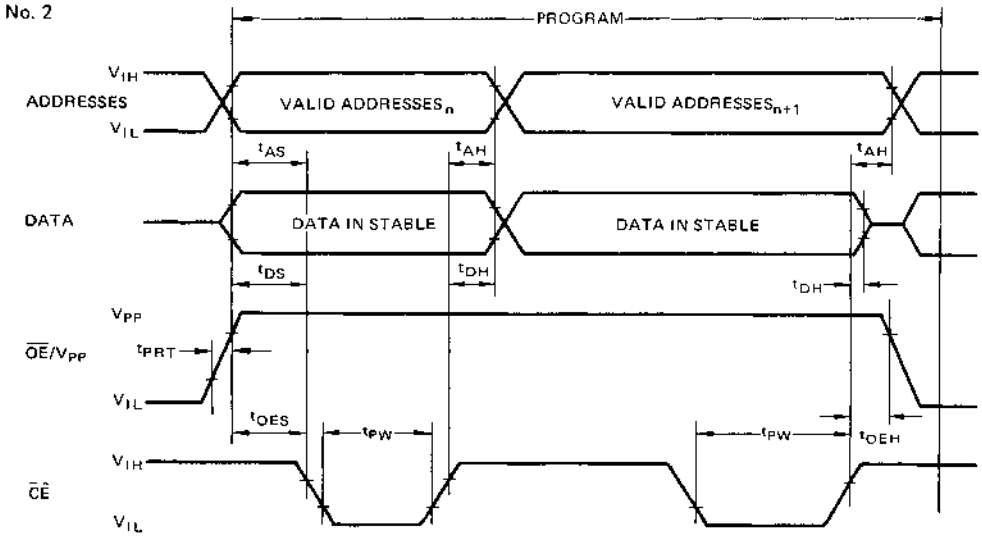
Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
Output Enable Setup Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Output Enable Hold Time	t_{OEH}	2	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Chip Enable to Output Float Delay ($\overline{OE}$ = V_{IL})	t_{DF}	0	—	120	ns
Chip Enable to Data Valid Time ($\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{IL})	t_{DV}	—	—	1	μs
Program Pulse Width	t_{PW}	45	50	55	ms
Program Pulse Rise Time	t_{PRT}	50	—	—	ns
V_{PP} Recovery Time	t_{VR}	2	—	—	μs

PROGRAMMING WAVEFORMS

No. 1



No. 2



Note: In PROGRAMMING WAVEFORMS No. 2, Address Hold Time t_{AH} must be more than 2 μs.

FUJITSU
MICROELECTRONICS

MBM2732A
MBM2732A-X

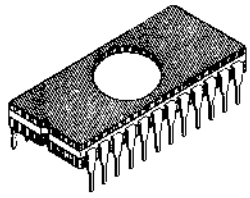
UV ERASABLE 32,768-BIT READ ONLY MEMORY

DESCRIPTION

The Fujitsu MBM2732A is a high speed 32,768-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

The MBM2732A is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 4096 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

A 24-pin dual in-line package with a transparent lid is used to package the MBM2732A. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

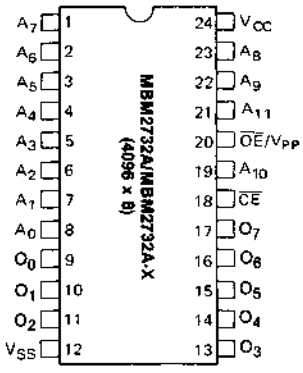


CERDIP PACKAGE
DIP-24C-C02

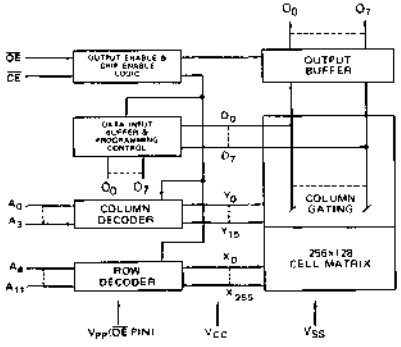
FEATURES

- **Organized as 4096 words by 8-bits, fully decoded**
- **Simple programming requirements**
- **Single location programming**
- **Programs with one 50ms pulse**
- **Programming Voltage:**
  MBM2732A-20/-25/-30: 21 volts
  MBM2732A-35/-35X: 21 or 25 volts
- **Low power requirement:**
  MBM2732A-20/-25/-30:
  Active: 788mW
  Standby: 184mW
  MBM2732A-35/-35X:
  Active: 825mW
  Standby: 165mW
- **Single +5V operation**
- **MBM2732A-35X: Extended temperature range of −40°C to +85°C**
- **TTL compatible inputs and outputs**
- **No clocks required, fully static operation**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Fast Access Time:**
  MBM2732A-20 200 ns max.
  MBM2732A-25 250 ns max.
  MBM2732A-30 300 ns max.
  MBM2732A-35 350 ns max.
  MBM2732A-35X 350 ns max.
- **Standard 24-pin DIP package**
- **Pin compatible with Intel 2732A**

PIN ASSIGNMENT



MBM2732A BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Temperature Under Bias		T_A	−25 to +85	°C
Storage Temperature	MBM2732A-20/-25/-30/-35	T_{stg}	−65 to +125	°C
	MBM2732A-35X		−50 to +95	
Inputs/Outputs (Except $\overline{OE}/V_{PP}$) with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.6 to +7	V
Output Enable/Program Input with Respect to V_{SS}		$\overline{OE}/V_{PP}$	−0.6 to +26	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONS AND PIN CONNECTIONS $V_{CC}(24) = +5$, $V_{SS}(12) = GND$

Mode \ Function (Pin No.)	Address Input (1 – 8, 19, 21 – 23)	Data I/O (9 – 11, 13 – 17)	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	I_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	I_{CC2}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	I_{CC2}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	I_{CC1}
Program	A_{IN}	D_{IN}	V_{IL}	V_{PP}	I_{CC2}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	I_{CC2}
Program Inhibit	Don't Care	High Z	V_{IH}	V_{PP}	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter		Symbol	Min	Typ	Max	Unit	Operating Temperature	
							MBM2732A	MBM2732A-35X
Supply Voltage(1)	-20/-25/-30	V_{CC}	4.75	5.0	5.25	V	0 °C to +70 °C	−40 °C to +85 °C
	-35/-35X		4.5	5.0	5.5			
Supply Voltage		V_{SS}	—	GND	—	V		
Input High Voltage		V_{IH}	2.0	—	$V_{CC}+1$	V		
Input Low Voltage		V_{IL}	−0.1	—	0.8	V		

Note: (1) V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

CAPACITANCE

(T_A = 25 °C; f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$, V_{IN} = 0V)	C_{IN1}	—	4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0V)	C_{IN2}	—	—	20	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

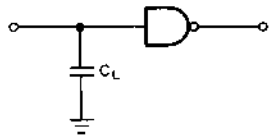
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}	—	—	10	μA
V_{CC} Supply Current (Standby) −20/−25/−30	I_{CC1}	—	—	35	mA
V_{CC} Supply Current (Active)	I_{CC2}	—	—	150	mA
V_{CC} Supply Current (Standby) -35/-35X	I_{CC3}	—	—	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

AC TEST CONDITIONS (Including Programming)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF

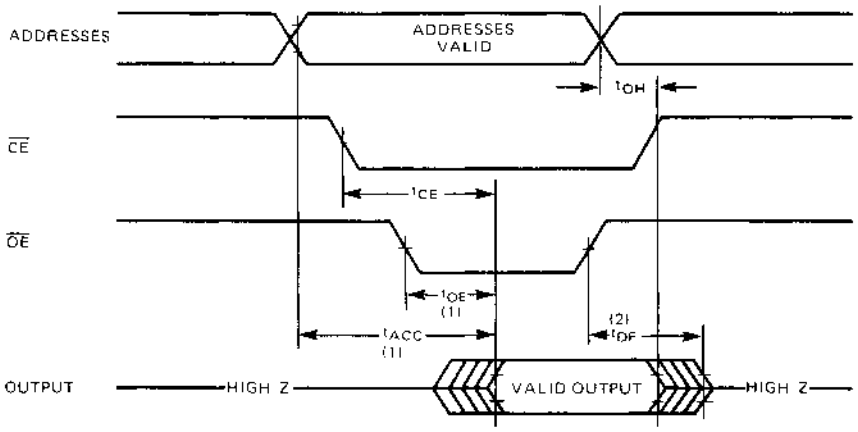


AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM2732A-20		MBM2732A-25		MBM2732A-30		MBM2732A-35 MBM2732A-35X		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}	—	200	—	250	—	300	—	350	ns
Chip Enable to Output Delay	t_{CE}	—	200	—	250	—	300	—	350	ns
Output Enable to Output Delay	t_{OE}	10	70	10	100	10	150	—	120	ns
Address to Output Hold	t_{OH}	0	—	0	—	0	—	0	—	ns
Output Enable High to Output Float	t_{DF}	0	60	0	90	0	130	0	100	ns

OPERATION TIMING DIAGRAM



Note: (1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING/ERASING INFORMATION

Memory Cell Description

The MBM2732A is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Fig. 1 — MEMORY CELL

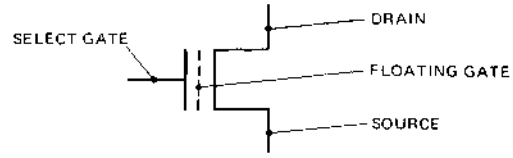
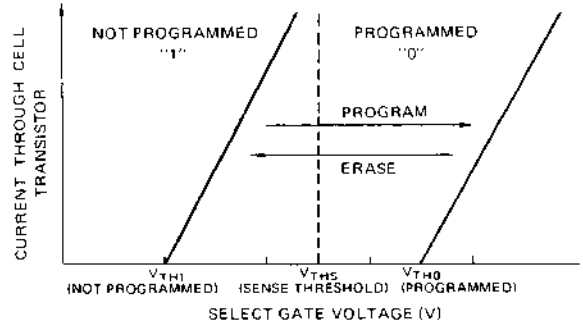


Fig. 2 — MEMORY CELL THRESHOLD SHIFT



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2732A has all 32,768 bits in the "1", of high, state. "0's" are loaded into the MBM2732A through the procedure of programming.

For MBM2732A-20/-25/-30, the programming mode is entered when +21V is applied to the $\overline{OE}/V_{PP}$ pin. For MBM2732A-35/-35X, the programming mode is entered when +25V or +21V is applied to the $\overline{OE}/V_{PP}$ pin. A 0.1μF capacitor between $\overline{OE}/V_{PP}$ and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL Low-level pulse is applied to the $\overline{CE}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{CE}$ input is prohibited when programming.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2732A to an ultraviolet light source. A dosage of 15 W-second/cm^2 is required to completely erase an MBM2732A. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM2732A should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2732A and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM2732A, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

PROGRAMMING / ERASING INFORMATION (continued)

DC Characteristics

(T_A = 25 ±3°C, V_{CC}(1) = 5V ±5%, V_{PP} = 21V ±0.5V, V_{SS} = 0V) **(For MBM2732A-35/-35X: V_{PP} = 21V or 25V)**

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}	—	—	10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{PP})	I_{PP}	—	—	30	mA
V_{CC} Supply Current	I_{CC2}	—	—	150	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IH}	2.0	—	V_{CC} +1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

(2) V_{PP} must not be greater than 21.5 volts (26.5 Volts for MBM2732A-35/-35X) including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = (21 volts for MBM2732A-20/-25/-30, 21 volts or 25 volts for MBM2732A-35/-35X). Also, during $\overline{CE}$, $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{IL} to V_{PP} volts or vise-versa.

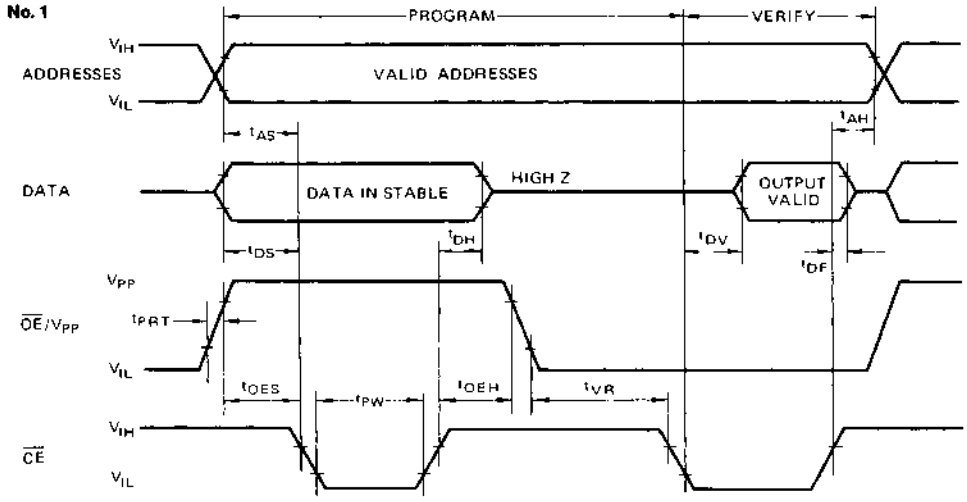
AC Characteristics

(T_A = 25 ± 3°C, V_{CC}(1) = 5V ±5%, V_{PP} = 21V ±0.5V) **(21V ± 0.5V or 25V ± 0.5V for MBM2732A-35/-35X)**

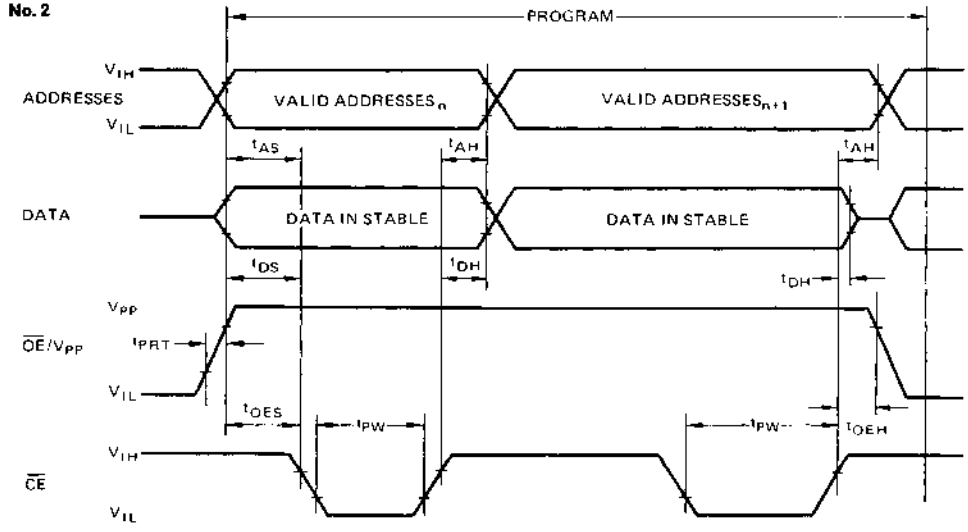
Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
Output Enable Setup Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Output Enable Hold Time	t_{OEH}	2	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Chip Enable to Output Float Delay ($\overline{OE}$ = V_{IL})	t_{DF}	0	—	130	ns
Chip Enable to Data Valid Time ($\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{IL})	t_{DV}	—	—	1	μs
Program Pulse Width	t_{PW}	45	50	55	ms
Program Pulse Rise Time	t_{PRT}	50	—	—	ns
V_{PP} Recovery Time	t_{VR}	2	—	—	μs

PROGRAMMING WAVEFORMS

No. 1



No. 2



Note: In PROGRAMMING WAVEFORMS No. 2, Address Hold Time t_{AH} must be more than 2 μs.

FUJITSU
MICROELECTRONICS

MBM27C32-25
MBM27C32-30

CMOS 32,768-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

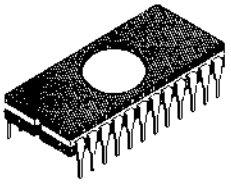
ADVANCE INFORMATION

DESCRIPTION

The Fujitsu MBM27C32 is a high speed 32,768-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential.

A 24-pin dual in-line package with a transparent lid is used to package the MBM27C32. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C32 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 4096 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

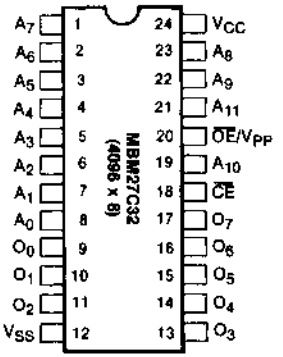


CERDIP PACKAGE
DIP-24C-C02

FEATURES

- **CMOS Power Consumption:**
  500μW max. (Standby)
  40mW/MHz (Active)
- **Organized as 4096 words by 8-bits, fully decoded**
- **Utilizes the same simple programming requirements as MBM2732A**
- **Single location programming**
- **Programming pulse may be reduced to 25 ns to cut programming time in half**
- **No clock required, fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin simplifies memory expansion**
- **Fast Access Time:**
  MBM27C32-25 250 ns max.
  MBM27C32-30 300 ns max.
- **Single +5V operation**
- **Jedec standard 24-pin DIP package**
- **Pin and function compatible with 2732A-type devices**

PIN ASSIGNMENT



THIS IS PRELIMINARY INFORMATION FOR A NEW PRODUCT TO BE INTRODUCED DURING 1982. THIS IS NOT A FINAL SPECIFICATION. PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU
MICROELECTRONICS

NMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

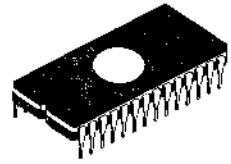
MBM2764-20
MBM2764-25
MBM2764-30
MBM2764-30X

DESCRIPTION

The Fujitsu MBM2764 is a high-speed 65,536-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package with a transparent lid is used to package the MBM2764. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2764 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERDIP PACKAGE
DIP-28C-C01

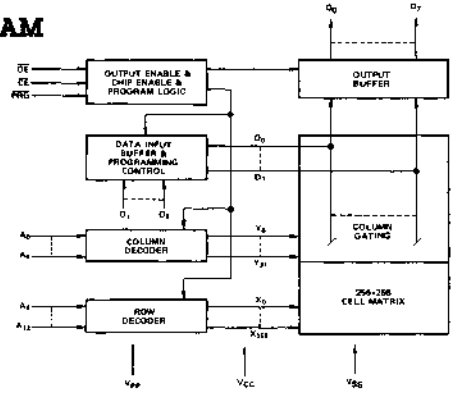
FEATURES

- **Organized as 8,192 words by 8-bits, fully decoded**
- **Fast Access Time:**

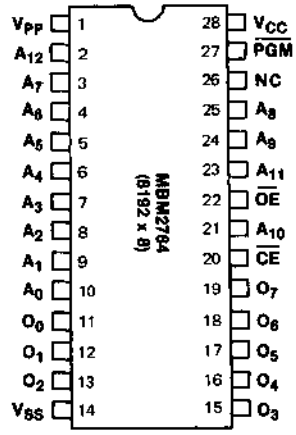
MBM2764-20	**200 ns**
MBM2764-25	**250 ns**
MBM2764-30	**300 ns**
MBM2764-30X	**300 ns**

- **Simple programming requirements**
- **Single location programming**
- **Programs with one 50 mS pulse**
- **Low power requirement:**
  788mW active
  184mW standby
- **Extended temperature range: MBM2764-30X: −40°C to +85°C**
- **No clocks required, Fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Single +5V Operation**
- **Standard 28-pin DIP package**
- **Pin compatible with Intel 2764**

MBM2764 BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Temperature Under Bias	MBM2764-20/-25/30	T_A	−25 to +85	°C
	MBM2764-30X		−50 to +95	
Storage Temperature		T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}		V_{PP}	−0.6 to +26.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

FUNCTIONS AND PIN CONNECTIONS V_{CC} (28) = +5, V_{SS} (14) = GND

Function (Pin No.) / Mode	Address Input (2 ~ 10,21,23 ~ 25)	Data I/O (11 ~ 13,15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$[1] (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	Don't Care	I_{CC2}	V_{CC}
				Don't Care	V_{IL}		
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{CC}
Program	A_{IN}	$\overline{D}_{IN}$	V_{IL}	Don't Care	V_{IL}	I_{CC2}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{PP}

Note: 1. $\overline{PGM}$ works as if $\overline{OE}$ (output enable) during reading operation. ($V_{PP} = V_{CC}$).

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Ouput Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature	
						MBM2764-20/-25/-30	MBM2764-30X
Supply Voltage[2]	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C	−40°C to +85°C
Supply Voltage	V_{PP}	V_{CC} − 0.6	—	V_{CC} + 0.6	V		
Supply Voltage	V_{SS}	—	GND	—	V		
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 1	V		
Input Low Voltage	V_{IL}	−0.1	—	0.8	V		

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Symbol	Min	Max	Unit
Input Load Current	$V_{IN} = 5.25V$	I_{LI}	—	10	μA
Output Leakage Current	$V_{OUT} = 5.25V$	I_{LO}	—	10	μA
V_{PP} Supply Current	$V_{PP} = V_{CC} \pm 0.6V$	I_{PP}	—	15	mA
V_{CC} Standby Current	$\overline{CE} = V_{IH}$	I_{CC1}	—	35	mA
V_{CC} Supply Current (Active)	$\overline{CE} = V_{IL}$	I_{CC2}	—	150	mA
Input Low Voltage	—	V_{IL}	−0.1	+0.8	V
Input High Voltage	—	V_{IH}	2.0	$V_{CC}+1$	V
Output Low Voltage	$I_{OL} = 2.1mA$	V_{OL}	—	0.45	V
Output High Voltage	$I_{OH} = -400\mu A$	V_{OH}	2.4	—	V

AC CHARACTERISTICS

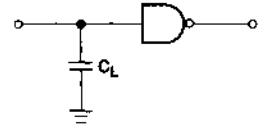
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM2764-20		MBM2764-25		MBM2764-30 MBM2764-30X		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}	10	70	10	100	10	150	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0	60	0	90	0	130	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0	—	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

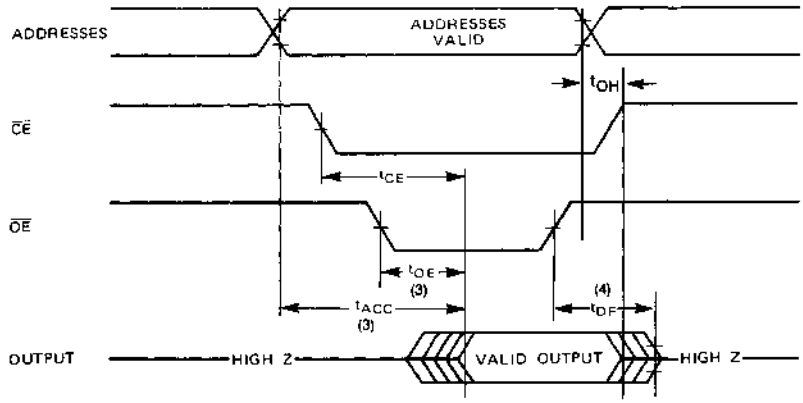
AC TEST CONDITIONS

Input Pulse levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤ 20nsec
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
1 TTL gate and $C_L = 100$ pF

Output Load:



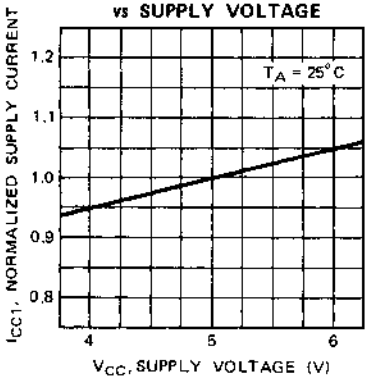
OPERATION TIMING DIAGRAM



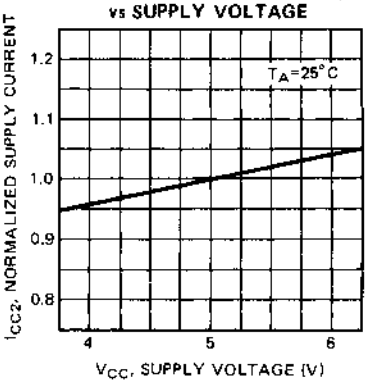
Notes: 3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

TYPICAL CHARACTERISTICS CURVES

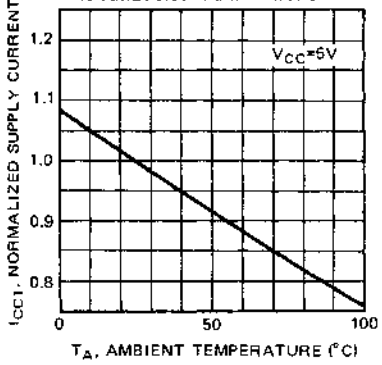
SUPPLY CURRENT (STANDBY) vs SUPPLY VOLTAGE



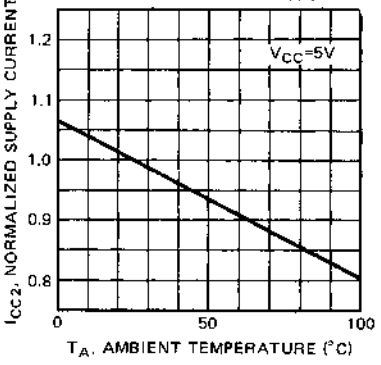
SUPPLY CURRENT (ACTIVE) vs SUPPLY VOLTAGE



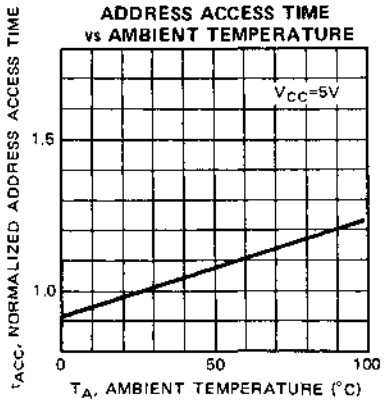
SUPPLY CURRENT (STANDBY) vs AMBIENT TEMPERATURE



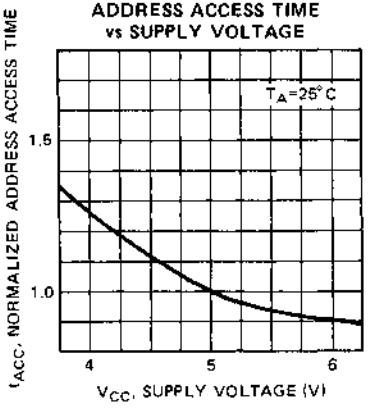
SUPPLY CURRENT (ACTIVE) vs AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

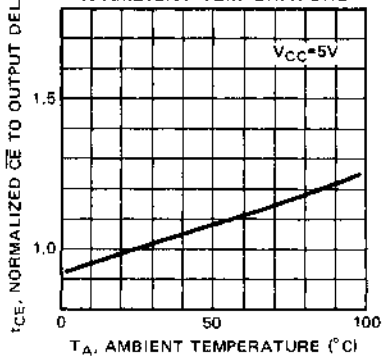


ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

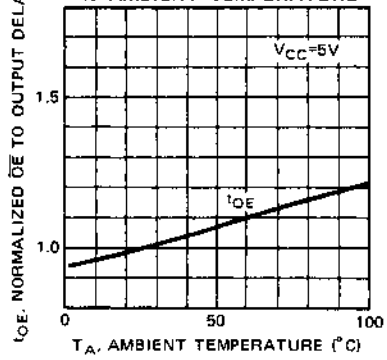


TYPICAL CHARACTERISTICS CURVES (Continued)

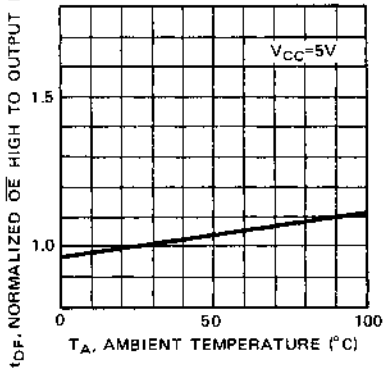
$\overline{CE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE



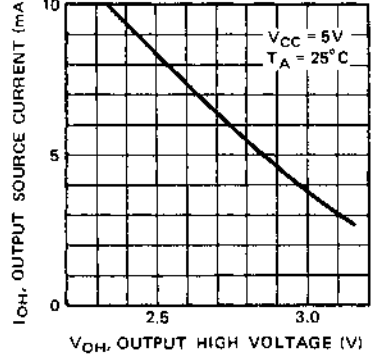
$\overline{OE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE



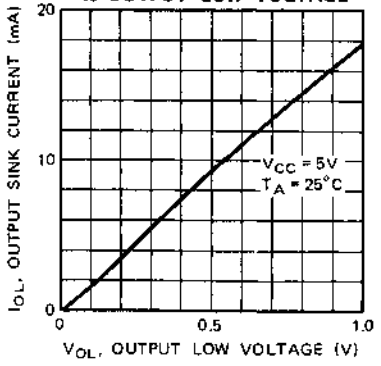
$\overline{OE}$ HIGH TO OUTPUT FLOAT vs AMBIENT TEMPERATURE



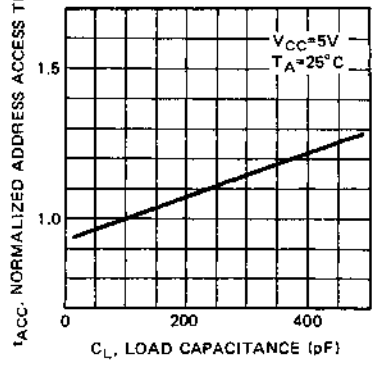
OUTPUT SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



OUTPUT SINK CURRENT vs OUTPUT LOW VOLTAGE



ADDRESS ACCESS TIME vs LOAD CAPACITANCE



PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM2764 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Fig. 1 — MEMORY CELL

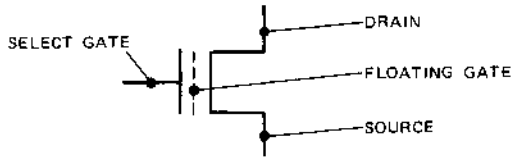
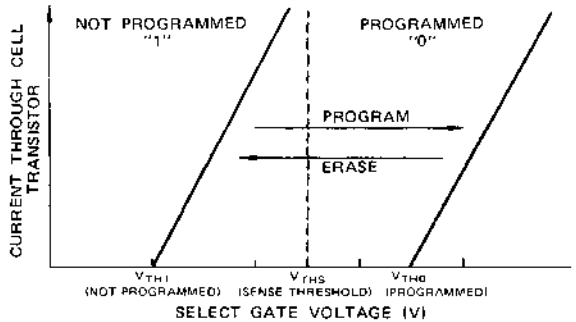


Fig. 2 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2764 has all 65536 bits in the "1" or high state. "0's" are loaded into the MBM2764 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the $\overline{PGM}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2764 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM2764. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2 for 15 to 20 minutes. The MBM2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2764 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM2764 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING/ERASING INFORMATION (Continued)

DC CHARACTERISTICS

(T_A = 25 ±3°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V)

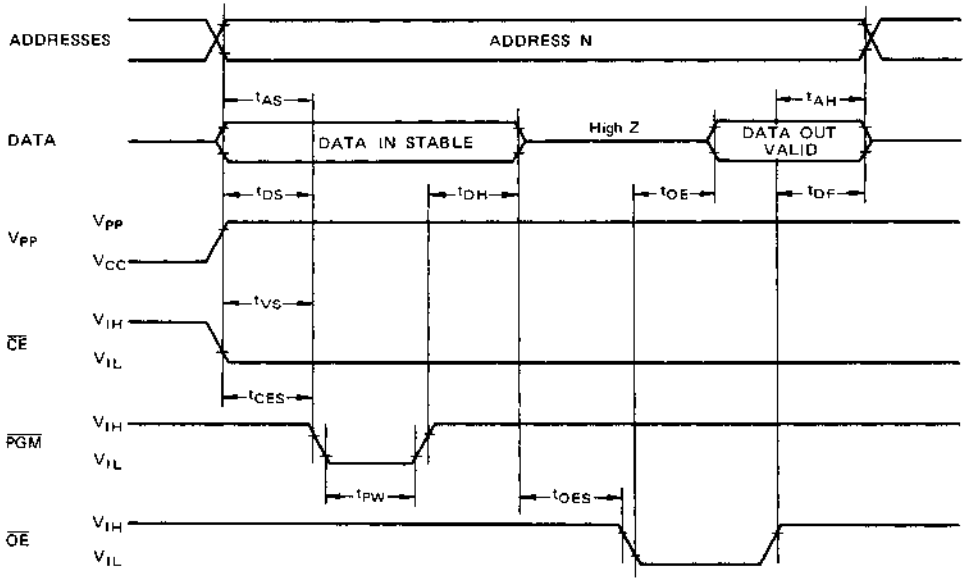
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 0.45V~5.25V
Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = −400μA
V_{CC} Supply Current	I_{CC2}	—	150	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} +1	V	—
V_{PP} Supply Current	I_{PP}	—	30	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

AC CHARACTERISTICS

(T_A = 25 ±3°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
$\overline{CE}$ Setup Time	t_{CES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Chip Enable to Output Float Delay	t_{DF}	—	—	130	ns
V_{PP} Setup Time	t_{VS}	2	—	—	μs
$\overline{PGM}$ Pulse Width	t_{PW}	45	50	55	ms
$\overline{OE}$ Setup Time	t_{OES}	2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}	—	—	150	ns

PROGRAMMING WAVEFORM



FUJITSU
MICROELECTRONICS

MBM27C64-25
MBM27C64-30

CMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

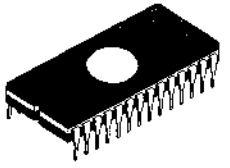
PRELIMINARY

DESCRIPTION

The Fujitsu MBM27C64 is a high speed 65,536-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential. The device dissipates only 40 mW/MHz when active, typically 5μW when in standby, yet it provides the same high performance as the NMOS MBM2764-type devices.

A 28-pin dual in-line package with a transparent lid is used to package the MBM27C64. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

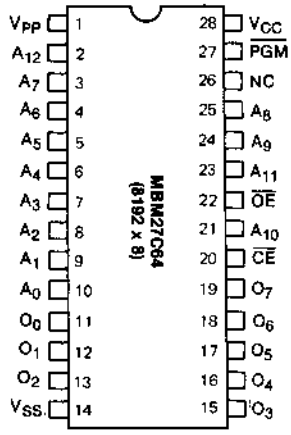


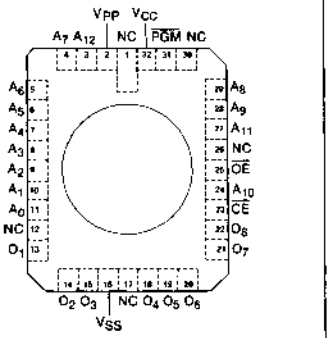
CERDIP PACKAGE
DIP-28C-C01
ALSO AVAILABLE IN 32-PAD
CERAMIC LEADLESS CHIP CARRIER
LCC-32C-A01

FEATURES

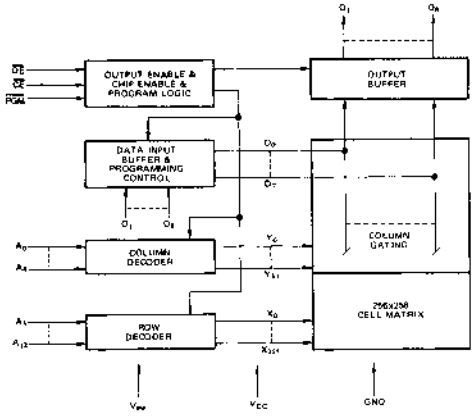
- **CMOS Power Consumption:**
  500μW max. (Standby)
  5μW typ. (Standby)
  40mW/MHz (Active)
- **Organized as 8192 words by 8-bits, fully decoded**
- **Utilizes the same simple programming requirements as MBM2764**
- **Single location programming**
- **Programming pulse may be reduced to 25 ns to cut programming time in half**
- **No clock required, fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin simplifies memory expansion**
- **Fast Access Time:**
  MBM27C64-25 250 ns max.
  MBM27C64-30 300 ns max.
- **Single +5V operation**
- **Jedec standard 28-pin DIP package**
- **Pin and function compatible with 2764-type devices**

PIN ASSIGNMENTS





MBM27C64 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}	V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONS AND PIN CONNECTIONS (V_{CC}(28) = +5, V_{SS}(14) = GND)

Function (Pin No.) / Mode	Address Input (2 ~ 10, 21, 23 ~ 25)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC1}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	Don't Care	I_{CC1}	V_{CC}
				Don't Care	V_{IL}		
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{SB1}	V_{CC}
Program	A_{IN}	D_{IN}	V_{IL}	Don't Care	V_{IL}	I_{CC1}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC1}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{SB1}	V_{PP}

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage[1]	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} +0.6	V	
Supply Voltage	V_{SS}	—	GND	—	V	
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

Note: 1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

PRELIMINARY

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current	I_{PP1}	—	1	100	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}	—	—	1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC} −0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}	—	1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL})	I_{CC1}	—	—	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}	—	—	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

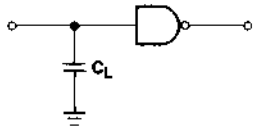
Parameter	Symbol	MBM27C64-25		MBM27C64-30			Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	t_{ACC}	—	—	250	—	—	300	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	t_{CE}	—	—	250	—	—	300	ns
$\overline{OE}$ to Output Delay ($\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	t_{OE}	10	—	100	10	—	150	ns
$\overline{PGM}$ to Output Delay ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{PGM}	10	—	100	10	—	150	ns
Output Enable High to Output Float (See Note)	t_{DF}	0	—	90	0	—	130	ns
Address to Output Hold	t_{OH}	0	—	—	0	—	—	ns

Note: t_{DF} is specified from $\overline{CE}$, $\overline{OE}$, or $\overline{PGM}$, whichever occurs first.

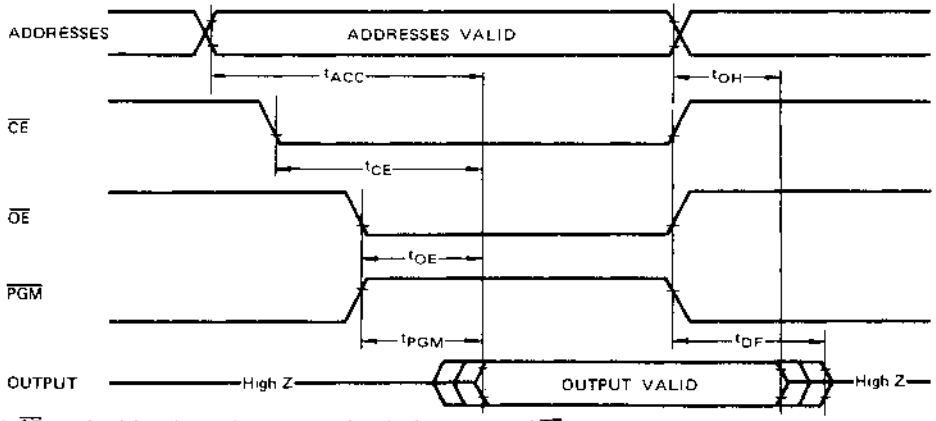
AC TEST CONDITIONS

Input Pulse levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤ 20nsec
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
1 TTL gate and C_L = 100 pF

Output Load:



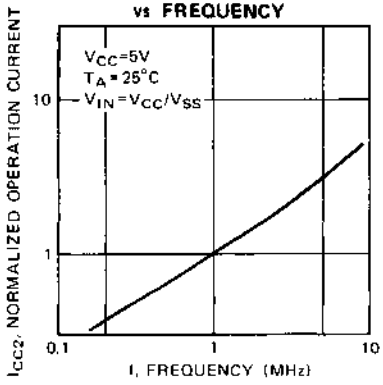
OPERATION TIMING DIAGRAM



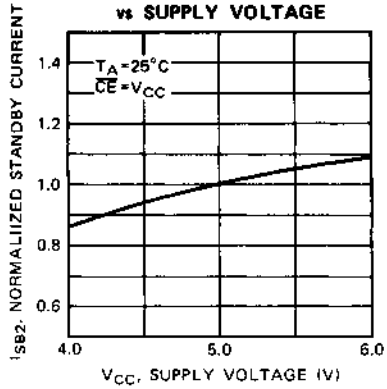
Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

TYPICAL CHARACTERISTICS CURVES

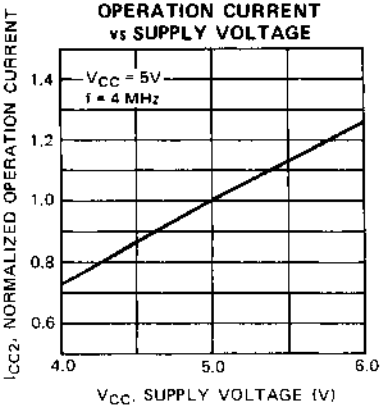
OPERATION CURRENT vs FREQUENCY



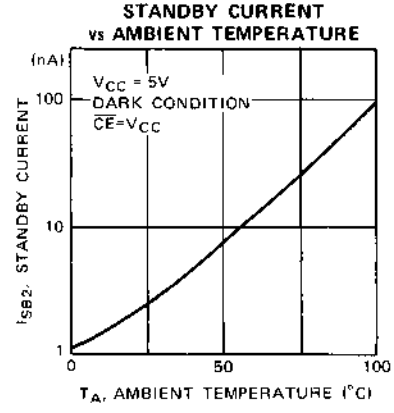
STANDBY CURRENT vs SUPPLY VOLTAGE



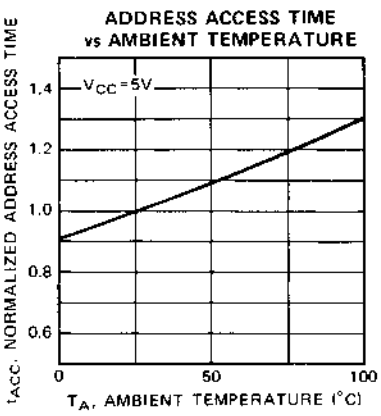
OPERATION CURRENT vs SUPPLY VOLTAGE



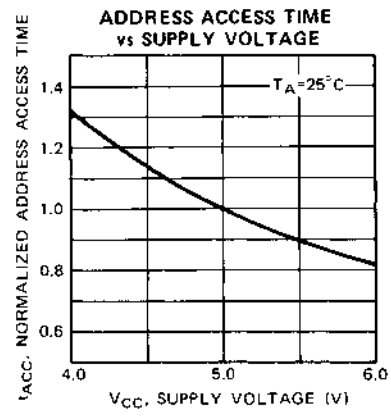
STANDBY CURRENT vs AMBIENT TEMPERATURE



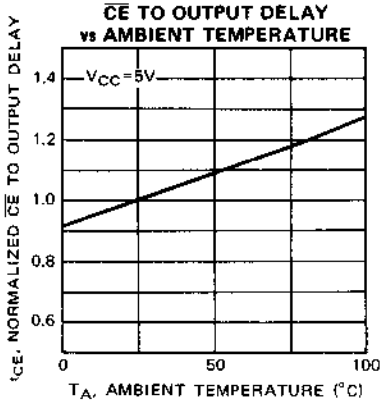
ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

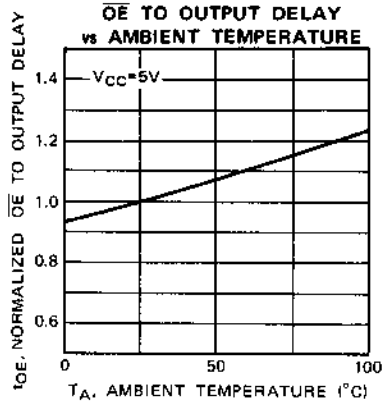


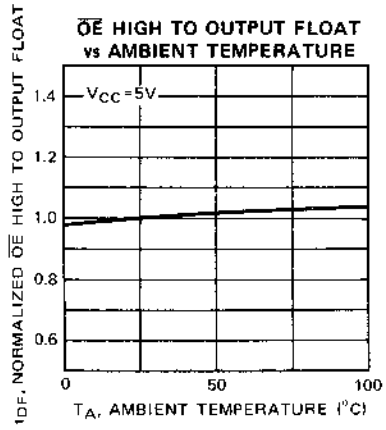
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

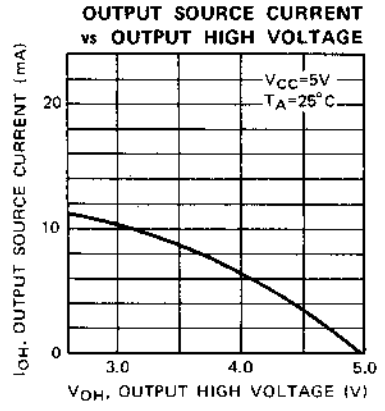


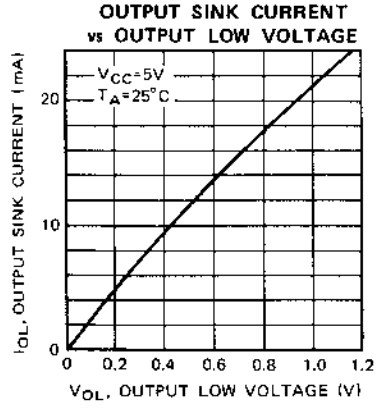
TYPICAL CHARACTERISTICS CURVES (Continued)

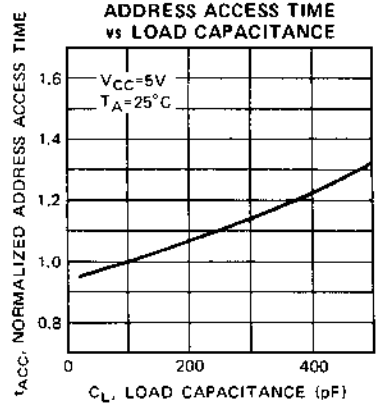












PROGRAMMING / ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Fig. 1 — MEMORY CELL

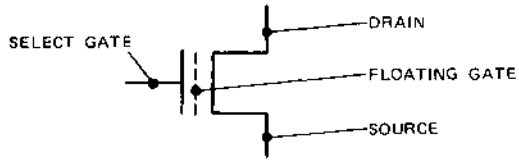
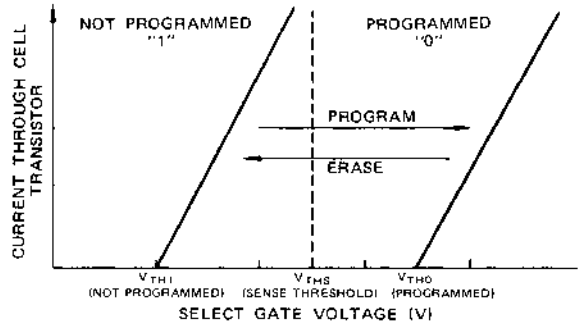


Fig. 2 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1" or high state. "0's" are loaded into the MBM27C64 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and CE and PGM are both at V_{IL}. During programming, CE is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the PGM input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2) for 15 to 20 minutes. The MBM27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C64 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

PROGRAMMING/ERASING INFORMATION (Continued)

DC CHARACTERISTICS

(T_A = 25 ±3°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 0.45V–5.25V
Output Low Voltage During Verify	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage During Verify	V_{OH}	2.4	—	V	I_{OH} = −400μA
V_{CC} Supply Current	I_{CC1}	—	30	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} +0.3	V	—
V_{PP} Supply Current During Progamming Pulse	I_{PP2}	—	30	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Note: 1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

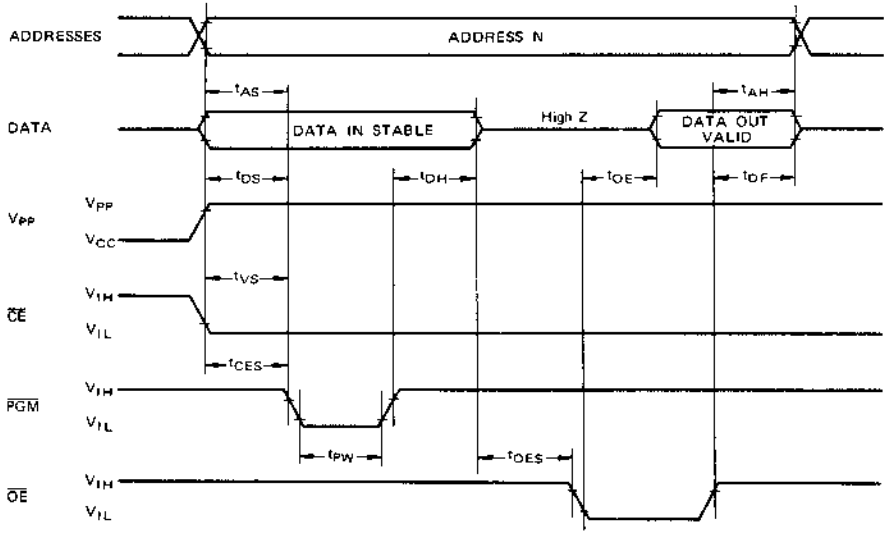
2. V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25 ±3°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
$\overline{CE}$ Setup Time	t_{CES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Chip Enable to Output Float Delay	t_{DF}	0	—	130	ns
V_{PP} Setup Time	t_{VS}	2	—	—	μs
$\overline{PGM}$ Pulse Width	t_{PW}	25	50	55	ms
$\overline{OE}$ Setup Time	t_{OES}	2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}	—	—	150	ns

PROGRAMMING WAVEFORM



BIPOLAR RAMS

BIPOLAR RAMS

QUICK GUIDE TO PRODUCTS IN THIS SECTION

Device	Technology	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB7072E	ECL	256 x 4	12nS	−5.2	1040mW	22-pin	5-2
MBM10415AH	ECL	1K x 1	20nS	−5.2	780mW	16-pin	5-7
MBM10422	ECL	256 x 4	10nS	−5.2	1040mW	24-pin	5-12
MBM10422A-7	ECL	256 x 4	7nS	−5.2	1040mW	24-pin	5-17
MBM10470A-20	ECL	4K x 1	20nS	−5.2	1040mW	18-pin	5-18
MBM10474	ECL	1K x 4	25nS	−5.2	1040mW	24-pin	5-23
MBM10474A-15	ECL	1K x 4	15nS	−5.2	1040mW	24-pin	5-28
MBM10480	ECL	16K x 1	20nS	−5.2	700mW	20-pin	5-29
MBM93419	TTL	64 x 9	45nS	+5	1000mW	28-pin	5-30
MBM100422	ECL	256 x 4	10nS	−4.5	900mW	24-pin	5-34
MBM100422A-7	ECL	256 x 4	7nS	−4.5	900mW	24-pin	5-39
MBM100470	ECL	4K x 1	20nS	−4.5	900mW	24-pin	5-40
MBM100474-15	ECL	1K x 4	15nS	−4.5	900mW	24-pin	5-45

FUJITSU
MICROELECTRONICS

MB7072E

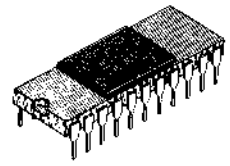
ECL 256 X 4-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MB7072 is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The MB7072 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production. Operation for the MB7072 is specified over a temperature range of 0°C to 75°C (ambient).

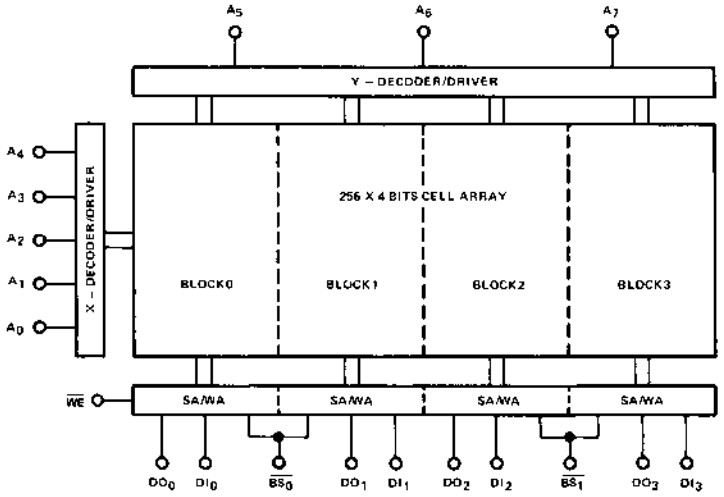
FEATURES

- **Organized as 256 words by 4-bits**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry standard 10K-series ECL families**
- **Address Access Time: MB7072E 12ns Max.**
- **DOPOS and IOP Processing**
- **Two block select pins for flexibility in organization**

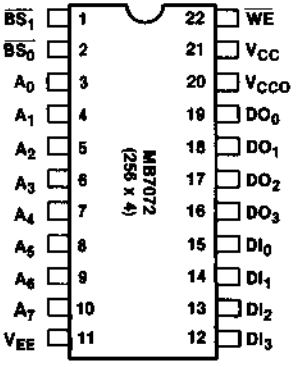


CERAMIC PACKAGE
DIP-22C-F01

Fig. 1-MB7072E BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DO	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−25 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in operational sections of this data sheet.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{EE})			Ambient Temperature
	Min	Typ	Max	
MB7072 E	−5.46V	−5.2V	−4.94V	0°C to 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
*Input Pin Capacitance	C_{IN}	—	—	8	pF
Output Pin Capacitance	C_{OUT}	—	—	8	pF

*$\overline{BS}$ Capacitance = 12pF (max)

DC CHARACTERISTICS

($V_{CC} = V_{CCO} = 0V, V_{EE} = -5.2V$, Output Load = 50Ω to −2.0V, with transverse airflow ≥ 2.5 m/s, unless otherwise noted.)

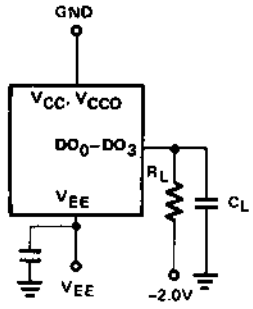
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IHmax}$ or V_{ILmin})	V_{OH}	−1000 −960 −900	— — —	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{INmax}$ or V_{ILmin})	V_{OL}	−1870 −1850 −1830	— — —	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax})	V_{OHC}	−1020 −980 −920	— — —	— — —	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax}	V_{OLC}	— — —	— — —	−1645 −1630 −1606	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	— — —	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	— — —	−1490 −1475 −1450	mV	0°C 25°C 75°C
*Input High Current ($V_{IN} = V_{IHmax}$)	I_{IH}	—	—	220	μA	0° to 75°C
**Input Low Current ($V_{IN} = V_{ILmin}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	−200	—	—	mA	0° to 75°C

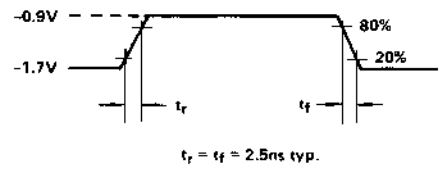
*$\overline{BS}$ Input High Current = 300μA (max)
**$\overline{BS}$ Input Low Current = 240μA (max)

AC CHARACTERISTICS

(V_{CC} = V_{CCO} = 0V, V_{EE} = −5.2V ±5%, T_A = 0° to +75°C with transverse airflow ≥ 2.5 m/s, Output Load = 50Ω to −2V and 15 pF to GND, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





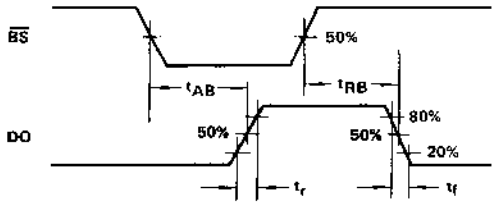
t_r = t_f = 2.5ns typ.

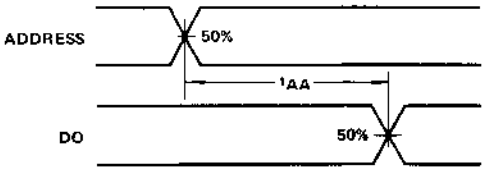
OUTPUT LOAD: R_L = 50Ω
C_L = 15 pF
(INCLUDING JIG AND STRAY CAPACITANCE)

READ CYCLE

Parameter	Symbol	MB7072E			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	—	—	12	ns
Block Select Access Time	t_{AB}	—	3.0	5.0	ns
Block Select Recovery Time	t_{RB}	—	3.0	5.0	ns

READ CYCLE

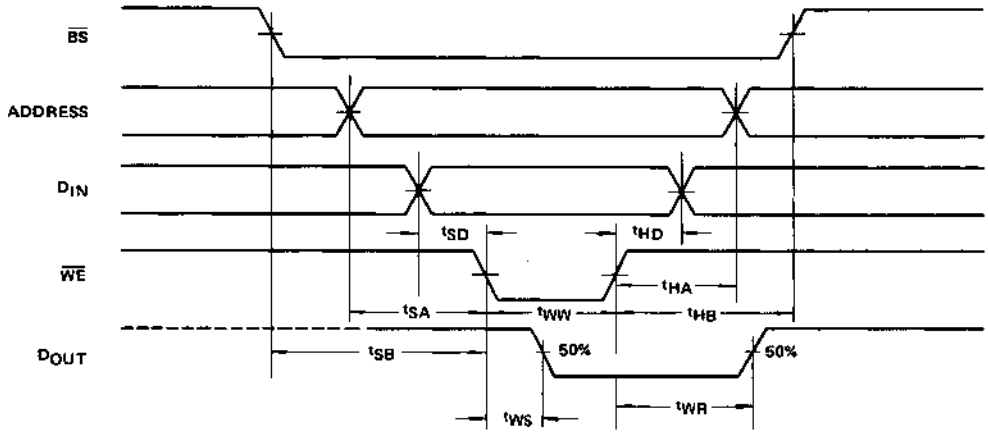




WRITE CYCLE

Parameter	Symbol	MB7072E			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	9.0	5.5	—	ns
Write Recovery Time	t_{WR}	—	6.0	9.0	ns
Write Disable Time	t_{WS}	—	3.0	5.0	ns
Address Set Up Time	t_{SA}	3.0	—	—	ns
Block Select Set Up Time	t_{SB}	2.0	—	—	ns
Data Set Up Time	t_{SD}	2.0	—	—	ns
Address Hold Time	t_{HA}	2.0	—	—	ns
Block Select Hold Time	t_{HB}	2.0	—	—	ns
Data Hold Time	t_{HD}	2.0	—	—	ns

WRITE CYCLE



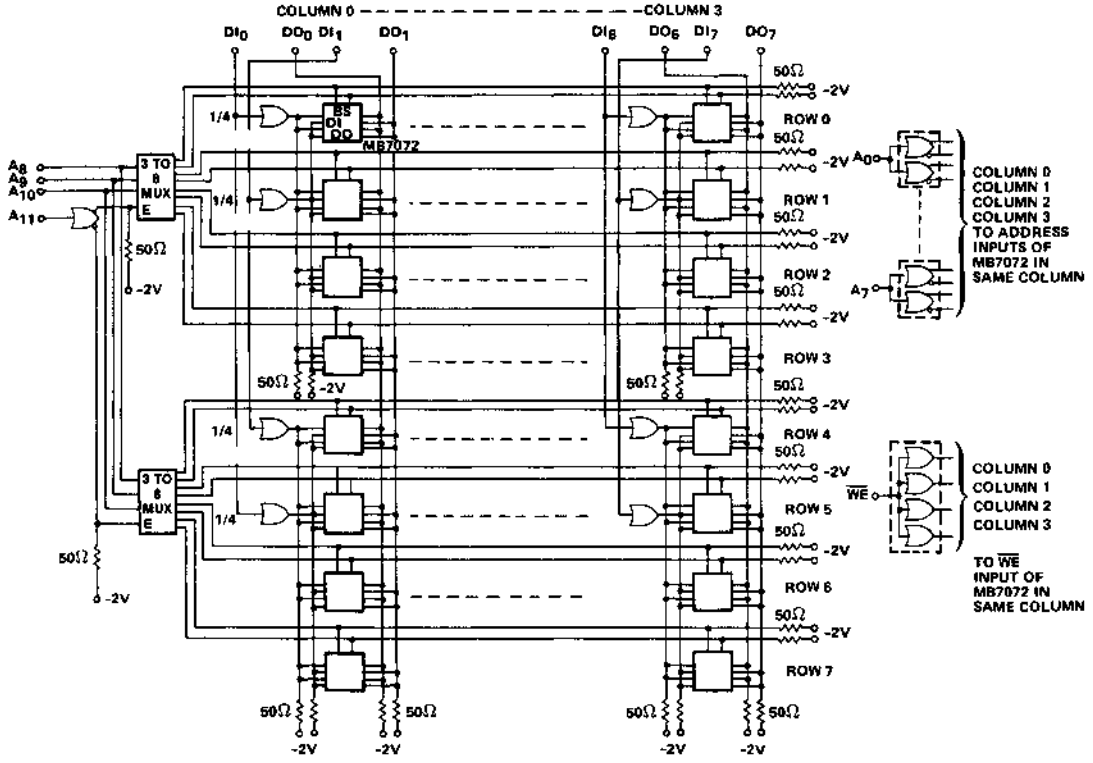
RISE TIME AND FALL TIME

Parameter	Symbol	MB7072E			Unit
		Min	Typ	Max	
Ouput Rise Time	t_r	—	3.0	—	ns
Output Fall Time	t_f	—	3.0	—	ns

APPLICATION INFORMATION

The Fujitsu MB7072E is a fully decoded 256 word by 4-bits ECL memory. High speed makes them ideally suited to mainframe applications, including cache and microprogram control. Figure 3 illustrates one application; a 4K word x 8-bit memory. As with all ECL memory systems, extreme care must be taken in PC board layout and bussing to minimize reflections and crosstalk.

Fig. 3 — 4K WORD X 8-BIT MEMORY SYSTEM



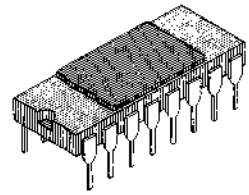
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10415AH is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. It is organized as 1024 words by one bit, and features on-chip voltage compensation for improved noise margin.

The MBM10415AH offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10415AH is specified over a temperature range of from 0 °C 75 °C (ambient). It also features frit-sealed 16-pin dual in-line packaging, and is fully compatible with industry-standard 10K-series ECL families.

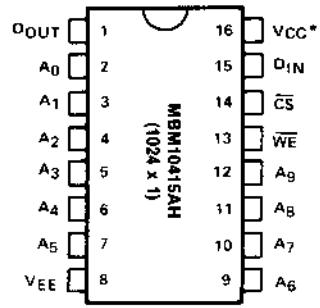


CERAMIC PACKAGE
DIP-16C-F01

FEATURES

- **1024 words x 1-bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time:**
  MBM10415AH: 20 ns Max.
- **Chip select access time:**
  MBM10415AH: 8 ns Max.
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.5mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with F10415 and MCM10146**

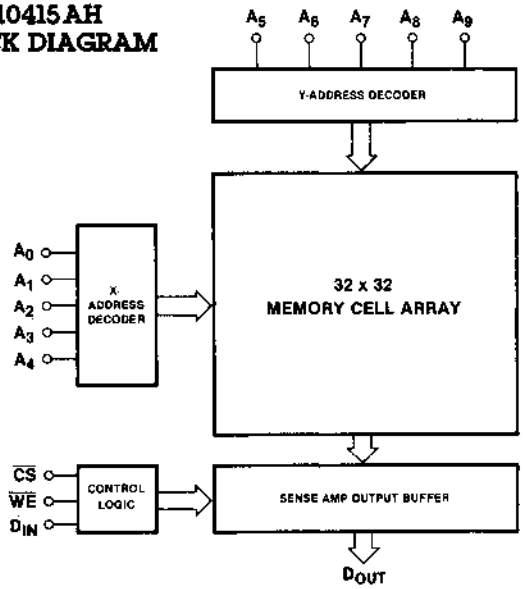
PIN ASSIGNMENT



*V_{CC} grounded

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM10415AH BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	L	L	WRITE "L"
L	L	H	L	WRITE "H"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	7	8	pF

DC CHARACTERISTICS

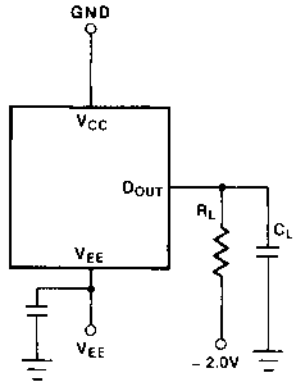
(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V and Airflow ≥ 2.5 m/s unless otherwise noted.)

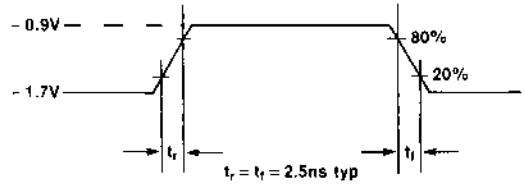
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−125 −150	—	—	mA	75°C 0°C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pf to GND and Airflow ≥ 2.5 m/s unless otherwise noted.)

AC TEST CONDITIONS





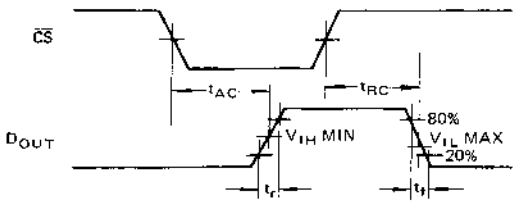
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

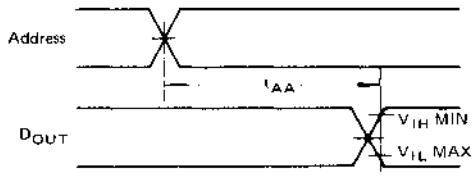
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10415AH		Unit
		Typ	Max	
Address Access Time	t_{AA}	13	20	ns
Chip Select Access Time	t_{AC}	5	8	ns
Chip Select Recovery Time	t_{RB}	5	8	ns

READ CYCLE

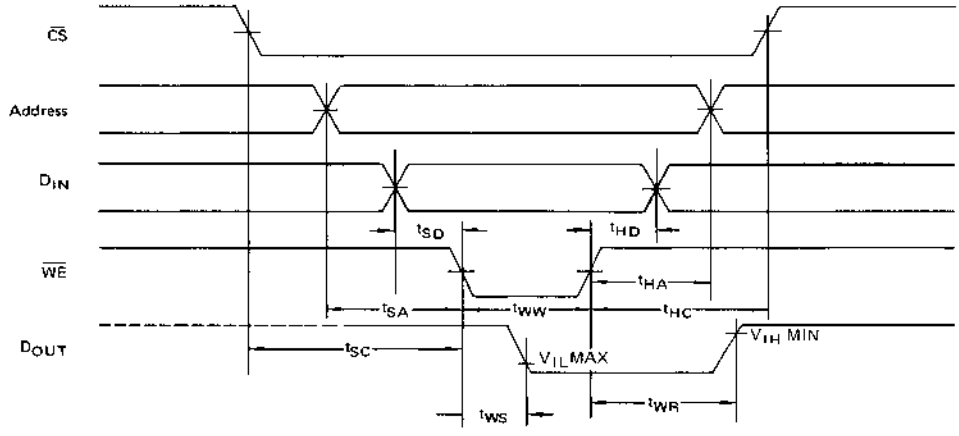




WRITE CYCLE

Parameter	Symbol	MBM10415AH			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	14	9	—	ns
Write Disable Time	t_{WS}	—	5	10	ns
Write Recovery Time	t_{WR}	—	5	10	ns
Address Set Up Time	t_{SA}	5	3	—	ns
Chip Select Set Up Time	t_{SC}	4	0	—	ns
Data Set Up Time	t_{SD}	4	0	—	ns
Address Hold Time	t_{HA}	3	0	—	ns
Chip Select Hold Time	t_{HC}	4	0	—	ns
Data Hold Time	t_{HD}	4	0	—	ns

WRITE CYCLE

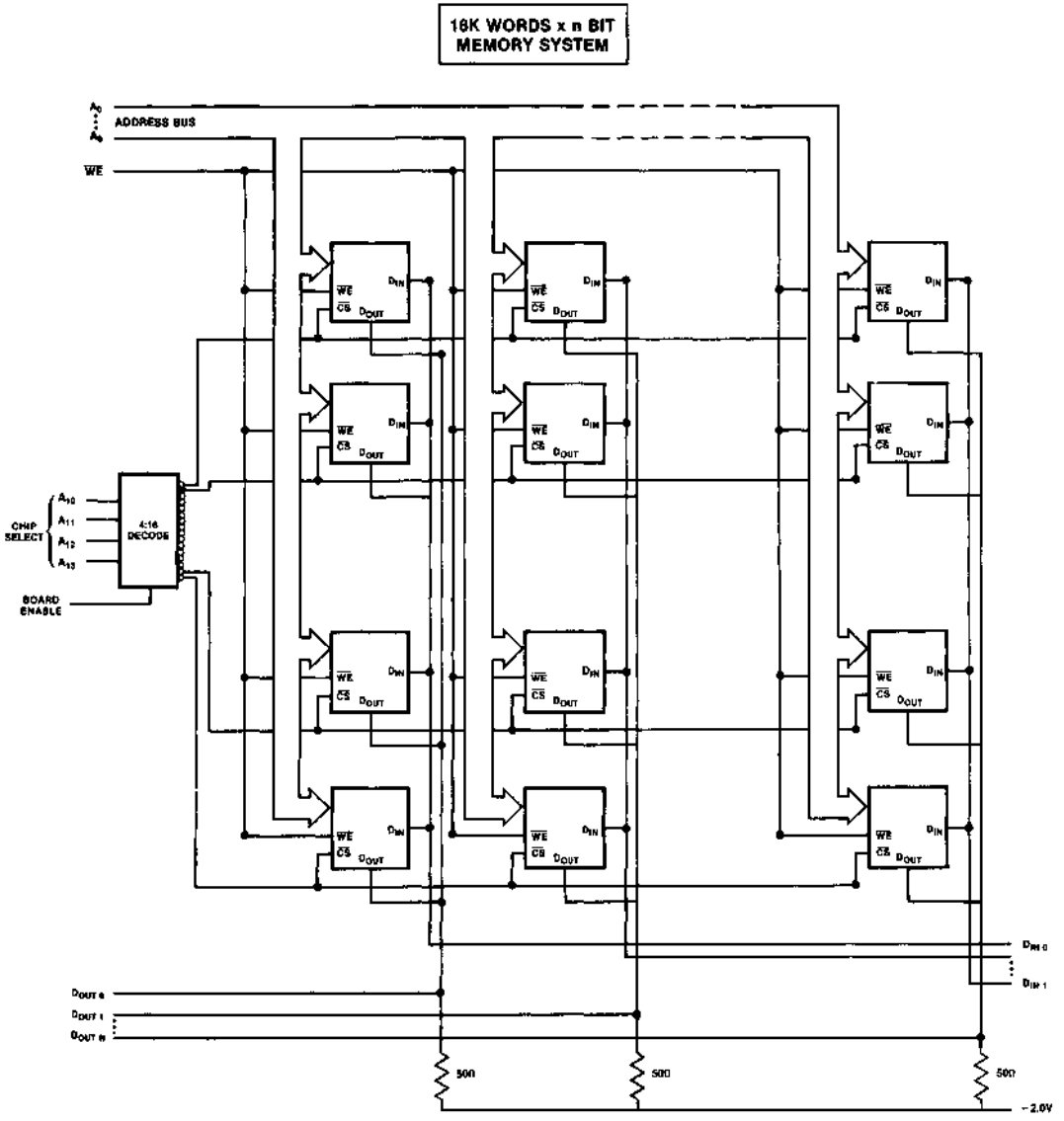


RISE TIME AND FALL TIME

Parameter	Symbol	MBM10415AH			Unit
		Min	Typ	Max	
Output Rise Time	t_r	—	5	—	ns
Output Fall Time	t_f	—	5	—	ns

APPLICATIONS INFORMATION

LARGE SYSTEM APPLICATION



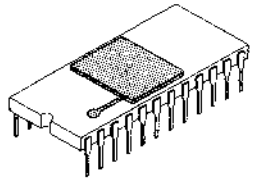
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10422 is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits and features on-chip voltage compensation for improved noise margin.

The MBM10422 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for MBM10422 is specified over a temperature range of 0° to 75°C (ambient). It features metal sealed 24-pin dual in-line packaging, and is fully compatible with industry standard 10K-series ECL families.

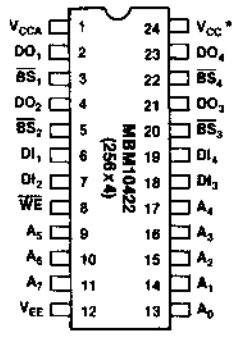


CERAMIC PACKAGE
DIP-24C-A02

FEATURES

- **256 words x 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time: 10ns max.**
- **Block select access time: 5ns max.**
- **Open emitter output for easy memory expansion**
- **Power dissipation of 0.7 mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with F10422**

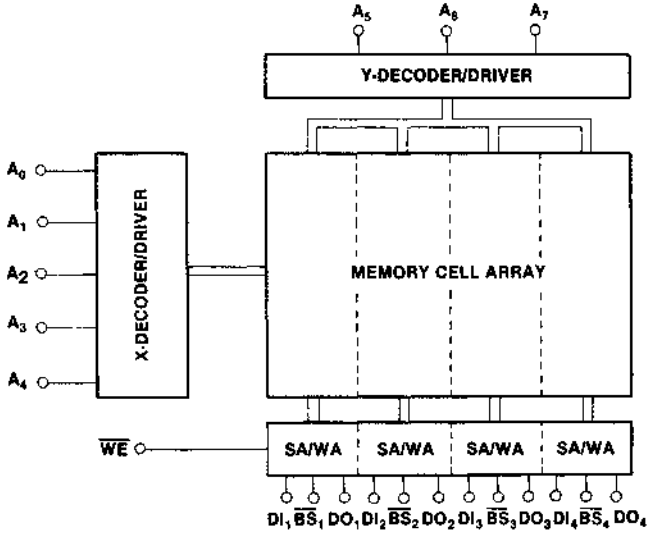
PIN ASSIGNMENT



*V_{CC} Grounded

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid appliction of any voltage higher than maximum rated voltages to this device.

MBM10422 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DI		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DO	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

DC CHARACTERISTICS

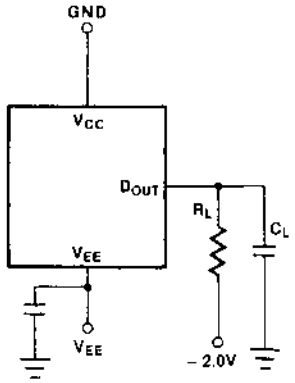
(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V and Airflow ≥ 2.5 m/s unless otherwise noted.)

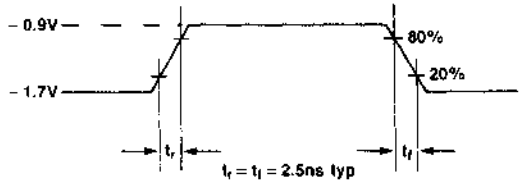
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75°C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥ 2.5m/s unless otherwise noted.)

AC TEST CONDITIONS





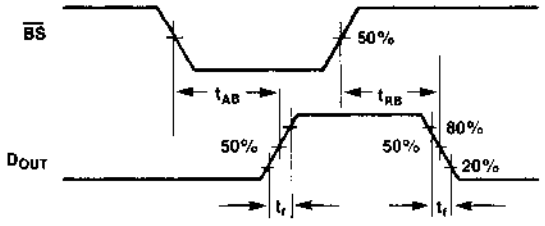
Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including jig and stray capacitance)

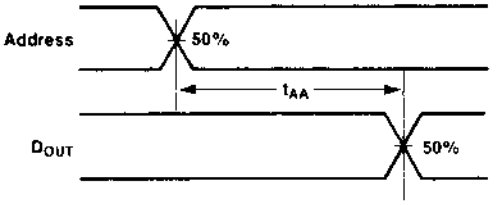
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	10	ns
Block Select Access Time	t_{AB}	—	—	5	ns
Block Select Recovery Time	t_{RB}	—	—	5	ns

READ CYCLE

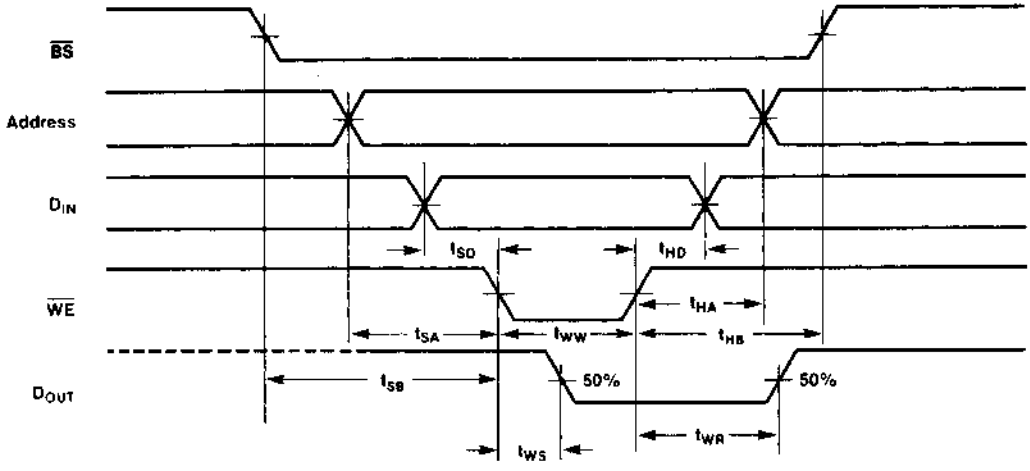




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	7	—	—	ns
Write Disable Time	t_{WS}	—	—	5	ns
Write Recovery Time	t_{WR}	—	—	10	ns
Address Set Up Time	t_{SA}	1	—	—	ns
Block Select Set Up Time	t_{SB}	1	—	—	ns
Data Set Up Time	t_{SD}	1	—	—	ns
Address Hold Time	t_{HA}	2	—	—	ns
Block Select Set Up Time	t_{HB}	2	—	—	ns
Data Hold Time	t_{HD}	2	—	—	ns

WRITE CYCLE

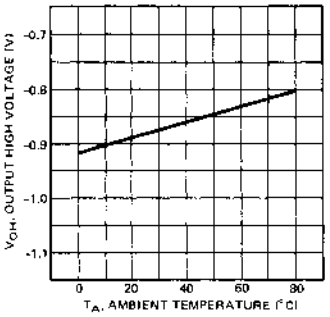


RISE TIME AND FALL TIME

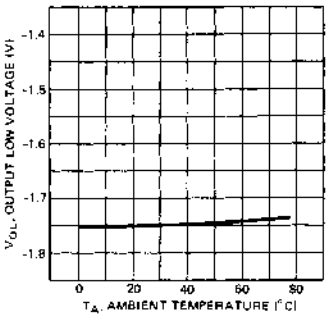
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL CHARACTERISTICS CURVES

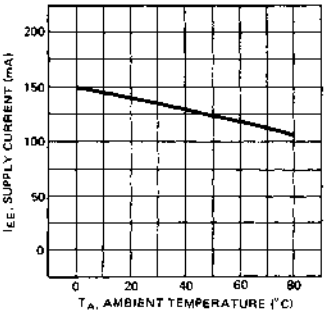
OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE



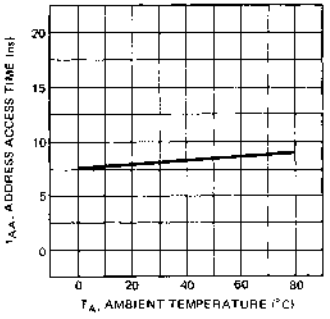
OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE



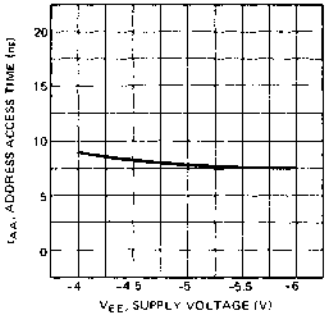
SUPPLY CURRENT vs AMBIENT TEMPERATURE



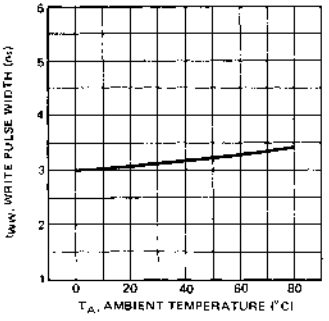
ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



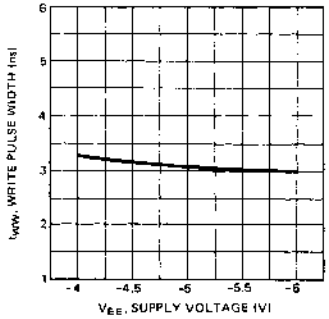
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs SUPPLY VOLTAGE



ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

ADVANCE INFORMATION

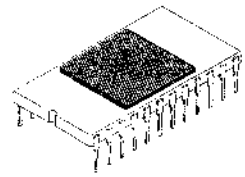
DESCRIPTION

The Fujitsu MBM10422A-7 is a fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, microprocessor and buffer storage applications.

The MBM10422A-7 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

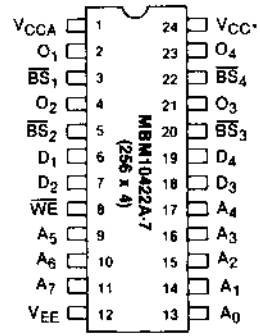
FEATURES

- **Organized as 256 x 4**
- **Address Access Time: 7ns Max.**
- **Fully compatible with industry standard 10K series ECL families**
- **Open emitter for easy memory expansion**
- **DOPOS and IOP processing**
- **Pin compatible with F10422**
- **Low power dissipation: 1040mW**



CERAMIC PACKAGE
DIP-24C-A01

PIN ASSIGNMENT



*V_{CC} Grounded

THIS IS PRELIMINARY INFORMATION FOR A NEW PRODUCT TO BE INTRODUCED DURING 1982. THIS IS NOT A FINAL SPECIFICATION. PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

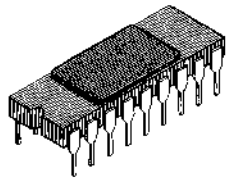
ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

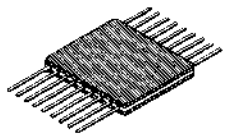
The Fujitsu MBM10470A is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one-bit and features on-chip voltage compensation for improved noise margin.

The MBM10470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10470A is specified over a temperature range of from 0°C to 75°C (ambient). It features frit-sealed 18-pin dual in-line packaging, and is fully compatible with industry-standard 10K-series ECL families.



CERAMIC PACKAGE
DIP-18C-F02

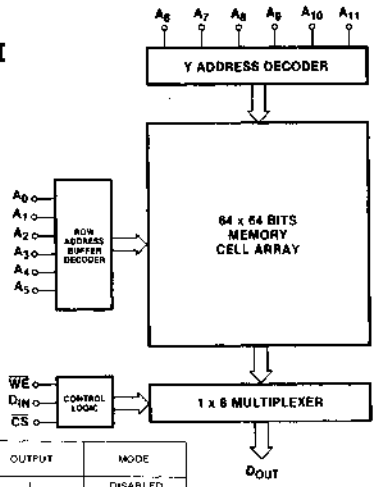


CERAMIC PACKAGE
FPT-18C-C01

FEATURES

- **4096 words x 1-bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time:**
  MBM10470A-20 20ns Max.
  13ns Typ.
- **Chip select access time:**
  15ns Max.
  5ns Typ.
- **Open emitter output for ease of memory expansion**
- **Low Power dissipation:**
  MBM10470A-20 0.19mW/bit
- **DOPOS and IOP processing**
- **Pin compatible with the F10470**

MBM10470A BLOCK DIAGRAM

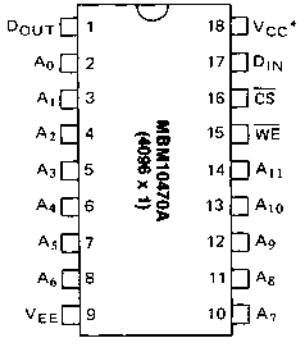


TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

PIN ASSIGNMENT



*V_{CC} grounded

Note: DIP and Flatpack Styles both conform to this pin assignment.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	7	—	pF

DC CHARACTERISTICS

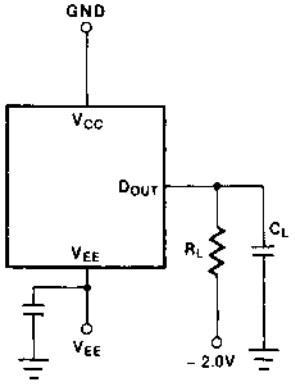
(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V and Airflow ≥ 2.5 m/s unless otherwise noted.)

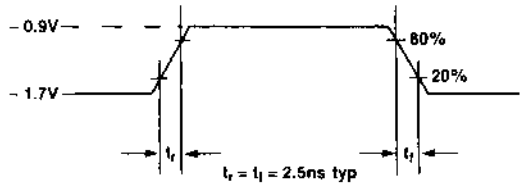
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200 −180	—	—	mA	0°C 75°C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥ 2.5m/s unless otherwise noted.)

AC TEST CONDITIONS





$t_r = t_f = 2.5$ns typ

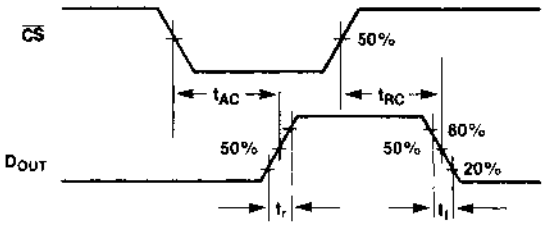
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

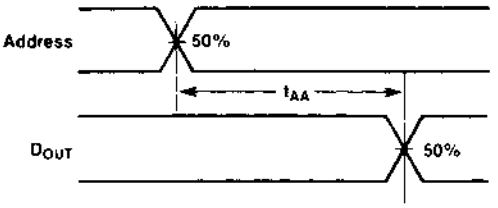
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10470A-20		Unit
		Typ	Max	
Address Access Time	t_{AA}	13	20	ns
Chip Select Access Time	t_{AC}	—	15	ns
Chip Select Recovery Time	t_{RC}	—	15	ns

READ CYCLE

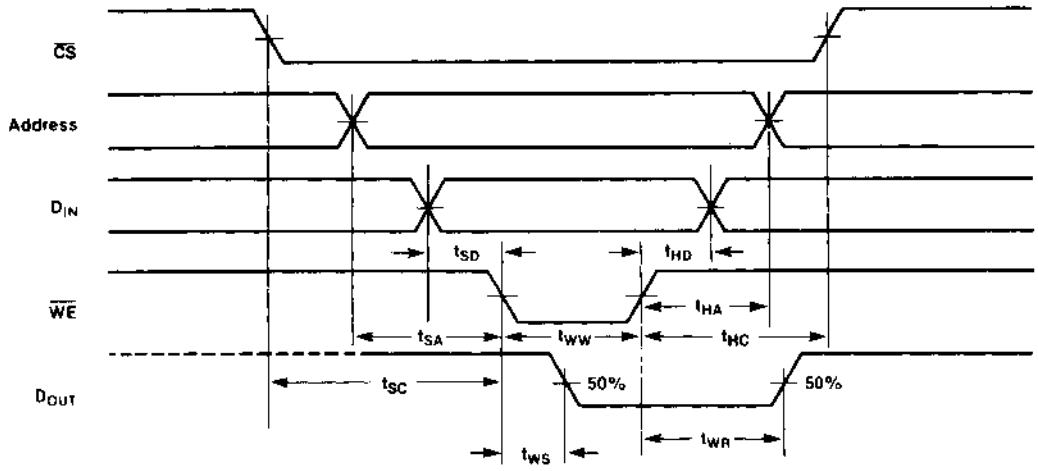




WRITE CYCLE

Parameter	Symbol	MBM10470A-20			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	15	6	—	ns
Write Disable Time	t_{WS}	—	—	15	ns
Write Recovery Time	t_{WR}	—	—	15	ns
Address Set Up Time	t_{SA}	3	0	—	ns
Chip Select Set Up Time	t_{SC}	2	0	—	ns
Data Set Up Time	t_{SD}	2	0	—	ns
Address Hold Time	t_{HA}	2	0	—	ns
Chip Select Hold Time	t_{HC}	2	0	—	ns
Data Hold Time	t_{HD}	2	0	—	ns

WRITE CYCLE

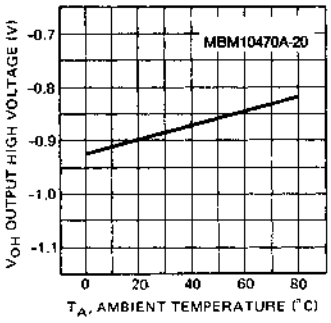


RISE TIME AND FALL TIME

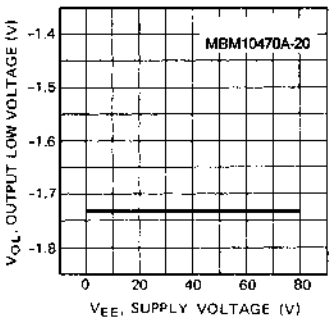
Parameter	Symbol	MBM10470A-20		Unit
		Typ	Max	
Output Rise Time	t_r	3	—	ns
Output Fall Time	t_f	3	—	ns

TYPICAL CHARACTERISTICS CURVES

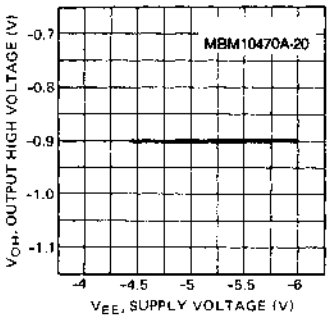
OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE



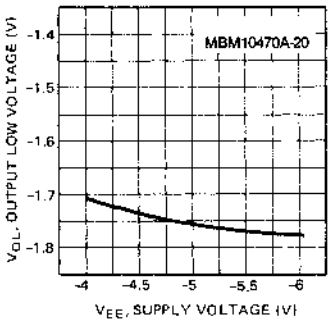
OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE



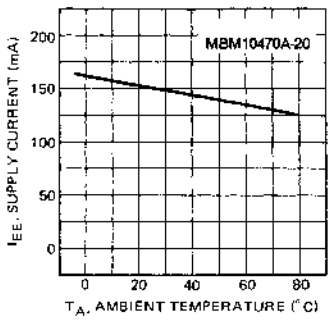
OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE



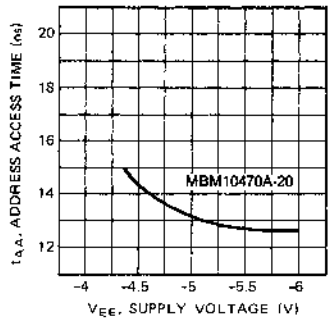
OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE



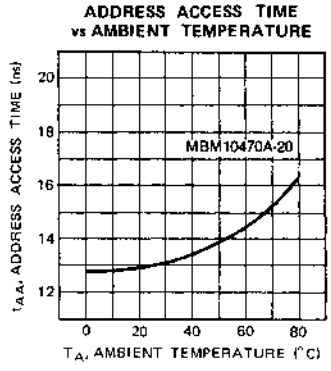
SUPPLY CURRENT vs AMBIENT TEMPERATURE



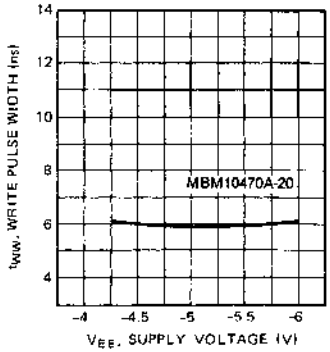
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



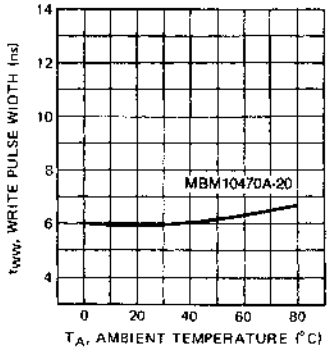
ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs SUPPLY VOLTAGE



WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



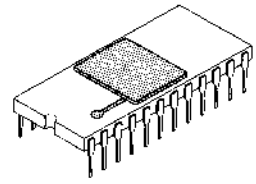
ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10474 is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications.

The MBM10474 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10474 is specified over a temperature range of 0°C to 75°C ambient. It features metal-sealed 24-pin dual in-line packaging and is fully compatible with industry-standard 10K-series ECL families.

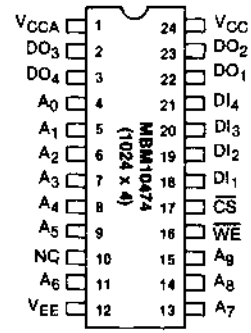


CERAMIC PACKAGE
DIP-24C-A02

FEATURES

- **1024 words x 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time:**
  25ns Max
  18ns Typ
- **Chip select time:**
  10ns Max
  7ns Typ.
- **Open emitter output for easy memory expansion**
- **Low power dissipation:**
  0.2mW/bit
- **DOPOS and IOP processing**
- **Pin compatible with F10474**

PIN ASSIGNMENT



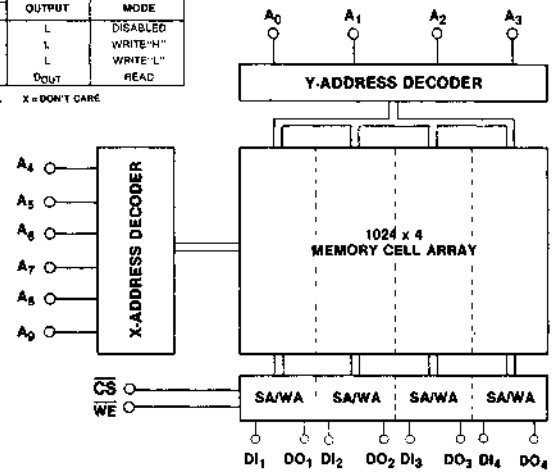
Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM10474 BLOCK DIAGRAM

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL X = DON'T CARE
L = LOW VOLTAGE LEVEL



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	7	—	pF

DC CHARACTERISTICS

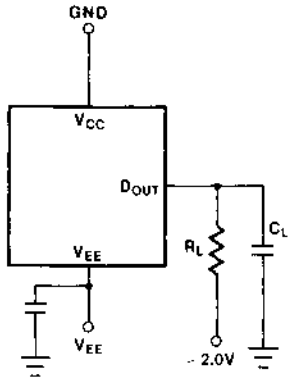
(V_{CC} = 0V, V_{EE} = −5.2V ±5%, Output load = 50Ω to −2.0V and Airflow ≥ 2.5m/s unless otherwise noted.)

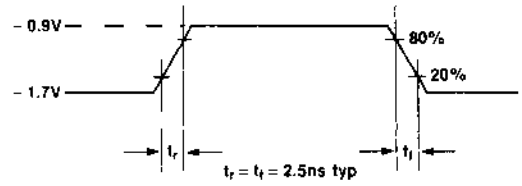
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −970 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current (V_{IN} = $V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75°C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥ 2.5m/s unless otherwise noted.)

AC TEST CONDITIONS





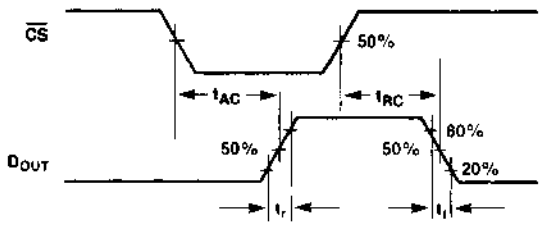
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

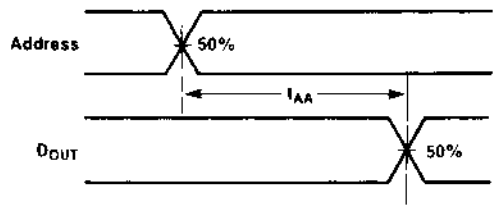
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	18	25	ns
Chip Select Access Time	t_{AC}	—	7	10	ns
Chip Select Recovery Time	t_{RC}	—	7	10	ns

READ CYCLE

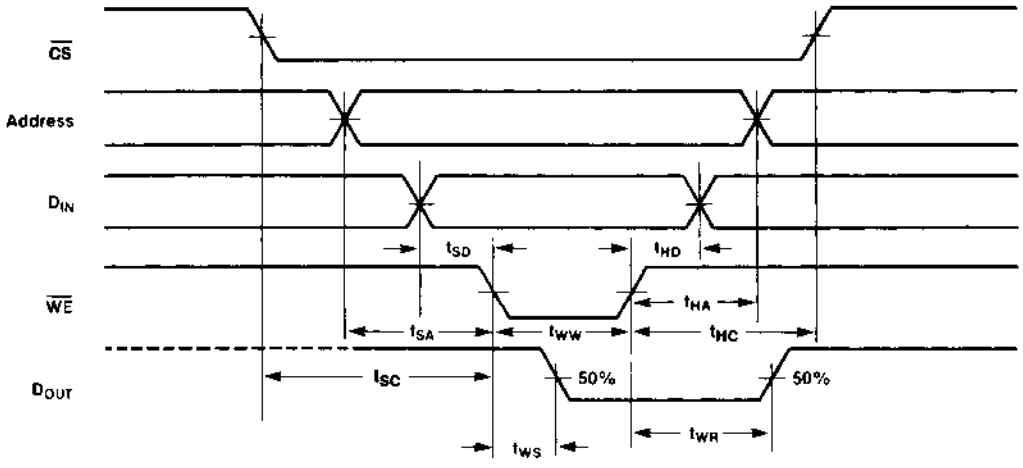




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15	—	—	ns
Write Disable Time	t_{WS}	—	—	8	ns
Write Recovery Time	t_{WR}	—	—	15	ns
Address Set Up Time	t_{SA}	8	—	—	ns
Chip Select Set Up Time	t_{SC}	5	—	—	ns
Data Set Up Time	t_{SD}	5	—	—	ns
Address Hold Time	t_{HA}	5	—	—	ns
Chip Select Hold Time	t_{HC}	5	—	—	ns
Data Hold Time	t_{HD}	5	—	—	ns

WRITE CYCLE

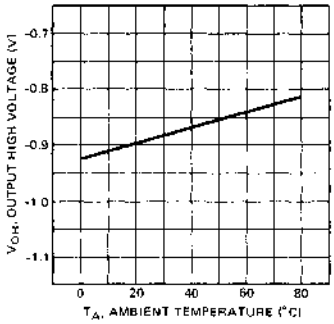


RISE TIME AND FALL TIME

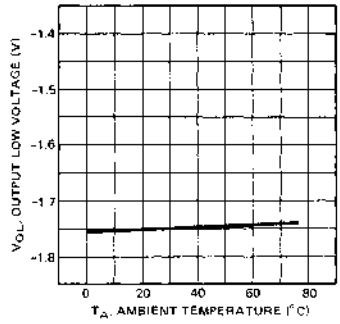
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	5	—	ns
Output Fall Time	t_f	—	5	—	ns

TYPICAL CHARACTERISTICS CURVES

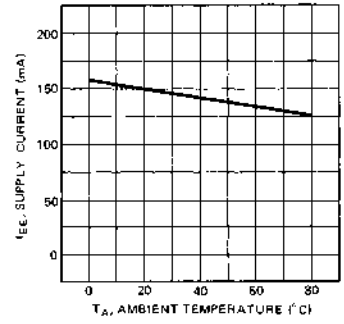
OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE



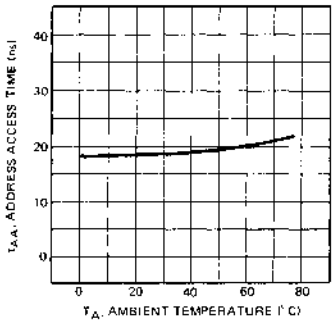
OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE



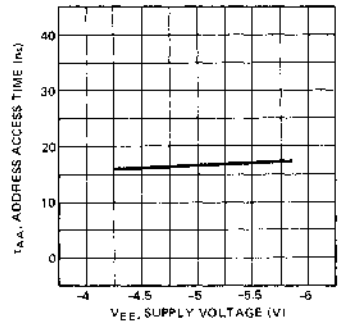
SUPPLY CURRENT vs AMBIENT TEMPERATURE



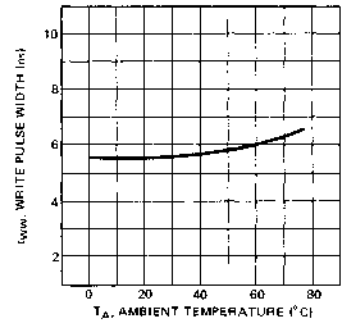
ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



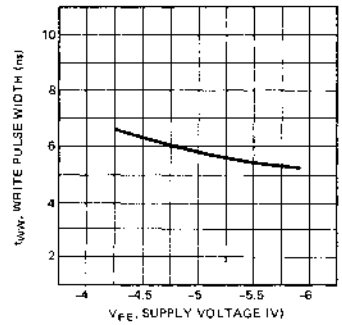
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs SUPPLY VOLTAGE



FUJITSU
MICROELECTRONICS

MBM10474A-15

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

ADVANCE INFORMATION

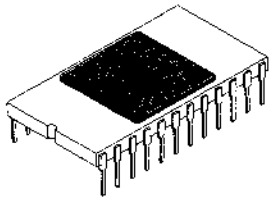
DESCRIPTION

The Fujitsu MBM10474A-15 is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, microprocessor and buffer storage applications.

The MBM10474A-15 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

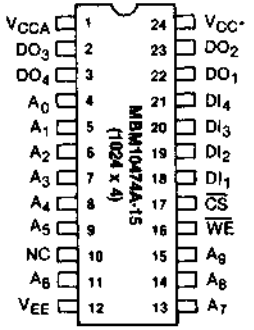
FEATURES

- **Organized as 1024 x 4**
- **Address Access Time: 15ns Max.**
- **Fully compatible with industry standard 10K series ECL families**
- **Open emitter for easy memory expansion**
- **DOPOS and IOP processing**
- **Pin compatible with F10474**
- **Low power dissipation: 1040mW**



CERAMIC PACKAGE
DIP-24C-A02

PIN ASSIGNMENT



*V_{CC} Grounded

THIS IS PRELIMINARY INFORMATION FOR A NEW PRODUCT TO BE INTRODUCED DURING 1982. THIS IS NOT A FINAL SPECIFICATION. PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

ECL 16,384-BIT BIPOLAR RANDOM ACCESS MEMORY

ADVANCE INFORMATION

DESCRIPTION

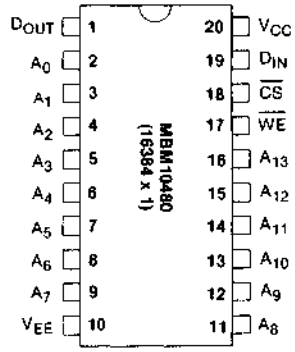
The Fujitsu MBM10480 is a fully decoded 16,384-bit ECL read/write random access memory designed for high speed scratch pad, microprocessor and buffer storage applications.

The MBM10480 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

FEATURES

- **Organized as 16,384 x 1**
- **Address Access Time: 20ns Max.**
- **Fully compatible with industry standard 10K series ECL families**
- **Open emitter for easy memory expansion**
- **DOPOS and IOP processing**
- **Pin compatible with F10480**
- **Low power dissipation: 700mW**
- **−5.2 V power supply**
- **Will be available in 100K series ECL**

PIN ASSIGNMENT



Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

THIS IS PRELIMINARY INFORMATION FOR A NEW PRODUCT TO BE INTRODUCED DURING 1982. THIS IS NOT A FINAL SPECIFICATION. PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

TTL 576-BIT BIPOLAR RANDOM ACCESS MEMORY

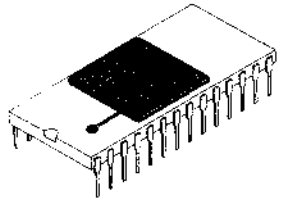
DESCRIPTION

The Fujitsu MBM93419 is a high speed TTL read/write random-access memory, organized as 64 words by 9 bits, with open-collector outputs.

MBM93419 is packaged in a 28-pin dual-in-line package, and is plug-in replaceable with F93419. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems.

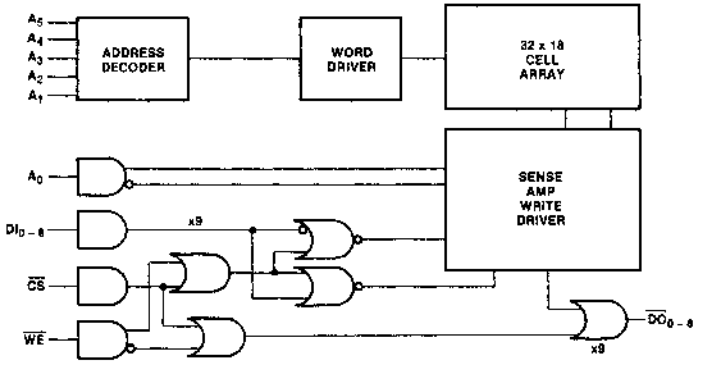
FEATURES

- **Organization: 64 words x 9-bits**
- **+5V Single Power Supply**
- **TTL Inputs and Outputs**
- **Open Collector Outputs**
- **Address Access Time: 45ns Max.**
- **Chip Select Access Time: 40ns Max.**
- **Power Dissipation: 1.3mW/bit Typ.**
- **Compatible with F93419**

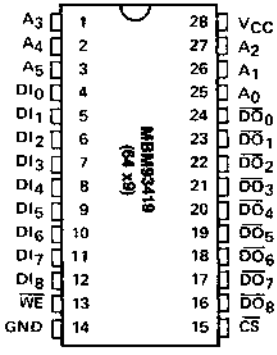


CERAMIC PACKAGE DIP-28C-A01

MBM93419 BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DI		
H	X	X	H	DISABLED
L	L	H	H	WRITE "H"
L	L	L	H	WRITE "L"
L	H	X	$\overline{D_{OUT}}$	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE
*DATA OUTPUT IS THE COMPLEMENT OF DATA INPUT

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (DC)	V_{IN}	−0.5 to +5.5	V
Input Current (DC)	I_{IN}	−12.0 to +5.0	mA
Output Voltage (V_{OUT} = "H")	V_{OUT}	−0.5 to +5.5	V
Output Current (DC, V_{OUT} = "L")	I_{OUT}	+20.0	mA
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +75°C
Input High Voltage	V_{IH}	2.1	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	

CAPACITANCE

(T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 2.0V, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	—	5.0	pF
Output Pin Capacitance	C_{OUT}	—	—	8.0	pF

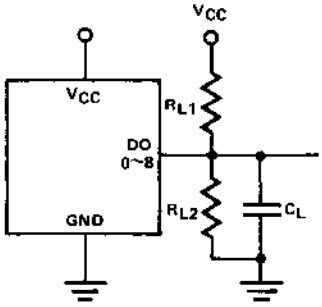
DC CHARACTERISTICS

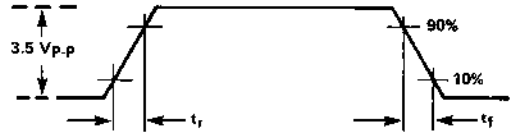
(V_{CC} = 5V ±5%, T_A = 0°C to 75°C, Air Flow ≥ 2.5m/sec, After Warm-up ≥ 2 min.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Low Voltage	V_{OL}	V_{CC} = Min, I_{OL} = 12mA	—	0.4	0.5	V
Input High Voltage	V_{IH}	—	—	1.6	—	V
Input Low Voltage	V_{IL}	—	—	1.5	—	V
Input Low Current	I_{IL}	V_{CC} = Max, V_{IN} = 0.4V	—	−250	−400	μA
Input High Current	I_{IH1}	V_{CC} = Max, V_{IN} = 4.5V	—	1.0	40	μA
Input High Current	I_{IH2}	V_{CC} = Max, V_{IN} = 5.25V	—	—	1.0	mA
Output Leakage Current	I_{CEX}	V_{CC} = Max, V_{OUT} = 4.5V	—	1.0	100	μA
Input Clamp Diode Voltage	V_{CD}	V_{CC} = Max, V_{OUT} = 4.5V	—	−1.0	−1.5	V
Power Supply Current	I_{CC}	V_{CC} = Max, T_A = 25°C All Input GND	—	160	200	mA

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 75°C, Air Flow ≥ 2.5 m/sec, After Warm-up ≥ 2 min.)



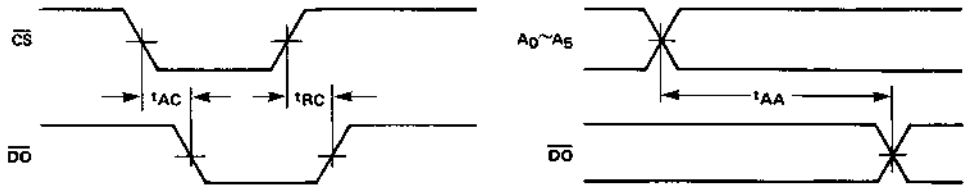


Input Pulse Voltage: 3.5V_{P-P}
Input Pulse Rise and Fall Time: 10ns
Output Load: R_{L1} = 450Ω
R_{L2} = 750Ω
C_L = 30pF (Including Jig)
Timing Measurement Levels: Input = 1.5V
Output = 1.5V

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	26	45	ns
Chip Select Access Time	t_{AC}	—	18	40	ns
Chip Select Recovery Time	t_{RC}	—	18	40	ns

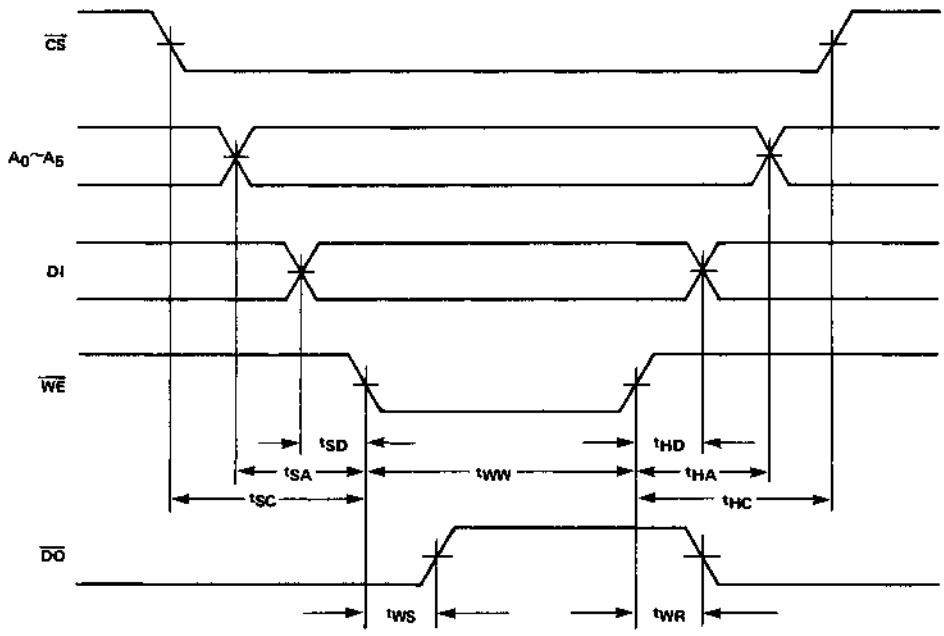
READ CYCLE



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	35	7	—	ns
Write Recovery Time	t_{WR}	—	20	45	ns
Write Delayed Time	t_{WS}	—	20	40	ns
Address Setup Time	t_{SA}	5	0	—	ns
Chip Select Setup Time	t_{SC}	5	0	—	ns
Data Setup Time	t_{SD}	5	0	—	ns
Address Hold Time	t_{HA}	5	0	—	ns
Chip Select Hold Time	t_{HC}	5	0	—	ns
Data Hold Time	t_{HD}	5	0	—	ns

WRITE CYCLE



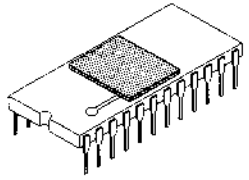
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM100422 is a fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits, and it features on-chip voltage compensation for improved noise margin.

The MBM100422 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM100422 is specified over a temperature range of 0°C to 85°C (ambient). It also features metal-sealed 24-pin dual in-line packaging, and is fully compatible with industry-standard 100K-series ECL families.



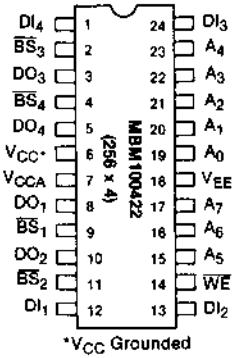
CERAMIC PACKAGE
DIP-24C-A02

ALSO AVAILABLE IN FLAT PACKAGE
FPT-24C-F02

FEATURES

- **256 words x 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 100K-series ECL families**
- **Address Access Time: 10ns max.**
- **Block Select Access Time: 5ns max.**
- **Open emitter output for easy memory expansion**
- **Low power dissipation of 0.7mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with the F100422**

PIN ASSIGNMENT



*V_{CC} Grounded

NOTE: DIP and Flat package styles conform to the same pin assignment

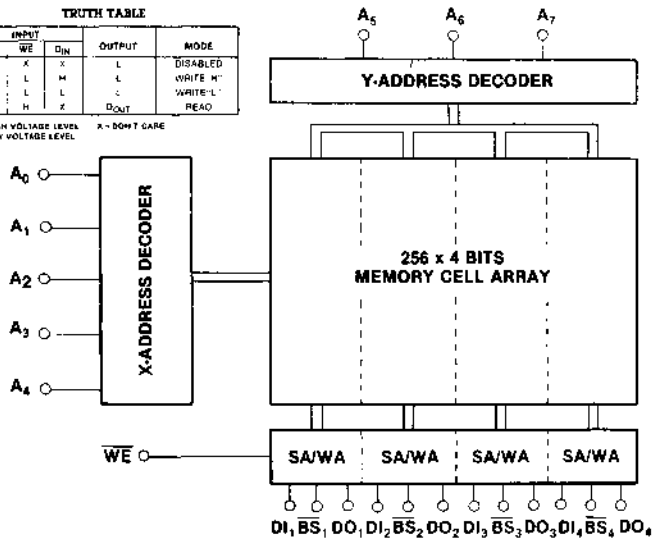
Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM100422 BLOCK DIAGRAM

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL X = DON'T CARE
L = LOW VOLTAGE LEVEL



FUNCTIONAL DESCRIPTION

The Fujitsu MBM100422 is fully decoded 1024-bit read/write random access memory organized as 256 words by 4 bits. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_7$. The active low Block Select ($\overline{BS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{BS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection,

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to +85°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

DC CHARACTERISTICS

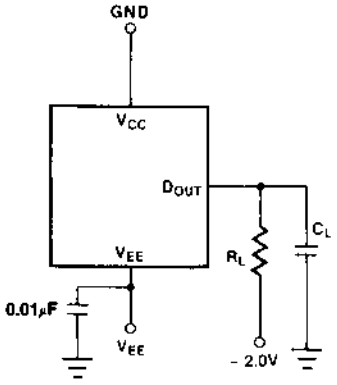
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω to −2.0V, T_A = 0°C to 85°C and Airflow ≥ 2.5 m/s, unless otherwise noted.)

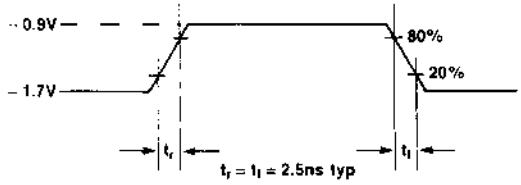
Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH}max. or V_{IL}min.)	V_{OH}	−1025	—	−880	mV
Output Low Voltage (V_{IN} = V_{IH}max. or V_{IL}min.)	V_{OL}	−1810	—	−1620	mV
Output High Voltage (V_{IN} = V_{IH}min. or V_{IL}max.)	V_{OHC}	−1035	—	—	mV
Output Low Voltage (V_{IN} = V_{IH}min. or V_{IL}max.)	V_{OLC}	—	—	−1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1165	—	−880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1810	—	−1475	mV
Input High Current (V_{IN} = V_{IH}max.)	I_{IH}	—	—	220	μA
Input Low Current (V_{IN} = V_{IL}min.)	I_{IL}	−50	—	—	μA
$\overline{BS}$ Input Low Current (V_{IN} = V_{IL}min.)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−180	—	—	mA

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, T_A = 0°C tp 85°C, Output Load = 50Ω to −2.0V and 30pF to GND, and Airflow ≥ 2.5 m/s, unless otherwise noted.)

AC TEST CONDITIONS





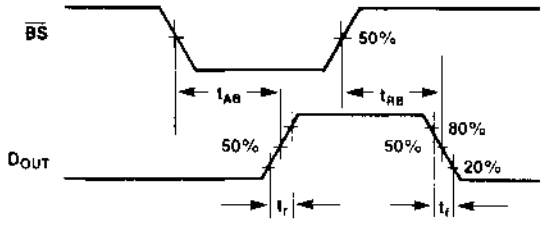
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

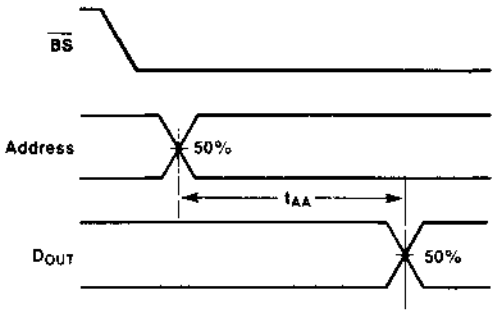
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	10	ns
Block Select Access Time	t_{AB}	—	—	5	ns
Block Select Recovery Time	t_{RB}	—	—	5	ns

READ CYCLE

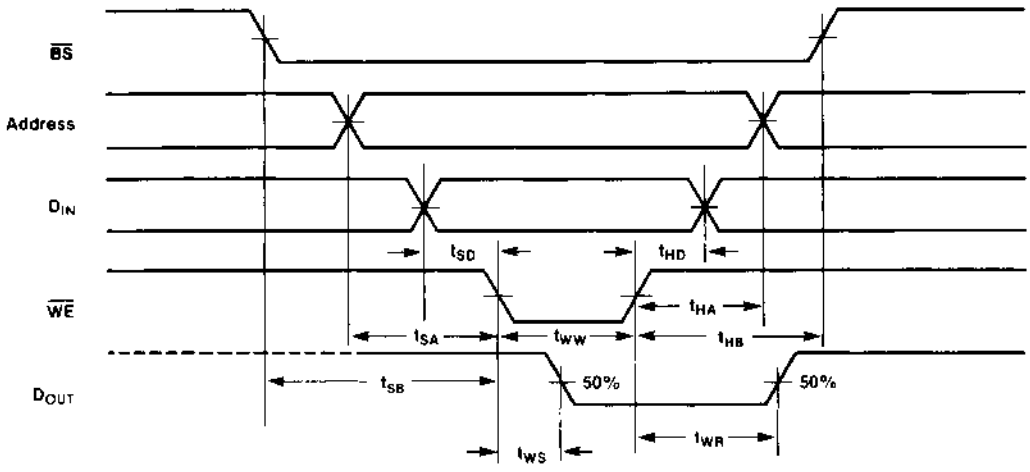




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	7	—	—	ns
Write Disable Time	t_{WS}	—	—	5	ns
Write Recovery Time	t_{WR}	—	—	10	ns
Address Set Up Time	t_{SA}	1	—	—	ns
Block Select Set Up Time	t_{SB}	1	—	—	ns
Data Set Up Time	t_{SD}	1	—	—	ns
Address Hold Time	t_{HA}	2	—	—	ns
Block Select Hold Time	t_{HB}	2	—	—	ns
Data Hold Time	t_{HD}	2	—	—	ns

WRITE CYCLE

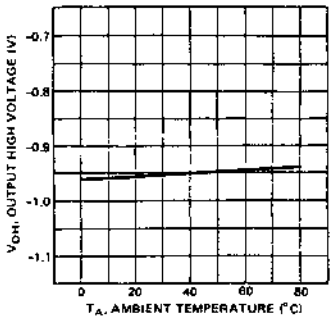


RISE TIME AND FALL TIME

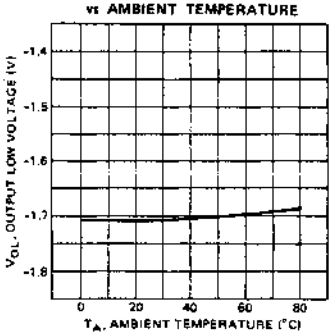
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL CHARACTERISTICS CURVES

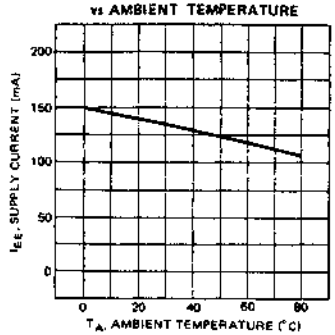
OUTPUT HIGH VOLTAGE
vs AMBIENT TEMPERATURE



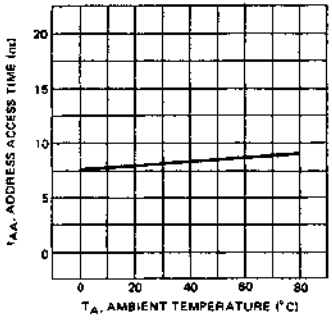
OUTPUT LOW VOLTAGE
vs AMBIENT TEMPERATURE



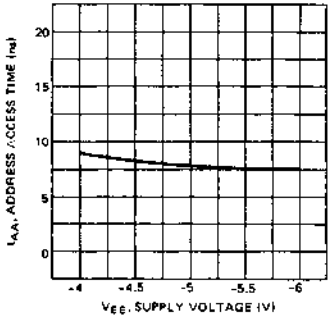
SUPPLY CURRENT
vs AMBIENT TEMPERATURE



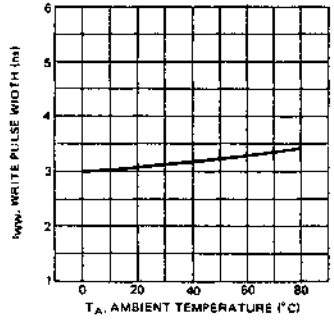
ADDRESS ACCESS TIME
vs AMBIENT TEMPERATURE



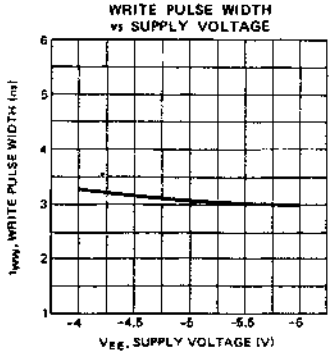
ADDRESS ACCESS TIME
vs SUPPLY VOLTAGE



WRITE PULSE WIDTH
vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH
vs SUPPLY VOLTAGE



FUJITSU
MICROELECTRONICS

MBM100422A-7

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

ADVANCE INFORMATION

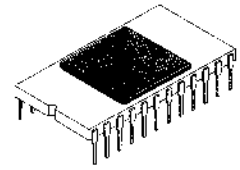
DESCRIPTION

The Fujitsu MBM100422A-7 is a fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, microprocessor and buffer storage applications.

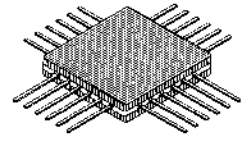
The MBM100422A-7 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

FEATURES

- **Organized as 256 x 4**
- **Address Access Time: 7ns Max.**
- **Fully compatible with industry standard 100K series ECL families**
- **Open emitter for easy memory expansion**
- **DOPOS and IOP processing**
- **Pin compatible with F100422**
- **Low power dissipation: 900mW**
- **−4.5V power supply**



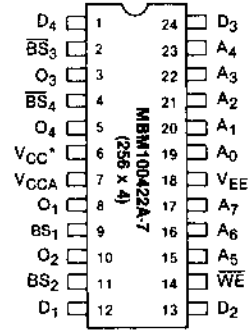
CERAMIC PACKAGE
DIP-24C-A01



CERAMIC PACKAGE
FPT-24C-C02

THIS IS PRELIMINARY INFORMATION FOR A NEW PRODUCT TO BE INTRODUCED DURING 1982. THIS IS NOT A FINAL SPECIFICATION. PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

PIN ASSIGNMENT



*V_{CC} Grounded

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

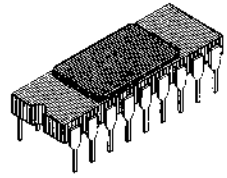
The Fujitsu MBM100470 is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized ad 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100470 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon) as well as IOP (Isolation by Oxide and Polysilicon), processing.

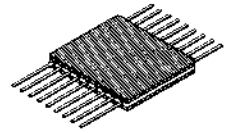
Operation for the MBM100470 is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package). It also features 18-pin Ceramic DIP and Flat Package, and is fully compatible with industry-standard 100K-series ECL families.

FEATURES

- **4096 words x 1-bit organization**
- **On-chip voltage/temperature compensation for improved noise margin**
- **Address access time:**
  20ns Max.
  14ns Typ.
- **Chip select access time:**
  15ns Max.
  5ns Typ.
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.16mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with the F100470**



CERAMIC PACKAGE
DIP-18C-F02



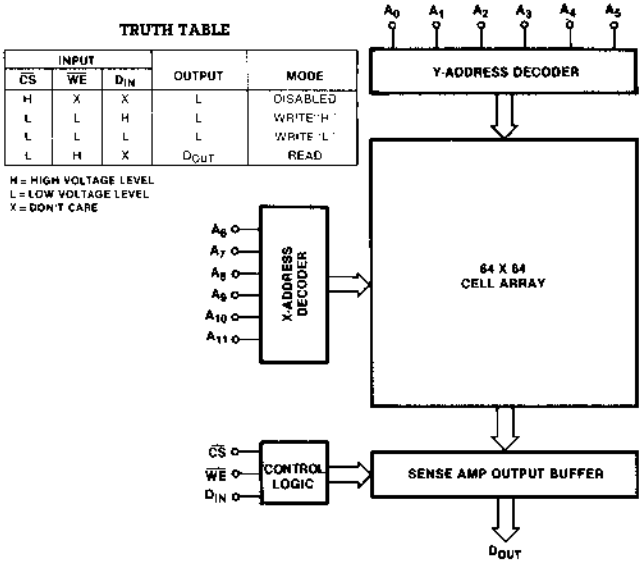
CERAMIC PACKAGE
FPT-18C-C01

MBM100470 BLOCK DIAGRAM

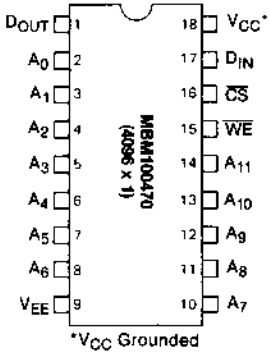
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE



PIN ASSIGNMENT



*V_{CC} Grounded

NOTE: DIP and Flatpack Styles conform to the same pin assignment

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL DESCRIPTION

The Fujitsu 100470 is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of 12-bit address designated $A_0 - A_{11}$. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP	−55 to +125	°C
	T_C for Flat Package	−55 to +125	
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply Voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to 85°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	7	—	pF

DC CHARACTERISTICS

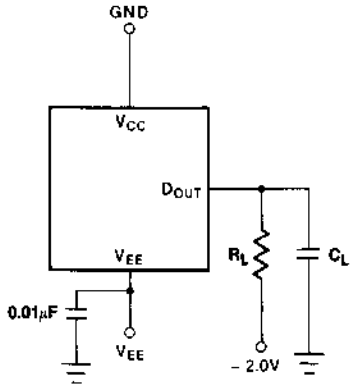
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30pF to −2.0V, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≧ 2.5 m/s, unless otherwise noted.)

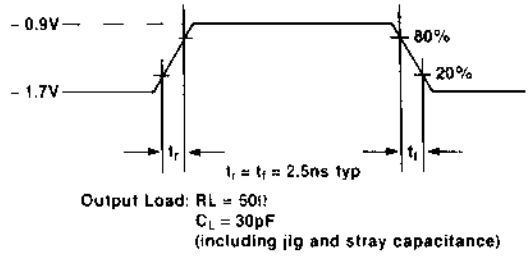
Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OH}	−1025	—	−880	mV
Output Low Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OL}	−1810	—	−1620	mV
Output High Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OHC}	−1035	—	—	mV
Output Low Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OLC}	—	—	−1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1165	—	−880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1810	—	−1475	mV
Input High Current (V_{IN} = $V_{IH\,max.}$)	I_{IH}	—	—	220	μA
Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	−50	—	—	μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	−195	—	—	mA

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≧ 2.5 m/s, unless otherwise noted.)

AC TEST CONDITIONS





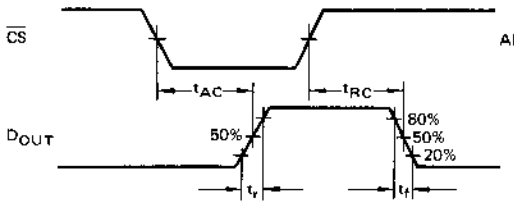
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

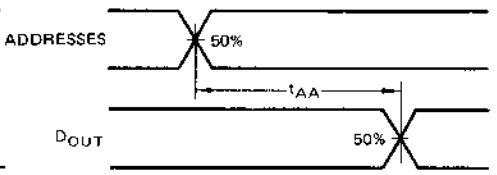
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	14	20	ns
Chip Select Access Time	t_{AC}	—	5	15	ns
Chip Select Recovery Time	t_{RC}	—	5	15	ns

READ CYCLE

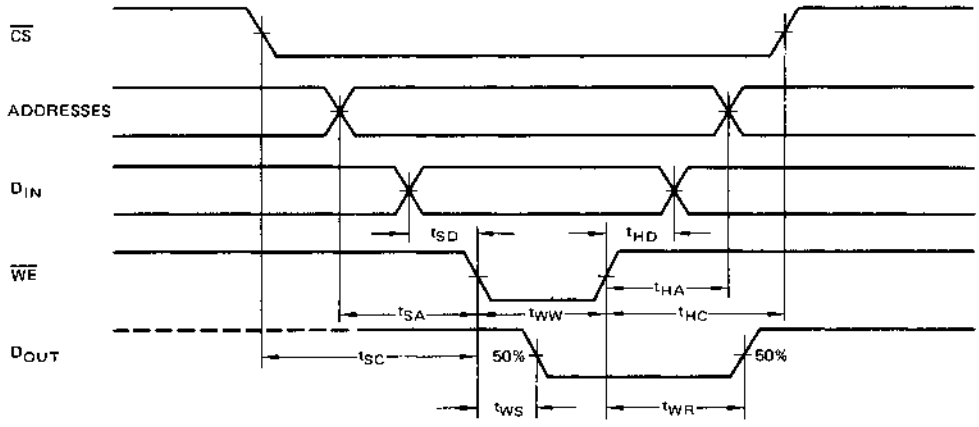




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15	6	—	ns
Write Disable Time	t_{WS}	—	—	15	ns
Write Recovery Time	t_{WR}	—	—	15	ns
Address Set Up Time	t_{SA}	3	0	—	ns
Chip Select Set Up Time	t_{SC}	2	0	—	ns
Data Set Up Time	t_{SD}	2	0	—	ns
Address Hold Time	t_{HA}	2	0	—	ns
Chip Select Set Up Time	t_{HC}	2	0	—	ns
Data Hold Time	t_{HD}	2	0	—	ns

WRITE CYCLE

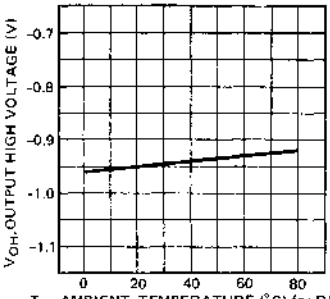


RISE TIME AND FALL TIME

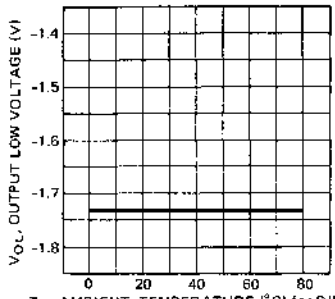
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	3	—	ns
Output Fall Time	t_f	—	3	—	ns

TYPICAL CHARACTERISTICS CURVES

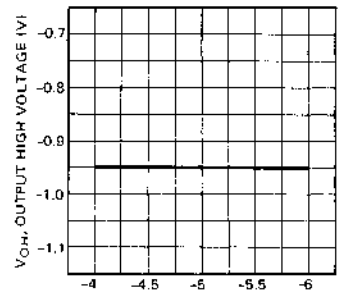
OUTPUT HIGH VOLTAGE vs TEMPERATURE



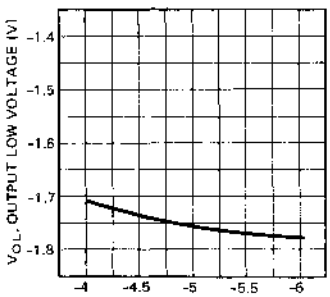
OUTPUT LOW VOLTAGE vs TEMPERATURE



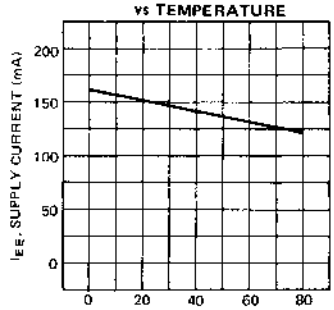
OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE



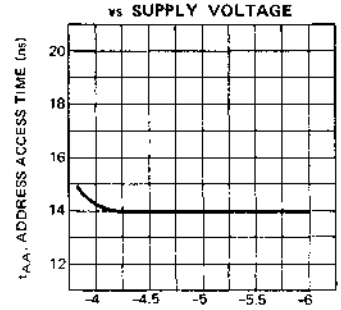
OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE



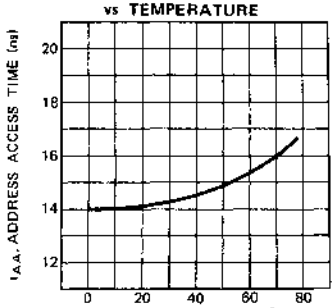
SUPPLY CURRENT vs TEMPERATURE



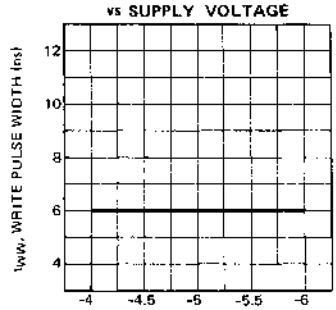
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



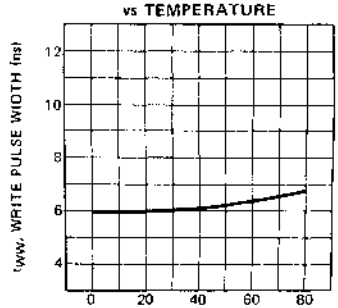
ADDRESS ACCESS TIME vs TEMPERATURE



WRITE PULSE WIDTH vs SUPPLY VOLTAGE



WRITE PULSE WIDTH vs TEMPERATURE



ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

ADVANCE INFORMATION

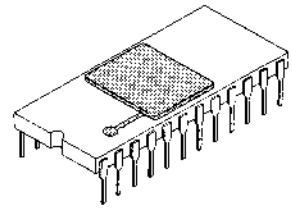
DESCRIPTION

The Fujitsu MBM100474-15 is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, microprocessor and buffer storage applications.

The MBM100474-15 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

FEATURES

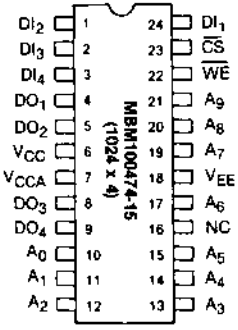
- **Organized as 1024 x 4**
- **Address Access Time: 15ns Max.**
- **Fully compatible with industry standard 100K series ECL families**
- **Open emitter for easy memory expansion**
- **DOPOS and IOP processing**
- **Pin compatible with F100474**
- **Low power dissipation: 900mW**
- **−4.5V power supply**

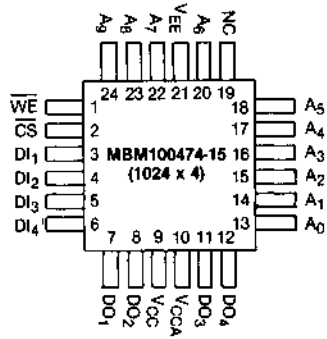


CERAMIC PACKAGE
DIP-24C-A02

ALSO AVAILABLE IN FLATPACK STYLE

PIN ASSIGNMENTS





THIS IS PRELIMINARY INFORMATION FOR A NEW PRODUCT TO BE INTRODUCED DURING 1982. THIS IS NOT A FINAL SPECIFICATION. PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

BIPOLAR PROMS

QUICK GUIDE TO PRODUCTS IN THIS SECTION

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB7121E	1K x 4	45nS	+5	787mW	18-pin	6-8
MB7121H	1K x 4	35nS	+5	787mW	18-pin	6-8
MB7122E	1K x 4	45nS	+5	787mW	18-pin	6-8
MB7122H	1K x 4	35nS	+5	787mW	18-pin	6-8
MB7123E	512 x 8	45nS	+5	850mW	20-pin	6-15
MB7123H	512 x 8	35nS	+5	850mW	20-pin	6-15
MB7124E	512 x 8	45nS	+5	850mW	20-pin	6-15
MB7124H	512 x 8	35nS	+5	850mW	20-pin	6-15
MB7127E	2K x 4	55nS	+5	820mW	18-pin	6-18
MB7127H	2K x 4	45nS	+5	820mW	18-pin	6-18
MB7128E	2K x 4	55nS	+5	820mW	18-pin	6-18
MB7128H	2K x 4	45nS	+5	820mW	18-pin	6-18
MB7131E	1K x 8	55nS	+5	920mW	24-pin	6-30
MB7131H	1K x 8	45nS	+5	920mW	24-pin	6-30
MB7132E	1K x 8	55nS	+5	920mW	24-pin	6-30
MB7132H	1K x 8	45nS	+5	920mW	24-pin	6-30
MB7134E	4K x 4	55nS	+5	895mW	20-pin	6-37
MB7134H	4K x 4	45nS	+5	895mW	20-pin	6-37
MB7137E	2K x 8	55nS	+5	950mW	24-pin	6-42
MB7137H	2K x 8	45nS	+5	950mW	24-pin	6-42
MB7138E	2K x 8	55nS	+5	950mW	24-pin	6-42
MB7138H	2K x 8	45nS	+5	950mW	24-pin	6-42
MB7141E	4K x 8	65nS	+5	1018mW	24-pin	6-49
MB7141H	4K x 8	55nS	+5	1018mW	24-pin	6-49
MB7142E	4K x 8	65nS	+5	1018mW	24-pin	6-49
MB7142H	4K x 8	55nS	+5	1018mW	24-pin	6-49

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 71XX series Schottky PROMs are fabricated using Schottky TTL, passive isolation technology known as Isolation by Oxide and Poly-silicon (IOP). The isolation is achieved by a thin-epitaxial and Shallow V-Grooving (SVG), Diffused Eutectic Aluminum Process (DEAP™) technology with fine emitter. It uses a pulse programming method which achieves high-speed operation, high-speed programming, high programmability and high reliability.

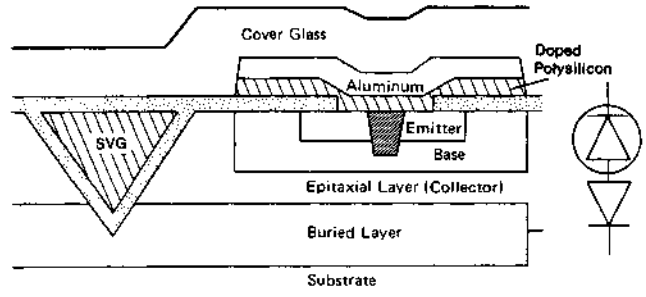
The memory cell is originally structured with an open-base NPN transistor and then programmed by shorting the base-emitter junction, i.e. shorted junction type cell which is achieved by eutectically melting aluminum and silicon adjacent to the P-N junction of the cell diode with relatively low temperatures.

Fast programming time of typically 150μs/bit is achieved with a fine emitter cell which requires less programming energy. The result is negligible thermal stress. This high reliability feature eliminates aluminum migration in the programmed cell. Further, Fujitsu's advanced technology allows very high programmability.

SPECIAL FACTORY TESTING

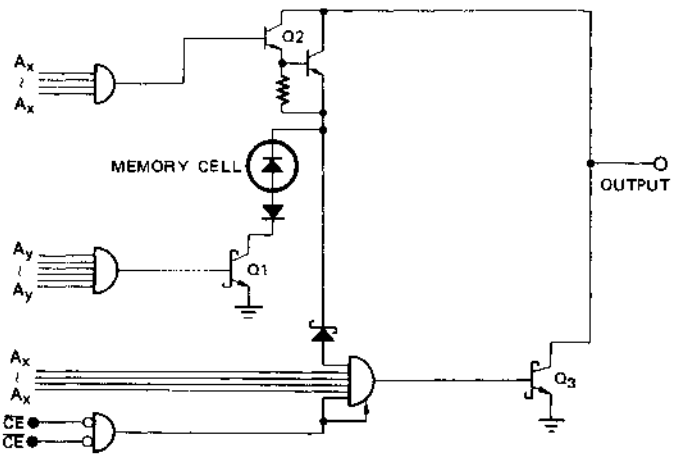
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMED CELL (CROSS SECTION)



Programmed by Diffused Eutectic Aluminum Process

INTERNAL PROGRAMMING CIRCUIT



PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells, To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using the address inputs to turn on transistors Q1 and Q2. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the appropriate output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the output voltage indicates that the selected bit is in the logic one state.

To assure that the element is programmed properly, two additional programming pulses are applied immediately after an output voltage indicates conduction in the programmed bit.

One output must be programmed at a time, since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

The outputs where no programming current pulse is being applied during programming, can be floated, grounded or tied to any voltage less than V_{CC} or PV_{CC}.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input active. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS (T_A = 25°C)

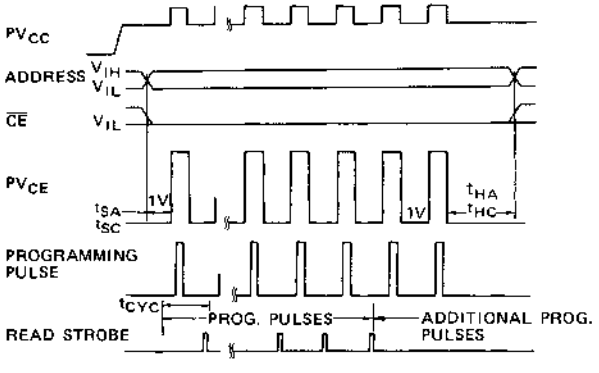
Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.5	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	125	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	—	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.0	V

AC SPECIFICATIONS (T_A = 25°C)

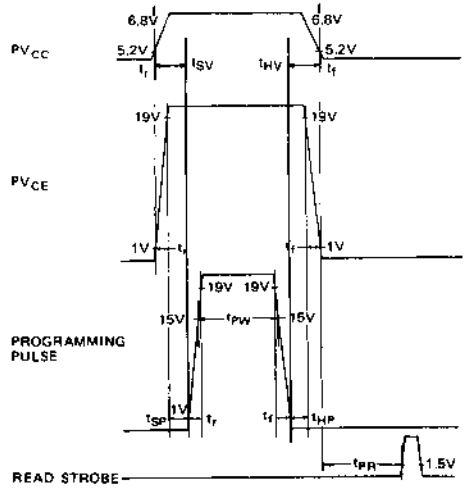
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	—	—	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	—	—	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	—	—	2	μs
Programming Pulse Fall Time	t_f(4)	—	—	2	μs
PV_{CC} Set-up Time	t_{SV}	2	—	—	μs
PV_{CE} Pulse Fall Time	t_f(4)	—	—	2	μs
PV_{CC} Hold Time	t_{HV}	2	—	—	μs
PV_{CC} Pulse Fall Time	t_f(5)	—	—	2	μs
Address Input Set-up Time	t_{SA}	2	—	—	μs
Chip Enable Input Set-up Time	t_{SC}	2	—	—	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	—	—	μs
Address Input Hold Time	t_{HA}	2	—	—	μs
Chip Enable Input Hold Time	t_{HC}	2	—	—	μs
PV_{CE} Hold Time	t_{HP}(7)	2	—	—	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	—	—	μs
Programming Pulse Number	—	—	—	100	Times
Programming Time/Bit	—	120	150	6120	μs/bit
Additional Programming Pulse Number	—	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



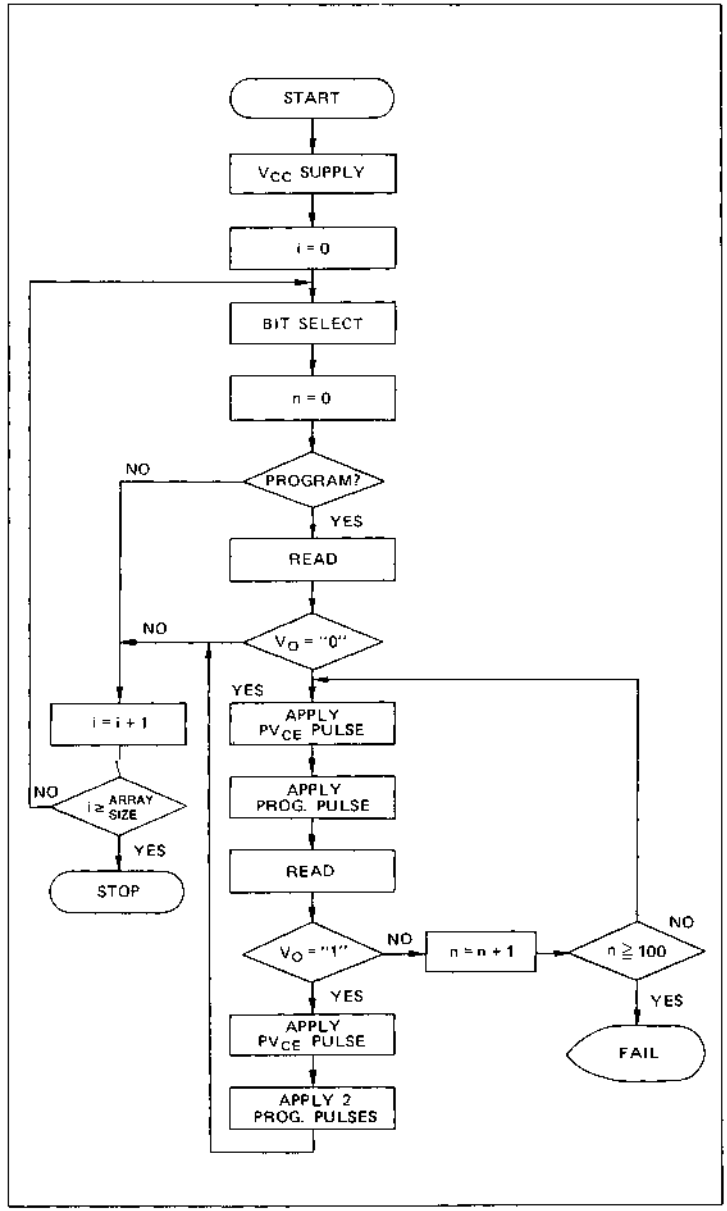
PROGRAMMING PROCEDURE

1. Apply power; V_{CC} = PV_{CC}, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 120 mA and duration of t_{PW} (10μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA}(2μs).

NOTE 1) Programming must be done bit by bit.

2) Ambient temperature during programming must be room temperature. (25°C ± 2°C).

PROGRAMMING FLOW CHART



PROGRAMMING SUPPORT

The Fujitsu MB71XX series is being supported by several commercial PROM Programmer manufacturers. Fujitsu, in order to guarantee not only programmability but long term reliability has an active program to qualify all PROM programmer manufacturer's products before they are approved. Data I/O, Toyo Telesonics and Stag have passed this qualification and information on their products which support the MB71XX family follows.

In order to support customers, Fujitsu Microelectronics will pre-program parts for qualification. Contact your local Fujitsu representative (see listing on page 7-11 for the location nearest you) for details.

DATA I/O REFERENCE CHART

Part Number	Array Size	Programming Module *909/919-xxxx	Socket Adapter
MB7122	1024 x 4	1488	1305-5
MB7128	2048 x 4	1488	1619
MB7132	1024 x 8	1488	1618-1
MB7138	2048 x 8	1488	1618-2
MB7142	4096 x 8	1488	715-0077-1

*Please note: Whether you use the 909 or 919 module is determined by which Data I/O model programmer you are using. (Contact Data I/O).

TOYO REFERENCE CHART

Part Number	Array Size	Programmer	Personality Module
MB7122	1024 x 4	PKW-7000	AD-7211
MB7128	2048 x 4	PKW-7000	AD-7211
MB7132	1024 x 8	PKW-7000	AD-7211
MB7138	2048 x 8	PKW-7000	AD-7211
MB7142	4096 x 8	PKW-7000	AD-7211

STAG REFERENCE CHART

Part Number	Array Size	Code	Adapter
MB7122	1024 x 4	75	AM 140-2
MB7128	2048 x 4	75	AM 140-3
MB7132	1024 x 8	75	AM 100-4
MB7138	2048 x 8	75	AM 100-5
MB7142	4096 x 8	75	—

FUJITSU MICROELECTRONICS
PROM CROSS REFERENCE GUIDE

SIZE: 4096 BITS **PINS: 18**
ORGANIZATION: 1024 X 4 **OUTPUT: OPEN COLLECTOR**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7121**
AMD	AM27S32
Fairchild	F93452
Harris	HM7642
Hitachi	HN25044
MMI	6352
Motorola	MCM7642
National	DM74S572
NEC	μPB406

SIZE: 4096 BITS **PINS: 18**
ORGANIZATION: 1024 X 4 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7122**
AMD	AM27S33C
Fairchild	93453C
Harris	HM7643A
Hitachi	HN25045
Intel	3625A
Intersil	IM5626
MMI	6353-1
Motorola	MCM7643C
National	74S573
NEC	μPB426
Raytheon	29641
Signetics	N82S137
TI	TBP24S41

SIZE: 4096 BITS **PINS: 20**
ORGANIZATION: 512 X 8 **OUTPUT: OPEN COLLECTOR**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7123**
Harris	HM7648
National	DM74S473

SIZE: 4096 BITS **PINS: 20**
ORGANIZATION: 512 X 8 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7124**
AMD	AM27S29
Harris	HM7649
National	DM74S472
Signetics	82S147
TI	TBP28S42

SIZE: 8192 BITS **PINS: 18**
ORGANIZATION: 2048 X 4 **OUTPUT: OPEN COLLECTOR**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7127**
Harris	HM7684
MMI	63100
National	DM87S184
Raytheon	29650
Signetics	82S184

SIZE: 8192 BITS **PINS: 18**
ORGANIZATION: 2048 X 4 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7128**
AMD	AM27S185C
Harris	HM7685
MMI	63101
Motorola	MCM7685C
National	87S185
Raytheon	29651/29653
Signetics	N82S185
TI	TBP24S81

SIZE: 8192 BITS **PINS: 24**
ORGANIZATION: 1024 X 8 **OUTPUT: OPEN COLLECTOR**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7131**
AMD	AM27S180
Fairchild	F93450
Harris	HM7680
Hitachi	HN25088
Intel	3608
MMI	6380
Signetics	82S180
Supertex	SM82S180

SIZE: 8192 BITS **PINS: 24**
ORGANIZATION: 1024 X 8 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7132**
AMD	AM27S181C
Fairchild	93451C
Harris	HM7681A
Hitachi	HN25089
Intel	3628
MMI	6381-1
Motorola	MCM7681C
National	87S181
Raytheon	29631
Signetics	N82S181
Supertex	SM82S181
TI	TBP28S86

SIZE: 16384 BITS **PINS: 20**
ORGANIZATION: 4096 X 4 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7137**
Fairchild	93510
Harris	HM76160
Intel	3616
National	DM87S190

SIZE: 16384 BITS **PINS: 24**
ORGANIZATION: 2048 X 8 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7138**
AMD	AM27S191C
Fairchild	93511C
Harris	HM76161
Hitachi	HN25169
Intel	3636
MMI	63S1681
National	87S191
NEC	μPB429
Raytheon	29681
Signetics	N82S191
Supertex	SM82S191
TI	TBP28S166

SIZE: 32768 BITS **PINS: 24**
ORGANIZATION: 4096 X 8 **OUTPUT: 3-STATE**

MANUFACTURER	PART NUMBER
FUJITSU	**MB7142**
Harris	HM76321
Intel	3632
Signetics	N82S321

HIGH SPEED SCHOTTKY TTL 4096-BIT PROMS

DESCRIPTION

The Fujitsu MB7121 and MB7122 are high speed Schottky TTL electrically field programmable read only memories. With open collector outputs on the MB7121 and three-state outputs on the MB7122, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

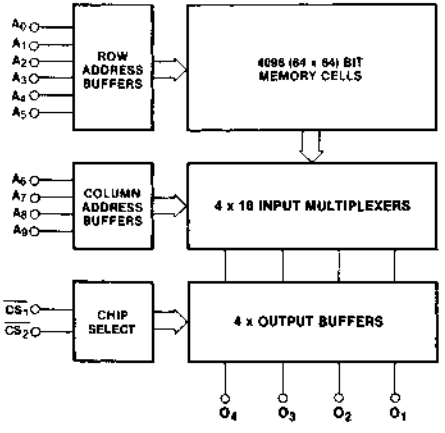
The sophisticated Schottky TTL process enables small chip size and fast access times.

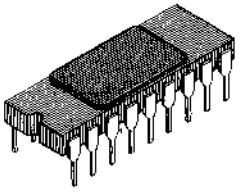
The extra test cells and unique testing methods provide extremely high programmability.

FEATURES

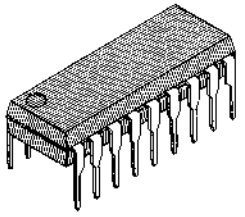
- **Organization as 1024 words by 4-bits, fully decoded**
- **TTL compatible input/output**
- **Fast access time:**
  - **MB7121E/MB7122E:**
    - **45ns Max.**
    - **25ns Typ.**
  - **MB7121H/MB7122H:**
    - **35ns Max.**
    - **25ns Typ.**
- **Low power dissipation: 150mA max.**
- **Single +5V supply voltage**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Low current PNP inputs**
- **Simplified and lower power programming**
- **MB7121: Open collector outputs**
- **MB7122: Three-state outputs**
- **Two chip enable leads for easy memory expansion**
- **Jedec standard 18-pin DIP package**
- **MB7121 pin compatible with industry standard products: 27S32, 7642, 6350, 93452, 74S477, 74S572, μPB406**
- **MB7122 pin compatible with industry standard products: 82S137, 7643, 6353-1, 93453, 36453, 3625, DM74S573, 29641, μPB426**

MB7121/MB7122 BLOCK DIAGRAM



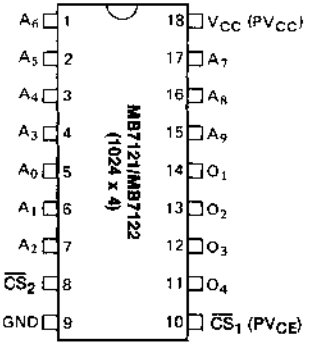


CERAMIC PACKAGE
DIP-18C-F02



PLASTIC PACKAGE
DIP-18P-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

(See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input Voltage		V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input Current		I_{IN}	−20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{stg}	−65 to +150	°C
	Plastic		−40 to +125	
Output Voltage		V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)		I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16 mA)		V_{OL}	—	—	0.50	V
Output Leakage Current	MB7121	I_{OLK}	—	—	40	μA
(V_O = 2.4V, chip disable from a low)	MB7122	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.5V, chip disabled from a high)	MB7122	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)		V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	105	150	mA
Output High Voltage (I_O = −2.4mA)	MB7122	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB7122	I_{OS}*	−15	—	−60	mA

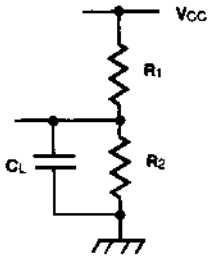
* **Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{CE} = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7121E/MB7122E		MB7121H/MB7122H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	25	45	25	35	ns
Output Disable Time	t_{DIS}	—	30	—	30	ns
Output Enable Time	t_{EN}	—	30	—	30	ns

AC TEST CONDITIONS

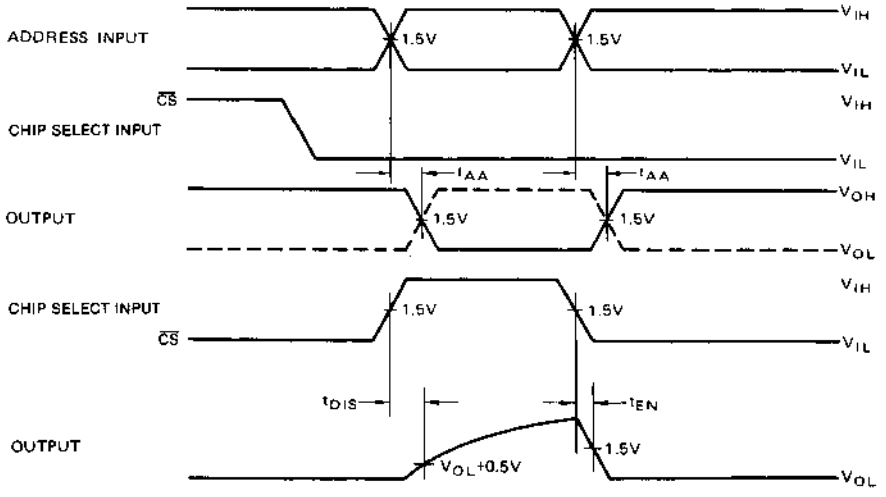


INPUT CONDITIONS

Amplitude	**0V to 3V**
Rise and Fall Time	**5 ns from 1V to 2V**
Frequency	**1 MHz**

MB7121/MB7122		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



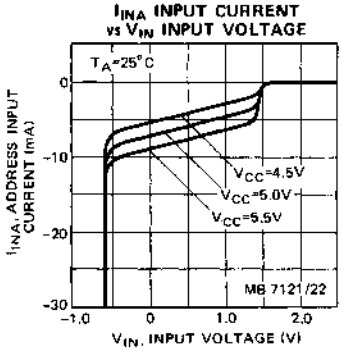
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

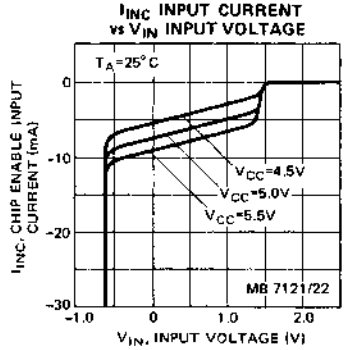
CAPACITANCE

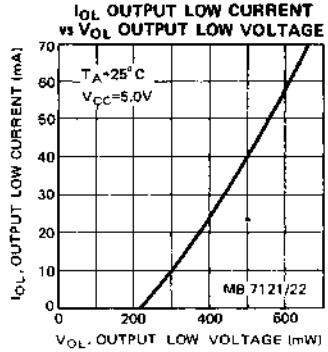
(f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

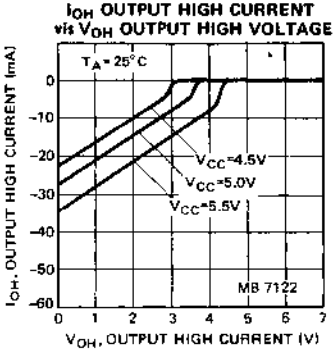
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	12	pF

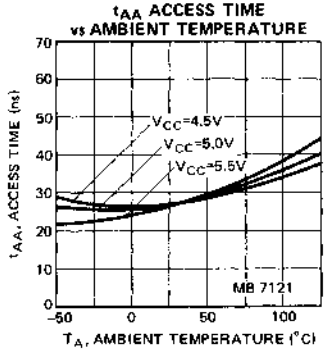
TYPICAL CHARACTERISTICS CURVES

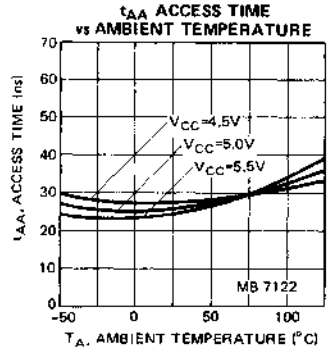


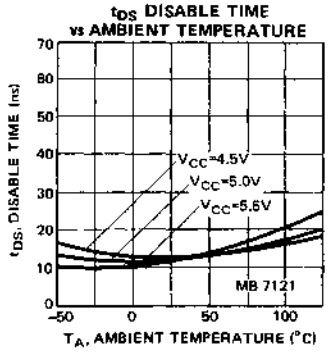


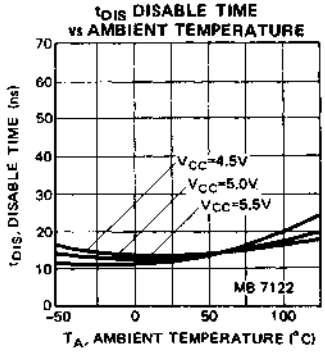


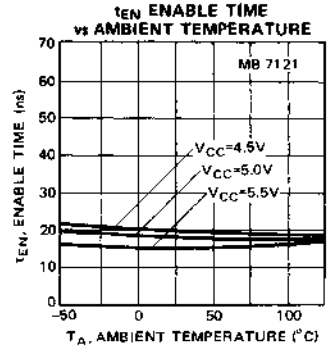




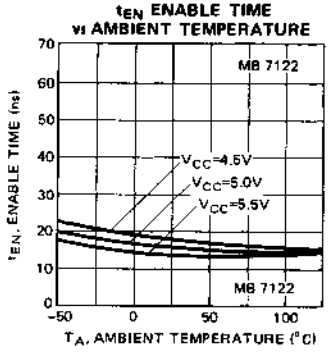


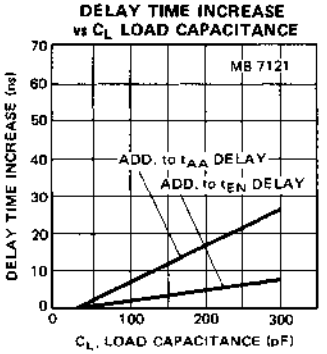


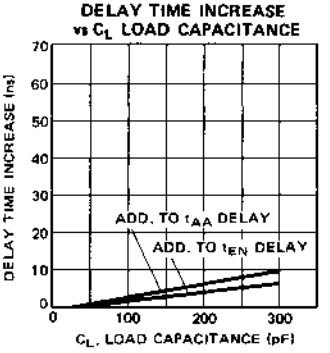




TYPICAL CHARACTERISTICS CURVES (Continued)







INPUT/OUTPUT CIRCUIT INFORMATION

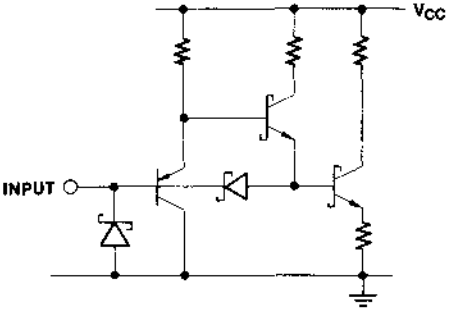
INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

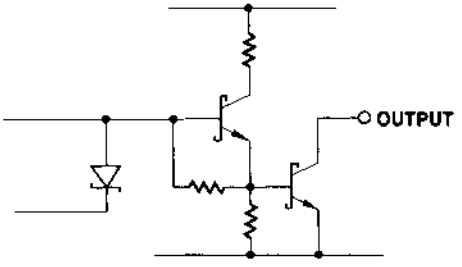
OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7122 (3-state) compared to 0mA for the MB7121 (open-collector).

MB7121/MB7122 INPUT CIRCUIT



MB7121 OUTPUT CIRCUIT



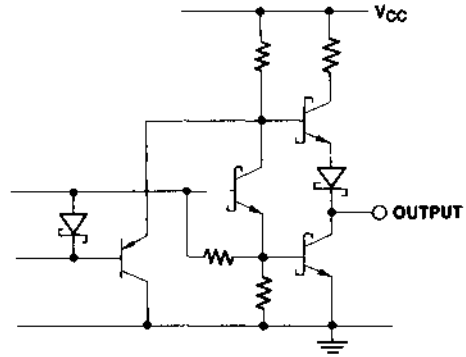
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized system.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Select circuit.

MB7122 OUTPUT CIRCUIT



MB7121/MB7122 BIT MAP

	A_8 A_7 A_6 A_9
O_1	0 0 0 0 ≀ 1 1 1 0
O_2	0 0 0 0 ≀ 1 1 1 0
O_3	0 0 0 0 ≀ 1 1 1 0
O_4	0 0 0 0 ≀ 1 1 1 0

A_5	1	1
A_2	0	1
A_4	0	1
A_1	0	1
A_0	0	1
A_3	0	1
	~	

Multiplexer

A_8	A_7	A_6	A_9
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

Decoder/Driver

A_5	10011001	10011001	10011001	10011001	10011001	10011001	10011001	10011001
A_2	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_4	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_1	00000000	11111111	00000000	11111111	00000000	11111111	00000000	11111111
A_0	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_3	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111

HIGH SPEED SCHOTTKY TTL 4096-BIT PROM

DESCRIPTION

The Fujitsu MB7123 and MB7124 are high speed Schottky TTL electrically field programmable read only memories. Uncommited collector outputs and three-state outputs are provided for easy memory expansion.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutetic Aluminum Process) during simple programming procedures.

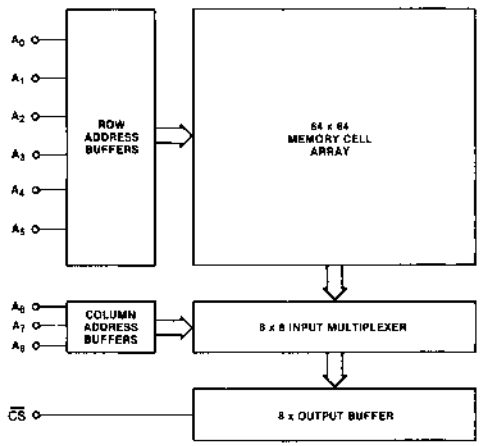
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon), and SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process enable small chip size and fast access time.

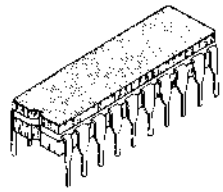
The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC, and programming tests prior to shipment. This results in extremely high programmability.

FEATURES

- **Organization:**
  512 words by 8-bits
- **TTL compatible input/output**
- **Fast access times:**
  MB7123E/MB7124E:
  45 ns max.
  MB7123H/MB7124H:
  35 ns max.
- **Low Power Dissipation:**
  170 mA Max.
- **Open collector outputs on MB7123**
- **Three-state outputs on MB7124**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **One chip enable lead for easy memory expansion**
- **Standard 20-pin DIP package**
- **MB7124 is pin compatible with AM27S28 and N82S147**

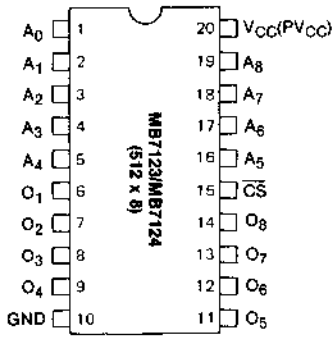
MB7123/MB7124 BLOCK DIAGRAM





CERDIP PACKAGE
DIP-20C-C01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)		I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16mA)		V_{OL}	—	—	0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled from a low)	MB7124	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.45V, chip disabled from a high)	MB7124	I_{OIL}	—	—	−40	μA
Output Leakage Current (V_O = 2.4V, chip disabled) (Open Collector)	MB7123	I_{OLK}	—	—	40	μA
Input Clamp Voltage (I_{IN} = −18mA)		V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	120	170	mA
Output High Voltage (I_O = −2.4mA)	MB7124	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB7124	I_{OS}*	−15	—	−60	mA

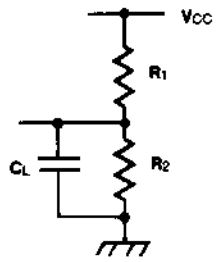
***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless othewise noted.

Parameter	Symbol	MB7123E/MB7124E		MB7123H/MB7124H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	25	45	25	35	ns
Output Disable Time	t_{DIS}	15	30	15	30	ns
Output Enable Time	t_{EN}	15	30	15	30	ns

AC TEST CONDITIONS

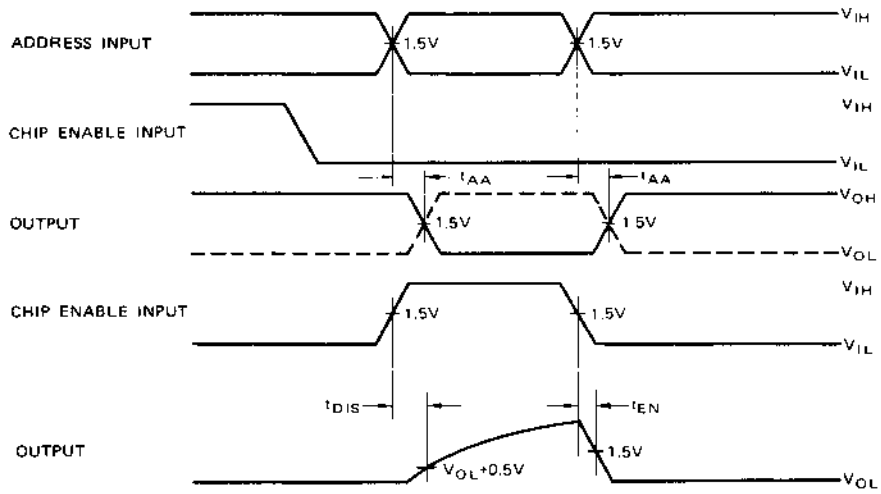


INPUT CONDITIONS

Amplitude	**0V to 3V**
Rise and Fall Time	**5 ns from 1V to 2V**
Frequency	**1 MHz**

MB7123/MB7124		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE

(f = 1MHz, V_{CC} = +5V, V_{IN} = +2V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	12	pF

MB7127E/H
MB7128E/H

HIGH SPEED SCHOTTKY TTL 8192-BIT PROM

DESCRIPTION

The Fujitsu MB7127/MB7128 are high speed Schottky TTL electrically field programmable read only memories. With open collector outputs on the MB7127 and three-state outputs on the MB7128, memory expansion is simple.

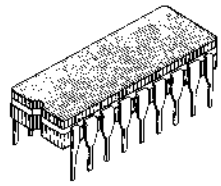
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutetic Aluminum Process) during a simple programming procedure.

The sophisticated Schottky TTL process enables small chip size and fast access time.

The extra test cells and unique testing methods provide extremely high programmability.

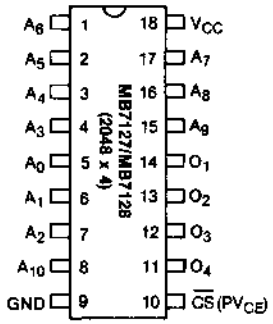
FEATURES

- **Organization:**
  2048 words by 4-bits
- **TTL compatible input/output**
- **Fast access time:**
  MB7127E/MB7128E:
  55 ns Max.
  30 ns Typ.
  MB7127H/MB7128H:
  45 ns Max.
  30 ns Max.
- **Low Power Dissipation:**
  155 mA Max.
- **Single +5V supply voltage**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **MB7127: Open collector outputs**
- **MB7128: Three-state outputs**
- **Chip select leads for easy memory expansion**
- **Standard 18-pin DIP package**
- **MB7128 pin is compatible with industry standard products: 82S185, HM7685, 63S841, 27S185**
- **MB7127 pin compatible with 82S184, HM7684, 63S840, 27S184**



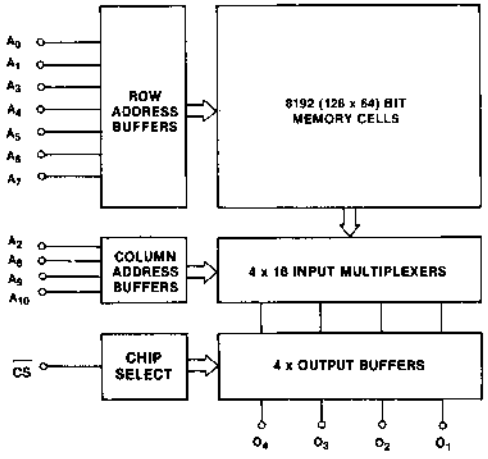
CERDIP PACKAGE
DIP-18C-C01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7127/MB7128 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to 5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)	I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)	I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)	I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16 mA)	V_{OL}	—	—	0.50	V
Output Leakage Current (V_{OL} = 2.4V, chip disabled from a low)	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.45V, chip disabled from a high)	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)	V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	I_{CC}	—	110	155	mA
Output High Voltage (I_O = −2.4mA)	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	I_{OS}*	−1.5	—	−60	mA

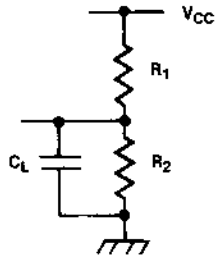
***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7127E/MB7128E		MB7127H/MB7128H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	30	55	30	45	ns
Output Disable Time	t_{DIS}	—	40	—	30	ns
Output Enable Time	t_{EN}	—	40	—	30	ns

AC TEST CONDITIONS

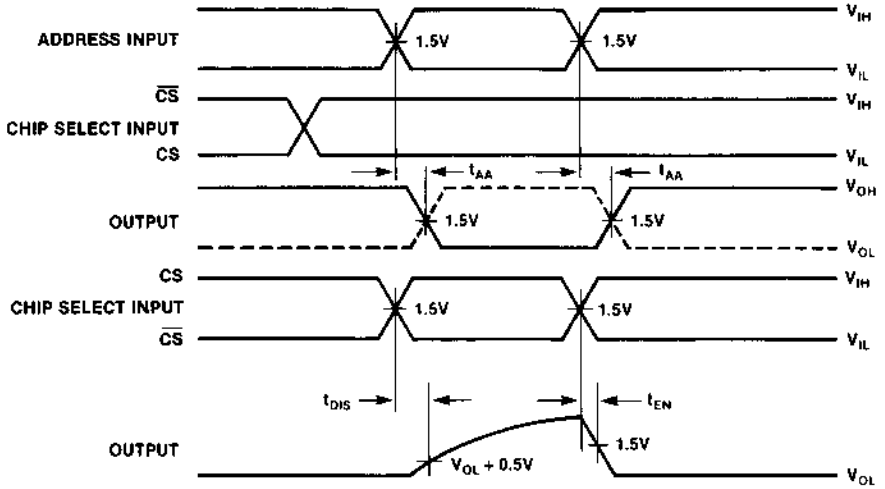


INPUT CONDITIONS

Amplitude	0V to 3V
Rise and Fall Time	5 ns from 1V to 2V
Frequency	1 MHz

MB7127/MB7128		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



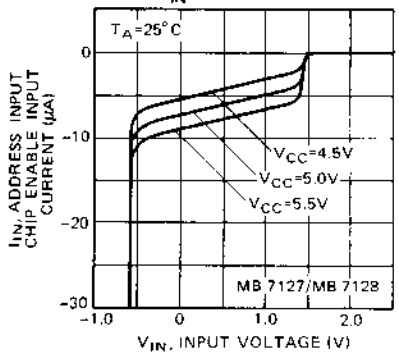
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

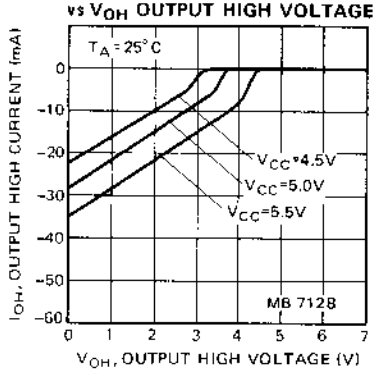
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

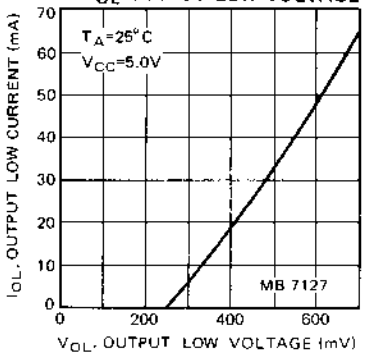
I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



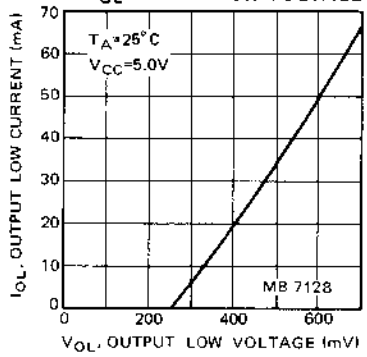
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



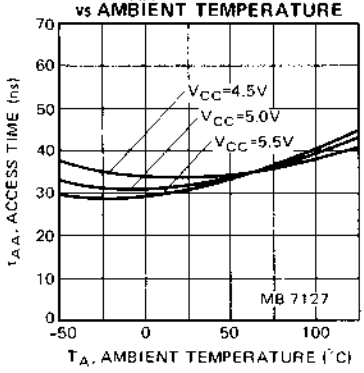
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



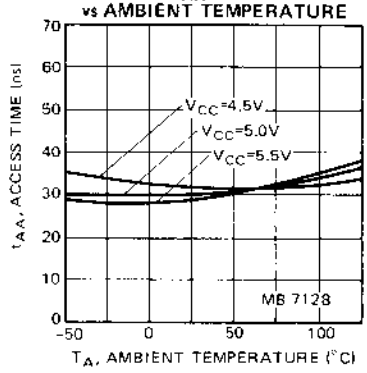
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

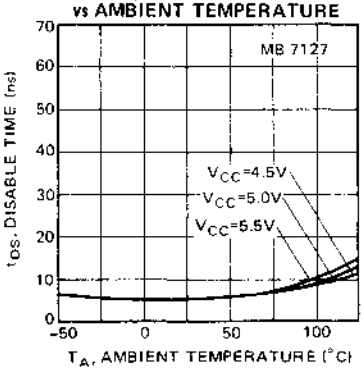


t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

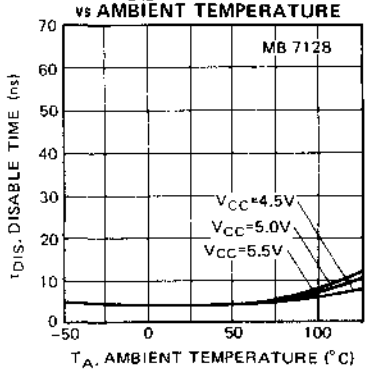


TYPICAL CHARACTERISTICS CURVES (Continued)

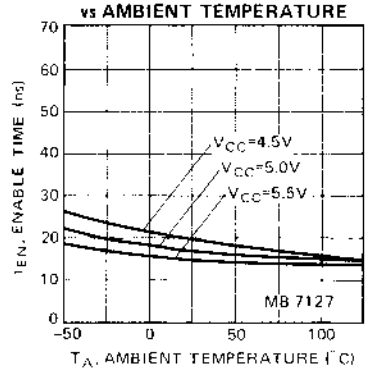
t_{OS} DISABLE TIME vs AMBIENT TEMPERATURE



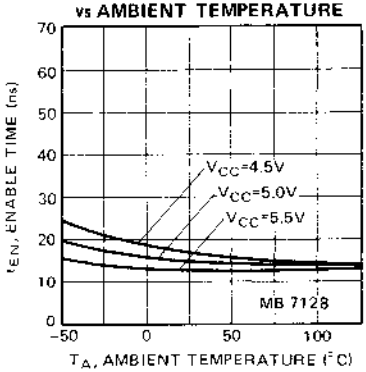
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



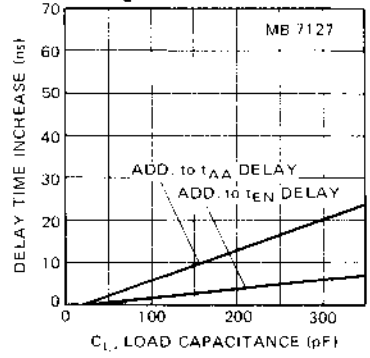
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



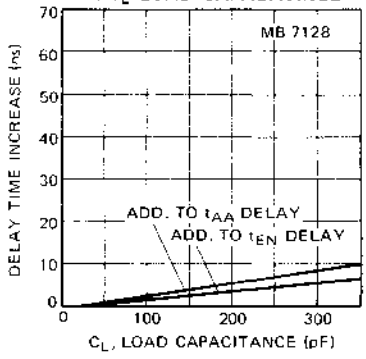
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Shottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL-totem pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7128 (3-state) compared to 0mA for the MB7127 (open collector).

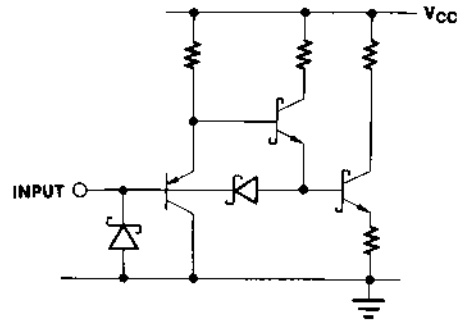
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH, and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a defineable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line drive capacity), plus the ability to connect to bus-organized systems.

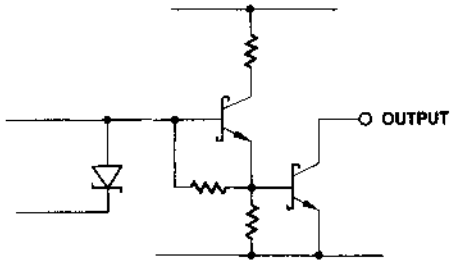
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease load on the Chip Enable circuit.

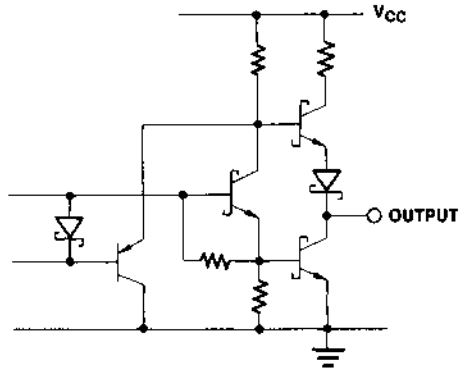
MB7127/MB7128 INPUT CIRCUIT



MB7127 OUTPUT CIRCUIT



MB7128 OUTPUT CIRCUIT



MB7127/MB7128 BIT MAP

	A_8 A_9 A_2 A_{10}
O_1	0 0 0 0 ≀ 1 1 1 0
O_2	0 0 0 0 ≀ 1 1 1 0
O_3	0 0 0 0 ≀ 1 1 1 0
O_4	0 0 0 0 ≀ 1 1 1 0

A_7	0	0
A_6	0	0
A_5	0	1
A_4	1	0
A_1	0	1
A_0	0	1
A_3	0	1

Multiplexer

A_8	A_9	A_2	A_{10}
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

Decoder/Driver

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111

FUJITSU
MICROELECTRONICS

MB7130E
MB7130H

HIGH SPEED SCHOTTKY TTL 8192-BIT PROM

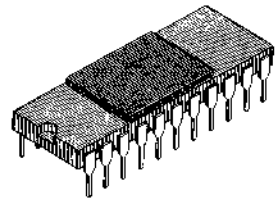
DESCRIPTION

The Fujitsu MB7130 is a high speed Schottky TTL electrically field programmable read only memory organized as 1024 words by 8-bits. With three-state outputs on the MB7130, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon), with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming tests prior to shipment. This results in extremely high programmability.

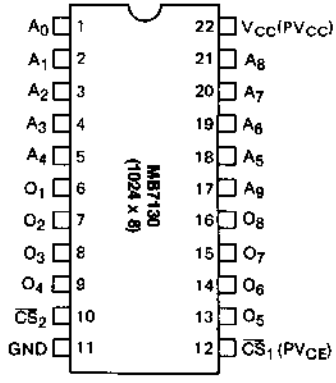


CERAMIC PACKAGE
DIP-22C-F01

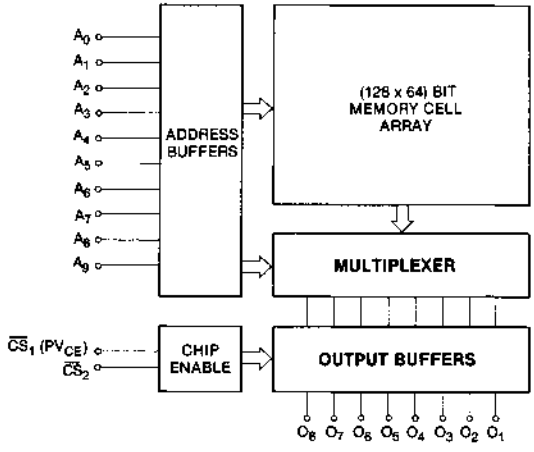
FEATURES

- **Organization: 1024 words by 8-bits, fully decoded**
- **TTL compatible inputs/output**
- **Fast Access Time:**
  MB7130E: 55 ns Max.
  30 ns Typ.
  MB7130H: 45 ns Max.
  30 ns Typ.
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Single +5V supply voltage**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Simplified and lower power programming**
- **Three-state outputs**
- **Two chip enable leads for simplified memory expansion**
- **Standard 22-pin DIP package**

PIN ASSIGNMENT



MB7130 BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to +V_{CC}	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

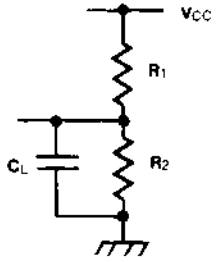
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)	I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)	I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)	I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16 mA)	V_{OL}	—	—	0.50	V
Output Leakage Current (V_{OL} = 2.4V, chip disabled from a low)	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.45V, chip disabled from a high)	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)	V_{IC}	—	—	1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	I_{CC}	—	125	175	mA
Output High Voltage (I_O = −2.4mA)	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	I_{OS}*	15	—	−60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7130E		MB7130H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	30	55	30	45	ns
Output Disable Time	t_{DIS}	—	40	—	30	ns
Output Enable Time	t_{EN}	—	40	—	30	ns



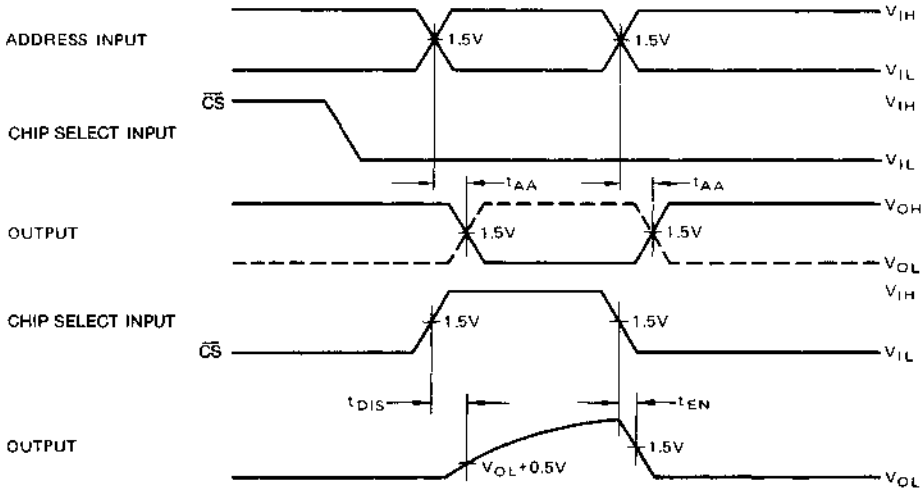
AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude	0V to 3V
Rise and Fall Time	5 ns from 1V to 2V
Frequency	1 MHz

MB7130		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



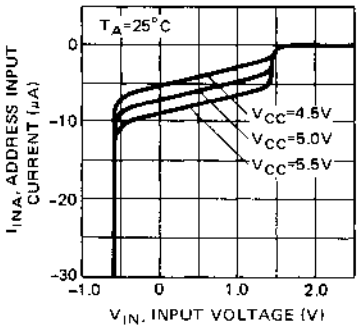
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

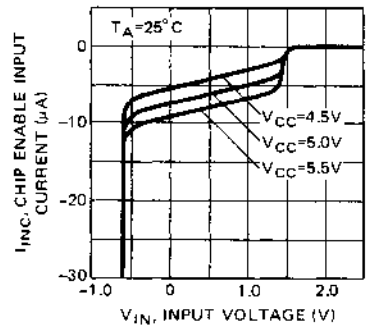
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

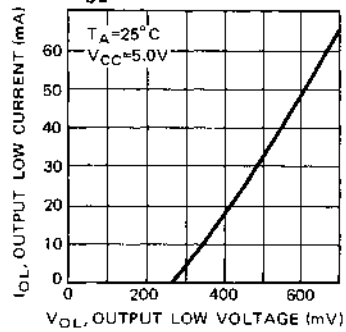
I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



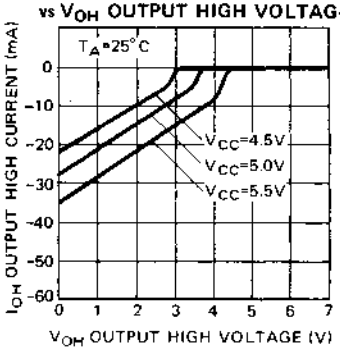
I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



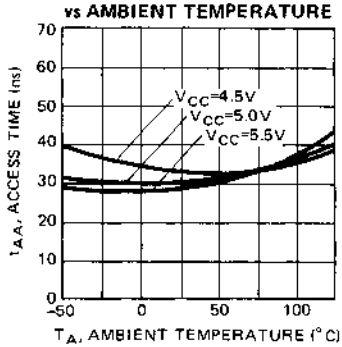
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



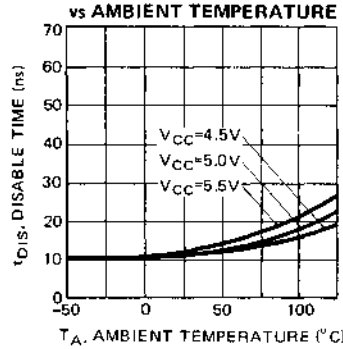
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



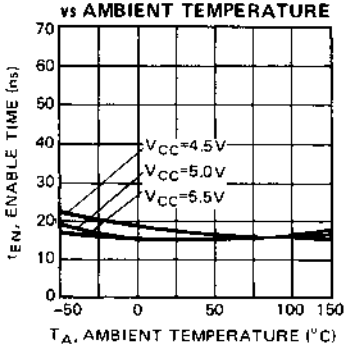
t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE



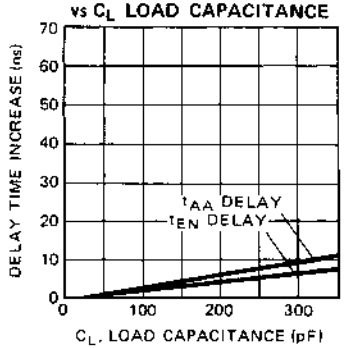
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

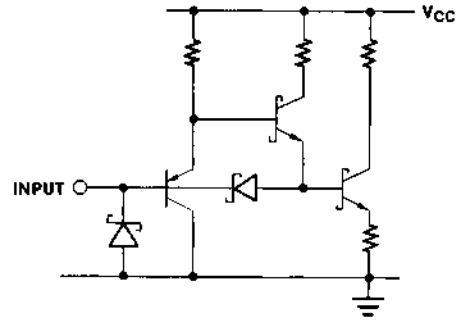
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

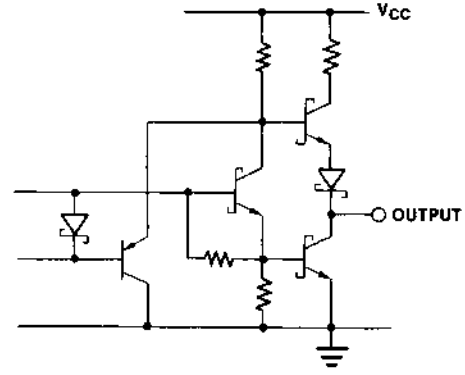
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Enable circuit.

MB7130 INPUT CIRCUIT



MB7130 OUTPUT CIRCUIT



MB7131E/H
MB7132E/H

HIGH SPEED SCHOTTKY TTL 8192-BIT PROMS

DESCRIPTION

The Fujitsu MB7131 and MB7132 are high speed Schottky TTL electrically field programmable read only memories. With open collector outputs on the MB7131 and three-state outputs on the MB7132, memory expansion is simple.

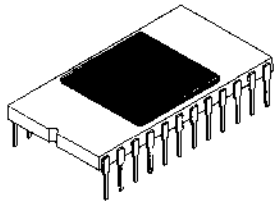
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutetic Aluminum Process) during simple programming procedure.

The sophisticated Schottky TTL process enables small chip size and fast access time.

The extra test cells and unique testing methods provide extremely high programmability.

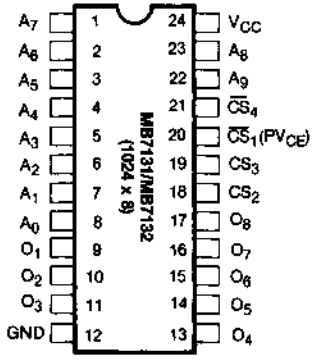
FEATURES

- **Organization: 1024 words by 8-bits**
- **TTL compatible input/output**
- **Fast access time:**
  - **MB7131E/MB7132E:**
    - **55 ns Max.**
    - **30 ns Typ.**
  - **MB7131H/MB7132H:**
    - **45 ns Max.**
    - **30 ns Max.**
- **Low Power Dissipation:**
  - **175 mA Max.**
- **Single +5V supply voltage**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **MB7131: Open collector outputs**
- **MB7132: Three-state outputs**
- **Chip select leads for easy memory expansion**
- **Standard 24-pin DIP package**
- **MB7131 pin compatible with 82S180, 6380, HM7680, 93450, 3608, 27S180**
- **MB7132 pin is compatible with industry standard products: 82S181, HM7681, 6381-1, 28S86, 93451, 3628**

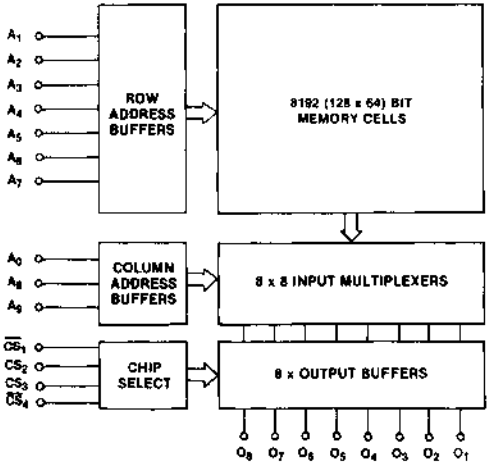


CERAMIC PACKAGE
DIP-24C-A01

PIN ASSIGNMENT



MB7131/MB7132 BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	μA
Input Load Current (V_{IL} = 0.45V)		I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16mA)		V_{OL}	—	—	0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled from a low)	MB7131	I_{OLK}	—	—	40	μA
	MB7132	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.5V, chip disabled from a low	MB7132	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)		V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	125	175	mA
Output High Voltage(I_O = −2.4mA	MB7132	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB7132	I_{OS}*	−15	—	−60	mA

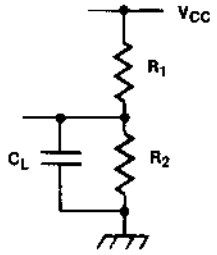
* **Note:** Denotes guaranteed characteristics of output high-level (ON) state when the chip enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7131E/MB7132E		MB7131H/MB7132H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	30	55	30	45	ns
Output Disable Time	t_{DIS}	—	40	—	30	ns
Output Enable Time	t_{EN}	—	40	—	30	ns

AC TEST CONDITIONS

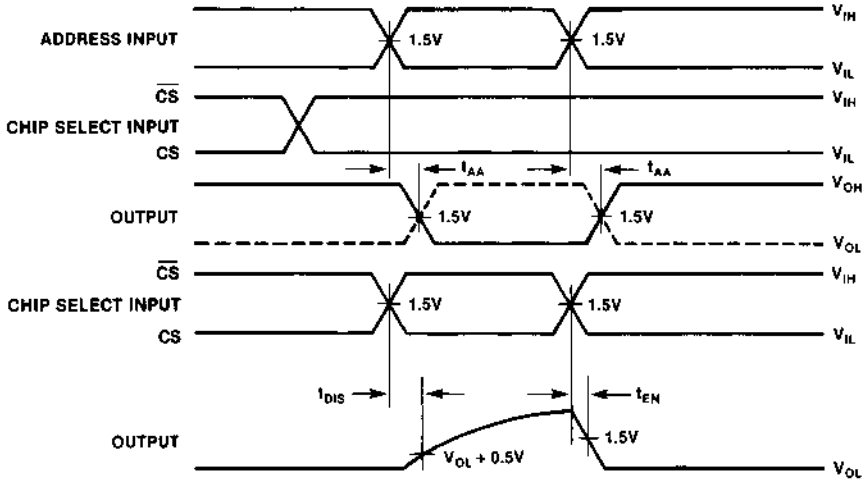


INPUT CONDITIONS

Amplitude	0V to 3V
Rise and Fall Time	5 ns from 1V to 2V
Frequency	1 MHz

MB7131/MB7132		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



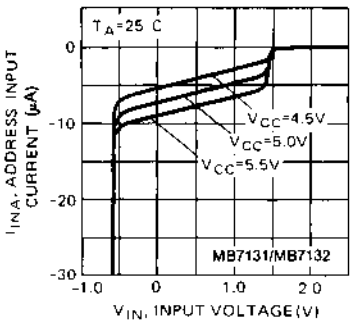
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE ($f = 1MHz$, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

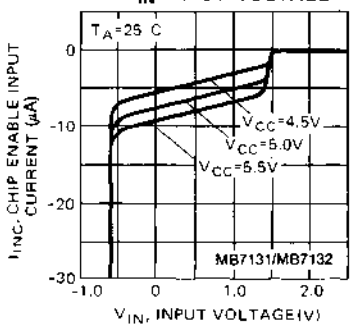
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

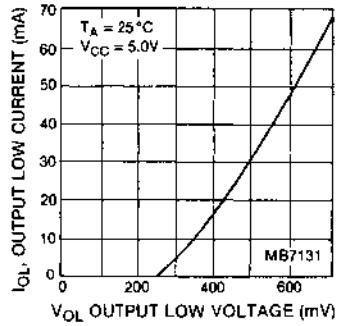
I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



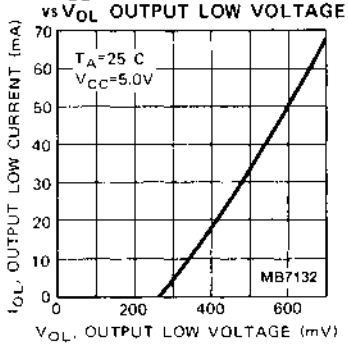
I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



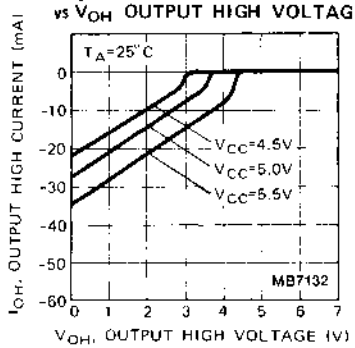
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



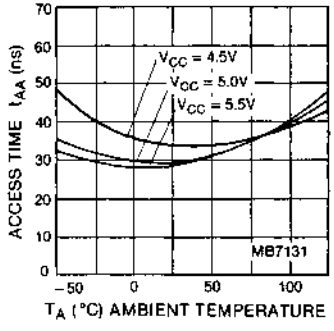
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



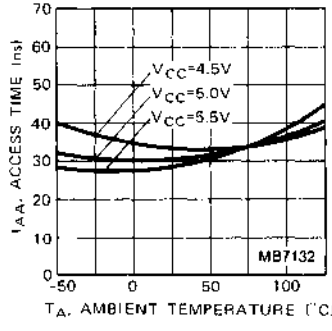
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



t_{AA} ACCESS TIME vs T_A AMBIENT TEMPERATURE

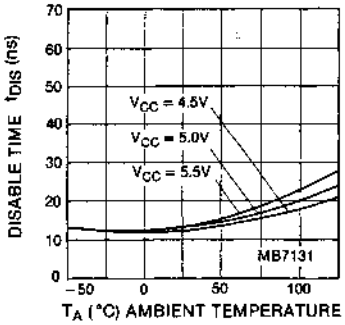


t_{AA} ACCESS TIME vs T_A AMBIENT TEMPERATURE

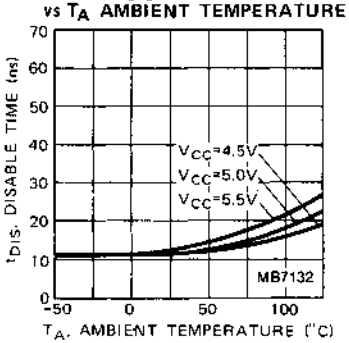


TYPICAL CHARACTERISTICS CURVES (Continued)

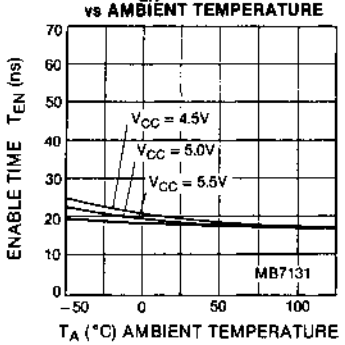
t_{DIS} DISABLE TIME vs T_A AMBIENT TEMPERATURE



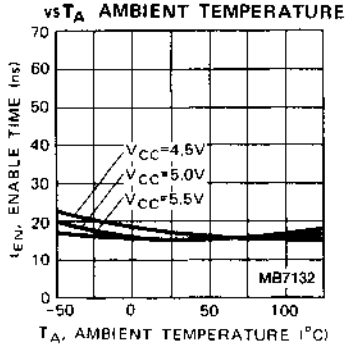
t_{DIS} DISABLE TIME vs T_A AMBIENT TEMPERATURE



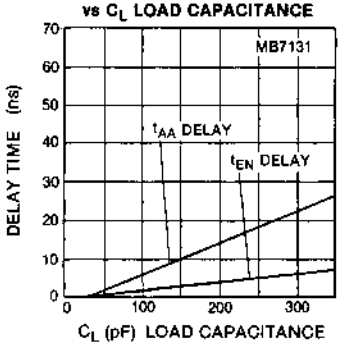
T_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



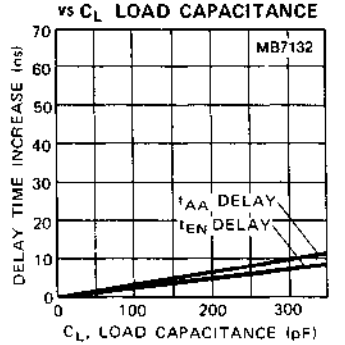
t_{EN} ENABLE TIME vs T_A AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

The open-collector is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to impedance low-level is typically 30mA for the MB7132 (3-state) compared to 0mA for the MB7131 (open collector).

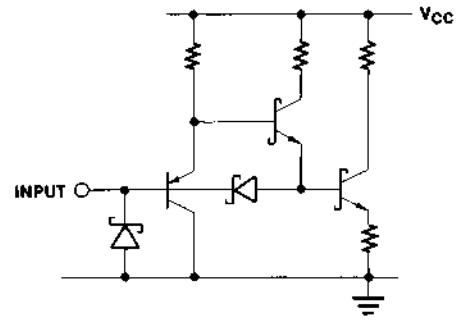
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH, and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a defineable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line drive capacity), plus the ability to connect to bus-organized systems.

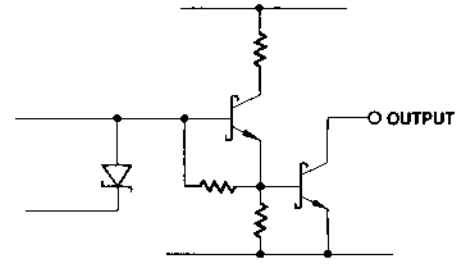
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease load on the Chip Select circuit.

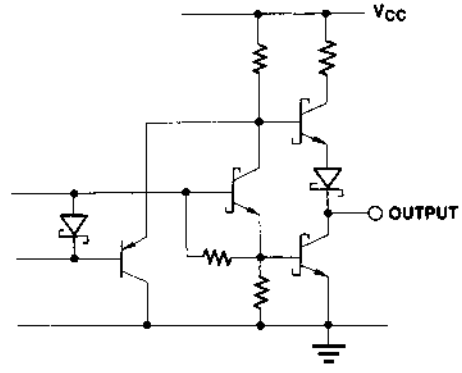
MB7131/MB7132 INPUT CIRCUIT



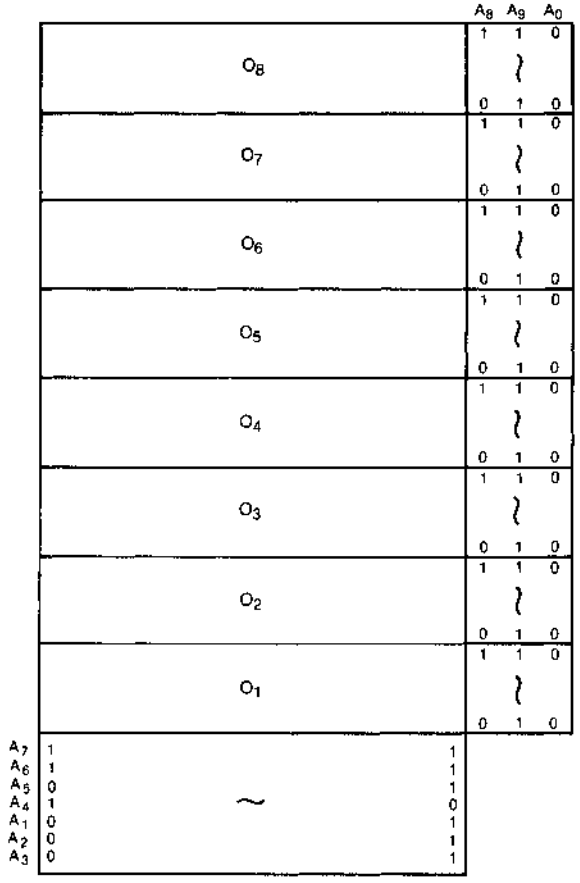
MB7131 OUTPUT CIRCUIT



MB7132 OUTPUT CIRCUIT



MB7131/MB7132 BIT MAP



Multiplexer

A_8	A_9	A_0
1	1	0
1	1	1
1	0	1
1	0	0
0	0	0
0	0	1
0	1	1
0	1	0

Decoder/Driver

A_7	10011001	10011001	10011001	10011001	10011001	10011001	10011001	10011001
A_6	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_2	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

A_7	10011001	10011001	10011001	10011001	10011001	10011001	10011001	10011001
A_6	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	111111 11	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_2	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111

HIGH SPEED SCHOTTKY TTL 16,384-BIT PROM

DESCRIPTION

The Fujitsu MB7134 is a high speed Schottky TTL electrically field programmable read only memory organized as 4096 words by 4-bits. With three-state outputs on the MB7134, memory expansion is simple.

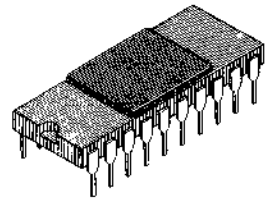
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming tests prior to shipment. This results in extremely high programmability.

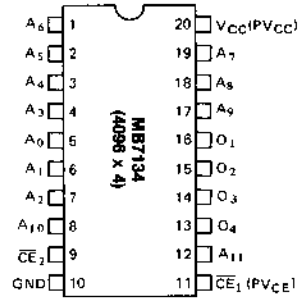
FEATURES

- **Organization: 4096 words by 4-bits, fully decoded**
- **TTL compatible inputs/output**
- **Fast Access Time:**
  MB7134E: 55 ns max.
  35 ns typ.
  MB7134H: 45 ns max.
  35 ns typ.
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Single +5V supply voltage**
- **Low Current PNP Inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Simplified and lower programming**
- **Three-state outputs**
- **Two chip enable leads for simplified memory expansion**
- **Standard 20-pin DIP package**



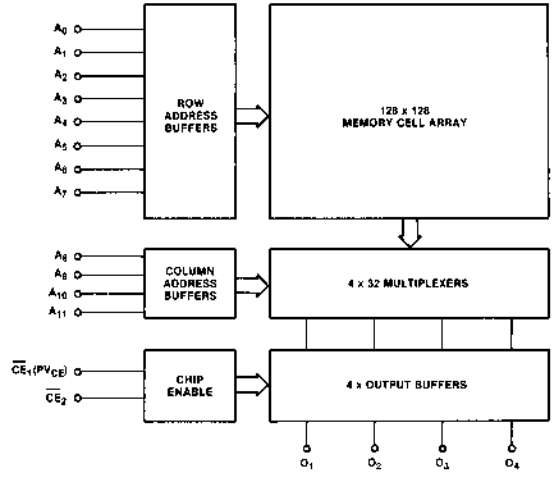
CERAMIC PACKAGE
DIP-20C-F01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due tl high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7134 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)	I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)	I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)	I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16mA)	V_{OL}	—	—	0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled from a low)	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.5V, chip disabled from a low)	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)	V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	I_{CC}	—	120	170	mA
Output High Voltage (I_O = −2.4mA)	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	I_{OS}*	−15	—	−60	mA

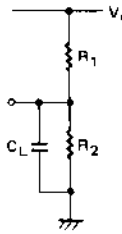
* **Note:** Denotes guaranteed characteristics of output high-level (ON) state when the chip enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7134E		MB7134H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	35	55	35	45	ns
Output Disable Time	t_{DIS}	—	40	—	40	ns
Output Enable Time	t_{EN}	—	40	—	40	ns

AC TEST CONDITIONS

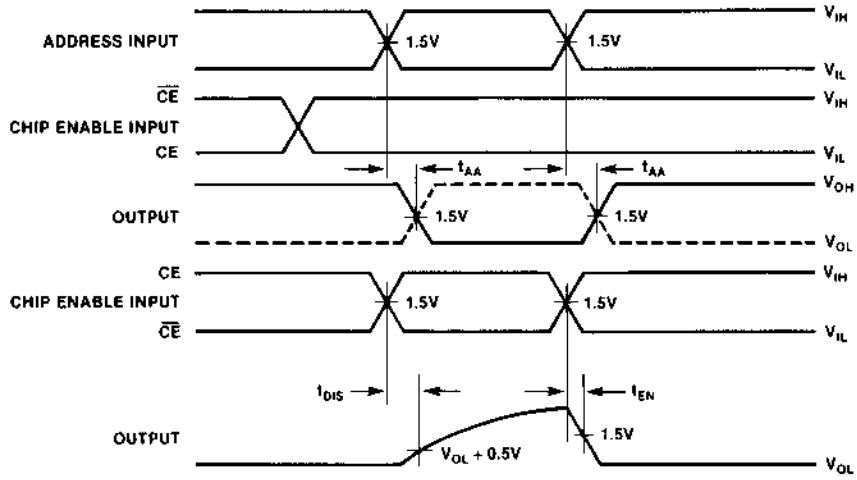


INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

MB 7134		
R_1	R_2	C_L
470Ω	1KΩ	30pF

OPERATION TIMING DIAGRAM



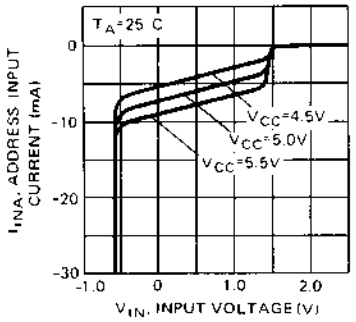
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

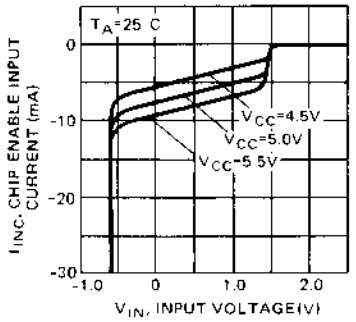
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

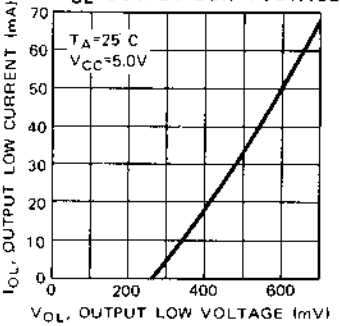
I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



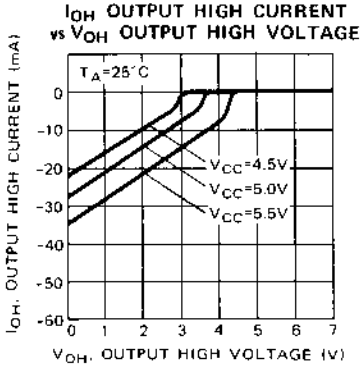
I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



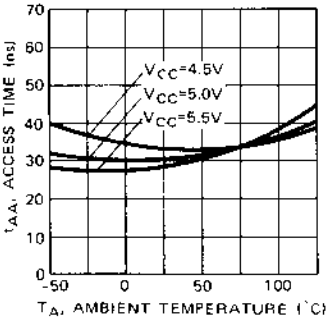
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



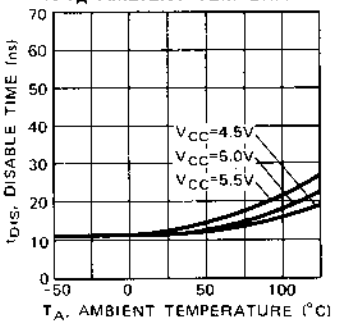
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



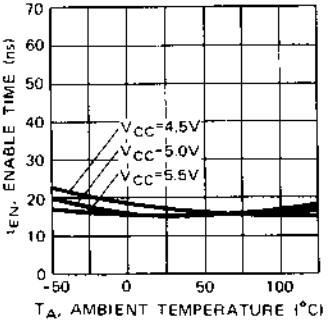
t_{AA} ACCESS TIME vs T_A AMBIENT TEMPERATURE



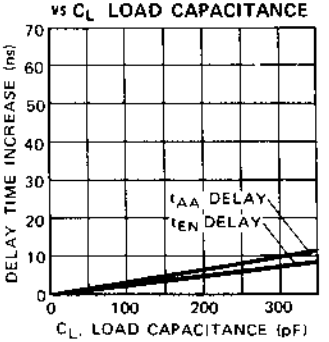
t_{DIS} DISABLE TIME vs T_A AMBIENT TEMPERATURE



t_{EN} ENABLE TIME vs T_A AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

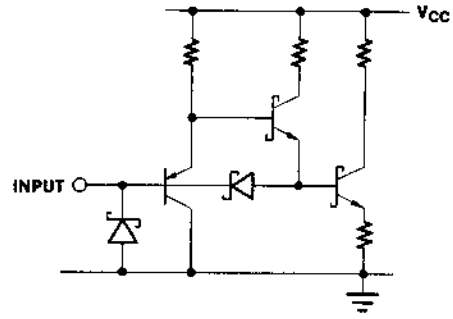


INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

MB7134 INPUT CIRCUIT



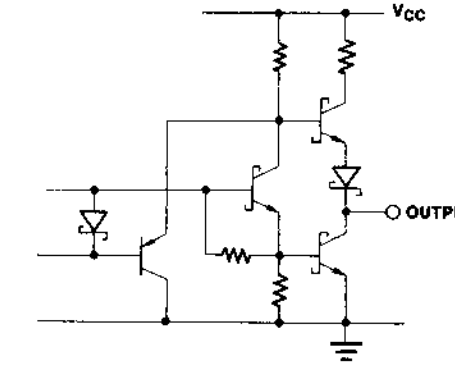
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Enable circuit.

MB7134 OUTPUT CIRCUIT



MB7137E/H
MB7138E/H

HIGH SPEED SCHOTTKY TTL 16,384-BIT PROM

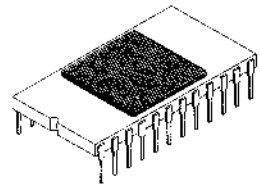
DESCRIPTION

The Fujitsu MB7137/MB7138 are high speed Schottky TTL electrically field programmable read only memories. With open collector outputs on the MB7137 and three-state outputs on the MB7138, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process enables small chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming tests prior to shipment. This results in extremely high programmability.

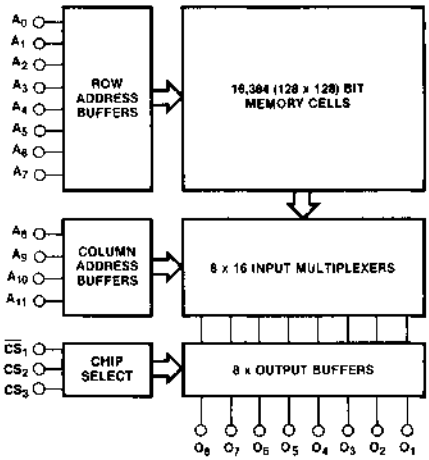


CERAMIC PACKAGE
DIP-24C-A01

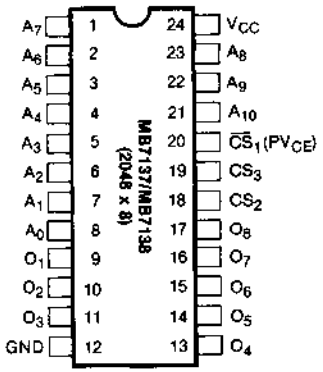
FEATURES

- **Organization: 2048 words x bits**
- **Fast Access Time:**
  MB7137E/MB7138E:
  55ns Max.
  35ns Typ.
  MB7137H/MB7138H:
  45ns Max.
  35ns Typ.
- **TTL compatible input/output**
- **AC characteristics are guaranteed over full operating voltage and temperature ranges via unique testing techniques**
- **Low power dissipation: 180mA max.**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **MB7137: Open collector outputs**
- **MB7138: Three-state outputs**
- **Three Chip Select leads for easy memory expansion**
- **Standard 24-pin DIP package**
- **MB7138 pin compatible with industry standard products: HM76161, 3636, 28S166, 82S191, 93511**
- **MB7137 pin compatible with: 82S190, 27S190, 98510, HM76160**

MB7137/MB7138 BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)		I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}	—	—	0.50	V
Output Leakage Current (V_O = 2.4V, chip disable from a low)	MB7137	I_{OLK}	—	—	40	μA
	MB7138	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.5V, chip disabled from a low)		I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)		V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND		I_{CC}	—	130	180	mA
Output High Voltage (I_O = −2.4mA)	MB7138	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND	MB7138	I_{OS}*	−15	—	−60	mA

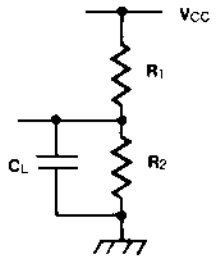
* **Note:** Denotes guaranteed characteristics of output high-level (ON) state when the chip enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7137E/MB7138E		MB7137H/MB7138H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	35	55	35	45	ns
Output Disable Time	t_{DIS}	—	40	—	40	ns
Output Enable Time	t_{EN}	—	40	—	40	ns

AC TEST CONDITIONS

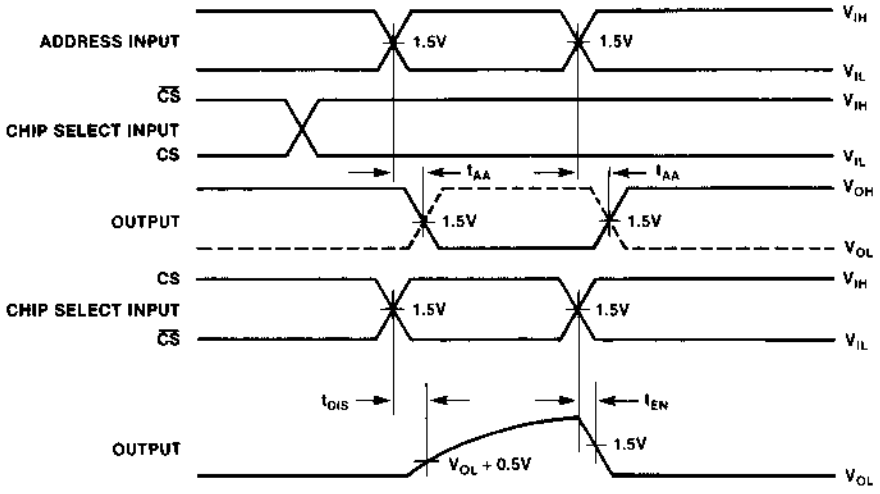


INPUT CONDITIONS

Amplitude	0V to 3V
Rise and Fall Time	5 ns from 1V to 2V
Frequency	1 MHz

MB7137/MB7138		
R_1	R_2	C_L
470Ω	1000Ω	30pF

OPERATION TIMING DIAGRAM



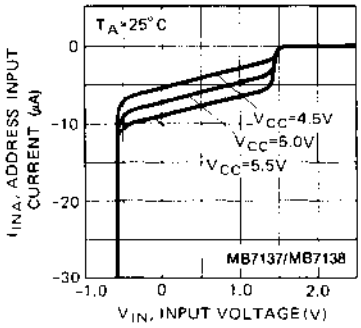
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

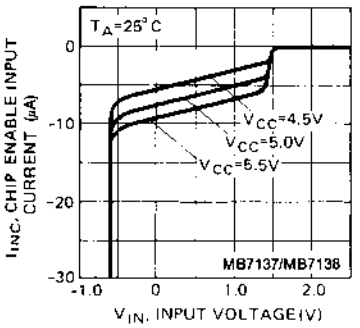
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

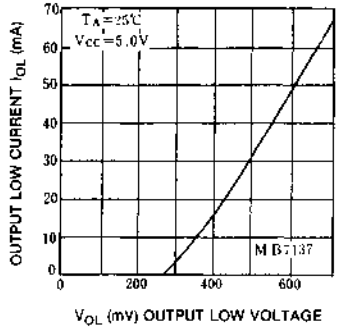
I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



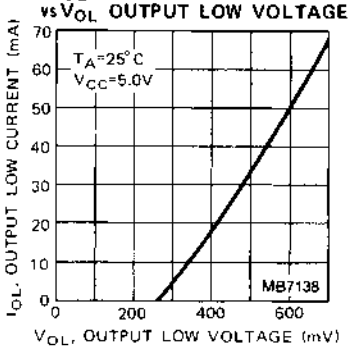
I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



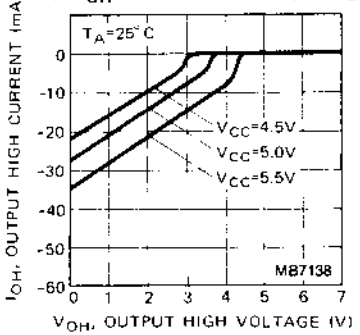
I_{OL} OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE



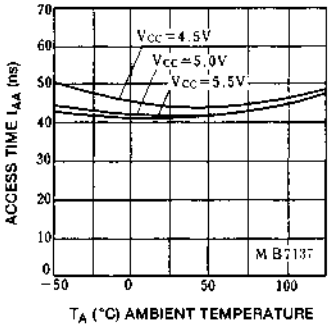
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



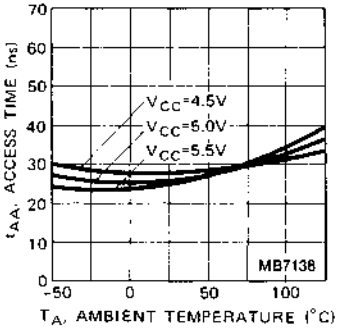
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

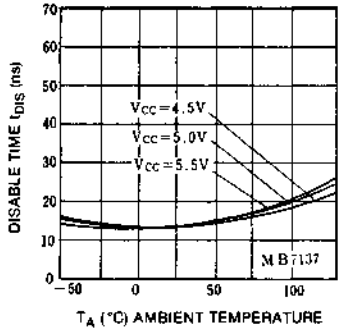


t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

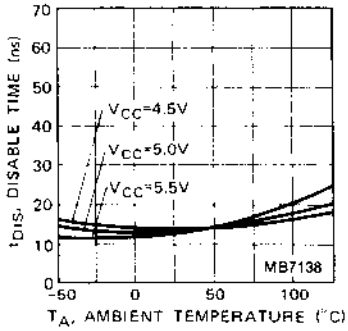


TYPICAL CHARACTERISTICS CURVES (Continued)

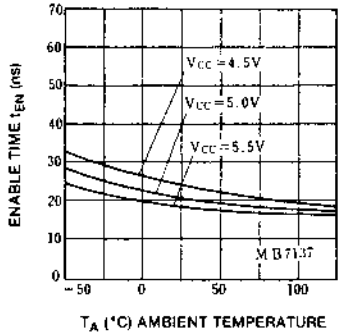
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



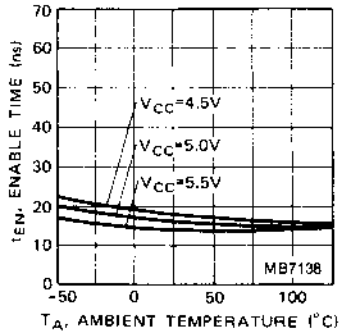
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



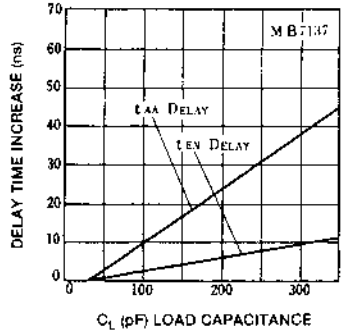
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



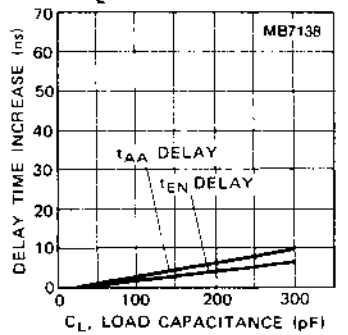
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit techology is used to achieve high-speed operation. A PNP transistor in the first stage of the input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

The open-collector is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7138 (3-state) compared to 0mA for the MB7137 (open-collector).

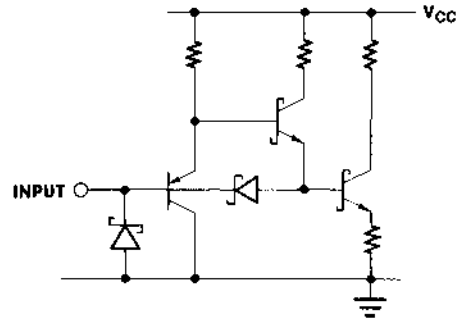
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

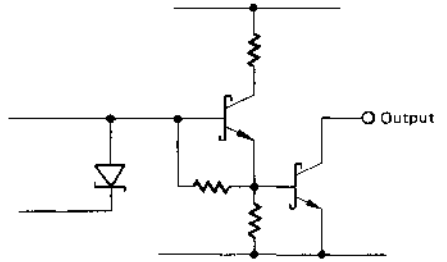
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Enable circuit.

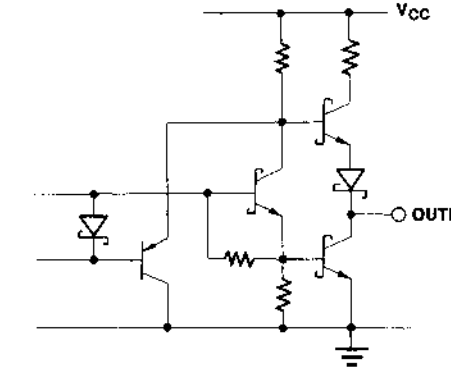
MB7137/MB7138 INPUT CIRCUIT



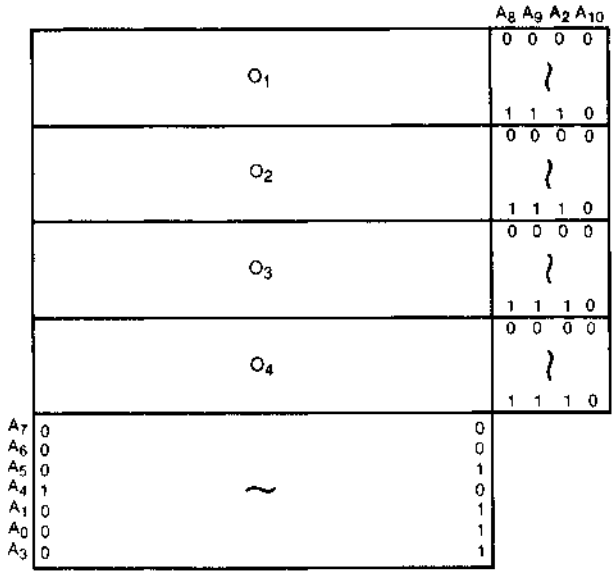
MB7137 OUTPUT CIRCUIT



MB7138 OUTPUT CIRCUIT



MB7137/MB7138 BIT MAP



Multiplexer

A_8	A_9	A_2	A_{10}
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

Decoder/Driver

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111

HIGH SPEED SCHOTTKY TTL 32,768-BIT PROM

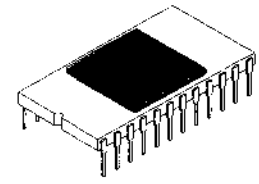
DESCRIPTION

The Fujitsu MB7141 and MB7142 are high speed electrically field programmable read only memories. With open collector outputs on the MB7141 and three-state outputs on the MB7142, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cell and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

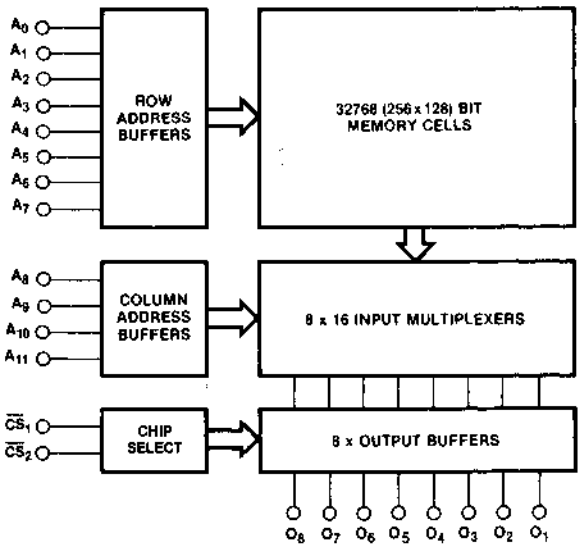


CERAMIC PACKAGE
DIP-24C-A01

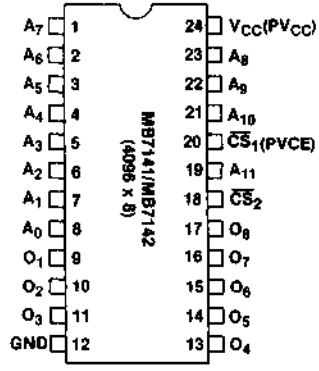
FEATURES

- **Organization: 4096 words x 8 bits, fully decoded**
- **TTL compatible input/output**
- **Fast Access Time:**
  MB7141E/MB7142E:
  65 ns Max.
  45 ns Typ.
  MB7141H/MB7142H:
  55 ns Max.
  45 ns Typ.
- **Low power dissipation: 185mA max**
- **Single +5V supply voltage**
- **Simplified and lower power programming**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Low current PNP inputs**
- **MB7141: Open collector outputs**
- **MB7142: Three-state outputs**
- **Two chip select leads for easy memory expansion**
- **Standard 24-pin DIP package**
- **MB7142 pin compatible with N82S321, HM76321 and 3632**

MB7141/MB7142 BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to +V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed ranges unless otherwise noted.

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)		I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16 mA)		V_{OL}	—	—	0.50	V
Output Leakage Current	MB7141	I_{OLK}	—	—	40	μA
(V_O = 2.4V, chip disable from a low)	MB7142	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.5V, chip disabled from a high)	MB7142	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)		V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	140	185	mA
Output High Voltage (I_O = −2.4mA)		V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)		I_{OS}*	−15	—	−60	mA

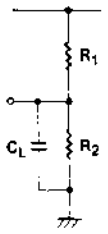
*Note: Denotes guaranteed characteristics of output high-level (ON) state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7141E/MB7142E		MB7141H/MB7142H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	45	65	45	55	ns
Output Disable Time	t_{DIS}	—	40	—	40	ns
Output Enable Time	t_{EN}	—	40	—	40	ns

AC TEST CONDITIONS

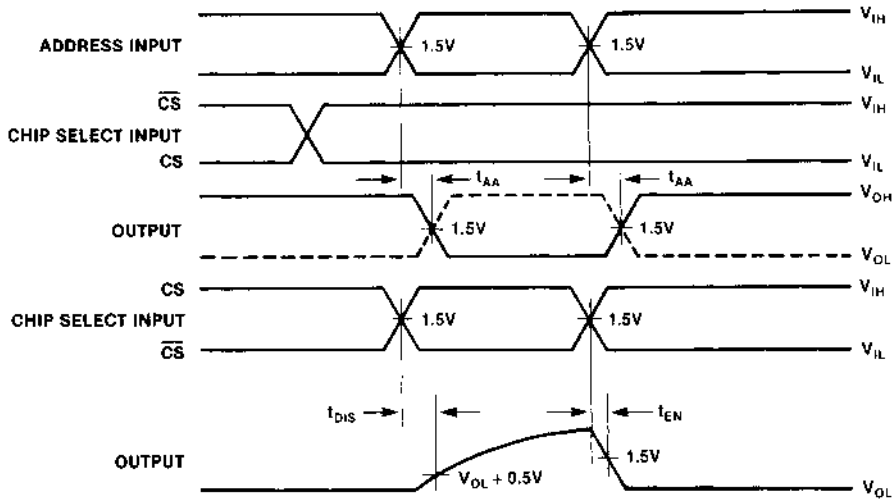


INPUT CONDITIONS

Amplitude	0V to 3V
Rise and Fall Time	5 ns from 1V to 2V
Frequency	1 MHZ

MB7141/MB7142		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



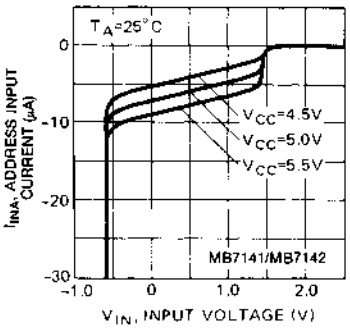
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

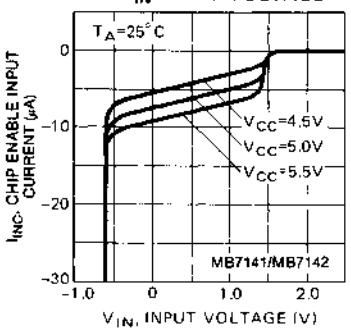
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

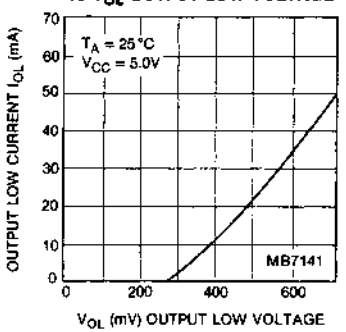
I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



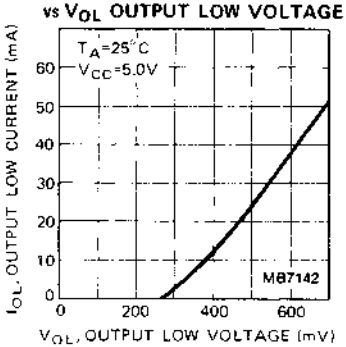
I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



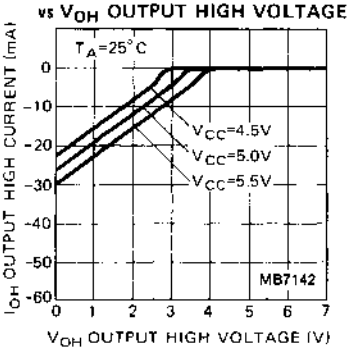
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



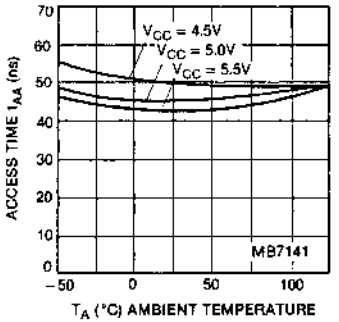
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



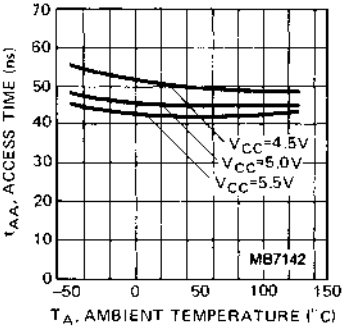
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

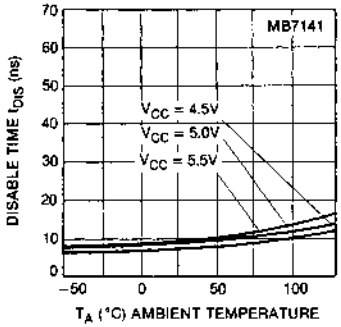


t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

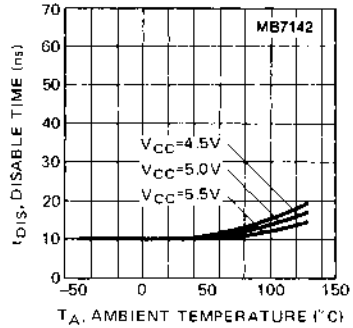


TYPICAL CHARACTERISTICS CURVES (Continued)

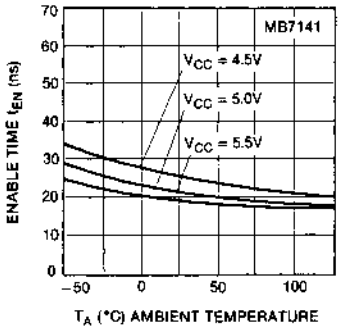
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



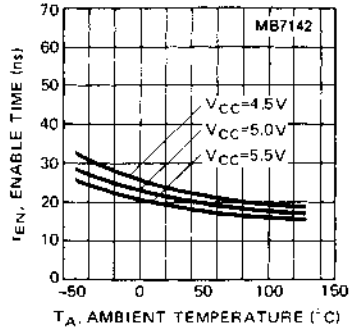
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



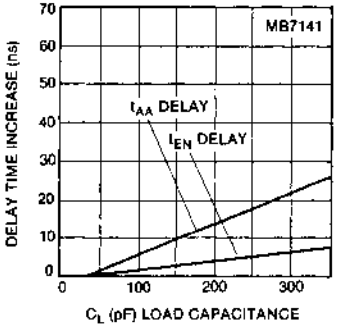
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



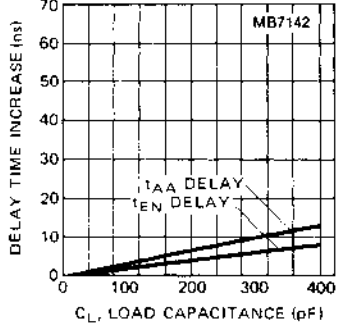
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7142 (3-state) compared to 0mA for the MB7141 (open-collector).

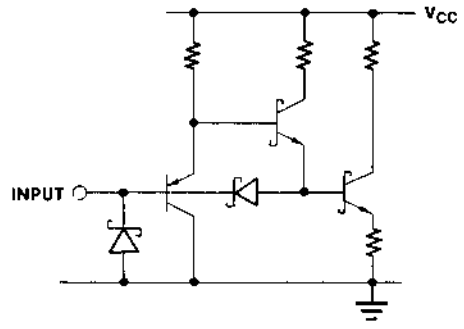
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

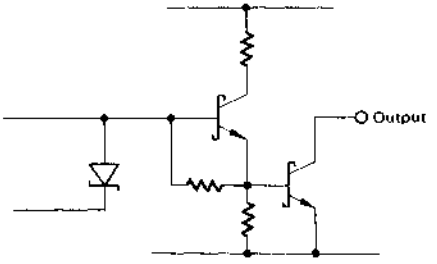
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Select circuit.

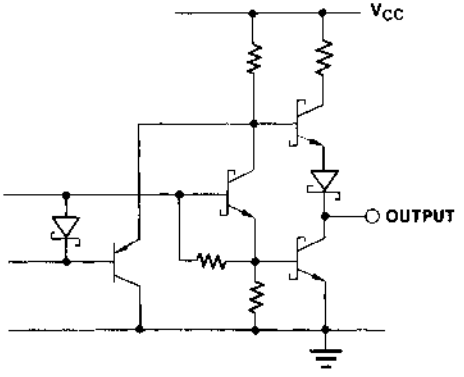
MB7141/MB7142 INPUT CIRCUIT



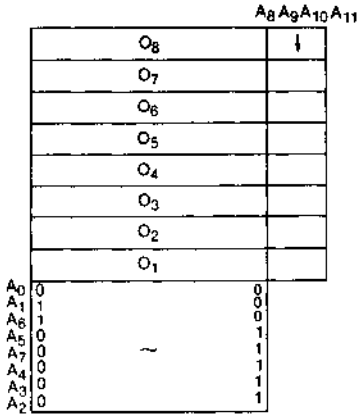
MB7141 OUTPUT CIRCUIT



MB7142 OUTPUT CIRCUIT



MB7141/MB7142 BIT MAP



Multiplexer

A_8	A_9	A_{10}	A_{11}
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

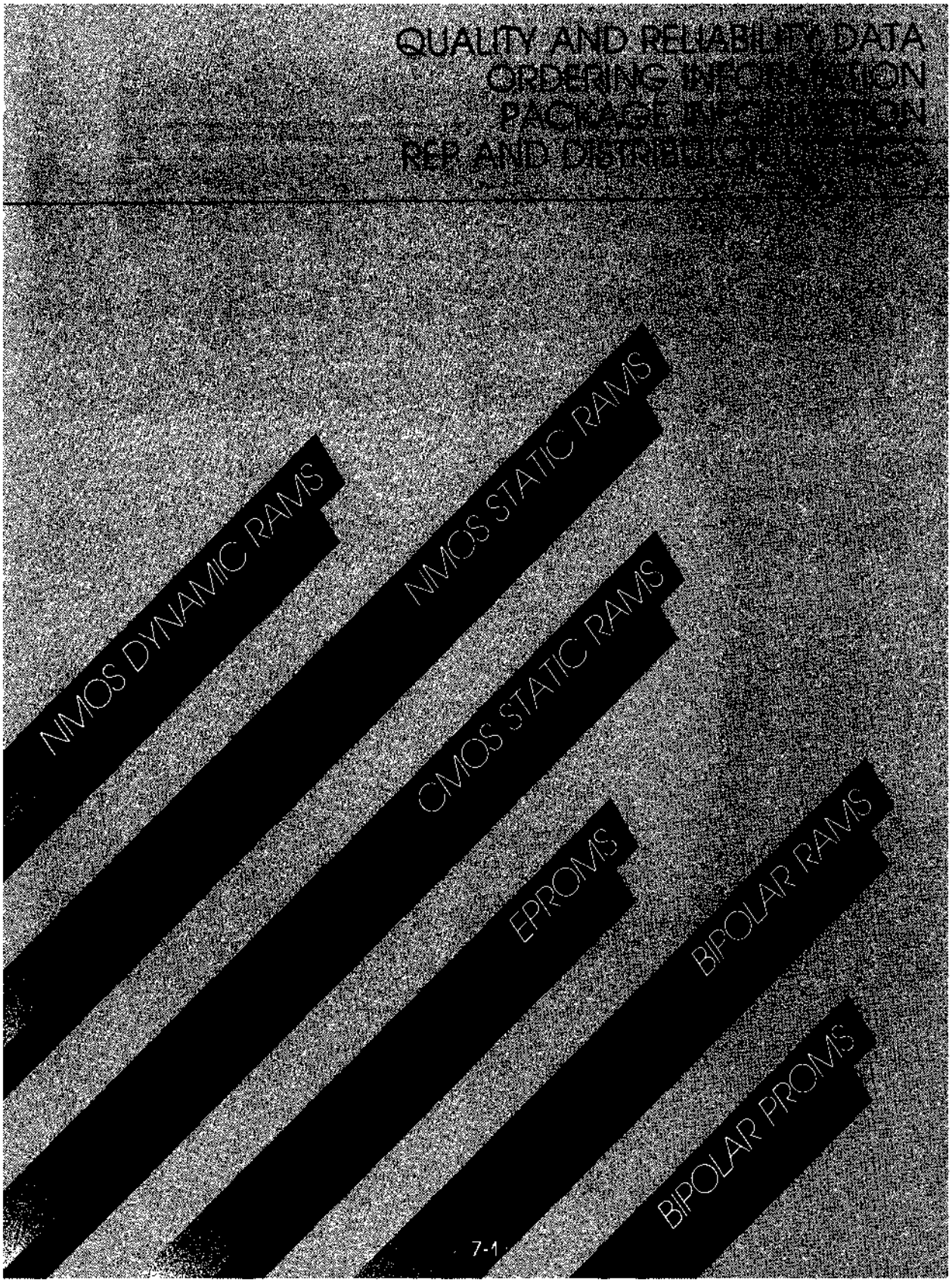
Decoder/Driver

A_0	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_1	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_6	11110000	11110000	11110000	11110000	11110000	11110000	11110000	11110000
A_5	00000000	11111111	00000000	11111111	00000000	11111111	00000000	11111111
A_7	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_4	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
A_2	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

A_0	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_1	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_6	11110000	11110000	11110000	11110000	11110000	11110000	11110000	11110000
A_5	00000000	11111111	00000000	11111111	00000000	11111111	00000000	11111111
A_7	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_4	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
A_2	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

A_0	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_1	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_6	11110000	11110000	11110000	11110000	11110000	11110000	11110000	11110000
A_5	00000000	11111111	00000000	11111111	00000000	11111111	00000000	11111111
A_7	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_4	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
A_2	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111

A_0	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_1	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_6	11110000	11110000	11110000	11110000	11110000	11110000	11110000	11110000
A_5	00000000	11111111	00000000	11111111	00000000	11111111	00000000	11111111
A_7	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_4	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
A_2	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111


QUALITY AND RELIABILITY DATA
ORDERING INFORMATION
PACKAGE INFORMATION
REP AND DISTRIBUTOR
NMOS DYNAMIC RAMS
NMOS STATIC RAMS
CMOS STATIC RAMS
EPROMS
BIPOLAR RAMS
BIPOLAR PROMS

LOT ASSURANCE TESTS

Test[1] Group	Test	MIL-STD-883B Method No.	Q'ty/Acceptance No. (LTPD)		
			Level A	Level B	Level C
A1	Static Tests at 25°C	Product Dependent	45/0 (5)	45/0 (5)	45/0 (5)
A2	Dynamic Tests at 25°C		45/0 (5)	45/0 (5)	45/0 (5)
A3	Functional Tests at 25°C		45/0 (5)	45/ (5)	45/0 (5)
A4	Static Tests at Max. Rated Operating Temp.		32/0 (7)	32/0 (7)	22/0 (10)
A5	Dynamic Tests at Max. Rated Operating Temp.		32/0 (7)	32/0 (7)	22/0 (10)
A6	Function Tests at Max. Rated Operating Temp.		22/0 (10)	22/0 (10)	15/0 (15)
B1	External Visual	2009.1	2/0	2/0	2/0
	Physical Dimensions	2016	2/0	2/0	2/0
B2	Thermal Shock	1011.2[3] (Test Conditions A ~ F)	10/0	—	—
	Temperature Cycling	1010.2[3] (Test Conditions A ~ G)	10/0	—	—
	Soldering Heat	2031.1[4]	10/0	—	—
B3	Mechanical Shock	2002.2[3] (Test Conditions A ~ G)	10/0	—	—
	Vibration, Variable Frequency	2007.1[3] (Test Conditions A ~ C)	10/0	—	—
	Constant Acceleration	2001.2[3] (Test Conditions A ~ J)	10/0	—	—
B4	Solderability	2003.2	10/0	10/0	10/0
B5	Lead Integrity	2004.2[3]	2/0	—	—
B6	Resistance to Solvents	2015.1	3/0	3/0	3/0
B7	Internal Visual and Mechanical	2014	2/0	1/0	1/0
B8	Bond Strength (10 Wires/Device)[5]	2011.2[3] (Test Conditions A ~ H)	2/0	1.5/0	1.5/0
B9	Die Shear	2019.1	3/0	—	—
B10	High Temperature Storage	1008.1[3,7] (Test Conditions A ~ H)	18/1	—	—
B11	Steady State Life	1005.2[3,7] (Test Conditions A ~ F)	25/1	—	—
B12	Steady State Humidity (Plastic Package Only)	103B[6]	18/1	—	—

Notes

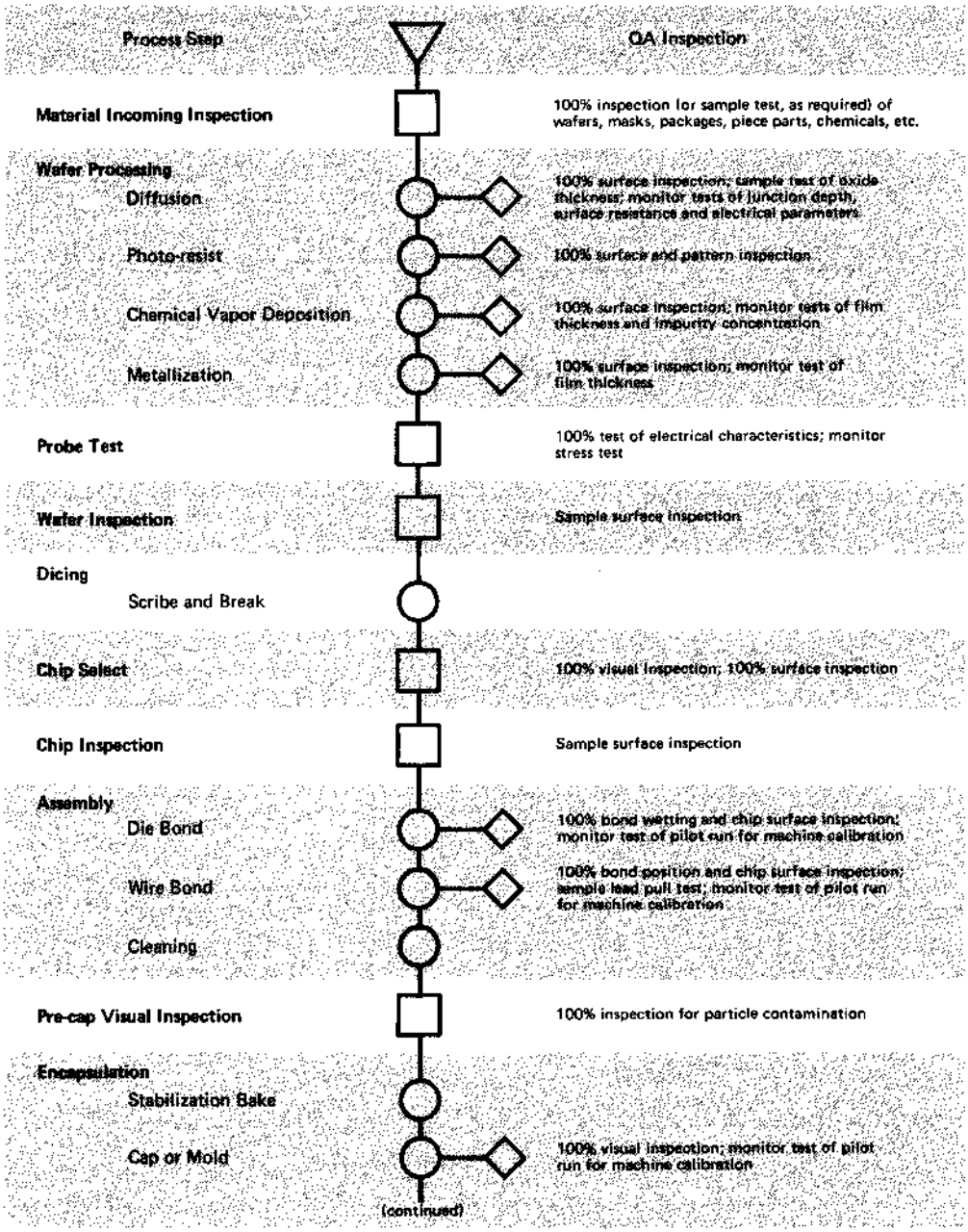
1. Test Groups denote individual tests employing individual samples; when several tests are grouped together within the same test, the sample is used to perform all tests within that test group.
2. Values given denote the minimum size of sample to be tested to assure, with 90% confidence, that a lot having a percent defective equal to the specified LTPD will not be accepted. Should the number of devices failing the specified tests exceed the acceptance number shown, the sample size may be increased one time only; for these cases, the LTPD value will be at least equivalent to (and in some cases may be more stringent than) that specified in this table.
3. Specific Test Condition employed will depend on the type and expected application of device being tested.
4. Tested in accordance with MIL-STD-750B.
5. The figures shown (e.g., 2/0, etc.) represent groups of 10 wires pulled per device.
6. Tested in accordance with MIL-STD-202E but with the Fujitsu specific conditions.
7. If no failures occur during the first 128 hours of testing, the test may be stopped and the lot accepted.

PERIODIC QUALITY CONFORMANCE TESTS [7]

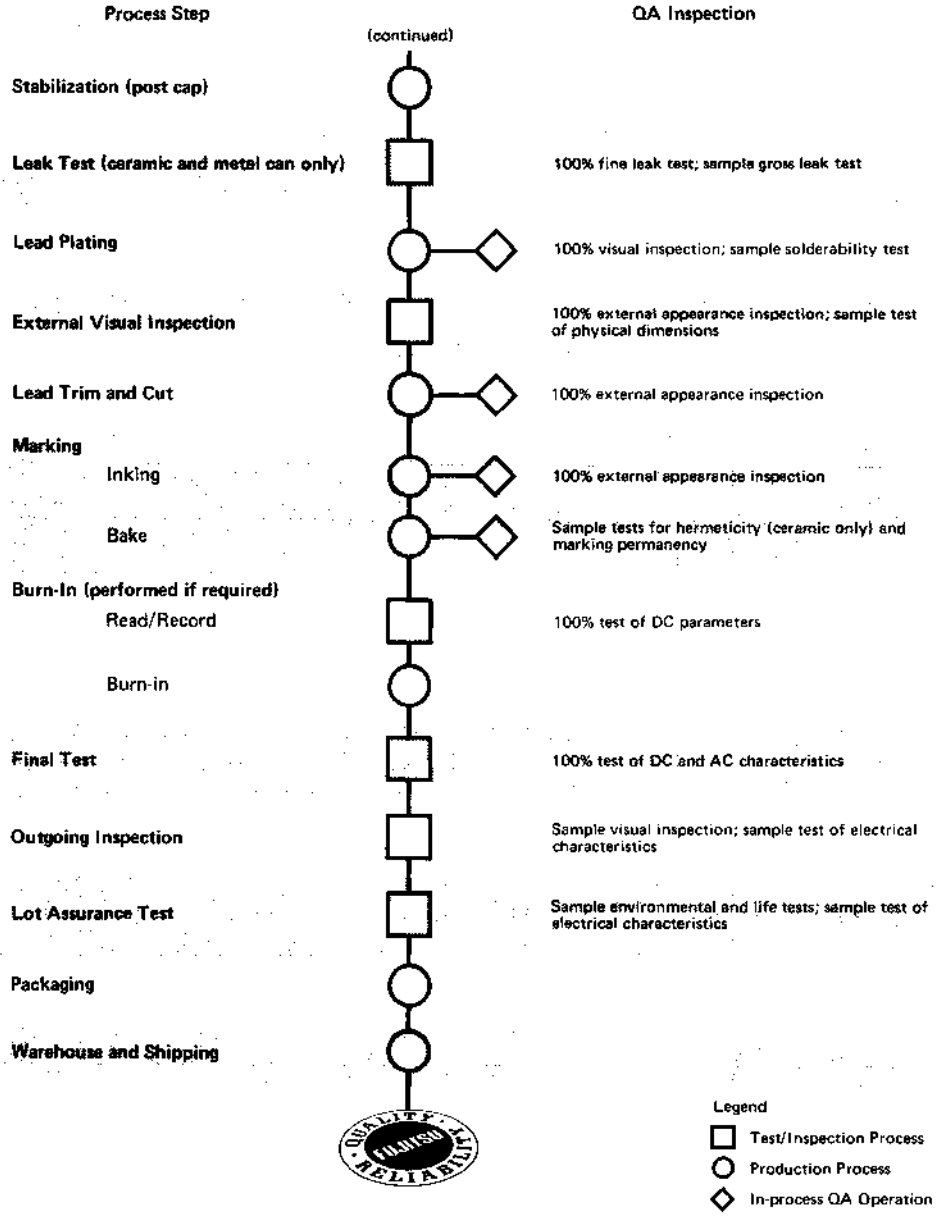
Test[1] Group	Test	MIL-STD-883B Method No.	Q'ty/Acceptance No. (LTPD)		
			Level A	Level B	Level C
A1	Static Tests at 25°C	Product Dependent	45/0 (5)	45/0 (5)	45/0 (5)
A2	Dynamic Tests at 25°C		45/0 (5)	45/0 (5)	45/0 (5)
A3	Functional Tests at 25°C		45/0 (5)	45/0 (5)	45/0 (5)
C1	External Visual	2009.1	2/0	2/0	2/0
	Physical Dimensions	2016	2/0	2/0	2/0
C2	Thermal Shock	1011.2[3] (Test Conditions A ~ F)	—	10/0	10/0
	Temperature Cycling	1010.2[3] (Test Conditions A ~ G)	—	10/0	10/0
	Soldering Heat	2031.1[4]	—	10/0	10/0
C3	Mechanical Shock	2002.2[3] (Test Conditions A ~ G)	—	10/0	10/0
	Vibration, Variable Frequency	2007.1[3] (Test Conditions A ~ C)	— —	10/0 10/0	10/0 10/0
	Constant Acceleration	2001.2[3] (Test Conditions A ~ J)	—	10/0	10/0
C4	Internal Visual and Mechanical	2014	3/0	2/0	2/0
C5	Bond Strength[5] (10 Wires/Device)	2011.2[3] (Test Conditions A ~ H)	3/0	2/0	2/0
C6	Die Shear	2019.1	—	3/0	3/0
C7	High Temperature Storage	1008.1[3] (Test Conditions A ~ H)	—	32/0 (7)	32/0 (7)
C8	Steady State Life	1005.2[3] (Test Conditions A ~ F)	—	32/0 (7)	32/0 (7)
D1	External Visual	2009.1	15/0 (15)	15/0 (15)	15/0 (15)
	Physical Dimensions	2016	15/0 (15)	15/0 (15)	15/0 (15)
D2	Thermal Shock	1011.2[3] (Test Conditions A ~ F)	15/0 (15)	15/0 (15)	15/0 (15)
	Temperature Cycling	1010.2[3] (Test Conditions A ~ G)	15/0 (15)	15/0 (15)	15/0 (15)
	Soldering Heat	2031.1[4]	15/0 (15)	15/0 (15)	15/0 (15)
D3	Mechanical Shock	2002.2[3]	15/0 (15)	15/0 (15)	15/0 (15)
	Vibration, Variable Frequency	2007.1[3] (Test Conditions A ~ C)	15/0 (15)	15/0 (15)	15/0 (15)
	Constant Acceleration	2001.2[3] (Test Conditions A ~ J)	15/0 (15)	15/0 (15)	15/0 (15)
D4	Solderability	2003.2	15/0 (15)	15/0 (15)	15/0 (15)
D5	Lead Integrity	2004.2[3]	—	15/0 (15)	15/0 (15)
D6	Resistance to Solvents	2015.1	15/0 (15)	15/0 (15)	15/0 (15)
D7	High Temperature Storage	1008.1[3]1 (Test Conditions A ~ H)	—	32/0 (7)	32/0 (7)
D8	Steady State Life	1005.2[3]	—	32/0 (7)	32/0 (7)
D9	Steady State Humidity (Plastic Package Only)	103B[6]	—	22/0 (10)	22/0 (10)
D10	Salt Atmosphere	1009.2[3] (Test Conditions A ~ D)	15/0 (15)	15/0 (15)	15/0 (15)

Notes 1. Test Groups denote individual tests employing individual samples; when several tests are grouped together within the same test group, the sample is used to perform all tests within that test group.
2. Values given denote the minimum size of sample to be tested to assure, with a 90% confidence, that a lot having a percent defective equal to the specified tests exceed the acceptance number shown, the sample size may be increased one time only; for these cases, the LTPD value will be at least equivalent to (and in some cases may be more stringent than) that specified in this table.
3. Specific Test Condition employed will depend on the type and expected application of device being tested.
4. Tested in accordance with MIL-STD-750B.
5. The figures shown (e.g., 2/0, etc.) represent groups of 10 wires pulled per device.
6. Tested in accordance with MIL-STD-202E but with the Fujitsu specific conditions.
7. Test Group C is for die-related testing performed every three months. Test Group D is for package-related testing and is performed every six months. Test Group A is performed each time either Test Group C or Test Group D is performed.

IC MANUFACTURING FLOW CHART



IC MANUFACTURING FLOW CHART



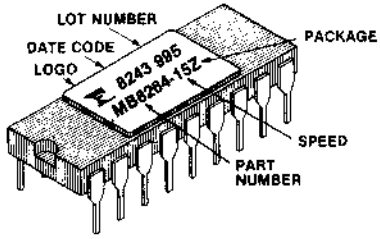
Note: Flow sequence may vary slightly due to individual product characteristics

ORDERING INFORMATION

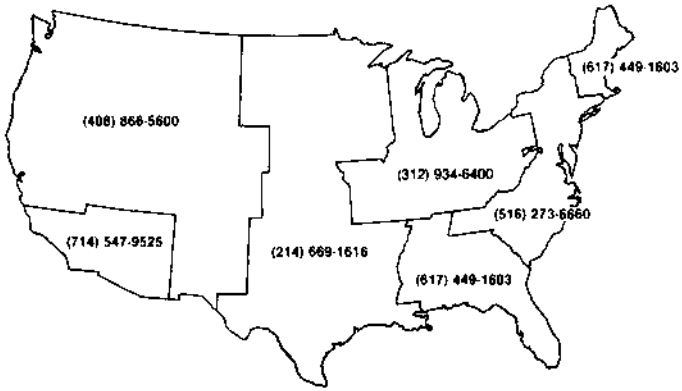
MB 8264-15 Z

- PACKAGE
  - C-CERAMIC
  - M-PLASTIC
  - Z-CERDIP
- PERFORMANCE VARIATIONS (WHEN USED)
  - E, H- OR DASH NUMBERS DENOTE ACCESS TIME VARIATIONS
  - L-DENOTES LOW POWER
- DEVICE TYPE
- MANUFACTURER DESIGNATOR
  - MB-DEVICE TYPE IS FUJITSU INTERNAL NUMBER
  - MBM-DEVICE TYPE IS INDUSTRY STANDARD MEMORY NUMBER

PRODUCT MARKING



FUJITSU MICROELECTRONICS SALES OFFICES



HEADQUARTERS
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2985 Kifer Road • Santa Clara, CA 95051 • (408) 727-1700 • Telex I/it: 910-338-0190

NORTHERN CALIFORNIA
Fujitsu Microelectronics
595 Millich Drive
Suite 210
Campbell, CA 95008
(408) 866-5600
TWX: 910-590-8003

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Fujitsu Microelectronics
525 N. Cabrillo Park Drive
Suite 314
Santa Ana, CA 97201
(714) 547-9525
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CHICAGO
Fujitsu Microelectronics
1833 Hicks Road
Suites B & C
Rolling Meadows, IL 60008
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Fujitsu Microelectronics
1131 Rockingham Dr. @ Arapaho
Suite 204
Richardson, TX 75080
(214) 669-1616
TWX: 910-867-9434

BOSTON
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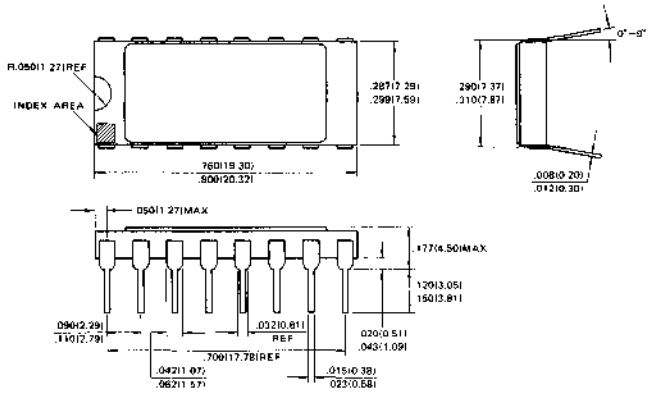
Suite 6
Needham Heights, MA 02194
(617) 449-1603
TWX: 710-325-0605

NEW YORK
Fujitsu Microelectronics
350 Vanderbilt Motor Parkway
Suite 303
Hauppauge, NY 11787
(516) 273-6660
TWX: 510-227-1049

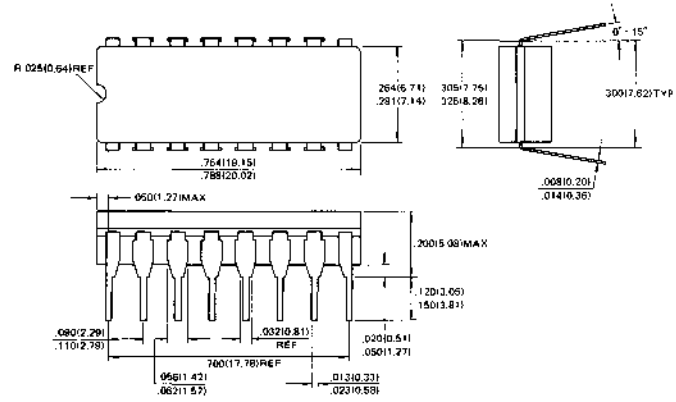
DIP-16C-A02

16-LEAD CERAMIC METAL SEAL DUAL IN-LINE PACKAGE



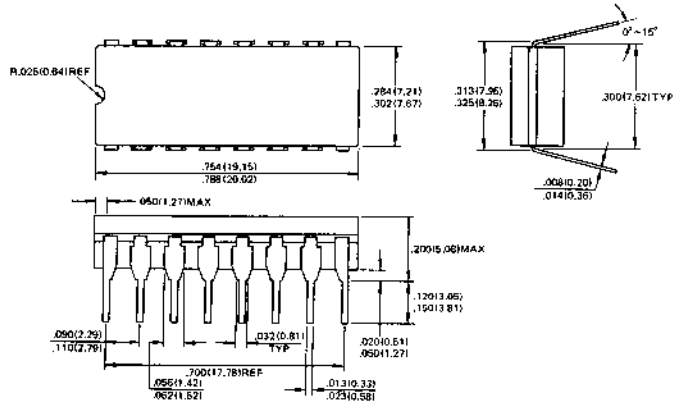
DIP-16C-C03

16-LEAD CERDIP DUAL IN-LINE PACKAGE



DIP-16C-C04

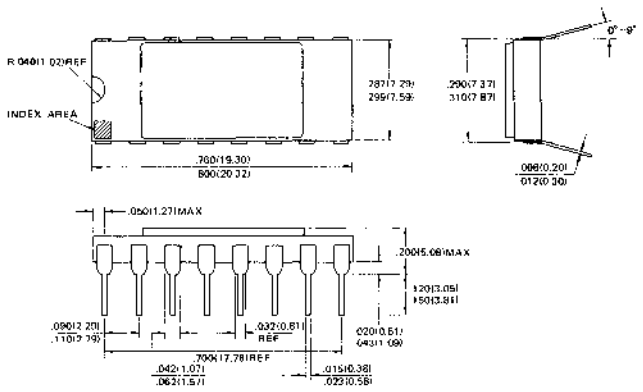
16-LEAD CERDIP DUAL IN-LINE PACKAGE



PACKAGE INFORMATION Dimensions in inches (millimeters)

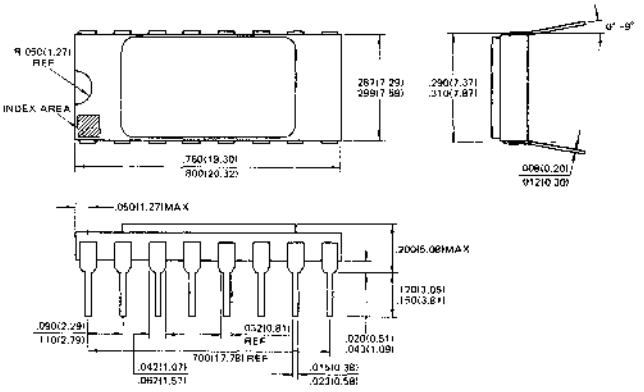
DIP-16C-F01

16-LEAD CERAMIC
FRIT SEAL
DUAL IN-LINE PACKAGE



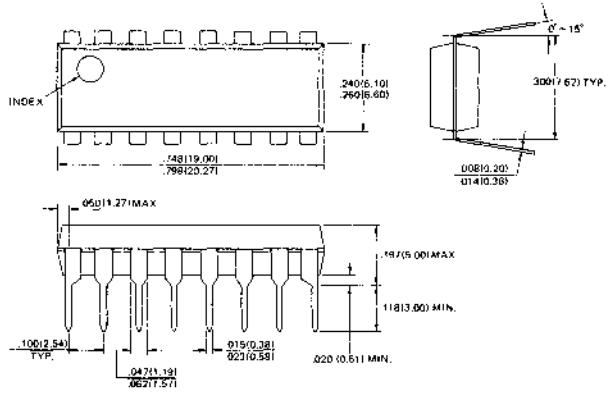
DIP-16C-F02

16-LEAD CERAMIC
FRIT SEAL
DUAL IN-LINE PACKAGE



DIP-16P-M01

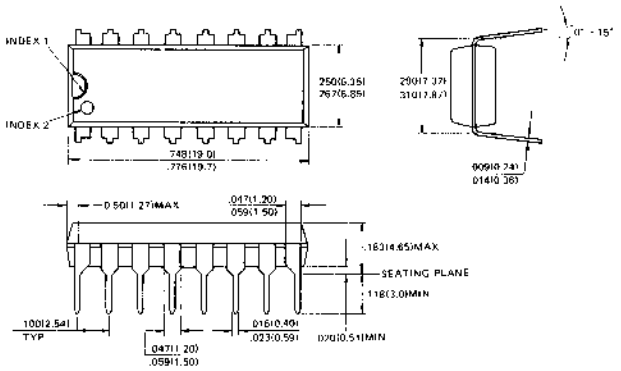
16-LEAD PLASTIC
DUAL IN-LINE PACKAGE



PACKAGE INFORMATION Dimensions in inches (millimeters)

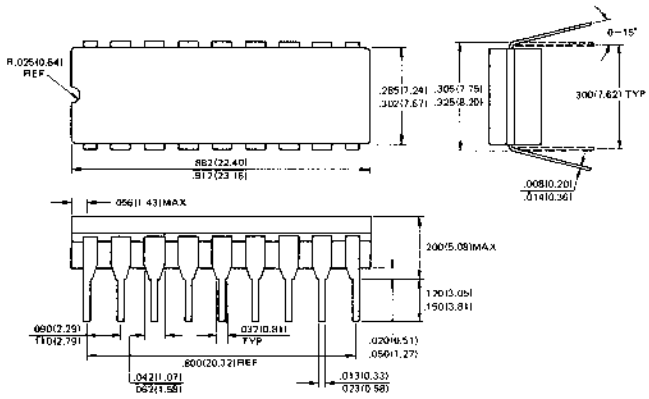
DIP-16P-M03

16-LEAD PLASTIC
DUAL IN-LINE PACKAGE



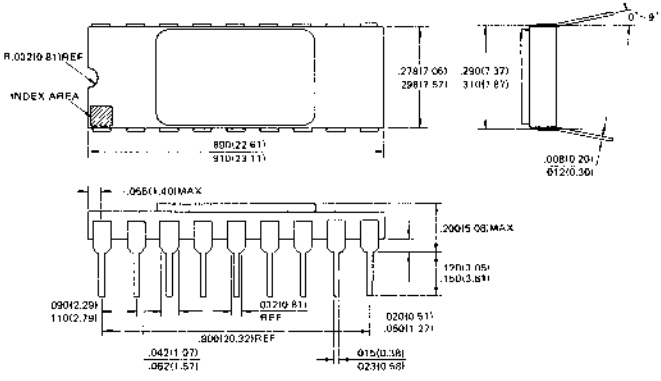
DIP-18C-C01

18-LEAD CERDIP
DUAL IN-LINE PACKAGE



DIP-18C-F02

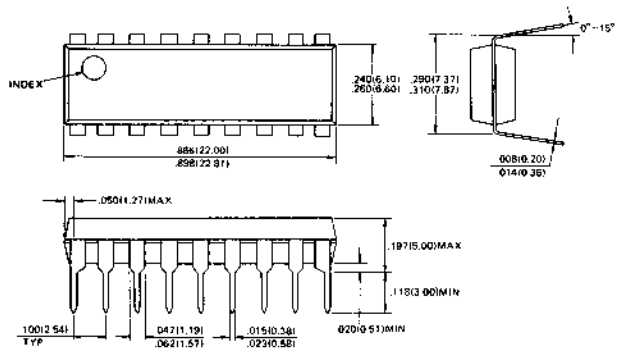
18-LEAD CERAMIC
FRIT SEAL
DUAL IN-LINE PACKAGE



PACKAGE INFORMATION Dimensions in inches (millimeters)

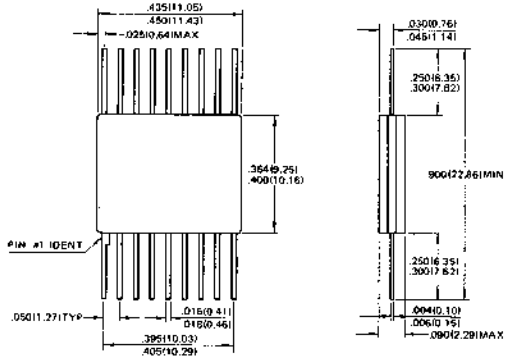
DIP-18P-M01

18-LEAD PLASTIC DUAL IN-LINE PACKAGE



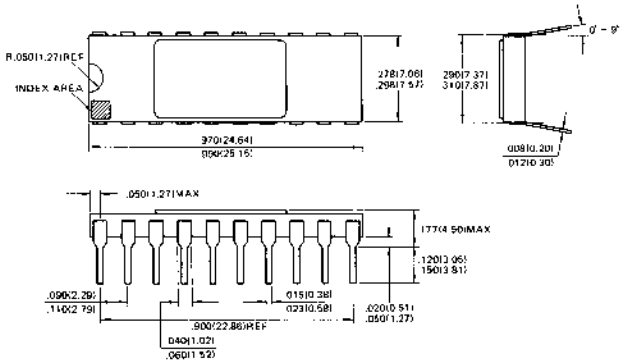
FPT-18C-C01

18-LEAD CERDIP FLAT PACKAGE



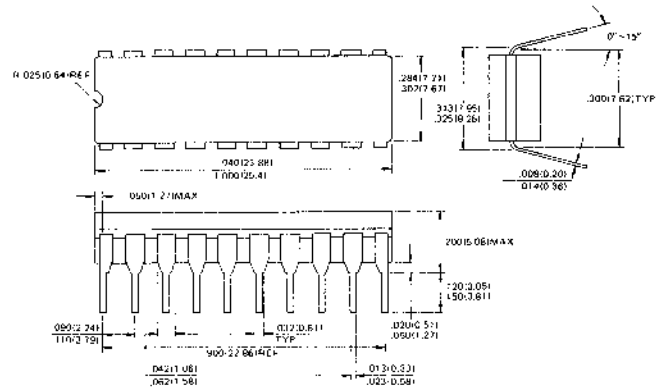
DIP-20C-A01

20-LEAD CERAMIC METAL SEAL DUAL IN-LINE PACKAGE



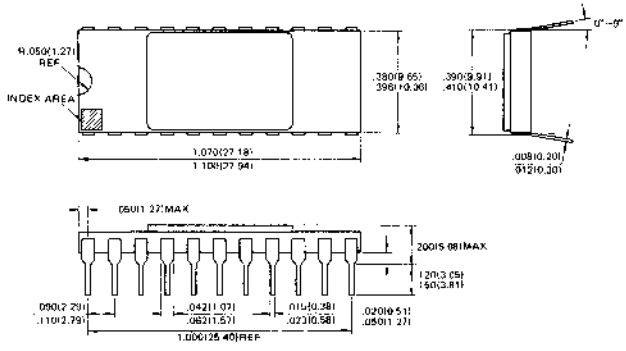
DIP-20C-C03

20-LEAD CERDIP
DUAL IN-LINE PACKAGE



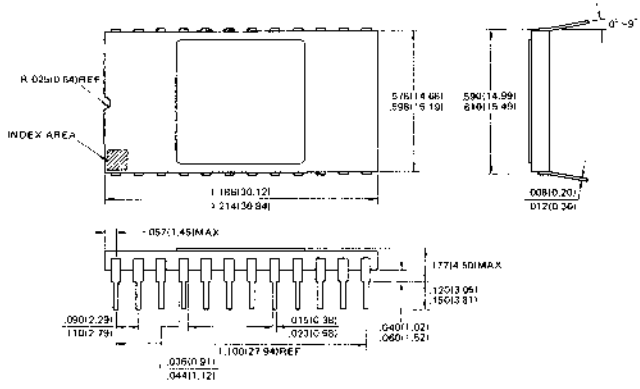
DIP-22C-F01

22-LEAD CERAMIC
FRIT SEAL
DUAL IN-LINE PACKAGE



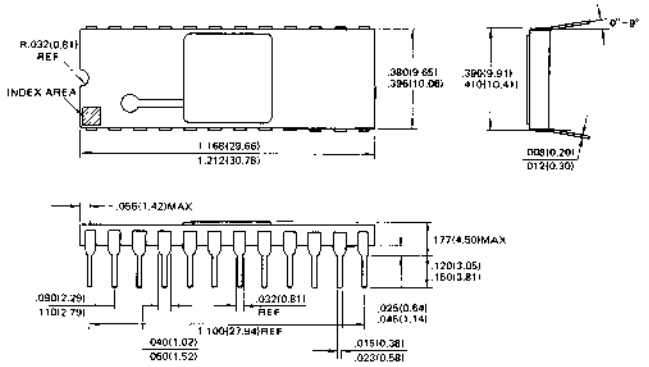
DIP-24C-A01

24-LEAD CERAMIC
METAL SEAL
DUAL IN-LINE PACKAGE



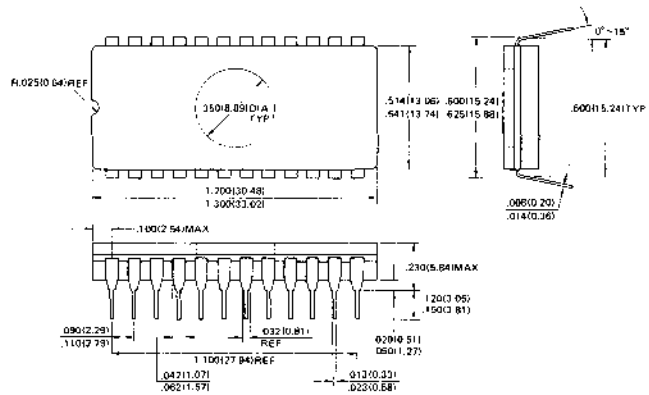
DIP-24C-A02

**24-LEAD CERAMIC
METAL SEAL
DUAL IN-LINE PACKAGE**



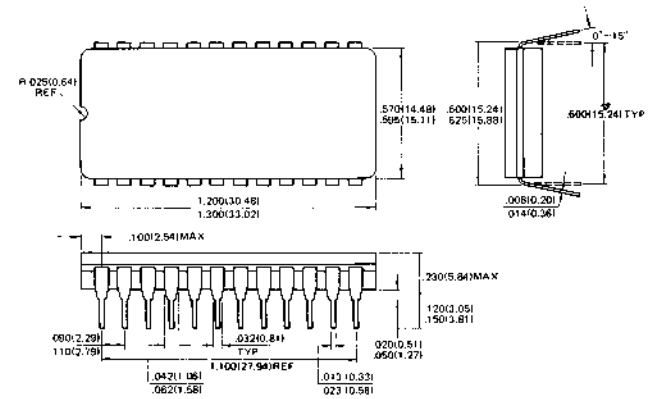
DIP-24C-C02

**24-LEAD CERDIP
WITH TRANSPARENT LID
DUAL IN-LINE PACKAGE**



DIP-24C-C03

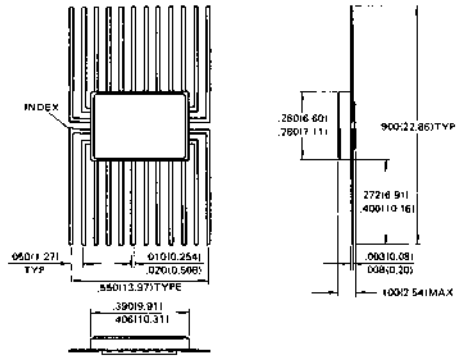
**24-LEAD CERDIP
DUAL IN-LINE PACKAGE**



PACKAGE INFORMATION Dimensions in inches (millimeters)

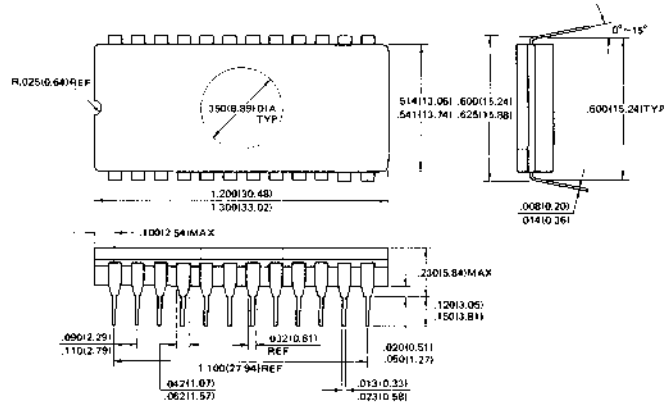
FPT-24C-F01

24-LEAD CERAMIC
FRIT SEAL
FLAT PACKAGE



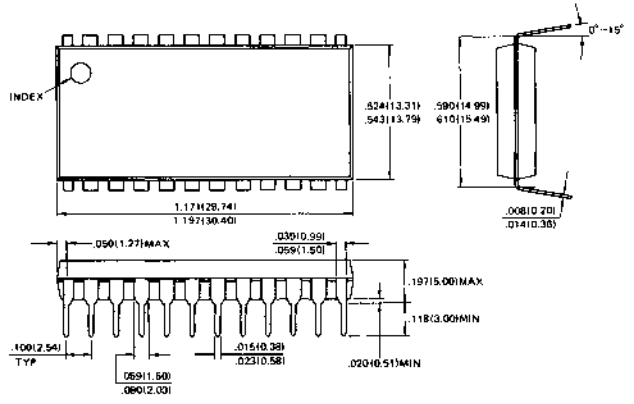
FPT-24-C02

24-LEAD CERDIP
FLAT PACKAGE



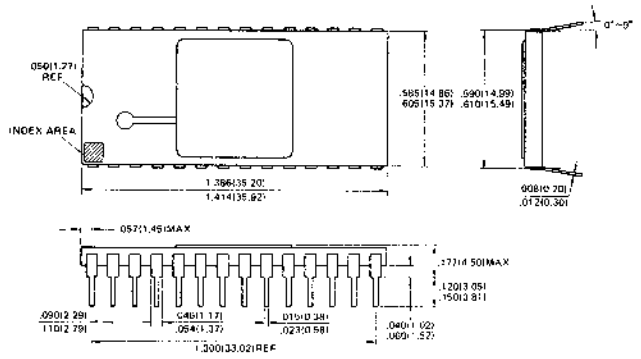
DIP-24P-M01

24-LEAD PLASTIC
DUAL IN-LINE PACKAGE



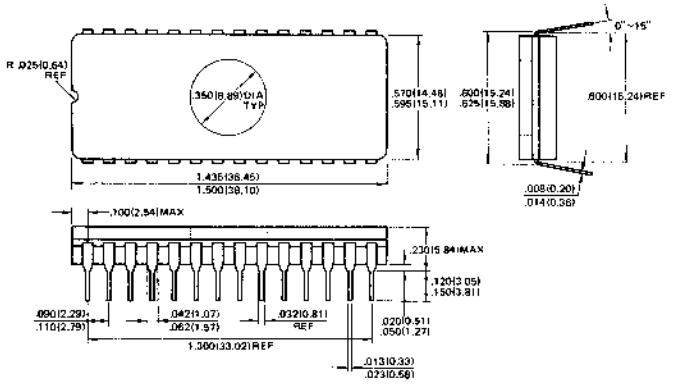
DIP-28C-A01

**28-LEAD CERAMIC
METAL SEAL
DUAL IN-LINE PACKAGE**



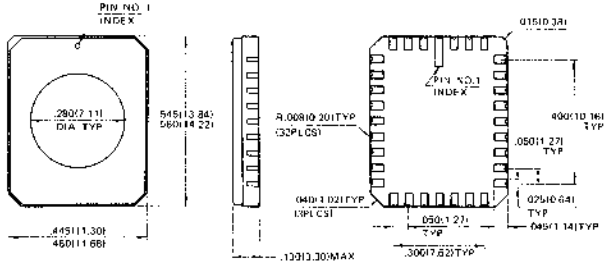
DIP-28C-C01

**28-LEAD CERDIP
WITH TRANSPARENT LID
DUAL IN-LINE PACKAGE**



LCC-32C-A01

**32-PAD CERAMIC
METAL SEAL
LEADLESS CHIP CARRIER**



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Florida
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TWX: 510-956-9872

Dyne-A-Mark Corporation
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Pennsylvania
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