2102/2102L/21L02
1024 x 1 Static RAM

Description

The 2102 family consists of 1024-word by 1-bit static Random Access read/write Memories (RAM) that require a single 5 V supply, have fully TTL-compatible inputs and output, and require no clocking or refresh. Chip Select ($\overline{CS}$) permits a 3-state output allowing the outputs to be wired-OR. Special features include low power dissipation (2102L) and a power-down capability (21L02).

The 2102, 2102L and 21L02 are manufactured using the n-channel Isoplanar process and are available in a 16-pin dual in-line package or flatpak.

- **FAST ACCESS—250 ns**
- **SINGLE +5 V SUPPLY**
- **TTL-COMPATIBLE INPUTS AND OUTPUT**
- **TOTALLY STATIC—NO CLOCKS OR REFRESH**
- **3-STATE OUTPUT**
- **LOW POWER (2102L)**
- **POWER-DOWN CAPABILITY (21L02)**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **16-PIN DUAL IN-LINE PACKAGE**

Pin Names

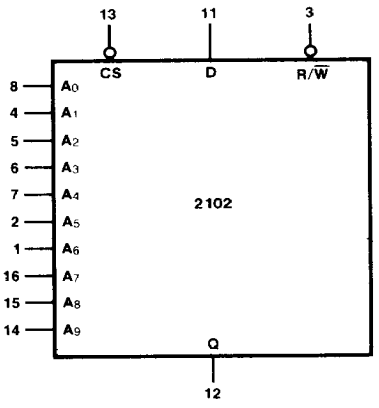
A_0-A_9	Address Inputs
D	Data Input
R/$\overline{W}$	Read/Write
$\overline{CS}$	Chip Select (active LOW)
Q	Data Output

Absolute Maximum Ratings

Voltage on Any Pin with Respect to V_{SS}	−0.5 V to +7.0 V
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

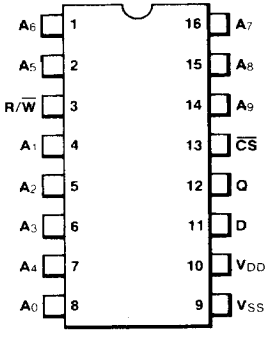
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabiliy.

Logic Symbol



V_{SS} = Pin 9
V_{DD} = Pin 10

Connection Diagram 16-Pin DIP

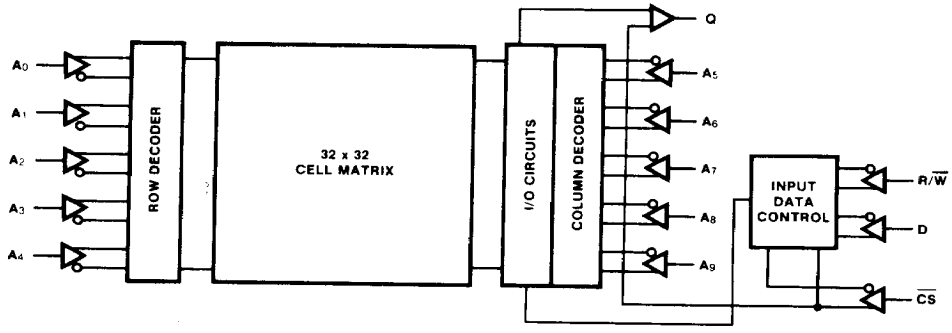


(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Plastic DIP	UC	P
Flatpak	II	F

Note
The Flatpak has the same pin number-to-function correspondence as the DIP.

Block Diagram



Truth Table

$\overline{CS}$	R/$\overline{W}$	D	Q	Comments
H	X	X	•	Chip Deselected
L	L	H	H	Write "1"†
L	L	L	L	Write "0"†
L	H	X	D_n	Read†

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
• = Output High Impedance State
D_n = Data at Address Location
† = Chip Selected

Power/Access Time Guide

	Part Number	Access Time	$I_{DD(MAX)}$
Power Down	21L02H	250 ns	30 mA
	21L02F	350 ns	30 mA
	21L021	450 ns	30 mA
	21L022	650 ns	30 mA
Low Power	2102LH	250 ns	30 mA
	2102LF	350 ns	30 mA
	2102L1	450 ns	30 mA
	2102L2	650 ns	30 mA
Standard	2102H	250 ns	55 mA
	2102F	350 ns	55 mA
	21021	450 ns	55 mA
	21022	650 ns	55 mA

Functional Description

The 2102, 2102L and 21L02 are 1024 x 1 static RAMs. When the Chip Select ($\overline{CS}$) goes HIGH, the Read/Write (R/$\overline{W}$) input is disabled and the Data Output (Q) is forced into a high impedance state. When $\overline{CS}$ goes LOW, the Read/Write input is enabled.

When R/$\overline{W}$ goes LOW, data from the Data Input (D) is written at the location specified by the Address Inputs (A_n). The Data Output will be identical to the Data Input during a write command. When R/$\overline{W}$ goes HIGH, the contents of the addressed location will appear at Q. Q is not inverted from D in the 2102. (See Truth Table).

DC Requirements T_A = 0°C to +70°C

Symbol	Characteristic, Note		2102, 2102L Min	2102, 2102L Max	21L02 Min	21L02 Max	Unit	Condition
V_{IH}	Input HIGH Voltage	H,F,1	2.0	V_{DD}	2.0	V_{DD}	V	
		2	2.2	V_{DD}	2.2	V_{DD}		
V_{IL}	Input LOW Voltage	H,F,1	−0.5	0.8	−0.5	0.8	V	
		2	−0.5	0.65	−0.5	0.65		
V_{DD}	Power Supply Voltage		4.75	5.25	4.5	5.5	V	

DC Characteristics V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to +70°C

Symbol	Characteristic, Note		2102, 2102L, 21L02 Min	2102, 2102L, 21L02 Max	Unit	Condition
V_{OH}	Output HIGH Voltage	H,F,1	2.4		V	I_{OH} = −100 μA
		2	2.2			
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1 mA
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{DD}$
I_{OH}	Output HIGH Current			5.0	μA	$V_{OUT} = V_{OH(Min)}$ $\overline{CS} = V_{IH(Min)}$
I_{OL}	Output LOW Current			−10	μA	$V_{OUT} = V_{OL(Max)}$ $\overline{CS} = V_{IH(Min)}$
I_{DD}	Power Supply Current 2102 2102L 21L02			 55 30 30	mA	Inputs = $V_{DD(Max)}$ D_{OUT} open, $T_A = T_{A(Min)}$

AC Requirements T_A = 0°C to +70°C

Symbol	Characteristic	2102H 2102LH 21L02H Min	2102F 2102LF 21L02F Min	21021 2102L1 21L021 Min	21022 2102L2 21L022 Min	Unit	Condition
t_{CYC}	Read or Write Cycle Time	250	350	450	650	ns	
t_{AW}	Address to Write Time	20	20	20	200	ns	
t_{WP}	Write Pulse Width	170	170	200	350	ns	V_{SS} = 0 V
t_{WR}	Write Recovery Time	0	0	0	50	ns	See DC Requirements
t_{DS}	Data Set-up Time	170	170	200	350	ns	for Conditions on V_{DD}
t_{DH}	Data Hold Time	0	0	0	20	ns	
t_{CW}	Chip Select to Write Time	170	170	200	400	ns	
t_{WC}	Write to Chip Select Time	0	0	0	50	ns	

Note
See Power/Access Time Guide and AC Characteristics for definitions of H, F, 1 and 2 speed grades.

AC Characteristics T_A = 0°C to +70°C

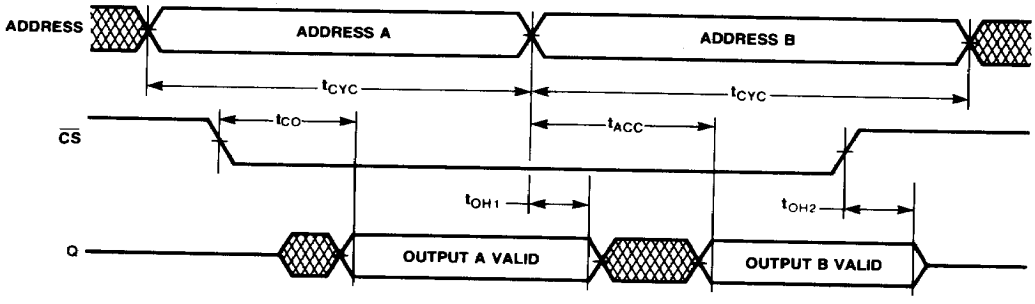
Symbol	Characteristic	2102H 2102LH 21L02H Min	2102H 2102LH 21L02H Max	2102F 2102LF 21L02F Min	2102F 2102LF 21L02F Max	21021 2102L1 21L021 Min	21021 2102L1 21L021 Max	21022 2102L2 21L022 Min	21022 2102L2 21L022 Max	Unit	Condition
t_{ACC}	Read Access Time		250		350		450		650	ns	
t_{CO}	Chip Select LOW to Output Valid Delay		130		170		200		400	ns	V_{SS} = 0 V
t_{OH1}	Data Valid after Address	40		50		50		50		ns	See DC Requirements for Conditions on V_{DD}
t_{OH2}	Previous Data Valid after Chip Deselect	0		0		0		0		ns	
C_{IN}	Input Capacitance		5.0		5.0		5.0		5.0	pF	V_{IN} = 0 V, V_{SS} = 0 V
C_{OUT}	Output Capacitance		10		10		10		10	pF	f = 1 MHz, T_A = 25°C

Power Down Characteristics (21L02 only) T_A = 0°C to +70°C

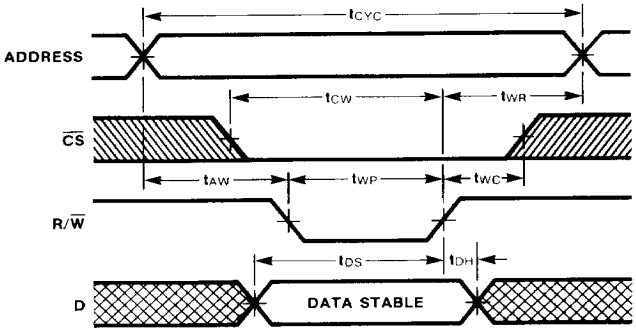
Symbol	Characteristic	21L02 Min	21L02 Max	Unit	Condition
$I_{DD(PD)}$	Power Supply Current		15	mA	V_{DD} = 1.6 V
$V_{DD(PD)}$	Power Supply Voltage	1.6		V	
t_{CSS}	Chip Select Set-up Time	100		ns	
t_{CSH}	Chip Select Hold Time	100		ns	
V_{CS}	Chip Select Voltage	2.0		V	
V'_{DD}	Power Supply Slew Rate		100	V/μs	

Timing Diagrams

Read Cycle Timing



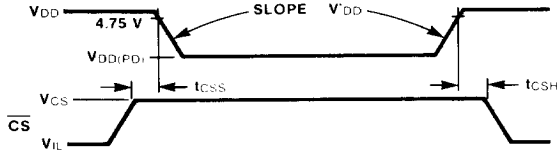
Write Cycle Timing



OUTPUT NOT VALID OR
INPUT IN HIGH OR LOW TRANSITION

HIGH-TO-LOW TRANSITION

LOW-TO-HIGH TRANSITION



AC Conditions

Input Levels: $V_{IL(Max)}$ to $V_{IH(Min)}$
Input Rise and Fall Times: 10 ns
Timing Measurement Reference Levels:
Inputs: 1.5 V
Output: 2.0 and 0.8 V
Output Load: 1 TTL Gate + 100 pF