Cypress Data Book

SRAMs

MODULEs

EPROMs

FIFOs

DUAL PORTs

DATACOM

FCT LOGIC

CLOCK CHIPS

PC CHIPSETs

1995

CYPRESS

Cypress Data Book

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MEMORIES

DATACOM

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PC PRODUCTS

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High Performance Data Book

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How To Use This Book

Overall Organization

This book has been organized by product type, beginning with Product Information. The products are next, starting with SRAMs, then Modules, Non-Volatile Memories, FIFOs, Dual-Ports, Data Communications, Bus Interface Products, FCT Logic, Timing Technology Products, and PC Chipsets. A section containing military information is next, followed by Quality and Reliability aspects, then Thermal Data and Packages. Within each section, data sheets are arranged in order of part number.

Recommended Search Paths

To search by:	Use:
Product line	Table of Contents or flip through the book using the tabs on the right-hand pages.
Size	The Product Selector Guide in section 1.
Numeric part number	Numeric Device Index following the Table of Contents. The book is also arranged in order of part number.
Other manufacturer's part number	The Cross Reference Guide in section 1.
Military part number	The Military Selector Guide in section 12.

Key to Waveform Diagrams

 = Rising edge of signal will occur during this time.

 = Falling edge of signal will occur during this time.

 = Signal may transition during this time (don't care condition).

 = Signal changes from high-impedance state to valid logic level during this time.

 = Signal changes from valid logic level to high-impedance state during this time.

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Cypress Semiconductor Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. This market is served by producing the highest-performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test. The company went public in May 1986 and has been listed on the New York Stock Exchange since October 1988.

The initial semiconductor process, a CMOS process employing 1.2-micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2-micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2-micron processes, a 0.8-micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8-micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high-performance markets with state-of-the-art integrated circuits, Cypress introduced two new processes in 1989. These were a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state of the art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest-performance circuits in the industry. Cypress's offers products in four divisions: the Static Memory Division, the Programmable Products Division, the Computation Products Division, and the Data Communications Division.

Static Memories Division

Cypress is a market-leading supplier of SRAMs, providing a wide range of SRAM memories for leading companies worldwide. SRAMs are used in high-performance personal computers, workstations, telecommunications systems, industrial systems, instrumentation devices, and networking products. Cypress's lower production cost structure allows the company to compete effectively in the high-volume personal computer and workstation market for SRAMs, including providing cache RAMs to support today's high-performance microprocessors, such as Pentium™, and PowerPC™. This business, combined with upcoming low-voltage products for the cellular communications, portable instrument, and laptop/notebook PC markets, positions Cypress for future success in this key product area.

Multichip modules is a fast-growing market segment that consists of multiple semiconductor chips mounted in packages that can be inserted in a computer circuit board. Cache modules for personal computers are the mainstay of this product line, and Cypress has announced major design wins for these products in IBM's PS/ValuePoint™ line of PCs, and in Apple Computer's highest performing Power Macintosh™ products.

Programmable Products Division

With increasing pressure on system designers to bring products to market more quickly, programmable logic devices (PLDs) are becoming extremely popular. PLDs are logic control devices that can be easily programmed by engineers in the field, and later erased and reprogrammed. This allows the designers to make key changes to their systems very late in the development cycle to ensure competitive advantage. Used extensively in an wide range of applications, PLDs constitute a large and growing market. Cypress's UltraLogic™ product line addresses the high-density programmable logic market. UltraLogic includes the pASIC380 family of field-programmable gate arrays (FPGAs), the industry's fastest. It also includes high performance complex PLDs, the FLASH370 family. Both of these product families are supported by Cypress's VHDL (Very high-speed integrated circuit Hardware Description Language) based *Warp3*™, the industry's most advanced software design tool. Cypress pioneered the use of VHDL for PLD programming, and *Warp* software is a key factor in the company's overall success in the PLD market.

Cypress is a leading provider of the industry-standard 22V10 PLD with a wide range of offerings including a BiCMOS 22V10 at 4 ns. Cypress is committed to competing in all ranges of the PLD market, with small devices, including the industry standard 16V8, the MAX™ CY7C340 EPLD line, and the UltraLogic products. To support these products, Cypress offers one of the industry's broadest range of programming tools and software for the programming of its PLDs.

Cypress provides one of the industry's broadest ranges of CMOS EPROMs and PROMs. Cypress owns a large share of the high-speed CMOS PROM market, and with its new cost structure, is effectively penetrating the mainstream EPROM market with a popular 256 Kbit EPROM, and the introduction of the world's fastest 512K and 1 Megabit EPROMs at 25 ns.

FCT Logic products are used in bus interface and data buffering applications in almost all digital systems. With the addition of the FCT logic product line, Cypress now offers over 46 standard logic and bus interface functions. The products are offered in the second generation FCT-T format, which is pin-compatible with the older FCT devices, but adds TTL (transistor-to-transistor logic) outputs for significantly lower ground bounce and improved system noise immunity. Cypress also offers the most popular devices with on-chip 25-ohm termination resistors (FCT2-T) to further lower ground bounce with no speed loss. Included in the new product family is the CYBUS3384, a bus switch that enables bidirectional data transfer between multiple bus systems or between 5 volt and 3.3 volt devices. Cypress also offers 16-bit versions of popular FCT products. This broad product offering is produced on Cypress's high-volume, CMOS manufacturing lines.

Data Communications Division

This is an especially significant area for Cypress since it represents a more market-driven orientation for the company in a fast-growing market segment. As part of the new company strategy, Cypress has dedicated this product line to serve the high-speed data communications market with a range of products from the physical connection layer to system-level solutions. HOTLink™, high-speed, point-to-point serial communications chips have been well received. HOTLink, along with the recently announced SONET/SDS Serial Transceiver (SST™), address the fast-growing market segments of Asynchronous Transfer Mode (ATM) and Fibre Channel communications. The data communications division encompasses related products includ-

ing RoboClock, a programmable skew clock buffer that adjusts complex timing control signals for a broad range of systems. The division also offers a broad range of First-In, First-Out (FIFO) memories, used to communicate data between systems operating at different frequencies, and Dual-Port Memories, used to distribute data to two different systems simultaneously.

Computation Products Division

This division focuses on the high-volume, high-growth market surrounding the desktop computer. It is the second of Cypress's market-oriented divisions. The division includes timing technology products offered through Cypress's IC Designs Subsidiary in Kirkland, Washington, and a new line of PC chipsets. IC Designs products are used widely in personal computers and disk drives, and the product line provides Cypress with major inroads into these growing markets. IC Designs clock oscillators control the intricate timing of all aspects of a computer system, including signals for the computer's central processing unit (CPU), keyboard, disk drives, system bus, serial port, and real-time clock. They replace all of the metal can oscillators used in the system. This product line includes QuiXTAL™ – a programmable metal can oscillator that replaces individual oscillators used to control timing signals in virtually every type of electronics equipment. Cypress's chipset offerings include products for 486-based personal computers, as well as PCI local bus controllers for graphics and multimedia desktop applications. Cypress has announced plans to introduce a low-power, 3.3 volt chipset for the Pentium P54C, as well as P54C bus controller.

Cypress Facilities

Cypress operates wafer fabrication facilities in California's Silicon Valley (San Jose), Round Rock (Austin), Texas, and Bloomington, Minnesota. The company's fourth wafer fab, located adjacent to the Bloomington, Minnesota facility, is scheduled to go on-line in mid-1995. There are additional Cypress Design Centers in Starkville, Mississippi, Colorado Springs, Colorado, and the United Kingdom, and a PLD software design group in Beaverton, Oregon. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas and Minnesota facilities, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.1 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

The company has also received ISO9000 registration, a standard model of quality assurance that is awarded to companies with exacting standards of quality management, production, and inspections.

Attention to assembly is equally critical. Cypress manufactures 100 percent of our wafers in the United States, at our front-end fabrication sites in California (San Jose), Minnesota (Bloomington), and Texas (Round Rock). Cypress Texas, our largest fab, and Cypress Minnesota, our newest fab, are both Class 1 facilities.

To improve our global competitiveness, we chose to move most of our back-end assembly, test, and mark operations to a facility in Thailand. Be assured that Cypress's total quality commitment extends to the new site—Cypress Bangkok.

The move to Bangkok consummated an intense search by Cypress for a world-class, environmentally sophisticated facility that we could bring on line quickly. The Cypress search team scrutinized fifteen manufacturing facilities in five countries and chose a site managed by Alphatec Electronics Co., Ltd., a privately owned, entrepreneurial company promoted by the Thailand Board of Investment. Cypress Bangkok occupies almost 25,000 square feet—a significant portion of the manufacturing floor space available within the facility. The full facility at Bangkok occupies more than 85,000 square feet on a site that encompasses 25 acres—sufficient room for expansion to a number of buildings in a campus-like setting.

Manufacturing at the site since 1990 with a charter to specialize in IC packaging, the Alphatec facility has almost a century of person-years experience working for U.S. semiconductor suppliers. Thoroughly modern, MIL 883-certified, and with fully developed administrative, logistic, and manufacturing systems in place, the facility has earned an exceptional reputation for hermetic assembly and out-going quality.

Cypress San Jose maintains complete management control of Cypress Bangkok's assembly, test, mark, and ship operations within the facility, thus assuring complete continuity of San Jose's back-end operations and quality.

Cypress has added Tape Automated Bonding (TAB) to its package offering. TAB, a surface-mount packaging technology, provides the densest lead and package footprint available for fully tested die.

From Cypress's facility in Minnesota, a VME Bus Interface Products group has been in operation since the acquisition of VTC's fab in 1990. Cypress manufactures VIC and VAC VME devices on the 0.8 micron CMOS process.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees ... all striving to make the best CMOS and BiCMOS products."

Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor overcame the classically held perceptions that CMOS was a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employed lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with older CMOS technologies.

Cypress pushed process development to new limits in the areas of PROMs (Programmable Read Only Memory) and EPLDs (Erasable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has been in use in MOS (Metal Oxide Silicon) since the early 1970s. EPROM technology has traditionally emphasized density while forsaking performance. Through improved technology, Cypress produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress introduced a sub-micron technology in 1987. This 0.8 micron breakthrough made Cypress's CMOS one of the most

advanced production processes in the world. The drive to maintain leadership in process technology has not stopped with the 0.8-micron devices. Cypress introduced a 0.65-micron process in 1991. A 0.5-micron process is currently in production.

Although not a requirement in the high-performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latch-up have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although in its earliest years, MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2-, 0.8-, 0.65-, and 0.5-micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules.

Latch-up, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: multilayer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching, and 100-percent stepper technology with the world's most advanced equipment.

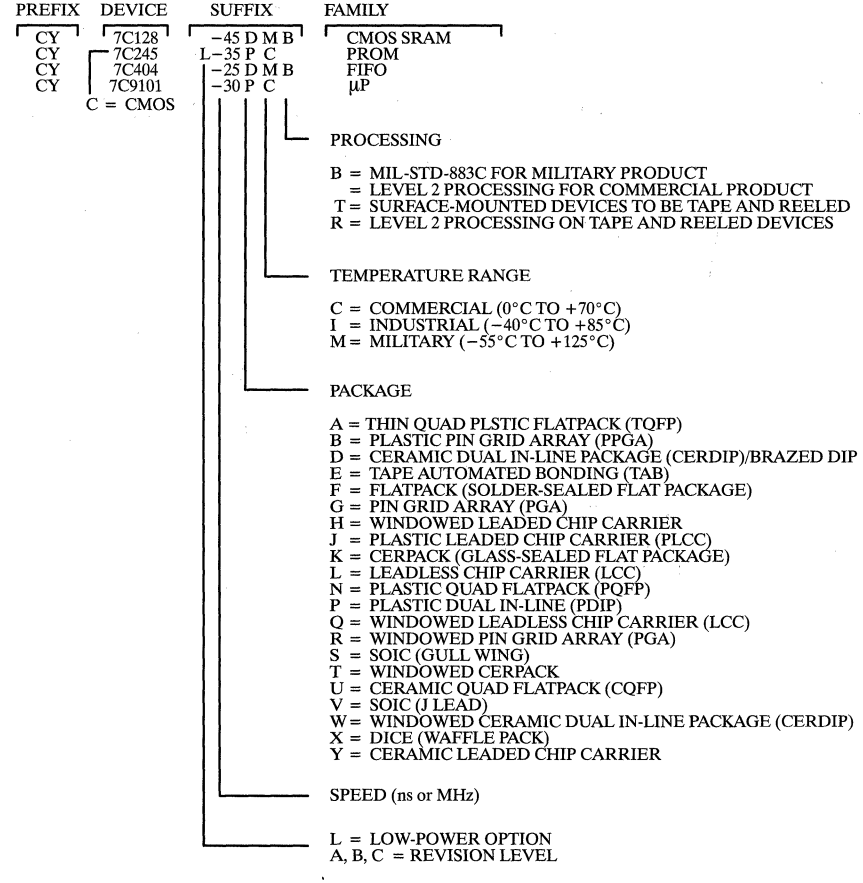
Cypress has developed BiCMOS technology to augment the capabilities of the Cypress CMOS processes. The new BiCMOS technology is based on the Cypress CMOS process for enhanced manufacturability. Like CMOS, the process is scalable, to take advantage of finer line lithography. Where speed is critical, Cypress BiCMOS allows increased transistor performance. It also allows reduced power in the non-speed critical sections of the design to optimize the speed/power balance. The BiCMOS process makes memories and logic operating up to 400 MHz possible.

Cypress technologies have been carefully designed, creating products that are "only the best" in high-speed, excellent reliability, and low power.

Ordering Information

In general, the valid ordering codes for all products (except modules and VMEbus products) follow the format below; e.g., CY7C128–45DMB, PALC16R8L–35PC.

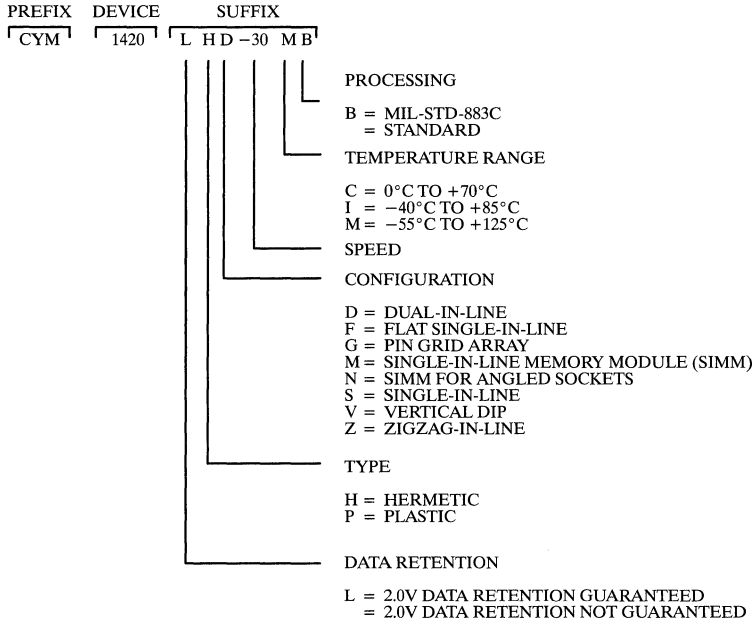
RAM, PROM, FIFO, µP, ECL



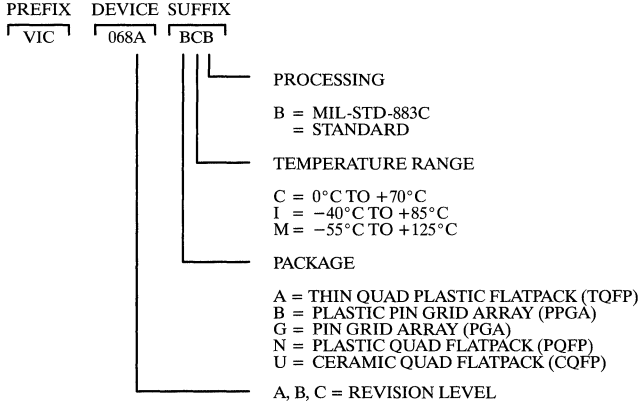
Cypress FSCM #65786

The codes for module and VMEbus products follow the the formats below.

Modules



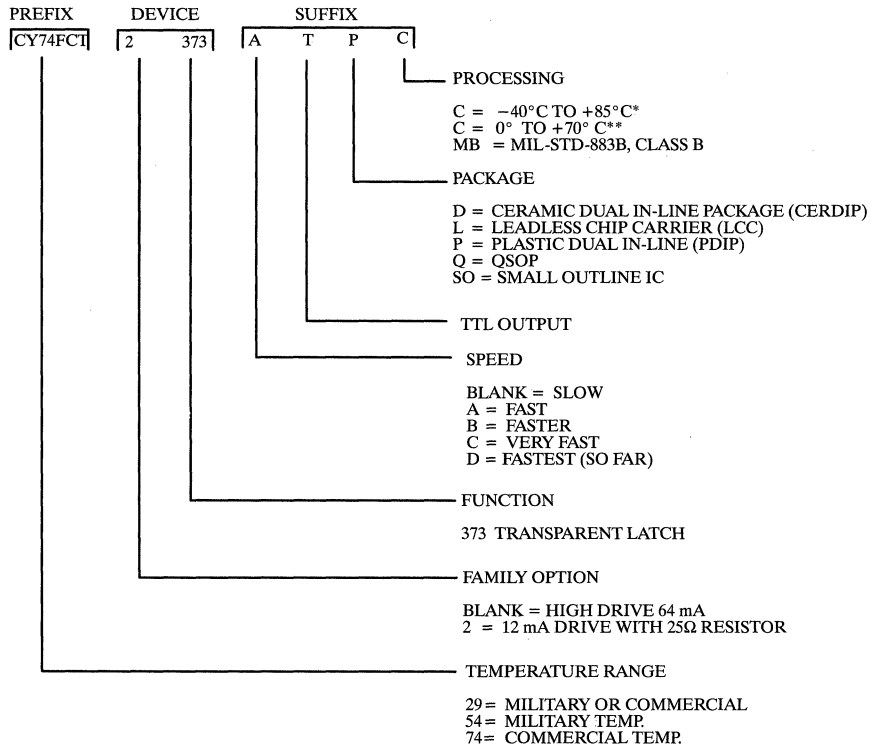
VMEbus Products



Cypress FSCM #65786

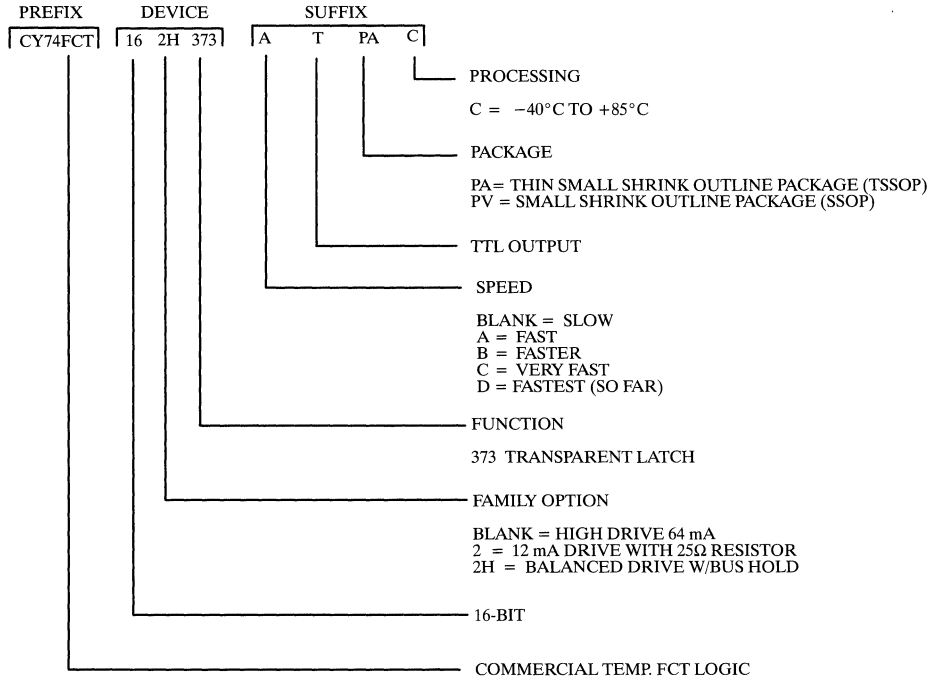
Ordering Information

FCT Octal Products



* COMMERCIAL TEMPERATURE IS −40°C TO +85°C FOR "STANDARD", "A", AND "B" SPEED
** COMMERCIAL TEMPERATURE IS 0°C TO +70°C FOR "C" SPEED

FCT 16-Bit Products



ICD

PREFIX	DEVICE	SUFFIX	OPTION
ICD	2061A	SC	−1
CY	2254	SC	−1

Datasheets Available Upon Request

Datasheets listed here are not in this catalog but can be obtained from a Cypress Sales Representative.

Static RAMs (Random Access Memory)

Device Number	Description
CY2147	4096 x 1 Static R/W RAM
CY2148/CY21L48/CY2149/CY21L49	1024 x 4 Static R/W RAM
CY6116	2048 x 8 Static R/W RAM
CY6116A/CY6117A	2048 x 8 Static R/W RAM
CY7C122	256 x 4 Static R/W RAM Separate I/O
CY7C128	2048 x 8 Static R/W RAM
CY7C147	4096 x 1 Static RAM
CY7C167	16,384 x 1 Static R/W RAM
CY7C168/CY7C169	4096 x 4 Static RAM
CY7C170	4096 x 4 Static R/W RAM
CY7C171/CY7C172	4096 x 4 Static R/W RAM Separate I/O
CY7C183/CY7C184	2 x 4096 x 16 Cache RAM
CY7C186	8K x 8 Static RAM
CY7C189/CY7C190	16 x 4 Static R/W RAM
CY7C198	32K x 8 Static R/W RAM
CY74S189/CY27LS03/CY27S03/CY27S07	16 x 4 Static R/W RAM
CY93L422A/CY93422/CY93L422	256 x 4 Static R/W RAM

FIFOs

Device Number	Description
CY3341	64 x 4 Serial Memory FIFO

Logic

Device Number	Description
CY2901C	CMOS 4-Bit Slice
CY2909/11	CMOS Microprogram Sequencers
CY2910	CMOS Microprogram Controller
CY7C901	CMOS 4-Bit Slice
CY7C909/11	CMOS Microprogram Sequencers
CY7C910	CMOS Microprogram Controller

Modules

Device Number	Description
CYM1466	512K x 8 Static RAM Module
CYM1611	16K x 16 Static RAM Module
CYM1830	64K x 32 Static RAM Module

Cypress Semiconductor Bulletin Board System (BBS) Announcement

Cypress Semiconductor supports a 24-hour electronic Bulletin Board System (BBS) that allows Cypress Applications to better serve our customers by allowing them to transfer files to and from the BBS.

The BBS is set up to serve in multiple ways. One of its purposes is to allow customers to receive the most recent versions of Cypress programming software. Another is to allow the customers to send PLD programming files that they are having trouble with to the BBS. Cypress Applications can then find the errors in the files, correct them, and place them back on the BBS for the customer to download. The customer may also ask questions in our open forum message area. The sysop (system operator) will forward these questions to the appropriate applications engineer for an answer. The answers then get posted back into the forum. The BBS also allows the customer to communicate with their local FAE electronically, and to download both application notes and the latest versions of selected datasheets.

Communications Set-Up

The BBS uses USRobotics HST Dual Standard modems capable of 14.4-Kbaud rates without compression and rates upwards of 19.2-Kbaud with compression. It is compatible with CCITT V.32 bis, V.32, V.22 (2400-baud), Bell 212A (1200-baud), CCITT V.42, and CCITT V.42 bis. It also handles MNP levels 2, 3, 4, and 5.

To call the BBS, set your communication package parameters as follows:

Baud Rate: 1200 baud to 19.2 Kbaud. Max. is determined by your modem.
Data Bits: 8
Parity: None (N)
Stop Bits: 1

In the U.S. the phone number for the BBS is (408) 943−2954. In Japan the BBS number is 81−423−69−8220. In Europe the BBS number is 49−810−62−2675. These numbers are for transmitting data only.

If the line is busy, please retry at a later time. When you access the BBS, an initial screen with the following statement will appear:

```
Rybbs Bulletin Board
```

After you choose the graphics format you want to use, the system will ask for your first and last name. If you are a first-time user, you will be asked a few questions for the purposes of registration. Otherwise you will be asked for your password, and then you will be logged onto the BBS, which is completely menu driven.

Downloading Application Notes and Datasheets

A complete listing of files that may be downloaded is included on the BBS. Application notes and selected datasheets are available for downloading in two formats, PCL and Postscript. An "hp" in front of the file name indicates it is a PCL file and can be downloaded to Hewlett-Packard LaserJets and compatible printers. Files without the hp preceding them are in Postscript and can be downloaded to any Postscript printer.

If you have any problems or questions regarding the BBS, please contact Cypress Applications at (408) 943−2821 (voice).

Contact a Cypress representative or use the Cypress Bulletin Board System to get copies of the application notes listed here.

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HOTLink Copper Interconnect—Maximum Length vs. Frequency
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VIC068 Special Features and Tips
VIC164 to Motorola 68040 Interface

Timing Products

Crystal Oscillator Topics
CY7B991 and CY7B992 (RoboClock) Test Mode
ECL Outputs
Everything You Need to Know About CY7B991/CY7B992 (RoboClock) But were Afraid to Ask
Innovative RoboClock Application
Using the CY7B991 with the 50-MHz 486 Cache Module and the 40-MHz R3000

Glossary - '91
Glossary - '93

Static RAMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
64	16x4—Inverting	16	CY7C189	t_{AA} = 15, 25	55 @ 25	D, P
64	16x4—Non-Inverting	16	CY7C190	t_{AA} = 15, 25	55 @ 25	L, P
64	16x4—Inverting	16	CY74S189	t_{AA} = 35	90 @ 35	D, P
64	16x4—Inverting	16	CY27S03A	t_{AA} = 25, 35	90 @ 25	D, P
64	16x4—Non-Inverting	16	CY27S07A	t_{AA} = 25, 35	90 @ 25	D, P
1K	256x4	22	CY7C122	t_{AA} = 15, 25, 35	60 @ 25	D, L, P, S
1K	256x4	24S	CY7C123	t_{AA} = 7, 9, 10, 12, 15	120 @ 7	L, P, V
1K	256x4	22	CY9122/91L22	t_{AA} = 25, 35, 45	120 @ 25	P
1K	256x4	22	CY93422A/93L422A	t_{AA} = 35, 45	80 @ 45	L, P
4K	4Kx1—CS Power-Down	18	CY7C147	t_{AA} = 25, 35, 45	80/10 @ 35	D, P
4K	4Kx1—CS Power-Down	18	CY2147/21L47	t_{AA} = 35, 45, 55	125/25 @ 35	D, P
4K	1Kx4—CS Power-Down	18	CY7C148	t_{AA} = 25, 35, 45	80/10 @ 35	D, P
4K	1Kx4—CS Power-Down	18	CY2148/21L48	t_{AA} = 35, 45, 55	120/20 @ 35	D, P
4K	1Kx4	18	CY7C149	t_{AA} = 25, 35, 45	80 @ 35	D, L, P
4K	1Kx4	18	CY2149/21L49	t_{AA} = 35, 45, 55	120 @ 35	D, P
4K	1Kx4—Separate I/O, Reset	24S	CY7C150	t_{AA} = 10, 12, 15, 25, 35	90 @ 12	D, P, S
16K	2Kx8—CS Power-Down	24	CY7C128A	t_{AA} = 15, 20, 25, 35, 45, 55	90/20 @ 55	D, L, P, V
16K	2Kx8—CS Power-Down	24	CY6116A	t_{AA} = 20, 25, 35, 45, 55	80/20 @ 55	D, L
16K	2Kx8—CS Power-Down	32	CY6117A	t_{AA} = 20, 25, 35, 45, 55	80/20 @ 55	L
16K	16Kx1—CS Power-Down	20	CY7C167A	t_{AA} = 15, 20, 25, 35, 45	50/15 @ 45	D, P, V
16K	4Kx4—CS Power-Down	20	CY7C168A	t_{AA} = 15, 20, 25, 35, 45	70/15 @ 45	D, P, V
16K	4Kx4	20	CY7C169A	t_{AA} = 15, 20, 25, 35, 45	70 @ 45	P
16K	4Kx4—Output Enable	22S	CY7C170A	t_{AA} = 15, 20, 25, 35, 45	90 @ 45	P, V
16K	4Kx4—Separate I/O	24S	CY7C171A	t_{AA} = 15, 20, 25, 35, 45	90 @ 45	D, L, P, V
16K	4Kx4—Separate I/O	24S	CY7C172A	t_{AA} = 15, 20, 25, 35, 45	90 @ 45	D, L, P
64K	8Kx8—CS Power-Down	28S	CY7C185	t_{AA} = 15, 20, 25, 35	120/20 @ 15	P, V
64K	8Kx8—CS Power-Down	28S	CY7C185A	t_{AA} = 15, 20, 25, 35, 45	125/40 @ 25	D, L
64K	8Kx8—CS Power-Down	28	CY7C186A	t_{AA} = 15, 20, 25, 35, 45	125/40 @ 25	D, L
64K	8Kx8—CS Power-Down	28	CY7C186	t_{AA} = 20, 25, 35	120/20 @15	P
64K	64Kx1—CS Power-Down	22S	CY7C187A	t_{AA} = 15, 20, 25, 35, 45	80/40 @ 25	D, L
64K	64Kx1—CS Power-Down	22S	CY7C187	t_{AA} = 15, 20, 25, 35	90/40 @ 15	P, V
64K	16Kx4—CS Power-Down	22S	CY7C164	t_{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Output Enable	24S	CY7C166	t_{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Separate I/O, Transparent Write	28S	CY7C161	t_{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Separate I/O	28S	CY7C162	t_{AA} = 15, 20, 25, 35	115/40 @ 15	P, V
64K	16Kx4—Separate I/O, Transparent Write	28	CY7C161A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
64K	16Kx4—Separate I/O	28	CY7C162A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
64K	16Kx4—CS Power-Down	22	CY7C164A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
64K	16Kx4—Output Enable	24	CY7C166A	t_{AA} = 15, 20, 25, 35, 45	100/40 @ 20	D, L
72K	8Kx9	28	CY7C182	t_{AA} = 25, 35, 45, 55	140/35 @ 25	P, V, S
256K	32Kx8—CS Power-Down	28	CY7C198	t_{AA} = 25, 35, 45	160/35 @ 25	L, P
256K	32Kx8—CS Power-Down	28S	CY7C199	t_{AA} = 12, 15, 20, 25, 35, 45, 55	170/30 @ 25	D, L, P, V, Z
256K	32Kx8—CS Power-Down (3.3V)	28S	CY7C1399	t_{AA} = 15, 20, 25	60/25 @ 20	P, V
256K	64Kx4—CS Power-Down	24	CY7C194	t_{AA} = 12, 15, 20, 25, 35, 45	160/30 @ 25	D, L, P, V

Note: Please contact a Cypress Representative for product availability.

Static RAMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
256K	64K x 4—CS Power Down with OE	28	CY7C196	t_{AA} = 12, 15, 20, 25, 35, 45	160/30 @ 25	D, L, P, V
256K	64K x 4—Separate I/O, Transparent Write	28	CY7C191	t_{AA} = 12, 15, 20, 25, 35, 45	120/30 @ 25	D, P
256K	64K x 4—Separate I/O	28	CY7C192	t_{AA} = 12, 15, 20, 25, 35, 45	120/30 @ 25	D, L, P, V
256K	64K x 4—CS Power-Down w/ OE	28	CY7C195	t_{AA} = 12, 15, 20, 25, 35	160/30 @ 25	D, L, P, V
256K	256K x 1—CS Power-Down	24	CY7C197	t_{AA} = 12, 15, 20, 25, 35, 45	105/30 @ 25	D, L, P, V
256K	32K x 8—Synchronous	28	CY7C193	t_{AA} = 20, 22	150 @ 20	V
288K	32K x 9—CS Power-Down	32	CY7C188	t_{AA} = 15, 20, 25, 35	160/40 @ 12	P, V
576K	32K x 18—Burst	52	CY7C178	t_{CDV} = 8, 10, 12 (@ 0 pF)	295/60 @ 8	J, N
576K	32K x 18—Burst	52	CY7C179	t_{CDV} = 8. 10. 12 (@ 0 pF)	295/60 @ 8	J, N
1M	64K x 18—Burst	52	CY7C1031	t_{CDV} = 8, 10, 12 (@ 0 pF)	265 @ 8	J, N
1M	64K x 18—Burst	52	CY7C1032	t_{CDV} = 8, 10, 12 (@ 0 pF)	265 @ 8	J, N
1M	64K x 18—Burst (3.3V)	52	CY7C1331	t_{CDV} = 12, 16, 19 (@ 0 pF)	180 @ 12	J, N
1M	64K x 18—Burst (3.3V)	52	CY7C1332	t_{CDV} = 12, 16, 19 (@ 0 pF)	180 @ 12	J, N
1M	128K x 8—CS Power-Down	32	CY7C1009	t_{AA} = 12, 15, 20, 25	185 @ 12	D, L, P, V
1M	128K x 8—CS Power-Down	32	CY7C109A	t_{AA} = 12, 15, 20, 25, 35	185 @ 12	D, L, P, V
1M	256K x 4—CS Power-Down	28	CY7C1006	t_{AA} = 12, 15, 20, 25	165 @ 12	D, P, V
1M	256K x 4—CS Power-Down w/ OE	28	CY7C106A	t_{AA} = 12, 15, 20, 25, 35	165 @ 12	D, P, V
1M	256K x 4—Separate I/O, Transparent Write	32	CY7C1001	t_{AA} = 12, 15, 20, 25	165 @ 12	D, P, V
1M	256K x 4—Separate I/O, Transparent Write	32	CY7C101A	t_{AA} = 12, 15, 20, 25, 35	165 @ 12	D, P, V
1M	256K x 4—Separate I/O	32	CY7C1002	t_{AA} = 12, 15, 20, 25	165 @ 12	D, P, V
1M	256K x 4—Separate I/O	32	CY7C102A	t_{AA} = 12, 15, 20, 25, 35	165 @ 12	D, P, V
1M	1M x 1—CS Power-Down	28	CY7C1007	t_{AA} = 12, 15, 20, 25	150 @ 12	D, P, V
1M	1M x 1—CS Power-Down	28	CY7C107A	t_{AA} = 12, 15, 20, 25, 35	150 @ 12	D, P, V

Dual-Port RAMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
8K	1K x 8—Dual-Port Master	48	CY7C130	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
8K	1K x 8—Dual-Port Slave	48	CY7C140	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
8K	1K x 8—Dual-Port Master	52	CY7C131	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
8K	1K x 8—Dual-Port Slave	52	CY7C141	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
16K	2K x 8—Dual Port Master	48	CY7C132	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
16K	2K x 8—Dual-Port Slave	48	CY7C142	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
16K	2K x 8—Dual-Port Master	52	CY7C136	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
16K	2K x 8—Dual-Port Slave	52	CY7C146	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
32K	4K x 8—Dual-Port, No Arbitration	48	CY7B134	t_{AA} = 20, 25, 35	240	D, L, P
32K	4K x 8—Dual-Port, w/Semaph	52	CY7B1342	t_{AA} = 20, 25, 35	240	J, L
32K	2K x 16—Dual-Port Slave	68	CY7C143	t_{AA} = 15, 25, 35	150	J, A
32K	2K x 16—Dual-Port Master	68	CY7C133	t_{AA} = 15, 25, 35	150	J, A
32K	4K x 8—Dual-Port, w/ Semaph, Busy, Int	68	CY7B138	t_{AA} = 15, 25, 35	260	J, L
32K	4K x 8—Dual-Port, No Arbitration	52	CY7B135	t_{AA} = 20, 25, 35	240	J, L
32K	4K x 9—Dual-Port, w/ Semaph, Busy, Int	68	CY7B139	t_{AA} = 15, 25, 35	260	J, L
64K	8K x 8—Dual-Port, w/ Semaph, Busy, Int	68	CY7B144	t_{AA} = 15, 25, 35	260	J, L, A
64K	8K x 9—Dual-Port, w/ Semaph, Busy, Int	68	CY7B145	t_{AA} = 15, 25, 35	260	J, L, A

Note: Please contact a Cypress Representative for product availability.

Dual-Port RAMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
64K	4K x 16—Dual-Port, w/ Semaph, Busy, Int	84	CY7C024	t_{AA} = 15, 25, 35	200	J,A
64K	4K x 18—Dual-Port, w/ Semaph, Busy, Int	84	CY7C0241	t_{AA} = 15, 25, 35	200	J,A
128K	8K x 16—Dual-Port w/ Semaph, Busy, Int	84	CY7C025	t_{AA}=15, 25, 35	200	J,A
128K	8K x 18—Dual-Port w/ Semaph, Busy, Int	84	CY7C0251	t_{AA}=15, 25, 35	200	J,A
128K	16K x 8—Dual-Port w/ Semaph, Busy, Int	68	CY7C006	t_{AA}=15, 25, 35	200	J,N
128K	16K x 9—Dual-Port w/ Semaph, Busy, Int	68	CY7C016	t_{AA}=15, 25, 35	200	J,N

SRAM Modules – Secondary Cache Subsystems

Size	Organization	Pins	Part Number	Speed (MHz)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
128K	PCIset Secondary Cache	112	CYM7420	f_{max}=33 MHz	1100	PB
256K	PCIset Secondary Cache	112	CYM7421	f_{max}=33 MHz	1200	PB
128K	PCIset Secondary Cache	112	CYM7424	f_{max}=33 MHz	1000	PB
256K	PCIset Secondary Cache	112	CYM7425	f_{max}=33 MHz	1600	PB
128K	i486 Secondary Cache	128	CYM7450	f_{max}=33 MHz	900	PM
256K	i486 Secondary Cache	128	CYM7451	f_{max}=33 MHz	1500	PM
128K	i486 Secondary Cache	112	CYM7427	f_{max}=33 MHz		
256K	i486 Secondary Cache	112	CYM7428	f_{max}=33 MHz		
256K	i486 Secondary Cache	128	CYM7491	f_{max}=33 MHz	1300	PM
128K	i486 Secondary Cache	112	CYM9236	f_{max}=33 MHz		
256K	i486 Secondary Cache	112	CYM9237	f_{max}=33 MHz		
256K	Pentium Cache	160	CYM7432	f_{max}=60 MHz	1300	PB
256K	P54C Cache (Intel™ Neptune)	160	CYM74AP54	f_{max}=60, 66 MHz		
256K	P54C Cache (Intel Neptune)	160	CYM74SP54	f_{max}=60, 66 MHz		
512K	P54C Cache (Intel Neptune)	160	CYM74SP55	f_{max}=60, 66 MHz		
256K	P54C Cache (Intel Triton)	160	CYM74A430	50, 60, 66 MHz		
256K	P54C Cache (Intel Triton)	160	CYM74S430	50, 60, 66 MHz		
512K	P54C Cache (Intel Triton)	160	CYM74S431	50, 60, 66 MHz		
256K	P54C Cache (OPTi Viper)	160	CYM74A550	50, 60, 66 MHz		
256K	P54C Cache (OPTi Viper)	160	CYM74S550	50, 60, 66 MHz		
512K	P54C Cache (OPTi Viper)	160	CYM74S551	50, 60, 66 MHz		
256K	P54C Cache (VLSI 590)	160	CYM74A590	60, 66 MHz		
256K	P54C Cache (VLSI 590)	160	CYM74S590	60, 66 MHz		
512K	P54C Cache (VLSI 590)	160	CYM74S591	60, 66 MHz		

32-Bit Standard SRAM Module Family

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
512K	16K x 32	64	CYM1821	t_{AA} = 12, 15 t_{AA} = 20, 25, 30, 35, 45	960 @ 12 720 @ 20	PM, PZ PM, PZ
2M	64K x 32	64	CYM1831	t_{AA} = 15, 20, 25, 30, 35, 45	720 @ 25	PM, PN, PZ
4M	128K x 32	64	CYM1836	t_{AA} = 20, 25, 30, 35, 45 t_{AA} = 15	480 @ 20 760 @ 15	PM, PZ
8M	256K x 32	64	CYM1841	t_{AA} = 25, 30, 35, 45, 55 t_{AA} = 20 t_{AA} = 15	960 @ 25 1120 @ 20 1600 @ 15	PM, PN, PZ
8M	256K x 32 (72-pin Superset)	72	CYM1841AP7	t_{AA}=15, 20, 25, 30, 35, 45	960@25 1120@20 1600@15	PM
16M	512K x 32 (72-pin Superset)	72	CYM1846	t_{AA}=25, 30, 35	800	PM, PZ
32M	1M x 32 (64-pin Superset)	72	CYM1851	t_{AA} = 25, 30, 35	1250 @ 30	PM, PN, PZ

Note: Please contact a Cypress Representative for product availability.

8-, 16-, and 24-Bit SRAM Modules, 32-Bit PGA and DIP Modules

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
2M	256Kx8—JEDEC Sep I/O	60	CYM1441	t_{AA} = 20, 25, 35, 45	960 @ 25	PZ
4M	512Kx8—JEDEC	32	CYM1464	t_{AA} = 20, 25, 30, 35, 45, 55, 70	300 @ 30	PD
4M	512Kx8—JEDEC	32	CYM1465	t_{AA} = 70, 85, 100, 120, 150	110 @ 70	PD
8M	1Mx8	36	CYM1471	t_{AA} = 85, 100, 120	110 @ 95	PS
16M	2Mx8	36	CYM1481	t_{AA} = 85, 100, 120	110 @ 85	PS
1M	64Kx16	40	CYM1622	t_{AA} = 15, 20, 25, 30, 35, 45	400 @ 25	PV
768K	32Kx24	56	CYM1720	t_{AA} = 15, 20, 25, 30, 35	330 @ 25	PZ
1.5M	64Kx24	56	CYM1730	t_{AA} = 25, 30, 35	510 @ 25	PZ
1M	32Kx32	66	CYM1828	t_{AA} = 25, 30, 35, 45, 55, 70	400 @ 25	HG
2M	64Kx32	60	CYM1830	t_{AA} = 25, 30, 35, 45, 55	880 @ 25	HD
4M	128Kx32	66	CYM1838	t_{AA} = 25, 30, 35	720 @ 25	HG
8M	256Kx32	60	CYM1840	t_{AA} = 20, 25, 30, 35, 45, 55	1120 @ 25	PD

DRAM Controller Modules

Organization	Bus Width	Part Number	Speed (MHz)	Package
DRAM Accelerator	32-Bit	CYM7232	25/33/40	PGC
DRAM Accelerator	64-Bit	CYM7264	25/33/40	PGC

PLDs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
PAL20	16L8	20	PAL16L8	t_{PD} = 4.5/5/7	180	D, J, L, P
PAL20	16R8	20	PAL16R8	$t_{S/CO}$ = 2.5/4.5, 2.5/5, 3.5/6	180	D, J, L, P
PAL20	16R6	20	PAL16R6	$t_{PD/S/CO}$ = 4.5/2.5/4.5, 5/2.5/5, 7/3.5/6	180	D, J, L, P
PAL20	16R4	20	PAL16R4	$t_{PD/S/CO}$ = 4.5/2.5/4.5, 5/2.5/5, 7/3.5/6	180	D, J, L, P
PAL20	16L8	20	PALC16L8/L	t_{PD} = 20	70, 45	D, L, P, Q, V, W
PAL20	16R8	20	PALC16R8/L	$t_{S/CO}$ = 15/12	70, 45	D, L, P, Q, V, W
PAL20	16R6	20	PALC16R6/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W
PAL20	16R4	20	PALC16R4/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W
PALCE20	16V8—Macrocell	20S	PALCE16V8	$t_{PD/S/CO}$ = 5/3/4, 7.5/5/5, 10/7.5/7, 15/12/10, 25/15/12	115/90	D, J, L, P
PALCE20	16V8—Macrocell	20S	PALCE16V8L	$t_{PD/S/CO}$ = 15/12/10, 25/15/12	55	D, J, L, P, Q
PALCE24	20V8—Macrocell	24	PALCE20V8	$t_{PD/S/CO}$ = 5/3/4, 7.5/5/5, 10/7.5/7, 15/12/10, 25/15/12	115/90	D, J, L, P
PALCE24	20V8—Macrocell	24	PALCE20V8L	$t_{PD/S/CO}$ = 15/12/10, 25/15/12	55	D, J, L, P, Q
PAL24	22V10—Macrocell	24S	PALC22V10/L	$t_{PD/S/CO}$ = 25/15/15	90, 55	D, J, K, L, P, Q, W
PAL24	22V10—Macrocell	24S	PALC22V10B	$t_{PD/S/CO}$ = 15/10/10	90	D, H, J, K, L, P, Q, W
PAL24	22V10—Macrocell	24S	PAL22V10C	$t_{PD/S/CO}$ = 6/3/5.5, 7.5/3/6, 10/3.6/7.5	190	D, J, L, P
PAL24	22VP10—Macrocell	24S	PAL22VP10C	$t_{PD/S/CO}$ = 6/3/5.5, 7.5/3/6, 10/3.6/7.5	190	D, J, L, P
PALCE24	22V10—Macrocell	24	PALC22V10D	$t_{PD/S/CO}$ = 7.5/5/5, 10/6/7, 15/10/8	130/90/90	D, J, L, P
PAL24	22V10—Macrocell	24	PAL22V10G	$t_{PD/S/CO}$ = 5/2.5/4, 6/3/5.5	190	J, L
PAL24	22VP10—Macrocell	24	PAL22VP10G	$t_{PD/S/CO}$ = 5/2.5/4, 6/3/5.5	190	J, L
PLD24	20G10—Generic	24S	PLDC20G10	$t_{PD/S/CO}$ = 25/15/15	55	D, J, L, P, Q, W
PLD24	20G10—Generic	24S	PLDC20G10B	$t_{PD/S/CO}$ = 15/12/10	70	D, H, J, L, P, Q, W
PLD24	20G10—Generic	24S	PLD20G10C	$t_{PD/S/CO}$ = 7.5/3/6.5, 10/3.6/7.5	190	D, J, L, P

Note: Please contact a Cypress Representative for product availability.

PLDs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
PLD24	20RA10—Asynchronous	24S	PLD20RA10	$t_{PD/S/CO}$ = 15/10/15	80	D, H, J, L, P, Q, W
PLD28	7C330—State Machine	28S	CY7C330	$f_{MAX.}$, t_{IS}, t_{CO} = 66 MHz/3ns/12ns	130@50 MHz	D, H, J, L, P, Q, W
PLD28	7C331—Asynchronous, Registered	28S	CY7C331	$t_{PD/S/CO}$ = 20/12/20	120@25 ns	D, H, J, L, P, Q, W
PLD28	7C335—Universal Synchronous	28S	CY7C335	f_{MAX}/t_{IS} = 100 MHz/2ns, 83 MHz/2ns	140	D, H, J, L, P, Q, W

CPLDs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA)	Packages
MAX28	7C344—32 Macrocell	28S	CY7C344/B	$t_{PD/S/CO}$ = 15/9/10, 10/6/5	200/150	D, H, J, P, W
MAX44	7C343—64 Macrocell	44	CY7C343/B	$t_{PD/S/CO}$ = 20/12/12, 12/8/6	135/125	H, J, R
MAX68	7C342—128 Macrocell	68	CY7C342/B	$t_{PD/S/CO}$ = 25/15/14, 12/8/6	250/225	H, J, R
MAX84	7C341—192 Macrocell	84	CY7C341/B	$t_{PD/S/CO}$ = 25/20/16, 15/10/7	380/360	H, J, R
MAX100	7C346—128 Macrocell	84, 100	CY7C346/B	$t_{PD/S/CO}$ = 25/15/14, 15/10/7	250/225	H, J, N, R
FLASH370—44	7C371—32-Macrocell Flash CPLD	44	CY7C371	$f_{MAX}/t_S/t_{CO}$=143MHz/6.5 ns/6.5 ns	150/TBD	J, Y, A
FLASH370—44	7C372—64-Macrocell Flash CPLD	44	CY7C372	$f_{MAX}/t_S/t_{CO}$=100 MHz/6.5 ns/6.5 ns	180/TBD	J, Y
FLASH370—84	7C373—64-Macrocell Flash CPLD	84, 100	CY7C373	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/6.5 ns	180/TBD	A, J, G, Y
FLASH370—84	7C374—128-Macrocell Flash CPLD	84, 100	CY7C374	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/6.5 ns	300/TBD	A, J, G, Y
FLASH370—160	7C375—128-Macrocell Flash CPLD	160	CY7C375	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/6.5 ns	300/TBD	A, G, U
FLASH370—160	7C376—192-Macrocell Flash CPLD	160	CY7C376	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	A, G
FLASH370—240	7C377—192-Macrocell Flash CPLD	240	CY7C377	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	BGA, N, G
FLASH370—160	7C378—256-Macrocell Flash CPLD	160	CY7C378	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	A, G
FLASH370—240	7C379—256-Macrocell Flash CPLD	240	CY7C379	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	BGA, N, G

FPGAs

Size	Organization	Pins	Part Number	Speed Grade	I_{CC}/I_{SB} (mA)	Packages
pASIC380—1K	CMOS 8x12, 1K Gates FPGA	44	CY7C381A	—X, —0, —1, —2	I_{SB} = 10	J
pASIC380—1K	CMOS 8x12, 1K Gates FPGA	68, 100	CY7C382A	—X, —0, —1, —2	I_{SB} = 10	A, G, J
pASIC3380—1K 3.3V	3.3V CMOS 8x12, 1K Gates FPGA	44	CY7C3381A	—0, —1	I_{SB} = 2	J
pASIC3380—1K 3.3V	3.3V CMOS 8x12, 1K Gates FPGA	68, 100	CY7C3382A	—0, —1	I_{SB} = 2	A, J
pASIC380—2K	CMOS 12x16, 2K Gates FPGA	68	CY7C383A	—X, —0, —1, —2	I_{SB} = 10	J
pASIC380—2K	CMOS 12x16, 2K Gates FPGA	84, 100	CY7C384A	—X, —0, —1, —2	I_{SB} = 10	A, G, J
pASIC3380—2K 3.3V	3.3V CMOS 12x16, 2K Gates FPGA	68	CY7C3383A	—0, —1	I_{SB} = 10	J
pASIC3380—2K 3.3V	3.3V CMOS 12x16, 2K Gates FPGA	84, 100	CY7C3384A	—0, —1	I_{SB} = 10	A, J
pASIC380—4K	CMOS 16x24, 4K Gates FPGA	84, 100	CY7C385A	—X, —0, —1, —2	I_{SB} = 10	A, J
pASIC380—4K	CMOS 16x24, 4K Gates FPGA	144, 160	CY7C386A	—X, —0, —1, —2	I_{SB} = 10	A, G, U
pASIC3380—4K 3.3V	3.3V CMOS 16x24, 4K Gates FPGA	84, 100	CY7C3385A	—0, —1	I_{SB} = 10	A, J

Note: Please contact a Cypress Representative for product availability.

FPGAs (continued)

Size	Organization	Pins	Part Number	Speed Grade	I_{CC}/I_{SB} (mA)	Packages
pASIC3380–4K3.3V	3.3V CMOS 16x24, 4K Gates FPGA	144	CY7C3386A	–0, –1	I_{SB} = 10	A
pASIC380–8K	CMOS 24x32, 8K Gates FPGA	144, 160	CY7C387A	–X, –0, –1, –2	I_{SB} = 10	A, G
pASIC380–8K	CMOS 24x32, 8K Gates FPGA	208, 223	CY7C388A	–X, –0, –1, –2	I_{SB} = 10	N, G
pASIC3380–8K3.3V	3.3V CMOS 24x32, 8K Gates FPGA	144	CY7C3387A	–0, –1	I_{SB} = 10	A
pASIC3380–8K3.3V	3.3V CMOS 24x32, 8K Gates FPGA	208	CY7C3388A	–0, –1	I_{SB} = 10	N

PROMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
4K	512x8—Registered	24S	CY7C225A	$t_{SA/CO}$ = 18/12, 25/12, 30/15, 35/20, 40/25	90 @ 18	D, J, L, P
8K	1024x8—Registered	24S	CY7C235A	$t_{SA/CO}$ = 18/12, 25/12, 30/15, 40/20	90 @ 18	D, J, L, P
8K	1Kx8	24S	CY7C281A	t_{AA} = 25, 30, 45	90@45, 100@30	D, J, P
8K	1Kx8	24	CY7C282A	t_{AA} = 25, 30, 45	90@45, 100@30	D, P
16K	2Kx8—Registered	24S	CY7C245A/ AL	$t_{SA/CO}$ = 15/10, 18/12, 25/12, 35/15, 45/25	120 @ 15, 90, 60 @ 25	D, J, K, L, P, Q, S, T, W
16K	2Kx8	24S	CY7C291A/ AL	t_{AA} = 20, 25, 35, 50	120 @ 20, 90, 60 @ 25	D, J, K, L, P, Q, S, T, W
16K	2Kx8	24	CY7C292A/ AL	t_{AA} = 20, 25, 35, 50	120 @ 20, 90 @ 25, 90, 60 @ 35	D, P
16K	2Kx8—Power-Down	24S	CY7C293A/ AL	t_{AA} = 20, 25, 35, 50	120/40 @ 20, 90/30 @ 25 60/15 @ 35	D, L, Q, P, W
32K	4Kx8	24S	CY7C243	t_{AA} = 20, 25, 35, 45, 55, 70	120	D, J, P, W
32K	4Kx8	24	CY7C244	t_{AA} = 20, 25, 35, 45, 55, 70	120	D, P, W
64K	8Kx8—Power-Down	24S	CY7C261	t_{AA} = 20, 25, 35, 45, 55	120/40 @ 20, 100/30 @ 35	D, J, L, P, Q, T, W
64K	8Kx8	24S	CY7C263	t_{AA} = 20, 25, 35, 45, 55	120 @ 20, 100 @ 35	D, J, L, P, Q, T, W
64K	8Kx8	24	CY7C264	t_{AA} = 20, 25, 35, 45, 55	120 @ 20, 100 @ 35	D, P, W
64K	8Kx8—Registered	28S	CY7C265	$t_{SA/CO}$ = 15/12, 18/15, 25/15, 40/20, 50/25	120 @ 15, 18, 100 @ 25, 40 80 @ 50	D, J, L, P, Q, W
64K	8Kx8—EPROM Pinout w/ Power-Down	28	CY7C266	t_{AA} = 20, 25, 35, 45	120/15 @ 20, 100/15 @ 35	D, L, P, Q, W
64K	8Kx8—Registered, Diagnostic	28S	CY7C269	$t_{SA/CO}$ = 15/12, 25/15, 40/20, 50/25	120 @ 15, 100 @ 40, 80 @ 50	D, J, L, P, Q, W
128K	16Kx8—CS Power-Down	28S	CY7C251	t_{AA} = 45, 55, 65	100/30	L, P, W
128K	16Kx8	28	CY7C254	t_{AA} = 45, 55, 65	100/30	P, W
256K	32Kx8—Power-Down	28S	CY7C271A	t_{AA} = 25, 30, 35, 45, 55	90/15	D, J, K, L, P, Q, T, W
256K	32Kx8—EPROM Pinout w/Power-Down	28	CY7C274	Replaced by CY27H256		
256K	32Kx8—Registered	28S	CY7C277	$t_{SA/CO}$ = 30/15, 40/20, 50/25	120	D, J, K L, P, Q, T, W
256K	16Kx16	44	CY7C276	t_{AA} = 25, 30, 35	175	H, J, Q
512K	64Kx8—EPROM Pinout w/Power-Down	28	CY7C286	Replaced by CY27H512		
512K	64Kx8—Registered	28S	CY7C287	$t_{SA/CO}$ = 45/15, 55/20, 65/25	120	D, J, L, P, Q, W

Note: Please contact a Cypress Representative for product availability.

EPROMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
64K	16Kx8—EPROM	24	CY27C64	t_{AA} = 70, 90, 120, 150, 200	100/15	D, J, P, W
128K	16Kx8—EPROM	28	CY27C128	t_{AA} = 45, 55, 70, 90, 120, 150, 200	45/15	D, J, P, W
256K	32Kx8—EPROM	28	CY27C256	t_{AA} = 45, 55, 70, 90, 120, 150, 200	45/15	D, J, P, W, Z (32-Pin)
256K	32Kx8—EPROM	28S	CY27C256T	t_{AA} = 45, 55, 70, 90, 120, 150, 200	45/15	W, Z (28-Pin)
256K	32Kx8—EPROM	28	CY27H256	t_{AA} = 25, 30, 35, 45, 55	50/15	D, J, P, W
512K	64Kx8—EPROM	28	CY27C512	t_{AA} = 70, 90, 120, 150, 200	40/15	D, J, L, P, Q, W, Z
512K	64Kx8—EPROM	28	CY27H512	t_{AA} = 25, 30, 35, 45, 55, 70	50/15	D, H, J, L, P, Q, W, Z
1M	128Kx8—EPROM	32	CY27C010	t_{AA} = 70, 90, 120, 150, 200	40/15	D, H, J, L, P, Q, W, Z
1M	128Kx8—EPROM	32	CY27H010	t_{AA} = 25, 30, 35, 45, 55	50/15	D, H, J, L, P, Q, W, Z

FIFOs

Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
64x4	16	CY3341	1.2, 2 MHz	45	D, P
64x4	16	CY7C401	5, 10, 15, 25 MHz	75	D, L, P
64x4—w/OE	16	CY7C403	10, 15, 25 MHz	75	D, L, P
64x5	18	CY7C402	5, 10, 15, 25 MHz	75	D, L, P
64x5—w/OE	18	CY7C404	10, 15, 25 MHz	75	D, L, P
64x8—w/OE and Almost Flags	28S	CY7C408A	15, 25, 35 MHz	120	D, L, P, V
64x9—w/Almost Flags	28S	CY7C409A	15, 25, 35 MHz	120	D, L, P, V
256x9—w/Half Full Flag	28	CY7C419	10, 15, 20, 25, 30, 40, 65	120	D, L, P, V
512x9—w/Half Full Flag	28	CY7C420	20, 25, 30, 40, 65	142/30	D, P
512x9—w/Half Full Flag	28S	CY7C421	10, 15, 20, 25, 30, 40, 65	142/30	D, J, L, P, V
512 x 9—Clocked	28S	CY7C441	14, 20, 30*	140/30	D, J, L, P, V
512 x 9—Clocked w/ Prog. Flags	32	CY7C451	14, 20, 30*	140/30	D, J, L
512x18—Clocked w/Prog. Flags	52	CY7C455	14, 20, 30*	160/40	J, L, N
1Kx9—w/ Half Full Flag	28	CY7C424	20, 25, 30, 40, 65	142/30	D, P
1Kx9—w/ Half Full Flag	28S	CY7C425	10, 15, 20, 25, 30, 40, 65	142/30	D, J, L, P, V
1Kx18—Clocked w/Prog. Flags	52	CY7C456	14, 20, 30*	160/40	J, L, N
2Kx9—w/ Half Full Flag	28	CY7C428	20, 25, 30, 40, 65	142/30	D, P
2Kx9—w/ Half Full Flag	28S	CY7C429	10, 15, 20, 25, 30, 40, 65	142/30	D, J, L, P, V
2Kx9—Bidirectional	28S	CY7C439	25, 30, 40, 65	147/40	D, J, L, P
2K x 9—Clocked	28S	CY7C443	14, 20, 30*	140/30	D, J, L, P, V
2K x 9—Clocked w/ Prog. Flags	32	CY7C453	14, 20, 30*	140/30	D, J, L
2Kx18—Clocked w/Prog. Flags	52	CY7C457	14, 20, 30*	160/40	J, L, N
4Kx9—w/ Half Full Flag	28	CY7C432	25, 30, 40, 65	140/25	D, P
4Kx9—w/Half Full Flag	28S	CY7C433	10, 15, 25, 30, 40, 65	140/25	D, J, L, P, V
8K x 9—w/ Half Full Flag	28	CY7C460	15, 25, 40	160	D, J, L, P
8K x 9—w/ Prog. Flags	28	CY7C470	15, 25, 40	160	D, J, L, P
16K x 9—w/ Half Full Flag	28	CY7C462	15, 25, 40	160	D, J, L, P
16K x 9—w/ Prog. Flags	28	CY7C472	15, 25, 40	160	D, J, L, P
32K x 9—w/ Half Full Flag	28	CY7C464	15, 25, 40	160	D, J, L, P
32K x 9—w/ Prog. Flags	28	CY7C474	15, 25, 40	160	D, J, L, P
64K x 9—Module	28	CYM4208	25, 30, 40	640/100	HD
128K x 9—Module	28	CYM4209	25, 30, 40	640/100	HD
64x9	32	CY7C4421	10, 15, 25, 35	50	J, A

Note: Please contact a Cypress Representative for product availability.

FIFOs (continued)

Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages
256x9	32	CY7C4201	10, 15, 25, 35	50	J, A
512x9	32	CY7C4211	10, 15, 25, 35	50	J, A
1Kx9	32	CY7C4221	10, 15, 25, 35	50	J, A
2Kx9	32	CY7C4231	10, 15, 25, 35	50	J, A
4Kx9	32	CY7C4241	10, 15, 25, 35	50	J, A
8Kx9	32	CY7C4251	10, 15, 25, 35	50	J, A
64x18	64, 68	CY7C4425	10, 15, 25, 35	100	J, A
256x18	64, 68	CY7C4205	10, 15, 25, 35	100	J, A
512x18	64, 68	CY7C4215	10, 15, 25, 35	100	J, A
1Kx18	64, 68	CY7C4225	10, 15, 25, 35	100	J, A
2Kx18	64, 68	CY7C4235	10, 15, 25, 35	100	J, A
4Kx18	64, 68	CY7C4245	10, 15, 25, 35	100	J, A

* Clocked FIFO [CY7C44x/45x] times are cycle times.

Logic

Description	Pins	Part Number	Speed	I_{CC}/I_{SB} (mA @ ns)	Packages
2901—4-Bit Slice	40	CY7C901	t_{CLK} = 23, 31 ns	70	D, J, L, P
2901—4-Bit Slice	40	CY2901	C	140	D, P
4x2901—16-Bit Slice	64	CY7C9101	t_{CLK} = 30, 40 ns	60	J, L, P, G
2909—Sequencer	28	CY7C909	t_{CLK} = 30, 40 ns	55	J, L, P
2911—Sequencer	20	CY7C911	t_{CLK} = 30, 40 ns	55	D, J, L, P
ECL/TTL Translator—10KH	84	CY10E383	t_{PD} = 2.5/3 ns	270	J, N
ECL/TTL Translator—100K	84	CY101E383	t_{PD} = 2.5/3 ns	270	J, N
2909—Sequencer	28	CY2909	A	70	D, P
2911—Sequencer	20	CY2911	A	70	D, P
2910—Controller (17-word Stack)	40	CY7C910	t_{CLK} = 40, 50, 93 ns	100	D, J, L, P
2910—Controller (9-word Stack)	40	CY2910	A	170	D, J, L, P

Design and Programming Tools

Description	Type	Part Number
Warp2 for PC	VHDL Design Tool	CY3120
Warp2 for Sun	VHDL Design Tool	CY3125
Warp3 for PC	VHDL/CAE Design Tool	CY3130
Warp3 for Sun	VHDL/CAE Design Tool	CY3135
Impulse3	Programmer	CY3500

VMEbus Interface Products

Description	Pins	Part Number	Transfer Rate (MB/s)	I_{CC} (mA)	Packages
VME Interface Controller	144/160	VIC068A	40	250	A, B, G, N, U
VME Address Controller	144/160	VAC068A	—	150	B, G, N, U
64-Bit VIC	144/160	VIC64	80	300	A, B, G, N, U
Bus Interface Logic Circuit	64	CY7C964	—	120	A, N, U
Slave VMEbus Interface Controller	64	CY7C960/1	80	250	A, G, N, U

Note: Please contact a Cypress Representative for product availability.

Communication Products

Description	Pins	Part Number	Speed (MHz)	I_{CC} (mA)	Packages
HOTLink Transmitter	28	CY7B923	160–330	70	J, L, S
HOTLink Receiver	28	CY7B933	160–330	130	J, L, S
Serial SONET Transceiver	24	CY7B951	51 & 155	50	S
10-Base 2/S Ethernet Coax Transceiver	16	CY7B8392	10	80	P, J
Fast Ethernet 100 Base-T4 Transceiver	80	CY7C971	10 & 100	—	N
HOTLink Evaluation Card	—	CY9266	160–330	—	C, T, F*
Integrated ATM Transceiver	100	CY7B955	51 & 155	—	N

* Interface: C–Coax; T–twisted pair; F–fiber

Timing Technology Products

Application	Part #	# of PLLs	# of Outputs	Features	Package
Motherboard Frequency Synthesizers	ICD2023	2	7	All PC clocks, 10–80 MHz, 5V	20S
	ICD2025	2	3	PC CPU & System clocks, 1.843–100MHz, 5V	16S
	ICD2027	2	6	All PC clocks, power-down, 0.76–100 MHz, 5V	20S
	ICD2028	3	8	All PC clocks, user-configurable, 0.35–100 MHz, 5V/3.3V	20S
	ICD2093	2	12	Super-Buffer: 8 skew-controlled CPU clocks, 5V	24S
	CY2254	2	14	Pentium Triton chipset compatible: 4 CPU/6 PCI buffered clocks, 3.3V	28S
	CY2255	2	14	OPTi Viper chipset compatible: 1 early/5 CPU/6 PCI buffered clocks, 3.3V	28S
	CY2257	2	14	Ali Aladdin chipset compatible: 1 early/5 CPU/6 PCI buffered clocks, 3.3V	28S
	CY2291	3	8	All PC clocks, factory EPROM programmable, 5V/3.3V	20S
PC Graphics Frequency Synthesizers	ICD2042A	2	3	PC video/memory clocks, addressable, 5V	16S
	ICD2061A	2	2	PC video/memory clocks, user-programmable, 5V	16S
	ICD2062B	2	6	PECL video clock for workstations, 0.5–165 MHz, 5V	20S
	ICD2063	2	2	PC video/memory clocks, user-programmable, 5V/3.3V	16S
General Purpose Programmable Products	ICD2051	2	5	User-programmable dual PLL, 0.3–120 MHz, 5V	16S
	ICD2053B	1	1	User-programmable single PLL, 0.4–100 MHz, 5V	8S
QuiXTAL Embedded Crystal Products	ICD6233	1	1	Metal can oscillator package, field programmable	—
Programmable Skew Clock Buffer (TTL Output)	CY7B991	1	8	3–80 MHz, Programmable Skew (700 ps increments)	J, L
Programmable Skew Clock Buffer (CMOS Output)	CY7B992	1	8	3–80 MHz, Programmable Skew (700 ps increments)	J, L

PC Chipsets

Description	Pins	Part Number	Package
Single-chip solution for 486-based systems with Green features. Supports SMI/CPU interface/cache control/ DRAM control/ISA Bus control/VESA control	160	CY82C597	N
Intelligent PCI Bus Bridge Chip. Connects ISA Bus to the PCI Bus.	160	CY82C599	N

Note: Please contact a Cypress Representative for product availability.

FCT–T Octal Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delays (ns) C Com'l	C Mil	B Com'l	B Mil	A Com'l	A Mil	Standard Com'l	Standard Mil	Package
CY29FCT52T	8-Bit Registered Transceiver	24	6.3	7.3	7.5	8.0	10.0	11.0			D, L, P, Q, SO
CY29FCT520T	Multilevel Pipeline Register	24	6.0	7.0	7.5	8.0	14.0	16.0			D, L, P, Q, SO
CY29FCT818T	Diagnostic Scan Register	24	6.0	7.6	7.5	9.0	9.0	12.0	13.0	18.0	D, L, P, Q, SO
CY54/74FCT138T	1-of-8 Decoder	16	5.0	6.0			5.8	7.8	9.0	12.0	D, L, P, Q, SO
CY54/74FCT157T	Quad 2-input Multiplexers	16	4.3	5.0			5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT158T	Quad 2-input Inverting Multiplexers	16	4.3	5.5			5.5	6.3	6.5	7.5	D, L, P, Q, SO
CY54/74FCT163T	4-Bit Binary Counter with Synchronous Reset	16	5.8	6.1			7.2	7.5	11.0	11.5	D, L, P, Q, SO
CY54/74FCT191T	4-Bit Up/Down Binary Counter	16	6.2	8.4			7.8	10.5	12.0	16.0	D, L, P, Q, SO
CY54/74FCT240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$	20	4.3	4.7			4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT244T	8-Bit Buffer/Line Driver with $\overline{OE}$	20	4.1	4.6			4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT245T	8-Bit Transceiver with $\overline{OE}$	20	4.1	4.5			4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT257T	Quad 2-input Multiplexers with $\overline{OE}$	16	4.3	5.0			5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT273T	8-Bit Register with Asynchronous Reset	20	5.8	6.5			7.2	8.3	13.0	15.0	D, L, P, Q, SO
CY54/74FCT373T	8-Bit Latch with $\overline{OE}$	20	4.2	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT374T	8-Bit Register with $\overline{OE}$	20	5.2	6.2			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT377T	8-Bit Register with Clock Enable	20	5.2	5.5			7.2	8.3	13.0	15.0	D, L, P, Q, SO
CY54/74FCT399T	Quad 2-input Registers	16	6.1	6.6			7.0	7.5	10.0	11.5	D, L, P, Q, SO
CY54/74FCT480T	Dual 8-Bit Odd-Parity Generators/ Checkers	24			5.6	7.0	7.5	9.5	13.0	17.0	D, L, P, Q, SO
CY54/74FCT540T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and Flow-Through Pinout	20	4.3	4.7			4.8	5.1	8.5	9.5	D, L, P, Q, SO
CY54/74FCT541T	8-Bit Buffer/Line Driver with $\overline{OE}$ and Flow-Through Pinout	20	4.3	4.7			4.8	5.1	8.5	9.5	D, L, P, Q, SO
CY54/74FCT543T	8-Bit Latched Transceiver with $\overline{OE}$	24	5.3	6.1			6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT573T	8-Bit Latch with $\overline{OE}$ and Flow-Through Pinout	20	4.2	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT574T	8-Bit Register with $\overline{OE}$ and Flow-Through Pinout	20	5.2	6.2			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT646T	8-Bit Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT652T	8-Bit Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT821T	10-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5			D, L, P, Q, SO
CY54/74FCT823T	9-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5			D, L, P, Q, SO
CY54/74FCT825T	8-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5			D, L, P, Q, SO
CY54/74FCT827T	10-Bit Buffer with $\overline{OE}$	24	4.4	5.0	5.0	6.5	8.0	9.0			D, L, P, Q, SO
CY54/74FCT841T	10-Bit Latch with $\overline{OE}$	24	5.5	6.3	6.5	7.5	9.0	10.0			D, L, P, Q, SO

Bus Switch

Part Number	Organization	Pins	Propagation Delays (ns) Com'l	Packages
CYBUS3384	10-Bit Bus Switch	24	0.25	D, L, P, Q, SO

Note: Please contact a Cypress Representative for product availability.

FCT2-T Octal Logic Products with Resistor (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delays (ns) C Com'l	C Mil	B Com'l	B Mil	A Com'l	A Mil	Standard Com'l	Standard Mil	Packages
CY54/74FCT2240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.3				4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2244T	8-Bit Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT2245T	8-Bit Transceiver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT2257T	Quad 2-input Multiplexers with $\overline{OE}$ and 25Ω Resistor	16	4.3				5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT2373T	8-Bit Latch with $\overline{OE}$ and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2374T	8-Bit Register with $\overline{OE}$ and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2541T	8-Bit Buffer/Line Driver with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.1	4.6			4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2543T	8-Bit Latched Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.5	6.1			6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT2573T	8-Bit Latch with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2574T	8-Bit Register with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2646T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2652T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2827T	10-Bit Buffer with $\overline{OE}$ and 25Ω Resistor	24	4.4	5.0	5.0	6.5	8.0	9.0			D, L, P, Q, SO

FCT16 16-Bit High Drive Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delays (ns) C Com'l	B Com'l	A Com'l	Standard Com'l	Package
CY74FCT16240T	16-Bit Inverting Buffer/Line Driver with $\overline{OE}$	48	4.3		4.8	8.0	PA, PV
CY74FCT16244T	16-Bit Buffer/Line Driver with $\overline{OE}$	48	4.1		4.8	6.5	PA, PV
CY74FCT16245T	16-Bit Transceiver with $\overline{OE}$	48	4.1		4.6	7.0	PA, PV
CY74FCT16373T	16-Bit Latch with $\overline{OE}$	48	4.2		5.2	8.0	PA, PV
CY74FCT16374T	16-Bit Register with $\overline{OE}$	48	5.2		6.5	10.0	PA, PV
CY74FCT16444T	16-Bit 244 with Single $\overline{OE}$	48	4.1		4.8	6.5	PA, PV
CY74FCT16445T	16-Bit 245 with Single $\overline{OE}$ and DIR	48	4.1		4.6	7.0	PA, PV
CY74FCT16500T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT16501T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT16543T	16-Bit Latched Transceiver with $\overline{OE}$	56	5.3		6.5	8.5	PA, PV
CY74FCT16646T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT16652T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT16823T	18-Bit Register with $\overline{OE}$	56	6.0	7.5	10.0		PA, PV
CY74FCT16827T	20-Bit Buffer with $\overline{OE}$	56	4.4	5.0	8.0		PA, PV
CY74FCT16841T	20-Bit Latch with $\overline{OE}$	56	5.5	6.5	9.0		PA, PV
CY74FCT16952T	16-Bit Registered Transceiver	56	6.3	7.5	10.0		PA, PV

Note: Please contact a Cypress Representative for product availability.

FCT162 16-Bit Balanced Drive Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delays (ns) C Com'l	B Com'l	A Com'l	Standard Com'l	Package
CY74FCT162240T	16-Bit Inverting Buffer/Line Driver with $\overline{OE}$	48	4.3		4.8	8.0	PA, PV
CY74FCT162244T	16-Bit Buffer/Line Driver with $\overline{OE}$	48	4.1		4.8	6.5	PA, PV
CY74FCT162245T	16-Bit Transceiver with $\overline{OE}$	48	4.1		4.6	7.0	PA, PV
CY74FCT162373T	16-Bit Latch with $\overline{OE}$	48	4.2		5.2	8.0	PA, PV
CY74FCT162374T	16-Bit Register with $\overline{OE}$	48	5.2		6.5	10.0	PA, PV
CY74FCT162500T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT162501T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT162543T	16-Bit Latched Transceiver with $\overline{OE}$	56	5.3		6.5	8.5	PA, PV
CY74FCT162646T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT162652T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT162823T	18-Bit Register with $\overline{OE}$	56	6.0	7.5	10.0		PA, PV
CY74FCT162827T	20-Bit Buffer with $\overline{OE}$	56	4.4	5.0	8.0		PA, PV
CY74FCT162841T	20-Bit Latch with $\overline{OE}$	56	5.5	6.5	9.0		PA, PV
CY74FCT162952T	16-Bit Registered Transceiver	56	6.3	7.5	10.0		PA, PV

FCT162H 16-Bit Balanced Drive, Bus Hold Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delays (ns) C Com'l	B Com'l	A Com'l	Standard Com'l	Package
CY74FCT162H244T	16-Bit Buffer/Line Driver with $\overline{OE}$ with Bus Hold	48	4.1		4.8	6.5	PA, PV
CY74FCT162H245T	16-Bit Transceiver with $\overline{OE}$ with Bus Hold	48	4.1		4.6	7.0	PA, PV
CY74FCT162H501T	18-Bit Universal Bus Transceiver with Bus Hold	56	4.6		5.1		PA, PV
CY74FCT162H952T	16-Bit Registered Transceiver with Bus Hold	56	6.3	7.5	10.0		PA, PV

Note: Please contact a Cypress Representative for product availability.

FCT2 Octal Logic Products with Resistor (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delays (ns) C Com'l	C Mil	B Com'l	B Mil	A Com'l	A Mil	Standard Com'l	Standard Mil	Packages
CY54/74FCT2240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.3				4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2244T	8-Bit Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT2245T	8-Bit Transceiver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT2257T	Quad 2-input Multiplexers with $\overline{OE}$ and 25Ω Resistor	16	4.3				5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT2373T	8-Bit Latch with $\overline{OE}$ and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2374T	8-Bit Register with $\overline{OE}$ and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2541T	8-Bit Buffer/Line Driver with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.1	4.6			4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2543T	8-Bit Latched Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.5	6.1			6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT2573T	8-Bit Latch with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2574T	8-Bit Register with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2646T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2652T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2827T	10-Bit Buffer with $\overline{OE}$ and 25Ω Resistor	24	4.4	5.0	5.0	6.5	8.0	9.0			D, L, P, Q, SO

Notes:

The above specifications are for the commercial temperature range of 0°C to 70°C. Military temperature range (−55°C to +125°C) product processed to MIL-STD-883 Revision C is also available for most products. Speed and power selections may vary from those above. Contact your local sales office for more information.

Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP, LCC, or PGA.

Power supplies for most product lines are V_{CC} = 5V ± 10%.

22S, 24S, 28S stands for 300 mil. 22-pin, 24-pin, 28-pin, respectively. 28.4 stands for 28-pin 400 mil, 24.4 stands for 24-pin 400 mil.

PLCC, SOJ, and SOIC packages are available on some products.

F, K, and T packages are special order only.
Please contact a Cypress representative for product availability.

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Package Code:

B = Plastic Pin Grid Array
D = CerDIP
E = Tape Automated Bond (TAB)
F = Flatpack
G = Pin Grid Array (PGA)
H = Windowed Hermetic LCC
J = PLCC
K = Cerpack
L = Leadless Chip Carrier (LCC)
N = Plastic Quad Flatpack
P = Plastic
Q = Windowed LCC
Q = QSOP
R = Windowed PGA
S = SOIC
T = Windowed Cerpack
U = Ceramic Quad Flatpack
V = SOJ
W = Windowed Cerdip
X = DICE
Y = Ceramic LCC
Z = TSOP
HD = Hermetic DIP (Module)
HG = Ceramic PGA (Module)
PA = TSSOP
PD = Plastic DIP (Module)
PM = Plastic SIMM
PN = Plastic Angled SIMM
PS = Plastic SIP
PV = SSOP
PZ = Plastic ZIP
SO = SOIC

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Note: Please contact a Cypress Representative for product availability.

CYPRESS	CYPRESS
2147–35C	7C147–35C
2147–45C	2147–35C
2147–45C	7C147–45C
2147–45M+	7C147–45M+
2147–55C	2147–45C
2147–55M	2147–45M
2148–35C	21L48–35C
2148–35C	7C148–35C
2148–35M	7C148–35M
2148–45C	2148–35C
2148–45C	21L48–45C
2148–45M	2148–35M
2148–45M+	7C148–45M+
2148–55C	2148–45C
2148–55C	21L48–55C
2148–55M	2148–45M
2149–35C	21L49–35C
2149–35C	7C149–35C
2149–35M	7C149–35M
2149–45C	21L49–45C
2149–45M	2149–35M
2149–45M	7C149–45M
2149–55C	2149–45C
2149–55C	21L49–55C
2149–55M	2149–45M
21L48–35C	7C148–35C
21L48–45C	21L48–35C
21L48–45C	7C148–45C
21L48–55C	21L48–45C
21L49–35C	7C149–25C
21L49–45C	21L49–35C
21L49–45C	7C149–45C
21L49–55C	21L49–45C
27S03AC	7C189–25C
27S03AM	7C189–25M
27S03C	27S03AC
27S03C	74S189C
27S03M	27S03AM
27S03M	54S189M
27S07AC	7C190–25C
27S07AM	7C190–25M
27S07C	27S07AC
27S07M	27S07AM
27S07M	7C190–25M
54S189M	27S03M
6116A–45C	6116A–35C
6116A–55C	6116A–45C
6116A–55M	6116A–45M
74S189C	27S03C
7C122–25C	7C122–15C+
7C122–35C	7C122–25C
7C122–35M	7C122–25M
7C123–12C	7C123–7C
7C128A–35C	7C128A–25C
7C128A–45C	7C128A–35C
7C128A–45M	7C128A–35M+
7C128A–55C	7C128A–45C+
7C128A–55M	7C128A–45M+
7C147–35C	7C147–25C+
7C147–45C	7C147–35C
7C148–35C	7C148–25C+
7C148–45C	7C148–35C

CYPRESS	CYPRESS
7C149–35C	7C149–25C+
7C149–45C	7C149–35C
7C149–45M	7C149–35M
7C150–25C	7C150–15C
7C150–35C	7C150–25C
7C150–35M	7C150–25M
7C167A–35C	7C167A–25C
7C167A–45M	7C167A–35M+
7C168A–35C	7C168A–25C
7C168A–45M	7C168A–35M+
7C169A–35C	7C169A–25C
7C169A–40M	7C169A–35M+
7C170A–35C	7C170A–25C
7C170A–45C	7C170A–35C
7C170A–45M	7C170A–35M
7C171A–35C	7C171A–25C
7C171A–45M	7C171A–35M+
7C172A–35C	7C172A–25C
7C172A–45M	7C172A–35M+
7C189–25C	7C189–15C+
7C190–25C	7C190–15C+
7C191–45M	7C191–35M
7C192–45M	7C192–35M
7C194–35C	7C194–25C
7C194–45C	7C194–35C+
7C194–45M	7C194–35M
7C196–35C	7C196–25C
7C196–45C	7C196–35C+
7C197–35C	7C197–25C
7C197–45C	7C197–35C+
7C197–45M	7C197–35M
7C198–45C	7C198–35C
7C198–55C	7C198–45C+
7C198–55M	7C198–45M
7C199–45C	7C199–35C
7C199–55C	7C199–45C+
7C199–55M	7C199–45M
7C225	7C225A
7C235	7C235A
7C245	7C245A
7C271	7C271A
7C274	27H256
7C281	7C281A
7C286	27H512
7C291	7C291A
7C292	7C292A
9122–25C	7C122–15C
9122–25C	91L22–25C
9122–35C	9122–25C
9122–35C	91L22–35C
9122–45C	93L422C
91L22–25C	7C122–25C
91L22–35C	7C122–35C
91L22–45C	93L422AC
93422AC	7C122–35C
93422AC	9122–35C
93422AM	7C122–35M
93422C	93L422AC
93422M	93422AM
93422M	93L422AM
93L422AC	7C122–35C
93L422AC	91L22–45C

CYPRESS	CYPRESS
93L422AM	7C122–35M
93L422C	93L422AC
93L422M	93L422AM
PALC16L8–25C	PALC16L8L–25C
PALC16L8–30M	PALC16L8–20M
PALC16L8–35C	PALC16L8–25C
PALC16L8–40M	PALC16L8–30M
PALC16L8L–35C	PALC16L8L–25C
PALC16R4–25C	PALC16R4L–25C
PALC16R4–30M	PALC16R4–20M
PALC16R4–35C	PALC16R4–25C
PALC16R4–40M	PALC16R4–30M
PALC16R4L–35C	PALC16R4L–25C
PALC16R6–25C	PALC16R6L–25C
PALC16R6–30M	PALC16R6–20M
PALC16R6–35C	PALC16R6–25C
PALC16R6–40M	PALC16R6–30M
PALC16R6L–35C	PALC16R6L–25C
PALC16R8–25C	PALC16R8L–25C
PALC16R8–30M	PALC16R8–20M
PALC16R8–35C	PALC16R8–25C
PALC16R8–40M	PALC16R8–30M
PALC16R8L–35C	PALC16R8L–25C
PALC22V10–35C	PALC22V10–25C
PALC22V10–40M	PALC22V10–30M
PALC22V10L–25C	PALC22V10–25C
PALC22V10L–35C	PALC22V10L–25C
PLDC20G10–35C	PLDC20G10–25C
PLDC20G10–40M	PLDC20G10–30M

ALTERA	CYPRESS
PREFIX EPM	PREFIX: CY
PREFIX: EP	PREFIX: PALC
22V10–10C	PALC22V10D–7C
22V10–10C	PALC22V10D–10C
22V10–10C	PAL22V10C–7C+
22V10–10C	PAL22V10C–10C+
22V10–15C	PALC22V10B–15C
22V10–15C	PALC22V10D–15C
5032DC	7C344–25WC
5032DC–2	7C344–20WC
5032DC–15	7C344–15WC
5032DC–17	Call Factory
5032DC–20	7C344–20WC
5032DC–25	7C344–25WC
5032DM	7C344–25WMB
5032DM–25	7C344–25WMB
5032JC	7C344–25HC
5032JC–2	7C344–20HC
5032JC–15	7C344–15HC
5032JC–17	Call Factory
5032JC–20	7C344–20HC
5032JC–25	7C344–25HC
5032JI–20	7C344–20HI
5032JM	7C344–25HMB
5032JM–25	7C344–25HMB
5032LC	7C344–25JC
5032LC–2	7C344–20JC
5032LC–15	7C344–15JC
5032LC–17	Call Factory
5032LC–20	7C344–20JC
5032LC–25	7C344–25JC
5032PC	7C344–25PC

ALTERA	CYPRESS
5032PC-2	7C344-20PC
5032PC-15	7C344-15PC
5032PC-17	Call Factory
5032PC-20	7C344-20PC
5032PC-25	7C344-25PC
5064JC	7C343-35HC
5064JC-1	7C343-25HC
5064JC-2	7C343-30HC
5064JI	7C343-35HI
5064JM	7C343-35HMB
5064LC	7C343-35JC
5064LC-1	7C343-25JC
5064LC-2	7C343-30JC
5128AGC-12	7C342B-12RC
5128AGC-15	7C342B-15RC
5128AGC-20	7C342B-20RC
5128AJC-12	7C342B-12HC
5128AJC-15	7C342B-15HC
5128AJC-20	7C342B-20HC
5128ALC-12	7C342B-12JC
5128ALC-15	7C342B-15JC
5128ALC-20	7C342B-20JC
5128GC	7C342-35RC
5128GC-1	7C342-25RC
5128GC-2	7C342-30RC
5128GM	7C342-35RMB
5128JC	7C342-35HC
5128JC-1	7C342-25HC
5128JC-2	7C342-30HC
5128JI	7C342-35HI
5128JI-2	7C342-30HI
5128JM	7C342-35HMB
5128LC	7C342-35JC
5128LC-1	7C342-25JC
5128LC-2	7C342-30JC
5128LI	7C342-35JI
5128LI-2	7C342-30HI
5130GC	7C346-35RC
5130GC-1	7C346-25RC
5130GC-2	7C346-30RC
5130GM	7C346-35RM
5130JC	7C346-35HC
5130JC-1	7C346-25HC
5130JC-2	7C346-30HC
5130JM	7C346-35HM
5130LC	7C346-35JC
5130LC-1	7C346-25JC
5130LC-2	7C346-30JC
5130LI	7C346-35JI
5130LI-2	7C346-30JI
5130QC	7C346-35NC
5130QC-1	7C346-25NC
5130QC-2	7C346-30NC
5130QI	7C346-35NI
5192AGC-15	7C341B-15RC
5192AGC-20	7C341B-20RC
5192AJC-15	7C341B-15HC
5192AJC-20	7C341B-20HC
5192ALC-1	7C341B-15JC
5192ALC-2	7C341B-20JC
5192GC	7C341-35RC
5192GC-1	7C341-25RC

ALTERA	CYPRESS
5192GC-2	7C341-30RC
5192JC	7C341-35HC
5192JC-1	7C341-25HC
5192JC-2	7C341-30HC
5192JI	7C341-35HI
5192LC	7C341-35JC
5192LC-1	7C341-25JC
5192LC-2	7C341-30JC

AMD	CYPRESS
PREFIX: Am	PREFIX: CY
PREFIX: SN	PREFIX: CY
SUFFIX: B	SUFFIX: B
SUFFIX: D	SUFFIX: W
SUFFIX: E	SUFFIX: Z
SUFFIX: F	SUFFIX: F
SUFFIX: J	SUFFIX: J
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
27C64-55C	7C266-55C
27C64-70C	27C64-70C
27C64-90C	27C64-90C
27C64-120C	27C64-120C
27C64-150C	27C64-150C
27C64-200C	27C64-200C
27C010-90C	27C010-90C
27C010-120C	27C010-120C
27C010-150C	27C010-150C
27C010-200C	27C010-200C
27C128-45C	27C128-45C
27C128-55C	27C128-55C
27C128-70C	27C128-70C
27C128-90C	27C128-90C+
27C128-120C	27C128-120C+
27C128-150C	27C128-150C+
27C128-200C	27C128-200C+
27C256-55C	27C256-55C
27C256-70C	27C256-70C+
27C256-90C	27C256-90C+
27C256-120C	27C256-120C+
27C256-150C	27C256-150C+
27C256-200C	27C256-200C+
27C512-75C	27H512-70C
27C512-90C	27H512-90C
27C512-120C	27H512-120C
27C512-150C	27H512-150C
27C512-200C	27H512-200C
27H010-45	27H010-45
27H010-55	27H010-55
27H010-70	27C010-70
27H010-90	27C010-90
27H256-35C	27H256-35C
27H256-45C	27C256-45C
27H256-45M	27C256-45M
27H256-55C	27C256-55C
27H256-55M	27C256-55M
27H256-70C	27C256-70C
27LS291M	7C291A-35M
27PS191AC	7C292A-50C
27PS191AM	7C292A-50M+
27PS191C	7C292A-50C
27PS191M	7C292A-50M+
27PS291AC	7C293A-50C

AMD	CYPRESS
27PS291AM	7C293A-50M+
27PS291C	7C293A-50C
27PS291M	7C293A-50M+
27S181AC	7C282A-30C
27S181AM	7C282A-45M
27S181C	7C282A-45C
27S181M	7C282A-45M
27S191AC	7C292A-35C
27S191AM	7C292A-50M
27S191C	7C292A-50C
27S191M	7C292A-50M
27S191SAC	7C292A-25C
27S191SAM	7C292A-30M
27S25AC	7C225A-30C
27S25AM	7C225A-35M
27S25C	7C225A-40C
27S25M	7C225A-40M
27S25SAC	7C225A-25C
27S25SAM	7C225A-30M
27S43AC	7C244-45C
27S43C	7C244-55C
27S281AC	7C281A-30C
27S281AM	7C281A-45M
27S281C	7C281A-45C
27S281M	7C281A-45M
27S291AC	7C291A-35C
27S291AM	7C291A-50M
27S291C	7C291A-50C
27S291M	7C291A-50M
27S291SAC	7C291A-25C
27S291SAM	7C291A-30M
27S35AC	7C235A-30C
27S35AM	7C235A-40M
27S35C	7C235A-40C
27S35M	7C235A-40M
27S45AC	7C245A-35C
27S45AM	7C245A-45M
27S45C	7C245A-45C
27S45M	7C245A-45M
27S45SAC	7C245A-25C
27S45SAM	7C245A-25M-
27S49A	7C264-40C
27S49AM	7C264-55M
27S49C	7C264-55C
27S49M	7C264-55M
27S49SAC	7C264-25C
27S49SAM	7C264-25M
2841AC	3341C
2841AM	3341M
2841C	3341C
2841M	3341M
7201-25	7C420-25
7201-25R	7C421-25
7201-35	7C420-30
7201-35R	7C421-30
7201-50	7C420-40
7201-50R	7C421-40
7201-65	7C420-65
7201-65R	7C421-65
7201-80	7C420-65
7201-80R	7C421-65
7202A-15	7C425A-15

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

AMD	CYPRESS
7202A-25	7C424-25
7202A-25R	7C425-25
7202A-35	7C424-30
7202A-35R	7C425-30
7202A-50	7C424-40
7202A-50R	7C425-40
7202A-65	7C424-65
7202A-65R	7C425-65
7202A-80	7C424-65
7202A-80R	7C425-65
7203A-15	7C429A-15
7203A-25	7C428-25
7203A-25R	7C429-25
7203A-35	7C428-30
7203A-35R	7C429-30
7203A-50	7C428-40
7203A-50R	7C429-40
7203A-65	7C428-65
7203A-65R	7C429-65
7203A-80	7C428-65
7203A-80R	7C429-65
7204A-15	7C433A-15
7204A-25	7C432-25
7204A-35	7C432-30
7204A-50	7C432-40
7204A-65	7C432-65
7204A-80	7C432-65
7205A-15	7C460-15
7205A-25	7C460-25
74S189C	74S189C
MACH110-12JC	7C371-83JC
MACH110-15JC	7C371-66JC
MACH110-20JC	7C371-66JC
MACH110-20/BXA	7C371-66YMB
MACH130-15JC	7C373-83JC
MACH130-20JC	7C373-66JC
MACH130-20/BXA	7C373-66YMB
MACH210-12JC	7C372-100JC
MACH210-15JC	7C372-83JC
MACH210-20JC	7C372-66JC
MACH210-20/BXA	7C372-66YMB
MACH210A-10JC	7C372-125JC
MACH210A-12JC	7C372-100JC
MACH230-15JC	7C374-83JC
MACH230-20JC	7C374-66JC
MACH435-15JC	7C374-83JC
MACH435-20JC	7C374-66JC
PAL16L8-4C	PAL16L8-4C
PAL16L8-5C	PAL16L8-5C
PAL16L8-7C	PAL16L8-7C
PAL16L8-10/B	PAL16L8-10M
PAL16L8-12/B	PAL16L8-10M
PAL16L8-D/2	PAL16L8-7C
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8ALC	PALC16L8-25C
PAL16L8ALM	PALC16L8-30M
PAL16L8AM	PALC16L8-30M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8LC	PALC16L8-35C

AMD	CYPRESS
PAL16L8LM	PALC16L8-40M
PAL16L8M	PALC16L8-40M
PAL16L8QC	PALC16L8L-35C
PAL16L8QM	PALC16L8-40M
PAL16R4-4C	PAL16R4-4C
PAL16R4-5C	PAL16R4-5C
PAL16R4-7C	PAL16R4-7C
PAL16R4-10/B	PAL16R4-10M
PAL16R4-12/B	PAL16R4-10M
PAL16R4-D/2	PAL16R4-7C
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M
PAL16R4ALC	PALC16R4-25C
PAL16R4ALM	PALC16R4-30M
PAL16R4AM	PALC16R4-30M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4LC	PALC16R4-35C
PAL16R4LM	PALC16R4-40M
PAL16R4M	PALC16R4-40M
PAL16R4QC	PALC16R4L-35C
PAL16R4QM	PALC16R4-40M
PAL16R6-4C	PAL16R6-4C
PAL16R6-5C	PAL16R6-5C
PAL16R6-7C	PAL16R6-7C
PAL16R6-10/B	PAL16R6-10M
PAL16R6-12/B	PAL16R6-10M
PAL16R6-D/2	PAL16R6-7C
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6ALC	PALC16R6-25C
PAL16R6ALM	PALC16R6-30M
PAL16R6AM	PALC16R6-30M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6LC	PALC16R6-35C
PAL16R6LM	PALC16R6-40M
PAL16R6M	PALC16R6-40M
PAL16R6QC	PALC16R6L-35C
PAL16R6QM	PALC16R6-40M
PAL16R8-4C	PAL16R8-4C
PAL16R8-5C	PAL16R8-5C
PAL16R8-7C	PAL16R8-7C
PAL16R8-10/B	PAL16R8-10M
PAL16R8-12/B	PAL16R8-10M
PAL16R8-D/2	PAL16R8-7C
PAL16R8A-4C	PALC16R8L-35
PAL16R8A-4M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8ALC	PALC16R8-25C
PAL16R8ALM	PALC16R8-30M
PAL16R8AM	PALC16R8-30M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8LC	PALC16R8-35C
PAL16R8LM	PALC16R8-40M
PAL16R8M	PALC16R8-40M
PAL16R8QC	PALC16R8L-35
PAL16R8QM	PALC16R8-40M
PAL22V10-7JC	PALC22V10D-7JC
PAL22V10-7PC	PALC22V10D-7PC

AMD	CYPRESS
PAL22V10-10DC	PALC22V10D-10DC
PAL22V10-10JC	PALC22V10D-10JC
PAL22V10-10PC	PALC22V10D-10PC
PAL22V10-12/B3A	PALC22V10B-10LMB
PAL22V10-12/BLA	PALC22V10B-10DMB
PAL22V10-15DC	PALC22V10B-15DC
PAL22V10-15JC	PALC22V10B-15JC
PAL22V10-15PC	PALC22V10B-15PC
PAL22V10-20/B3A	PALC22V10B-20LM
PAL22V10-20/BLA	PALC22V10B-20DM
PAL22V10/B3A	PALC22V10-35LMB
PAL22V10/BLA	PALC22V10-35DMB
PAL22V10A/B3A	PALC22V10-25LMB
PAL22V10A/BLA	PALC22V10-25DMB
PAL22V10ADC	PALC22V10-25DC
PAL22V10AJC	PALC22V10-25JC
PAL22V10APC	PALC22V10-25PC
PAL22V10DC	PALC22V10-35DC
PAL22V10JC	PALC22V10-35JC
PAL22V10PC	PALC22V10-35PC
PALCE16V8H-5JC/4	PALCE16V8-5JC
PALCE16V8H-7JC/4	PALCE16V8-7JC
PALCE16V8H-7PC/4	PALCE16V8-7PC
PALCE16V8H-10JC/4	PALCE16V8-10JC
PALCE16V8H-10PC/4	PALCE16V8-10PC
PALCE16V8H-15JC/4	PALCE16V8-15JC
PALCE16V8H-15PC/4	PALCE16V8-15PC
PALCE16V8H-25JC/4	PALCE16V8-25JC
PALCE16V8H-25PC/4	PALCE16V8-25PC
PALCE16V8Q-15JC/4	PALCE16V8L-15JC
PALCE16V8Q-15PC/4	PALCE16V8L-15PC
PALCE16V8Q-25JC/4	PALCE16V8L-25JC
PALCE16V8Q-25PC/4	PALCE16V8L-25PC
PALCE22V10H-7JC	PALC22V10D-10JC
PALCE22V10H-10PC	PALC22V10D-7PC
PALCE22V10H-10JC	PALC22V10D-10JC
PALCE22V10H-10PC	PALC22V10D-10P
PALCE22V10H-15/B3A	PALC22V10D-15LMB
PALCE22V10H-15/BLA	PALC22V10D-15DMB
PALCE22V10H-15JC	PALC22V10D-15JC
PALCE22V10H-15PC	PALC22V10D-15PC
PALCE22V10H-20/B3A	PALC22V10D-20LMB
PALCE22V10H-20/BLA	PALC22V10D-20DMB
PALCE22V10H-25/B3A	PALC22V10D-25LMB
PALCE22V10H-25/BLA	PALC22V10D-25DMB
PALCE22V10H-25JC	PALC22V10D-25JC
PALCE22V10H-25PC	PALC22V10D-25PC
PALCE22V10H-30/B3A	PALC22V10D-25LMB
PALCE22V10H-30/BLA	PALC22V10D-25DMB

Product Line Cross Reference

ANALOG DEV	CYPRESS
PREFIX: ADSP	PREFIX: CY
SUFFIX: 883B	SUFFIX: B
SUFFIX: D	SUFFIX: D
SUFFIX: E	SUFFIX: L
SUFFIX: F	SUFFIX: F
SUFFIX: G	SUFFIX: G

ATMEL	CYPRESS
PREFIX: AT	PREFIX: CY
SUFFIX: D	SUFFIX: W
SUFFIX: K	SUFFIX: H
SUFFIX: L	SUFFIX: Q
SUFFIX: J	SUFFIX: J
SUFFIX: P	SUFFIX: P
SUFFIX: T	SUFFIX: Z
22V10	PALC22V10
22V10–15	PALC22V10B
27C010–45C	27H010–45C
27C010–55C	27H010–55C
27C010–70C	27C010–50C
27C010–90C	27C010–90C
27C010–120C	27C010–120C
27C010–150C	27C010–150C
27C010–200C	27C010–200C
27C512–70C	27H512–70C
27C512–90C	27C512–90C
27C512–120C	27C512–120C
27C512–150C	27C512–150C
27C512–200C	27C512–200C
27C256R–70C	27C256–70C
27C256R–90C	27C256–90C+
27C256R–120C	27C256–120C+
27C256R–150C	27C256–150C+
27C256R–200C	27C256–200C+
27HC256R–35C	27C256–35C
27HC256R–45C	27C256–45C
27HC256R–55C	27C256–55C
27HC256R–70C	27C256–70C
27HC256R–70M	27C256–70M
27HC641–35C	7C264–35C
27HC641–45C	7C264–45C
27HC641–45M	7C264–45M
27HC641–55C	7C264–55C
27HC641–55M	7C264–55M
27HC641–70C	7C264–70C
27HC642–35C	7C261–35C
27HC642–45C	7C261–45C
27HC642–45M	7C261–45M
27HC642–55C	7C261–55C
27HC642–55M	7C261–55M
27HC642–70C	7C261–55C

AUSTIN SEMICONDUCTOR	CYPRESS
PREFIX: MT	PREFIX: CY
5C1608–25M	7C128A–25M
5C1608–30M	7C128A–25M
5C1608–35M	7C128A–35M
5C2561–25M	7C197–25MB
5C2561–35M	7C197–35MB
5C2561–45M	7C197–45MB
5C2564–25M	7C194–25MB
5C2564–35M	7C194–35MB

AUSTIN SEMICONDUCTOR	CYPRESS
5C2564–45M	7C194–45MB
5C2568–25M	7C199–25MB
5C2568–35M	7C199–35MB
5C2568–45B	7C199–45MB
5C2568CW–25M	7C198–25MB
5C2568CW–35M	7C198–35MB
5C2568CW–45B	7C198–45MB
5C2568W–25M	7C198–25MB
5C2568W–35M	7C198–35MB
5C2568W–45B	7C198–45MB
5C6401–20M	7C187A–20MB
5C6401–25M	7C187A–25MB
5C6401–30M	7C187A–25MB
5C6401–35M	7C187A–35MB
5C6404–20M	7C164A–20MB
5C6404–25M	7C164A–25MB
5C6404–30M	7C164A–25MB
5C6404–35M	7C164A–35MB
5C6408–20M	7C185A–20MB
5C6408–25M	7C185A–25M
5C6408–30M	7C185A–25MB
5C6408–35M	7C185A–35MB

CATALYST	CYPRESS
PREFIX: CAT	PREFIX: CY
27HC256–55L	27C256–55C+
27HC256–70L	27C256–70C+
27HC256–90L	27C256–70C+
27HC256–120L	27C256–120C+
27HC256L/LI–55	27C256–55C/I
27HC256L/LI–70	27C256–70C/I

DALLAS	CYPRESS
PREFIX: DS	PREFIX: CY
2009	7C421–25C
2010	7C425–25C
2011	7C429–25C

DENSEPAK	CYPRESS
PREFIX: DPS	PREFIX: CYM
6432–45C	1830HD–45C
6432–55C	1830HD–55C

EDI	CYPRESS
PREFIX: ED	PREFIX: CYM
8464C–45	7C194–45
8F32256C	1841PZ
8F3264C	1831PZ
8F8512CXXBC	1465PC–XXC
8F8512LPXXB6C	1465LPD–XXC
8F8512PXXB6C	1465LPD–XXC
8M3264CXXC6B	M1830HD–XXMB
8M3264CXXC6C	M1830HD–XXC
8M32256CXXC6B	M1840HD–XXMB
8M32256CXXC6B	M1840HD–XXC
8M8512CXXM6C	1464PD–XXC

FUJITSU	CYPRESS
PREFIX: MB	PREFIX: CY
PREFIX: MBM	PREFIX: CY
SUFFIX: F	SUFFIX: F
SUFFIX: M	SUFFIX: P
SUFFIX: Z	SUFFIX: D

FUJITSU	CYPRESS
2147H–35	2147–35C
2147H–45	2147–45C
2149–45	2149–45C
27C128–170C	27C128–150C+
27C128–200C	27C128–200C+
27C128–250C	27C128–200C+
27C256A–150C	27C256–150C+
27C256A–170C	27C256–150C+
27C256A–200C	27C256–200C+
7132E	7C282A–45C
7132E–SK	7C281A–45C
7132E–W	7C282A–45M
7132H	7C282A–45C
7132H–SK	7C281A–45C
7132L–70	7C281/2A–45C
7132Y	7C282A–30C
7132Y–SK	7C281A–30C
7138E–55	7C291/2A–50C
7138E–W	7C291/2A–50M
7138H–45	7C291/2A–35C
7138Y–35	7C291/2A–35C
7144E	7C264–55C
7144E–W	7C264–55M
7144H	7C264–55C
71A38–25	7C291/2A–25C
71A38–35	7C291/2A–35C
71C44–35	7C264–35C
71C44–45	7C264–45C
71C46–45	7C254–45C
7226RA/S–25	7C225A–25C
7232RA–25	7C235A–25C
7238RA–20	7C245A–18C
7238RA–20–W	7C245A–18M
7238RA–25	7C245A–25C
7238RA–25–W	7C245A–25M
8128–10	7C128A–55C
8128–15	7C128A–55C
8167–70W	7C167A–45M
8167A–55	7C167A–45C
8167A–70	7C167A–45C
8168–55	7C168A–45C
8171–55	7C187–45C
8171–70	7C187–45C
81C67–35	7C167A–35C
81C67–45	7C167A–45C
81C67–55W	7C167A–45M
81C68–45	7C168A–45C
81C68–55W	7C168A–45M+
81C71–45	7C187–45C
81C71–55	7C187–45C
81C74–25	7C164–25C
81C74–35	7C164–35C+
81C74–45	7C164–45C
81C75–25	7C166–25C
81C75–35	7C166–35C
81C78–45	7C186–45C
81C78–55	7C186–55C
81C81A–35	7C197–35
81C81A–45	7C197–45
81C84A–35	7C194–35
81C84A–45	7C194–45
81C86–70	7C192–45C+

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

FUJITSU	CYPRESS
8287−35	7C199−35
8287−45	7C199−45
8299	7C188
8464L−70	7C185−45C+
8464L−100	7C185−55C+

HARRIS	CYPRESS
PREFIX: HM	PREFIX: CY
PREFIX: HPL	PREFIX: CY
SUFFIX: 8	SUFFIX: B
PREFIX: 1	SUFFIX: D
PREFIX: 9	SUFFIX: F
PREFIX: 4	SUFFIX: L
PREFIX: 3	SUFFIX: P
16LC8−5	PALC16L8L−35C
16LC8−8	PALC16L8−40M
16LC8−9	PALC16L8−40M
16RC4−5	PALC16R4L−35C
16RC4−8	PALC16R4−40M
16RC4−9	PALC16R4−40M
16RC6−5	PALC16R6L−35C
16RC6−8	PALC16R6−40M
16RC6−9	PALC16R6−40M
16RC8−5	PALC16R8L−35C
16RC8−8	PALC16R8−40M
16RC8−9	PALC16R8−40M
6−7681−5	7C281A−45C
6−7681A−5	7C281A−45C
6−76161−2	7C291A−50M
6−76161−5	7C291A−50C
6−76161A−2	7C291A−50M
6−76161A−5	7C291A−50C
6−76161B−5	7C291A−35C
76641−2	7C264−55M
76641−5	7C264−55C
76641A−5	7C264−45C
7681−2	7C282A−45M
7681−5	7C282A−45C
7681A−5	7C282A−45C
76161−2	7C292A−50M
76161A−2	7C292A−50M
76161A−5	7C292A−50C
76161B−5	7C292A−35C

HITACHI	CYPRESS
PREFIX: HM	PREFIX: CY
PREFIX: HN	PREFIX: CY
PREFIX: HN48	PREFIX: CY
SUFFIX: CG	SUFFIX: L
SUFFIX: G	SUFFIX: D
SUFFIX: P	SUFFIX: P
25089	7C282−45C
25089S	7C282−45C
25169S	7C292−50C
27128G−25C	27128−200C+
27256G−15	27C256−150C+
27256G−17	27C256−150C+
27256G−20	27C256−200C+
4847	2147−55C
4847−2	2147−45C
4847−3	2147−55C
6116ALS−12	6116A−55C*
6116AS−12	6116A−55C+

HITACHI	CYPRESS
6147	7C147−45C*
6147−3	7C147−45C*
6147H−35	7C147−35C+
6147H−45	7C147−45C+
6147H−55	7C147−45C+
6147HL−35	7C147−35C*
6147HL−45	7C147−45C*
6148	7C148−45C
6148H−35	21L48−35C
6148H−45	7C148−45C+
6148H−55	7C14845C+
6148HL−35	21L48−35C*
6148HL−45	7C148−45C*
6148L	7C148−45C*
6167−6	7C167A−45C+
6167−8	7C167A−45C+
6167H−55	7C167A−45C
6167H−70	7C167A−45C
6167L−6	7C167A−45C*
6167L−8	7C167A−45C*
6168H−45	7C168A−45C+
6168HL−45	7C168A−45C*
6207P−35	7C197−35
6207P−45	7C197−45
6208P−35	7C194−35
6208P−45	7C194−45
62256	7C198*
6267−35	7C167A−35C+
6267−45	7C167A−45C
6268−25	7C168A−25C
6268−35	7C168A−35C
62832H	7C199+
62832	7C199
6288−35	7C164−35C
62932	7C188
6707−20	7C197−20C
6707−25	7C197−25C
6707A−15	7C197−15C
6707A−20	7C197−20C
6707A−25	7C197−25C
6708−20	7C194−20C
6708−25	7C194−25C
6708A−15	7C194−15C
6708A−20	7C194−20C
6708A−25	7C194−25C
6709−20	7C195−20C
6709−25	7C195−25C
6709A−15	7C195−15C
6709A−20	7C195−20C
6709A−25	7C195−25C
6716−25	7C128A−25C
6716−30	7C128A−25C
6787−30	7C187−25C
6788−25	7C164−25C
6788−30	7C164−25C

ICT	CYPRESS
27CX256−35C	27H256−35C
27CX256−45C	CY27C256−45C
27CX256−55C	CY27C256−55C

IDT	CYPRESS
PREFIX: IDT	PREFIX: CY
PREFIX: IDT	PREFIX: CYM
SUFFIX: B	SUFFIX: B
SUFFIX: D	SUFFIX: D
SUFFIX: F	SUFFIX: F
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
39C01CB	7C901−32M+
39C01CC	2901CC+
39C01CM	2901CM+
39C01DB	7C901−27M+
39C01DC	7C901−23C+
39C09A	7C909−40C+
39C09AB	7C909−40M+
39C10B	7C910−50C−
39C10BB	7C910−51M
39C11A	7C911−40C+
39C11AB	7C911−40M+
6116SA25	7C128A−25C
6116SA35	7C128A−35C
6116SA35	6116A−35C
6116SA35B	7C128A−35MB
6116SA35B	6116A−35MB
6116SA45	7C128A−45C
6116SA45	6116A−45C
6116SA45B	7C128A−45MB
6116SA45B	6116A−45MB
6116SA55B	7C128A−55MB
6116SA55B	6116A−55MB
61298SA15	7C196−15
61298SA25	7C196−25C
61298SA25B	7C196−25MB
61298SA35	7C196−35C
61298SA35B	7C196−35MB
61298SA45	7C196−45C
61298SA45B	7C196−45MB
6167SA15	7C167A−15C
6167SA20	7C167A−20C
6167SA20B	7C167A−20B
6167SA25	7C167A−25C
6167SA25B	7C167A−25M
6167SA35	7C167A−35C
6167SA35B	7C167A−35MB
6167SA45B	7C167A−45MB
6168SA15	7C168A−15C
6168SA20	7C168A−20C
6168SA20B	7C168A−20B
6168SA25	7C168A−25C
6168SA25B	7C168A−25MB
6168SA35	7C168A−35C
6168SA35B	7C168A−35MB
6168SA45B	7C168A−45MB
6197SA15	7C170A−15C
6197SA15	7C170A−20C
6197SA25	7C170A−25C
6197SA35	7C170A−35C
6197SA35B	7C170A−35MB
6197SA45B	7C170A−45MB
6197SA55	7C170A−45C
6197SA55B	7C170A−45MB
6198SA15	7C166−15C
6198SA20	7C166−20C

IDT	CYPRESS
6198SA20B	7C166–A20MB
6198SA25	7C166–25C
6198SA25B	7C166–A25MB
6198SA30B	7C166A–25MB
61B298S12	7C195–12C
61B298S15	7C195–15C
61B298S20	7C195–20C
61B298S15B	7C195–15MB
61B298S20B	7C195–20MB
7005S35	7B144–25C
7005S35	7B144–35C
7005S45B	7B144–35MB
7006S25	7006S25C
7006S35	7006S35C
7015S25	7C145–25C
7015S35	7C145–35C
7016S25	7C016–25C
7016S35	7C016–35C
7024S25	7C024–25C
7024S35	7C024–35C
7025S25	7C025–25C
7025S35	7C025–35C
7133S25	7C133–25C
7133S35	7C133–35C
7143S25	7C143–25C
7143S35	7C143–35C
71V256–15	7C1399–15C
71V256–20	7C1399–20C
71V256–25	7C1399–25C
71024–15	7C109A–15C
71024–20	7C109A–20C
71024–20	7C109–20C
71024–25	7C109–25C
71028–15	7C106A–15C
71028–20	7C106A–20C
71028–25	7C106A–25C
71256SA15	7C199–15C
71256SA20	7C199–20C
71256SA20B	7C199–20MB
71256SA25	7C198–25C
71256SA30	7C198–25C
71256SA30B	7C198–25MB
71256SA35	7C198–35C
71256SA35B	7C198–35MB
71256SA45	7C198–45C
71256SA45B	7C198–45MB
71257SA25	7C197–25C
71257SA25B	7C197–25MB
71257SA35	7C197–35C
71257SA35B	7C197–35MB
71257SA45	7C197–45C
71257SA45B	7C197–45MB
71257SA55	7C197–45C
71258SA25	7C194–25C
71258SA25B	7C194–25MB
71258SA35	7C194–35C
71258SA35B	7C194–35MB
71258SA45	7C194–45C
71258SA45B	7C194–45MB
71281SA25	7C191–25C
71281SA25B	7C191–25MB
71281SA35	7C191–35C

IDT	CYPRESS
71281SA35B	7C191–35MB
71281SA45	7C191–45C
71281SA45B	7C191–45MB
71282SA25	7C192–25C
71282SA25B	7C192–25MB
71282SA35	7C192–35C
71282SA35B	7C192–35MB
71282SA45	7C192–45C
7130LA25	7C130–25C
7130LA25J	7C131–25JC
7130LA30	7C130–30C
7130LA30J	7C131–30JC
7130LA35	7C130–35C
7130LA35B	7C130–35MB
7130LA35J	7C131–35JC
7130LA35LB	7C130–35LMB
7130LA45	7C130–45C
7130LA45B	7C131–45MB
7130LA45J	7C131–45JC
7130LA45LB	7C130–45LMB
7130LA55	7C130–55C
7130LA55B	7C131–55MB
7130LA55J	7C131–55JC
7130LA55L52B	7C130–55LMB
7130LA70	7C130–55C
7130LA70B	7C131–55MB
7130LA70J	7C131–55JC
7130LA70LB	7C130–55LMB
7130LA90LB	7C131–55LMB
7130SA25	7C130–25C
7130SA25J	7C131–25JC
7130SA30	7C130–25C
7130SA30J	7C131–30JC
7130SA35	7C130–35C
7130SA35B	7C130–35MB
7130SA35J	7C131–35JC
7130SA35LB	7C131–35LMB
7130SA45	7C130–45C
7130SA45B	7C130–45MB
7130SA45J	7C131–45JC
7130SA45LB	7C131–45LMB
7130SA55	7C130–55C
7130SA55B	7C130–55M
7130SA55J	7C131–55JC
7130SA55LB	7C131–55LMB
7130SA70	7C130–55C
7130SA70B	7C130–55MB
7130SA70J	7C131–55JC
7130SA70LB	7C131–55LMB
7130SA90	7C130–55C
7130SA90B	7C130–55MB
7130SA90J	7C131–55JC
7130SA90LB	7C131–55LMB
7130SA100	7C130–55C
7130SA100B	7C130–55MB
7130SA100LB	7C131–55LMB
71321LA25	7C136–25C
71321LA30	7C136–30C
71321LA35	7C136–35C
71321LA35B	7C136–35MB
71321LA45	7C136–45C
71321LA45B	7C136–45MB

IDT	CYPRESS
71321LA55	7C136–55C
71321LA55B	7C136–55MB
71321LA70	7C136–55C
71321LA70B	7C136–55MB
71321LA90	7C136–55C
71321LA90B	7C136–55MB
71321SA25	7C136–25C
71321SA30	7C136–30C
71321SA35	7C136–35C
71321SA35B	7C136–35MB
71321SA45	7C136–45C
71321SA45B	7C136–45MB
71321SA55	7C136–55C
71321SA55B	7C136–55MB
71321SA70	7C136–55C
71321SA70B	7C136–55MB
71321SA90	7C136–55C
71321SA90B	7C136–55MB
713256–20	7C1399–20C
713256–25	7C1399–25C
7132LA25	7C132–25C
7132LA30	7C132–30C
7132LA35	7C132–35C
7132LA35B	7C132–35MB
7132LA45	7C132–45C
7132LA45B	7C132–45MB
7132LA55	7C132–55C*
7132LA55B	7C132–55MB
7132LA70	7C132–55C*
7132LA70B	7C132–55M*
7132LA90	7C132–55C*
7132LA90B	7C132–55M*
7132LA100	7C132–55C*
7132LA100B	7C132–55M*
7132LA120B	7C132–55M*
7132SA25	7C132–25C
7132SA30	7C132–30C
7132SA35	7C132–35C
7132SA35B	7C132–35MB
7132SA45	7C132–45C
7132SA45B	7C132–45MB
7132SA55	7C132–55C+
7132SA55B	7C132–55MB
7132SA70	7C132–55C+
7132SA70B	7C132–55M+
7132SA90	7C132–55C+
7132SA90B	7C132–55M+
7132SA100	7C132–55C+
7132SA100B	7C132–55M+
7132SA120B	7C132–55M+
71342S35	7C1342–25C
71342S35	7C1342–35C
71342S45B	7C1342–35MB
7134S35	7B134–25C
7134S35	7B134–35C
7134S35J52	7B135–25JC
7134S35J52	7B135–35JC
7134S35L52	7B135–25LC
7134S35L52	7B135–35LC
7134S45B	7B134–35MB
7134S45L52B	7B135–35LMB
7140LA25	7C140–25C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

IDT	CYPRESS
7140LA25J	7C141–25JC
7140LA30	7C140–30C
7140LA30J	7C141–30JC
7140LA30L52	7C141–30LC
7140LA35	7C140–35C
7140LA35B	7C140–35MB
7140LA35J	7C141–35JC
7140LA35LB	7C141–35LMB
7140LA45	7C140–45C
7140LA45B	7C140–45MB
7140LA45J	7C141–45JC
7140LA45LB	7C141–45LMB
7140LA55	7C140–55C
7140LA55B	7C140–55MB
7140LA55J52	7C141–55JC
7140LA55LB	7C141–55LMB
7140LA70	7C140–55C
7140LA70B	7C140–55MB
7140LA70J	7C141–55JC
7140LA70LB	7C141–55LMB
7140LA90J	7C141–55JC
7140LA90LB	7C141–55LMB
7140SA25	7C140–25C
7140SA25J	7C141–25JC
7140SA30	7C140–30C
7140SA30J	7C141–30JC
7140SA35	7C140–35C
7140SA35B	7C140–35MB
7140SA35J	7C141–35JC
7140SA35LB	7C141–35LMB
7140SA45	7C140–45C
7140SA45B	7C140–45MB
7140SA45J	7C141–45JC
7140SA45LB	7C141–45LMB
7140SA55	7C140–55C
7140SA55B	7C140–55MB
7140SA55J	7C141–55JC
7140SA55LB	7C141–55LMB
7140SA70	7C140–55C
7140SA70B	7C140–55MB
7140SA70J	7C141–55JC
7140SA70LB	7C141–55LMB
7140SA90	7C140–55C
7140SA90B	7C140–55MB
7140SA90J	7C141–55JC
7140SA90LB	7C141–55LMB
7140SA100	7C140–55C
7140SA100B	7C140–55MB
7140SA100L	7C141–55C
7140SA100LB	7C141–55MB
71420–9	7C178–8.5
71420–10	7C178–9.5
71420–12	7C178–12
71421LA25	7C146–25C
71421LA30	7C146–30C
71421LA35	7C146–35C
71421LA35B	7C146–35MB
71421LA45	7C146–45C
71421LA45B	7C146–45MB
71421LA55	7C146–55C
71421LA55B	7C146–55MB
71421LA70	7C146–55C

IDT	CYPRESS
71421LA70B	7C146–55MB
71421LA90	7C146–55C
71421LA90B	7C146–55MB
71421SA25	7C146–25C
71421SA30	7C146–30C
71421SA35	7C146–35C
71421SA35B	7C146–35MB
71421SA45	7C146–45C
71421SA45B	7C146–45MB
71421SA55	7C146–55C
71421SA55B	7C146–55MB
71421SA70	7C146–55C
71421SA70B	7C146–55MB
71421SA90	7C146–55C
71421SA90B	7C146–55MB
7142LA25	7C142–25C
7142LA30	7C142–30C
7142LA35	7C142–35C
7142LA35B	7C142–35MB
7142LA45	7C142–45C
7142LA45B	7C142–45MB
7142LA55	7C142–55C
7142LA55B	7C142–55MB
7142LA70	7C142–55C
7142LA70B	7C142–55MB
7142SA25	7C142–25C
7142SA30	7C142–30C
7142SA35	7C142–35C
7142SA35B	7C142–35MB
7142SA45	7C142–45C
7142SA45B	7C142–45MB
7142SA55	7C142–55C
7142SA55B	7C142–55MB
7142SA70	7C142–55C
7142SA70B	7C142–55MB
7164SA20	7C185–20C
7164SA20P	7C186–20C
7164SA25	7C185–25C
7164SA25B	7C185A–25MB
7164SA25P	7C186–25C
7164SA25PB	7C186A–25MB
7164SA30	7C185–25C
7164SA30B	7C185A–25MB
7164SA30P	7C186–25C
7164SA30PB	7C186A–25MB
7164SA35	7C185–35C
7164SA35B	7C185A–35MB
7164SA35P	7C186–35C
7164SA35PB	7C186A–35MB
7164SA45B	7C185A–45MB
7164SA45PB	7C186A–45MB
7164SA55B	7C185A–55MB
7164SA55BP	7C185A–55MB
71681SA25	7C171A–25C
71681SA25B	7C171A–25MB
71681SA35	7C171A–35C
71681SA35B	7C171A–35MB
71681SA45	7C171A–45C
71681SA45B	7C171A–45MB
71681SA55B	7C171A–45MB
71681SA70B	7C171A–45MB
71681SA85B	7C171A–45MB

IDT	CYPRESS
71682SA25	7C172A–25C
71682SA25B	7C172A–25MB
71682SA35	7C172A–35C
71682SA35B	7C172A–35MB
71682SA45	7C172A–45C
71682SA45B	7C172A–45MB
71682SA100B	7C172A–45MB
7187SA15	7C187–15C
7187SA20	7C187–20C
7187SA25	7C187–25C
7187SA25B	7C187A–25MB
7187SA30	7C187–25C
7187SA30B	7C187A–25MB
7187SA35	7C187–35C
7187SA35B	7C187A–35MB
7187SA45B	7C187A–45MB
7188SA15	7C164–15C
7188SA20	7C164–20C
7188SA20B	7C164A–20MB
7188SA25	7C164–25C
7188SA25B	7C164A–25MB
7188SA30	7C164–25C
7188SA35	7C164–35C
7188SA35B	7C164A–35MB
71981S35	7C161–35C
71981S35B	7C161A–35M
71981S45	7C161–45C
71981S45B	7C161A–45M
71981S55B	7C161A–45M
71981S70B	7C161A–45M
71981S85B	7C161A–45M
71982S35	7C162–35C
71982S35B	7C162A–35M
71982S45B	7C162A–45M
7198S35	7C166–35C
7198S35B	7C166A–35M
7198S45B	7C166A–45M
71B256A12	7C199–12C
71B256S20	7C199–20C
71B256S20B	7C199–20MB
71B256SA12	7C199–12C
71B258S12	7C194–12C
71B258S15	7C194–15C
71B258S15B	7C194–15MB
71B258S20	7C194–20C
71B258S20B	7C194–20MB
71B259	7C188
7200LA15	7C419–15
7200LA20T	7C419–20
7200LA25T	7C419–25
7200LA30T	7C419–30
7200LA35T	7C419–30
7200LA40T	7C419–40
7200LA50T	7C419–50
7200LA65T	7C419–65
7200LA80T	7C419–65
7200SA15	7C419–15
7200SA20T	7C419–20
7200SA25T	7C419–25
7200SA30T	7C419–30
7200SA35T	7C419–30
7200SA40T	7C419–40

Product Line Cross Reference

IDT	CYPRESS
7200SA50T	7C419–50
7200SA65T	7C419–65
7200SA80T	7C419–65
7201LA15	7C421–15
7201LA20	7C420–20C
7201LA20T	7C421–20C
7201LA25	7C420–25C
7201LA25T	7C421–25C
7201LA30B	7C420–30MB
7201LA30TB	7C421–30MB
7201LA35	7C420–30C+
7201LA35T	7C421–30C
7201LA40B	7C420–40MB+
7201LA40TB	7C421–40MB
7201LA50	7C420–40C+
7201LA50B	7C420–40MB+
7201LA50T	7C421–40C
7201LA50TB	7C421–40MB
7201LA65	7C420–65C+
7201LA65B	7C420–65MB+
7201LA65T	7C421–65C
7201LA65TB	7C421–65MB
7201LA80	7C420–65C+
7201LA80B	7C420–65MB+
7201LA120	7C420–65C+
7201LA120B	7C420–65MB+
7201SA15	7C421–15
7201SA20	7C420–20C
7201SA20T	7C421–20C
7201SA25	7C420–25C
7201SA25T	7C421–25C
7201SA30B	7C420–30MB
7201SA30TB	7C421–30MB
7201SA35	7C420–30C
7201SA35T	7C421–30C
7201SA40B	7C420–40MB
7201SA40TB	7C421–40MB
7201SA50	7C420–40C
7201SA50B	7C420–40MB
7201SA50T	7C421–40C
7201SA50TB	7C421–40MB
7201SA65	7C420–65C
7201SA65B	7C420–65MB
7201SA65T	7C421–65C
7201SA65TB	7C421–65MB
7201SA80	7C420–65C
7201SA80B	7C420–65MB
7201SA120	7C420–65C
7201SA120B	7C420–65MB
7202LA15	7C425–15
7202LA20	7C424–20C
7202LA20T	7C425–20C
7202LA25	7C424–25C
7202LA25T	7C425–25C
7202LA30B	7C424–30MB
7202LA30TB	7C425–30MB
7202LA35	7C424–30C+
7202LA35T	7C425–30C
7202LA40B	7C424–40MB+
7202LA40TB	7C425–40MB
7202LA50	7C424–40C+
7202LA50B	7C424–40MB+

IDT	CYPRESS
7202LA50T	7C425–40C
7202LA50TB	7C425–40MB
7202LA65	7C424–65C+
7202LA65B	7C424–65MB+
7202LA65T	7C425–65C
7202LA65TB	7C425–65MB
7202LA80	7C424–65C+
7202LA80B	7C424–65MB+
7202LA120	7C424–65C+
7202LA120B	7C424–65MB+
7202SA15	7C425–15
7202SA20	7C424–20C
7202SA20T	7C425–20C
7202SA25	7C424–25C
7202SA25T	7C425–25C
7202SA30B	7C424–30MB
7202SA30TB	7C425–30MB
7202SA35	7C424–30C
7202SA35T	7C425–30C
7202SA40B	7C424–40MB
7202SA40TB	7C425–40MB
7202SA50	7C424–40C
7202SA50B	7C424–40MB
7202SA50T	7C425–40C
7202SA50TB	7C425–40MB
7202SA65	7C424–65C
7202SA65B	7C424–65MB
7202SA65T	7C425–65C
7202SA65TB	7C425–65MB
7202SA80	7C424–65C
7202SA80B	7C424–65MB
7202SA120	7C424–65C
7202SA120B	7C424–65MB
7203L20	7C428–20C
7203L20T	7C429–20C
7203L25	7C428–25C
7203L25B	7C428–25MB
7203L25T	7C429–25C
7203L25TB	7C429–25MB
7203L30	7C428–30C
7203L30T	7C429–30C
7203L35B	7C428–30MB
7203L35TB	7C429–30MB
7203L40	7C428–40C
7203L40T	7C429–40C
7203L55B	7C428–40MB
7203L55TB	7C429–40MB
7203L65	7C428–65C
7203L65B	7C428–65MB
7203L65T	7C429–65C
7203L65TB	7C429–65MB
7203L80	7C428–65C
7203L80B	7C428–65MB
7203L80T	7C429–65C
7203L80TB	7C429–65MB
7203S20	7C428–20C
7203S20T	7C429–20C
7203S25	7C428–25C
7203S25B	7C428–25MB
7203S25T	7C429–25C
7203S25TB	7C429–25MB
7203S30	7C428–30C

IDT	CYPRESS
7203S30T	7C429–30C
7203S35B	7C428–30MB
7203S35TB	7C429–30MB
7203S40	7C428–40C
7203S40T	7C429–40C
7203S55B	7C428–40MB
7203S55TB	7C429–40MB
7203S65	7C428–65C
7203S65B	7C428–65MB
7203S65T	7C429–65C
7203S65TB	7C429–65MB
7203S80	7C428–65C
7203S80B	7C428–65MB
7203S80T	7C429–65C
7203S80TB	7C429–65MB
7204S25	7C432–25C
7204S25T	7C433–25C
7204S30	7C432–30C
7204S30T	7C433–30C
7204S35B	7C432–30MB
7204S35TB	7C433–30MB
7204S40	7C432–40C
7204S40T	7C433–40C
7204S55B	7C432–40MB
7204S55TB	7C433–40MB
7204S65	7C432–65C
7204S65B	7C432–65MB
7204S65T	7C433–65C
7204S65TB	7C433–65MB
7204S80B	7C432–65MB
7204S80TB	7C433–65MB
7205L20	7C460–15C
7205L25	7C460–25C
7205L30B	7C460–15MB
7205L30B	7C460–25MB
7205L35	7C460–25C
7205L50	7C460–40C
7205L50B	7C460–40MB
7206–15	7C462–15
7206–20	7C462–20
7206–25	7C462–25
72201L15	7C4201–15
72201L25	7C4201–25
72201L35	7C4201–35
72205LB15	7C4205–15
72205LB25	7C4205–25
72205LB35	7C4205–35
72211L15	7C4211–15
72211L25	7C4211–25
72211L35	7C4211–35
72215LB15	7C4215–15
72215LB25	7C4215–25
72215LB35	7C4215–35
72221L15	7C4221–15
72221L25	7C4221–25
72221L35	7C4221–35
72225LB15	7C4225–15
72225LB25	7C4225–25
72225LB35	7C4225–35
72231L15	7C4231–15
72231L25	7C4231–25
72231L35	7C4231–35

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

\+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

IDT	CYPRESS
72235LB15	7C4235–15
72235LB25	7C4235–25
72235LB35	7C4235–35
72241L15	7C4241–15
72241L25	7C4241–25
72241L35	7C4241–35
72245LB15	7C4245–15
72245LB25	7C4245–25
72245LB35	7C4245–35
72401L10	7C401–10C
72401L10B	7C401–10MB
72401L15	7C401–15C
72401L15B	7C401–15MB
72401L25	7C401–25C
72401L25B	7C401–25MB
72401L35	7C401–25C
72401L35B	7C401–25MB
72401L45	7C401–25C
72402L10	7C402–10C
72402L10B	7C402–10MB
72402L15	7C402–15C
72402L15B	7C402–15MB
72402L25	7C402–25C
72402L25B	7C402–25MB
72402L35	7C402–25C
72402L35B	7C402–25MB
72402L45	7C402–25C
72403L10	7C403–10C
72403L10B	7C403–10MB
72403L15	7C403–15C
72403L15B	7C403–15MB
72403L25	7C403–25C
72403L25B	7C403–25MB
72403L35	7C403–25C
72403L35B	7C403–25MB
72403L45	7C403–25C
72404L10	7C404–10C
72404L10B	7C404–10MB
72404L15	7C404–15C
72404L15B	7C404–15MB
72421L15	7C4421–15
72421L25	7C4421–25
72421L35	7C4421–35
72404L25	7C404–25C
72404L25B	7C404–25MB
72404L35	7C404–25C
72404L35B	7C404–25MB
72404L45	7C404–25C
7M4017S40C	1830HD–35C
7M4017S45C	1830HD–45C
7M4017S50C	1830HD–45C
7M4017S50CB	1830HD–45MB
7M4017S55C	1830HD–55C
7M4017S60C	1830HD–55C
7M4017S60CB	1830HD–55MB
7M4017S70C	1830HD–55C
7M4017S70CB	1830HD–55MB
7MP4031	M1821PZ
7MP4036Z	M1831PZ
7MP4036M	M1831PM
7MP4036Z	M1836PZ
7MP4036M	M1836PM

IDT	CYPRESS
7MP4045Z	M1841PZ
7MP4045M	M1841PM
7MP4120Z	M1851PZ
7MP4120M	M1851PM
7MP6121S	M7450PM–33C
7MP6122S	M7451PM–33C
7MP6133S33	M7427PB–20
7MP6134S33	M7428PB–20
7MP6151S33	M9230PB–20
7MP6152S33	M9231PB–20
7MP6157S	M7432PB–12/15C
7MP6183S	M7424PB–20C
7MP6184S	M7425PB–20C

INTEL	CYPRESS
PREFIX: 85C	PREFIX: CY
PREFIX: 85C	PREFIX: PLD
PREFIX: D	SUFFIX: D
PREFIX: L	SUFFIX: L
PREFIX: P	SUFFIX: P
SUFFIX: /B	SUFFIX: B
1223–35	7C148–35C
1223M–35	7C148–25M+
1400–35	7C167A–35C
1400M–45	7C167A–45M
1403–25	7C167A–25C
1403–35	7C167A–35C+
1403LM–35	7C167A–35M*
1403M–35	7C167A–35M+
1420–45	7C168A–35C
1420M–55	7C168A–45M+
1423–25	7C168A–25C+
1423–35	7C168A–35C+
1423M–35	7C168A–35M*
1433–30	7C128A–25C+
1433–35	7C128A–35C+
1433M–35	7C128A–35M+

ISSI	CYPRESS
PREFIX: IS	PREFIX: CY
SUFFIX: CW	SUFFIX: W
SUFFIX: PL	SUFFIX: J
27HC010–30C	27H010–30C
27HC010–45C	27H010–45C
27HC010–55C	27H010–55C
27HC010–70C	27C010–70C

LATTICE	CYPRESS
PREFIX: EE	PREFIX: CY
PREFIX: GAL	PREFIX: CY
PREFIX: ST	PREFIX: CY
SUFFIX: B	SUFFIX: B
SUFFIX: D	SUFFIX: D
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
GAL16V8A–10LJ	PALCE16V8–10JC
GAL16V8A–10LP	PALCE16V8–10PC
GAL16V8A–15LJ	PALCE16V8–15JC
GAL16V8A–15LP	PALCE16V8–15PC
GAL16V8A–15QJ	PALCE16V8L–15JC
GAL16V8A–15QP	PALCE16V8L–15PC
GAL16V8A–L5LJ	PALCE16V8–25JC
GAL16V8A–25LP	PALCE16V8–25PC

LATTICE	CYPRESS
GAL16V8A–25QJ	PALCE16V8L–25JC
GAL16V8A–25QP	PALCE16V8L–25PC
GAL16V8B–7LJ	PALCE16V8–7JC
GAL16V8B–7LP	PALCE16V8–7PC
GAL16V8B–10LJ	PALCE16V8–10JC
GAL16V8B–10LJI	PALCE16V8–10JI
GAL16V8B–10LP	PALCE16V8–10PC
GAL16V8B–10LPI	PALCE16V8–10PI
GAL16V8B–15LJI	PALCE16V8–15JI
GAL16V8B–15LPI	PALCE16V8–15PI
GAL16V8B–25LJI	PALCE16V8–25JI
GAL16V8B–25LPI	PALCE16V8–25PI
GAL16V8C–5LJ	PALCE16V8–5JC
GAL20V8A	PALCE20V8
GAL20V8B	PALCE20V8
GAL22V10B–7LJ	PALC22V10D–7JC
GAL22V10B–7LP	PALC22V10D–7PC
GAL22V10B–10LJ	PALC22V10D–10JC
GAL22V10B–10LP	PALC22V10D-10PC
GAL22V10B–15LD /883	PALC22V10D–15DMB
GAL22V10B–15LJ	PALC22V10D-15JC
GAL22V10B–15LJI	PALC22V10D–15JI
GAL22V10B–15LP	PALC22V10D-15PC
GAL22V10B–15LPI	PALC22V10D–15PI
GAL22V10B–15LR /883	PALC22V10D–15LMB
GAL22V10B–20LJI	PALC22V10D–15JI
GAL22V10B–20LD /883	PALC22V10D–15DMB
GAL22V10B–20LPI	PALC22V10D–15PI
GAL22V10B–20LR /883	PALC22V10D–15LMB
GAL22V10B–25LD /883	PALC22V10D–25DMB
GAL22V10B–25LJ	PALC22V10D-25JC
GAL22V10B–25LJI	PALC22V10D–25JI
GAL22V10B–25LP	PALC22V10D-25PC
GAL22V10B–25LPI	PALC22V10D–25PI
GAL22V10B–25LR /883	PALC22V10D–25LMB
GAL22V10B–30LD /883	PALC22V10D–25DMB
GAL22V10B–30LR /883	PALC22V10D–25LMB
GAL22V10C–5LJ	PAL22V10G–5JC
GAL22V10C–7LJ	PAL22V10D–7JC
GAL22V10C–7PC	PAL22V10D–7PC

MACRONIX	CYPRESS
PREFIX: MX	PREFIX: CY
SUFFIX: P	SUFFIX: P
SUFFIX: Q	SUFFIX: J
SUFFIX: D	SUFFIX: W
SUFFIX: T	SUFFIX: Z
27C1000–45C	27H010–45C
27C1000–55C	27C010–55C
27C1000–70C	27C010–70C
27C1000–90C	27C010–90C
27C1000–120C	27C010–120C
27C1000–150C	27C010–150C
27C1000–200C	27C010–200C
27C256–45C	27C256–45C

Product Line Cross Reference

MACRONIX	CYPRESS
27C256–55C	27C256–55C
27C256–70C	27C256–70C
27C256–90C	27C256–90C
27C256–120C	27C256–120C
27C256–150C	27C256–150C
27C256–200C	27C256–200C
27C512–45C	27H512–45C
27C512–55C	27H512–55C
27C512–70C	27H512–70C
27C512–90C	27C512–90C
27C512–120C	27C512–120C
27C512–150C	27C512–150C
27C512–200C	27C512–200C

MICROCHIP	CYPRESS
SUFFIX: J	SUFFIX: W
SUFFIX: P	SUFFIX: P
SUFFIX: L	SUFFIX: J
27C64–12	27C64–120C
27C64–15	27C64–150C
27C64–17	27C64–150C
27C64–20	27C64–200C
27C64–25	27C64–200C
27C128–12	CY27C128–120C+
27C128–15	CY27C128–150C+
27C128–17	CY27C128–150C+
27C128–20	CY27C128–200C+
27C128–25	CY27C128–200C+
27C256–10	CY27C256–90C+
27C256–12	CY27C256–120C+
27C256–15	CY27C256–150C+
27C256–20	CY27C256–200C+
27C512–10	27C512–90C
27C512–12	27C512–120C
27C512–15	27C512–150C
27C512–20	27C512–200C
27C512–90	27C512–90C
27HC256–55	CY27C256–55C
27HC256–70	CY27C256–70C
27HC256–90	CY27C256–90C

MICRON**	CYPRESS
PREFIX: MT	PREFIX: CY
58LC64K18B2	7C1331
5C1001–15C	7C107A–15C
5C1001–20C	7C107A–20C
5C1001–25C	7C107A–25C
5C1008–20C	7C109–20C
5C1008–25C	7C109–25C
5C1008–12C	7C109A–12C
5C1008–15C	7C109A–15C
5C1008–20C	7C109A–20C
5C1601–15	7C167A–15C
5C1601–20C	7C167A–20C
5C1601–25C	7C167A–25C
5C1601–30	7C167A–25C
5C1601–35C	7C167A–35C
5C1604–15	7C168A–15C
5C1604–20C	7C168A–20C
5C1604–25C	7C168A–25C
5C1604–30	7C168A–25C
5C1604–35C	7C168A–35C
5C1605–15	7C170A–15C

MICRON**	CYPRESS
5C1605–20C	7C170A–20C
5C1605–25C	7C170A–25C
5C1605–30	7C170A–25C
5C1605–35C	7C170A–35C
5C1608–15	7C128A–15C
5C1608–20C	7C128A–20C
5C1608–25C	7C128A–25C
5C1608–35C	7C128A–35C
5C2561–12	7C197–12
5C2561–15	7C197–15
5C2561–20	7C197–20
5C2561–25	7C197–25C
5C2561–30	7C197–25C
5C2561–35	7C197–35C
5C2561–45	7C197–45C
5C2564–12	7C194–12
5C2564–15	7C194–15
5C2564–20	7C194–20
5C2564–25	7C194–25C
5C2564–30	7C194–25C
5C2564–35	7C194–35C
5C2564–45	7C194–45C
5C2565–12	7C195–12
5C2565–15	7C195–15
5C2565–20	7C195–20
5C2565–25	7C195–25C
5C2565–30	7C195–25C
5C2565–35	7C195–35C
5C2565–45	7C195–45C
5C2568–12	7C199–12
5C2568–15	7C199–15
5C2568–20	7C199–20
5C2568–25	7C199–25C
5C2568–30	7C199–25C
5C2568–35	7C199–35C
5C2568–45	7C199–45C
5C2889–20C	7C188–20C
5C2889–25C	7C188–25C
5C6404–15	7C164–15C
5C6404–20	7C164–20C
5C6404–25	7C164–25C
5C6404–30	7C164–25C
5C6404–35	7C164–35C
5C6405–15	7C166–15C
5C6405–20C	7C166–20C
5C6405–25C	7C166–25C
5C6405–30	7C166–25C
5C6405–35C	7C166–35C
5C6408–15	7C185–15C
5C6408–20C	7C185–20C
5C6408–25C	7C185–25C
5C6408–30	7C185–25C
5C6408–35C	7C185–35C
5LC2568–15	7C1399–15
5LC2568–20C	7C1399–20C
5LC2568–25C	7C1399–25C
58LC64K18–9	7C1031–8.5
58LC64K18–10	7C1031–10
85C1664–30C	1620HD–30C
85C8128–25	M1420PD–25C
85C8128–35	M1420PD–35C
85C8128–45C	1423PD–45C

MICRON**	CYPRESS
8S1632Z	M1821PZ
8S1632M	M1821PM
8S6432Z	M1831PZ
8S6432M	M1831PM
8S25632Z	M1841PZ
8S25632M	M1841PM
4S12832Z	M1836PZ
4S12832M	M1836PM

MITSUBISHI	CYPRESS
PREFIX: M5L	PREFIX: CY
PREFIX: M5M	PREFIX: CY
SUFFIX: AP	SUFFIX: L
SUFFIX: FP	SUFFIX: F
SUFFIX: K	SUFFIX: D
SUFFIX: P	SUFFIX: P
21C67P–35	7C167A–35C
21C67P–45	7C167A–45C
21C67P–55	7C167A–45C
21C68P–35	7C168A–35C
21C68P–45	7C168A–45C
21C68P–55	7C168A–45C
27C256–85	27C256–70C+
27C256–100	27C256–90C+
27C256–120	27C256–120C+
27C256–150	27C256–150C+
27C256–170	27C256–150C+
5165L–70	7C186–55C+
5165L–100	7C186–55C+
5165L–120	7C186–55C+
5165P–70	7C186–55C+
5165P–100	7C186–55C+
5165P–120	7C186–55C+
5178P–45	7C186–45C+
5178P–55	7C186–55C+
5187P–25	7C187–25C
5187P–35	7C187–35C
5187P–45	7C187–45C
5187P–55	7C187–45C
5188P–25	7C164–25C
5188P–35	7C164–35C
5188P–45	7C164–45C
5188P–55	7C164–45C
5257J–35	7C197–35C
5257J–45	7C197–45C
5257P–35	7C197–35C
5257P–45	7C197–45C
5258J–45	7C194–45C
5258P–35	7C194–35C
5258P–45	7C194–45C
52B79P/J	7C188

MMI/AMD	CYPRESS
SUFFIX: 883B	SUFFIX: B
SUFFIX: F	SUFFIX: F
SUFFIX: J	SUFFIX: D
SUFFIX: L	SUFFIX: L
SUFFIX: N	SUFFIX: P
SUFFIX: SHRP	SUFFIX: B
PAL12L10C	PLDC20G10–35C
PAL12L10M	PLDC20G10–40M
PAL14L8C	PLDC20G10–35C
PAL14L8M	PLD20G10–40M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

MMI/AMD	CYPRESS
PAL16L6C	PLD20G10–35C
PAL16L6M	PLDC20G10–40M
PAL16L8A–2C	PALC16L8–35C
PAL16L8A–2M	PALC16L8–40M
PAL16L8A–4C	PALC16L8L–35C
PAL16L8A–4M	PALC16L8–40M
PAL16L8AC	PALC16L8–25C
PAL16L8AM	PALC16L8–30M
PAL16L8B–2C	PALC16L8–35C
PAL16L8B–2M	PALC16L8–30M
PAL16L8B–4C	PALC16L8L–35C
PAL16L8B–4M	PALC16L8–40M
PAL16L8BM	PALC16L8–20M
PAL16L8C	PALC16L8–35C
PAL16L8D–4C	PALC16L8L–25C
PAL16L8D–4M	PALC16L8–30M
PAL16L8M	PALC16L8–40M
PAL16R4A–2C	PALC16R4–35C
PAL16R4A–2M	PALC16R4–40M
PAL16R4A–4C	PALC16R4L–35C
PAL16R4A–4M	PALC16R4–40M
PAL16R4AC	PALC16R4–25C
PAL16R4AM	PALC16R4–30M
PAL16R4B–2C	PALC16R4–25C
PAL16R4B–2M	PALC16R4–30M
PAL16R4B–4C	PALC16R4L–35C
PAL16R4B–4M	PALC16R4–40M
PAL16R4BM	PALC16R4–20M
PAL16R4C	PALC16R4–35C
PAL16R4D–4C	PALC16R4L–25C
PAL16R4M	PALC16R4–40M
PAL16R6A–2C	PALC16R6–35C
PAL16R6A–2M	PALC16R6–40M
PAL16R6A–4C	PALC16R6L–35C
PAL16R6A–4M	PALC16R6–40M
PAL16R6AC	PALC16R6–25C
PAL16R6AM	PALC16R6–30M
PAL16R6B–2C	PALC16R6–25C
PAL16R6B–2M	PALC16R6–30M
PAL16R6B–4C	PALC16R6L–35C
PAL16R6B–4M	PALC16R6–40M
PAL16R6BM	PALC16R6–20M
PAL16R6C	PALC16R6–35C
PAL16R6D–4C	PALC16R6L–25C
PAL16R6M	PALC16R6–40M
PAL16R8A–2C	PALC16R8–35C
PAL16R8A–2M	PALC16R8–40M
PAL16R8A–4C	PALC16R8L–35C
PAL16R8A–4M	PALC16R8–40M
PAL16R8AC	PALC16R8–25C
PAL16R8AM	PALC16R8–30M
PAL16R8B–2C	PALC16R8–25C
PAL16R8B–2M	PALC16R8–30M
PAL16R8B–4C	PALC16R8L–35C
PAL16R8B–4M	PALC16R8–40M
PAL16R8BM	PALC16R8–20M
PAL16R8C	PALC16R8–35C
PAL16R8D–4C	PALC1648L–25C
PAL16R8M	PALC16R8–40M
PAL18L4C	PLDC20G10–35C
PAL18L4M	PLDC20G10–40M
PAL20L10AC	PLDC20G10–35C
PAL20L10AM	PLDC20G10–30M

MMI/AMD	CYPRESS
PAL20L10C	PLDC20G10–35C
PAL20L10M	PLDC20G10–40M
PAL20L2C	PLDC20G10–35C
PAL20L2M	PLDC20G10–40M
PAL20L8A–2C	PLDC20G10–35C
PAL20L8A–2M	PLDC20G10–40M
PAL20L8AC	PLDC20G10–25C
PAL20L8AM	PLDC20G10–30M
PAL20L8C	PLDC20G10–35C
PAL20L8M	PLDC20G10–40M
PAL20R4A–2C	PLDC20G10–35C
PAL20R4A–2M	PLDC20G10–40M
PAL20R4AC	PLDC20G10–25C
PAL20R4AM	PLDC20G10–30M
PAL20R4C	PLDC20G10–35C
PAL20R4M	PLDC20G10–40M
PAL20R6A–2C	PLDC20G10–35C
PAL20R6A–2M	PLDC20G10–40M
PAL20R6AC	PLDC20G10–25C
PAL20R6AM	PLDC20G10–30M
PAL20R6C	PLDC20G10–35C
PAL20R6M	PLDC20G10–40M
PAL20R8A–2C	PLDC20G10–35C
PAL20R8A–2M	PLDC20G10–40M
PAL20R8AC	PLDC20G10–25C
PAL20R8AM	PLDC20G10–30M
PAL20R8C	PLDC20G10–35C
PAL20R8M	PLDC20G10–40M
PALC22V10/A	PALC22V10–35C

MOTOROLA	CYPRESS
PREFIX: MCM	PREFIX: CY
SUFFIX: BXAJC	SUFFIX: MB
SUFFIX: P	SUFFIX: P
SUFFIX: S	SUFFIX: D
SUFFIX: Z	SUFFIX: L
1423–45	7C168A–45C+
2016H–45	6116A–45C
2018–35	7C128A–35C
2167H–35	7C167A–35C
2167H–45	7C167A–45C
6164–45	7C186–45C
6168–35	7C168A–35C+
6205D–20	7C188–20C
6205D–25	7C188–25C
6206D–12	7C199–12C
6206D–15	7C199–15
6206D–20	7C199–20
6206D–25	7C199–25
6206D–35	7C199–35C
6207C–15	7C197–15
6207C–20	7C197–20
6207C–25	7C197–25
6207C–35	7C197–35
6208C–12	7C194–12C
6208C–15	7C194–15C
6208C–20	7C194–20
6208C–25	7C194–25
6208C–35	7C194–35
6209C–12	7C195–12C
6209–15	7C195–15C
6209C–20	7C195–20C
6209C–25	7C195–25C

MOTOROLA	CYPRESS
6226–20	7C109–20C
6226–25	7C109–25C
6264–15C	7C185–15C
6264–25	7C185–25C
6264–25	7C186–25C
6264–30	7C185–25C
6264–30	7C186–25C
6264–35	7C185–35C
6264–35	7C186–35C
6264–45	7C186–45C
6265C–25	7C182–25C
6268P25	7C168A–25C
6268P35	7C168A–35C
6268P40	7C168A–40C
6268P45	7C168A–45C
6269P20	7C169A–20C
6269P25	7C169A–25C
6269P35	7C169A–35C
6270–20	7C170A–20C
6270–25	7C170A–25C
6270–35	7C170A–35C
6287–15	7C187–15C
6287–20	7C187–20C
6287–25	7C187–25C
6287–35	7C187–35C
6288–15	7C164–15C
6288–25	7C164–25C
6288–30	7C164–25C
6288–35	7C164–35C
6290–15	7C166–15C
6290–20	7C166–20C
6290–25	7C166–25C
6290–35	7C166–35C
62V06D–20	7C1399–20C
62V06D–25	7C1399–25C
6726A–12	7C109A–12C
6726A–15	7C109A–15C
6726A–20	7C109A–20C
67H518–9	7C178–8.5
67H518–12	7C178–12
67H518–9	7C1031–8.5
67H518–12	7C1031–12

NATIONAL	CYPRESS
PREFIX: DM	PREFIX: CY
PREFIX: GAL	PREFIX: None
PREIFX: IDM	PREFIX: CY
PREFIX: NM	PREFIX: CY
PREFIX: NM	PREFIX: CY
SUFFIX: A	SUFFIX: Z
SUFFIX: J	SUFFIX: D
SUFFIX: N	SUFFIX: P
SUFFIX: Q	SUFFIX: W
SUFFIX: V	SUFFIX: J
18L4C	PLDC20G10–35C
18L4M	PLDC20G10–40M
20L2M	PLDC20G10–40M
2147H	2147–C
2147H	7C147–C
2148H	7C148–C
2148H	2148–C
2148H	21L48–C

NATIONAL	CYPRESS
27C010–120C	27C010–120C
27C010–150C	27C010–150C
27C010–200C	27C010–200C
27C64–100C	27C64–90C
27C64–120C	27C64–120C
27C64–150C	27C64–150C
27C64–200C	27C64–200C
27C128–12C	27C128–120C+
27C128–15C	27C128–150C+
27C128–20C	27C128–200C+
27C256–100	27C256–90C+
27C256–120	27C256–120C+
27C256–150	27C256–150C+
27C256–200	27C256–200C+
27C512–120C	27C512–120C
27C512–150C	27C512–150C
27C512–200C	27C512–200C
27P010–70C	27C010–70C
27P010–90C	27C010–90C
27P010–100C	27C010–90C
77LS181	7C282A–45M
77S181	7C282A–45M
77S181A	7C282A–45M
77S281	7C281A–45M
77S281A	7C281A–45M
77S401	7C401–10M
77S401A	7C401–10M
77S402	7C402–10M
77S402A	7C402–10M
77SR181	7C235A–40M
77SR476	7C225A–40M–
77SR476B	7C225A–40M–
85S07A	7C128–45C+
87LS181	7C282A–45C
87S181	7C282A–45C
87S281	7C281A–45C
87S281A	7C281A–45C
87S401	7C401–10C
87S401A	7C401–15C
87S402	7C402–10C
87S402A	7C402–15C
87SR181	7C235–40C
87SR476	7C225A–40C
87SR476B	7C225A–30C
93L422A	7C122–C
C27C53–55	27C256–55C
C27C53–70	27C256–70C
GAL22V10–15C	PALC22V10D–15C
GAL22V10–20I	PALC22V10D–15I
GAL22V10–20M	PALC22V10D–15M
GAL22V10–25C	PALC22V10D–25C
GAL22V10–30I	PALC22V10D–25I
GAL22V10–30M	PALC22V10D–25M
NMF512X9–15	7C421A–15
NMF512X9–25	7C421–25
NMF2048X9–20	7C429–20
NMF4096X9A–25	7C433–25
PAL164A2M	PALC16R4–40M
PAL16L8A2C	PALC16L8–35C
PAL16L8A2M	PALC16L8–40M
PAL16L8AC	PALC16L8–25C
PAL16L8AM	PALC16L8–30M

NATIONAL	CYPRESS
PAL16L8B2C	PALC16L8–25C
PAL16L8B2M	PALC16L8–30M
PAL16L8B4C	PALC16L8L–35C
PAL16L8B4M	PALC16L8–40M
PAL16L8BM	PALC16L8–20M
PAL16L8C	PALC16L8–35C
PAL16L8M	PALC16L8–40M
PAL16R4A2C	PALC16R4–35C
PAL16R4AC	PALC16R4–25C
PAL16R4AM	PALC16R4–30M
PAL16R4B2C	PALC16R4–25C
PAL16R4B2M	PALC16R4–30M
PAL16R4B4C	PALC16R4L–35C
PAL16R4B4M	PALC16R4–40M
PAL16R4BM	PALC16R4–20M
PAL16R4C	PALC16R4–35C
PAL16R4M	PALC16R4–40M
PAL16R6A2C	PALC16R6–35C
PAL16R6A2M	PALC16R6–40M
PAL16R6AC	PALC16R6–25C
PAL16R6AM	PALC16R6–30M
PAL16R6B2C	PALC16R6–25C
PAL16R6B2M	PALC16R6–30M
PAL16R6B4C	PALC16R6L–35C
PAL16R6B4M	PALC16R6–40M
PAL16R6BM	PALC16R6–20M
PAL16R6C	PALC16R6–35C
PAL16R6M	PALC16R6–40M
PAL16R8A2C	PALC16R8–35C
PAL16R8A2M	PALC16R8–40M
PAL16R8AC	PALC16R8–25C
PAL16R8AM	PALC16R8–30M
PAL16R8B2C	PALC16R8–25C
PAL16R8B2M	PALC16R8–30M
PAL16R8B4C	PALC16R8L–35C
PAL16R8B4M	PALC16R8–40M
PAL16R8BM	PALC16R8–20M
PAL16R8C	PALC16R8–35C
PAL16R8M	PALC16R8–40M
PAL20L2C	PLDC20G10–35C
PAL20L8AC	PLDC20G10–25C
PAL20L8AM	PLDC20G10–30M
PAL20L8BC	PLDC20G10–25C
PAL20L8BM	PLDC20G10–30M
PAL20L8C	PLDC20G10–35C
PAL20L8M	PLDC20G10–40M
PAL20L10B2C	PLDC20G10–25C
PAL20L10B2M	PLDC20G10–30M
PAL20L10C	PLDC20G10–35C
PAL20L10M	PLDC20G10–40M
PAL20R4AC	PLDC20G10–25C
PAL20R4AM	PLDC20G10–30M
PAL20R4BC	PLDC20G10–25C
PAL20R4BM	PLDC20G10–30M
PAL20R4C	PLDC20G10–35C
PAL20R4M	PLDC20G10–40M
PAL20R6AC	PLDC20G10–25C
PAL20R6AM	PLDC20G10–30M
PAL20R6BC	PLDC20G10–25C
PAL20R6BM	PLDC20G10–30M
PAL20R6C	PLDC20G10–35C
PAL20R6M	PLDC20G10–40M

NATIONAL	CYPRESS
PAL20R8AC	PLDC20G10–25C
PAL20R8AM	PLDC20G10–30M
PAL20R8BC	PLDC20G10–25C
PAL20R8BM	PLDC20G10–30M
PAL20R8C	PLDC20G10–35C
PAL20R8M	PLDC20G10–40M

NEC	CYPRESS
PREFIX: uPD	PREFIX: CY
SUFFIX: C	SUFFIX: P
SUFFIX: D	SUFFIX: D
SUFFIX: K	SUFFIX: L
SUFFIX: L	SUFFIX: F
2147A	7C147–C
2149	2149–C
2149	7C149–C
2167–2	7C167A–C
27HC65–25	7C263/4–25C
27HC65–35	7C263/4–35C
27HC65–45	7C263/4–45C
4311–45	7C167A–45C
4311–55	7C167A–45C
43254C–35	7C194–35
43254C–45	7C194–45
4361	7C187–C
4362	7C164–C
4363	7C166–C
43259–20	7C188–20
43259–25	7C188–25
431001–20	7C107A–20C
431001–25	7C107A–25C
431004–20	7C106A–20C
431004–25	7C106A–25C
431008–15	7C109A–15
431008–20	7C109A–20
431008–20	7C109–20

OKI	CYPRESS
PREFIX: MSM	PREFIX: CY
27128A–12C	27C128–120C+
27128A–15C	27C128–150C+
27128A–20C	27C128–200C+
27256–100	27C256–90C+
27256–120	27C256–120C+
27256–150	27C256–150C+
27256–200	27C256–200C+
27256H–55	27C256–55C
27256H–70	27C256–70C

PARADIGM	CYPRESS
PREFIX: PDM	PREFIX: CY
41251L	7C191–C
41251LB	7C191–MB*
41251S	7C191–C
41251SB	7C191–MB
41252L	7C192–C
41252LB	7C192–MB*
41252S	7C192–C
41252SB	7C192–MB
41256L	7C199/8–C*
41256LB	7C199/8–MB*
41256S	7C199/8–C
41256SB	7C199/8–MB

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}
– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

PARADIGM	CYPRESS
41258L	7C194–C*
41258LB	7C194–B*
41258S	7C194–C
41258SB	7C194–B

PERFORMANCE	CYPRESS
PREFIX: P	PREFIX: CY
SUFFIX: L	SUFFIX: L
SUFFIX: S	SUFFIX: S
41256–35	7C199–35
41256–45	7C199–45
4C1256–25	7C199–25
4C1256–35	7C199–35
4C1256–45	7C198–45
4C1257–25	7C197–25
4C1257–35	7C197–35
4C1257–45	7C197–45
4C1258–25	7C194–25
4C1258–35	7C194–35
4C1258–45	7C194–45
4C150–12C	7C150–12C
4C150–15C	7C150–15C
4C150–15M	7C150–15M
4C150–20C	7C150–15C
4C150–20M	7C150–15M
4C150–25C	7C150–25C
4C150–25M	7C150–25M
4C150–35M	7C150–35M
4C164DW–20C	7C186–20C
4C164DW–25C	7C186–25C
4C164DW–25M	7C186A–25M
4C164DW–35C	7C186–35C
4C164DW–35M	7C186A–35M
4C164DW–55C	7C186–55C
4C164P–20C	7C185–20C
4C164P–25C	7C185–25C
4C164P–25M	7C185A–25M
4C164P–35C	7C185–35C
4C164P–35M	7C185A–35M
4C164P–45M	7C185A–45M
4C1681–25C	7C171A–25C
4C1681–35C	7C171A–35C
4C1681–35M	7C171A–35M
4C1681–45C	7C171A–45C
4C1681–45M	7C171A–45M
4C1682–25C	7C172A–25C
4C1682–35C	7C172A–35C
4C1682–35M	7C172A–35M
4C1682–45C	7C172A–45C
4C1682–45M	7C172A–45M
4C169–25C	7C169A–25C
4C169–30C	7C169A–25C
4C169–35C	7C169A–35C
4C169–35M	7C169A–35M
4C169–45M	7C169A–45M
4C187–20C	7C187–20C
4C187–25C	7C187–25C
4C187–25M	7C187A–25M
4C187–35M	7C187A–35M
4C188–20C	7C164–20C
4C188–25C	7C164–25C
4C188–25M	7C164A–25M

PERFORMANCE	CYPRESS
4C188–35C	7C164–35C
4C188–35M	7C164A–35M
4C188–45M	7C164A–45M
4C198–20C	7C166–20C
4C198–25C	7C166–25C
4C198–25M	7C166A–25M
4C198–35C	7C166–35C
4C198–35M	7C166A–35M
4C198–45M	7C166A–45M
4C1981–20C	7C161–20C
4C1981–25C	7C161–25C
4C1981–25M	7C161A–25M
4C1981–35C	7C161–35C
4C1981–35M	7C161A–35M
4C1982–20C	7C162–20C
4C1982–25C	7C162–25C
4C1982–25M	7C162A–25M
4C1982–35C	7C162–35C
4C1982–35M	7C162A–35M
93U422–35C	7C122–15C
93U422–35C	7C122–25C
93U422–35C	7C122–35C
93U422–35M	7C122–25M
93U422–35M	7C122–35M

PHILIPS-SIGNETICS	CYPRESS
SUFFIX: G	SUFFIX: L
SUFFIX: N	SUFFIX: P
SUFFIX: R	SUFFIX: F
SUFFIX: F	SUFFIX: W
SUFFIX: A	SUFFIX: J
27C256–12	27C256–120C+
27C256–15	27C256–150C+
27C256–17	27C256–150C+
27C256–20	27C256–200C+
27C256–90	27C256–90C+
27HC641–45C	7C263/4–45C
27HC641–55C	7C263/4–55C
N74S189	74S189C
N82HS321	7C243/4–45C
N82HS321A	7C243/4–35C
N82HS321B	7C243/4–30C
N82HS321C	7C243/4–25C
N82HS641	7C263/4–55C
N82HS641A	7C263/4–45C
N82HS641B	7C263/4–35C
N82HS641C	7C263/4–25C
N82LHS191–3	7C291A–35C
N82LHS191–6	7C292A–35C
N82S181	7C281/2A–45C
N82S181A	7C281/2A–45C
N82S181C	7C281/2A–30C
N82S191–3	7C291A–50C
N82S191–6	7C292A–50C
N82S191A–3	7C291A–50C
N82S191A–6	7C292A–50C
N82S191C–3	7C291A–35C
N82S191C–6	7C292A–35C
S82HS641	7C263/4–55M
S82LS181	7C282A–45M
S82S181	7C282A–45M
S82S181A	7C282A–45M

PHILIPS-SIGNETICS	CYPRESS
S82S191–3	7C291A–50M
S82S191–6	7C292A–50M
S82S191A–3	7C291A–50M
S82S191A–6	7C292A–50M
S82S191B–3	7C291A–50M
S82S191B–6	7C292A–50M

QUICKLOGIC	CYPRESS
PREFIX: QL	PREFIX: CY
8X12B–*CG68M	7C382A–*GMB
8X12B–*PF100C	7C382A–*AC
8X12B–*PF100I	7C382A–*AI
8X12B–*PL44C	7C381A–*JC
8X12B–*PL44I	7C381A–*JI
8X12B–*PL68C	7C382A–*JC
8X12B–*PL68I	7C382A–*JI
8X12BL–*PF100C	7C3382A–*AC
8X12BL–*PF100I	7C3382A–*AI
8X12BL–*PL44C	7C3381A–*JC
8X12BL–*PL44I	7C3381A–*JI
8X12BL–*PL68C	7C3382A–*JC
8X12BL–*PL68I	7C3382A–*JI
12X16B–*CG84M	7C384A–*GMB
12X16B–*PF100C	7C384A–*AC
12X16B–*PF100I	7C384A–*AI
12X16B–*PL68C	7C383A–*JC
12X16B–*PL68I	7C383A–*JI
12X16B–*PL84C	7C384A–*JC
12X16B–*PL84I	7C384A–*JI
12X16BL–*PF100C	7C3384A–*AC
12X16BL–*PF100I	7C3384A–*AI
12X16BL–*PL68C	7C3383A–*JC
12X16BL–*PL68I	7C3383A–*JI
12X16BL–*PL84C	7C3384A–*JC
12X16BL–*PL84I	7C3384A–*JI
16X24B–*GC144M	7C386A–*GMB
16X24B–*PF100C	7C385A–*AC
16X24B–*PF100I	7C385A–*AI
16X24B–*PF144C	7C386A–*AC
16X24B–*PF144I	7C386A–*AI
16X24B–*PL84C	7C385A–*JC
16X24B–*PL84I	7C385A–*JI
16X24B–*CF160M	7C386A–*UMB
16X24BL–*PF100C	7C3385A–*AC
16X24BL–*PF100I	7C3385A–*AI
16X24BL–*PF144C	7C3386A–*AC
16X24BL–*PF144I	7C3386A–*AI
16X24BL–*PL84C	7C3385A–*JC
16X24BL–*PL84I	7C3385A–*JI
24X32B–*GC223M	7C388A–*GMB
24X32B–*PF144C	7C387A–*AC
24X32B–*PF144I	7C387A–*AI
24X32B–*PF208C	7C388A–*AC
24X32B–*PF208I	7C388A–*AI
24X32BL–*PF144C	7C3387A–*AC
24X32BL–*PF144I	7C3387A–*AI
24X32BL–*PF208C	7C3388A–*NC
24X32BL–*PF208I	7C3388A–*NI

SAMSUNG	CYPRESS
PREFIX: KM	PREFIX: CY
18V87–8	7C1031–8.5
61257A–25	7C197–25C
61257A–35	7C197–35C
61257A–45	7C197–45C
64257A–25	7C194–25C
64257A–35	7C194–35C
64257A–45	7C194–45C
64258B–15	7C194–15C
64258B–20	7C194–20C
64259B–15	7C196–15C
64259B–20	7C196–20C
641001–20	7C106A–20C
681001–20	7C109A–20C
681002–15	7C1009–15C
681002–20	7C1009–20C
68257–12	7C199–12C
68257–15	7C199–15C
718B514–8	7C178–8.5
75C01A–15	7C421–15
75C01A–20	7C421–20C
75C01A–25	7C421–25C
75C01A–35	7C421–30C
75C01A–50	7C421–40C
75C01A–80	7C421–65C
75C01AP–20	7C420–20C
75C01AP–25	7C420–25C
75C01AP–35	7C420–35C
75C01AP–50	7C420–50C
75C01AP–80	7C420–80C
75C02A–15	7C425–15
75C02A–20	7C425–20C
75C02A–25	7C425–25C
75C02A–35	7C425–30C
75C02A–50	7C425–40C
75C02A–80	7C425–65C
75C02AP–20	7C424–20C
75C02AP–25	7C424–25C
75C02AP–35	7C424–30C
75C02AP–50	7C424–40C
75C02AP–80	7C424–65C
75C03A–15	7C429–15C
75C03A–20	7C429–20C
75C03A–25	7C429–25C
75C03A–35	7C429–30C
75C03A–50	7C429–40C
75C03A–80	7C429–65C
75C03AP–20	7C428–20C
75C03AP–25	7C428–25C
75C03AP–35	7C428–30C
75C03AP–50	7C428–40C
75C03AP–80	7C428–65C
75C102A–20	7C425–20C
75C102A–25	7C425–25C
75C102A–35	7C425–25C
75C102A–80	7C425–65C

SGS-THOMSON	CYPRESS
PREFIX: M	PREFIX: CY
SUFFIX: F1	SUFFIX: W
SUFFIX: B1	SUFFIX: P
SUFFIX: C1	SUFFIX: J
SUFFIX: N1	SUFFIX: Z

SGS-THOMSON	CYPRESS
27256–150	27C256–150C
27256–170	27C256–150C
27256–200	27C256–200C
27C64A–12	27C64–120C
27C64A–15	27C64–150C
27C64A–20	27C64–200C
27C64A–25	27C64–200C
27C64A–30	27C64–200C
27C128A–12	27C128–120C+
27C128A–15	27C128–150C+
27C128A–20	27C128–200C+
27C256B–80	27C256–70C+
27C256B–90	27C256–90C+
27C256B–100	27C256–90C+
27C256B–120	27C256–120C+
27C512–10	27C512–90C
27C512–12	27C512–120C
27C512–15	27C512–150C
27C512–20	27C512–200C
27C512–25	27C512–200C
27C512–80	27H512–70C
27C512–90	27C512–90C
27C1001–60X	27H010–55C
27C1001–70	27C010–70C
27C1001–90	27C010–90C
27C1001–120	27C010–120C
27C1001–150	27C010–150C
27C1001–200	27C010–200C

SHARP	CYPRESS
PREFIX: LH	PREFIX: CY
52251–35	7C197–35C
52251–45	7C197–45C
52252–35	7C194–35C
52252–45	7C194–45C
52254D–25	7C199–25C
52254D–35	7C199–35C
52254D–45	7C199–45C
52259	7C188
5481–15	7C408A–15C
5481–25	7C408A–25C
5481–35	7C408A–35C
5491–15	7C409A–15C
5491–25	7C409A–25C
5491–35	7C409A–35C
5496–20	7C420–20C
5496–35	7C420–30C
5496–50	7C420–40C
5496D–15	7C421A–15
5496D–20	7C421–20C
5496D–35	7C421–30C
5496D–50	7C421–40C
5497–20	7C424–20C
5497–35	7C424–30C
5497–50	7C424–40C
5497D–15	7C425A–15
5497D–20	7C425–20C
5497D–35	7C425–30C
5497D–50	7C425–40C

SONY	CYPRESS
PREFIX: CXK	PREFIX: CY
51256P–35	7C197–35
51256P–45	7C197–45
55464–20	7C194–20C
55464–25	7C194–25C
58258A–15	7C199–15C
58258A–20	7C199–20C
58258A–25	7C199–25C
59288–20C	7C188–20C
59288–25C	7C188–25C

TI	CYPRESS
PREFIX: JBP	PREFIX: CY
PREFIX: PAL	SUFFIX: P
PREFIX: SM	PREFIX: CY
PREFIX: SMJ	PREFIX: CY
PREFIX: SN	PREFIX: CY
PREFIX: TBP	PREFIX: CY
PREFIX: TIB	PREFIX: CY
PREFIX: TMS	PREFIX: CY
SUFFIX: FM	SUFFIX: J
SUFFIX: J	SUFFIX: W
SUFFIX: N	SUFFIX: P
SUFFIX: DD	SUFFIX: Z
SUFFIX: N	SUFFIX: P
22V10AC	PALC22V10–25C
22V10AM	PALC22V10–30M
27C010–120	27C010–120C
27C010–150	27C010–150C
27C010–200	27C010–200C
27C128–12	27C128–120
27C512–100	27C512–90C
27C512–120	27C512–120C
27C512–150	27C512–150C
27C512–200	27C512–200C
27C/PC128–15	27C128–150
27C/PC128–20	27C128–200
27C256–10	27C256–90C+
27C256–12	27C256–120C+
27C256–15	27C256–150C+
27C256–17	27C256–150C+
27C256–20	27C256–200C+
27PC010–120	27PC010–120C
27PC010–150	27PC010–150C
27PC010–200	27PC010–200C
27PC256–10	27C256–90C+
27PC256–12	27C256–120C+
27PC256–15	27C256–150C+
27PC256–17	27C256–150C+
27PC256–20	27C256–200C+
27PC512–100	27PC512–90C
27PC512–120	27PC512–120C
27PC512–150	27PC512–150C
27PC512–200	27PC512–200C
PAL16L8–5C	PAL16L8–5C
PAL16L8–7C	PAL16L8–7C
PAL16L8–7M	PAL16L8–7M
PAL16L8–10C	PAL16L8–7C
PAL16L8–10M	PAL16L8–10M
PAL16L8–12M	PAL16L8–10M
PAL16L8–15C	PAL16L8–7C
PAL16L8–15M	PAL16L8–10M
PAL16L8–20M	PALC16L8–20M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

\+ = meets all performance specs but may not meet I_{CC} or I_{SB}

* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}

– = functionally equivalent

† = SOIC only

‡ = 32-pin LCC crosses to the 7C198M

** = See Austin Semiconductor for military products

TI	CYPRESS
PAL16L8-25C	PALC16L8-25C
PAL16L8-30M	PALC16L8-30M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16R4-5C	PAL16R4-5C
PAL16R4-7C	PAL16R4-7C
PAL16R4-7M	PAL16R4-7M
PAL16R4-10C	PAL16R4-7C
PAL16R4-10M	PAL16R4-10M
PAL16R4-12M	PAL16R4-10M
PAL16R4-15C	PAL16R4-7C
PAL16R4-15M	PAL16R4-10M
PAL16R4-20M	PALC16R4-20M
PAL16R4-25C	PALC16R4-25C
PAL16R4-30M	PALC16R4-30M
PAL16R4A-2C	PALC16R4-25C
PAL16R4A-2M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R6-5C	PAL16R6-5C
PAL16R6-7C	PAL16R6-7C
PAL16R6-7M	PAL16R6-7M
PAL16R6-10C	PAL16R6-7C
PAL16R6-10M	PAL16R6-10M
PAL16R6-12M	PAL16R6-10M
PAL16R6-15C	PAL16R6-7C
PAL16R6-15M	PAL16R6-10M
PAL16R6-20M	PALC16R6-20M
PAL16R6-25C	PALC16R6-25C
PAL16R6-30M	PALC16R6-30M
PAL16R6A-2C	PALC16R6-25C
PAL16R6A-2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R8-5C	PAL16R8-5C
PAL16R8-7C	PAL16R8-7C
PAL16R8-7M	PAL16R8-7M
PAL16R8-10C	PAL16R8-7C
PAL16R8-10M	PAL16R8-10M
PAL16R8-12M	PAL16R8-10M
PAL16R8-15C	PAL16R8-7C
PAL16R8-15M	PAL16R8-10M
PAL16R8-20M	PALC16R8-20M
PAL16R8-25C	PALC16R8-25C
PAL16R8-30M	PALC16R8-30M
PAL16R8A-2C	PALC16R8-25C
PAL16R8A-2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL20L8A-2C	PLDC20G10-25C
PAL20L8A-2M	PLDC20G10-30M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L10A-2C	PLDC20G10-25C
PAL20L10A-2M	PLDC20G10-30M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20R4A-2C	PLDC20G10-25C
PAL20R4A-2M	PLDC20G10-30M
PAL20R4AC	PLDC20G10-25C

TI	CYPRESS
PAL20R4AM	PLDC20G10-30M
PAL20R6A-2C	PLDC20G10-25C
PAL20R6A-2M	PLDC20G10-30M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R8A-2C	PLDC20G10-25C
PAL20R8A-2M	PLDC20G10-30M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL22V10-7C	PALC22V10D-7C
PAL22V10-7C	PAL22V10C-7C
PAL22V10-15C	PALC22V10B-15C
PAL22V10-20M	PALC22V10B-20M
PAL22V10AC	PALC22V10-25C
PAL22V10AC	PALC22V10L-25C
PAL22V10AM	PALC22V10-25MB
PAL22V10AM	PALC22V10-30MB
PAL22V10C	PALC22V10-35C
PAL22V10C	PALC22V10L-35C
SN74ACT7201LA15	7C421-15
SN74ACT7201LA25	7C421-25
SN74ACT7202LA15	7C425-15
SN74ACT7202LA25	7C425-25
SN74ACT7203L15	7C429-15
SN74ACT7203L25	7C429-25
SN74ACT7204L15	7C433-15
SN74ACT7204L25	7C433-25

TOSHIBA	CYPRESS
PREFIX: P	SUFFIX: P
PREFIX: TC	PREFIX: CY
PREFIX: TMM	PREFIX: CY
SUFFIX: D	SUFFIX: D
2015A	7C128A-55C+
2018-25	7C128A-25C
2018-35	7C128A-35C
2018-45	7C128A-45C
2018-55	7C128A-55C+
2018AP-35	7C128A-35C
2018AP-45	7C128A-45C
2068-25	7C168A-25C
2068-35	7C168A-35C
2068-45	7C168A-45C
2068-55	7C168A-45C
2069-35	7C169A-35C
2078-35	7C170A-35C
2078-45	7C170A-45C
2078-55	7C170A-45C
2088-35	7C186-35C
315	2147-55C
55257-10	7C199-55C
55257-70	7C199-55C
55257-85	7C199-55C
55328-15	7C199-15C
55328-20	7C199-20C
55328-25	7C199-25C
55328-35	7C199-35C
55328-25	7C199-25C
55328-35	7C199-35C
55329P/J	7C188
55399-20	7C188-20C
55399-25	7C188-25C
55416-35	7C164-35C

TOSHIBA	CYPRESS
55417-25	7C166-25C
55417-35	7C166-35C
55417P/J-15	7C166-15C
55417P/J-20	7C166-20C
55417P/J-25	7C166-25C
55417P/J-35	7C166-35C
55464-12	7C194-12C
55464-15	7C194-15C
55464-20	7C194-20C
55464-25	7C194-25C
55464-35	7C194-35C
55464-25	7C194-25C
55464-35	7C194-35C
55465-12	7C196-12C
55465-15	7C196-15C
55465-20	7C196-20C
55465-25	7C196-25C
55465-25	7C195-25C
55465-35	7C196-35C
55465-35	7C195-35C
5561P/J	7C187-C
5562	7C187-C
5563	7C185-C
5588P/J	7C185-C
5589P/J-25	7C182-25C
55B328-12	7C199-12C
55B328-15	7C199-15C
55B464-12	7C194-12C
55B465-12	7C196-12C
57C256A-120	27C256-120C+
57C256A-150	27C256-150C+
57C256A-200	27C256-200C+

WSI	CYPRESS
PREFIX: WS	PREFIX: CY
SUFFIX: C	SUFFIX: Q
SUFFIX: D/T	SUFFIX: W
SUFFIX: P/S	SUFFIX: P
57C43C-55C	7C243/4-55C
57C43C-45C	7C243/4-45C
57C43C-35C	7C243/4-35C
57C43C-25C	7C243/4-25C
57C45-25	7C245A-25C
57C45-25M	7C245A-25M
57C45-35	7C245A-35C
57C45-35M	7C245A-35M
57C45-45	7C245A-45C
57C45-45M	7C245A-45M
57C49B-35	7C263/4-35C
57C49B-45	7C263/4-45C
57C49B-45M	7C263/4-45C
57C49B-55	7C263/4-55C
57C49B-55M	7C263/4-55C
57C49B-70	7C263/4-55C
57C49B-70M	7C263/4-55C
57C49C-25	7C263/4-25C
57C49C-35	7C263/4-35C
57C49C-45	7C263/4-45C
57C49C-45M	7C263/4-45C
57C49C-55	7C263/4-55C
57C49C-55M	7C263/4-55C
57C49C-70	7C263/4-55C
57C49C-70M	7C263/4-55C

WSI	CYPRESS
57C64F–55	7C266–55C
57C51C–45	7C251/4–45C
57C51C–45M	7C251/4–45M
57C51C–55	7C251/4–55C
57C51C–55M	7C251/4–55M
57C51C–70	7C251/4–55M
57C51C–70M	7C251/4–55M
57C71C–35	7C271A–35C
57C71C–45	7C271A–45C
57C71C–55	7C271A–55C
57C71C–55M	7C271A–55M
57C71C–70	7C271A–55M
57C71C–70M	7C271A–55M
57C128F–55C	27C128–55C+
57C128F–70C	27C128–70C+
57C128FB–45	27C128–45C
57C128FB–55	27C128–55C
57C128FB–70	27C128–70C
57C191B–35	7C292A–35C
57C191B–35M	7C292A–35M
57C191B–45	7C292A–35C
57C191B–45M	7C292A–35M
57C191B–50M	7C292A–50M
57C191B–55	7C292A–50C
57C191B–55M	7C292A–50M
57C191C–25	7C292A–25C
57C191C–35	7C292A–35C
57C191C–45	7C292A–35C
57C191C–45M	7C292A–35M
57C191C–55	7C292A–50C
57C191C–55M	7C292A–50M
57C256F–35	27H256–35C
57C256F–45	27C256–45C+
57C256F–55	27C256–55C+
57C256F–55M	27C256–55M
57C256F–70	27C256–70C+
57C256F–70M	27C256–70M
57C256F–90	27C256–90C+
57C291B–35	7C291A–35C
57C291B–35M	7C291A–35M
57C291B–45	7C291A–35C
57C291B–45M	7C291A–35M
57C291B–50M	7C291A–50M
57C291B–55	7C291A–50C
57C291B–55M	7C291A–50M
57C291C–25	7C291A–25C
57C291C–35	7C291A–35C
57C291C–45	7C291A–35C
57C291C–45M	7C291A–35M
57C291C–55	7C291A–50C
57C291C–55M	7C291A–50M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

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– = functionally equivalent
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M
** = See Austin Semiconductor for military products

FCT Commercial Cross Reference

CYPRESS		IDT		PERICOM		QUALITY	
CY29FCT52	A, B, C	IDT29FCT52	A, B, C, D	PI74FCT2952	A, B, C	QS29FCT52	A, B, C
CY29FCT520	A, B, C	IDT29FCT520	A, B, C, D			QS29FCT520	A, B, C
CY29FCT818	Std, A, B, C						
CY74FCT138	Std, A, C	IDT74FCT138	Std, A, C	PI74FCT138	Std, A, C	QS74FCT138	Std, A, C, D
CY74FCT157	Std, A, C	IDT74FCT157	Std, A, C, D	PI74FCT157	Std, A, C	QS74FCT157	Std, A, C
CY74FCT158	Std, A, C					QS74FCT158	Std, A, C
CY74FCT163	Std, A, C	IDT74FCT163	Std, A, C			QS74FCT163	Std, A, C, D
CY74FCT191	Std, A, C	IDT74FCT191	Std, A			QS74FCT191	Std, A, C
CY74FCT2240	Std, A, C	IDT74FCT2240	Std, A, C, D	PI74FCT2240	Std, A, C	QS74FCT2240	Std, A, C
CY74FCT2244	Std, A, C, D	IDT74FCT2244	Std, A, C, D	PI74FCT2244	Std, A, C	QS74FCT2244	Std, A, C
CY74FCT2245	Std, A, C, D	IDT74FCT2245	Std, A, C, D	PI74FCT2245	Std, A, C	QS74FCT2245	Std, A, C, D
CY74FCT2257	Std, A, C			PI74FCT2257	Std, A, C	QS74FCT2257	Std, A, C
CY74FCT2373	Std, A, C, D	IDT74FCT2373	Std, A, C, D	PI74FCT2373	Std, A, C	QS74FCT2373	Std, A, C, D
CY74FCT2374	Std, A, C, D	IDT74FCT2374	Std, A, C, D	PI74FCT2374	Std, A, C	QS74FCT2374	Std, A, C, D
CY74FCT240	Std, A, C, D	IDT74FCT240	Std, A, C, D	PI74FCT240	Std, A, C, D	QS74FCT240	Std, A, C, D
CY74FCT244	Std, A, C, D	IDT74FCT244	Std, A, C, D	PI74FCT244	Std, A, C, D	QS74FCT244	Std, A, C, D
CY74FCT245	Std, A, C, D	IDT74FCT245	Std, A, C, D	PI74FCT245	Std, A, C, D	QS74FCT245	Std, A, C, D
CY74FCT2541	Std, A, C,			PI74FCT2541	Std, A, C,	QS74FCT2541	Std, A, C,
CY74FCT2543	Std, A, C, D	IDT74FCT2543	Std, A, C, D	PI74FCT2543	Std, A, C	QS74FCT2543	Std, A, C, D
CY74FCT257	Std, A, C	IDT74FCT257	Std, A, C	PI74FCT257	Std, A, C	QS74FCT257	Std, A, C
CY74FCT2573	Std, A, C, D	IDT74FCT2573	Std, A, C, D	PI74FCT2573	Std, A, C, D	QS74FCT2573	Std, A, C
CY74FCT2574	Std, A, C, D	IDT74FCT2574	Std, A, C, D	PI74FCT2574	Std, A, C	QS74FCT2574	Std, A, C, D
CY74FCT2646	Std, A, C	IDT74FCT2646	Std, A, C, D	PI74FCT2646	Std, A, C	QS74FCT2646	Std, A, C, D
CY74FCT2648	Std, A, C	IDT74FCT2648	Std, A, C			QS74FCT2648	Std, A, C
CY74FCT2652	Std, A, C, D	IDT74FCT2652	Std, A, C, D	PI74FCT2652	Std, A, C, D	QS74FCT2652	Std, A, C, D
CY74FCT273	Std, A, C	IDT74FCT273	Std, A, C	PI74FCT273	Std, A, C	QS74FCT273	Std, A, C
CY74FCT2827	A, B, C	IDT74FCT2827	A, B, C	PI74FCT2827	A, B, C	QS74FCT2827	A, B, C
CY74FCT373	Std, A, C, D	IDT74FCT373	Std, A, C, D	PI74FCT373	Std, A, C, D	QS74FCT373	Std, A, C, D
CY74FCT374	Std, A, C, D	IDT74FCT374	Std, A, C, D	PI74FCT374	Std, A, C, D	QS74FCT374	Std, A, C, D
CY74FCT377	Std, A, C	IDT74FCT377	Std, A, C, D	PI74FCT377	Std, A, C, D	QS74FCT377	Std, A, C
CY74FCT399	Std, A, C	IDT74FCT399	Std, A, C	PI74FCT399	Std, A, C		
CY74FCT480	Std, A, B						
CY74FCT540	Std, A, C, D	IDT74FCT540	Std, A, C	PI74FCT540	Std, A, C, D	QS74FCT540	Std, A, C, D
CY74FCT541	Std, A, C, D	IDT74FCT541	Std, A, C	PI74FCT541	Std, A, C, D	QS74FCT541	Std, A, C, D
CY74FCT543	Std, A, C, D	IDT74FCT543	Std, A, C, D	PI74FCT543	Std, A, C, D	QS74FCT543	Std, A, C, D
CY74FCT573	Std, A, C, D	IDT74FCT573	Std, A, C, D	PI74FCT573	Std, A, C, D	QS74FCT573	Std, A, C
CY74FCT574	Std, A, C, D	IDT74FCT574	Std, A, C, D	PI74FCT574	Std, A, C, D	QS74FCT574	Std, A, C, D
CY74FCT646	Std, A, C, D	IDT74FCT646	Std, A, C, D	PI74FCT646	Std, A, C, D	QS74FCT646	Std, A, C
CY74FCT648	Std, A, C	IDT74FCT648	Std, A, C	PI74FCT648	Std, A, C, D	QS74FCT648	Std, A, C, D
CY74FCT652	Std, A, C, D	IDT74FCT652	Std, A, B, D	PI74FCT652	Std, A, C, D	QS74FCT652	Std, A, B, D
CY74FCT821	A, B, C	IDT74FCT821	A, B, C, D	PI74FCT821	A, B, C, D	QS74FCT821	A, B, C, D
CY74FCT823	A, B, C	IDT74FCT823	A, B, C, D	PI74FCT823	A, B, C, D	QS74FCT823	A, B, C, D
CY74FCT825	A, B, C	IDT74FCT825	A, B, C	PI74FCT825	A, B, C, D	QS74FCT825	A, B, C
CY74FCT827	A, B, C	IDT74FCT827	A, B, C	PI74FCT827	A, B, C, D	QS74FCT827	A, B, C
CY74FCT841	A, B, C	IDT74FCT841	A, B, C, D	PI74FCT841	A, B, C, D	QS74FCT841	A, B, C
CYBUS3384				PI5C3384		QS3384	

Package	Code	Package	Code	Package	Code	Package	Code
Plastic DIP	P	Plastic DIP	P	Plastic DIP	P	Plastic DIP	P
QSOP	Q	QSOP	Q	QSOP	Q	QSOP	Q
SOIC	SO	SOIC	SO	SOIC	SO	SOIC	SO

FCT Commercial Cross Reference (continued)

CYPRESS	TI
CY74FCT52C	74ABT2952A
CY74FCT2240A	SN74ABT2240
CY74FCT2244A	SN74ABT2244
CY74FCT2245A	SN74ABT2245
CY74FCT240A	SN74ABT240
CY74FCT244A	SN74ABT244
CY74FCT245A	SN74ABT245
CY74FCT273A	SN74ABT273
CY74FCT373A	SN74ABT373
CY74FCT374A	SN74ABT374
CY74FCT377A	SN74ABT377
CY74FCT540A	SN74ABT540
CY74FCT541A	SN74ABT541
CY74FCT543A	SN74ABT543
CY74FCT573A	SN74ABT573
CY74FCT574A	SN74ABT574
CY74FCT646A	SN74ABT646
CY74FCT646C	SN74ABT646A
CY74FCT652A	SN74ABT652
CY74FCT652C	SN74ABT652A
CY74FCT821C	SN74ABT821
CY74FCT827C	SN74ABT827
CY74FCT841C	SN74ABT841
CYBUS3384	SN74CBT3384

Package		Code
Plastic DIP	P	N
SOIC	SO	DW

FCT Military Cross Reference

CYPRESS		IDT		QUALITY	
CY29FCT52	A, B, C	IDT29FCT52	A, B, C	QS29FCT52	A, B, C
CY29FCT520	A, B, C	IDT29FCT520	A, B, C	QS29FCT520	A, B, C
CY29FCT818	Std, A, B, C				
CY54FCT138	Std, A, C	IDT54FCT138	Std, A, C	QS54FCT138	Std, A, C
CY54FCT157	Std, A, C	IDT54FCT157	Std, A, C	QS54FCT157	Std, A, C
CY54FCT158	Std, A, C			QS54FCT158	Std, A, C
CY54FCT163	Std, A, C	IDT54FCT163	Std, A, C	QS54FCT163	Std, A, C
CY54FCT191	Std, A, C	IDT54FCT191	Std, A	QS54FCT191	Std, A, C
CY54FCT2240	Std, A, C	IDT54FCT2240	Std, A, C	QS54FCT2240	Std, A
CY54FCT2244	Std, A, C	IDT54FCT2244	Std, A, C	QS54FCT2244	Std, A
CY54FCT2245	Std, A, C	IDT54FCT2245	Std, A, C	QS54FCT2245	Std, A
CY54FCT2257	Std, A, C			QS54FCT2257	Std, A, C
CY54FCT2373	Std, A, C	IDT54FCT2373	Std, A, C	QS54FCT2373	Std, A
CY54FCT2374	Std, A, C	IDT54FCT2374	Std, A, C	QS54FCT2374	Std, A
CY54FCT240	Std, A, C	IDT54FCT240	Std, A, C	QS54FCT240	Std, A, C
CY54FCT244	Std, A, C	IDT54FCT244	Std, A, C	QS54FCT244	Std, A
CY54FCT245	Std, A, C	IDT54FCT245	Std, A, C	QS54FCT245	Std, A
CY54FCT2541	Std, A, C			QS54FCT2541	Std, A
CY54FCT2543	Std, A, C	IDT54FCT2543	Std, A, C	QS54FCT2543	Std, A, C, D
CY54FCT257	Std, A, C	IDT54FCT257	Std, A, C	QS54FCT257	Std, A, C, D
CY54FCT2573	Std, A, C	IDT54FCT2573	Std, A, C	QS54FCT2573	Std, A
CY54FCT2574	Std, A, C	IDT54FCT2574	Std, A, C	QS54FCT2574	Std, A, C
CY54FCT2646	Std, A, C	IDT54FCT2646	Std, A, C	QS54FCT2646	Std, A, C
CY54FCT2648	Std, A, C	IDT54FCT2648	Std, A, C	QS54FCT2648	Std, A, C
CY54FCT2652	Std, A, C	IDT54FCT2652	Std, A, C	QS54FCT2652	Std, A, C, D
CY54FCT273	Std, A, C	IDT54FCT273	Std, A, C	QS54FCT273	Std, A
CY54FCT2827	A, B, C	IDT54FCT2827	A, B, C	QS54FCT2827	A, B
CY54FCT373	Std, A, C	IDT54FCT373	Std, A, C	QS54FCT373	Std, A
CY54FCT374	Std, A, C	IDT54FCT374	Std, A, C	QS54FCT374	Std, A, C
CY54FCT377	Std, A, C	IDT54FCT377	Std, A, C	QS54FCT377	Std, A
CY54FCT399	Std, A, C	IDT54FCT399	Std, A, C		
CY54FCT480	Std, A, B				
CY54FCT540	Std, A, C	IDT54FCT540	Std, A, C	QS54FCT540	Std, A, C, D
CY54FCT541	Std, A, C	IDT54FCT541	Std, A, C	QS54FCT541	Std, A, C, D
CY54FCT543	Std, A, C	IDT54FCT543	Std, A, C	QS54FCT543	Std, A
CY54FCT573	Std, A, C	IDT54FCT573	Std, A, C	QS54FCT573	Std, A
CY54FCT574	Std, A, C	IDT54FCT574	Std, A, C	QS54FCT574	Std, A, C
CY54FCT646	Std, A, C	IDT54FCT646	Std, A, C	QS54FCT646	Std, A, C
CY54FCT648	Std, A, C	IDT54FCT648	Std, A, C	QS54FCT648	Std, A, C
CY54FCT652	Std, A, C	IDT54FCT652	Std, A, C	QS54FCT652	Std, A, C, D
CY54FCT652	Std, A, C				
CY54FCT821	A, B, C	IDT54FCT821	A, B, C	QS54FCT821	A, B, C
CY54FCT823	A, B, C	IDT54FCT823	A, B, C	QS54FCT823	A, B, C
CY54FCT825	A, B, C	IDT54FCT825	A, B, C	QS54FCT825	A, B, C
CY54FCT827	A, B, C	IDT54FCT827	A, B, C	QS54FCT827	A
CY54FCT841	A, B, C	IDT54FCT841	A, B, C	QS54FCT841	A, B, C

Package	Code	Package	Code	Package	Code
CERDIP	D	CERDIP	D	CERDIP	
LCC	L	LCC	L	LCC	L
HQSOP		HQSOP		HQSOP	H

Commercial Cross Reference

CYPRESS		IDT		PERICOM	
CY74FCT16240	Std, A, C	IDT74FCT16240	Std, A, C, E	PI74FCT16240	Std, A, C, D
CY74FCT16244	Std, A, C	IDT74FCT16244	Std, A, C, E	PI74FCT16244	Std, A, C, D
CY74FCT16245	Std, A, C	IDT74FCT16245	Std, A, C, E	PI74FCT16245	Std, A, C, D
CY74FCT16373	Std, A, C	IDT74FCT16373	Std, A, C, E	PI74FCT16373	Std, A, C, D
CY74FCT16374	Std, A, C	IDT74FCT16374	Std, A, C, E	PI74FCT16374	Std, A, C, D
CY74FCT16444	Std, A, C				
CY74FCT16445	Std, A, C				
CY74FCT16500	A, C	IDT74FCT16500	A, C, E	PI74FCT16500	A, C, D
CY74FCT16501	A, C	IDT74FCT16501	A, C, E	PI74FCT16501	A, C, D
CY74FCT16543	Std, A, C	IDT74FCT16543	Std, A, C, E	PI74FCT16543	Std, A, C, D
CY74FCT16646	Std, A, C	IDT74FCT16646	Std, A, C, E	PI74FCT16646	Std, A, C, D
CY74FCT16652	Std, A, C	IDT74FCT16652	Std, A, C, E	PI74FCT16652	Std, A, C, D
CY74FCT16823	A, B, C	IDT74FCT16823	A, B, C, E	PI74FCT16823	A, B, C
CY74FCT16827	A, B, C	IDT74FCT16827	A, B, C, E	PI74FCT16827	A, B, C
CY74FCT16841	A, B, C	IDT74FCT16841	A, B, C, E	PI74FCT16841	A, B, C
CY74FCT16952	A, B, C	IDT74FCT16952	A, B, C, E	PI74FCT16952	A, B, C, D
CY74FCT162240	Std, A, C	IDT74FCT162240	Std, A, C, E	PI74FCT162240	Std, A, C, D
CY74FCT162244	Std, A, C	IDT74FCT162244	Std, A, C, E	PI74FCT162244	Std, A, C, D
CY74FCT162245	Std, A, C	IDT74FCT162245	Std, A, C, E	PI74FCT162245	Std, A, C, D
CY74FCT162373	Std, A, C	IDT74FCT162373	Std, A, C, E	PI74FCT162373	Std, A, C, D
CY74FCT162374	Std, A, C	IDT74FCT162374	Std, A, C, E	PI74FCT162374	Std, A, C, D
CY74FCT162444	Std, A, C				
CY74FCT162445	Std, A, C				
CY74FCT162500	A, C	IDT74FCT162500	A, C, E	PI74FCT162500	A, C, D
CY74FCT162501	A, C	IDT74FCT162501	A, C, E	PI74FCT162501	A, C, D
CY74FCT162543	Std, A, C	IDT74FCT162543	Std, A, C, E	PI74FCT162543	Std, A, C, D
CY74FCT162646	Std, A, C	IDT74FCT162646	Std, A, C, E	PI74FCT162646	Std, A, C, D
CY74FCT162652	Std, A, C	IDT74FCT162652	Std, A, C, E	PI74FCT162652	Std, A, C, D
CY74FCT162823	A, B, C	IDT74FCT162823	A, B, C, E	PI74FCT16H823	A, B, C
CY74FCT162827	A, B, C	IDT74FCT162827	A, B, C, E	PI74FCT162827	A, B, C
CY74FCT162841	A, B, C	IDT74FCT162841	A, B, C, E	PI74FCT162841	A, B, C
CY74FCT162952	A, B, C	IDT74FCT162952	A, B, C, E	PI74FCT162952	A, B, C, D
CY74FCT162H952	A, B, C	IDT74FCT162H952	A, B, C, E		
CY74FCT162H501	A, C	IDT74FCT162H501	A, C, E		
CY74FCT162H244	Std, A, C	IDT74FCT162H244	Std, A, C, E		
CY74FCT162H245	Std, A, C	IDT74FCT162H245	Std, A, C, E		
CY74FCT162H373	Std, A, C	IDT74FCT162H373	Std, A, C, E		
Package	**Code**	**Package**	**Code**	**Package**	**Code**
SSOP	PV	SSOP	PV	SSOP	PV
TSSOP	PA	TSSOP	PA	TSSOP	PA

CYPRESS		TEXAS INSTRUMENTS		PHILLIPS	
CY74FCT16240CT		SN74ABT16240			
CY74FCT16244CT		SN74ABT16244A		74ABT16244	
CY74FCT16245CT		SN74ABT16245		74ABT16245	
CY74FCT16373CT		SN74ABT16373A		74ABT16373	
CY74FCT16374CT		SN74ABT16374A		74ABT16374	
CY74FCT16500CT		SN74ABT16500B			
CY74FCT16543CT		SN74ABT16543B		74ABT16543	
CY74FCT162240CT		SN74ABT162240			
CY74FCT162244CT		SN74ABT162244			
CY74FCT162245CT		SN74ABT162245			
CY74FCT162373					
CY74FCT162374					
CY74FCT162500CT		SN74ABT162500			
Package	**Code**	**Package**	**Code**	**Package**	**Code**
SSOP	PV	SSOP	DL	SSOP	PV
TSSOP	PA	TSSOP	DDG	TSSOP	

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Section Contents

Static RAMs (Random Access Memory)

Static RAMs (Random Access Memory) (continued)

8K x 8 Static RAM

Features

- **55, 70 ns access times**
- **CMOS for optimum speed/power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

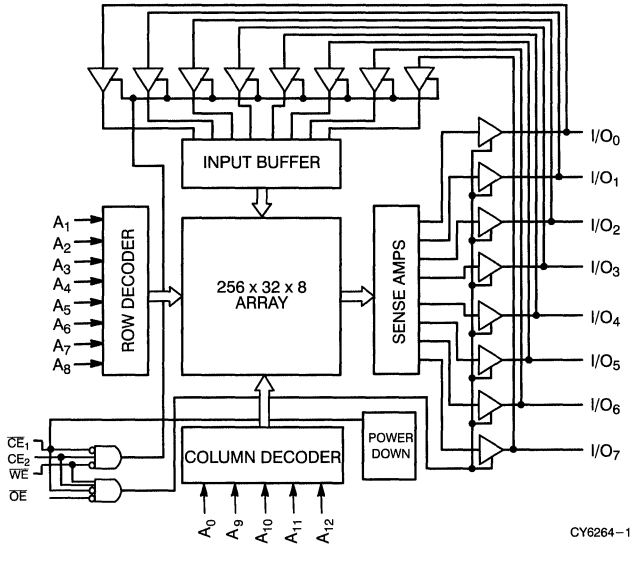
Functional Description

The CY6264 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by over 70% when deselected. The CY6264 is in a 330-mil-wide SOIC.

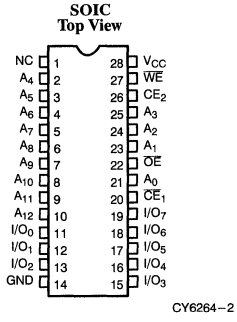
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

	CY6264–55	CY6264–70
Maximum Access Time (ns)	55	70
Maximum Operating Current (mA)	100	100
Maximum Standby Current (mA)	20/15	20/15

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	6264−55		6264−70		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		100		100	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		20		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		15		15	mA

Shaded area contains advanced information.

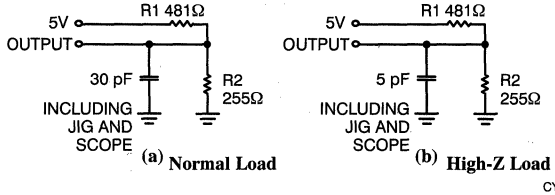
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

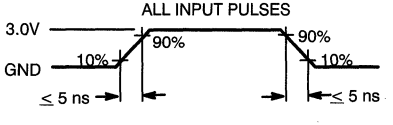
Notes:

1. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

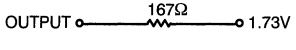


CY6264−3



CY6264−4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

Parameter	Description	6264–55		6264–70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		55		70	ns
t_{ACE2}	CE_2 HIGH to Data Valid		40		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		20		30	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[6]	5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[5, 6] CE_2 LOW to High Z		20		30	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		25		30	ns
WRITE CYCLE[7]						
t_{WC}	Write Cycle Time	50		70		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	40		60		ns
t_{SCE2}	CE_2 HIGH to Write End	30		50		ns
t_{AW}	Address Set-Up to Write End	40		55		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		40		ns
t_{SD}	Data Set-Up to Write End	25		35		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]		20		30	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		ns

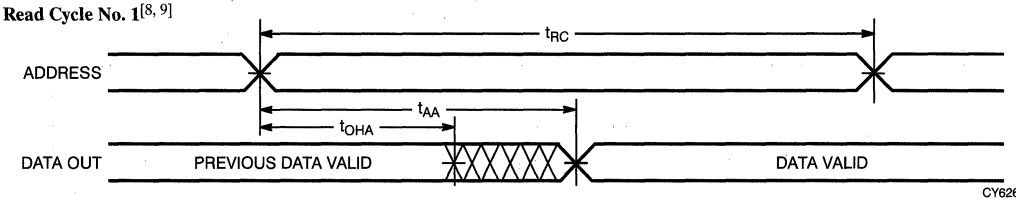
Shaded area contains advanced information.

Notes:

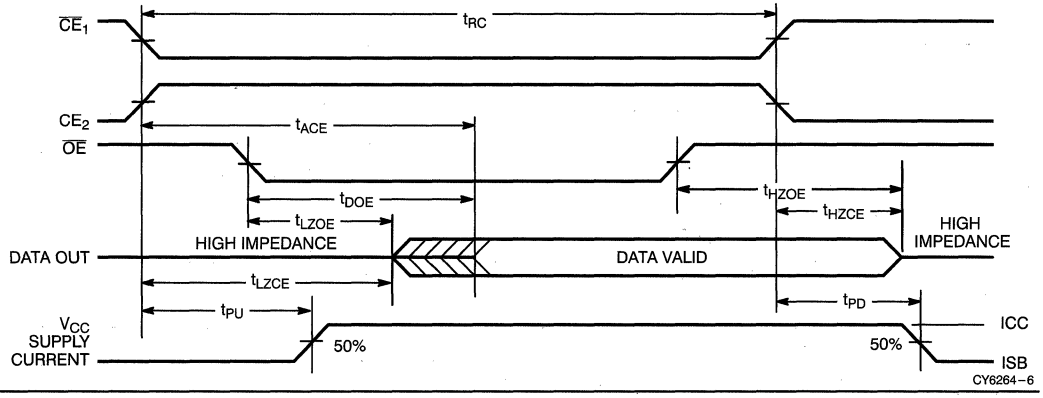
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

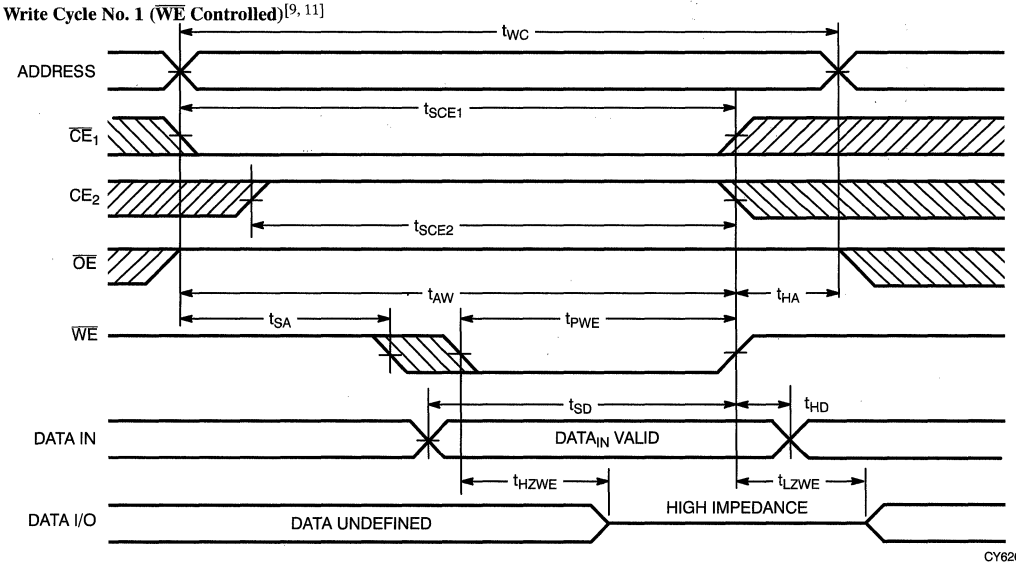
Read Cycle No. 1[8, 9]



Read Cycle No. 2[10, 11]



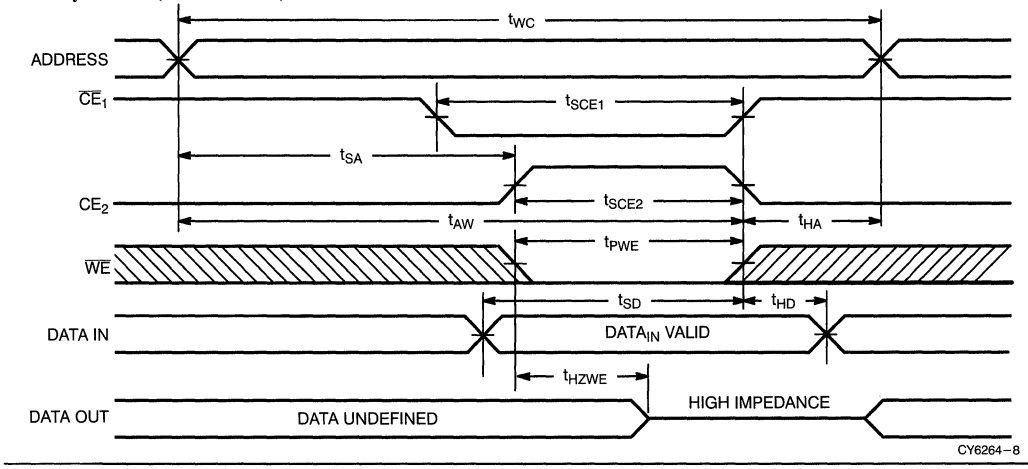
Write Cycle No. 1 (WE Controlled)[9, 11]



Notes:
8. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.
9. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
10. $\overline{WE}$ is HIGH for read cycle.
11. Data I/O is High Z if $\overline{OE}$ = V_{IH}, $\overline{CE_1}$ = V_{IH}, or $\overline{WE}$ = V_{IL}.

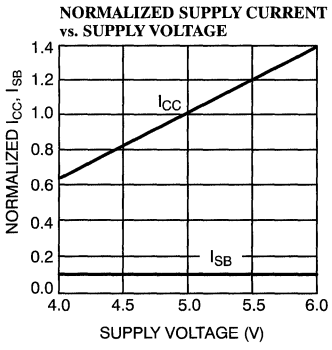
Switching Waveforms (continued)

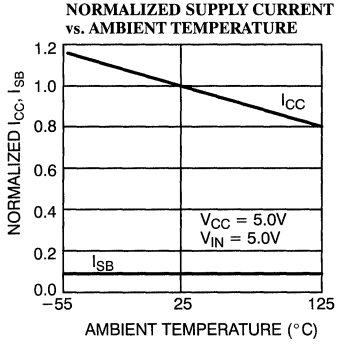
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 11, 12]

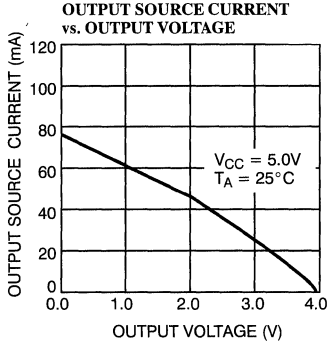


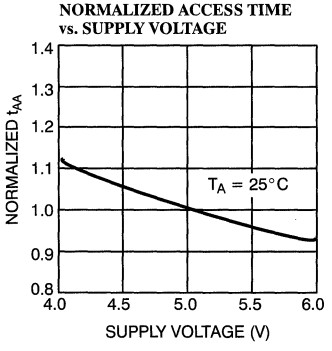
Note:
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

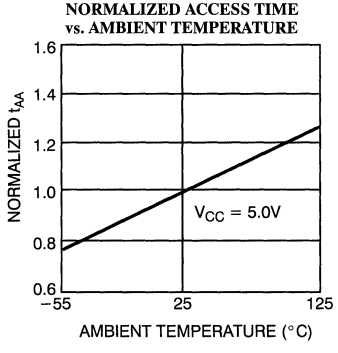
Typical DC and AC Characteristics

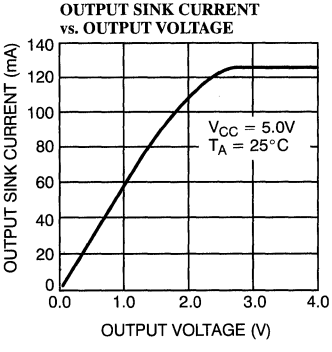






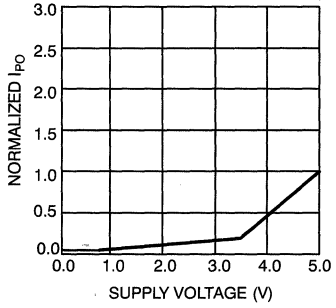




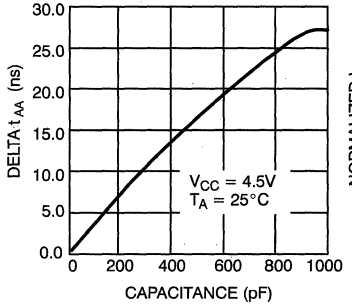


Typical DC and AC Characteristics (continued)

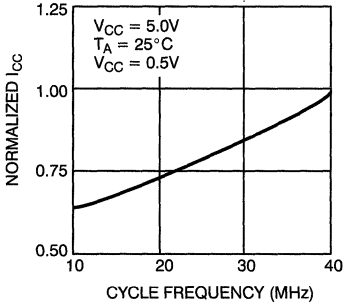
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY6264-55SC	S23	28-Lead 330-Mil SOIC	Commercial
70	CY6264-70SC	S23	28-Lead 330-Mil SOIC	Commercial

Shaded area contains advanced information.

Document #: 38-00425

CY7C101A
CY7C102A

256K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Transparent write (7C101A)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 910 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention (optional)**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C101A and CY7C102A are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

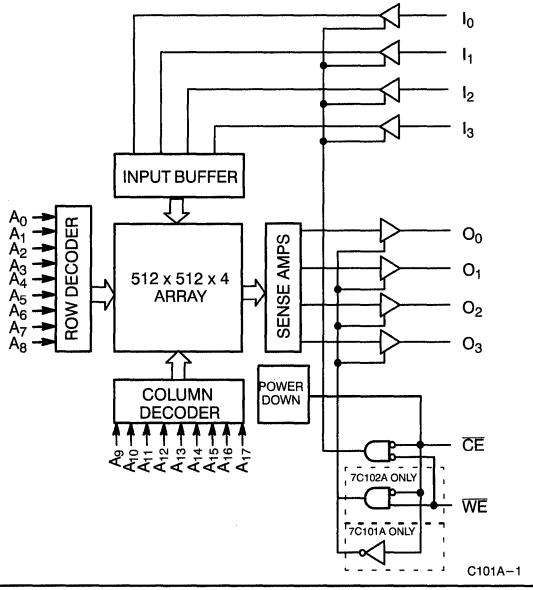
Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

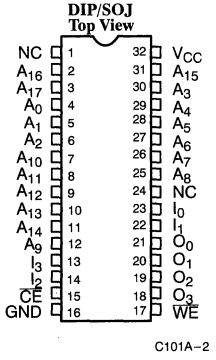
The data output pins on the CY7C101A and the CY7C102A are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C102A's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C101A, the output pins will carry the same data as the inputs after a specified delay.

The CY7C101A and CY7C102A are available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C101A–12 7C102A–12	7C101A–15 7C102A–15	7C101A–20 7C102A–20	7C101A–25 7C102A–25	7C101A–35 7C102A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	165	155	140	130	125
	Military		165	150	140	135
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C101A−12 7C102A−12 Min.	7C101A−12 7C102A−12 Max.	7C101A−15 7C102A−15 Min.	7C101A−15 7C102A−15 Max.	7C101A−20 7C102A−20 Min.	7C101A−20 7C102A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140	mA
			Mil				165		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Electrical Characteristics Over the Operating Range[3] (continued)

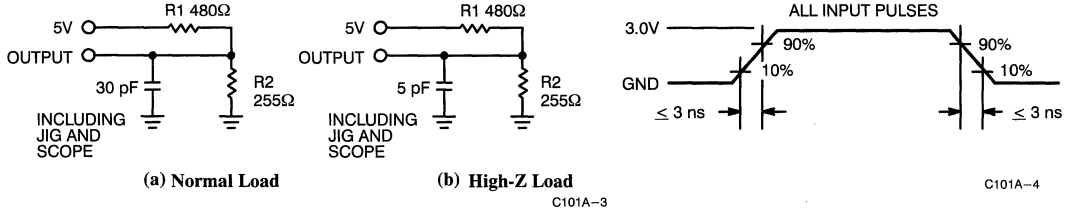
Parameter	Description	Test Conditions		7C101A–25 7C102A–25 Min.	7C101A–25 7C102A–25 Max.	7C101A–35 7C102A–35 Min.	7C101A–35 7C102A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		130		125	mA
			Mil		140		135	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



(a) Normal Load **(b) High-Z Load**

C101A–3 C101A–4

Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C101A–12 7C102A–12		7C101A–15 7C102A–15		7C101A–20 7C102A–20		7C101A–25 7C102A–25		7C101A–35 7C102A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t_{ADV}	Data Valid to Output Valid (7C101A)		12		15		20		25		35	ns

Notes:

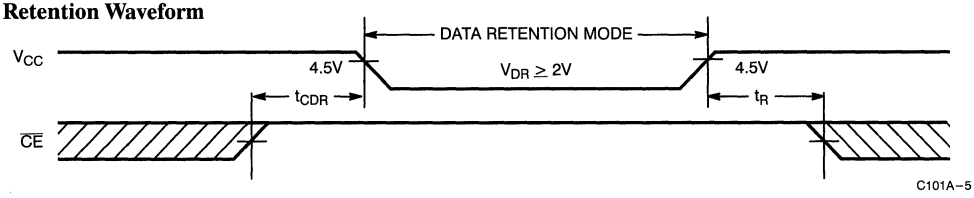
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3$ or $V_{IN} \leq 0.3V$		50		70	μA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

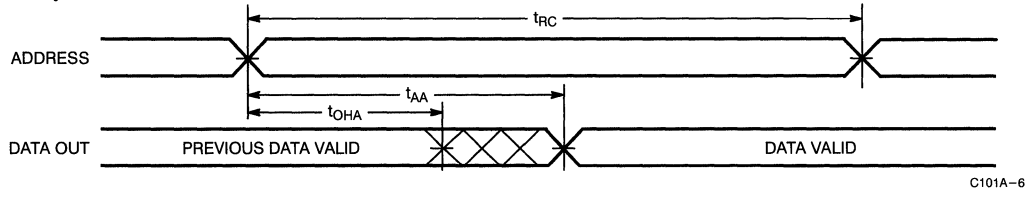
2

Data Retention Waveform

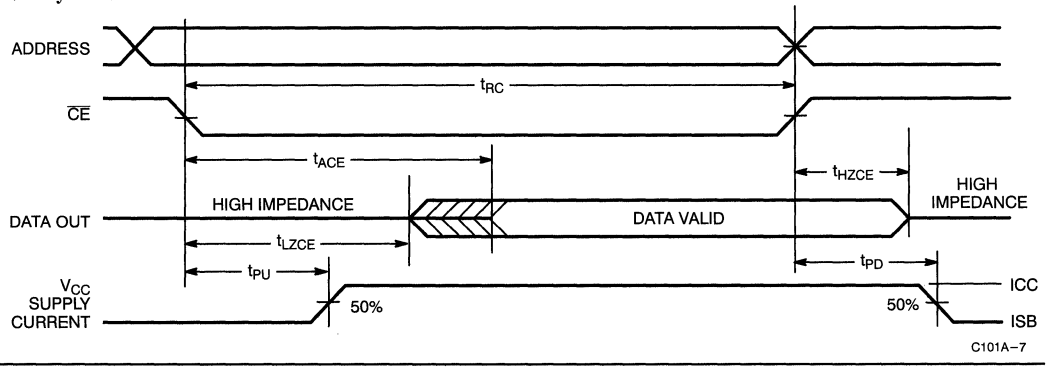


Switching Waveforms

Read Cycle No. 1[11, 12]



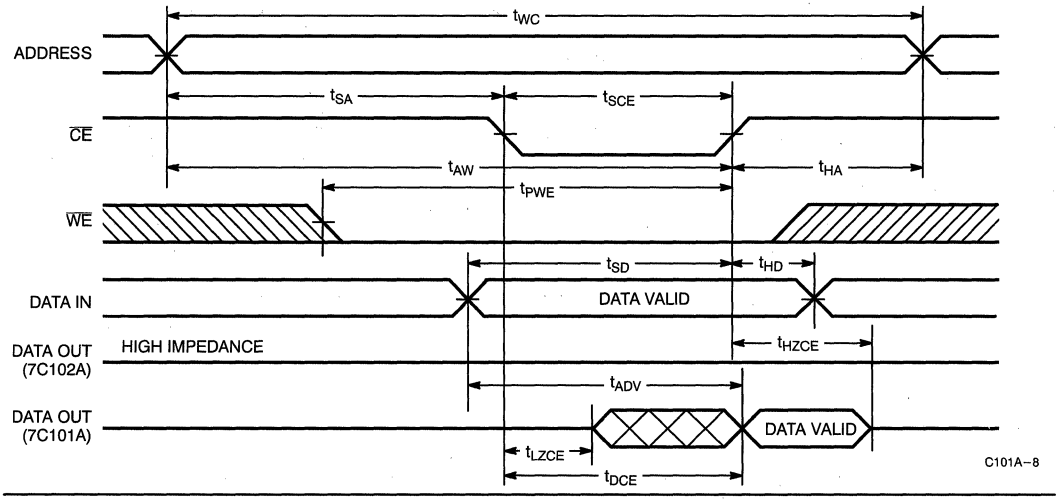
Read Cycle No. 2[12, 13]



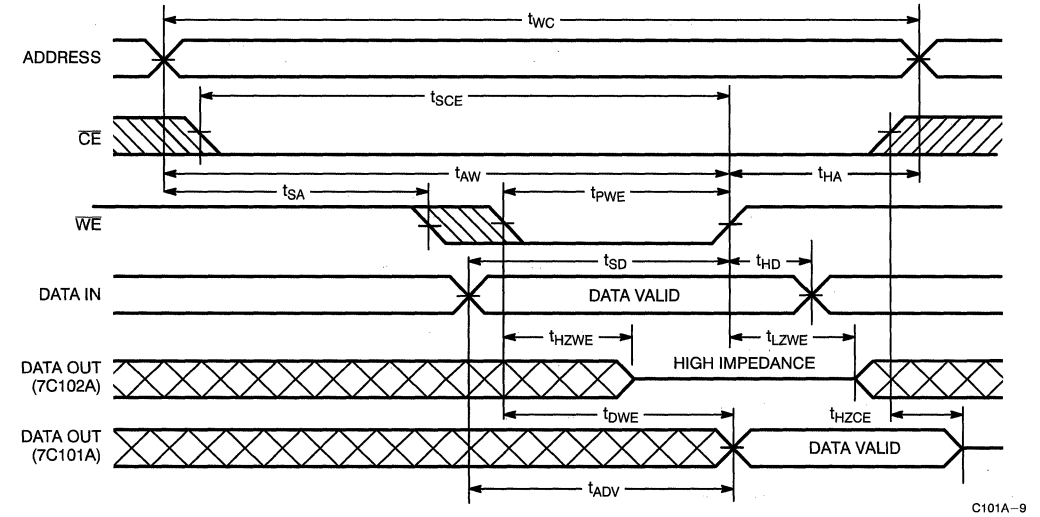
Notes:
10. No input may exceed V_{CC} + 0.5V.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[9, 14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[9]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C102A only).

Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C102A: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C101A: Transparent Write[15]	Active (I_{CC})

Note:
15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	PackageType	Operating Range
12	CY7C101A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C101A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C101A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C101A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C101A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C102A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C102A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C102A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C102A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C102A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}[16]	7, 8, 9, 10, 11

Note:
16. 7C101A only.

Document #: 38−00231−A

256K x 4 Static RAM

Features

- **High speed**
  — t_{AA} = 12 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 910 mW
- **Low standby power**
  — 275 mW
- **2.0V data retention (optional)**
  — 100 µW
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C106A is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

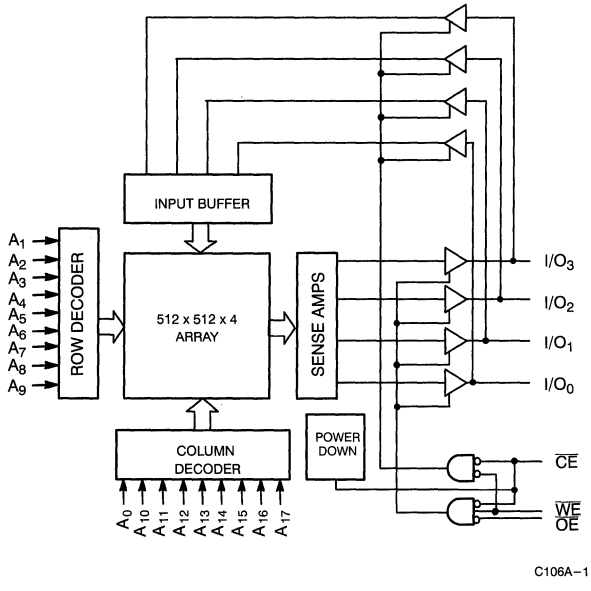
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C106A is available in standard 400-mil-wide DIPs and SOJs.

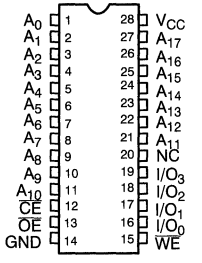
Logic Block Diagram



C106A–1

Pin Configuration

DIP/SOJ
Top View



C106A–2

Selection Guide

		7C106A–12	7C106A–15	7C106A–20	7C106A–25	7C106A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	165	155	140	130	125
	Military		165	150	140	135
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C106A−12 Min.	7C106A−12 Max.	7C106A−15 Min.	7C106A−15 Max.	7C106A−20 Min.	7C106A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140	mA
			Mil				165		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Notes:

1. V_{IL} (min.) = − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

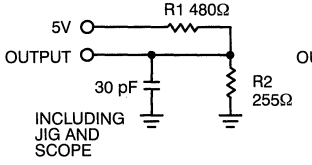
Parameter	Description	Test Conditions		7C106A–25 Min.	7C106A–25 Max.	7C106A–35 Min.	7C106A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		130		125	mA
			Mil		140		135	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

Capacitance[5]

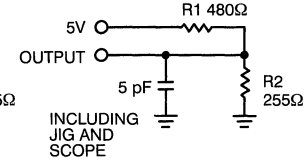
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

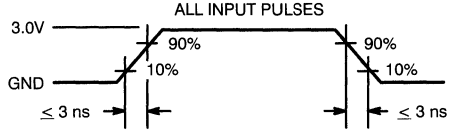


(a) Normal Load



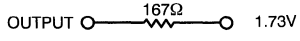
(b) High-Z Load

C106A–3



C106A–4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C106A–12		7C106A–15		7C106A–20		7C106A–25		7C106A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9,10]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns

Notes:

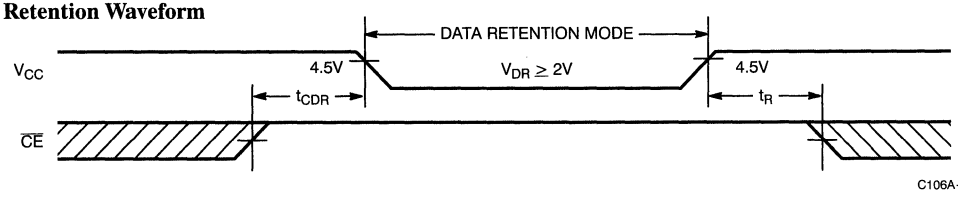
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

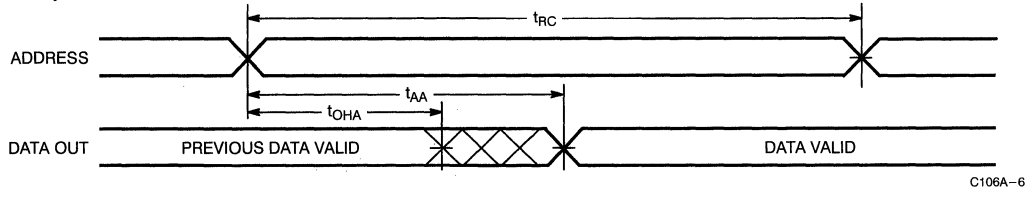
2

Data Retention Waveform

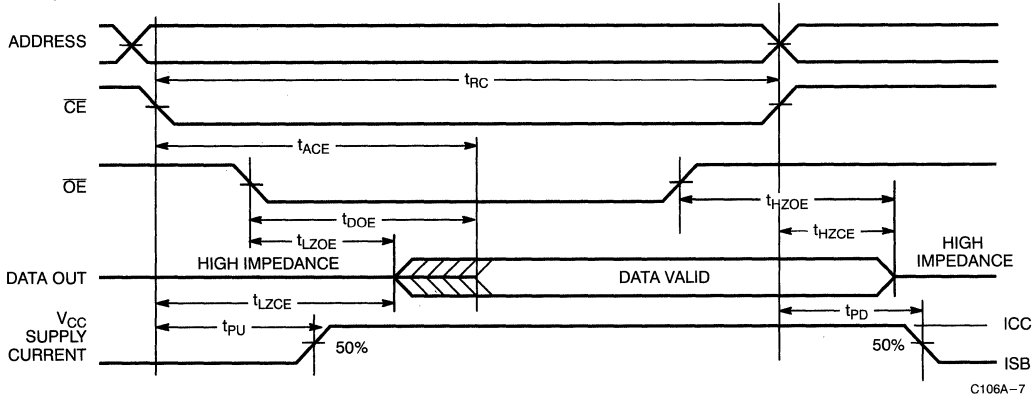


Switching Waveforms

Read Cycle No. 1[12, 13]



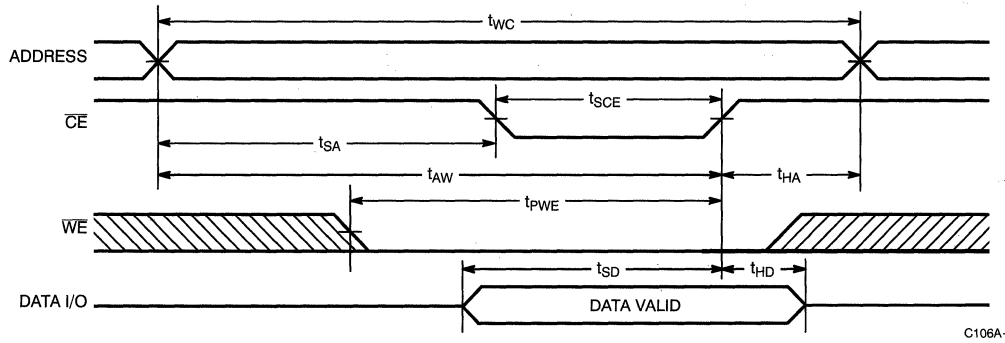
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



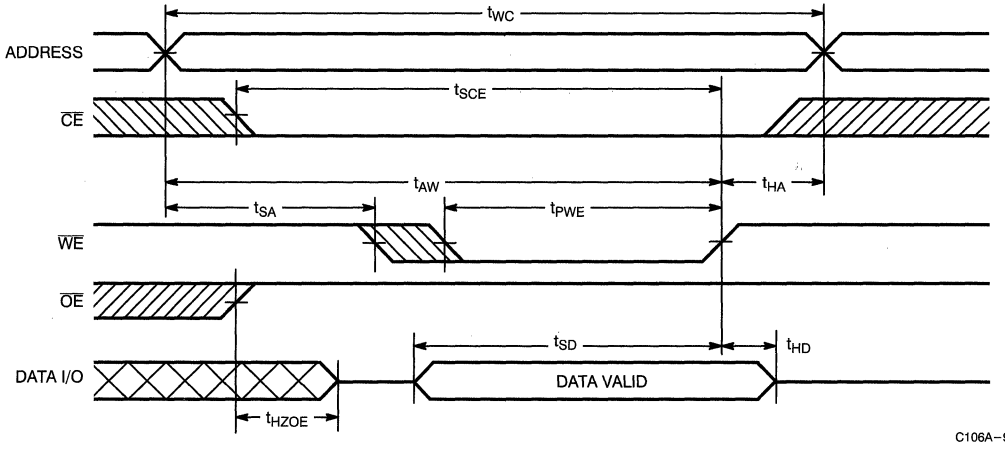
Notes:
11. No input may exceed V_{CC} +0.5V.
12. Device is continuously selected, $\overline{OE}$ and $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15,16]

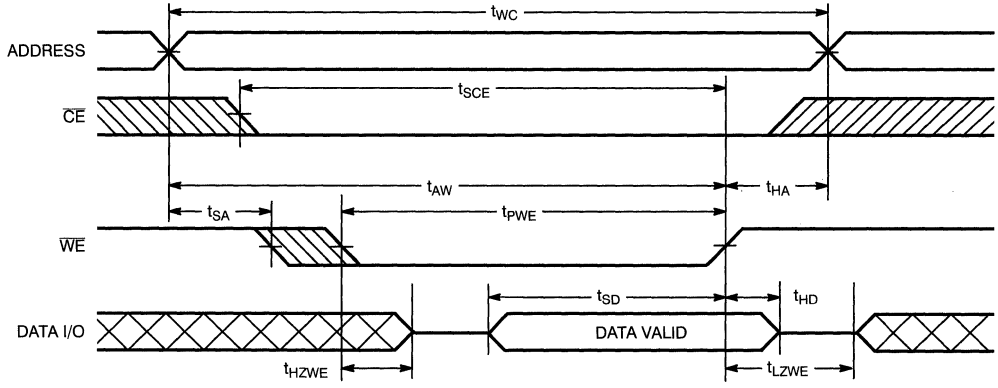


Notes:

15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



C106A–10

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C106A–12PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–12VC	V28	28-Lead (400-Mil) Molded SOJ	
15	CY7C106A–15PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–15VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–15DMB	D42	28-Lead (400-Mil) CerDIP	Military
20	CY7C106A–20PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–20VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–20DMB	D42	28-Lead (400-Mil) CerDIP	Military
25	CY7C106A–25PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–25VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–25DMB	D42	28-Lead (400-Mil) CerDIP	Military
35	CY7C106A–35PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C106A–35VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C106A–35DMB	D42	28-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00230–A

1M x 1 Static RAM

Features

- **High speed**
  — t_{AA} = 12 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 825 mW
- **Low standby power**
  — 275 mW
- **2.0V data retention (optional)**
  — 100 µW
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C107A is a high-performance CMOS static RAM organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

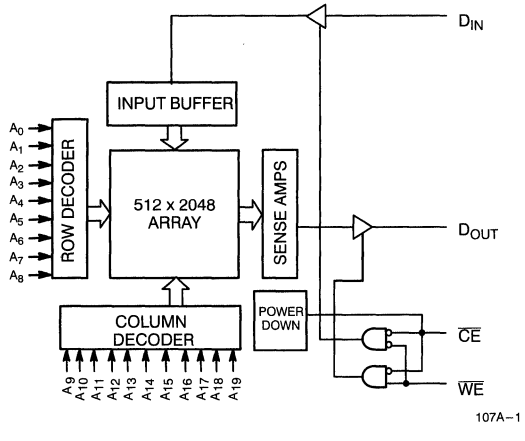
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

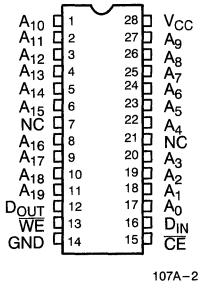
The CY7C107A is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration

DIP/SOJ
Top View



Selection Guide

		7C107A–12	7C107A–15	7C107A–20	7C107A–25	7C107A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	150	135	125	120	110
	Military		145	135	130	120
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C107A−12 Min.	7C107A−12 Max.	7C107A−15 Min.	7C107A−15 Max.	7C107A−20 Min.	7C107A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		135		125	mA
			Mil				145		135	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current − TTL Inputs	Max.. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions		7C107A-25 Min.	7C107A-25 Max.	7C107A-35 Min.	7C107A-35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+ 0.3	2.2	V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$	Com'l		120		110	mA
			Mil		130		120	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current − TTL Inputs	Max.. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

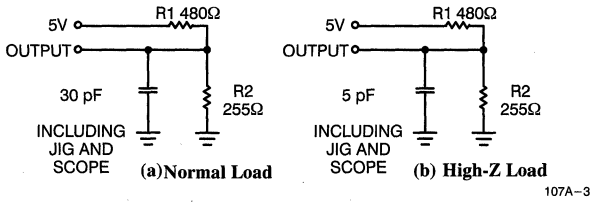
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

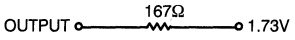
Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics[3, 6] Over the Operating Range

Parameter	Description	7C107A–12		7C107A–15		7C107A–20		7C107A–25		7C107A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns

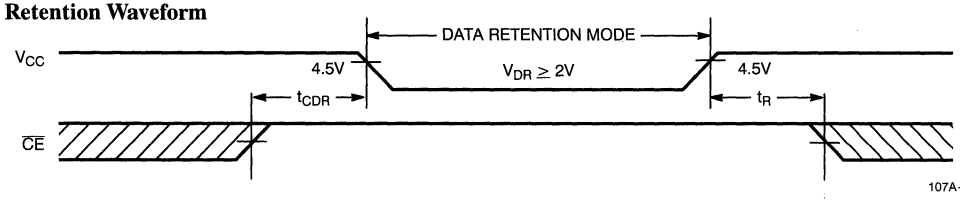
Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L Version Only)

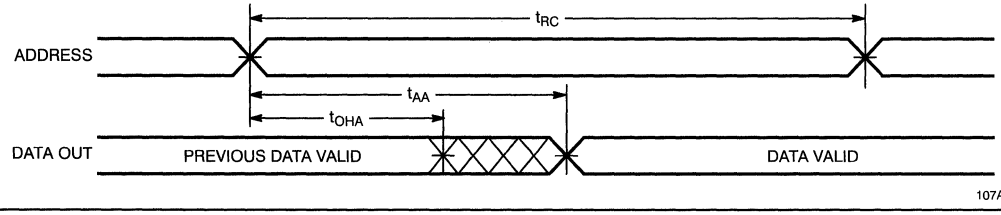
Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform

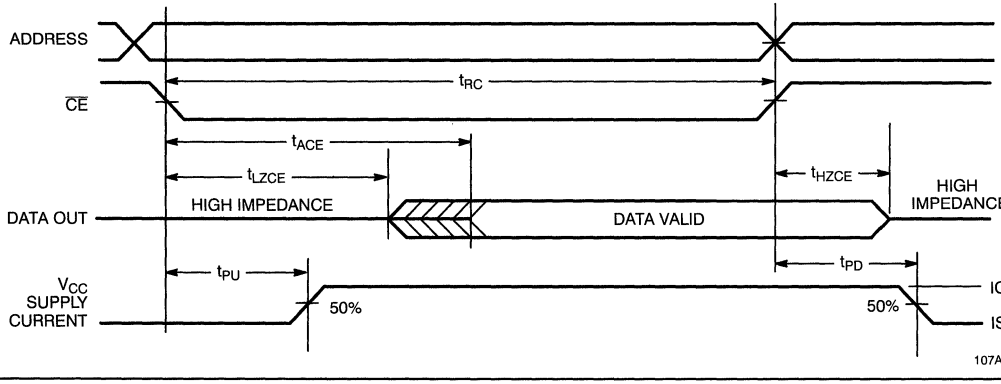


Switching Waveforms

Read Cycle No. 1[11, 12]



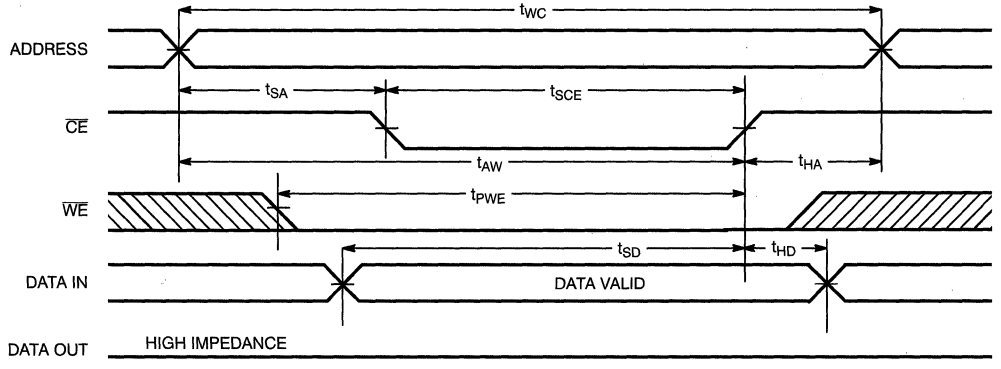
Read Cycle No. 2[12, 13]



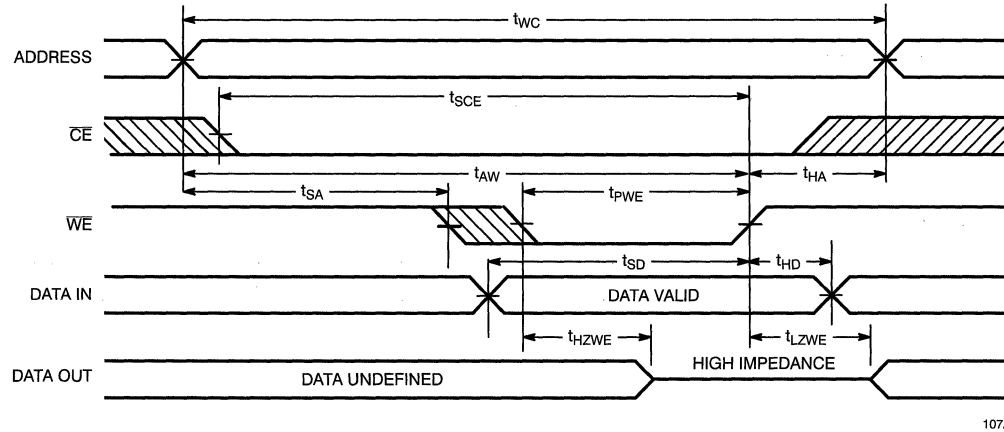
Notes:
10. No input may exceed V_{CC} + 0.5V.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[14]



Truth Table

$\overline{CE}$	$\overline{WE}$	D_{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C107A–12PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–12VC	V28	28-Lead (400-Mil) Molded SOJ	
15	CY7C107A–15PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–15VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–15DMB	D42	28-Lead (400-Mil) CerDIP	Military
20	CY7C107A–20PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–20VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–20DMB	D42	28-Lead (400-Mil) CerDIP	Military
25	CY7C107A–25PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–25VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–25DMB	D42	28-Lead (400-Mil) CerDIP	Military
35	CY7C107A–35PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A–35VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A–35DMB	D42	28-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00232–A

CY7C109

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 20 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 770 mW**
- **Low standby power**
  - **— 165 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C109 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

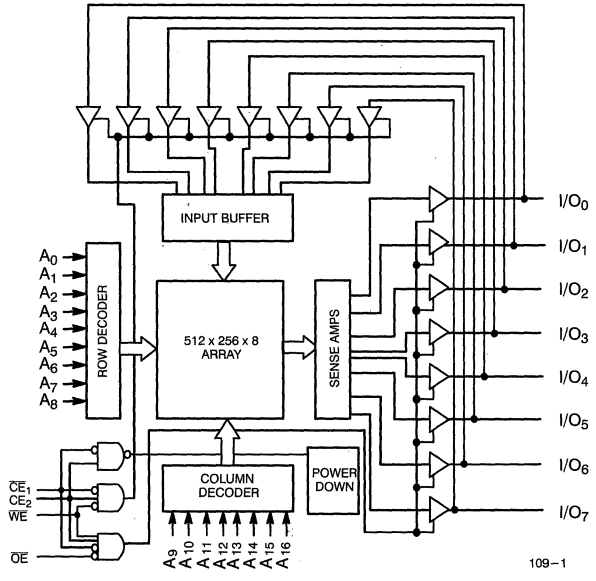
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

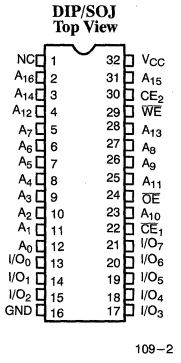
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C109 is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C109–20	7C109–25	7C109–35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	140	135	125
Maximum Standby Current (mA)	Commercial	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .. −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C109−20 Min.	7C109−20 Max.	7C109−25 Min.	7C109−25 Max.	7C109−35 Min.	7C109−35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		140		135		125	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		30		30		25	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ − 0.3V, or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V, or $V_{IN} \leq$ 0.3V, f=0	Com'l		10		10		10	mA

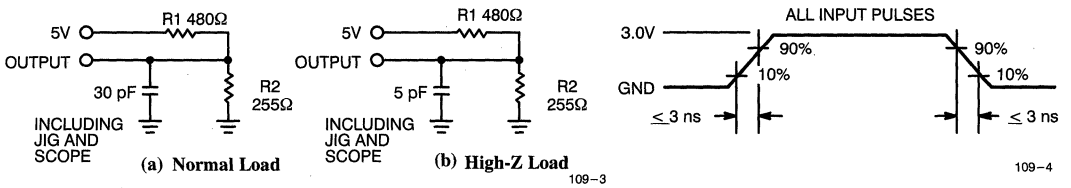
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9	pF
C_{OUT}	Output Capacitance		9	pF

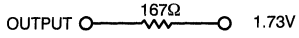
Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics[3, 6] Over the Operating Range

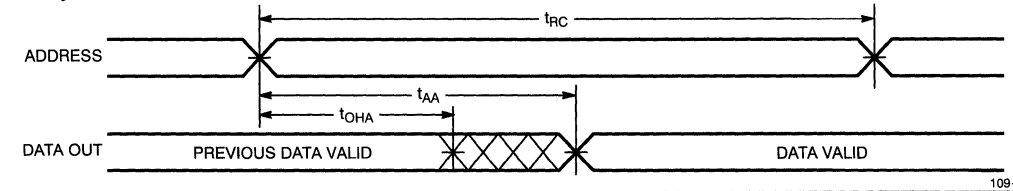
Parameter	Description	7C109–20		7C109–25		7C109–35		Unit
		Min.	Max.	Min.	Max.	Min.	Min.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		35		ns
t_{AA}	Address to Data Valid		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		8		10		15	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	3		5		5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7, 8]		8		10		15	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		20		25		35	ns
WRITE CYCLE[9, 10]								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	15		20		25		ns
t_{AW}	Address Set-Up to Write End	15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		8		10		15	ns

Notes:

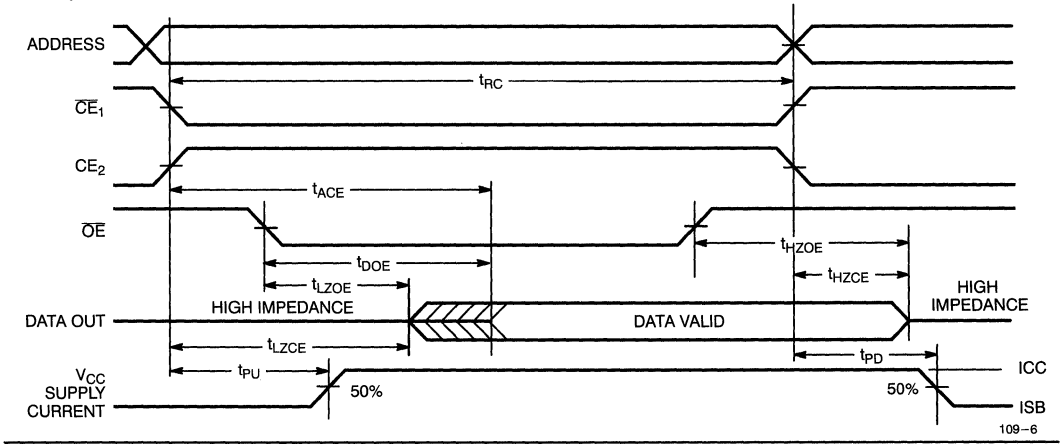
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

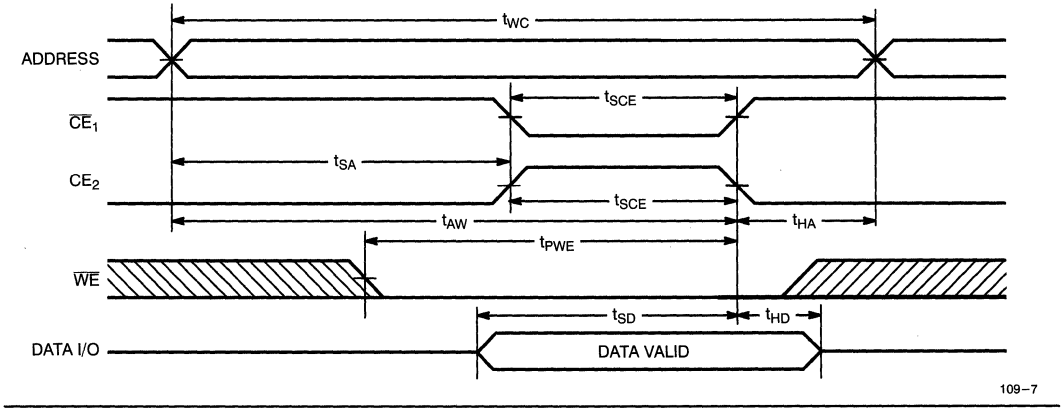
Read Cycle No. 1[11, 12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



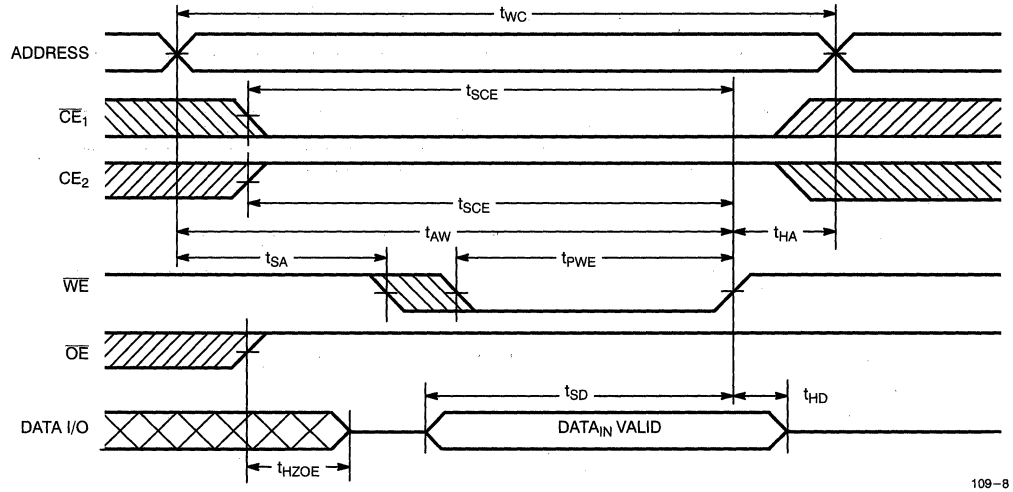
Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[14, 15]



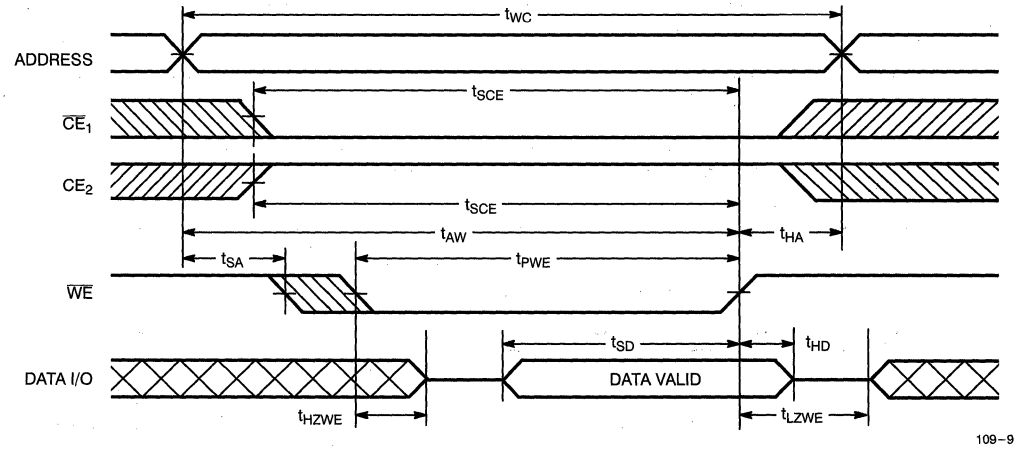
Notes:
11. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14, 15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 15]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C109–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109–20VC	V33	32-Lead (400-Mil) Molded SOJ	
25	CY7C109–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109–25VC	V33	32-Lead (400-Mil) Molded SOJ	
35	CY7C109–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109–35VC	V33	32-Lead (400-Mil) Molded SOJ	

Document #: 38–00140–F

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Low standby power**
  - **— 250 mW**
- **2.0V data retention (optional)**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C109A is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

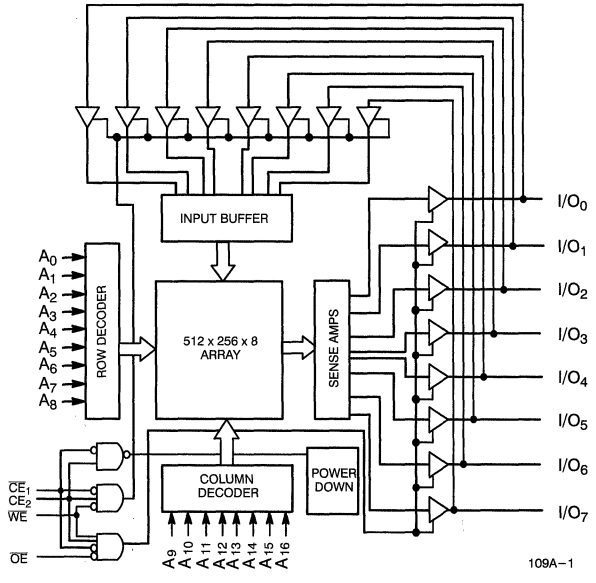
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

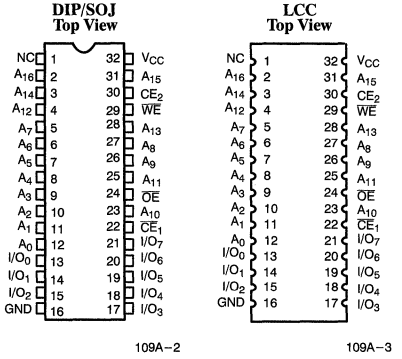
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C109A is available in standard 400-mil-wide DIPs and SOJs and a leadless chip carrier.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C109A–12	7C109A–15	7C109A–20	7C109A–25	7C109A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	185	170	155	145	140
	Military		180	170	160	150
Maximum Standby Current (mA)	Commercial	45	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .. −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C109A−12 Min.	7C109A−12 Max.	7C109A−15 Min.	7C109A−15 Max.	7C109A−20 Min.	7C109A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		185		170		155	mA
			Mil				180		170	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		45		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ − 0.3V, or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V, or $V_{IN} \leq$ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

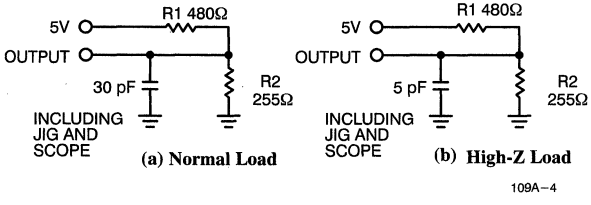
Electrical Characteristics Over the Operating Range[3] (continued)

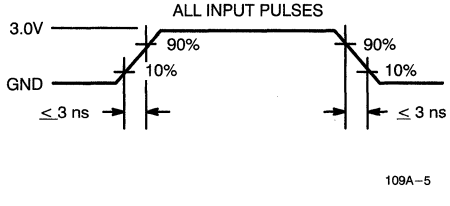
Parameter	Description	Test Conditions		7C109A–25 Min.	7C109A–25 Max.	7C109A–35 Min.	7C109A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		145		140	mA
			Mil		160		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

Capacitance[5]

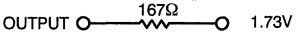
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics[3, 6] Over the Operating Range

Parameter	Description	7C109A–12		7C109A–15		7C109A–20		7C109A–25		7C109A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Min.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9, 10]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns

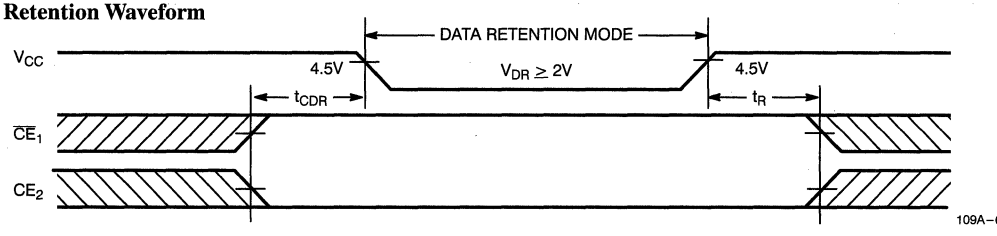
Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (L Version Only)

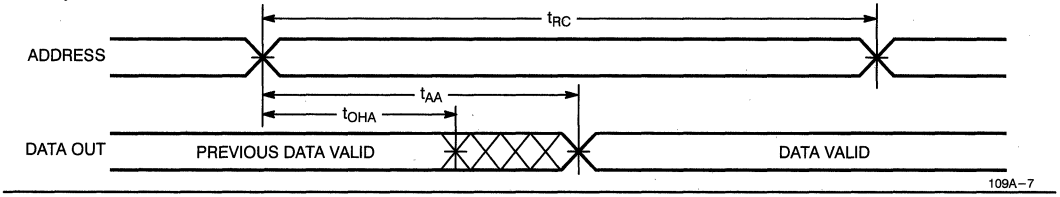
Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform

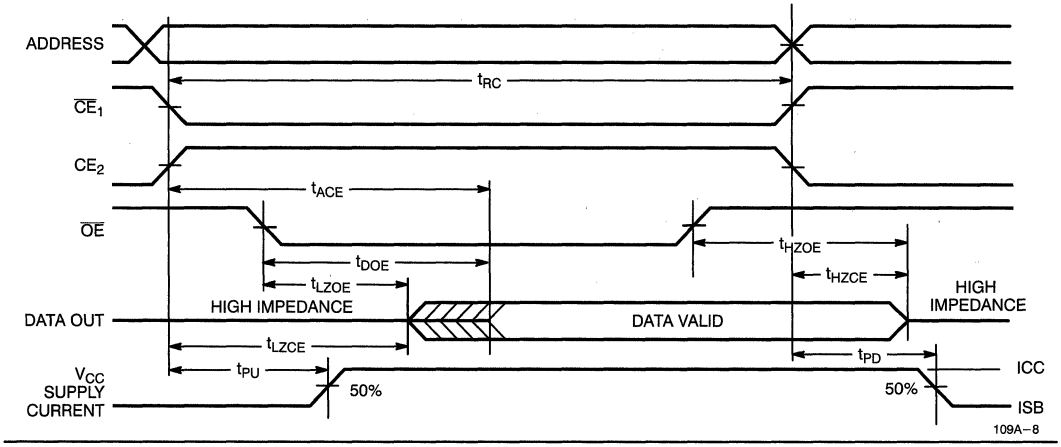


Switching Waveforms

Read Cycle No. 1[12, 13]



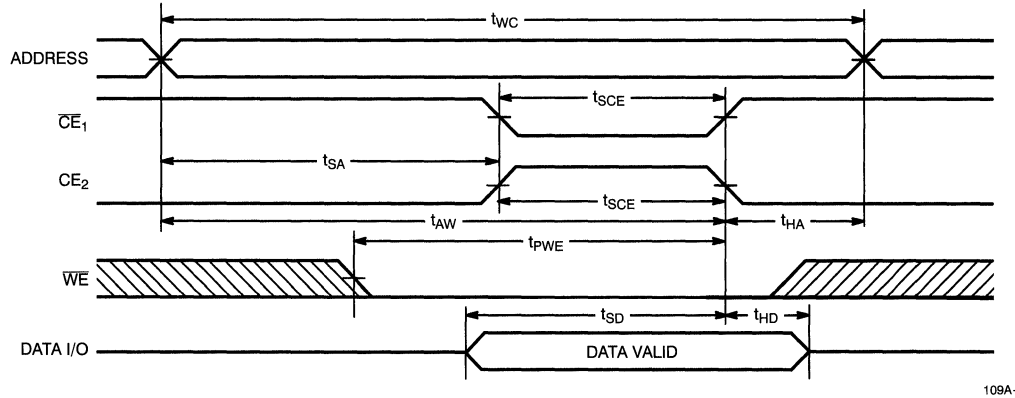
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



Notes:
11. No input may exceed V_{CC} +0.5V.
12. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

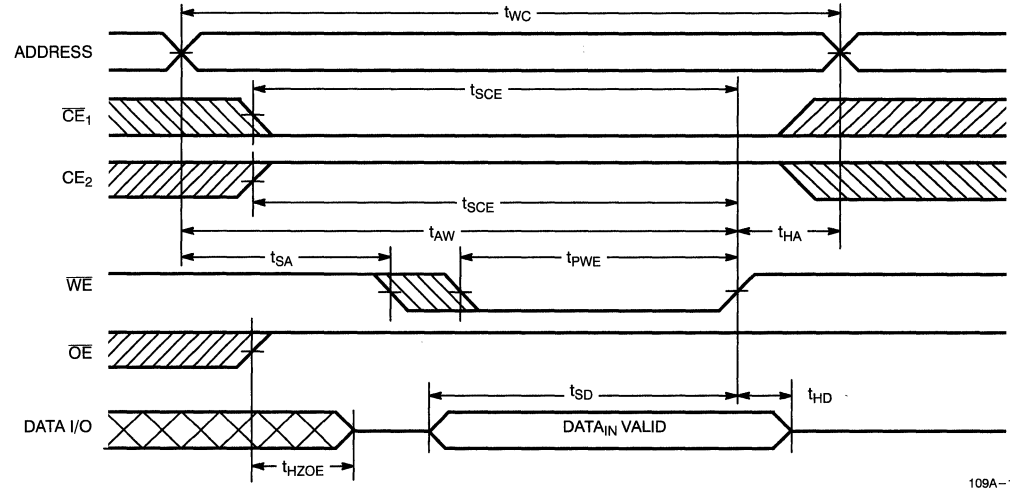
Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[15, 16]



109A–9

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]

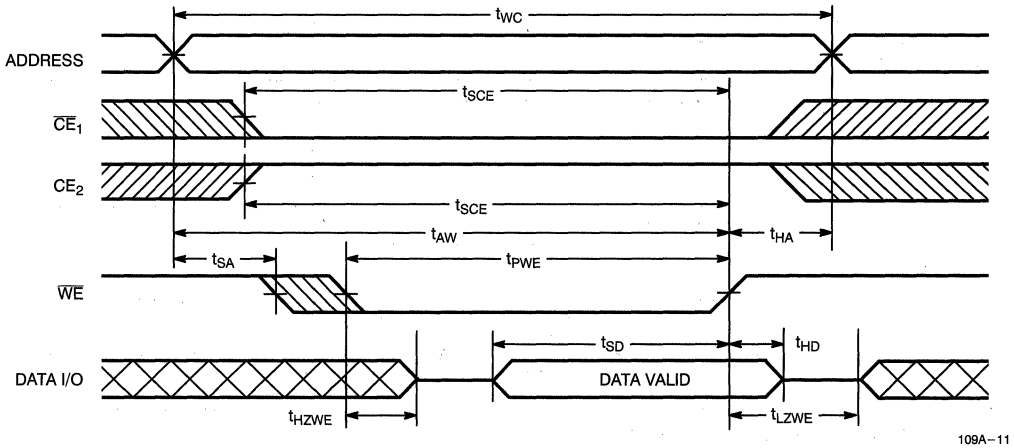


109A–10

Notes:
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C109A-12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C109A-15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A-15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A-15DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A-15LMB	L75	32-Pin Leadless Chip Carrier	
20	CY7C109A-20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A-20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A-20DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A-20LMB	L75	32-Pin Leadless Chip Carrier	

Contact factory for "L" version availability.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C109A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–25LMB	L75	32-Pin Leadless Chip Carrier	
35	CY7C109A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–35LMB	L75	32-Pin Leadless Chip Carrier	

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00233–A

CY7C123

256 x 4 Static RAM

Features

- **256 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 7 ns (commercial)**
  - **— 10 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 825 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance both commercial and military**
- **TTL-compatible inputs and outputs**
- **24 pins**
- **300-mil package**

Functional Description

The CY7C123 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

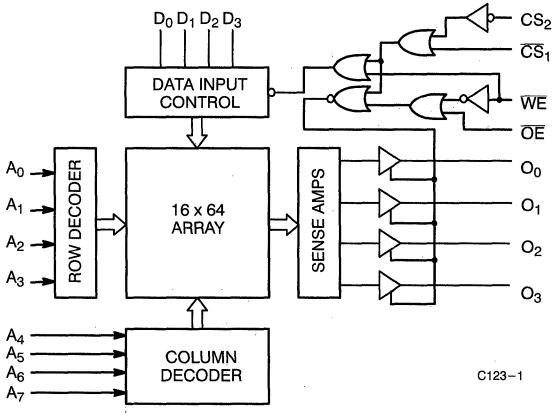
Writing to the device is accomplished when the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are both LOW and the chip select two input is HIGH. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_7). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking the chip select one ($\overline{CS_1}$) and output enable ($\overline{OE}$) inputs LOW, while the write enable ($\overline{WE}$) and chip select two (CS_2) inputs remain HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

The output pins remain in high-impedance state when chip select one ($\overline{CS_1}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip select two (CS_2) is LOW.

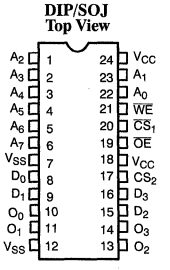
A die coat is used to insure alpha immunity.

Logic Block Diagram



C123–1

Pin Configuration



C123–2

Selection Guide

		7C123–7	7C123–9	7C123–10	7C123–12	7C123–15
Maximum Access Time (ns)	Commercial	7	9		12	
	Military			10	12	15
Maximum Operating Current (mA)	Commercial	120	120		120	
	Military			150	150	150

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pins 24 and 18 to Pins 7 and 12)[1] ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C123−7 7C123−9 Min.	7C123−7 7C123−9 Max.	7C123−10 7C123−15 Min.	7C123−10 7C123−15 Max.	7C123−12 Min.	7C123−12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.8	+0.8	−0.8	+0.8	−0.8	+0.8	V
I_{IX}	Input Load Current	$V_{SS} \le V_I \le V_{CC}$		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Current (High Z)	$V_{SS} \le V_{OUT} \le V_{CC}$, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Commercial		120				120	mA
			Military				150		150	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

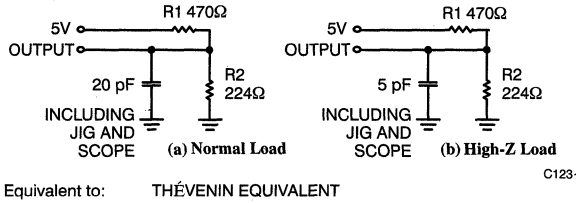
Logic Table[5]

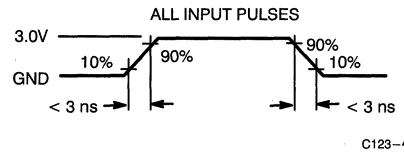
Input $\overline{OE}$	Input $\overline{CS_1}$	Input CS_2	Input $\overline{WE}$	Input $D_0 - D_3$	Outputs	Mode
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	$O_0 - O_3$	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

Notes:

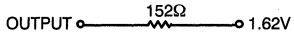
1. V_{IL}(min.) = −3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. H = High Voltage, L = Low Voltage, X = Don't Care, and High Z = High Impedance.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

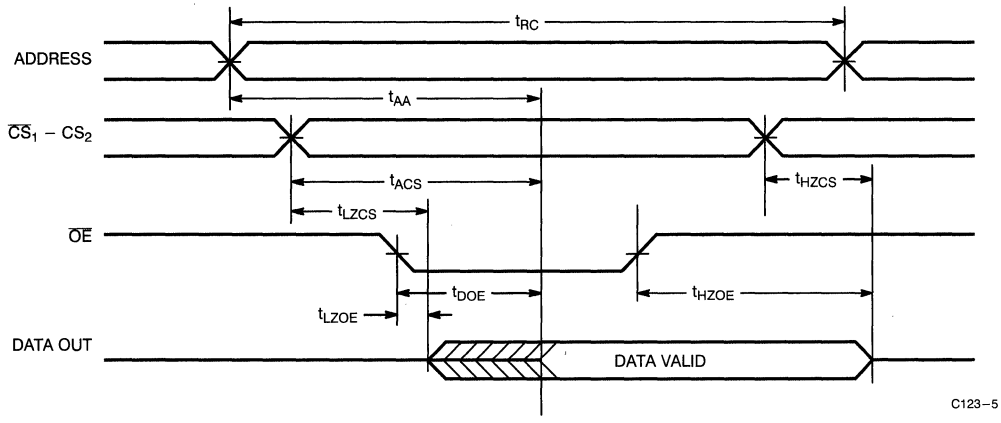
Parameter	Description	7C123-7		7C123-9		7C123-10		7C123-12		7C123-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	7		9		10		12		15		ns
t_{AA}	Address to Data Valid		7		9		10		12		15	ns
t_{ACS}	Chip Select to Data Valid		7		8		8		8		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		8		8		10	ns
t_{HZCS}	Chip Select to High Z[6, 7]		5		6		6		6.5		8	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		5		6		6		6.5		8	ns
t_{LZCS}	Chip Select to Low Z[7]	2		2		2		2		2		ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		2		2		2		ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	7		9		10		12		15		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		5.5		6		6		7		8	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	5		6.5		7		8		11		ns
t_{SD}	Data Set-Up to Write End	5		6		7		8		11		ns
t_{HD}	Data Hold from Write End	1		1		1		1		1		ns
t_{SA}	Address Set-Up to Write Start	0.5		1		1		2		2		ns
t_{HA}	Address Hold from Write End	1.5		1.5		2		2		2		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	5		6.5		7		8		11		ns
t_{AW}	Address Set-Up to Write End	5.5		7.5		8		10		13		ns

Notes:

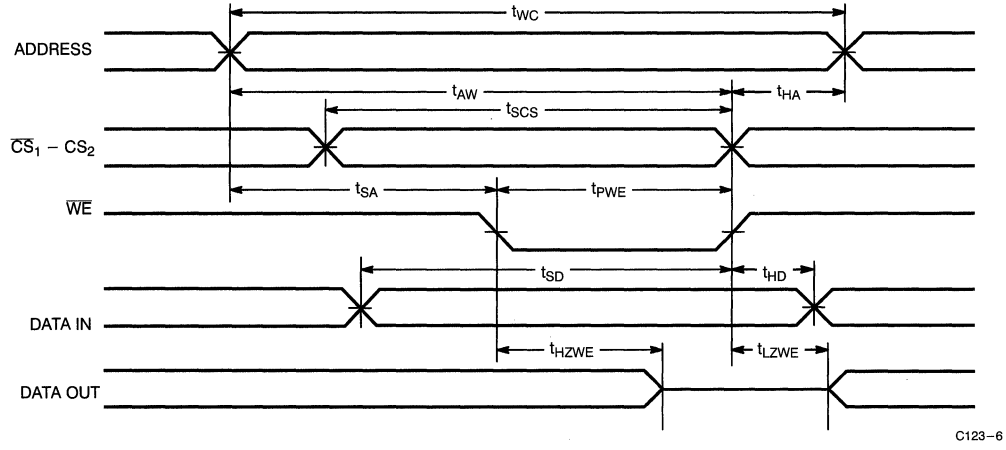
6. Transition is measured at steady-state HIGH level − 500 mV or steady-state LOW level +500 mV on the output from 1.5V level on the input with load shown in part (b) of AC Test Loads.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.

Switching Waveforms

Read Cycle [8, 9]



Write Cycle [8, 9]

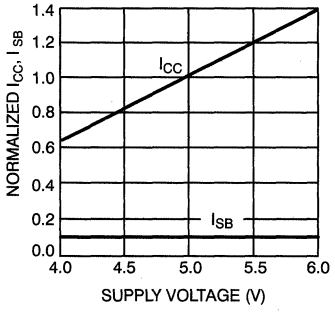


Notes:

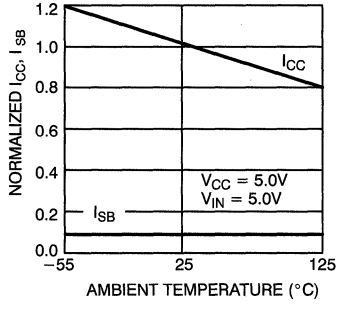
8. Measurements are referenced to 1.5V unless otherwise stated.
9. Timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

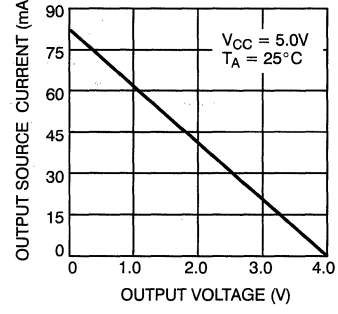
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



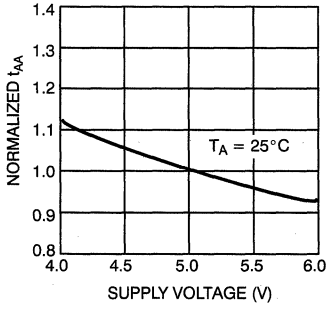
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



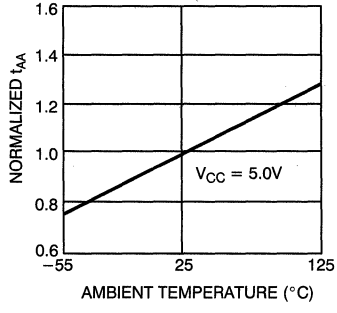
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



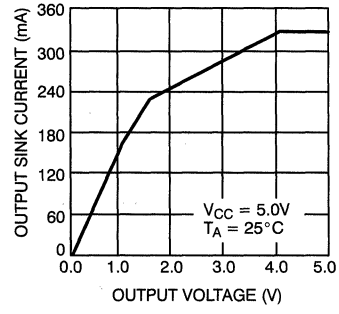
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



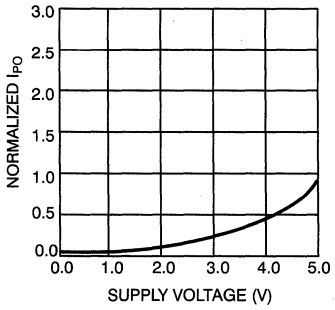
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



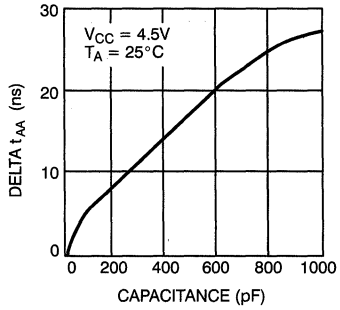
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



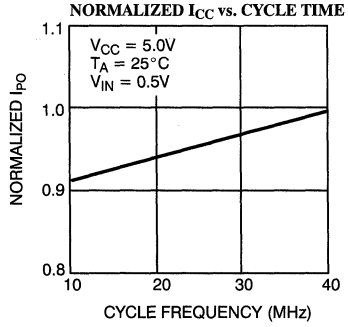
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TOTAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C123–7PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123–7VC	V13	24-Lead Molded SOJ	
9	CY7C123–9PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123–9VC	V13	24-Lead Molded SOJ	
10	CY7C123–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
12	CY7C123–12PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C123–15DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

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CY7C128A

2K x 8 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 550 mW (military)**
- **Low standby power**
  - **— 110 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

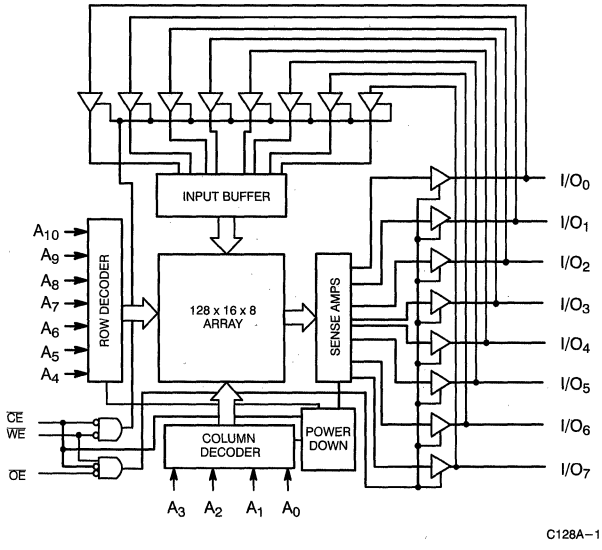
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The CY7C128A utilizes a die coat to ensure alpha immunity.

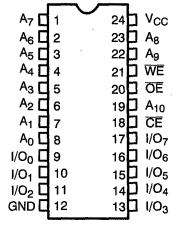
Logic Block Diagram



C128A–1

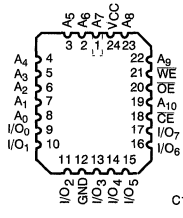
Pin Configurations

DIP/SOJ
Top View



C128A–2

LCC
Top View



C128A–3

Selection Guide

		7C128A–15	7C128A–20	7C128A–25	7C128A–35	7C128A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	120	100	100	100	
	Military		125	125	100	100
Maximum Standby Current (mA)	Commercial	40/40	40/20	20	20	
	Military		40/20	40	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C128A−15		7C128A−20		7C128A−25		7C128A−35, 45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		120		100		100		100	mA
			Mil				125		125		100	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Com'l		40		40		20		20	mA
			Mil				40		40		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} −0.3V or V_{IN} ≤ 0.3V	Com'l		40		20		20		20	mA
			Mil				20		20		20	

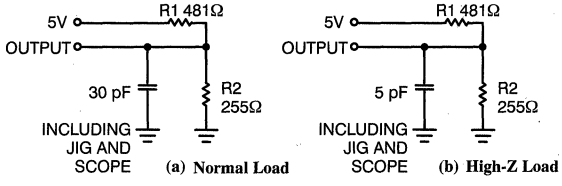
Capacitance[5]

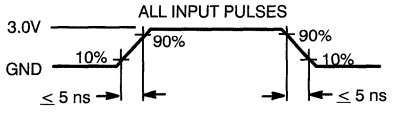
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

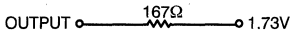
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 6]

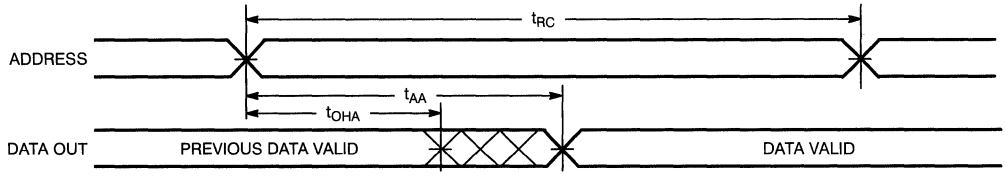
Parameter	Description	7C128A–15		7C128A–20		7C128A–25		7C128A–35		7C128A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Note:

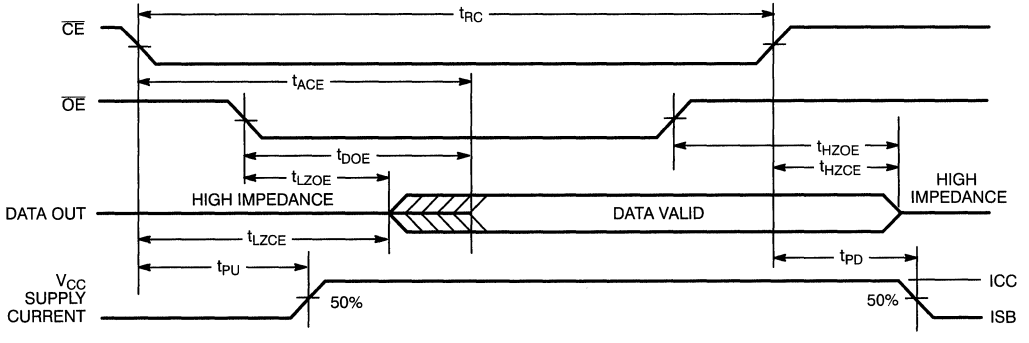
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

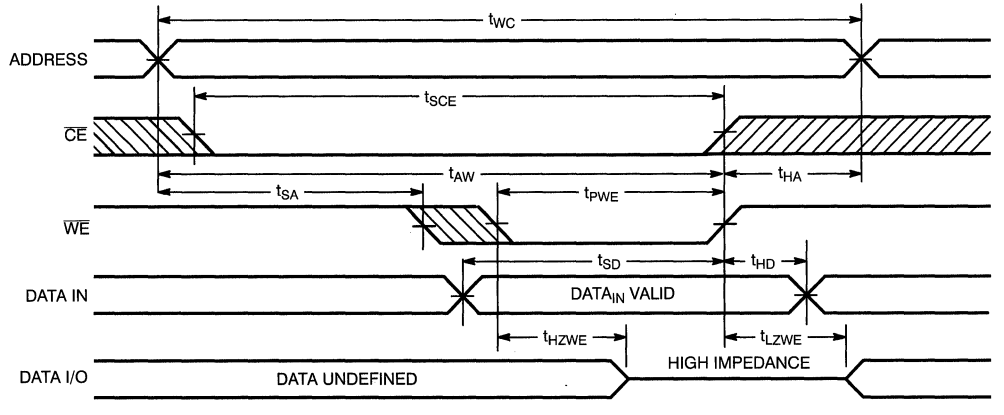
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



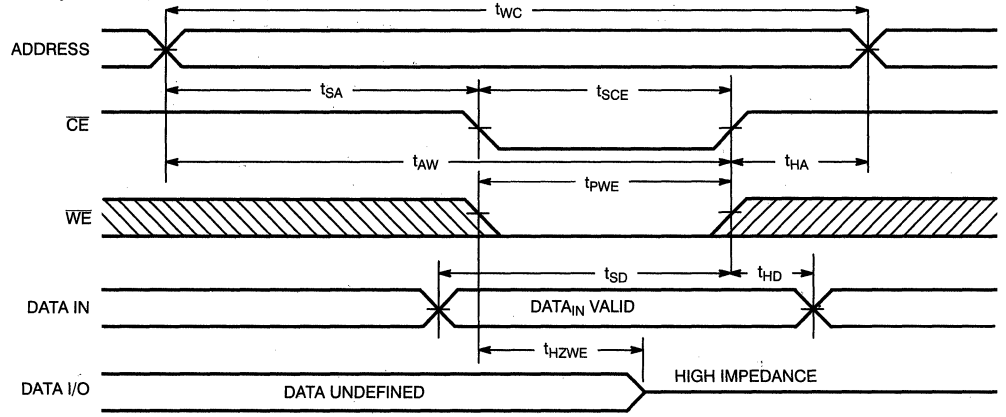
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

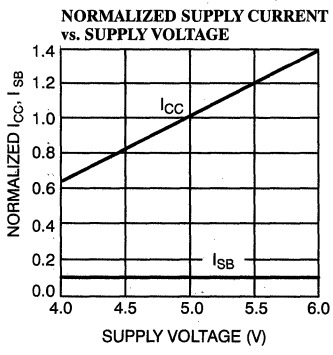
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13, 14]

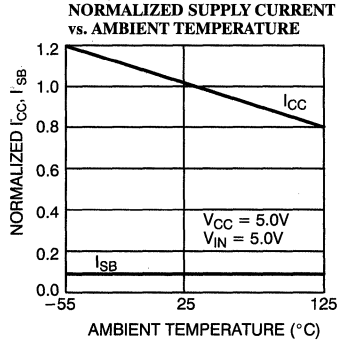


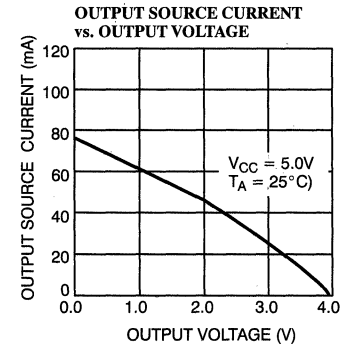
C128A–9

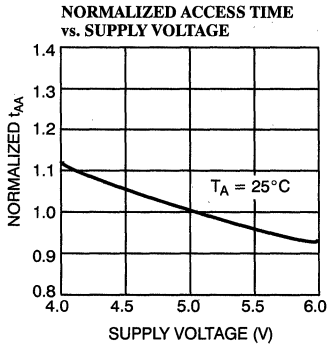
Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

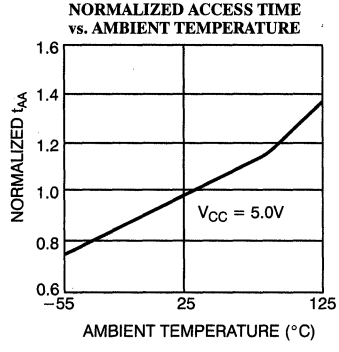
Typical DC and AC Characteristics

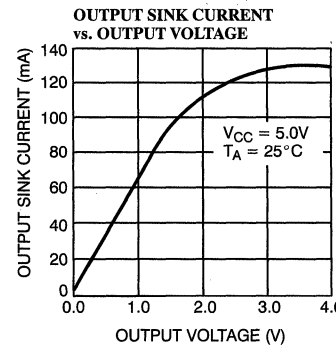






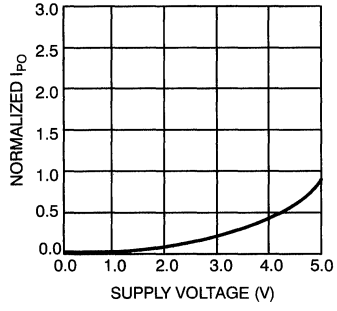




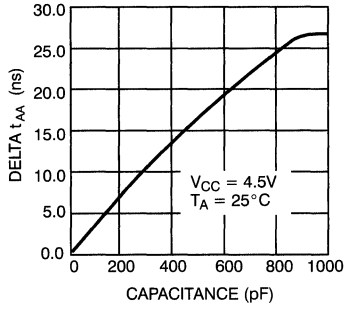


Typical DC and AC Characteristics (continued)

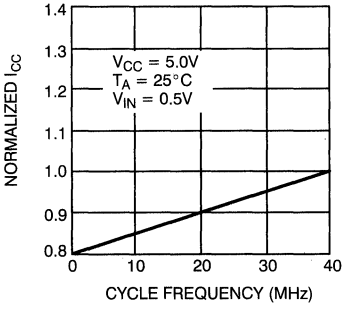
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C128A–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–15VC	V13	24-Lead Molded SOJ	
20	CY7C128A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–20VC	V13	24-Lead Molded SOJ	
	CY7C128A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–20LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
25	CY7C128A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–25VC	V13	24-Lead Molded SOJ	
	CY7C128A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–25LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
35	CY7C128A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A–35VC	V13	24-Lead Molded SOJ	
	CY7C128A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–35LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
45	CY7C128A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A–45LMB	L53	24-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00094-B

CY7C148
CY7C149

1K x 4 Static RAM

Features

- **Automatic power-down when deselected (7C148)**
- **CMOS for optimum speed/power**
- **25-ns access time**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power (7C148)**
  - **— 82.5 mW (25-ns version)**
  - **— 55 mW (all others)**
- **5-volt power supply ± 10% tolerance, both commercial and military**
- **TTL-compatible inputs and outputs**

Functional Description

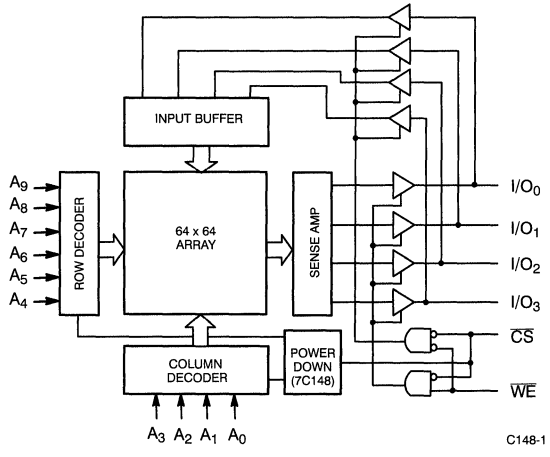
The CY7C148 and CY7C149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY7C148 remains in a low-power mode as long as the device remains unselected; i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_3) is written into the memory locations specified on the address pins (A_0 through A_9).

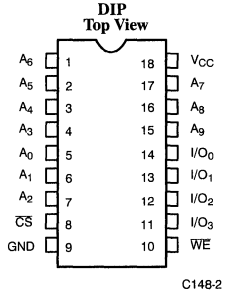
Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data I/O pins.

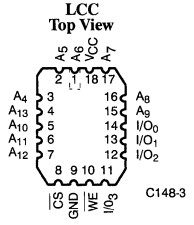
The I/O pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C148–25	7C148–35	7C148–45	7C149–25	7C149–35	7C149–45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C148−25 7C149−25 Min.	7C148−25 7C149−25 Max.	7C148−35, 45 7C149−35, 45 Min.	7C148−35, 45 7C149−35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage				−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled			−50	50	−50	50	µA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS}$ ≤ V_{IL}, Output Open		Com'l		90		80	mA
				Mil				110	
I_{SB}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}	7C148 Only	Com'l		15		10	mA
				Mil				10	
I_{PO}	Peak Power-On Current[3]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}	7C148 Only	Com'l		15		10	mA
				Mil				10	
I_{OS}	Output Short Circuit Current[4]	GND ≤ V_O ≤ V_{CC}		Com'l		±275		±275	mA
				Mil				±350	

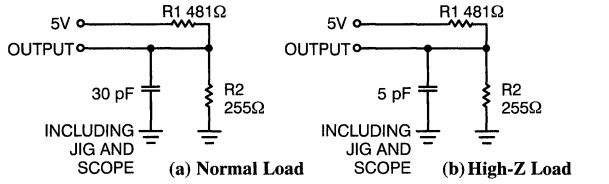
Capacitance[5]

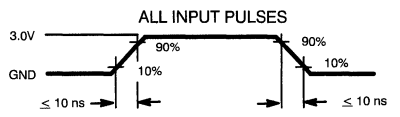
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

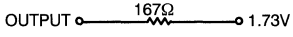
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
4. For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



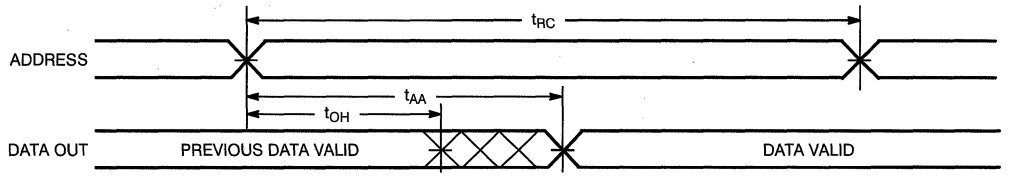
Switching Characteristics Over the Operating Range[2]

Parameter	Description		7C148–25 7C149–25 Min.	7C148–25 7C149–25 Max.	7C148–35 7C149–35 Min.	7C148–35 7C149–35 Max.	7C148–45 7C149–45 Min.	7C148–45 7C149–45 Max.	Unit
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1}	Chip Select LOW to Data Out Valid (7C148 only)			25[6]		35		45	ns
t_{ACS2}				30[7]		35		45	ns
t_{ACS}	Chip Select LOW to Data Out Valid (7C149 only)			15		15		20	ns
t_{LZ}[8]	Chip Select LOW to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[8]	Chip Select HIGH to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		20		30		35		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable to Output in High Z		0	8	0	8	0	8	ns
t_{DW}	Data in Valid to Write Enable HIGH		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		20		30		40		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		ns

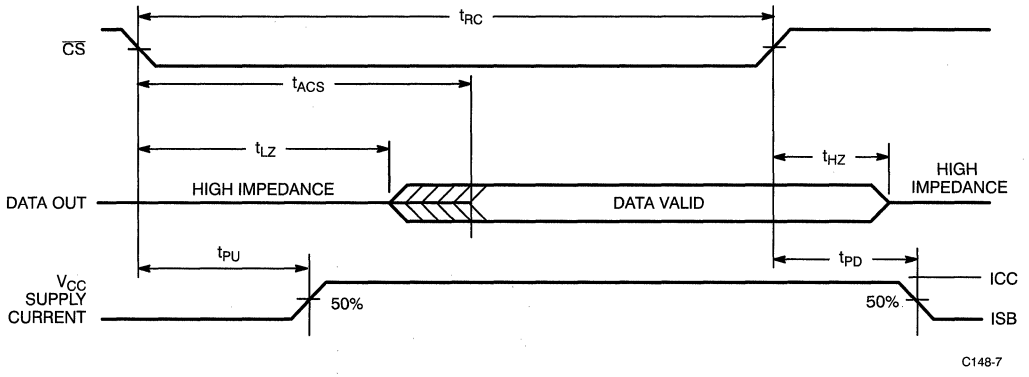
Notes:
6. Chip deselected greater than 25 ns prior to selection.
7. Chip deselected less than 25 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady-state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

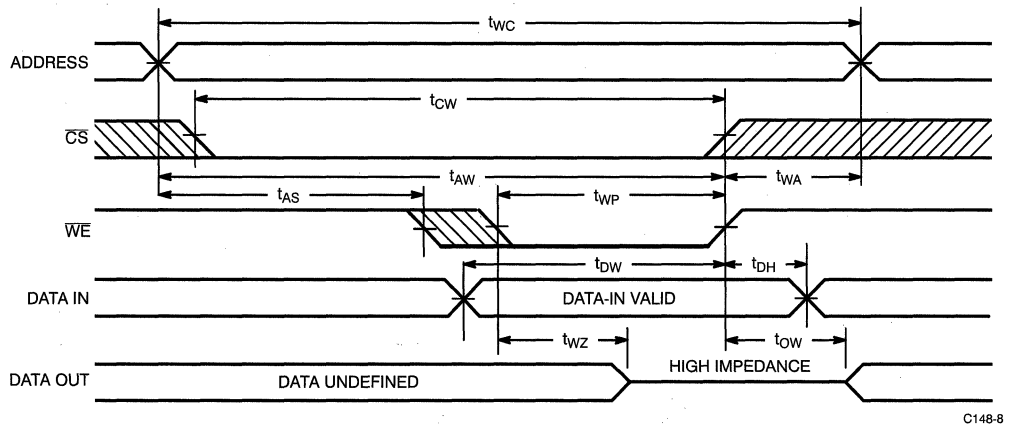
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



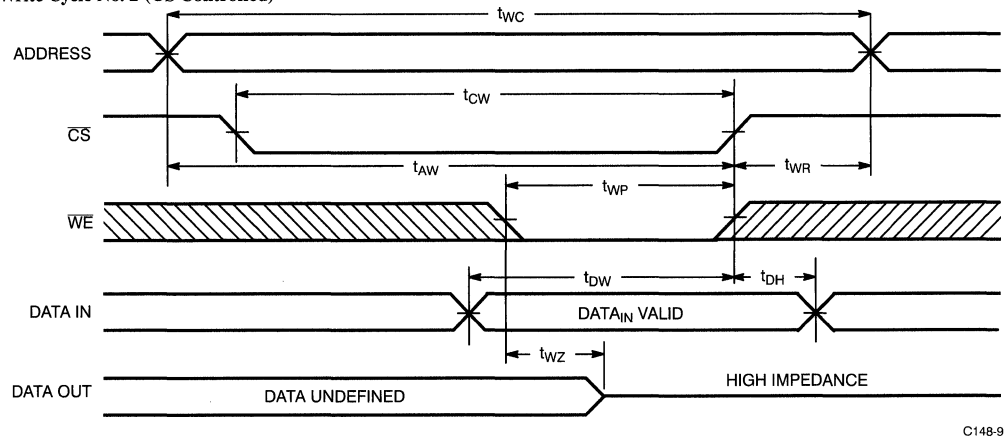
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

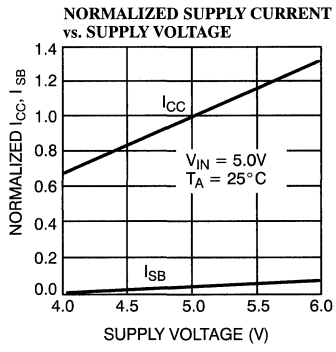
Switching Waveforms (continued)

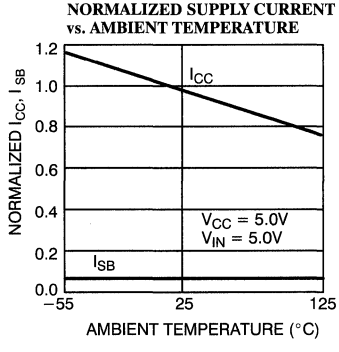
Write Cycle No. 2 ($\overline{CS}$ Controlled)[13]

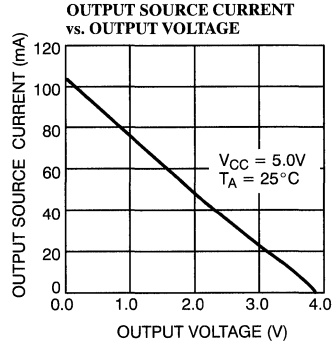


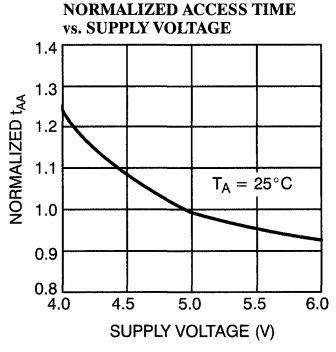
Notes:
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

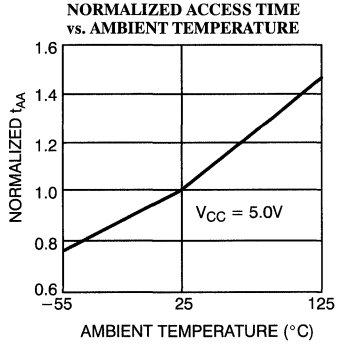
Typical DC and AC Characteristics

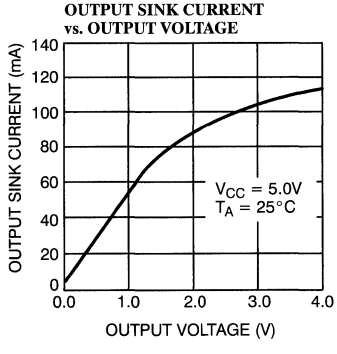






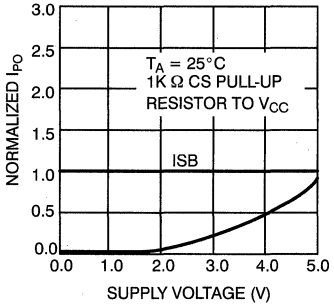




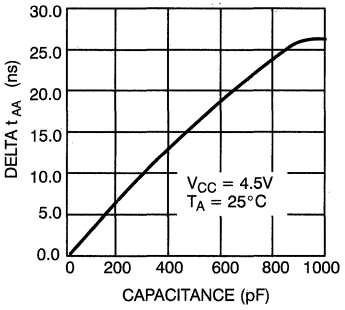


Typical DC and AC Characteristics

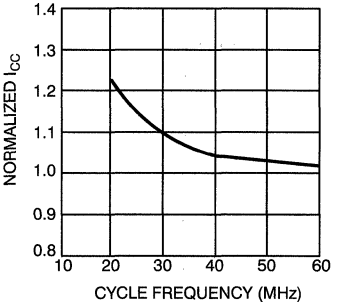
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. ACCESS TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C148–25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C148–35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148–35DMB	D4	18-Lead (300-Mil) CerDIP	Military
45	CY7C148–45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C148–45DMB	D4	18-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C149–25PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
35	CY7C149–35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149–35DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149–35LMB	L50	18-Pin Rectangular Leadless Chip Carrier	
45	CY7C149–45PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
	CY7C149–45DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C149–45LMB	L50	18-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[14]	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[14]	7, 8, 9, 10, 11
t_{ACS2}[14]	7, 8, 9, 10, 11
t_{ACS}[15]	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WP}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{DW}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

Notes:
14 7C148 only.
15. 7C149 only.

Document #: 38−00031−D

CY7C150

1K x 4 Static RAM

Features

- **Memory reset function**
- **1024 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 10 ns (commercial)**
  - **— 12 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 550 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance in both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C150 is a high-performance CMOS static RAM designed for use in cache memory, high-speed graphics, and data-acquisition applications. The CY7C150 has a memory reset feature that allows the entire memory to be reset in two memory cycles.

Separate I/O paths eliminates the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are three-stated during write, reset, deselect, or when output enable ($\overline{OE}$) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device ($\overline{CS}$ = LOW) and taking the reset ($\overline{RS}$) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be employed, with only selected devices being cleared at any given time.

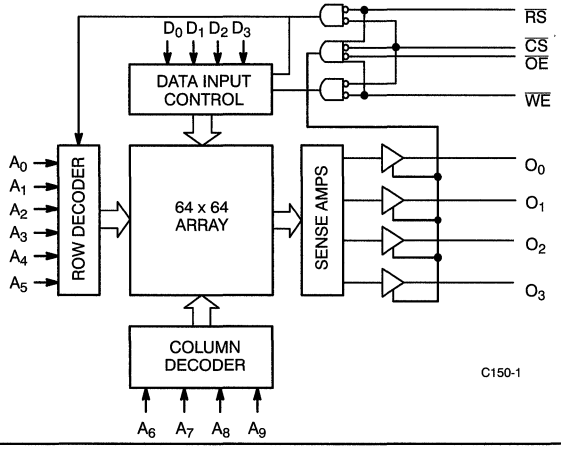
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data inputs (D_0–D_3) is written into the memory location specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

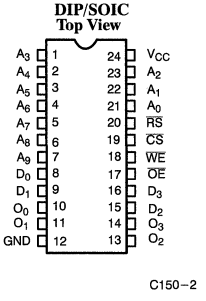
The output pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or reset ($\overline{RS}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C150–10	7C150–12	7C150–15	7C150–25	7C150–35
Maximum Access Time (ns)	Commercial	10	12	15	25	
	Military		12	15	25	35
Maximum Operating Current (mA)	Commercial	90	90	90	90	90
	Military		100	100	100	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

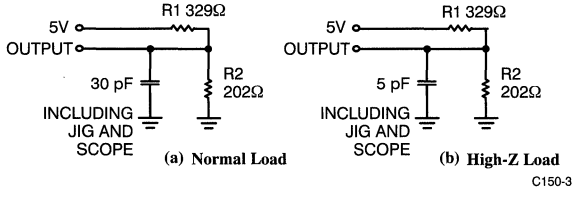
Electrical Characteristics Over the Operating Range[2]

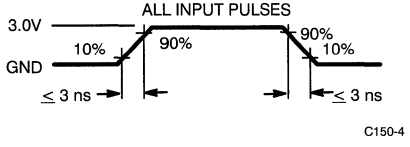
Parameter	Description	Test Conditions		7C150 Min.	7C150 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 0.4 mA		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 12 mA			0.4	V
V_{IH}	Input HIGH Level			2.0	V_{CC}	V
V_{IL}	Input LOW Level			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Current (High Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90	mA
			Military		100	mA

Capacitance[4]

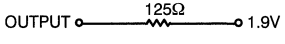
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 5]

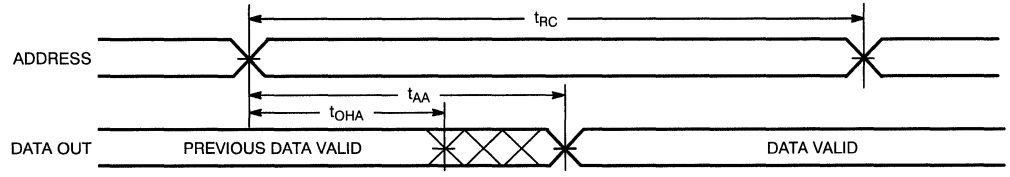
Parameter	Description	7C150–10		7C150–12		7C150–15		7C150–25		7C150–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	10		12		15		25		35		ns
t_{AA}	Address to Data Valid		10		12		15		25		35	ns
t_{OHA}	Output Hold from Address Change	2		2		2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		8		10		12		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		6		8		11		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		8		9		20		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	10		12		15		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	6		8		11		15		20		ns
t_{AW}	Address Set-Up to Write End	8		10		13		20		30		ns
t_{HA}	Address Hold from Write End	2		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		8		11		15		20		ns
t_{SD}	Data Set-Up to Write End	6		8		11		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		8		12		20		25	ns
RESET CYCLE												
t_{RRC}	Reset Cycle Time	20		24		30		50		70		ns
t_{SAR}	Address Valid to Beginning of Reset	0		0		0		0		0		ns
t_{SWER}	Write Enable HIGH to Beginning of Reset	0		0		0		0		0		ns
t_{SCSR}	Chip Select LOW to Beginning of Reset	0		0		0		0		0		ns
t_{PRS}	Reset Pulse Width	10		12		15		20		30		ns
t_{HCSR}	Chip Select Hold After End of Reset	0		0		0		0		0		ns
t_{HWER}	Write Enable Hold After End of Reset	8		12		15		30		40		ns
t_{HAR}	Address Hold After End of Reset	10		12		15		30		40		ns
t_{LZRS}	Reset HIGH to Output in Low Z[6]	0		0		0		0		0		ns
t_{HZRS}	Reset LOW to Output in High Z[6, 7]		6		8		12		20		25	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCS}, t_{HZOE}, t_{HZR}, and t_{HZWE} are tested with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be reference to the rising edge of the signal that terminates the write.

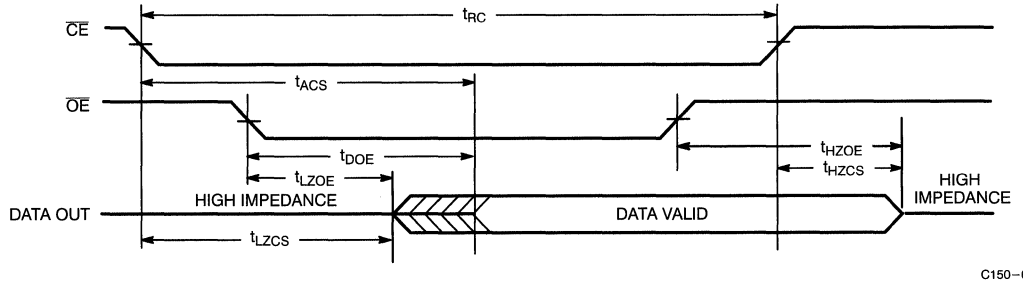
Switching Waveforms

Read Cycle No. 1[9, 10]



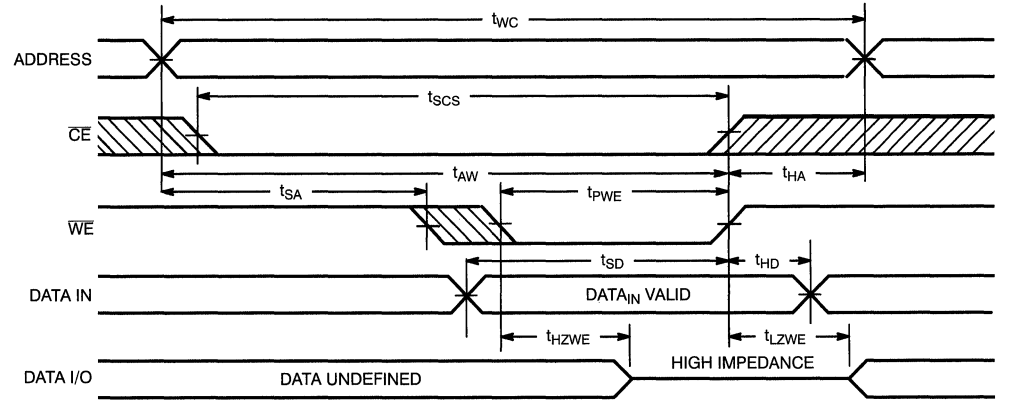
C150–5

Read Cycle No. 2[9, 11]



C150–6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]

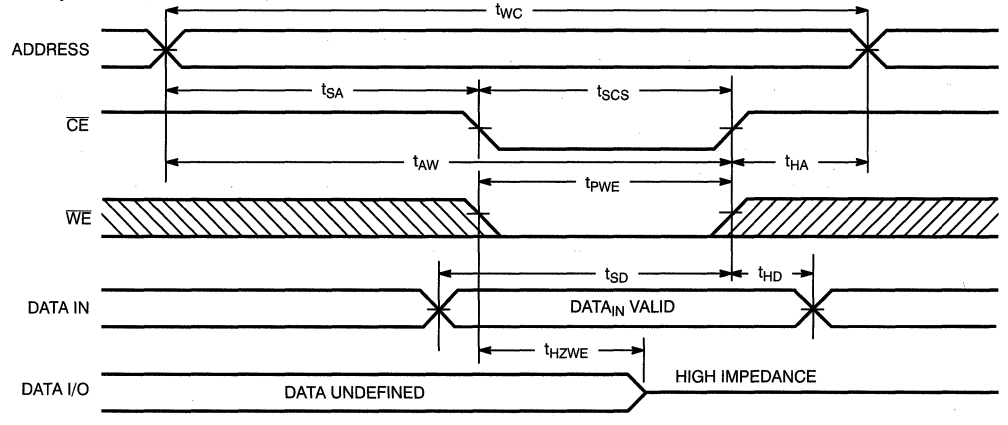


C150–7

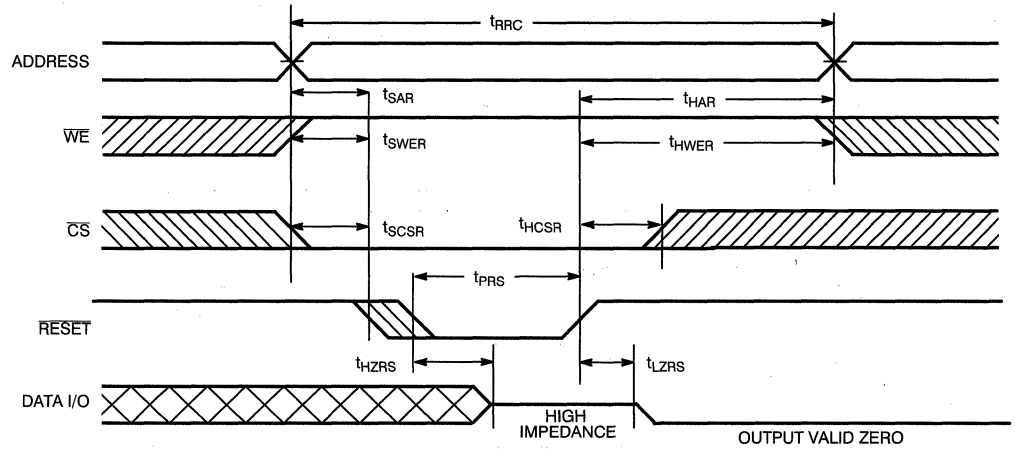
Notes:
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ and $\overline{OE}$ = V_{IL}.
11. Address prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[8, 12]



Reset Cycle[13]

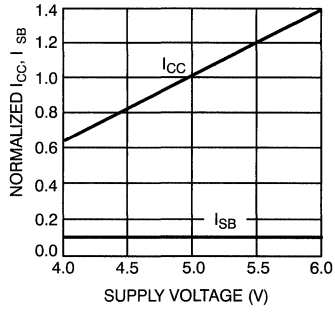


Notes:

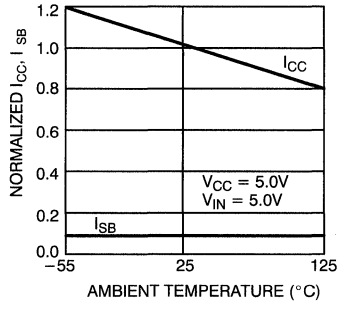
12. If $\overline{CS}$ goes HIGH with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
13. Reset cycle is defined by the overlap of $\overline{RS}$ and $\overline{CS}$ for the minimum reset pulse width.

Typical DC and AC Characteristics

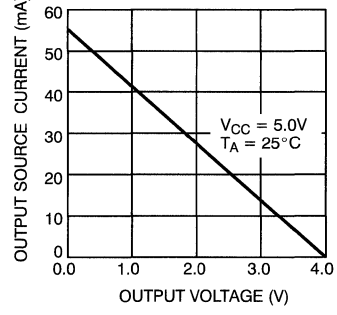
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



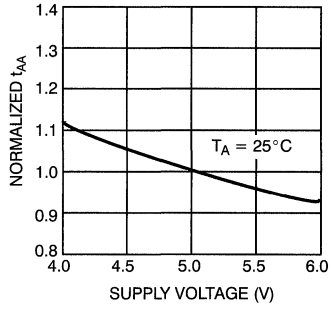
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



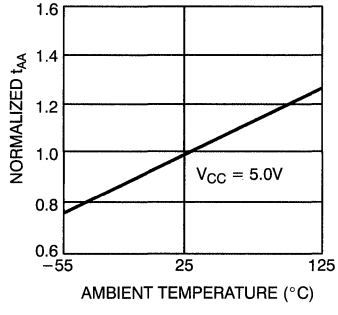
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



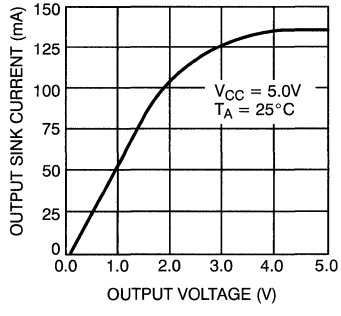
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



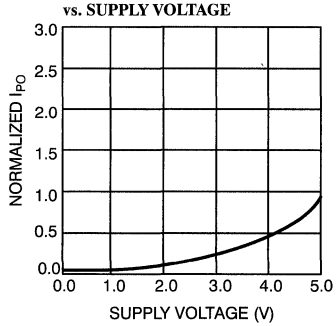
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



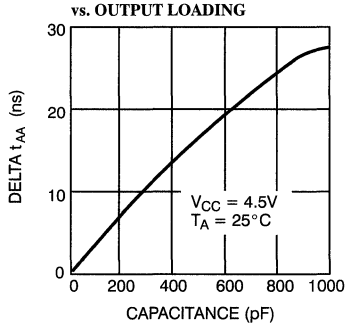
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



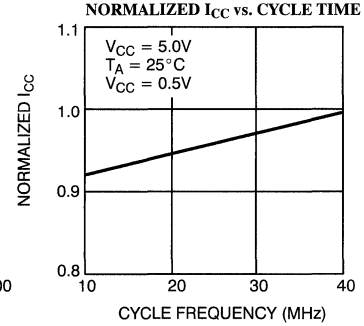
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

Inputs				Outputs	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{RS}$		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O_0-O_3	Read
L	X	H	H	High Z	Output Disable

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C150–10PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–10SC	S13	24-Lead Molded SOIC	
12	CY7C150–12PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–12SC	S13	24-Lead Molded SOIC	
	CY7C150–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C150–15PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–15SC	S13	24-Lead Molded SOIC	
	CY7C150–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C150–25PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–25SC	S13	24-Lead Molded SOIC	
	CY7C150–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C150–35DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
RESET CYCLE	
t_{RRC}	7, 8, 9, 10, 11
t_{SAR}	7, 8, 9, 10, 11
t_{SWER}	7, 8, 9, 10, 11
t_{SCSR}	7, 8, 9, 10, 11
t_{PRS}	7, 8, 9, 10, 11
t_{HCSR}	7, 8, 9, 10, 11
t_{HWER}	7, 8, 9, 10, 11
t_{HAR}	7, 8, 9, 10, 11

Document #: 38–00028–F

CY7C161
CY7C162

16K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **15-ns**
- **Transparent write (7C161)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **633 mW**
- **Low standby power**
  - **220 mW**
- **TTL compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C161 and CY7C162 are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 65% when deselected.

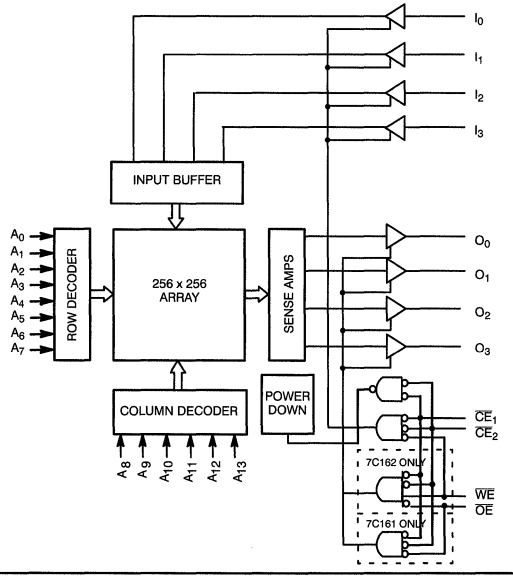
Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in a high-impedance state when write enable ($\overline{WE}$) is LOW (7C162 only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

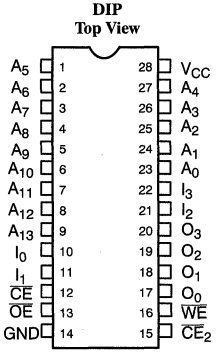
A die coat is used to ensure alpha immunity.

Logic Block Diagram



C162-1

Pin Configurations



C162-2

Selection Guide[1]

	7C161–12 7C162–12	7C161–15 7C162–15	7C161–20 7C162–20	7C161–25 7C162–25	7C161–35 7C162–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded areas indicate preliminary information.

Note:
1. For military specifications, see the CY7C161A/CY7C162A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C161−12 7C162−12		7C161−15 7C162−15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		160		115	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} Min. Duty Cycle = 100%		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20	mA

Shaded areas indicate preliminary information.

Electrical Characteristics Over the Operating Range (continued)

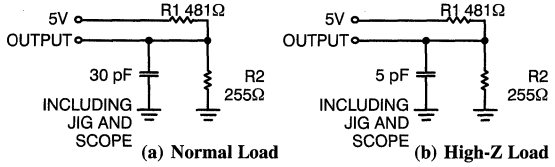
Parameter	Description	Test Conditions	7C161–20 7C162–20		7C161–25,35 7C162–25,35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		80		70	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} Min. Duty Cycle = 100%		40		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20	mA

Capacitance[4]

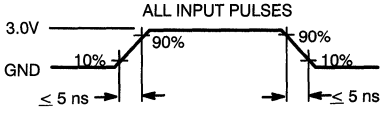
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
2. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

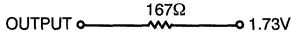


C162-3



C162-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5, 6]

Parameter	Description	7C161–12 7C162–12		7C161–15 7C162–15		7C161–20 7C162–20		7C161–25 7C162–25		7C161–35 7C162–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		10		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		7		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		7		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		20	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	8		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		12		15		15		20		ns
t_{SD}	Data Set-Up to Write End	6		10		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7] (7C162)	3		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8] (7C162)		6		7		7		7		10	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C161)		12		15		20		25		30	ns
t_{ADV}	Data Valid to Output Valid (7C161)		12		15		20		20		30	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns

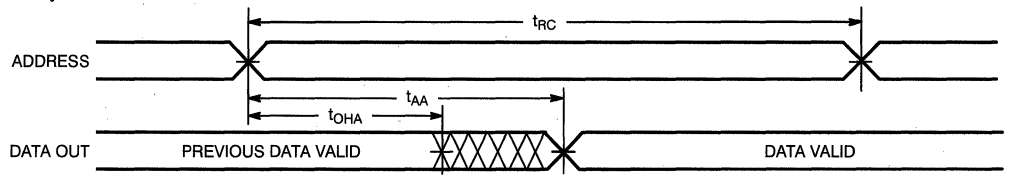
Shaded areas indicate preliminary information.

Notes:

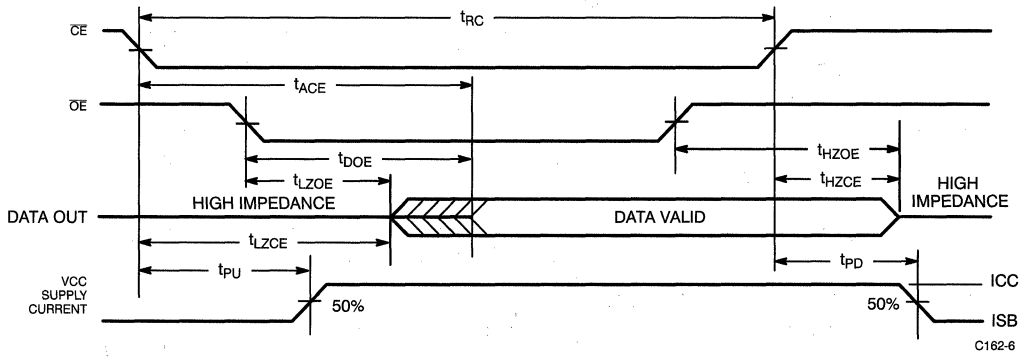
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms[8]

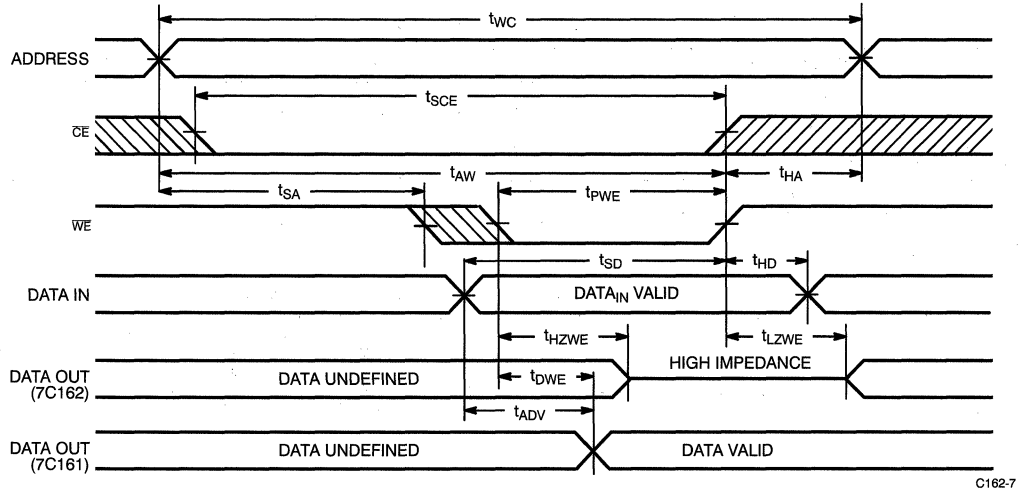
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



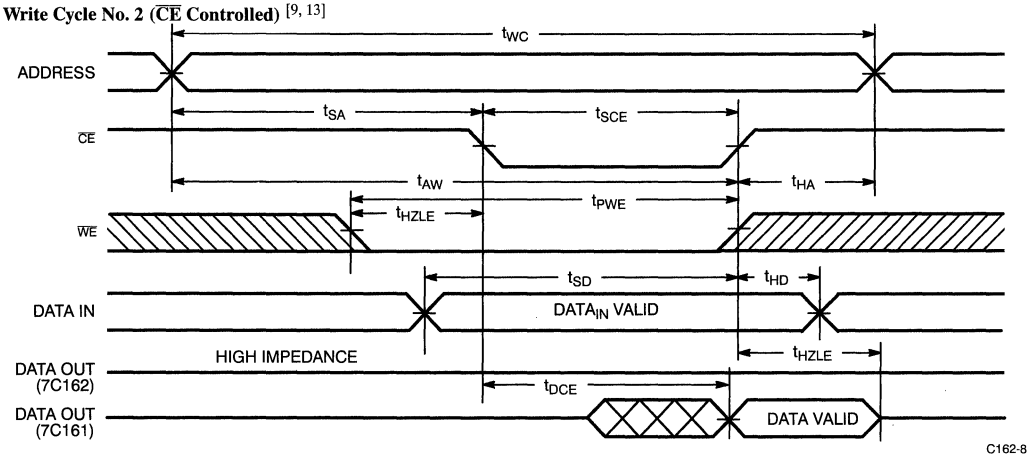
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.

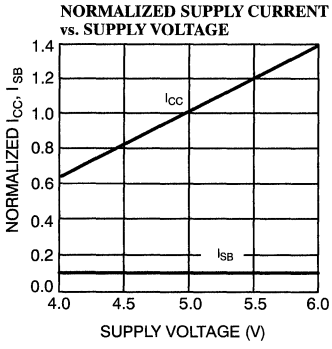
Switching Waveforms[8] (continued)

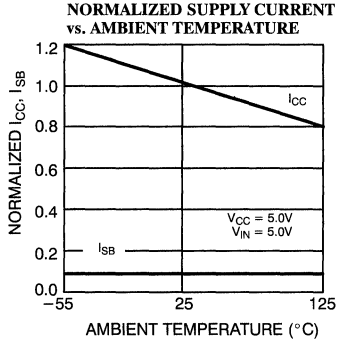
Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13]

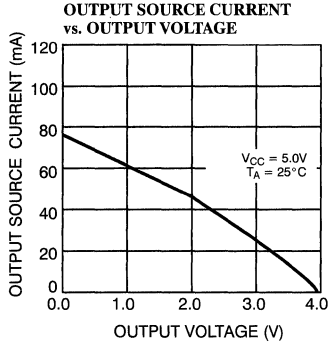


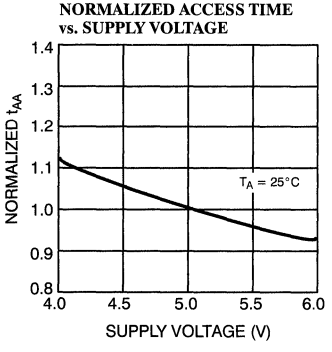
Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162 only).

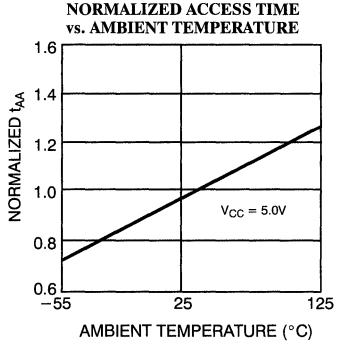
Typical DC and AC Characteristics

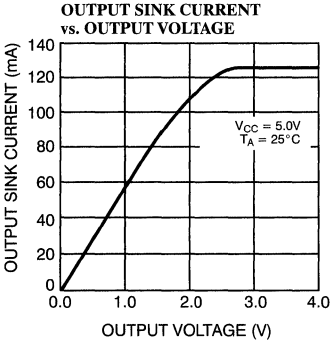






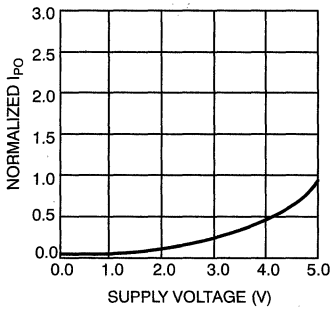




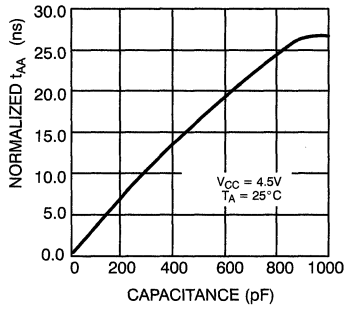


Typical DC and AC Characteristics (continued)

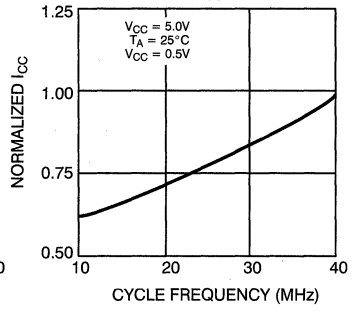
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C161-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-12VC	V21	28-Lead Molded SOJ	
15	CY7C161-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-15VC	V21	28-Lead Molded SOJ	
20	CY7C161-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-20VC	V21	28-Lead Molded SOJ	
25	CY7C161-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-25VC	V21	28-Lead Molded SOJ	
35	CY7C161-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C161-35VC	V21	28-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C162-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-12VC	V21	28-Lead Molded SOJ	
15	CY7C162-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-15VC	V21	28-Lead Molded SOJ	
20	CY7C162-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-20VC	V21	28-Lead Molded SOJ	
25	CY7C162-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-25VC	V21	28-Lead Molded SOJ	
35	CY7C162-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C162-35VC	V21	28-Lead Molded SOJ	

Shaded areas indicate preliminary information.

Document #: 38-00029-I

CY7C161A
CY7C162A

16K x 4 Static RAM with Separate I/O

Features

- **High speed**
  — 20 ns t_{AA}
- **CMOS for optimum speed/power**
- **Transparent write (7C161A)**
- **Low active power**
  — 550 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organizes as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

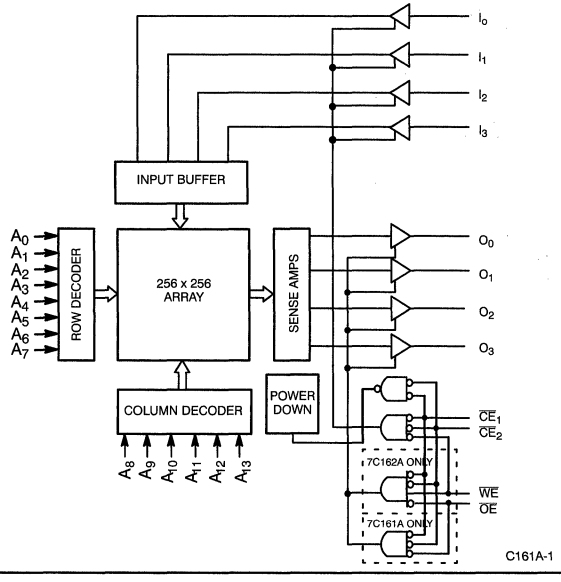
Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

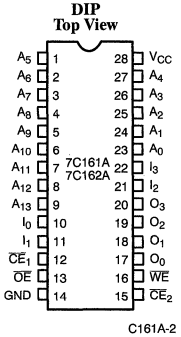
The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C162A only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

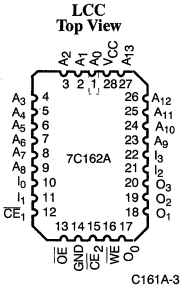
A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configurations





Selection Guide[1]

		7C161A–15 7C162A–15	7C161A–20 7C162A–20	7C161A–25 7C162A–25	7C161A–35 7C162A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	100	100	100
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

Note:
1. For commercial specifications, see the CY7C161/CY7C162 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	−55°C to +125°C	5V ± 10%

Notes:

2. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C161A−15 7C162A−15 Min.	7C161A−15 7C162A−15 Max.	7C161A−20 7C162A−20 Min.	7C161A−20 7C162A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		160		100	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Military		20		20	mA

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range[4] (continued)

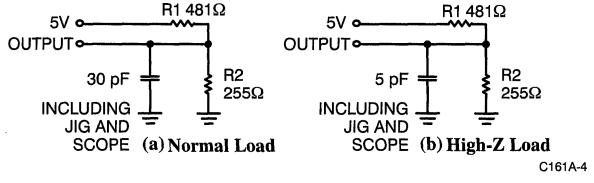
Parameter	Description	Test Conditions		7C161A–25 7C162A–25 Min.	7C161A–25 7C162A–25 Max.	7C161A–35 7C162A–35 Min.	7C161A–35 7C162A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		100		100	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Military		20		20	mA

Capacitance[6]

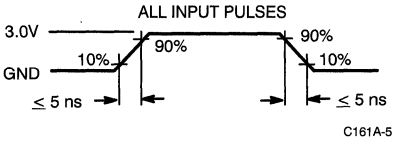
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

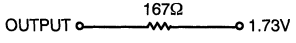


C161A-4



C161A-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 7, 8]

Parameter	Description	7C161A–15 7C162A–15		7C161A–20 7C162A–20		7C161A–25 7C162A–25		7C161A–35 7C162A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to HIGH Z		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9] (7C162A)	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10] (7C162A)		7		7		7		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C161A)		15		20		25		30	ns
t_{ADV}	Data Valid to Output Valid (7C161A)		15		20		20		30	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C161A)		15		20		25		35	ns

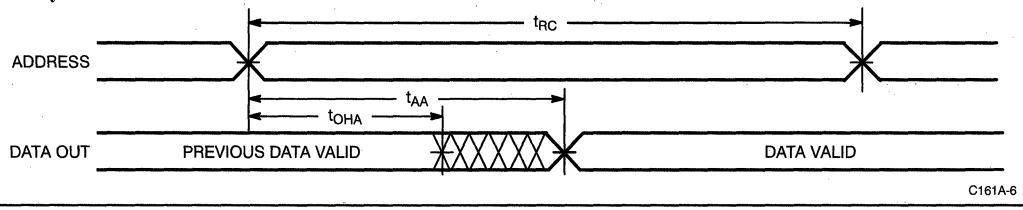
Shaded area contains preliminary information.

Notes:

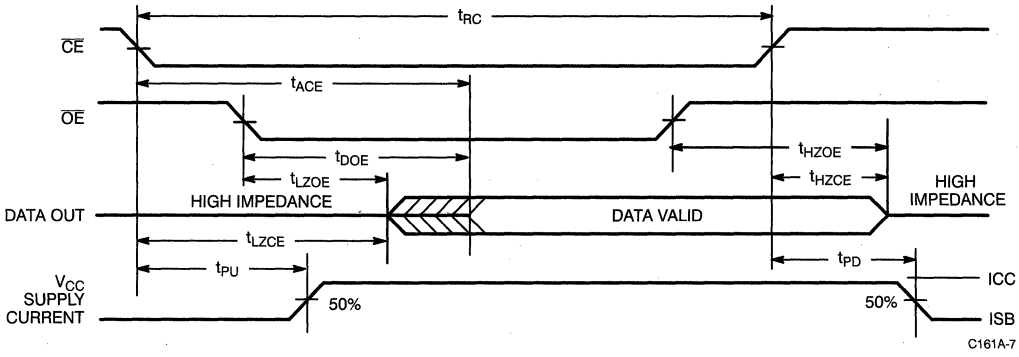
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
9. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms[8]

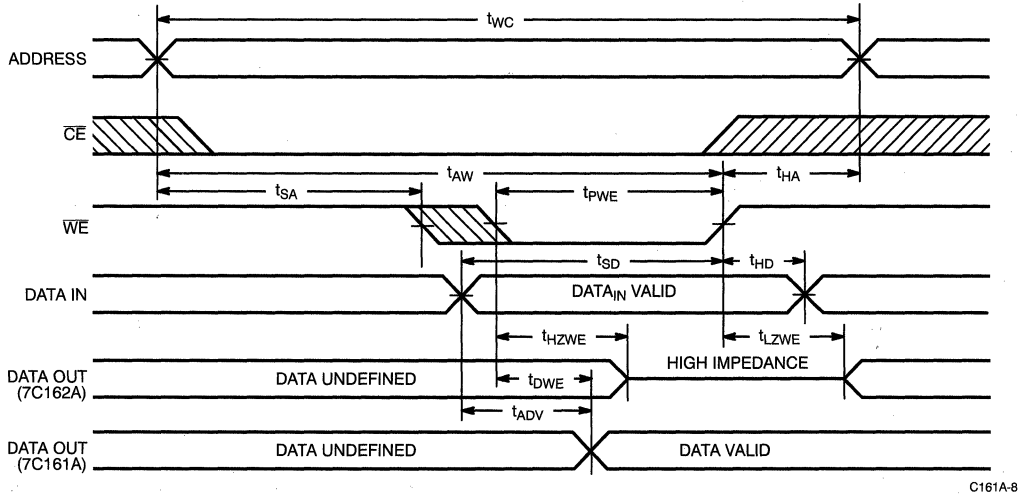
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



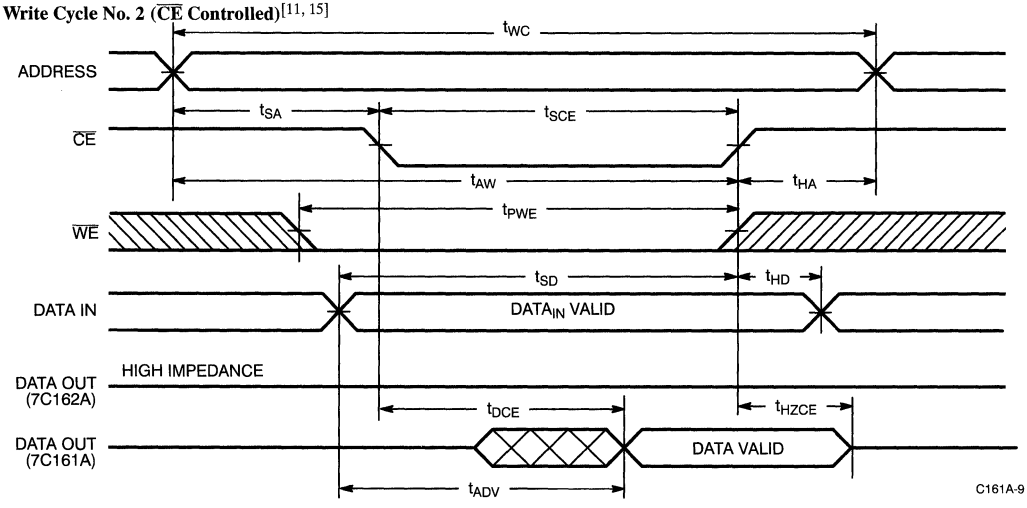
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
14. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.

Switching Waveforms (continued)

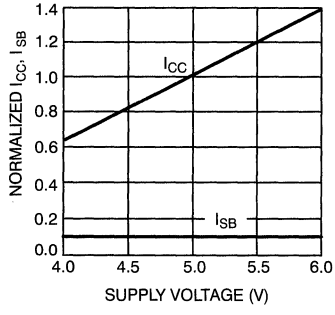
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15]



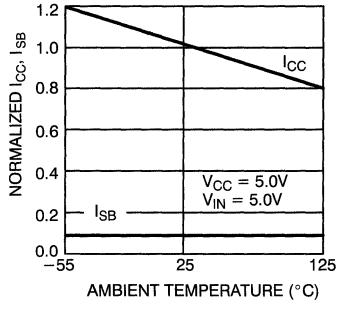
Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162A only).

Typical DC and AC Characteristics

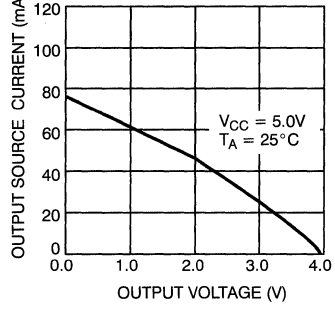
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

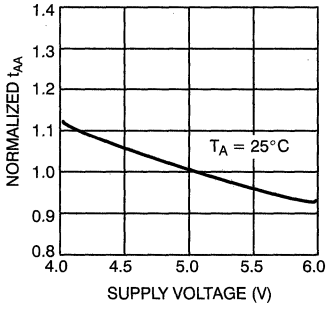


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

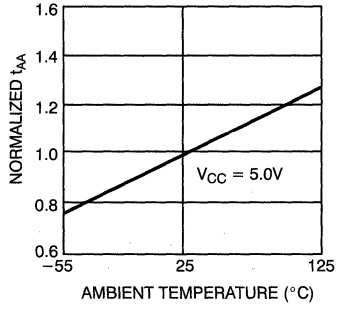


Typical DC and AC Characteristics (continued)

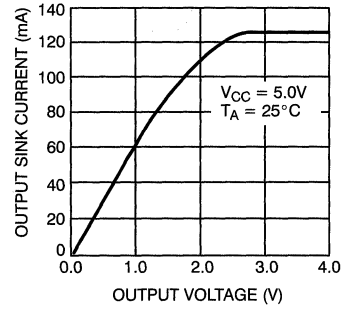
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



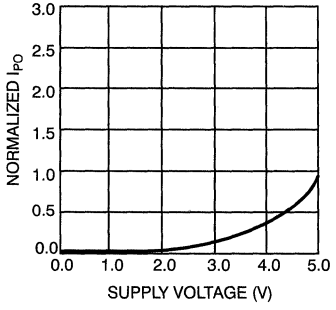
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



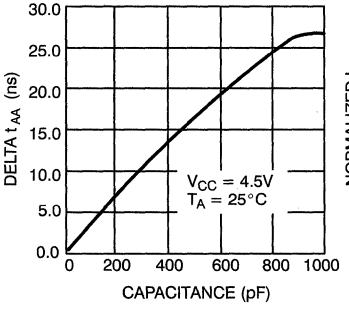
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



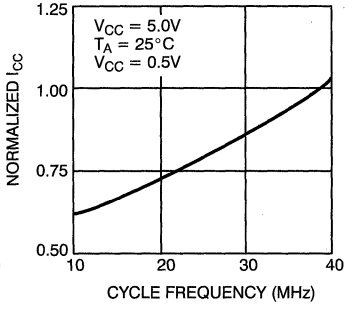
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C161A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C161A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C161A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
35	CY7C161A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C162A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C162A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C162A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C162A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}	7, 8, 9, 10, 11

Notes:
16. 7C161A only.

Document #: 38–00116–C

CY7C164
CY7C166

16K x 4 Static RAM

Features

- **High speed**
  — 15 ns
- **Output enable ($\overline{OE}$) feature (7C166)**
- **CMOS for optimum speed/power**
- **Low active power**
  — 633 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

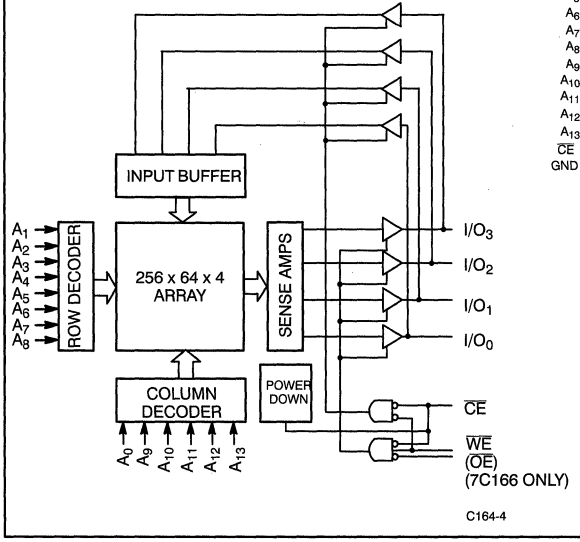
The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166 has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in a high-impedance state when chip enable ($\overline{CE}$) is HIGH (or output enable ($\overline{OE}$) is HIGH for 7C166). A die coat is used to insure alpha immunity.

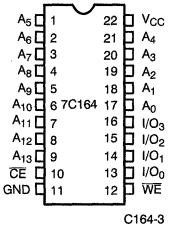
Logic Block Diagram



C164-4

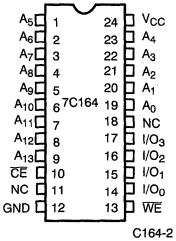
Pin Configurations

DIP
Top View



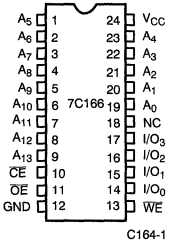
C164-3

SOJ
Top View



C164-2

DIP/SOJ
Top View



C164-1

Selection Guide[1]

	7C164–12 7C166–12	7C164–15 7C166–15	7C164–20 7C166–20	7C164–25 7C166–25	7C164–35 7C166–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded area contains preliminary information.

Note:
1. For military specifications, see the CY6C164A/CY7C166A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C164−12 7C166−12		7C164−15 7C166−15		7C164−20 7C166−20		7C164−25, 35 7C166−25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−350		−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		160		115		80		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%		40		40		40		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20		20		20	mA

Shaded area contains preliminary information.

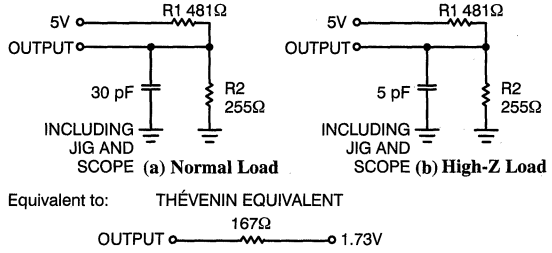
Capacitance[5]

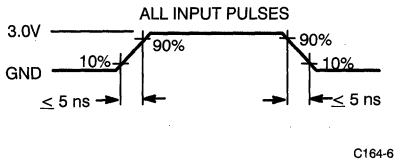
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[6]

Parameter	Description		7C164–12 7C166–12 Min.	7C164–12 7C166–12 Max.	7C164–15 7C166–15 Min.	7C164–15 7C166–15 Max.	7C164–20 7C166–20 Min.	7C164–20 7C166–20 Max.	7C164–25 7C166–25 Min.	7C164–25 7C166–25 Max.	7C164–35 7C166–35 Min.	7C164–35 7C166–35 Max.	Unit
READ CYCLE													
t_{RC}	Read Cycle Time		12		15		20		25		35		ns
t_{AA}	Address to Data Valid			12		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change		3		3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C166		6		10		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7C166	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	7C166		7		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]		3		3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]			7		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			12		15		20		20		20	ns
WRITE CYCLE[9]													
t_{WC}	Write Cycle Time		12		15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		8		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End		9		12		15		20		25		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		8		12		15		15		20		ns
t_{SD}	Data Set-Up to Write End		6		10		10		10		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		3		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]			6		7		7		7		10	ns

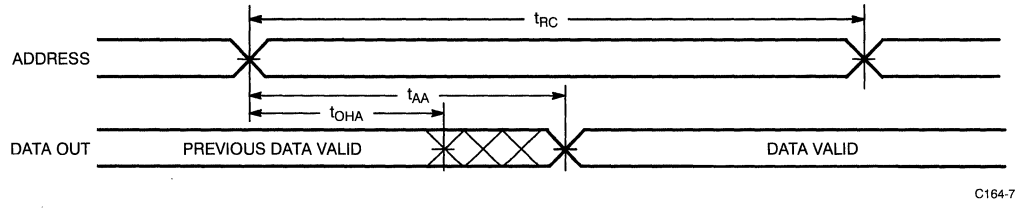
Shaded area contains preliminary information.

Notes:

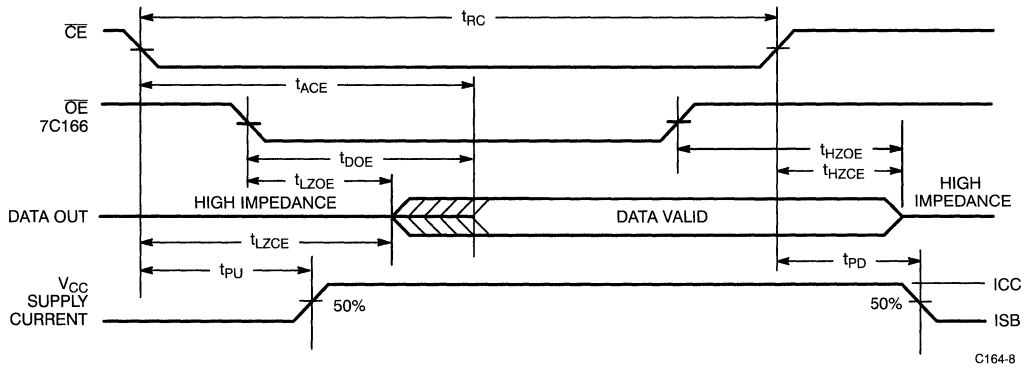
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed by design and not 100% tested.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

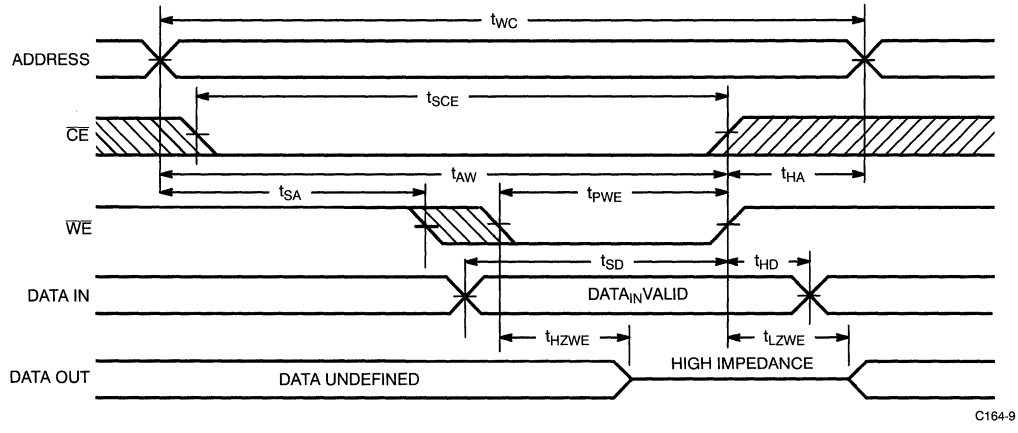
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



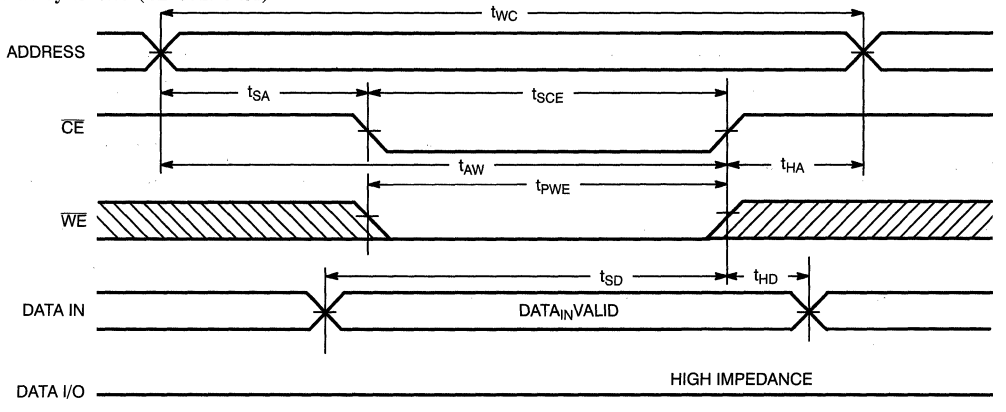
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7C166: $\overline{OE}$ = V_{IL} also).
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. 7C166 only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

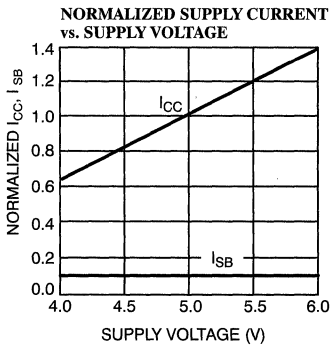
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13, 14]

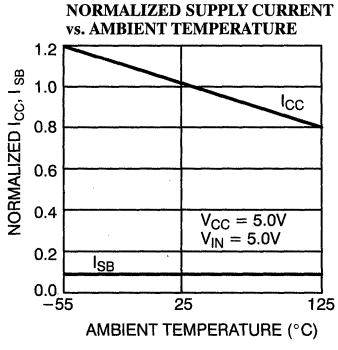


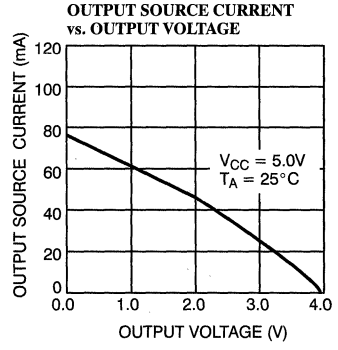
C164-10

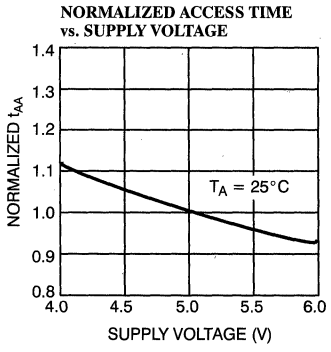
Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

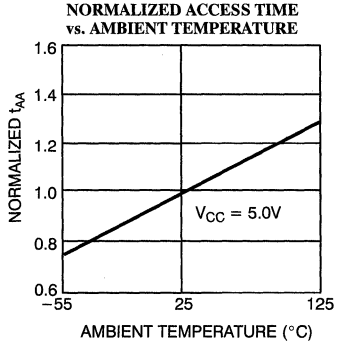
Typical DC and AC Characteristics

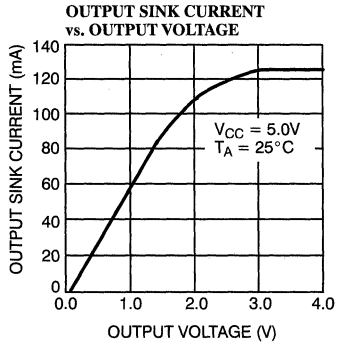




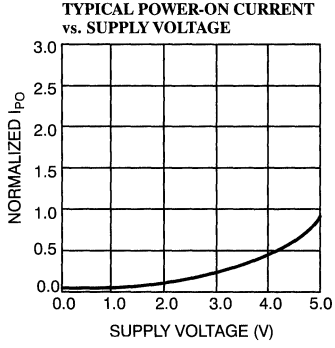


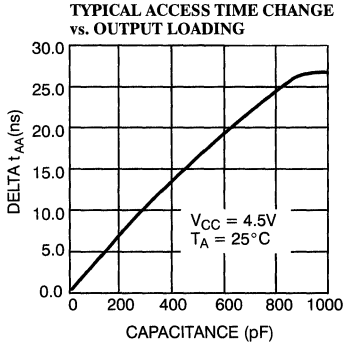


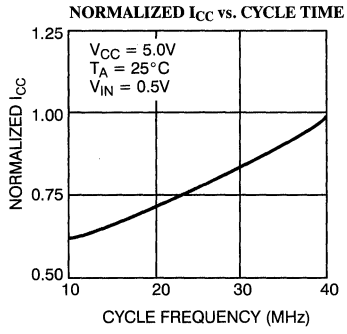




Typical DC and AC Characteristics (continued)







CY7C164 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

CY7C166 Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	H	Data In	Write
L	H	H	High Z	Write

Address Designators

Address Name	Address Function	CY 7C164 Pin Number	CY7C166 Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C164-12PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-12VC	V13	24-Lead Molded SOJ	
15	CY7C164-15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-15VC	V13	24-Lead Molded SOJ	
20	CY7C164-20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-20VC	V13	24-Lead Molded SOJ	
25	CY7C164-25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-25VC	V13	24-Lead Molded SOJ	
35	CY7C164-35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-35VC	V13	24-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C166-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-12VC	V13	24-Lead Molded SOJ	
15	CY7C166-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-15VC	V13	24-Lead Molded SOJ	
20	CY7C166-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-20VC	V13	24-Lead Molded SOJ	
25	CY7C166-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-25VC	V13	24-Lead Molded SOJ	
35	CY7C166-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-35VC	V13	24-Lead Molded SOJ	

Shaded areas contain preliminary information.

Document #: 38-00032-I

CY7C164A
CY7C166A

16K x 4 Static RAM

Features

- **High speed**
  - **20 ns**
- **Output enable ($\overline{OE}$) feature (7C166A)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **550 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C164A and CY7C166A are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166A has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

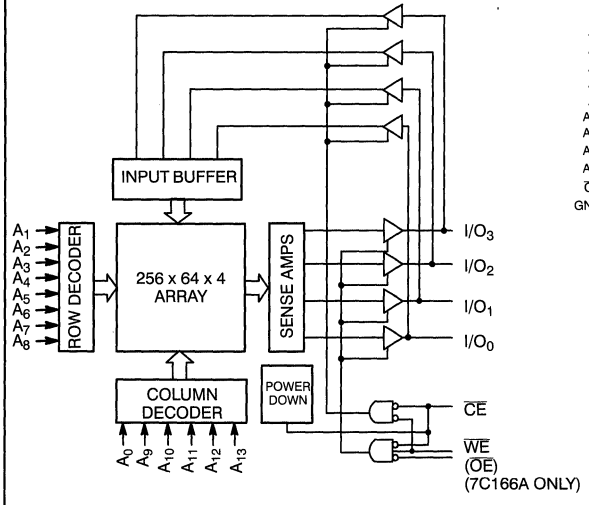
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166A). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166A), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or output enable ($\overline{OE}$) is HIGH for 7C166A.

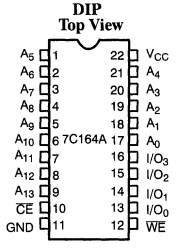
A die coat is used to ensure alpha immunity.

Logic Block Diagram

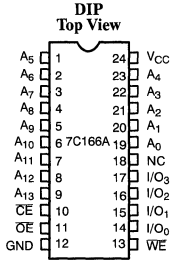


C164A-1

Pin Configurations



C164A-2



C164A-3

Selection Guide[1]

		7C164A-15 7C166A-15	7C164A-20 7C164A-20	7C164A-25 7C166A-25	7C164A-35 7C166A-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	100	100	100
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

Note:

1. For commercial specifications, see the CY7C164/CY7C166 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	−55°C to +125°C	5V ± 10%

Notes:

2. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C164A−15 7C166A−15 Min.	7C164A−15 7C166A−15 Max.	7C164A−20 7C166A−20 Min.	7C164A−20 7C166A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		160		100	mA
I_{SB1}	Automatic $\overline{CE}$[6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}$[6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Military		20		20	mA

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range [4](continued)

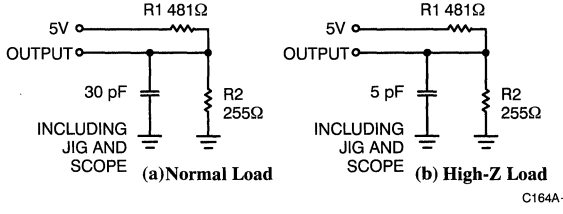
Parameter	Description	Test Conditions		7C164A–25 7C166A–25 Min.	7C164A–25 7C166A–25 Max.	7C164A–35 7C166A–35 Min.	7C164A–35 7C166A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		100		100	mA
I_{SB1}	Automatic $\overline{CE}$[6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}$[6] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Military		20		20	mA

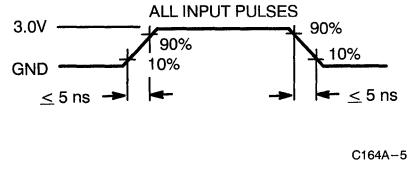
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

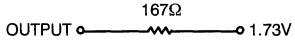
Notes:
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 8]

Parameter	Description	7C164A–15 7C166A–15		7C164A–20 7C166A–20		7C164A–25 7C166A–25		7C164A–35 7C166A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid (7C166A)		7		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z (7C166A)	0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z (7C166A)		8		8		10		12	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7		7		10	ns

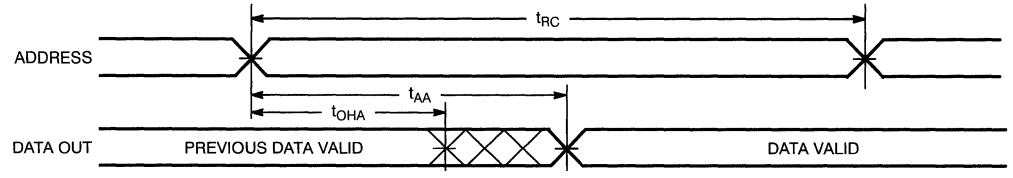
Shaded area contains preliminary information.

Notes:

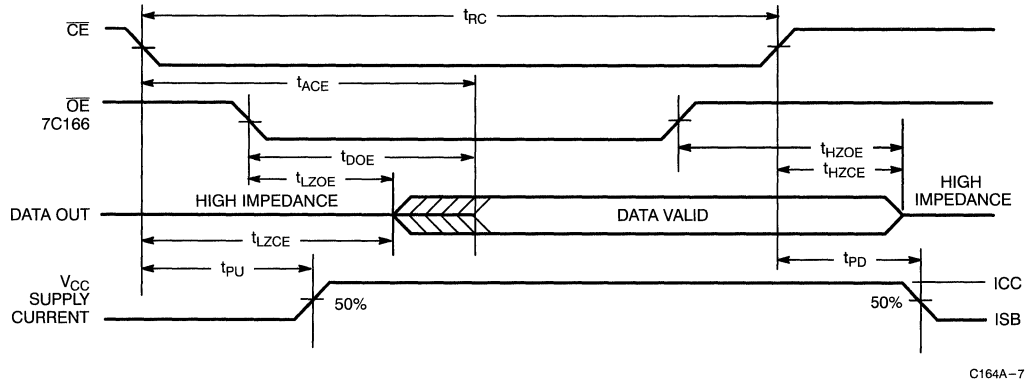
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed by design and not 100% tested.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

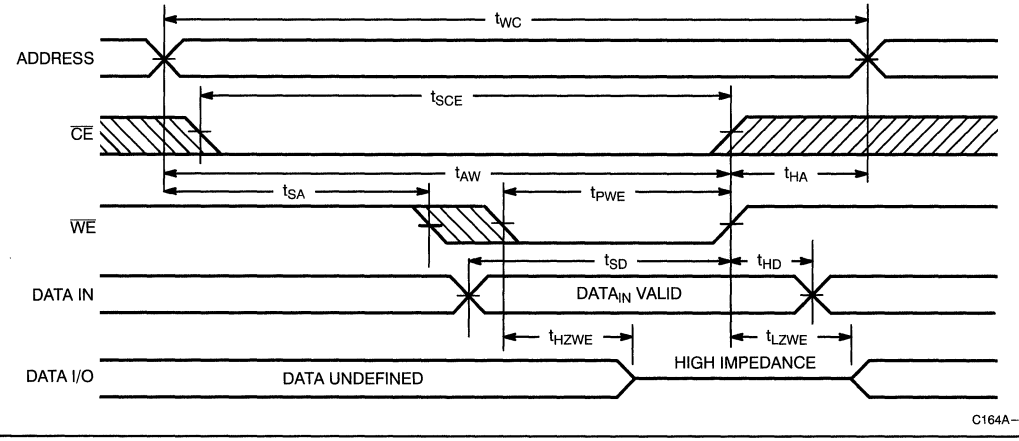
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



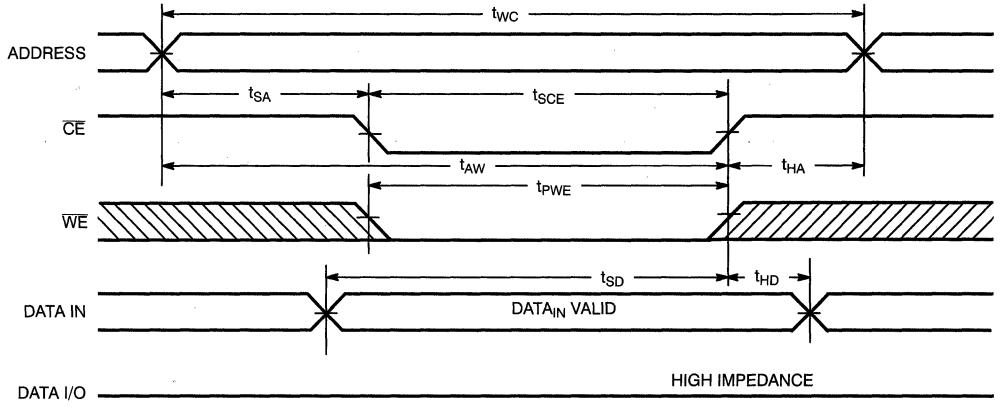
Write Cycle No. 1 (WE Controlled)[11, 15]



Notes:
12. WE is HIGH for read cycle.
13. Device is continuously selected, CE = V_{IL}. (7C166A OE = V_{IL} also).
14. Address valid prior to or coincident with CE transition LOW.
15. 7C166A only: Data I/O will be high impedance if OE = V_{IH}.

Switching Waveforms (continued)

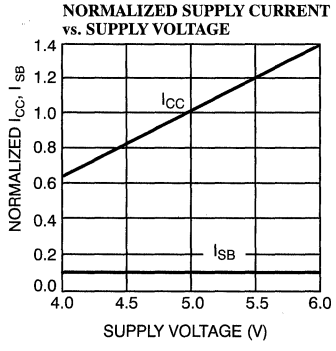
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15, 16]

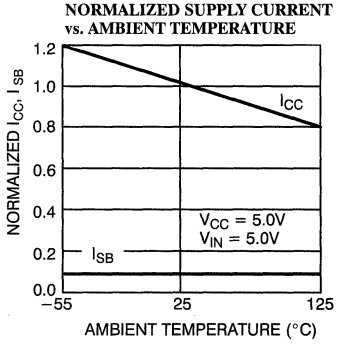


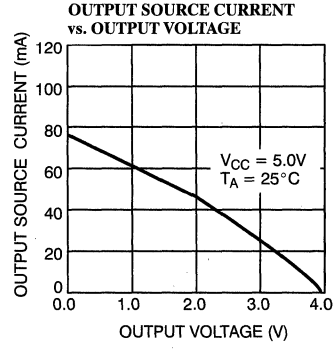
C164A–9

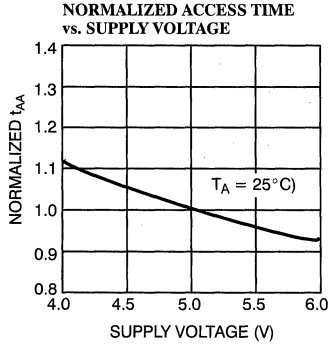
Note:
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

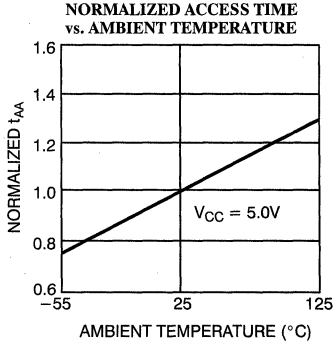
Typical DC and AC Characteristics

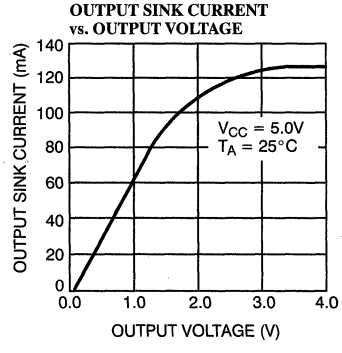




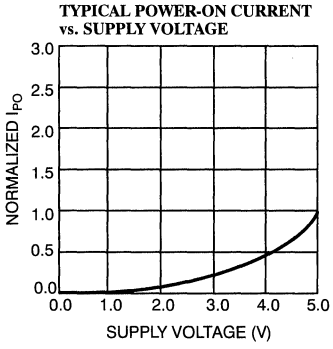


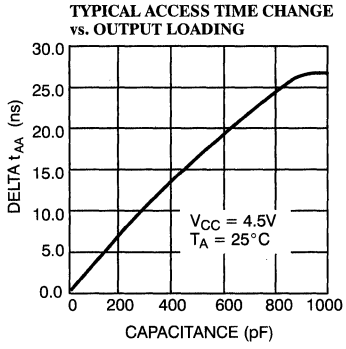


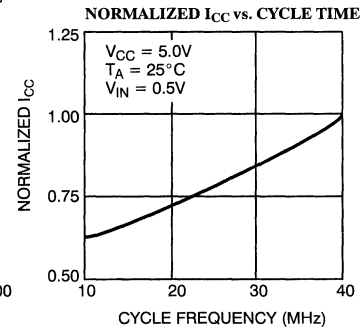




Typical DC and AC Characteristics (continued)







CY7C164A Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

CY7C166A Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	CY7C164A Pin Number	CY7C166A Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C164A–15DMB	D10	22-Lead (300-Mil) CerDIP	Military
20	CY7C164A–20DMB	D10	22-Lead (300-Mil) CerDIP	Military
25	CY7C164A–25DMB	D10	22-Lead (300-Mil) CerDIP	Military
35	CY7C164A–35DMB	D10	22-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7C166A–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7C166A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C166A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C166A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[17]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
17. 7C166A only.

16K x 1 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  — 15 ns
- **Low active power**
  — 275 mW
- **Low standby power**
  — 83 mW
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C167A is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C167A has an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

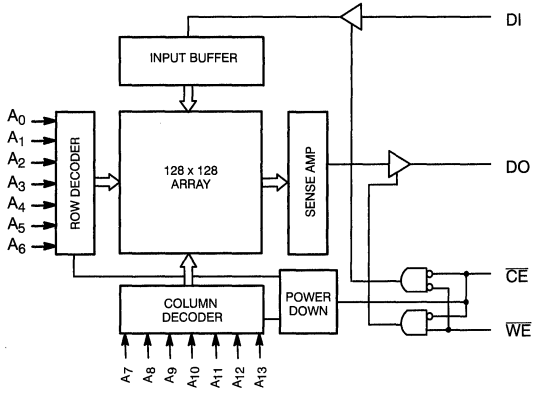
Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the data output (DO) pin.

The output pin remains in a high-impedance state when chip enable is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to ensure alpha immunity.

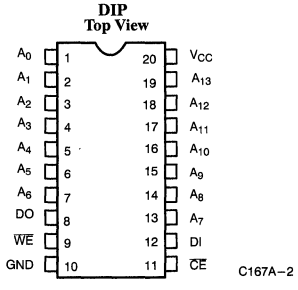
2

Logic Block Diagram



C167A–1

Pin Configuration



C167A–2

Selection Guide

		7C167A–15	7C167A–20	7C167A–25	7C167A–35	7C167A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	60	60	
	Military		80	70	60	50

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C167A−15 Min.	7C167A−15 Max.	7C167A−20 Min.	7C167A−20 Max.	7C167A−25 Min.	7C167A−25 Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2..4		2..4		2..4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		80		60	mA
			Mil				80		70	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40		20	mA
			Mil				40		20	

Parameter	Description	Test Conditions		7C167A−35 Min.	7C167A−35 Max.	7C167A−45 Min.	7C167A−45 Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2..4		2..4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[3]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		60		50	mA
			Mil		60		50	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20			mA
			Mil		20		20	

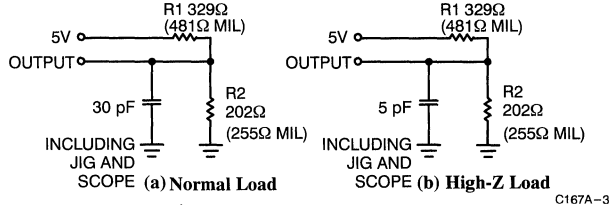
Notes:

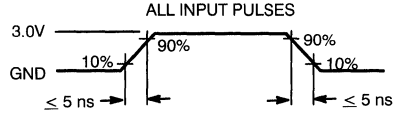
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Capacitance[6]

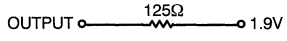
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF
C_{CE}	Chip Enable Capacitance		6	pF

AC Test Loads and Waveforms

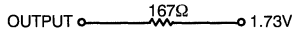




Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

Switching Characteristics Over the Operating Range[2, 7]

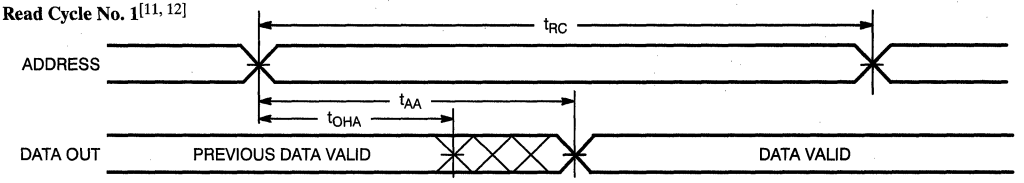
Parameter	Description		7C167A–15		7C167A–20		7C167A–25		7C167A–35		7C167A–45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE													
t_{RC}	Read Cycle Time	Com'l	15		20		25		30				ns
		Mil			20		25		35		40		ns
t_{AA}	Address to Data Valid	Com'l		15		20		25		30			ns
		Mil				20		25		35		40	ns
t_{OHA}	Data Hold from Address Change		5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]		5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]			8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			15		20		20		20		25	ns
WRITE CYCLE[10]													
t_{WC}	Write Cycle Time		15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]			7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]		5		5		5		5		5		ns

Notes:

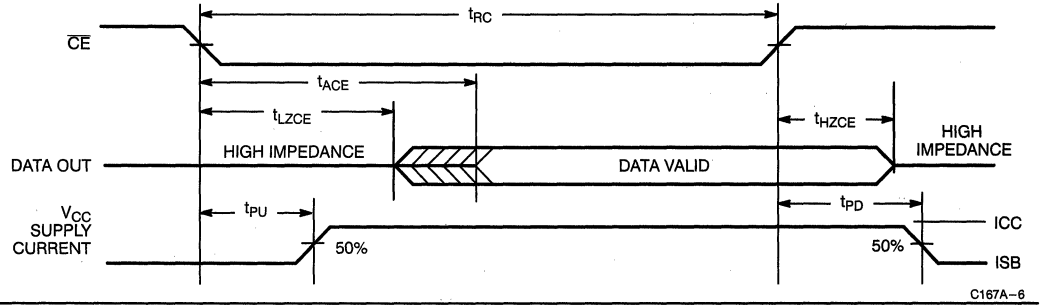
6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
9. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

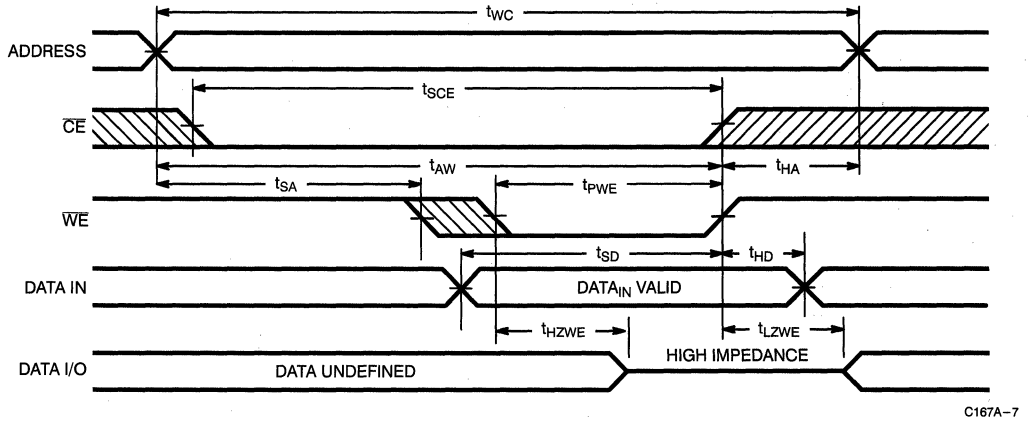
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



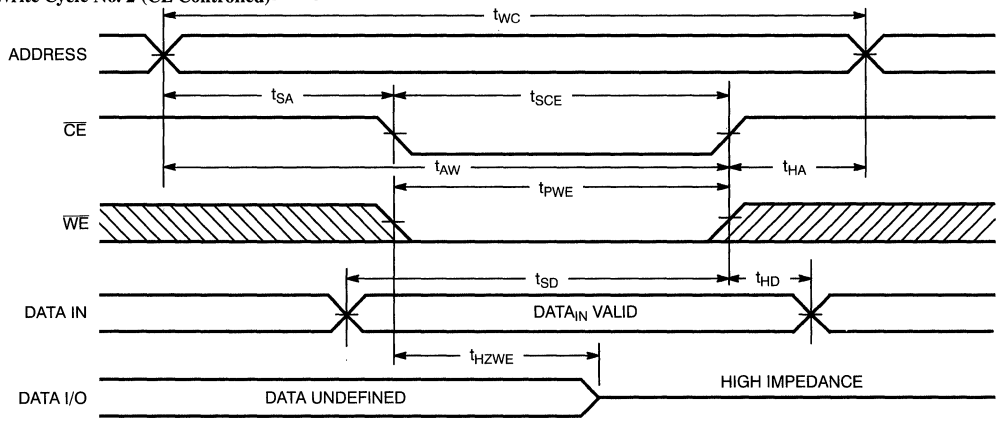
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



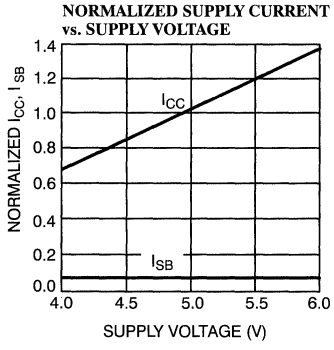
Notes:
11. $\overline{WE}$ is high for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

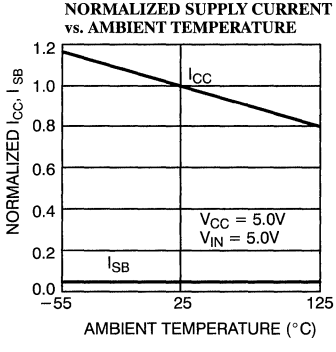
Switching Waveforms (continued)

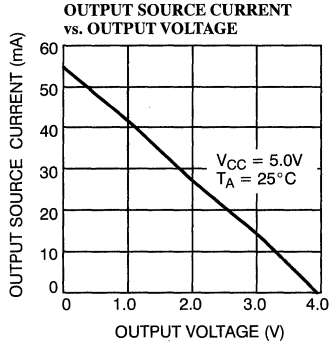
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

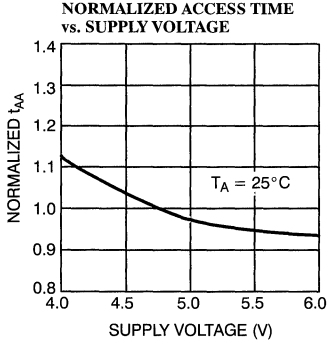


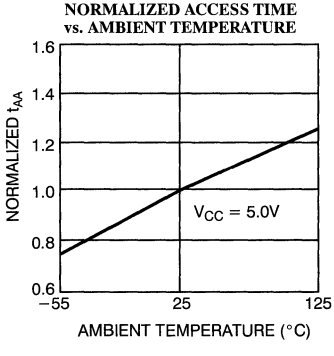
Typical DC and AC Characteristics

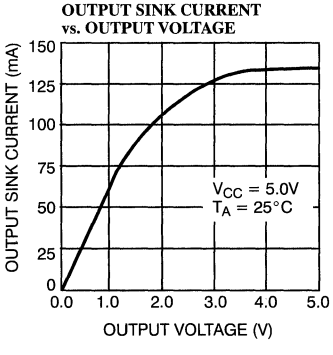




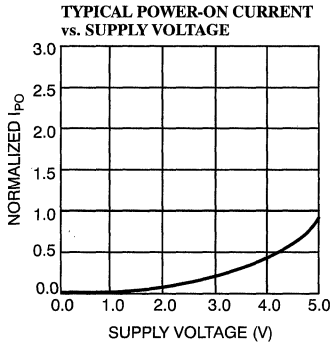


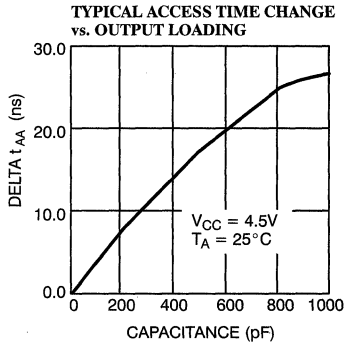


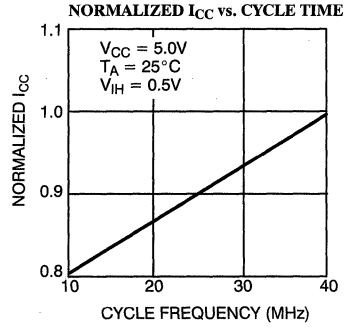




Typical DC and AC Characteristics (continued)







Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	80	CY7C167A–15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–15VC	V5	20-Lead Molded SOJ	
20	80	CY7C167A–20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–20VC	V5	20-Lead Molded SOJ	
		CY7C167A–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
25	60	CY7C167A–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–25VC	V5	20-Lead Molded SOJ	
		CY7C167A–25DMB	D6	20-Lead (300-Mil) CerDIP	Military
35	60	CY7C167A–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A–35VC	V5	20-Lead Molded SOJ	
		CY7C167A–35DMB	D6	20-Lead (300-Mil) CerDIP	Military
45	50	CY7C167A–45DMB	D6	20-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{OHA}	7,8,9,10,11
t_{ACE}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{SCE}	7,8,9,10,11
t_{AW}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{SA}	7,8,9,10,11
t_{PWE}	7,8,9,10,11
t_{SD}	7,8,9,10,11
t_{HD}	7,8,9,10,11

CY7C168A
CY7C169A

4K x 4 Static RAM

Features

- **Automatic power-down when deselected (CY7C168A)**
- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 15 ns**
  - **— t_{ACE} = 10 ns (CY7C169A)**
- **Low active power**
  - **— 385 mW**
- **Low standby power (CY7C168A)**
  - **— 83 mW**
- **TTL-compatible inputs and outputs**
- **V_{IH} of 2.2V**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C168A and CY7C169A are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

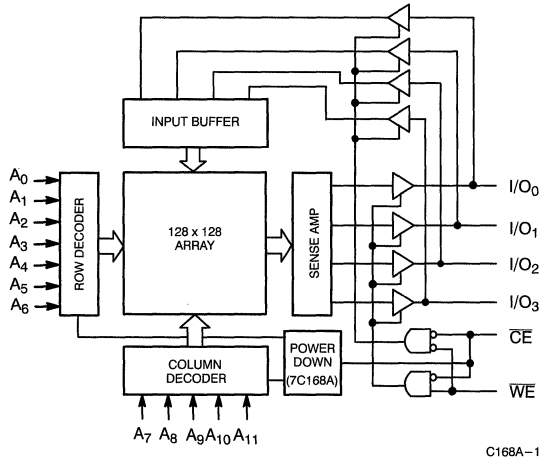
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when chip enable is HIGH or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

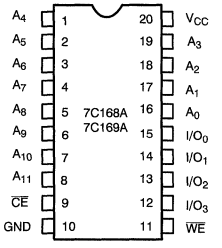
Logic Block Diagram



C168A–1

Pin Configurations

DIP/SOJ
Top View



C168A–2

Selection Guide

		7C168A–15 7C169A–15	7C168A–20 7C169A–20	7C168A–25 7C169A–25	7C168A–35 7C169A–35	7C168A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	90	70	70	
	Military		90	80	70	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C168A−15 7C169A−15 Min.	7C168A−15 7C169A−15 Max.	7C168A−20 7C169A−20 Min.	7C168A−20 7C169A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil				90	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40	mA
			Mil				40	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ VCC − 0.3 V	Com'l		20		20	mA
			Mil				20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

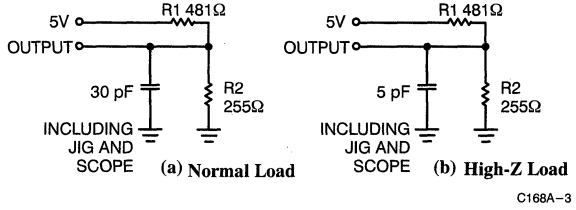
Electrical Characteristics Over the Operating Range[2] (continued)

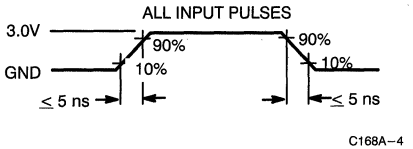
Parameter	Description	Test Conditions		7C168A–25 7C169A–25 Min.	7C168A–25 7C169A–25 Max.	7C168A–35 7C169A–35 Min.	7C168A–35 7C169A–35 Max.	7C168A–45 Min.	7C168A–45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−50	50	−50	50	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70			mA
			Mil		80		70		70	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20		20			mA
			Mil		20		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ VCC − 0.3 V	Com'l		20		20			mA
			Mil		20		20		20	

Capacitance[5]

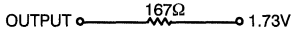
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:
5. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 6]

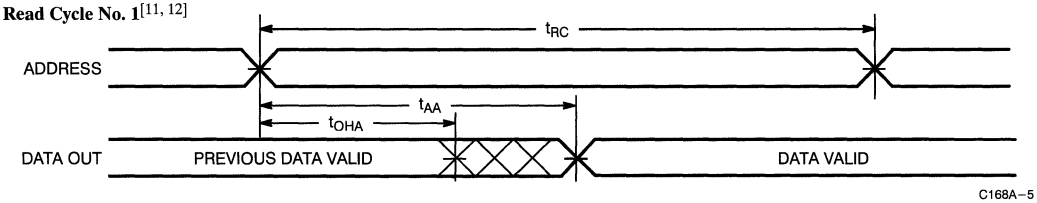
Parameter	Description		7C168A–15 7C169A–15 Min.	7C168A–15 7C169A–15 Max.	7C168A–20 7C169A–20 Min.	7C168A–20 7C169A–20 Max.	7C168A–25 7C169A–25 Min.	7C168A–25 7C169A–25 Max.	7C168A–35 7C169A–35 Min.	7C168A–35 7C169A–35 Max.	7C168A–45 Min.	7C168A–45 Max.	Unit
READ CYCLE													
t_{RC}	Read Cycle Time		15		20		25		35		45		ns
t_{AA}	Address to Data Valid			15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change		5		5		5		5		5		ns
t_{ACE}	Power Supply Current	7C168A		15		20		25		35		45	ns
		7C169A		10		12		15		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7, 8]		5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 9]			8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168A)		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down (7C168A)			15		20		20		20		25	ns
t_{RCS}	Read Command Set-Up		0		0		0		0		0		ns
t_{RCH}	Read Command Hold		0		0		0		0		0		ns
WRITE CYCLE[10]													
t_{WC}	Write Cycle Time		15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		7		7		7		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9]			5		5		5		10		15	ns

Notes:

6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, T_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
8. 3-ns minimum for the CY7C169A.
9. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition low.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

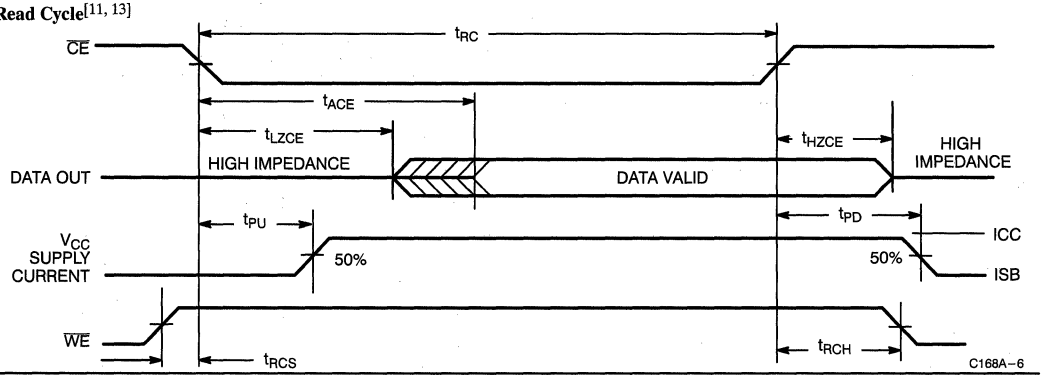
Read Cycle No. 1[11, 12]



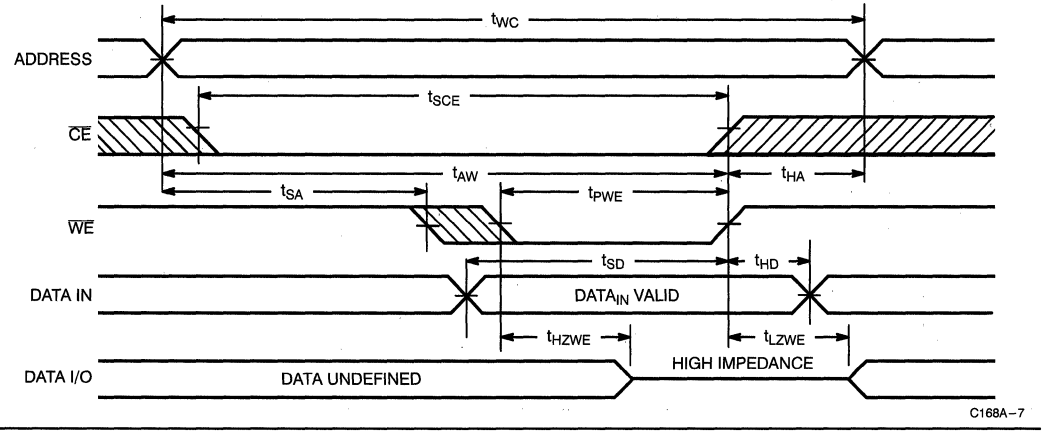
C168A–5

Switching Waveforms (continued)

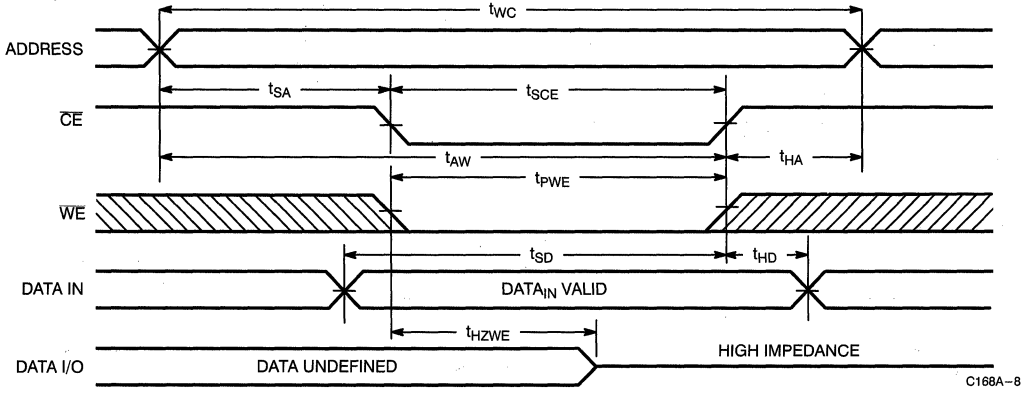
Read Cycle[11, 13]



Write Cycle No. 1 (WE Controlled)[10]

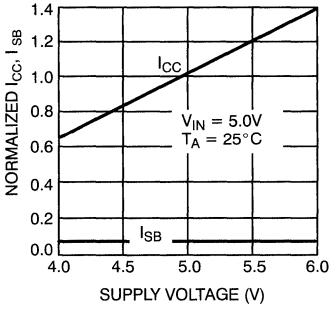


Write Cycle No. 2 (CS Controlled) [10, 14]

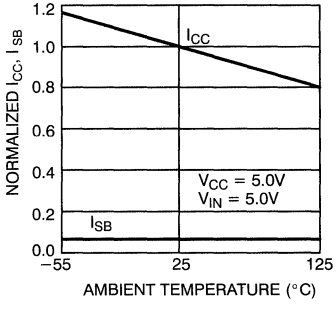


Typical DC and AC Characteristics

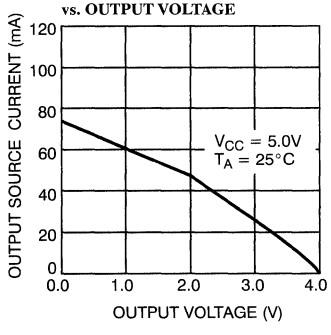
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



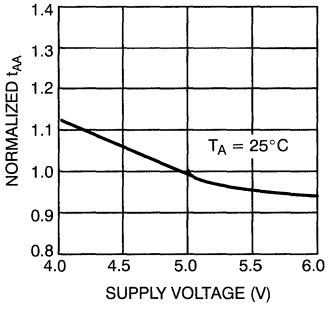
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



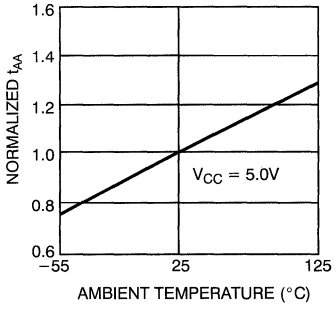
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



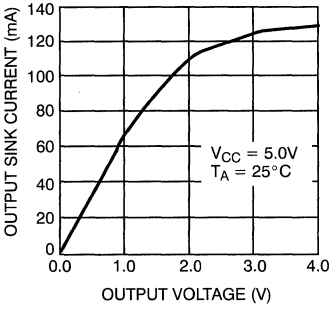
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



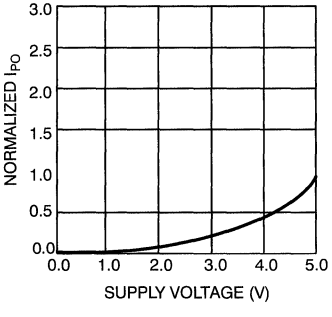
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



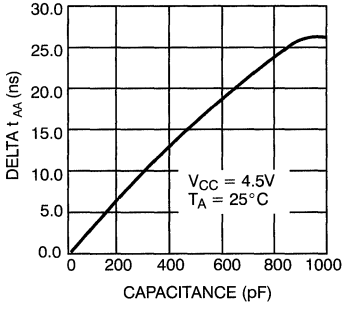
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



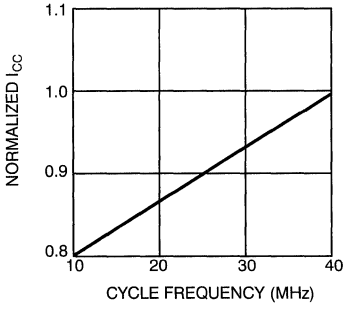
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C168A–15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–15VC	V5	20-Lead Molded SOJ	
20	90	CY7C168A–20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–20VC	V5	20-Lead Molded SOJ	
		CY7C168A–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
25	70	CY7C168A–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–25VC	V5	20-Lead Molded SOJ	
	80	CY7C168A–25DMB	D6	20-Lead (300-Mil) CerDIP	Military
35	70	CY7C168A–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A–35VC	V5	20-Lead Molded SOJ	
		CY7C168A–35DMB	D6	20-Lead (300-Mil) CerDIP	Military
45	70	CY7C168A–45DMB	D6	20-Lead (300-Mil) CerDIP	Military

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C169A–15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–15VC	V5	20-Lead Molded SOJ	
20	90	CY7C169A–20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–20VC	V5	20-Lead Molded SOJ	
25	70	CY7C169A–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–25VC	V5	20-Lead Molded SOJ	
35	70	CY7C169A–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C169A–35VC	V5	20-Lead Molded SOJ	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}[15]	1, 2, 3
I_{SB2}[15]	1, 2, 3

Note:
15. CY7C168A only.

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CY7C170A

4K x 4 Static RAM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 15 ns**
  - **— t_{ACS} = 10 ns**
- **Low active power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Output enable**
- **V_{IH} of 2.2V**

Functional Description

The CY7C170A is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$) and three-state drivers.

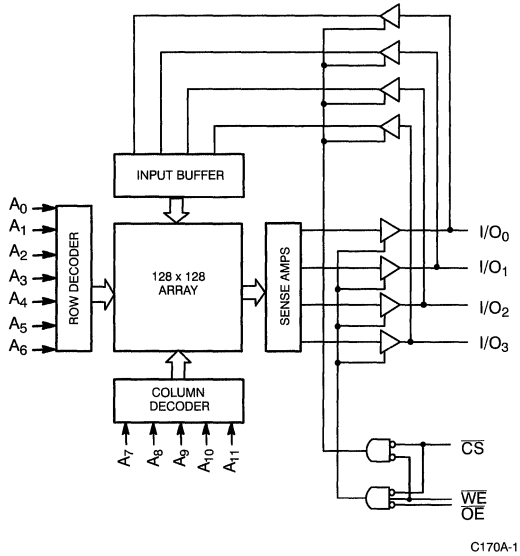
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to ensure alpha immunity.

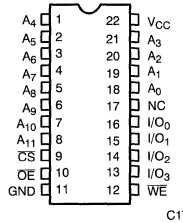
Logic Block Diagram



C170A-1

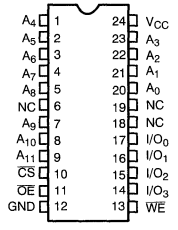
Pin Configurations

DIP
Top View



C170A-2

SOJ
Top View



C170A-3

Selection Guide

		7C170A–15	7C170A–20	7C170A–25	7C170A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Commercial	115	90	90	90
	Military			120	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 21) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C170A−15 Min.	7C170A−15 Max.	7C170A−20, 25, 35, 45 Min.	7C170A−20, 25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil				120	mA

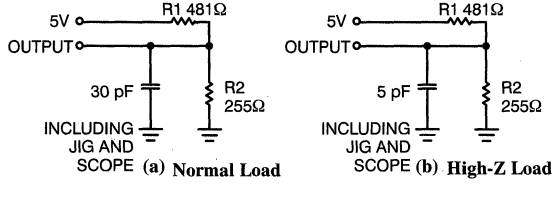
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

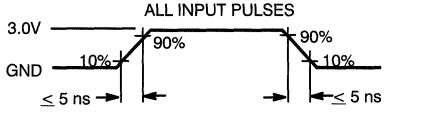
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

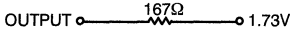


C170A-4



C170A-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 5]

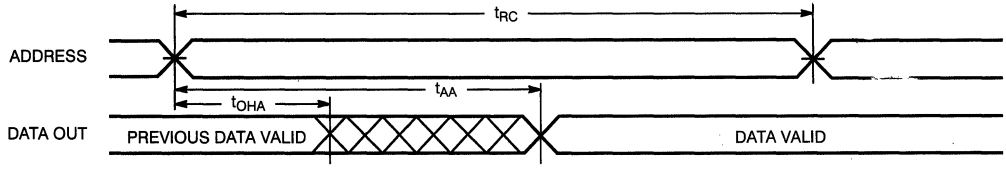
Parameter	Description	7C170A–15		7C170A–20		7C170A–25		7C170A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		10		15		15		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		8		8		10		12	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		8		8		10		15	ns
WRITE CYCLE[8]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ HIGH to High Z		7		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
6. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.

Switching Waveforms

Read Cycle No. 1[9, 10]



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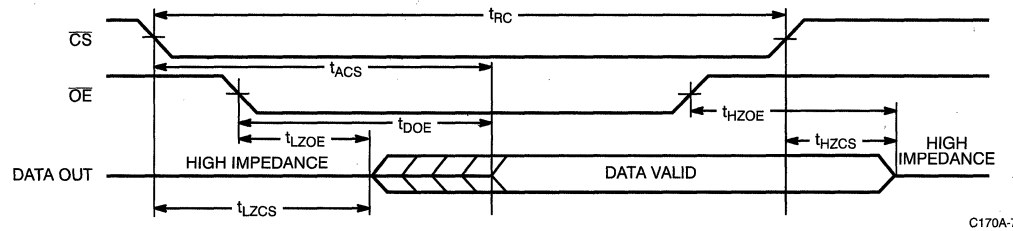
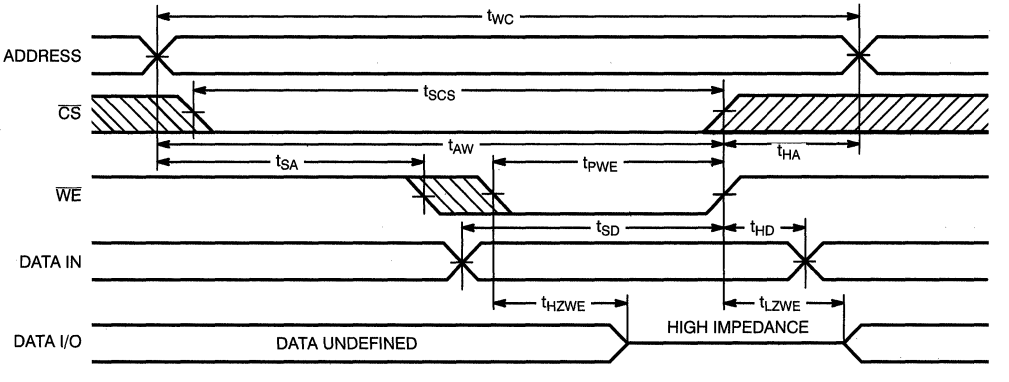
Switching Waveforms (continued)

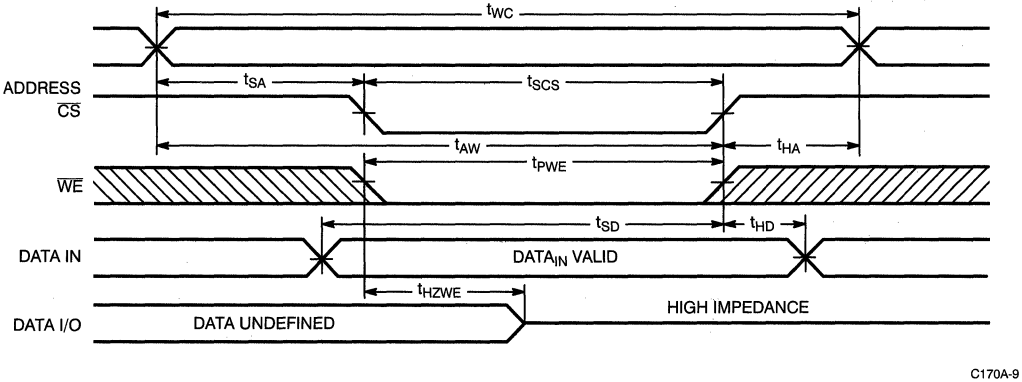
Read Cycle No. 2[9, 11]



Write Cycle No. 1[8, 12]



Write Cycle No. 2[8, 12, 13]



Notes:
11. Data I/O will be high-impedance if $\overline{OE}$ = V_{IH}.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C170A–15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–15VC	V13	24-Lead Molded SOJ	
20	CY7C170A–20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–20VC	V13	24-Lead Molded SOJ	
25	CY7C170A–25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–25VC	V13	24-Lead Molded SOJ	
	CY7C170A–25DMB	D10	22-Lead (300-Mil) CerDIP	Military
35	CY7C170A–35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C170A–35VC	V13	24-Lead Molded SOJ	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

CY7C171A
CY7C172A

4K x 4 Static RAM with Separate I/O

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  — t_{AA} = 15 ns
- **Transparent write (CY7C171A)**
- **Low active power**
  — 375 mW
- **Low standby power**
  — 93 mW
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C171A and CY7C172A are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

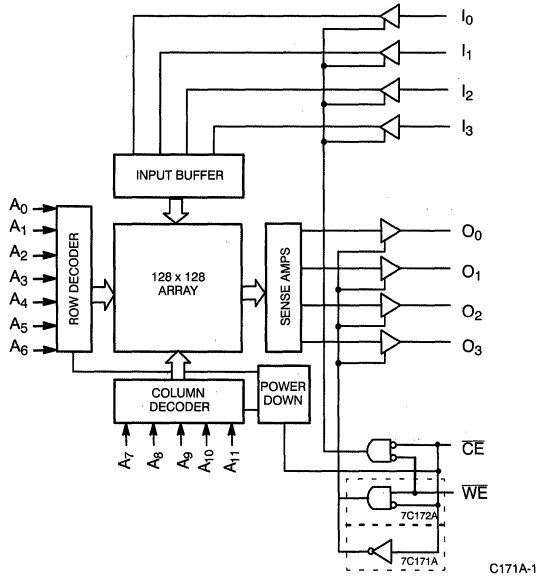
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

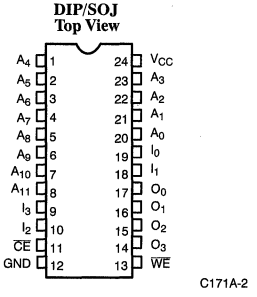
The output pins remain in a high-impedance state when write enable ($\overline{WE}$) is LOW (7C172A only), or chip enable is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C171A–15 7C172A–15	7C171A–20 7C172A–20	7C171A–25 7C172A–25	7C171A–35 7C172A–35	7C171A–45 7C172A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	80	70	70	
	Military		90	80	70	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C171A−15 7C172A−15 Min.	7C171A−15 7C172A−15 Max.	7C171A−20 7C172A−20 Min.	7C171A−20 7C172A−20 Max.	7C171A−25 7C172A−25 Min.	7C171A−25 7C172A−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		80		70	mA
			Mil				90		80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		40		40		20	mA
			Mil				40		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20		20	mA
			Mil				20		20	

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2] (continued)

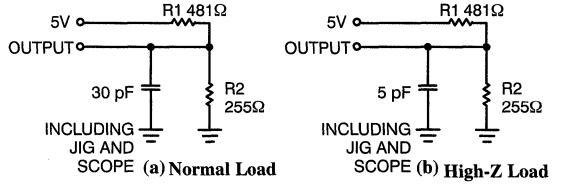
Parameter	Description	Test Conditions		7C171A–35 7C172A–35 Min.	7C171A–35 7C172A–35 Max.	7C171A–45 7C172A–45 Min.	7C171A–45 7C172A–45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		70			mA
			Mil		70		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		20			mA
			Mil		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20			mA
			Mil		20		20	

Capacitance[4]

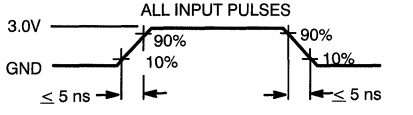
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms

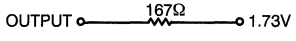


C171A-3



C171A-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,5]

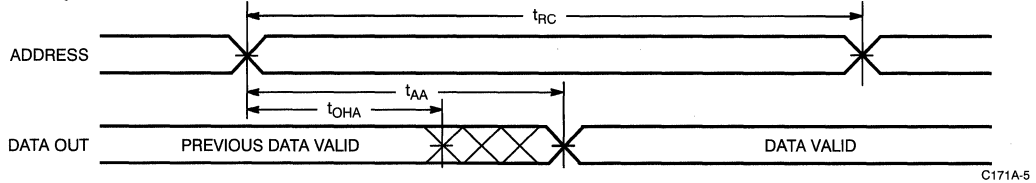
Parameter	Description	7C171A–15 7C172A–15		7C171A–20 7C172A–20		7C171A–25 7C172A–25		7C171A–35 7C172A–35		7C171A–45 7C172A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to LOW Z[6]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to HIGH Z[6, 7]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		20		20		25	ns
t_{RCS}	Read Command Set-Up	0		0		0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		0		0		ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6] (7C172A)	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7] (7C172A)		7		7		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C171A)		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C171A)		15		20		25		30		35	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C172A).

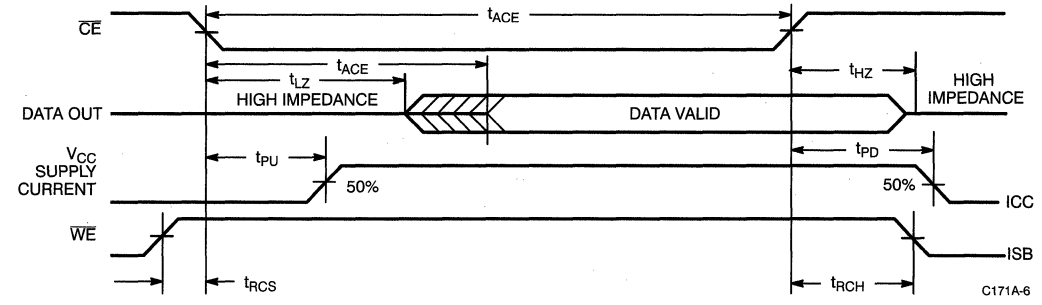
Switching Waveforms

Read Cycle No. 1[9, 10]

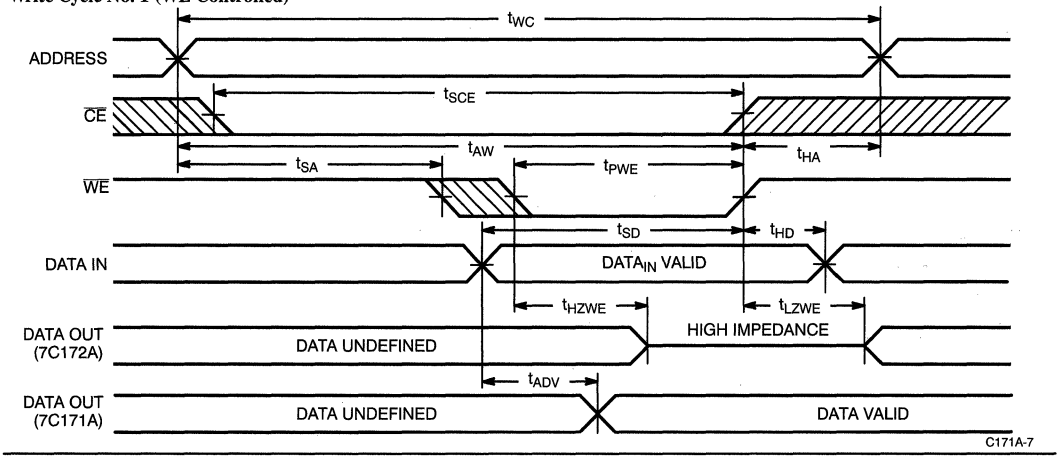


Switching Waveforms (continued)

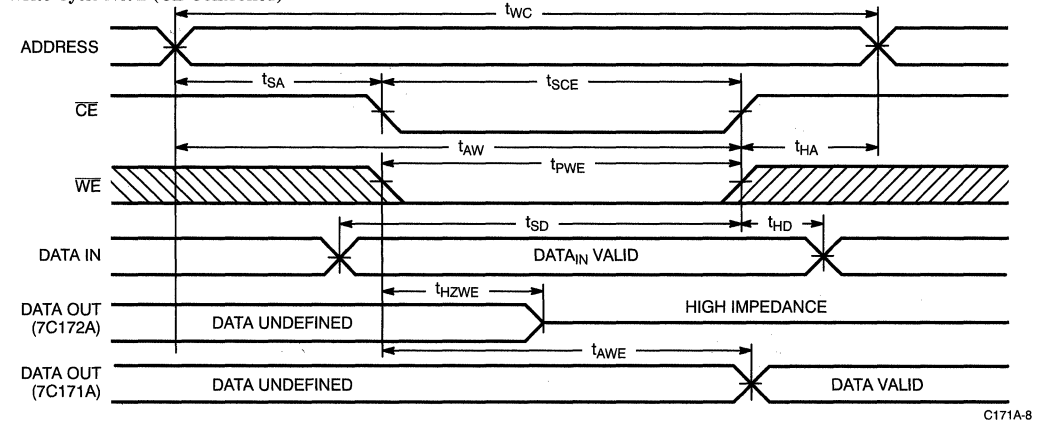
Read Cycle No. 2[9, 11]



Write Cycle No. 1 (WE Controlled)[8]

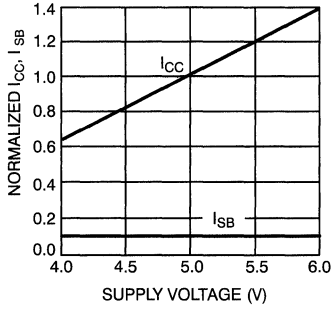


Write Cycle No. 2 (CE Controlled)[8, 12]

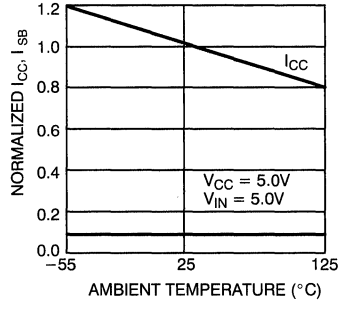


Typical DC and AC Characteristics

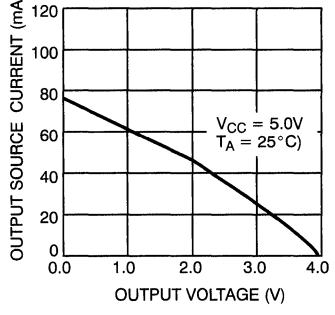
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



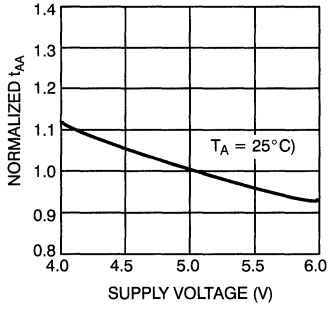
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



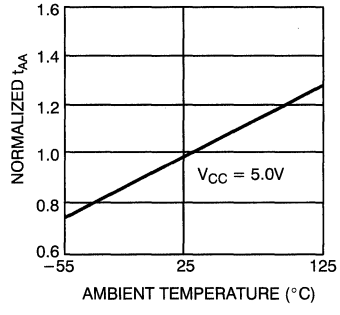
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



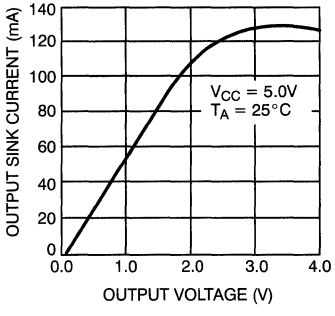
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



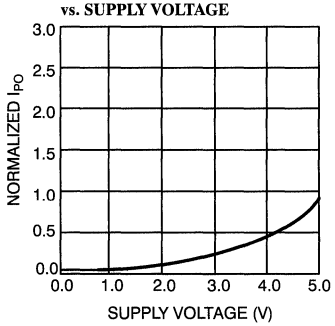
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



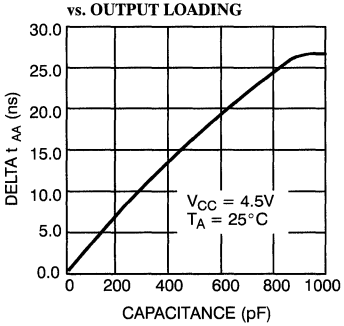
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



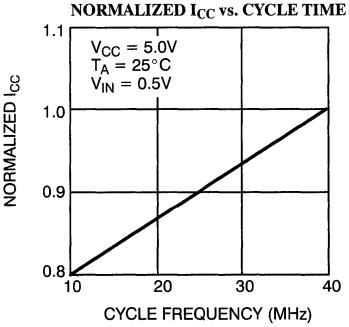
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C171A–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
20	CY7C171A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
25	CY7C171A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
35	CY7C171A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commerical

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C172A–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–15VC	V13	24-Lead Molded SOJ	
20	CY7C172A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–20VC	V13	24-Lead Molded SOJ	
	CY7C172A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C172A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–25VC	V13	24-Lead Molded SOJ	
	CY7C172A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C172A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
45	CY7C172A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{ADV}[13]	7, 8, 9, 10, 11

Note:
13. 7C171A only.

Document #: 38−00104−D

PRELIMINARY

CY7C178
CY7C179

32K x 18 Synchronous Cache RAM

Features

- **Supports 66-MHz Pentium™ microprocessor cache systems with zero wait states**
- **32K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 8.5 ns**
- **Two-bit wraparound counter supporting Pentium and 486 burst sequence (CY7C178)**
- **Two-bit wraparound counter supporting linear burst sequence (CY7C179)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **I/Os capable of 3.3V operation**
- **Industry-standard pinout**
- **52-pin PLCC and PQFP**

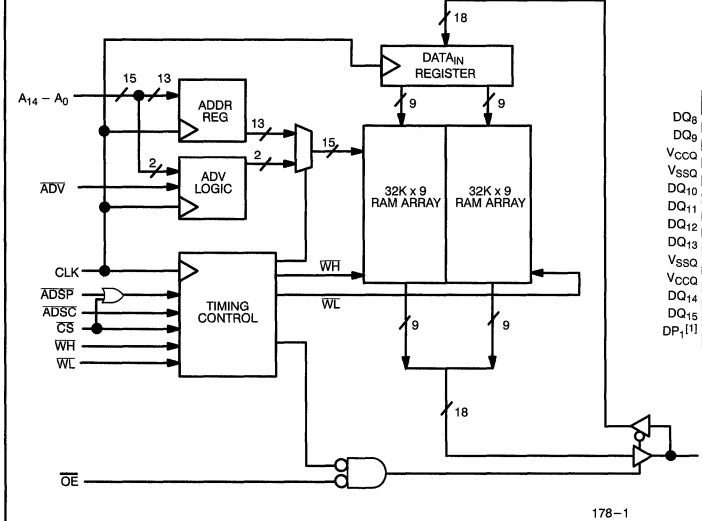
Functional Description

The CY7C178 and CY7C179 are 32K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C178 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C179 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



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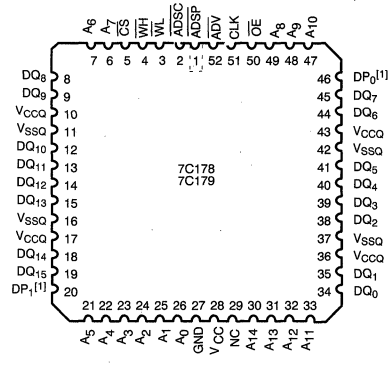
Pin Configuration

PLCC
Top View



178–2

Selector Guide

		7C178–8 7C179–8	7C178–10 7C179–10	7C178–12 7C179–12
Maximum Access Time (ns)		8.5	10.5	12.5
Maximum Operating Current (mA)	Commercial	225	210	180
	Military			270

Shaded area contains advanced information.

Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_X.

Pentium is a trademark of Intel Corporation.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C178 and CY7C179 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C178 and CY7C179 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. Since the CY7C178 and the CY7C179 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data and parity lines. As a safety precaution, the appropriate data and parity lines are three-stated in the cycle where $\overline{WH}$ and $\overline{WL}$ are sampled LOW regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

Burst Sequences

The CY7C178 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the 486 and Pentium processor's address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C179 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 256-Kbyte secondary cache for the Pentium microprocessor using four CY7C178 cache RAMs.

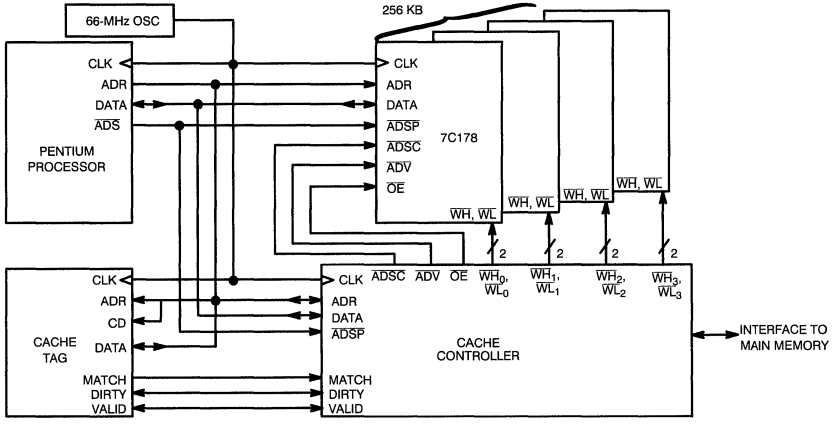


Figure 1. Cache Using Four CY7C178s

Pin Definitions

Signal Name	Type	# of Pins	Description
V_{CC}	Input	1	+5V Power
V_{CCQ}	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
V_{SSQ}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{14} - A_0$	Input	15	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Input Signals

CLK — I — Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CS}$, $\overline{WH}$, $\overline{WL}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).

A_{14}–A_0 — I — Fifteen address lines used to select one of 32K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.

$\overline{ADSP}$ — I — Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, $A_0 - A_{14}$ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.

$\overline{ADSC}$ — I — Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, $A_0 - A_{14}$ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.

$\overline{WH}$ — I — Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.

$\overline{WL}$ — I — Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect of $\overline{WL}$ if $\overline{CS}$ is HIGH.

$\overline{ADV}$ — I — Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C179, the address will be incremented linearly. In the CY7C178, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$.. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.

$\overline{CS}$ — I — Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ_{15}–DQ_0	I/O	Sixteen bidirectional data I/O lines. DQ_{15} – DQ_8 are inputs to and outputs from the high-order half of the RAM array, while DQ_7 – DQ_0 are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. DQ_{15} – DQ_8 and DQ_7 – DQ_0 are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, is sampled LOW at clock rise.
DP_1–DP_0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as DQ_{15} – DQ_0, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}	V_{CCQ}
Com'l	0°C to +70°C	5V ± 5%	3.0V to V_{CC}
Mil	−55°C to +125°C	5V ± 5%	5V ± 5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	7C178–8 7C179–8		7C178–10 7C179–10		7C178–12 7C179–12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH}=−4.0 mA	2.4	V_{CCQ}	2.4	V_{CCQ}	2.4	V_{CCQ}	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL}=8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}	−1	1	−1	1	−1	1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	5	−5	5	−5	5	μA

Notes:

2. Minimum voltage equals −2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page for Group A subgroup testing information.

Electrical Characteristics Over the Operating Range (continued)[4]

Parameter	Description	Test Conditions		7C178–8 7C179–8 Min.	7C178–8 7C179–8 Max.	7C178–10 7C179–10 Min.	7C178–10 7C179–10 Max.	7C178–12 7C179–12 Min.	7C178–12 7C179–12 Max.	Unit
I_{OS}	Output Short Circuit Current[5]	V_{CC}=Max., V_{OUT}=GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX} =1/t_{RC}	Com'l		225		210		190	mA
			Mil						270	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		50		40		30	mA
			Mil						50	
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V, f=0[6]	Com'l		20		20		20	mA
			Mil						20	

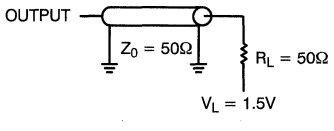
Shaded areas contain advanced information

Capacitance[7]

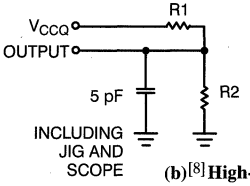
Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	Com'l	4.5	pF
			Mil	6	
C_{IN}: Other Inputs			Com'l	5	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	8	pF
			Mil	10	

Shaded areas contain advanced information

AC Test Loads and Waveforms

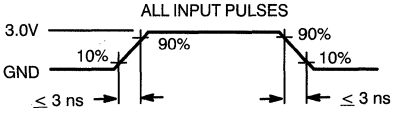


(a) Normal Load



(b)[8] High-Z Load

178–3



178–4

Notes:
5. Not more than one output should be shortened at one time. Duration of the short circuit should not exceed 30 seconds.
6. Inputs are disabled, clock signal allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Resistor values for V_{CCQ}=5V are: R1=481Ω and R2=255Ω. Resistor values for V_{CCQ}=3.3V are R1=1179Ω and R2=868Ω.

Switching Characteristics Over the Operating Range[9]

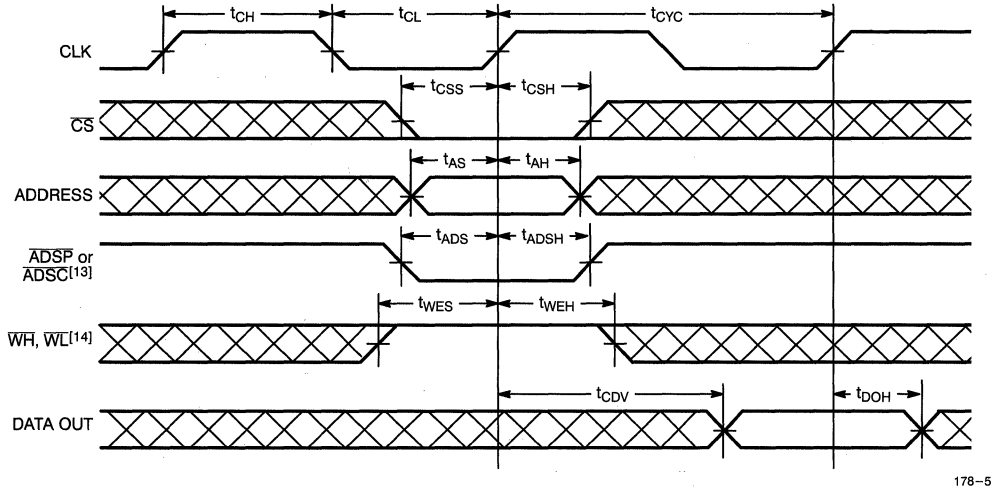
Parameter	Description	7C178–8 7C179–8		7C178–10 7C179–10		7C178–12 7C179–12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	12.5		15		20		ns
t_{CH}	Clock HIGH	5		6		8		ns
t_{CL}	Clock LOW	5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		8.5		10		12	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		2.5		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[10]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[10]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		6	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[10, 11]		5		6		7	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[11]		8.5		10		12	ns

Notes:

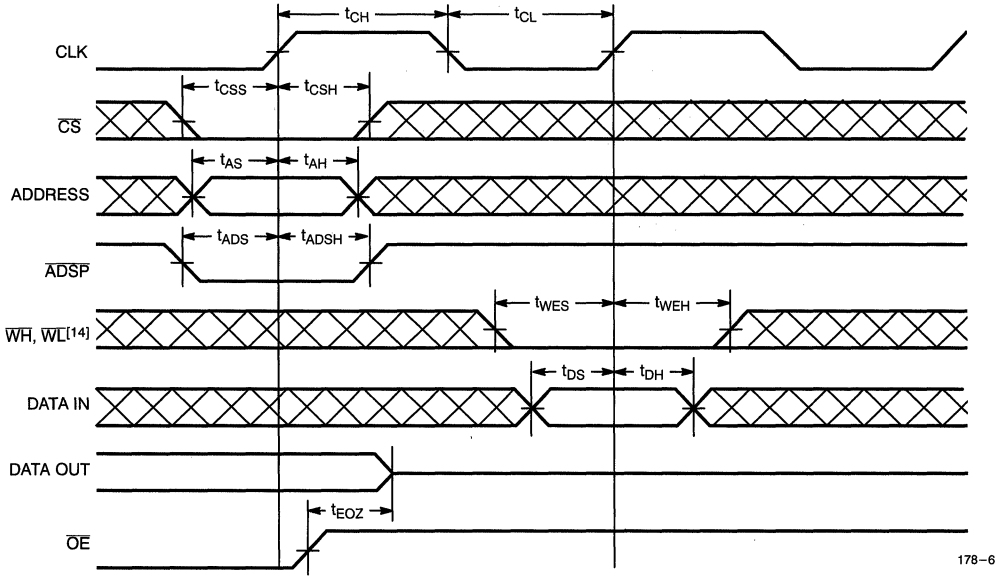
9. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in Figure (a) and (b) of AC Test Loads.
10. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
11. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[12]



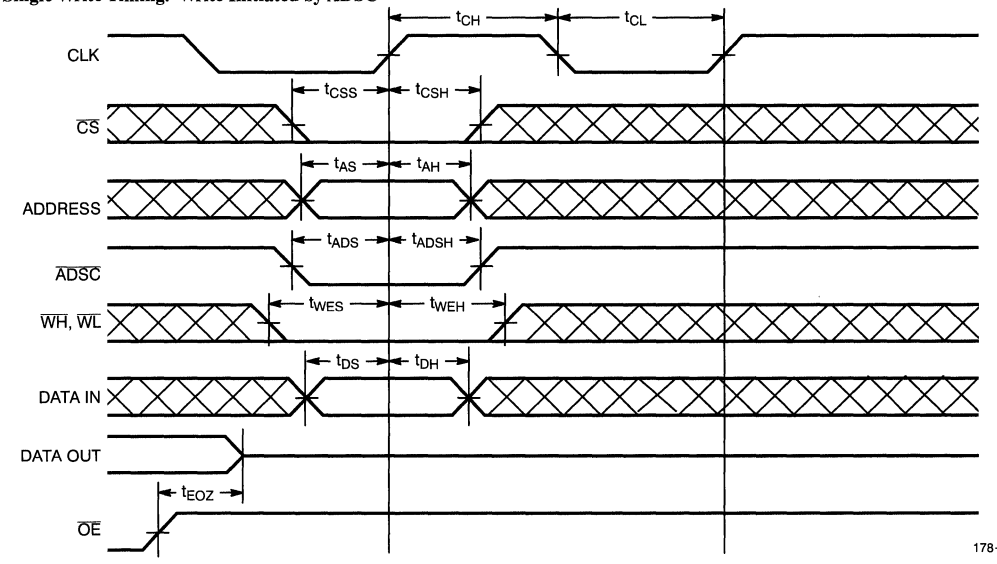
Single Write Timing: Write Initiated by $\overline{ADSP}$



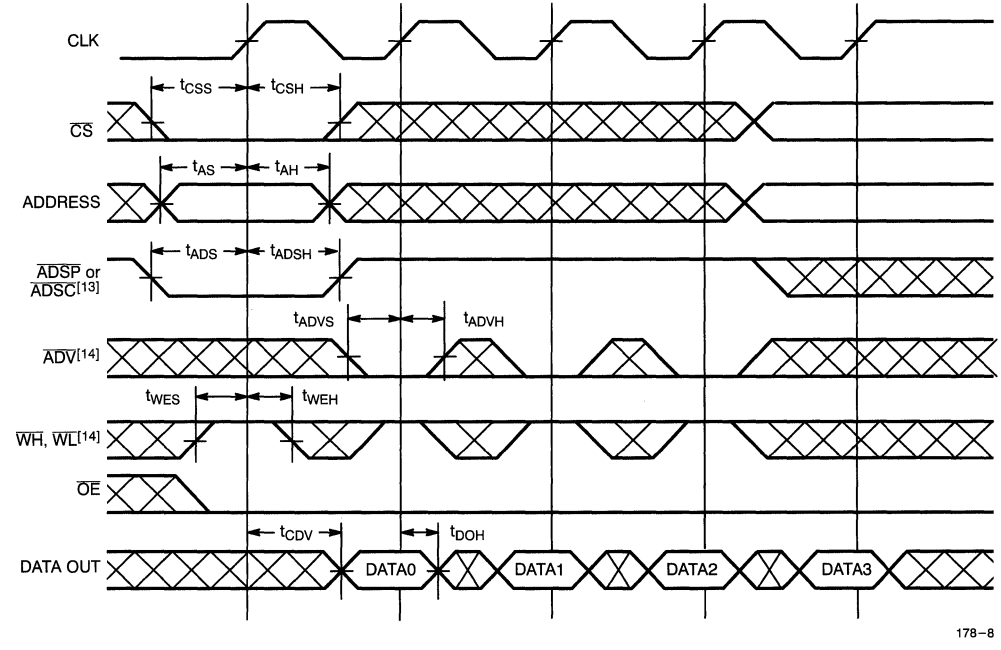
Notes:
12. $\overline{OE}$ is LOW throughout this operation.
13. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
14. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WH}$, and $\overline{WL}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$

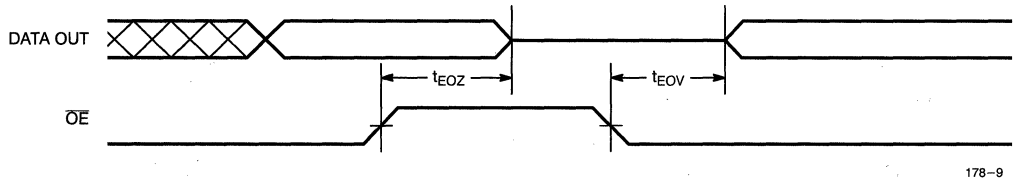


Burst Read Sequence with Four Accesses

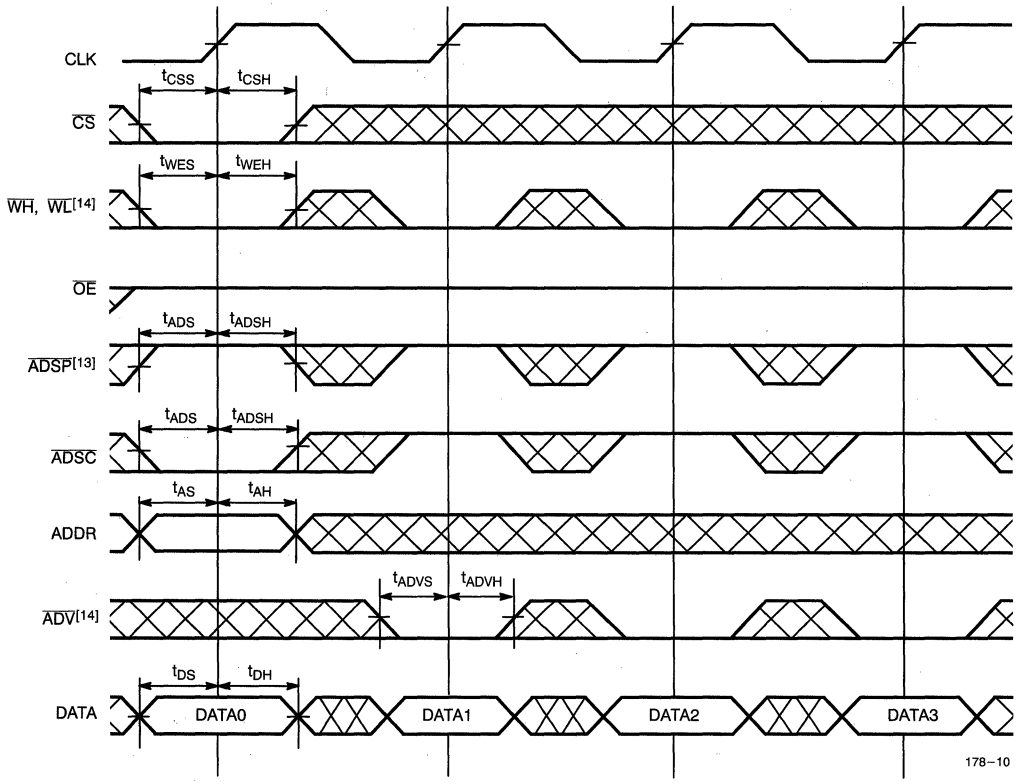


Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)

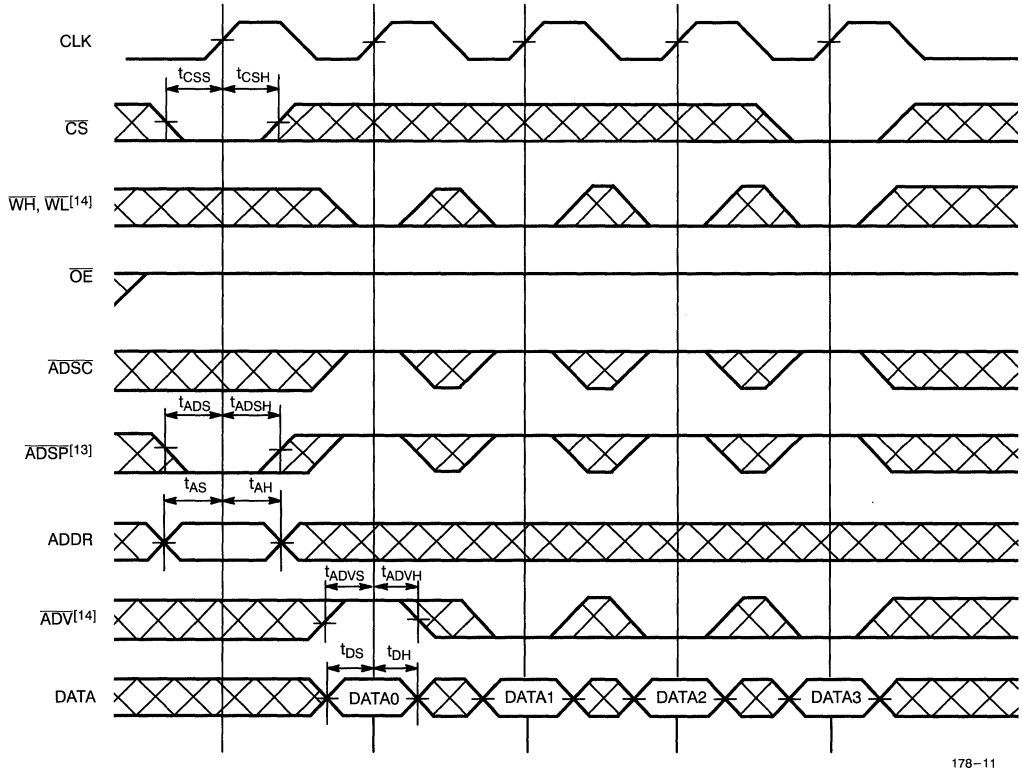


Write Burst Timing: Write Initiated by $\overline{ADSC}$



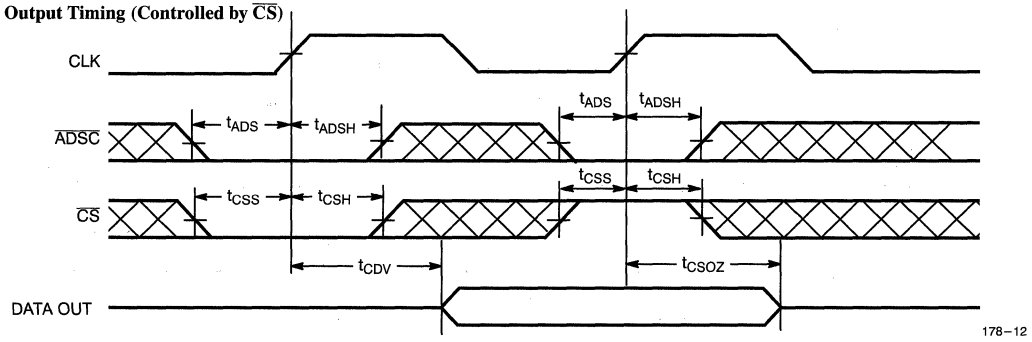
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

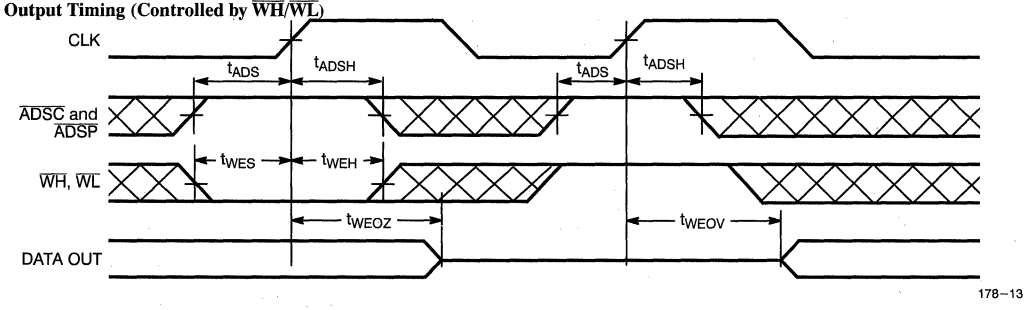


Switching Waveforms (continued)

Output Timing (Controlled by $\overline{CS}$)



Output Timing (Controlled by $\overline{WH}/\overline{WL}$)



Truth Table

Input						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	L	H	H	H	L→H	Same address as previous cycle	$\overline{ADSP}$ ignored, read cycle
H	L	H	L	H	L→H	Incremented burst address	$\overline{ADSP}$ ignored, read cycle in burst sequence
H	L	H	H	L	L→H	Same address as previous cycle	$\overline{ADSP}$ ignored, write cycle
H	L	H	L	L	L→H	Incremented burst address	$\overline{ADSP}$ ignored, write cycle in burst sequence
H	X	L	X	X	L→H	N/A	Chip deselected
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C178–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178–8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C178–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178–10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C178–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178–10NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C178–12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C179–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179–8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C179–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179–10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C179–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179–12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C179–12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

Document #: 38–00243

CY7C182

8K x 9 Static RAM

Features

- **High speed**
  - **— t_{AA} = 25 ns**
- **9-bit organization is ideal for cache memory applications**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 770 mW**
- **Low standby power**
  - **— 195 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, $\overline{OE}$ options**

Functional Description

The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 770 mW.

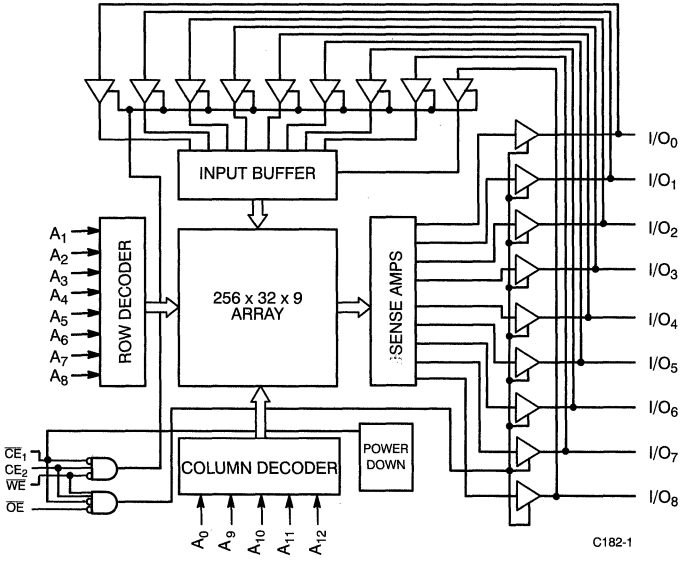
The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by more than 70% when the circuit is deselected. Easy memory expansion is provided by an active-LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active-LOW output enable ($\overline{OE}$), and three-state drivers.

An active-LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_8) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, ($\overline{CE}_1$ and $\overline{OE}$ active LOW and CE_2 active HIGH), while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

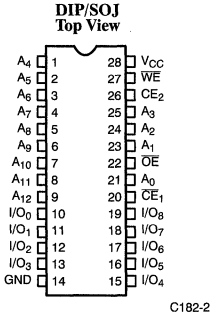
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C182–20	7C182–25	7C182–35	7C182–45
Maximum Access Time (ns)		20	25	35	45
Maximum Operating Current (mA)	Com'l	150	140	140	140
Maximum Standby Current (mA)		35	35	35	35

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential[1] ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C182−20		7C182−25, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} Min., I_{OH} = −4.0 mA.	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}, GND < V_{OUT} < V_{CC}, Output Disabled	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Circuit Current	V_{CC} Max., Output Current = 0 mA, f = Max., V_{IN} = V_{CC} or GND		150		140	mA
I_{SB1}	Automatic Power-Down Current — TTL Inputs	Max V_{CC}, $\overline{CE_1}$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		35		35	mA
I_{SB2}	Automatic Power-Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE_1}$ ≥ V_{CC} − 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0		20		20	mA

Shaded area contains preliminary information.

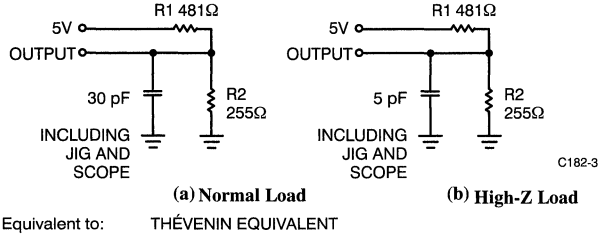
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{IN}	Input Capacitance		10	pF

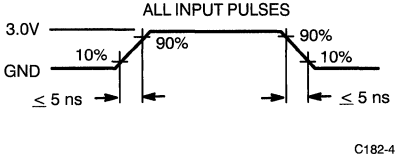
Notes:

1. V_{IL} (min.) = −3.0V for pulse durations of less than 20 ns.
2. Duration of the short circuit should not exceed 30 seconds. Not more than one output should be shorted at one time.
3. Tested initially and after any design or process changes that may affect these parameters.

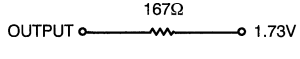
AC Test Loads and Waveforms



(a) Normal Load (b) High-Z Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	7C182–20		7C182–25		7C182–35		7C182–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[4]										
t_{RC}	Read Cycle Time	20		25		35		45		ns
t_{AA}	Address to Data Valid		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ Access Time		20		25		35		45	ns
t_{ACE2}	CE_2 Access Time		20		25		35		45	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z	5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	5		5		5		5		ns
t_{HZCE1}	$\overline{CE}_1$ HIGH to High Z[5]		15		18		20		25	ns
t_{HZCE2}	CE_2 LOW to High Z[5]		15		18		20		25	
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25	ns
t_{DOE}	$\overline{OE}$ Access Time		15		18		20		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		15		18		20		25	ns
WRITE CYCLE[6]										
t_{WC}	Write Cycle Time	20		25		35		45		ns
t_{SA}	Address Set-Up Time	0		0		0		0		ns
t_{AW}	Address Valid to End of Write	15		20		30		40		ns
t_{SD}	Data Set-Up Time	10		15		20		25		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	15		20		30		40		ns
t_{SCE2}	CE_2 HIGH to Write End	15		20		30		40		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		30		ns
t_{HA}	Address Hold from End of Write	0		0		0		0		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{LZWE}	Write HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	Write LOW to High Z[5, 7, 8]		13		13		15		20	ns

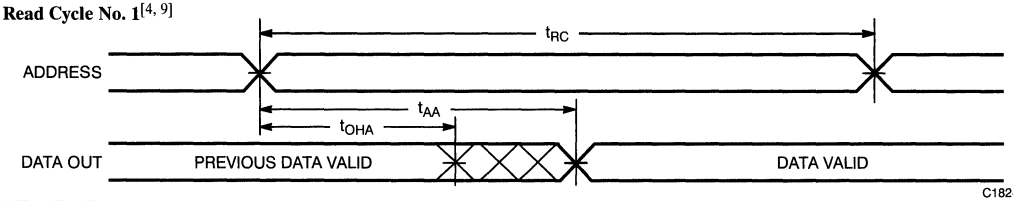
Shaded area contains preliminary information.

Notes:

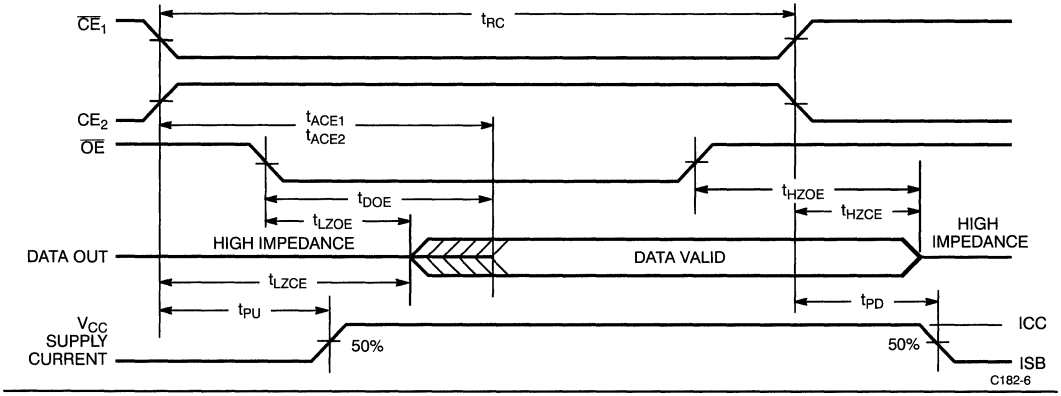
4. $\overline{WE}$ is HIGH for read cycle.
5. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF. Transition is measured ± 500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. At any given temperature and voltage condition, t_{LZWE} is less than t_{HZWE} for any given device. These parameters are sampled and not 100% tested.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms

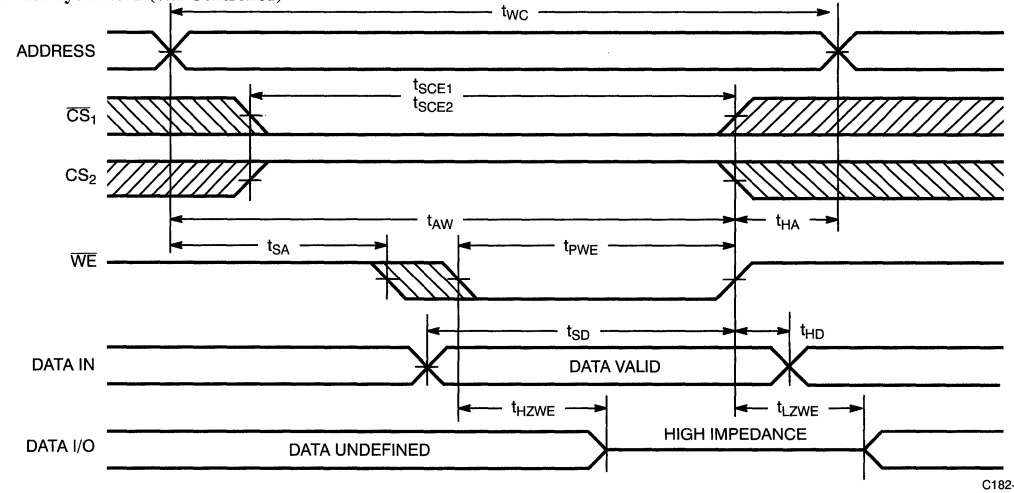
Read Cycle No. 1[4, 9]



Read Cycle No. 2[4, 10]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]

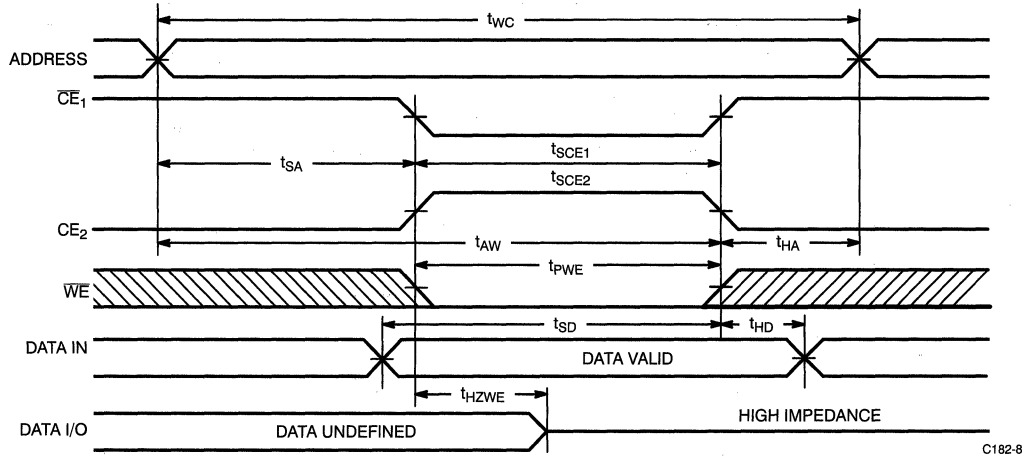


Notes:

9. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}. CE_2 = V_{IH}.
10. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[6, 10]



Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Data In	Data Out	Mode
H	X	X	X	Z	Z	Deselect/Power-Down
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output Disable
X	L	X	X	Z	Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C182–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–20VC	V21	28-Lead Molded SOJ	
25	CY7C182–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–25VC	V21	28-Lead Molded SOJ	
35	CY7C182–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–35VC	V21	28-Lead Molded SOJ	
45	CY7C182–45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C182–45VC	V21	28-Lead Molded SOJ	

Shaded area contains preliminary information.

Document #: 38–00110–E

CY7C185

8K x 8 Static RAM

Features

- **High speed**
  — 15 ns
- **Fast t_{DOE}**
- **Low active power**
  — 715 mW
- **Low standby power**
  — 220 mW
- **CMOS for optimum speed/power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

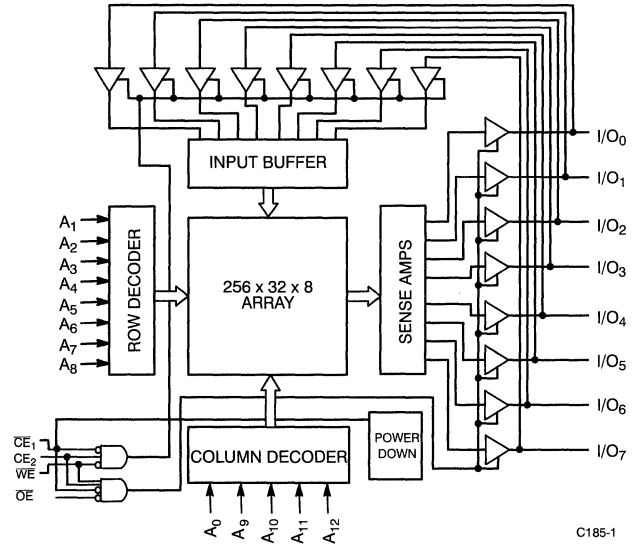
Functional Description

The CY7C185 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP and SOJ package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

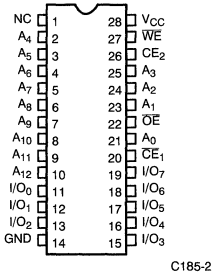
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configurations

DIP/SOJ
Top View



Selection Guide[1]

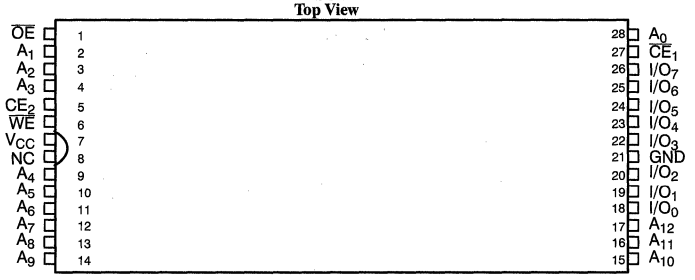
	7C185–12	7C185–15	7C185–20	7C185–25	7C185–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	140	130	110	100	100
Maximum Standby Current (mA)	40/15	40/15	20/15	20/15	20/15

Shaded areas contain preliminary information.

Note:
1. For military specifications, see the CY7C185A/CY7C186A datasheet.

Pin Configurations (continued)

TSOP
Top View



C185-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C185−12		7C185−15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		140		130	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		15		15	mA

Shaded areas contain preliminary information.

Notes:

2. Minimum voltage is equal to −3.0V for pulse durations less than 30 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

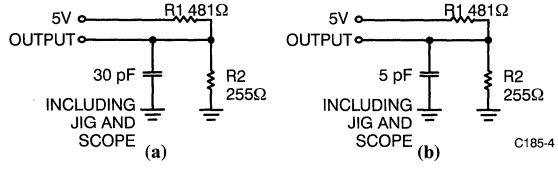
Electrical Characteristics Over the Operating Range (continued)

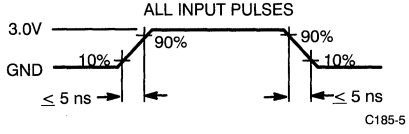
Parameter	Description	Test Conditions	7C185–20		7C185–25, 35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		110		100	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		20		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		15		15	mA

Capacitance[4]

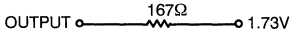
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C185–12		7C185–15		7C185–20		7C185–25		7C185–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		5		5		5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		12		15		20		25		35	ns
t_{ACE2}	CE_2 HIGH to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		9		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		6		7		8		10		10	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[7]	3		3		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[6, 7] CE_2 LOW to High Z		6		7		8		10		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		12		15		20		20		20	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		12		15		20		20		ns
t_{SCE2}	CE_2 HIGH to Write End	8		12		15		20		20		ns
t_{AW}	Address Set-Up to Write End	9		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		12		15		15		20		ns
t_{SD}	Data Set-Up to Write End	6		8		10		10		12		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		6		7		7		7		8	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		5		5		ns

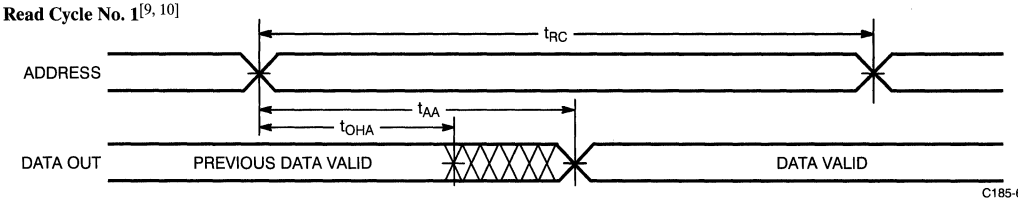
Shaded areas contain preliminary information.

Notes:

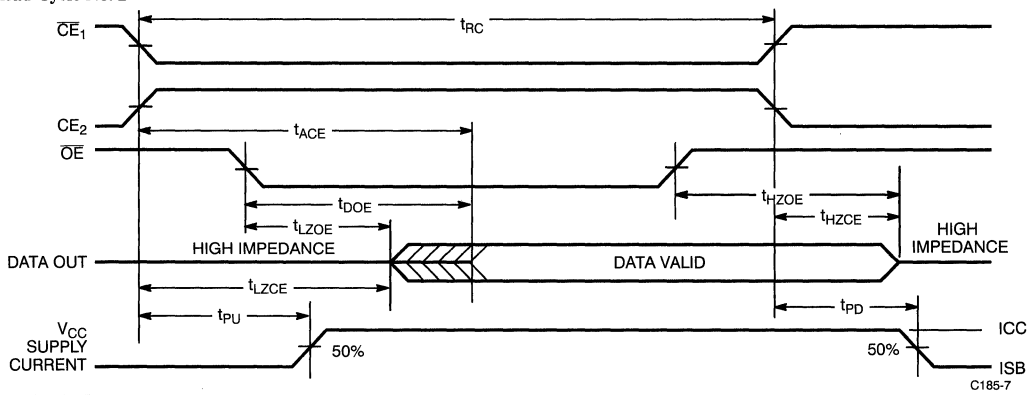
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

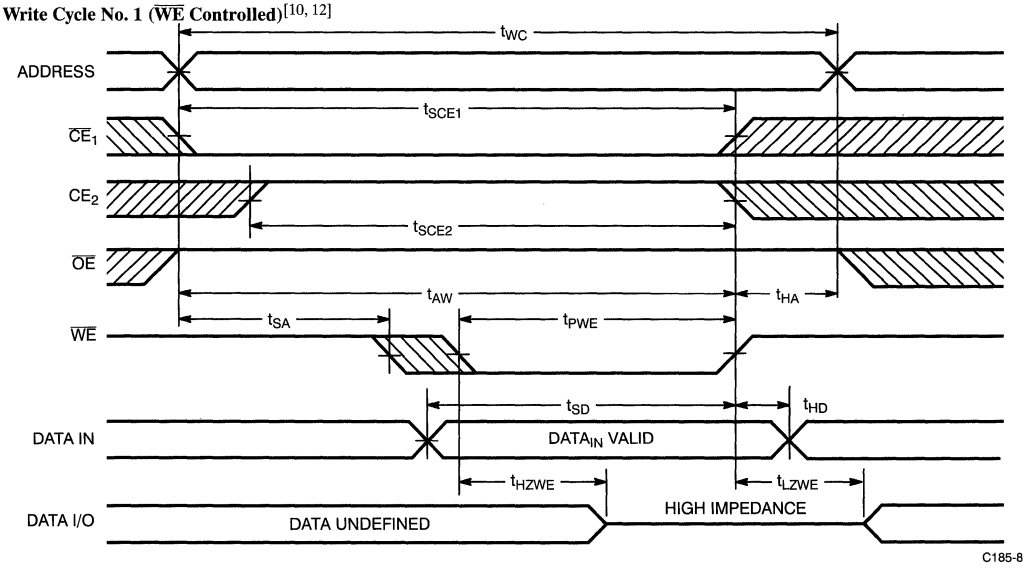
Read Cycle No. 1[9, 10]



Read Cycle No. 2[11, 12]



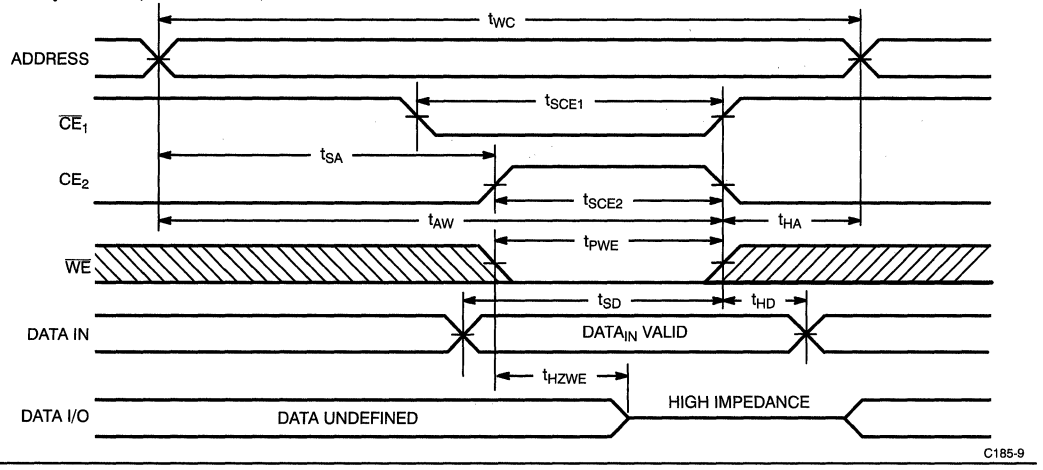
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10, 12]



Notes:
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. $\overline{WE}$ is HIGH for read cycle.
12. Data I/O is High Z if $\overline{OE}$ = V_{IH}, $\overline{CE}_1$ = V_{IH}, or $\overline{WE}$ = V_{IL}.

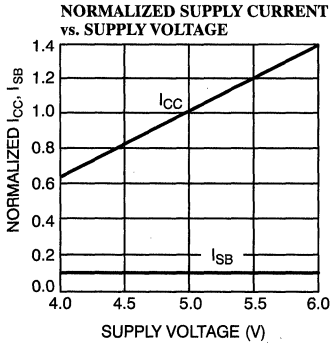
Switching Waveforms (continued)

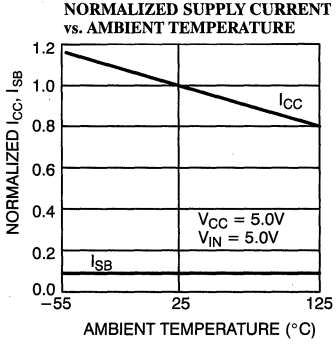
Write Cycle No. 2 ($\overline{CE}$ Controlled) [10, 12, 13]

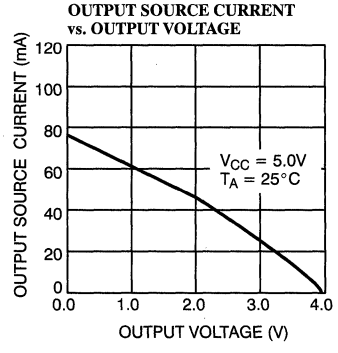


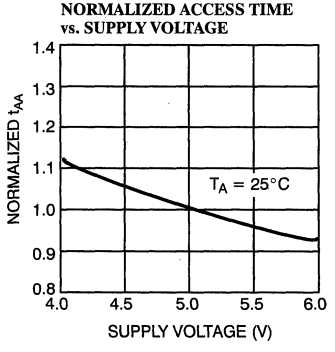
Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

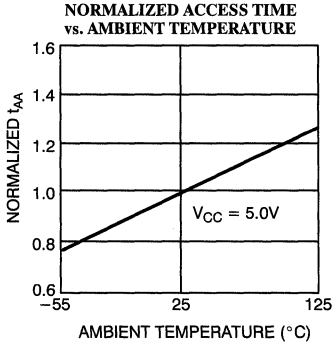
Typical DC and AC Characteristics

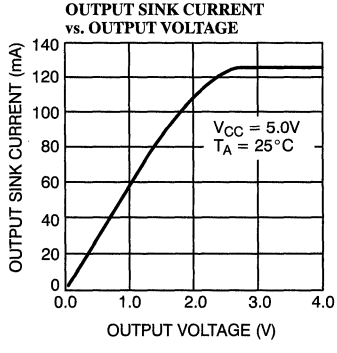






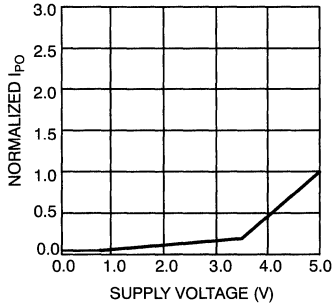




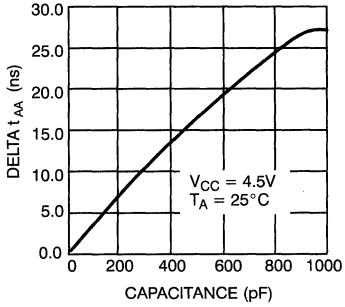


Typical DC and AC Characteristics (continued)

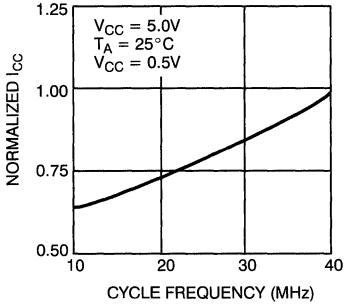
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C185–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–12VC	V21	28-Lead Molded SOJ	
15	CY7C185–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–15VC	V21	28-Lead Molded SOJ	
	CY7C185–15ZC	Z28	28-Lead Thin Small Outline Package	
20	CY7C185–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–20VC	V21	28-Lead Molded SOJ	
	CY7C185–20ZC	Z28	28-Lead Thin Small Outline Package	
25	CY7C185–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–25VC	V21	28-Lead Molded SOJ	
	CY7C185–25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C185–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185–35VC	V21	28-Lead Molded SOJ	
	CY7C185–35ZC	Z28	28-Lead Thin Small Outline Package	

Shaded areas contain preliminary information.

Document #: 38–00037–J

CY7C185A

8K x 8 Static RAM

Features

- **High speed**
  - **20 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **743 mW**
- **Low standby Power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**

Functional Description

The CY7C185A is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by over 70% when deselected. The CY7C185A is in the standard 300-mil-wide DIP package and leadless chip carrier.

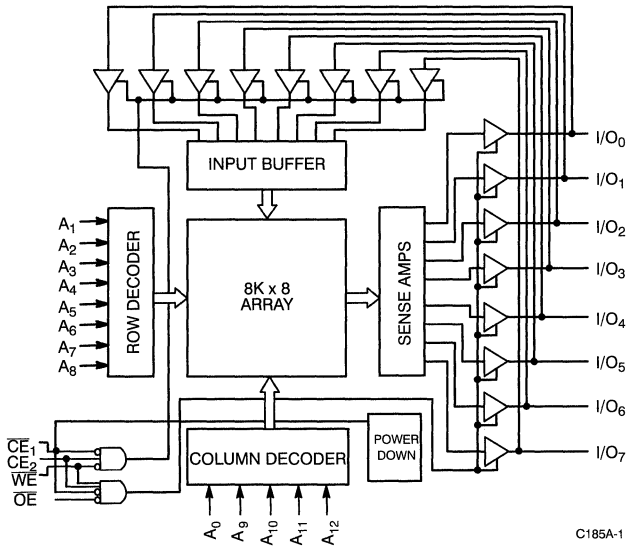
Writing to the device is accomplished when the chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs are both LOW, and the chip enable two (CE_2) input is HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

Reading the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW, while taking write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in a high-impedance state when chip enable one ($\overline{CE}_1$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip enable two (CE_2) is LOW.

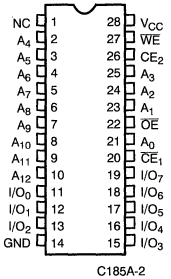
A die coat is used to ensure alpha immunity.

Logic Block Diagram



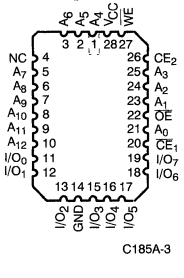
Pin Configurations

DIP
Top View



C185A-2

LCC
Top View



C185A-3

Selection Guide[1]

		7C185A–15	7C185A–20	7C185A–25	7C185A–35	7C185A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Military	170	135	125	125	125
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see the CY7C185 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C185A−15		7C185A−20		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Military		170		135	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≥ 0.3V	Military		20		20	mA

Shaded area contains advanced information.

Notes:

2. V_{IL} (min.) = − 3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[4] (continued)

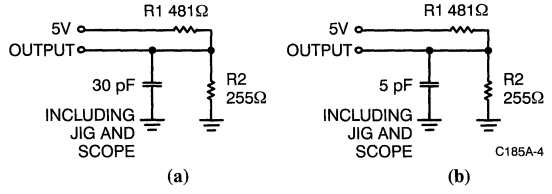
Parameter	Description	Test Conditions		7C185A–25 Min.	7C185A–25 Max.	7C185A–35, 45 Min.	7C185A–35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		125		125	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC} $\overline{CE}_1$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≥ 0.3V	Military		20		20	mA

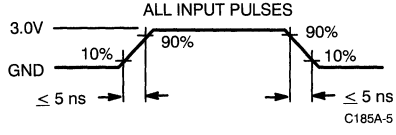
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

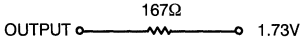
Note:
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7C185A–15		7C185A–20		7C185A–25		7C185A–35		7C185A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		15		20		25		35		45	ns
t_{ACE2}	CE_2 HIGH to Data Valid		15		20		25		35		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8]		8		8		10		12		15	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[9]	3		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[8, 9] CE_2 LOW to High Z		8		8		10		15		15	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	10		15		20		25		30		ns
t_{SCE2}	CE_2 HIGH to Write End	10		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8]		7		7		7		10		15	ns

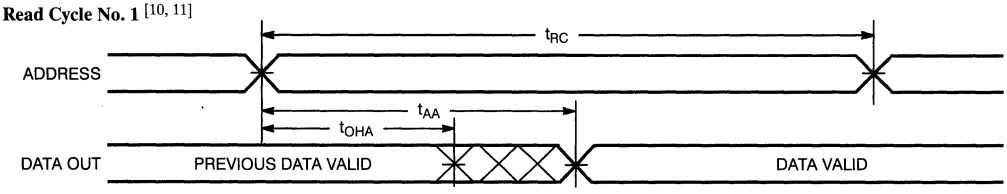
Shaded area contains advanced information.

Notes:

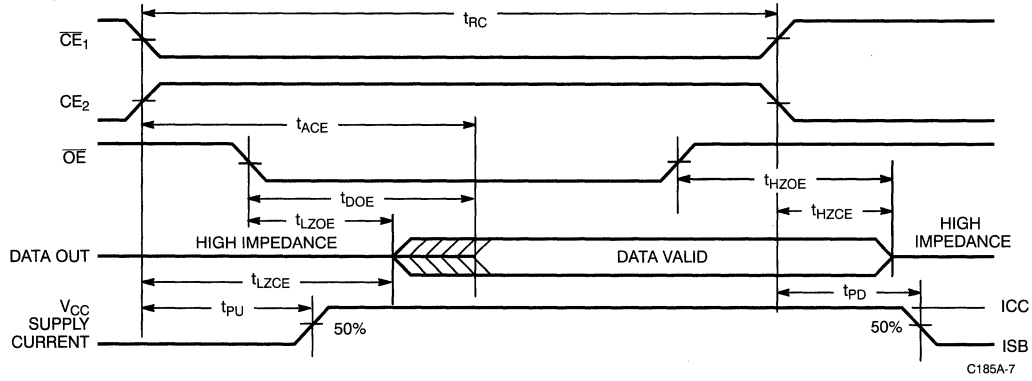
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.

Switching Waveforms

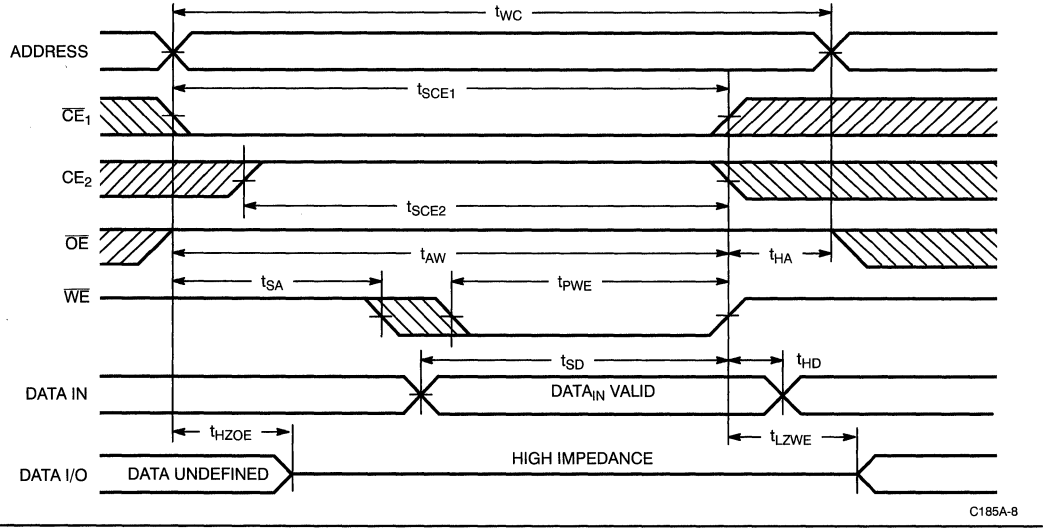
Read Cycle No. 1 [10, 11]



Read Cycle No. 2 [11, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [13, 14]

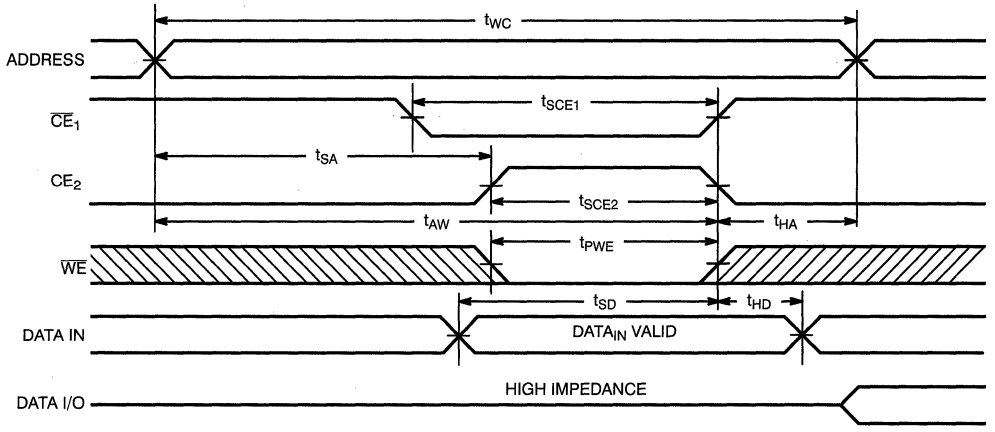


Notes:

11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. $\overline{WE}$ is HIGH for read cycle.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms (continued)

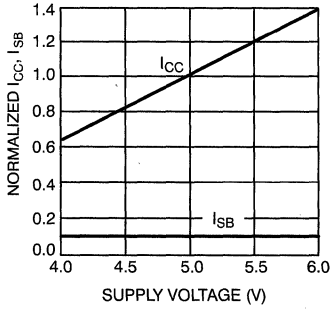
Write Cycle No. 2 ($\overline{CE}$ Controlled) [13, 14, 15]



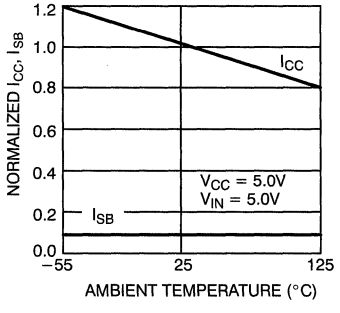
Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

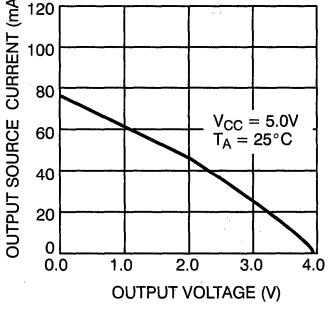
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



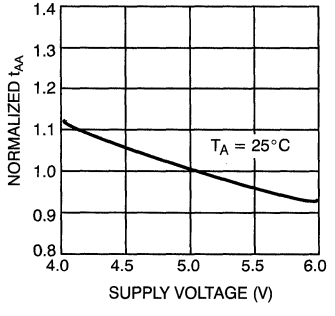
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



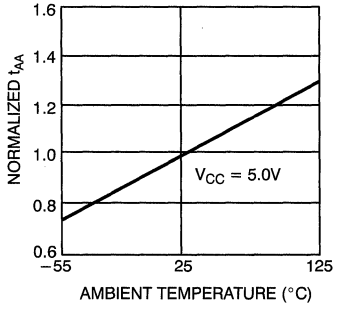
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



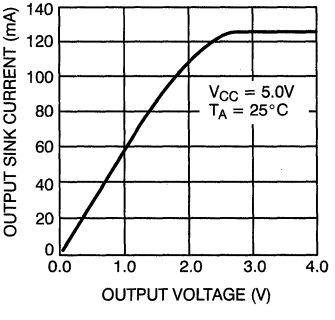
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

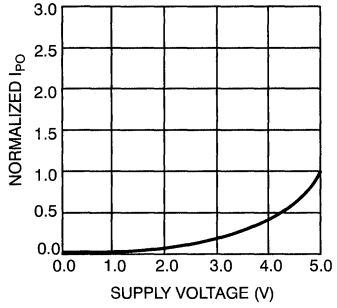


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

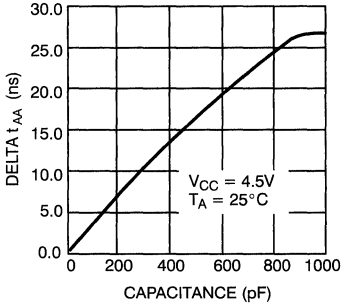


Typical DC and AC Characteristics (continued)

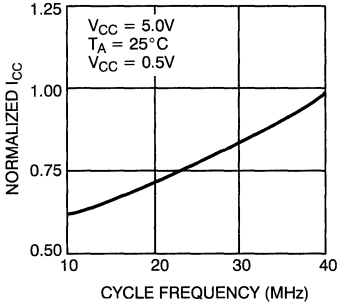
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C185A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C185A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C185A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C185A–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE1}	7, 8, 9, 10, 11
t_{ACE2}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE1}	7, 8, 9, 10, 11
t_{SCE2}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00114–B

CY7C187

64K x 1 Static RAM

Features

- **High speed**
  — 15 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 495 mW
- **Low standby power**
  — 220 mW
- **TTL compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C187 is a high-performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 56% when deselected.

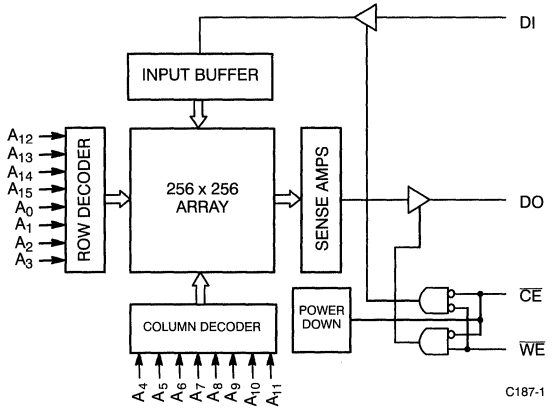
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

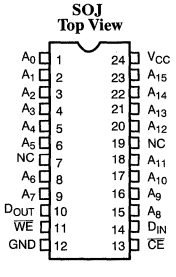
The CY7C187 utilizes a die coat to ensure alpha immunity.

Logic Block Diagram

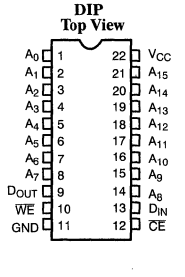


C187-1

Pin Configurations



C187-2



C187-3

Selection Guide[1]

	7C187–12	7C187–15	7C187–20	7C187–25	7C187–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	90	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded area indicates preliminary information.

Note:
1. For military specifications, see the CY7C187A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C187−12		7C187−15		7C187−20		7C187−25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−350		−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		160		90		80		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		40		40		40		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20		20		20	mA

Shaded area indicates preliminary information.

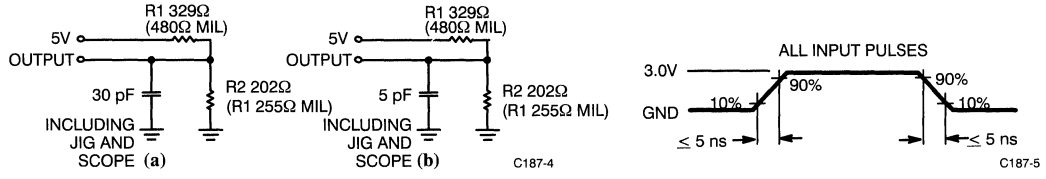
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

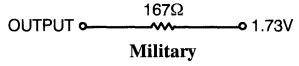
Notes:

2. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

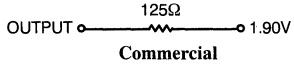
AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C187–12		7C187–15		7C187–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Output Hold from Address Change	3		3		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		7		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		12		15		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		12		15		ns
t_{AW}	Address Set-Up to Write End	9		12		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		12		15		ns
t_{SD}	Data Set-Up to Write End	6		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		6		7		7	ns

Shaded area indicates preliminary information.

Notes:

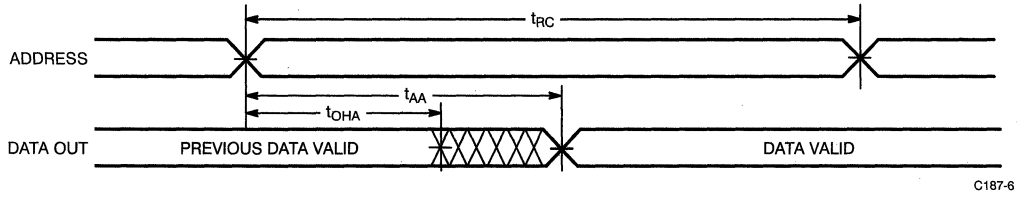
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.

Switching Characteristics Over the Operating Range[6] (continued)

Parameters	Description	7C187–25		7C187–35		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Output Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20	ns
WRITE CYCLE[9]						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		ns
t_{AW}	Address Set-Up to Write End	20		25		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	10		15		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		7		10	ns

Switching Waveforms

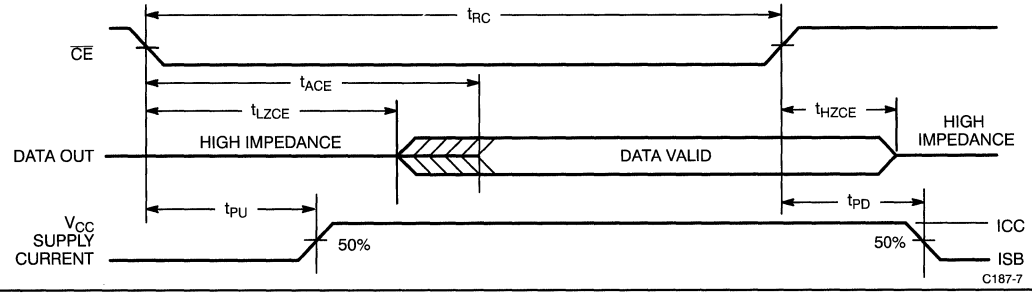
Read Cycle No. 1[10, 11]



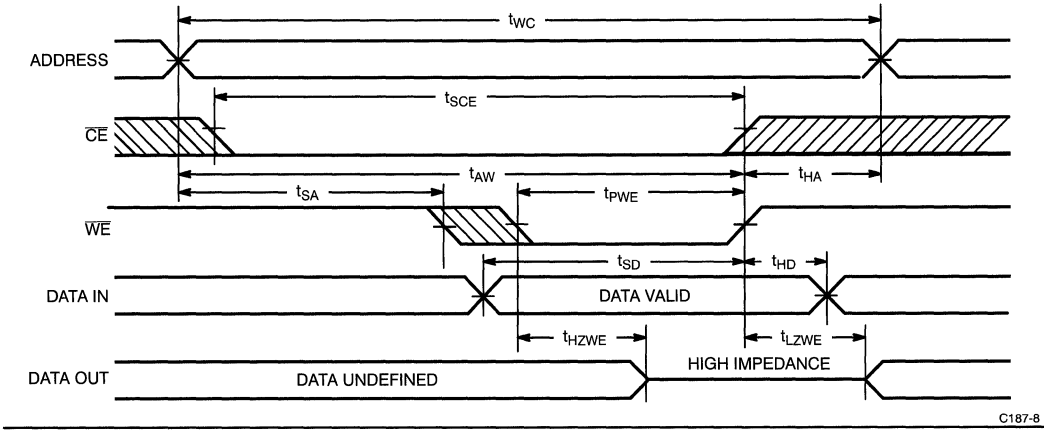
Note:
11. Device is continuously selected, $\overline{CE} = V_{IL}$.

Switching Waveforms (continued)

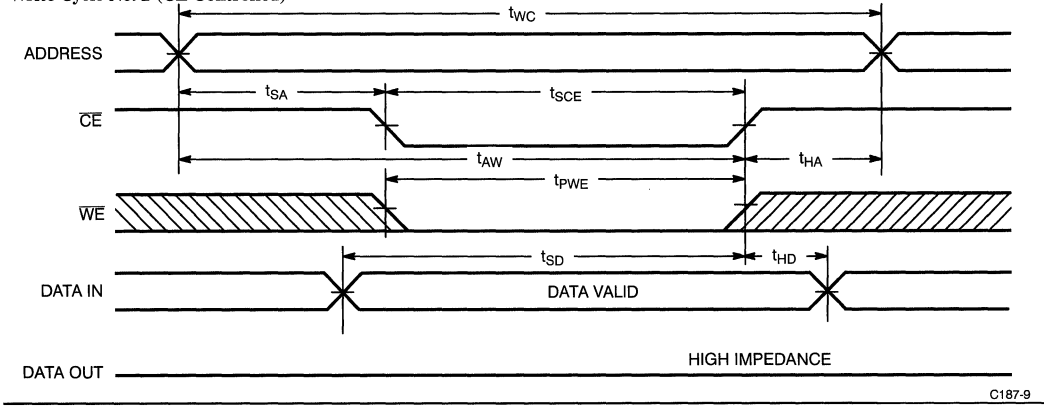
Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 13]

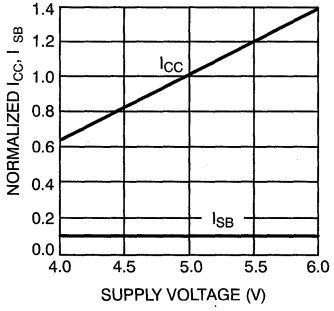


Notes:

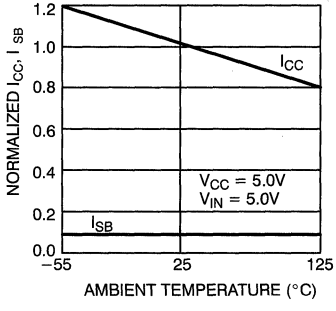
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

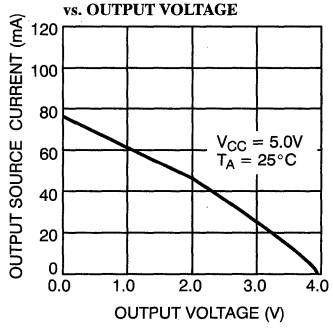
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



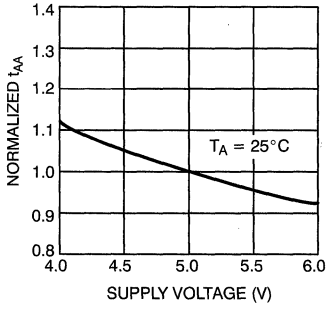
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



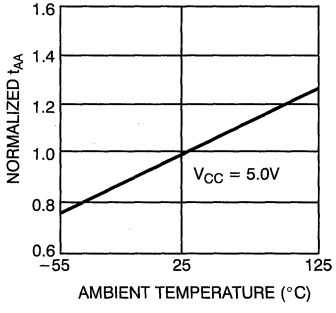
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



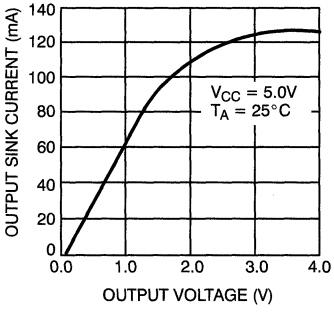
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



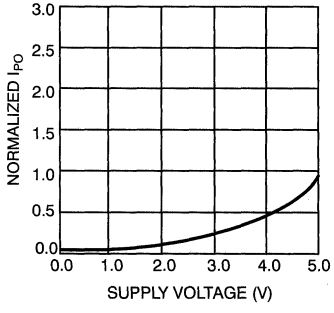
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



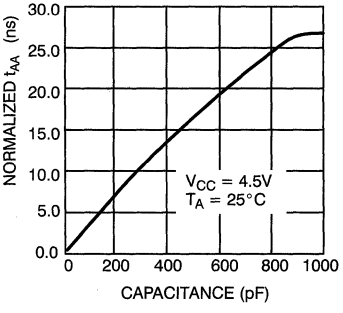
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



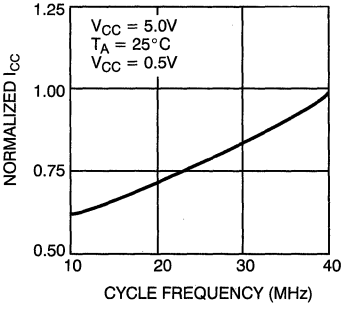
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information[14]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C187-12PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-12VC	V13	24-Lead Molded SOJ	
15	CY7C187-15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-15VC	V13	24-Lead Molded SOJ	
20	CY7C187-20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-20VC	V13	24-Lead Molded SOJ	
25	CY7C187-25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-25VC	V13	24-Lead Molded SOJ	
35	CY7C187-35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-35VC	V13	24-Lead Molded SOJ	

Shaded area contains preliminary information.

Note:
14. For military variations, see the CY7C187A datasheet.

Document #: 38-00038-J

CY7C187A

64K x 1 Static RAM

Features

- **High speed**
  — 20 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 495 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C187A is a high-performance CMOS static RAM organized as 65,536 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187A has an automatic power-down feature, reducing the power consumption by 55% when deselected.

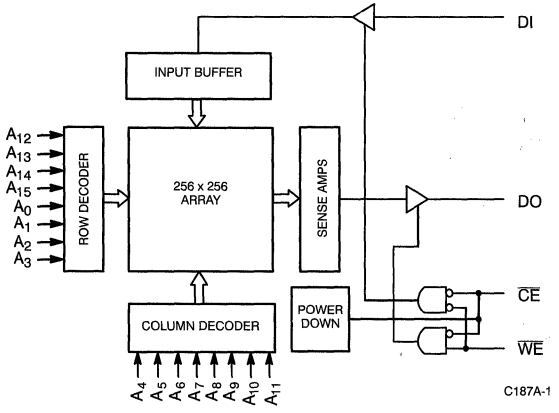
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

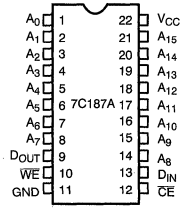
The CY7C187A utilizes a die coat to insure alpha immunity.

Logic Block Diagram



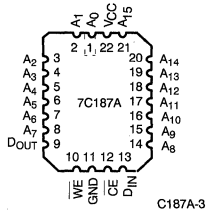
Pin Configurations

DIP
Top View



C187A-2

LCC
Top View



C187A-3

Selection Guide[1]

		7C187A–15	7C187A–20	7C187A–25	7C187A–35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	90	80	80
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

Note:
1. For commercial specifications, see CY7C187 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C187A−15 Min.	7C187A−15 Max.	7C187A−20 Min.	7C187A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Mil		160		90	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Mil		40		40	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Mil		20		20	mA

Shaded area contains preliminary information.

Notes:

2. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range[4] (continued)

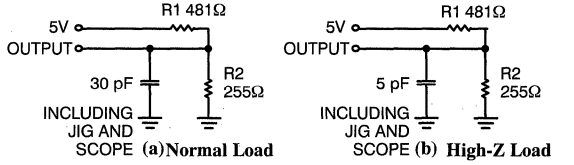
Parameter	Description	Test Conditions		7C187A–25 Min.	7C187A–25 Max.	7C187A–35 Min.	7C187A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Mil		80		80	mA
I_{SB1}	Automatic $\overline{CE}$ Power–Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Mil		40		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Mil		20		20	mA

Capacitance[7]

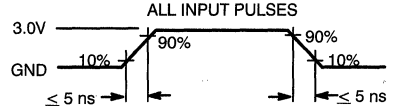
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

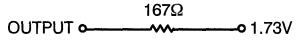


C187A-4



C187A-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 8]

Parameter	Description	7C187A–15		7C187A–20		7C187A–25		7C187A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7		7		10	ns

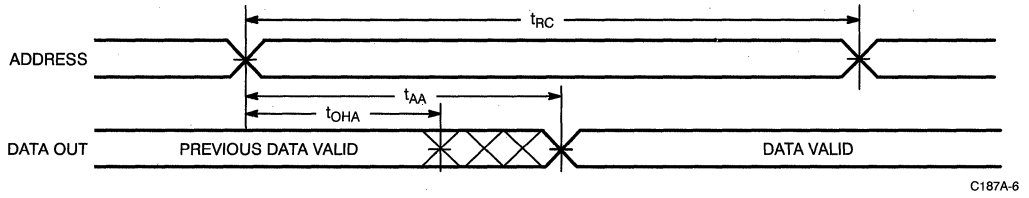
Shaded area contains preliminary information.

Notes:

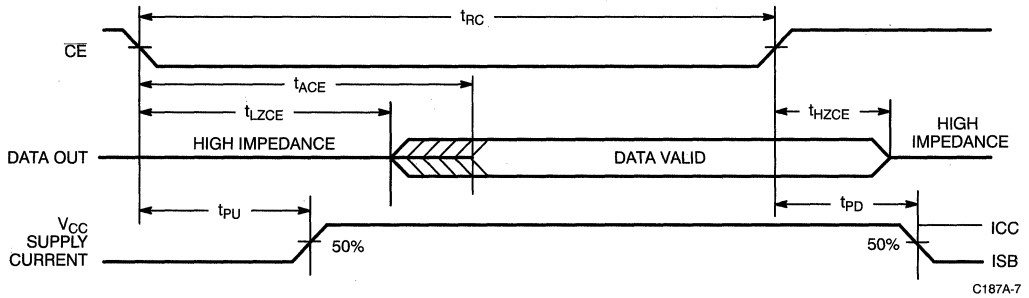
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

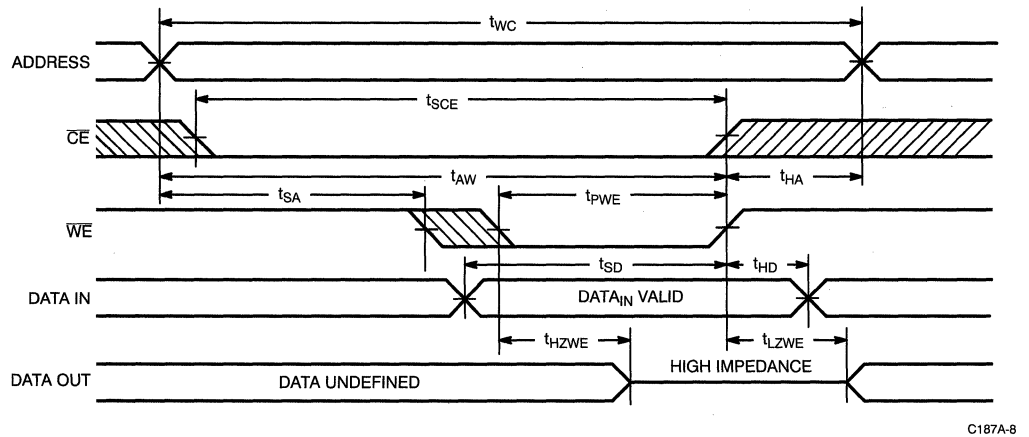
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



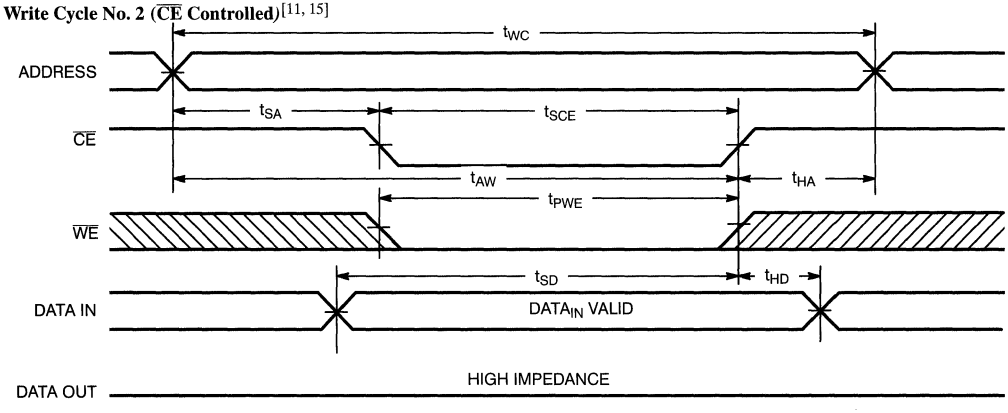
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

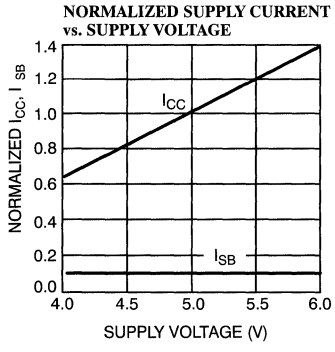
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15]

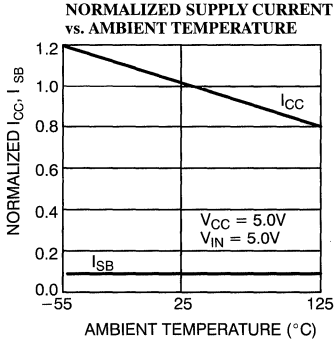


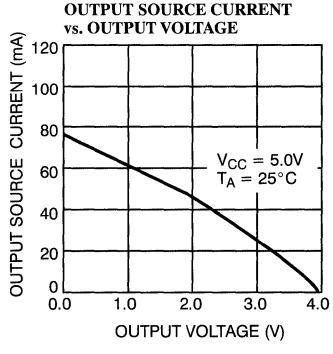
C187A-9

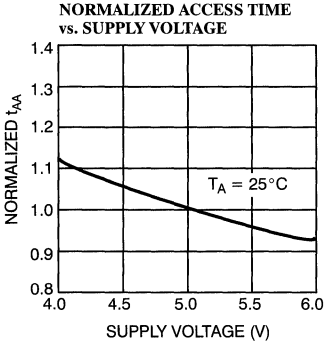
Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

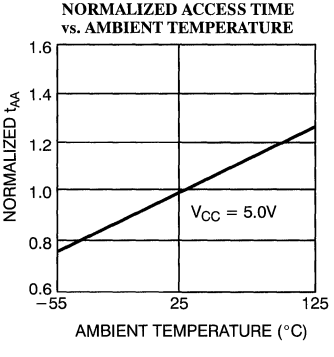
Typical DC and AC Characteristics

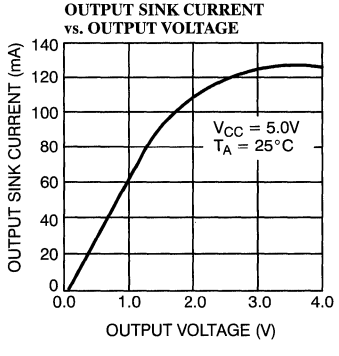




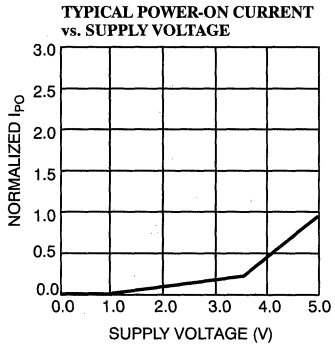


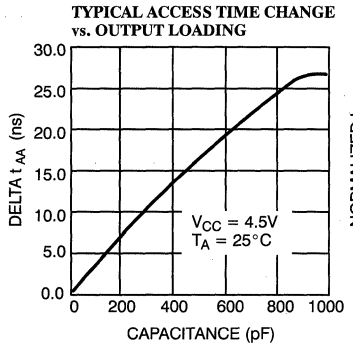


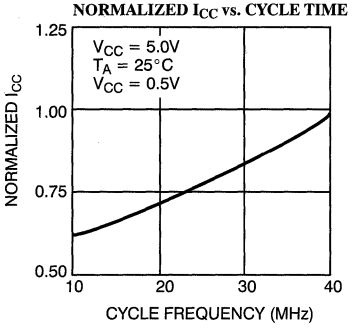




Typical DC and AC Characteristics (continued)







Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C187A–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–15LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
20	CY7C187A–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–20LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
25	CY7C187A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–25LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
35	CY7C187A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A–35LMB	L52	22-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00115–D

CY7C188

32K x 9 Static RAM

Features

- **High speed**
  - **20 ns**
- **Automatic power-down when deselected**
- **Low active power**
  - **965 mW**
- **Low standby power**
  - **220 mW**
- **CMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**

Functional Description

The CY7C188 is a high-performance CMOS static RAM organized as 32,768 words by 9 bits. Easy memory expansion is provided by an active-LOW chip enable ($\overline{CE}_1$), an active-HIGH chip enable (CE_2), an active-LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking $\overline{CE}_1$ and write enable ($\overline{WE}$) inputs LOW and CE_2 input HIGH. Data on the nine I/O pins (I/O_0 – I/O_8) is then written into the location specified on the address pins (A_0 – A_{14}).

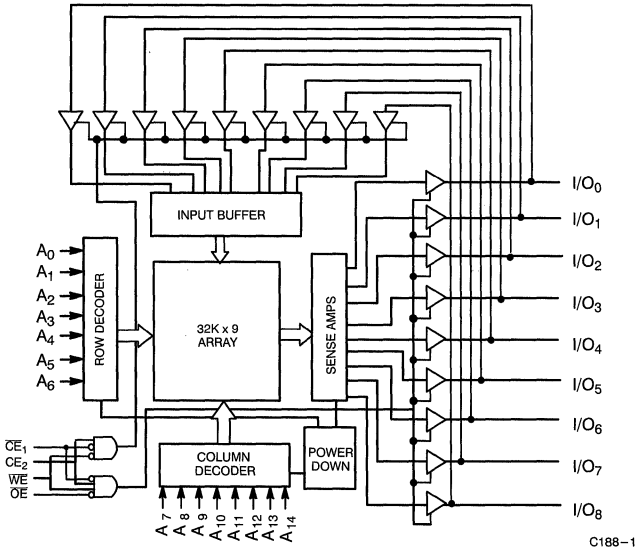
Reading from the device is accomplished by taking $\overline{CE}_1$ and $\overline{OE}$ LOW while forcing $\overline{WE}$ and CE_2 HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The nine input/output pins (I/O_0 – I/O_8) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C188 is available in standard 300-mil-wide DIPs and SOJs.

A die coat is used to ensure alpha immunity.

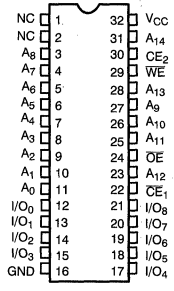
Logic Block Diagram



C188–1

Pin Configuration

DIP/SOJ
Top View



C188–2

Selection Guide

		7C188–20	7C188–25	7C188–35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)	Commercial	170	165	160
	Military		175	160
Maximum Standby Current (mA)		35	35	30

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND (Pin 32 to Pin 16) ..... −0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C188−20 Min.	7C188−20 Max.	7C188−25 Min.	7C188−25 Max.	7C188−35 Min.	7C188−35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		170		165		160	mA
			Mil				175		170	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		35		35		30	mA
			Mil				35		30	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ −0.3V or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V or $V_{IN} \leq$ 0.3V, f = 0	Com'l		15		15		15	mA
			Mil				20		20	mA

Shaded areas contain preliminary information.

Notes:

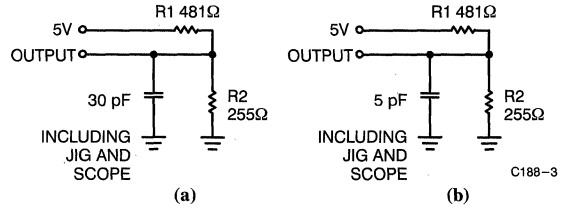
1. Minimum voltage is equal to −2.0V for pulse durations less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

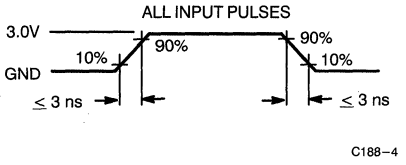
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{IN}: Controls			8	pF
C_{OUT}	Output Capacitance		8	pF

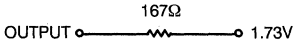
Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[6, 7]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

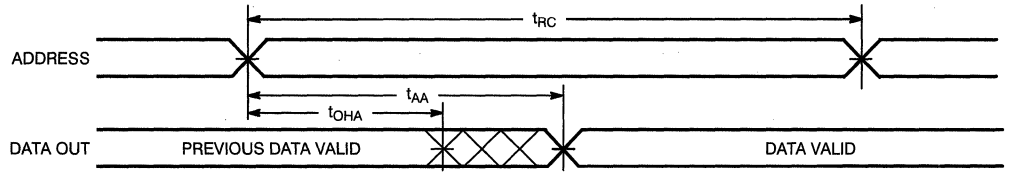
Parameter	Description	7C188–20		7C188–25		7C188–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		35		ns
t_{AA}	Address to Data Valid		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Data Valid		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		9		10		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		9		11		15	ns
t_{LZCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[7, 8]		9		11		15	ns
t_{PU}	$\overline{CE}_1$ LOW or CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power-Down		20		20		20	ns
WRITE CYCLE[9, 10]								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{SCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Write End	15		18		22		ns
t_{AW}	Address Set-Up to Write End	15		20		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		18		22		ns
t_{SD}	Data Set-Up to Write End	10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]	0	7	0	11	0	15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7, 8]	3		3		3		ns

Notes:

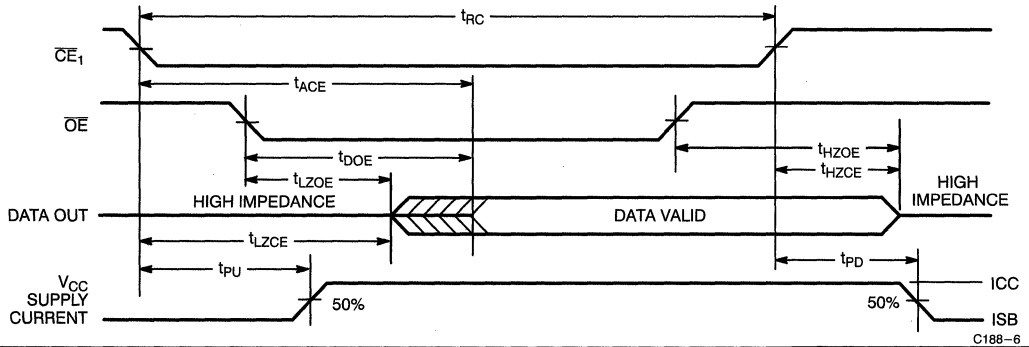
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$, LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

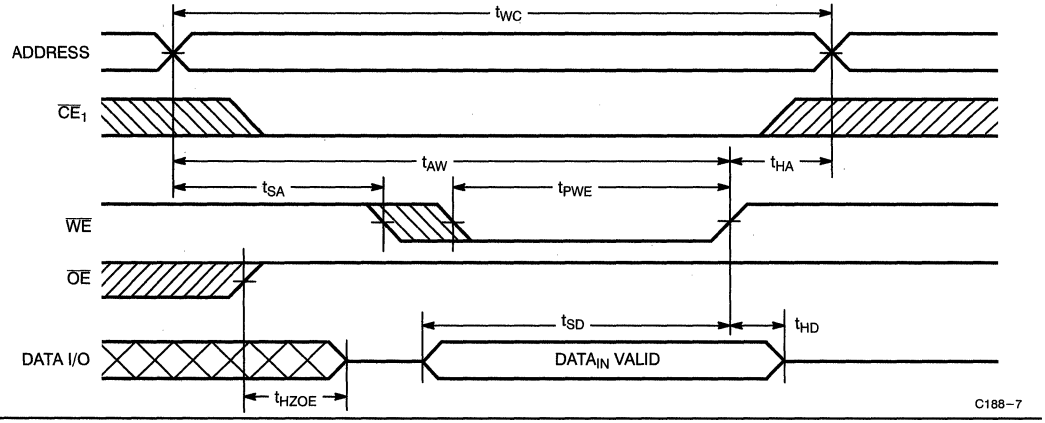
Read Cycle No. 1[11, 12]



Read Cycle No. 2 (Chip-Enable Controlled)[12, 13, 14]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 14, 15, 16]

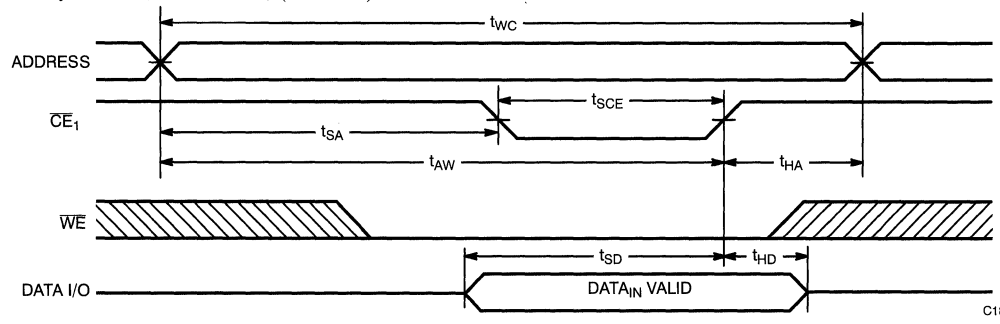


Notes:

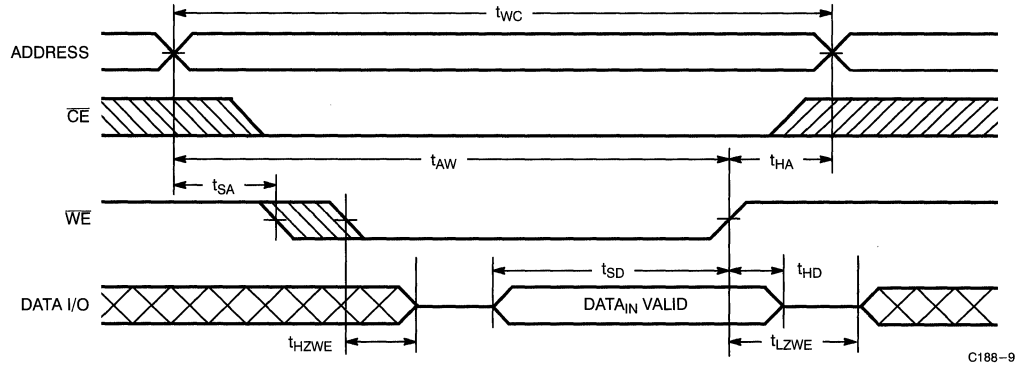
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Timing parameters are the same for all chip enable signals ($\overline{CE_1}$ and CE_2), so only the timing for $\overline{CE_1}$ is shown.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) (continued) [9, 14, 15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [10, 14, 16]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C188–20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188–20VC	V32	32-Lead (300-Mil) Molded SOJ	
25	CY7C188–25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188–25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188–25DMB	D32	32-Lead (300-Mil) CerDIP	Military
35	CY7C188–35PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C188–35VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C188–35DMB	D32	32-Lead (300-Mil) CerDIP	Military

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00220–C

CY7C191
CY7C192

64K x 4 Static RAM with Separate I/O

Features

- **High speed**
  — 12 ns
- **Transparent write (CY7C191)**
- **CMOS for optimum speed/power**
- **Low active power**
  — 880 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C191 and CY7C192 are high-performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

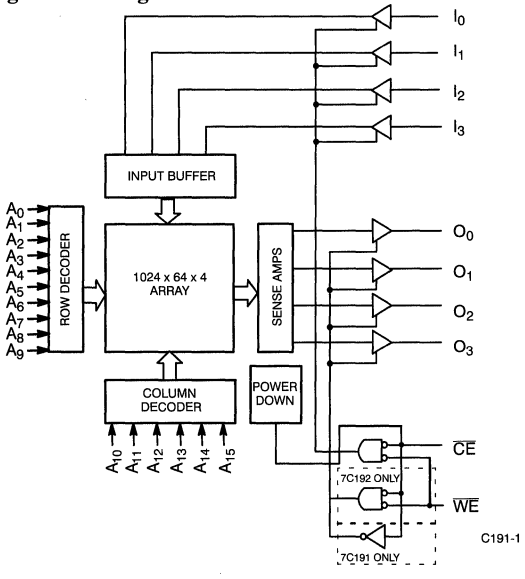
Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

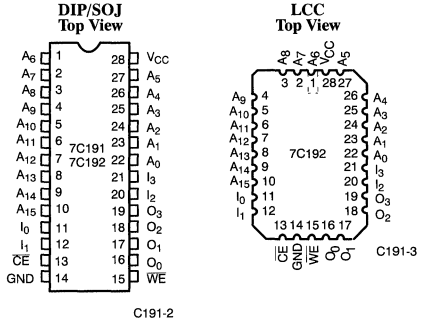
The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (CY7C192 only), or chip enable ($\overline{CE}$) is HIGH.

A die coat ensures alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C191–12 7C192–12	7C191–15 7C192–15	7C191–20 7C192–20	7C191–25 7C192–25	7C191–35 7C192–35	7C191–45 7C192–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	155	145	135	115	115	
	Military		160	150	125	125	125
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C191−12 7C192−12 Min.	7C191−12 7C192−12 Max.	7C191−15 7C192−15 Min.	7C191−15 7C192−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		155		145	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10	mA
			Mil				15	

Shaded area contains preliminary information.

Notes:

1. Minimum voltage is equal to − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

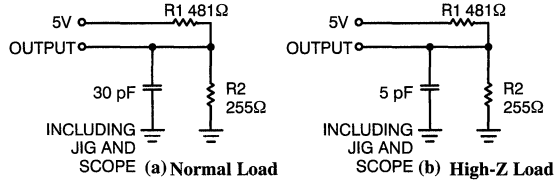
Parameter	Description	Test Conditions		7C191–20 7C192–20 Min.	7C191–20 7C192–20 Max.	7C191–25, 35, 45 7C192–25, 35, 45 Min.	7C191–25, 35, 45 7C192–25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		135		115	mA
			Mil		150		125	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≤ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			15		15	mA

Shaded area contains advanced information.

Capacitance[5]

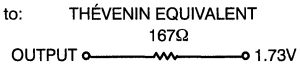
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

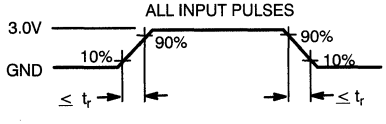
AC Test Loads and Waveforms[6]



C191-4

Equivalent to: THÉVENIN EQUIVALENT





C191-5

Notes:
5. Tested initially and after any design or process changes that may affect these parameters.
6. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3,7]

Parameter	Description	7C191–12 7C192–12		7C191–15 7C192–15		7C191–20 7C192–20		7C191–25 7C192–25		7C191–35 7C192–35		7C192–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,9]		5		7		9		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35		45	ns
WRITE CYCLE[10]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		18		22		22		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		18		22		22		ns
t_{SD}	Data Set-Up to Write End	8		9		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z (7C192)[8]	3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z (7C192)[8,9]		7		7		10		11		15		15	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C191)		12		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C191)		12		15		20		20		30		35	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C191)		12		15		20		25		35		45	ns

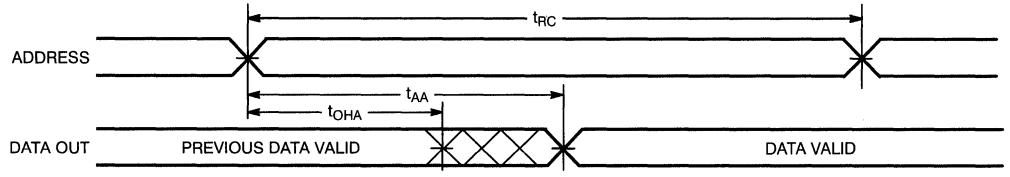
Shaded area contains preliminary information.

Notes:

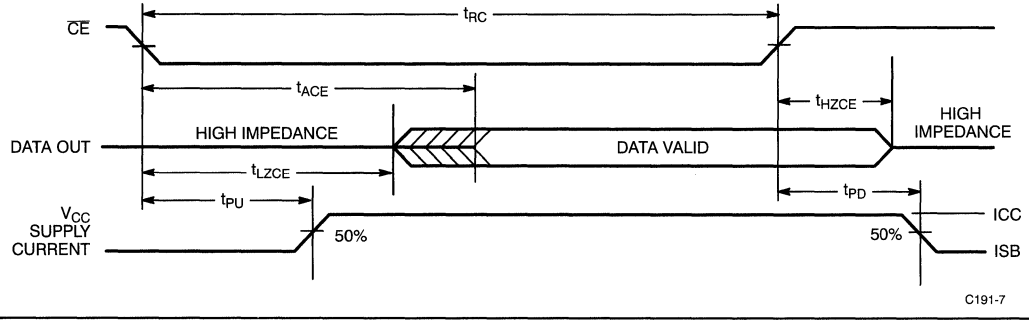
7. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 through −45 speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed by design and not 100% tested.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

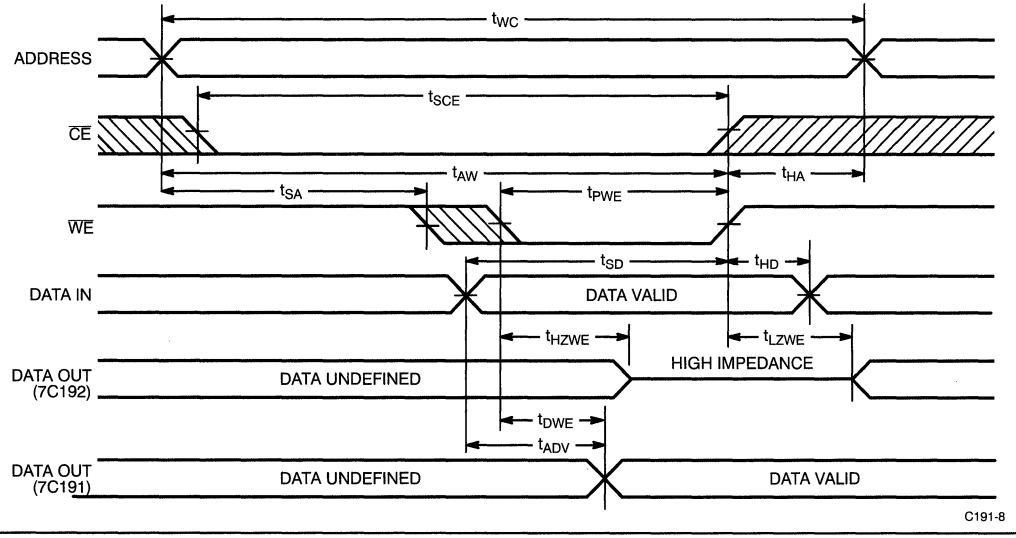
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



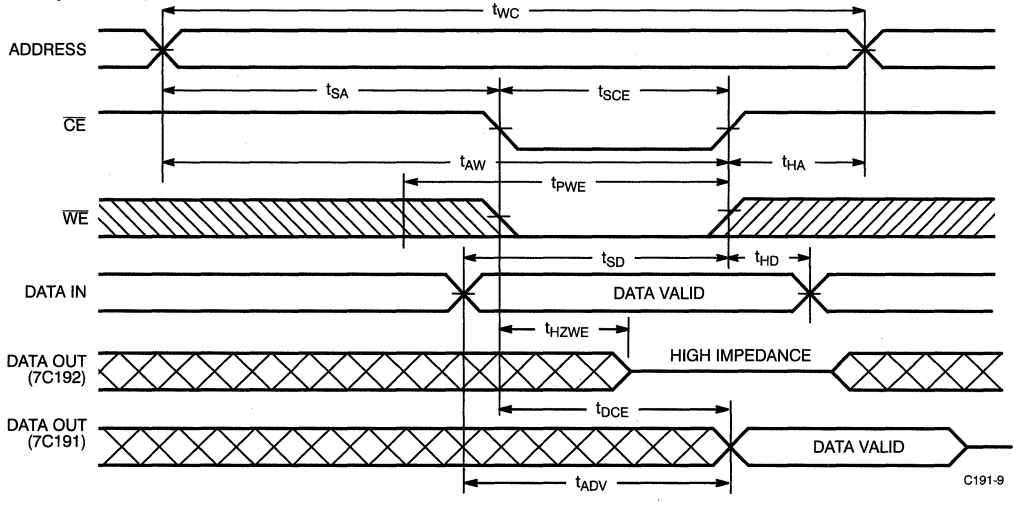
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



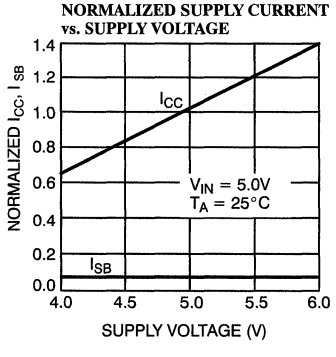
Notes:
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C192 only).

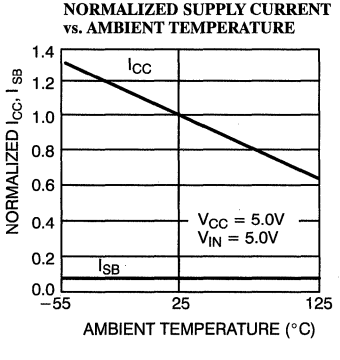
Switching Waveforms (continued)

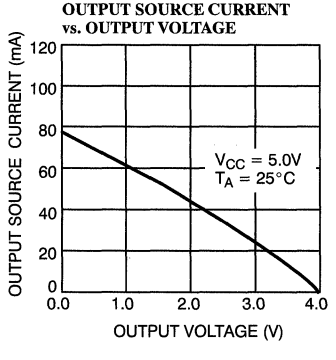
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

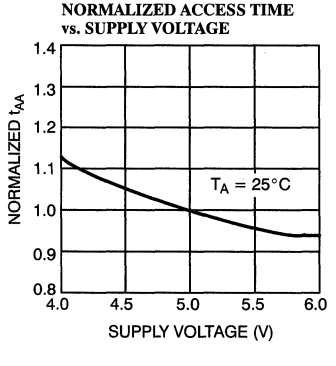


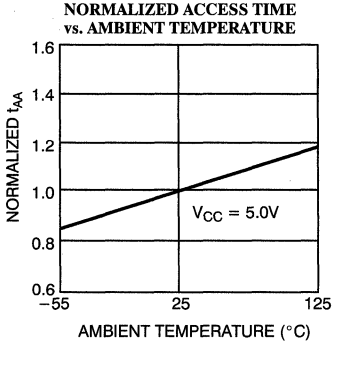
Typical DC and AC Characteristics

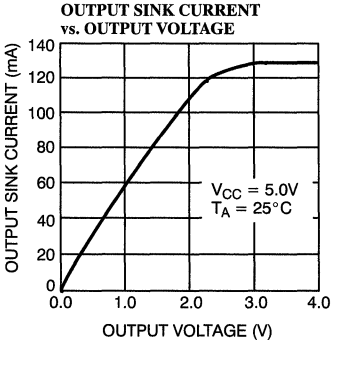




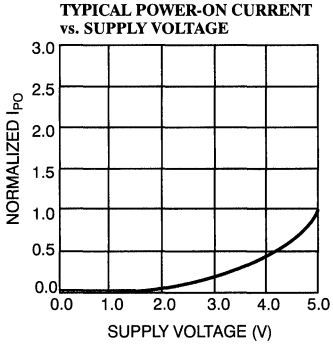


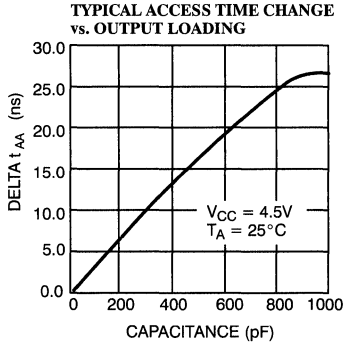


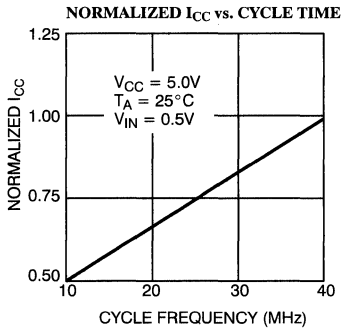




Typical DC and AC Characteristics (continued)







Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C191–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191–12VC	V21	28-Lead Molded SOJ	
15	CY7C191–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191–15VC	V21	28-Lead Molded SOJ	
20	CY7C191–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
25	CY7C191–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
35	CY7C191–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial

Shaded area contains preliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C192–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–12VC	V21	28-Lead Molded SOJ	
15	CY7C192–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–15VC	V21	28-Lead Molded SOJ	
	CY7C192–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C192–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–20VC	V21	28-Lead Molded SOJ	
	CY7C192–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C192–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–25VC	V21	28-Lead Molded SOJ	
	CY7C192–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C192–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192–35VC	V21	28-Lead Molded SOJ	
	CY7C192–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C192–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Note:
15. CY7C191 only

CY7C193

32K x 8 Synchronous SRAM

Features

- **Synchronous 32K x 8 SRAM**
- **Supports 33-MHz 486 cache systems with zero wait states**
- **Clock-to-output time**
  — 20 ns into 30 pF
- **Synchronous self-timed write**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{OE}$ feature**

Functional Description

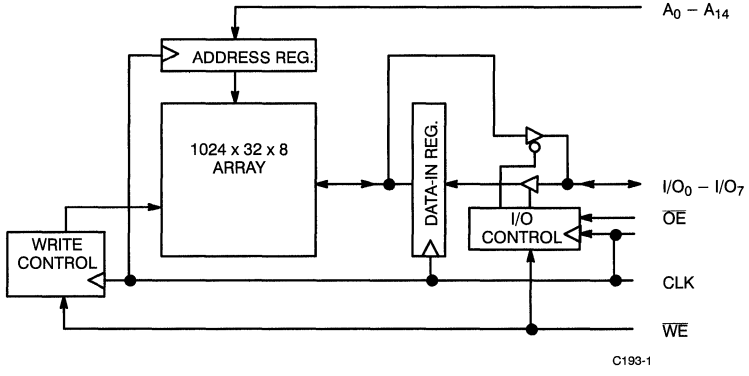
The CY7C193 is a synchronous 32K x 8 SRAM designed to allow zero-wait-state cache designs, both write back and write through, in microprocessor-based systems with 33-MHz bus speeds. The SRAM has a fast clock-to-output time of 20 ns into a load of 30 pF. The address, data, and $\overline{WE}$ signals are all synchronous, while the $\overline{OE}$ signal is asynchronous.

If $\overline{WE}$ is sampled HIGH at the rising edge of CLK (signifying a read cycle), the address is captured in the on-chip address register. The data is then driven out a maximum of 20 ns later (if the load on the data lines is 30 pF) allowing ample time for the data to be set up to the next rising edge of the clock in a 33-MHz cache system. If the load on the data lines is less than 30 pF, the clock-to-output time will be faster than 20 ns. See the derating curve at the end of the datasheet for details. The output data can also be controlled asynchronously by $\overline{OE}$. The data I/O lines will switch from outputs to inputs (i.e., to the high-impedance state) within 7 ns of $\overline{OE}$ going HIGH. Valid data will be driven back out within 10 ns of $\overline{OE}$ going LOW again.

If the $\overline{WE}$ signal is sampled LOW at the rising edge of CLK (signifying a write cycle), the address is captured in the on-chip address register and the data to be written is captured in the data-in register. The CY7C193 then performs a synchronous self-timed write of the data to the specified location. The data I/O lines should be put into the high-impedance state by bringing $\overline{OE}$ HIGH before the data to be written is driven in to the SRAM.

Although the CY7C193 is ideally suited for 33-MHz 486-based cache systems, it is very useful in many other applications as well. The synchronous address and data interface, along with the synchronous self-timed write feature, simplify designs of almost any system.

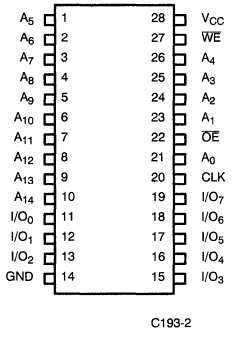
Logic Block Diagram



C193-1

Pin Configuration

DIP/SOJ
Top View



C193-2

Selection Guide

		7C193–20
Maximum Access Time (ns)		20
Maximum Operating Current (mA)	Commercial	160

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage ..... − 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

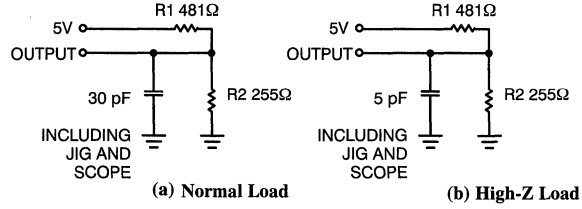
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C193−20		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−5	+5	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		160	mA

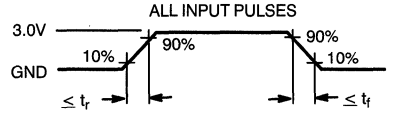
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms

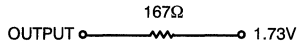


C193-3



C193-4

Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[3]

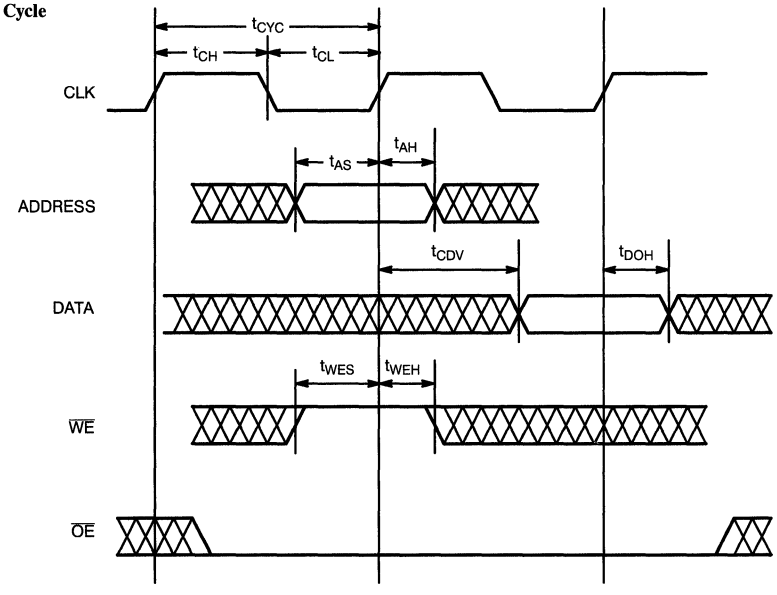
Parameter	Description	7C193–20		Unit
		Min.	Max.	
t_{CYC}	Clock Cycle Time	30		ns
t_{CH}	Clock Pulse Width High	11		ns
t_{CL}	Clock Pulse Width Low	11		ns
t_{CDV}	Clock Rise to Data Output Valid		20	ns
t_{DOH}	Data Output Hold after Clock Rise	3		ns
t_{AS}	Address Setup Before Clock Rise	5		ns
t_{AH}	Address Hold After Clock Rise	1		ns
t_{WES}	$\overline{WE}$ Setup Before Clock Rise	5		ns
t_{WEH}	$\overline{WE}$ Hold After Clock Rise	1		ns
t_{DS}	Data Input Setup Before Clock Rise	5		ns
t_{DH}	Data Input Hold After Clock Rise	1		ns
t_{DOE}	$\overline{OE}$ Low to Output Valid		9	ns
t_{HZOE}	$\overline{OE}$ High to Output High-Z[4, 5]		7	ns
t_{WEHZ}	$\overline{WE}$ Sampled Low to Output High-Z[4]		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[5]	0		
t_{CLZ}	Clock Rise to Low-Z	8		

Notes:

3. Test conditions assume signal transition time (t_r, t_f) of 3 ns or less, timing reference level of 1.5V, input pulse level of 0 to 3.0V, and outputs loading per specified I_{OH}/I_{OL}, outputs loaded with 30 pF per (a) in AC Test Loads and Waveforms.
4. t_{HZOE} and t_{WEHZ} are specified with 5 pF capacitive load per (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZOE} is less than t_{LZOE} and t_{WEHZ} is less than t_{CLZ} for any given device.

Switching Waveforms

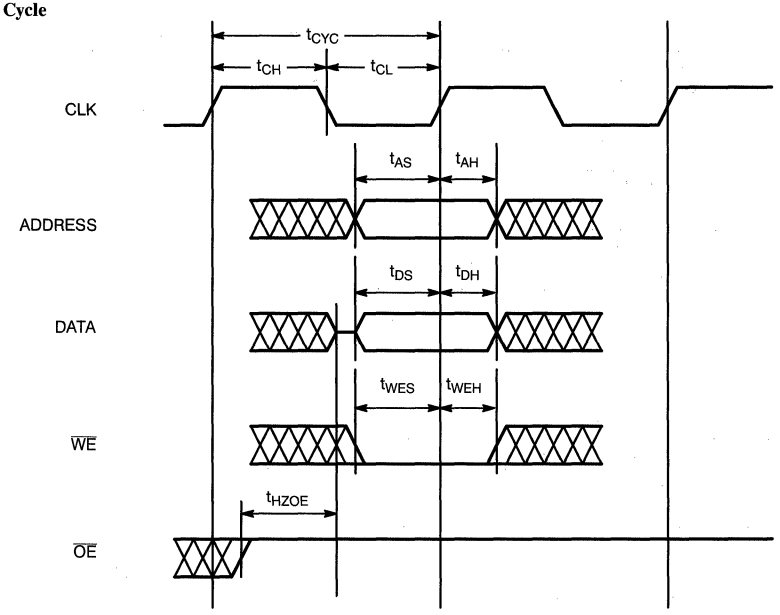
Read Cycle



C193-5

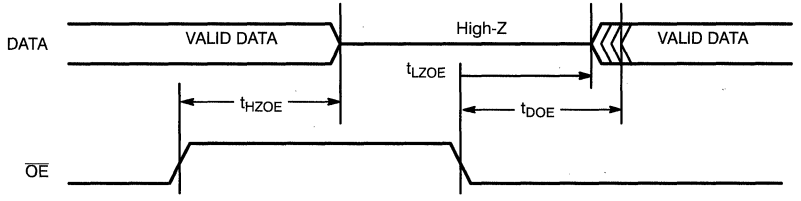
Switching Waveforms (continued)

Write Cycle



C193-6

$\overline{OE}$ Timing



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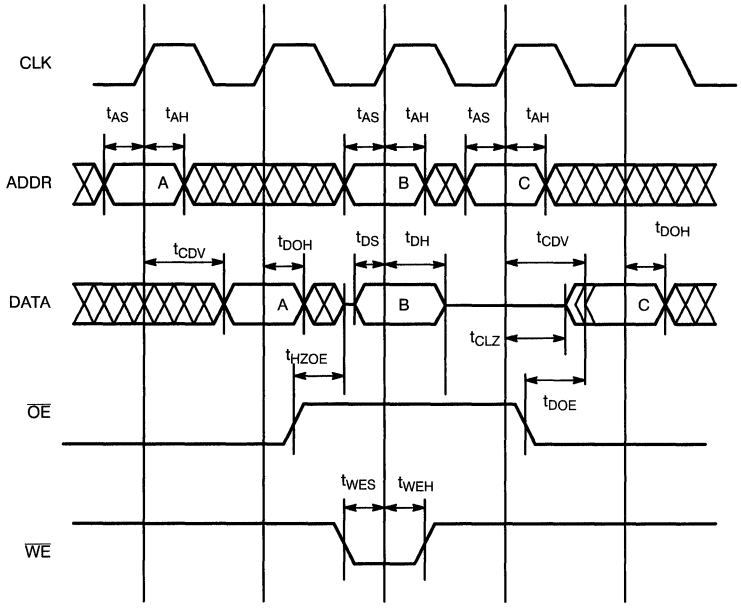
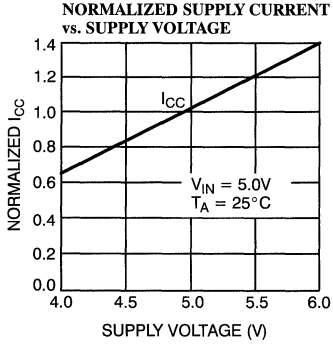
Switching Waveforms (continued)

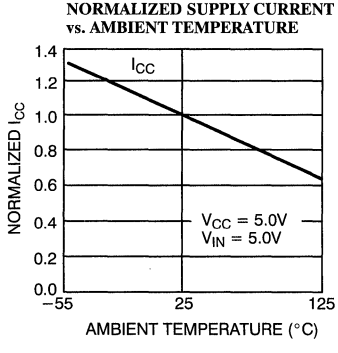
Read-Write-Read Timing

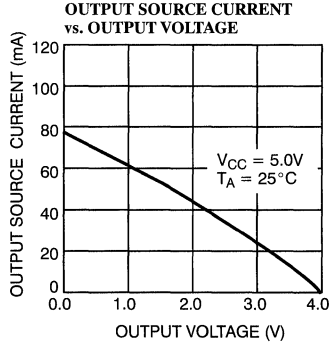


C193-8

Typical DC and AC Characteristics

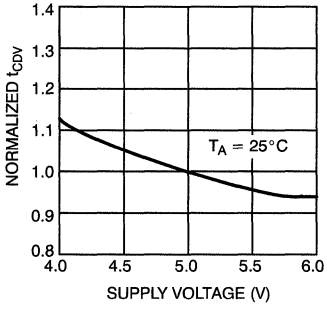




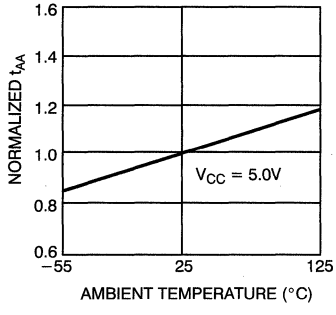


Typical DC and AC Characteristics (continued)

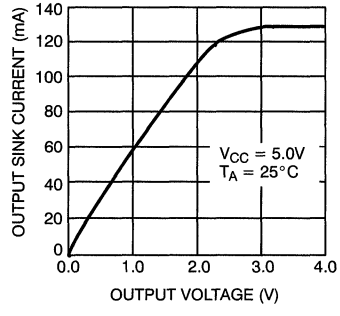
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



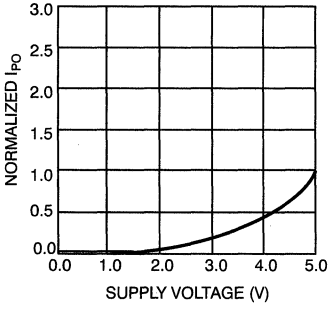
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



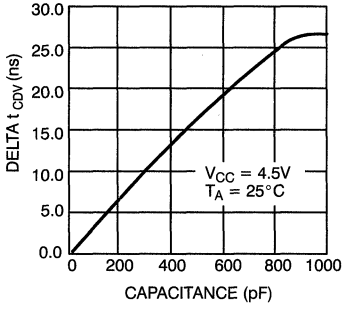
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



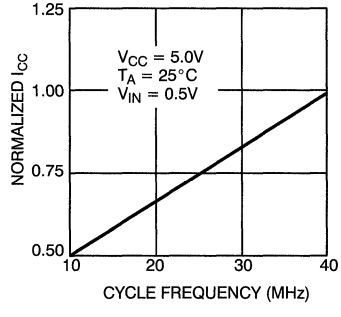
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C193–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C193–20VC	V21	28-Lead Molded SOJ	

Shaded area contains preliminary information.

Document #: 38–00254–A

CY7C194
CY7C195
CY7C196

64K x 4 Static RAM

Features

- **High speed**
  - **— 12 ns**
- **Output enable ($\overline{OE}$) feature (7C195 and 7C196)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 880 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

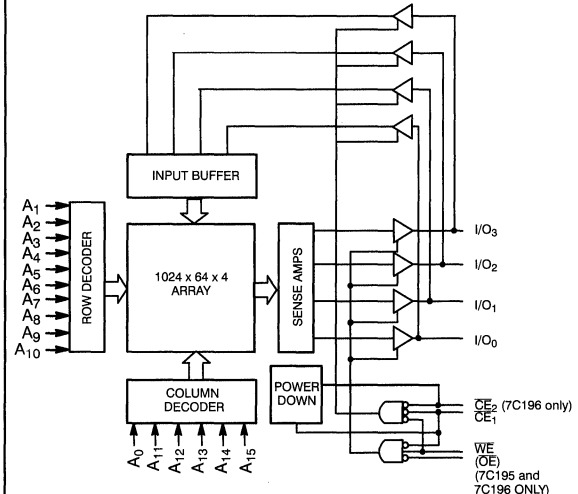
The CY7C194, CY7C195, and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) is written into the memory location, specified on the address pins (A_0 through A_{15}).

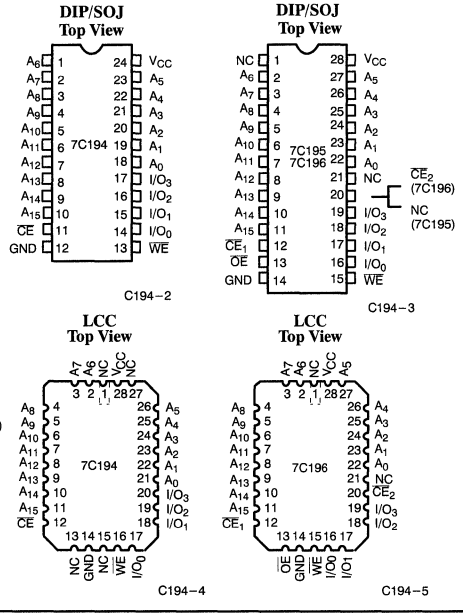
Reading the device is accomplished by taking the chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C194-12 7C195-12 7C196-12	7C194-15 7C195-15 7C196-15	7C194-20 7C195-20 7C196-20	7C194-25 7C195-25 7C196-25	7C194-35 7C195-35 7C196-35	7C194-45 7C196-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	155	145	135	115	115	
	Military		160	150	125	125	125
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C194−12 7C195−12 7C196−12 Min.	7C194−12 7C195−12 7C196−12 Max.	7C194−15 7C195−15 7C196−15 Min.	7C194−15 7C195−15 7C196−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}[1]	Input LOW Voltage			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		155		145	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10	mA
			Mil				15	

Shaded area contains preliminary information.

Notes:

1. Minimum voltage is equal to −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

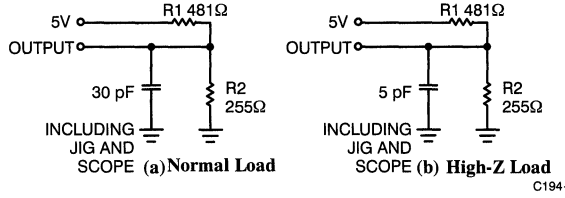
Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions		7C194–20 7C195–20 7C196–20 Min.	7C194–20 7C195–20 7C196–20 Max.	7C194–25, 35, 45 7C195–25, 35 7C196–25, 35, 45 Min.	7C194–25, 35, 45 7C195–25, 35 7C196–25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		135		115	mA
			Mil		150		125	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}_{1,2}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			15		15	mA

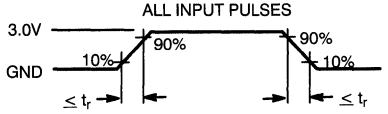
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[7]

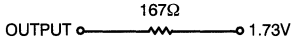


C194–6



C194–7

Equivalent to: THÉVENIN EQUIVALENT



Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3, 8]

Parameter	Description		7C194–12 7C195–12 7C196–12		7C194–15 7C195–15 7C196–15		7C194–20 7C195–20 7C196–20		7C194–25 7C195–25 7C196–25		7C194–35 7C195–35 7C196–35		7C194–45 7C196–45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE															
t_{RC}	Read Cycle Time		12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid			12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		3		3		3		ns
t_{ACE1}, t_{ACE2}	$\overline{CE}$ LOW to Data Valid			12		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C195 7C196		5		7		9		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7C195 7C196	0		0		0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10]	7C195 7C196		5		7		9		11		15		15	ns
t_{LZCE1}, t_{LZCE2}	$\overline{CE}$ LOW to Low Z[9]		3		3		3		3		3		3		ns
t_{HZCE1}, t_{HZCE2}	$\overline{CE}$ HIGH to High Z[9,10]			5		7		9		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			12		15		20		25		35		45	ns
WRITE CYCLE[11]															
t_{WC}	Write Cycle Time		12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		9		10		15		18		22		22		ns
t_{AW}	Address Set-Up to Write End		9		10		15		20		25		35		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		8		9		15		18		22		22		ns
t_{SD}	Data Set-Up to Write End		8		9		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]		3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 8]			7		7		10	0	13	0	15	0	20	ns

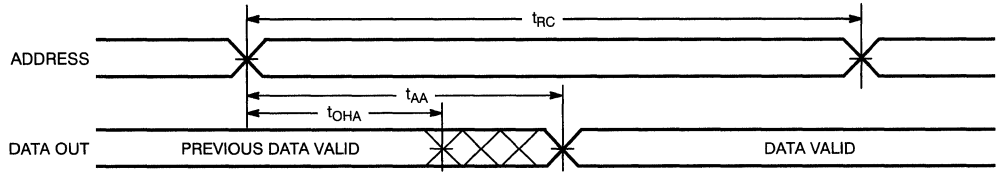
Shaded area contains preliminary information.

Notes:

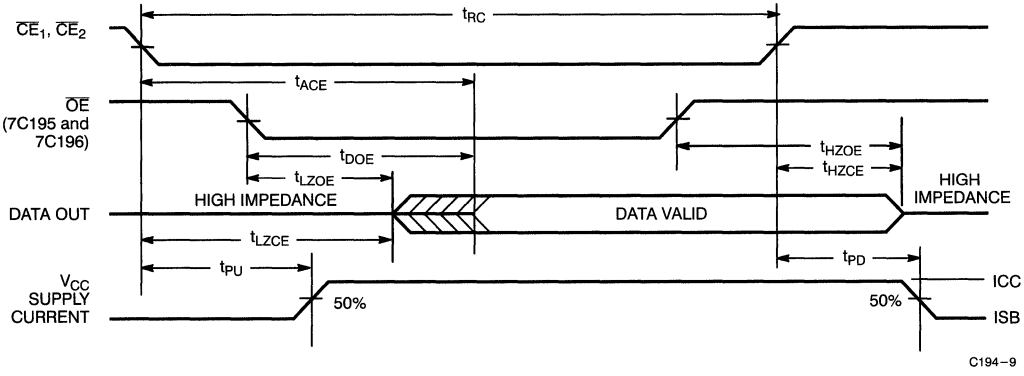
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

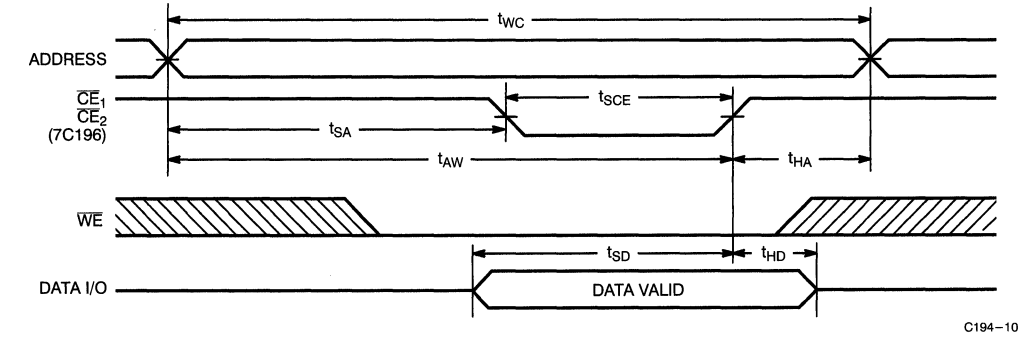
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



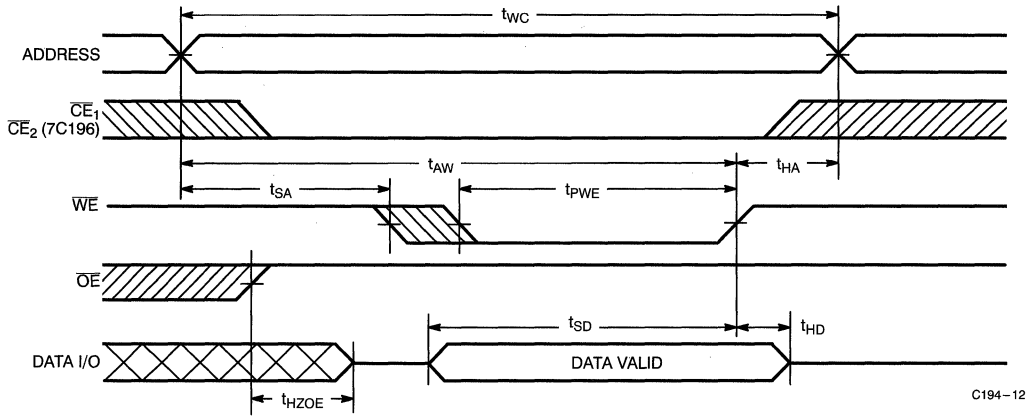
Write Cycle No. 1 ($\overline{CE}$ Controlled)[11, 15, 16]



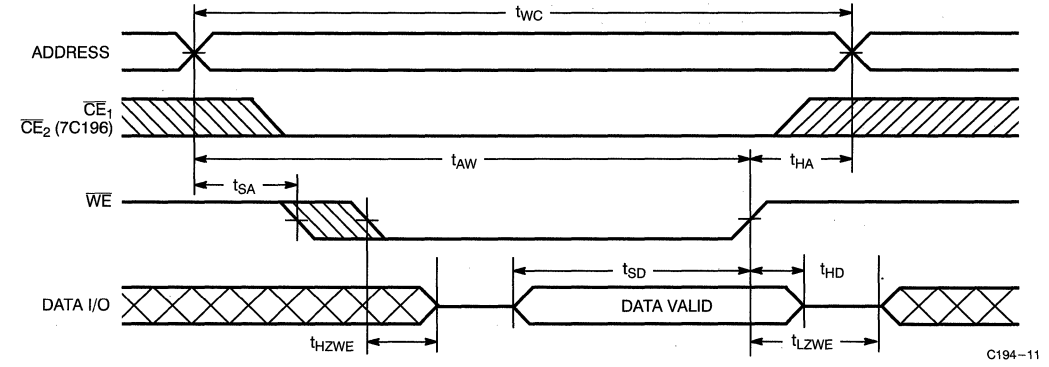
Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected: $\overline{CE_1} = V_{IL}$, $\overline{CE_2} = V_{IL}$ (7C196), and $\overline{OE} = V_{IL}$ (7C195 and 7C196).
14. Address valid prior to or coincident with $\overline{CE_1}$ and $\overline{CE_2}$ transition LOW.
15. Data I/O will be high impedance if $\overline{OE} = V_{IH}$ (7C195 and 7C196).
16. If any $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

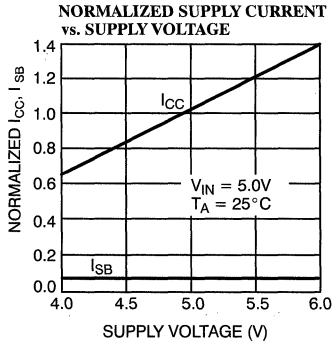
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for 7C195 and 7C196 only)[11, 15, 16]

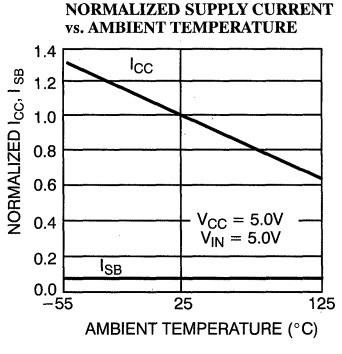


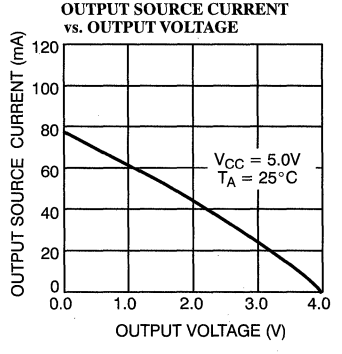
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16, 17]



Typical DC and AC Characteristics

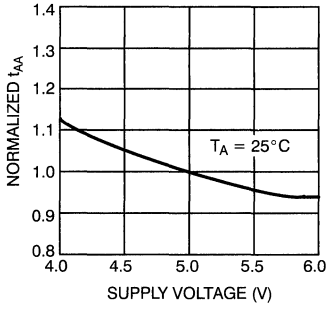




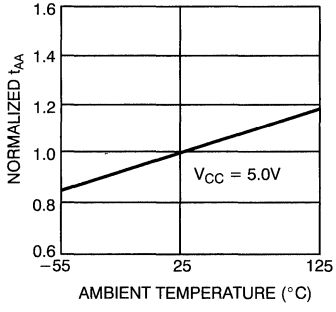


Typical DC and AC Characteristics (continued)

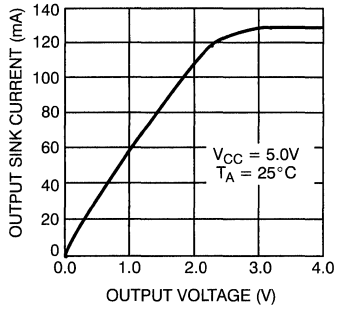
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



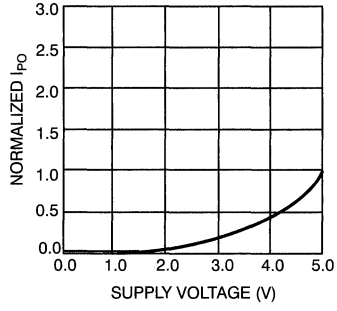
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



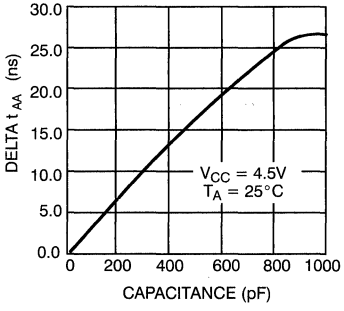
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



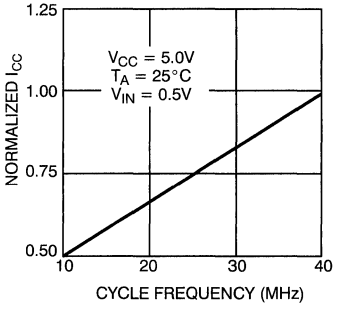
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C194 Truth Table

$\overline{CE}$	$\overline{WE}$	Data I/O	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7C195 Truth Table

$\overline{CE}_1$	$\overline{WE}$	$\overline{OE}$	Data I/O	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect	Active (I_{CC})

7C196 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Data I/O	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	H	X	X			
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Deselect	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C194–12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–12VC	V13	24-Lead Molded SOJ	
15	CY7C194–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–15VC	V13	24-Lead Molded SOJ	
	CY7C194–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C194–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–20VC	V13	24-Lead Molded SOJ	
	CY7C194–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C194–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–25VC	V13	24-Lead Molded SOJ	
	CY7C194–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C194–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194–35VC	V13	24-Lead Molded SOJ	
	CY7C194–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C194–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C195–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–12VC	V21	28-Lead Molded SOJ	
15	CY7C195–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–15VC	V21	28-Lead Molded SOJ	
20	CY7C195–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–20VC	V21	28-Lead Molded SOJ	
25	CY7C195–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–25VC	V21	28-Lead Molded SOJ	
35	CY7C195–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195–35VC	V21	28-Lead Molded SOJ	

Shaded areas contain preliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C196–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–12VC	V21	28-Lead Molded SOJ	
15	CY7C196–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–15VC	V21	28-Lead Molded SOJ	
	CY7C196–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
20	CY7C196–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–20VC	V21	28-Lead Molded SOJ	
	CY7C196–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
25	CY7C196–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–25VC	V21	28-Lead Molded SOJ	
	CY7C196–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
35	CY7C196–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196–35VC	V21	28-Lead Molded SOJ	
	CY7C196–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
45	CY7C196–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}, $_{ACE2}$	7, 8, 9, 10, 11
t_{DOE}[18]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
18. 7C195 and 7C196 only.

Document #: 38–00081–J

CY7C197

256K x 1 Static RAM

Features

- **High speed**
  — 12 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 880 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 75% when deselected.

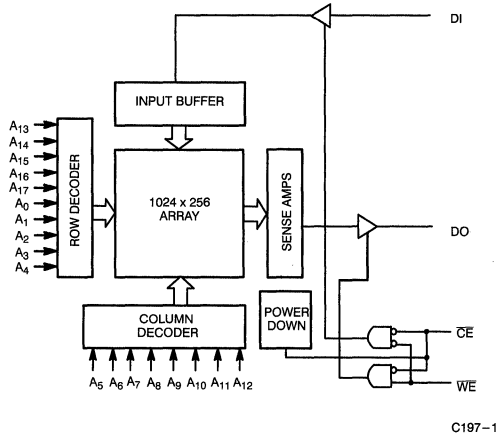
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The CY7C197 utilizes a die coat to ensure alpha immunity.

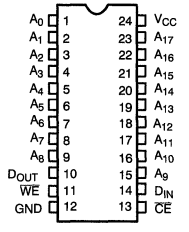
Logic Block Diagram



C197–1

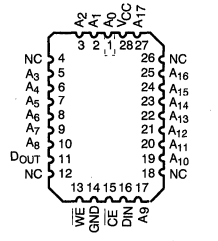
Pin Configurations

DIP/SOJ
Top View



C197–2

LCC
Top View



C197–3

Selection Guide

		7C197–12	7C197–15	7C197–20	7C197–25	7C197–35	7C197–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	150	140	135	95	95	
	Military		160	150	105	105	105
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			7C197−12 Min.	7C197−12 Max.	7C197−15 Min.	7C197−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA	Com'l		0.4		0.4	V
			I_{OL} = 8.0 mA	Mil				0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		Com'l		150		140	mA
				Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} < 0.3V		Com'l		10		10	mA
				Mil				15	

Shaded area contains preliminary information.

Notes:

1. $V_{(min.)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

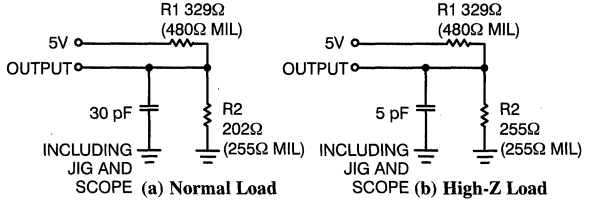
Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions			7C197–20 Min.	7C197–20 Max.	7C197–25, 35, 45 Min.	7C197–25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA	Mil		0.4		0.4	V
			I_{OL} = 12.0 mA	Com'l		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		Com'l		135		95	mA
				Mil		150		105	
I_{SB1}	Automatic $\overline{CE}$ Power Down Current—TTL Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} < 0.3V				15		15	mA

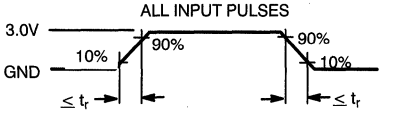
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[7]

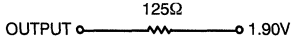


C197–4

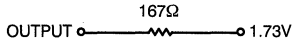


C197–5

Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3, 8]

Parameter	Description	7C197–12		7C197–15		7C197–20		7C197–25		7C197–35		7C197–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		5		7	0	9	0	11	0	15	0	15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		25		30	ns
WRITE CYCLE[11]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		20		30		40		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		20		25		30		ns
t_{SD}	Data Set-Up to Write End	8		9		10		15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	2		2		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7	0	10	0	11	0	15	0	15	ns

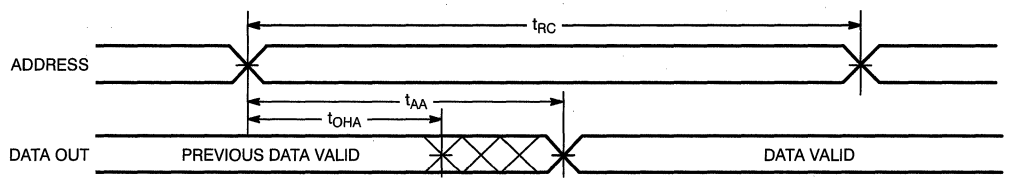
Shaded area contains preliminary information.

Notes:

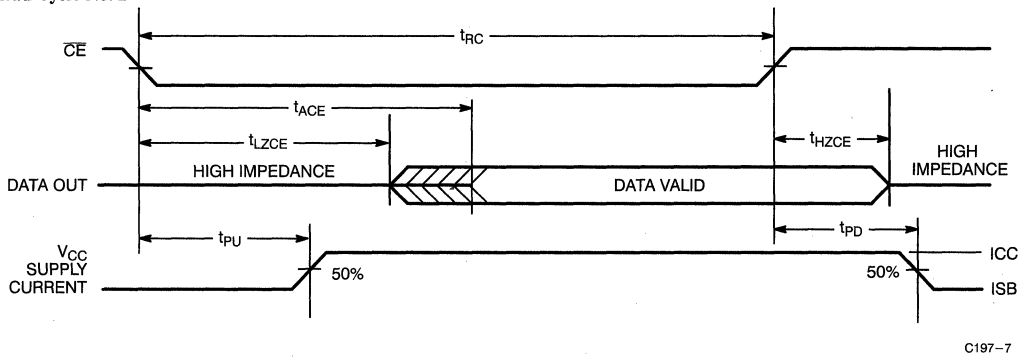
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

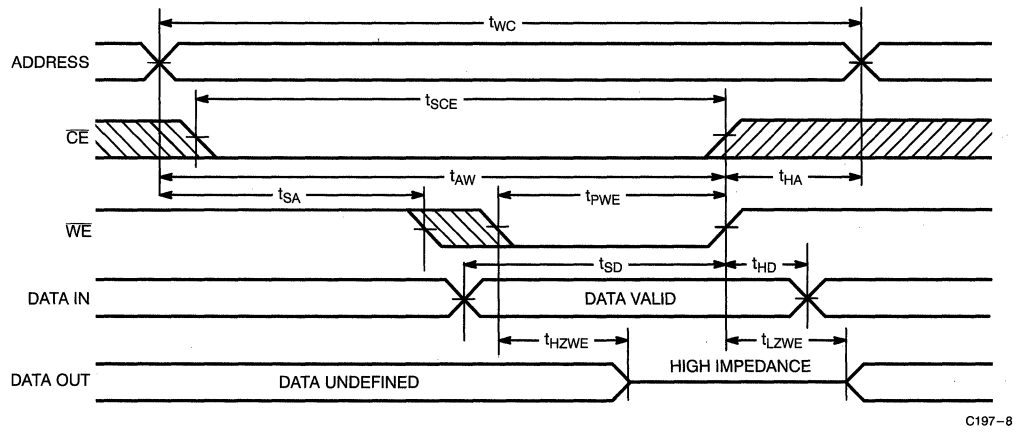
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12]



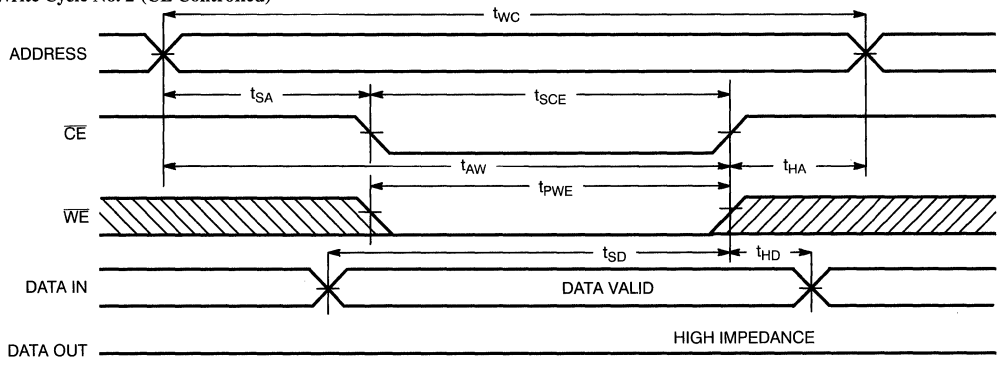
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

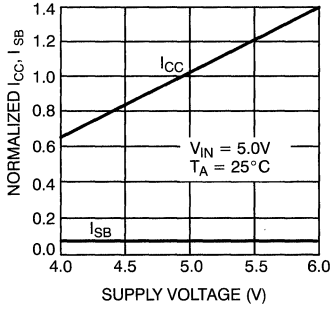
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 14]

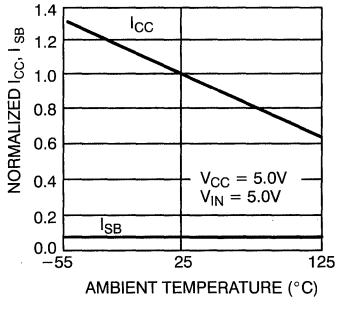


Typical DC and AC Characteristics

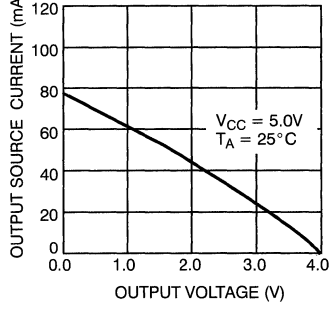
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



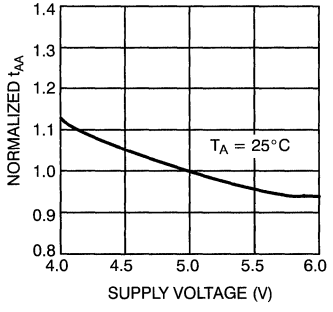
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



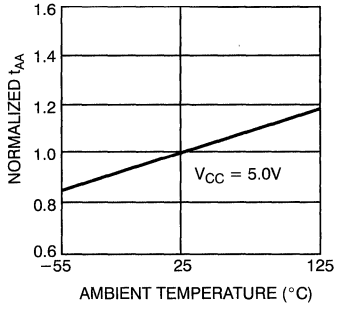
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



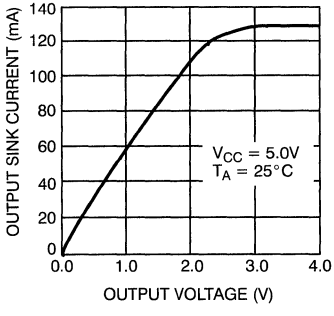
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

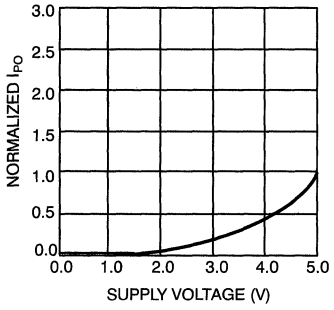


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

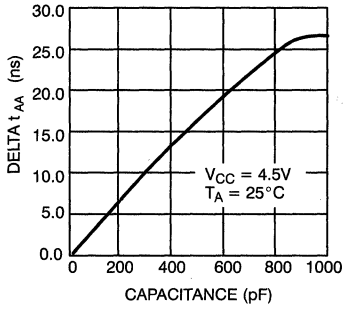


Typical DC and AC Characteristics (continued)

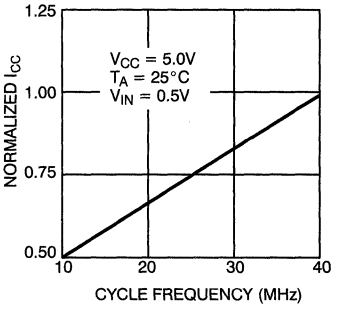
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C197 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C197–12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–12VC	V13	24-Lead Molded SOJ	
15	CY7C197–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–15VC	V13	24-Lead Molded SOJ	
	CY7C197–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7C197–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–20VC	V13	24-Lead Molded SOJ	
	CY7C197–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C197–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–25VC	V13	24-Lead Molded SOJ	
	CY7C197–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–25LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
35	CY7C197–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–35VC	V13	24-Lead Molded SOJ	
	CY7C197–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–35LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
45	CY7C197–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–45LMB	L54	24-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00078-L

CY7C199

32K x 8 Static RAM

Features

- **High speed**
  - **— 12 ns**
- **Fast t_{DOE}**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 880 mW**
- **Low standby power**
  - **— 165 mW**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

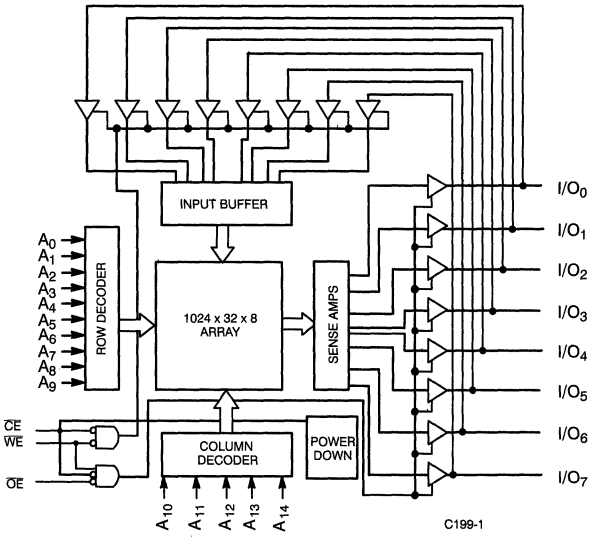
Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

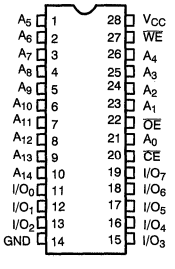
Logic Block Diagram



C199-1

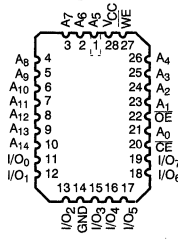
Pin Configurations

DIP/SOJ
Top View



C199-2

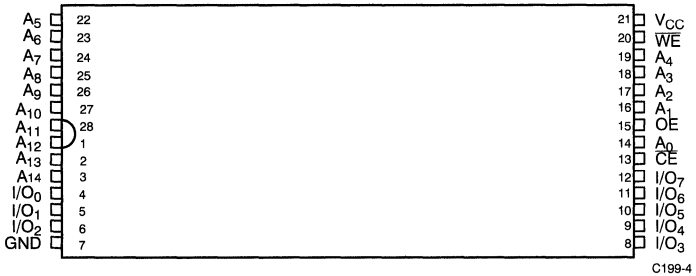
LCC
Top View



C199-3

Pin Configurations (continued)

TSOP
Top View



C199-4

Selection Guide

		7C199–10	7C199–12	7C199–15	7C199–20	7C199–25	7C199–35	7C199–45
Maximum Access Time (ns)		10	12	15	20	25	35	45
Maximum Operating Current (mA)	Com'l	160	160	155	150	150	140	
	L		130	110	100	100	100	100
	Mil			180	170	150	150	150
	L			150	130	130	130	130
Maximum Standby Current (mA)		30	30	30	30	30	25	25
	L		20	20	15	15	15	15

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions	7C199–10		7C199–12		7C199–15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	−5	+5	µA

Shaded area contains preliminary information.

Notes:
1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions		7C199–10 Min.	7C199–10 Max.	7C199–12 Min.	7C199–12 Max.	7C199–15 Min.	7C199–15 Max.	Unit
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Com'l		160		160		155	mA
			L				130		110	
			Mil						180	
			L						150	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$			30		30		30	mA
			L				20		20	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, f = 0	Com'l		10		10		10	mA
			L				500		500	μA
			Mil						15	mA
			L						5	

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range[3] (continued)

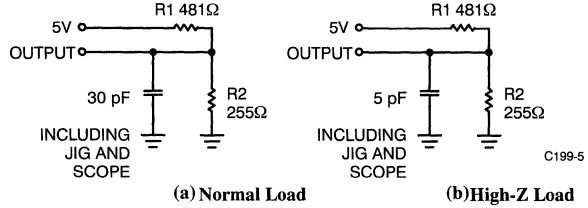
Parameter	Description	Test Conditions		7C199–20 Min.	7C199–20 Max.	7C199–25 Min.	7C199–25 Max.	7C199–35, 45 Min.	7C199–35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC}$, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Com'l		150		150		140	mA
			L		100		100		100	
			Mil		170		150		150	
			L		130		130		130	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$			30		30		25	mA
			L		15		15		15	
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, f=0	Com'l		15		15		15	mA
			L		500		500		500	μA
			Mil		15		15		15	mA
			L		5		5		5	

Note:
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

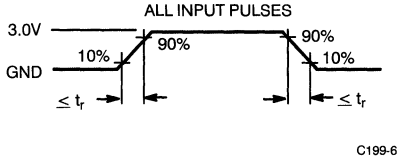
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

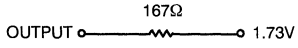
AC Test Loads and Waveforms[6]



(a) Normal Load (b)High-Z Load



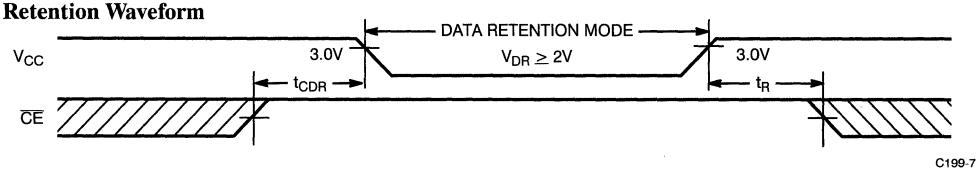
Equivalent to: THÉVENIN EQUIVALENT



Data Retention Characteristics (Over the Operating Range)

Parameter	Description		Conditions[7]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		10	µA
		Mil			100	
t_{CDR}[5]	Chip Deselect to Data Retention Time			0		ns
t_R[5]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform



Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. $t_r \leq 3$ ns for the −12 and −15 speeds. $t_r \leq 5$ ns for the −20 and slower speeds.
7. No input may exceed V_{CC} +0.5V.

Switching Characteristics Over the Operating Range[3, 8]

Parameter	Description	7C199–10		7C199–12		7C199–15		7C199–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		7		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		5		5		7		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		5		5		7		9	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[11, 12]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		9		10		15		ns
t_{AW}	Address Set-Up to Write End	7		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		9		15		ns
t_{SD}	Data Set-Up to Write End	5		8		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		5		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		3		3		ns

Shaded area contains preliminary information.

Notes:

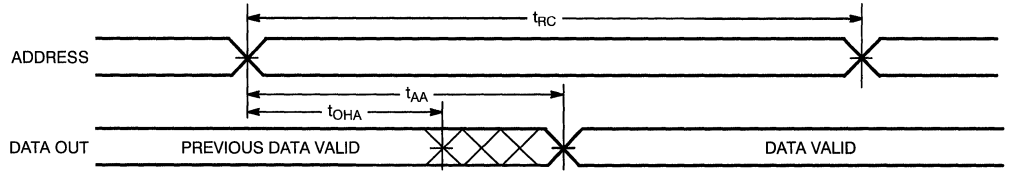
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range[3, 8] (continued)

Parameter	Description	7C199–25		7C199–35		7C199–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		11		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
WRITE CYCLE[11, 12]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	18		22		22		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		22		22		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		11		15		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		3		ns

Switching Waveforms

Read Cycle No. 1[13, 14]

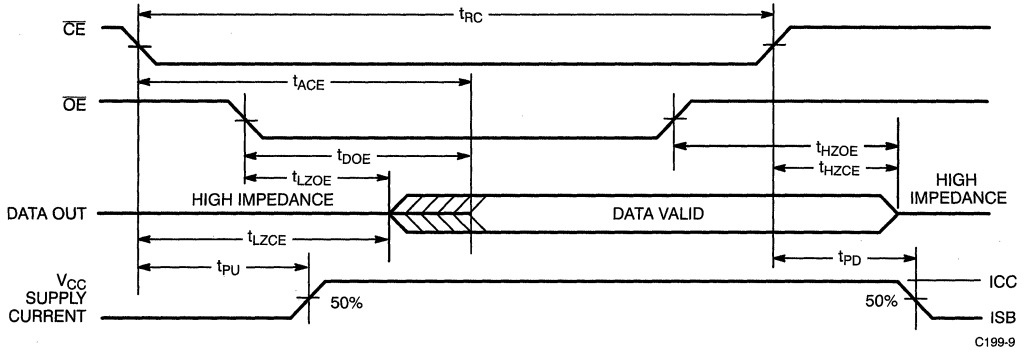


C199-8

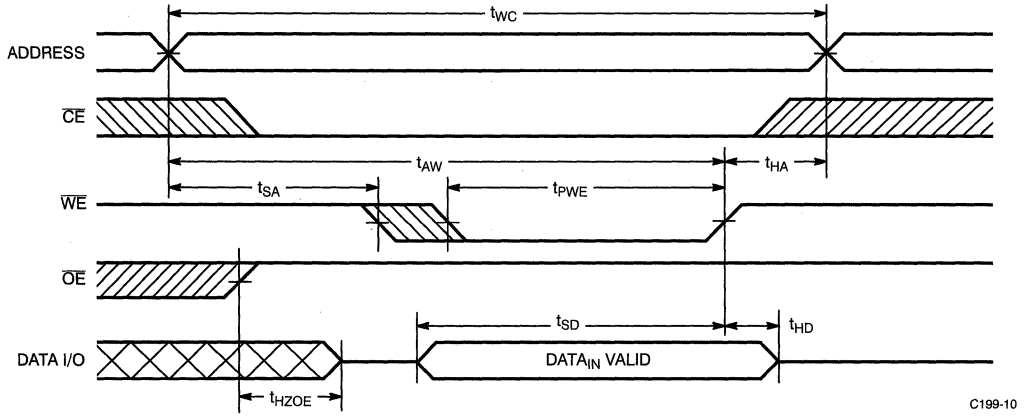
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

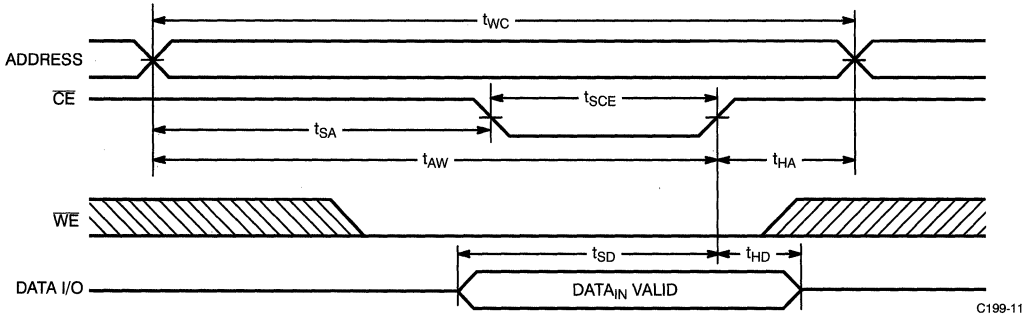
Read Cycle No. 2[14, 15]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[11, 16, 17]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 16, 17]

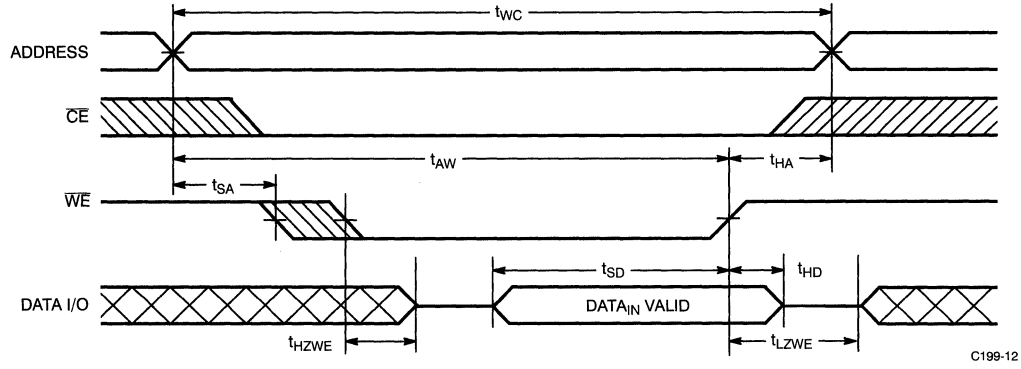


Notes:

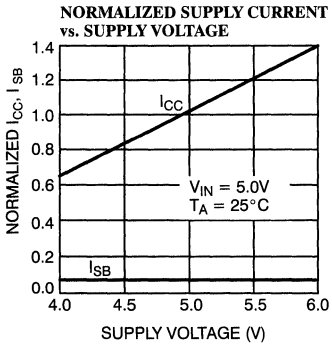
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

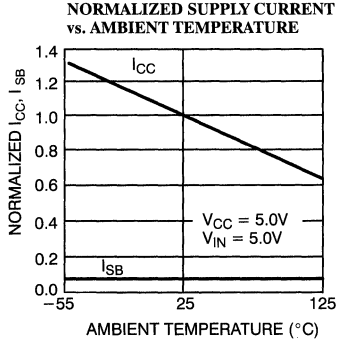
Switching Waveforms (continued)

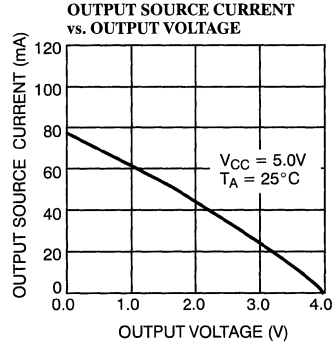
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[12, 17]

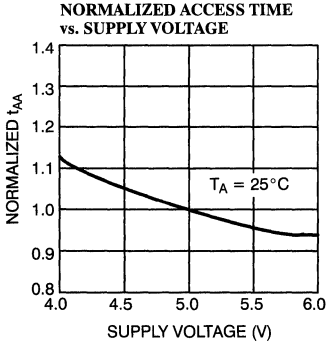


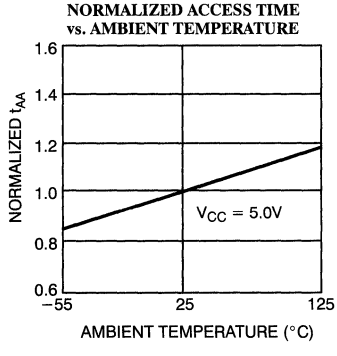
Typical DC and AC Characteristics

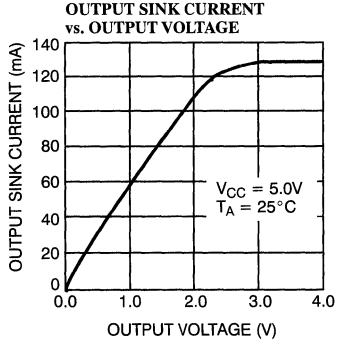






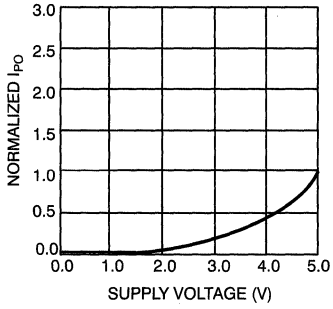




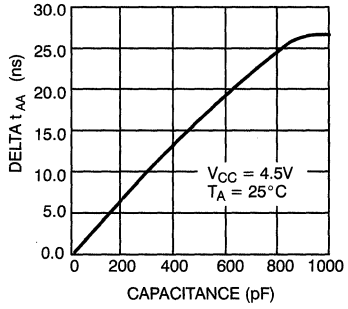


Typical DC and AC Characteristics (continued)

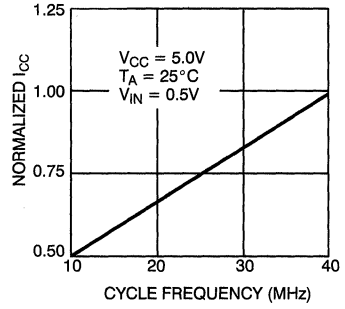
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-12VC	V21	28-Lead Molded SOJ	
	CY7C199L-12VC	V21	28-Lead Molded SOJ	
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-15VC	V21	28-Lead Molded SOJ	
	CY7C199L-15VC	V21	28-Lead Molded SOJ	
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-20VC	V21	28-Lead Molded SOJ	
	CY7C199L-20VC	V21	28-Lead Molded SOJ	
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C199–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L–20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199–25VC	V21	28-Lead Molded SOJ	
	CY7C199L–25VC	V21	28-Lead Molded SOJ	
	CY7C199–25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L–25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L–25DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L–35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199–35VC	V21	28-Lead Molded SOJ	
	CY7C199L–35VC	V21	28-Lead Molded SOJ	
	CY7C199–35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L–35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L–35DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L–45DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38−00239−B

CY7C1001
CY7C1002

256K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Transparent write (7C1001)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 910 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention (optional)**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1001 and CY7C1002 are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

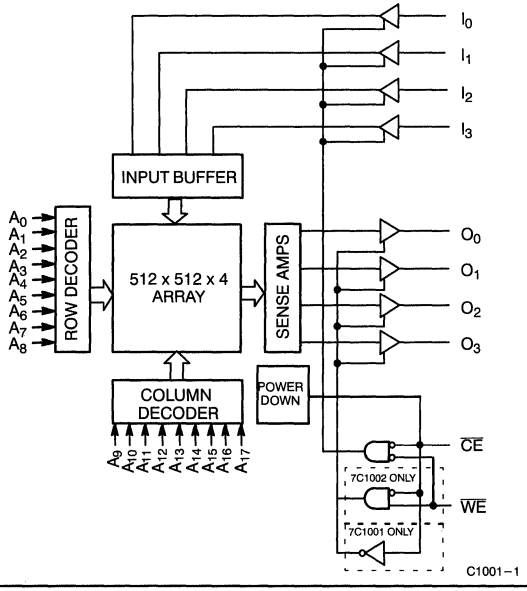
Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

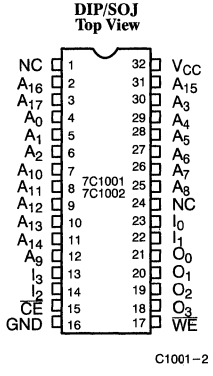
The data output pins on the CY7C1001 and the CY7C1002 are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C1002's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C1001, the output pins will carry the same data as the inputs after a specified delay.

The CY7C1001 and CY7C1002 are available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1001–12 7C1002–12	7C1001–15 7C1002–15	7C1001–20 7C1002–20	7C1001–25 7C1002–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	165	155	140	130
	Military		165	150	140
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1001−12 7C1002−12 Min.	7C1001−12 7C1002−12 Max.	7C1001−15 7C1002−15 Min.	7C1001−15 7C1002−15 Max.	7C1001−20 7C1002−20 Min.	7C1001−20 7C1002−20 Max.	7C1001−25 7C1002−25 Min.	7C1001−25 7C1002−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140		130	mA
			Mil				165		150		140	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

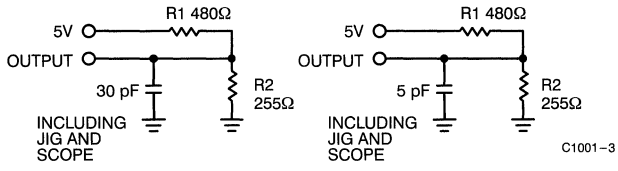
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

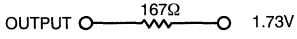
1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



(a) Normal Load **(b) High-Z Load**

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C1001-12 7C1002-12 Min.	7C1001-12 7C1002-12 Max.	7C1001-15 7C1002-15 Min.	7C1001-15 7C1002-15 Max.	7C1001-20 7C1002-20 Min.	7C1001-20 7C1002-20 Max.	7C1001-25 7C1002-25 Min.	7C1001-25 7C1002-25 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C1001)		12		15		20		25	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C1001)		12		15		20		25	ns
t_{ADV}	Data Valid to Output Valid (7C1001)		12		15		20		25	ns

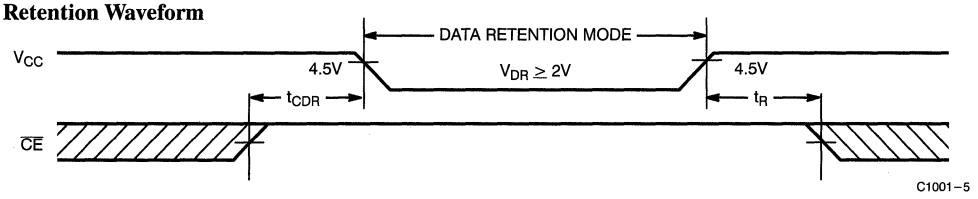
Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L Version Only)

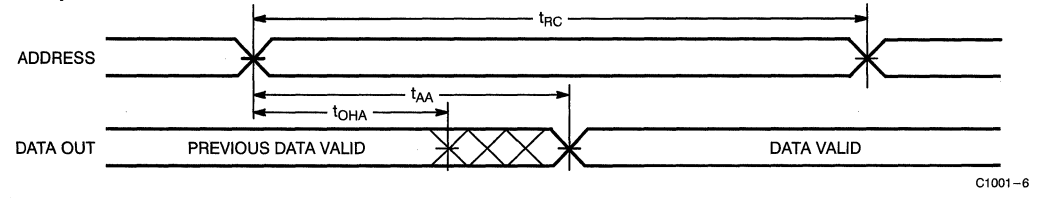
Parameters	Description	Conditions[10]	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform

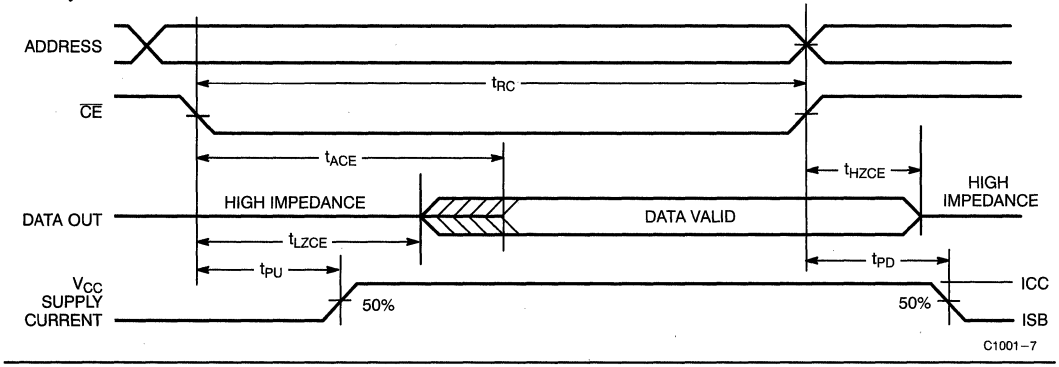


Switching Waveforms

Read Cycle No. 1[11, 12]



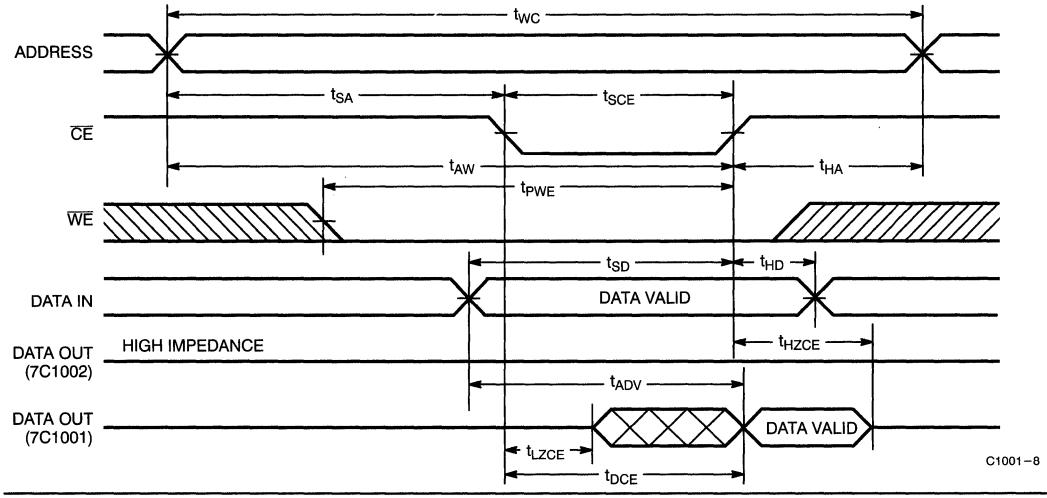
Read Cycle No. 2[12, 13]



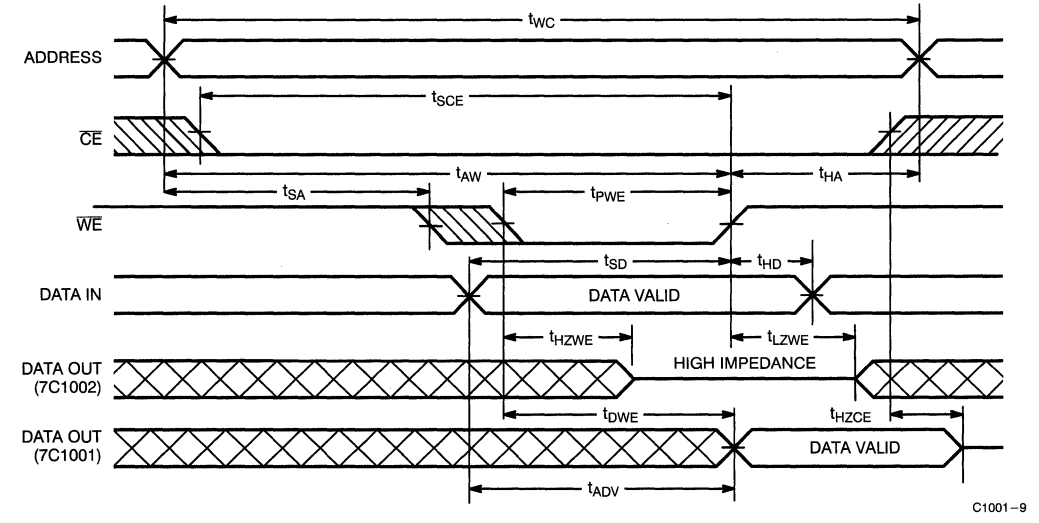
Notes:
10. No input may exceed V_{CC} + 0.5V.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[9, 14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[9]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C1002 only).

Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C1002: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C1001: Transparent Write[15]	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1001-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1001-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1001-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1001-25DC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1002-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1002-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1002-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1002-25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

Note:
15. Outputs track inputs after specified delay.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}[16]	7, 8, 9, 10, 11

Note:
16. 7C1001 only.

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256K x 4 Static RAM

Features

- **High speed**
  - **t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **910 mW**
- **Low standby power**
  - **275 mW**
- **2.0V data retention (optional)**
  - **100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1006 is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

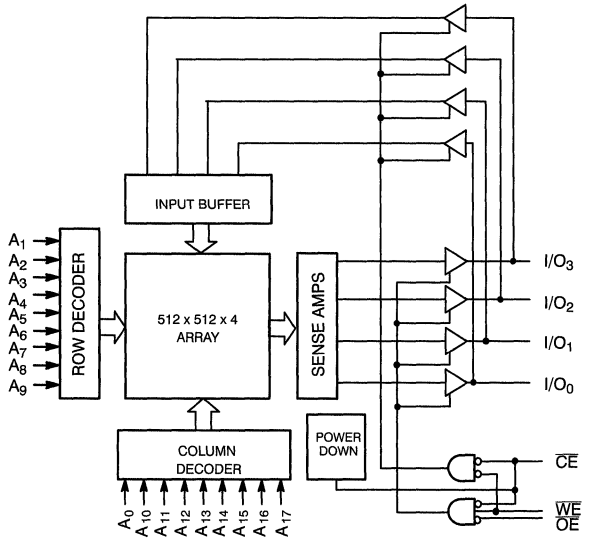
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

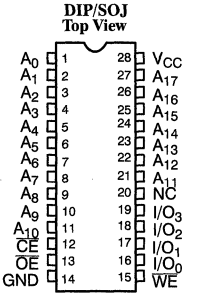
The CY7C1006 is available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



C1006–1

Pin Configuration



C1006–2

Selection Guide

		7C1006–12	7C1006–15	7C1006–20	7C1006–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	165	155	140	130
	Military		165	150	140
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1006−12		7C1006−15		7C1006−20		7C1006−25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140		130	mA
			Mil				165		150		140	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

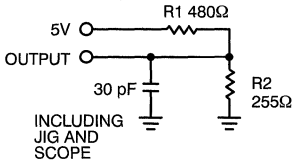
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

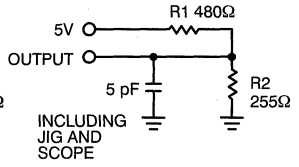
Notes:

1. V_{IL} (min.) = − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

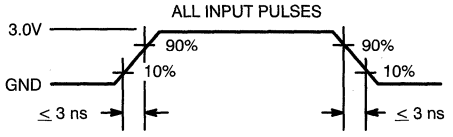


(a) Normal Load



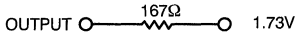
(b) High-Z Load

C1006-3



C1006-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C1006-12		7C1006-15		7C1006-20		7C1006-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE[9, 10]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns

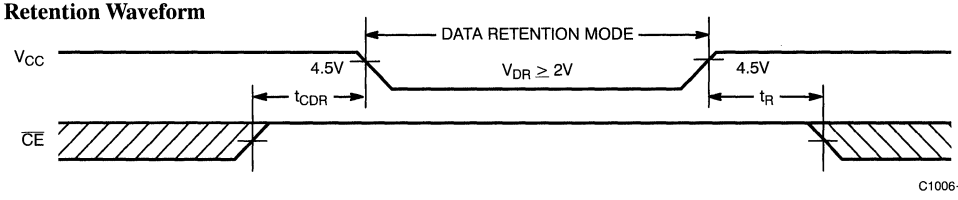
Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (L Version Only)

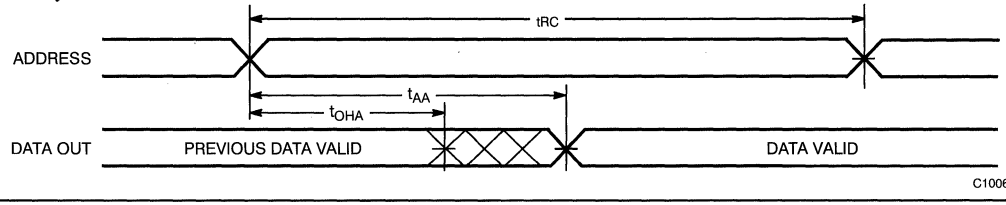
Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform

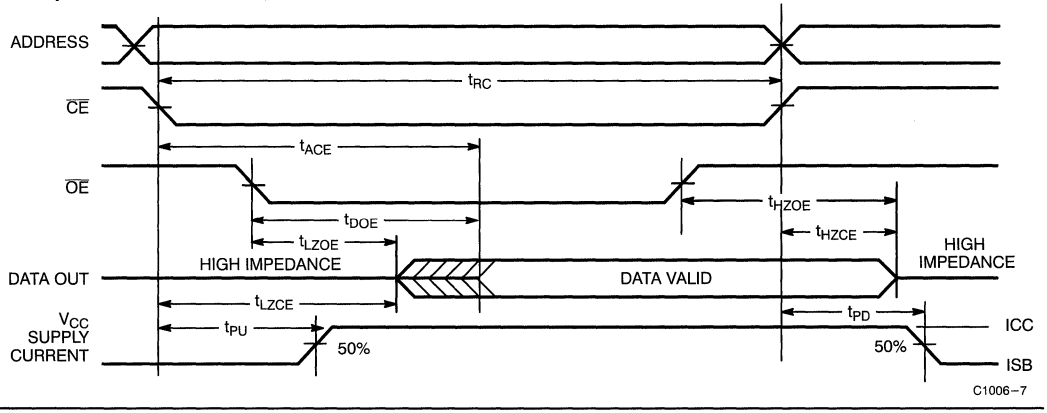


Switching Waveforms

Read Cycle No. 1[12, 13]



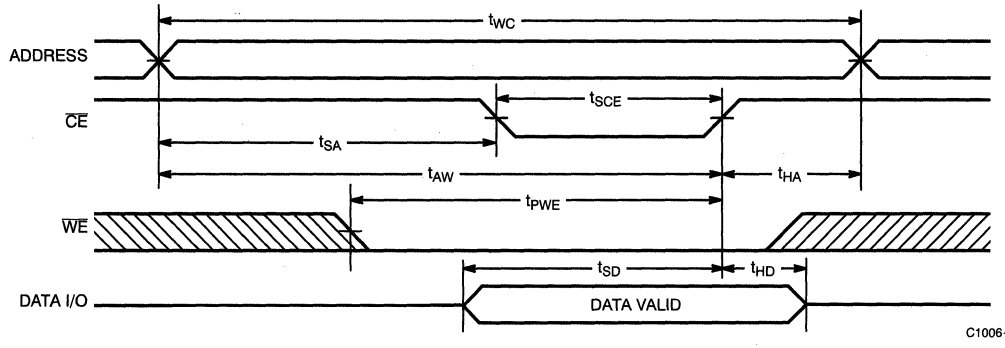
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



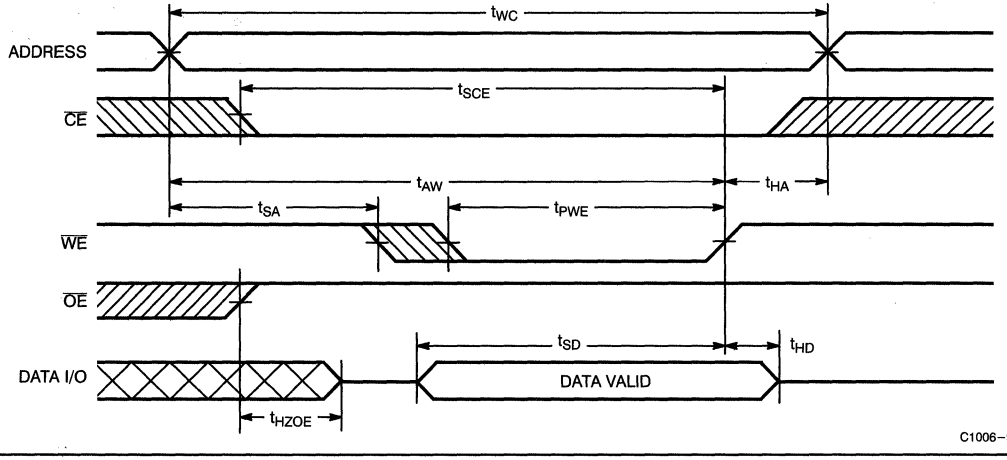
Notes:
11. No input may exceed V_{CC} + 0.5V.
12. Device is continuously selected, $\overline{OE}$ and $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]

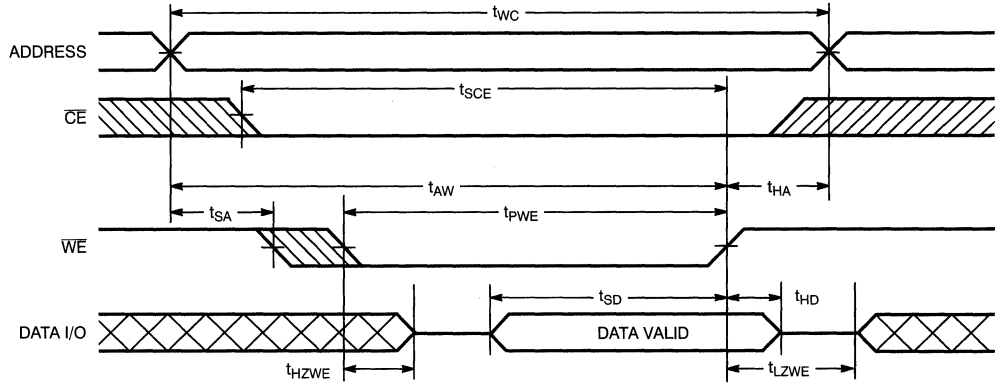


Notes:

15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1006–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–12VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C1006–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1006–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C1006–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1006–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C1006–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1006–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1006–25DMB	D22	28-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00201–B

1M x 1 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 825 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention (optional)**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1007 is a high-performance CMOS static RAM organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

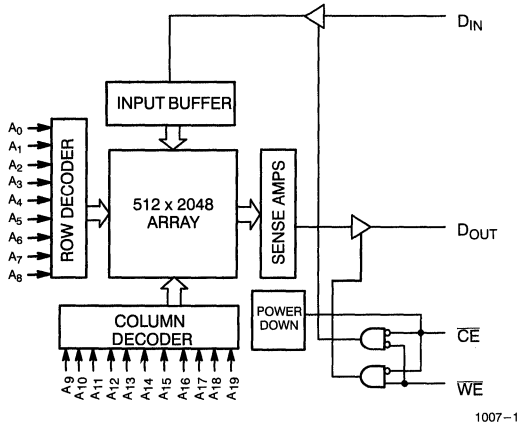
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C1007 is available in standard 300-mil-wide DIPs and SOJs.

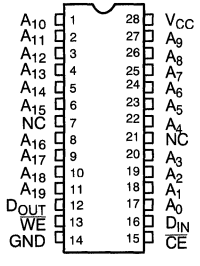
Logic Block Diagram



1007–1

Pin Configuration

DIP/SOJ
Top View



1007–2

Selection Guide

		7C1007–12	7C1007–15	7C1007–20	7C1007–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	150	135	125	120
	Military		145	135	130
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1007−12 Min.	7C1007−12 Max.	7C1007−15 Min.	7C1007−15 Max.	7C1007−20 Min.	7C1007−20 Max.	7C1007−25 Min.	7C1007−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		135		125		120	mA
			Mil				145		135		130	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current − TTL Inputs	Max.. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current − CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

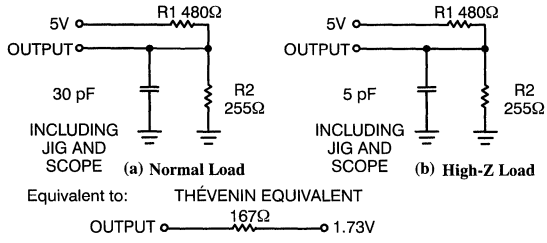
Capacitance[5]

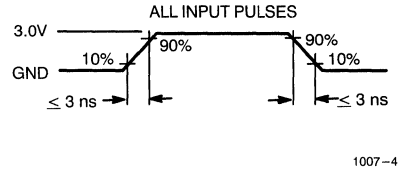
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics[3, 6] Over the Operating Range

Parameter	Description	7C1007–12		7C1007–15		7C1007–20		7C1007–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns

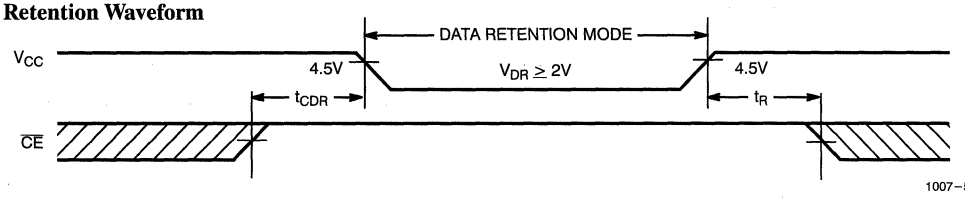
Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L Version Only)

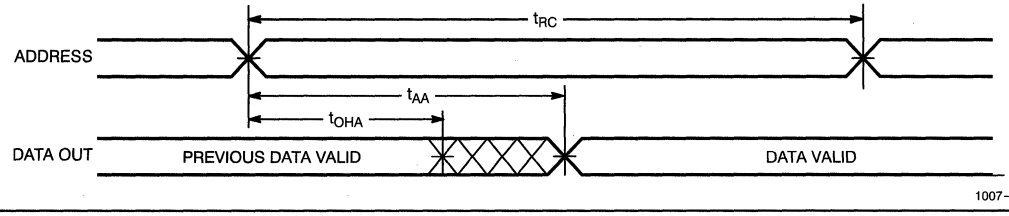
Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform

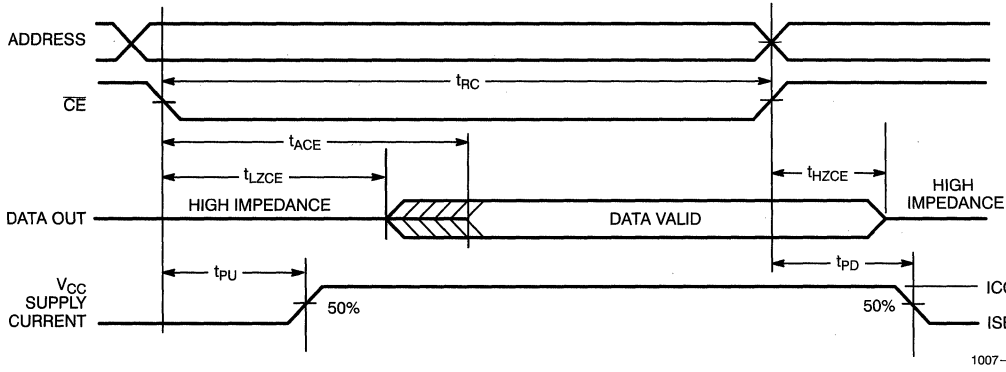


Switching Waveforms

Read Cycle No. 1[11, 12]



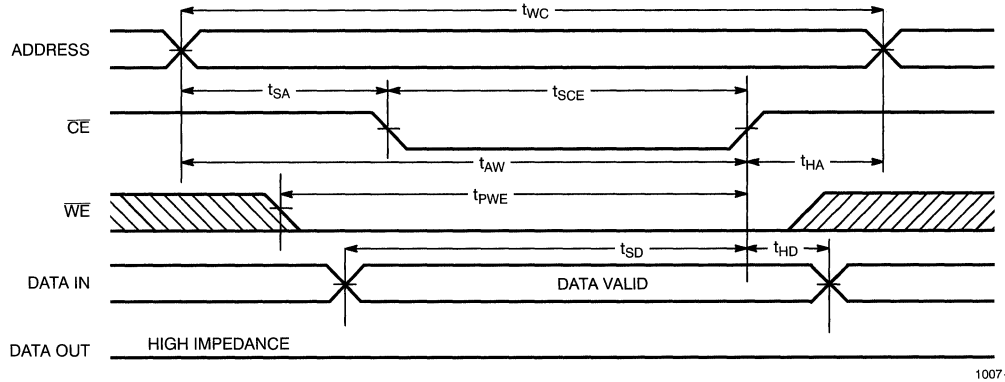
Read Cycle No. 2[12, 13]



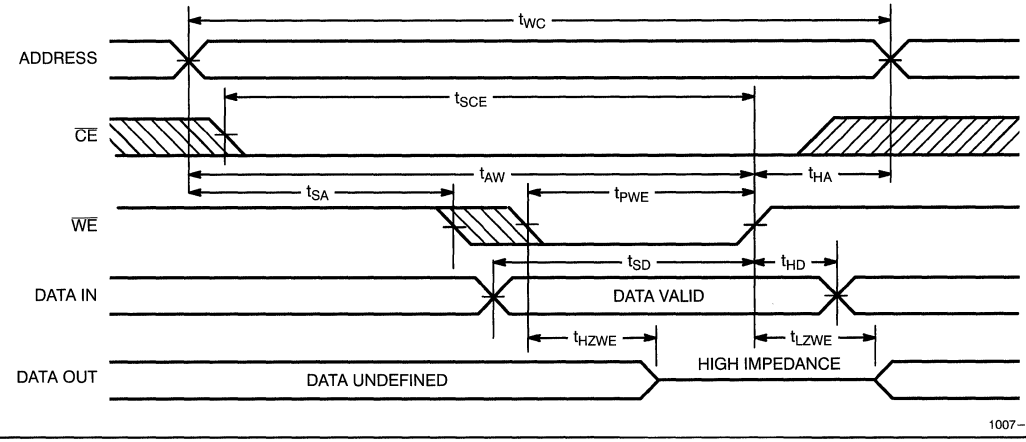
Notes:
10. No input may exceed V_{CC} + 0.5V.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[14]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	D_{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1007–12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–12VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C1007–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1007–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C1007–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1007–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C1007–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1007–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C1007–25DMB	D22	28-Lead (300-Mil) CerDIP	Military

Contact factory for "L' version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Low standby power**
  - **— 250 mW**
- **2.0V data retention (optional)**
  - **— 100 µW**
- **Available in 450 x 550-mil LCC**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C1009 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

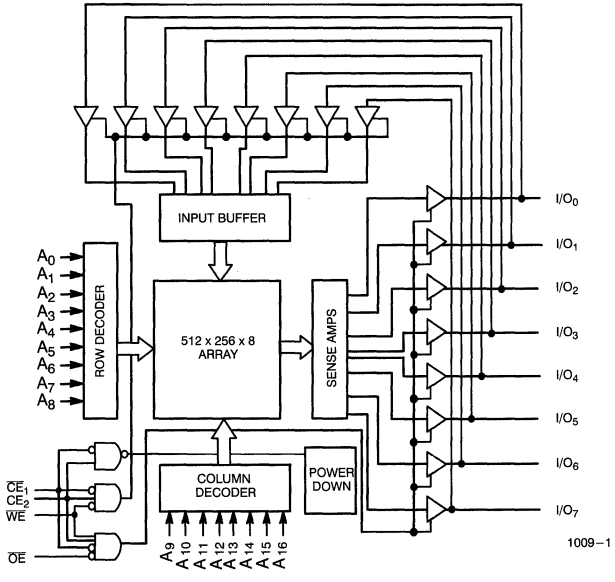
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

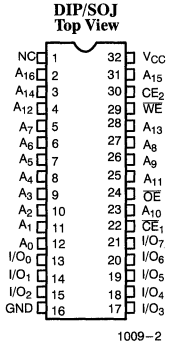
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

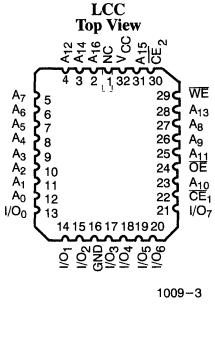
The CY7C1009 is available in standard 300-mil-wide DIPs, SOJs and a small footprint 450 x 550-mil leadless chip carrier.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C1009–12	7C1009–15	7C1009–20	7C1009–25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	185	170	155	145
	Military		180	170	160
Maximum Standby Current (mA)	Commercial	45	40	30	30
	Military		40	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .. −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C1009−12 Min.	7C1009−12 Max.	7C1009−15 Min.	7C1009−15 Max.	7C1009−20 Min.	7C1009−20 Max.	7C1009−25 Min.	7C1009−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		185		170		155		145	mA
			Mil				180		170		160	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		45		40		30		30	mA
			Mil				40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ − 0.3V, or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V, or $V_{IN} \leq$ 0.3V, f=0	Com'l		2		2		2		2	mA
			Mil				2		2		2	

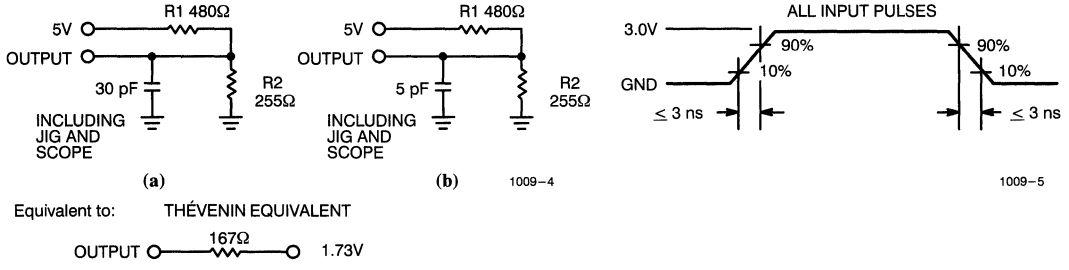
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Address	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C1009–12		7C1009–15		7C1009–20		7C1009–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address to Data Valid		12		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		12		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		12		15		20		25	ns
WRITE CYCLE[9, 10]										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10	ns

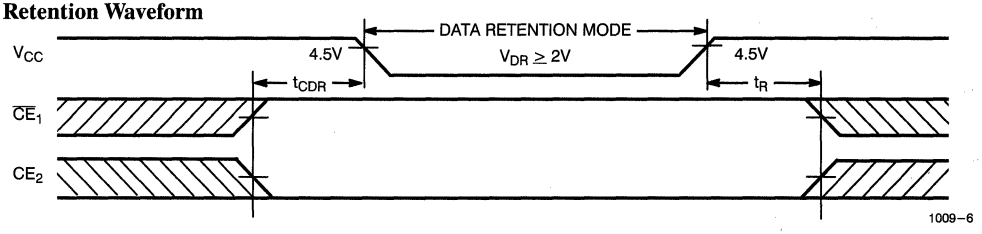
Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (L Version Only)

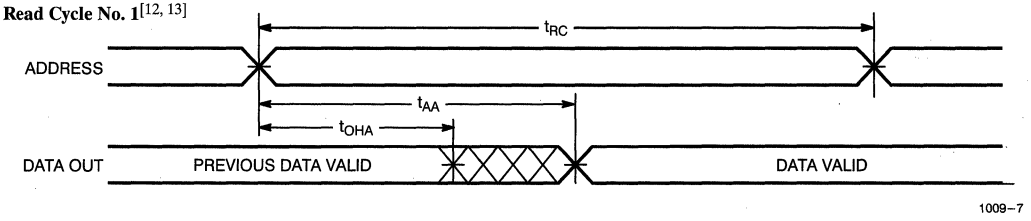
Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform

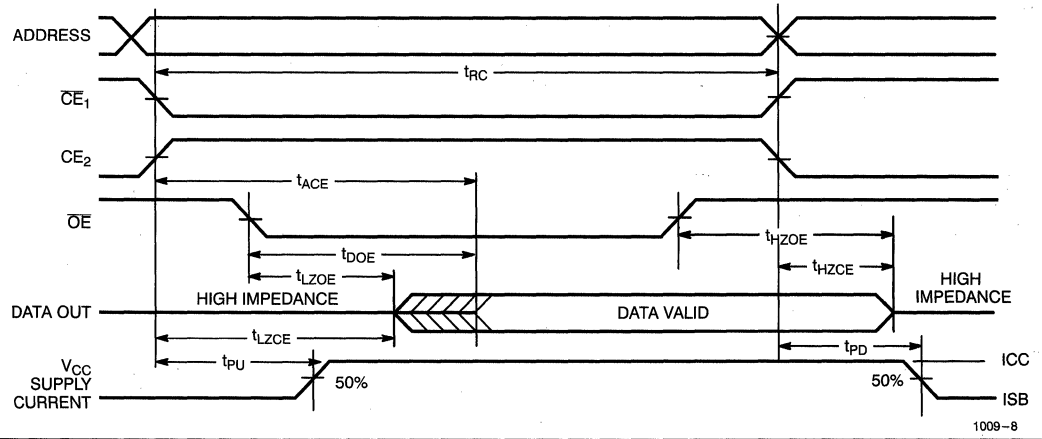


Switching Waveforms

Read Cycle No. 1[12, 13]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]

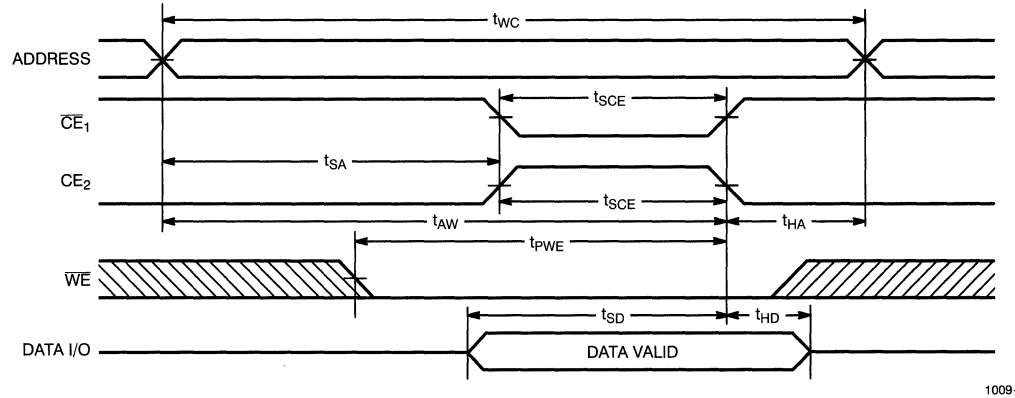


Notes:

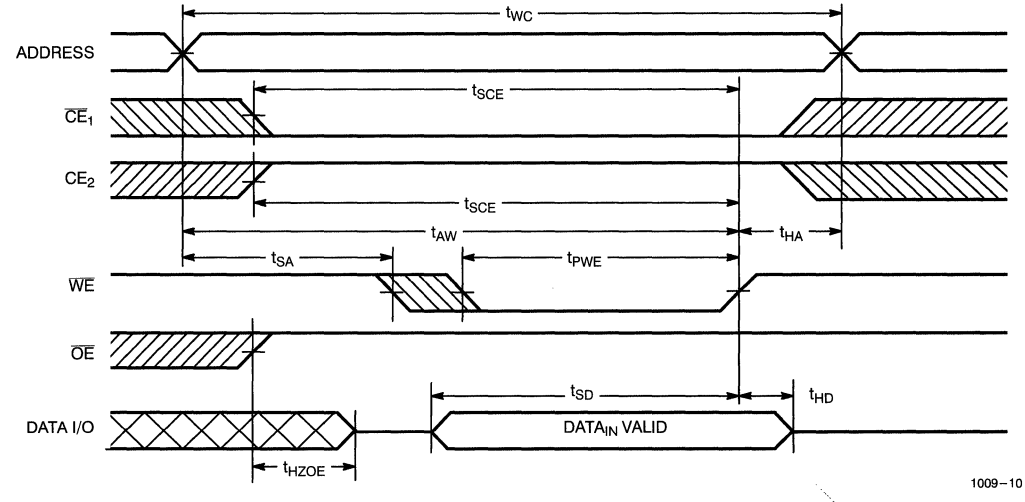
11. No input may exceed V_{CC} + 0.5V.
12. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[15, 16]



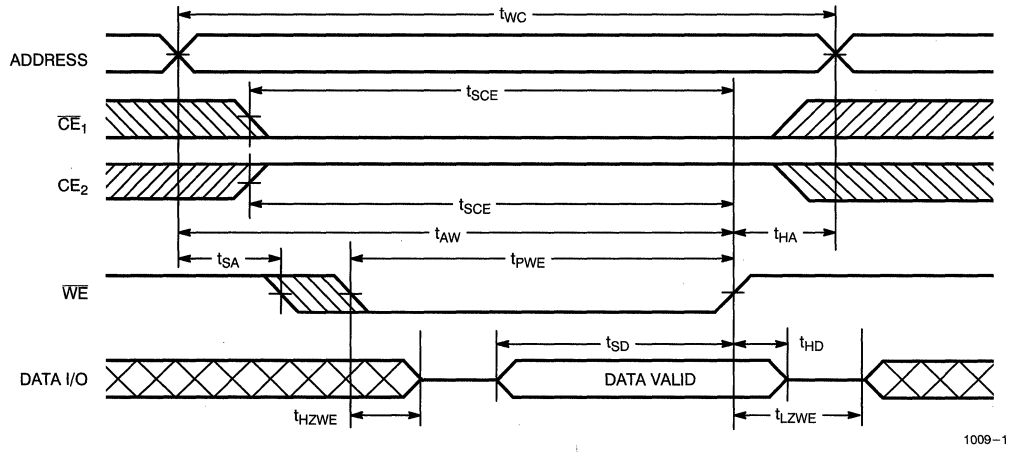
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]



Notes:
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1009–12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1009–15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–15DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C1009–20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C1009–25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–25DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00199–B

256K x 4 Static RAM

Features

- **High speed**
  - **t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1014 is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and three-state drivers. The device has an automatic power-down feature that significantly reduces power consumption when deselected.

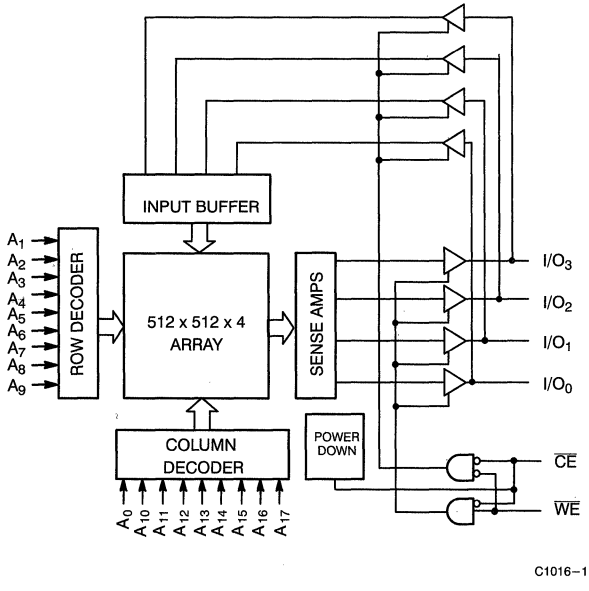
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

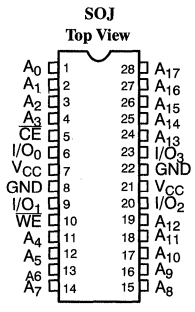
The CY7C1014 is available in standard 400-mil-wide SOJs.

Logic Block Diagram



C1016–1

Pin Configuration



C1016–2

Selection Guide

		7C1014–10	7C1014–12	7C1014–15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	175	165	155
	Military		175	165
Maximum Standby Current (mA)	Commercial	55	50	40
	Military		50	40

Document #: 38–00454

256K x 4 Static RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **Output enable ($\overline{OE}$) feature**
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1016 is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that significantly reduces power consumption when deselected.

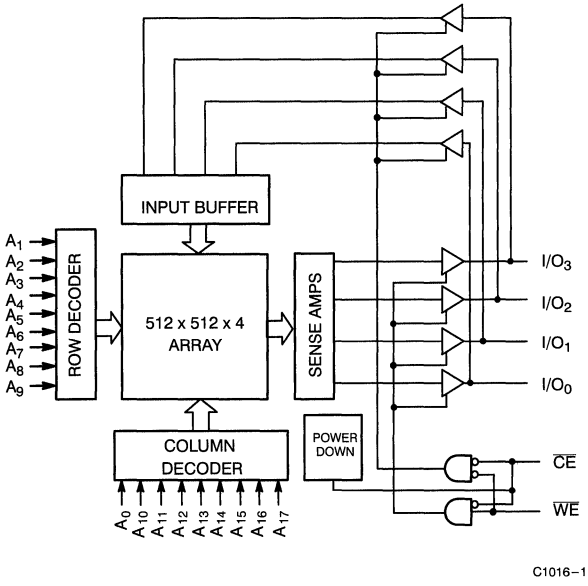
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C1016 is available in standard 400-mil-wide SOJs.

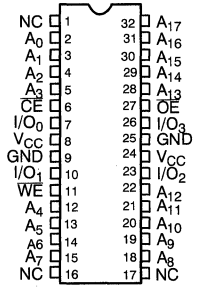
Logic Block Diagram



C1016–1

Pin Configuration

SOJ
Top View



C1016–2

Selection Guide

		7C1016–10	7C1016–12	7C1016–15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	175	165	155
	Military		175	165
Maximum Standby Current (mA)	Commercial	55	50	40
	Military		50	40

Document #: 38–00439

CYPRESS *ADVANCED INFORMATION* **CY7C1019**

128K x 8 Static RAM

Features

- **High speed**
  — t_{AA} = 10 ns
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options**

Functional Description

The CY7C1019 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption significantly when deselected.

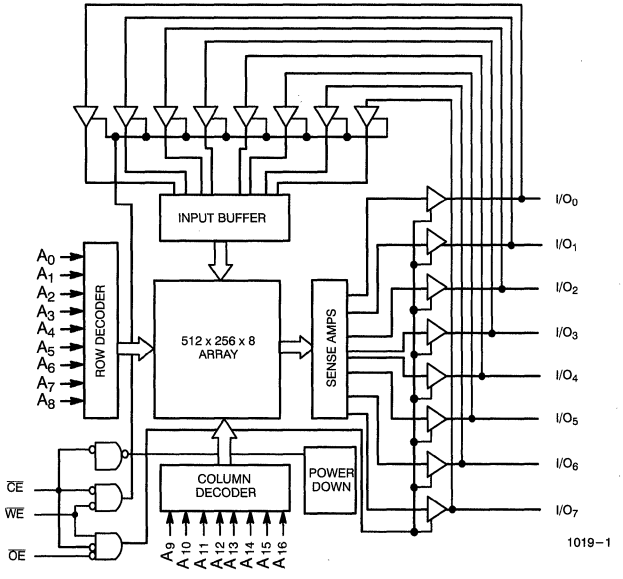
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

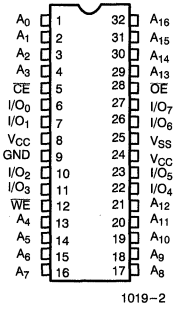
The CY7C1019 is available in standard 400-mil-wide SOJs.

Logic Block Diagram



Pin Configurations

SOJ
Top View



Selection Guide

		7C1019–10	7C1019–12	7C1019–15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	195	185	170
	Military		195	180
Maximum Standby Current (mA)	Commercial	50	45	40
	Military		50	40

Document #: 38–00440

CY7C1021

64K x 16 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Available in 450 x 550-mil LCC**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C1021 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

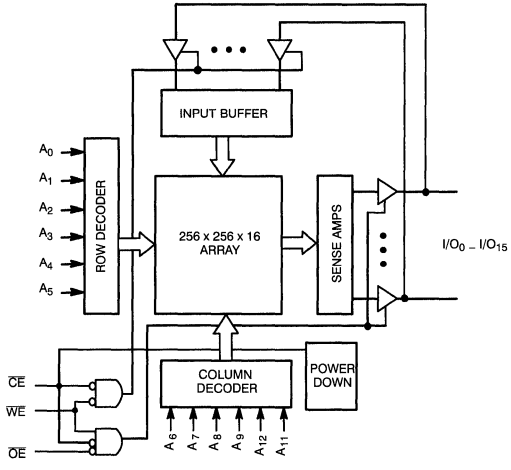
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and byte write enable ($\overline{BHE}$/$\overline{BLE}$) inputs LOW. Data on the appropiate eight I/O pins (I/O_0 through I/O_7 and/or I/O_8 through I/O_{15}) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enables ($\overline{BHE}$ and/or $\overline{BLE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the appropiate I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021 is available in standard 400-mil-wide DIPs and SOJs.

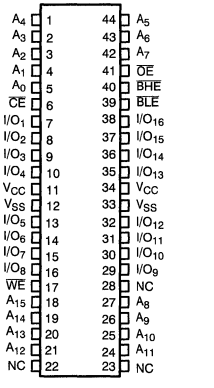
Logic Block Diagram



1021–1

Pin Configurations

DIP/SOJ
Top View



1021–2

Selection Guide

		7C1021–12	7C1021–15	7C1021–20
Maximum Access Time (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	195	180	165
	Military		195	180

Document #: 38–00224

CY7C1031
CY7C1032

64K x 18 Synchronous Cache RAM

Features

- **Supports 66-MHz Pentium™ microprocessor cache systems with zero wait states**
- **64K by 18 common I/O**
- **Fast clock-to-output times**
  - **8.5 ns**
- **Two-bit wraparound counter supporting Pentium microprocessor and 486 burst sequence (CY7C1031)**
- **Two-bit wraparound counter supporting linear burst sequence (CY7C1032)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **I/Os capable of 3.3V operation**
- **JEDEC-standard pinout**
- **52-pin PLCC and PQFP packaging**

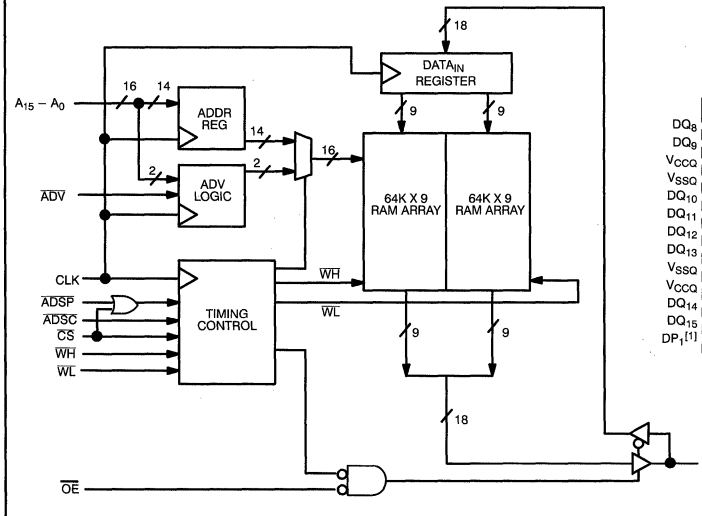
Functional Description

The CY7C1031 and CY7C1032 are 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

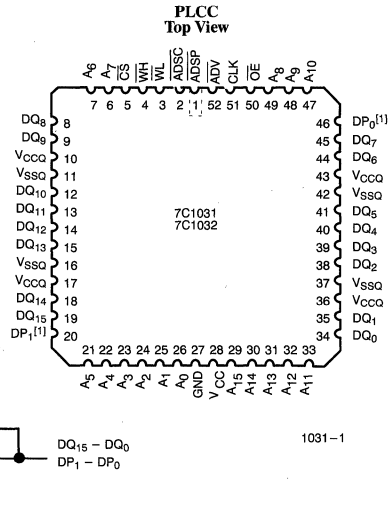
The CY7C1031 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1032 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1031–7 7C1032–7	7C1031–8 7C1032–8	7C1031–10 7C1032–10	7C1031–12 7C1032–12
Maximum Access Time (ns)		7	8.5	10	12
Maximum Operating Current (mA)	Commercial	300	280	280	230
	Military				235

Shaded area contains preliminary information.
Pentium is a trademark of Intel Corporation.

Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_x.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1031 and CY7C1032 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C1031 and CY7C1032 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. Since the CY7C1031 and the CY7C1032 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data and parity lines. As a safety precaution, the appropriate data and parity lines are three-stated in the cycle where $\overline{WH}$ and $\overline{WL}$ are sampled LOW regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

Burst Sequences

The CY7C1031 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor's address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C1032 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 512-Kbyte secondary cache for the Pentium microprocessor using four CY7C1031 cache RAMs.

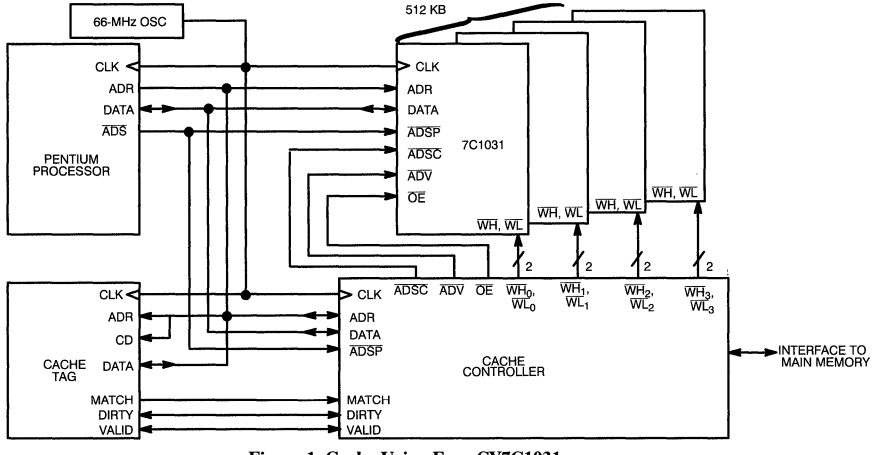


Figure 1. Cache Using Four CY7C1031s

Pin Definitions

Signal Name	Type	# of Pins	Description
V_{CC}	Input	1	+5V Power
V_{CCQ}	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
V_{SSQ}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{15} - A_0$	Input	16	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CS}$, $\overline{WH}$, $\overline{WL}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A_{15}–A_0	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C1032, the address will be incremented linearly. In the CY7C1031, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ_{15}–DQ_0	I/O	Sixteen bidirectional data I/O lines. DQ_{15} – DQ_8 are inputs to and outputs from the high-order half of the RAM array, while DQ_7 – DQ_0 are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. DQ_{15} – DQ_8 and DQ_7 – DQ_0 are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, is sampled LOW at clock rise.
DP_1–DP_0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as DQ_{15} – DQ_0, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}	V_{CCQ}
Com'l	0°C to +70°C	5V ± 5%	3.0V to V_{CC}
Mil	−55°C to +125°C	5V ± 5%	5V ± 5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	7C1031−7 7C1032−7		7C1031−8 7C1032−8		7C1031−10 7C1032−10		7C1031−12 7C1032−12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH}=−4.0 mA	2.4	V_{CCQ}	2.4	V_{CCQ}	2.4	V_{CCQ}	2.4	V_{CCQ}	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL}=8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}	−1	1	−1	1	−1	1	−1	1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	5	−5	5	−5	5	−5	5	µA

Shaded area contains preliminary information.

Notes:

2. Minimum voltage equals −2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page for Group A subgroup testing information.

Electrical Characteristics (continued)

Parameter	Description	Test Conditions		7C1031–7 7C1032–7 Min.	7C1031–7 7C1032–7 Max.	7C1031–8 7C1032–8 Min.	7C1031–8 7C1032–8 Max.	7C1031–10 7C1032–10 Min.	7C1031–10 7C1032–10 Max.	7C1031–12 7C1032–12 Min.	7C1031–12 7C1032–12 Max.	Unit
I_{OS}	Output Short Circuit Current[5]	V_{CC}=Max., V_{OUT}=GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX} =1/t_{CYC}	Com'l		300		280		280		230	mA
			Mil								250	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		90		80		80		60	mA
			Mil								70	
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f=0[6]	Com'l		30		30		30		30	mA
			Mil								50	

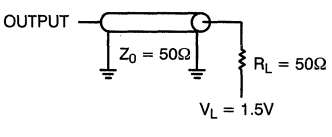
Shaded areas contain peliminary information

Capacitance[7]

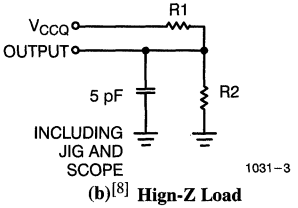
Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	Com'l	4.5	pF
			Mil	6	
C_{IN}: Other Inputs			Com'l	5	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	8	pF
			Mil	10	

Shaded areas contain advanced information

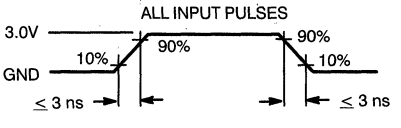
AC Test Loads and Waveforms



(a) Normal Load



(b)[8] Hign-Z Load



Notes:

5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Inputs are disabled, clock is allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Resistor values for V_{CCQ}=5V are: R1=1179Ω and R2=868Ω. Resistor values for V_{CCQ}=3.3V are R1=317Ω and R2=348Ω.

Switching Characteristics Over the Operating Range[9]

Parameter	Description	7C1031–7 7C1032–7		7C1031–8 7C1032–8		7C1031–10 7C1032–10		7C1031–12 7C1032–12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	13.3		15		15		20		ns
t_{CH}	Clock HIGH	5		5		6		8		ns
t_{CL}	Clock LOW	5		5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		7		8.5		10		12	ns
t_{DOH}	Data Output Hold After CLK Rise	2		3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		2.5		2.5		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2.5		2.5		2.5		2.5		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		2.5		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		2.5		2.5		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[10]	2	6	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[10]	2	6	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		5		6	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[10,11]		5		5		6		7	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[11]		7		8.5		10		12	ns

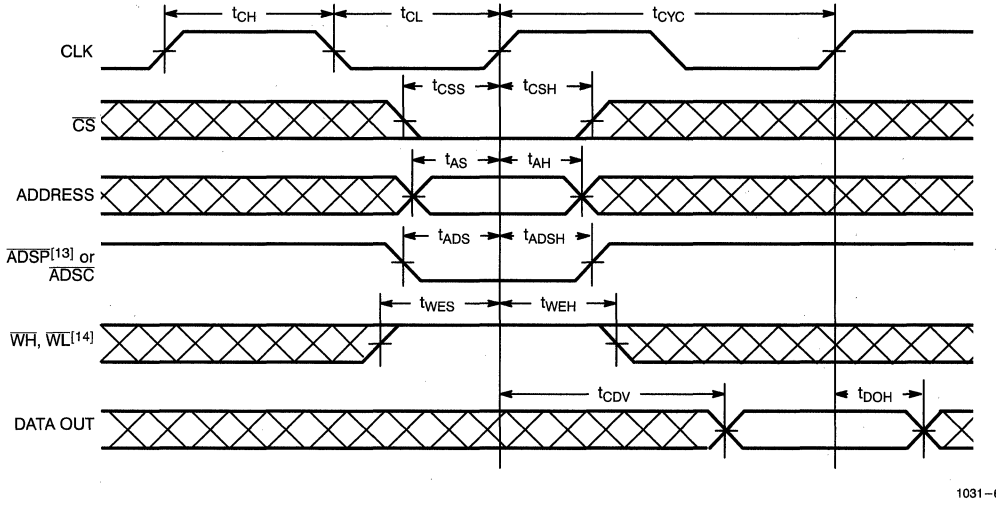
Shaded areas contain preliminary information

Notes:

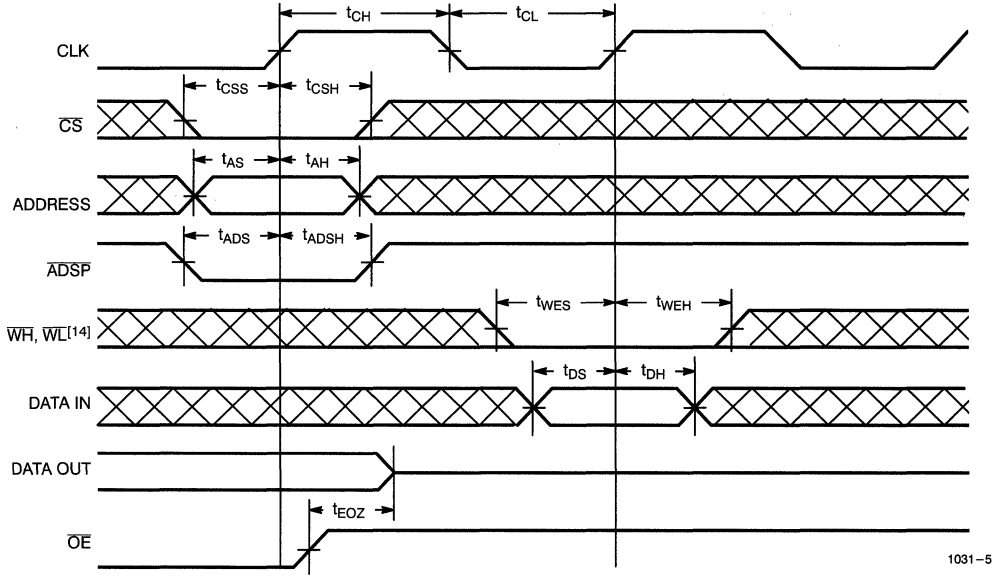
9. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) os AC test loads.
10. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
11. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[12]



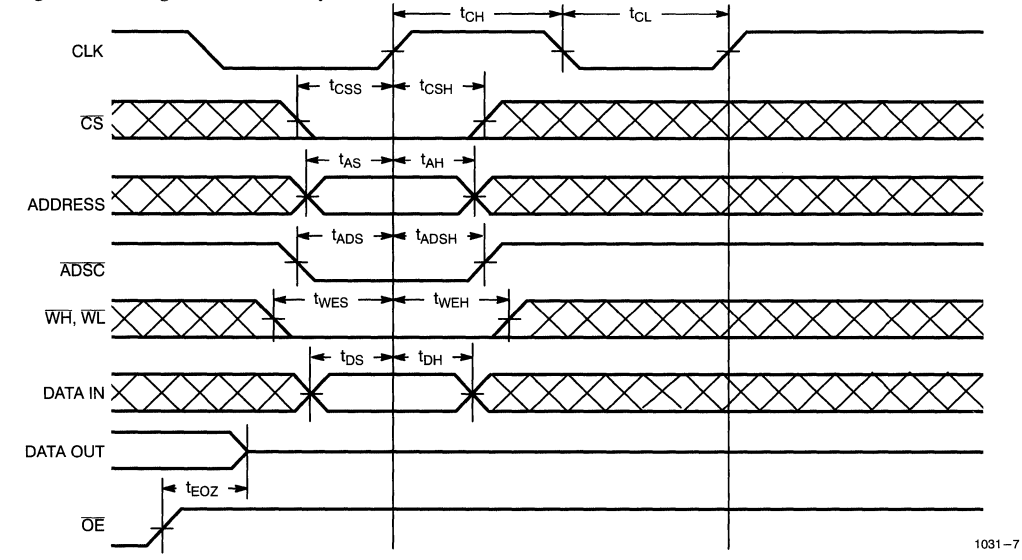
Single Write Timing: Write Initiated by $\overline{ADSP}$



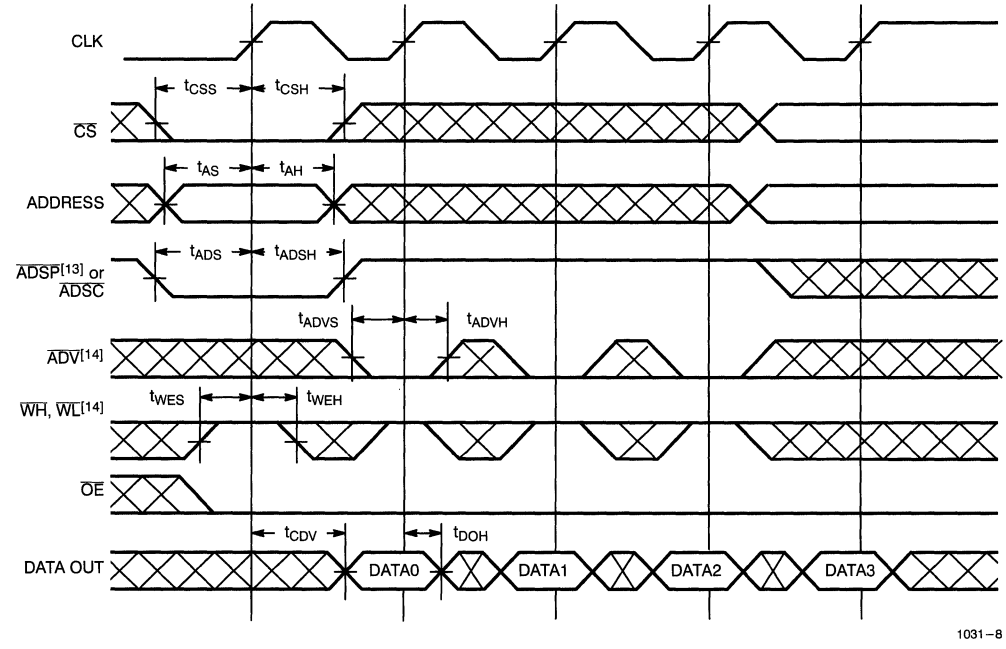
Notes:
12. $\overline{OE}$ is LOW throughout this operation.
13. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
14. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WL}$, and $\overline{WH}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$

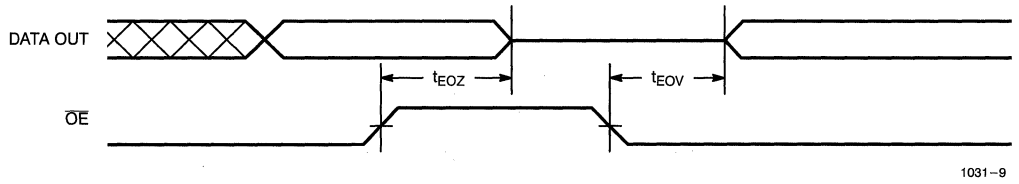


Burst Read Sequence with Four Accesses

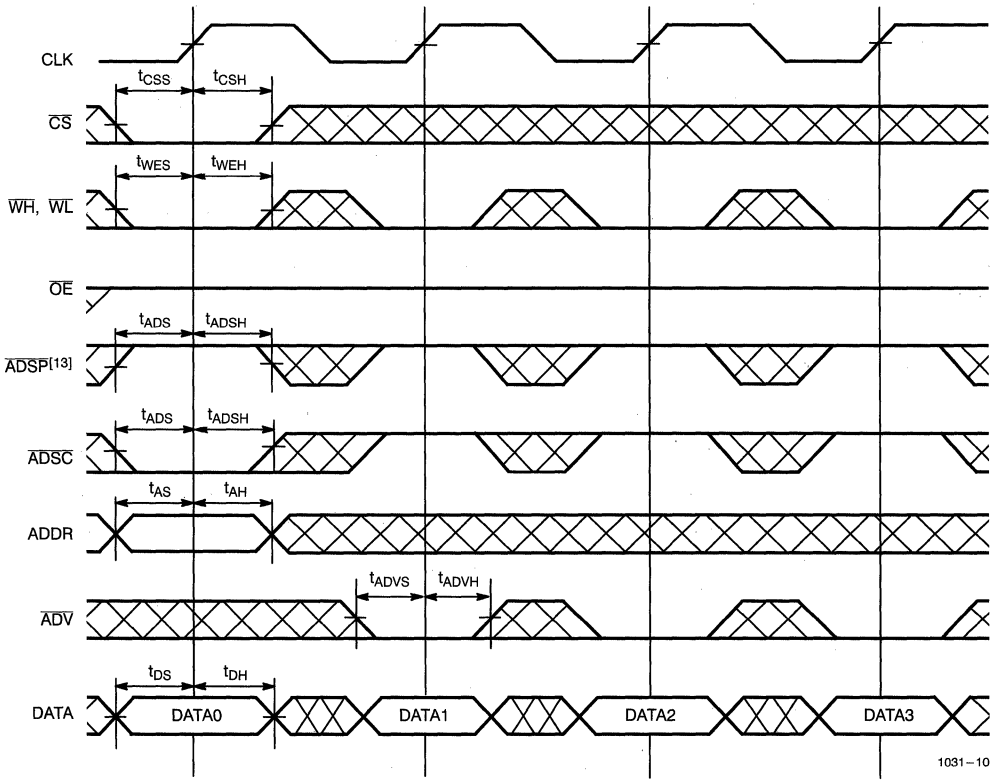


Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)

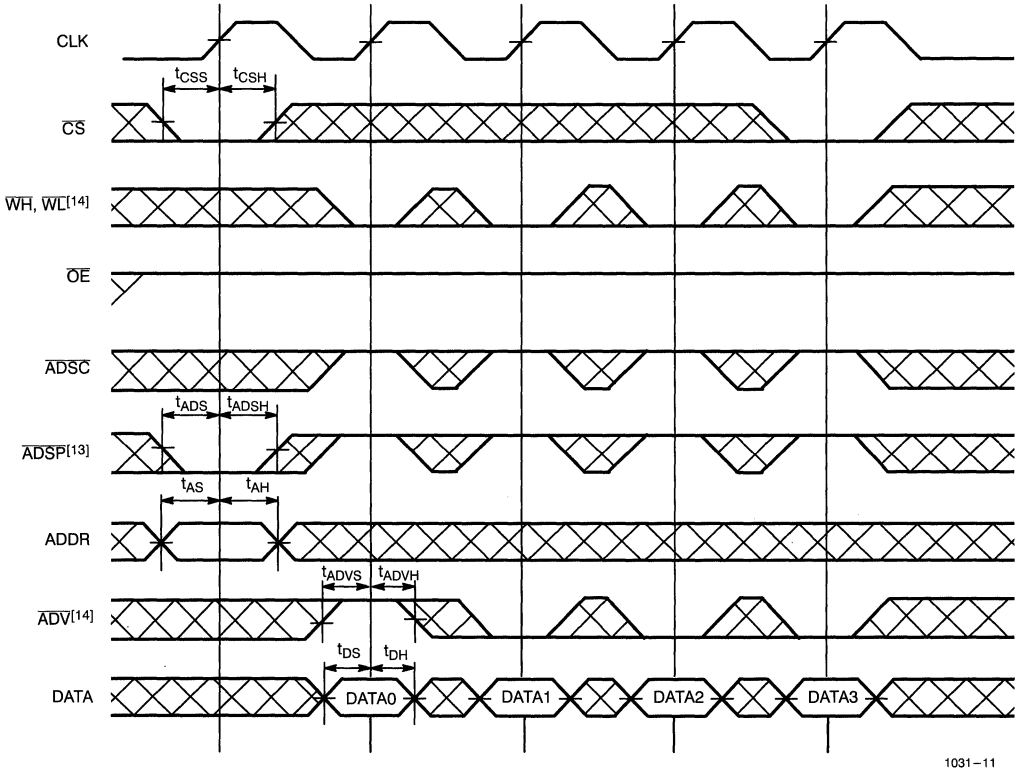


Write Burst Timing: Write Initiated by $\overline{ADSC}$



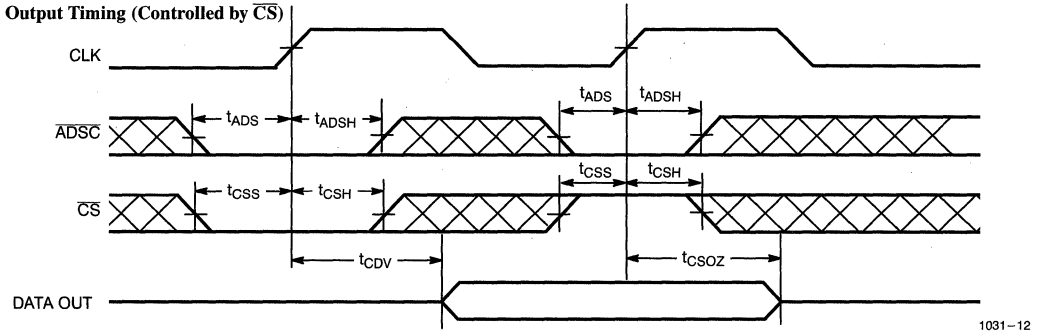
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

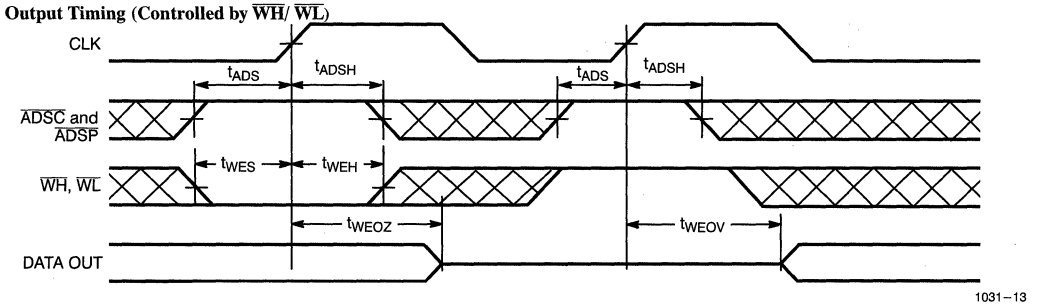


Switching Waveforms (continued)

Output Timing (Controlled by $\overline{CS}$)



Output Timing (Controlled by $\overline{WH}$/ $\overline{WL}$)



Truth Table

Input						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C1031-7JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031-7NC	TBD	52-Lead Plastic Quad Flatpack	
8	CY7C1031-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031-8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C1031-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031-10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C1031-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1031-12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C1031-12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C1032-7JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032-7NC	TBD	52-Lead Plastic Quad Flatpack	
8	CY7C1032-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032-8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C1032-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032-10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C1032-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1032-12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C1032-12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain preliminary information.

Document #: 38-00219-B

128K x 9 Static RAM

Features

- **High speed**
  — t_{AA} = 12 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 1020 mW
- **Low standby power**
  — 250 mW
- **2.0V data retention**
  — 100 µW
- **Available in plastic 32-pin 400-mil SOJ**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C1088 is a high-performance CMOS static RAM organized as 131,072 words by 9 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

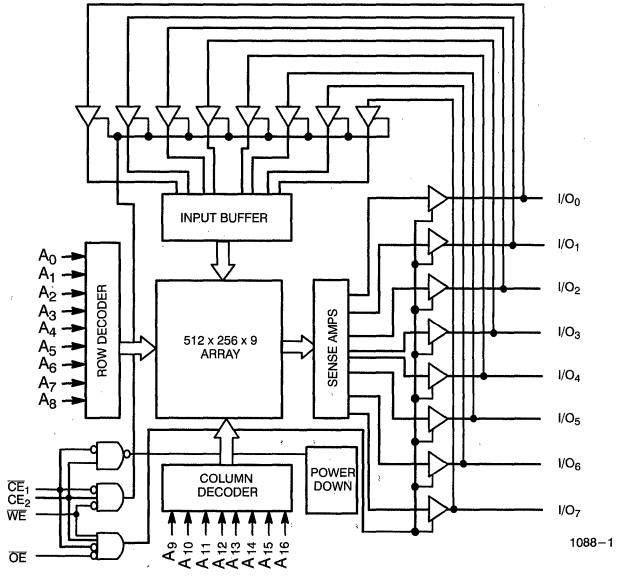
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

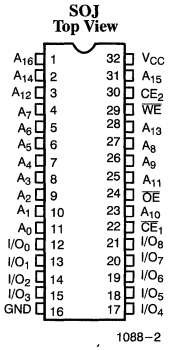
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1088 is available in standard 32-pin 400-mil-wide SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1088–12	7C1088–15	7C1088–20	7C1088–25
Maximum Access Time (NS)		12	15	20	25
Maximum Operating Current (mA)	Commercial	185	170	155	145
	Military		180	170	160
Maximum Standby Current (mA)	Commercial	45	40	30	30
	Military		40	30	30

Document #: 38–00451

CY7C1331
CY7C1332

64K x 18 Synchronous Cache 3.3V RAM

Features

- **Supports 66-MHz Pentium™ processor cache systems with zero wait states**
- **Single 3.3V power supply**
- **64K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 8.5 ns**
- **Two-bit wraparound counter supporting the Pentium and 486 burst sequence (CY7C1331)**
- **Two-bit wraparound counter supporting linear burst sequence (CY7C1332)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **JEDEC-standard pinout**
- **52-pin PLCC and PQFP packaging**

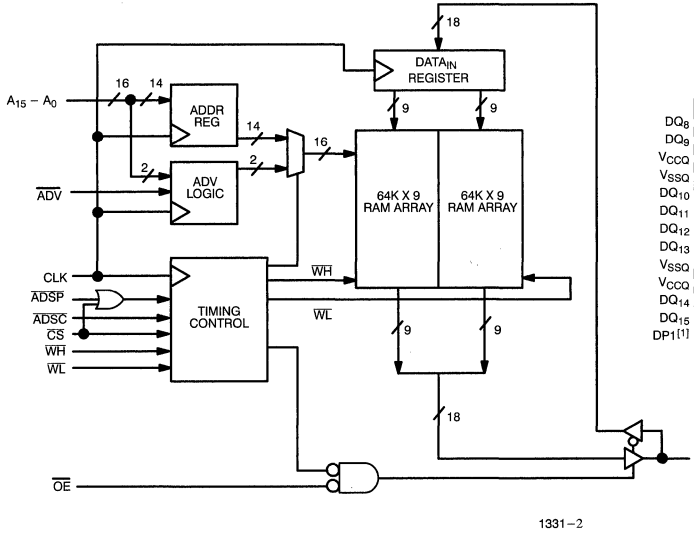
Functional Description

The CY7C1331 and CY7C1332 are 3.3V 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

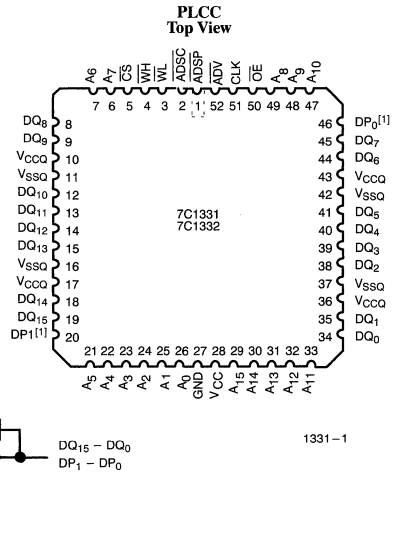
The CY7C1331 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1332 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1331–8 7C1332–8	7C1331–10 7C1332–10	7C1331–12 7C1332–12
Maximum Access Time (ns)		8.5	10	12
Maximum Operating Current (mA)	Commercial	200	200	170
	Military			200

Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_x.

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Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1331 and CY7C1332 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C1331 and CY7C1332 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Since the CY7C1331 and the CY7C1332 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data lines. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise.

Burst Sequences

The CY7C1331 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C1332 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 512-Kbyte secondary cache for a hypothetical 3.3V, 66-MHz Pentium or i486 processor using four CY7C1331 cache RAMs.

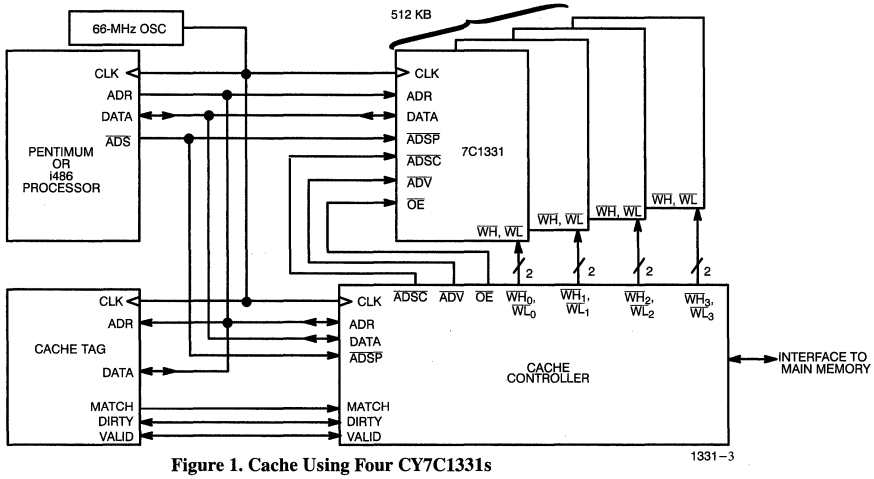


Figure 1. Cache Using Four CY7C1331s

Pin Definitions

Signal Name	Type	# of Pins	Description
V_{CC}	Input	1	+3.3V Power
V_{CCQ}	Input	4	+3.3V (Outputs)
GND	Input	1	Ground
V_{SSQ}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{15} - A_0$	Input	16	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{WH}$, $\overline{WL}$, $\overline{CS}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A_{15}–A_0	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$,$\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the two-bit on-chip auto-address-increment counter. In the CY7C1332, the address will be incremented linearly. In the CY7C1331, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ_{15}–DQ_0	I/O	Sixteen bidirectional data I/O lines. $DQ_{15} - DQ_8$ are inputs to and outputs from the high-order half of the RAM array, while $DQ_7 - DQ_0$ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. $DQ_{15} - DQ_8$ and $DQ_7 - DQ_0$ are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, are sampled LOW at clock rise.
DP_1–DP_0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as $DQ_{15} - DQ_0$, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .... −0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to V_{CC} + 0.3V

DC Input Voltage[2] ..... −0.5V to V_{CC} + 0.3V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}, V_{CCQ}
Com'l	0°C to +70°C	3.3V ± 0.3V
Mil	−55°C to +125°C	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C1331−8 7C1332−8 Min.	7C1331−8 7C1332−8 Max.	7C1331−10 7C1332−10 Min.	7C1331−10 7C1332−10 Max.	7C1331−12 7C1332−12 Min.	7C1331−12 7C1332−12 Min.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX}=1/t_{CYC}	Com'l		200		200		170	mA
			Mil						200	

Notes:

2. Minimum voltage equals − 2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

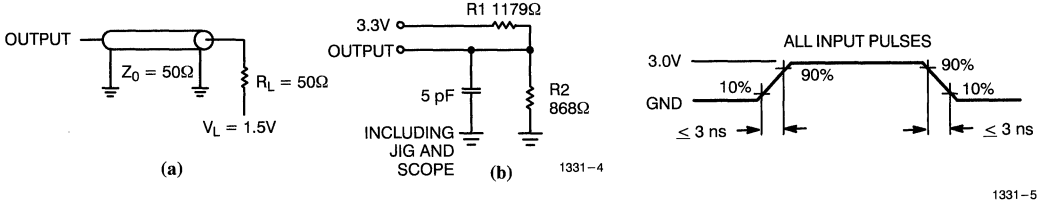
Electrical Characterictics Over the Operating Range[4](continued)

Parameter	Description	Test Conditions		7C1331–8 7C1332–8 Min.	7C1331–8 7C1332–8 Max.	7C1331–10 7C1332–10 Min.	7C1331–10 7C1332–10 Max.	7C1331–12 7C1332–12 Min.	7C1331–12 7C1332–12 Min.	Unit
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		60		60		40	mA
			Mil						40	
I_{SB2}	Automatic CE Power-Down Current –CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC}$ –0.3V, $V_{IN} \geq V_{CC}$ –0.3V or $V_{IN} \leq$ 0.3V, f=f_{MAX}[6]	Com'l		20		20		20	mA
			Mil						20	

Capacitance[7]

Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	Com'l	5	pF
			Mil	6	
C_{IN}: Other Inputs	Input Capacitance		Com'l	5	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	8	pF
			Mil	16	

AC Test Loads and Waveforms



Notes:

6. Inputs are disabled, clock is allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[8]

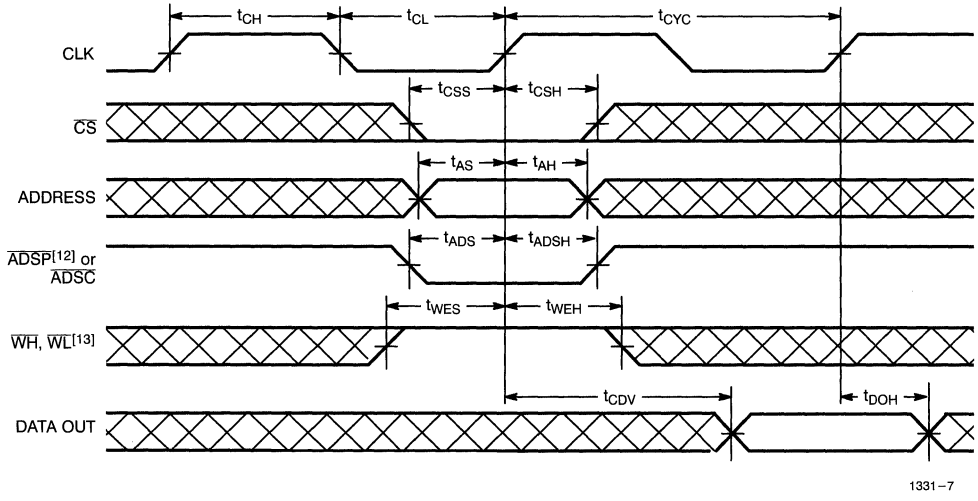
Parameter	Description	7C1331–8 7C1332–8		7C1331–10 7C1332–10		7C1331–12 7C1332–12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15		15		20		ns
t_{CH}	Clock HIGH	5		6		8		ns
t_{CL}	Clock LOW	5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		8.5		10		12	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		2.5		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[9]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[9]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		6	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[9,10]		5		6		7	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[10]		8.5		10		12	ns

Notes:

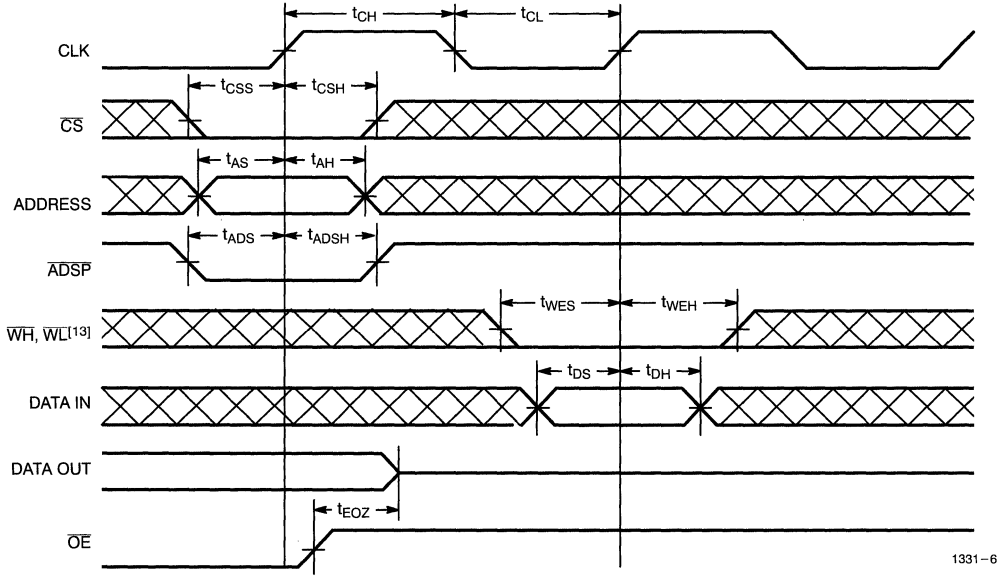
8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance as shown in (a) and (b) of AC Test Loads.
9. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[11]



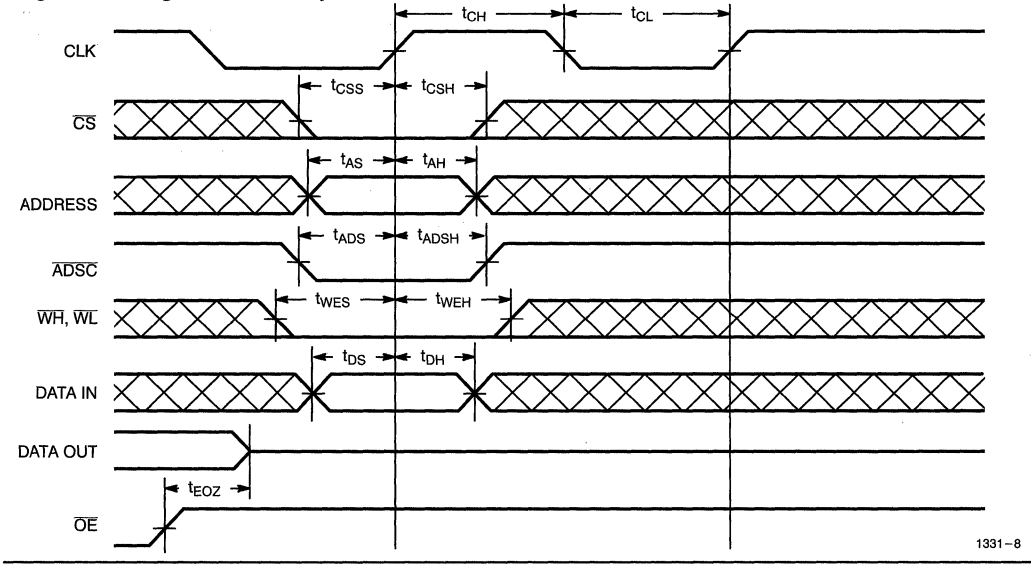
Single Write Timing: Write Initiated by $\overline{ADSP}$



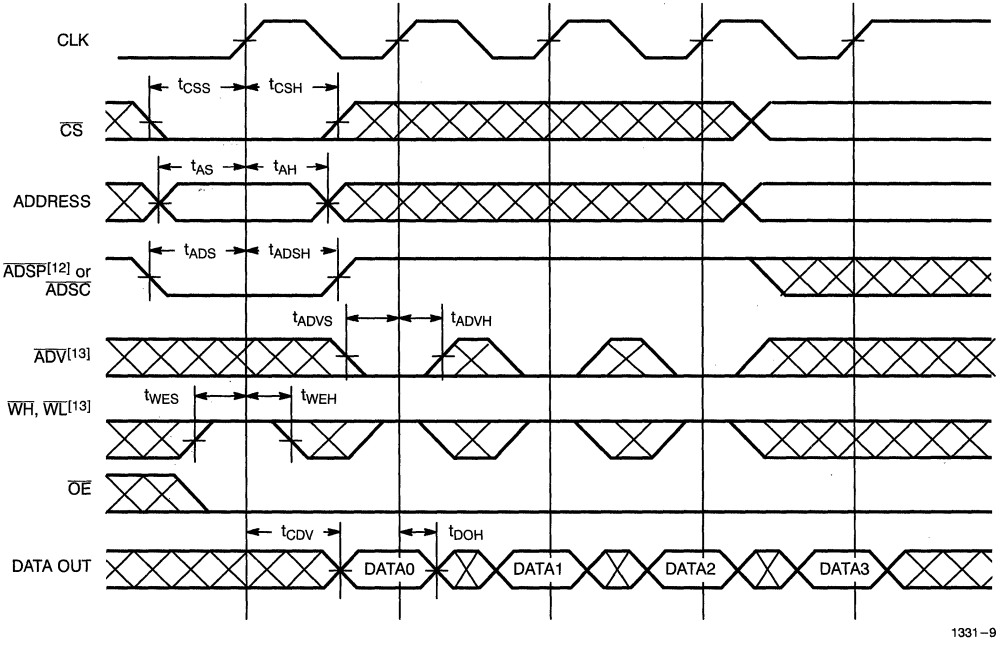
Notes:
11. $\overline{OE}$ is LOW throughout.
12. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
13. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WH}$, and $\overline{WL}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$

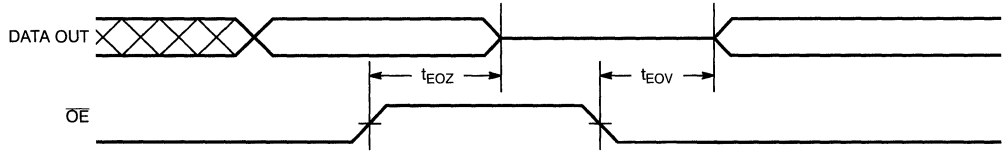


Burst Read Sequence with Four Accesses



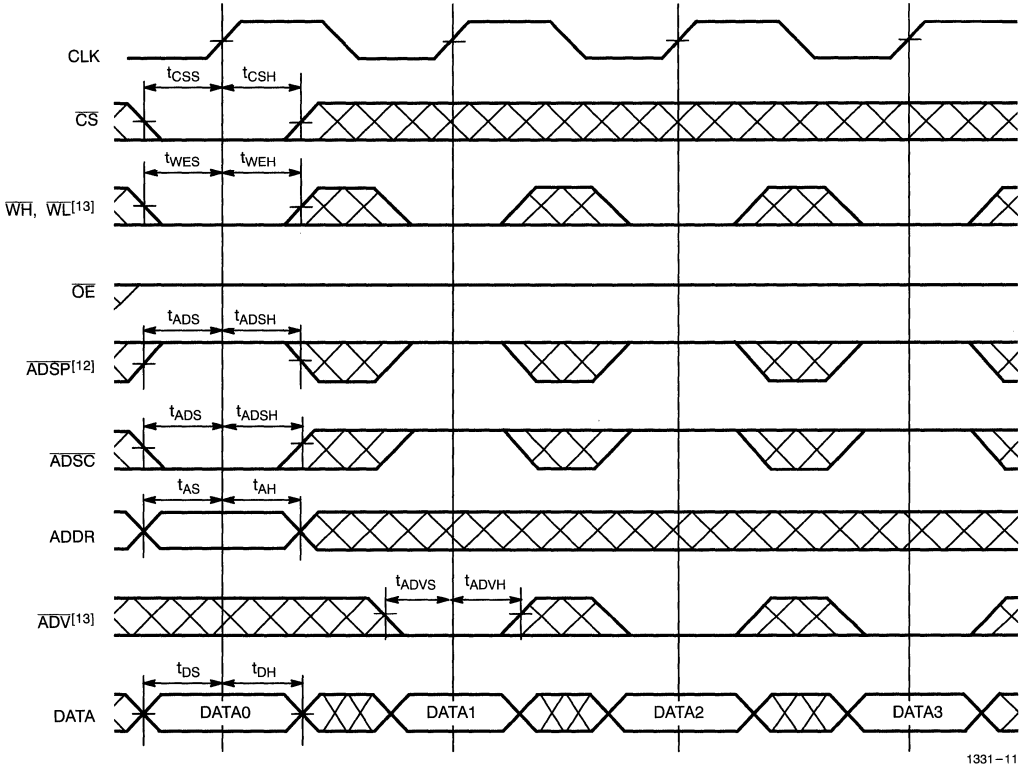
Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)



1331–10

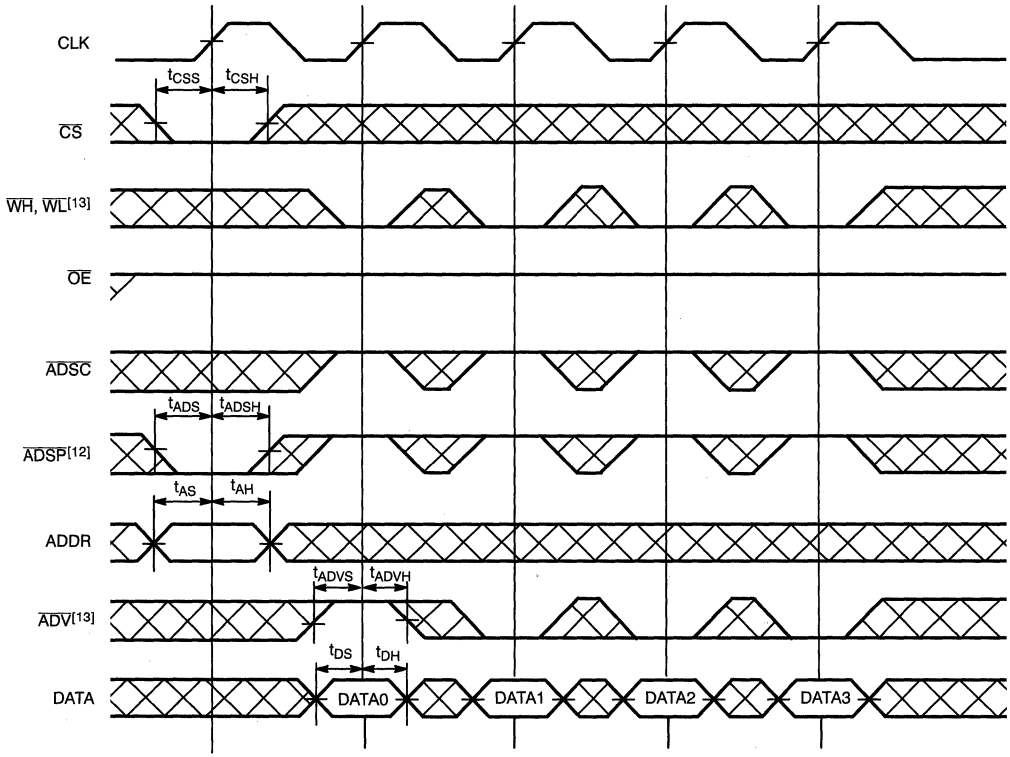
Write Burst Timing: Write Initiated by $\overline{ADSC}$



1331–11

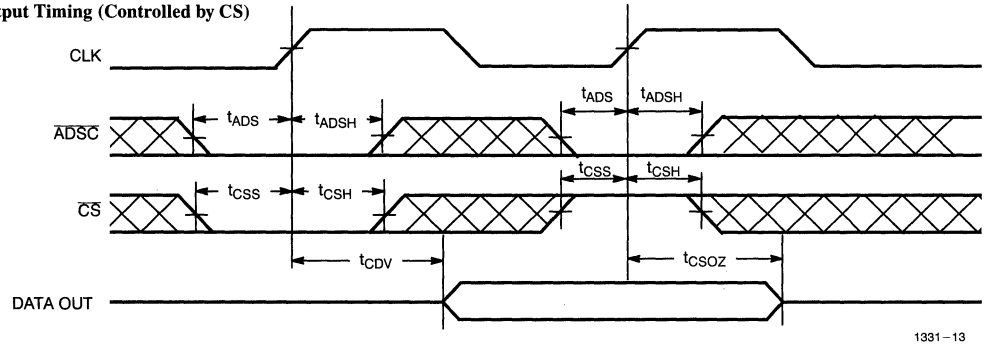
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$



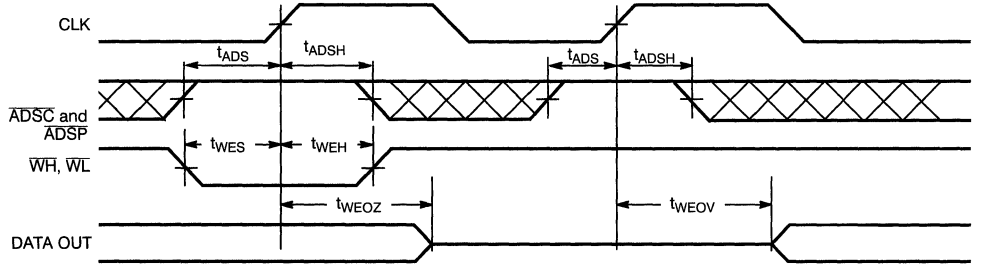
Switching Waveforms (continued)

Output Timing (Controlled by CS)



1331–13

Output Timing (Controlled by $\overline{WH}/\overline{WL}$)



1331–14

Truth Table

Inputs						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, begin burst
X	H	H	L	H	L→H	Incremented burst address	Read cycle, begin burst
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8.5	CY7C1331–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–8NC	N52	52-Lead Plastic Quad Flatpack	
10	CY7C1331–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–10NC	N52	52-Lead Plastic Quad Flatpack	
12	CY7C1331–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–12NC	N52	52-Lead Plastic Quad Flatpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8.5	CY7C1332–8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–8NC	N52	52-Lead Plastic Quad Flatpack	
10	CY7C1332–10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–10NC	N52	52-Lead Plastic Quad Flatpack	
12	CY7C1332–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–12NC	N52	52-Lead Plastic Quad Flatpack	

Document #: 38–00223–B

CY7C1335
CY7C1336

32K x 32 Synchronous Cache RAM

Features

- **Supports 75-MHz Pentium™ and PowerPC™ operations with zero wait states**
- **Fully registers inputs and outputs for pipelined operation**
- **32K x 32 common I/O architecture**
- **Single 3.3V power supply**
- **Fast Clock-to-output times**
  - **— 7.0 ns with 0 pF (for 75-MHz systems)**
  - **— 8.5 ns with 0 pF (for 66-MHz systems)**
  - **— 10 ns with 0 pF (for 60-MHz systems)**
- **Burst counter supporting Intel Pentium processor (CY7C1335)**
- **Burst counter supporting PowerPC (CY7C1336)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **JEDEC-standard 100 TQFP pinout**

Functional Description

The CY7C1335 and CY7C1336 are 3.3V 32K by 32 synchronous cache SRAMs designed to support zero wait state secondary cache with minimal glue logic.

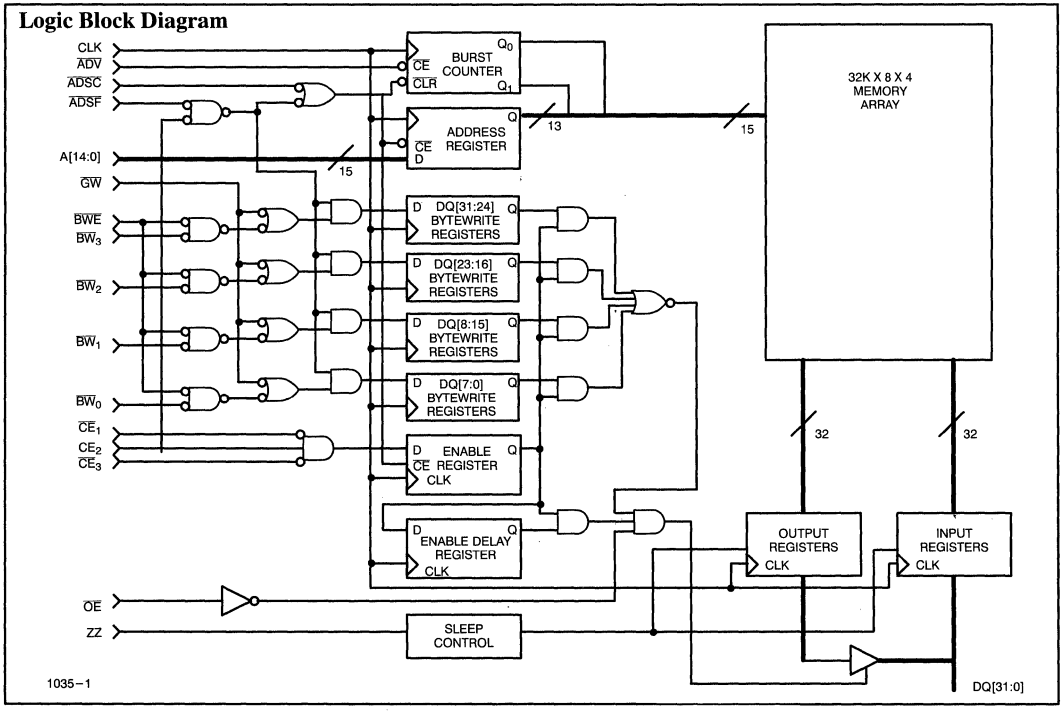
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 7.0 ns (0 pF load). A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY7C1335 supports secondary cache in systems utilizing Pentium possessors. Its counter follows the burst sequence of the Pentium processor. The CY7C1336 is designed for processors that utilize a linear burst sequence, such as the PowerPC. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) of the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{0-3}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and write data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CS}_1$, CS_2, $\overline{CS}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masking during the first clock of a read cycle.

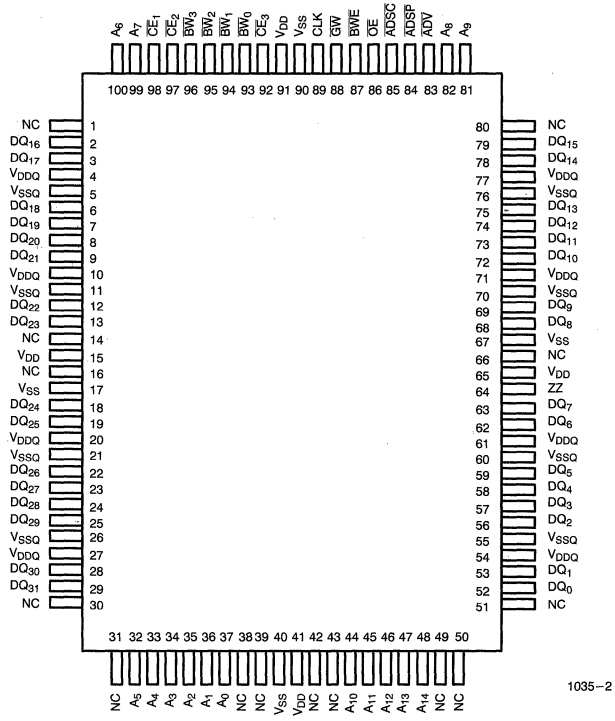
Logic Block Diagram



Pentium is a trademark of Intel Corporation.
PowerPC is a trademark of IBM Corporation.

Pin Configuration

Top View



1035–2

Selection Guide

		7C1335–7 7C1336–7	7C1335–8 7C1336–8	7C1335–10 7C1336–10
Maximum Access Time (ns) (0-pF load)		7.0	8.5	10
Maximum Operating Current (mA)	Commercial	180	170	160

Pin Definitions

Pin Number	Name	I/O	Description
32–37, 44–48, 81, 82, 99, 100	A[14:0]	Input-Synchronous	Address Inputs used to select one of the 32K address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW.
93–96	BW[3:0]	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BW}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted. (ALL bytes are written, regardless of the values on $\overline{BW}$[3:0].)
87	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	CLK	Input-Clock	Clock input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
98	$\overline{CE_1}$	Input-Synchronous	Chip Select 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. Also used to gate $\overline{ADSP}$.
97	CE_2	Input-Synchronous	Chip Select 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. Also used to gate $\overline{ADSP}$.
92	$\overline{CE_3}$	Input-Synchronous	Chip Select 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
86	$\overline{OE}$	Input-Synchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked (deasserted) during the first clock of a read cycle.
83	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A[0–14] is captured in the address registers. A_0 and A_1 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE_1}$ is deasserted HIGH.
85	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, A[0–14] is captured in the address registers. A_0 and A_1 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
64	ZZ	Input-Synchronous	ZZ "sleep" Input. When ZZ is implemented, places the device in a non-time critical "sleep" condition with data integrity preserved.
29, 28, 25–22, 19, 18, 13, 12, 9–6, 3, 2, 79, 78, 75–72, 69, 68, 63, 62 59–56, 53, 52	DQ[31:0]	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A[14:0] during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ[31:0] are placed in a three-state condition.
15,41,65, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
17,40,67, 91	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54,61,70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 3.3V power supply.
5, 10, 21, 26, 55,60,71, 76	V_{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.

Document #: 38–00452

32K x 8 3.3V Static RAM

Features

- **Single 3.3V power supply**
- **Ideal for low-voltage cache memory applications**
- **High speed**
  - **12 ns**
- **Low active power**
  - **255 mW**
- **Low standby power**
  - **90 mW**
- **2.0V data retention**
  - **100 μW**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Plastic DIP, SOJ, and TSOP packaging**

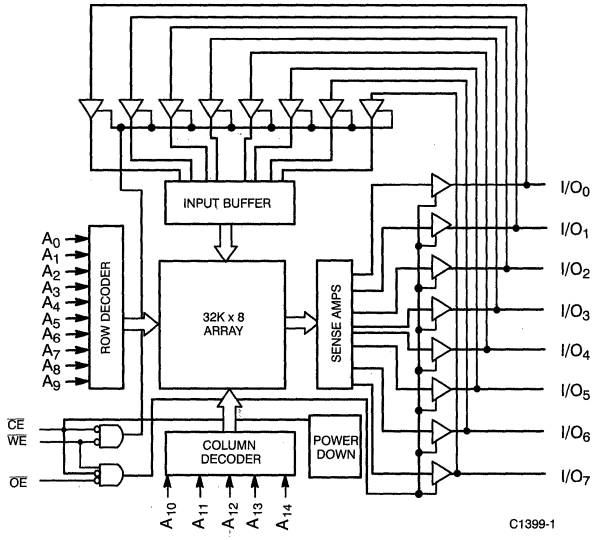
Functional Description

The CY7C1399 is a high-performance 3.3V CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 60% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. The CY7C1399 is available in standard 300-mil-wide DIP and SOJ packages. A die coat is used to ensure alpha immunity.

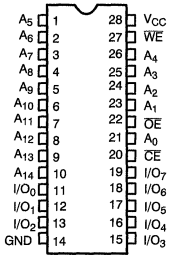
Logic Block Diagram



C1399-1

Pin Configurations

DIP/SOJ
Top View



C1399-2

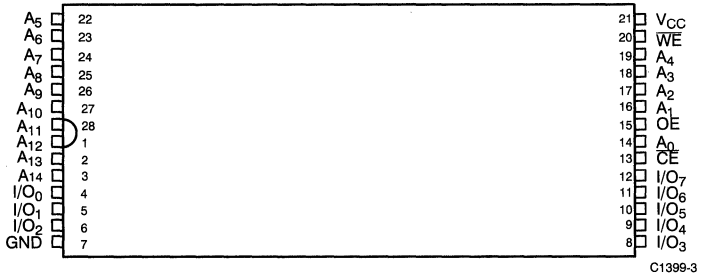
Selection Guide

	7C1399–12	7C1399–15	7C1399–20	7C1399–25	7C1399–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	60	55	50	45	40
Maximum Standby Current (mA)	5	5	5	5	5

Shaded area contains advanced information.

Pin Configurations (continued)

TSOP
Top View



C1399-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .. −0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±0.3 mV

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	7C1399−12 Min.	7C1399−12 Max.	7C1399−15 Min.	7C1399−15 Max.	7C1399−20 Min.	7C1399−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = −8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		60		55		50	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}		5		5		5	mA
I_{SB2}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC}, 0.3V or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f=0		50		50		50	µA

Shaded area contains advanced information.

Notes:

1. Minimum voltage is equal to − 2.0V for pulse durations of less than 20 ns.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

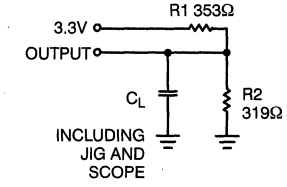
Electrical Characteristics Over the Operating Range[2] (continued)

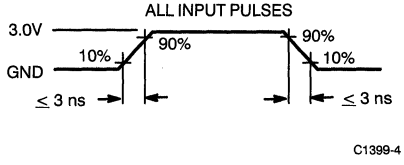
Parameter	Description	Test Conditions	7C1399–25		7C1399–35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current		−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		45		40	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		5		5	mA
I_{SB2}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} 0.3V or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0		50		50	µA

Capacitance[4]

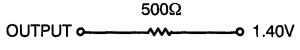
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	pF
C_{IN}: Controls			6	pF
C_{OUT}	Output Capacitance		6	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Note:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 5]

Parameter	Description	7C1399–12		7C1399–15		7C1399–20		7C1399–25		7C1399–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		5		6		6		7		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		6		7		7		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[8, 9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	8		10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	6		9		10		11		12		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		7		7		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		3		ns

Shaded area contains advanced information.

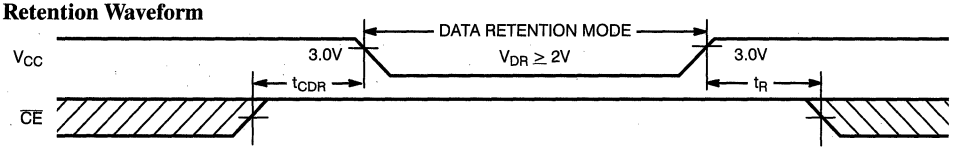
Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		ns
t_R[4]	Operation Recovery Time		t_{RC}		ns

Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. No input may exceed V_{CC} + 0.3V.

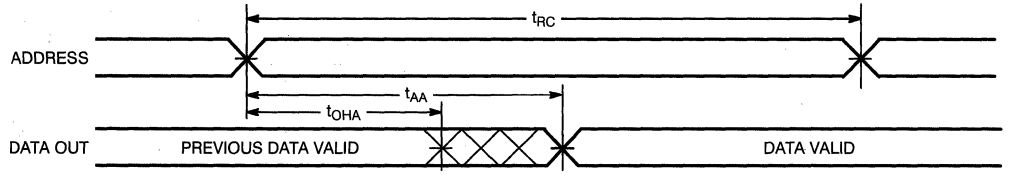
Data Retention Waveform



C1399-5

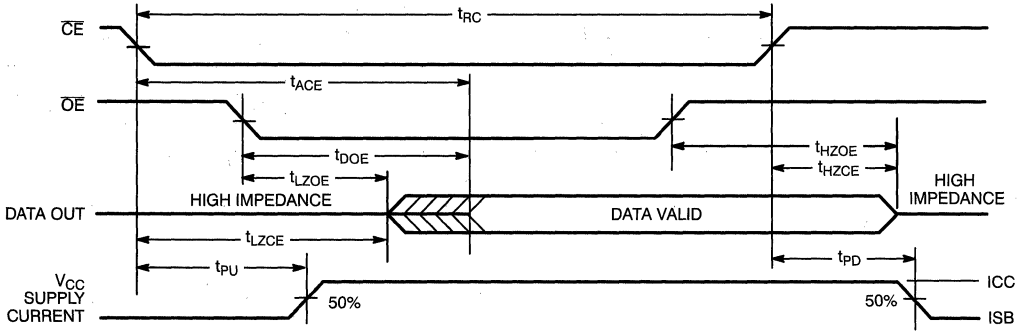
Switching Waveforms

Read Cycle No. 1[11, 12]



C1399-6

Read Cycle No. 2[12, 13]



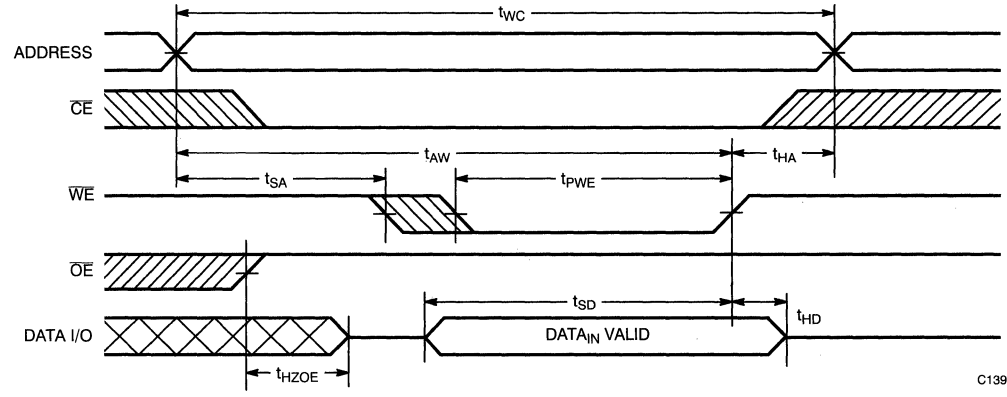
C1399-7

Notes:

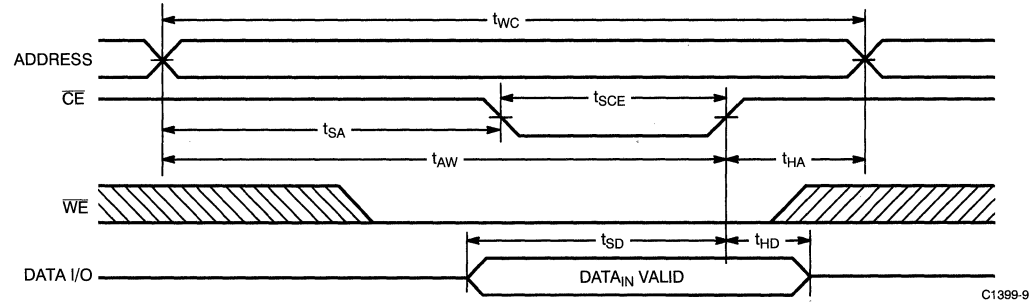
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

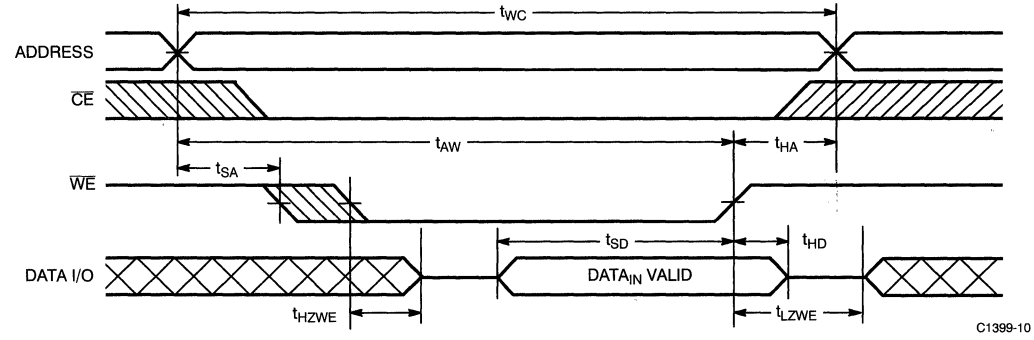
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 14, 15]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 14, 15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 15]



Notes:

14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1399-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-12VC	V21	28-Lead Molded SOJ	
	CY7C1399-12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C1399-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-15VC	V21	28-Lead Molded SOJ	
	CY7C1399-15ZC	Z28	28-Lead Thin Small Outline Package	
20	CY7C1399-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-20VC	V21	28-Lead Molded SOJ	
	CY7C1399-20ZC	Z28	28-Lead Thin Small Outline Package	
25	CY7C1399-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-25VC	V21	28-Lead Molded SOJ	
	CY7C1399-25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C1399-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C1399-35VC	V21	28-Lead Molded SOJ	
	CY7C1399-35ZC	Z28	28-Lead Thin Small Outline Package	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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Section Contents

Modules (continued)

Custom Module Capabilities

Introduction

Cypress's Multichip Products group is a leading supplier of custom memory and/or logic modules. This turnkey capability provides designers with a fast, low-risk solution for when they require the ultimate in system performance and density. Detailed information on standard modules can be found in the Static RAM and Module sections of this book.

Packaging Guidelines

High-density memory modules are now available in a wide variety of package styles that satisfy a variety of needs for high-performance system design. Since board space is a primary concern, the choice of a package style is important in meeting layout constraints as well as thermal and mechanical design objectives.

Multichip Products currently supports several commonly used module technologies including plastic components on FR4 or polyimide substrate, and ceramic components mounted on ceramic substrates. Advanced technologies suitable for the demands of higher integration components are also available.

The plastic technology employs plastic encapsulated, surface-mount components and an epoxy laminate (FR4 or polyimide) substrate. The plastic components can be SOJ, SOIC, VSOP, TSOP, QFP, or other surface-mount packages. Die can also be mounted directly to the substrate and wire bonded to the substrate.

The ceramic technology employs hermetic, ceramic-packaged devices mounted on a ceramic substrate. The components are typically leadless chip carriers, but may include other package types. The ceramic substrate has a custom interconnect for the particular components it carries. The ceramic substrate and components offer improved thermal characteristics over the plastic modules. This makes these modules suitable for extended temperature range operation, such as in military applications.

Common Packaging Options

This section describes several common module packaging options available from Cypress. A summary table (*Table 1*) compares relative board areas of each option based on a module with eight 28-pin components.

SIP

The single in-line pin package, or SIP, is a vertically mounted module with a single row of pins along one edge for through-hole mounting. The SIP configuration is typically constructed with plastic-encapsulated components mounted on an FR4 or polyimide substrate, although ceramic SIPs are also used. The pins are on a 100-mil pitch. The vertical orientation and the mounting of components on both sides of the module can increase the component density by a factor of four or more.

Flat SIP

The flat single in-line pin package, or FSIP, is virtually identical to the SIP except that the substrate is mounted in the horizontal rather than the vertical direction. When mounted to a circuit board, the flat SIP lies close and parallel to the board. Flat SIP modules save board area since they, like other modules, employ fine lead pitch surface-mount components on a high-density substrate. The flat SIP density approximates double-sided surface-mounted boards with the advantage of a very low profile and improved mechanical stability over the vertical SIP.

ZIP

The zigzag in-line pin package, or ZIP, is vertically mounted and is usually built with plastic encapsulated components on an FR4 or polyimide substrate. The ZIP module has pins along both sides of the substrate and the pins on alternate sides are staggered by 50 mils. Adjacent pins on the same side of the substrate are separated by 100 mils. The dual row of staggered pins allows a higher connection density than that of the SIP while maintaining 100-mil minimum spacing between any adjacent pins. The ZIP is especially useful in large pin count devices where the host board is designed with through-hole design rules.

SIMM

The single in-line memory module, or SIMM, is similar to the ZIP except that there are no pins for through-hole mounting. Instead, the bottom edge of the module is equipped with edge connector contacts that are plated to the substrate. The SIMM is designed to plug into motherboard sockets. The contacts are on both sides of the substrate, and contacts directly opposite each other are connected together. SIMM edge connector contacts are on a 50-mil or 100-mil pitch. SIMMs allow greater system functionality and flexibility by allowing easy use of multiple densities and speed grades.

Some module devices are available in both ZIP and SIMM packages with the same form factor. The pin out is designed so that the pinout and footprint of the SIMM socket matches the footprint of the ZIP module allowing ZIPs or SIMMs to be used interchangeably with only one board layout. The SIMM may be used in prototyping to test different speed versions of a system and then replaced with a companion ZIP for production, or SIMMs may be used in production for flexibility in memory size or memory speed.

VDIP

The VDIP, or vertical dual in-line pin package, is a vertically mounted module with two rows of pins on 100-mil centers. Row to row spacing is 100 mils, with pins of the two rows aligned directly across from one another. The dual row of pins allows a higher connection density than that of the SIP while maintaining 100-mil minimum spacing between any adjacent pins. VDIP may be either plastic or ceramic. The VDIP is useful in large pin count devices where the host board is designed with through-hole design rules.

DIP

The DIP, or dual in-line pin module, is a low-profile package with excellent mechanical ruggedness. The ceramic DIP is ideally suited for military applications. Plastic DIPs are often used when a low vertical profile is required. In some cases, the DIP device is intended to have an identical footprint and similar form factor to standard integrated circuit components and can provide larger memory capacity in the same footprint.

PGA

The PGA, or pin grid array, has an array of pins that are perpendicular to the package plane. These pins are arranged in a matrix on a 100-mil grid. Most of the matrix is filled with pins except for a central square that is normally devoid of pins.

QUIP

The QUIP, or quad in-line pin package, is very similar to the DIP package except that there is a dual row of pins along the package edge. In-row and row-to-row pin spacing is 100 mils with pins in adjacent rows aligned directly across form one another. The QUIP is a low-profile package with excellent mechanical ruggedness, with the added advantage of higher pin density for the same package length.

QFP

The QFP, or quad flat pack, is a surface-mounted module. Gull wing pins extend out from the square package on all four sides and are formed to be coplanar with the package bottom. Lead pitches are typically 50 mils or smaller.

Package Summary

Table 1 summarizes the various characteristics of the packages discussed above.

Table 1. Package Types

Package Type	Typical Pin Count		Typical Height[1]		Mil[2]	Advantages	Disadvantages	Board Space (sq. in.)[3]	
	Min.	Max.	Min.	Max.				FR4	Cer
SIP	24	50	0.5	0.9	N	Vertical orientation. FR4 or ceramic technology.	Limited pin count.	1.2	0.9
FSIP	24	50	0.2	0.4	N	Very low profile. Mechanical stability. FR4 or ceramic technology.	Lower density due to horizontal orientation.	2.7	2.4
ZIP	24	100	0.5	0.9	N	Vertical orientation. JEDEC-standard pinouts. Pinout compatible with SIMM.		1.2	N/A
SIMM	24	100	0.5	0.9	N	Vertical orientation. Socket mounting. Pinout compatible with ZIP.		1.2	N/A
VDIP	36	104	0.5	0.95	Y	Vertical orientation.		1.2	0.9
DIP	24	60	0.17	0.37	Y	Low profile. Excellent mechanical ruggedness.	Horizontal orientation.	2.9	2.9
QUIP	48	200			Y	Low profile. Excellent mechanical ruggedness. Increased number of pins.	Horizontal orientation.	2.9	2.9
QFP	68	144			Y	Surface mount. Low profile. Excellent mechanical ruggedness. Large number of pins in small area.	Surface-mount technology required. Horizontal orientation. Components on one side only.	3.1	3.1
PGA	68	144			Y	Large number of pins in thru-hole technology. Low profile. Excellent mechanical ruggedness.	Multilayer boards. Horizontal orientation. Components on one side only.	2.9	2.9

Notes:
1. Minimum and maximum height are given in inches.
2. The Mil entry contains a Y(es) or N(o) indicating if the package type is suitable for military applications.
3. Board space roughly quantifies the main board area, in square inches, taken up by the module when the module contains eight, 28-pin components.

Component Selection

Cypress's Multichip Products group handles many types of components to build custom modules. Typically, any digital component that is available in surface-mount packaging can be used, but the module is not limited to this. Standard and custom modules include SRAM, FIFOs, dual ports, EPROM, Flash, and E^2PROM devices, combined or mixed. Logic may also be employed to provide decoding, pipelined storage, or extra drive capability. The CYM1461 and the CYM1540 are examples of such devices. In the CYM1461, sixteen 32K x 8 RAMs are arranged to form a 512K x 8 module and the individual SRAMs are selected by an on board decode. The CYM1540 provides address and control buffering for a 256K x 9 static RAM module so that only a single device load and capacitance is presented to the system. Other custom modules provide for unusual memory word widths. The CYM1720 is a memory module specifically designed for 24-bit-wide DSP processors.

ECL is also a logic family suitable for collecting into a module. Unless the system is largely ECL, it makes sense to place the ECL components onto a module that is optimized for performance. Delivered as a tested component, the ECL module can be assembled into the system with high confidence of proper functionality. Typical examples of custom ECL modules include wide ECL-to-TTL translators and deep and/or wide ECL PROM or RAM memory arrays.

More complex functions may also be integrated onto a custom module; e.g., processor subsystems, embedded within a system that are dedicated to specific functions. These functions may include several forms of memory, a microprocessor or DSP, communication ports, and bus interface circuitry with possibly shared memory control. A custom module may also include an ASIC designed especially to implement the desired function. One example of such a device is the CYM4241 deep FIFO. This device includes three high-speed SRAMs, a surface-mount 50-MHz crystal oscillator, and a wire-bonded ASIC die on substrate that integrates the RAM interface control and port access arbitration. This combination of components yields a 64K by 9 FIFO in a single 28-pin DIP. By simply changing the memory content, the device can be extended to 256K by 9.

Modules undergo complete characterization and qualification before being released to production. Characterization includes the following: AC and DC characterization over voltage and temperature, and complete custom specification review. Release to production requires a verified test program with test hardware and correlation samples, complete assembly drawings and approved parts list, production and test travelers, a formal design review, and customer approval. In production, custom (and standard) modules are built using fully tested components, and are rigorously tested before they are shipped. As an example of the rigorous production testing, memory modules are tested for all DC parametrics, all AC parametrics, and functionality. Functional testing includes a select set of memory pattern sensitivity tests. This complete testing allows the module to be treated by the user as a true component with a set of specifications that are guaranteed by the manufacturer. This saves time and effort during system manufacture and provides a degree of reliability not obtainable from operations focused on only assembly.

Future Technologies

The ultimate in multichip technology is multiple die on a substrate that offers highly efficient interconnect and the densest multichip assembly technology. The technology is available now for multichip configurations with silicon chips on ceramic, epoxy laminate, and silicon substrates.

Introduction to Modules for the New User

The use of modules is growing rapidly since it is a vehicle for obtaining high integration and high performance with minimal impact on cost. Almost every personal computer now has main memory as plug in SIMM packages constructed from surface-mount DRAM components. High-performance RISC and CISC CPU subsystems are available as modules where the supplier has optimized the component I/O design and the substrate layout for maximum performance amongst the tightly coupled components.

Size is one obvious advantage of modules; their small size allows a function to fit into a very small space. Consider the economics of having a large memory array together with the system CPU on a single card in contrast to the cost of multiple memory cards connected via a backplane bus and the resulting performance loss. In many cases, the module approach is a considerable savings in materials and manufacturing cost by reducing the total number of system cards.

Applying the tight design rules of modules has its limitations. A module has line widths and spacings that support close packing of VSOP and die components, and these spacing/width design rules are at the limit of what can be handled by capable volume production substrate producers. The use of fully tested modules gives the density gain of tight design rules at economically attractive system manufacturing yields. Therefore in the manufacturing process, the module exhibits the characteristics of a monolithic device: high integration, ease of application, and high system manufacturing yield. The module brings high-density surface-mount technology to the through-hole manufacturing environment.

Performance is another significant gain obtainable from module application. Unfortunately this is the most difficult gain to quantify. Consider a memory subsystem collected tightly around a CPU versus the same memory capacity spread over one or more boards. It seems intuitively plausible that the larger subsystem will be slower: the distance to travel is longer, and the memory address and data bus lines have larger capacitance due to their longer length and the larger number of stubs on the lines. This is indeed the case. Many of the custom modules include buffers for reduced loading, registers for data pipelining, and simple or specialized decoders to ease system bus interfacing. Taken as a component, these modules typically exhibit higher capacitance than a monolithic component and incur about 5 ns additional delay for on board decoders or buffers. However, the module is from four to sixteen times as dense as through-hole monolithic devices and consequently achieve a net performance advantage.

Custom Module Development Flow

Multichip's focus is on providing turnkey memory modules. *Figure 1* illustrates the tasks performed during the development of the module.

Module development commences with the generation of a detailed Objective Specification. The module is designed to this specification, and once in production it will be guaranteed to perform as indicated in the Objective Specification.

Components are selected while the specification is being generated. In many cases, the spec is designed such that multiple sources of components can be utilized. Once the spec is complete and the components are selected, a schematic for the module is generated. The netlist from the schematic is used to drive the circuit simulator.

Custom Module Development Flow (continued)

During simulation, several types of analyses are performed. A function simulation is used to ensure that the module's logic is designed properly. Timing simulation is run to verify that the module will function when subjected to the worst-case timing delays of the components. Finally, thermal analysis may be performed to determine the thermal characteristics of the module.

The layout of the module is also netlist driven. An autorouter may be used, depending on the complexity and density of the module. Design rule checks are run to ensure that the layout does not violate any electrical or mechanical design rules. Finally, the layout output is used to generate the module substrate.

The layout output is also used to drive the pick and place equipment. This ensures consistency between design and manufacturing. While the module prototypes are being assembled, the test program is generated and the test fixture is constructed. Test program generation is largely automated, using as inputs the simulation outputs and pre-defined test program subroutines for common configurations.

Once prototypes have been generated, the standard release procedure is initiated. This procedure includes steps such as bench testing, module characterization and qualification, and fine tuning of the test program. Following customer approval of the module, it is released to production.

Quoting Information

In order to prepare a quotation or proposal, we need as much as possible of the following information:

- Circuit schematic
- Functional description
- Mechanical dimensions required
- Speed and power requirements
- Prototype and production deadlines
- Production quantity estimates
- An engineering contact to answer questions

Once the above information is received, a budgetary quotation will typically be provided within one to two weeks.

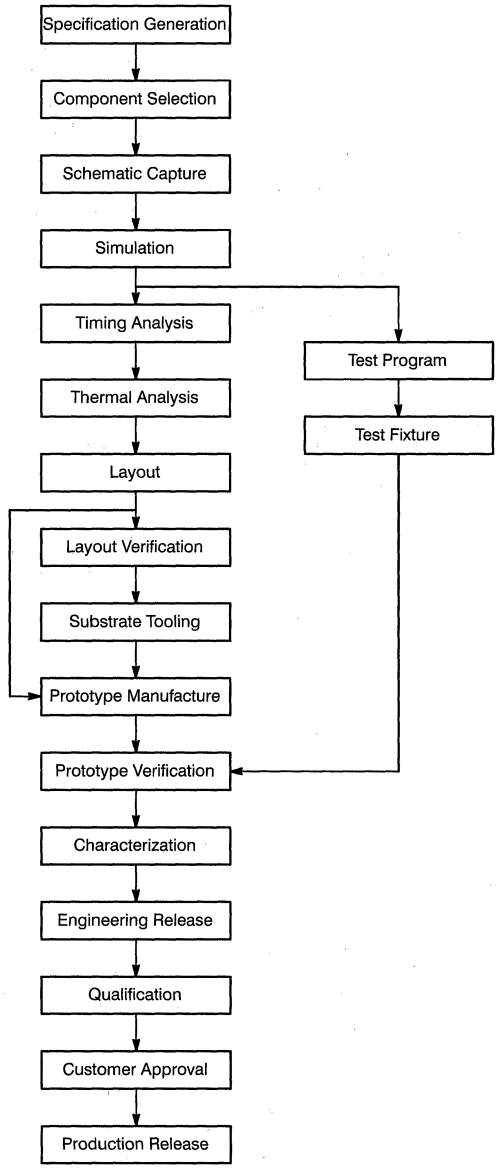


Figure 1. Custom Module Flow

CYM1420

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **32-pin, 0.6-inch-wide DIP package**
- **Low active power**
  - **1.2W (max.)**
- **FR4 SMD technology**
- **TTL-compatible inputs and outputs**
- **JEDEC-compatible pinout**
- **Commercial temperature range**

Functional Description

The CYM1420 is a very high performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 32K x 8 static RAMs mounted onto a substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and to select one of the four RAMs.

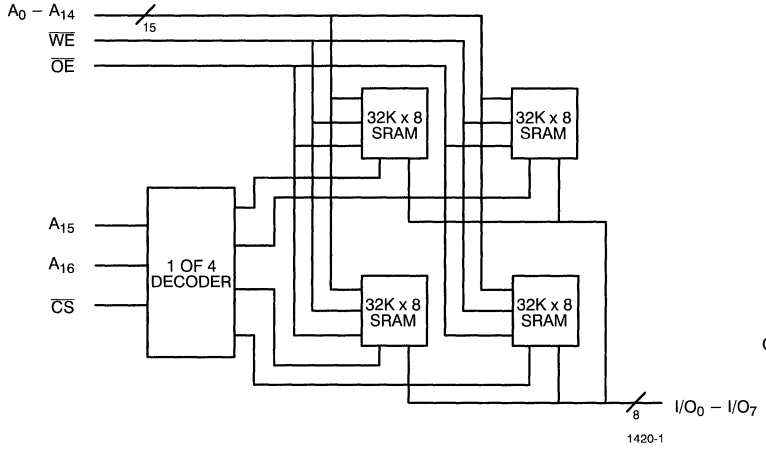
Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

3

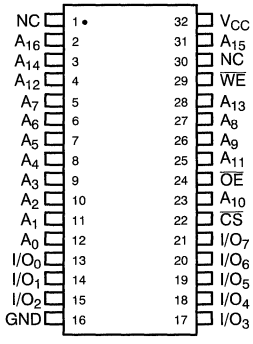
Logic Block Diagram



1420-1

Pin Configuration

DIP
Top View



1420-2

Selection Guide

		1420–20	1420–25	1420–30	1420–35	1420–45	1420–55
Maximum Access Time (ns)		20	25	30	35	45	55
Maximum Operating Current (mA)	Commercial	210	210	210	210	210	210
Maximum Standby Current (mA)	Commercial	140	140	140	140	140	140

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with .. − 10°C to +85°C (Commercial)

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

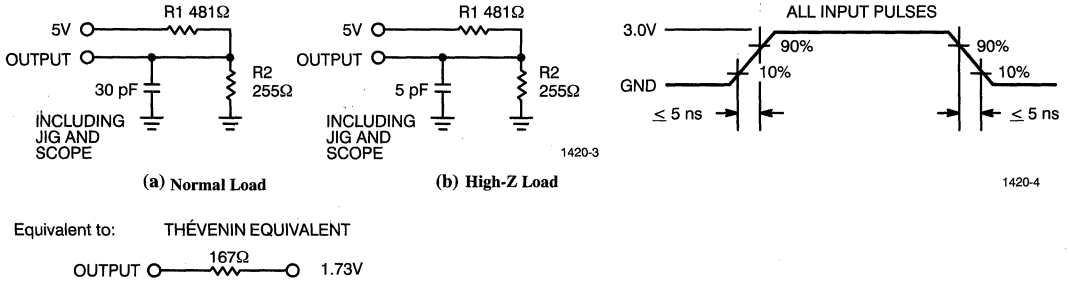
Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	µA
I_{OS}	Output Short Circuit Current[1, 2]	V_{CC} = Max., V_{OUT} = GND		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		210	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[3]	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[3]	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		80	mA

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

AC Test Loads and Waveforms



(a) Normal Load (b) High-Z Load

Equivalent to: THÉVENIN EQUIVALENT

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Switching Characteristics Over the Operating Range[4]

Parameters	Description	1420–20		1420–25		1420–30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		10		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		20		25		ns
t_{AW}	Address Set-Up to Write End	15		20		25		ns
t_{HA}	Address Hold from Write End	2		2		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	10		12		18		ns
t_{HD}	Data Hold from Write End	2		2		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	8	0	10	0	15	ns

Notes:

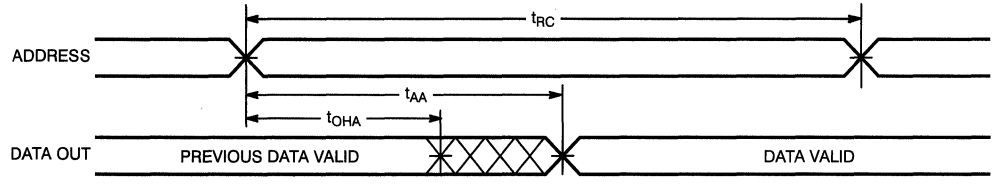
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[4]

Parameters	Description	1420–35		1420–45		1420–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		18		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		25	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		45		ns
t_{AW}	Address Set-Up to Write End	30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		25		30		ns
t_{SD}	Data Set-Up to Write End	18		20		25		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	0	25	ns

Switching Waveforms

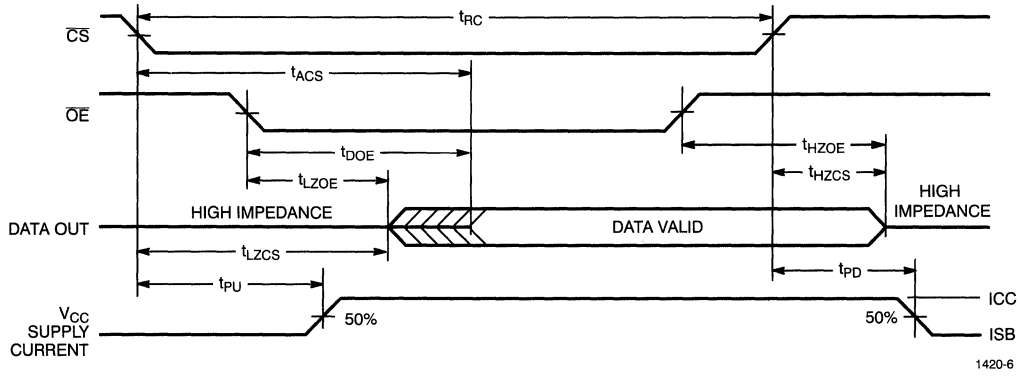
Read Cycle No. 1[8, 9]



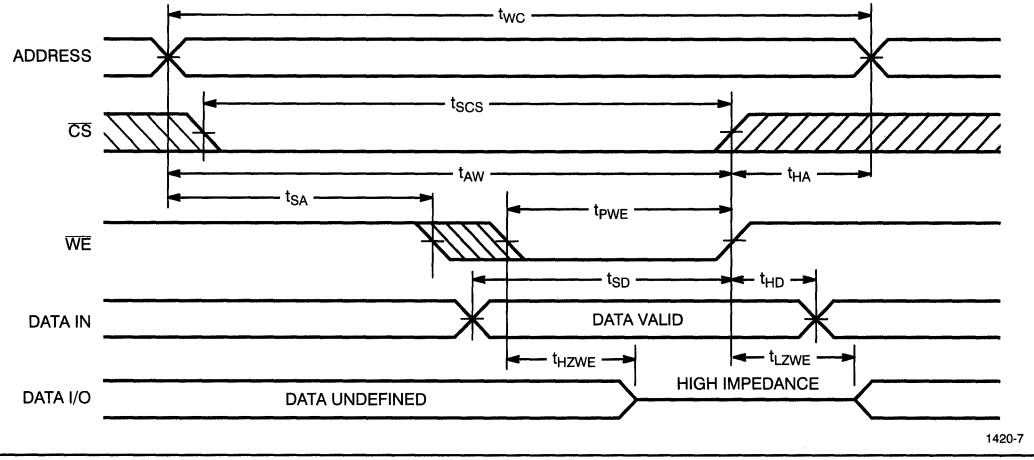
Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.

Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



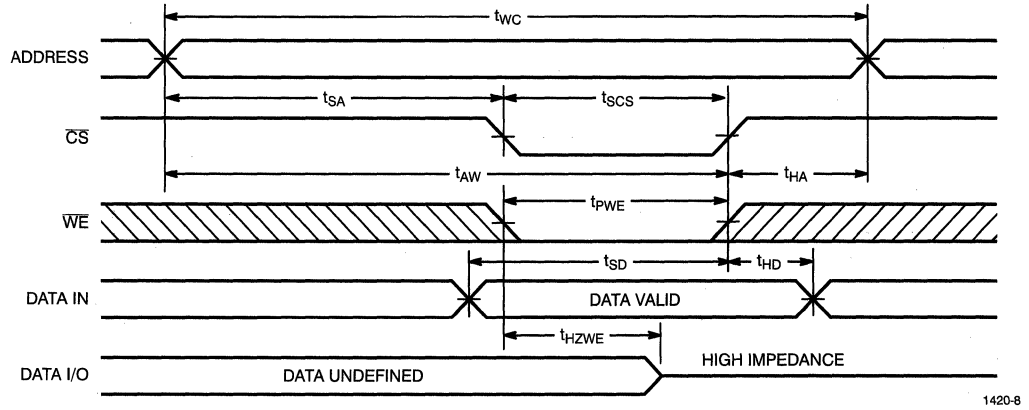
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



Notes:
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 12]



Note:
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1420PD–20C	PD05	32-Pin DIP Module	Commercial
25	CYM1420PD–25C	PD05	32-Pin DIP Module	Commercial
30	CYM1420PD–30C	PD05	32-Pin DIP Module	Commercial
35	CYM1420PD–35C	PD05	32-Pin DIP Module	Commercial
45	CYM1420PD–45C	PD05	32-Pin DIP Module	Commercial
55	CYM1420PD–55C	PD05	32-Pin DIP Module	Commercial

Document #: 38–M–00001–E

CYM1441

256K x 8 Static RAM Module

Features

- **High-density 2-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **5.3W (max.)**
- **SMD technology**
- **Separate data I/O**
- **60-pin ZIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.5 in.**
- **Small PCB footprint**
  - **1.14 sq. in.**

Functional Description

The CYM1441 is a very high performance 2-megabit static RAM module organized as 256K words by 8 bits. The module is constructed using eight 256K x 1 static RAMs in SOJ packages mounted onto an epoxy laminate substrate with pins. Two chip selects ($\overline{CS}_L$ and $\overline{CS}_U$) are used to independently enable the upper and lower 4 bits of the data word.

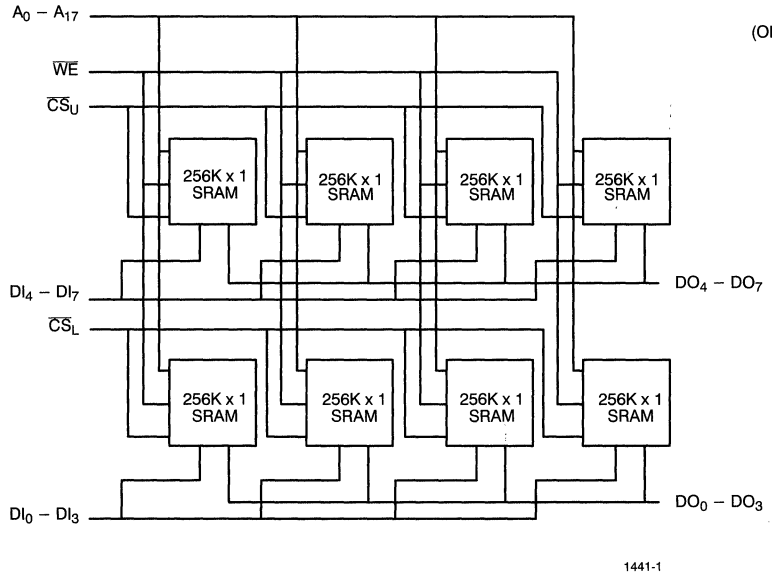
Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (DI_0 through DI_7) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data output pins (DO_0 through DO_7).

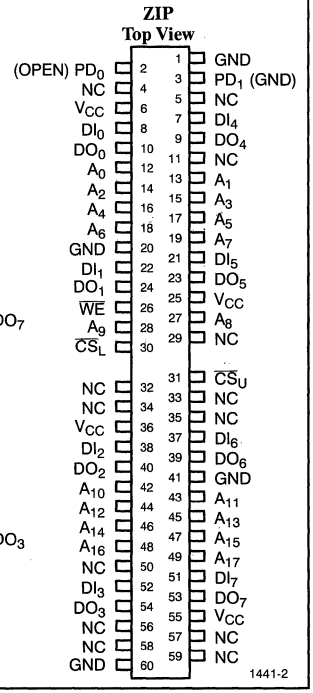
The data output pins remain in a high-impedance state unless the module is selected and write enable ($\overline{WE}$) is HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration



Selection Guide

	1441–20	1441–25	1441–35	1441–45
Maximum Access Time (ns)	20	25	35	45
Maximum Operating Current (mA)	960	960	960	960
Maximum Standby Current (mA)	320	320	320	320

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

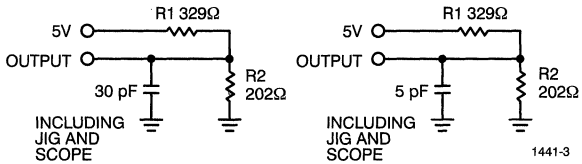
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−80	+80	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	+50	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		160	mA

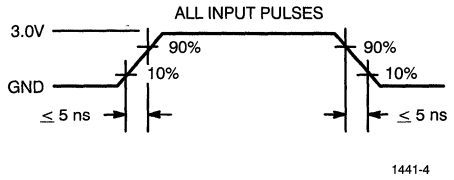
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	60	pF
C_{OUT}	Output Capacitance		15	pF

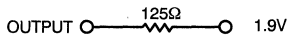
AC Test Loads and Waveforms



(a) Normal Load (b) High-Z Load



Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. V_{IN} (min.) = − 3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

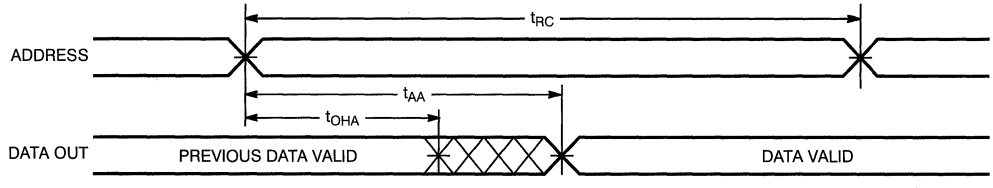
Switching Characteristics Over the Operating Range[3]

Parameter	Description	1441–20		1441–25		1441–35		1441–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	20		25		35		45		ns
t_{AA}	Address to Data Valid		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		12		15		25		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		35		45	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	20		25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		20		30		35		ns
t_{AW}	Address Set-Up to Write End	15		20		30		35		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		30		ns
t_{SD}	Data Set-Up to Write End	13		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	13	0	15	0	20	0	25	ns

Shaded area contains preliminary information.

Switching Waveforms

Read Cycle No. 1[6, 7]



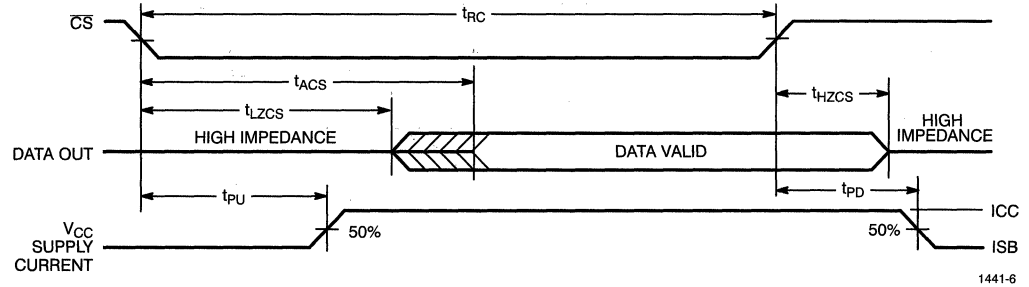
1441-5

Notes:

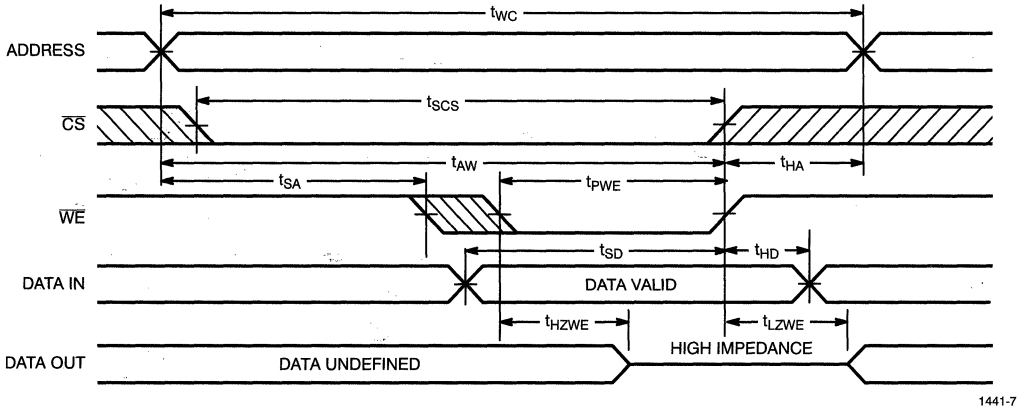
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.

Switching Waveforms (continued)

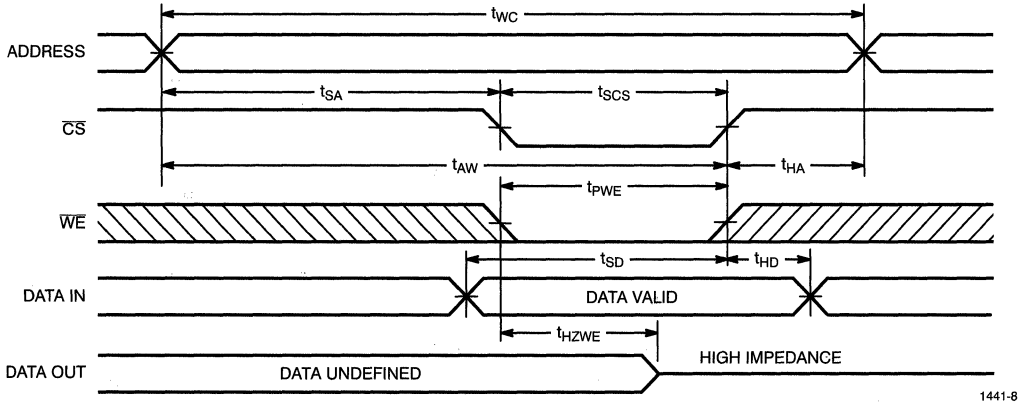
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:

8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1441PZ–20C	PZ04	60-Pin ZIP Module	Commercial
25	CYM1441PZ–25C	PZ04	60-Pin ZIP Module	Commercial
35	CYM1441PZ–35C	PZ04	60-Pin ZIP Module	Commercial
45	CYM1441PZ–45C	PZ04	60-Pin ZIP Module	Commercial

Document #: 38–M–00020–B

CYM1464

512K x 8 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **1.93W (max.)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.34 inches**

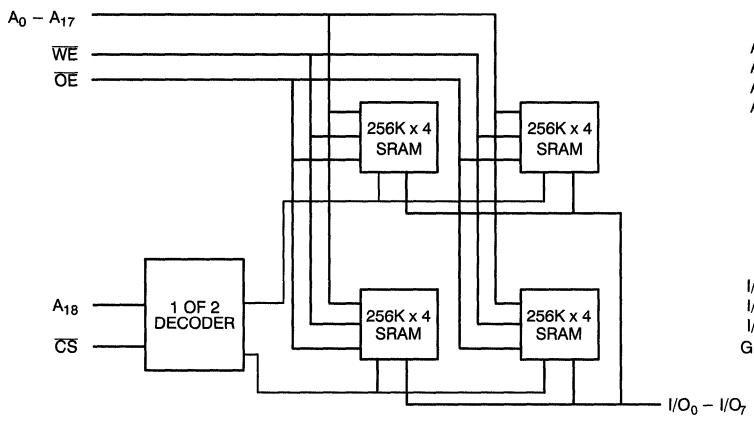
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

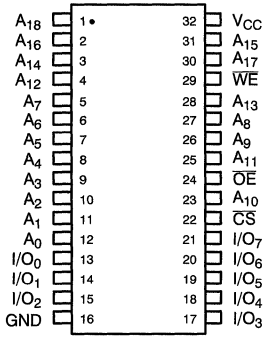
Logic Block Diagram



1464-1

Pin Configuration

DIP
Top View



1464-2

Selection Guide

	1464–20	1464–22	1464–25	1464–30	1464–35	1464–45	1464–55
Maximum Access Time (ns)	20	22	25	30	35	45	55
Maximum Operating Current (mA)	350	350	350	300	300	300	300
Maximum Standby Current (mA)	240	240	240	240	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1464−20, 22, 25		1464−30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		350		300	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		240		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		60		60	mA

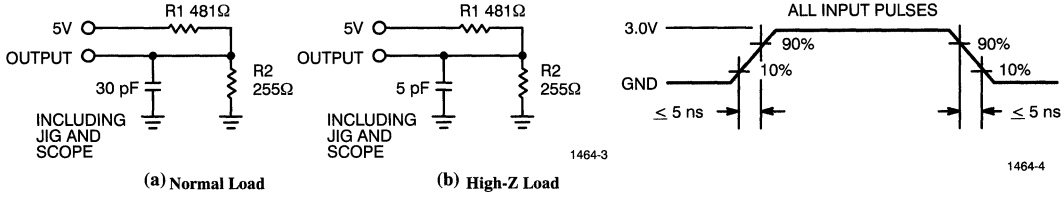
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

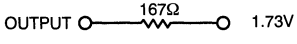
1. V_{IL} (min.) = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



(a) **Normal Load** (b) **High-Z Load**

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1464–20		1464–22		1464–25		1464–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	20		22		25		30		ns
t_{AA}	Address to Data Valid		20		22		25		30	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		22		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		13		13		15		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	10	0	10	0	10	0	10	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	15	0	15	0	15	0	20	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	20		22		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		17		20		25		ns
t_{AW}	Address Set-Up to Write End	15		15		20		25		ns
t_{HA}	Address Hold from Write End	3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		15		20		ns
t_{SD}	Data Set-Up to Write End	12		12		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		15		15		15	ns

Notes:

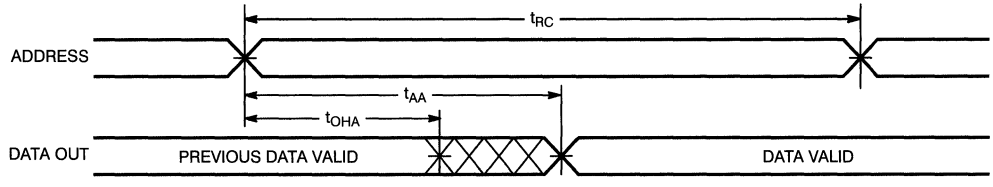
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[3]

Parameter	Description	1464–35		1464–45		1464–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	15	0	15	0	15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	20	0	20	0	20	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	6		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		35		40		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	2		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		15		20	ns

Switching Waveforms

Read Cycle No. 1[6, 7]

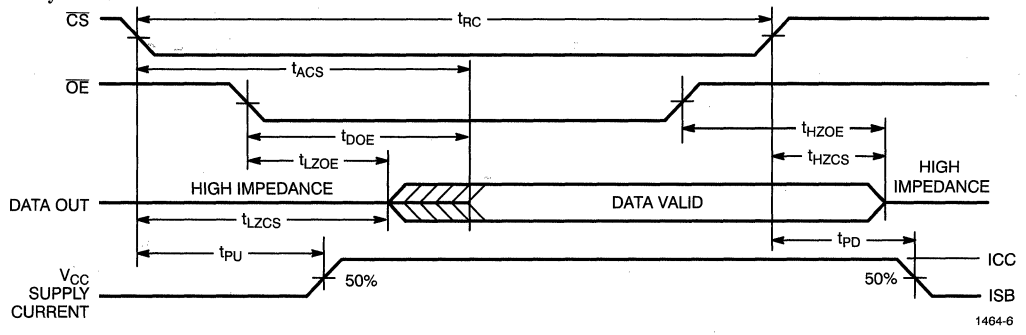


1464-5

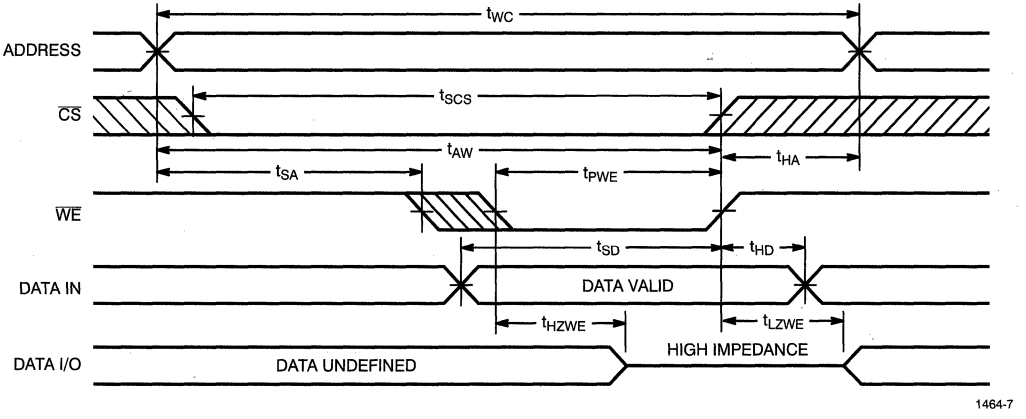
Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.

Switching Waveforms (continued)

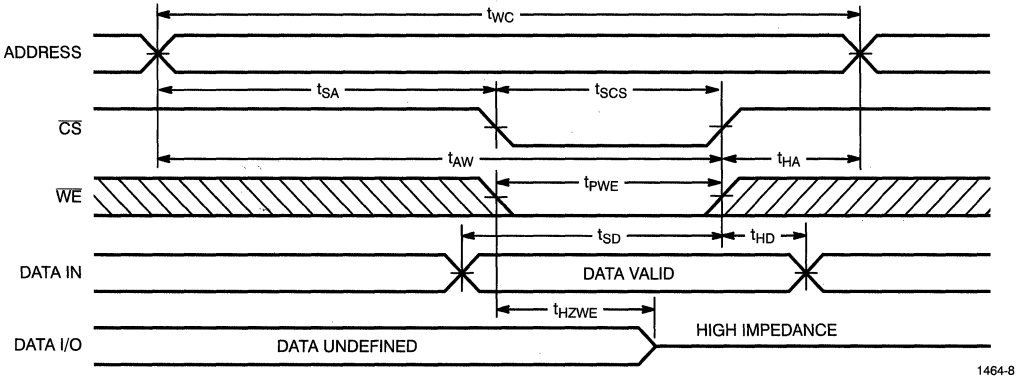
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:

8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CYM1464PD–20C	PD02	32-Pin DIP Module	Commercial
22	CYM1464PD–22C	PD02	32-Pin DIP Module	Commercial
25	CYM1464PD–25C	PD02	32-Pin DIP Module	Commercial
30	CYM1464PD–30C	PD02	32-Pin DIP Module	Commercial
35	CYM1464PD–35C	PD02	32-Pin DIP Module	Commercial
45	CYM1464PD–45C	PD02	32-Pin DIP Module	Commercial
55	CYM1464PD–55C	PD02	32-Pin DIP Module	Commercial

Document #: 38–M–00030–D

CYM1465

512K x 8 SRAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **Low active power**
  - **605 mW (max.)**
- **2V data retention (L Version)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.27 in.**
- **Small PCB footprint**
  - **0.98 sq. in.**

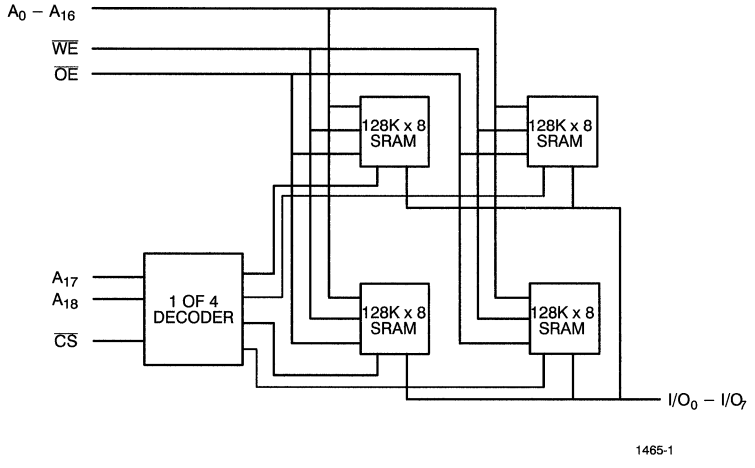
Functional Description

The CYM1465 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 128K x 8 RAMs mounted on a substrate with pins. A decoder is used to interpret the higher-order addresses (A_{17} and A_{18}) and to select one of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

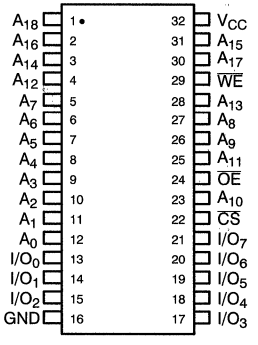
Logic Block Diagram



1465-1

Pin Configuration

DIP
Top View



1465-2

Selection Guide

	1465–70	1465–85	1465–100	1465–120	1465–150
Maximum Access Time (ns)	70	85	100	120	150
Maximum Operating Current (mA)	110	110	110	110	110
Maximum Standby Current (mA)	12	12	12	12	12

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −55°C to +150°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

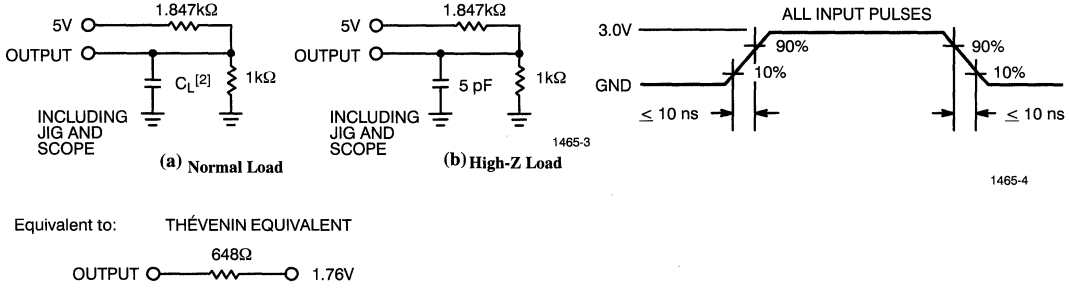
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		1465 Min.	1465 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 1.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			110	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			12	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	Standard Version		8	mA
			L Version		420	µA

Capacitance[1]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	45	pF
C_{OUT}	Output Capacitance		45	pF

AC Test Loads and Waveforms



Notes:

1. Tested on a sample basis.
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance for 85-, 100-, 120-, and 150-ns speeds. C_L = 30 pF for 70-ns speed.

Switching Characteristics Over the Operating Range[2]

Parameter	Description	1465–70		1465–85		1465–100		1465–120		1465–150		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	70		85		100		120		150		ns
t_{AA}	Address to Data Valid		70		85		100		120		150	ns
t_{OHA}	Data Hold from Address Change	10		10		10		10		10		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		70		85		100		120		150	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		45		50		60		75	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		25		30		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		30		30		35		45		60	ns
WRITE CYCLE[4]												
t_{WC}	Write Cycle Time	70		85		100		120		150		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	65		75		90		100		115		ns
t_{AW}	Address Set-Up to Write End	65		75		90		100		110		ns
t_{HA}	Address Hold from Write End	0		5		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	0		5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	55		65		75		85		95		ns
t_{SD}	Data Set-Up to Write End	30		35		40		45		50		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		25		30		35		40		45	ns

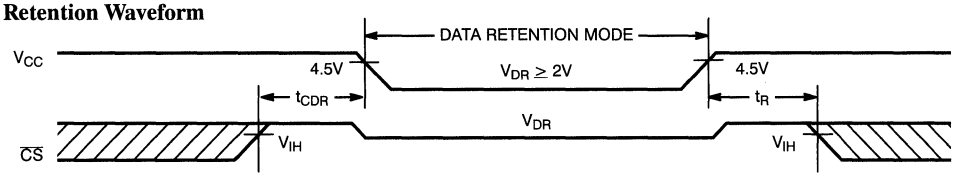
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Test Conditions	Commercial		Industrial		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2		2		V
I_{CCDR3}	Data Retention Current	$V_{DR} = 3.0V$, $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		50		150	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		5		5		ms

Notes:

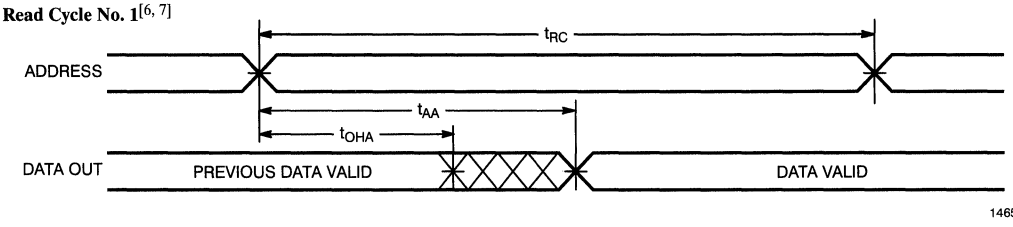
3. $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Guaranteed, not tested.

Data Retention Waveform

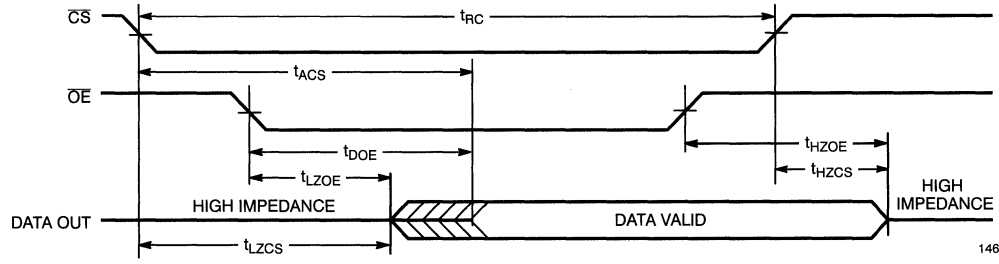


Switching Waveforms

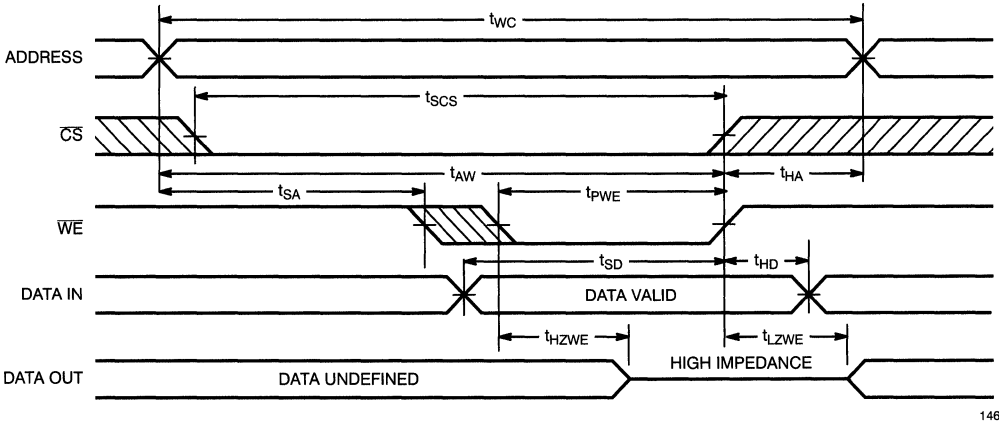
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[4]

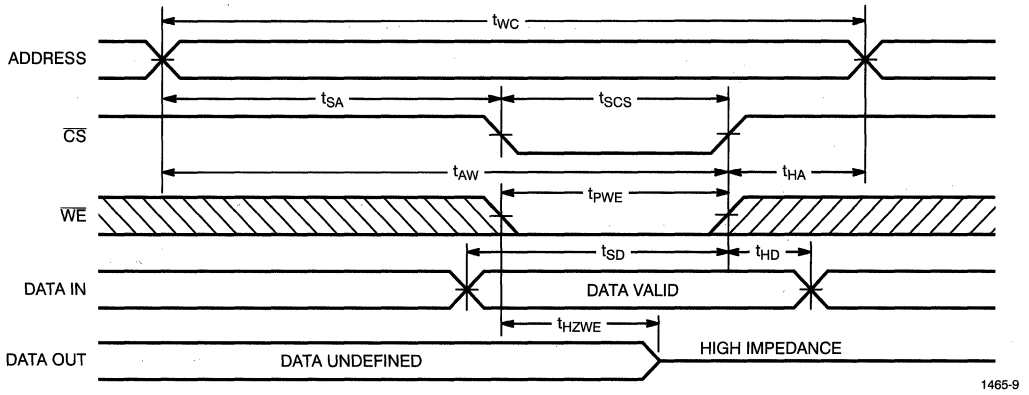


Notes:

6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[4, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM1465PD–70C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–70C			
85	CYM1465PD–85C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–85C			
	CYM1465PD–85I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–85I			
100	CYM1465PD–100C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–100C			
	CYM1465PD–100I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–100I			
120	CYM1465PD–120C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–120C			
	CYM1465PD–120I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–120I			
150	CYM1465PD–150C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD–150C			
	CYM1465PD–150I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD–150I			

Document #: 38–M–00036–D

CYM1471
CYM1481

1024K x 8 SRAM Module
2048K x 8 SRAM Module

Features

- **High-density 8-/16-megabit SRAM modules**
- **High-speed CMOS SRAMs**
  - **Access time of 85 ns**
- **Low active power**
  - **605 mW (max.), 2M x 8**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Small footprint SIP**
  - **PCB layout area of 0.72 sq. in.**
- **2V data retention (L version)**

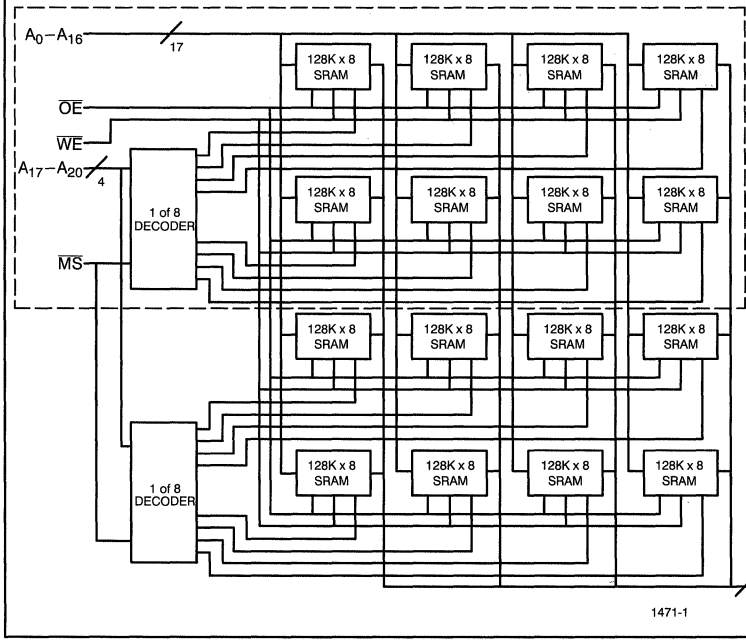
Functional Description

The CYM1471 and CYM1481 are high-performance 8-megabit and 16-megabit static RAM modules organized as 1024K words (1471) or 2048K words (1481) by 8 bits. These modules are constructed from eight (1471) or sixteen (1481) 128K x 8 SRAMs in plastic surface-mount packages on an epoxy laminate board with pins. On-board decoding selects one of the SRAMs from the high-order address lines, keeping the remaining devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs $\overline{MS}$ and $\overline{OE}$ active LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

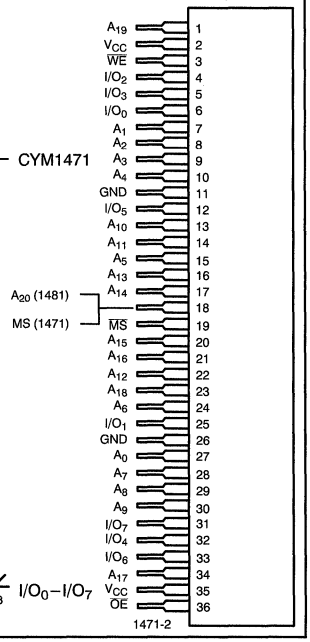
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration

SIP
Top View



Selection Guide

	CYM1471			CYM1481		
Maximum Access Time (ns)	85	100	120	85	100	120
Maximum Operating Current (mA)	95	95	95	110	110	110
Maximum Standby Current (mA)	32	32	32	64	64	64

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential ..... −0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.3V to +7.0V

DC Input Voltage ..... −0.3V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

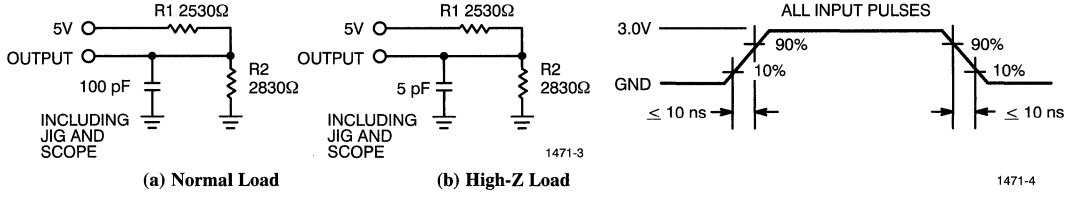
Parameter	Description	Test Conditions		1471 Min.	1471 Max.	1481 Min.	1481 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 1.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $\overline{MS}$ ≤ V_{IL}, I_{OUT} = 0 mA			95		110	mA
I_{SB1}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			32		64	mA
I_{SB2}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V	Standard		16		32	mA
			L Version −100,−120		250		500	µA
			L Version −85		800		1600	µA

Capacitance[1]

Parameter	Description	Test Conditions	CYM1471 Max.	CYM1481 Max.	Unit
C_{INA}	Input Capacitance (A_{0-16}, $\overline{OE}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	75	125	pF
C_{INB}	Input Capacitance (A_{17-20}, $\overline{MS}$)		25	25	pF
C_{OUT}	Output Capacitance		95	165	pF

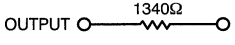
Note:
1. Tested on a sample basis.

AC Test Loads and Waveforms



(a) Normal Load (b) High-Z Load

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2]

Parameter	Description	1471–85 1481–85		1471–100 1481–100		1471–120 1481–120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	85		100		120		ns
t_{AA}	Address to Data Valid		85		100		120	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{AMS}	$\overline{MS}$ LOW to Data Valid		85		100		120	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		45		50		60	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		30		35		45	ns
t_{LZMS}	$\overline{MS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZMS}	$\overline{MS}$ HIGH to High Z[3, 4]		30		35		45	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	85		100		120		ns
t_{SMS}	$\overline{MS}$ LOW to Write End	75		90		100		ns
t_{AW}	Address Set-Up to Write End	75		90		100		ns
t_{HA}	Address Hold from Write End	7		7		7		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	65		75		85		ns
t_{SD}	Data Set-Up to Write End	35		40		45		ns
t_{HD}	Data Hold from Write End	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		30		35		40	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

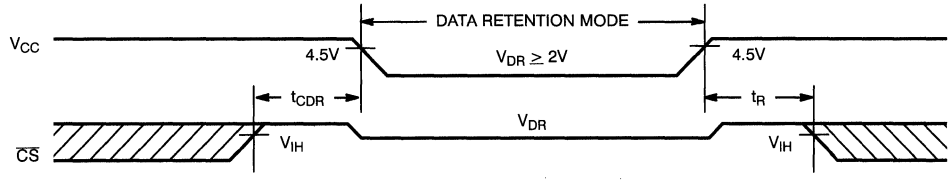
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1471–85		1471–100 1471–120		1481–85		1481–100 1481–120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2		2		2		2		V
I_{CCDR}	Data Retention Current	V_{DR} = 3.0V, $\overline{MS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		400		125		800		250	µA
t_{CDR}[6]	Chip Deselect to Data Retention Time		0		0		0		0		ns
t_R	Operation Recovery Time		5		5		5		5		ns

Notes:

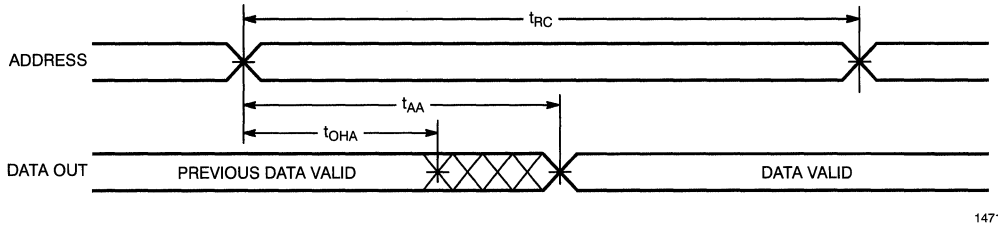
2. Test conditions assume signal transition time of 10 µs or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of 1 TTL load, and 100-pF load capacitance.
3. t_{HZOE}, t_{HZMS}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. Guaranteed, not tested.

Data Retention Waveform

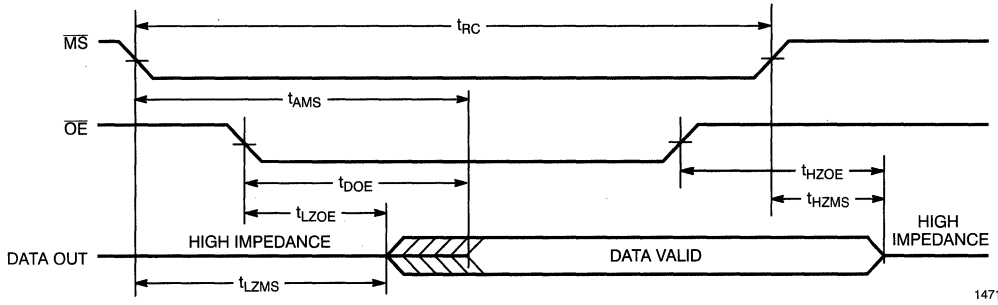


Switching Waveforms

Read Cycle No. 1[7, 8]



Read Cycle No. 2[8, 9]



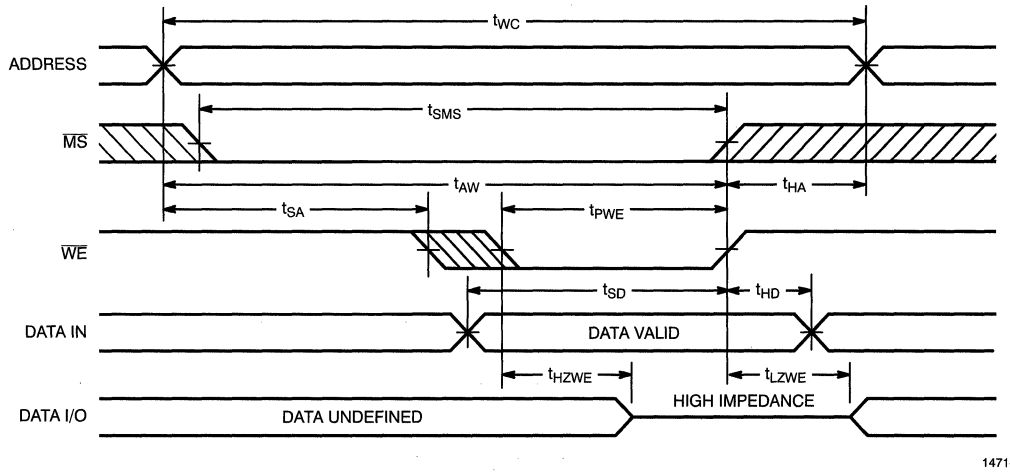
Notes:
7. Device is continuously selected. $\overline{OE}$, $\overline{MS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{MS}$ transition LOW
9. $\overline{WE}$ is HIGH for read cycle.

Truth Table

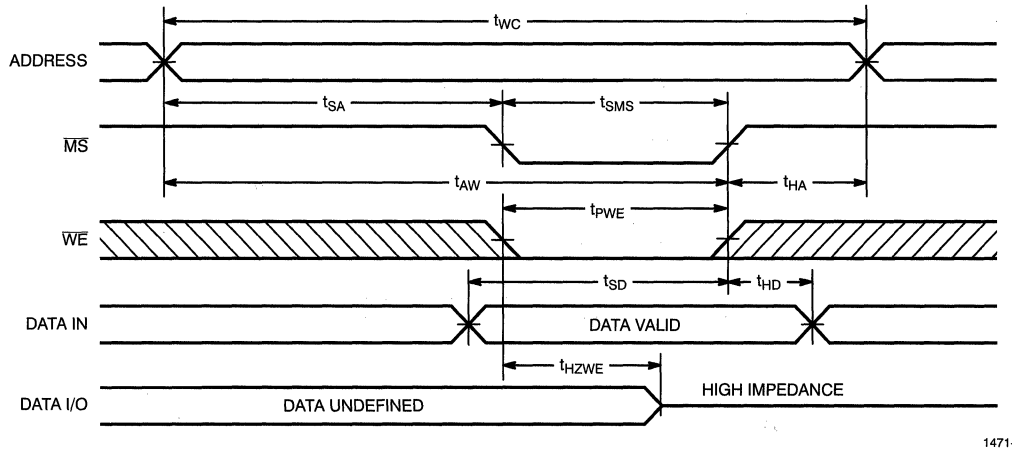
$\overline{MS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Switching Waveforms (continued)

Write Cycle No. 1[5, 10]



Write Cycle No. 2[5, 10, 11]



Notes:
10. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
11. If $\overline{MS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
85	CYM1471PS–85C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS–85C			
100	CYM1471PS–100C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS–100C			
120	CYM1471PS–120C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS–120C			

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
85	CYM1481PS–85C	PS06	36-Pin SIP Module	Commercial
	CYM1481LPS–85C			
100	CYM1481PS–100C	PS06	36-Pin SIP Module	Commercial
	CYM1481LPS–100C			
120	CYM1481PS–120C	PS06	36-Pin SIP Module	Commercial
	CYM1481LPS–120C			

Document #: 38–M–00041–B

CYM1622

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 15 ns**
- **Low active power**
  - **2.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pinout compatible with CYM1611**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **0.68 sq. in.**

Functional Description

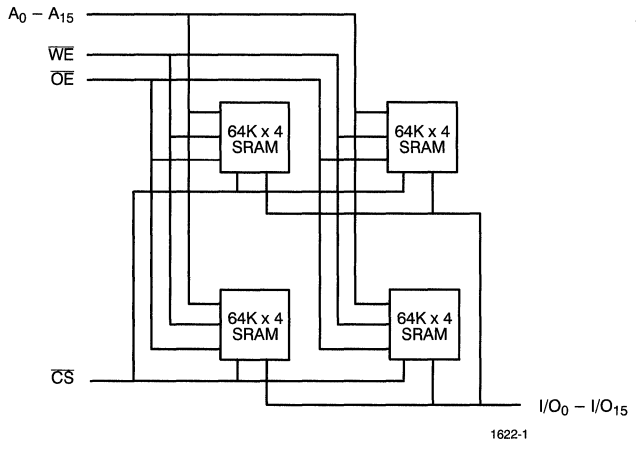
The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 64K x 4 static RAMs mounted onto a vertical substrate with pins. The pinout of this module is compatible with another Cypress module (CYM1611) to maximize system flexibility.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

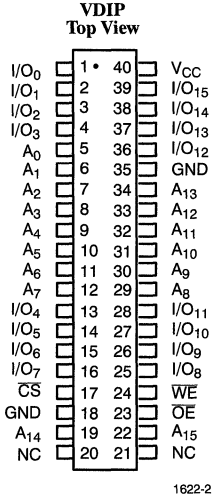
Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1622–15	1622–20	1622–25	1622–30	1622–35	1622–45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	600	500	400	400	400	400
Maximum Standby Current (mA)	80	80	140	140	140	140

Shaded areas contain preliminary information.

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +80°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1622−15		1622−20		1622−25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		600		500		400	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		160		160		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		80		80		80	mA

Shaded areas contain preliminary information.

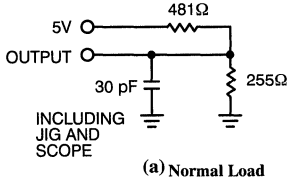
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		15	pF

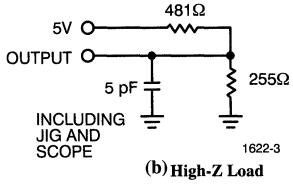
Notes:

1. V_{IL}(min.) = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms

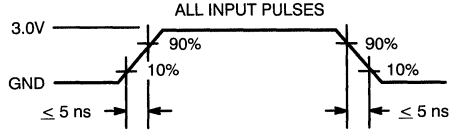


(a) Normal Load



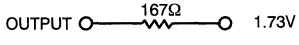
(b) High-Z Load

1622-3



1622-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1622–15		1622–20		1622–25		1622–30		1622–35		1622–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		10		15		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	0		0		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		6		8		15		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0	25	0	30	0	35	0	45	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		15		20		25		30		35		45	ns
WRITE CYCLE[5]														
t_{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		15		20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	8		12		15		20		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	7	0	10	0	15	0	15	0	15	0	20	ns

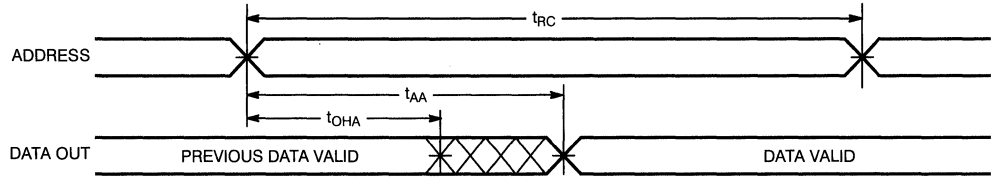
Shaded areas contain preliminary information.

Notes:

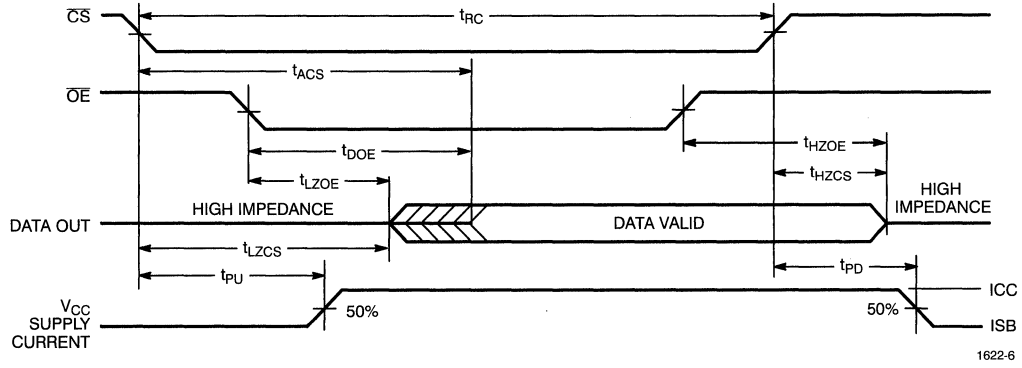
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

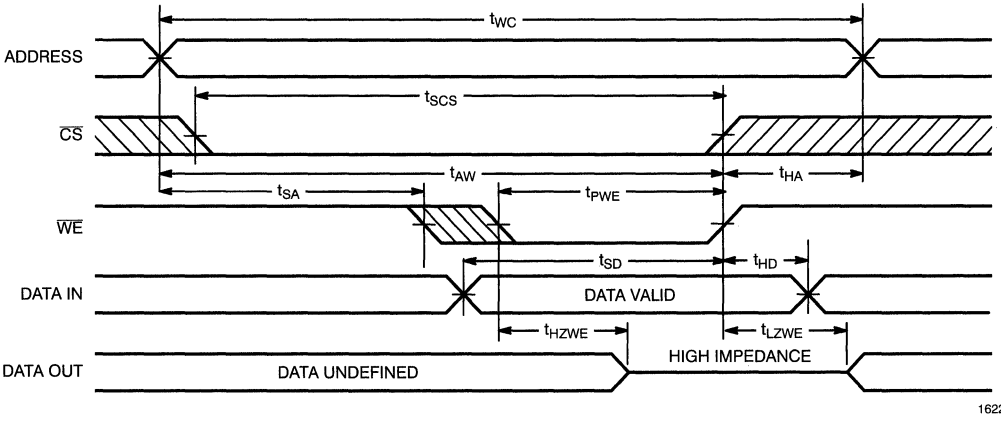
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]



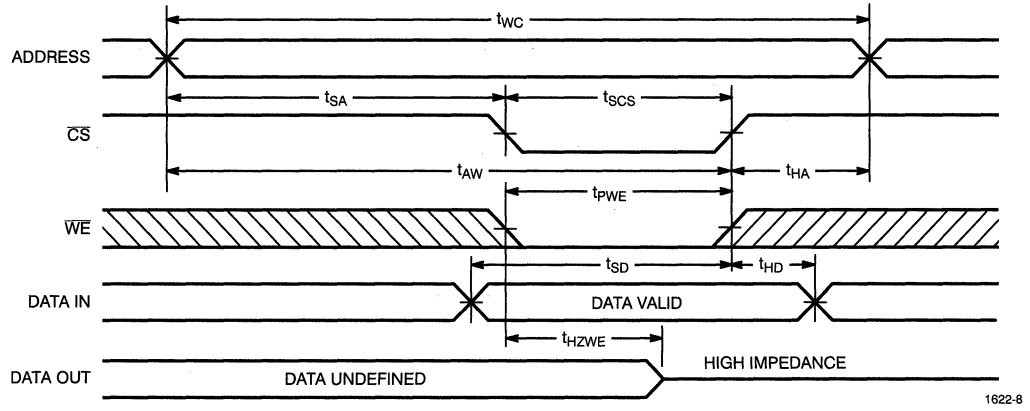
Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1622PV-15C	PV04	40-Pin Plastic VDIP Module	Commercial
20	CYM1622PV-20C	PV04	40-Pin Plastic VDIP Module	Commercial
25	CYM1622PV-25C	PV04	40-Pin Plastic VDIP Module	Commercial
30	CYM1622PV-30C	PV04	40-Pin Plastic VDIP Module	Commercial
35	CYM1622PV-35C	PV04	40-Pin Plastic VDIP Module	Commercial
45	CYM1622PV-45C	PV04	40-Pin Plastic VDIP Module	Commercial

Shaded areas contain preliminary information.

Document #: 38-M-00001-D

CYM1720

32K x 24 Static RAM Module

Features

- **High-density 768-kilobit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 15 ns**
- **56-pin, 0.5-inch-high ZIP package**
- **Low active power**
  - **1.8W (max. for t_{AA} = 25 ns)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **0.66 sq. in.**

Functional Description

The CYM1720 is a high-performance 768-kilobit static RAM module organized as 32K words by 24 bits. This module is constructed using three 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

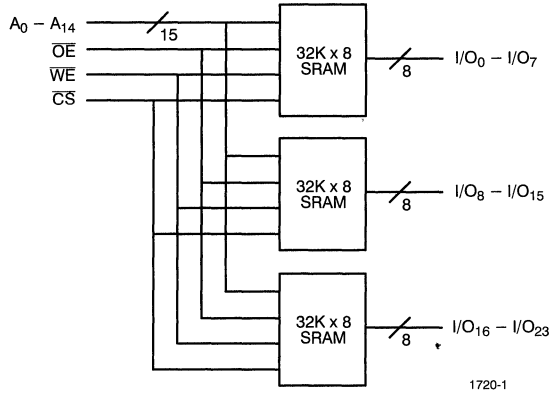
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking the chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

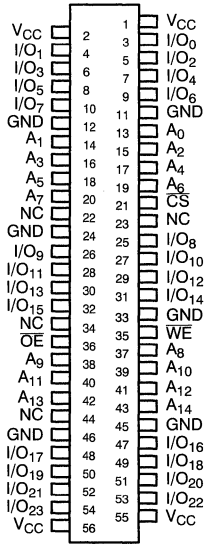
3

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1720–15	1720–20	1720–25	1720–30	1720–35
Maximum Access Time (ns)	15	20	25	30	35
Maximum Operating Current (mA)	450	450	330	330	330
Maximum Standby Current (mA)	120	120	60	60	60

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1720−15, 20		CYM1720−25, 30, 35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		450		330	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		120		60	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		90		60	mA

Shaded area contains preliminary information.

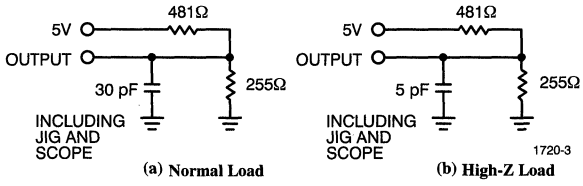
Capacitance[2]

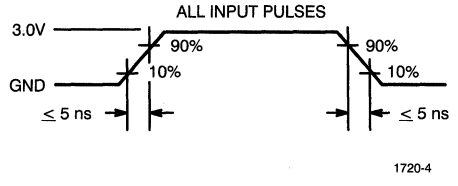
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Notes:

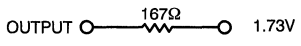
1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1720–15		1720–20		1720–25		1720–30		1720–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		30		35		ns
t_{AA}	Address to Data Valid		15		20		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		10		15		18	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		6		8		10		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		5		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		6		8		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		15		20		25		25		30	ns
WRITE CYCLE[6]												
t_{WC}	Write Cycle Time	15		20		25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		20		25		30		ns
t_{AW}	Address Set-Up to Write End	10		12		20		25		30		ns
t_{HA}	Address Hold from Write End	1		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	1		2		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		20		25		25		ns
t_{SD}	Data Set-Up to Write End	9		10		12		18		18		ns
t_{HD}	Data Hold from Write End	1		2		2		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	8	0	8	0	10	0	15	0	15	ns

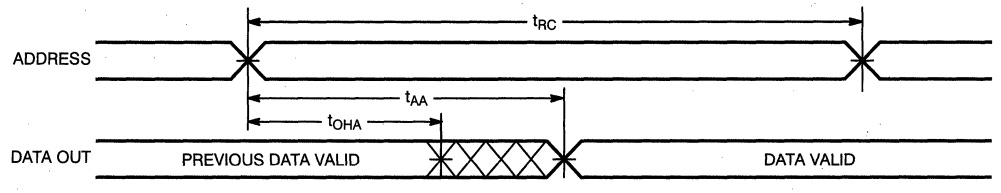
Shaded area contains preliminary information.

Notes:

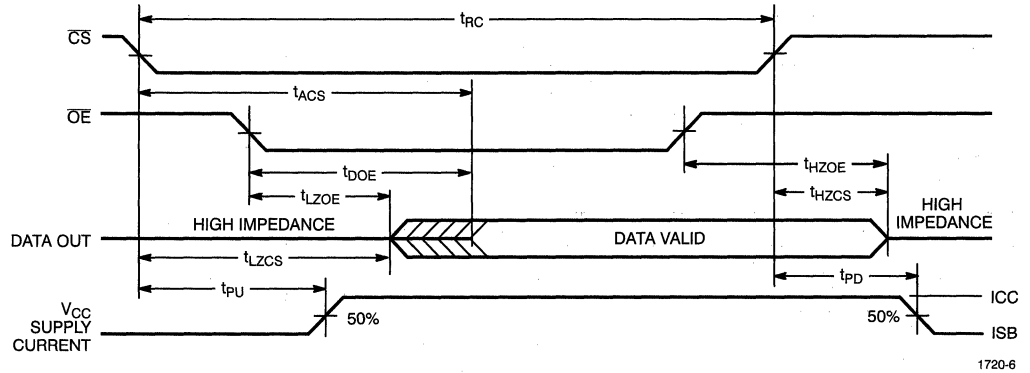
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZOE}, t_{HZCS}, and t_{LZCE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

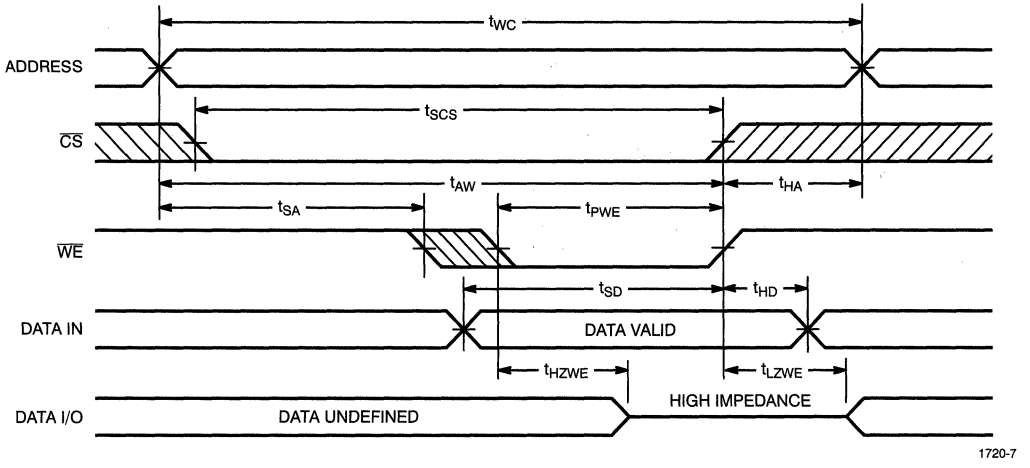
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



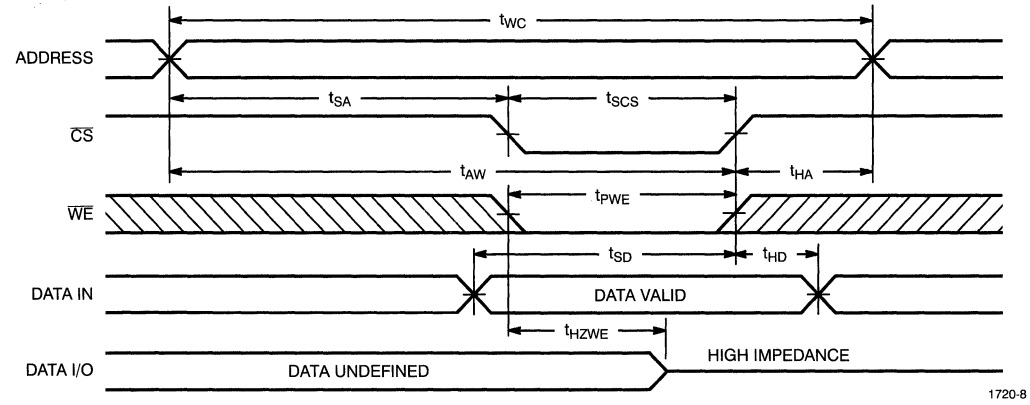
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1720PZ–15C	PZ05	56-Pin ZIP Module	Commercial
20	CYM1720PZ–20C	PZ05	56-Pin ZIP Module	Commercial
25	CYM1720PZ–25C	PZ05	56-Pin ZIP Module	Commercial
30	CYM1720PZ–30C	PZ05	56-Pin ZIP Module	Commercial
35	CYM1720PZ–35C	PZ05	56-Pin ZIP Module	Commercial

Document #: 38–M–00021–A

64K x 24 Static RAM Module

Features

- **High-density 1.5M SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **56-pin, 0.5-inch-high ZIP package**
- **Low active power**
  - **2.8W (max. for t_{AA} = 25 ns)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **1.05 sq. in.**

Functional Description

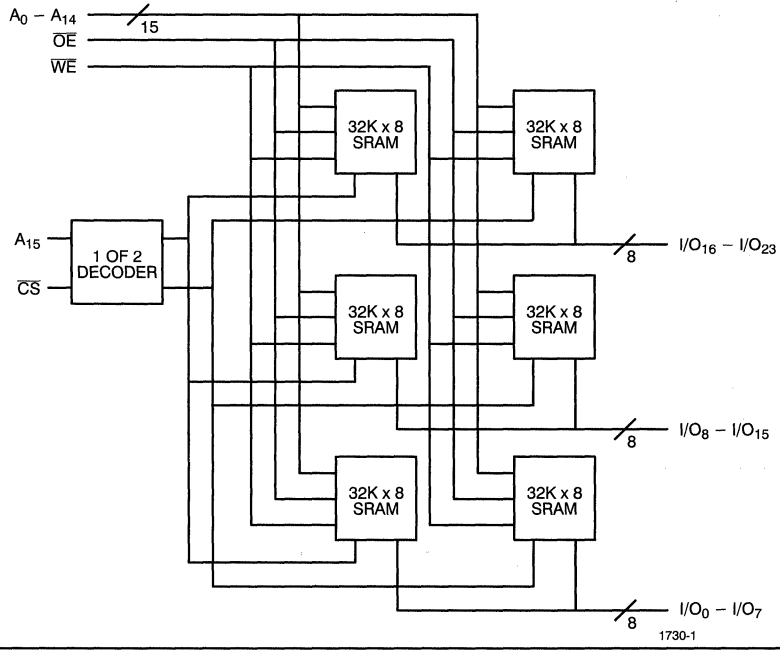
The CYM1730 is a high-performance 1.5M static RAM module organized as 64K words by 24 bits. This module is constructed using six 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

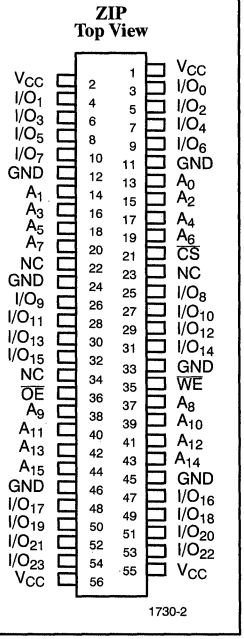
Reading the device is accomplished by taking the chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1730–25	1730–30	1730–35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	510	510	510
Maximum Standby Current (mA)	180	180	180

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		510	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		180	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		180	mA

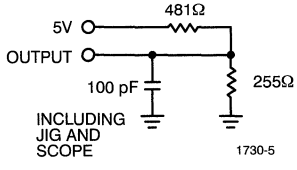
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		20	pF

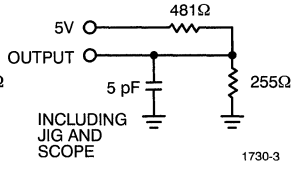
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

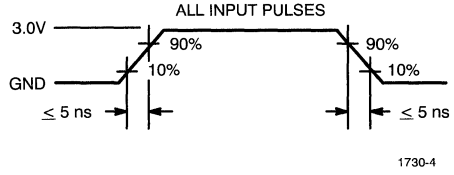
AC Test Loads and Waveforms



(a) Normal Load



(b) High-Z Load



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[3]

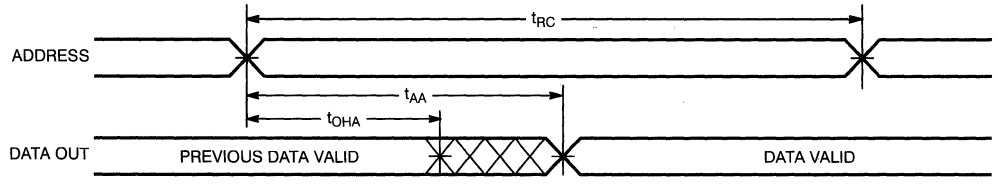
Parameter	Description	1730–25		1730–30		1730–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		15		15	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	22		25		30		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		23		25		ns
t_{SD}	Data Set-Up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	10	0	10	0	15	ns

Notes:

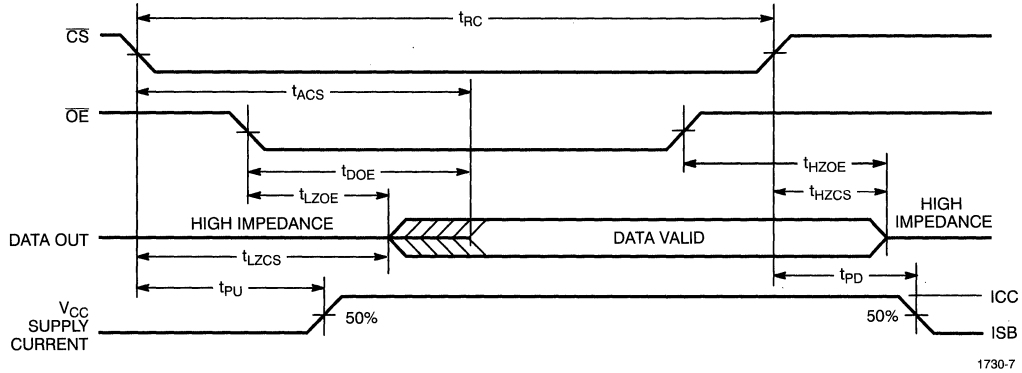
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZOE}, t_{HZCS}, and t_{LZCE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

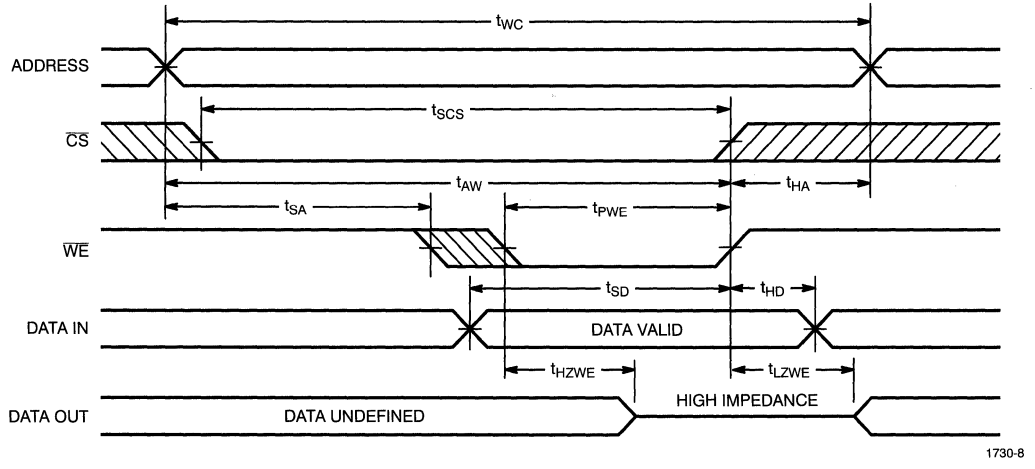
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



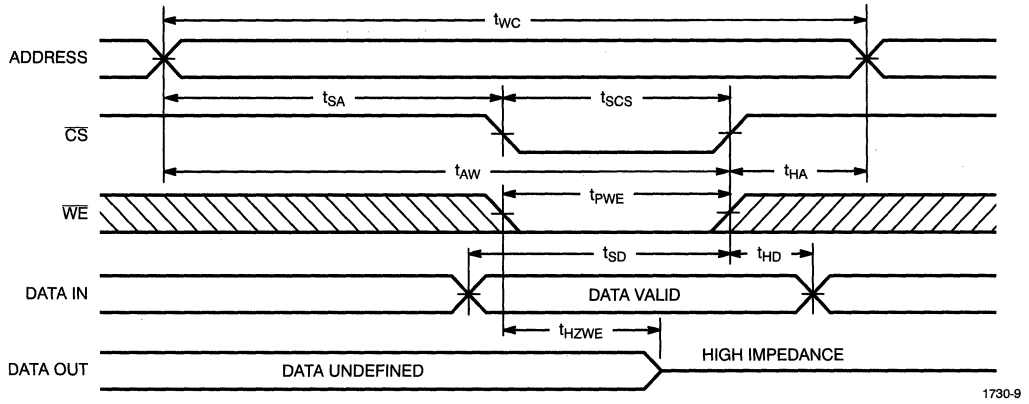
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1730PZ–25C	PZ07	56-Pin ZIP Module	Commercial
30	CYM1730PZ–30C	PZ07	56-Pin ZIP Module	Commercial
35	CYM1730PZ–35C	PZ07	56-Pin ZIP Module	Commercial

Document #: 38–M–00049–A

CYM1821

16K x 32 Static RAM Module

Features

- **High-density 512-Kbit SRAM module**
- **32-bit standard footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power**
  - **4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **1.0 sq. in.**
- **JEDEC-compatible pinout**

Functional Description

The CYM1821 is a high-performance 512-Kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 SRAM SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

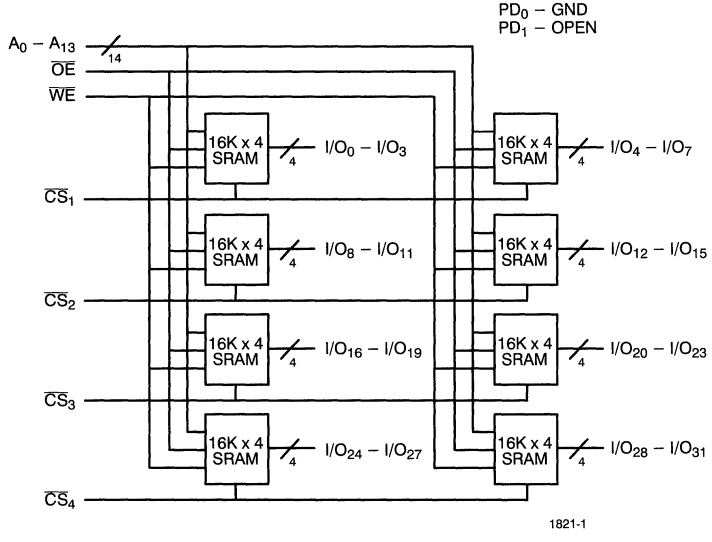
Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

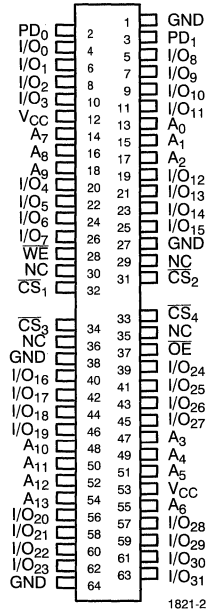
3

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1821–12	1821–15	1821–20	1821–25	1821–35	1821–45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	960	960	720	720	720	720
Maximum Standby Current (mA)	450	450	160	160	160	160

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1821−12 1821−15		1821−20 1821−25 1821−35 1821−45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		450		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_N$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		160		160	mA

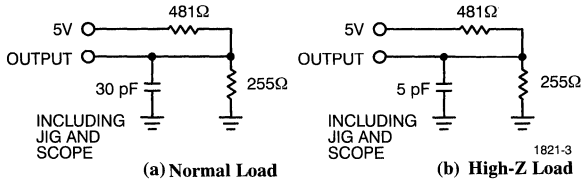
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance (ADDR, $\overline{OE}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		35	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

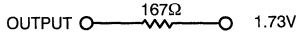
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



(a) Normal Load (b) High-Z Load

Equivalent to: THÉVENIN EQUIVALENT



3

Switching Characteristics Over the Operating Range[4]

Parameter	Description	1821–12		1821–15		1821–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	7	0	7	0	7	ns

Notes:

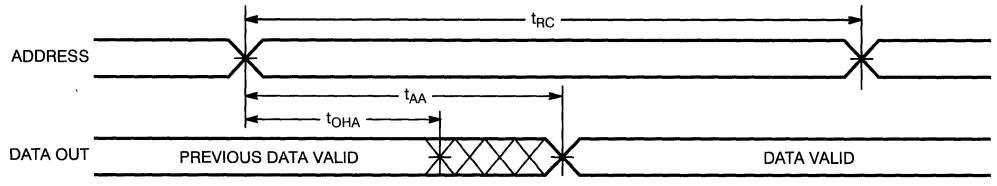
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[4]

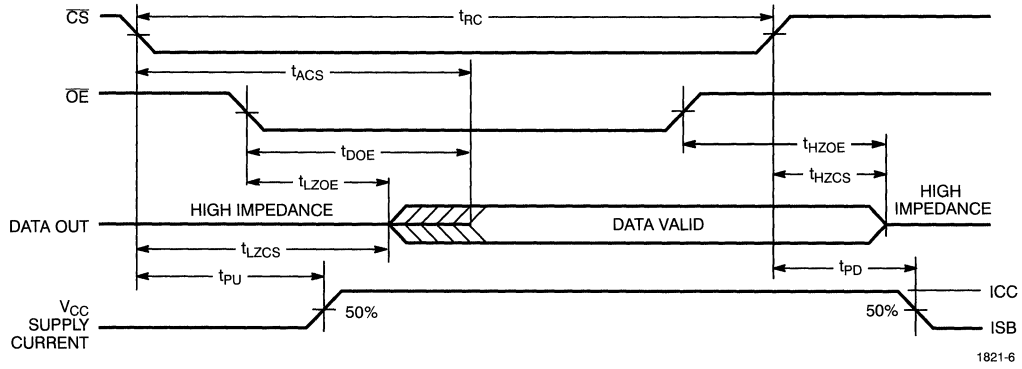
Parameter	Description	1821–25		1821–35		1821–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	5		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		10		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	7	0	10	0	15	ns

Switching Waveforms

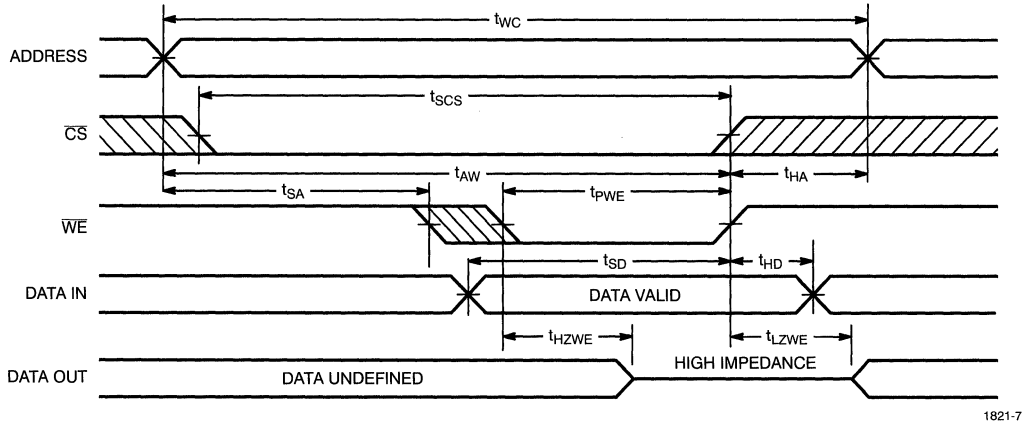
Read Cycle No. 1[8, 9]



Read Cycle No. 2 ($\overline{WE}$ Controlled)[8, 10]



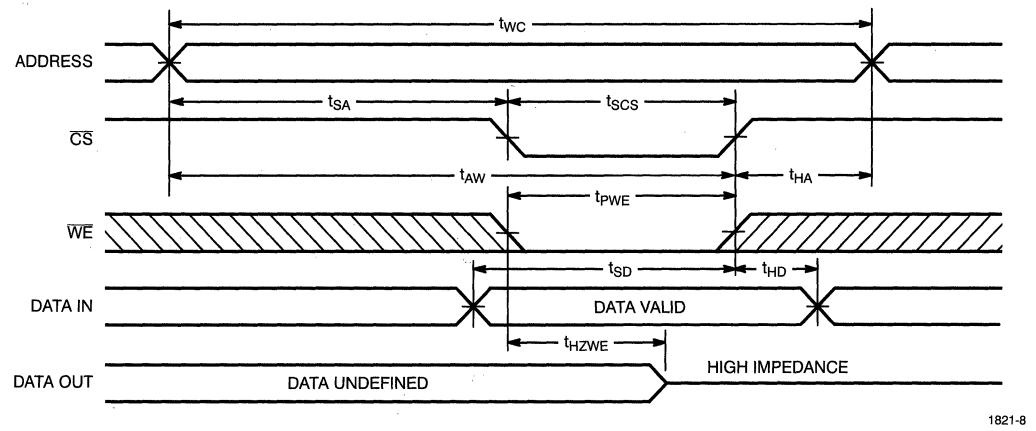
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
12	CYM1821PM–12C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–12C	PZ01	64-Pin Plastic ZIP Module	
15	CYM1821PM–15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1821PM–20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1821PM–25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–25C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1821PM–35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1821PM–45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1821PZ–45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38–M–00015–E

32K x 32 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **66-pin, 1.1-inch-square PGA package**
- **Low active power**
  - **3.3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

The CYM1828 is a very high performance 1-megabit static RAM module organized as 32K words by 32 bits. The module is constructed using four 32K x 8 static RAMs mounted onto a multilayer ceramic substrate. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW.

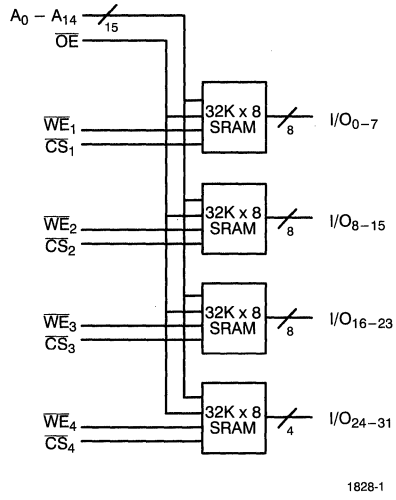
Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip selects LOW while write enable remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins.

The data input/output pins remain in a high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

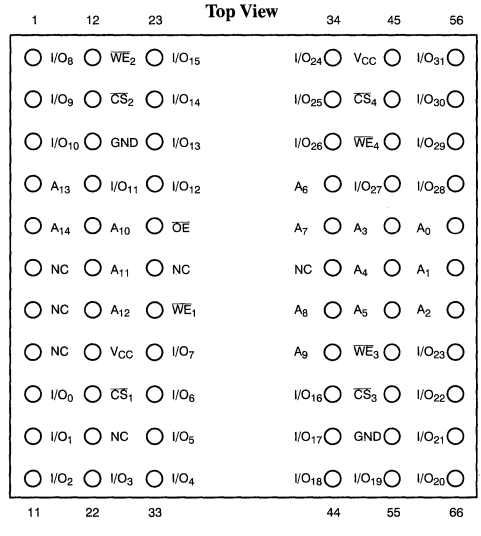
3

Logic Block Diagram



Pin Configuration

PGA
Top View



Selection Guide

		1828–25	1828–30	1828–35	1828–45	1828–55	1828–70
Maximum Access Time (ns)		25	30	35	45	55	70
Maximum Operating Current (mA)	Commercial	600	600	600	600	600	600
	Military			600	600	600	600
Maximum Standby Current (mA)	Commercial	200	200	200	200	200	200
	Military			200	200	200	200

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +150°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		1828 Min.	1828 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	µA
I_{CCx32}	V_{CC} Operating Supply Current by 32 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			600	mA
			L Version		400	
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			360	mA
			L Version		230	
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			240	mA
			L Version		145	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			200	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V			100	mA

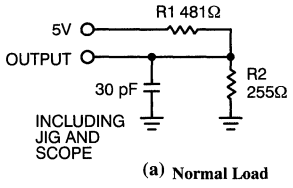
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		20	pF

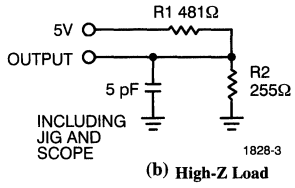
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms

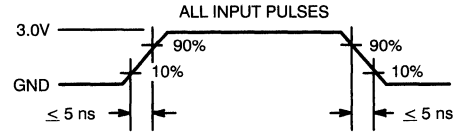


(a) **Normal Load**



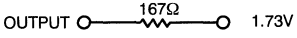
(b) **High-Z Load**

1828-3



1828-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1828–25		1828–30		1828–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		17		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		15		15		25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-Up to Write End	15		20		17		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	20	0	30	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[3]

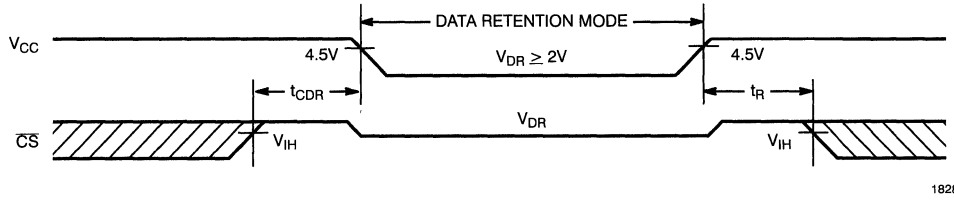
Parameter	Description	1828–45		1828–55		1828–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		25		30		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		25		30		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	40		45		55		ns
t_{AW}	Address Set-Up to Write End	40		45		55		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	25		30		40		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	30	0	30	0	30	ns

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1828		Unit
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2		V
I_{CCDR3}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $V_{DR} = 3.0V$		320	µA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0		ns
t_R[7]	Operation Recovery Time		t_{RC}		ns

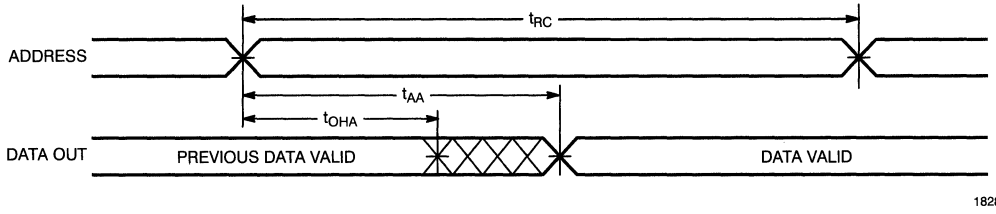
Note:
7. Guaranteed, not tested.

Data Retention Waveform

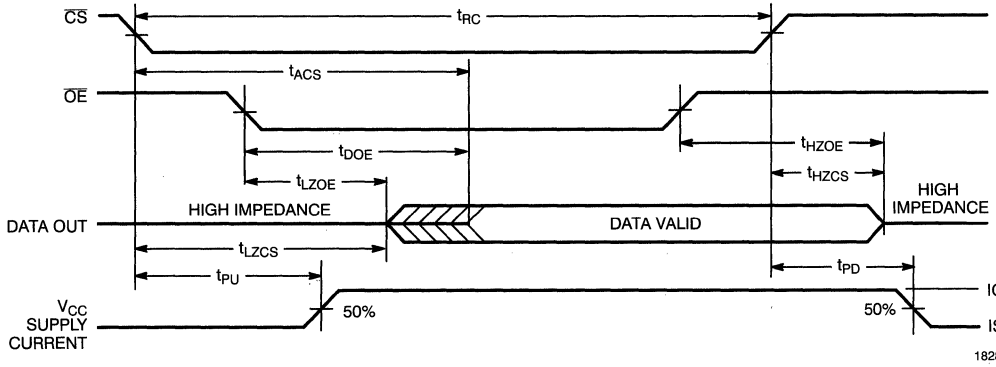


Switching Waveforms

Read Cycle No. 1[8, 9]



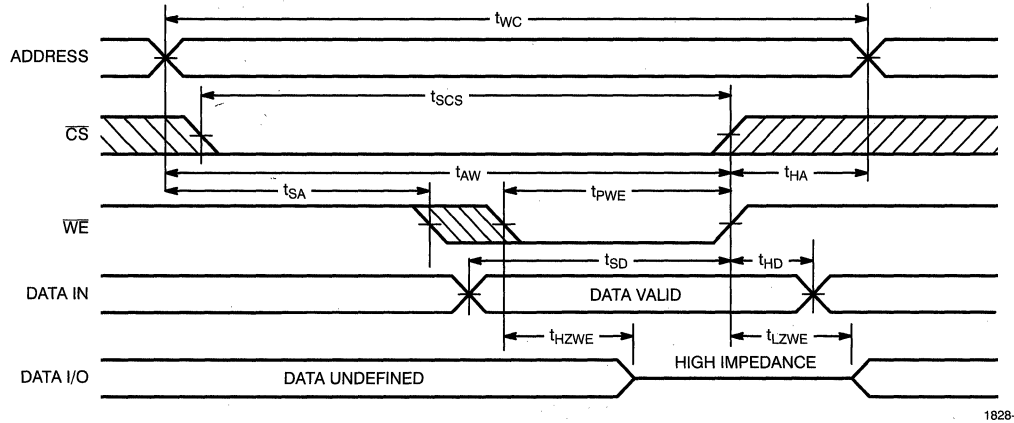
Read Cycle No. 2[8, 10]



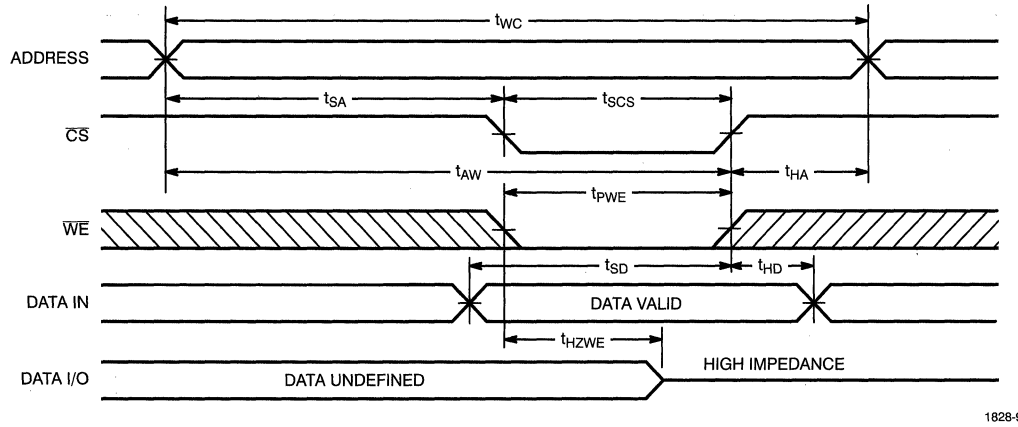
Notes:
8. $\overline{WE}_N$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 11]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 11, 12]



Notes:

11. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
12. If $\overline{CS}_N$ goes HIGH simultaneously with $\overline{WE}_N$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS_N}$	$\overline{OE}$	$\overline{WE_N}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1828HG–25C	HG01	66-Pin PGA Module	Commercial
30	CYM1828HG–30C	HG01	66-Pin PGA Module	Commercial
35	CYM1828HG–35C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–35C	HG01	66-Pin PGA Module	
	CYM1828HG–35MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–35MB	HG01	66-Pin PGA Module	
45	CYM1828HG–45C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–45C	HG01	66-Pin PGA Module	
	CYM1828HG–45MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–45MB	HG01	66-Pin PGA Module	
55	CYM1828HG–55C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–55C	HG01	66-Pin PGA Module	
	CYM1828HG–55MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–55MB	HG01	66-Pin PGA Module	
70	CYM1828HG–70C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG–70C	HG01	66-Pin PGA Module	
	CYM1828HG–70MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG–70MB	HG01	66-Pin PGA Module	

Document #: 38–M–00042

CYM1831

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **32-bit standard footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 15 ns**
- **Low active power**
  - **5.3W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **1.2 sq. in.**

Functional Description

The CYM1831 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

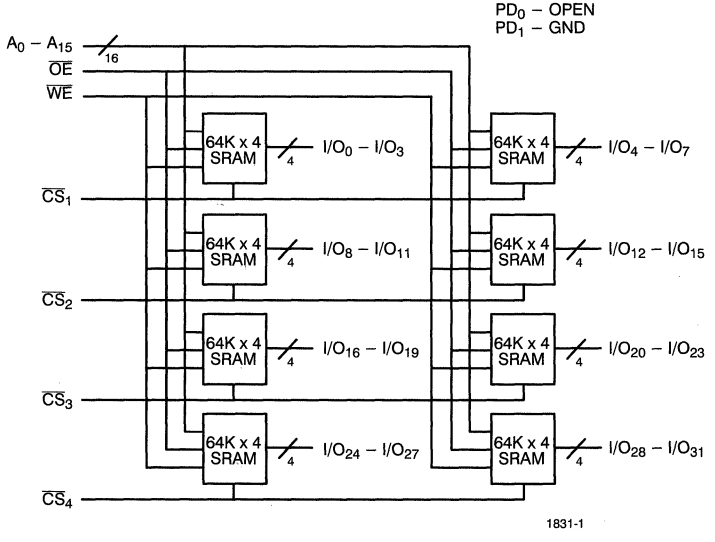
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW or the appropriate chip selects are HIGH.

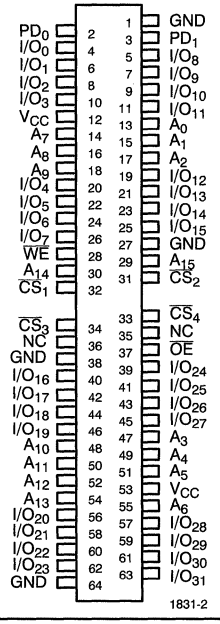
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration

ZIP/SIMM
Top View



Selection Guide

	1831–15	1831–20	1831–25	1831–30	1831–35	1831–45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	1120	960	720	720	720	720
Maximum Standby Current (mA)	160	160	160	160	160	160

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1831−15		1831−20		1831−25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}		1120		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max., $\overline{CS}_N$ ≥ V_{IH}, Min. Duty Cycle = 100%		320		320		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max., $\overline{CS}_N$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		160		160		160	mA

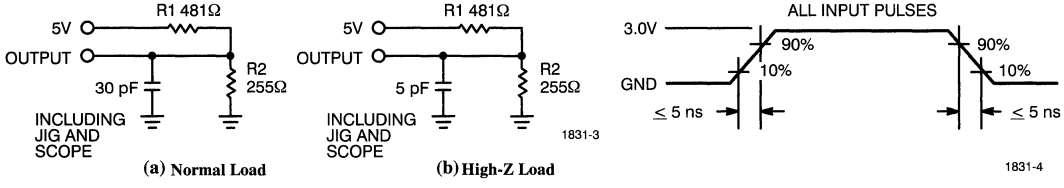
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance (A_0 − A_{15}, $\overline{WE}$, $\overline{OE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		15	pF
C_{OUT}	Output Capacitance		20	pF

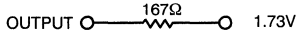
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

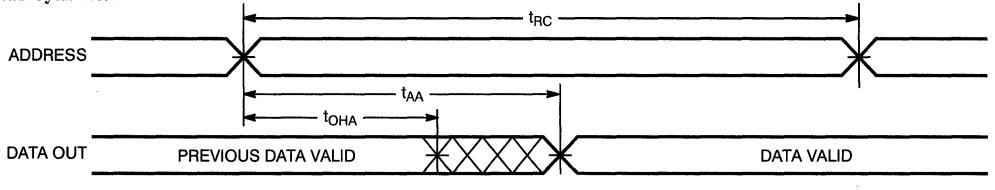
Parameter	Description	1831–15		1831–20		1831–25		1831–30		1831–35		1831–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		15		20		20		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ LOW to High Z		8		10		15		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	0		0		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		6		8		13		15		20		20	ns
WRITE CYCLE[6]														
t_{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		15		20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	8		12		15		15		20		20		ns
t_{HD}	Data Hold from Write End	2		2		2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	7	0	10	0	13	0	15	0	20	0	20	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.

Switching Waveforms

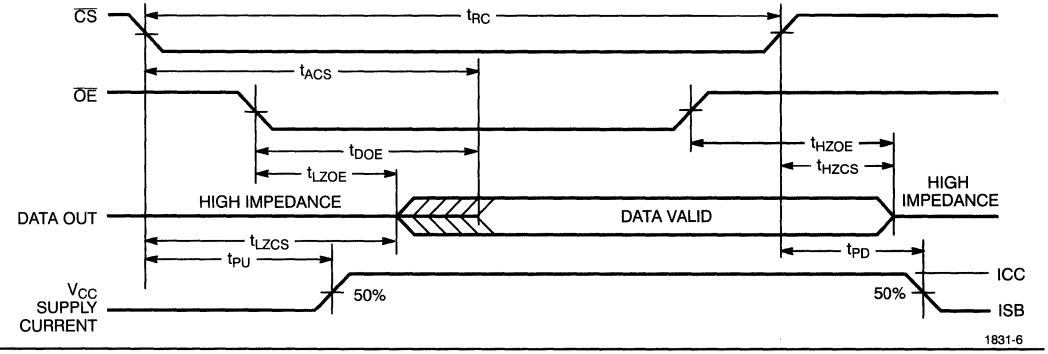
Read Cycle No. 1[7, 8]



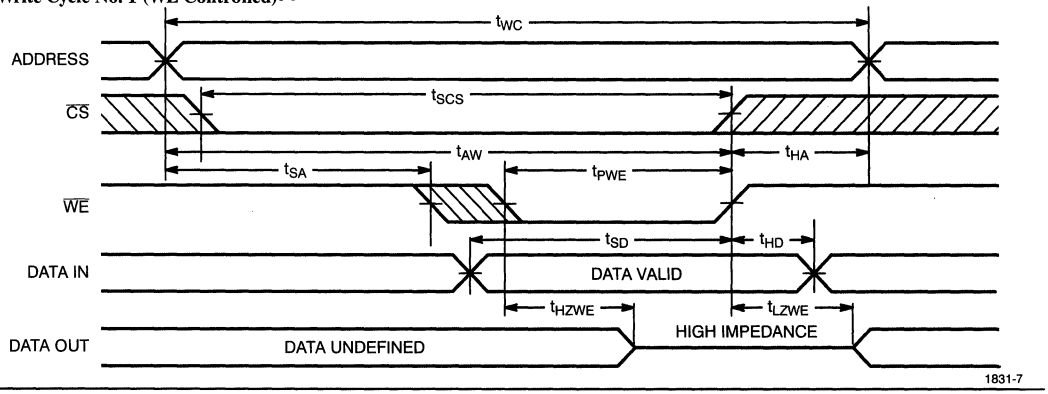
1831-5

Switching Waveforms

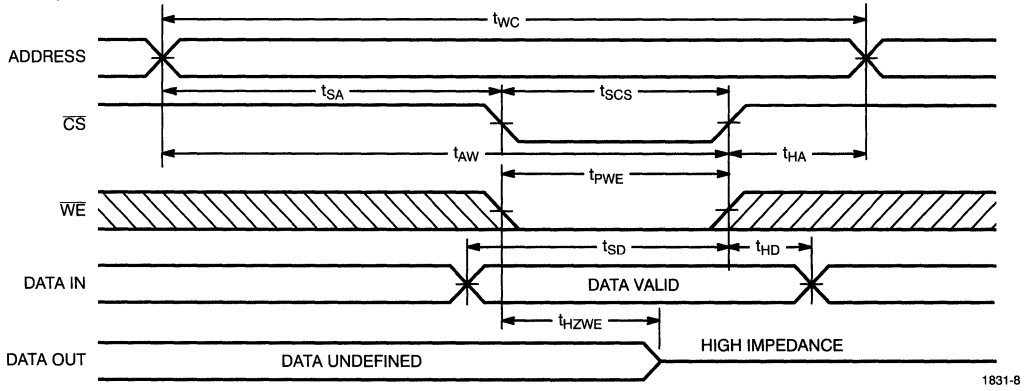
Read Cycle No. 2[7, 9]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Notes:

9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1831PM–15C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–15C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–15C	PZ01	64-Pin Plastic ZIP Module	
20	CYM1831PM–20C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–20C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–20C	PZ01	64-Pin Plastic ZIP Module	
25	CYM1831PM–25C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–25C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–25C	PZ01	64-Pin Plastic ZIP Module	
30	CYM1831PM–30C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–30C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–30C	PZ01	64-Pin Plastic ZIP Module	
35	CYM1831PM–35C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–35C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–35C	PZ01	64-Pin Plastic ZIP Module	
45	CYM1831PM–45C	PM01	64-Pin Plastic SIMM Module	Commercial
	CYM1831PN–45C	PN01	64-Pin Plastic Angled SIMM Module	
	CYM1831PZ–45C	PZ01	64-Pin Plastic ZIP Module	

Document #: 38–M–00018–E

CYM1832

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **5.4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .5 in.**
- **Small PCB footprint**
  - **1.0 sq. in.**

Functional Description

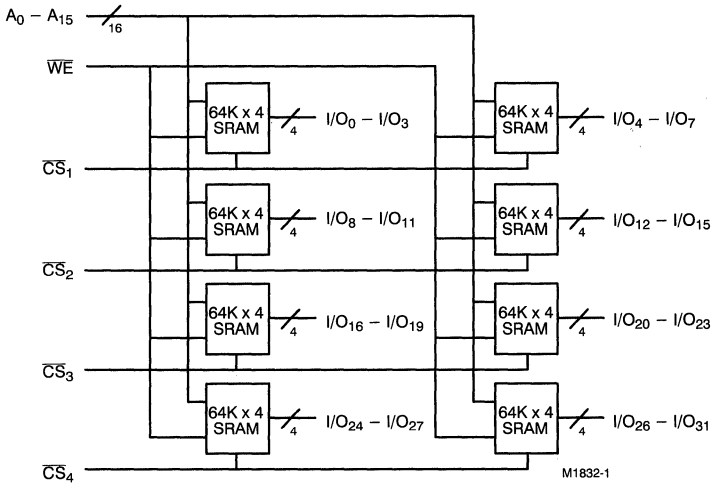
The CYM1832 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$, and $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the chip select ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

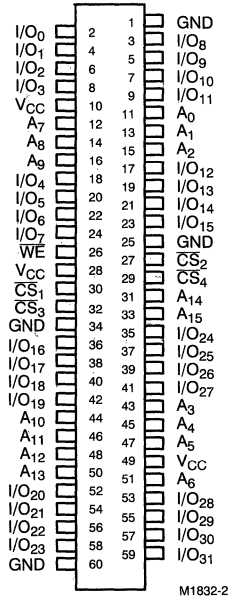
The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1832–25	1832–35	1832–45	1832–55
Maximum Access Time (ns)	25	35	45	55
Maximum Operating Current (mA)	980	980	980	980
Maximum Standby Current (mA)	240	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −45°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1832 Min.	CYM1832 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−100	+100	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N \le V_{IL}$		980	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_N \ge V_{IH}$, Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_N \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V or $V_{IN} \le 0.2V$		120	mA

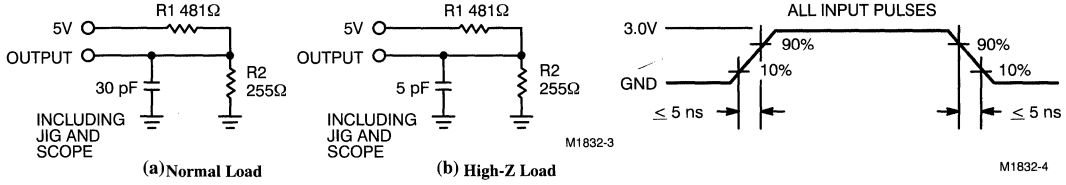
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance (A_X, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	60	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		25	pF
C_{OUT}	Output Capacitance		15	pF

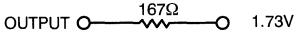
Notes:

1. V_{IL}(min.) = −3.0V for pulse widths less than 20 ns.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

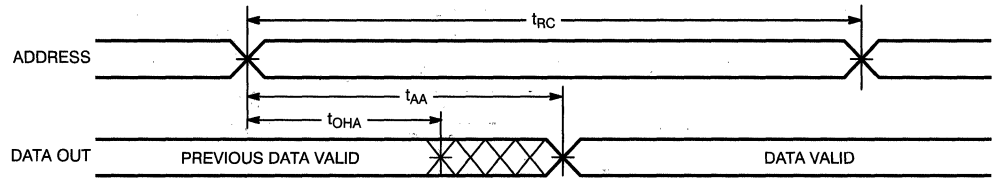
Parameter	Description	1832–25		1832–35		1832–45		1832–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	2		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]	0	15	0	25	0	30	0	30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45		55	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		40		45		ns
t_{AW}	Address Set-Up to Write End	20		30		35		45		ns
t_{HA}	Address Hold from Write End	2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		3		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		30		35		45		ns
t_{SD}	Data Set-Up to Write End	15		20		25		35		ns
t_{HD}	Data Hold from Write End	3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	0	20	0	30	ns

Notes:

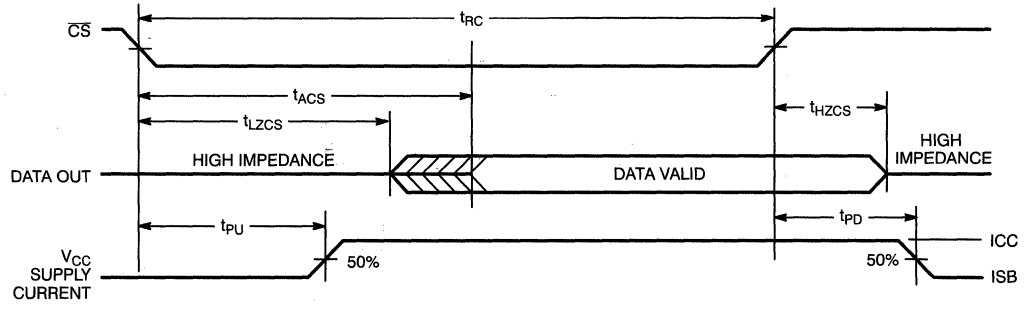
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

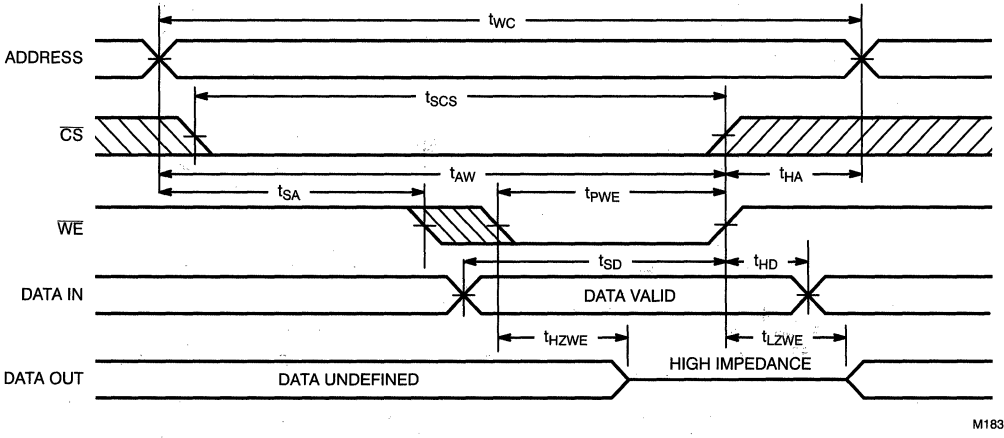
Read Cycle No. 1[8, 9]



Read Cycle No. 2[9, 10]



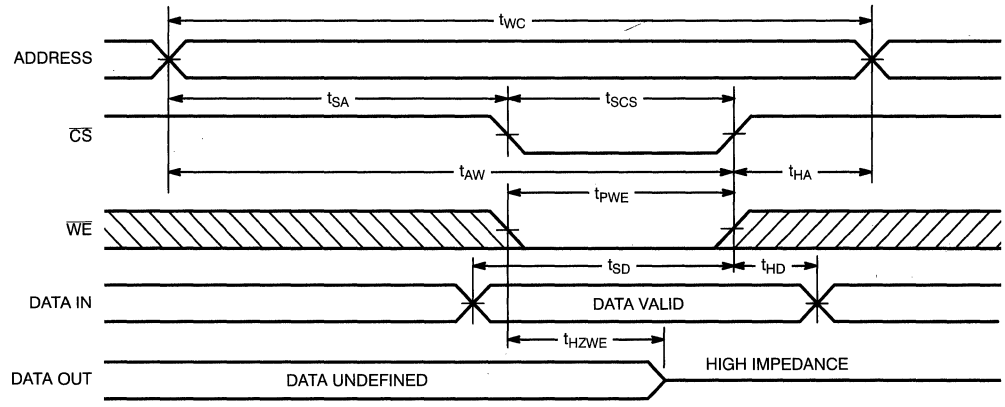
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Notes:
8. Device is continuously selected, $\overline{CS} = V_{IL}$.
9. $\overline{WE}$ is HIGH for read cycle.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11]



M1832-8

Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1832PZ–25C	PZ02	60-Pin Plastic ZIP Module	Commercial
35	CYM1832PZ–35C	PZ02	60-Pin Plastic ZIP Module	Commercial
45	CYM1832PZ–45C	PZ02	60-Pin Plastic ZIP Module	Commercial
55	CYM1832PZ–55C	PZ02	60-Pin Plastic ZIP Module	Commercial

Document #: 38–M–00019–A

CYM1836

128K x 32 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **32-bit standard footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 15 ns**
- **Low active power**
  - **2.6W (max.) at 20 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.57 in.**
- **Small PCB footprint**
  - **0.78 sq. in.**
- **Available in SIMM, ZIP format. SIMM suitable for vertical or angled sockets.**

Functional Description

The CYM1836 is a high-performance 4-megabit static RAM module organized as 128K words by 32 bits. This module is constructed from four 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

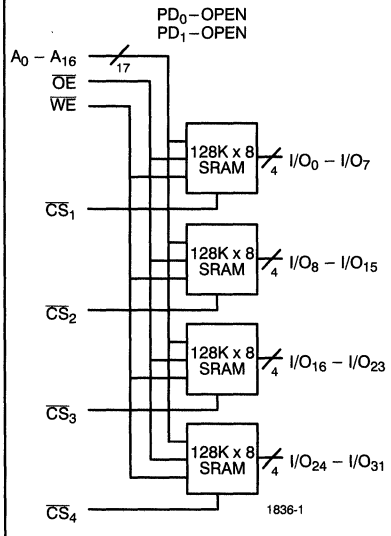
Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking the chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

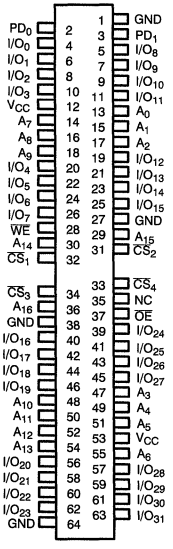
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration

ZIP/SIMM
Top View



Selection Guide

	1836–15	1836–20	1836–25	1836–30	1836–35	1836–45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	760	480	480	480	480	480
Maximum Standby Current (mA)	180	100	100	100	100	100

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commereial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1836−15		1836−20, 25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		760		480	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		180		100	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		60		28	mA

Shaded area contains preliminary information.

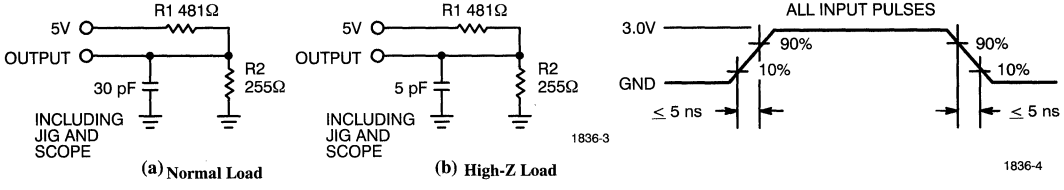
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[3]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40/20	pF
C_{OUT}	Output Capacitance		15	pF

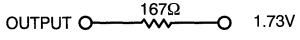
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis
3. 20 pF on $\overline{CS}$, 40 pF all others

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

Parameter	Description	1836–15		1836–20		1836–25		1836–30		1836–35		1836–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		8		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		7		8		10		11		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		7		10		10		13		15		18	ns
WRITE CYCLE[7]														
t_{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	12		15		15		18		20		25		ns
t_{AW}	Address Set-Up to Write End	12		15		15		18		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		18		20		25		ns
t_{SD}	Data Set-Up to Write End	7		10		10		13		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	6	0	8	0	10	0	15	0	15	0	18	ns

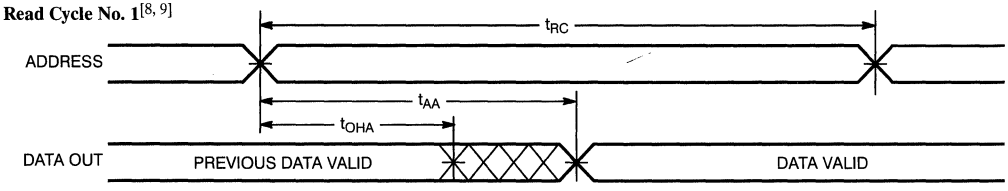
Shaded area contains preliminary information.

Notes:

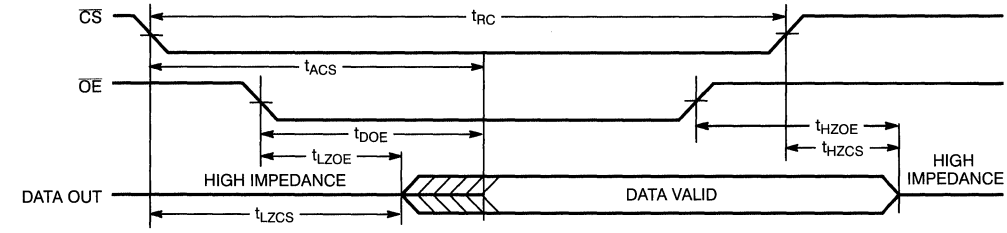
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

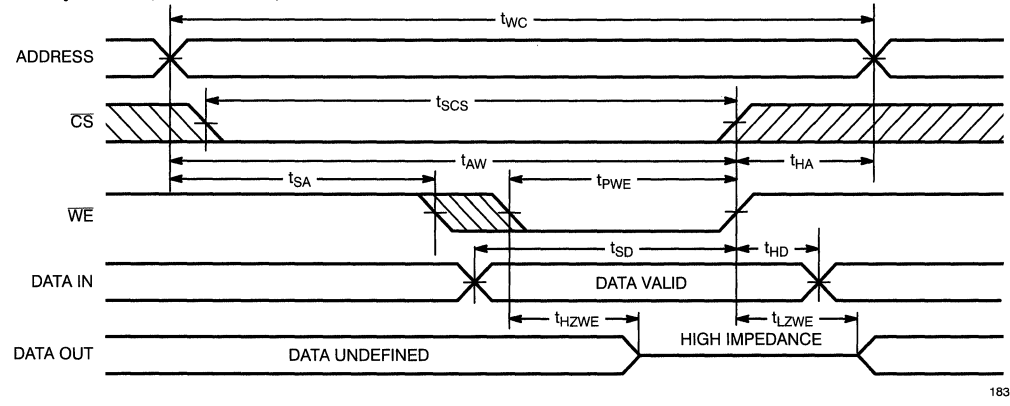
Read Cycle No. 1[8, 9]



Read Cycle No. 2[8, 10]



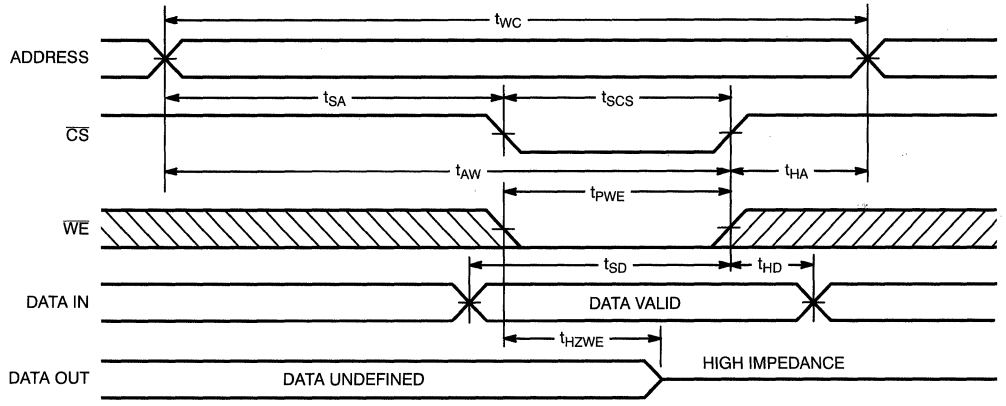
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11]



Truth Table

$\overline{CS}_N$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information[12]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1836PM-15C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-15C	PZ08	64-Pin ZIP Module	
20	CYM1836PM-20C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-20C	PZ08	64-Pin ZIP Module	
25	CYM1836PM-25C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-25C	PZ08	64-Pin ZIP Module	
30	CYM1836PM-30C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-30C	PZ08	64-Pin ZIP Module	
35	CYM1836PM-35C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-35C	PZ08	64-Pin ZIP Module	
45	CYM1836PM-45C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-45C	PZ08	64-Pin ZIP Module	

Shaded area contains preliminary information.

Notes:

11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
12. 64-pin SIMM suitable for use in angled SIMM aplications.

Document #: 38-M-00050-B

128K x 32 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  — Access time of 25 ns
- **66-pin, 1.1-inch-square PGA package**
- **Low active power**
  — 4.0W (max.)
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

The CYM1838 is a very high performance 4-megabit static RAM module organized as 128K words by 32 bits. The module is constructed using four 128K x 8 static RAMs mounted onto a multilayer ceramic substrate. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW.

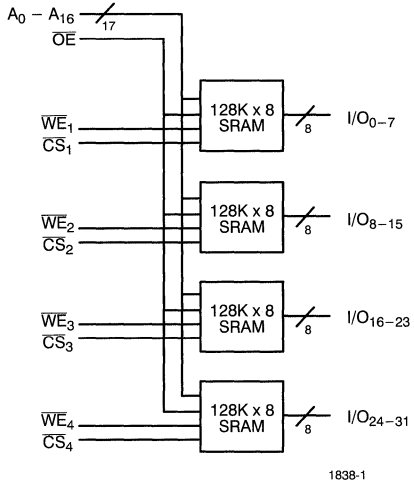
Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking chip selects LOW while write enable remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins.

The data input/output pins remain in a high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

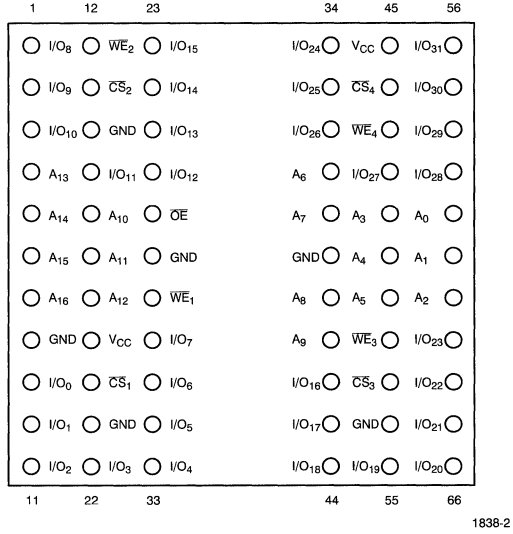
3

Logic Block Diagram



Pin Configuration

PGA
Top View



Selection Guide

		1838–25	1838–30	1838–35
Maximum Access Time (ns)		25	30	35
Maximum Operating Current (mA)	Commercial	720	720	720
	Military	720	720	720
Maximum Standby Current (mA)	Commercial	240	240	240
	Military	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +150°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1838 Min.	1838 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{CCx32}	V_{CC} Operating Supply Current by 32 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		720	mA
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		480	mA
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		360	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		40	mA

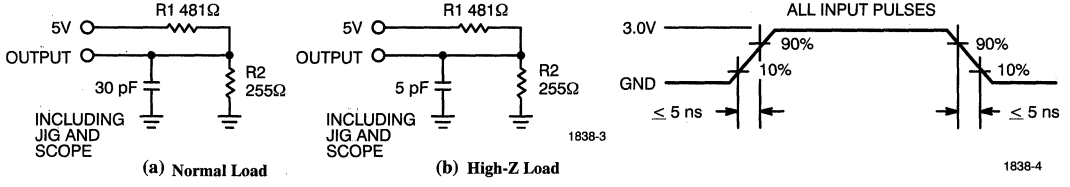
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		50	pF

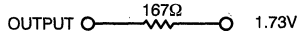
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

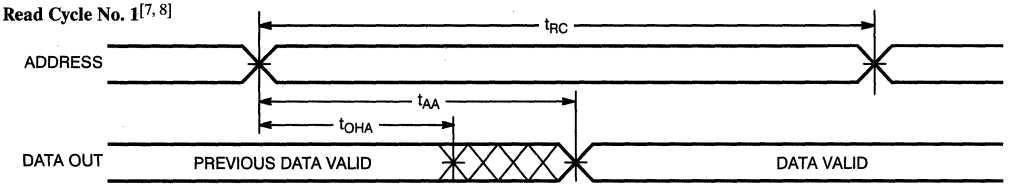
Parameter	Description	1838–25		1838–30		1838–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		13		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		15		18		20	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	17		21		25		ns
t_{SD}	Data Set-Up to Write End	12		13		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	10	0	12	0	15	ns

Notes:

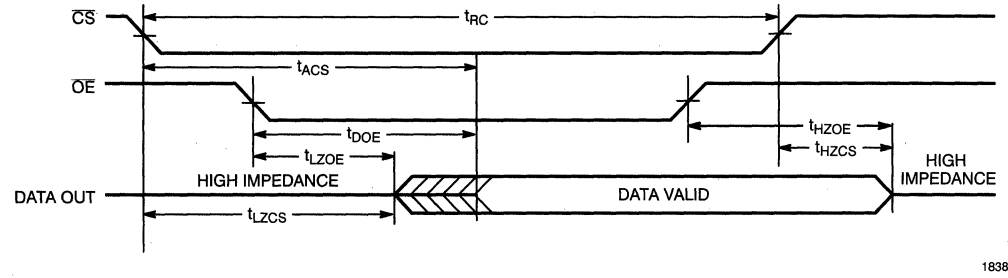
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

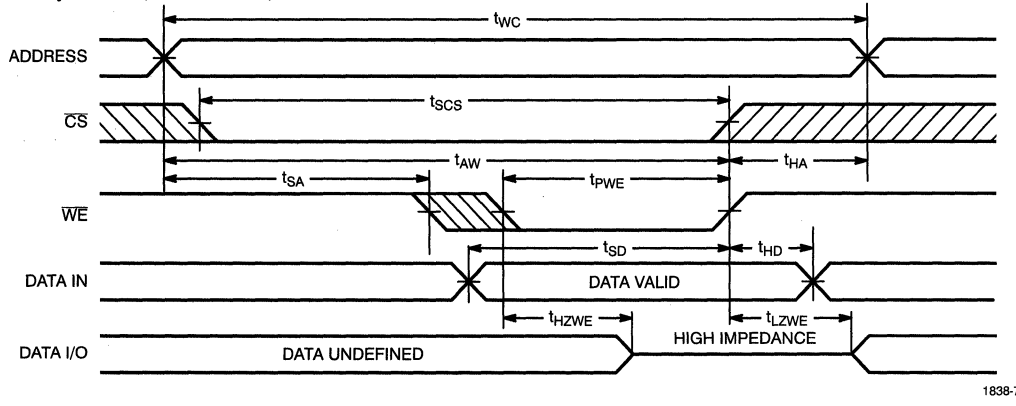
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



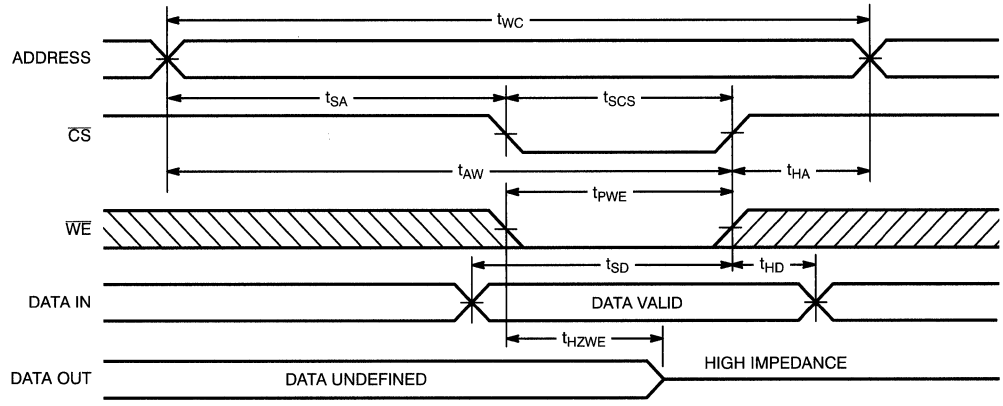
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}_N$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{OE}$	$\overline{WE}_N$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1838HG–25C	HG01	66-Pin PGA Module	Commercial
	CYM1838HG–25M	HG01	66-Pin PGA Module	Military
	CYM1838HG–25MB	HG01	66-Pin PGA Module	
30	CYM1838HG–30C	HG01	66-Pin PGA Module	Commercial
	CYM1838HG–30M	HG01	66-Pin PGA Module	Military
	CYM1838HG–30MB	HG01	66-Pin PGA Module	
35	CYM1838HG–35C	HG01	66-Pin PGA Module	Commercial
	CYM1838HG–35M	HG01	66-Pin PGA Module	Military
	CYM1838HG–35MB	HG01	66-Pin PGA Module	

Document #: 38–M–00046–B

CYM1840

256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Independent byte and word controls**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .350 in.**
- **Small PCB footprint**
  - **1.8 sq. in.**

Functional Description

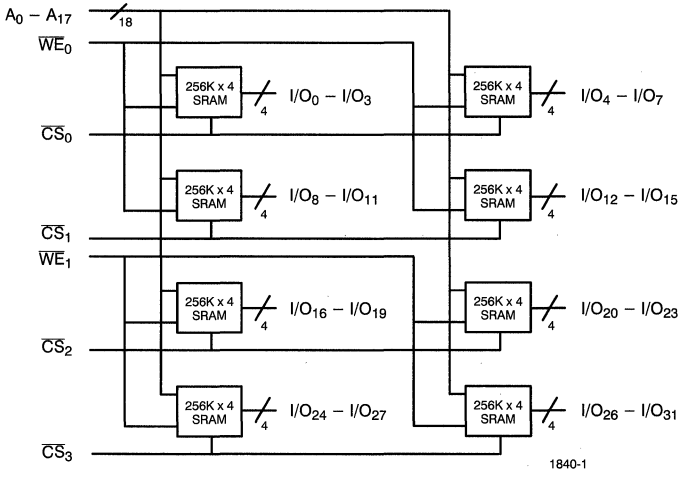
The CYM1840 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate with pins. Four chip selects ($\overline{CS_0}$, $\overline{CS_1}$, $\overline{CS_2}$, and $\overline{CS_3}$) are used to independently enable the four bytes. Two write enables ($\overline{WE_0}$ and $\overline{WE_1}$) are used to independently write to either the upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through the proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins ($\overline{I/O_X}$) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}$) LOW, while write enables ($\overline{WE}$) remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O}$).

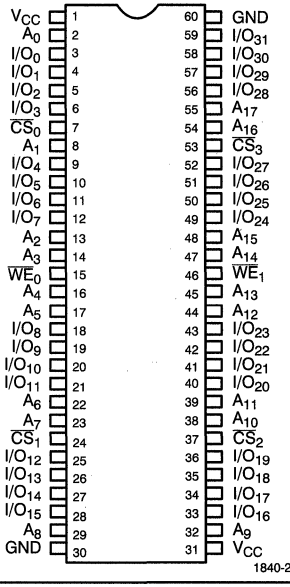
The data input/output pins stay in the high-impedance state when write enables ($\overline{WE}$) are LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration

DIP
Top View



Selection Guide

	1840–20	1840–25	1840–30	1840–35	1840–45	1840–55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	1120	1120	1120	1120	1120
Maximum Standby Current (mA)	320	320	320	320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied (PD) ..... −10°C to +85°C

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1840		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	+50	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_X$ ≤ V_{IL}		1120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_X$ ≥ V_{IH}, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_X$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		160	mA

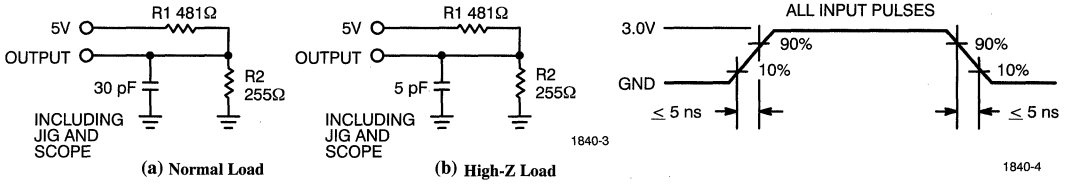
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance, Address Pins	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	100	pF
C_{INB}	Input Capacitance, I/O Pins		30	pF
C_{OUT}	Output Capacitance		30	pF

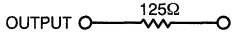
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1840–20		1840–25		1840–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	18		20		25		ns
t_{AW}	Address Set-Up to Write End	18		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Notes:

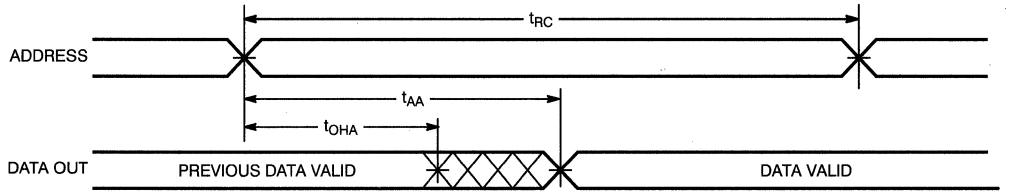
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3] (continued)

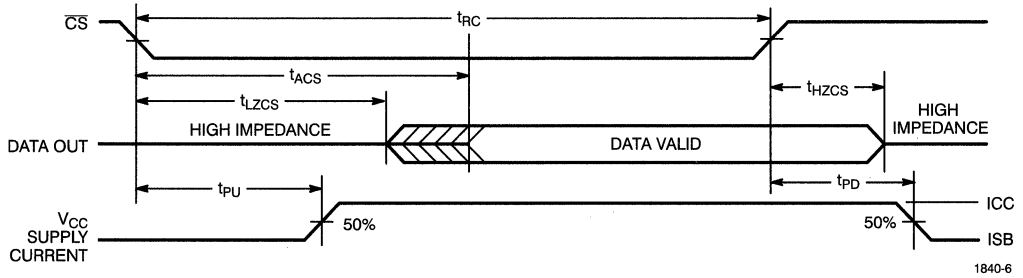
Parameter	Description	1840–35		1840–45		1840–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		25		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	6		6		6		ns
t_{SA}	Address Set-Up to Write Start	6		6		6		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		30		40		ns
t_{SD}	Data Set-Up to Write End	25		30		35		ns
t_{HD}	Data Hold from Write End	6		6		6		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	25	0	25	0	25	ns

Switching Waveforms

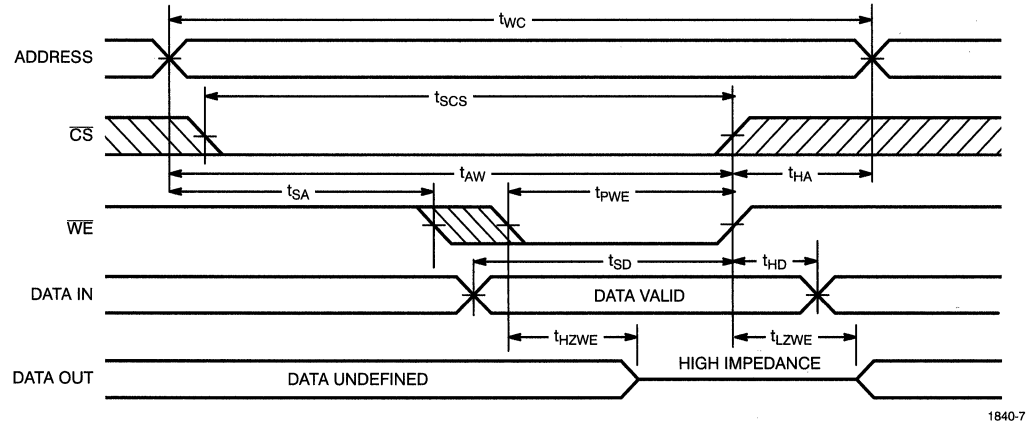
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 8]



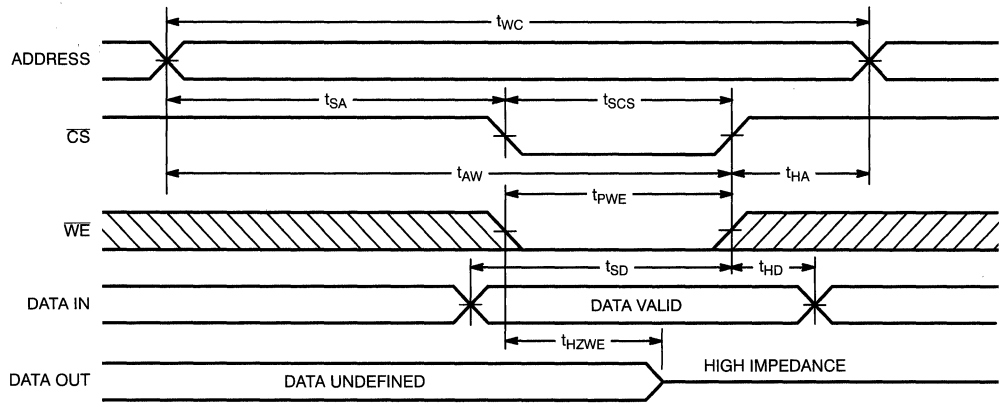
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1840PD–20C	PD06	60-Pin DIP Module	Commercial
25	CYM1840PD–25C	PD06	60-Pin DIP Module	Commercial
30	CYM1840PD–30C	PD06	60-Pin DIP Module	Commercial
35	CYM1840PD–35C	PD06	60-Pin DIP Module	Commercial
45	CYM1840PD–45C	PD06	60-Pin DIP Module	Commercial
55	CYM1840PD–55C	PD06	60-Pin DIP Module	Commercial

Document #: 38–M–00040–B

CYM1841
CYM1841A

256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **32-bit standard footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power**
  - **5.3W (max.) at 25 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.58 in.**
- **Available in ZIP, SIMM, and angled SIMM footprint**
- **72-pin SIMM version compatible with 1M x 32 (CYM1851)**

Functional Description

The CYM1841/1841A is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{17}).

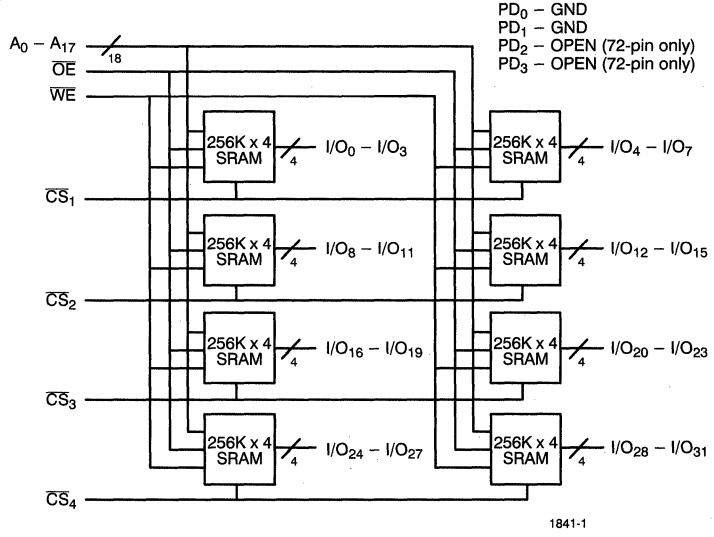
Reading the device is accomplished by taking the chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

A 72-pin SIMM is offered for compatibility with the 1M x 32 CYM1851. This version is socket upgradable to the CYM1851.

Logic Block Diagram



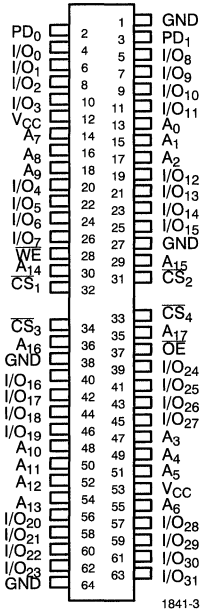
Selection Guide

	1841A–12	1841A–15	1841–20 1841A–20	1841–25 1841A–25	1841–30 1841A–30	1841–35 1841A–35	1841–45 1841A–45	1841–55 1841A–55
Maximum Access Time (ns)	12	15	20	25	30	35	45	55
Maximum Operating Current (mA)	1600	1600	1120	960	960	960	960	960
Maximum Standby Current (mA)	480	480	480	480	480	480	480	480

Shaded area contains preliminary information.

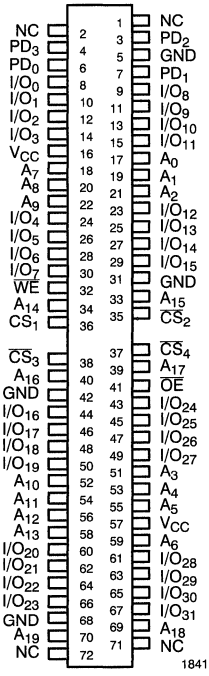
Pin Configurations (continued)

64-Pin ZIP/SIMM Top View



1841-3

72-Pin (1841AP7 only) SIMM Top View



1841-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 55°C to +125°C

Ambient Temperature with Power Applied ..... – 10°C to +85°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1841A–12 1841A–15 Min.	1841A–12 1841A–15 Max.	1841–20 1841A–20 Min.	1841–20 1841A–20 Max.	1841–25, 30, 35, 45, 55 1841A–25, 30, 35, 45, 55 Min.	1841–25, 30, 35, 45, 55 1841A–25, 30, 35, 45, 55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	−16	+16	− 16	+16	− 16	+16	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		1600		1120		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		480		480		480	mA
I_{SB2} 1841	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V				16		16	mA
I_{SB2} 1841A	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V		240		120		120	mA

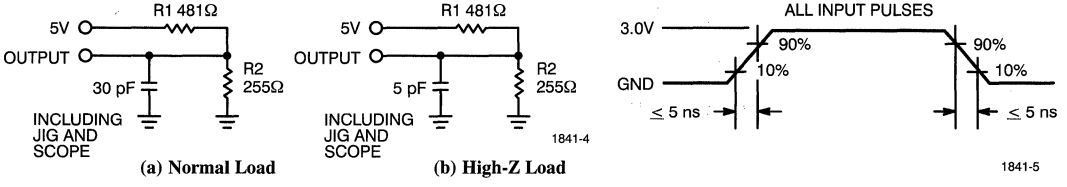
Shaded area contains preliminary information.

Capacitance[2]

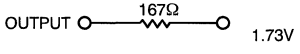
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[3]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70/20	pF
C_{OUT}	Output Capacitance		20	pF

Note:
1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.
3. 20 pF on $\overline{CS}$, 70 pF all others.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

Parameter	Description	1841A–12		1841A–15		1841–20 1841A–20		1841–25 1841A–25		1841–30 1841A–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		30		ns
t_{AA}	Address to Data Valid		12		15		20		25		30	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		13		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		7		8		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		7		8		20		20		20	ns
WRITE CYCLE[7]												
t_{WC}	Write Cycle Time	12		15		20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	9		10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	9		10		18		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	1		1		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		13		15		15		ns
t_{HD}	Data Hold from Write End	1		1		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	5	0	7	0	15	0	15	0	15	ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range (continued)[4]

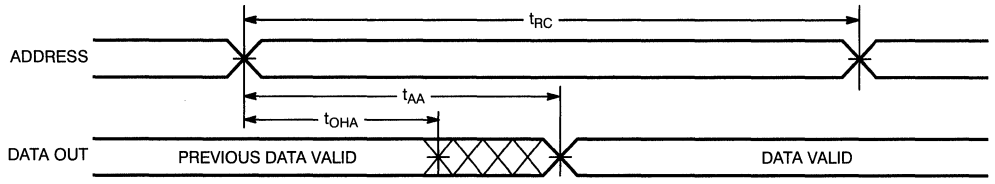
Parameter	Description	1841–35 1841A–35		1841–45 1841A–45		1841–55 1841A–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ LOW to High Z		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		20	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	0	15	ns

Notes:

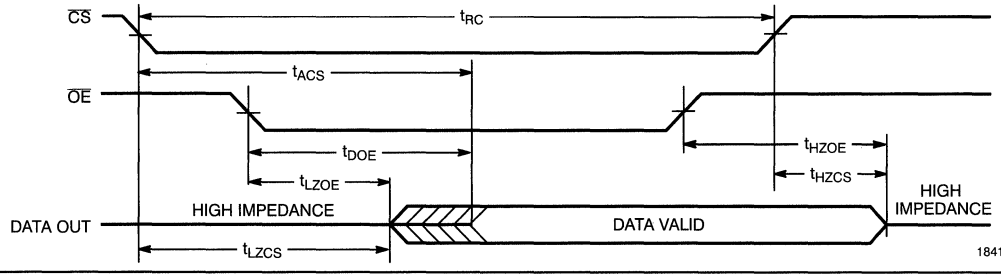
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

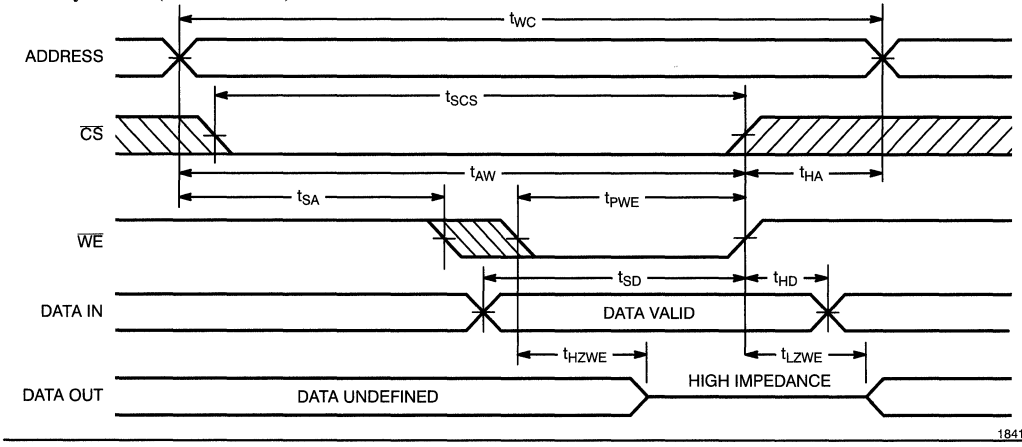
Read Cycle No. 1[8, 9]



Read Cycle No. 2[8, 10]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]

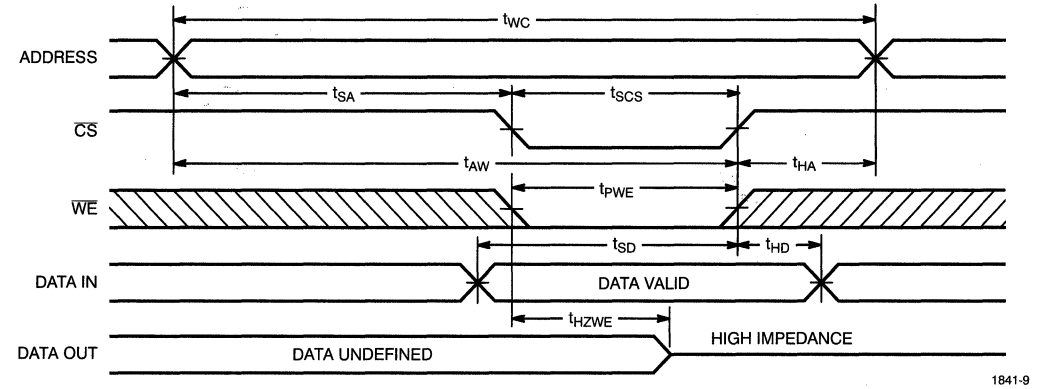


Notes:

8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CYM1841APM–12C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841APN–12C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–12C	PZ03	64-Pin Plastic ZIP Module	
15	CYM1841APM–15C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841AP7–15C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–15C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–15C	PZ03	64-Pin Plastic ZIP Module	
20	CYM1841PM–20C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–20C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–20C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM–20C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7–20C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–20C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–20C	PZ03	64-Pin Plastic ZIP Module	
25	CYM1841PM–25C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–25C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–25C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM–25C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7–25C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–25C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–25C	PZ03	64-Pin Plastic ZIP Module	
30	CYM1841PM–30C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–30C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–30C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM–30C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7–30C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–30C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–30C	PZ03	64-Pin Plastic ZIP Module	
35	CYM1841PM–35C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–35C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–35C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM–35C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7–35C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–35C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–35C	PZ03	64-Pin Plastic ZIP Module	

Shaded area contains prliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CYM1841PM–45C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–45C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–45C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM–45C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7–45C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–45C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–45C	PZ03	64-Pin Plastic ZIP Module	
55	CYM1841PM–55C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–55C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–55C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APM–55C	PM02	64-Pin Plastic SIMM Module	
	CYM1841AP7–55C	PM04	72-Pin Plastic SIMM Module	
	CYM1841APN–55C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841APZ–55C	PZ03	64-Pin Plastic ZIP Module	

Document #: 38–M–00031–D

512K x 32 Static RAM Module

Features

- **High-density 16-megabit SRAM module**
- **32-bit standard footprint supports from 16Kx32 through 1Mx32**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **4.4W (max.) at 25 ns**
- **Compatible with CYM1821, CYM1831, CYM1836, CYM1841, and CYM1851 JEDEC modules**
- **Available in 72-pin ZIP or SIMM/ Angled SIMM**

Functional Description

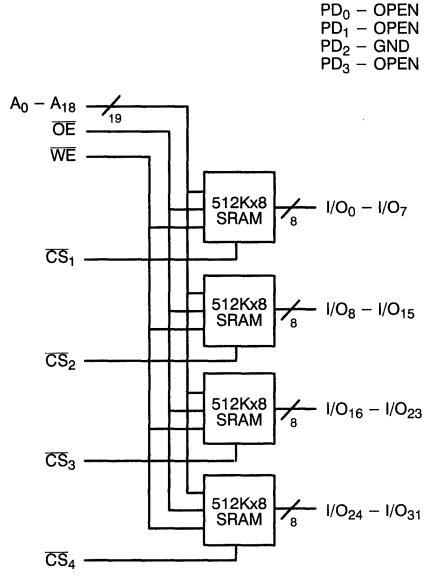
The CYM1846 is a high-performance 16-megabit static RAM module organized as 512K words by 32 bits. This module is constructed from four 512K x 8 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of the chip selects.

The CYM1846 is designed for use with standard 72-pin SIMM socket and ZIP footprint. The pinout is compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841) and the 72-pin CYM1851. Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1024K words (CYM1851). The standard SIMM can be used in Angled SIMM sockets.

Presence detect pins (PD_0 – PD_3) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.

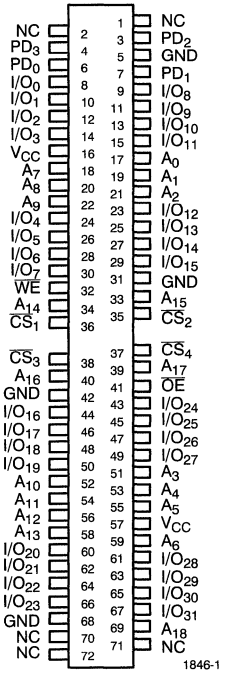
3

Logic Block Diagram



Pin Configuration

ZIP/SIMM Top View



1846-1

Selection Guide

	1846–25	1846–30	1846–35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	800	800	800
Maximum Standby Current (mA)	240	240	240

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +V_{CC}

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}		800	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V		40	mA

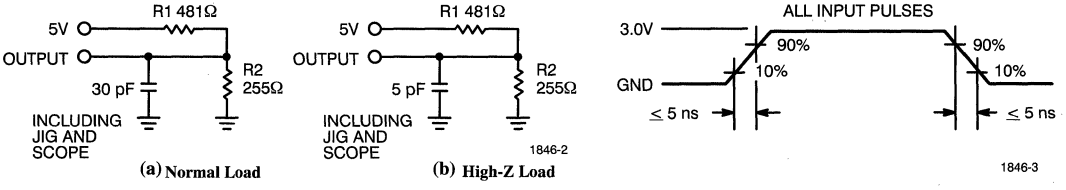
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance ($\overline{WE}$, $\overline{OE}$, A_{0-18})	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		20	pF
C_{OUT}	Output Capacitance		20	pF

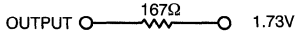
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

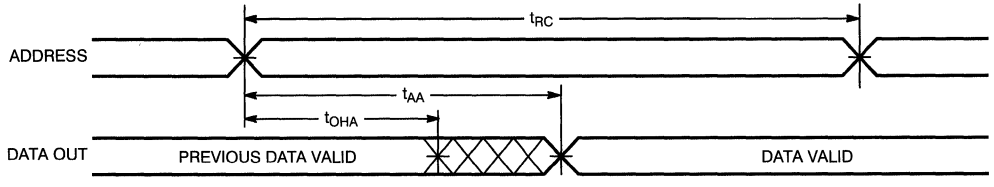
Parameter	Description	1846–25		1846–30		1846–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		12		12		12	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		12		12		12	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	12	0	12	0	12	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

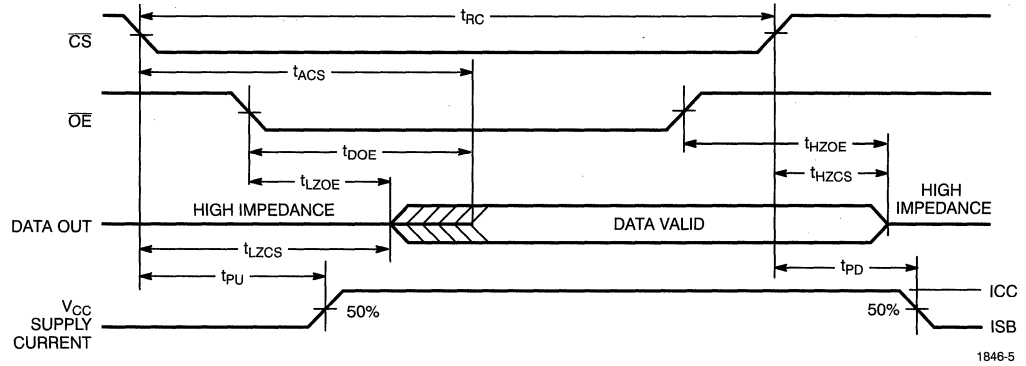
Read Cycle No. 1[7, 8]



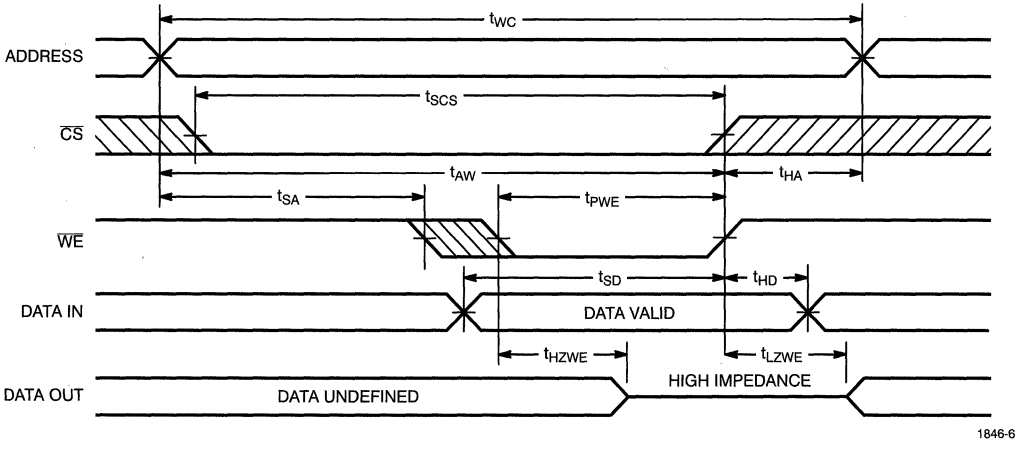
1846-4

Switching Waveforms (continued)

Read Cycle No. 2[7, 9]



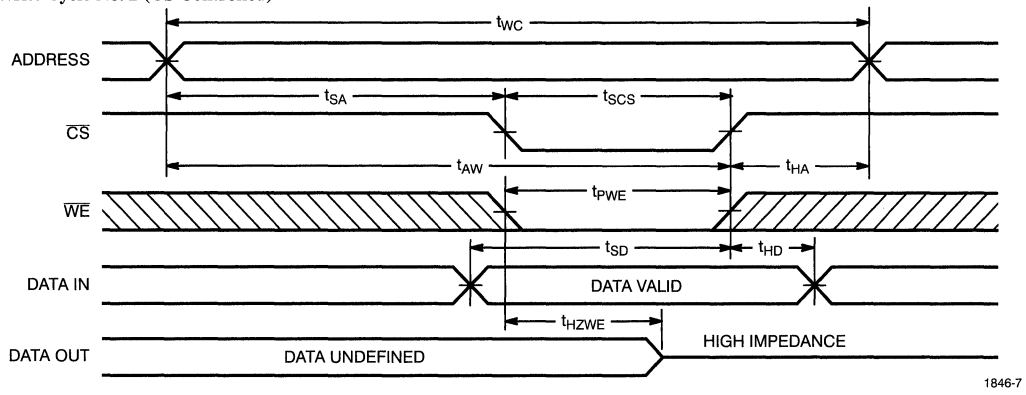
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL}, and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Note:
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
25	CYM1846PM–25C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846PZ–25C	PZ11	72-Pin Plastic ZIP Module	
30	CYM1846PM–30C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846PZ–30C	PZ11	72-Pin Plastic ZIP Module	
35	CYM1846PM–35C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846PZ–35C	PZ11	72-Pin Plastic ZIP Module	

Document #: 38–M–00073

PRELIMINARY **CYM1851**

1,024K x 32 Static RAM Module

Features

- **High-density 32-megabit SRAM module**
- **32-bit Standard Footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **6.6W (max.) at 25 ns**
- **72 pins**
- **Available in ZIP, SIMM, or angled SIMM format**

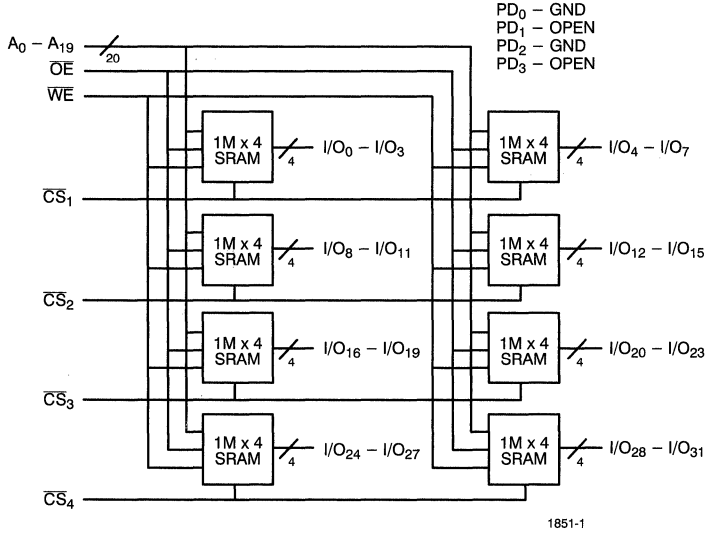
Functional Description

The CYM1851 is a high-performance 32-megabit static RAM module organized as 1,024K words by 32 bits. This module is constructed from eight 1,024K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The CYM1851 is designed for use with standard 72-pin SIMM sockets. The pinout is downward compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841). Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1,024K words (CYM1851).

Presence detect pins ($PD_0 - PD_3$) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.

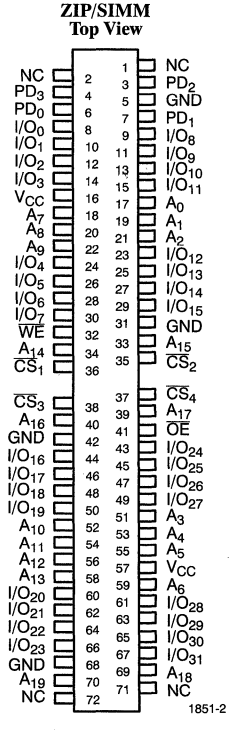
Logic Block Diagram



1851-1

Pin Configuration

ZIP/SIMM Top View



1851-2

Selection Guide

	1851–25	1851–30	1851–35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	1200	1200	960
Maximum Standby Current (mA)	480	480	480

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +V_{CC}

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}		1200	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		480	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V		80	mA

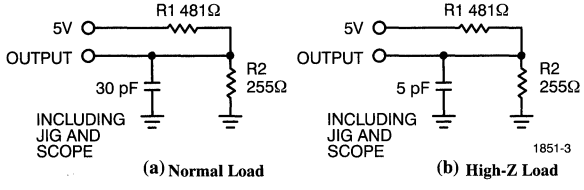
Capacitance[2]

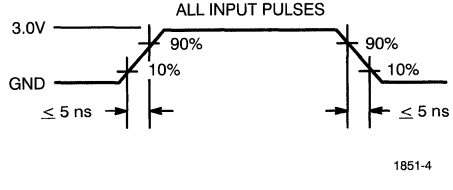
Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance ($\overline{WE}$, $\overline{OE}$, A_{0-19})	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		20	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

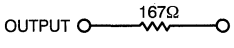
1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

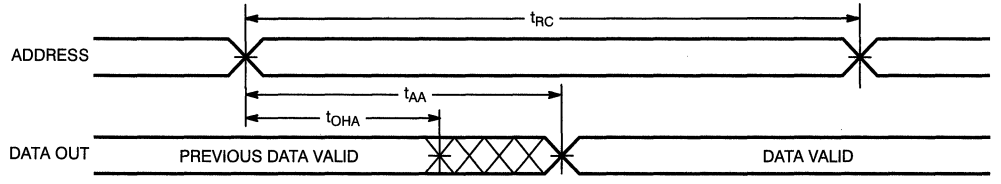
Parameter	Description	1851–25		1851–30		1851–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		12		12		12	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		12		12		12	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	12	0	12	0	12	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

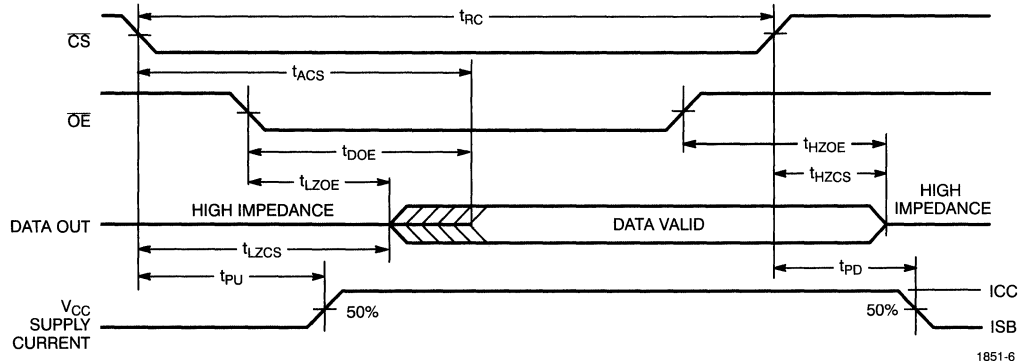
Read Cycle No. 1[7, 8]



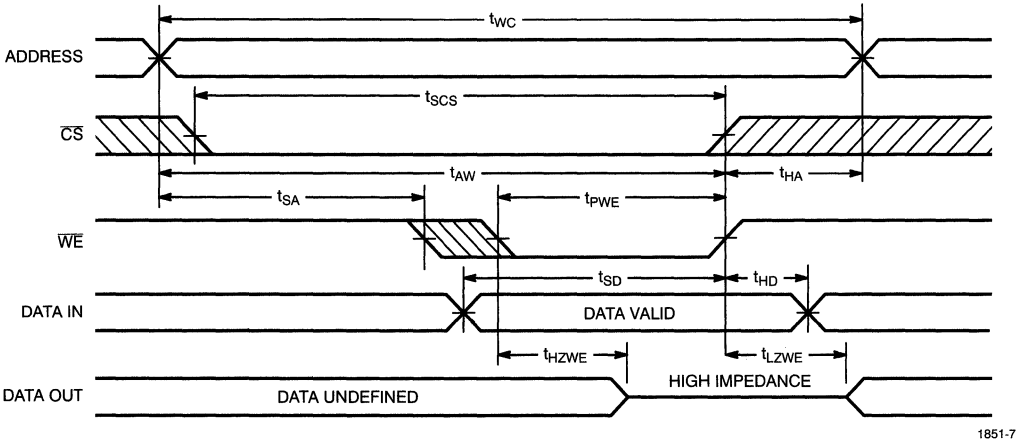
1851-5

Switching Waveforms (continued)

Read Cycle No. 2[7, 9]



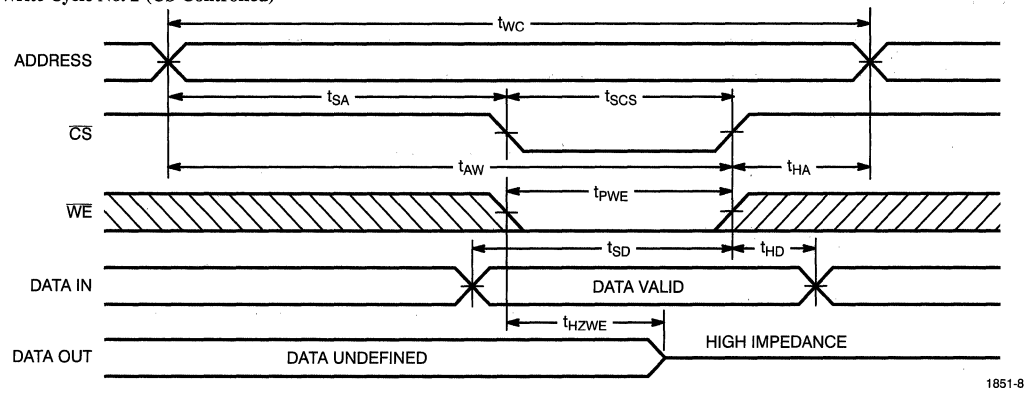
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL}, and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Note:
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
25	CYM1851PM–25C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN–25C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ–25C	PZ09	72-Pin Plastic ZIP Module	
30	CYM1851PM–30C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN–30C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ–30C	PZ09	72-Pin Plastic ZIP Module	
35	CYM1851PM–35C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851PN–35C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851PZ–35C	PZ09	72-Pin Plastic ZIP Module	

Document #: 38–M–00052–A

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM7232
CYM7264

DRAM Accelerator Module

Features

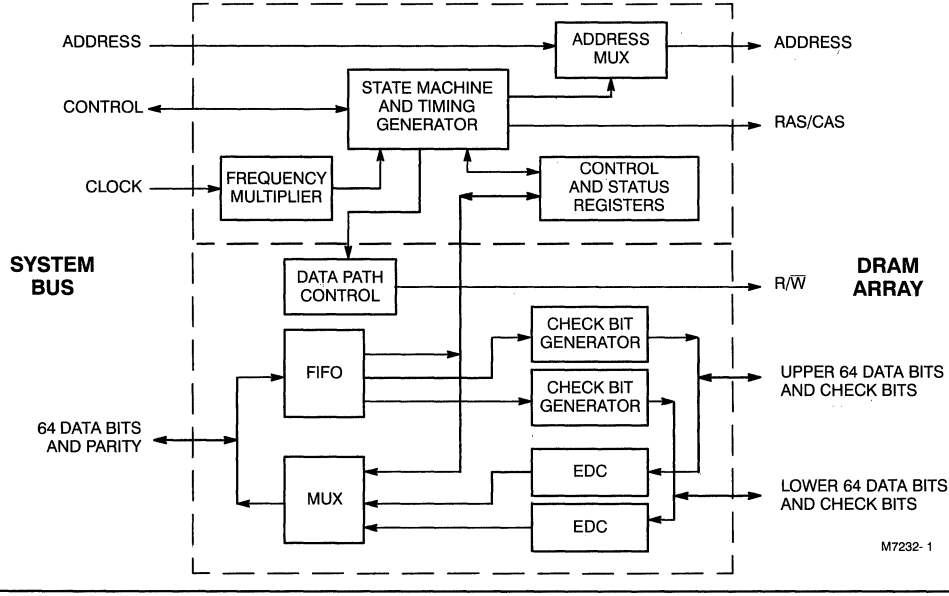
- 4-megabyte to 1-gigabyte control capability
- 32- or 64-bit bus interface (M7232 only)
- 32- or 64-bit EDC versions
  - — 1-bit correct; 2-bit detect
- Multiplexed or non-multiplexed bus
- i486, Pentium™, i860, 68040, 88110, PowerPC™, SPARC, and MIPS compatible
- Synchronous bus interface
- 25-, 33-, and 40-MHz versions
- Error-logging facilities
- Cache line fill burst support; posted writes
- Cache line write-back support; write FIFO
- High performance
  - — 25-ns writes
  - — 175-, 25-, 50-, 25-ns burst read/80-ns DRAMs
- Automatic refresh with scrubbing
- Multiprocessor compatible
  - — Inhibited reads and writes
  - — Reflective reads
  - — Reads for ownership
- Bus parity generation and checking
- Very small size

Functional Description

The CYM7232 and the CYM7264 consist of a full-function DRAM controller and a pipelined/FIFO data multiplexer/demultiplexer with error correction for cache-based, uniprocessor, and multiprocessor systems memory control. The CYM7232 performs 32-bit Error Detection and Correction (EDC) while CYM7264 performs 64-bit EDC. They both connect to the system bus through a 64-bit-wide data bus, and a 36-bit wide address bus. The CYM7232 also supports 32-bit system buses. The bus transfer control signals support i486, Pentium, i860, 68040, 88110, SPARC MBus, MIPS R4000, or other interfaces. The controller module interfaces to the DRAM array through a 16-byte-wide data bus plus check bits, a 12-bit row/column address bus, four $\overline{RAS}$ outputs, four $\overline{CAS}$ outputs, and four read/write control lines.

During write operations, data passes from the system bus through a FIFO array that acts as an incoming queue. Writes occur at the system bus speed until the FIFO is full (sixteen 64-bit words). The FIFO supports cache-line copy-back and fill operations, reducing system bus traffic to a minimum. The module supports posted writes, by suspending the actual write to DRAM until the cache-line read is completed during cache-line write-back. This speeds cache-line fill operations. The module pipelines a 16-byte-wide DRAM access into the data path for EDC, and multiplexes the data to the system bus during reads. This supports high-speed burst line fills with error corrected data. Reads and writes may be inhibited for multiprocessor support. Inhibited reads may be turned into reflective reads, and inhibited writes may be turned into reads-for-ownership.

Logic Block Diagram



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PowerPC is a trademark of IBM.

Document #: 38–00441

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM7420
CYM7421

82420 PCIset-Compatible Level II Cache Modules

Features

- **128 Kbytes (CYM7420), 256 Kbytes (CYM7421) cache module organized as 32K by 32 or 64K by 32**
- **Tag width of 7/8 bits plus valid bit**
- **Independent dirty bit**
- **Operates with systems based on the Intel™ 82420 core logic**
- **Zero-wait state operation at 33 Mhz**
- **Constructed using standard asynchronous SRAMs**
- **112-pin Burndy Connector, Part Number CELP2X56SC3Z48**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

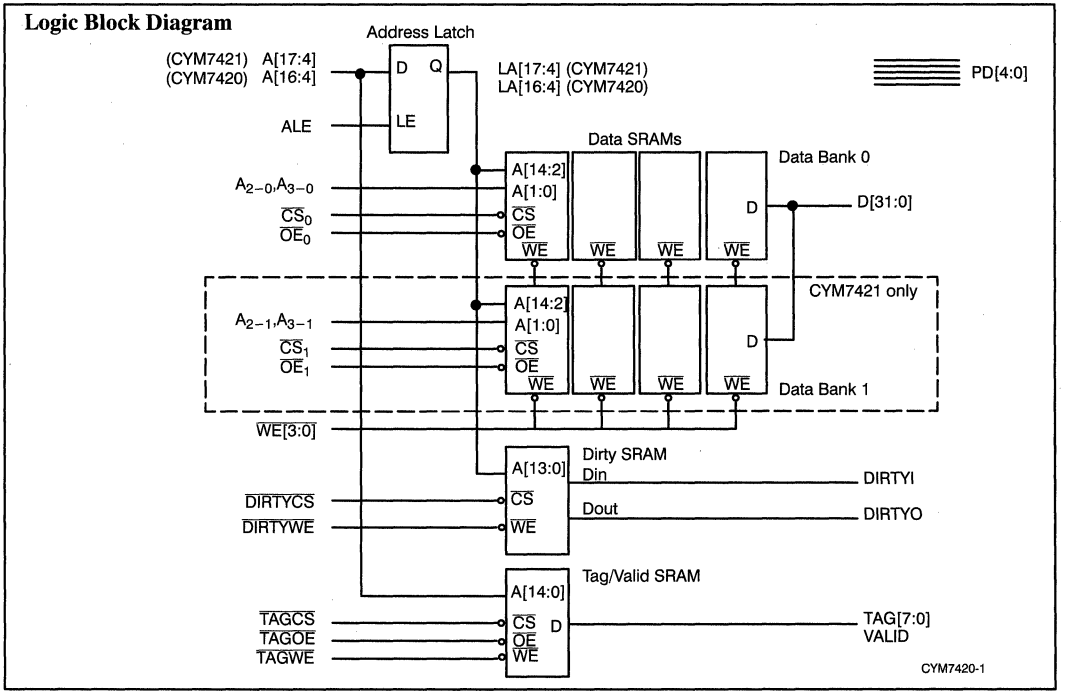
Functional Description

The CYM7420 module series is a family of cache memory subsystems for Intel 486-based systems. Each module contains either one or two banks of 32-bit wide Data SRAM, 8K/32K entries of 7/8-bit tag, and one Valid bit, and a single bit wide, separate I/O Dirty SRAM. CYM7420 has 8-bit tags, while CYM7421 support 7-bit tags. The address signals for the Data and Dirty SRAMs are latched.

The modules are configured as a 112-pin card-edge memory module. It is constructed using standard asynchronous SRAMs in SOJ packages mounted on a multilayer epoxy laminate (FR4) substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

These modules are designed for zero wait state operation in 486-based systems operating at a bus speed of 33 Mhz. They are designed for compatibility with the Intel 82420 PCIset and other chip sets. The baseline speed grade is built using 12 nanosecond Tag SRAMs and 20 nanosecond Data SRAMs.

Logic Block Diagram



Selection Guide

	CYM7420PB–20	CYM7421PB–20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

Intel is a trademark of Intel Corporation.

Document #: 38–M–00065–A

CYM7424
CYM7425

128K/256K Cache Module for the Intel™ 82420EX PCIset

Features

- **128 Kbyte (CYM7424) or 256 Kbyte (CYM7425) secondary cache module organized as 32K by 32 or 64K by 32**
- **Ideal for Intel 486-based systems with the 82420EX PCIset**
- **Supports 486 CPUs running at clock speeds up to 50 MHz**
- **Constructed using cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **112-position Burndy connector, part # CELP2X56SC3Z48**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

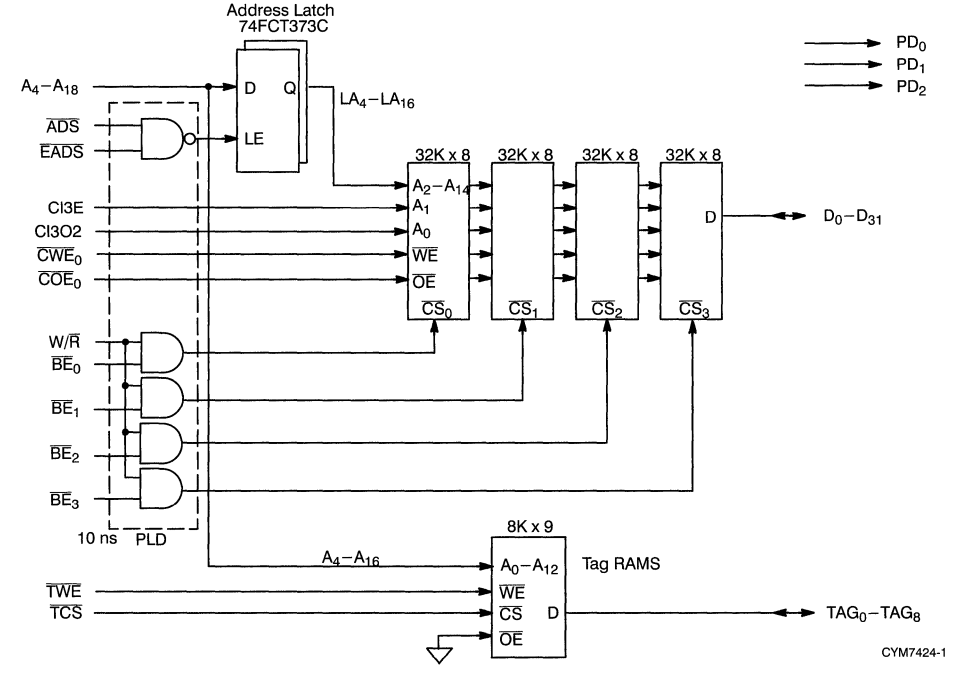
Functional Description

These modules are designed specially to function as the secondary cache in Intel 486-based systems with the 82420EX (Aries) PCIset. Each module contains either one or two banks of 32-bit wide data SRAMs, a 9-bit wide tag, address latch, and byte write logic. Asynchronous CMOS SRAMs are used to provide a high-performance, low-cost, and low-power solution for CPU speeds up to 50 MHz. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 112-pin Burndy connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The package dimensions are 3.145″ x 0.380″ x 1.105″. All inputs and outputs of the CYM7424 and CYM7425 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

3

Logic Block Diagram CYM7424

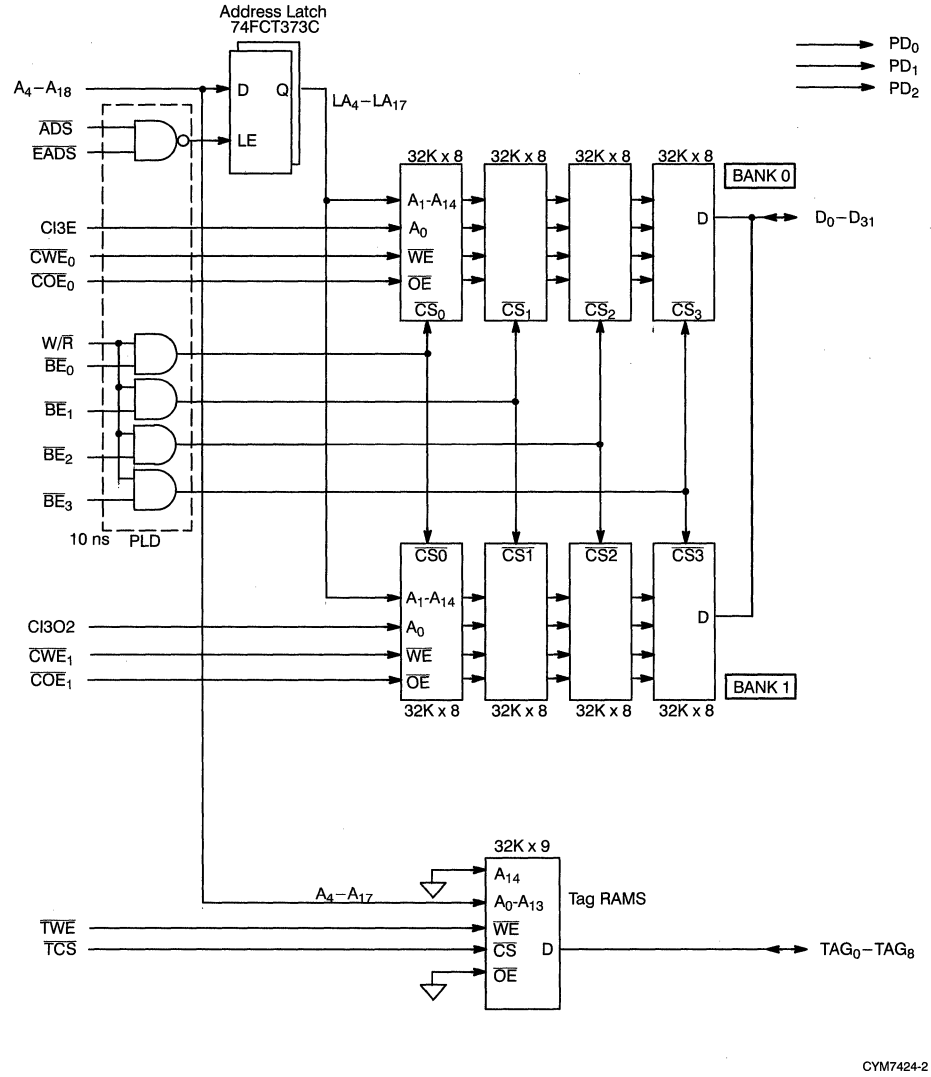


Selection Guide

	CYM7424–20	CYM7425–20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Tag/Valid SRAM (ns)	15	15

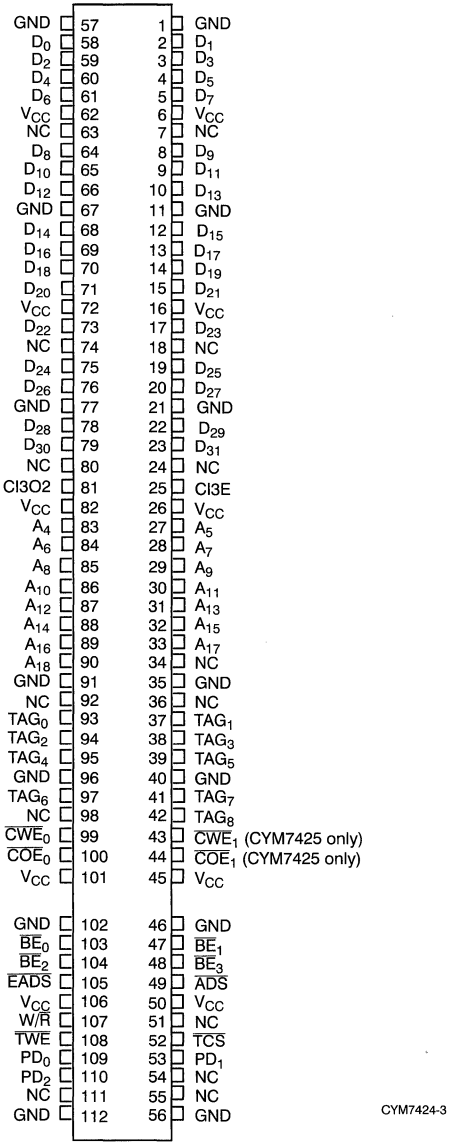
Intel 82420EX PCIset is a trademark of Intel Corporation.

Logic Block Diagram CYM7425



Pin Configuration

Dual Read-out SIMM
Top View



CYM7424-3

Pin Descriptions

Name	Description
A_4–A_{18}	Cache Address Inputs
CI3O2, CI3E	Cache Index Address Inputs
D_0–D_{31}	Cache Data Input/Outputs
$\overline{BE}_0$–$\overline{BE}_3$	Byte Enable Inputs
$\overline{CWE}_0$	Bank 0 Write Enable Input
$\overline{CWE}_1$	Bank 1 Write Enable Input
$\overline{COE}_0$	Bank 0 Output Enable
$\overline{COE}_1$	Bank 1 Output Enable
W/$\overline{R}$	Write/Read Input
$\overline{ADS}$	CPU Address Strobe Input
$\overline{EADS}$	External Address Strobe Input
TAG_0–TAG_8	Tag Data Input/Output
$\overline{TWE}$	Tag Write Input
$\overline{TCE}$	Tag Chip Enable Input
PD_0–PD_2	Presence Detect Pins
NC	No Connection

Presence Detect Table

	PD_2	PD_1	PD_0
CYM7424	NC	V_{CC}	NC
CYM7425	NC	NC	V_{CC}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7424 CYM7425 Min.	CYM7424 CYM7425 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = 4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current (CYM7424 only.)	V_{CC} = Max., I_{OUT} = 0 mA		1250	mA
I_{CC}	V_{CC} Operating Supply Current (CYM7425 only.)	V_{CC} = Max., I_{OUT} = 0 mA		1850	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current (CYM7424)	Max. V_{CC}, CS $\geq V_{IH}$, f=fmax $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$		550	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current (CYM7425)	Max. V_{CC}, CS $\geq V_{IH}$, f=0 $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V		360	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, CS $\geq V_{IH}$, f=fmax $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$		800	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, CS $\geq V_{IH}$, f=0 $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V		420	mA

Ordering Information

Cache Memory Size	Ordering Code	Package Name	Package Type	Operating Range
128 Kbyte	CYM7424PB−20C	PM11	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM7425PB−20C	PM12	112-Pin Dual-Readout SIMM	Commercial

Document #: 38−M−00067

CYM7427
CYM7428

82420 PCIset-Compatible Level II Cache Module Family

Features

- **Cache size 128 Kbytes or 256 Kbytes**
- **Tag width of 7 bits plus valid bit**
- **Independent dirty bit**
- **Operates with systems based on the Intel 82420 core logic**
- **Zero-wait state operation at 33 MHz**
- **Constructed using standard asynchronous SRAMs**
- **112-pin Burndy Connector, Part Number CELP2X56SC3Z48**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

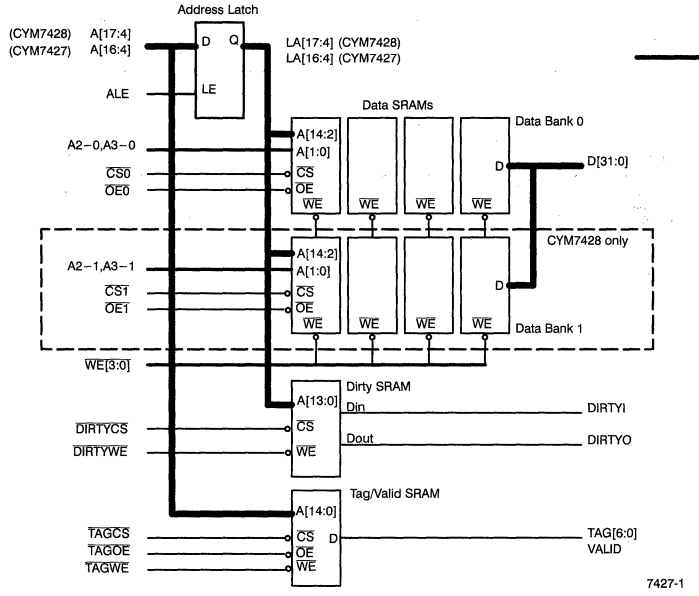
Functional Description

The CYM7427/28 module series is a family of cache memory subsystems for Intel 486-based systems. The CYM7427 (128 Kbytes) contains one memory bank organized as 32K by 32. The CYM7428 (256 Kbytes) contains two banks for interleaved operation. In addition, each module contains one 8-bit wide SRAM, supporting a 7-bit tag and one Valid bit, and a single-bit, separate I/O SRAM supporting a Dirty bit. The address signals for the Data and Dirty SRAMs are latched.

The 7427/28 is configured as a 112-pin card-edge memory module. It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

These modules are designed for zero-wait-state operation in 486-based systems operating at a bus speed of 33 MHz. They are designed for compatibility with the Intel 82420 PCIset and other chipsets. The baseline speed grade is built using 12-nanosecond Tag SRAMs and 20-nanosecond Data SRAMs.

Logic Block Diagram



Selection Guide

	CYM7427PB–20	CYM7428PB–20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

Document #: 38–M–00077

256K Pentium™-Compatible Cache Module

Features

- **256-Kbyte secondary cache module organized as 32K by 64**
- **Ideal for Intel™ Pentium-based systems and systems with 64-bit data**
- **Operates with 60- and 66-MHz Pentium processors**
- **Uses cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **160-position Burndy Computerbus™ connector**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

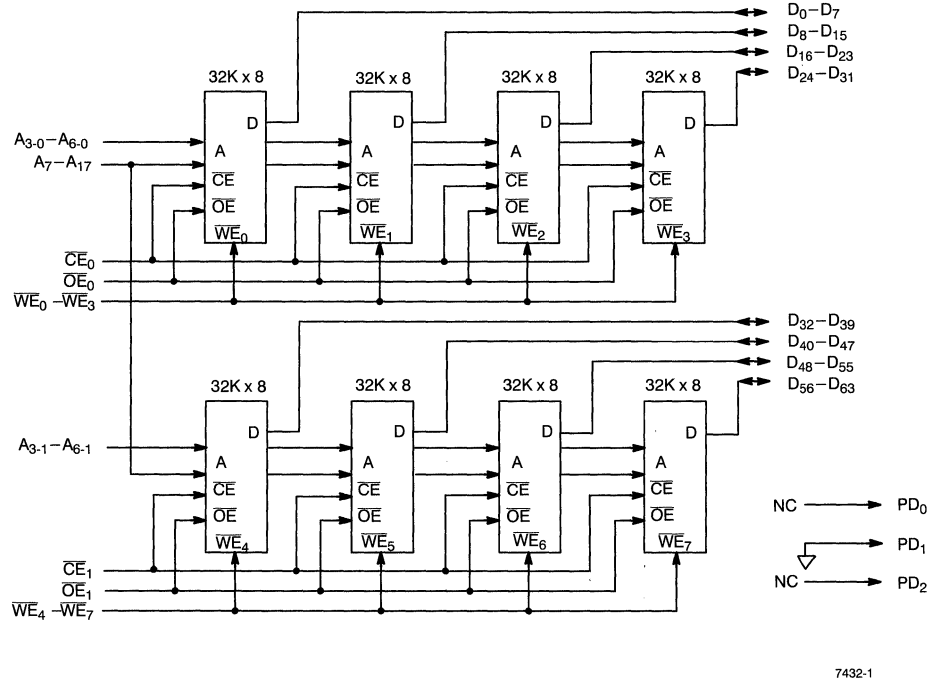
Functional Description

The CYM7432 is a 256-Kbyte secondary cache module designed for Intel Pentium CPU-based systems. The 32K by 64 organization is designed using asynchronous CMOS SRAMs to provide a low-cost, low-power, and high-performance solution for CPU speeds up to 66 MHz. CYM7432–12 contains 12 ns SRAMs suitable for 66-MHz operations. For 60-MHz applications, CYM7432–15 with 15 ns SRAMs can be used. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The package dimensions are 4.35″ x 0.365″ x 0.7″. All inputs and outputs of the CYM7432 are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.

3

Logic Block Diagram



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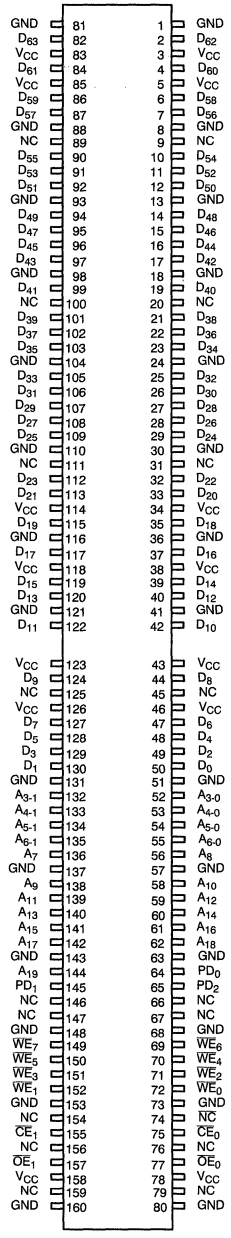
Computerbus is a trademark of Burndy.

Pin Configuration

Dual Read-out SIMM

Top View



7432b-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7432 Min.	CYM7432 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_R		1450	mA

Ordering Information

Operating Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
66	CYM7432PB−12C		160-Pin Dual-Readout SIMM	Commercial
60	CYM7432PB−15C		160-Pin Dual-Readout SIMM	Commercial

Document #: 38−M−00068

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM7450
CYM7451

128K/256K Cache Module for VLSI VL82C483 Chipset

Features

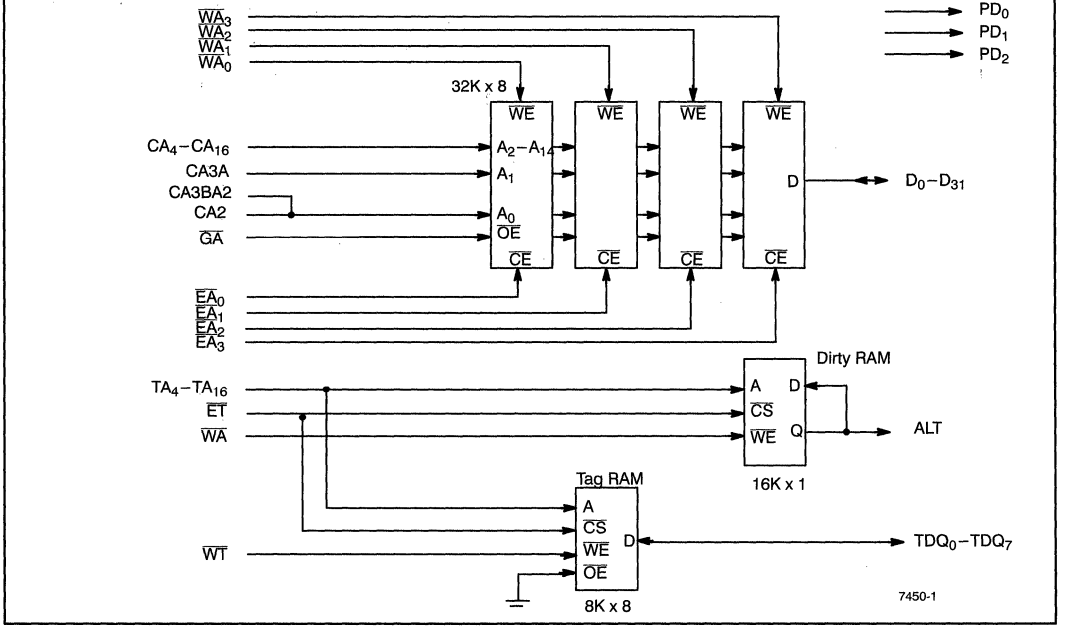
- **128 Kbyte (CYM7450) or 256 Kbyte (CYM7451) secondary cache module organized as 32K by 32 or 64K by 32**
- **Ideal for Intel™ 486-based systems with the VLSI VL82C483 chipset**
- **Zero-wait-state operations at 33 MHz**
- **Constructed using cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **128-position Dual Readout SIMM**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

Functional Description

These modules are designed specially to function as the secondary cache in Intel 486-based systems with the VLSI VL82C483 chipset. Each module contains either one or two banks of 32-bit wide data SRAMs, an 8-bit wide tag RAM, and a single-bit dirty RAM with separate I/O. Each byte in the data cache can be written individually. Separate address lines for the data RAMs and the tag/dirty RAMs are supported. Asynchronous CMOS SRAMs are used to provide a low-cost, low-power, and zero-wait-state solution for CPU speeds up to 33 MHz. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 128-pin connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The package dimensions are 3.85″ x 0.33″ x 1.07″. All inputs and outputs of the CYM7450 and CYM7451 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.

Logic Block Diagram CYM7450



Selection Guide

	CYM7450PB–20C	CYM7451PB–20C
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	15	15

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Document #: 38–M–00066–A

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM7490
CYM7491
CYM7492

i486™ Level II Cache Module Family

Features

- **Cache sizes of 64 KB, 256 KB, or 1 MB**
- **Tag width of 8 bits**
- **Independent dirty bit**
- **Operates with 33-MHz Intel™ i486™ processors**
- **Zero-wait-state operation**
- **Constructed using standard asynchronous SRAMs**
- **64-position (128-signal) dual-readout SIMM**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

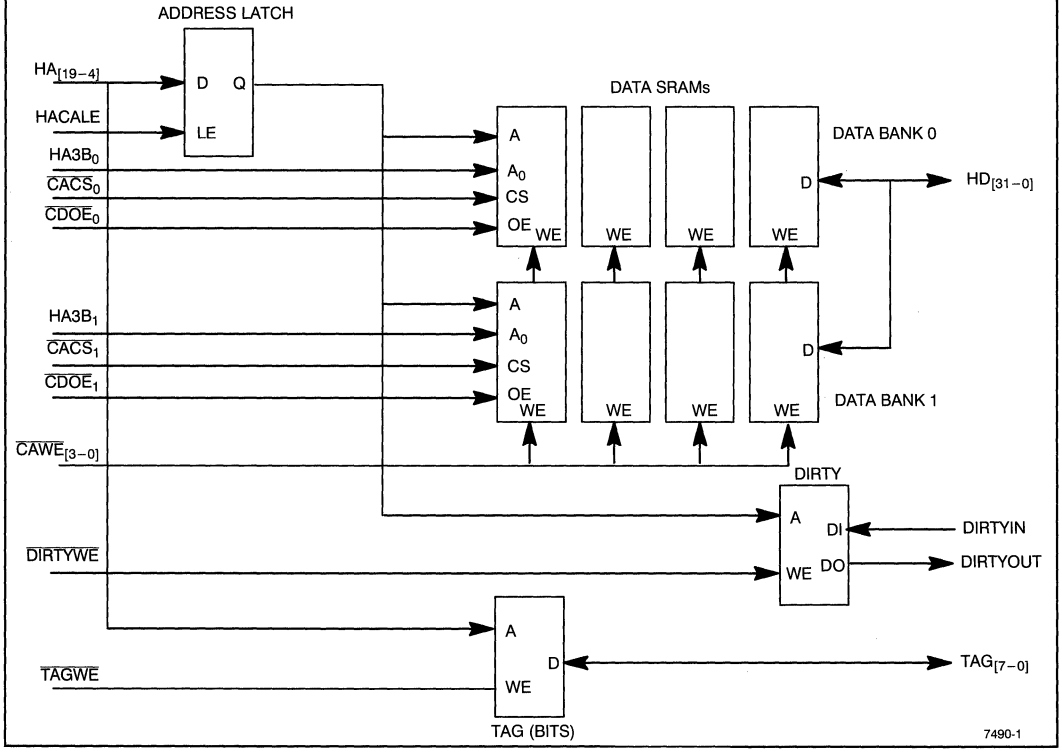
Functional Description

The CYM7490 module series is a family of cache memory subsystems for Intel i486-based systems. Each module contains two banks of 32-bit-wide data SRAM, an 8-bit-wide tag SRAM, and a single-bit-wide, separate I/O dirty SRAM. Bank sizes of 8K x 32, 32K x 32, and 128K x 32 are supported, yielding cache sizes of 64 kilobytes, 256 kilobytes, and 1 megabyte. The address signals for the data and dirty SRAMs are latched.

The module is configured as a 128-pin dual-readout single-in-line memory module (SIMM). It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The SIMM contacts are plated with five micro-inches of gold over 100 micro-inches of nickel. Module dimensions are 3.85 inches long by 1.15 inches high by 0.33 inches thick.

These modules are designed for zero-wait-state operation in 486-based systems operating at a bus speed of 33 MHz. They are designed for compatibility with off-the-shelf cache controllers and chipsets. The 15-ns device is built using data and tag SRAMs with an access time of 15 ns, while the 20-ns version is built with 15-ns tag SRAMs and 20-ns data SRAMs.

Logic Block Diagram



i486 and Intel are trademarks of Intel Corporation.

Document #: 38–M–00061–A

PRELIMINARY

Intel™ 82430NX Chipset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74AP54) or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins**
- **Ideal for Intel P54C-based systems with the 82430NX (Neptune) chipset**
- **Operates at 60 and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chipset.

CYM74AP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution for CPU bus speeds up to 66 MHz. The CYM74AP54 is organized as 32K by 64.

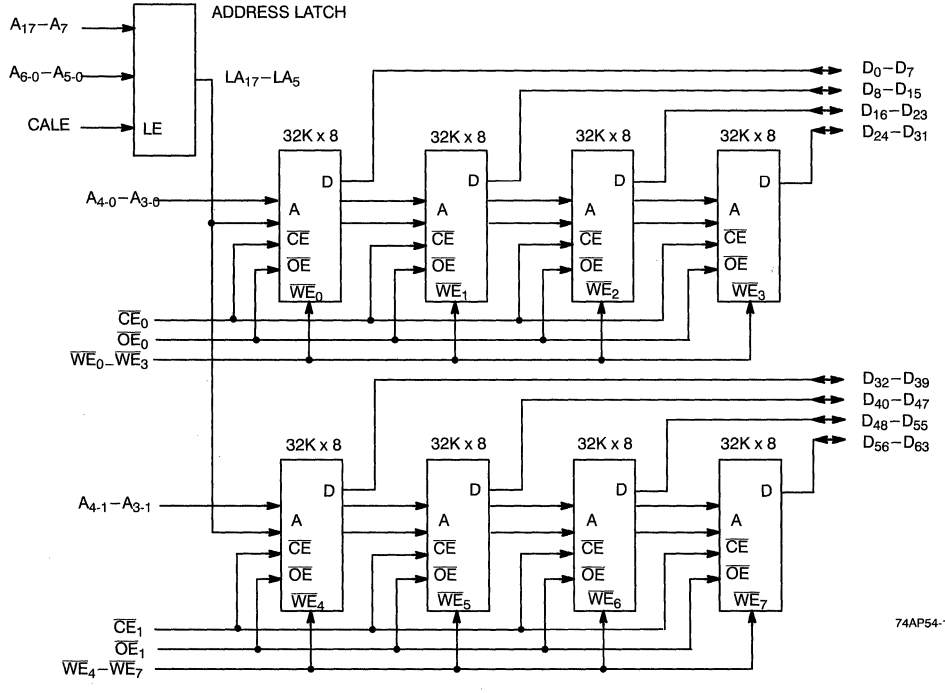
The CYM74SP54 and CYM74SP55 are synchronous cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity.

The CYM74SP55 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

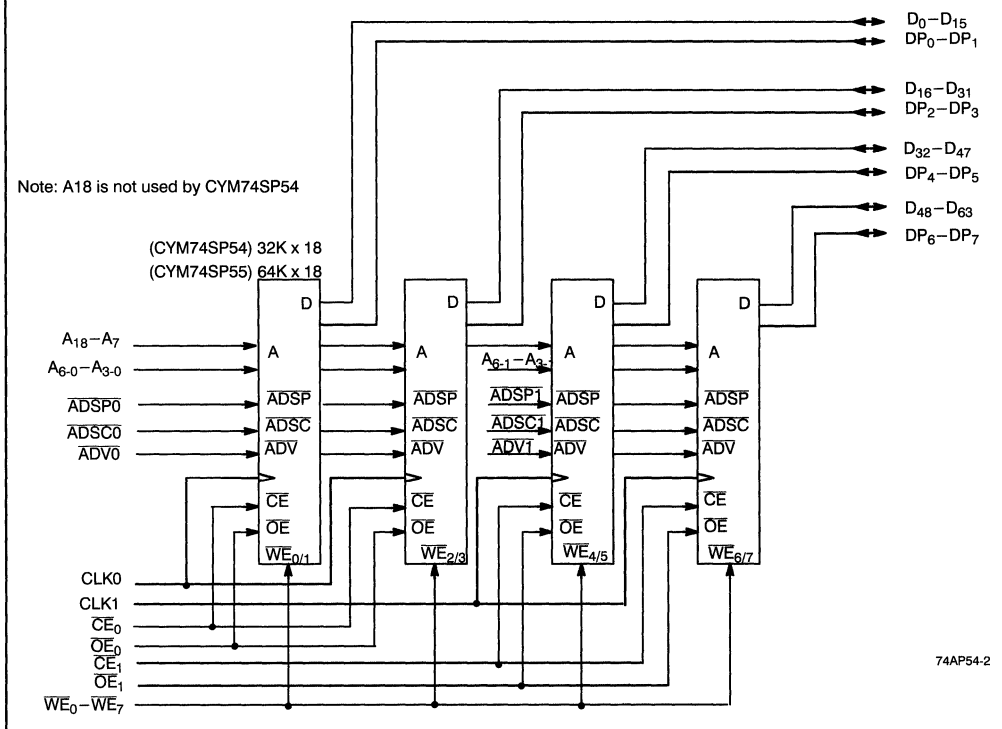
All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram – CYM74AP54



Intel is a trademark of Intel Corporation.

Logic Block Diagram – CYM74SP54/CYM74SP55

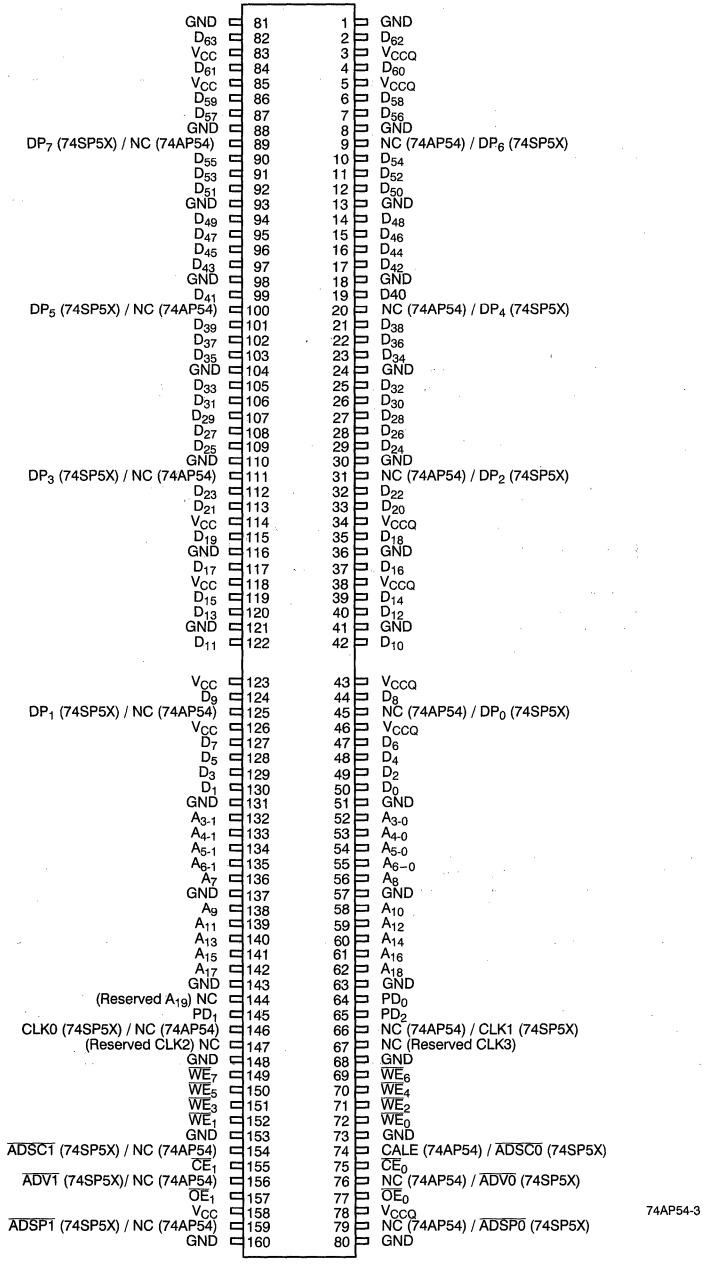


Selection Guide

	74AP54–60	74AP54–66	74SP54–60	74SP54–66	74SP55–60	74SP55–66
Cache Size (KB)	256	256	256	256	512	512
System Clock (MHz)	60	66	60	66	60	66
RAM Clock	Asynchronous	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous
RAM Speed	t_{AA}=15 ns	t_{AA}=12 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



74AP54-3

Pin Definitions

Signal Name	Description
V_{CC}	5V Supply
V_{CCQ}	3.3V Supply
GND	Ground
A_7–A_{19}	Addresses from processor
A_{3-0}, A_{4-0}, A_{5-0}, A_{6-0}	Lower address from chip set, identical to the bank1 addresses
A_{3-1}, A_{4-1}, A_{5-1}, A_{6-1}	Lower address from chip set, identical to the bank0 addresses
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable (same signal)
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable (same signal)
$\overline{WE}_0$, $\overline{WE}_1$, $\overline{WE}_2$, $\overline{WE}_3$, $\overline{WE}_4$, $\overline{WE}_5$, $\overline{WE}_6$, $\overline{WE}_7$	Byte Write Enables
CALE	Latch Enable – CYM74AP54 only
PD_0–PD_2	Presence Detect pins
D_0–D_{63}	Data lines from processor
DP_0–DP_7	Data Parity lines (Optional), CYM74SP54 or CYM74SP55 only
$\overline{ASDP0}$, $\overline{ADSP1}$	Processor Address Strobe, CYM74SP54 or CYM74SP55 only
$\overline{ADSC0}$,$\overline{ADSC1}$	Cache Controller Address Strobe, CYM74SP54 or CYM74SP55 only
$\overline{ADV0}$, $\overline{ADV1}$	Burst Address Advance – CYM74SP54 or CYM74SP55 only
CLK0, CLK1, CLK2, CLK3	Clock signals – CYM74SP54 or CYM74SP55 only, should be given own clk drivers
NC	Signal not connected on module.

Presence Detect Pins

	PD_2	PD_1	PD_0
Asynchronous – CYM74AP54	NC	GND	NC
Synchronous – CYM74SP54	GND	GND	NC
Synchronous – CYM74SP55	GND	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74AP54)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74SP54)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74SP55)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74AP54PM−60C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 15-ns Access RAMs	Commercial
	CYM74SP54PM−60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM−60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
66	CYM74AP54PM−66C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 12-ns Access RAMs	Commercial
	CYM74SP54PM−66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM−66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	

Document #: 38−M−00070−A

PRELIMINARY

Intel™ 82430FX PCIset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family that adheres to the Intel COAST 1.1 specification,**
- **Asynchronous (CYM74A430) or synchronous (CYM74S430, CYM74S431) configurations with presence and configuration detect pins**
- **Ideal for Intel P54C-based systems with the 82430FX (Triton) chip set**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V compatible inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430FX (Triton) chip set.

CYM74A430 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution. The CYM74A430 is organized as 32K by 64 data with an 8Kx8 tag that supports 3-2-2-2 read and 4-2-2-2 writes at 66 MHz.

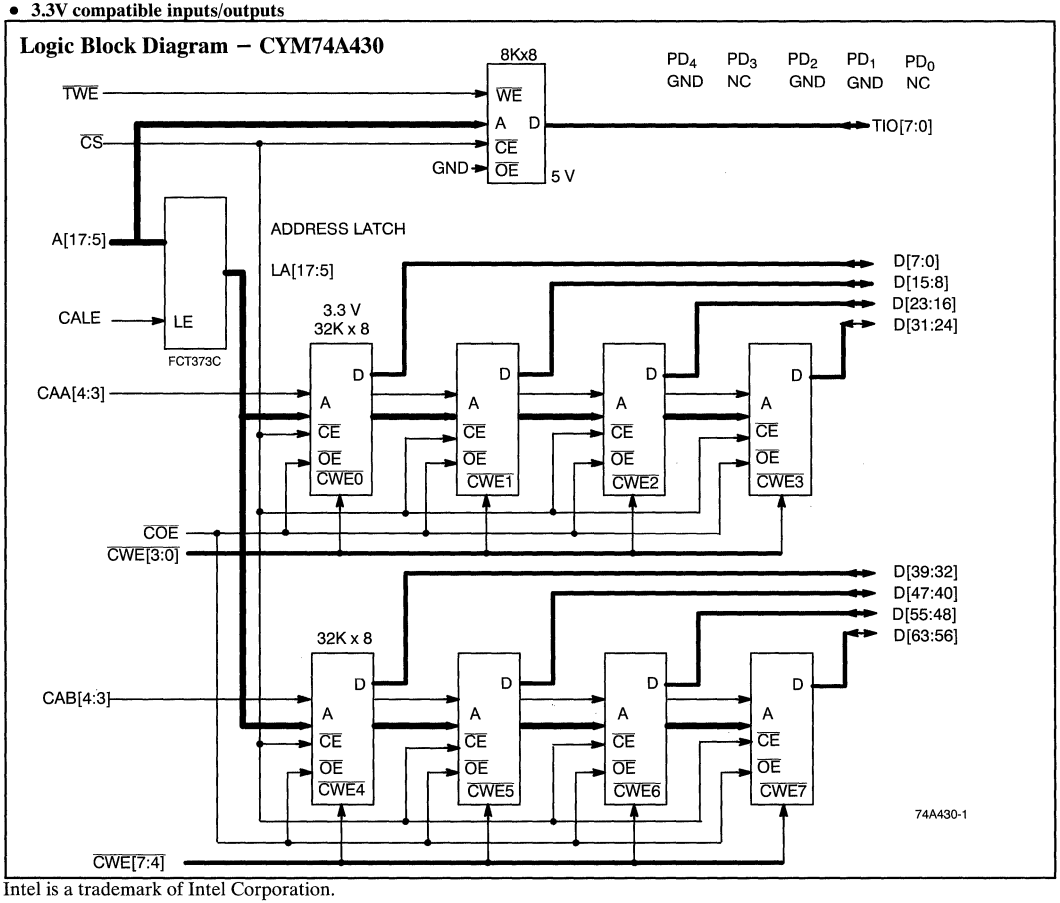
The CYM74S430 and CYM74S431 are synchronous cache modules that provide 3-1-1-1 performance at 66 MHz. The CYM74S430 is a 256-Kbyte cache module organized as 32Kx64 with an 8Kx8 tag. The CYM74S431 is a 512-Kbyte cache module organized as 64Kx64 with a 16Kx8 tag.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

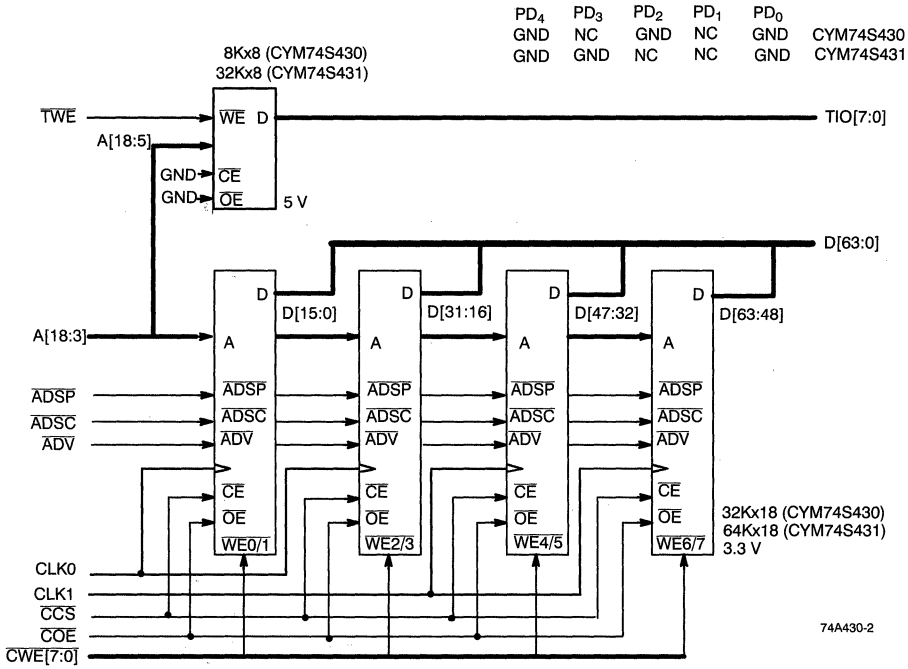
3

Logic Block Diagram – CYM74A430



Intel is a trademark of Intel Corporation.

Logic Block Diagram – CYM74S430/CYM74S431[1]



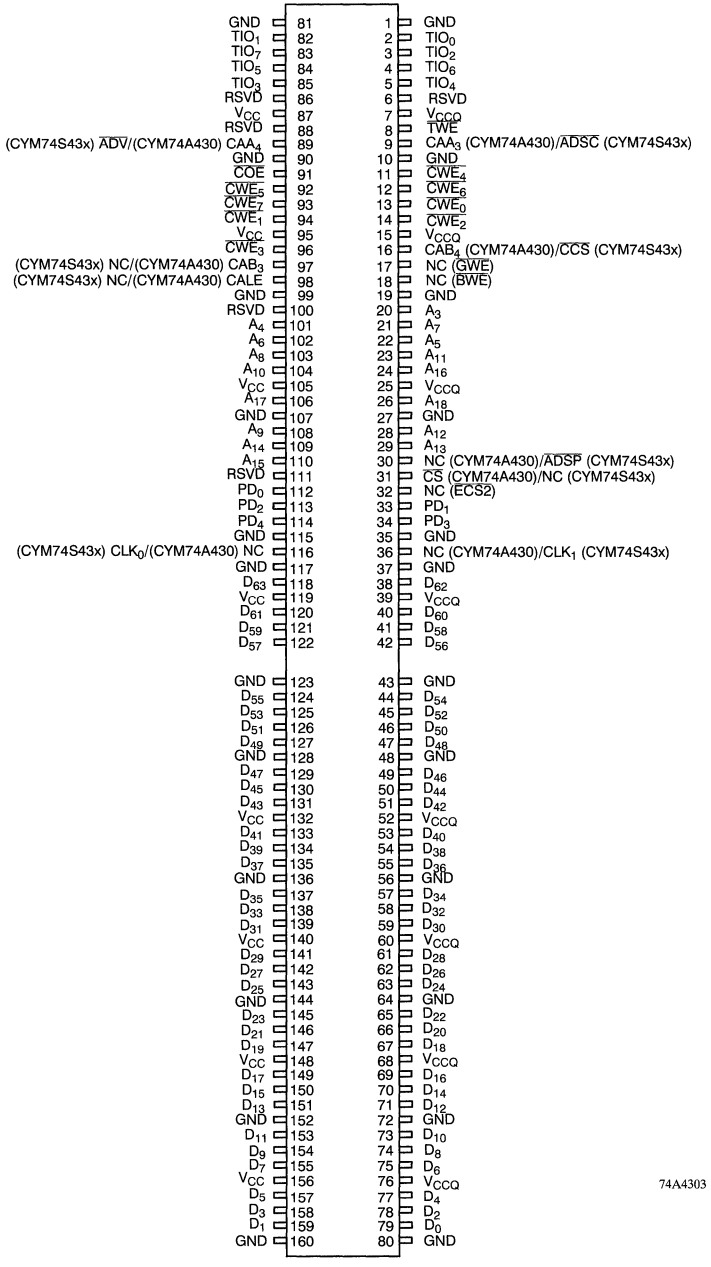
Selection Guide

	74A430–50	74A430–60	74A430–66	74S430–50	74S430–60	74S430–66	74S431–50	74S431–60	74S431–66
Cache Size	256 KB			256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66	50	60	66
RAM Type	Async			Sync Burst			Sync Burst		
Data t_{AA}	20 ns	17 ns	15 ns						
Data t_{CDV}				13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t_{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns

Notes:
1. A18 is not used by CYM74S430. DP pins are pulled high through 10 KΩ

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



74A4303

Pin Definitions

Signal Name	Description
V_{CC}	5V Supply
V_{CCQ}	3.3V Supply
GND	Ground
A[18:3]	Addresses from processor
CAA[4:3]	Lower two address bits for bank 0 of CYM74A430
CAB[4:3]	Lower two address bits for bank 1 of CYM74A430
$\overline{CS}$	Chip Select (CYM74A430 only)
$\overline{CCS}$	Chip Select for CYM74S430 and CYM74S431
$\overline{COE}$	Output Enable
$\overline{CWE}$[7:0]	Byte Write Enables
CALE	Latch Enable – CYM74A430 only
PD_0–PD_4	Presence Detect output pins
D[63:0]	Data lines from processor
TIO[7:0]	Tag data bits
$\overline{TWE}$	Tag Writen Enable signal
$\overline{ASDP}$	Processor Address Strobe for CYM74S430 and CYM74S431
$\overline{ADSC}$	Cache Controller Address Strobe for CYM74S430 and CYM74S431
$\overline{ADV}$	Burst Address Advance for CYM74S430 and CYM74S431
CLK[1:0]	Clock signals for CYM74S430 and CYM74S431
NC	Signal not connected on module.
RSVD	Reserved.

Presence Detect Pins

	PD_4	PD_3	PD_2	PD_1	PD_0
Asynchronous – CYM74A430	GND	NC	GND	GND	NC
Synchronous – CYM74S430	GND	NC	GND	NC	GND
Synchronous – CYM74S431	GND	GND	NC	NC	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74A430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74S430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1200	mA
I_{CC} (74S431)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1200	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74A430PM−50C	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM−50C	PM28		Sync 256 KB	
	CYM74S431PM−50C	PM28		Sync 512 KB	
60	CYM74A430PM−60C	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM−60C	PM28		Sync 256 KB	
	CYM74S431PM−60C	PM28		Sync 512 KB	
66	CYM74A430PM−66C	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM−66C	PM28		Sync 256 KB	
	CYM74S431PM−66C	PM28		Sync 512 KB	

Document #: 38−M−00074

CYM74A550, CYM74A551
PRELIMINARY **CYM74S550, CYM74S551**

OPTi Viper™ Chipset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74A550, CYM74A551) or synchronous (CYM74S550, CYM74S551) modules with presence and configuration detect pins**
- **Ideal for Intel™ P54C-based systems with the OPTi Viper™ chipset**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the OPTi Viper chipset.

CYM74A550 and CYM74A551 are low-cost asynchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules offer 3-2-2-2 performance at CPU bus speeds up to 66 MHz.

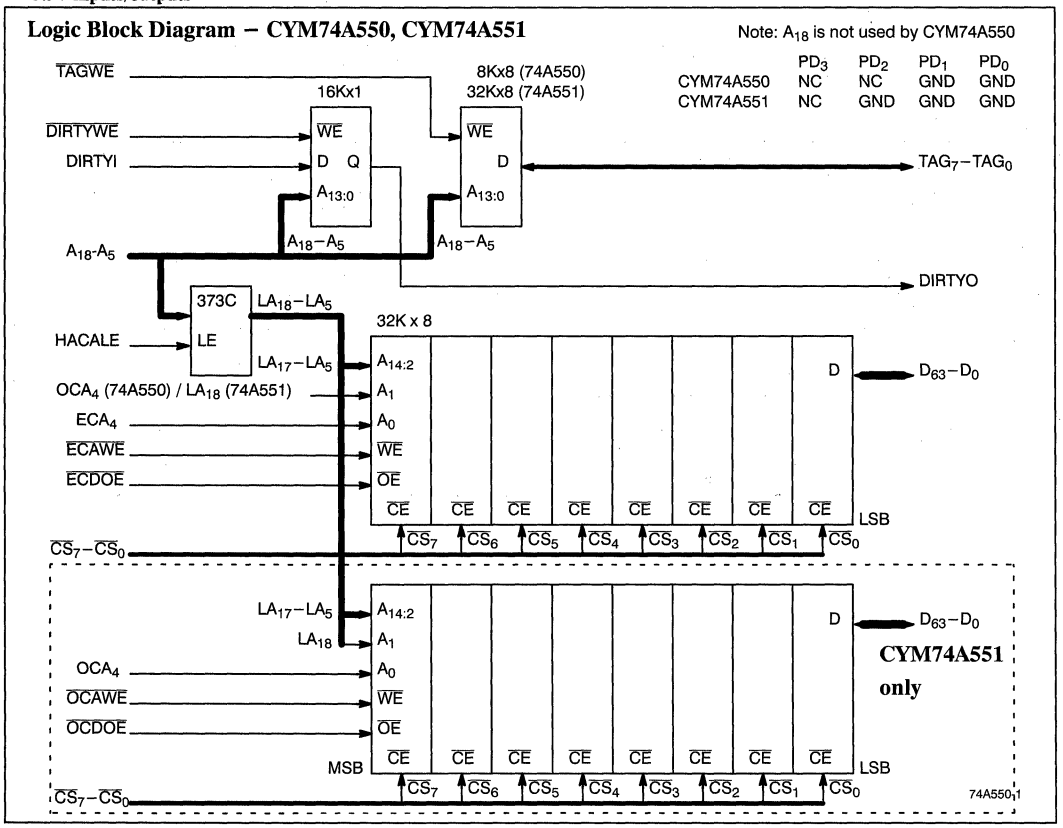
The CYM74S550 and CYM74S551 are high performance synchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules support 3-1-1-1 performance at 66 MHz.

All of these modules include storage for 8 bits of tag and one dirty bit.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V-only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

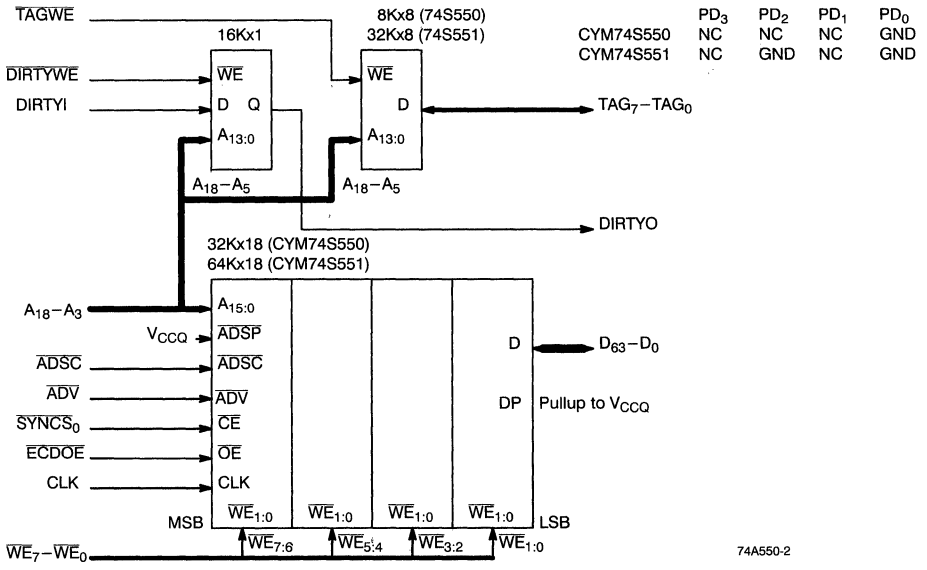
Logic Block Diagram – CYM74A550, CYM74A551



Viper is a trademark of OPTi.
Intel is a trademark of Intel Corporation.

Logic Block Diagram – CYM74S550, CYM74S551

Note: A_{18} is not used by CYM74S550



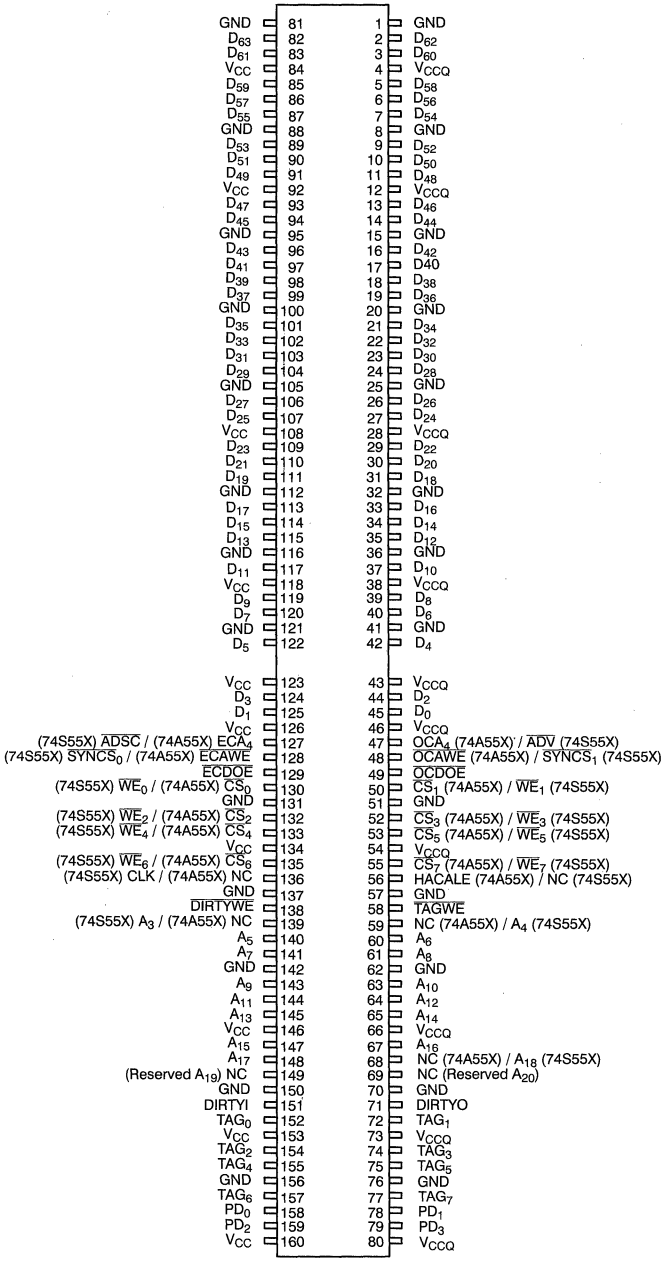
Selection Guide

	Asynchronous Cache Modules					
Part Number	**74A550–50**	**74A550–60**	**74A550–66**	**74A551–50**	**74A551–60**	**74A551–66**
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t_{AA}	25 ns	15 ns	15 ns	25 ns	15 ns	15 ns
Tag t_{AA}	20 ns	15 ns	12 ns	20 ns	15 ns	12 ns

	Synchronous Cache Modules					
Part Number	**74S550–50**	**74S550–60**	**74S550–66**	**74S551–50**	**74S551–60**	**74S551–66**
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t_{CDV}	12 ns	9 ns	9 ns	12 ns	9 ns	9 ns
Tag t_{AA}	20 ns	15 ns	12 ns	20 ns	15 ns	12 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



74A550-3

Pin Definitions

Common Signals	Description
V_{CC}	5V Supply
V_{CCQ}	3.3V Supply
GND	Ground
$A_{18}-A_5$	Addresses from processor
$D_{63}-D_0$	64-bit Data bus from processor
$\overline{ECDOE}$	Even bank output enable input
TAG_7-TAG_0	8-bit Tag RAM bidirectional bus
$\overline{TAGWE}$	Tag RAM write enable input
DIRTYI	1-bit Dirty RAM input
DIRTYO	1-bit Dirty RAM output
$\overline{DIRTYWE}$	Dirty RAM write enable input
PD_3-PD_0	Presence Detect pins
NC	Signal not connected on module.
CYM74A55X Only Signals	**Description**
HACALE	Address Latch Enable input to transparent address latches
OCA_4	Address bit A_3 in single bank async cache module (CYM74A550) Address bit A_4 of odd bank in two bank async cache module (CYM74A551)
ECA_4	Address bit A_4 in single bank async cache module (CYM74A550) Address bit A_4 of even bank in two bank async cache module (CYM74A551)
$\overline{CS_7}-\overline{CS_0}$	Data RAM Chip Select inputs
$\overline{ECAWE}$	Even bank write enable input
$\overline{OCAWE}$	Odd bank write enable input (CYM74A551 only)
CYM74S55X Only Signals	**Description**
CLK	Clock input
A_4-A_3	Lower order address bits from processor
$\overline{ADSC}$	Cache Controller Address Strobe input
$\overline{ADV}$	Burst Address Advance input
$\overline{SYNCS_0}$	Even bank synchronous burst RAM chip select input
$\overline{SYNCS_1}$	Odd bank synchronous burst RAM chip select input (not used)
$\overline{WE_7}-\overline{WE_0}$	Write enable inputs to Data RAMs

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74A550)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74A551)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		2700	mA
I_{CC} (74S550)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74S551)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74A550PM−50C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM−50C	PM32		Async 512 KB	
	CYM74S550PM−50C	PM33		Sync 256 KB	
	CYM74S551PM−50C	PM33		Sync 512 KB	
60	CYM74A550PM−60C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM−60C	PM32		Async 512 KB	
	CYM74S550PM−60C	PM33		Sync 256 KB	
	CYM74S551PM−60C	PM33		Sync 512 KB	
66	CYM74A550PM−66C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM−66C	PM32		Async 512 KB	
	CYM74S550PM−66C	PM33		Sync 256 KB	
	CYM74S551PM−66C	PM33		Sync 512 KB	

Document #: 38−M−00076

PRELIMINARY

VLSI 82C590 Chip Set Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74A590) or synchronous (CYM74S590, CYM74S591) configurations with presence and configuration detect pins**
- **Ideal for Intel P54C-based systems with the VLSI 82C590 chip set**
- **Operates at 60 and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the VLSI 82C590 chip set.

CYM74A590 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution for CPU bus speeds up to 66 MHz. The CYM74A590 is organized as 32K by 64.

The CYM74S590 and CYM74S591 are synchronous cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74S590 is a 256-Kbyte cache module with byte parity.

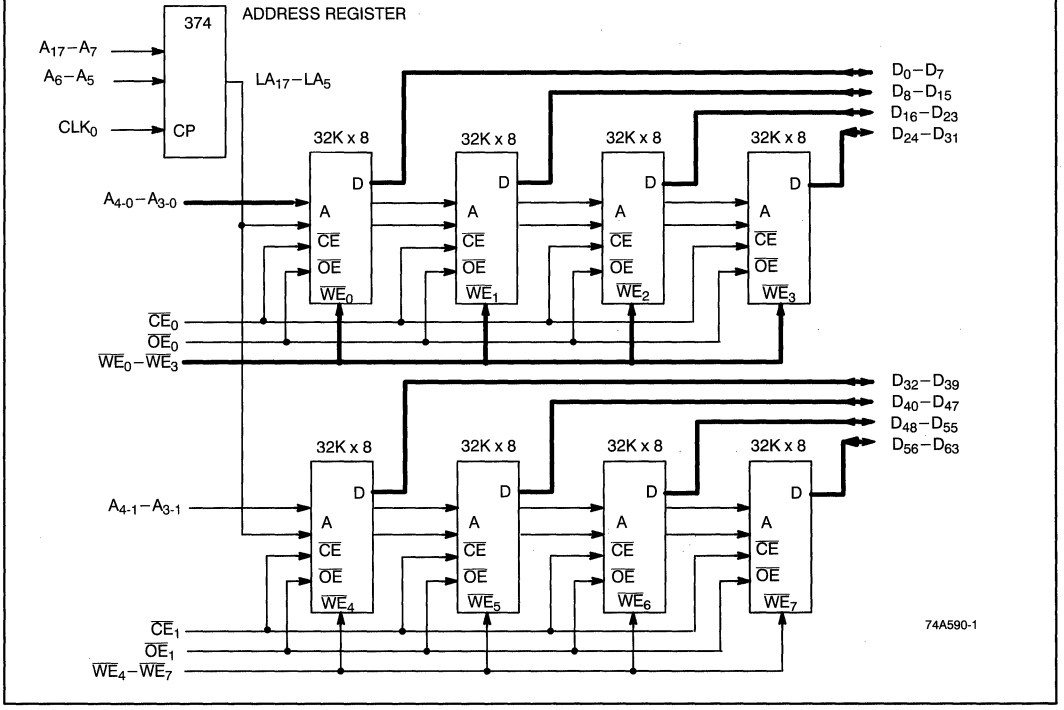
The CYM74S591 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V-only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

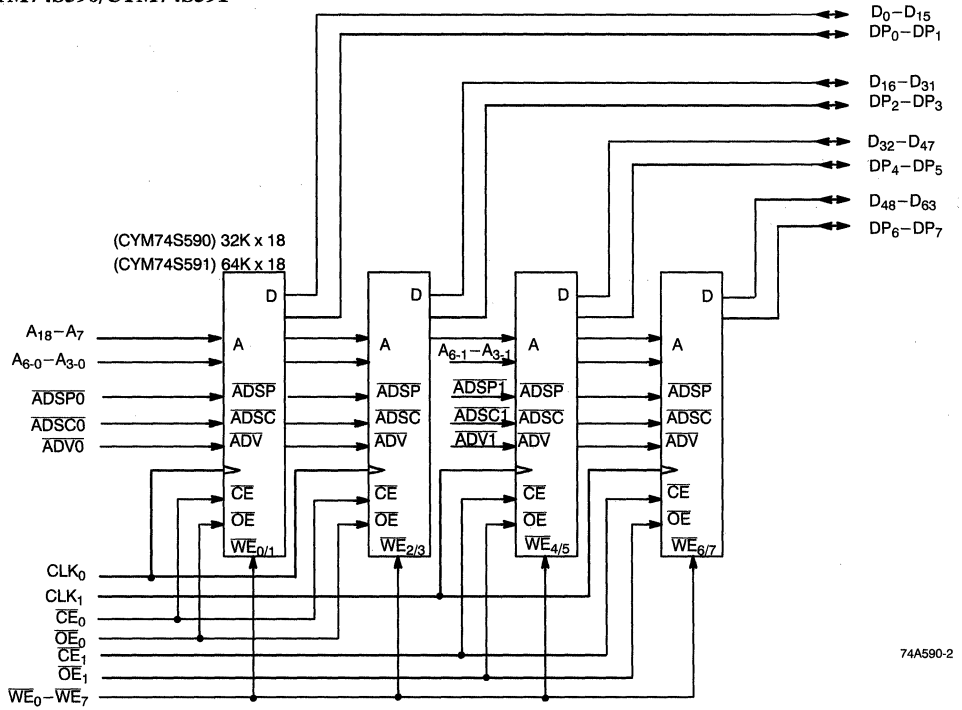
3

Logic Block Diagram – CYM74A590



Intel is a trademark of Intel Corporation.

Logic Block Diagram – CYM74S590/CYM74S591[1]



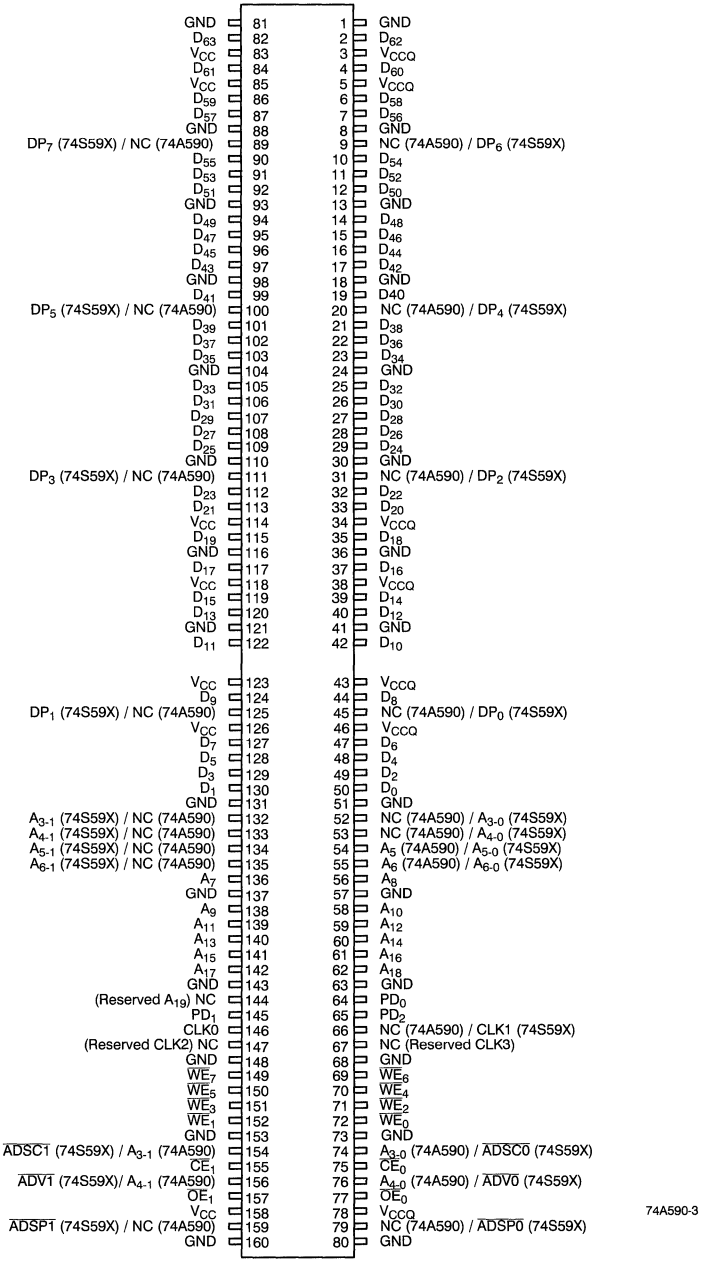
Selection Guide

	74A590–60	74A590–66	74S590–60	74S590–66	74S591–60	74S591–66
Cache Size (KB)	256	256	256	256	512	512
System Clock (MHz)	60	66	60	66	60	66
RAM Clock	Asynchronous	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous
RAM Speed	t_{AA}=15 ns	t_{AA}=15 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns

Notes:
1. A18 is not used by CYM74S590..

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



74A590-3

Pin Definitions

Signal Name	Description
V_{CC}	5V Supply
V_{CCQ}	3.3V Supply
GND	Ground
A_7–A_{19}	Addresses from processor
A_{3-0}, A_{4-0}, A_{5-0}, A_{6-0}	Lower address from chip set for bank0, identical to the bank1 addresses
A_{3-1}, A_{4-1}, A_{5-1}, A_{6-1}	Lower address from chip set for bank1, identical to the bank0 addresses
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable (same signal)
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable (same signal)
$\overline{WE}_0$, $\overline{WE}_1$, $\overline{WE}_2$, $\overline{WE}_3$ $\overline{WE}_4$, $\overline{WE}_5$, $\overline{WE}_6$, $\overline{WE}_7$	Byte Write Enables
CALE	Latch Enable – CYM74A590 only
PD_0–PD_2	Presence Detect pins
D_0–D_{63}	Data lines from processor
DP_0–DP_7	Data Parity lines (Optional), CYM74S590 or CYM74S591 only
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Strobe, CYM74S590 or CYM74S591 only
$\overline{ADSC0}$,$\overline{ADSC1}$	Cache Controller Address Strobe, CYM74S590 or CYM74S591 only
$\overline{ADV0}$, $\overline{ADV1}$	Burst Address Advance – CYM74S590 or CYM74S591 only
CLK0, CLK1, CLK2, CLK3	Clock signals
NC	Signal not connected on module.

Presence Detect Pins

	PD_2	PD_1	PD_0
Asynchronous – CYM74A590	NC	GND	NC
Synchronous – CYM74S590	GND	GND	NC
Synchronous – CYM74S591	GND	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74A590)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74S590)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74S591)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74A590PM−60C	PM25	160-Pin Dual-Readout SIMM	Asynchronous 256 KB	Commercial
	CYM74S590PM−60C	PM26	160-Pin Dual-Readout SIMM	Synchronous 256 KB	
	CYM74S591PM−60C	PM26	160-Pin Dual-Readout SIMM	Synchronous 512 KB	
66	CYM74A590PM−66C	PM25	160-Pin Dual-Readout SIMM	Asynchronous 256 KB	Commercial
	CYM74S590PM−66C	PM26	160-Pin Dual-Readout SIMM	Synchronous 256 KB	
	CYM74S591PM−66C	PM26	160-Pin Dual-Readout SIMM	Synchronous 512 KB	

Document #: 38−M−00075

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYM9230
CYM9231

82420 PCIset-Compatible Level II Cache Modules

Features

- **128K-byte (CYM9230) or 256K-byte (CYM9231) cache moducle organized as 32K by 32 or 64K by 32**
- **Tag width of 9 bits plus valid bit**
- **Independent dirty bit**
- **Operates with systems based on the Intel™ 82420 core logic**
- **Zero-wait state operation at 33 Mhz**
- **Constructed using sandard asynchronous SRAMs**
- **112-pin Burndy Connector, Part Number CELP2X56SC3Z48**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

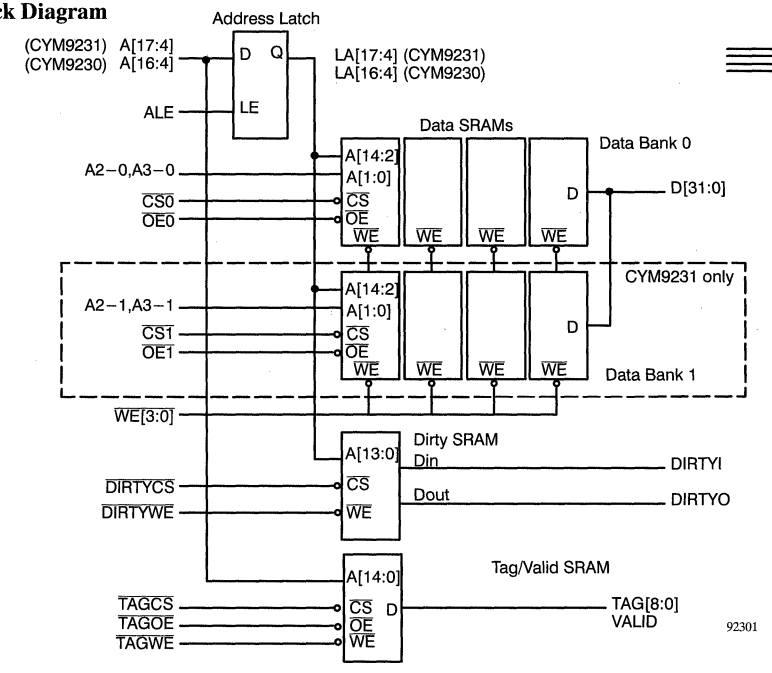
Functional Description

The CYM9230 module series is a family of cache memory subsystems for Intel 486-based systems. The CYM9230 (128Kbytes) contains one memory bank organized as 32K by 32. The CYM9231 (256Kbytes) contains two banks for interleaved operation. In addition, each module contains two SRAMs, supporting a 9-bit tag and valid bit, and a single-bit, separate I/O SRAM supporting a dirty bit. The address signals for the Data and Dirty SRAMs are latched.

These modules are designed for zero wait state operation in 486-based systems operating at a bus speed of 33 Mhz. They are designed for compatibility with the Intel 82420 PCIset and other chip sets. The baseline speed grade is built using 12 nanosecond Tag SRAMs and 20 nanosecond Data SRAMs.

The modules are configured as a 112-pin card-edge memory module. It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

Logic Block Diagram



Selection Guide

	CYM9230PB–20	CYM9231PB–20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

Document #: 38–M–00064–A

CYM9236
CYM9237

128K/256K Cache Module for the UMC491 Chipset

Features

- **128 K-byte (CYM9236) or 256 K-byte (CYM9237) secondary cache module organized as 32K by 32 or 64K by 32**
- **Ideal for Intel™ 486-based systems with the UMC491 chipset**
- **Zero-wait-state operations at 33 MHz**
- **Constructed using cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **112-position Burndy Connector, Part Number CELP2X56SC3Z48**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

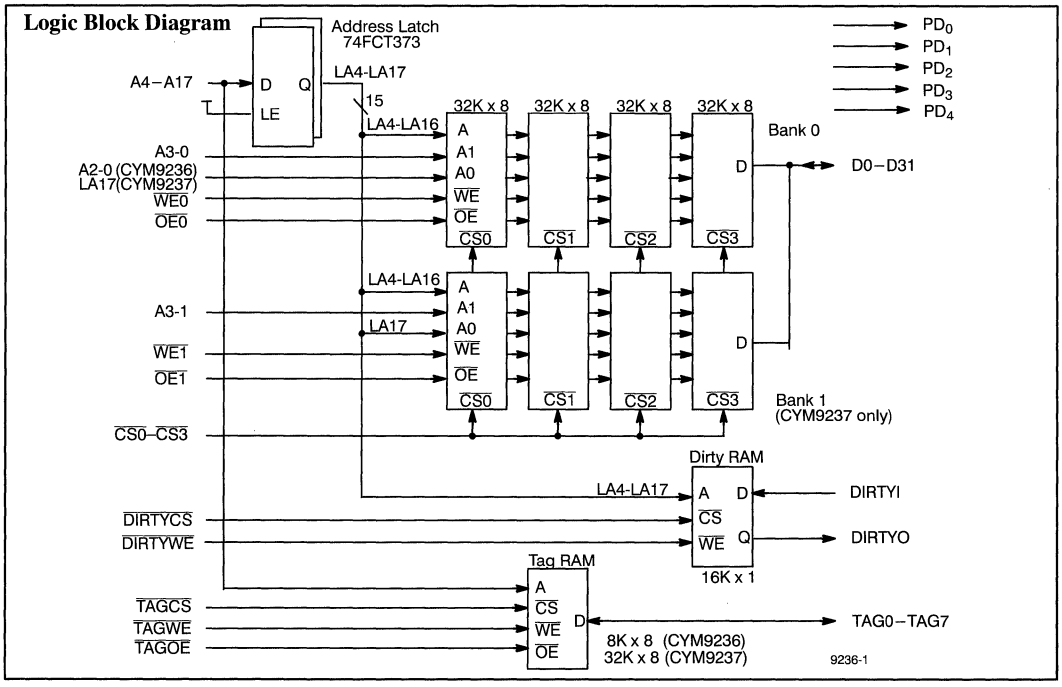
Functional Description

These modules are designed specially to function as the secondary cache in Intel 486-based systems with the UMC491 chipset. Each module contains either one or two banks of 32-bit wide data SRAMs, an 8-bit wide tag RAM, and a single-bit dirty RAM with separate I/O. The addresses for the data and the dirty SRAMs are buffered by an on-board latch. Asynchronous CMOS SRAMs are used to provide a low-cost, low-power, and zero-wait-state solution for CPU speeds up to 33 MHz. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 112-pin Burndy connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) board. The package dimensions are 3.15″ x 0.365″ x 1.1″. All inputs and outputs of the CYM9236 and CYM9237 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.

3

Logic Block Diagram



Selection Guide

	CYM9236PB–20C	CYM9237PB–203C
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	20	20
Tag/Valid SRAM (ns)	15	15

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Document #: 38–M–00069–A

CYM9244, CYM9245 CYM9246, CYM9247

128K/256K Cache Module Family for the OPTi 802GP Chipset

Features

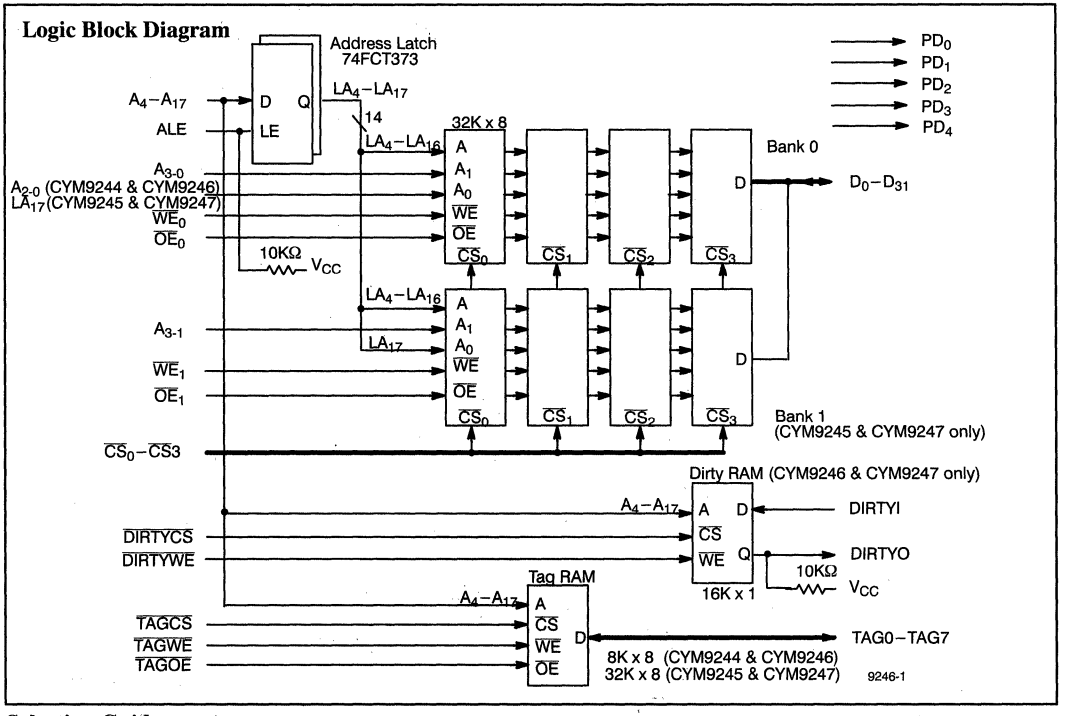
- **128 Kbyte (CYM9244 & CYM9246), 256 Kbyte (CYM9245 & CYM9247), secondary cache modules**
- **Ideal for Intel™ 486 systems with the OPTi 802GP chipset**
- **Zero-wait-state operations at 33 MHz**
- **Constructed using cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **112-position Burndy Connector, Part Number CELP2X56SC3Z48**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

Functional Description

These modules are designed to function as the secondary cache in Intel 486-based systems with the OPTi 802GP chipset. Each module contains either one or two banks of 32-bit wide data SRAMs, an 8-bit wide tag RAM, and a single-bit dirty RAM with separate I/O (CYM9246 and CYM9247 only). The addresses for the data SRAMs are buffered by an on-board latch. Asynchronous CMOS SRAMs are used to provide a low-cost, low-power, and zero-wait-state solution for CPU speeds up to 33 MHz. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 112-pin Burndy connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) board. The package dimensions are 3.15″ x 0.365″ x 1.1″. All inputs and outputs of the CYM9244, CYM9245, CYM9246, and CYM9247 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram



Selection Guide

	CYM9244PB–20C	CYM9245PB–20C	CYM9246PB–20C	CYM9247PB–20C
Cache Size (KB)	128	256	128	256
Data SRAM (ns)	20	20	20	20
Dirty SRAM (ns)			20	20
Tag/Valid SRAM (ns)	15	15	15	15

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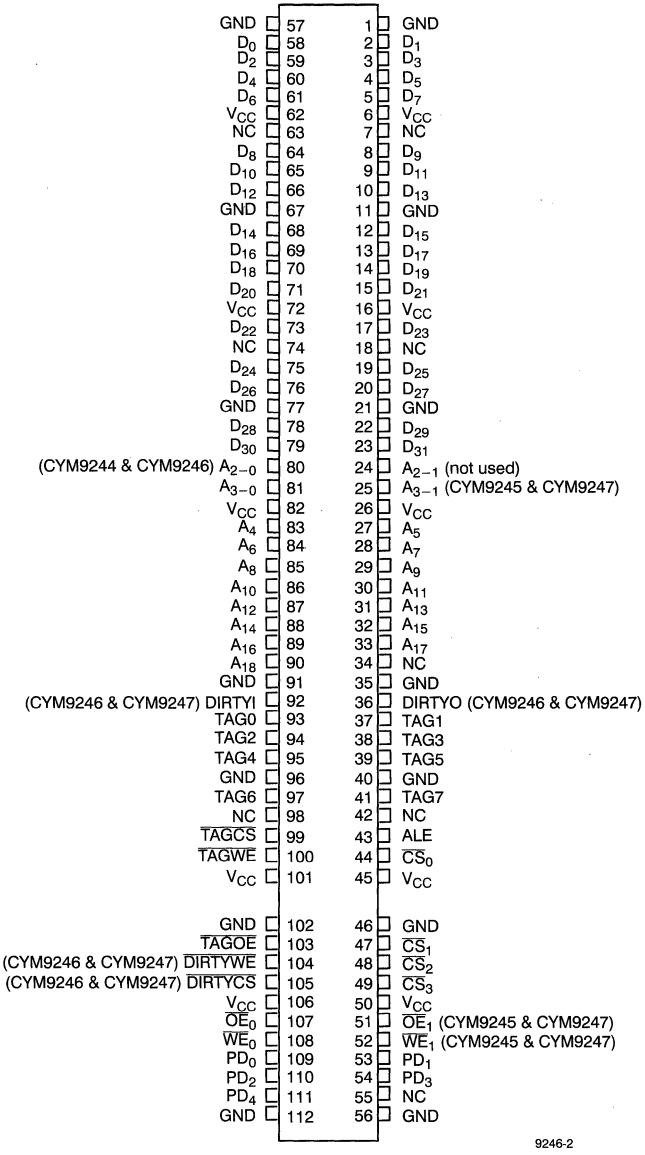
Pin Configuration

Dual Read-out SIMM
Top View



9246-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

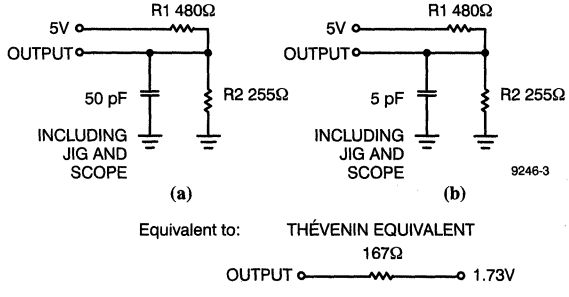
Electrical Characteristics Over the Operating Range

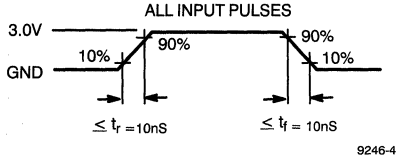
Parameter	Description	Test Conditions	CYM9244, CYM9245, CYM9246, CYM9247 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current (CYM9244)	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		950	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9245)	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1700	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9246)	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1050	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9247)	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1800	mA

Presence Detect Table

	PD_4	PD_3	PD_2	PD_1	PD_0
CYM9244	NC	NC	NC	NC	GND
CYM9245	NC	NC	NC	GND	NC
CYM9246	GND	NC	NC	NC	GND
CYM9247	GND	NC	NC	GND	NC

AC Test Loads and Waveforms





Switching Characteristics

Parameter	Description	Min.	Max.	Unit
ALE Timing				
t_{LE}	ALE HIGH to Change in Latched Address	8.5		ns
t_{PD}	Address Propagation Delay Through FCT373A Latch		5.2	ns
Data SRAM Read Timing				
t_{RC}	Read Cycle Time[1]	27		ns
t_{AA1}	Address Access Time (A_4-A_{17}, Latch Transparent)		27	ns
t_{AA2}	Address Access Time (A_{2-0}, A_{3-0}, A_{3-1}, No Latch Path)		22	ns
t_{OHA}	Output Hold from Address Change[2]	3		ns
t_{OE}	$\overline{OE}$[1:0] LOW to Output Valid		11	ns
t_{CE}	$\overline{CS}$[7:0] LOW to Data Output Valid		22	ns
t_{LZOE}	$\overline{OE}$[1:0] LOW to Low Z[2]	0		ns
t_{HZOE}	$\overline{OE}$[1:0] HIGH to High Z[2]		11	ns
t_{LZCE}	$\overline{CS}$[7:0] LOW to Low Z[2]	3		ns
t_{HZCE}	$\overline{CS}$[7:0] HIGH to High Z[2]		11	ns
t_{PU}	$\overline{CS}$[7:0] LOW to Power-Up[2]	0		ns
t_{PD}	$\overline{CS}$[7:0] HIGH to Power-Down[2]		22	ns
Tag SRAM Read Timing				
t_{TRC}	Tag Read Cycle Time[1]	17		ns
t_{TTAA}	Tag Address Access Time		17	ns
t_{TOHA}	Tag Output Hold from Address Change[2]	3		ns
t_{TCS}	$\overline{TAGCS}$ LOW to Tag Valid		17	ns
t_{TOE}	$\overline{TAGOE}$ LOW to Tag Valid		9	ns
t_{TLZOE}	$\overline{TAGOE}$ LOW to Tag Low Z[2]	0		ns
t_{THZOE}	$\overline{TAGOE}$ HIGH to Tag High Z[2]		10	ns
t_{TLZCE}	$\overline{TAGCS}$ LOW to Tag Low Z[2]	3		ns
t_{THZCE}	$\overline{TAGCS}$ HIGH to Tag High Z[2]		10	ns
t_{TPU}	$\overline{TAGCS}$ LOW to Tag RAM Power-Up[2]	0		ns
Dirty SRAM Read Timing (CYM9246 & CYM 9247)				
t_{DRC}	Dirty Read Cycle Time[1]	22		ns
t_{DAA}	Dirty Address Access Time		22	ns
t_{DOHA}	DIRTYO Hold from Address Change[2]	1		ns
t_{DCS}	$\overline{DIRTYCS}$ LOW to DIRTYO Valid		20	ns
t_{DLZCE}	$\overline{DIRTYCS}$ LOW to DIRTYO Low Z[2]	5		ns
t_{DHZCE}	$\overline{DIRTYCS}$ HIGH to DIRTYO High Z[2]		10	ns
t_{DPU}	$\overline{DIRTYCS}$ LOW to Dirty RAM Power-Up[2]	0		ns
t_{DPD}	$\overline{DIRTYCS}$ HIGH to Dirty RAM Power-Down[2]		17	ns

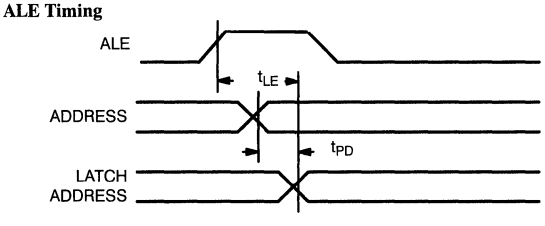
Switching Characteristics (continued)

Parameters	Description	Min.	Max.	Units
Data SRAM Write Timing				
t_{WC}	Write Cycle Time[1]	27		ns
t_{SCE}	$\overline{CS[7:0]}$ LOW to End of Write[1]		22	ns
t_{AW1}	Address Set-Up to End of Write (A_4-A_{17})[1]	20		ns
t_{AW2}	Address Set-Up to End of Write (A_{2-0}, A_{3-0}, A_{3-1}, No Latch Path)[1]	15		ns
t_{HA}	Address Hold from End of Write [2]	0		ns
t_{SA}	Address Set-Up to Start of Write [2]	0		ns
t_{PWE}	$\overline{WE[1:0]}$ Pulse Width[1]	15		ns
t_{SD}	Data Set-Up to End of Write[2]	12		ns
t_{HD}	Data Hold from End of Write[2]	0		ns
t_{LZWE}	$\overline{WE[1:0]}$ LOW to High Z[2]		12	ns
t_{HZWE}	$\overline{WE[1:0]}$ HIGH to Low Z[2]	3		ns
Tag SRAM Write Timing				
t_{TWC}	Tag Write Cycle Time[1]	17		ns
t_{TSCE}	$\overline{TAGCS}$ LOW to End of Tag Write[1]	10		ns
t_{TAW}	Address Set-Up to End of Tag Write [1]	10		ns
t_{THA}	Address Hold from End of Tag Write [2]	0		ns
t_{TSA}	Address Set-Up to Start of Tag Write [2]	0		ns
t_{TWPE}	$\overline{TAGWE}$ Pulse Width[1]	10		ns
t_{TSD}	Tag Set-Up to End of Tag Write[2]	11		ns
t_{THD}	Tag Hold from End of Tag Write[2]	0		ns
t_{TLZWE}	$\overline{TAGWE}$ LOW to Tag High Z[2]		9	ns
t_{THZWE}	$\overline{TAGWE}$ HIGH to Tag Low Z[2]	3		ns
Dirty SRAM Write Timing (CYM9246 & CYM9247)				
t_{DWC}	Dirty Write Cycle Time[1]	27		ns
t_{DDW}	DIRTYI Set-Up to End of Dirty Write [1]	12		ns
t_{DDHW}	DIRTYI Hold from End of Dirty Write [1]	0		ns
t_{DSCE}	$\overline{DIRTYCS}$ LOW to End of Dirty Write[2]	12		ns
t_{DAW}	Address Set-Up to End of Dirty Write [2]	16		ns
t_{DHA}	Address Hold from End of Dirty Write [2]	0		ns
t_{DSA}	Address Set-Up to Start of Dirty Write [2]	0		ns
t_{DWPE}	$\overline{DIRTYWE}$ Pulse Width[1]	12		ns
t_{DLZWE}	$\overline{DIRTYWE}$ LOW to DIRTYO pulled HIGH[2]		9	ns
t_{DHZWE}	$\overline{DIRTYWE}$ HIGH to DIRTYO Low Z[2]	5		ns

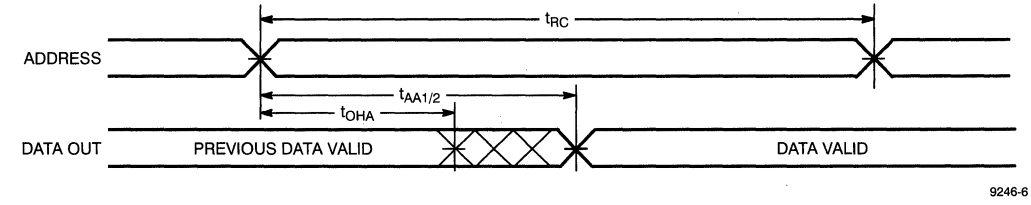
Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Parameters guaranteed by design, not tested.

Switching Waveforms

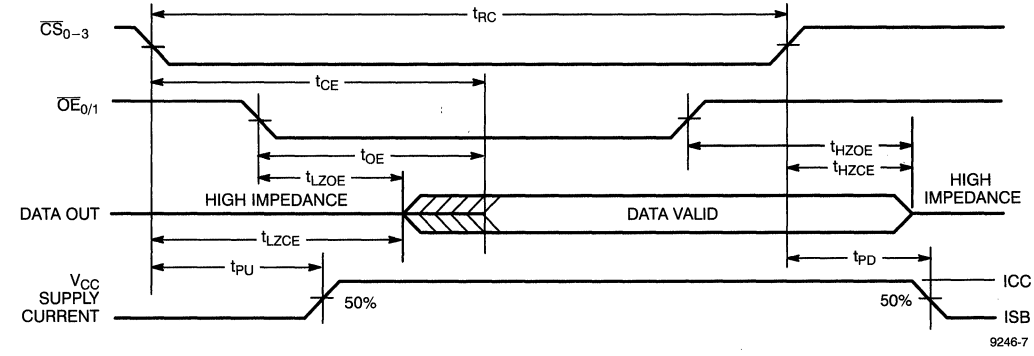
ALE Timing



Data Read Cycle No. 1[3, 4]



Data Read Cycle No. 2[14, 5]

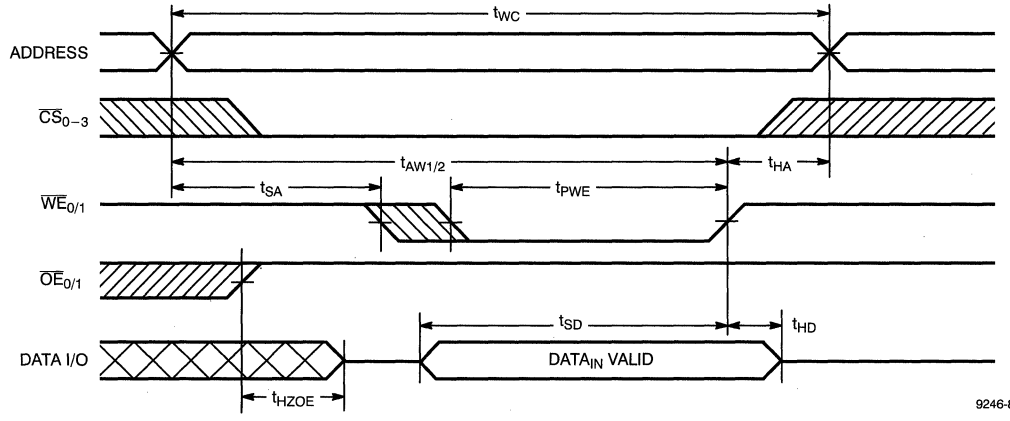


Notes:

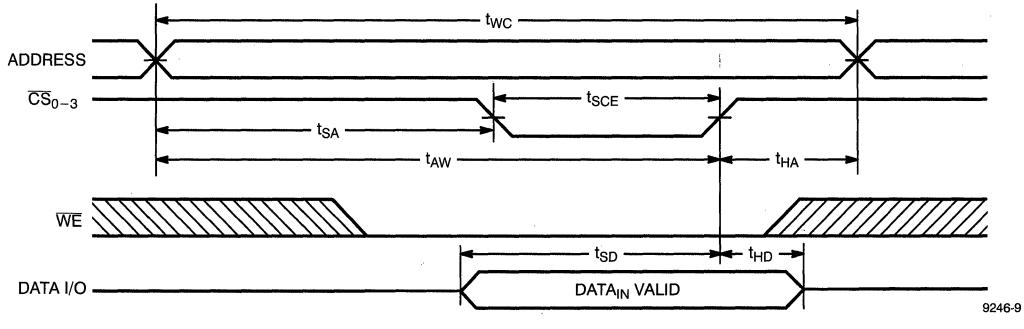
3. Device is continuously selected. $\overline{OE}_{0/1}$, $\overline{CS}_{0-3} = V_{IL}$.
4. $\overline{WE}_{0/1}$ is HIGH for read cycle.
5. Address valid prior to or coincident with $\overline{CS}_0$–$\overline{CS}_3$ transition LOW.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)

Data Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 7, 8]



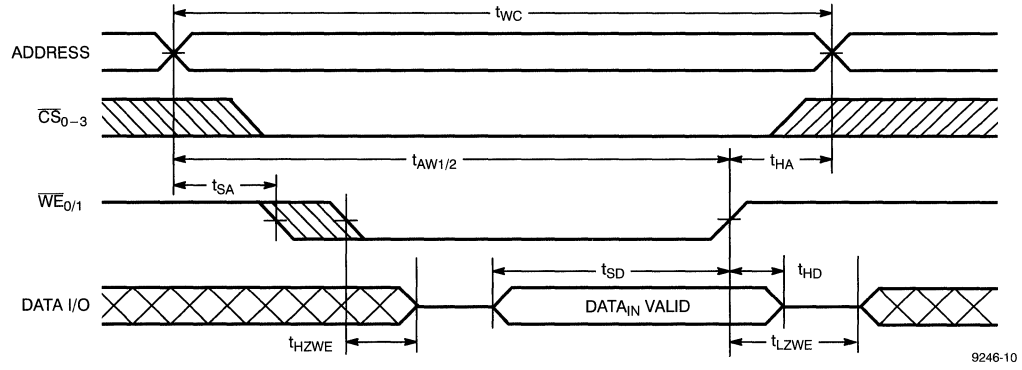
Data Write Cycle No. 2 ($\overline{CS}$[0–3] Controlled)[16, 17, 8]



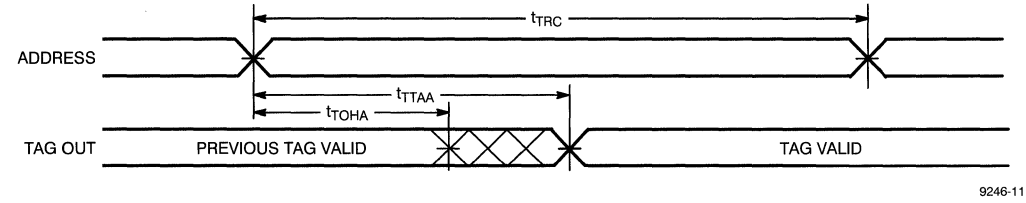
Notes:

7. Data I/O is high impedance if $\overline{OE}$0/1 = V_{IH}.
8. If $\overline{CS}_0$ – $\overline{CS}_3$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Data Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[8, 9]



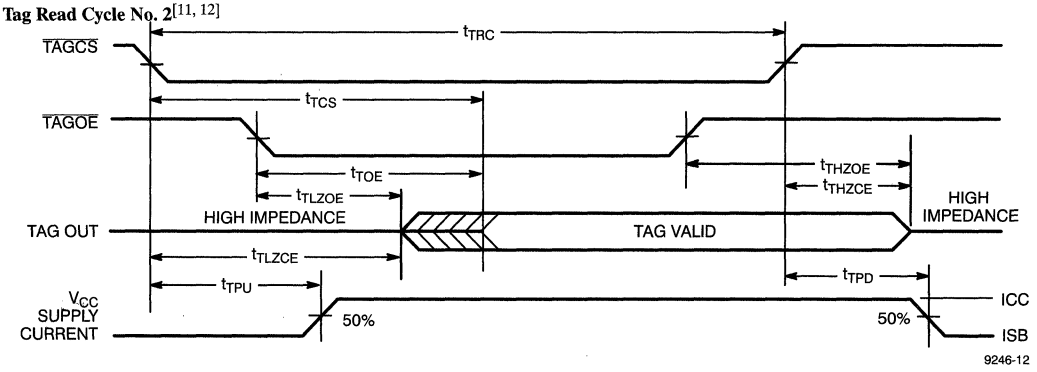
Tag Read Cycle No. 1[10, 11]



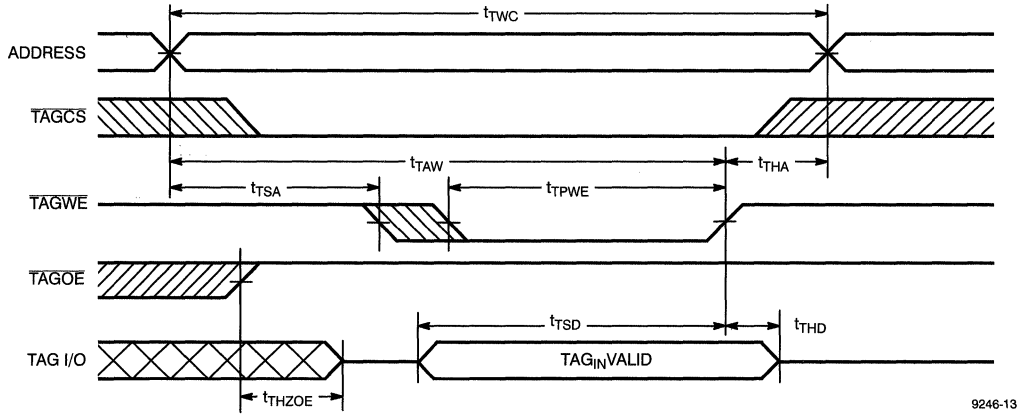
Notes:
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. $\overline{TAGOE}$, $\overline{TAGCS}$ = V_{IL}.
11. $\overline{TAGWE}$ is HIGH for read cycle.

Switching Waveforms (continued)

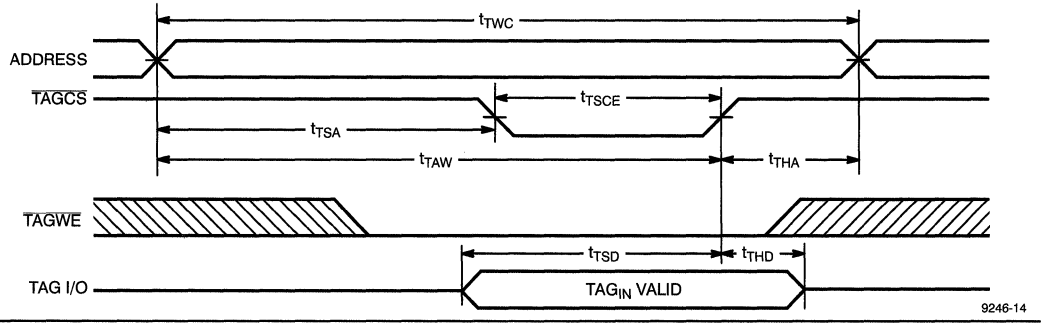
Tag Read Cycle No. 2[11, 12]



Tag Write Cycle No. 1 (TAGWE Controlled)[13, 14, 15]



Tag Write Cycle No. 2 (TAGCS Controlled)[13, 14, 15]

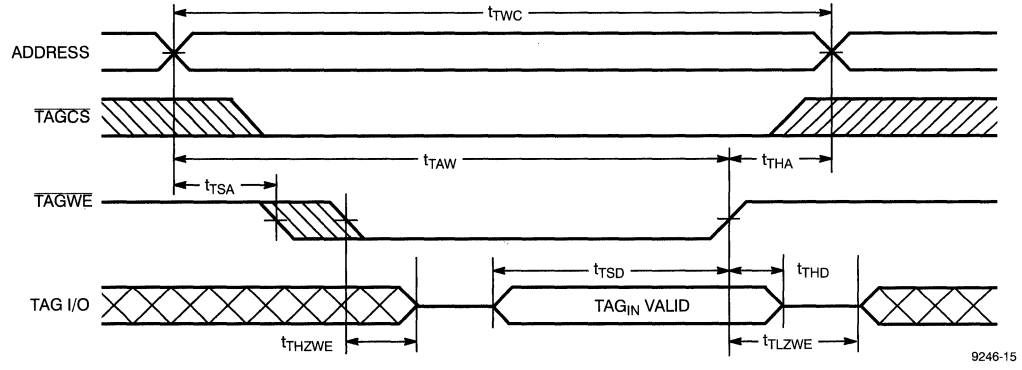


Notes:

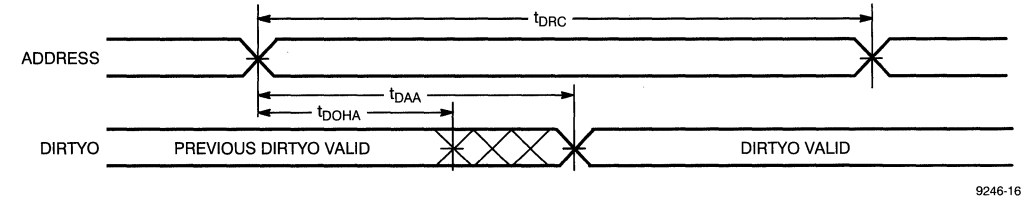
12. Address valid prior to, or coincident with $\overline{\text{TAGCS}}$ transition LOW.
13. The internal write time of the memory is defined by the overlap of $\overline{\text{TAGCS}}$ LOW and $\overline{\text{TAGWE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. TAG I/O is high impedance if $\overline{\text{TAGOE}}$ = LOW.

Switching Waveforms (continued)

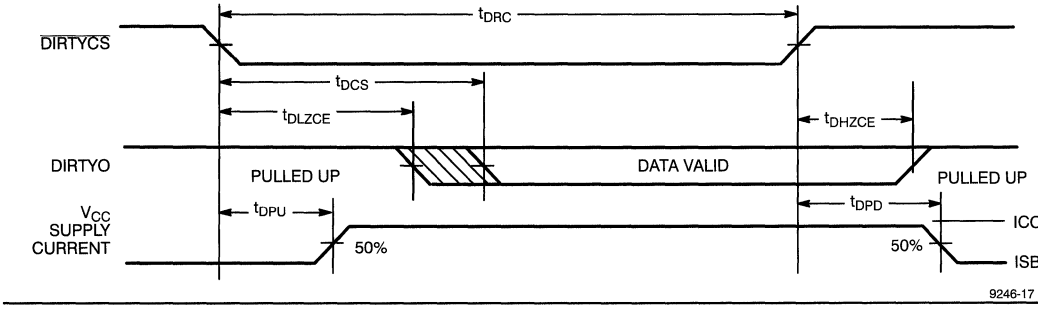
Tag Write Cycle No. 3 ($\overline{TAGWE}$ Controlled, $\overline{TAGOE}$ LOW)[15]



Dirty Read Cycle No. 1[16, 17]



Dirty Read Cycle No. 2[11, 18]

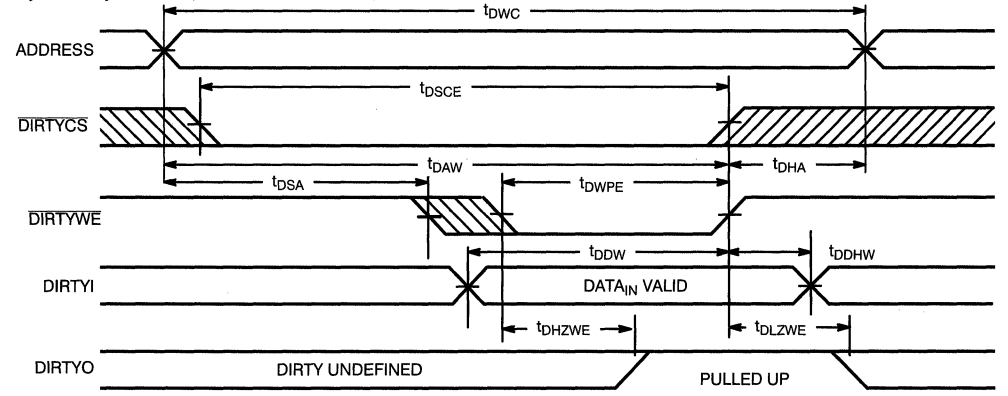


Notes:

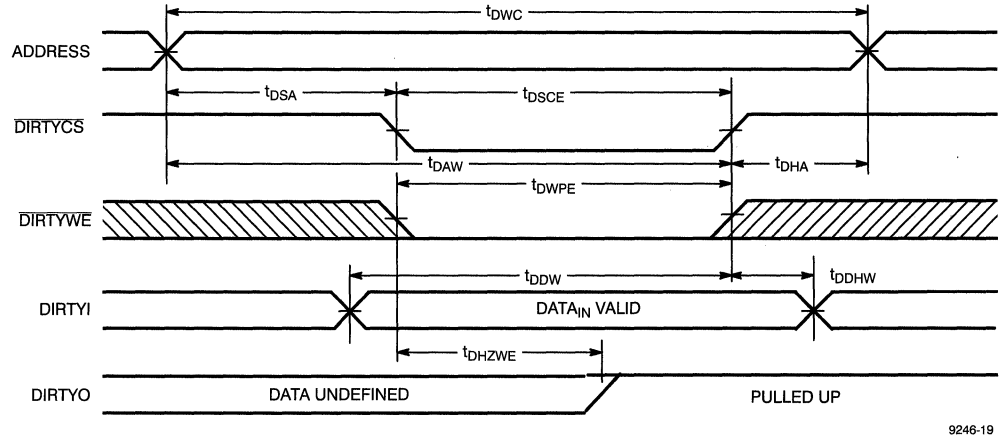
15. If $\overline{TAGCE}$ goes HIGH simultaneously with $\overline{TAGWE}$ HIGH, the output remains in a high-impedance state.
16. $\overline{DIRTYWE}$ is high for read cycle.
17. Device is continuously selected, $\overline{DIRTYCS}$ = V_{IL}.
18. Address valid prior to or coincident with $\overline{DIRTYCS}$ transition LOW.

Switching Waveforms (continued)

Dirty Write Cycle No. 1 ($\overline{\text{DIRTYWE}}$ Controlled)[19]



Dirty Write Cycle No. 2 ($\overline{\text{DIRTYCS}}$ Controlled)[19, 20]



Notes:

19. The internal write time of the memory is defined by the overlap of $\overline{\text{DIRTYCS}}$ LOW and $\overline{\text{DIRTYWE}}$ LOW. Both signals msut be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
20. If $\overline{\text{DIRTYCS}}$ goes HIGH simultaneously with $\overline{\text{DIRTYWE}}$ HIGH, the output remains in a high-impedance state.

Ordering Information

Cache Memory Size	Ordering Code	Package Name	Package Type	Operating Range
128 Kbyte	CYM9244PB–20C	PB17	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM9245PB–20C	PB18	112-Pin Dual-Readout SIMM	Commercial
128 Kbyte	CYM9246PB–20C	PB17	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM9247PB–20C	PB18	112-Pin Dual-Readout SIMM	Commercial

Document #: 38–M–00072

Section Contents

Non-Volatile Memories

Introduction to CMOS Non-Volatile Memories

Product Line Overview

The Cypress CMOS family of high-performance byte-wide and word-wide (x16) non-volatile memories spans 4-kilobit to 1-megabit densities and three functional configurations. Products are typically available as EPROMs (Erasable, Programmable ROMs) in 300- and 600-mil windowed cerDIP packages, leadless chip carriers (LCCs), leaded chip carriers (CLCC, PLCC) and flatpacks. They are also available as PROMs in similarly configured plastic and opaque hermetic packages. With the exception of the 4K PROMs (registered only) and 1M EPROMs, all densities are available in both registered and non-registered versions. The registered devices operate in either synchronous or asynchronous modes and may have an INITIALIZATION feature to preload the pipeline register, which allows the pipeline register to be loaded or examined via a serial path.

Cypress PROMs perform at or above the speed level of their bipolar counterparts with the advantages of lower power consumption and reprogrammability inherent in CMOS technology. They operate with 10% power supply tolerances and can withstand 2000 volts of electrostatic discharge.

Technology Introduction

Cypress non-volatile memories are executed in N-well CMOS EPROM processes that provide basic gate delays of 235 picoseconds for a fanout of one with a power consumption of 45 femtojoules. These processes provide the basis for the development of Cypress LSI products, which outperform the fastest bipolar equivalents.

Historically, CMOS static RAMs have challenged bipolar RAMs for speed, while CMOS PROMs have been slower than the fused bipolar devices because (1) the typical single transistor CMOS cell is slow compared to any "fuse," and (2) CMOS technologies were optimized for programmability and density at the expense of speed. Innovative Cypress EPROM technology overcomes both of these historical limitations. A substrate bias generator is employed in an EPROM technology to improve performance and raise latch-up immunity to greater than 200 mA. The result is a CMOS EPROM technology that outperforms bipolar fuse technology for both density and speed, particularly at higher densities. Limitations of devices implemented in the bipolar fuse technology such as programming yield, power dissipation and higher-density performance are eliminated or greatly reduced using Cypress CMOS EPROM technology.

Programming

Differential Memory Cells

Cypress non-volatile memories are programmed a byte at a time by applying V_{PP} (~12V) to the programming pin and the desired logic levels to input pins. Both logic 1 and logic 0 are programmed into the differential cell. A bit is programmed by applying V_{PP} on the control gate and 9 volts on the drain of the floating-gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate, thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts, resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is the corrected logic state. Because an unprogrammed cell has neither a 1 nor a 0 in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference, which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual bits allowing the monitoring of the quality of programming during the manufacturing operation.

Single-Ended Memory Cells (All CY7C products except CY7C271A, CY27C128, and CY27C256)

The programming mechanism of the EPROM transistor in a single-ended memory cell is the same as its counterpart in a double-ended memory cell. The difference is that only 1s are programmed in a single-ended cell. A 1 applied to the I/O pin during programming causes an erased EPROM transistor to be programmed, while a 0 allows the EPROM transistor to remain unprogrammed. Erasure resets all bits to 0.

Single-Ended Memory Cells (All CY27H and CY27C products except CY27C128, and CY27C256)

These devices are similar except that 0s are programmed. A 1 does not program a bit. After erasure, all bits are reset to 1.

Erasability

This is available for devices in windowed packages, both registered and non-registered. Wavelengths of light less than 4000 Angstroms begin to erase Cypress non-volatile memories. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mV/cm^2 power rating, the exposure time would be approximately 35 minutes.

The device needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity light for an extended period of time. The recommended maximum dosage is 7258 Wsec/cm^2.

Some devices are sensitive to photo-electric effects during programming. Cypress recommends covering the windows of reprogrammable devices during programming.

Reliability

CMOS technology has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed an erased multiple times, CMOS PROMs from Cypress can be tested 100% for programmability during the manufacturing process. Because each device contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged, thus assuring the user that not only will every cell program, but that the product performs to the specification.

General Testing Information

Incoming test procedures on high speed (faster that 45 ns) devices should be carefully planned, taking into account the high-performance and output drive capabilities of the parts. The following notes may be useful:

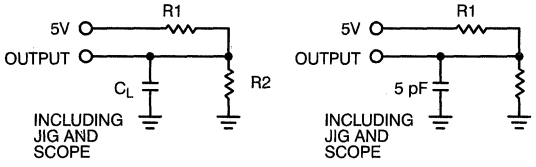
- Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 µF or larger capacitor and a 0.01 µF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in

large variations of power supply voltage, creating erroneous function or transient performance failures.

- All device test loads should be located within 2″ of device outputs.
- Do not leave any inputs disconnected (floating) during any tests.
- Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
- V_{OH} and V_{OL} are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- Capacitance is tested initially and after any design or process changes that may affect these parameters.
- The CMOS process does not provide a clamp diode. However, the Cypress PROM Products are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50%).

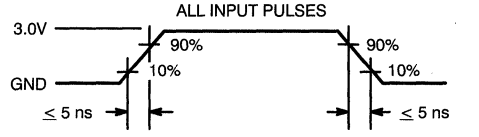
Switching Tests

AC Test Loads and Waveforms



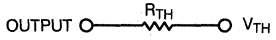
(a) Normal Load **(b) High Z Load**

INTRO-1



INTRO-2

Equivalent to: THÉVENIN EQUIVALENT



Load circuit (a) is used to test all switching characteristics except High Z parameters. Load circuit (b) is used to test High Z parameters. R1 is a resistor connected from the output to V_{CC} and R2 is connected between the output and ground for testing purposes.

Values of R1 and R2 are given in the individual datasheet for each product. Speed is measured at 1.5V reference levels except for delay to output High Z.

Document #: 38−00234−A

CY27C64

8K x 8 EPROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 70 ns (commercial)**
- **Low power**
  - **— 440 mW (commercial)**
  - **— 530 mW (military)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**

Functional Description

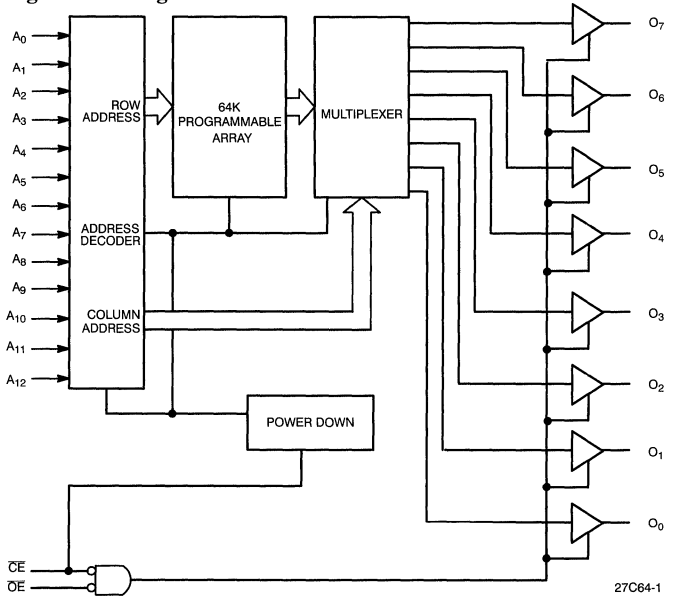
The CY27C64 is a high-performance 8192 word by 8 bit CMOS PROM. When deselected, the CY27C64 automatically powers down into a low-power standby mode. It is packaged in a 600-mil-wide package. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these EPROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The EPROM cell requires only 12.5V for the super voltage and low-current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each EPROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 through A_{12}) will become available on the output lines (O_0 through O_7).

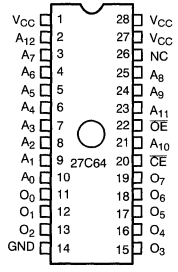
4

Logic Block Diagram



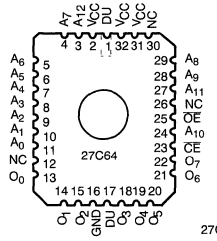
Pin Configurations

DIP/CerDIP
Top View



27C64-23

PLCC[1]
Top View



27C64-34

Selection Guide

		27C64–70	27C64–90	27C64–120	27C64–150	27C64–200
Maximum Access Time (ns)		70	90	120	150	200
Maximum Operating Current (mA)	Commercial	80	80	80	80	80
	Military	100	100	100	100	100
Maximum Standby Current (mA)	Commercial	15	15	15	15	15
	Military	15	15	15	15	15

Note:
1. Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (DIP Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	−40°C to +85°C	5V ± 10%
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0		V
V_{IL}	Input LOW Voltage				0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 5		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA f=10 MHz	Com'l		80	mA
			Mil		100	
I_{SB}	Standby Supply Current	Chip Enable Inactive, $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA	Com'l		15	mA
			Mil		15	

Capacitance[5]

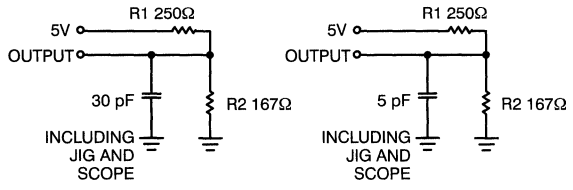
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. Contact a Cypress representative regarding industrial temperature range specification.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. See the "Introduction to CMOS NVMs" section of the Cypress Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

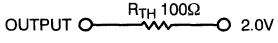
AC Test Loads and Waveforms

Test Load



(a) Normal Load **(b) High-Z Load** 27C64-45

Equivalent to: THÉVENIN EQUIVALENT



4

Switching Characteristics Over the Operating Range[2, 3, 5]

Parameter	Description	27C64–70		27C64–90		27C64–120		27C64–150		27C64–200		Unit
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{HZCE}	Chip Enable Inactive to High Z		45		45		45		45		45	ns
t_{HZOE}	Output Enable Inactive to High Z		25		25		30		30		30	ns
t_{OE}	Output Enable Active to Output Valid		40		40		50		50		50	ns
t_{CE}	Chip Enable Active to Output Valid		70		90		120		150		200	ns
t_{OH}	Data Hold from Address Change	3		3		3		3		3		ns
t_{PU}	Chip Enable Active to Power-Up		70		90		120		150		200	ns
t_{PD}	Chip Enable Inactive to Power-Down		70		90		120		150		200	ns

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C64 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative. When programming, select the Cypress CY7C266 algorithm.

Table 1. Mode Selection

Mode		Pin Function[7, 8]							
	Normal Operation	**A_8**	**A_9**	**A_{10}**	**A_{11}**	**A_{12}**	**$\overline{CE}$**	**$\overline{OE}$**	**$D_7 - D_0$**
	Program	**$\overline{VFY}$**	**$\overline{PGM}$**	**LAT**	**NA**	**NA**	**$\overline{CE}$**	**V_{PP}**	**$D_7 - D_0$**
Read		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IL}	$O_7 - O_0$
Standby		X	X	X	X	X	V_{IH}	X	Three-Stated
Output Disable		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IH}	Three-Stated
Program		V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	Three-Stated
Blank Check		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$

Notes:
7. X = "don't care" but must not exceed V_{CC} + 5%.
8. Address $A_8 - A_{12}$ must be latched through lines $A_0 - A_4$ in Programming modes.

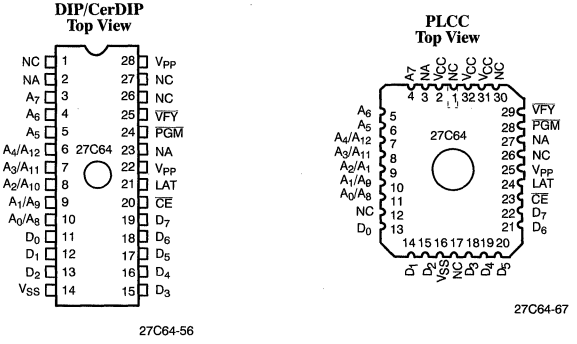
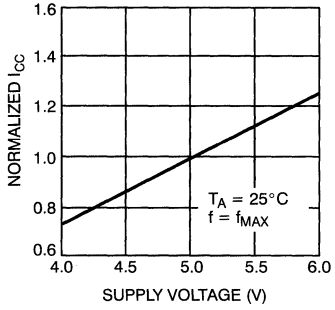


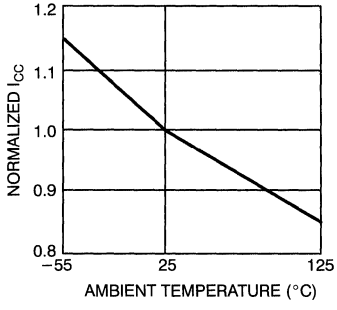
Figure 1. Programming Pinout

Typical DC and AC Characteristics

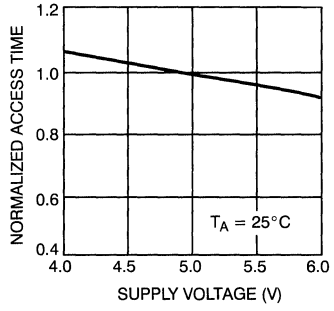
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



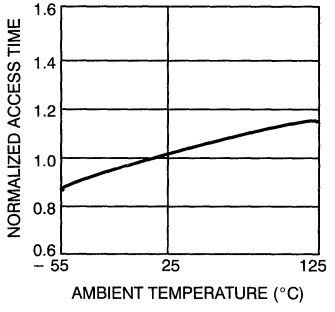
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



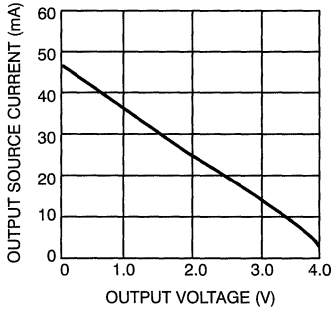
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



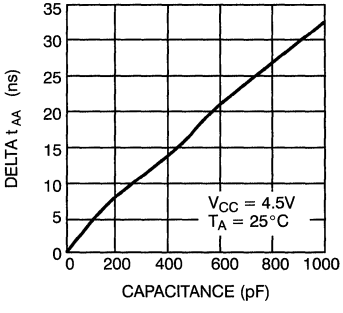
NORMALIZED ACCESS TIME vs. TEMPERATURE



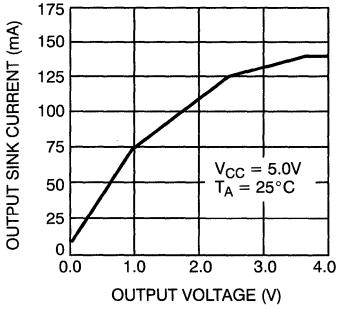
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C64–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64–70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
90	CY27C64–90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64–90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64–90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
120	CY27C64–120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64–120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64–120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
150	CY27C64–150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64–150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64–150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
200	CY27C64–200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64–200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64–200WC	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38–00448

128K x 8 CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 70 ns max.**
- **Low power**
  - **— 220 mW max.**
  - **— Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 32-pin TSOP-I**
  - **— 32-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

The CY27C010 is a high-performance, 1-megabit CMOS EPROM organized in 128 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, 32-pin LCC and PLCC, and 32-pin TSOP-I packages. The CY27C010 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

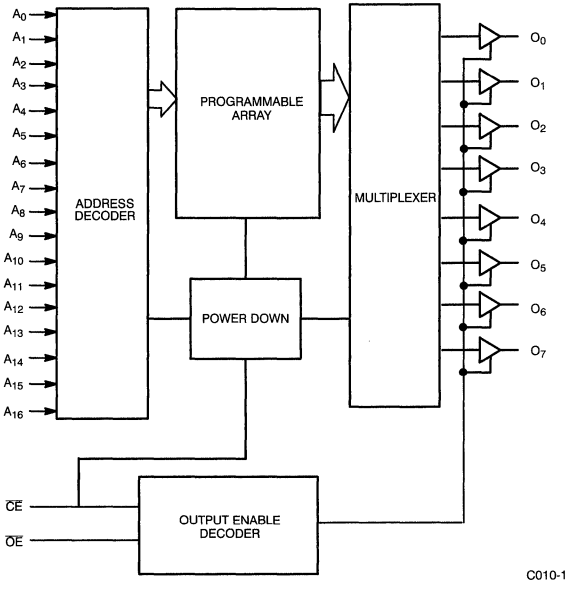
The CY27C010 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27C010 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{16}-A_0$ will appear at the outputs O_7-O_0.

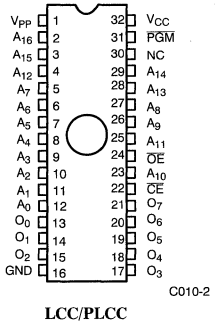
4

Logic Block Diagram

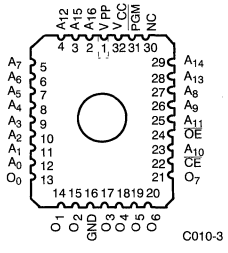


Pin Configurations

DIP
Top View

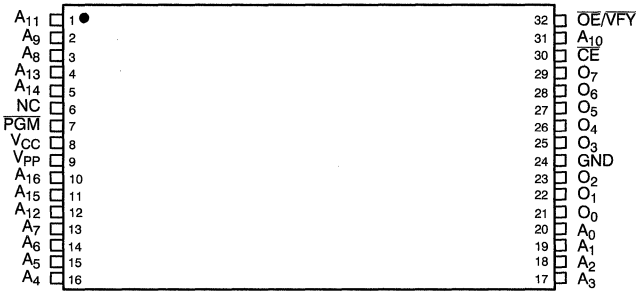


LCC/PLCC
Top View



Pin Configurations (continued)

TSOP
Top View



C010-4

Selection Guide

		27C010–70	27C010–90	27C010–120	27C010–150	27C010–200
Maximum Access Time (ns)		70	90	120	150	200
$\overline{CE}$ Access Time (ns)		70	90	120	150	200
$\overline{OE}$ Access Time (ns)		25	30	40	50	60
I_{CC}[1] (mA) Power Supply Current	Com'l	40	40	40	40	40
	Mil	50	50	50	50	50
I_{SB}[2] (mA) Stand-by Current	Com'l	15	15	15	15	15
	Mil	25	25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[3]	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
3. Contact a Cypress representative for industrial temperature range specification.
4. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[5, 6]

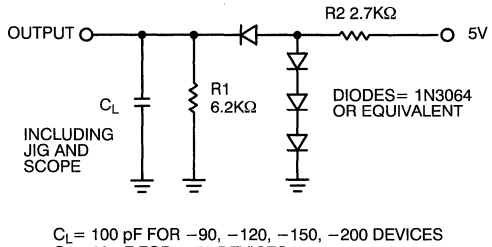
Parameter	Description	Test Conditions		27C010–70, 27C010–90, 27C010–120, 27C010–150, 27C010–200 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=5 MHz	Com'l		40	mA
			Mil		50	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15	mA
			Mil		25	mA

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

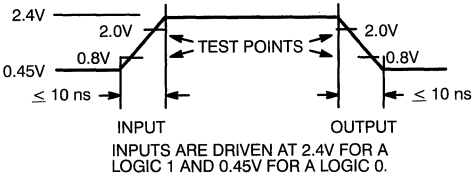
Notes:
5. See the last page of this specification for Group A subgroup testing information.
6. See Introduction to CMOS NVMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

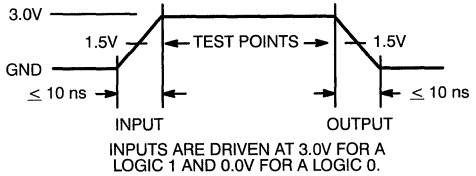


C_L= 100 pF FOR −90, −120, −150, −200 DEVICES
C_L= 30 pF FOR −70 DEVICES

C010-5



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 AND 0.45V FOR A LOGIC 0.



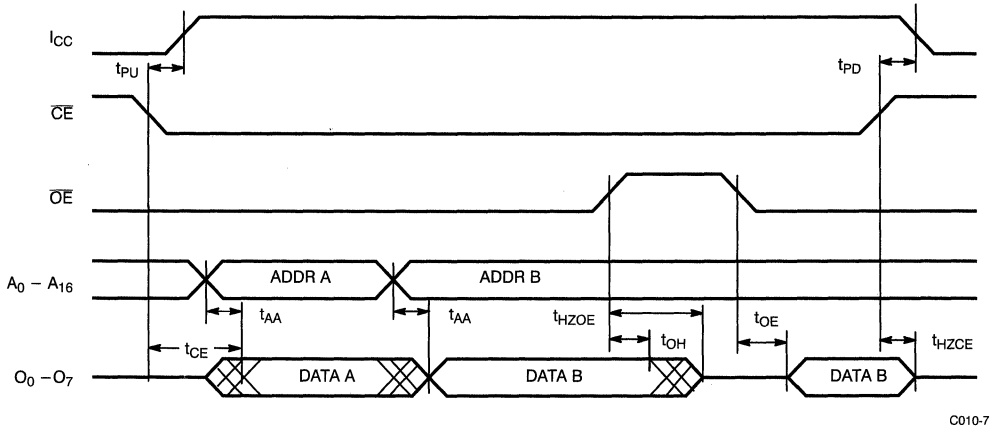
INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC 1 AND 0.0V FOR A LOGIC 0.

C010-6

Switching Characteristics Over the Operating Range

Parameter	Description	27C010–70		27C010–90		27C010–120		27C010–150		27C010–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		25		30		40		50		60	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		25		30		40		50		60	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		25		30		30		30		30	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		60		65		65		65		65	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform



C010-7

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C010 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C010 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function[7]						
	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A_0	A_9	Data
Read	V_{IL}	V_{IL}	X	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	X	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{HV}[8]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_{HV}[8]	1DH[9]

Note:
7. X can be V_{IL} or V_{IH}.
8. V_{HV}=12V±0.5V
9. Subject to change before final version.

Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C010–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010–70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C010–70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010–70ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010–70DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C010–70WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
90	CY27C010–90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010–90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010–90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010–90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010–90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010–90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010–90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C010–90WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
120	CY27C010–120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010–120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010–120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010–120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010–120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010–120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010–120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C010–120WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
150	CY27C010–150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010–150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010–150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010–150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010–150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010–150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010–150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C010–150WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
200	CY27C010–200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C010–200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C010–200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C010–200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C010–200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C010–200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C010–200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C010–200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38–00428

CY27C020

256K x 8 CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 70 ns max.**
- **Low power**
  - **— 140 mW max.**
  - **— Less than 550 µW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 32-pin TSOP-I**
  - **— 32-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

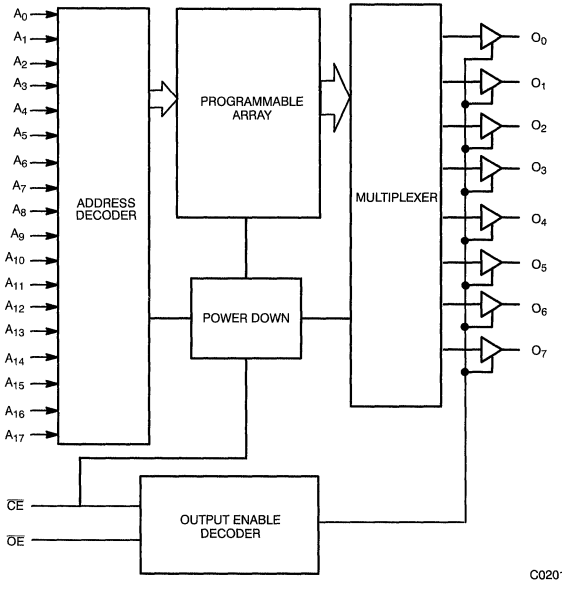
The CY27C020 is a high-performance, 2-megabit CMOS EPROM organized in 256 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, 32-pin LCC and PLCC, and 32-pin TSOP-I packages. The CY27C020 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27C020 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

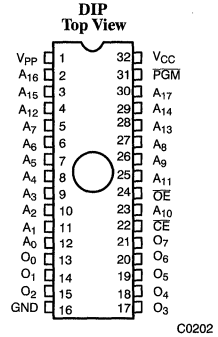
The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

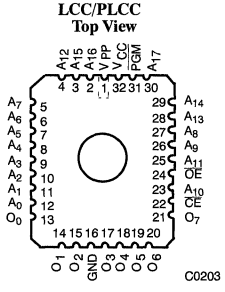
The CY27C020 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{17}-A_0$ will appear at the outputs O_7-O_0.

Logic Block Diagram



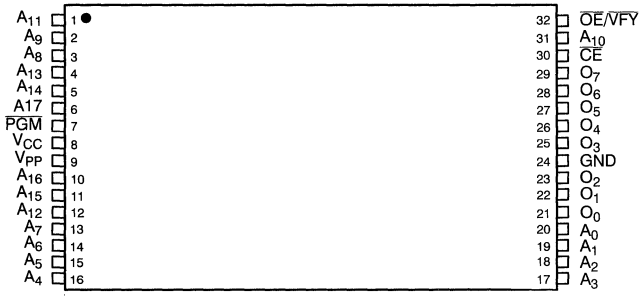
Pin Configurations





Pin Configurations (continued)

TSOP
Top View



Selection Guide

		27C020–70	27C020–90	27C020–120	27C020–150	27C020–200
Maximum Access Time (ns)		70	90	120	150	200
$\overline{CE}$ Access Time (ns)		70	90	120	150	200
$\overline{OE}$ Access Time (ns)		30	35	40	50	60
I_{CC}[1] (mA) Power Supply Current	Com'l	25	25	25	25	25
	Mil		30	30	30	30
I_{SB}[2] (μA) CMOS Stand-by Current		100	100	100	100	100
I_{SB}[3] (mA) TTL Stand-by Current		1	1	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{CC} − 0.3V to V_{CC} + 1.0V.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=5 MHz	Com'l		25	mA
			Mil		30	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		1	mA
			Mil		1	mA

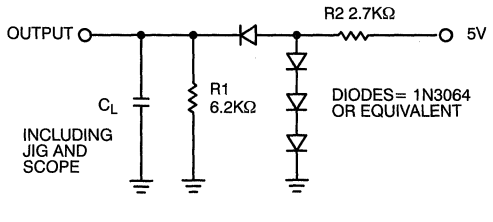
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

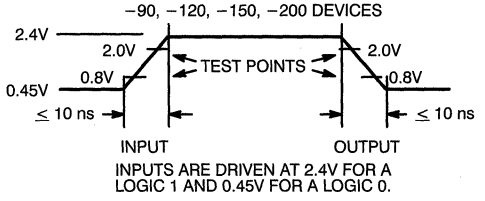
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

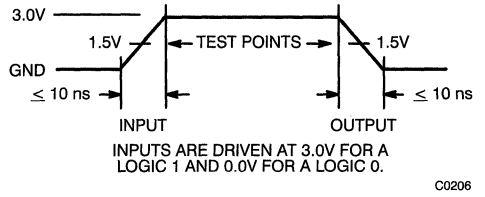
AC Test Loads and Waveforms



C_L= 100 pF FOR −90, −120, −150, −200 DEVICES
C_L= 30 pF FOR −70 DEVICES

C0205



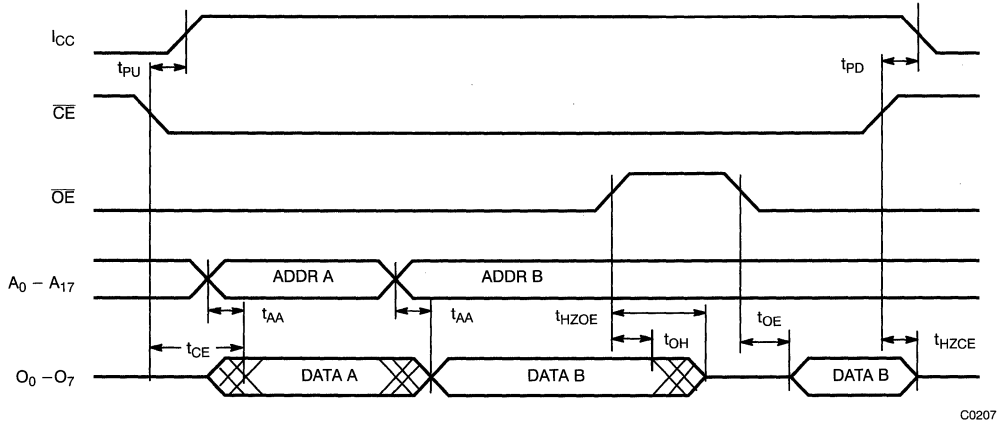


C0206

Switching Characteristics Over the Operating Range

Parameter	Description	27C020–70		27C020–90		27C020–120		27C020–150		27C020–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		30		35		40		50		60	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		25		25		30		30		40	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		25		25		30		30		40	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		60		65		65		65		70	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform



C0207

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C020 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C020 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection

	Pin Function[8]						
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A_0	A_9	**Data**
Read	V_{IL}	V_{IL}	X	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	X	V_{IH}	A_0	A_9	High Z
Stand-by (CMOS)	V_{CC} − 0.3V	X	X	V_{IH}	X	X	High Z
Stand-by (TTL)	V_{IH}	X	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_{HV}[8]	Note 10

Note:
8. X can be V_{IL} or V_{IH}.
9. V_{HV}=12V±0.5V
10. To be determined.

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C020–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C020–70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–70ZC	Z32	32-Lead Thin Small Outline Package	
90	CY27C020–90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–90WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
120	CY27C020–120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–120WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
150	CY27C020–150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–150WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
200	CY27C020–200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C020–200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C020–200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C020–200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C020–200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C020–200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C020–200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C020–200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:
11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38−00449

512K x 8 CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 70 ns max.**
- **Low power**
  - **— 140 mW max.**
  - **— Less than 550 µW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 32-pin TSOP-I**
  - **— 32-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

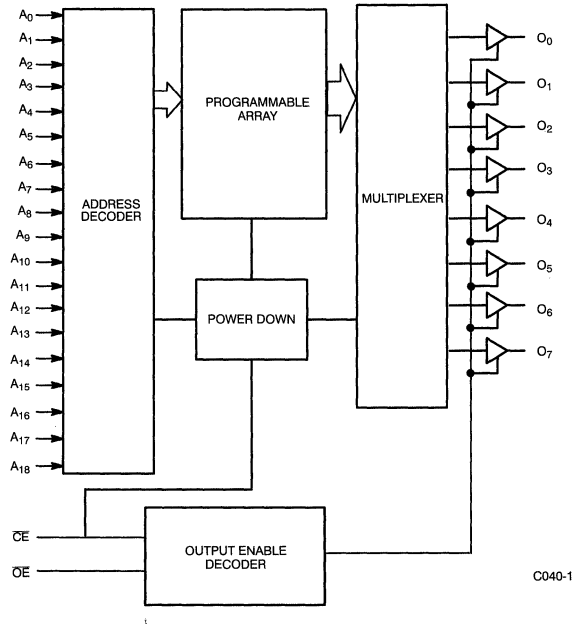
The CY27C040 is a high-performance, 4-megabit CMOS EPROM organized in 512 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, 32-pin LCC and PLCC, and 32-pin TSOP-I packages. The CY27C040 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27C040 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

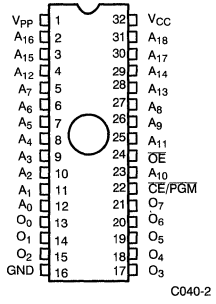
The CY27C040 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{18}-A_0$ will appear at the outputs O_7-O_0.

Logic Block Diagram

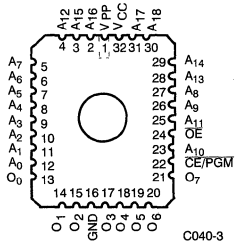


Pin Configurations

DIP
Top View

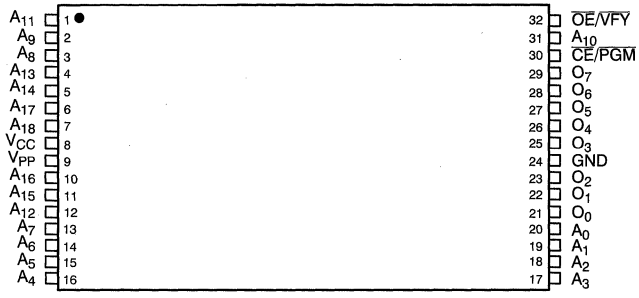


LCC/PLCC
Top View



Pin Configurations (continued)

TSOP
Top View



C040-4

Selection Guide

		27C040–70	27C040–90	27C040–120	27C040–150	27C040–200
Maximum Access Time (ns)		70	90	120	150	200
$\overline{CE}$ Access Time (ns)		70	90	120	150	200
$\overline{OE}$ Access Time (ns)		30	35	40	50	60
I_{CC}[1] (mA) Power Supply Current	Com'l	25	25	25	25	25
	Mil		30	30	30	30
I_{SB}[2] (μA) CMOS Stand-by Current		100	100	100	100	100
I_{SB}[3] (mA) TTL Stand-by Current		1	1	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{CC} − 0.3V to V_{CC} + 1.0V.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

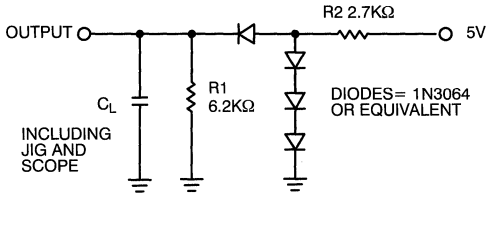
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=5 MHz	Com'l		25	mA
			Mil		30	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		1	mA
			Mil		1	mA

Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

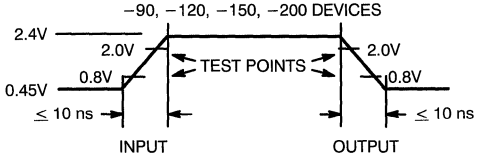
Notes:
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

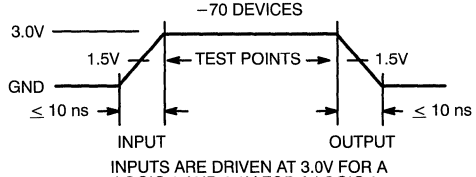


C_L= 100 pF FOR −90, −120, −150, −200 DEVICES
C_L= 30 pF FOR −70 DEVICES

C040-5



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 AND 0.45V FOR A LOGIC 0.



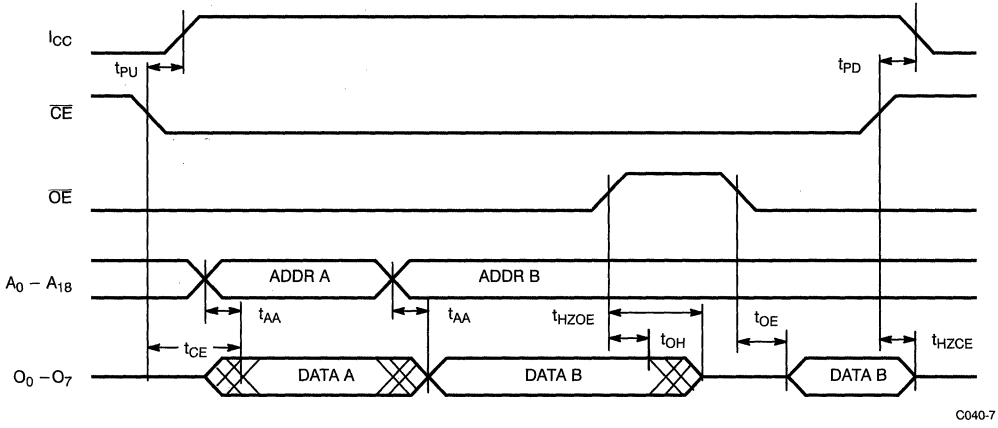
INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC 1 AND 0.0V FOR A LOGIC 0.

C040-6

Switching Characteristics Over the Operating Range

Parameter	Description	27C040–70		27C040–90		27C040–120		27C040–150		27C040–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		30		35		40		50		60	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		25		25		30		30		40	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		25		25		30		30		40	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		60		65		65		65		70	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform



C040-7

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C040 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C040 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function[8]					
	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	A_0	A_9	Data
Read	V_{IL}	V_{IL}	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	V_{IH}	A_0	A_9	High Z
Stand-by (CMOS)	$V_{CC}-0.3V$	X	V_{IH}	A_0	A_9	High Z
Stand-by (TTL)	V_{IH}	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{IHP}	X	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{HV}[9]	Note 10

Note:
8. X can be V_{IL} or V_{IH}.
9. $V_{HV}=12V\pm0.5V$
10. To be determined.

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C040–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040–70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C040–70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040–70ZC	Z32	32-Lead Thin Small Outline Package	
90	CY27C040–90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040–90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040–90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040–90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040–90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040–90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040–90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040–90WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
120	CY27C040–120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040–120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040–120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040–120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040–120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040–120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040–120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040–120WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
150	CY27C040–150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040–150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040–150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040–150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040–150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040–150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040–150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040–150WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
200	CY27C040–200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040–200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040–200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040–200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040–200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040–200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040–200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040–200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:
11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

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CY27C128

128K (16K x 8-Bit) CMOS EPROM

Features

- **Wide speed range**
  - **— 45 ns to 200 ns (commercial and military)**
- **Low power**
  - **— 248 mW (commercial)**
  - **— 303 mW (military)**
- **Low standby power**
  - **— Less than 83 mW when deselected**
- **±10% Power supply tolerance**

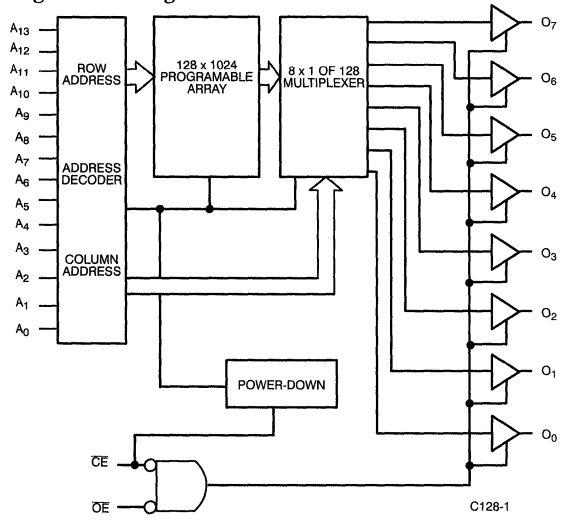
Functional Description

The CY27C128 is a high-performance 16,384-word by 8-bit CMOS EPROM. When disabled ($\overline{CE}$ HIGH), the CY27C128 automatically powers down into a low-power stand-by mode. The CY27C128 is packaged in the industry standard 600-mil DIP and LCC packages. The CY27C128 is also available in a Cer-DIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the EPROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

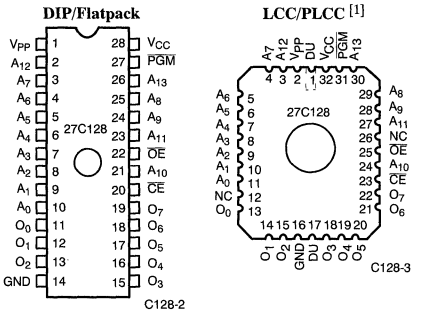
The CY27C128 offers the advantage of lower power and superior performance and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each EPROM is also tested for AC performance to guarantee that after customer programming, the product will meet both DC and AC specification limits.

Reading the CY27C128 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines ($A_0 - A_{13}$) will become available on the output lines ($O_0 - O_7$).

Logic Block Diagram



Pin Configurations



Selection Guide

		27C128–45	27C128–55	27C128–70	27C128–90	27C128–120	27C128–150	27C128–200
Maximum Access Time (ns)		45	55	70	90	120	150	200
Maximum Operating Current (mA)[2]	Com'l	45	45	45	45	45	45	45
	Mil	55	55	55	55	55	55	55
Standby Current (mA)	Com'l	15	15	15	15	15	15	15
	Mil	20	20	20	20	20	20	20
Chip Select Time (ns)		45	55	70	90	120	150	200
Output Enable Time (ns)		15	20	25	30	30	40	40

Notes:

1. For PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They must therefore be DU (don't use) for the PLCC package.
2. Add 2 mA/MHz for AC power component.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[3]	−40°C to +85°C	5V ±10%
Military[4]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		27C128−45, 55, 70, 90, 120, 150, 200 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA[6]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	Commercial	−10	+10	µA
			Military	−40	+40	
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current [2]	V_{CC} = Max., V_{IN} = V_{IH}, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Commercial		45	mA
			Military		55	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}	Commercial		15	mA
			Military		20	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

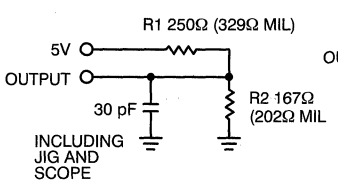
Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

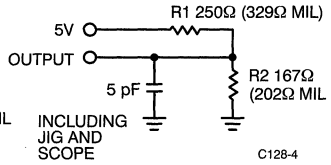
Notes:

3. Contact a Cypress representative for information on industrial temperature range specifications.
4. T_A is the "instant on" case temperature.
5. See the last page of this specification for Group A subgroup testing information.
6. I_{OL}=12.0 mA for military devices.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. See Introduction to CMOS PROMs in this Data Book for general information on testing.

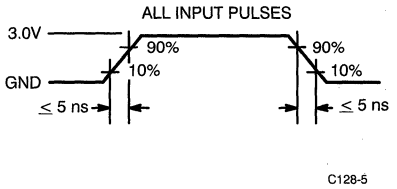
AC Test Loads and Waveforms



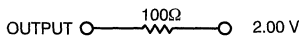
(a) Normal Load



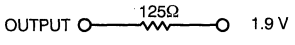
(b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

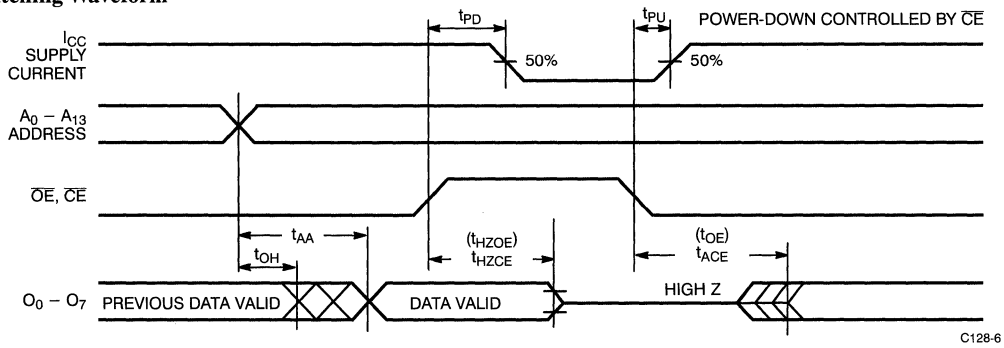
Switching Characteristics Over the Operating Range[4, 7]

Parameter	Description	27C128–45		27C128–55		27C128–70		27C128–90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		70		90	ns
t_{HZOE}	Outpout Enable Inactive to High Z		15		20		25		25	ns
t_{OE}	Output Enable Active to Output Valid		15		20		25		30	ns
t_{HZCE}	Chip Enable Inactive to High Z		20		25		25		25	ns
t_{ACE}	Chip Enable Active to Output Valid		45		55		70		90	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		45		55		70		90	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Switching Characteristics Over the Operating Range[4, 7] (continued)

Parameter	Description	27C128–120		27C128–150		27C128–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		120		150		200	ns
t_{HZOE}	Outpout Enable Inactive to High Z		30		30		30	ns
t_{OE}	Output Enable Active to Output Valid		30		40		40	ns
t_{HZCE}	Chip Enable Inactive to High Z		30		30		30	ns
t_{ACE}	Chip Enable Active to Output Valid		120		150		200	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		120		150		200	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the 27C128 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C128 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the EPROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

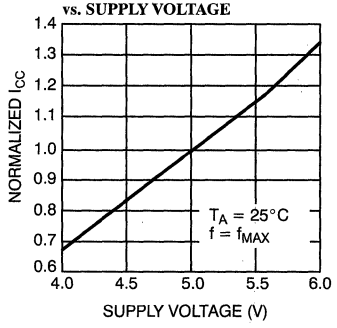
Table 1. CY27C128 Mode Selection

Mode	Pin Function[9]					
	$A_{13} - A_0$	$\overline{OE}$	$\overline{CE}$	V_{PP}	$\overline{PGM}$	$O_7 - O_0$
Read	$A_{13} - A_0$	V_{IL}	V_{IL}	X	Note 10	$O_7 - O_0$
Output Disable	$A_{13} - A_0$	V_{IH}	X	X	Note 10	High Z
Power Down	$A_{13} - A_0$	X	V_{IH}	X	Note 10	High Z

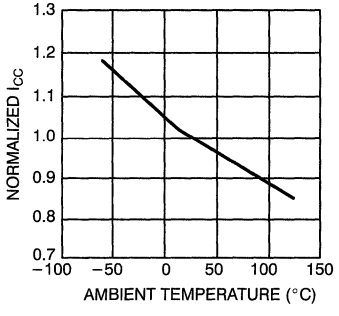
Notes:
9. X must be either V_{IL} or V_{IH}.
10. X must be either V_{IL} or V_{IH} (must not switch).

Typical DC and AC Characteristics

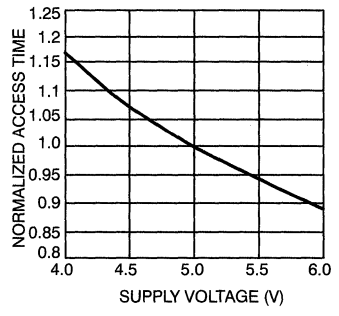
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



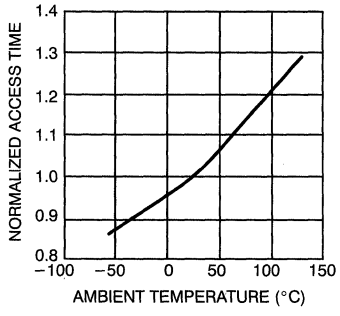
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



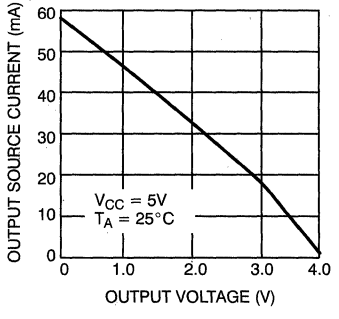
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



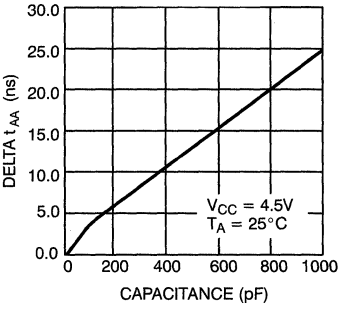
NORMALIZED ACCESS TIME vs. TEMPERATURE



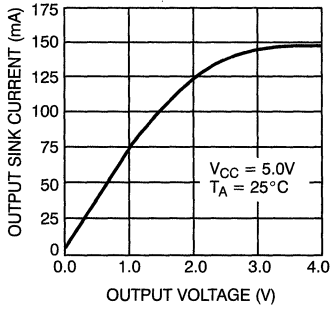
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



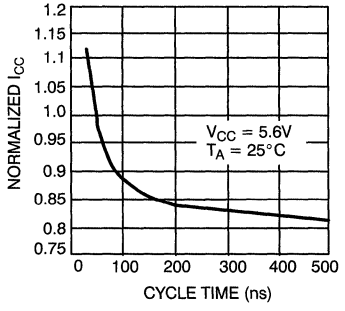
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZEDSUPPLY CURRENT vs. ACCESS TIME



Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY27C128–45JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
55	CY27C128–55JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
70	CY27C128–70JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
90	CY27C128–90JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–90WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
120	CY27C128–120JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–120WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
150	CY27C128–150JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–150WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
200	CY27C128–200JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C128–200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C128–200WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C128–200WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military

Note:
11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Document #: 38−00357

CY27C256

32K x 8-Bit CMOS EPROM

Features

- **Wide speed range**
  - **— 45 ns to 200 ns (commercial and military)**
- **Low power**
  - **— 248 mW (commercial)**
  - **— 303 mW (military)**
- **Low standby power**
  - **— Less than 83 mW when deselected**
- **±10% Power supply tolerance**

Functional Description

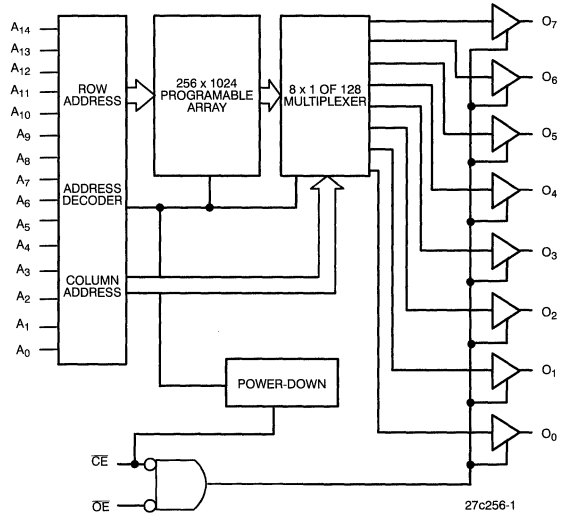
The CY27C256 is a high-performance 32,768-word by 8-bit CMOS EPROM. When disabled ($\overline{CE}$ HIGH), the CY27C256 automatically powers down into a low-power stand-by mode. The CY27C256 is packaged in the industry standard 600-mil DIP, PLCC, and TSOP packages. The CY27C256 is also available in a CerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the EPROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY27C256 offers the advantage of lower power and superior performance and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each EPROM is also tested for AC performance to guarantee that after customer programming, the product will meet both DC and AC specification limits.

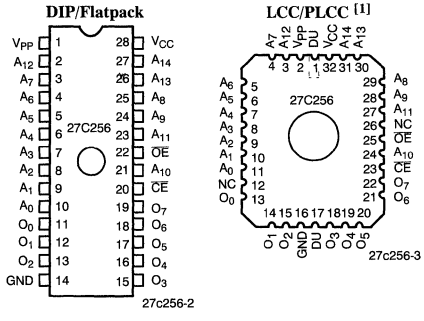
Reading the CY27C256 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 – A_{14}) will become available on the output lines (O_0 – O_7).

4

Logic Block Diagram



Pin Configurations



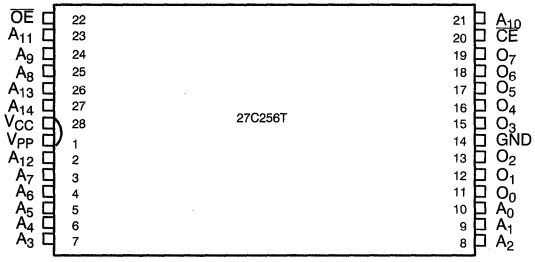
Selection Guide

		27C256–45	27C256–55	27C256–70	27C256–90	27C256–120	27C256–150	27C256–200
Maximum Access Time (ns)		45	55	70	90	120	150	200
Maximum Operating Current (mA)	Com'l	45	45	45	45	45	45	45
	Mil	55	55	55	55	55	55	55
Standby Current (mA)	Com'l	15	15	15	15	15	15	15
	Mil	20	20	20	20	20	20	20
Chip Select Time (ns)		45	55	70	90	120	150	200
Output Enable Time (ns)		15	20	25	30	30	40	40

Notes:
1. For PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They must therefore be DU (don't use) for the PLCC package.

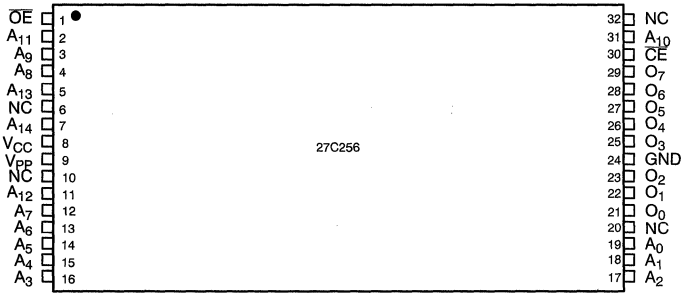
Pin Configurations

28-Pin TSOP
Top View



27c256-4

32-Pin TSOP
Top View



27c256-5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[2]	−40°C to +85°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		27C256-45, 55, 70, 90, 120, 150, 200 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA[5]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	Commercial	−10	+10	µA
			Military	−40	+40	
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = V_{IH}, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Commercial		45	mA
			Military		55	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}	Commercial		15	mA
			Military		20	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

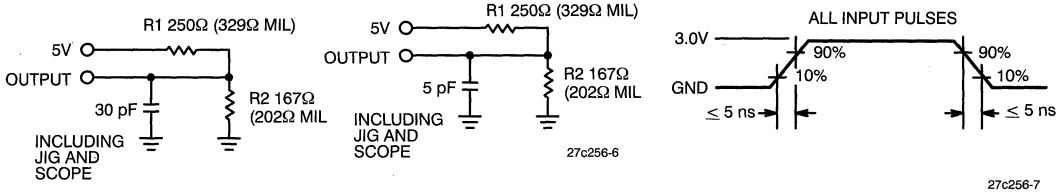
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. Contact a Cypress representative for information on industrial temperature range specifications.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. I_{OL}=12.0 mA for military devices.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms



(a) Normal Load **(b) High Z Load**

Equivalent to: THÉVENIN EQUIVALENT

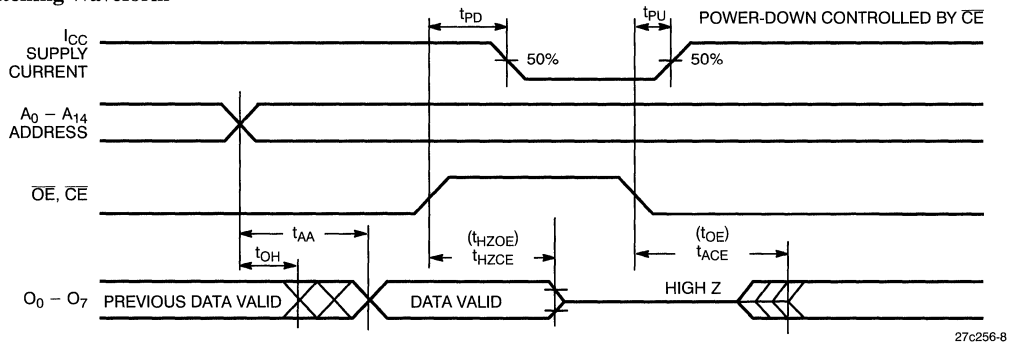
Switching Characteristics Over the Operating Range[4, 7]

Parameter	Description	27C256–45		27C256–55		27C256–70		27C256–90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		70		90	ns
t_{HZOE}	Outpout Enable Inactive to High Z		15		20		25		25	ns
t_{OE}	Output Enable Active to Output Valid		15		20		25		30	ns
t_{HZCE}	Chip Enable Inactive to High Z		20		25		25		25	ns
t_{ACE}	Chip Enable Active to Output Valid		45		55		70		90	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		45		55		70		90	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Switching Characteristics Over the Operating Range[4, 7]

Parameter	Description	27C256–120		27C256–150		27C256–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		120		150		200	ns
t_{HZOE}	Outpout Enable Inactive to High Z		30		30		30	ns
t_{OE}	Output Enable Active to Output Valid		30		40		40	ns
t_{HZCE}	Chip Enable Inactive to High Z		30		30		30	ns
t_{ACE}	Chip Enable Active to Output Valid		120		150		200	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		120		150		200	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the 27C256 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C256 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the EPROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

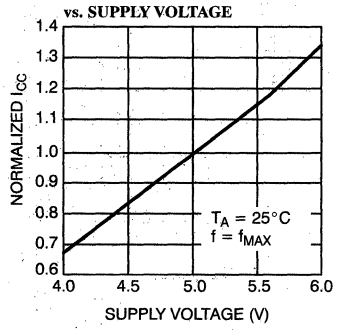
Table 1. CY27C256 Mode Selection

	Pin Function[8]				
Mode	$A_{14}-A_0$	$\overline{OE}$	$\overline{CE}$	V_{PP}	O_7-O_0
Read	$A_{14}-A_0$	V_{IL}	V_{IL}	X[9]	O_7-O_0
Output Disable	$A_{14}-A_0$	V_{IH}	V_{IL}	X	High Z
Power Down	$A_{14}-A_0$	X	V_{IH}	X	High Z

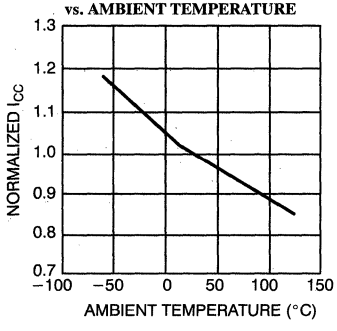
Notes:
8. X can be V_{IL} or V_{IH}.
9. V_{PP} should not exceed V_{CC} in read mode.

Typical DC and AC Characteristics

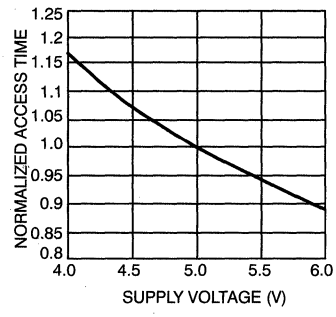
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



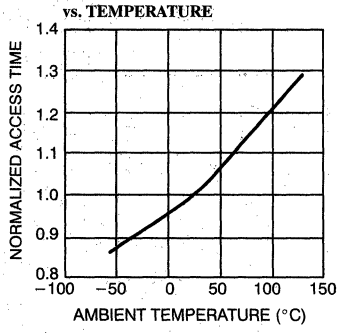
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



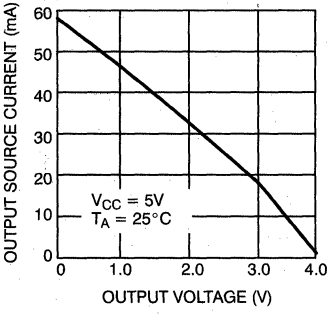
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



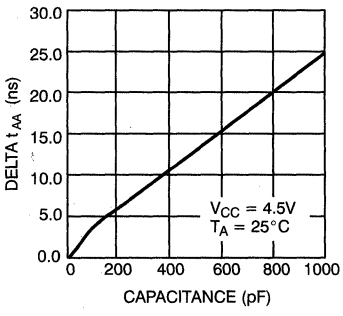
NORMALIZED ACCESS TIME vs. TEMPERATURE



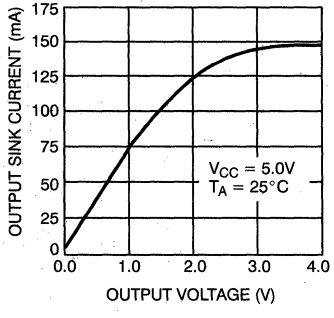
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



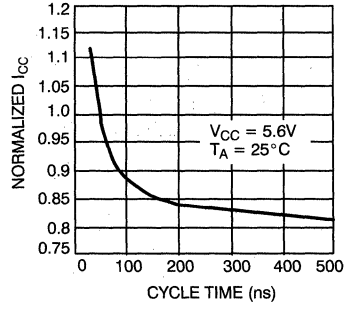
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ACCESS TIME



Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY27C256–45JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–45ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
55	CY27C256–55JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–55ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
70	CY27C256–70JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–70ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
90	CY27C256–90JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–90WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
120	CY27C256–120JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–120WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
150	CY27C256–150JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–150WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
200	CY27C256–200JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY27C256–200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C256–200WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C256–200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C256–200WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military

Note:
10. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY27C256T–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
	CY27C256T–45ZC	Z28	28-Thin Small Outline Package	
	CY27C256T–45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
55	CY27C256T–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
	CY27C256T–55ZC	Z28	28-Thin Small Outline Package	
	CY27C256T–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
70	CY27C256T–70WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
	CY27C256T–70ZC	Z28	28-Thin Small Outline Package	
	CY27C256T–70WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Document #: 38–00245–D

CY27C512

64K x 8 CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 70 ns max.**
- **Low power**
  - **— 220 mW max.**
  - **— Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 28-pin TSOP-I**
  - **— 28-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

The CY27C512 is a high-performance, 512K CMOS EPROM organized in 64 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. The CY27C512 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

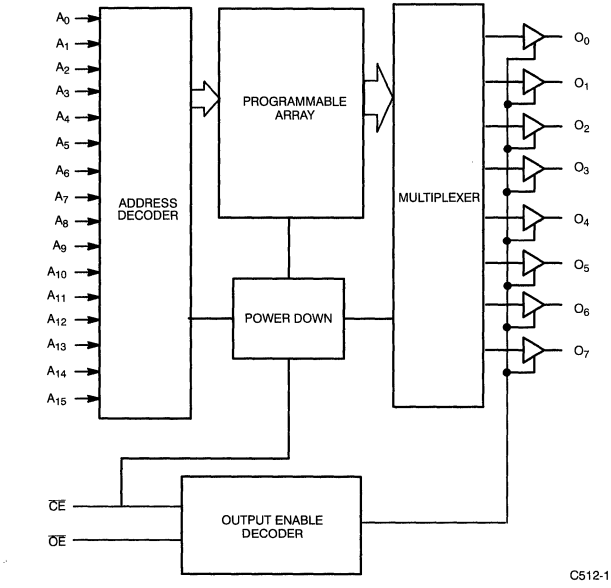
The CY27C512 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27C512 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{15}-A_0$ will appear at the outputs O_7-O_0.

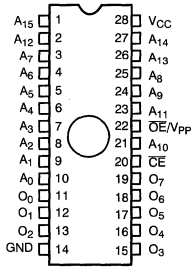
4

Logic Block Diagram



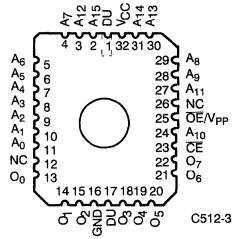
Pin Configurations

DIP
Top View



C512-2

LCC/PLCC[1]
Top View

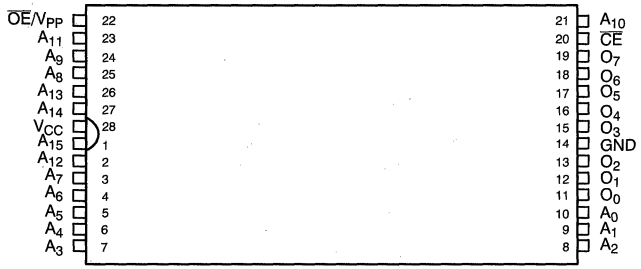


C512-3

Note:
1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Pin Configurations (continued)

TSOP
Top View
Type 1



C512-4

Selection Guide

		27C512–70	27C512–90	27C512–120	27C512–150	27C512–200
Maximum Access Time (ns)		70	90	120	150	200
$\overline{CE}$ Access Time (ns)		70	90	120	150	200
$\overline{OE}$ Access Time (ns)		25	30	40	50	60
I_{CC}[2] (mA) Power Supply Current	Com'l	40	40	40	40	40
	Mil	50	50	50	50	50
I_{SB}[3] (mA) Stand-by Current	Com'l	15	15	15	15	15
	Mil	25	25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
3. Contact a Cypress representative for industrial temperature range specification.
4. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

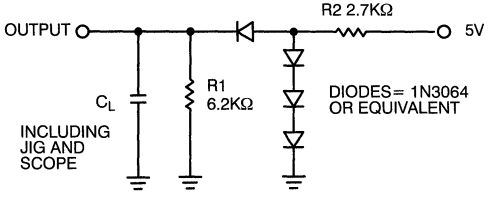
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −400 μA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	μA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=5 MHz	Com'l		40	mA
			Mil		50	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15	mA
			Mil		25	mA

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

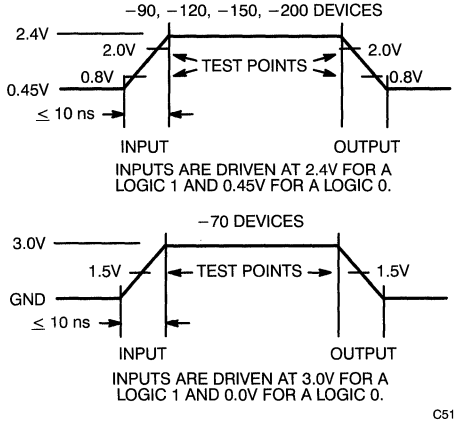
Notes:
5. See the last page of this specification for Group A subgroup testing information.
6. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms



C_L= 100 pF FOR −90, −120, −150, −200 DEVICES
C_L= 30 pF FOR −70 DEVICES

C512-5

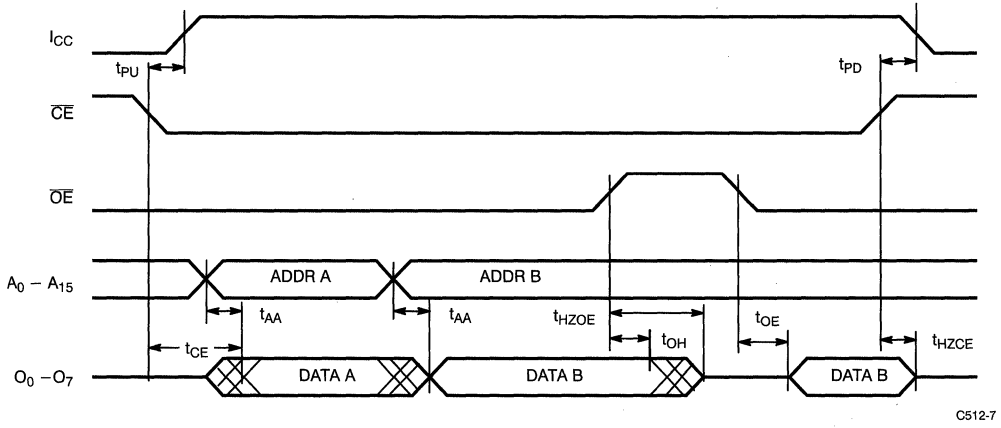


C512-6

Switching Characteristics Over the Operating Range

Parameter	Description	27C512–70		27C512–90		27C512–120		27C512–150		27C512–200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		25		30		40		50		60	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		25		30		40		50		60	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		25		30		30		30		30	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		60		65		65		65		65	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27C512 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C512 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function[8]				
	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_0	A_9	Data
Read	V_{IL}	V_{IL}	A_0	A_9	$O_7 - O_0$
Output Disable	X	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	X	X	High Z
Program	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	V_{IH}	V_{HV}[9]	1FH[10]

Note:
8. X can be V_{IL} or V_{IH}.
9. $V_{HV} = 12 \pm 0.5V$.
9. Subject to change before final version.

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C512–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512–70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512–70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512–70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512–70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
90	CY27C512–90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512–90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512–90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512–90ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512–90DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512–90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512–90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512–90WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
120	CY27C512–120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512–120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512–120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512–120ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512–120DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512–120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512–120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512–120WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
150	CY27C512–150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512–150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512–150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512–150ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512–150DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512–150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512–150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512–150WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
200	CY27C512–200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512–200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512–200WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512–200ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512–200DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27C512–200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C512–200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C512–200WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Notes:
10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38–00427

CY27H010

128K x 8 High-Speed CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 25 ns max. (commercial)**
  - **— t_{AA} = 35 ns max. (military)**
- **Low power**
  - **— 275 mW max.**
  - **— Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 32-pin TSOP-I**
  - **— 32-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

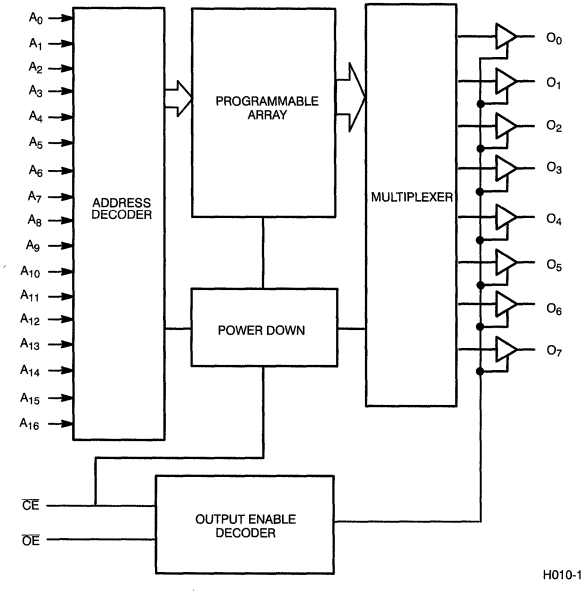
The CY27H010 is a high-performance, 1-megabit CMOS EPROM organized in 128 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, LCC, PLCC, and TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H010 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H010 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27H010 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{16}-A_0$ will appear at the outputs O_7-O_0.

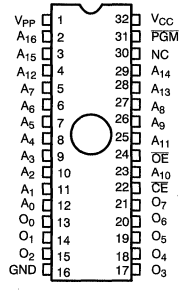
Logic Block Diagram



H010-1

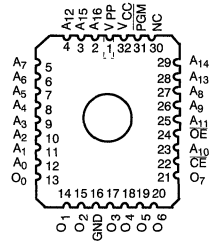
Pin Configurations

DIP
Top View



H010-2

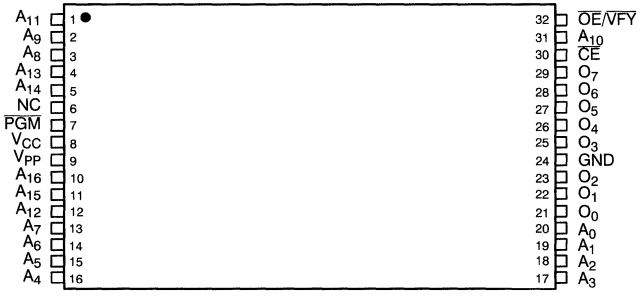
LCC/PLCC
Top View



H010-3

Pin Configurations (continued)

TSOP
Top View



H010-4

4

Selection Guide

		27H010–25	27H010–30	27H010–35	27H010–45	27H010–55	27H010–70
Maximum Access Time (ns)		25	30	35	45	55	70
$\overline{CE}$ Access Time (ns)	Com'l	30	35	40	45	55	70
	Mil			40	45	55	70
$\overline{OE}$ Access Time (ns)	Com'l	12	20	20	20	25	35
	Mil			20	20	25	35
I_{CC}[1] (mA) Power Supply Current	Com'l	75	75	50	50	50	50
	Mil			85	60	60	60
I_{SB}[2] (mA) Stand-by Current	Com'l	15	15	15	15	15	15
	Mil			25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[3]	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f=10 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
3. Contact a Cypress representative for industrial temperature range specification.
4. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[5, 6]

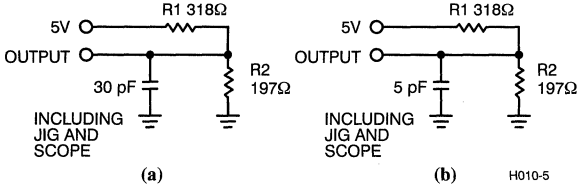
Parameter	Description	Test Conditions		27H010–25 27H010–30 Min.	27H010–25 27H010–30 Max.	27H010–35 Min.	27H010–35 Max.	27H010–45 27H010–55 27H010–70 Min.	27H010–45 27H010–55 27H010–70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.45		0.45		0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=10 MHz	Com'l		75		50		50	mA
			Mil				85		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA
			Mil				25		25	mA

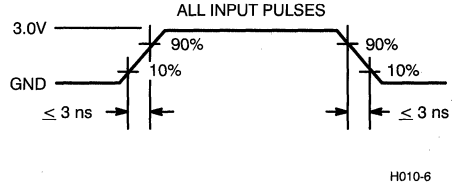
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

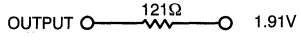
Notes:
5. See the last page of this specification for Group A subgroup testing information.
6. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms





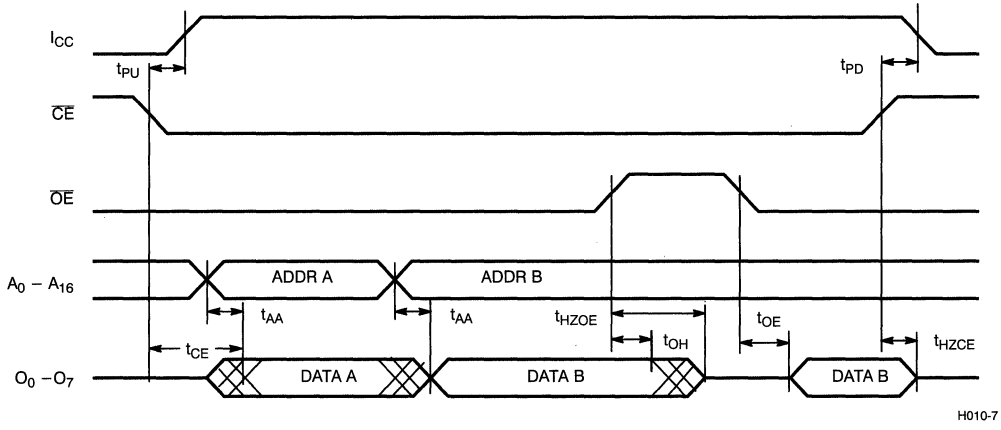
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	27H010–25		27H010–30		27H010–35		27H010–45		27H010–55		27H010–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45		55		70	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		12		20		20		20		25		35	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		12		20		20		20		25		35	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		30		35		40		45		55		70	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		20		20		20		25		35	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		50		60		75	ns
t_{OH}	Output Data Hold	0		0		0		0		0		0		ns

Switching Waveform



H010-7

Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27H010 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27H010 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

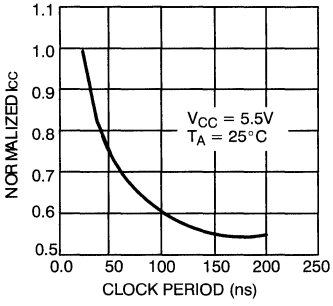
Table 2. Mode Selection

	Pin Function[7]						
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A_0	A_9	**Data**
Read	V_{IL}	V_{IL}	X	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	X	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{HV}[8]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_{HV}[8]	1DH

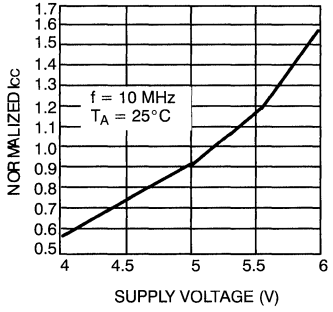
Note:
7. X can be V_{IL} or V_{IH}.
8. V_{HV}=12V±0.5V

Typical DC and AC Characteristics

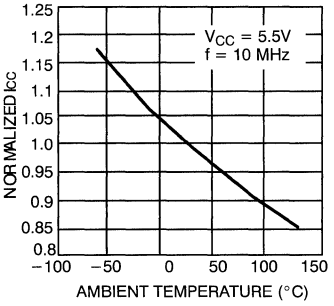
NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



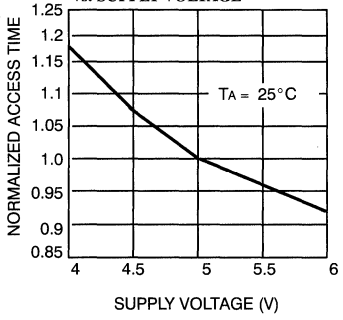
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



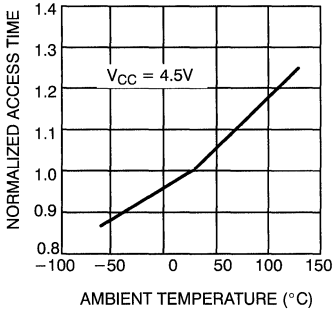
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



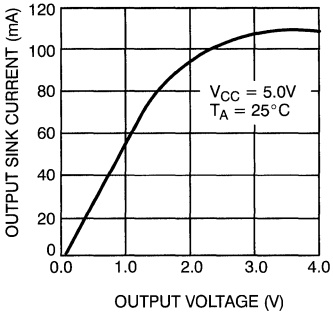
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



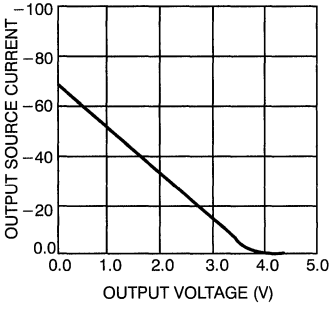
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



H010-8

4

Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H010–25HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010–25ZC	Z32	32-Lead Thin Small Outline Package	
30	CY27H010–30HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010–30PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–30WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–30ZC	Z32	32-Lead Thin Small Outline Package	
35	CY27H010–35HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010–35PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–35WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–35ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–35HMB	H65	32-Pin Windowed Leaded Chip Carrier	Military
	CY27H010–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H010–45HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010–45JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010–45PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–45WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–45ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–45DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27H010–45HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H010–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010–45WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
55	CY27H010–55HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010–55JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010–55PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–55WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–55ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–55DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27H010–55HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H010–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010–55WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:
9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[9] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27H010–70HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H010–70JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H010–70PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–70ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–70DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27H010–70HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H010–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010–70WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

4

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38–00171–B

32K x 8 High-Speed CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 25 ns max. (commercial)**
  - **— t_{AA} = 35 ns max. (military)**
- **Low power**
  - **— 275 mW max.**
  - **— Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001 V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 28-pin TSOP-I**
  - **— 28-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

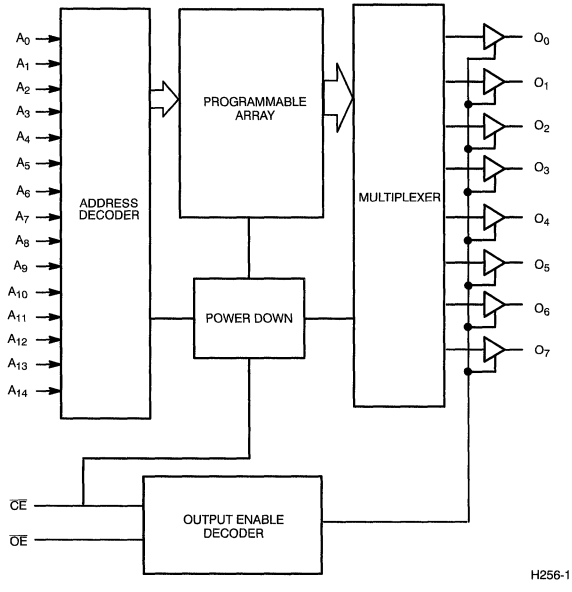
The CY27H256 is a high-performance, 256K CMOS EPROM organized in 32 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H256 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H256 is equipped with a power-down chip enable ($\overline{CE}$) input as well as an output enable ($\overline{OE}$) input. When $\overline{CE}$ is deasserted, the device powers down to a low-power stand-by mode. The $\overline{OE}$ pin three-states the outputs without putting the device into stand-by mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27H256 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{14}-A_0$ will appear at the outputs O_7-O_0.

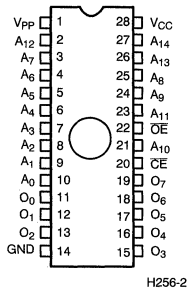
Logic Block Diagram



H256-1

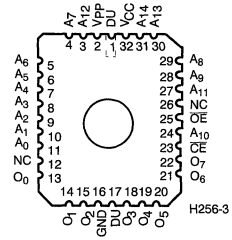
Pin Configurations

DIP
Top View



H256-2

LCC/PLCC[1]
Top View

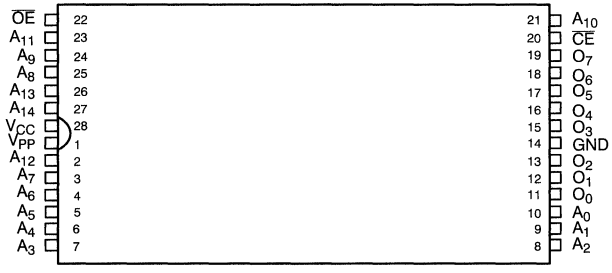


H256-3

Note:
1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Pin Configurations (continued)

TSOP
Top View
Type 1



H256-4

4

Selection Guide

		27H256–25	27H256–30	27H256–35	27H256–45	27H256–55	27H256–70
Maximum Access Time (ns)		25	30	35	45	55	70
$\overline{CE}$ Access Time (ns)	Com'l	30	35	35	45	55	70
	Mil			40	45	55	70
$\overline{OE}$ Access Time (ns)	Com'l	12	15	15	15	20	25
	Mil			20	20	20	25
I_{CC}[2] (mA) Power Supply Current	Com'l	75	75	50	50	50	50
	Mil			85	60	60	60
I_{SB}[3] (mA) Stand-by Current	Com'l	15	15	15	15	15	15
	Mil			25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for < 20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

2. V_{CC} = Max., I_{OUT} = 0 mA, f=10 MHz.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

Parameter	Description	Test Conditions		27H256–25 27H256–30 Min.	27H256–25 27H256–30 Max.	27H256–35 Min.	27H256–35 Max.	27H256–45 27H256–55 27H256–70 Min.	27H256–45 27H256–55 27H256–70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.45		0.45		0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=10 MHz	Com'l		75		50		50	mA
			Mil				85		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA
			Mil				25		25	mA

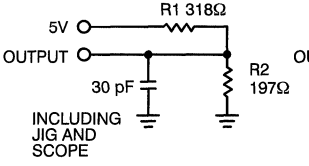
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

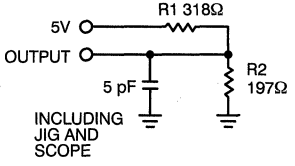
Notes:

6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

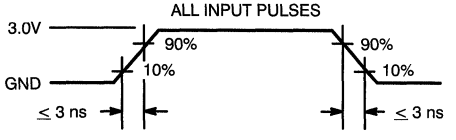


(a) Normal Load



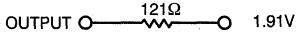
(b) High-Z Load

H256-5



H256-6

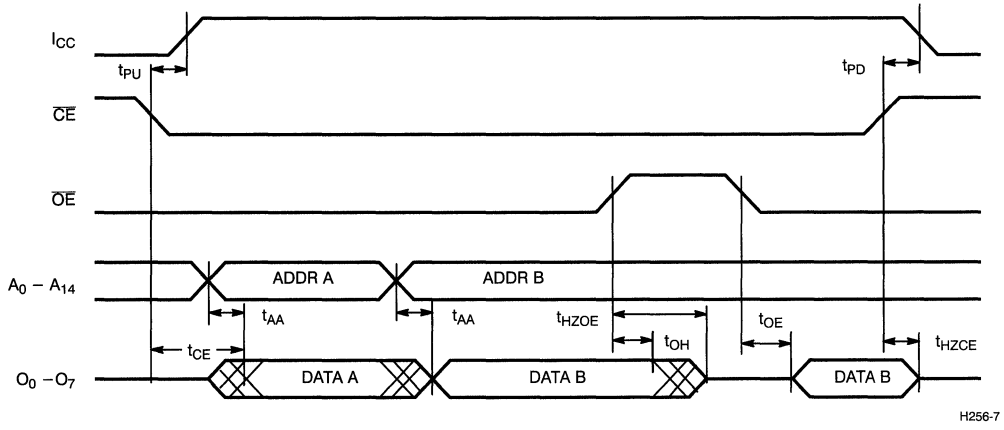
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	27H256–25		27H256–30		27H256–35		27H256–45		27H256–55		27H256–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45		55		70	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		12		15		15		15		20		25	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		12		15		15		15		20		25	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		30		35		35		45		55		70	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		15		15		15		20		25	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		40		50		60	ns
t_{OH}	Output Data Hold	0		0		0		0		0		0		ns

Switching Waveform



H256-7

Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27H256 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27H256 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

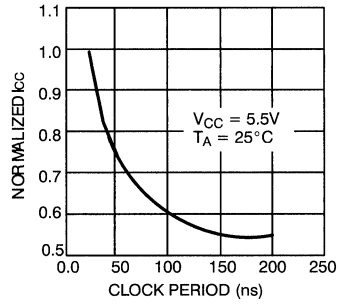
Table 2. Mode Selection

Mode	Pin Function[8]					
	$\overline{CE}$	$\overline{OE}$	V_{PP}	A_0	A_9	Data
Read	V_{IL}	V_{IL}	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{IHP}	V_{ILP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{HV}[9]	21H

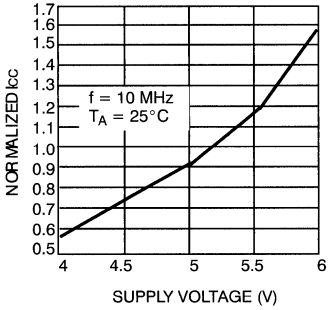
Notes:
8. X can be V_{IL} or V_{IH}.
9. V_{HV}=12±0.5V

Typical DC and AC Characteristics

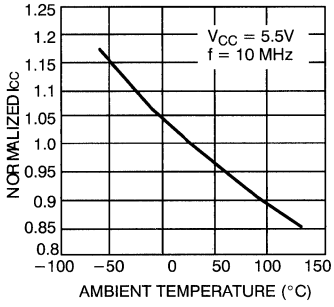
NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



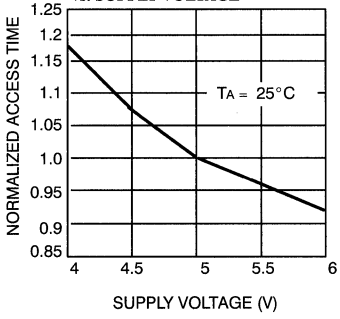
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



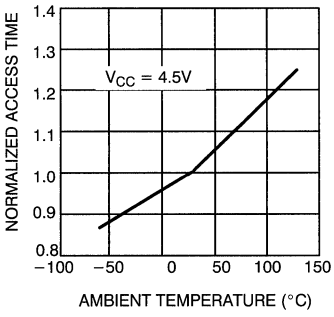
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



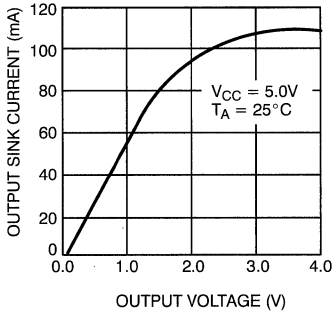
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



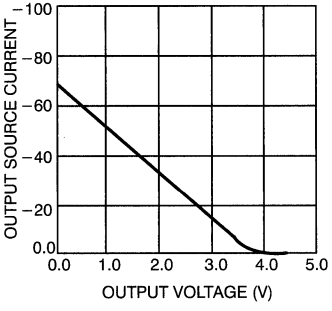
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



H256-8

Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H256–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256–25ZC	Z28	28-Lead Thin Small Outline Package	
30	CY27H256–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256–30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256–30ZC	Z28	28-Lead Thin Small Outline Package	
35	CY27H256–35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256–35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256–35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256–35ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
	CY27H256–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H256–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256–45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27H256–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256–55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
70	CY27H256–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256–70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256–70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256–70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256–70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:
10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

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64K x 8 High-Speed CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 25 ns max. (commercial)**
  - **— t_{AA} = 35 ns max. (military)**
- **Low power**
  - **— 275 mW max.**
  - **— Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 28-pin TSOP-I**
  - **— 28-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

Functional Description

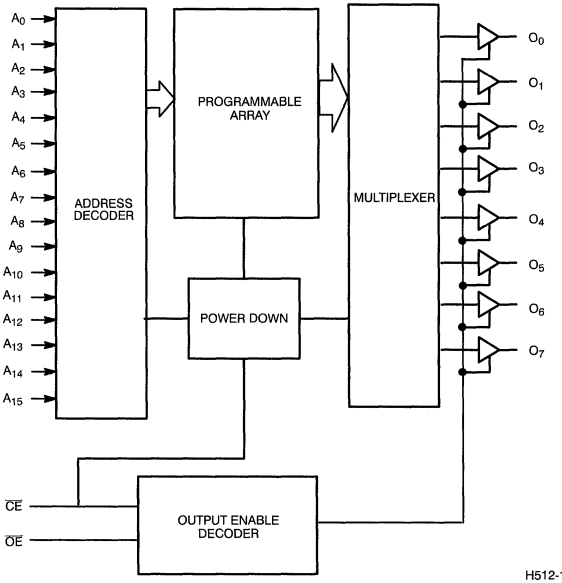
The CY27H512 is a high-performance, 512K CMOS EPROM organized in 64 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H512 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H512 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27H512 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{15}-A_0$ will appear at the outputs O_7-O_0.

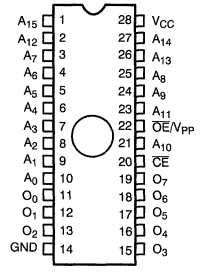
Logic Block Diagram



H512-1

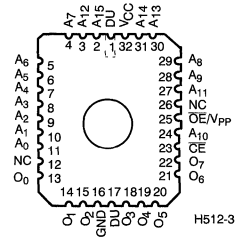
Pin Configurations

DIP
Top View



H512-2

LCC/PLCC[1]
Top View

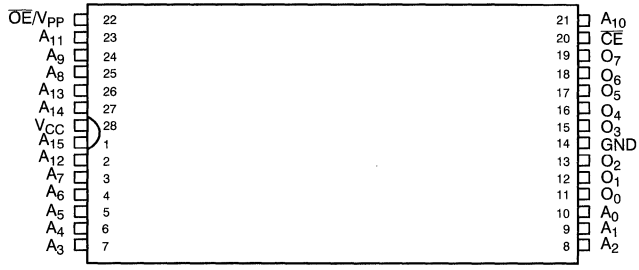


H512-3

Note:
1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Pin Configurations (continued)

TSOP
Top View
Type 1



H512-4

4

Selection Guide

		27H512–25	27H512–30	27H512–35	27H512–45	27H512–55	27H512–70
Maximum Access Time (ns)		25	30	35	45	55	70
$\overline{CE}$ Access Time (ns)	Com'l	30	35	35	45	55	70
	Mil			40	45	55	70
$\overline{OE}$ Access Time (ns)	Com'l	12	15	15	15	20	25
	Mil			20	20	20	25
I_{CC}[2] (mA) Power Supply Current	Com'l	75	75	50	50	50	50
	Mil			85	60	60	60
I_{SB}[3] (mA) Stand-by Current	Com'l	15	15	15	15	15	15
	Mil			25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

2. V_{CC} = Max., I_{OUT} = 0 mA, f=10 MHz.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

Parameter	Description	Test Conditions		27H512–25 27H512–30 Min.	27H512–25 27H512–30 Max.	27H512–35 Min.	27H512–35 Max.	27H512–45 27H512–55 27H512–70 Min.	27H512–45 27H512–55 27H512–70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.45		0.45		0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=10 MHz	Com'l		75		50		50	mA
			Mil				85		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA
			Mil				25		25	mA

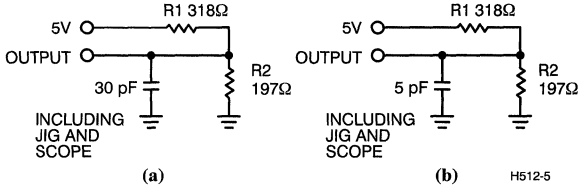
Capacitance[7]

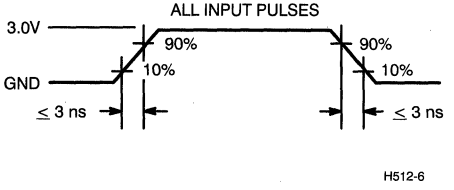
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

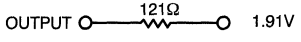
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms





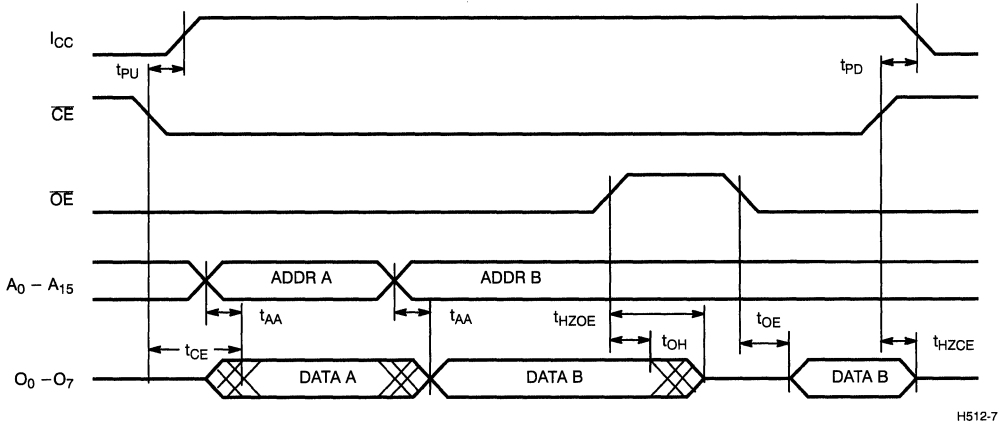
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	27H512–25		27H512–30		27H512–35		27H512–45		27H512–55		27H512–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45		55		70	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		12		15		15		15		20		25	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		12		15		15		15		20		25	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		30		35		35		45		55		70	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		15		15		15		20		25	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		40		50		60	ns
t_{OH}	Output Data Hold	0		0		0		0		0		0		ns

Switching Waveform



H512-7

Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY27H512 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27H512 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming VCC	6.0	6.5	V

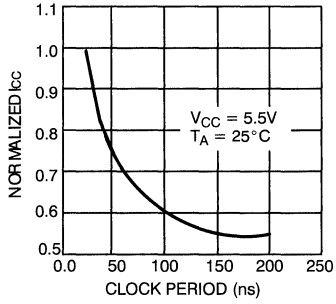
Table 2. Mode Selection

Mode	Pin Function[8]				
	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_0	A_9	Data
Read	V_{IL}	V_{IL}	A_0	A_9	$O_7 - O_0$
Output Disable	X	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	X	X	High Z
Program	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	V_{IH}	V_{HV}[9]	1FH

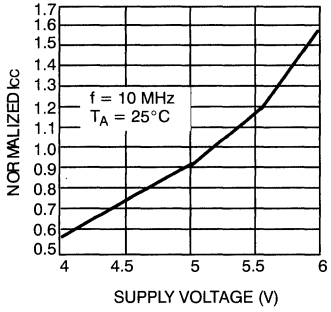
Note:
8. X can be V_{IL} or V_{IH}.
9. V_{HV}=12±0.5V.

Typical DC and AC Characteristics

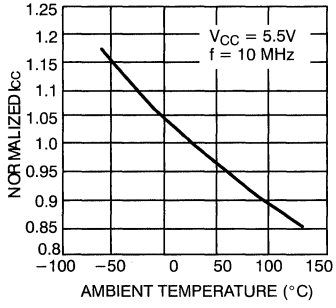
NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



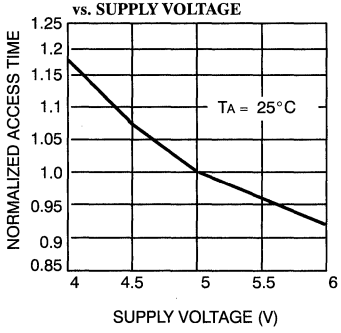
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



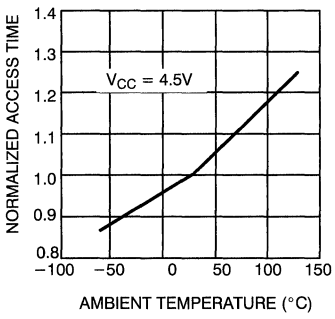
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



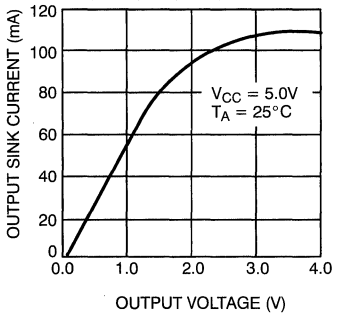
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



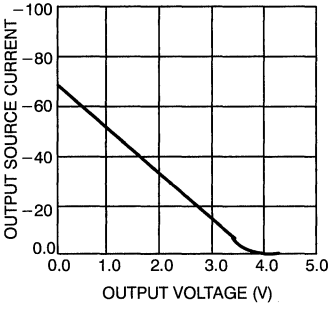
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



H512-8

4

Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H512–25HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512–25ZC	Z28	28-Lead Thin Small Outline Package	
30	CY27H512–30HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512–30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512–30ZC	Z28	28-Lead Thin Small Outline Package	
35	CY27H512–35HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512–35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512–35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512–35ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512–35HMB	H65	32-Pin Windowed Leaded Chip Carrier	Military
	CY27H512–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H512–45HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512–45JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512–45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512–45HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27H512–55HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512–55JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512–55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512–55HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Notes:
10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[10] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27H512–70HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512–70JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512–70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512–70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512–70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512–70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512–70HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512–70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

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CY7C225A

512 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 18 ns address set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs**
- **EPROM technology, 100% programmable**
- **Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

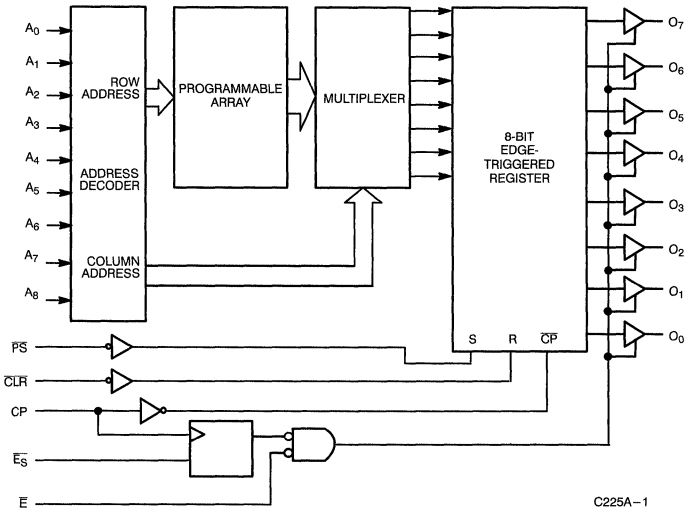
Functional Description

The CY7C225A is a high-performance 512 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC.

The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225A replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

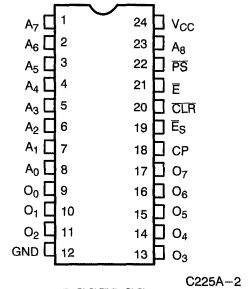
Logic Block Diagram



C225A-1

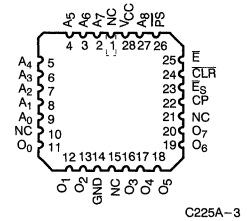
Pin Configurations

DIP
Top View



C225A-2

LCC/PLCC
Top View



C225A-3

Selection Guide

		7C225A–18	7C225A–25	7C225A–30	7C225A–35	7C225A–40
Minimum Address Set-Up Time (ns)		18	25	30	35	40
Maximum Clock to Output (ns)		12	12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90	90		90
	Military		120	120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		−10	+10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

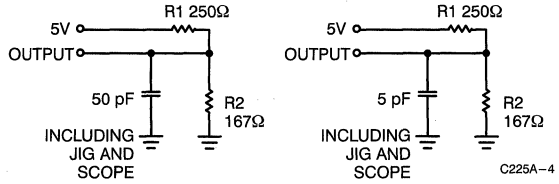
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

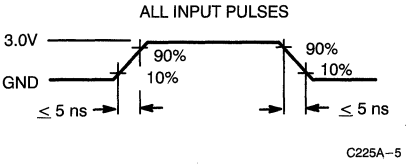
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

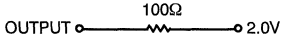
AC Test Loads and Waveforms[4]



(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C225A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and $\overline{CLEAR}$ and $\overline{PRESET}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs ($A_0 - A_8$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225A has buffered asynchronous $\overline{CLEAR}$ and $\overline{PRESET}$ inputs. Applying a LOW to the $\overline{PRESET}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{CLEAR}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

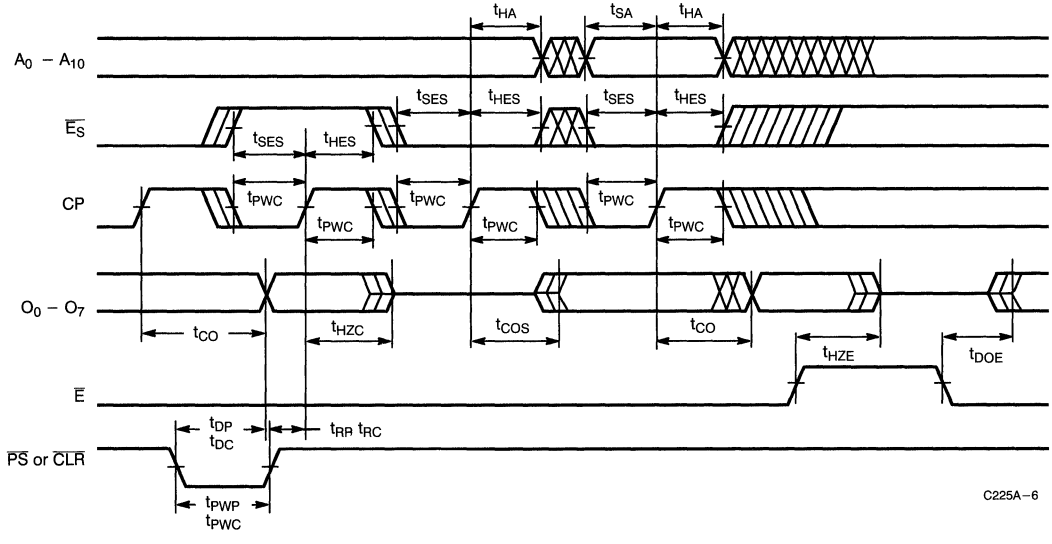
When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C225A–18		7C225A–25		7C225A–30		7C225A–35		7C225A–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		10		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		10		10		10		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	0		0		5		5		5		ns
t_{DP}, t_{DC}	Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ to Valid Output		20		20		20		20		20	ns
t_{RP}, t_{RC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Recovery to Clock HIGH	15		15		20		20		20		ns
t_{PWP}, t_{PWC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Pulse Width	15		15		20		20		20		ns
t_{COS}	Valid Output from Clock HIGH[7]		15		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		20		20		25		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		15		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		15		20		20		25		30	ns

Note:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.

Switching Waveforms[4]



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]						
	Read or Output Disable	$A_8 - A_0$	CP	$\overline{E_S}$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	$O_7 - O_0$
	Other	$A_8 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	$D_7 - D_0$
Read		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_8 - A_0$	X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_8 - A_0$	X	X	V_{IH}	V_{IH}	V_{IH}	High Z
Clear		$A_8 - A_0$	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
Preset		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Program Verify		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_8 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Blank Check		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	Zeros

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

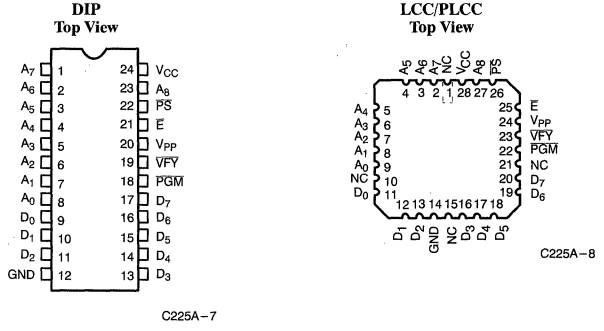
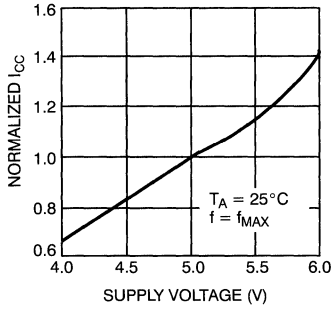


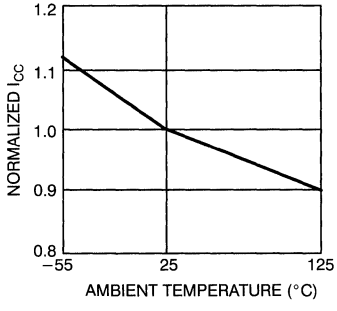
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

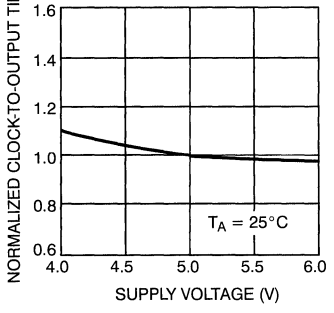
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



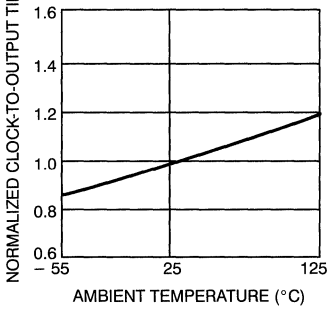
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



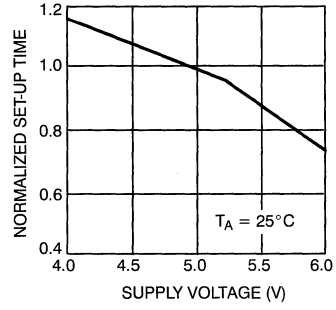
CLOCK TO OUTPUT TIME vs. V_{CC}



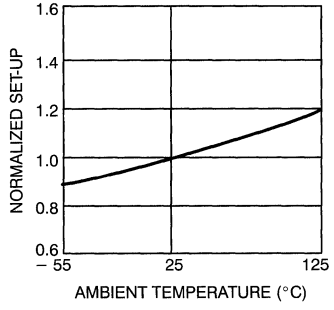
CLOCK TO OUTPUT TIME vs. TEMPERATURE



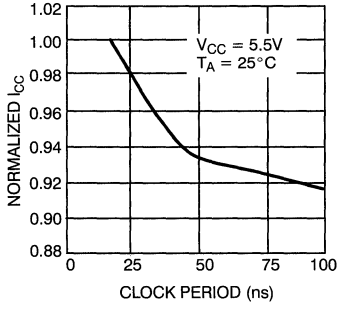
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



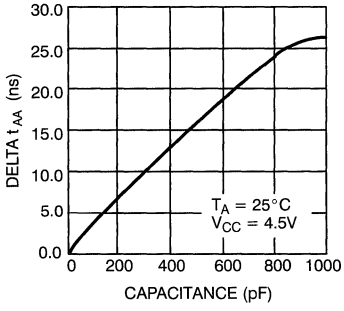
NORMALIZED SET-UP TIME vs. TEMPERATURE



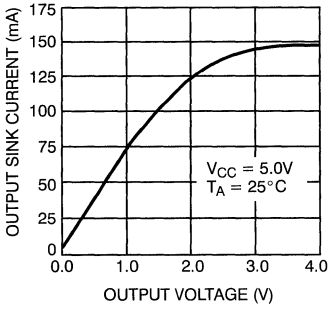
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C225A–9

Ordering Information[9]

Speed (ns)		Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}				
18	12	CY7C225A–18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C225A–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C225A–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–30LMB	L64	28-Square Leadless Chip Carrier	
35	20	CY7C225A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–35LMB	L64	28-Square Leadless Chip Carrier	
40	25	CY7C225A–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A–40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A–40LMB	L64	28-Square Leadless Chip Carrier	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DP}	7, 8, 9, 10, 11
t_{RP}	7, 8, 9, 10, 11

Document #: 38–00228–C

CY7C235A

1K x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 18 ns address set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous registers ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP or 28-pin LCC and PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

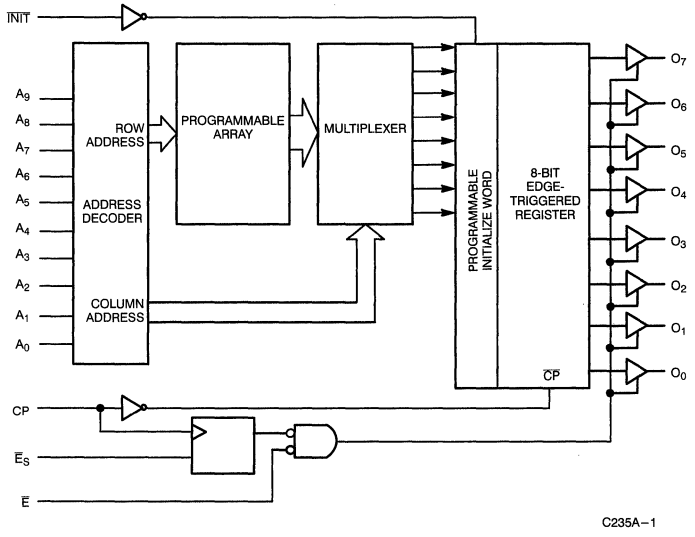
Functional Description

The CY7C235A is a high-performance 1024 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, or 28-pin plastic leaded chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

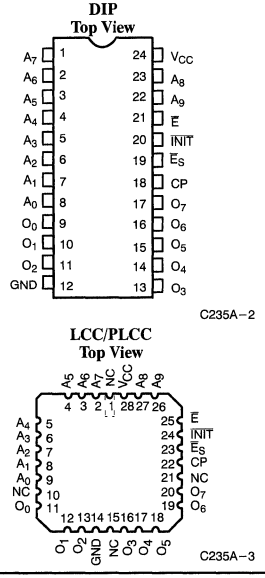
The CY7C235A replaces bipolar devices pin for pin and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet AC specification limits after customer programming.

4

Logic Block Diagram



Pin Configurations



Selection Guide

		7C235A–18	7C235A–25	7C235A–30	7C235A–40
Minimum Address Set-Up Time (ns)		18	25	30	40
Maximum Clock to Output (ns)		12	12	15	20
Maximum Operating Current (mA)	Commercial	90	90	90	90
	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20 for DIP) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 5				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled[4]		−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

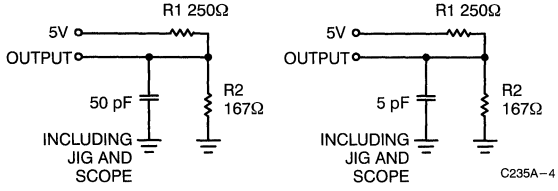
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

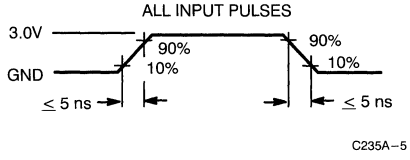
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

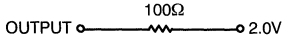
AC Test Loads and Waveforms[5]



(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



4

Operating Modes

The CY7C235A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{INIT}$).

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address input ($A_0 - A_9$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$), provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C235A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235A has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

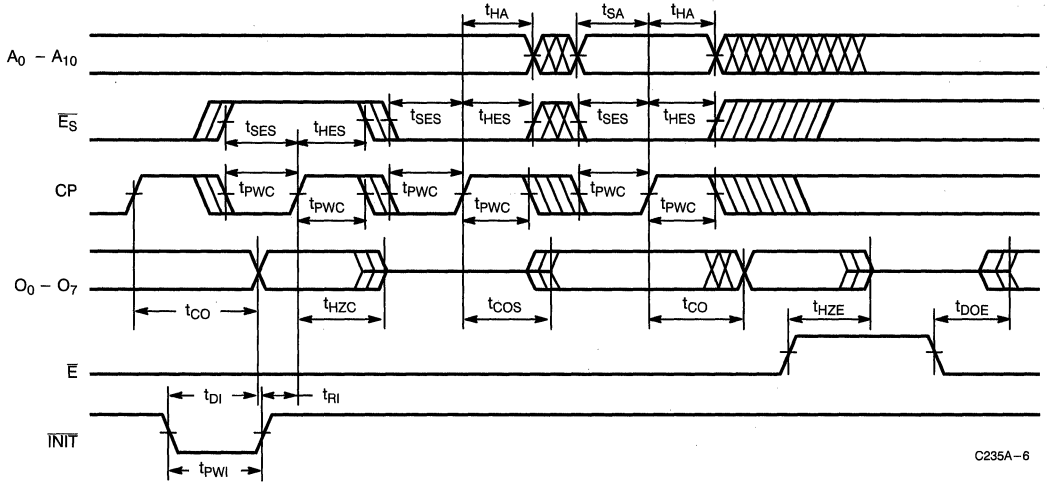
When the asynchronous initialize input, $\overline{INIT}$, is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

Switching Characteristics Over Operating Range[3, 5]

Parameter	Description	7C235A–18		7C235A–25		7C235A–30		7C235A–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		12		15		20		ns
t_{SES}	$\overline{E_S}$ Set-Up to Clock HIGH	10		10		10		15		ns
t_{HES}	$\overline{E_S}$ Hold from Clock HIGH	5		5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		20		25		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	15		20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH[7]		15		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		20		20		25	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		15		20		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		15		20		20		25	ns

Note:
7. Applies only when the synchronous ($\overline{E_S}$) function is used.

Switching Waveforms[5]



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]							
	Read or Output Disable	**A_0, A_3 – A_9**	**A_1**	**A_2**	**CP**	**$\overline{E}_S$**	**$\overline{E}$**	**$\overline{INIT}$**	**O_7 – O_0**
	Other	**A_0, A_3 – A_9**	**A_1**	**A_2**	**$\overline{PGM}$**	**$\overline{VFY}$**	**$\overline{E}$**	**V_{PP}**	**D_7 – D_0**
Read		A_0, A_3 – A_9	A_1	A_2	X	V_{IL}	V_{IL}	V_{IH}	O_7 – O_0
Output Disable		A_0, A_3 – A_9	A_1	A_2	X	V_{IH}	X	V_{IH}	High Z
Output Disable		A_0, A_3 – A_9	A_1	A_2	X	X	V_{IH}	V_{IH}	High Z
Initialize		A_0, A_3 – A_9	A_1	A_2	X	X	V_{IL}	V_{IL}	Init Byte
Program		A_0, A_3 – A_9	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	D_7 – D_0
Program Verify		A_0, A_3 – A_9	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	O_7 – O_0
Program Inhibit		A_0, A_3 – A_9	A_1	A_2	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		A_0, A_3 – A_9	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	D_7 – D_0
Program Initialize Byte		A_0, A_3 – A_9	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	D_7 – D_0
Blank Check		A_0, A_3 – A_9	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	Zeros

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

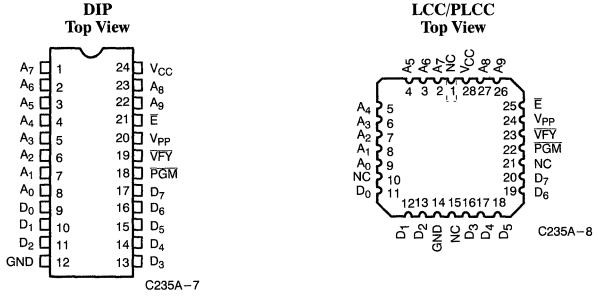
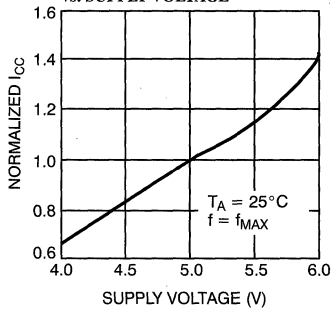


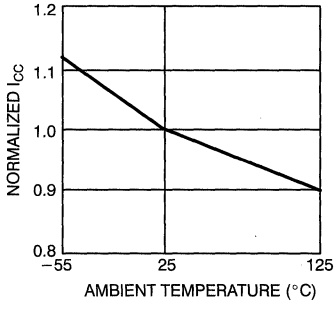
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

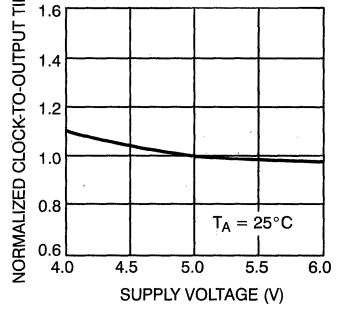
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



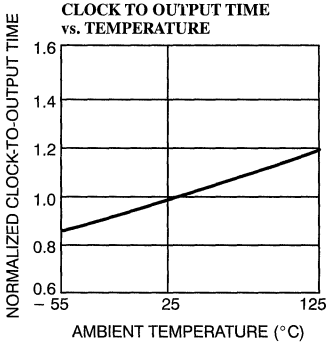
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



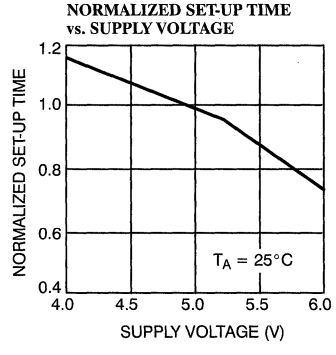
CLOCK TO OUTPUT TIME vs. V_{CC}



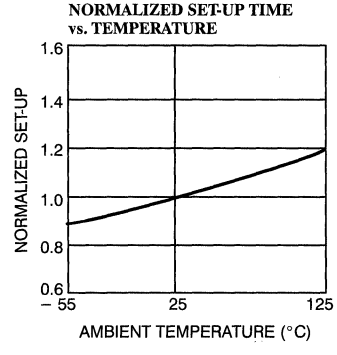
CLOCK TO OUTPUT TIME vs. TEMPERATURE



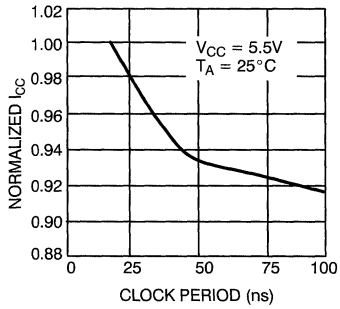
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



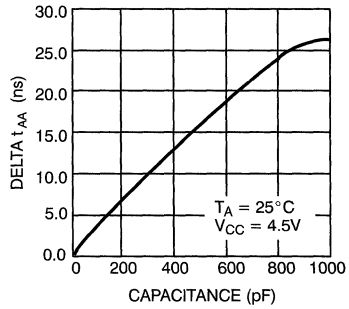
NORMALIZED SET-UP TIME vs. TEMPERATURE



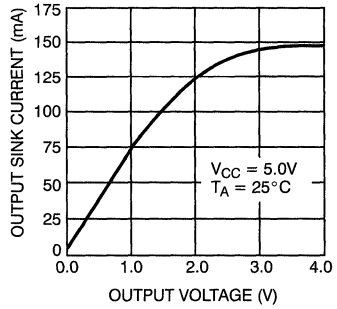
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C235A–9

Ordering Information[9]

Speed (ns)		Ordering Code	Package Name	Package Type	Operating Range
t_{SA}	t_{CO}				
18	12	CY7C235A–18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A–18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C235A–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A–25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C235A–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A–30LMB	L64	28-Square Leadless Chip Carrier	
40	20	CY7C235A–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A–40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A–40LMB	L64	28-Square Leadless Chip Carrier	

Note:
9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

Document #: 38–00229–C

CY7C243
CY7C244

4K x 8 Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **300-mil or 600-mil packaging available**
- **5V ± 10% V_{CC}, commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**

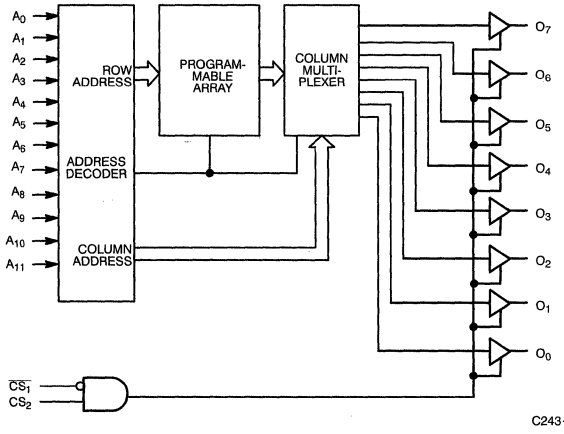
Functional Description

The CY7C243 and CY7C244 are high-performance 4K x 8 CMOS PROMs. The CY7C243 and CY7C244 are packaged in 300-mil-wide and 600-mil-wide packages respectively. The reprogrammable packages are equipped with an erasure window. When exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C243 and CY7C244 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each cell is programmed, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

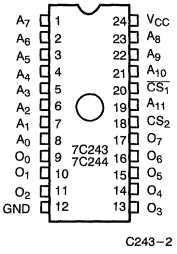
Read is accomplished by placing an active LOW signal on $\overline{CS_1}$ and an active HIGH on CS_2. The contents of the memory location addressed by the address line (A_0 – A_{11}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram

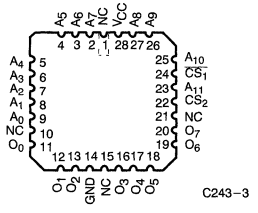


Pin Configurations

DIP/Flatpack
Top View



LCC/PLCC (Opaque Only)
Top View



Selection Guide

		7C243–20 7C244–20	7C243–25 7C244–25	7C243–35 7C244–35	7C243–45 7C244–45	7C243–55 7C244–55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	100	100	80	80	80
	Military		120	100	100	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (V_{CC} to GND) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pin 19 DIP, Pin 23 LCC) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial[1]	−40°C to + 85°C	5V ± 10%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C243−20, 25 7C244−20, 25 Min.	7C243−20, 25 7C244−20, 25 Max.	7C243−35, 45, 55 7C244−35, 45, 55 Min.	7C243−35, 45, 55 7C244−35, 45, 55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4				V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA				2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA (6 mA Mil)			0.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA					0.4	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4		Note 4		
I_{OZ}	Output Leakage Current	0 ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		100		80	mA
			Mil		120		100	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA

Capacitance[4]

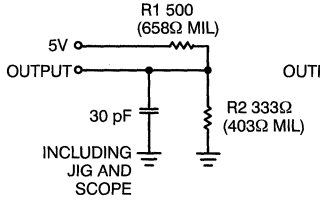
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

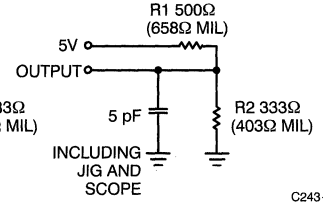
1. See the Ordering Information section regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[4]

Test Load for −20 through −25 speeds

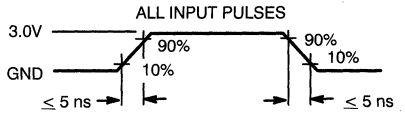


(a) Normal Load



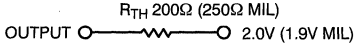
C243−4

(b) High Z Load

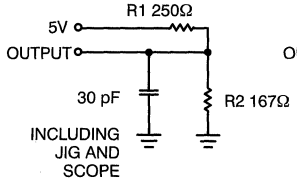


C243−5

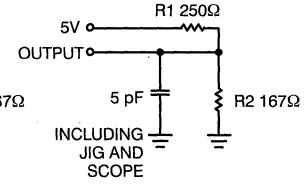
Equivalent to: THÉVENIN EQUIVALENT



Test Load for −35 through −55 speeds



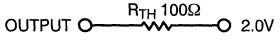
(c) Normal Load



C243−6

(d) High Z Load

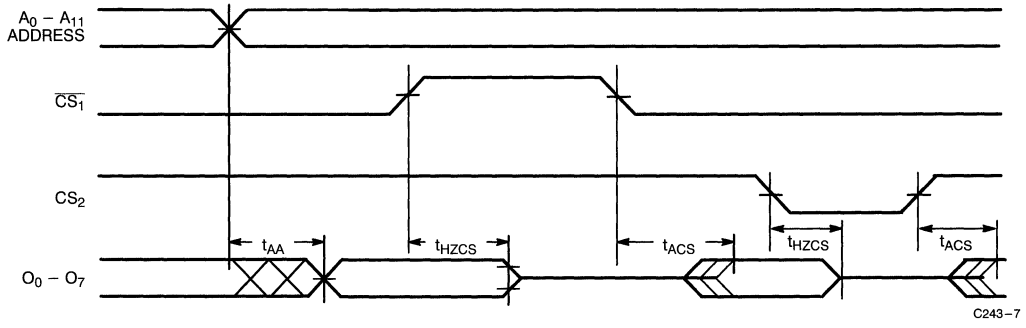
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 3, 4]

Parameter	Description	7C243−20 7C244−20		7C243−25 7C244−25		7C243−35 7C244−35		7C243−45 7C244−45		7C243−55 7C244−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45		55	ns
t_{HZCS} (Com'l)	Chip Select Inactive to High Z		12		12		20		25		25	ns
t_{HZCS} (Mil)	Chip Select Inactive to High Z				15		20		25		25	ns
t_{ACS} (Com'l)	Chip Select Active to Output Valid		12		12		20		25		25	ns
t_{ACS} (Mil)	Chip Select Active to Output Valid				15		20		25		25	ns

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C243 or CY7C244 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Operating Modes

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 12-bit field, an active LOW signal is applied to $\overline{CS_1}$, an active HIGH is applied to CS_2, and the contents of the addressed location appear on the data out pins.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

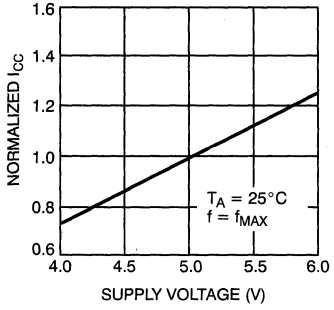
Table 1. Mode Selection

		Pin Function[6]						
	Read or Output Disable	**A_{11}**	**A_{10}**	**A_9**	**A_8**	**$\overline{CS_1}$**	**CS_2**	**$O_7 - O_0$**
Mode	**Program**	**V_{PP}**	**LATCH**	**$\overline{PGM}$**	**$\overline{VFY}$**	**$\overline{CS_1}$**	**NA**	**$D_7 - D_0$**
Read		A_{11}	A_{10}	A_9	A_8	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		A_{11}	A_{10}	A_9	A_8	V_{IH}	X	High Z
Output Disable		A_{11}	A_{10}	A_9	A_8	X	V_{IL}	High Z

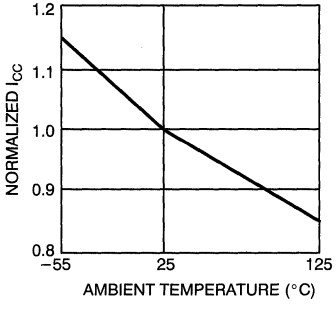
Notes:
6. X can be V_{IL} or V_{IH}.

Typical DC and AC Characteristics

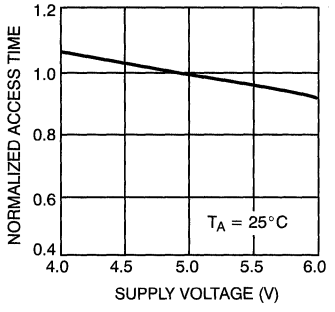
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



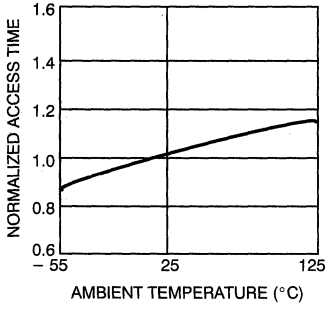
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



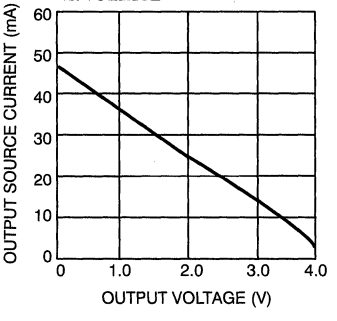
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



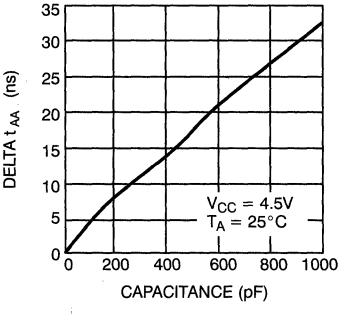
NORMALIZED ACCESS TIME vs. TEMPERATURE



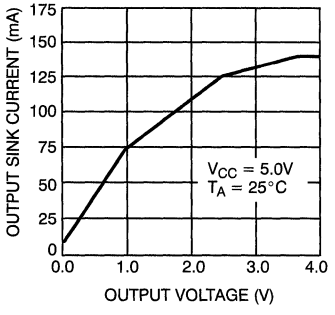
OUTPUT SOURCE CURRENT vs. VOLTAGE



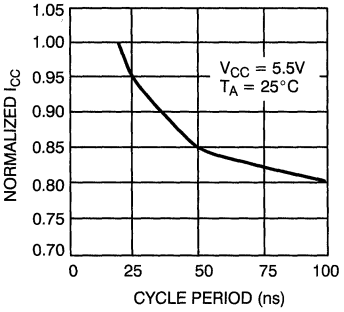
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



Ordering Information[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C243–20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C243–20PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C243–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C243–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C243–25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C243–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C243–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C243–25LMB	L64	28-Square Leadless Chip Carrier	
	CY7C243–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C243–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C243–35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C243–35PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C243–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C243–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C243–35LMB	L64	28-Square Leadless Chip Carrier	
	CY7C243–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C243–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C243–45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C243–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C243–45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C243–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C243–45LMB	L64	28-Square Leadless Chip Carrier	
	CY7C243–45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C243–45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C243–55JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C243–55PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C243–55WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C243–55DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C243–55LMB	L64	28-Square Leadless Chip Carrier	
	CY7C243–55QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C243–55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

7. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information (continued)[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C244–20PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244–20WC	W12	24-Lead (600-Mil) Windowed CerDIP	
25	CY7C244–25PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244–25WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244–25DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C244–25WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
35	CY7C244–35PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244–35WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244–35DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C244–35WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
45	CY7C244–45PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244–45WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244–45DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C244–45WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
55	CY7C244–55PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C244–55WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C244–55DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C244–55WMB	W12	24-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11

Document #: 38–00360–A

CY7C245A

2K x 8 Reprogrammable Registered PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15-ns address set-up**
  - **— 10-ns clock to output**
- **Low power**
  - **— 330 mW (commercial) for −25 ns**
  - **— 660 mW (military)**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

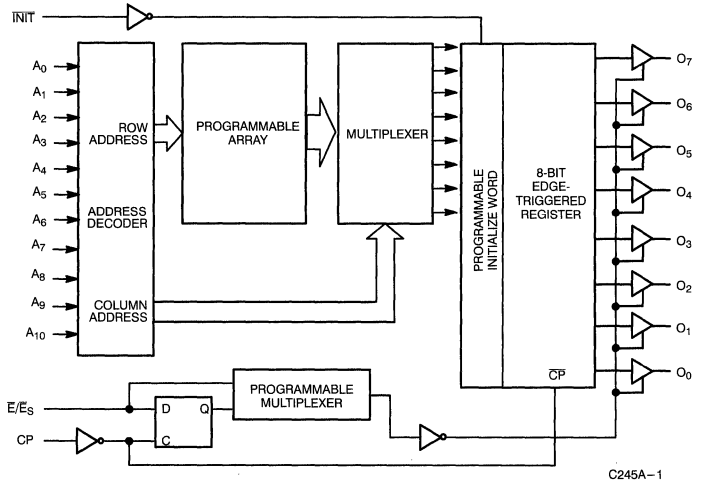
The CY7C245A is a high-performance, 2K x 8, electrically programmable, read only memory packaged in a slim 300-mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C245A replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow gang programming. The EPROM cells allow each memory location to be tested 100%, because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245A has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word, or may be used as a PRESET or CLEAR function on the outputs. $\overline{INIT}$ is triggered by a low level, not an edge.

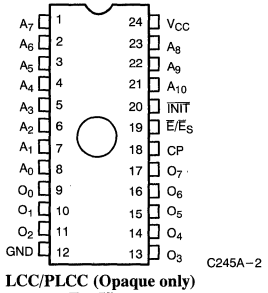
4

Logic Block Diagram

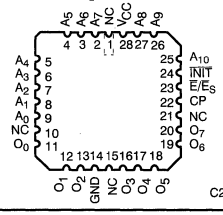


Pin Configurations

DIP
Top View



LCC/PLCC (Opaque only)
Top View



Selection Guide

			7C245A−15	7C245A−18	7C245A−25 7C245AL−25	7C245A−35 7C245AL−35	7C245A−45 7C245AL−45
Minimum Address Set-Up Time (ns)			15	18	25	35	45
Maximum Clock to Output (ns)			10	12	12	15	25
MaximumOperating Current (mA)	Standard	Commercial	120	120	90	90	90
		Military		120	120	120	120
	L	Commercial			60	60	60

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C245A−15		7C245A−18		7C245A−25 7C245A−35 7C245A−45		7C245AL−25 7C245AL−35 7C245AL−45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 4										
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[5]		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		90		60	mA
			Mil				120		120			
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4		0.4	V

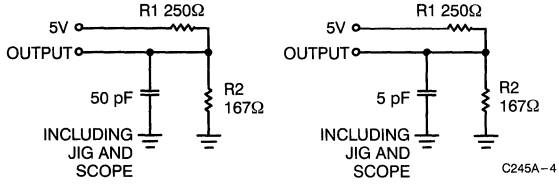
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

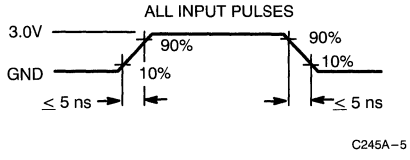
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

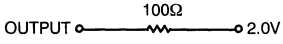
AC Test Loads and Waveforms[3, 4]



(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[3, 4]

Parameter	Description	7C245A–15		7C245A–18		7C245A–25 7C245AL–25		7C245A–35 7C245AL–35		7C245A–45 7C245AL–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	15		18		25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		10		12		12		15		25	ns
t_{PWC}	Clock Pulse Width	10		12		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		15		20		20		20		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	10		12		15		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	10		12		15		20		25		ns
t_{COS}	Valid Output from Clock HIGH[7]		15		15		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		15		15		20		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[8]		12		15		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[8]		15		15		15		20		30	ns

Notes:

7. Applies only when the synchronous ($\overline{E}_S$) function is used.
8. Applies only when the asynchronous ($\overline{E}$) function is used.

Operating Modes

The CY7C245A is a CMOS electrically programmable read only memory organized as 2048 words x 8 bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{INIT}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high-impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs ($A_0 - A_{10}$) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C245A decoders and

Operating Modes (continued)

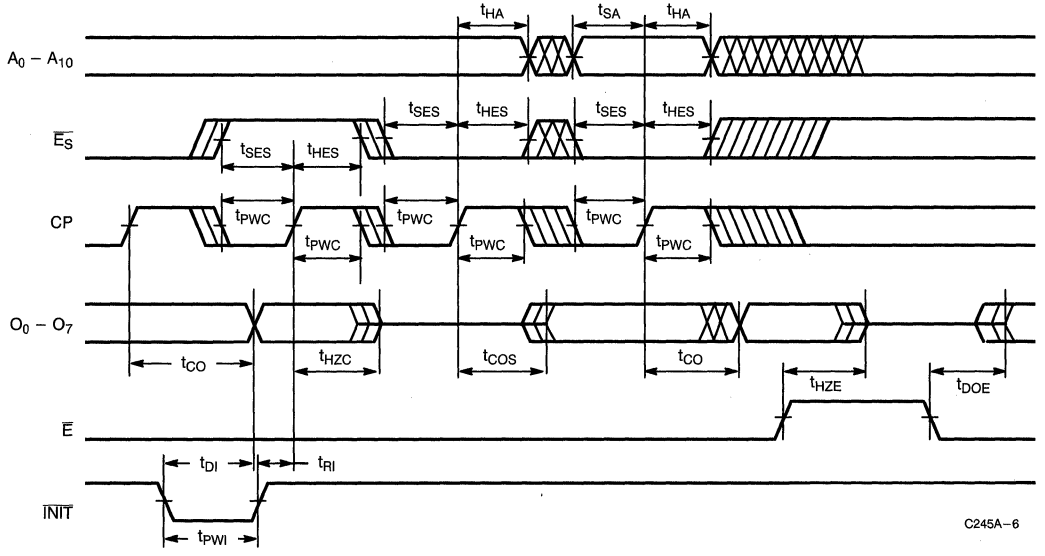
sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user-programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
.	.	.
2047	7FF	Data
2048	800	Init Byte
2049	801	Control Byte

Control Byte

00 Asynchronous output enable (default state)
01 Synchronous output enable

Table 1. Mode Selection

Mode		Pin Function[9]							
	Read or Output Disable	**$A_{10} - A_4$**	**A_3**	**$A_2 - A_1$**	**A_0**	**CP**	**$\overline{E}$, $\overline{E}_S$**	**$\overline{INIT}$**	**$O_7 - O_0$**
	Other	**$A_{10} - A_4$**	**A_3**	**$A_2 - A_1$**	**A_0**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IL}/V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	X	V_{IH}	V_{IH}	High Z
Initialize		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	X	V_{IL}	V_{IL}	Init. Byte
Program		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IHP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Synchronous Enable		$A_{10} - A_4$	V_{IHP}	$A_2 - A_1$	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Initialization Byte		$A_{10} - A_4$	V_{ILP}	$A_2 - A_1$	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Blank Check Zeros		$A_{10} - A_4$	A_3	$A_2 - A_1$	A_0	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Note:
9. X = "don't care" but not to exceed V_{CC} +5%.

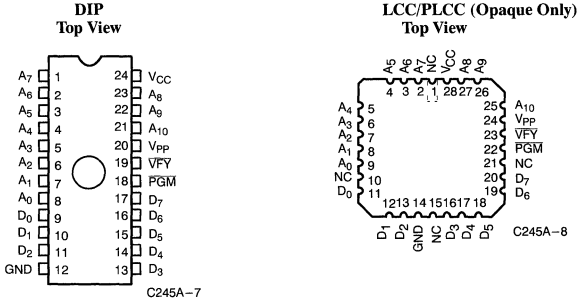
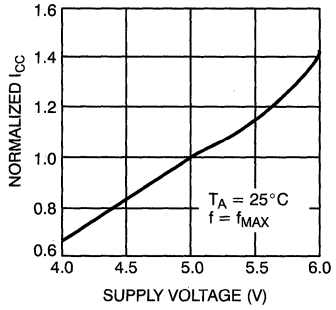


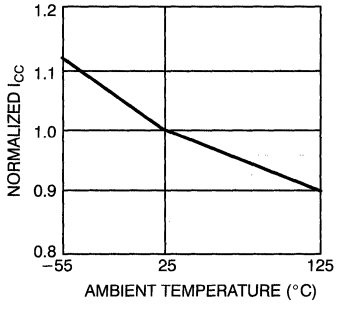
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

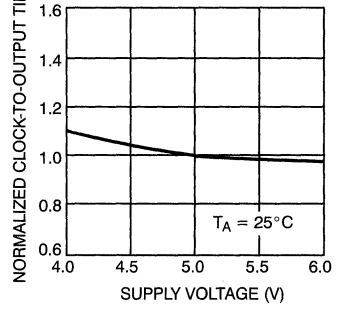
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



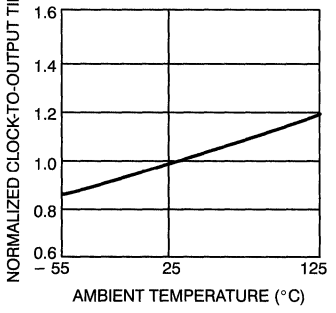
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



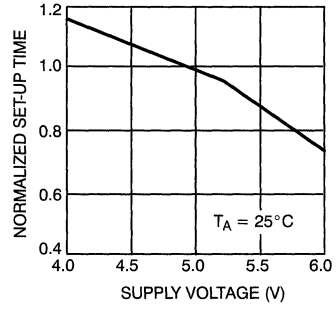
CLOCK TO OUTPUT TIME vs. V_{CC}



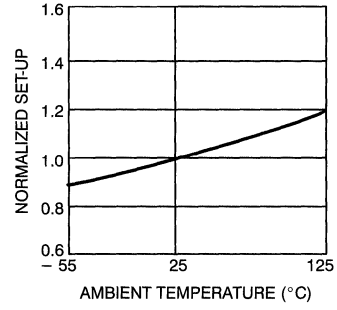
CLOCK TO OUTPUT TIME vs. TEMPERATURE



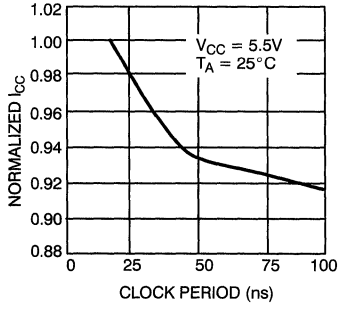
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



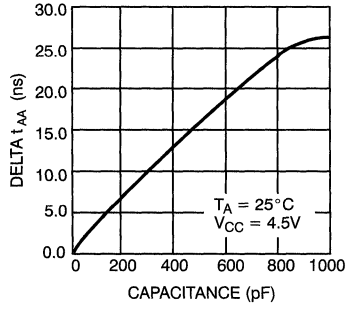
NORMALIZED SET-UP TIME vs. TEMPERATURE



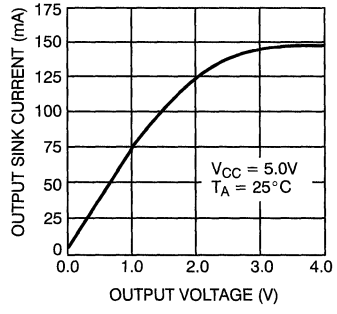
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C245A–9

Ordering Information[10]

Speed (ns)		I_{CC} (mA)	Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}					
15	10	120	CY7C245A–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C245A–15PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
18	12	120	CY7C245A–18JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C245A–18PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–18WC	W14	24-Lead (300-Mil) Windowed CerDIP	
			CY7C245A–18DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–18LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–18QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–18TMB	T73	24-Lead Windowed Cerpack	
			CY7C245A–18WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
25	15	60	CY7C245AL–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
			CY7C245AL–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		90	CY7C245A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A–25PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–25SC	S13	24-Lead Molded SOIC	
			CY7C245A–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		120	CY7C245A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–25LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–25TMB	T73	24-Lead Windowed Cerpack	
			CY7C245A–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	20	60	CY7C245AL–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
			CY7C245AL–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		90	CY7C245A–35JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A–35PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–35SC	S13	24-Lead Molded SOIC	
			CY7C245A–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		120	CY7C245A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–35LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–35TMB	T73	24-Lead Windowed Cerpack	
			CY7C245A–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	25	60	CY7C245A–45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			CY7C245A–45PC	P13	24-Lead (300-Mil) Molded DIP	
		90	CY7C245A–45JC	J64	28-Lead Plastic Leaded Chip Carrier	
			CY7C245A–45PC	P13	24-Lead (300-Mil) Molded DIP	
			CY7C245A–45SC	S13	24-Lead Molded SOIC	
			CY7C245A–45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		120	CY7C245A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
			CY7C245A–45LMB	L64	28-Square Leadless Chip Carrier	
			CY7C245A–45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
			CY7C245A–45TMB	T73	24-Lead Windowed Cerpack	
			CY7C245A–45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:
10. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88735	01KX	CY7C245A–45KMB
5962–88735	01LX	CY7C245A–45DMB
5962–88735	013X	CY7C245A–45LMB
5962–88735	02KX	CY7C245A–35KMB
5962–88735	02LX	CY7C245A–35DMB
5962–88735	023X	CY7C245A–35LMB
5962–88735	03KX	CY7C245A–35KMB
5962–88735	03LX	CY7C245A–35DMB
5962–88735	033X	CY7C245A–25LMB
5962–88735	04KX	CY7C245A–25KMB
5962–88735	04LX	CY7C245A–25DMB
5962–88735	043X	CY7C245A–25LMB
5962–87529	01KX	CY7C245A–45TMB
5962–87529	01LX	CY7C245A–45WMB
5962–87529	013X	CY7C245A–45QMB
5962–87529	02KX	CY7C245A–35TMB
5962–87529	02LX	CY7C245A–35WMB
5962–87529	023X	CY7C245A–35QMB
5962–89815	01LX	CY7C245A–35WMB
5962–89815	01KX	CY7C245A–35TMB
5962–89815	013X	CY7C245A–35QMB
5962–89815	02LX	CY7C245A–25WMB
5962–89815	02KX	CY7C245A–25TMB
5962–89815	023X	CY7C245A–25QMB
5962–89815	03LX	CY7C245A–18WMB
5962–89815	03KX	CY7C245A–18TMB
5962–89815	033X	CY7C245A–18QMB

Document #: 38–00074–G

CY7C251
CY7C254

16K x 8 Power-Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 45 ns**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **Super low standby power (7C251)**
  - **— Less than 165 mW when deselected**
  - **— Fast access: 50 ns**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

Functional Description

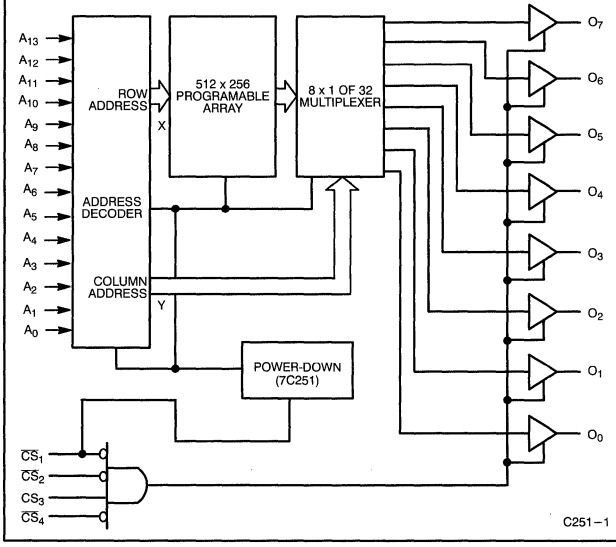
The CY7C251 and CY7C254 are high-performance 16,384-word by 8-bit CMOS PROMs. When deselected, the CY7C251 automatically powers down into a low-power stand-by mode. It is packaged in a 300-mil-wide package. The 7C254 is packaged in a 600-mil-wide package and does not power down when deselected. The 7C251 and 7C254 are available in reprogrammable packages equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C251 and CY7C254 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

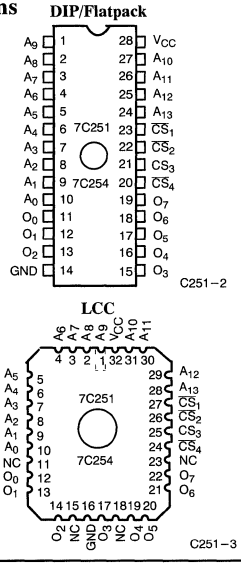
Reading is accomplished by placing all four chip selects in their active states. The contents of the memory location addressed by the address lines (A_0 – A_{13}) will become available on the output lines (O_0 – O_7).

4

Logic Block Diagram



Pin Configurations



Selection Guide

		7C251–45, 7C254–45	7C251–55, 7C254–55	7C251–65, 7C254–65
Maximum Access Time (ns)		45	55	65
Maximum Operating Current (mA)	Commercial	100	100	100
	Military	120	120	120
Standby Current (mA) (7C251 only)	Commercial	30	30	30
	Military	35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pin 22) 13.5V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C251−45, 55, 65 7C254−45, 55, 65 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		100	mA
			Mil		120	
I_{SB}	Standby Supply Current (7C251)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, I_{OUT} = 0 mA	Com'l		30	mA
			Mil		35	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

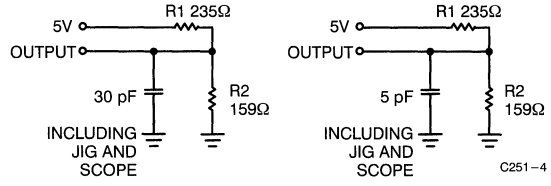
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

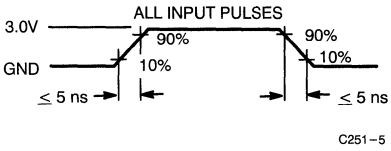
Notes:

1. Contact a Cypress representative regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

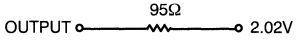
AC Test Loads and Waveforms[4]



(a) Normal Load (b) High Z Load



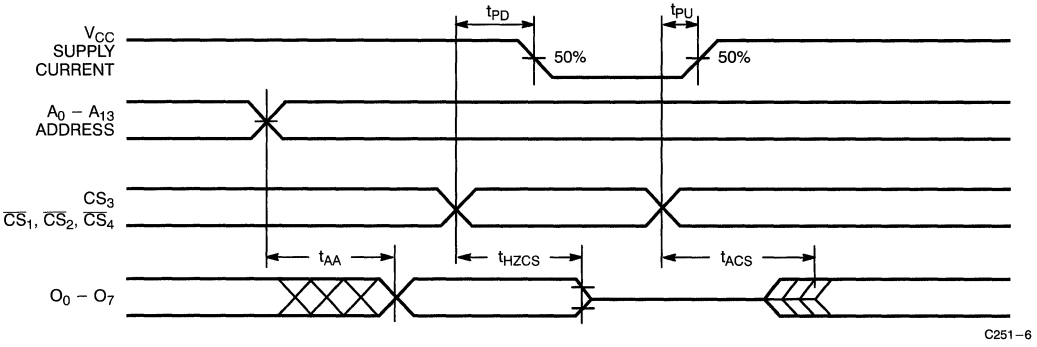
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 4]

Parameter	Description	7C251-45 7C254-45		7C251-55 7C254-55		7C251-65 7C254-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		65	ns
t_{HZCS1}	Chip Select Inactive to High Z[6]		25		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C251, $\overline{CS_1}$ Only)		50		60		70	ns
t_{ACS1}	Chip Select Active to Output Valid[6]		25		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C251, $\overline{CS_1}$ Only)		50		60		70	ns
t_{PU}	Chip Select Active to Power Up (7C251)	0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C251)[7]		50		60		70	ns

Switching Waveform[4, 7]



Notes:

6. t_{HZCS1} and t_{ACS1} refers to 7C254 (all chip selects); and 7C251 ($\overline{CS_2}$, CS_3 and $\overline{CS_4}$ only).
7. Power-down controlled by 7C251 $\overline{CS_1}$ only.

Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the 7C251 and 7C254 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C251 or 7C254 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{VFY}$ toggles on each address), sequencing through all memory address locations, where all the data read will be zeros.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

		Pin Function[8]					
	Read or Output Disable	**$A_{13} - A_0$**	**$\overline{CS}_4$**	**CS_3**	**$\overline{CS}_2$**	**$\overline{CS}_1$**	**$O_7 - O_0$**
Mode	**Other**	**$A_{13} - A_0$**	**NA**	**$\overline{VFY}$**	**V_{PP}**	**$\overline{PGM}$**	**$D_7 - D_0$**
Read		$A_{13} - A_0$	V_{IL}	V_{IH}	V_{IL}	V_{IL}	$O_7 - O_0$
Output Disable		$A_{13} - A_0$	X	X	X	V_{IH}	High Z
Output Disable		$A_{13} - A_0$	X	X	V_{IH}	X	High Z
Output Disable		$A_{13} - A_0$	X	V_{IL}	X	X	High Z
Output Disable		$A_{13} - A_0$	V_{IH}	X	X	X	High Z
Program		$A_{13} - A_0$	X	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Program Verify		$A_{13} - A_0$	X	V_{ILP}	V_{PP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_{13} - A_0$	X	V_{IHP}	V_{PP}	V_{IHP}	High Z
Blank Check		$A_{13} - A_0$	X	V_{ILP}	V_{PP}	V_{IHP}	$O_7 - O_0$

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

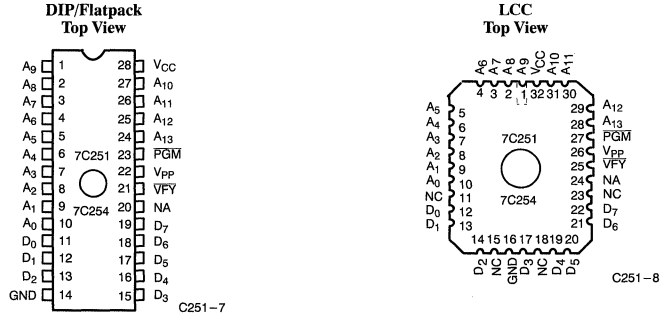
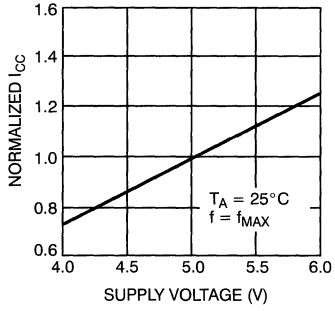


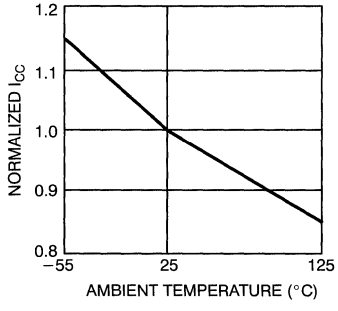
Figure 1. Programming Pinout

Typical DC and AC Characteristics

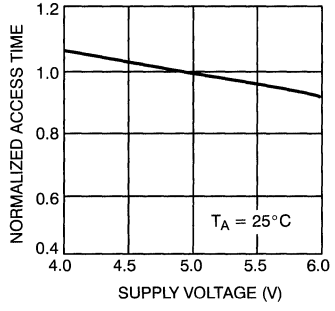
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



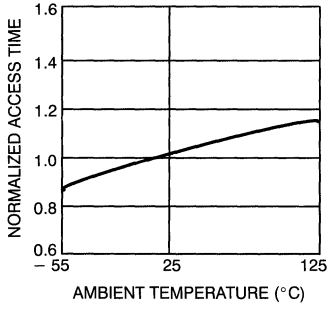
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



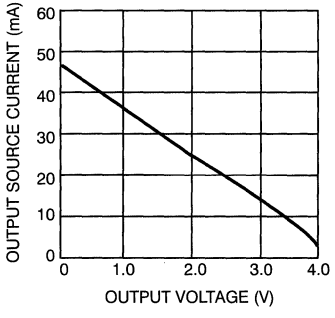
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



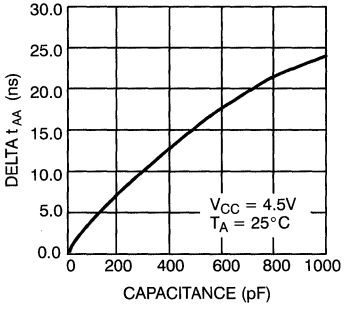
NORMALIZED ACCESS TIME vs. TEMPERATURE



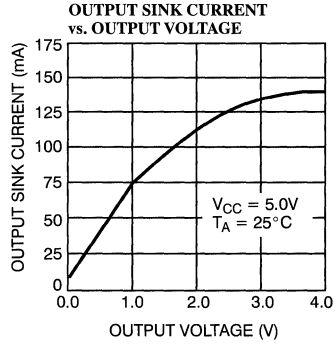
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C251–45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251–45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C251–55PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251–55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C251–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C251–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
65	CY7C251–65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C251–65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C251–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C251–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C251–65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C251–65WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C254–45PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY7C254–55PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C254–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
65	CY7C254–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C254–65WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C254–65DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C254–65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C254–65WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[10]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[11]	7, 8, 9, 10, 11
t_{ACS2}[10]	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–8953701	YX	CY7C251–65WMB
5962–8953701	ZX	CY7C251–65TMB
5962–8953701	VX	CY7C251–65QMB
5962–8953702	YX	CY7C251–55WMB
5962–8953702	ZX	CY7C251–55TMB
5962–8953702	VX	CY7C251–55QMB
5962–8953801	XX	CY7C254–65WMB
5962–8953801	ZX	CY7C254–65TMB
5962–8953801	VX	CY7C254–65QMB
5962–8953802	XX	CY7C254–55WMB
5962–8953802	ZX	CY7C254–55TMB
5962–8953802	VX	CY7C254–55QMB

Notes:
10. 7C251 ($\overline{CS}_1$ only).
11. 7C254 and 7C251 ($\overline{CS}_2$, CS_3 and $\overline{CS}_4$ only).

Document #: 38–00056–G

CY7C261
CY7C263/CY7C264

8K x 8 Power-Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **Super low standby power (7C261)**
  - **— Less than 220 mW when deselected**
  - **— Fast access: 20 ns**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ± 10% V_{CC}, commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**

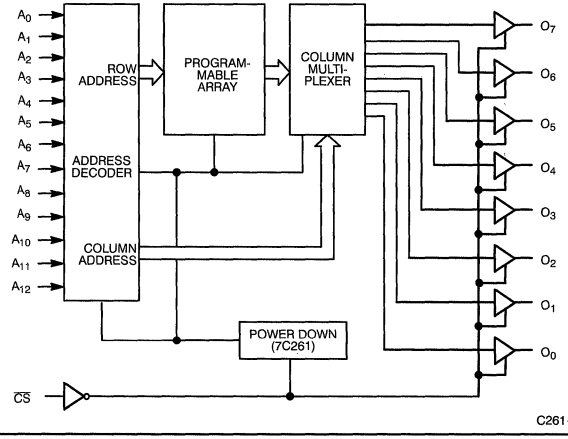
Functional Description

The CY7C261, CY7C263, and CY7C264 are high-performance 8192-word by 8-bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low-power standby mode. It is packaged in a 300-mil-wide package. The 7C263 and 7C264 are packaged in 300-mil-wide and 600-mil-wide packages respectively, and do not power down when deselected. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263, and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

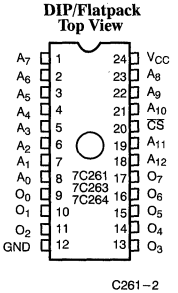
Read is accomplished by placing an active LOW signal on $\overline{CS}$. The contents of the memory location addressed by the address line (A_0 – A_{12}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram

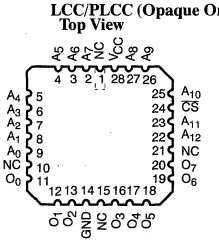


C261–1

Pin Configurations



C261–2



C261–3

Selection Guide

		7C261–20 7C263–20 7C264–20	7C261–25 7C263–25 7C264–25	7C261–35 7C263–35 7C264–35	7C261–45 7C263–45 7C264–45	7C261–55 7C263–55 7C264–55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	120	120	100	100	100
	Military		140	120	120	120
Maximum Standby Current (mA) (7C261 only)	Commercial	40	40	30	30	30
	Military		40	30	30	30

For an 8K x 8 Registered PROM, see theCY7C265.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to + 7.0V

DC Program Voltage (Pin 19 DIP, Pin 23 LCC) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial[1]	−40°C to + 85°C	5V ± 10%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C261−20, 25 7C263−20, 25 7C264−20, 25 Min.	7C261−20, 25 7C263−20, 25 7C264−20, 25 Max.	7C261−35, 45, 55 7C263−35, 45, 55 7C264−35, 45, 55 Min.	7C261−35, 45, 55 7C263−35, 45, 55 7C264−35, 45, 55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4				V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA				2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA (6 mA Mil)			0.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA					0.4	V
V_{IH}	Input HIGH Level			2.0		2.0		V
V_{IL}	Input LOW Level				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4		Note 4		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled	Com'l	−10	+10	−10	+10	µA
			Mil	−40	+40	−40	+40	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., f = Max. I_{OUT} = 0 mA	Com'l		120		100	mA
			Mil		140		120	
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}	Com'l		40		30	mA
			Mil		40		30	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			4.75		4.75		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Capacitance[4]

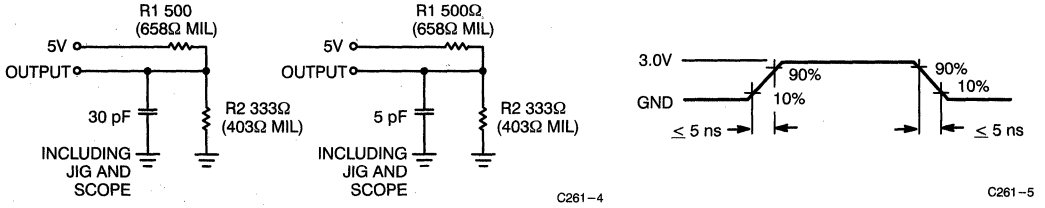
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. See the Ordering Information section regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

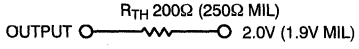
AC Test Loads and Waveforms[4]

Test Load for −20 through −30 speeds

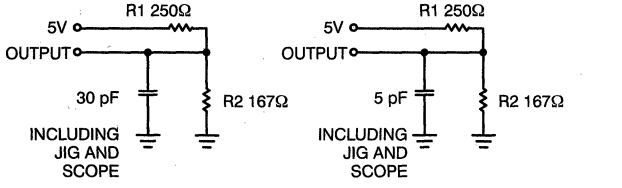


(a) Normal Load **(b) High Z Load**

Equivalent to: THÉVENIN EQUIVALENT

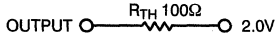


Test Load for −35 through −55 speeds



(c) Normal Load **(d) High Z Load**

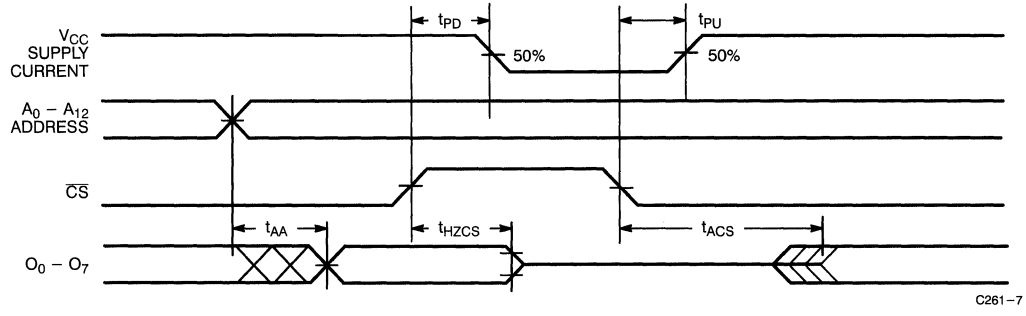
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 3, 4]

Parameter	Description	7C261−20 7C263−20 7C264−20		7C261−25 7C263−25 7C264−25		7C261−35 7C263−35 7C264−35		7C261−45 7C263−45 7C264−45		7C261−55 7C263−55 7C264−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45		55	ns
t_{HZCS1}	Chip Select Inactive to High Z (7C263 and 7C264)		12		12		20		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C261)		20		25		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid (7C263 and 7C264)		12		12		20		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		20		25		35		45		55	ns
t_{PU}	Chip Select Active to Power-Up (7C261)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down (7C261)		20		25		35		45		55	ns

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13-bit field, a chip select, (active LOW), is applied to the $\overline{CS}$ pin, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP}. In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{PGM}$) signal and pin 23 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The verify mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the program inhibit mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. Program inhibit is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Programming Information

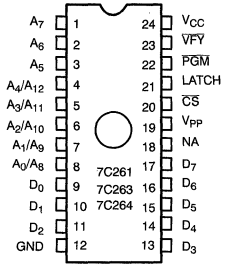
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Read or Output Disable / Program	Pin Function[6, 7] A_{12} / NA	A_{11} / V_{PP}	A_{10} / LATCH	A_9 / $\overline{PGM}$	A_8 / $\overline{VFY}$	$\overline{CS}$ / $\overline{CS}$	$O_7 - O_0$ / $D_7 - D_0$
Read		A_{12}	A_{11}	A_{10}	A_9	A_8	V_{IL}	$O_7 - O_0$
Output Disable		A_{12}	A_{11}	A_{10}	A_9	A_8	V_{IH}	High Z
Program		V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	$D_7 - D_0$
Program Inhibit		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	High Z
Program Verify		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	$O_7 - O_0$
Blank Check		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	$O_7 - O_0$

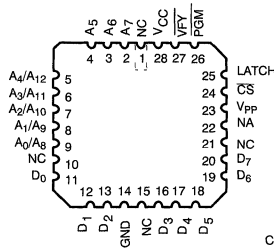
Notes:
6. X = "don't care" but not to exceed V_{CC} ±5%.
7. Addresses $A_8 - A_{12}$ must be latched through lines $A_0 - A_4$ in programming modes.

DIP/Flatpack
Top View



C261–8

LCC/PLCC (Opaque only)
Top View

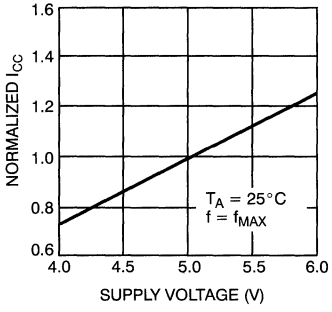


C261–9

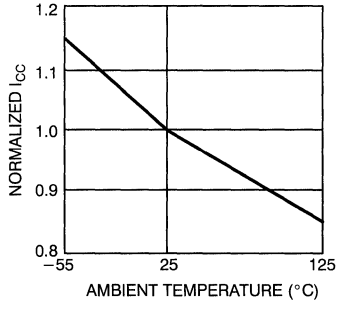
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

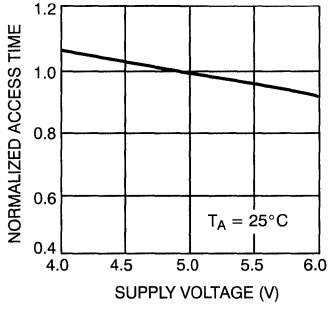
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



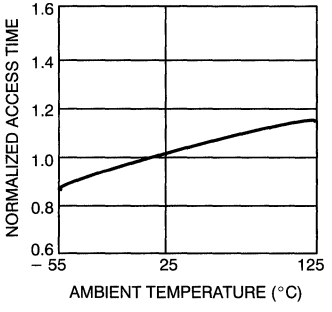
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



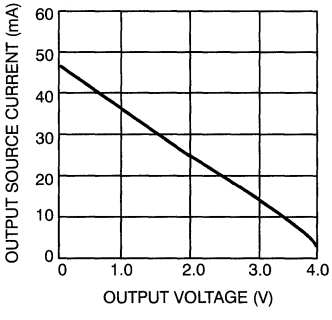
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



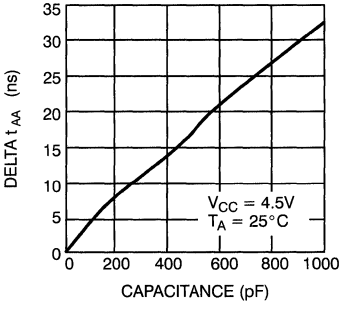
NORMALIZED ACCESS TIME vs. TEMPERATURE



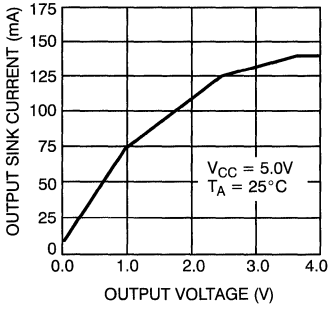
OUTPUT SOURCE CURRENT vs. VOLTAGE



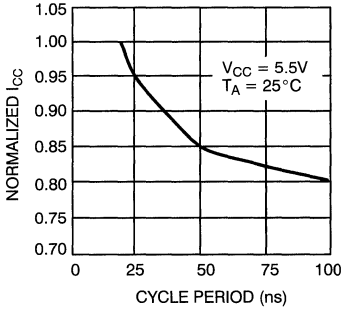
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C261–20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261–20PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C261–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261–25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261–25LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261–25TMB	T73	24-Lead Windowed Cerpack	
	CY7C261–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C261–35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261–35PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261–35LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261–35TMB	T73	24-Lead Windowed Cerpack	
	CY7C261–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C261–45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261–45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261–45LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261–45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261–45TMB	T73	24-Lead Windowed Cerpack	
	CY7C261–45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C261–55JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261–55PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261–55WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261–55DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C261–55LMB	L64	28-Square Leadless Chip Carrier	
	CY7C261–55QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C261–55TMB	T73	24-Lead Windowed Cerpack	
	CY7C261–55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:

8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[8] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C263–20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–20PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C263–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–25LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–25TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C263–35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–35PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–35LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–35TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C263–45JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–45LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–45QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–45TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C263–55JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263–55PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C263–55WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263–55DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C263–55LMB	L64	28-Square Leadless Chip Carrier	
	CY7C263–55QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C263–55TMB	T73	24-Lead Windowed Cerpack	
	CY7C263–55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C264–20DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–20PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–20WC	W12	24-Lead (600-Mil) Windowed CerDIP	
25	CY7C264–25DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–25PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–25WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–25DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–25WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
35	CY7C264–35DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–35PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–35WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–35DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–35WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
45	CY7C264–45DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–45PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–45WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–45DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–45WMB	W12	24-Lead (600-Mil) Windowed CerDIP	
55	CY7C264–55DC	D12	24-Lead (600-Mil) CerDIP	Commercial
	CY7C264–55PC	P11	24-Lead (600-Mil) Molded DIP	
	CY7C264–55WC	W12	24-Lead (600-Mil) Windowed CerDIP	
	CY7C264–55DMB	D12	24-Lead (600-Mil) CerDIP	Military
	CY7C264–55WMB	W12	24-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[9]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[10]	7, 8, 9, 10, 11
t_{ACS2}[9]	7, 8, 9, 10, 11

Notes:
9. 7C261 only.
10. 7C263 and 7C264 only.

Document #: 38–00005–J

8K x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed (commercial and military)**
  - **— 15 ns address set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **On-chip edge-triggered registers**
  - **— Ideal for pipelined microprogrammed systems**
- **EPROM technology**
  - **— 100% programmable**
  - **— Reprogrammable (7C265W)**
- **5V ±10% V_{CC}, commercial and military**
- **Capable of withstanding >2001V static discharge**
- **Slim 28-pin, 300-mil plastic or hermetic DIP**

Functional Description

The CY7C265 is a 8192 x 8 registered PROM. It is organized as 8,192 words by 8 bits wide, and has a pipeline output register. In addition, the device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM and its value is programmed at the time of use.

Packaged in 28 pins, the PROM has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{E}/\overline{I}$ (enable or initialize), and CLOCK.

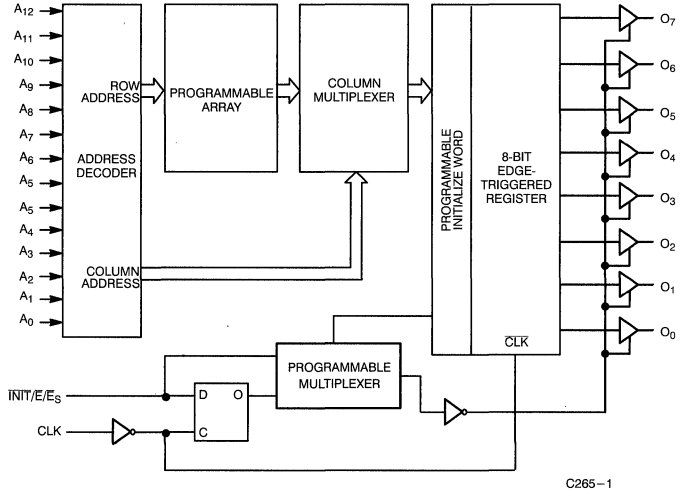
CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the CY7C265 is programmed to perform either the enable or the initialize function.

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C265 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

4

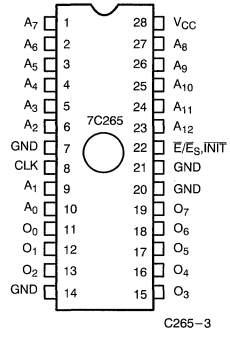
Logic Block Diagram



C265–1

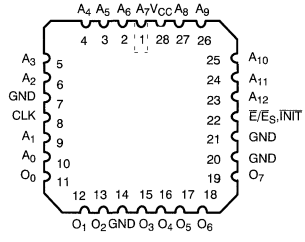
Pin Configurations

DIP/Flatpack
Top View



C265–3

LCC/PLCC (Opaque Only)
Top View



C265–2

Functional Description (continued)

If the E/I pin is used for $\overline{INIT}$ (asynchronous), then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences, and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1's and 0's into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register clear (all outputs LOW). If all the bits of the initialize word are programmed to be a 1, activating $\overline{INIT}$ performs a register preset (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The $\overline{INIT}$ LOW disables clock and must return HIGH to enable clock independent of all other inputs, including the clock.

Selection Guides

		7C265–15	7C265–25	7C265–40	7C265–50
Minimum Address Set-Up Time (ns)		15	25	40	50
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Com'l	120	120	100	80
	Mil	140	140		120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C265–15, 25 Min.	7C265–15, 25 Max.	7C265–40 Min.	7C265–40 Max.	7C265–50 Min.	7C265–50 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4						V
		V_{CC} = Min., I_{OH} = −4.0 mA				2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4					V
		V_{CC} = Min., I_{OL} = 12.0 mA					0.4		0.4	
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4					
		V_{CC} = Min., I_{OL} = 8.0 mA							0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	µA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		100		80	mA
			Mil		140				120	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA

Electrical Characteristics Over the Operating Range[3](continued)

Parameter	Description	Test Conditions	7C265–15, 25		7C265–40		7C265–50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{IHP}	Input HIGH Programming Voltage		3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage			0.4		0.4		0.4	V

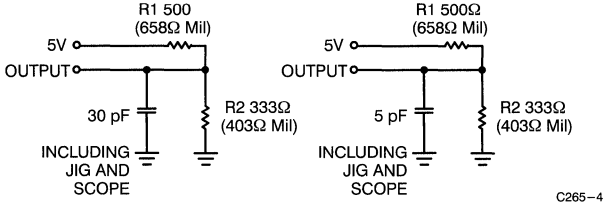
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

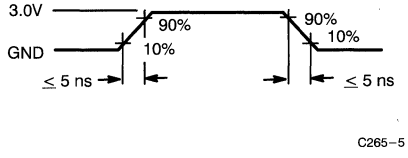
Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

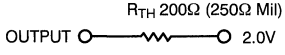
Test Load for −15 through −25 speeds



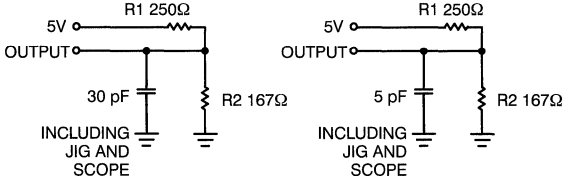
(a) Normal Load **(b) High Z Load**



Equivalent to: THÉVENIN EQUIVALENT

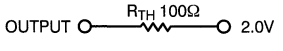


Test Load for −40 through −50 speeds



(c) Normal Load **(d) High Z Load**

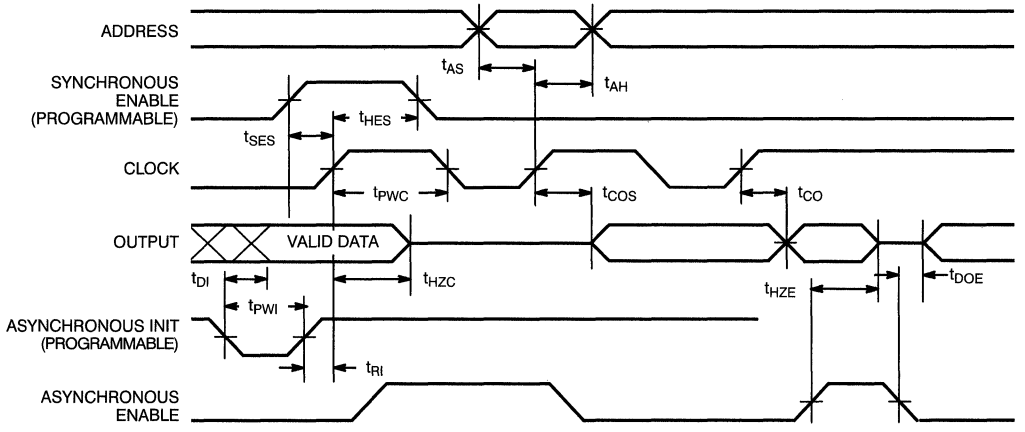
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 5]

Parameter	Description	7C265–15		7C265–25		7C265–40		7C265–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{HA}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync. Enable Only)	12		15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		5		ns
t_{DI}	$\overline{INIT}$ to Output Valid		15		18		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		12		15		20		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20		25	ns

Switching Waveform



C265–7

Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the 7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity • exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C265 needs to be within one inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	INIT Byte
8193	2001	Control Byte

Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize

Programming Modes

The 7C265 offers a limited selection of programmed architectures. Programming these features should be done with a single 10-ms-wide pulse in place of the intelligent algorithm, mainly because these features are verified operationally, not with the $\overline{VFY}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture, V_{PP} is applied to pins 3, 9, and 22. The choice of a particular mode depends on the states of the other pins during programming, so it is important that the condition of the other pins be met as set forth in the mode table. The considerations that apply with respect to power-up and power-down during intelligent programming also apply during architecture programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{PGM}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

Table 1. Mode Selection

		Pin Function						
	Read or Output Disable	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**
Mode	**Other**	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**
Asynchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Synchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Asynchronous Initialization Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Memory		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Verify		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Inhibit		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2
Program Synchronous Enable		V_{IHP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{IHP}
Program Initialize		V_{ILP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}
Program Initial Byte		A_{12}	V_{ILP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}

		Pin Function						
	Read or Output Disable	**A_1**	**A_0**	**GND**	**CLK**	**GND**	**$\overline{E}, \overline{I}$**	**$O_7 - O_0$**
Mode	**Other**	**A_1**	**A_0**	**$\overline{PGM}$**	**CLK**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Asynchronous Enable Read		A_1	A_0	GND	V_{IL}	GND	V_{IL}	$O_7 - O_0$
Synchronous Enable Read		A_1	A_0	GND	V_{IL}/V_{IH}	GND	V_{IL}	$O_7 - O_0$
Asynchronous Initialization Read		A_1	A_0	GND	V_{IL}	GND	V_{IL}	$O_7 - O_0$
Program Memory		A_1	A_0	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		A_1	A_0	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		A_1	A_0	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initial Byte		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$

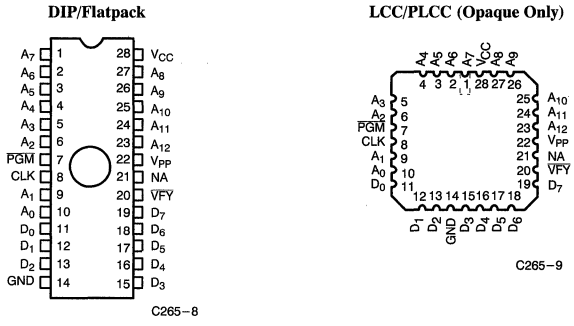
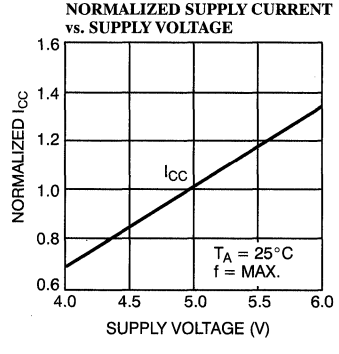


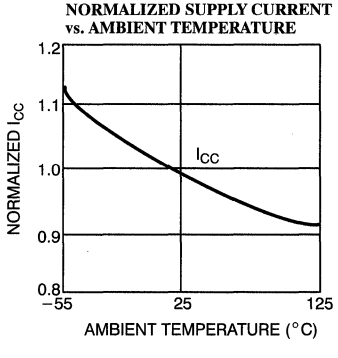
Figure 1. Programming Pinout

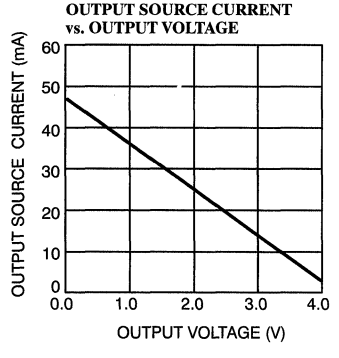
Programming Information

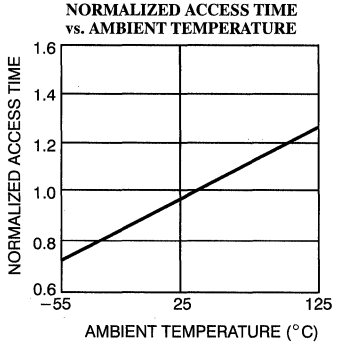
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

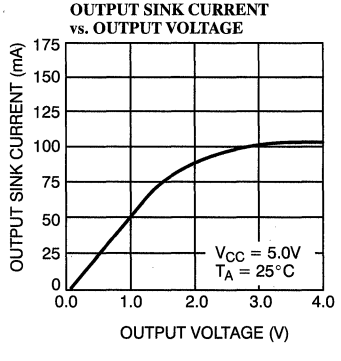
Typical DC and AC Characteristics

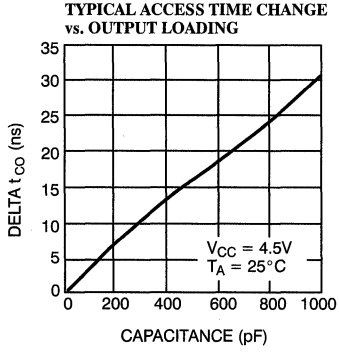




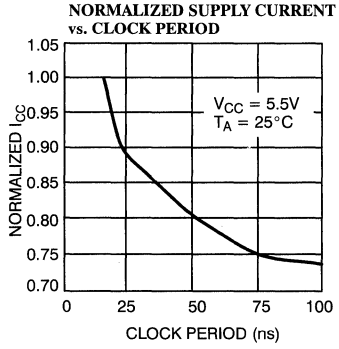








Typical DC and AC Characteristics (continued)



Ordering Information[6]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	120	CY7C265–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–15PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C265–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265–15LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265–15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
25	120	CY7C265–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–25PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C265–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265–25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Notes:
6. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[6]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
40	100	CY7C265–40JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–40PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	80	CY7C265–50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	120	CY7C265–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

Document #: 38–00084–E

8K x 8 Power-Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 770 mW (military)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for 27C64 EPROMs**

Functional Description

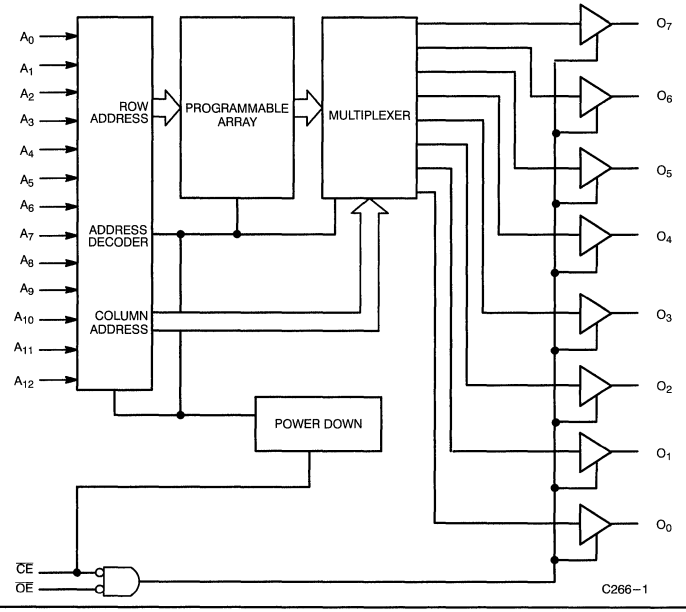
The CY7C266 is a high-performance 8192 word by 8 bit CMOS PROM. When deselected, the CY7C266 automatically powers down into a low-power standby mode. It is packaged in a 600-mil-wide package. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C266 is a plug-in replacement for EPROM devices. The EPROM cell requires only 12.5V for the super voltage and low-current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

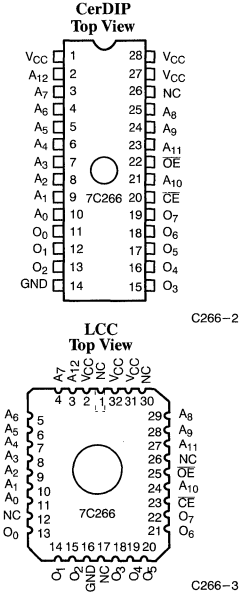
Reading is accomplished by placing an active LOW signal on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 through A_{12}) will become available on the output lines (O_0 through O_7).

4

Logic Block Diagram



Pin Configurations



Selection Guide

		7C266–20	7C266–25	7C266–35	7C266–45
Maximum Access Time (ns)		20	25	35	45
Maximum Operating Current (mA)	Commercial	120	120	100	100
	Military		140		120
Maximum Standby Current (mA)	Commercial	15	15	15	15
	Military		15		15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C266−20 Min.	7C266−20 Max.	7C266−25 Min.	7C266−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	Com'l	2.4		2.4		V
			Mil			2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil				0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4				
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA	Com'l		120		120	mA
			Mil				140	
I_{SB}	Standby Supply Current	Chip Enable Inactive, $\overline{CE}$ ≥ V_{IH}, I_{OUT} = 0 mA	Com'l		15		15	mA
			Mil				15	

Notes:

1. Contact a Cypress representative regarding industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[4, 5] (continued)

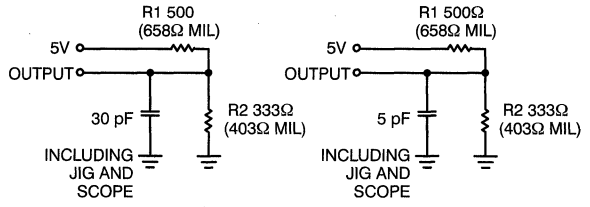
Parameter	Description	Test Conditions		7C266–35 Min.	7C266–35 Max.	7C266–45 Min.	7C266–45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 4				
I_{OZ}	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA	Com'l		100		100	mA
			Mil				120	
I_{SB}	Standby Supply Current	Chip Enable Inactive, $\overline{CE} \ge V_{IH}$, I_{OUT} = 0 mA	Com'l		15		15	mA
			Mil				15	

Capacitance[5]

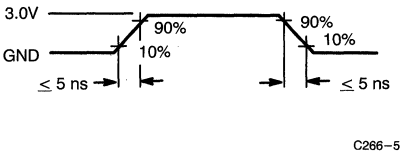
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms

Test Load for −20 through −25 speeds

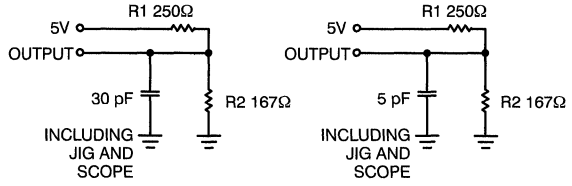


(a) Normal Load **(b) High Z Load** C266−4



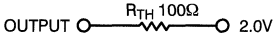
Equivalent to: THEVENIN EQUIVALENT

Test Load for −35 through −55 speeds



(c) Normal Load **(d) High Z Load** C266−6

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 3, 5]

Parameter	Description	7C266−20		7C266−25		7C266−35		7C266−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45	ns
t_{HZCE}	Chip Enable Inactive to High Z		25		30		40		45	ns
t_{HZOE}	Output Enable Inactive to High Z		12		12		20		25	ns
t_{AOE}	Output Enable Active to Output Valid		12		12		20		25	ns
t_{ACE}	Chip Enable Active to Output Valid		25		30		40		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{PU}	Chip Enable Active to Power-Up		25		30		40		45	ns
t_{PD}	Chip Enable Inactive to Power-Down		25		30		40		45	ns

Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C266 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[6, 7]							
	Normal Operation	**A_8**	**A_9**	**A_{10}**	**A_{11}**	**A_{12}**	**$\overline{CE}$**	**$\overline{OE}$**	**$D_7 - D_0$**
	Program	**$\overline{VFY}$**	**$\overline{PGM}$**	**LAT**	**NA**	**NA**	**$\overline{CE}$**	**V_{PP}**	**$D_7 - D_0$**
Read		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IL}	$O_7 - O_0$
Standby		X	X	X	X	X	V_{IH}	X	Three-Stated
Output Disable		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IH}	Three-Stated
Program		V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	Three-Stated
Blank Check		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$

Notes:

6. X = "don't care" but must not exceed V_{CC} + 5%.
7. Address $A_8 - A_{12}$ must be latched through lines $A_0 - A_4$ in Programming modes.

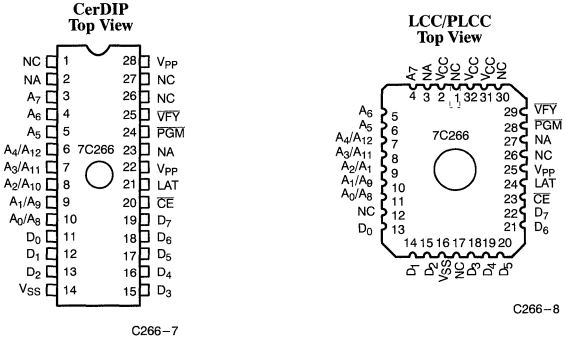
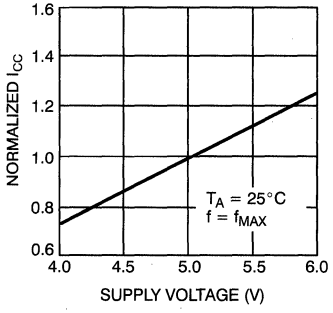


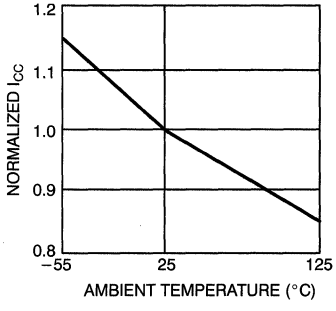
Figure 1. Programming Pinout

Typical DC and AC Characteristics

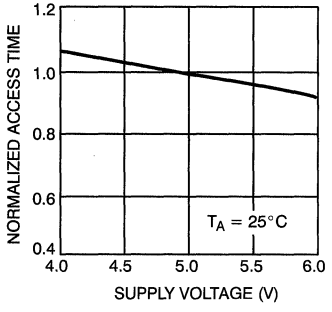
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



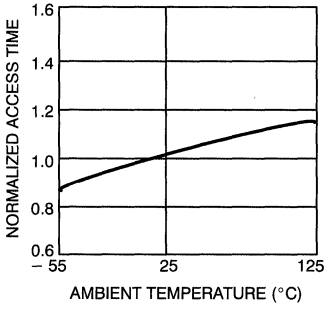
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



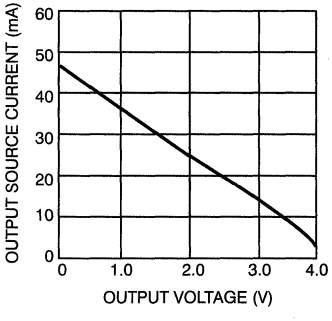
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



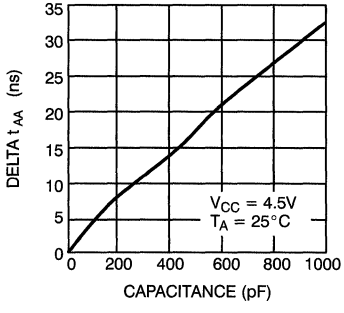
NORMALIZED ACCESS TIME vs. TEMPERATURE



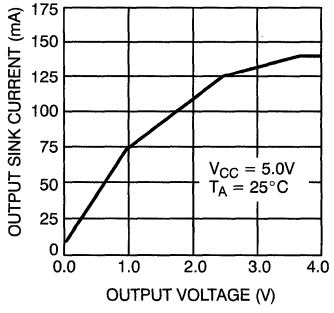
OUTPUT SOURCE CURRENT vs. VOLTAGE



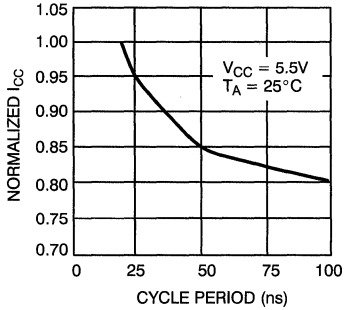
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C266–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–20WC	W16	28-Lead (600-Mil) Windowed CerDIP	
25	CY7C266–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–25WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C266–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C266–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C266–25QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C266–25WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
35	CY7C266–35PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
45	CY7C266–45PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C266–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C266–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C266–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C266–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:
9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{AOE}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Document #: 38–00086–D

CY7C269

8K x 8 Registered Diagnostic PROM

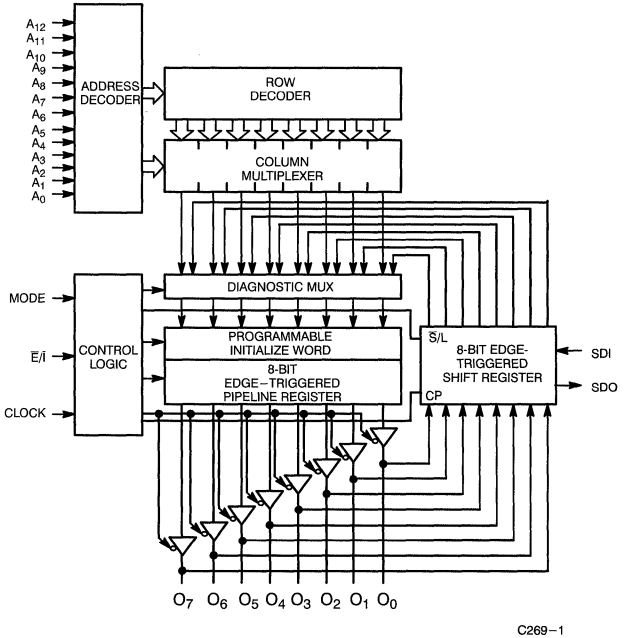
Features

- CMOS for optimum speed/power
- High speed (commercial and military)
  - 15-ns address set-up
  - 12-ns clock to output
- Low power
  - 660 mW (commercial)
  - 770 mW (military)
- On-chip edge-triggered registers
  - Ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register
  - For serial observability and controllability of the output register
- EPROM technology
  - 100% programmable
  - Reprogrammable (7C269W)
- 5V ±10% V_{CC}, commercial and military
- Capable of withstanding >2001V static discharge
- Slim 300-mil, 28-pin plastic or hermetic DIP

Functional Description

The CY7C269 is a 8K x 8 registered diagnostic PROM. It is organized as 8,192 words by 8 bits wide, and has both a pipeline output register and an onboard diagnostic shift register. The device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM, and may be programmed to any desired value.

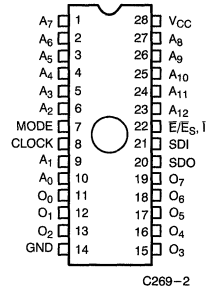
Logic Block Diagram



C269-1

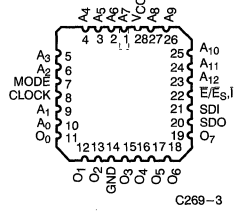
Pin Configurations

CerDIP/Flatpack Top View



C269-2

LCC/PLCC (Opaque Only) Top View



C269-3

Selection Guide

		7C269-15	7C269-25	7C269-40	7C269-50
Minimum Address Set-Up Time (ns)		15	25	40	50
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	120	120	100	80
	Military	140	140		120

Functional Description (continued)

The CY7C269 is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, it has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{E}/I$ (Enable or Initialize), and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SDI (shift in), and SDO (shift out). Normal pipelined operation and diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the 7C269 is programmed to perform either the Enable or the Initialize function. If the $\overline{E}/I$ pin is used for a $\overline{INIT}$ (asynchronous initialize) function, the outputs are permanently enabled and the initialize word is loaded into the pipeline register on a HIGH to LOW transition of the $\overline{INIT}$ signal. The $\overline{INIT}$ LOW disables CLOCK and must return high to re-enable CLOCK. If the $\overline{E}/I$ pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation.

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The $\overline{E}/I$ signal becomes a secondary mode signal designating whether to shift the diagnostic shift register or to load either the diagnostic register or the pipeline register. If $\overline{E}/I$ is HIGH, it shifts SDI into the least-significant location of the diagnostic register and all bits one location toward the most-significant location on each rising edge. The contents of the most-significant location in the diagnostic register are available on the SDO pin.

If the $\overline{E}/I$ signal is LOW, SDI becomes a direction signal, transferring the contents of the diagnostic register into the pipeline register when SDI is LOW. When SDI is HIGH, the contents of the output pins are transferred into the diagnostic register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the outputs are enabled, the contents of the pipeline register are transferred into the diagnostic register. If the outputs are disabled, an external source of data may be loaded into the diagnostic register. In this condition, the SDO signal is internally driven to be the same as the SDI signal, thus propagating the "direction of transfer information" to the next device in the string.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C269–15, 25 Min.	7C269–15, 25 Max.	7C269–40 Min.	7C269–40 Max.	7C269–50 Min.	7C269–50 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4						V
		V_{CC} = Min., I_{OH} = −4.0 mA				2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4					V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4					
		V_{CC} = Min., I_{OL} = 12.0 mA	Com'l				0.4		0.4	V
		V_{CC} = Min., I_{OL} = 8.0 mA	Mil				0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	µA
I_{OS}[5]	Output Short Circuit Current				90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		100		80	mA
			Mil		140				120	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

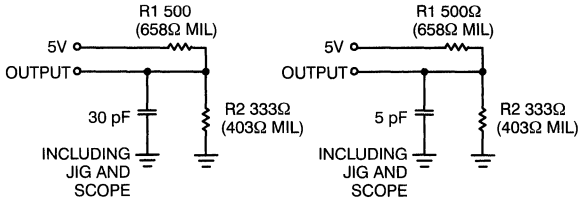
Capacitance[4, 6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

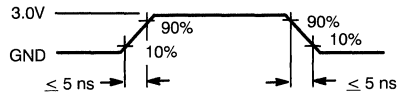
AC Test Loads and Waveforms

Test Load for −15 through −25 speeds



(a) Normal Load (b) High Z Load

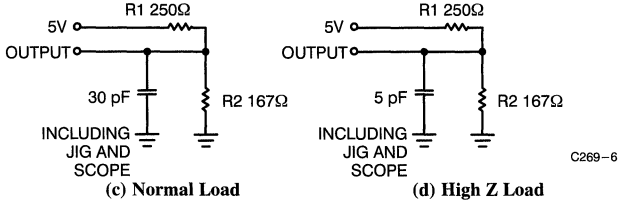
C269-4



C269-5

Equivalent to: THÉVENIN EQUIVALENT

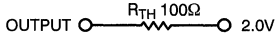
Test Load for −40 through −50 speeds



(c) Normal Load (d) High Z Load

C269-6

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 4]

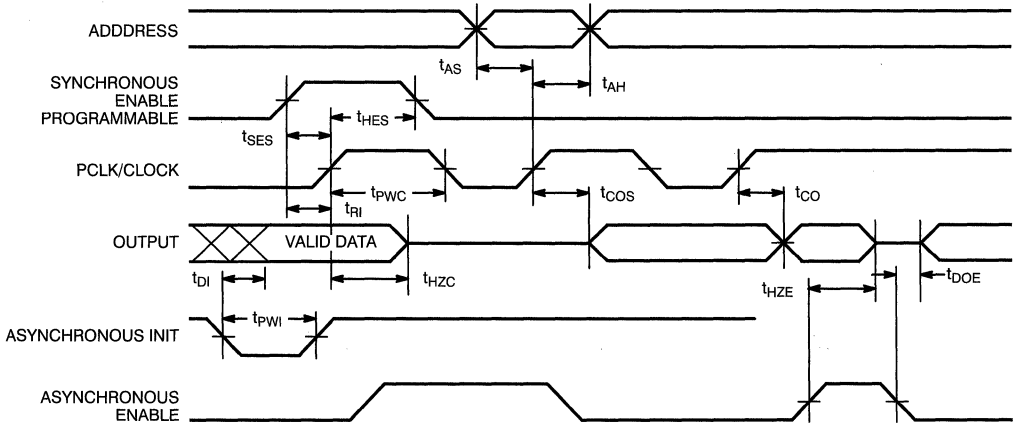
Parameter	Description	7C269−15		7C269−25		7C269−40		7C269−50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{AH}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync Enable Only)	12		15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		5		ns
t_{DI}	$\overline{INIT}$ to Out Valid		15		18		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		12		15		20		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20		25	ns

Diagnostic Mode Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description		7C269–15 Min.	7C269–15 Max.	7C269–25 Min.	7C269–25 Max.	7C269–40,50 Min.	7C269–40,50 Max.	Unit
t_{SSDI}	Set-Up SDI to Clock	Com'l	20		25		30		ns
		Mil	25		30		35		
t_{HSDI}	SDI Hold from Clock	Com'l	0		0		0		ns
		Mil	0		0		0		
t_{DSDO}	SDO Delay from Clock	Com'l		20		25		30	ns
		Mil		25		30		40	
t_{DCL}	Minimum Clock LOW	Com'l	20		25		25		ns
		Mil	25		25		25		
t_{DCH}	Minimum Clock HIGH	Com'l	20		25		25		ns
		Mil	25		25		25		
t_{SM}	Set-Up to Mode Change	Com'l	20		25		25		ns
		Mil	25		30		30		
t_{HM}	Hold from Mode Change	Com'l	0		0		0		ns
		Mil	0		0		0		
t_{MS}	Mode to SDO	Com'l		20		25		25	ns
		Mil		25		30		30	
t_{SS}	SDI to SDO	Com'l		30		40		40	ns
		Mil		35		40		45	
t_{SO}	Data Set-Up to DCLK	Com'l	20		25		25		ns
		Mil	25		30		30		
t_{HO}	Data Hold from DCLK	Com'l	10		10		10		ns
		Mil	13		13		15		

Switching Waveforms[3, 4]

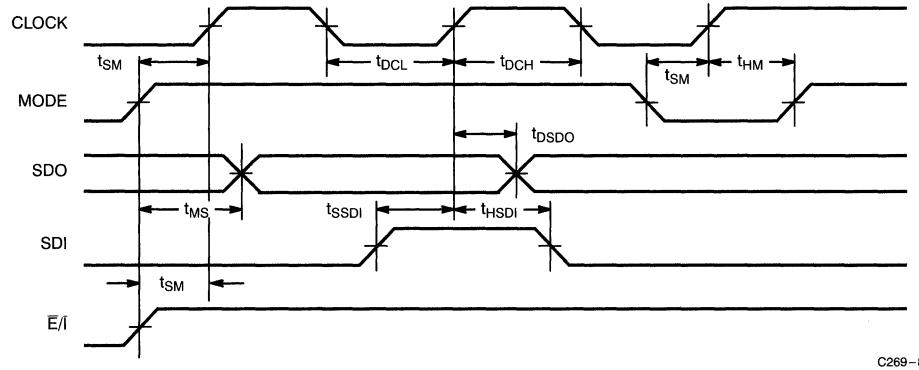
Pipeline Operation (Mode = 0)



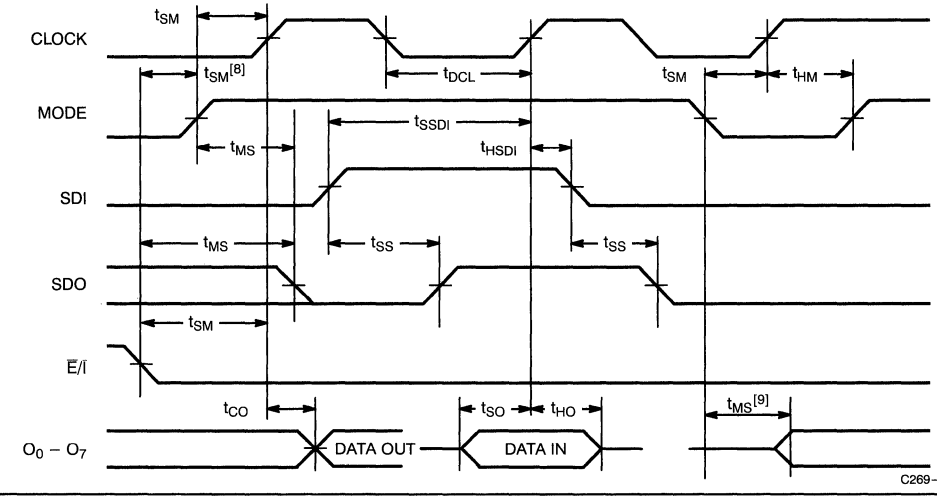
C269–7

Switching Waveforms[3, 4] (continued)

Diagnostic Application (Shifting the Shadow Register[7])



Diagnostic Application (Parallel Data Transfer)



Notes:

7. Diagnostic register = shadow register = shift register.
8. Asynchronous enable mode only.
9. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H ⧫ L) then the output impedance change delay is t_{MS}.

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	**Hex**	**Contents**
0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	Init Byte
8193	2001	Control Byte

Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

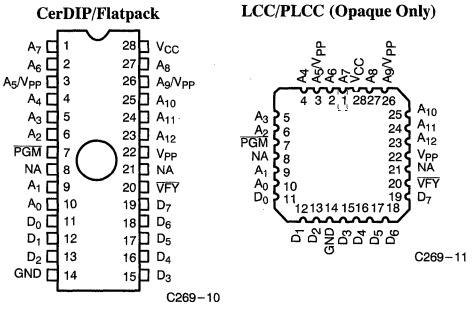


Figure 1. Programming Pinouts

Mode Selection

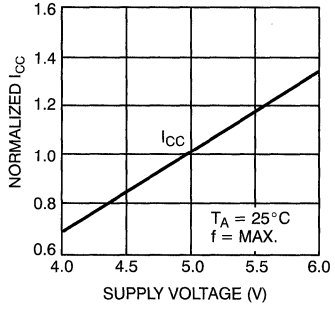
Mode	Read or Output Disable / Other	Pin Function[10]							
	Read or Output Disable	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**	**A_1**
	Other	**A_{12}**	**A_{11}**	**$A_{10} - A_7$**	**A_6**	**A_5**	**$A_4 - A_3$**	**A_2**	**A_1**
Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load SR to PR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load Output to SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Shift SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Synchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Initialization Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Memory		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Verify		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Inhibit		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Synchronous Enable		V_{IHP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{IHP}	A_1
Program Initialize		V_{ILP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	A_1
Program Initial Byte		A_{12}	V_{ILP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	A_1

Mode	Read or Output Disable / Other	Pin Function[10]						
	Read or Output Disable	**A_0**	**MODE**	**CLK**	**SDI**	**SDO**	**$\overline{E}, \overline{I}$**	**$O_7 - O_0$**
	Other	**A_0**	**$\overline{PGM}$**	**CLK**	**NA**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Read		A_0	V_{IL}	V_{IL}/V_{IH}	X	High Z	V_{IL}	$O_7 - O_0$
Load SR to PR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IL}	SDI	V_{IL}	$O_7 - O_0$
Load Output to SR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IH}	SDI	V_{IL}	$O_7 - O_0$
Shift SR		A_0	V_{IH}	V_{IL}/V_{IH}	D_{IN}	SDO	V_{IH}	$O_7 - O_0$
Asynchronous Enable Read		A_0	V_{IL}	V_{IL}	X	High Z	V_{IL}	$O_7 - O_0$
Synchronous Enable Read		A_0	V_{IL}	V_{IL}/V_{IH}	X	High Z	V_{IL}	$O_7 - O_0$
Asynchronous Initialization Read		A_0	V_{IL}	V_{IL}	X	High Z	V_{IL}	$O_7 - O_0$
Program Memory		A_0	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		A_0	V_{IHP}	V_{ILP}	X	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		A_0	V_{IHP}	V_{ILP}	X	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{ILP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize		V_{ILP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initial Byte		V_{IHP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$

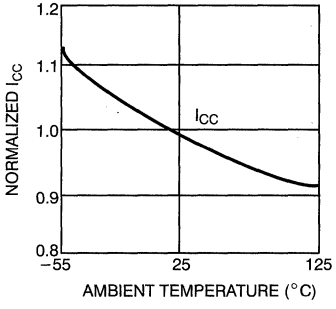
Note:
10. X = "don't care" but not to exceed $V_{CC} \pm 5\%$.

Typical DC and AC Characteristics

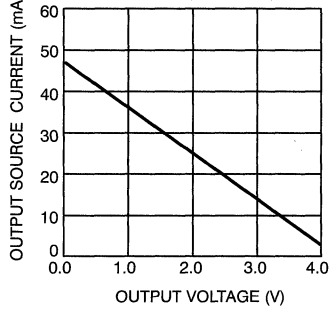
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



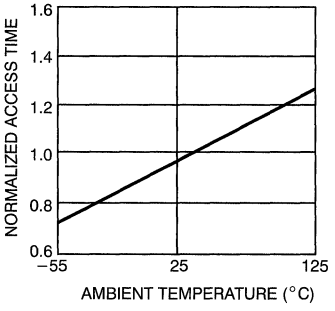
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



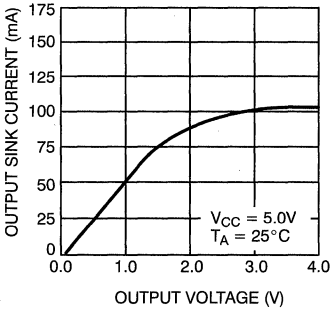
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



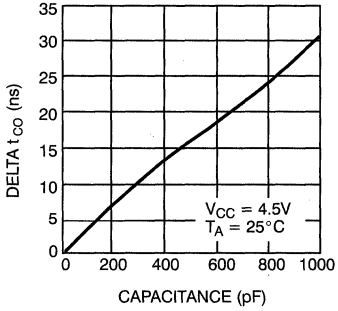
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



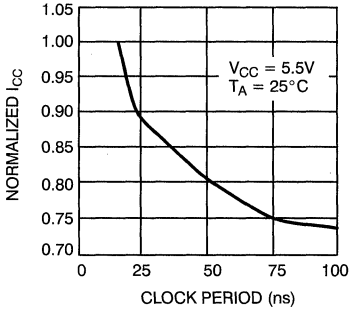
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



Ordering Information[11]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	120	CY7C269–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–15PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C269–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C269–15LMB	L64	28-Square Leadless Chip Carrier	
		CY7C269–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C269–15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
25	140	CY7C269–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–25PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C269–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C269–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C269–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C269–25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	100	CY7C269–40JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–40PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	80	CY7C269–50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C269–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C269–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	120	CY7C269–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C269–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C269–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C269–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:

11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

Diagnostic Mode Switching Characteristics

Parameters	Subgroups
t_{SSDI}	7, 8, 9, 10, 11
t_{HSDI}	7, 8, 9, 10, 11
t_{DSDO}	7, 8, 9, 10, 11
t_{DCL}	7, 8, 9, 10, 11
t_{DCH}	7, 8, 9, 10, 11
t_{HM}	7, 8, 9, 10, 11
t_{MS}	7, 8, 9, 10, 11
t_{SS}	7, 8, 9, 10, 11

Document #: 38−00069−G

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CY7C271
CY7C274

32K x 8 Power-Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 30 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 715 mW (military)**
- **Super low standby power**
  - **— Less than 165 mW when deselected**
- **EPROM technology 100% programmable**
- **Slim 300-mil package (7C271)**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

Functional Description

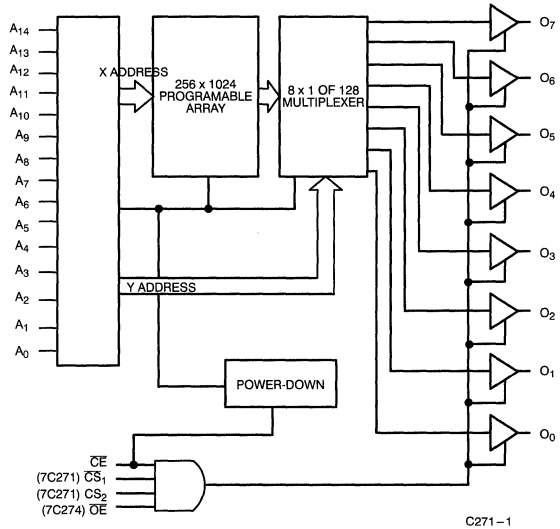
The CY7C271 and CY7C274 are high-performance 32,768-word by 8-bit CMOS PROMs. When disabled ($\overline{CE}$ HIGH), the 7C271/7C274 automatically powers down into a low-power stand-by mode. The CY7C271 is packaged in the 300-mil slim package. The CY7C274 is packaged in the industry standard 600-mil package. Both the 7C271 and 7C274 are available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271 and CY7C274 offer the advantage of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

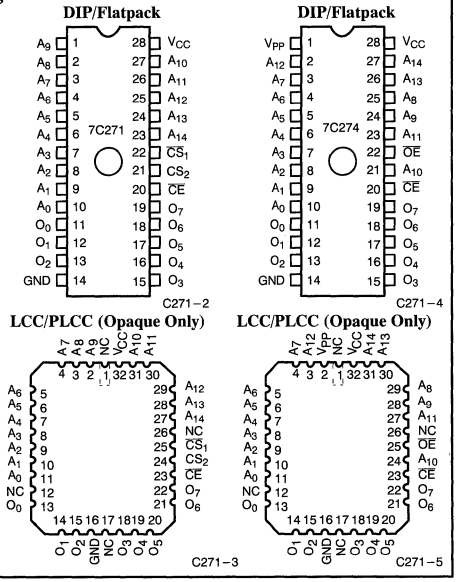
Reading the 7C271 is accomplished by placing active LOW signals on $\overline{CS_1}$ and $\overline{CE}$, and an active HIGH on CS_2. Reading the 7C274 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 – A_{14}) will become available on the output lines (O_0 – O_7).

4

Logic Block Diagram



Pin Configurations



For all new designs, please refer to the CY7C271A or CY27H256. The CY7C271A is a lower power pin-compatible replacement for the CY7C271. The CY27H256 is a lower power pin-compatible replacement for the CY7C274.

Document #: 38–00068–H

PRELIMINARY **CY7C271A**

32K x 8 Power-Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 25 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 275 mW (commercial)**
  - **— 330 mW (military)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100% programmable**
- **Slim 300-mil package**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >4001V static discharge**

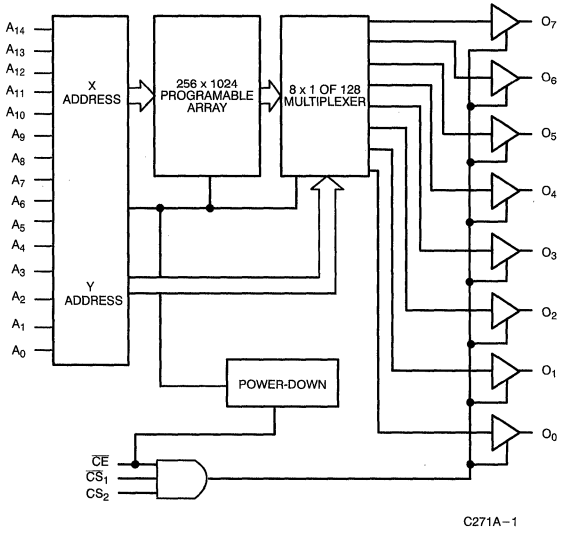
Functional Description

The CY7C271A is a high-performance 32,768-word by 8-bit CMOS PROM. When disabled ($\overline{CE}$ HIGH), the 7C271A automatically powers down into a low-power stand-by mode. The CY7C271A is packaged in the 300-mil slim package and is available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271A offers the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading the 7C271A is accomplished by placing active LOW signals on $\overline{CS_1}$ and $\overline{CE}$, and an active HIGH on CS_2. The contents of the memory location addressed by the address lines (A_0 – A_{14}) will become available on the output lines (O_0 – O_7).

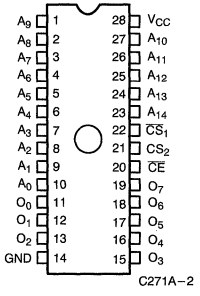
Logic Block Diagram



C271A–1

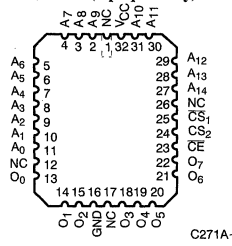
Pin Configurations

DIP/Flatpack



C271A–2

LCC/PLCC (Opaque Only)



C271A–3

Selection Guide

		7C271A–25	7C271A–30	7C271A–35	7C271A–45	7C271A–55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l	75	75	50	50	50
	Military			85	60	60
Standby Current (mA)	Com'l	15	15	15	15	15
	Military			25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >4001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C271A−25 7C271A−30 Min.	7C271A−25 7C271A−30 Max.	7C271A−35 Min.	7C271A−35 Max.	7C271A−45 7C271A−55 Min.	7C271A−45 7C271A−55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC}=Max, VO_{UT}=GND		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=10 MHz	Com'l		75		50		50	mA
			Mil				85		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA
			Mil				25		25	mA

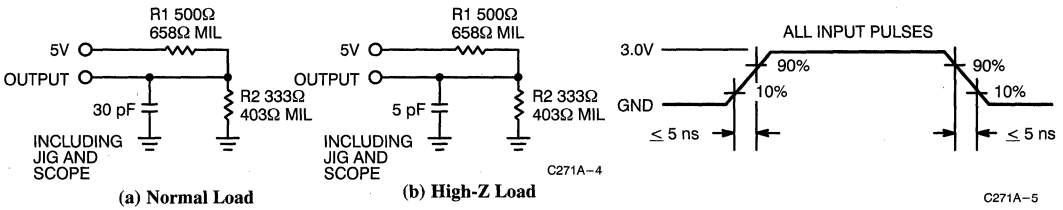
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

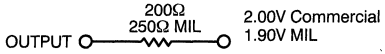
Notes:

1. Contact a Cypress representative for information on industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms



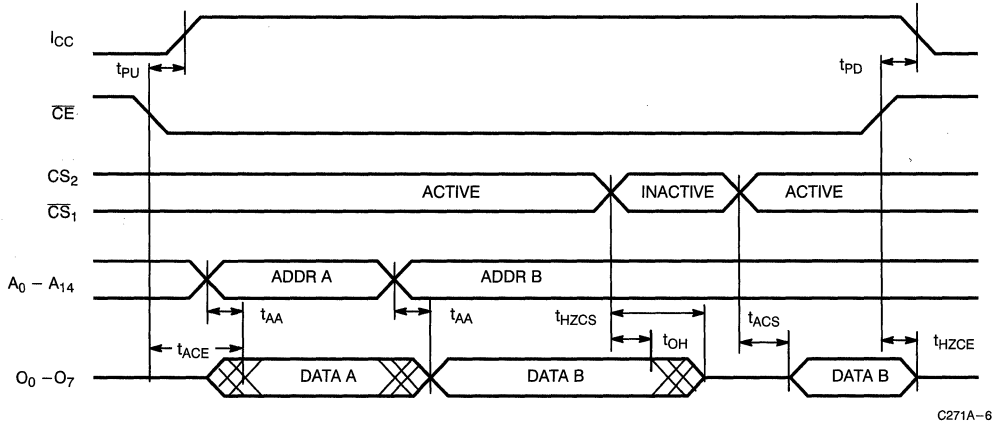
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C271A–25		7C271A–30		7C271A–35		7C271A–45		7C271A–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45		55	ns
t_{ACS}	$\overline{CS_1}/CS_2$ Active to Output Valid		12		15		15		15		20	ns
t_{ACE}	$\overline{CE}$ Active to Output Valid		30		35		35		45		55	ns
t_{HZCS}	$\overline{CS_1}/CS_2$ Inactive to High Z		12		15		15		15		20	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		15		15		15		20	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		40		50	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY7C271A in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C271A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

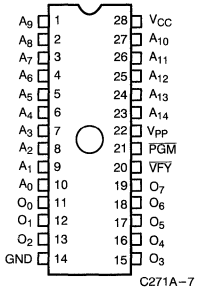
Table 2. Mode Selection

Mode	Pin Function[6]					
	$\overline{CS_1}/V_{PP}$	$CS_2/\overline{PGM}$	$\overline{CE}/\overline{VFY}$	A_0	A_9	Data
Read	V_{IL}	V_{IH}	V_{IL}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IH}	V_{IH}	V_{IL}	A_0	A_9	High Z
Output Disable	V_{IL}	V_{IL}	V_{IL}	A_0	A_9	High Z
Stand-by	X	X	V_{IH}	A_0	A_9	High Z
Program	V_{PP}	V_{ILP}	V_{IHP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	X	X	X
Signature (MFG)	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{HV}[7]	34H
Signature (DEV)	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{HV}[7]	20H

Notes:
6. X can be V_{IL} or V_{IH}.
7. V_{HV}=12±0.5V

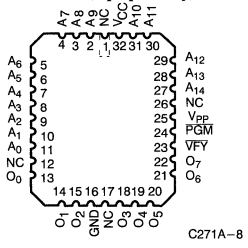
Programming Pinouts

DIP/Flatpack



C271A–7

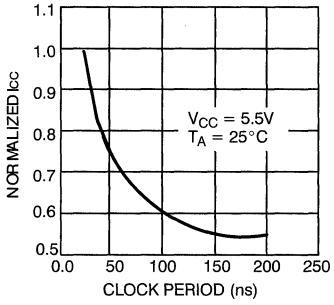
LCC/PLCC (Opaque Only)



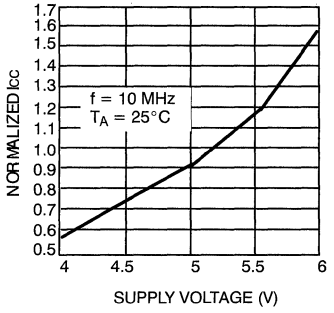
C271A–8

Typical DC and AC Characteristics

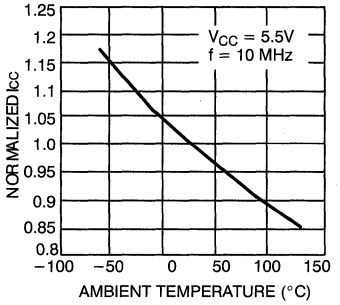
NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



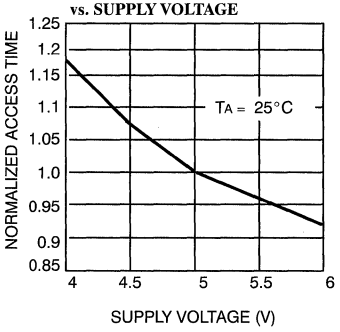
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



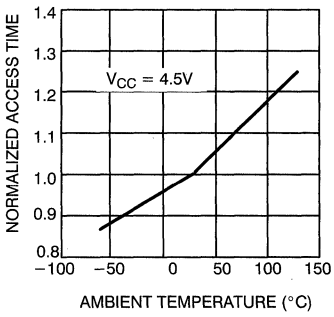
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



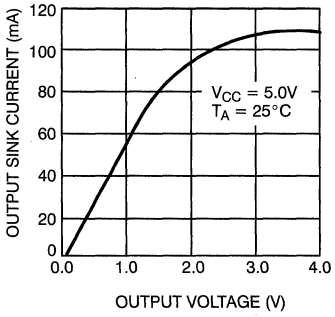
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



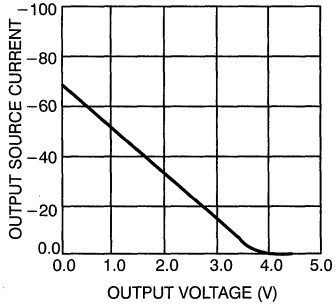
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C271A–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C271A–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271A–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271A–30WC	W22	28-Lead (300-Mil) Windowed CerDIP	
35	CY7C271A–35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271A–35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271A–35WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C271A–35KMB	K74	28-Lead Rectangular Cerpack	
	CY7C271A–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C271A–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271A–35TMB	T74	28-Lead Windowed Cerpack	
	CY7C271A–35WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
45	CY7C271A–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271A–45PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271A–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271A–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C271A–45KMB	K74	28-Lead Rectangular Cerpack	
	CY7C271A–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C271A–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271A–45TMB	T74	28-Lead Windowed Cerpack	
	CY7C271A–45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C271A–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C271A–55PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C271A–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271A–55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C271A–55KMB	K74	28-Lead Rectangular Cerpack	
	CY7C271A–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C271A–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271A–55TMB	T74	28-Lead Windowed Cerpack	
	CY7C271A–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Document #: 38−00424

16K x 16 Reprogrammable PROM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed (for commercial and military)**
  - **— 25-ns access time**
- **16-bit-wide words**
- **Three programmable chip selects**
- **Programmable output enable**
- **44-pin PLCC and 44-pin LCC packages**
- **100% reprogrammable in windowed packages**
- **TTL-compatible I/O**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

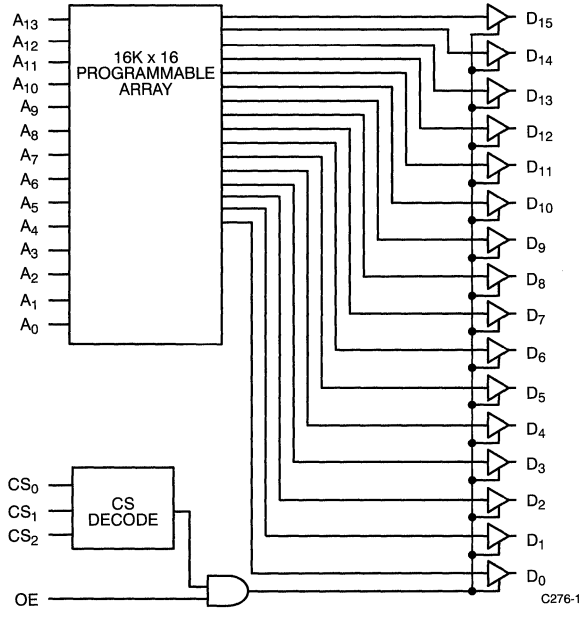
The CY7C276 is a high-performance 16K-word by 16-bit CMOS PROM. It is available in a 44-pin PLCC/CLCC and a 44-pin LCC packages, and is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating gate technology and word-wide programming algorithms.

The CY7C276 allows the user to independently program the polarity of each chip select ($CS_2 - CS_0$). This provides on-chip decoding of up to eight banks of PROM. The polarity of the asynchronous output enable pin (OE) is also programmable.

In order to read the CY7C276, all three chip selects must be active and OE must be asserted. The contents of the memory location addressed by the address lines ($A_{13} - A_0$) will become available on the output lines ($D_{15} - D_0$). The data will remain on the outputs until the address changes or the outputs are disabled.

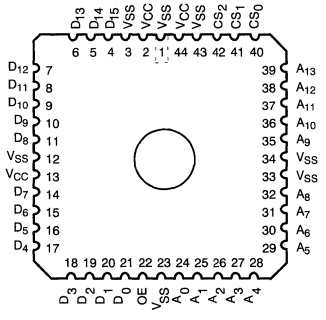
4

Logic Block Diagram



Pin Configuration

LCC/PLCC/CLCC
Top View



Selection Guide

		CY7C276–25	CY7C276–30	CY7C276–35
Maximum Access Time (ns)		25	30	35
Maximum Operating Current (mA)	Commercial	175	175	175
	Military	200	200	200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics[3, 4]

Parameter	Description	Test Conditions		CY7C276−25 CY7C276−30 CY7C276−35 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA (6.0 mA Mil)			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
V_{CD}	Input Clamp Diode Voltage			Note 3		µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[5]		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0.0 mA	Com'l		175	mA
			Military		200	mA

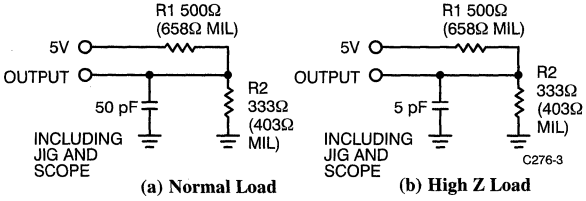
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

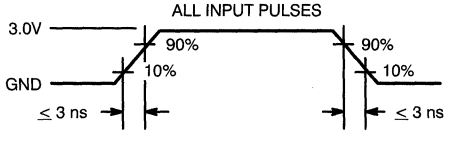
1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature
3. See Introduction to CMOS PROMs in this Data Book for general information on testing.
4. See the last page of this specification for Group A subgroup testing information.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms

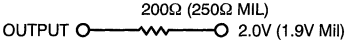


(a) Normal Load

(b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	CY7C276–25		CY7C276–30		CY7C276–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Data Valid		25		30		35	ns
t_{CSOV}	CS Active to Output Valid		13		15		18	ns
t_{CSOZ}	CS Inactive to High Z Output		13		15		18	ns
t_{OEV}	OE Active to Output Valid		11		12		15	ns
t_{OEZ}	OE Inactive to High Z Output		11		12		15	ns

Erasure Characteristics

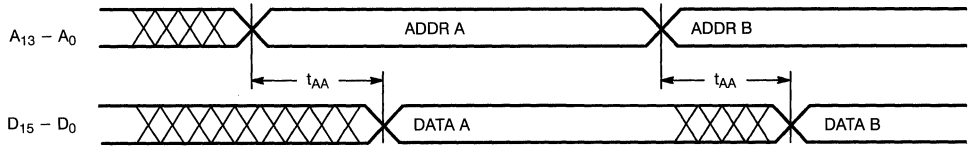
The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C276 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Wavelengths of light less than 4000 Å begin to erase the 7C276 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

4

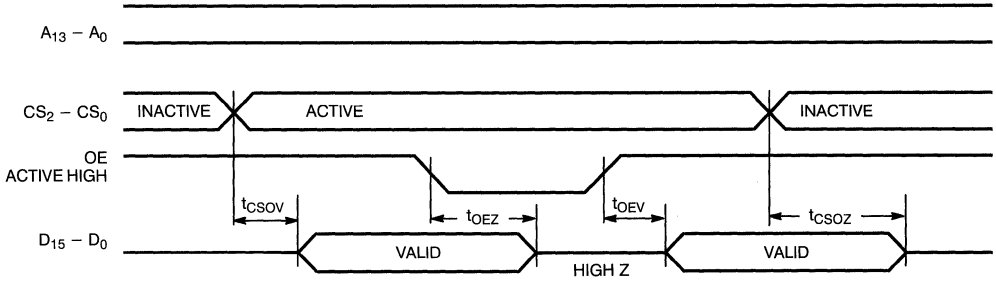
Switching Waveforms

Read Operation Timing Diagram[6]



C276-5

Chip Select and Output Enable Timing Diagrams



C276-6

Notes:
6. $CS_2 - CS_0$, OE assumed active.

Architecture Configuration Bits

The CY7C276 has four user-programmable options in addition to the reprogrammable data array. For detailed programming information contact your local Cypress representative.

The programmable options determine the active polarity for the three chip selects (CS_2 – CS_0) and OE. When these control bits are programmed with a 0 the inputs are active LOW. When these control bits are programmed with a 1 the inputs are active HIGH.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Control Word for Architecture Configuration

Control Option	Control Word		Function
	Bit	Programmed Level	
OE	D_0	0=Default 1=Programmed	OE Active LOW OE Active HIGH
CS_0	D_{12}	0=Default 1=Programmed	CS_0 Active LOW CS_0 Active HIGH
CS_1	D_{13}	0=Default 1=Programmed	CS_1 Active LOW CS_1 Active HIGH
CS_2	D_{14}	0=Default 1=Programmed	CS_2 Active LOW CS_2 Active HIGH

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
.	.
3FFF	Data
4000	Control Word

Control Word (4000H)

D_{15} D_0

X CS_2 CS_1 CS_0 X X X X X X X X 1 X X OE

Table 2. Program Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	D_0 – D_{15}
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	High Z
Program Enable	V_{PP}	V_{ILP}	V_{IHP}	Data
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	Data

Table 3. Configuration Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_2	D_0 – D_{15}
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Program Control Word	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	Control Word
Verify Control Word	V_{PP}	V_{IHP}	V_{ILP}	V_{PP}	Control Word

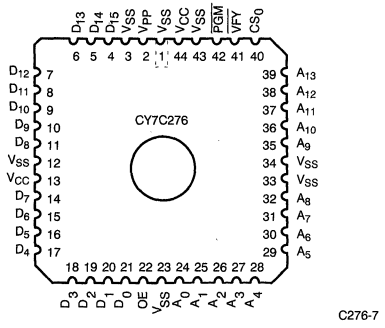
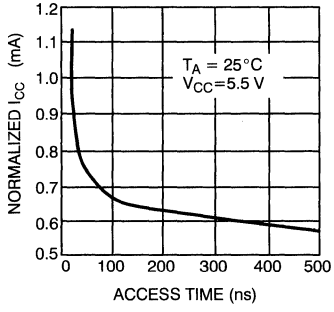


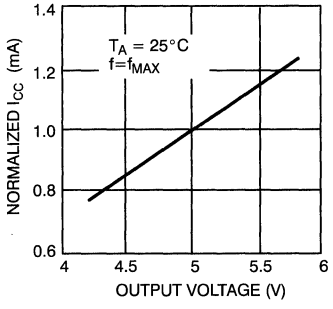
Figure 1. Programming Pinout

Typical DC and AC Characteristics

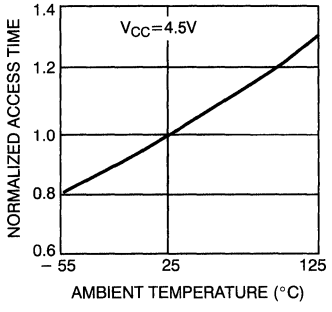
NORMALIZED I_{CC} vs. t_{CKA} CYCLE



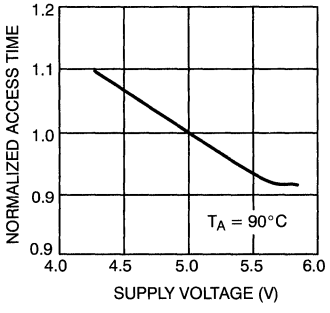
NORMALIZED I_{CC} vs. OUTPUT VOLTAGE



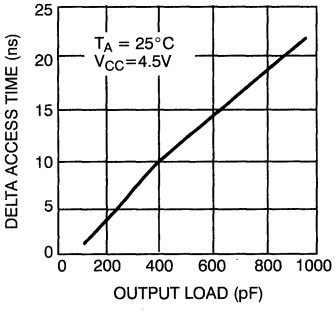
NORMALIZED t_{CKA} vs. TEMPERATURE



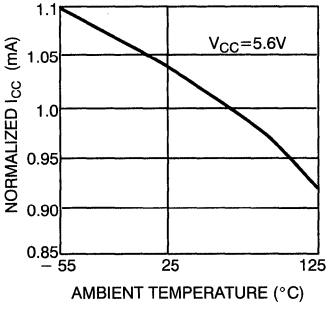
NORMALIZED t_{CKA} vs. SUPPLY VOLTAGE



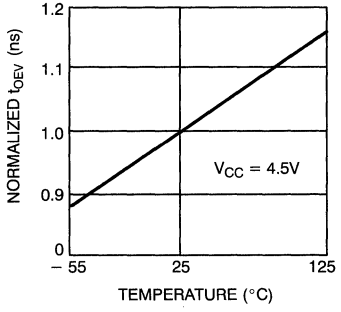
t_{CKA} CHANGE vs. OUTPUT LOADING



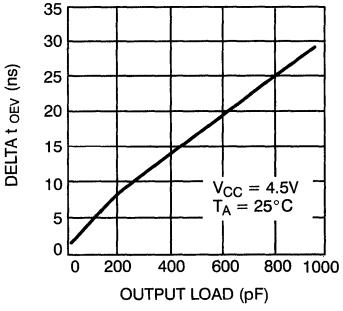
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



NORMALIZED t_{OEV} vs. TEMPERATURE



t_{OEV} CHANGE vs. OUTPUT LOADING



Ordering Information[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C276–25HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276–25JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276–25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276–25QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
30	CY7C276–30HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276–30JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276–30QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
35	CY7C276–35HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276–35JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276–35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276–35QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

Note:

7. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{CSOV}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11

Document #: 38–00183–D

CY7C277

32K x 8 Reprogrammable Registered PROM

Features

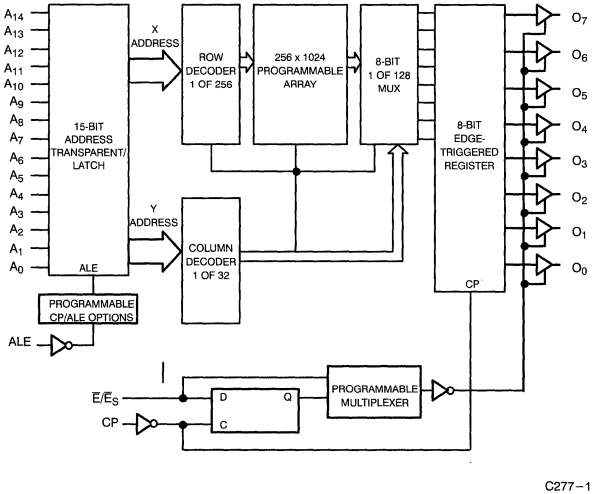
- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 30-ns address set-up**
  - **— 15-ns clock to output**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 715 mW (military)**
- **Programmable address latch enable input**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered output registers**
- **EPROM technology, 100% programmable**
- **Slim 300-mil, 28-pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C277 is a high-performance 32K word by 8-bit CMOS PROMs. It is packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

4

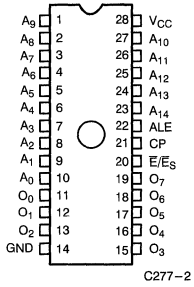
Logic Block Diagram



C277–1

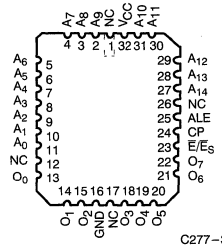
Pin Configurations

DIP/Flatpack
Top View



C277–2

LCC/PLCC (Opaque Only)
Top View



C277–3

Selection Guides

		7C277–30	7C277–40	7C277–50
Minimum Address Set-Up Time (ns)		30	40	50
Maximum Clock to Output (ns)		15	20	25
Maximum Operating Current (mA)	Com'l	120	120	120
	Mil		130	130

Functional Description (continued)

The CY7C277 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8-bit edge triggered output register. The $\overline{E}/\overline{E}_S$ input provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin operates as an asynchronous output enable. If the synchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin is sampled on the rising edge of CP to enable and disable the outputs. The 7C277 also provides a programmable bit to enable the Address Latch input. If this bit is not programmed, the device will ignore the ALE pin and the address will enter the device asynchronously. If the ALE function is selected, the address enters the PROM while the ALE pin is active, and is captured when ALE is deasserted. The user may define the polarity of the ALE signal, with the default being active HIGH.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C277−30 Min.	7C277−30 Max.	7C277−40, 50 Min.	7C277−40, 50 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	µA
V_{CD}	Input Clamp Diode Voltage			Note 4				
I_{OZ}	Output Leakage Current	0 ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, I_{OUT} = 0 mA	Commercial		120		120	mA
			Military				130	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

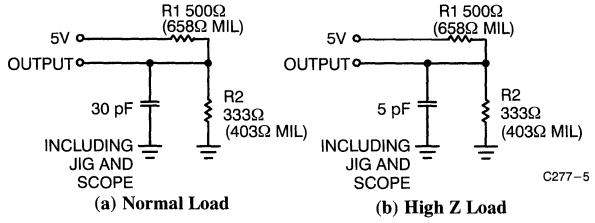
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

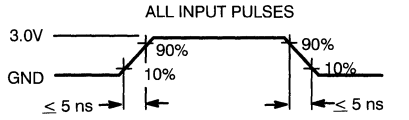
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

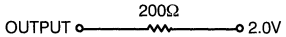
AC Test Loads and Waveforms[4]



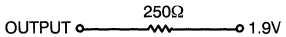
(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

CY7C277 Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C277-30		7C277-40		7C277-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AL}	Address Set-Up to ALE Inactive	5		10		10		ns
t_{LA}	Address Hold from ALE Inactive	10		10		15		ns
t_{LL}	ALE Pulse Width	10		10		15		ns
t_{SA}	Address Set-Up to Clock HIGH	30		40		50		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		10		10		ns
t_{CO}	Clock HIGH to Output Valid		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{LZC}[7]	Output Valid from Clock HIGH		15		20		30	ns
t_{HZC}	Output High Z from Clock HIGH		15		20		30	ns
t_{LZE}[8]	Output Valid from $\overline{E}$ LOW		15		20		30	ns
t_{HZE}[8]	Output High Z from $\overline{E}$ HIGH		15		20		30	ns

Notes:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.
8. Applies only when the asynchronous ($\overline{E}$) function is used.

Architecture Configuration Bits

Architecture Bit	Architecture Verify $D_7 - D_0$		Function
ALE	D_1	0 = DEFAULT	Input Transparent
		1 = PGMED	Input Latched
ALEP	D_2	0 = DEFAULT	ALE = Active HIGH
		1 = PGMED	ALE = Active LOW
$\overline{E}/\overline{E}_S$	D_0	0 = DEFAULT	Asynchronous Output Enable ($\overline{E}$)
		1 = PGMED	Synchronous Output Enable ($\overline{E}_S$)

Bit Map

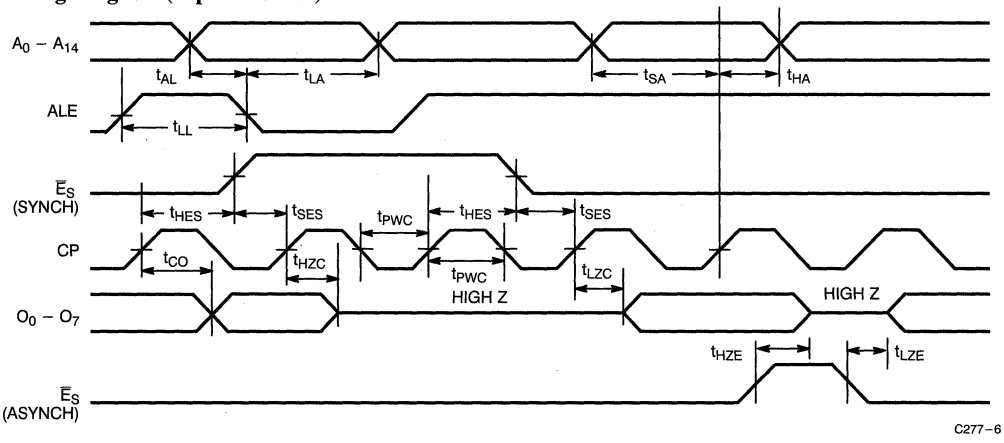
Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
.	.
7FFF	Data
8000	Control Byte

Architecture Byte (8000)

D_7 D_0

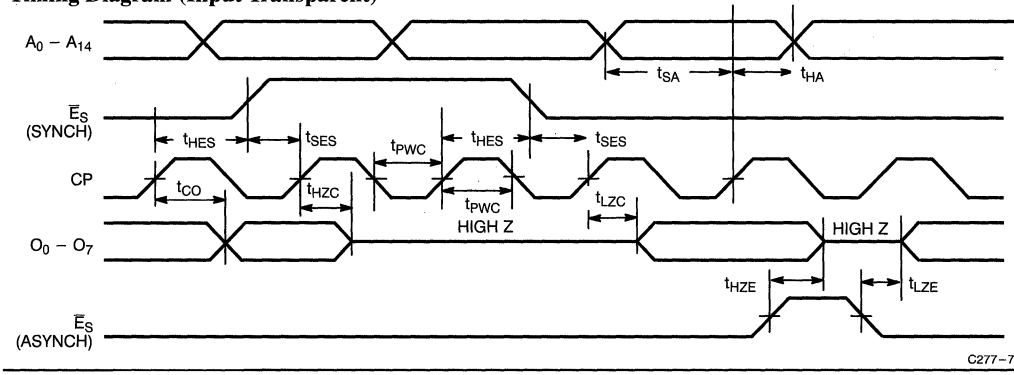
C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Timing Diagram (Input Latched)[9]



C277-6

Timing Diagram (Input Transparent)



C277-7

Note:

9. ALE is shown with positive polarity.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[10]				
	Read or Output Disable	**$A_{14} - A_0$**	**$\overline{E}, \overline{E}_S$**	**CP**	**ALE**	**$O_7 - O_0$**
	Other	**$A_{14} - A_0$**	**$\overline{VFY}$**	**$\overline{PGM}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{14} - A_0$	V_{IL}	V_{IH}	V_{IL}	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$

Note:
10. X = "don't care" but not to exceed V_{CC} ±5%.

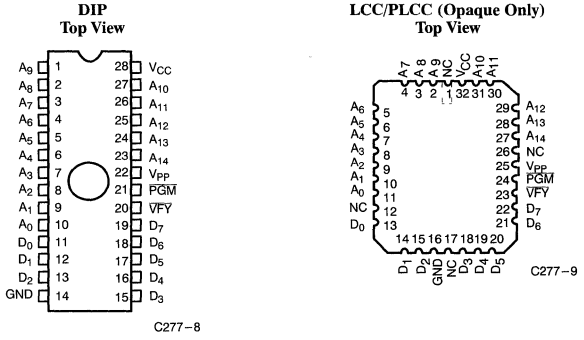
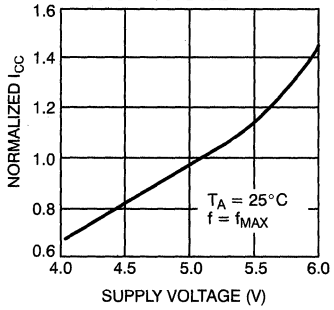


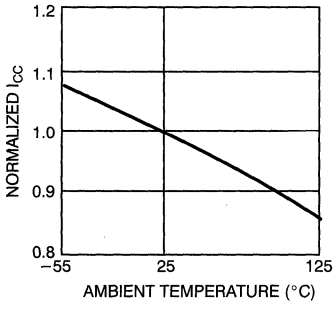
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

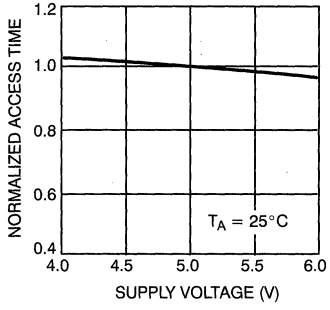
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



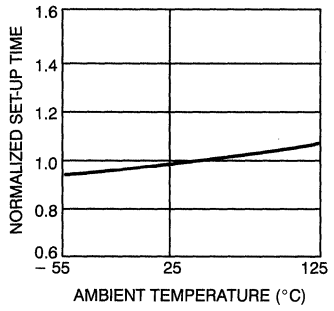
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



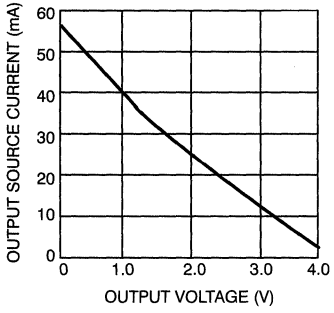
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



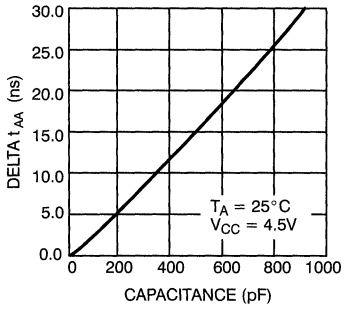
NORMALIZED SET-UP TIME vs. TEMPERATURE



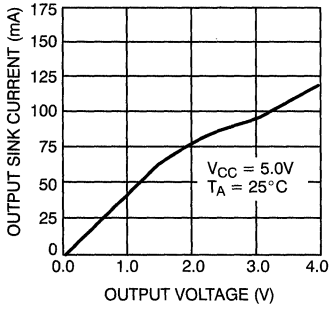
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C277–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C277–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C277–30WC	W22	28-Lead (300-Mil) Windowed CerDIP	
40	CY7C277–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C277–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C277–40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C277–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C277–40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C277–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C277–40QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C277–40TMB	T74	28-Lead Windowed Cerpack	
	CY7C277–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
50	CY7C277–50JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C277–50PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C277–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C277–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C277–50KMB	K74	28-Lead Rectangular Cerpack	
	CY7C277–50LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C277–50QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C277–50TMB	T74	28-Lead Windowed Cerpack	
	CY7C277–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

Document #: 38–00085–E

CY7C281A
CY7C282A

1K x 8 PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns (commercial)**
  - **— 30 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil DIP or 28-pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

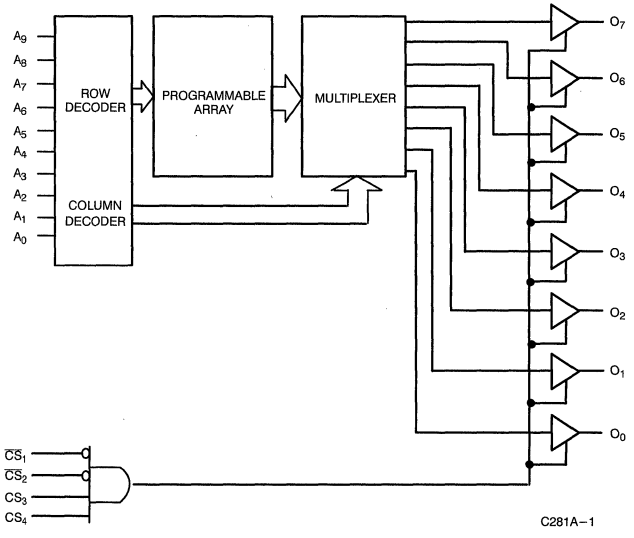
Functional Description

The CY7C281A and CY7C282A are high-performance 1024-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil and 600-mil-wide packages respectively. The CY7C281A is also available in a 28-pin leadless chip carrier. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C281A and CY7C282A are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$ and $\overline{CS}_2$, and active HIGH signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines (A_0 – A_9) will become available on the output lines (O_0 – O_7).

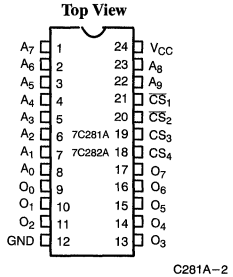
Logic Block Diagram



C281A–1

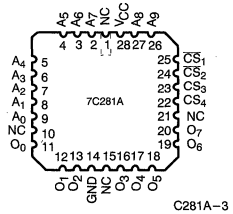
Pin Configurations

DIP
Top View



C281A–2

LCC/PLCC
Top View



C281A–3

Selection Guide

		7C281A–25 7C282A–25	7C281A–30 7C282A–30	7C281A–45 7C282A–45
Maximum Access Time (ns)		25	30	45
Maximum Operating Current (mA)	Commercial	100	100	90
	Military		120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	−40°C to +85°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C281A−25 7C282A−25 Min.	7C281A−25 7C282A−25 Max.	7C281A−30 7C282A−30 Min.	7C281A−30 7C282A−30 Max.	7C281A−45 7C282A−45 Min.	7C281A−45 7C282A−45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	−20	− 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		100		90	mA
			Military				120		120	
V_{PP}	Program Voltage			12	13	12	13	12	13	V
V_{IHP}	Program HIGH Voltage			3.0		3.0		3.0		V
V_{ILP}	Program LOW Voltage				0.4		0.4		0.4	V
I_{PP}	Program Supply Current				50		50		50	mA

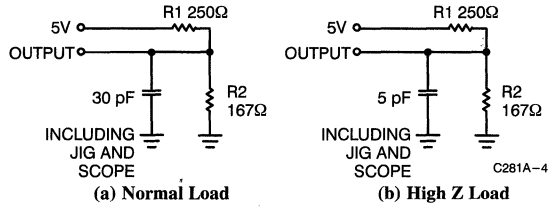
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

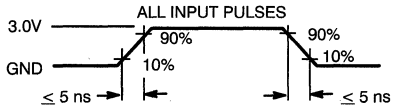
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

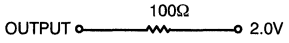
AC Test Loads and Waveforms[4]



(a) Normal Load (b) High Z Load



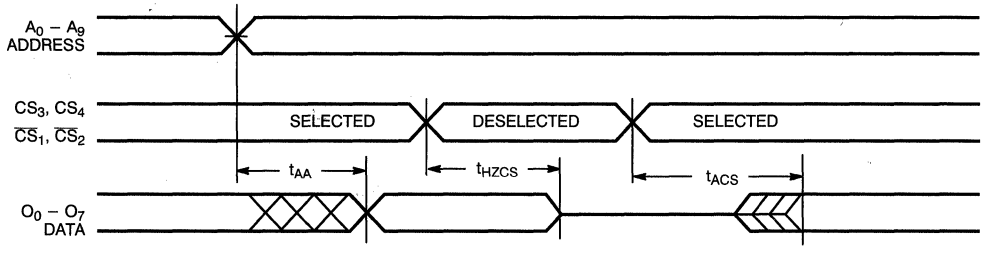
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,4]

Parameter	Description	7C281A–25 7C282A–25		7C281A–30 7C282A–30		7C281A–45 7C282A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		15		20		25	ns

Switching Waveforms



Programming Information

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[6]					
	Read or Output Disable	$A_9 - A_0$	CS_4	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	$O_7 - O_0$
	Other	$A_9 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{CS}_1$	$D_7 - D_0$
Read		$A_9 - A_0$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	$O_7 - O_0$
Output Disable		$A_9 - A_0$	X	X	V_{IH}	X	High Z
Output Disable		$A_9 - A_0$	X	V_{IL}	X	X	High Z
Output Disable		$A_9 - A_0$	V_{IL}	X	X	X	High Z
Output Disable		$A_9 - A_0$	X	X	X	V_{IH}	High Z
Program		$A_9 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Program Verify		$A_9 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	$O_7 - O_0$
Program Inhibit		$A_9 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		$A_9 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	$D_7 - D_0$
Blank Check		$A_9 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Zeros

Note:
6. X = "don't care" but not to exceed V_{CC} ±5%.

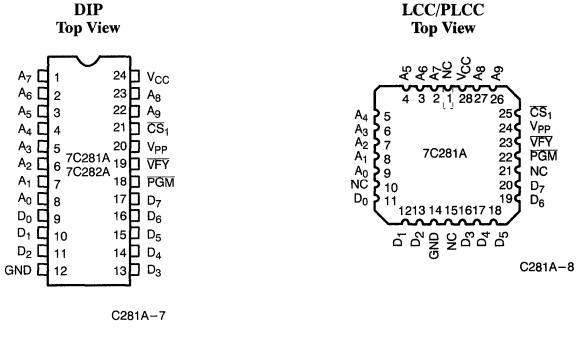
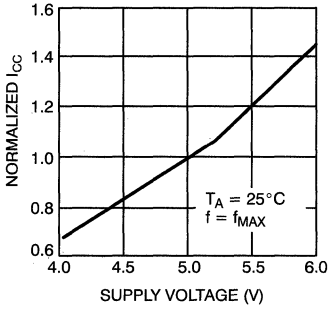


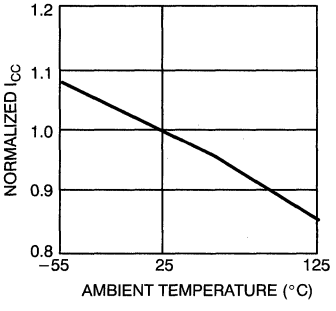
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

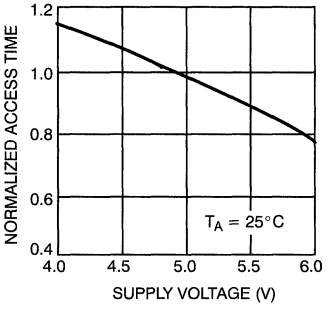
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



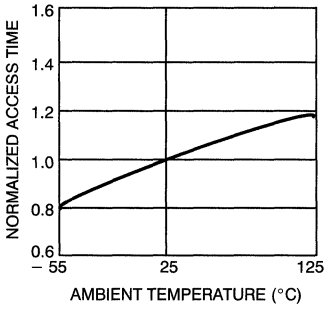
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



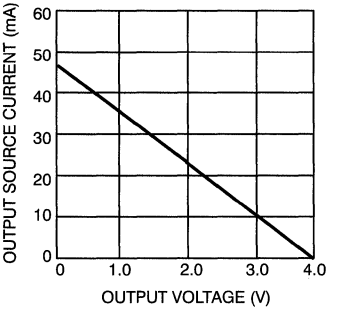
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



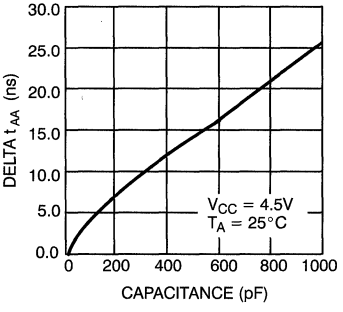
NORMALIZED ACCESS TIME vs. TEMPERATURE



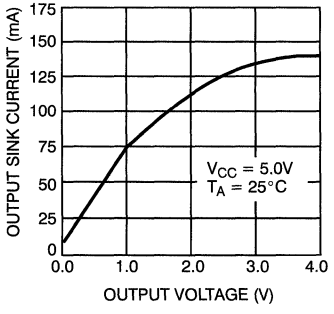
OUTPUT SOURCE CURRENT vs. VOLTAGE



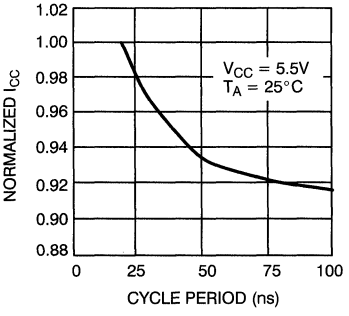
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



I_{CC} vs. CYCLE PERIOD



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C281A–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281A–25PC	P13	24-Lead (300-Mil) Molded DIP	
30	CY7C281A–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281A–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281A–30PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C281A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
45	CY7C281A–45DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7C281A–45JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C281A–45PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C281A–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C281A–45KMB	K73	24-Lead Rectangular Cerpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C282A–25PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
30	CY7C282A–30PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C282A–30DMB	D12	24-Lead (600-Mil) CerDIP	Military
45	CY7C282A–45PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	CY7C282A–45DMB	D12	24-Lead (600-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11

Document #: 38–00227–C

CY7C287

64K x 8 Reprogrammable Registered PROM

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - t_{SA} = 45 ns
  - t_{CO} = 15 ns
- Low power
  - 120 mA
- On-chip, edge-triggered output registers
- Programmable synchronous or asynchronous output enable
- EPROM technology, 100% programmable
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Slim 300-mil package
- Capable of withstanding >2001V static discharge

Functional Description

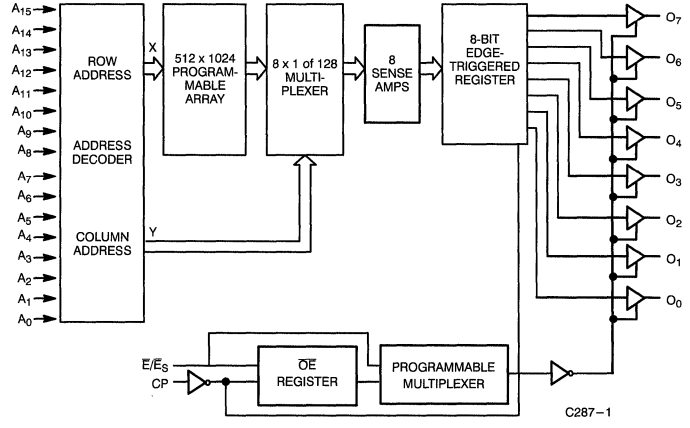
The CY7C287 is a high-performance 64K x 8 CMOS PROM. The CY7C287 is equipped with an output register and an output enable that can be programmed to be synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$). It is available in a 28-pin, 300-mil package. The address set-up time is 45 ns and the time from clock HIGH to output valid is 15 ns.

The CY7C287 is available in a cerDIP package equipped with an erasure window to provide reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

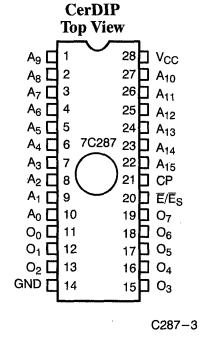
The CY7C287 offers the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested with each cell being programmed, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

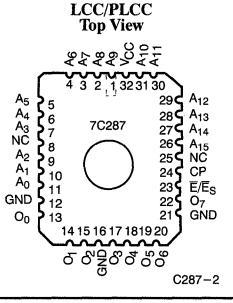
Reading the CY7C287 is accomplished by placing an active LOW signal on $\overline{E}/\overline{E}_S$. The contents of the memory location addressed by the address lines (A_0 – A_{15}) will become available on the output lines (O_0 – O_7) on the next rising of CP.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C287–45	7C287–55	7C287–65
Maximum Set-Up Time (ns)		45	55	65
Maximum Clock to Output (ns)		15	20	25
Maximum Operating Current (mA)	Com'l	120	120	120
	Mil		150	150

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C287–45 Min.	7C287–45 Max.	7C287–55 Min.	7C287–55 Max.	7C287–65 Min.	7C287–65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil				0.4		0.4	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for Inputs			0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4						
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[5]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		120	mA
			Mil				150		150	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

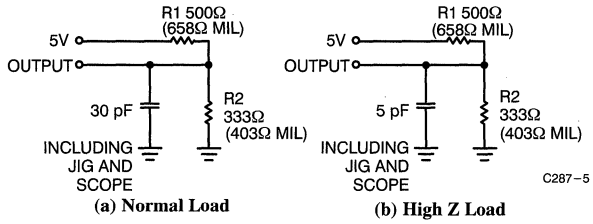
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs for general information on testing.
5. Short circuit test should not exceed 30 seconds.

AC Test Loads and Waveform[4]



(a) Normal Load (b) High Z Load

Equivalent to: THÉVENIN EQUIVALENT

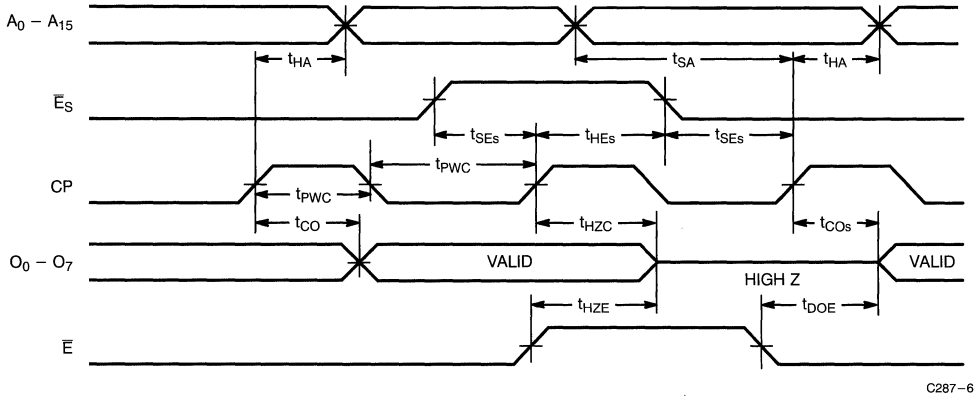
Commercial Military

Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C287–45		7C287–55		7C287–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	45		55		65		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Output Valid		15		20		25	ns
t_{HZE}	Output High Z from $\overline{E}$		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		25		ns
t_{SEs}[6]	$\overline{E}_S$ Set-Up to Clock HIGH	12		15		18		ns
t_{HEs}[6]	$\overline{E}_S$ Hold from Clock HIGH	5		8		10		ns
t_{HZC}[6]	Output High Z from CLK/$\overline{E}_S$		20		25		30	ns
t_{COs}[6]	Output Valid from CLK/$\overline{E}_S$		20		25		30	ns

Note:
6. Parameters with synchronous $\overline{E}_S$ option.

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Å begin to erase the CY7C287 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C287 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

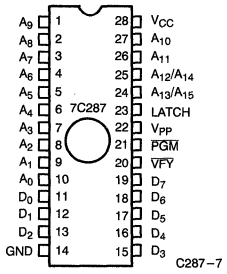
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C287 Mode Selection

	Pin Function[7]				
Mode: Read or Output Disable	**CP**	**A_{14}**	**$\overline{E}$, $\overline{E}_S$**	**A_{15}**	**$O_7 - O_0$**
Synchronous Read	V_{IL}/V_{IH}	A_{14}	V_{IL}	A_{15}	$O_7 - O_0$
Output Disable – Asynchronous	X	A_{14}	V_{IH}	A_{15}	High Z
Output Disable – Synchronous	V_{IL}/V_{IH}	A_{14}	V_{IH}	A_{15}	High Z
Mode: Other	**$\overline{PGM}$**	**LATCH**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Program	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Blank Check	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	Zeros

Note:
7. X = "don't care" but not to exceed V_{CC} ±5%. X can be V_{IL} ir V_{IH}.

DIP



LCC

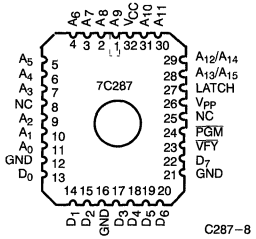


Figure 1. Programming Pinouts

Architecture Configuration Bits

Architecture Bit	Device	Architecture Verify D_0		Function
$\overline{E}/\overline{E}_S$	7C287	D_0	0 = Erased	Asynchronous Output Enable (Pin 20 = $\overline{E}$)
			1 = PGMED	Synchronous Output Enable (Pin 20 = $\overline{E}_S$)

Bit Map

Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
FFFF	Data
10000	Control Byte

Architecture Byte (10000H)

D_7 D_0

C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C287–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C287–45PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C287–45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C287–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C287–55PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C287–55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C287–55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C287–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C287–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C287–55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
65	CY7C287–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C287–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C287–65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C287–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C287–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C287–65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C287–65WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
t_{PWC}	7, 8, 9, 10, 11

Document #: 38–00363

CY7C291A
CY7C292A/CY7C293A

2K x 8 Reprogrammable PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 660 mW (commercial and military)**
- **Low standby power**
  - **— 220 mW (commercial and military)**
- **EPROM technology 100% programmable**
- **Slim 300-mil or standard 600-mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

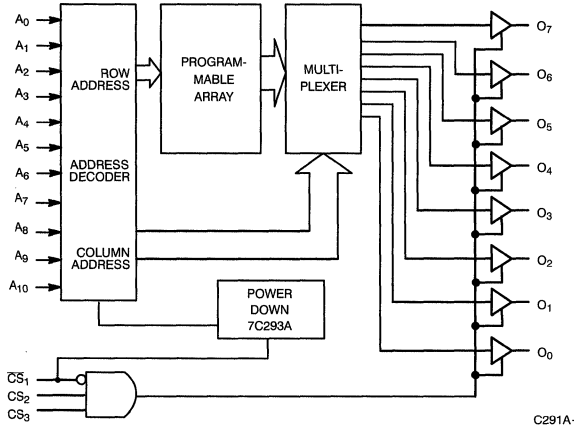
Functional Description

The CY7C291A, CY7C292A, and CY7C293A are high-performance 2K-word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil (7C291A, 7C293A) and 600-mil wide plastic and hermetic DIP packages (7C292A). The CY7C293A has an automatic power down feature which reduces the power consumption by over 70% when deselected. The 300-mil ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C291A, CY7C292A, and CY7C293A are plug-in replacements for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

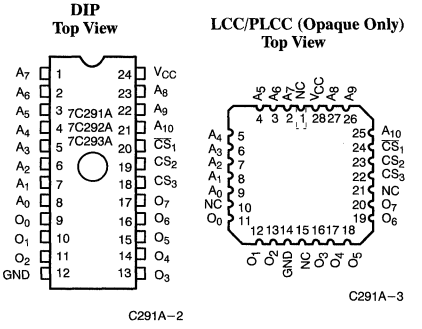
A read is accomplished by placing an active LOW signal on $\overline{CS_1}$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address line (A_0 – A_{10}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram



C291A–1

Pin Configurations



C291A–2

C291A–3

Window available on 7C291A and 7C293A only.

Selection Guide

			7C291A–20 7C292A–20 7C293A–20	7C291A–25 7C292A–25 7C293A–25 7C291AL–25 7C292AL–25 7C293AL–25	7C291A–35 7C292A–35 7C293A–35 7C291AL–35 7C292AL–35 7C293AL–35	7C291A–50 7C292A–50 7C293A–50 7C291AL–50 7C292AL–50 7C293AL–50
Maximum Access Time (ns)			20	25	35	50
Maximum Operating Current (mA)	Standard	Commercial	120	90	90	90
		Military		120	90	90
	L	Commercial		60	60	60
Standby Current (mA) 7C293A Only		Commercial	40	30	30	30
		Military		40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ±10%
Industrial[1]	−40°C to + 85°C	5V ±10%
Military[2]	−55°C to + 125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C291A−20 7C292A−20 7C293A−20 Min.	Max.	7C291A−25 7C292A−25 7C293A−25 Min.	Max.	7C291AL−25 7C292AL−25 7C293AL−25 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4						
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		90		60	mA
			Mil				120			
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}	Com'l		40		30		30	mA
			Mil				40			
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

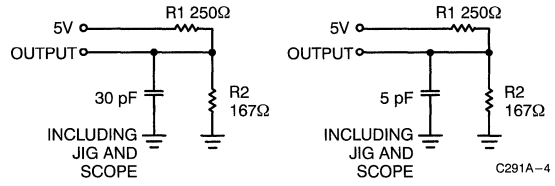
Electrical Characteristics Over the Operating Range[3, 4] (continued)

Parameter	Description	Test Conditions		7C291AL–35, 50 7C292AL–35, 50 7C293AL–35, 50		7C291A–35, 50 7C292A–35, 50 7C293A–35, 50		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT}=0 mA	Commercial		60		90	mA
			Military				90	
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}	Commercial		30		30	mA
			Military				40	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

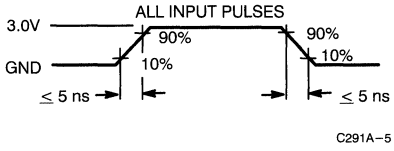
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

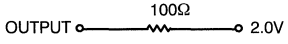
AC Test Loads and Waveforms[4]

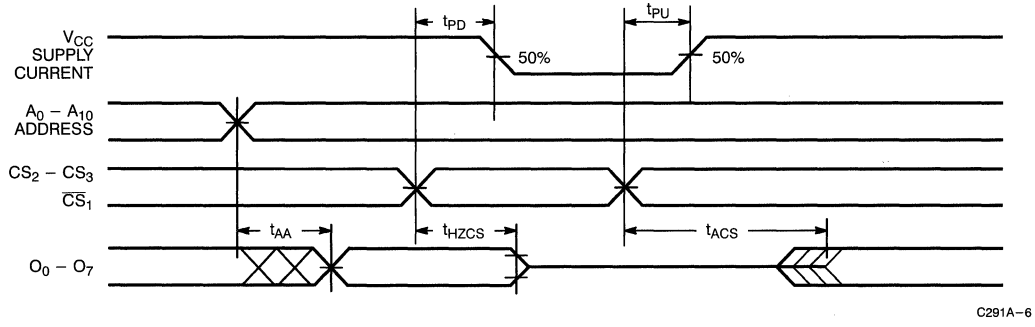


(a) Normal Load (b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C291A–20 7C292A–20 7C293A–20		7C291A–25 7C292A–25 7C293A–25 7C291AL–25 7C292AL–25 7C293AL–25		7C291A–35 7C292A–35 7C293A–35 7C291AL–35 7C292AL–35 7C293AL–35		7C291A–50 7C292A–50 7C293A–50 7C291AL–50 7C292AL–50 7C293AL–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		50	ns
t_{HZCS1}	Chip Select Inactive to High Z		15		15		20		20	ns
t_{ACS1}	Chip Select Active to Output Valid		15		15		20		20	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C293A $\overline{CS}_1$ Only)[6]		22		27		35		45	ns
t_{ACS2}	Chip Select Active to Output Valid (7C293A $\overline{CS}_1$ Only)[6]		22		27		35		45	ns
t_{PU}	Chip Select Active to Power-Up (7C293A $\overline{CS}_1$ Only)	0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down (7C293A $\overline{CS}_1$ Only)		22		27		35		45	ns

Notes:
6. t_{HZCS2} and t_{ACS2} refer to 7C293A $\overline{CS}_1$ only.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes.

These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[7]				
	Read or Output Disable	**$A_{10} - A_0$**	**CS_3**	**CS_2**	**$\overline{CS}_1$**	**$O_7 - O_0$**
	Other	**$A_{10} - A_0$**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{10} - A_0$	V_{IH}	V_{IH}	V_{IL}	$O_7 - O_0$
Output Disable[8]		$A_{10} - A_0$	X	X	V_{IH}	High Z
Output Disable		$A_{10} - A_0$	X	V_{IL}	X	High Z
Output Disable		$A_{10} - A_0$	V_{IL}	X	X	High Z
Program		$A_{10} - A_0$	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{10} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{10} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		$A_{10} - A_0$	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Blank Check Zeros		$A_{10} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Notes:

7. X = "don't care" but not to exceed V_{CC} +5%.
8. The power-down mode for the CY7C293A is activated by deselecting $\overline{CS}_1$.

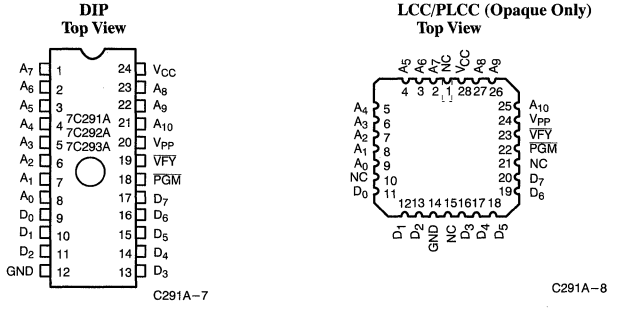
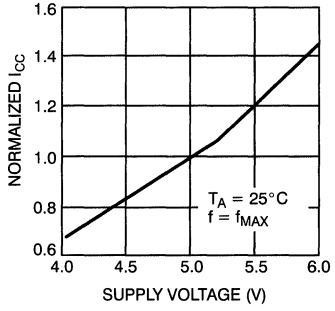


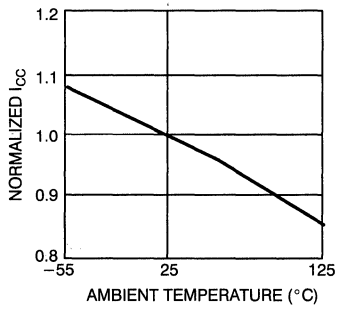
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

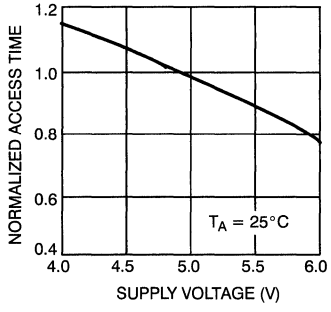
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



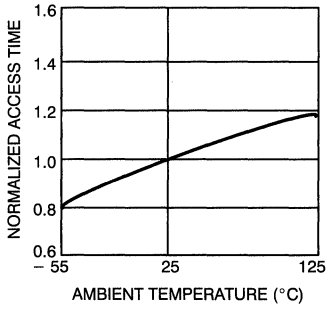
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



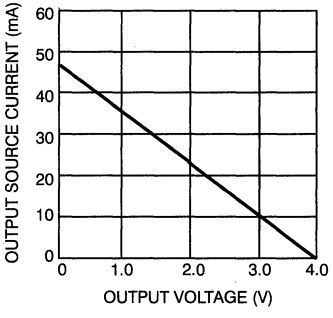
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



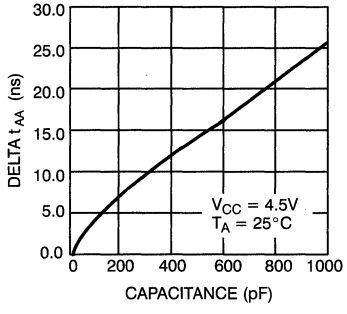
NORMALIZED ACCESS TIME vs. TEMPERATURE



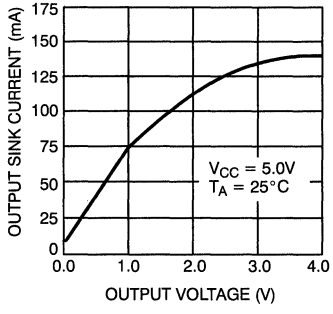
OUTPUT SOURCE CURRENT vs. VOLTAGE



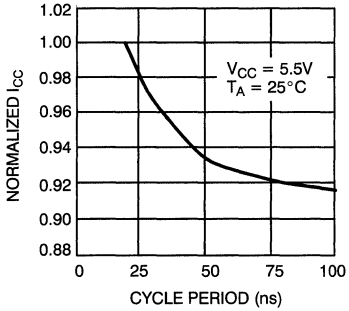
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



I_{CC} vs. CYCLE PERIOD



Ordering Information[9]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C291A–20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291A–20PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–20SC	S13	24-Lead Molded SOIC	
		CY7C291A–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	60	CY7C291AL–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C291A–25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–25SC	S13	24-Lead Molded SOIC	
		CY7C291A–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	CY7C291A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–25TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	120	CY7C291A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–30LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–30QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–30TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	60	CY7C291AL–35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL–35PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–35SC	S13	24-Lead Molded SOIC	Commercial
		CY7C291A–35PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	CY7C291A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–35LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–35TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
50	60	CY7C291AL–50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL–50PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–50SC	S13	24-Lead Molded SOIC	Commercial
		CY7C291A–50PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A–50DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C291A–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C291A–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C291A–50TMB	T73	24-Lead Windowed Cerpack	
		CY7C291A–50WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:
9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[9] (continued)

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C292A–20DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–20PC	P11	24-Lead (600-Mil) Molded DIP	
25	120	CY7C292A–25DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–25PC	P11	24-Lead (600-Mil) Molded DIP	
		CY7C292A–25DMB	D12	24-Lead (600-Mil) CerDIP	Military
30	120	CY7C292A–30DMB	D12	24-Lead (600-Mil) CerDIP	Military
35	60	CY7C292AL–35PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	90	CY7C292A–35DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–35PC	P11	24-Lead (600-Mil) Molded DIP	
	120	CY7C292A–35DMB	D12	24-Lead (600-Mil) CerDIP	Military
50	60	CY7C292AL–50PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
	90	CY7C292A–50DC	D12	24-Lead (600-Mil) CerDIP	Commercial
		CY7C292A–50PC	P11	24-Lead (600-Mil) Molded DIP	
	120	CY7C292A–50DMB	D12	24-Lead (600-Mil) CerDIP	Military

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C293A–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	120	CY7C293A–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
		CY7C293A–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	120	CY7C293A–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–30LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–30QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	60	CY7C293AL–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293AL–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–35LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
50	60	CY7C293AL–50PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293AL–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–50PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C293A–50WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C293A–50DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C293A–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C293A–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C293A–50WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[10]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[11]	7, 8, 9, 10, 11
t_{ACS2}[10]	7, 8, 9, 10, 11

Notes:
10. 7C293A only.
11. 7C291A and 7C292A only.

Document #: 38−00075−G

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962−87650	01KX	CY7C291−50TMB
5962−87650	01LX	CY7C291−50WMB
5962−87650	013X	CY7C291−50QMB
5962−87650	03KX	CY7C291−35TMB
5962−87650	03LX	CY7C291−35WMB
5962−87650	033X	CY7C291−35QMB
5962−88680	01LX	CY7C293A−50WMB
5962−88680	01KX	CY7C293A−50TMB
5962−88680	013X	CY7C293A−50QMB
5962−88680	02LX	CY7C293A−35WMB
5962−88680	02KX	CY7C293A−35TMB
5962−88680	023X	CY7C293A−35QMB
5962−88680	03LX	CY7C293A−30WMB
5962−88680	03KX	CY7C293A−30TMB
5962−88680	033X	CY7C293A−30QMB
5962−88680	04LX	CY7C293A−25WMB
5962−88680	04KX	CY7C293A−25TMB
5962−88680	043X	CY7C293A−25QMB
5962−88734	02JX	CY7C292A−45DMB
5962−88734	02KX	CY7C291A−45KMB
5962−88734	02LX	CY7C291A−45DMB
5962−88734	023X	CY7C291A−45LMB
5962−88734	03JX	CY7C292A−35DMB
5962−88734	03KX	CY7C291A−35KMB
5962−88734	03LX	CY7C291A−35DMB
5962−88734	033X	CY7C291A−35LMB
5962−88734	04JX	CY7C292A−25DMB
5962−88734	04KX	CY7C291A−25KMB
5962−88734	04LX	CY7C291A−25DMB
5962−88734	043X	CY7C291A−25LMB

Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970s and continue to provide the highest-speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are intact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a programming system. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. The result of this inability to completely test is less than 100% yield during programming by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or by trouble shooting an assembled board or system.

Cypress non-volatile memories use an EPROM programming mechanism. This technology has been in use in MOS technologies since the late 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is faster than bipolar and, coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point of view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate, which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. When these cells are programmed, the performance of each cell in the memory can be tested, ensuring that we ship devices that program every time and will perform as specified when programmed. In addition, when these devices are supplied in a windowed package they can be programmed and erased indefinitely providing the designer a reprogrammable PROM for development.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

Programming Algorithm

Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis, unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data-out pins during the programming operation, and the data is read from these same pins for verification that the byte has been programmed.

Blank Check for Differential Cells

Since a differential cell contains neither a 1 not a 0 before it is programmed, the conventional blank check is not valid. For this reason, Cypress CMOS PROMs that use differential cells contain a special blank check mode of operation. Blank check is performed by separately examining the 0 and 1 sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes: one comparing the 0 side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier, and then repeating this operation for the 1 side of the cell. The modes are called blank check ones and blank check zeros. These modes are entered by applying a supervoltage to the device.

Blank Check for Single-Ended Cells

Single-ended cells blank check in a conventional manner. An erased device contains all 0s or all 1s depending on the device and a programmed cell will contain a 1 or a 0 again depending on the device. Cypress PROMs that use the single-ended approach provide a specific mode to perform the blank check, which also provides the verify function. This makes the need to switch high voltages unnecessary during the program verify operation. See specific datasheets for details. All CY7CXX (except CY7C271A), CY27C128 and CY27C256 blank check with all 0s. All CY27HXX, CY27CXX (except CY27C128 and CY27C256), and CY7C271A blank check with all 1s.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a read and write pin in the programming mode. These are active-LOW signals and cause the data on the output pins to be written into the addressed memory location in the case of the write signal or read out of the device in the case of the read signal. When both the read and write signals are HIGH, the outputs are disabled and in a high-impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the write signal. Verification of data is accomplished by reading the information on the output pins while the read signal is active.

The timing for actual programming is supplied in the unique programming specifications for each device.

Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable Initial Byte and Programmable Synchronous/Asynchronous Enable available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature. Several Cypress non-volatile memories feature an automatic device identification mode. This mode is accessed by placing the supervoltage on the A_9 address pin. While A_9 is HIGH, taking A_0 LOW will cause the Cypress manufacturer ID (34H) to appear on the outputs. Taking A_0 HIGH will cause the device identifier to appear on the outputs. See the specific datasheet for details.

Programming Support

Programming support for Cypress CMOS PROMs is available on Cypress's QuickPro II and Impulse 3. Support is also available from a number of programmer manufacturers, some of which are listed below. In addition, Cypress offers factory programming for all of these devices. Parts are programmed and 100% speed tested to your code to ensure performance. Custom marking is available also on programmed plastic (OTP) devices. Minimum quantities apply. Contact a Cypress sales representative for more information.

Cypress Semiconductor, Inc.
3901 North First St.
San Jose, CA 95134
(408) 943–2600

AVAL Data Corp.
M. K. Bldg. 2F 4–8 Nakaitabashi,
Itabashi–ku
Tokyo, Japan 173
03 (5375)–7321

BP Microsystems
10681 Haddington, Ste. #190
Houston, TX 77043
(800) 225–2102

Data I/O
Customer Resource Center
10525 Willows Rd. NE
P.O. Box 97046
Redmond, WA 98073–9746
(800) 247–5700
(206) 881–6444

Logical Devices Inc.
692 South Military Trail
Deerfield, FL 33442
(305) 428–6868

Minato Electronics
4105, Minami Yamada-cho
Kohoku-ku
Yokohama, Japan 223
(045) 591–5611

SMS Mikrocomputersystem GmbH
Im Grund 15
D–7988 Wangen im Allgeau
BRD
(49) 7522–5018

SMS Microcomputer
P.O. Box 1348
Lawrence, MA 01842
(508) 683–4659

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988–1118

System General
510 S. Park Victoria
Milpitas, CA 95035
(408) 263–6667

Document #: 38–00235–A

Section Contents

FIFOs

CY7C401/CY7C403
CY7C402/CY7C404

64 x 4 Cascadable FIFO
64 x 5 Cascadable FIFO

Features

- **64 x 4 (CY7C401 and CY7C403) 64 x 5 (CY7C402 and CY7C404) High-speed first-in first-out memory (FIFO)**
- **Processed with high-speed CMOS for optimum speed/power**
- **25-MHz data rates**
- **50-ns bubble-through time—25 MHz**
- **Expandable in word width and/or length**
- **5-volt power supply ±10% tolerance, both commercial and military**
- **Independent asynchronous inputs and outputs**
- **TTL-compatible interface**
- **Output enable function available on CY7C403 and CY7C404**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Pin compatible with MMI 67401A/67402A**

Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out memories (FIFOs) organized as 64 four-bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five-bit words. Both the CY7C403 and CY7C404 have an output enable (OE) function.

The devices accept 4- or 5-bit words at the data input (DI_0 – DI_n) under the control of the shift in (SI) input. The stored words stack up at the output (DO_0 – DO_n) in the order they were entered. A read command on the shift out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The input ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for cascading. The output ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

Parallel expansion for wider words is accomplished by logically ANDing the IR and OR signals to form composite signals.

Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The IR pin of the receiving device is connected to the SO pin of the sending device, and the OR pin of the sending device is connected to the SI pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25-MHz operation makes these FIFOs ideal for high-speed communication and controller applications.

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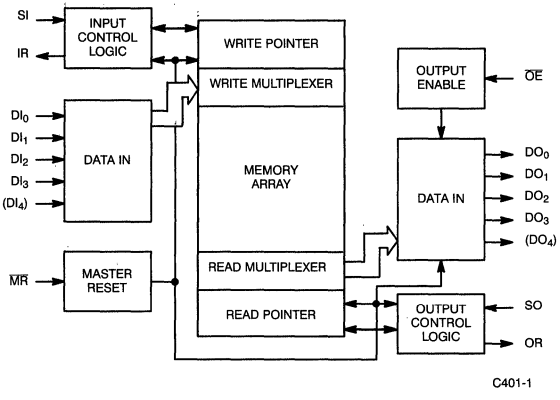
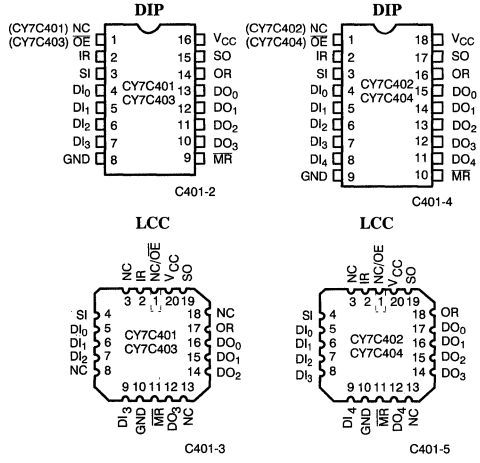
Logic Block Diagram



Pin Configurations



Selection Guide

		7C401/2–5	7C40X–10	7C40X–15	7C40X–25
Operating Frequency (MHz)		5	10	15	25
Maximum Operating Current (mA)	Commercial	75	75	75	75
	Military		90	90	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

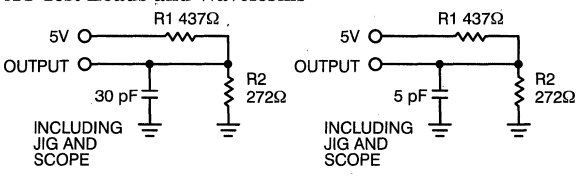
Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[2]

Parameter	Description	Test Conditions		7C40X−10, 15, 25 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	µA
V_{CD}[3]	Input Diode Clamp Voltage[3]					
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)		− 50	+50	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		75	mA
			Military		90	mA

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms



(a) Normal Load (b) High-Z Load

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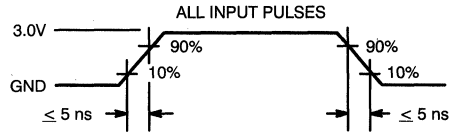

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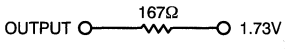
Equivalent to: THÉVENIN EQUIVALENT



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Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% output).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 6]

Parameter	Description	Test Conditions	7C401–5 7C402–5		7C40X–10		7C40X–15		7C40X–25[7]		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 8		5		10		15		25	MHz
t_{PHSI}	SI HIGH Time		20		20		20		11		ns
t_{PLSI}	SO LOW Time		45		30		25		20		ns
t_{SSI}	Data Set-Up to SI	Note 9	0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 9	60		40		30		20		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			75		40		35		21/22	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			75		45		40		28/30	ns
t_{PHSO}	SO HIGH Time		20		20		20		11		ns
t_{PLSO}	SO LOW Time		45		25		25		20		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			75		40		35		19/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			80		55		40		34/37	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		ns
t_{BT}	Bubble-Through Time			200	10	95	10	65	10	50/60	ns
t_{SIR}	Data Set-Up to IR	Note 10	5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 10	30		30		30		20		ns
t_{PIR}	Input Ready Pulse HIGH		20		20		20		15		ns
t_{POR}	Output Ready Pulse HIGH		20		20		20		15		ns
t_{PMR}	MR Pulse Width		40		30		25		25		ns
t_{DSI}	MR HIGH to SI HIGH		40		35		25		10		ns
t_{DOR}	MR LOW to OR LOW			85		40		35		35	ns
t_{DIR}	MR LOW to IR HIGH			85		40		35		35	ns
t_{LZMR}	MR LOW to Output LOW	Note 11		50		40		35		25	ns
t_{OOE}	Output Valid from OE LOW			—		35		30		20	ns
t_{HZOE}	Output High Z from OE HIGH	Note 12		—		30		25		15	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads and Waveforms.
7. Commercial/Military
8. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$
9. t_{SSI} and t_{HSI} apply when memory is not full.
10. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
11. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.
12. High-Z transitions are referenced to the steady-state V_{OH} −500 mV and V_{OL} +500 mV levels on the output. t_{HZOE} is tested with 5-pF load capacitance as in part (b) of AC Test Loads and Waveforms.

Operational Description

Concept

Unlike traditional FIFOs, these devices are designed using a dual-port memory, read and write pointer, and control logic. The read and write pointers are incremented by the SO and SI respectively. The availability of an empty space to shift in data is indicated by the IR signal, while the presence of data at the output is indicated by the OR signal. The conventional concept of bubble-through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an OR signal. The output enable ($\overline{OE}$) signal provides the capability to OR tie multiple FIFOs together on a common bus.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset (MR) signal. This causes the FIFO to enter an empty condition signified by the OR signal being LOW at the same time the IR signal is HIGH. In this condition, the data outputs ($DO_0 - DO_n$) will be in a LOW state.

Shifting Data In

Data is shifted in on the rising edge of the SI signal. This loads input data into the first word location of the FIFO. On the falling edge of the SI signal, the write pointer is moved to the next word position and the IR signal goes HIGH, indicating the readiness to accept new data. If the FIFO is full, the IR will remain LOW until a word of data is shifted out.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of the SO signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the OR signal will go HIGH. If data is not present, the OR signal will stay LOW indicating the FIFO is empty. Upon the rising edge of SO, the OR signal goes LOW. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

Bubble-Through

Two bubble-through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the OR flag goes HIGH, indicating valid data at the output.

The second bubble-through condition occurs when the device is full. Shifting data out creates an empty location that propagates to the input. After a delay, the IR flag goes HIGH. If the SI signal is HIGH at this time, data on the input will be shifted in.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

When this violation occurs, the operation of the FIFO is unpredictable. It must then be reset, and all data is lost.

Application of the 7C403–25/7C404–25 at 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFOs requires knowledge of characteristics that are not easily specified in a datasheet, but which are necessary for reliable operation under all conditions, so we will specify them here.

When an empty FIFO is filled with initial information at maximum "shift in" SI frequency, followed by immediate shifting out of the data also at maximum "shift out" SO frequency, the designer must be aware of a window of time which follows the initial rising edge of the OR signal, during which time the SO signal is not recognized. This condition exists only at high-speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full-frequency operation, but rather delays the full 25-MHz operation until after the window has passed.

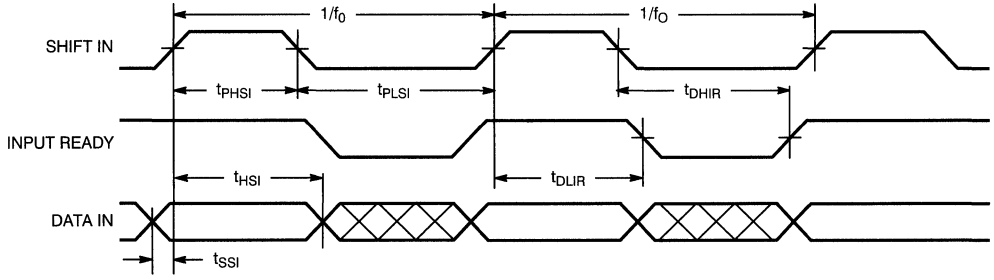
There are several implementation techniques for managing the window so that all SO signals are recognized:

1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns "initiated by the SI signal only when the FIFO is empty" to inhibit or gate the SO activity. However, this requires that the SO operation be at least temporarily synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is more than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR signal. This however involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of IR and SI conditions as well as SO.
4. Handshaking with the OR signal is a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This ensures that the SO pulse that is initiated in the window will be automatically extended long enough to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the SO signal is most appropriate because data is guaranteed to be stable prior to and after the SO leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will ensure the correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and is dependent on the specific application needs.

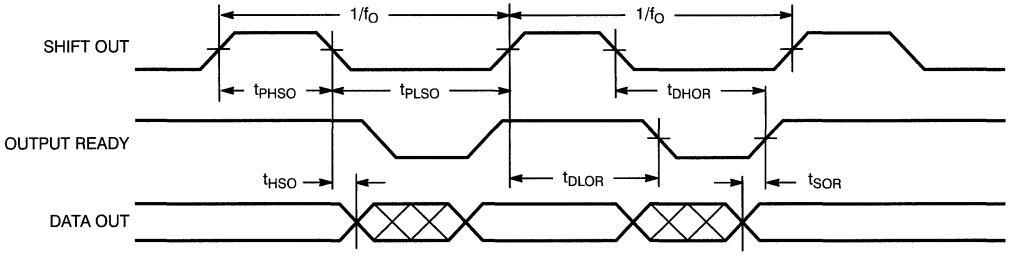
Switching Waveforms

Data In Timing Diagram



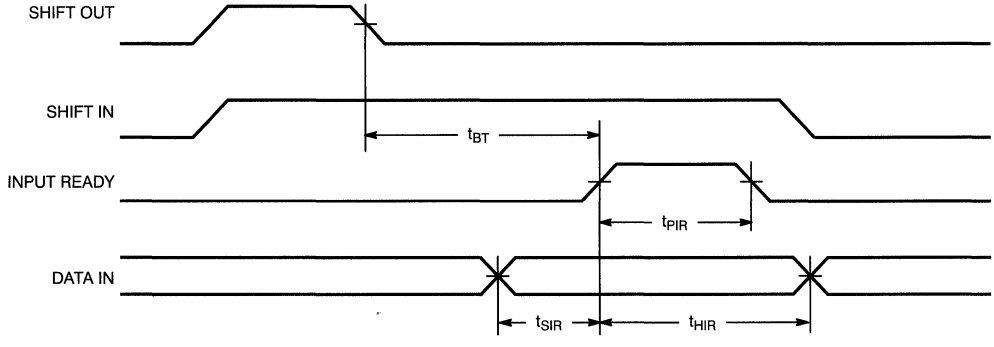
C401-9

Data Out Timing Diagram



C401-10

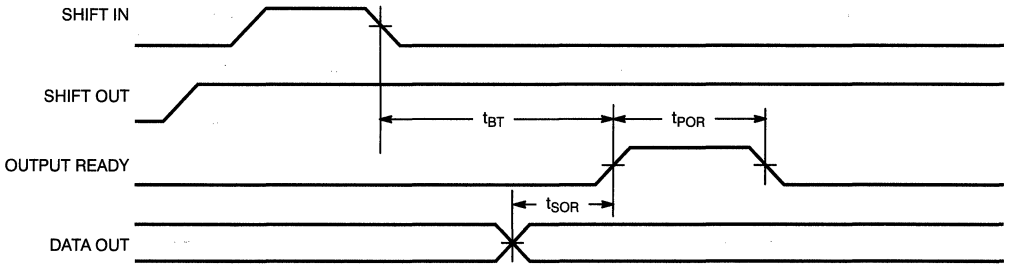
Bubble Through, Data Out To Data In Diagram



C401-11

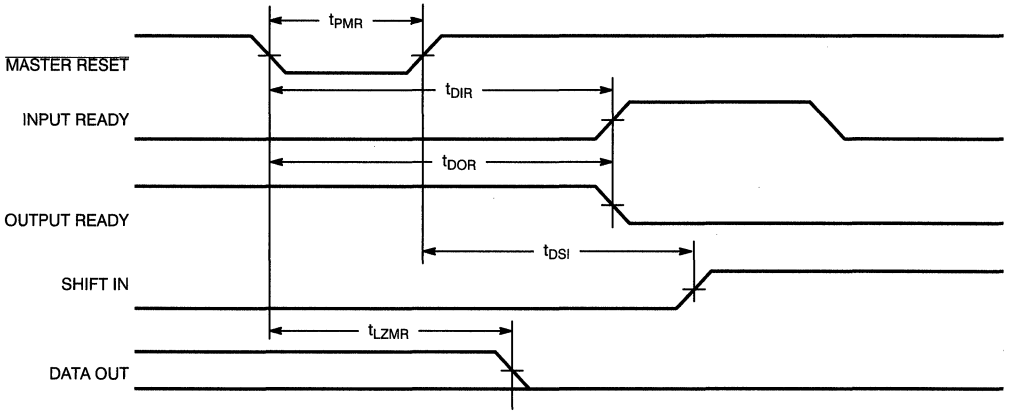
Switching Waveforms (continued)

Bubble Through, Data In To Data Out Diagram



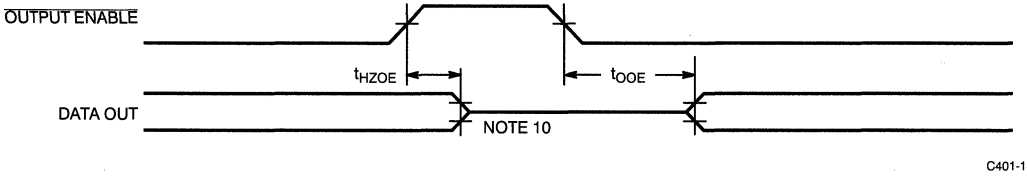
C401-12

Master Reset Timing Diagram



C401-13

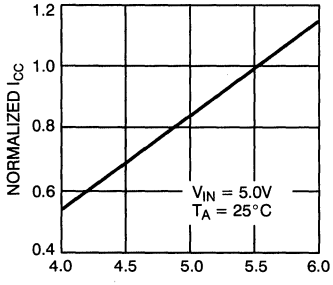
Output Enable Timing Diagram



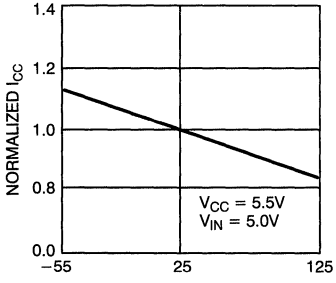
C401-14

Typical DC and AC Characteristics

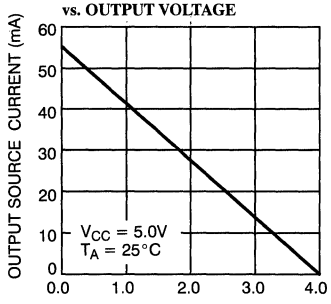
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



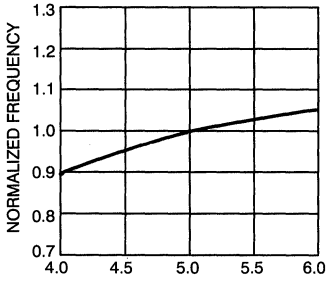
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



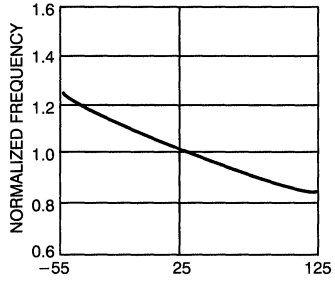
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



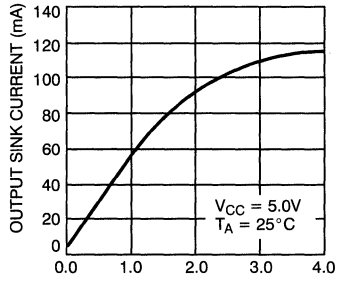
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



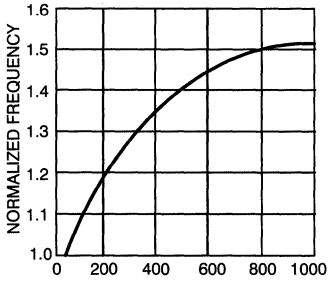
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



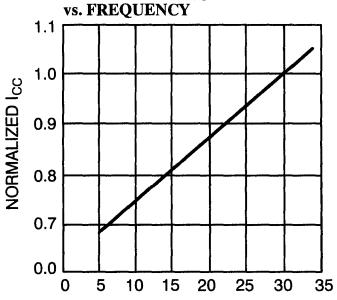
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



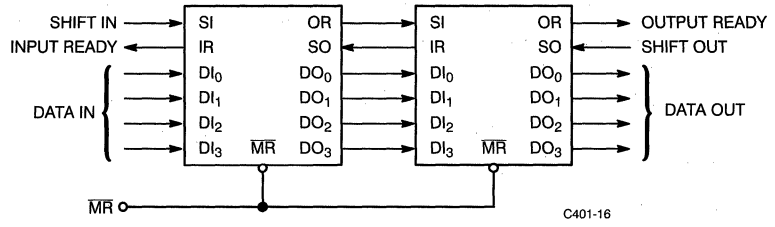
NORMALIZED I_{CC} vs. FREQUENCY



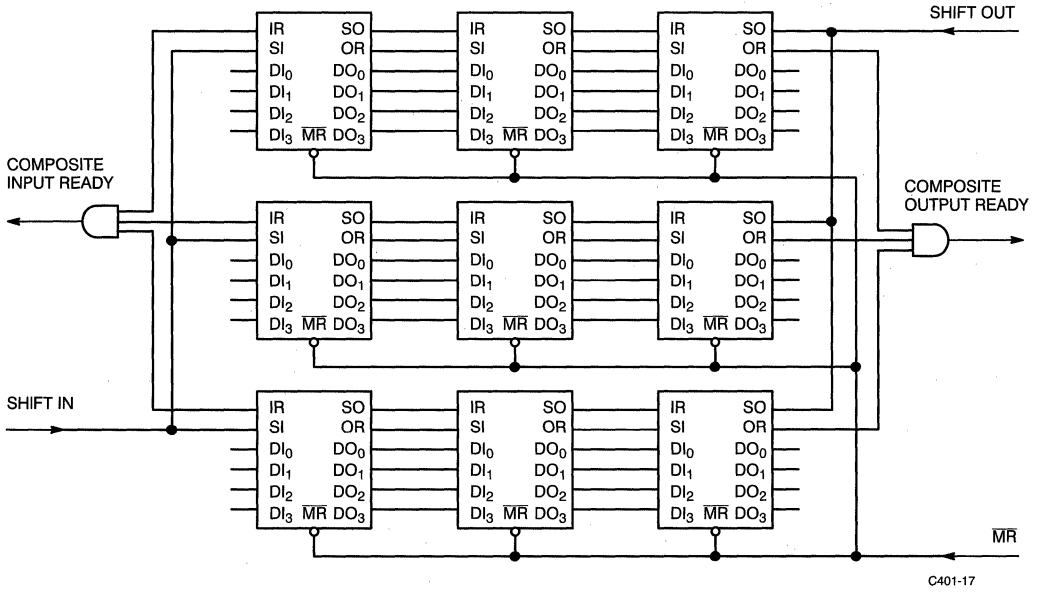
C401-15

FIFO Expansion[13, 14, 15, 16, 17]

128 x 4 Application[18]



192 x 12 Application[19]



Notes:

13. When the memory is empty, the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
14. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data, and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid, stable data on the outputs.
15. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
16. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH, then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
17. All Cypress FIFOs will cascade with other Cypress FIFOs. However, hey may not cascade with pin-compatible FIFOs from other manufacturers.
18. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
19. FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite input and output ready flags. This need is due to the variation of delays of the FIFOs.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
5	CY7C401–5PC	P1	16-Lead (300-Mil) Molded DIP	Commercial
10	CY7C401–10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C401–15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C401–25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C401–25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C401–25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C401–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
5	CY7C402–5PC	P3	18-Lead (300-Mil) Molded DIP	Commercial
10	CY7C402–10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–10PC	P3	20-Pin Square Leadless Chip Carrier	
	CY7C402–10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C402–15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C402–15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C402–25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C402–25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C402–25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C402–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information (continued)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C403–10DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–10PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–10DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C403–15DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–15PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–15DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C403–25DC	D2	16-Lead (300-Mil) CerDIP	Commercial
	CY7C403–25PC	P1	16-Lead (300-Mil) Molded DIP	
	CY7C403–25DMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY7C403–25LMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C404–10DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–10PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–10DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–10LMB	L61	20-Pin Square Leadless Chip Carrier	
15	CY7C404–15DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–15PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–15DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–15LMB	L61	20-Pin Square Leadless Chip Carrier	
25	CY7C404–25DC	D4	18-Lead (300-Mil) CerDIP	Commercial
	CY7C404–25PC	P3	18-Lead (300-Mil) Molded DIP	
	CY7C404–25DMB	D4	18-Lead (300-Mil) CerDIP	Military
	CY7C404–25LMB	L61	20-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{OOE}	7, 8, 9, 10, 11
t_{HZOE}	7, 8, 9, 10, 11

Document #: 38–00040–H

CY7C408A
CY7C409A

64 x 8 Cascadable FIFO
64 x 9 Cascadable FIFO

Features

- **64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory**
- **35-MHz shift in and shift out rates**
- **Almost Full/Almost Empty and Half Full flags**
- **Dual-port RAM architecture**
- **Fast (50-ns) bubble-through**
- **Independent asynchronous inputs and outputs**
- **Output enable (CY7C408A)**
- **Expandable in word width and FIFO depth**
- **5V ±10% supply**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge voltage**
- **300-mil, 28-pin DIP**

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry-standard handshaking signals, almost full/almost empty (AFE) and half full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an output enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI_0 – DI_8) under the control of the shift in (SI) input when the input ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO_0 – DO_8 output pins under the control of the shift out (SO) input when the output ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored; if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

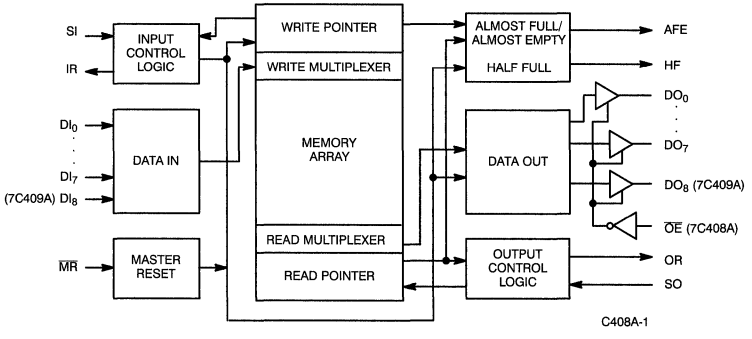
The IR and OR signals are also used to connect the FIFOs in parallel to make a wider word or in series to make a deeper buffer, or both.

Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together (*Figure 5*). The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

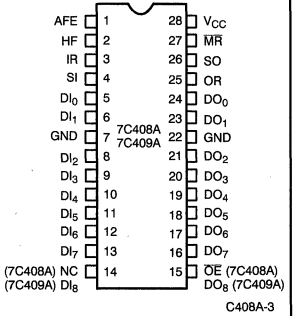
Serial expansion (cascading) for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO (*Figure 4*). In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

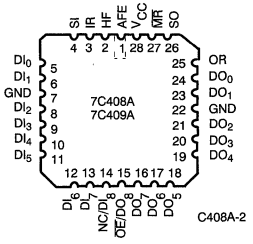
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift in and shift out rates of these FIFOs, and their high throughput rate due to the fast bubblethrough time, which is due to their dual-port RAM architecture, make them ideal for high-speed communications and controllers.

Logic Block Diagram



Pin Configurations





Flag Definitions

HF	AFE	Words Stored
L	H	0 – 8
L	L	9 – 31
H	L	32 – 55
H	H	56 – 64

Selection Guide

		7C408A–15 7C409A–15	7C408A–25 7C409A–25	7C408A–35 7C409A–35
Maximum Shift Rate (MHz)		15	25	35
Maximum Operating Current (mA)[1]	Commercial	115	125	135
	Military	140	150	N/A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State (7C408A) ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Power Dissipation 1.0W
Output Current, into Outputs (Low) ..... 20 mA
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

5

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		100	mA
			Military		125	mA
I_{CC}	Power Supply Current	$I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$				

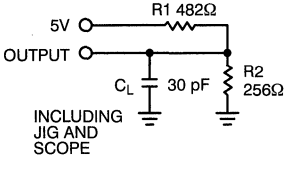
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

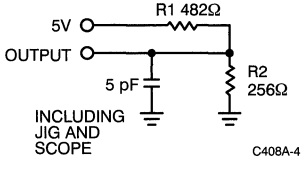
Notes:

1. $I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

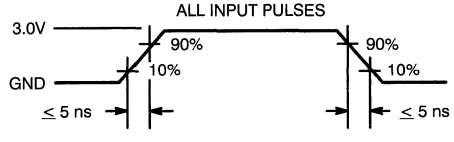


(a) Normal Load



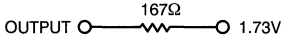
C408A-4

(b) High-Z Load



C408A-5

Equivalent to: THÉVENIN EQUIVALENT



C408A-6

Switching Characteristics Over the Operating Range[3, 6]

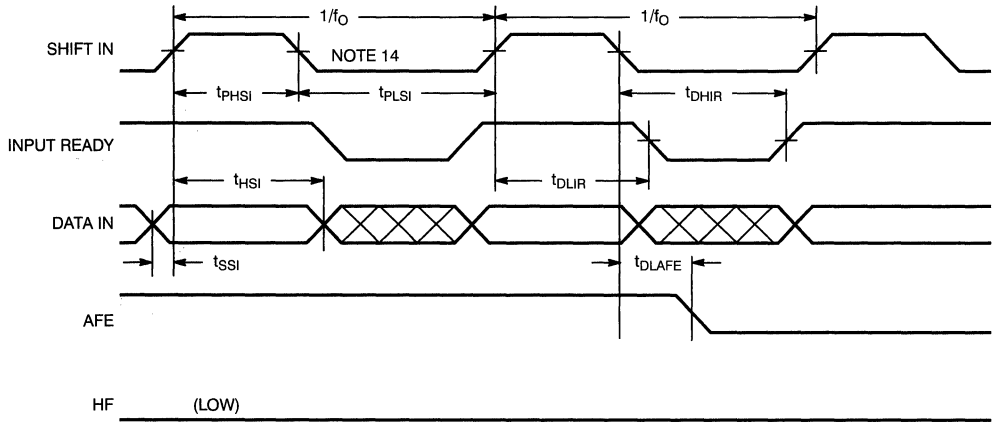
Parameter	Description	Test Conditions	7C408A–15 7C409A–15		7C408A–25 7C409A–25		7C408A–35 7C409A–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 7		15		25		35	MHz
t_{PHSI}	SI HIGH Time	Note 7	23		11		9		ns
t_{PLSI}	SI LOW Time	Note 7	25		24		17		ns
t_{SSI}	Data Set-Up to SI	Note 8	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 8	30		20		12		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t_{PHSO}	SO HIGH Time	Note 7	23		11		9		ns
t_{PLSO}	SO LOW Time	Note 7	25		24		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		0		0		0		ns
t_{BT}	Fall-through, Bubble-back Time		10	65	10	60	10	50	ns
t_{SIR}	Data Set-Up to IR	Note 9	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 9	30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH	Note 10	6		6		6		ns
t_{POR}	Output Ready Pulse HIGH	Note 11	6		6		6		ns
t_{DLZOE}	OE LOW to LOW Z (7C408A)	Note 12		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (7C408A)	Note 7		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 13		55		45		35	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH			55		45		35	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW			55		45		35	ns
t_{OD}	SO LOW to Next Data Out Valid			28		20		16	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in parts (a) and (b) of AC Test Loads and Waveforms.
7. $1/f_O \geq (t_{PHSI} + t_{PLSI})$, $1/f_O \geq (t_{PHSO} + t_{PLSO})$.
8. t_{SSI} and t_{HSI} apply when memory is not full.
9. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
10. At any given operating condition $t_{PIR} \geq (t_{PHSO}$ required).
11. At any given operating condition $t_{POR} \geq (t_{PHSI}$ required).
12. t_{DHZOE} and t_{DLZOE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. t_{DHZOE} transition is measured ±500 mV from steady-state voltage. t_{DLZOE} transition is measured ±100 mV from steady-state voltage. These parameters are guaranteed and not 100% tested.
13. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

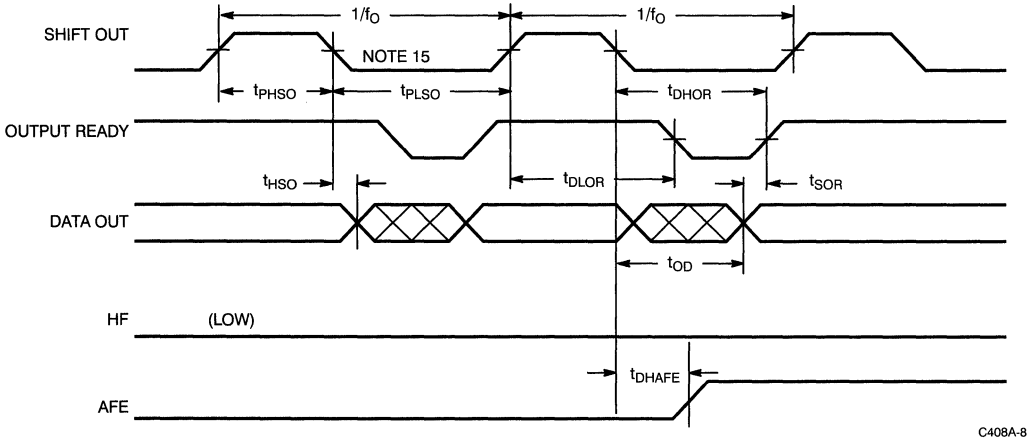
Switching Waveforms

Data In Timing Diagram



C408A-7

Data Out Timing Diagram

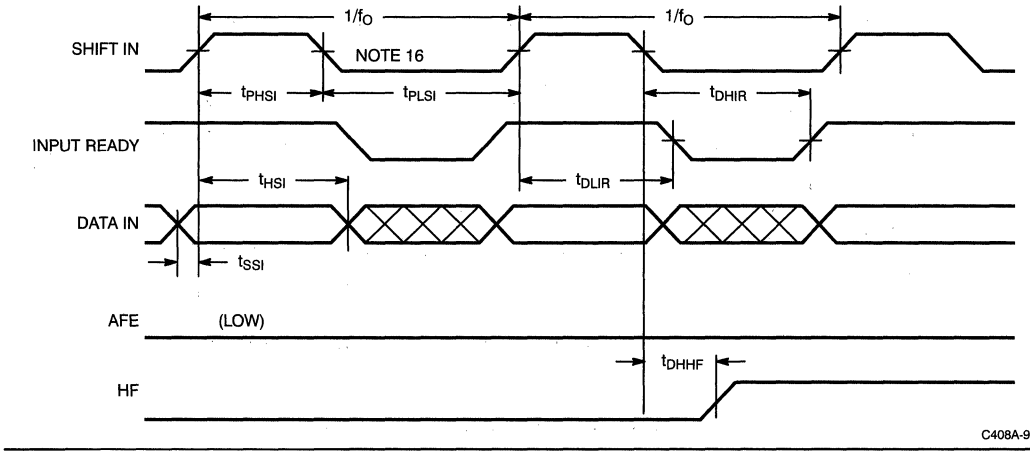


C408A-8

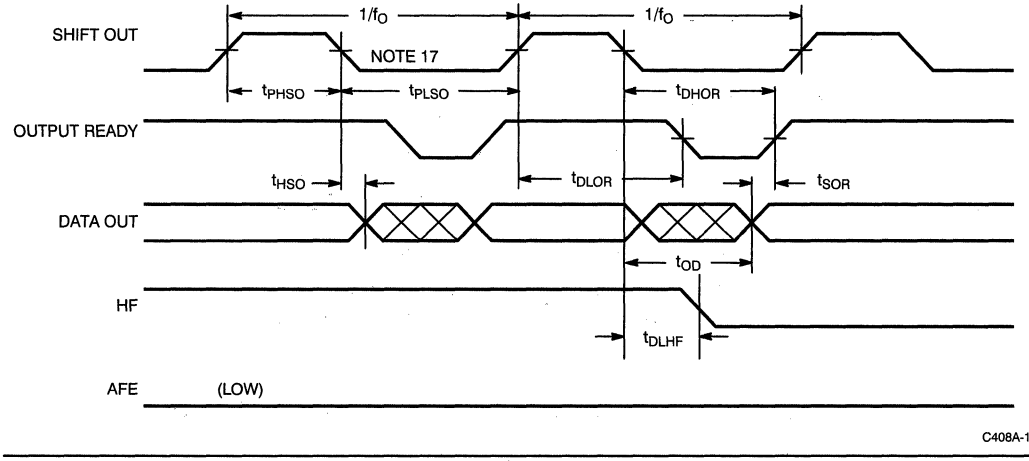
Notes:
14. FIFO contains 8 words.
15. FIFO contains 9 words.

Switching Waveforms (continued)

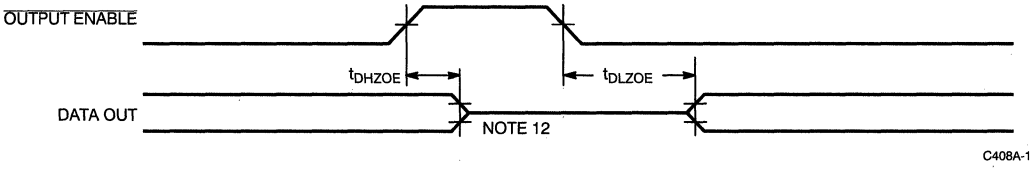
Data In Timing Diagram



Data Out Timing Diagram



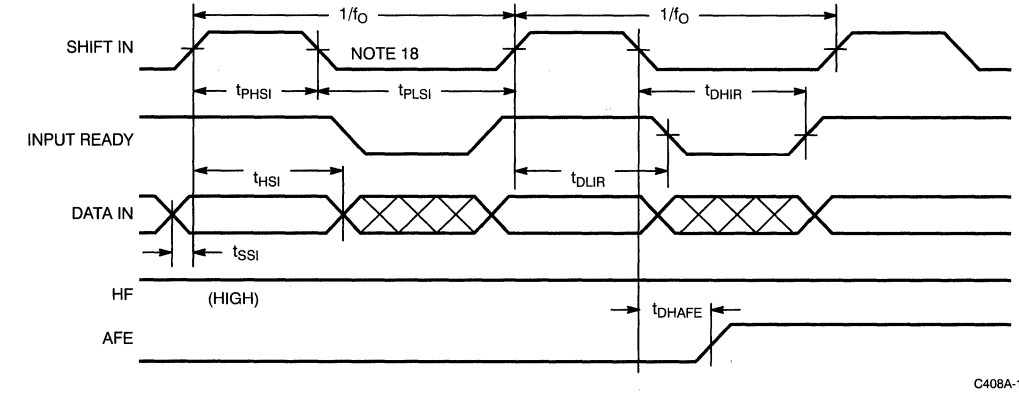
Output Enable (CY7C408A only)



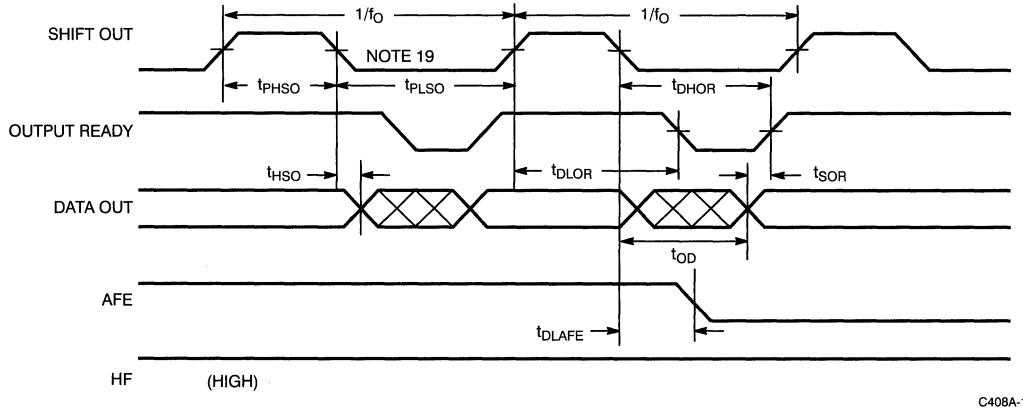
Notes:
16. FIFO contains 31 words.
17. FIFO contains 32 words.

Switching Waveforms (continued)

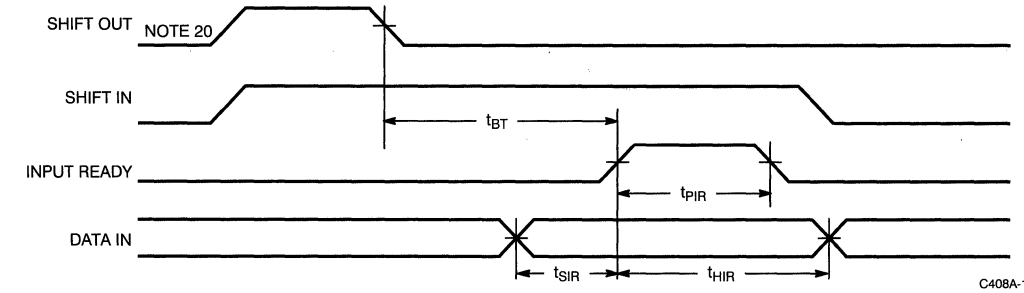
Data In Timing Diagram



Data Out Timing Diagram



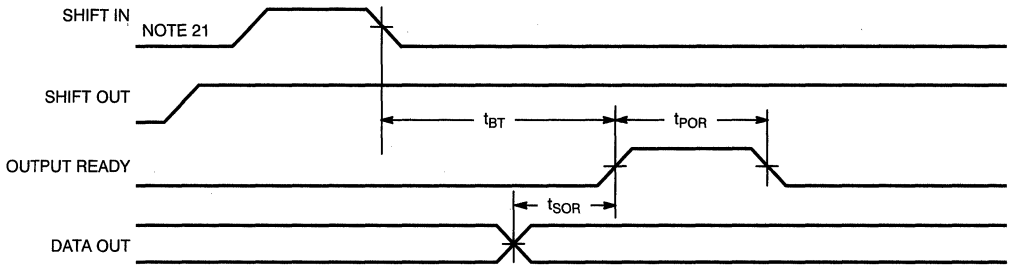
Bubble-Back, Data Out To Data In Diagram



Notes:
18. FIFO contains 55 words.
19. FIFO contains 56 words.
20. FIFO contains 64 words.

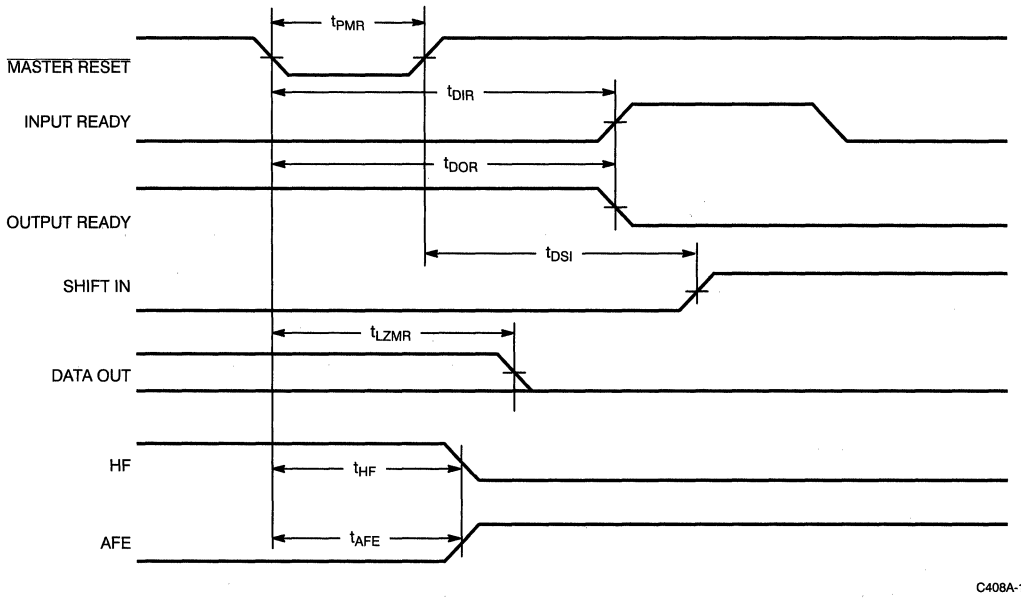
Switching Waveforms (continued)

Fall-Through, Data In to Data Out Diagram



C408A-15

Master Reset Timing Diagram



C408A-16

Note:
21. FIFO is empty.

Architecture of the CY7C408A and CY7C409A

The CY7C408A and CY7C409A FIFOs consist of an array of 64 words of 8 or 9 bits each (which are implemented using a dual-port RAM cell), a write pointer, a read pointer, and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the almost full/almost empty (AFE) and half full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which it would have to do if the memory were implemented using the conventional register array architecture.

Fall-Through and Bubble-Back

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the fall-through time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the bubble-back time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-through time when it is empty (or near empty) and by the bubble-back time when it is full (or near full).

The conventional definitions of fall-through and bubble-back do not apply to the CY7C408A and CY7C409A FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst-case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0 – DO_8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the input ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the shift in (SI) pin will clock the data on the DI_0 – DI_8 inputs into the FIFO. Data propagates through the device at the falling edge of SI.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH-to-LOW transition of the SI signal initiates the LOW-to-HIGH transition of the IR signal if the FIFO is not full. If the FIFO is full, IR will remain LOW.

Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the output ready (OR) signal. After the FIFO is reset all data outputs (DO_0 – DO_8) will be in the LOW state. As long as the FIFO remains empty, the OR signal will be LOW and all SO pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

AFE and HF Flags

Two flags, almost full/almost empty (AFE) and half full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are 8 or fewer or 56 or more words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO (*Figures 1* and *2*).

Due to the asynchronous nature of the SI and SO signals, it is possible to encounter specific timing relationships which may cause short pulses on the AFE and HF flags. These pulses are entirely due to the dynamic relationship of the SI and SO signals. The flags, however, will always settle to their correct state after the appropriate delay (t_{DHAFE}, t_{DLAFE}, t_{DHHF} or t_{DLHF}). Therefore, use of level-sensitive rather than edge-sensitive flag detection devices is recommended to avoid false flag encoding.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

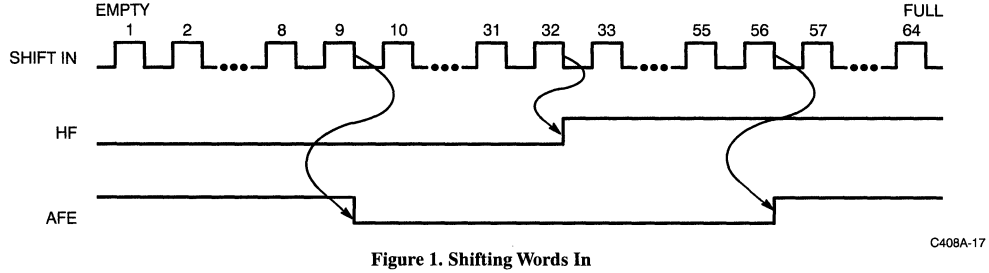


Figure 1. Shifting Words In

Cascading the 7C408/9A–35 Above 25 MHz

First, the capacity of N cascaded FIFOs is decreased from N × 64 to (N × 63) + 1.

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal must be inverted before being fed back to the interface SO pin (*Figure 3*). Two things should be noted when this configuration is implemented.

First. the capacity of N cascaded FIFOs id decreased from N × 64 to (N × 63)+1.

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data shifted in faster than it is shifted out, and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.[28]

When data packets[29] are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 (=2 × 63 + 1) words may be shifted in at up to 35 MHz and then the entire packet may be shifted out at up to 35 MHz.

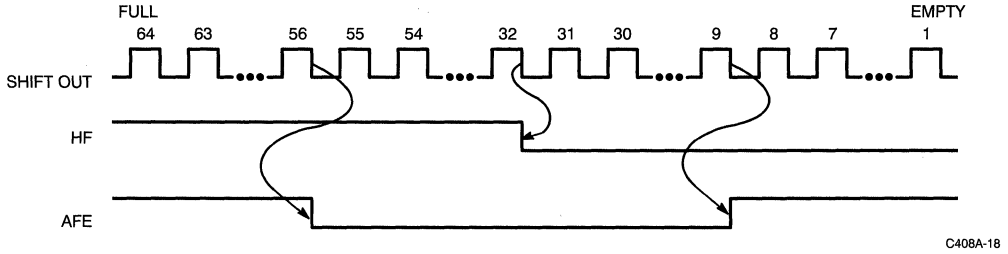


Figure 2. Shifting Words Out

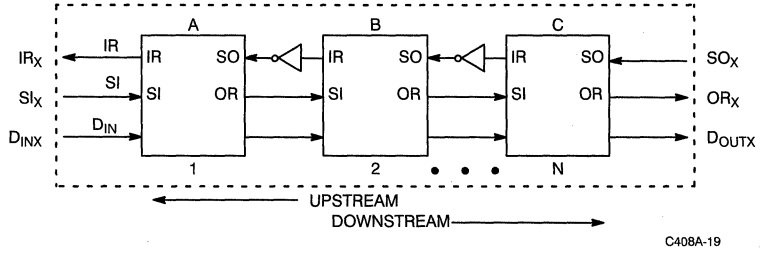


Figure 3. Cascaded Configuration Above 25 MHz

128 x 9 Configuration

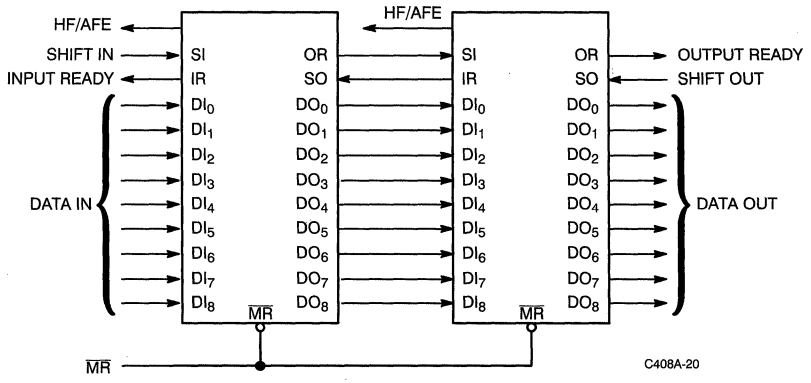


Figure 4. Cascaded Configuration at or below 25 MHz[22, 23, 24, 25, 26]

192 x 27 Configuration

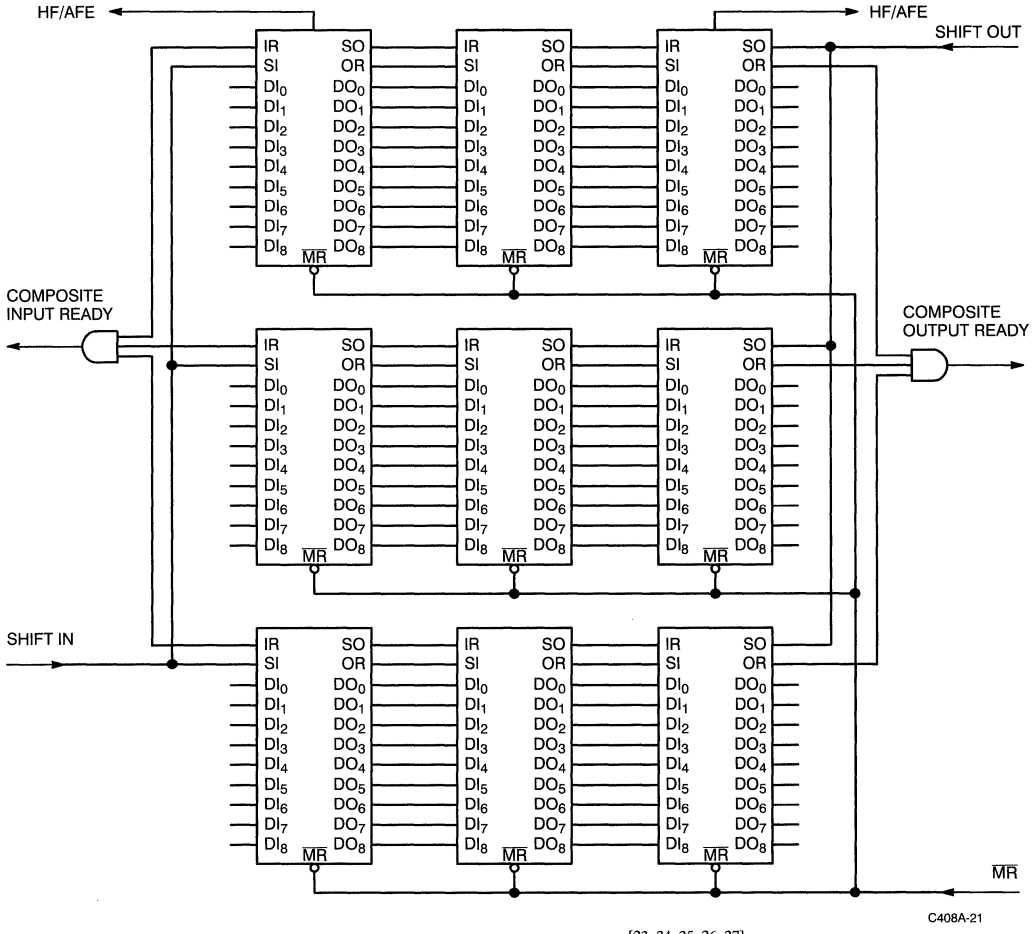


Figure 5. Depth and Width Expansion[23, 24, 25, 26, 27]

Notes:

22. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
23. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output.
24. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
25. If SO is held HIGH while the memory is empty and a word is written into the input, that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
26. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH, and OR goes LOW.
27. FIFOs are expandable in depth and width. However, in forming wider words, two external gates are required to generate composite input ready and output ready flags. This need is due to the variation of delays of the FIFOs.

If data is to be shifted out simultaneously with the data being shifted in, the concept of "virtual capacity" is introduced. Virtual capacity is simply how large a packet of data can be shifted in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted out at any given frequency. *Figure 6* is a graph of packet size[30] vs. shift out frequency (f_{SOx}) for two different values of shift in frequency (f_{SIx}) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high shift out frequency is to be maintained, i.e., a 35 MHz f_{SOx} can be sustained when reading data packets from devices cascaded two or three deep.[31] If data is shifted in simultaneously, *Figure 6* applies with f_{SIx} and f_{SOx} interchanged.

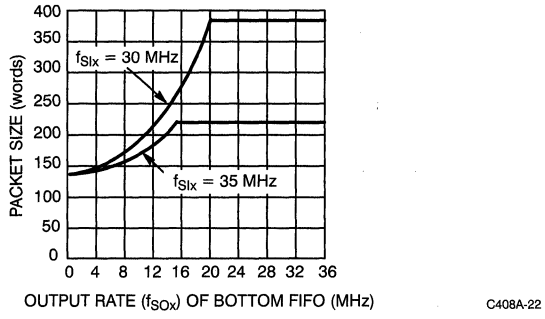


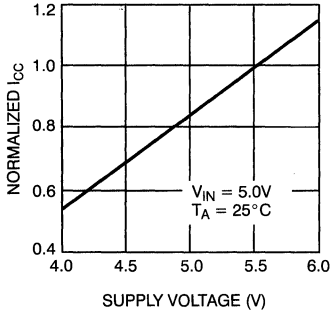
Figure 6. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter

Notes:

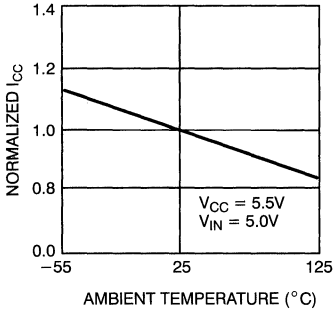
28. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
29. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is shifted in without simultaneous shift out clock occurring. The complement of this holds when data is shifted out as a packet.
30. These are typical packet sizes using an inverter whose delay is 4 ns.
31. Only devices with the same speed grade are specified to cascade together.

Typical DC and AC Characteristics

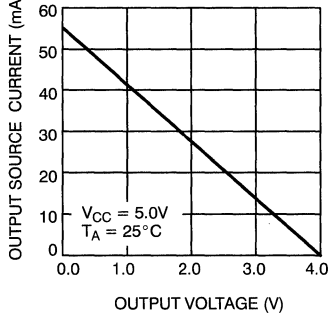
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



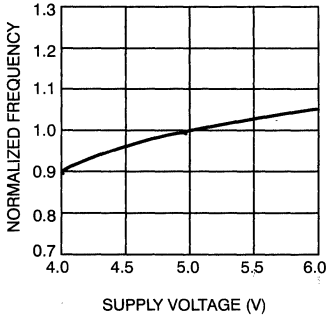
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



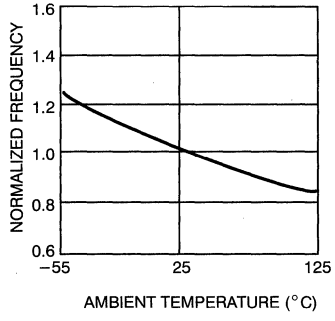
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



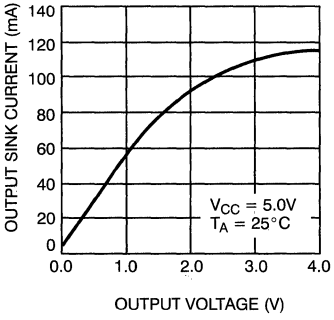
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



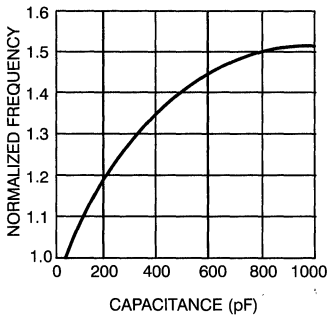
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



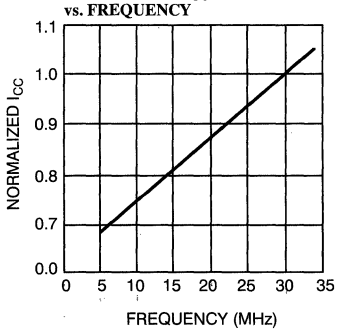
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



C408A-23

Ordering Information

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C408A–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A–15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C408A–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C408A–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A–35VC	V21	28-Lead (300-Mil) Molded SOJ	

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C409A–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A–15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C409A–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C409A–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A–35VC	V21	28-Lead (300-Mil) Molded SOJ	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CCQ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{SIIR}	7, 8, 9, 10, 11
t_{SOOR}	7, 8, 9, 10, 11
t_{DLZOE}	7, 8, 9, 10, 11
t_{DHZOE}	7, 8, 9, 10, 11
t_{DHHF}	7, 8, 9, 10, 11
t_{DLHF}	7, 8, 9, 10, 11
t_{DLAFE}	7, 8, 9, 10, 11
t_{DHAFE}	7, 8, 9, 10, 11
t_B	7, 8, 9, 10, 11
t_{OD}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{AFE}	7, 8, 9, 10, 11
t_{HF}	7, 8, 9, 10, 11

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256 x 9, 512 x 9, 1K x 9, 2K x 9, 4K x 9 Cascadable FIFO

Features

- **256 x 9, 512 x 9, 1,024 x 9, 2048 x 9, and 4096 x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 50.0-MHz read/write independent of depth/width**
- **Low operating power**
  - **I_{CC1} = 35 mA**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil DIP packaging**
- **7x7 TQFP**
- **300-mil SOJ packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7200, IDT7201, IDT7202, IDT7203, and IDT7204**

Functional Description

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, and CY7C432/3 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. They are, respectively, 256, 512, 1,024, 2,048, and 4,096 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

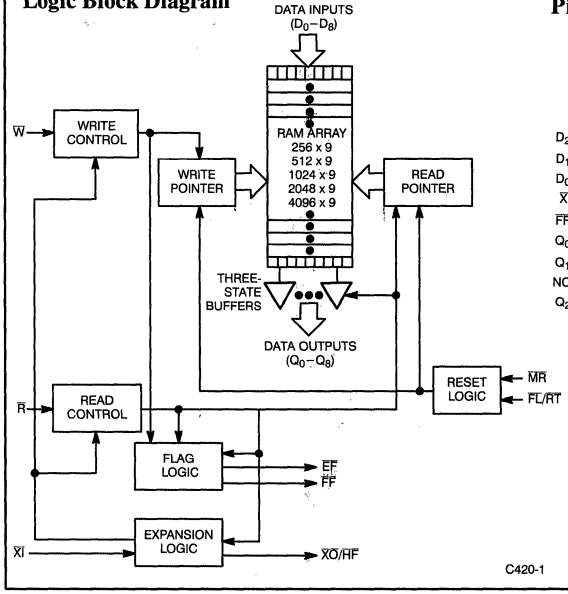
The read and write operations may be asynchronous; each can occur at a rate of 50.0 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

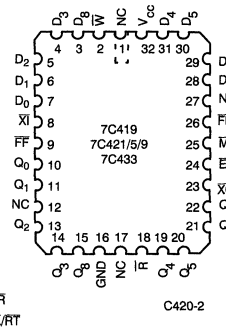
The CY7C419, CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, CY7C429, CY7C432, and CY7C433 are fabricated using an advanced 0.65-micron P-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout and guard rings.

Logic Block Diagram

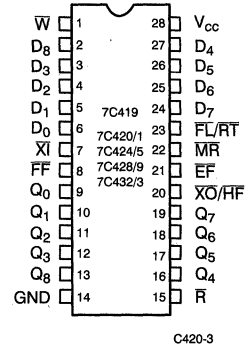


Pin Configurations

PLCC/LCC
Top View



DIP
Top View

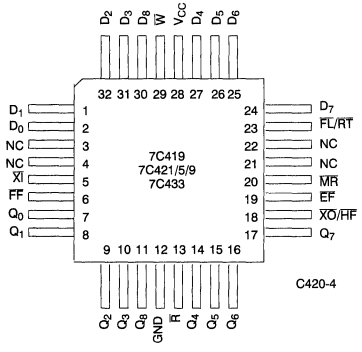


Selection Guide

256 x 9	**7C419–10**	**7C419–15**	**7C419–20**	**7C419–25**	**7C419–30**	**7C419–40**	**7C419–65**
512 x 9 (600-mil only)			**7C420–20**	**7C420–25**	**7C420–30**	**7C420–40**	**7C420–65**
512 x 9	**7C421–10**	**7C421–15**	**7C421–20**	**7C421–25**	**7C421–30**	**7C421–40**	**7C421–65**
1K x 9 (600-mil only)			**7C424–20**	**7C424–25**	**7C424–30**	**7C424–40**	**7C424–65**
1K x 9	**7C425–10**	**7C425–15**	**7C425–20**	**7C425–25**	**7C425–30**	**7C425–40**	**7C425–65**
2K x 9 (600-mil only)			**7C428–20**	**7C428–25**	**7C428–30**	**7C428–40**	**7C428–65**
2K x 9	**7C429–10**	**7C429–15**	**7C429–20**	**7C429–25**	**7C429–30**	**7C429–40**	**7C429–65**
4K x 9 (600-mil only)				**7C432–25**	**7C432–30**	**7C432–40**	**7C432–65**
4K x 9	**7C433–10**	**7C433–15**	**7C433–20**	**7C433–25**	**7C433–30**	**7C433–40**	**7C433–65**
Frequency (MHz)	50	40	33.3	28.5	25	20	12.5
Maximum Access Time (ns)	10	15	20	25	30	40	65
I_{CC1} (mA)	35	35	35	35	35	35	35

Pin Configurations (continued)

TQFP
Top View



Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C419–10, 15, 20, 25, 30, 40, 65 7C420/1–10, 15, 20, 25, 30, 40, 65 7C424/5–10, 15, 20, 25, 30, 40, 65 7C428/9–10, 15, 20, 25, 30, 40, 65 7C432/3–10, 15, 20, 25, 30, 40, 65 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			Note 3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−90	mA

Electrical Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Test Conditions		7C419–10 7C421–10 7C425–10 7C429–10 7C433–10 Min.	Max.	7C419–15 7C421–15 7C425–15 7C429–15 7C433–15 Min.	Max.	7C419–20 7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20 7C433–20 Min.	Max.	7C419–25 7C420–25 7C421–25 7C424–25 7C425–25 7C428–25 7C429–25 7C432–25 7C433–25 Min.	Max.	Unit
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = f_{MAX}	Com'l		85		65		55		50	mA
			Mil/Ind				100		90		80	
I_{CC1}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA F = 20 MHz	Com'l		35		35		35		35	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		10		10		10		10	mA
			Mil/Ind				15		15		15	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		5		5		5		5	mA
			Mil/Ind				8		8		8	

Electrical Characteristics Over the Operating Range[2] (continued)

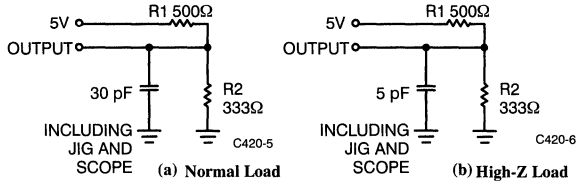
Parameter	Description	Test Conditions		7C419–30 7C420–30 7C421–30 7C424–30 7C425–30 7C428–30 7C429–30 7C432–30 7C433–30 Min.	Max.	7C419–40 7C420–40 7C421–40 7C424–40 7C425–40 7C428–40 7C429–40 7C432–40 7C433–40 Min.	Max.	7C419–65 7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65 7C432–65 7C433–65 Min.	Max.	Units
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = f_{MAX}	Com'l		40		35		35	mA
			Mil/Ind		75		70		65	
I_{CC1}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA F = 20 MHz	Com'l		35		35		35	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		10		10		10	mA
			Mil		15		15		15	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		5		5		5	mA
			Mil		8		8		8	

Capacitance[5]

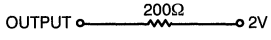
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	6	pF
C_{OUT}	Output Capacitance		6	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (Min.) = −2.0V for pulse durations of less than 20 ns.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[6, 7]

Parameter	Description	7C419-10 7C421-10 7C425-10 7C429-10 7C433-10 Min.	Max.	7C419-15 7C421-15 7C425-15 7C429-15 7C433-15 Min.	Max.	7C419-20 7C420-20 7C421-20 7C424-20 7C425-20 7C428-20 7C429-20 7C433-20 Min.	Max.	7C419-25 7C420-25 7C421-25 7C424-25 7C425-25 7C428-25 7C429-25 7C432-25 7C433-25 Min.	Max.	Unit
t_{RC}	Read Cycle Time	20		25		30		35		ns
t_A	Access Time		10		15		20		25	ns
t_{RR}	Read Recovery Time	10		10		10		10		ns
t_{PR}	Read Pulse Width	10		15		20		25		ns
t_{LZR}[5,8]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[8,9]	Data Valid After Read HIGH	5		5		5		5		ns
t_{HZR}[5,8,9]	Read HIGH to High Z		15		15		15		18	ns
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{PW}	Write Pulse Width	10		15		20		25		ns
t_{HWZ}[5,8]	Write HIGH to Low Z	5		5		5		5		ns
t_{WR}	Write Recovery Time	10		10		10		10		ns
t_{SD}	Data Set-Up Time	6		8		12		15		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	20		25		30		35		ns
t_{PMR}	$\overline{MR}$ Pulse Width	10		15		20		25		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		10		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	10		15		20		25		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	10		15		20		25		ns
t_{RTC}	Retransmit Cycle Time	20		25		30		35		ns
t_{PRT}	Retransmit Pulse Width	10		15		20		25		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		ns

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
7. See the last page of this specification for Group A subgroup testing information.
8. t_{HZR} transition is measured at +200 mV from V_{OL} and −200 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
9. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load and Waveforms.

Switching Characteristics Over the Operating Range[6, 7] (continued)

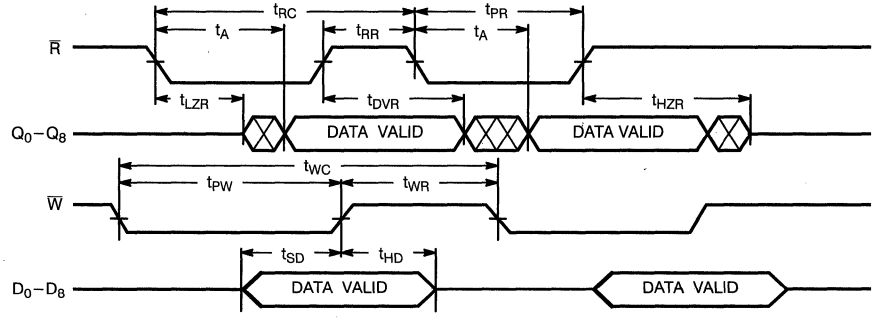
Parameter	Description	7C419–10 7C421–10 7C425–10 7C429–10 7C433–10		7C419–15 7C421–15 7C425–15 7C429–15 7C433–15		7C419–20 7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20 7C433–20		7C419–25 7C420–25 7C421–25 7C424–25 7C425–25 7C428–25 7C429–25 7C432–25 7C433–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		20		25		30		35	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		20		25		30		35	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		20		25		30		35	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		10		15		20		25	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		10		15		20		25	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		10		15		20		25	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		10		15		20		25	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		10		15		20		25	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		10		15		20		25	ns
t_{RAE}	Effective Read from Write HIGH		10		15		20		25	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	10		15		20		25		ns
t_{WAF}	Effective Write from Read HIGH		10		15		20		25	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	10		15		20		25		ns
t_{XOL}	Expansion Out LOW Delay from Clock		10		15		20		25	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		10		15		20		25	ns

Switching Characteristics Over the Operating Range[6, 7] (continued)

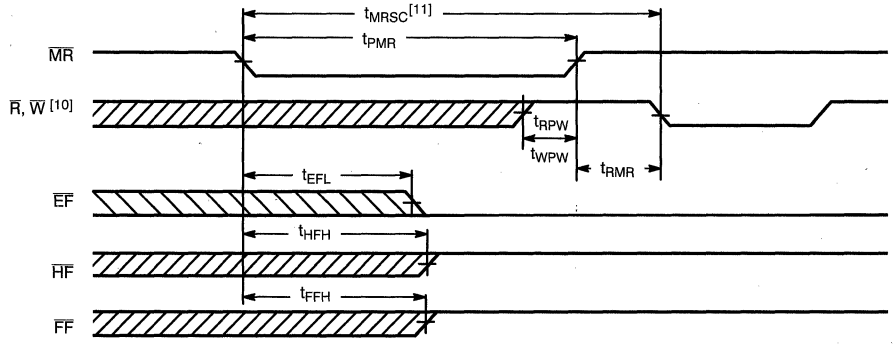
Parameter	Description	7C419–30 7C420–30 7C421–30 7C424–30 7C425–30 7C428–30 7C429–30 7C432–30 7C433–30		7C419–40 7C420–40 7C421–40 7C424–40 7C425–40 7C428–40 7C429–40 7C432–40 7C433–40		7C419–65 7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65 7C432–65 7C433–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		80		ns
t_A	Access Time		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}[5,8]	Read LOW to Low Z	3		3		3		ns
t_{DVR}[8,9]	Data Valid After Read HIGH	5		5		5		ns
t_{HZR}[5,8,9]	Read HIGH to High Z		20		20		20	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{HWZ}[5,8]	Write HIGH to Low Z	5		5		5		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	30		40		65		ns
t_{RTC}	Retransmit Cycle Time	40		50		80		ns
t_{PRT}	Retransmit Pulse Width	30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		30		35		60	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		30		35		60	ns
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		30		35		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		40		65	ns

Switching Waveforms

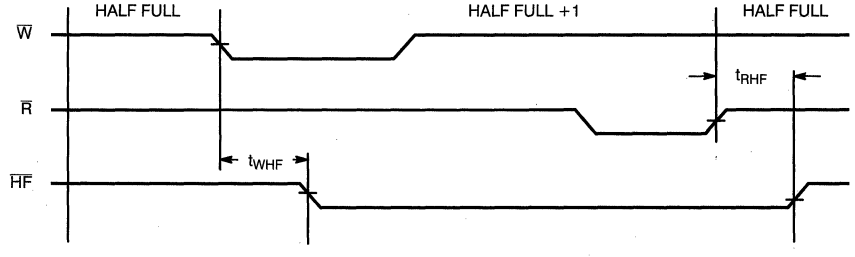
Asynchronous Read and Write



Master Reset



Half-Full Flag

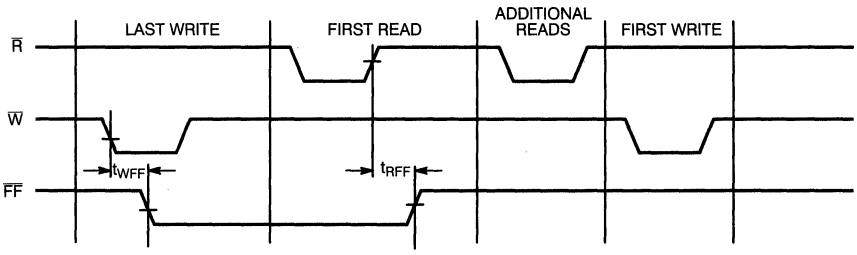


Notes:

10. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
11. $t_{MRSC} = t_{PMR} + t_{RMR}$.

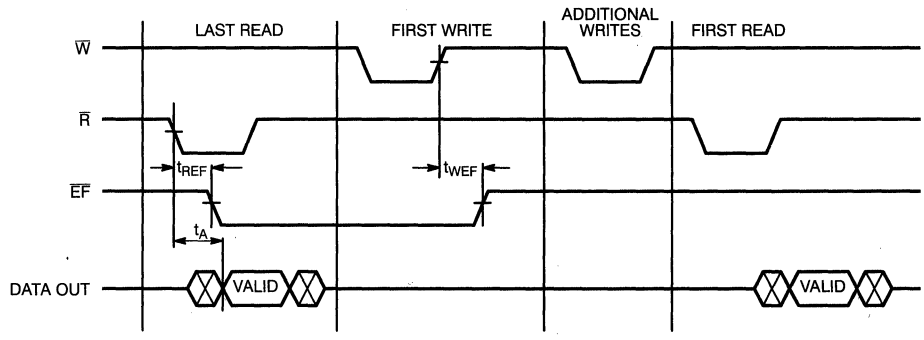
Switching Waveforms (continued)

Last Write to First Read Full Flag



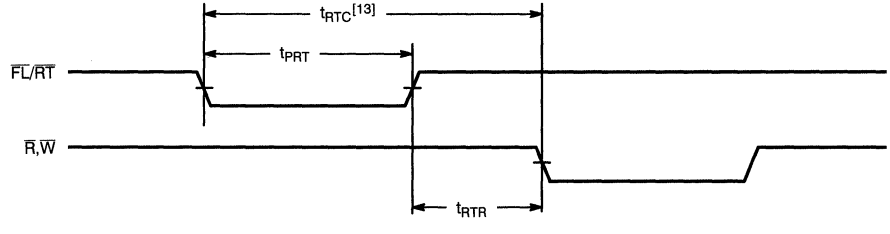
C420-11

Last Read to First Write Empty Flag



C420-12

Retransmit[12]



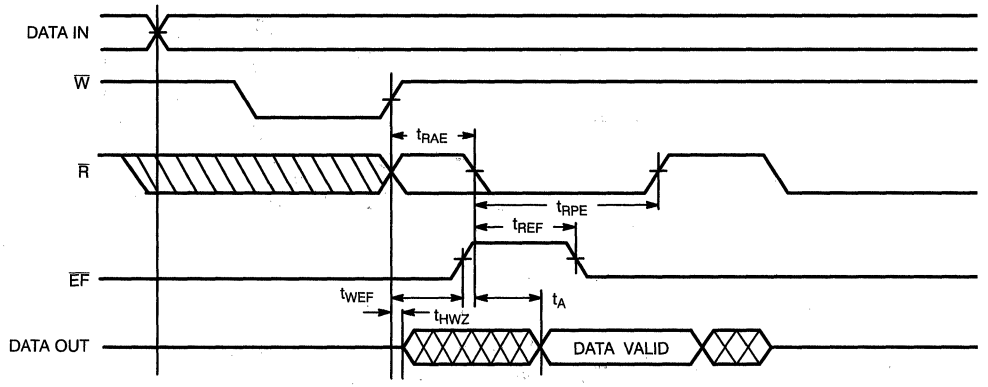
C420-13

Notes:

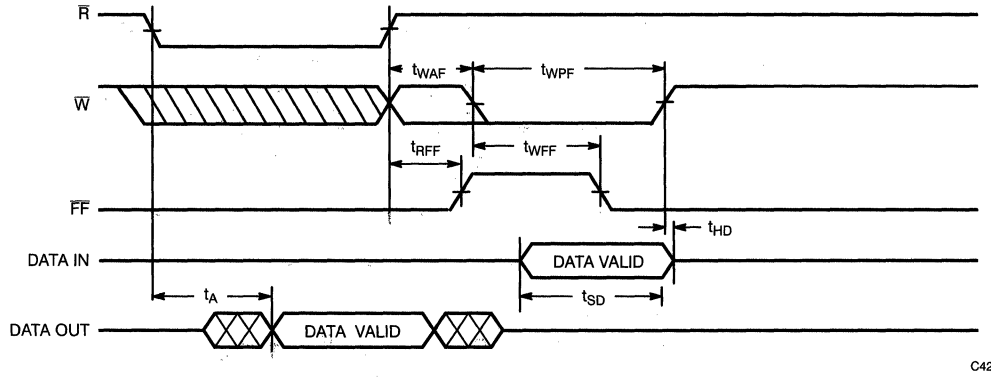
12. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
13. $t_{RTC} = t_{PRT} + t_{RTR}$.

Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode

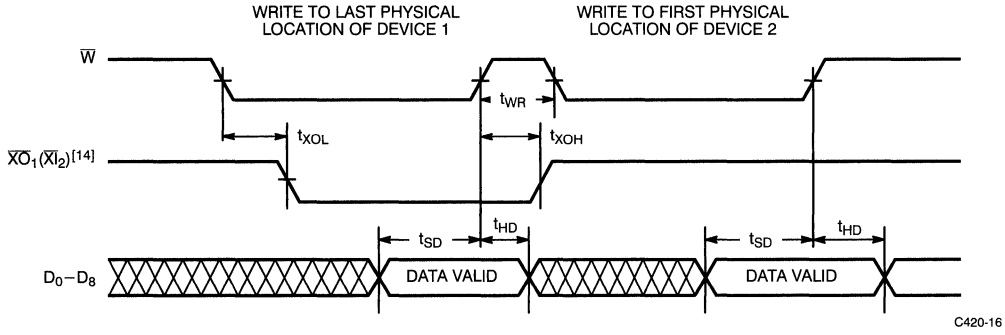


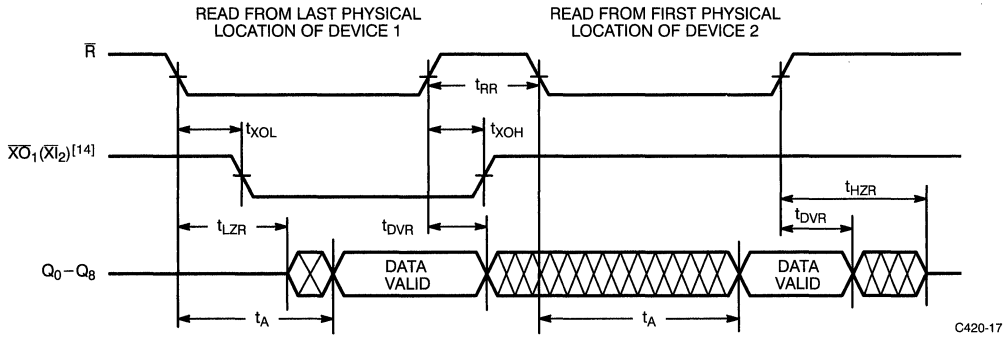
Full Flag and Write Data Flow-Through Mode



Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
14. Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

Architecture

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, CY7C432/3 FIFOs consist of an array of 256, 512, 1024, 2048, 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0 - Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. The rising edge of $\overline{R}$ causes the data outputs to go to the high-impedance state and remain such until a write is performed. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data as well as not previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

Up to the full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

Use of the Empty and Full Flags

In order to achieve the maximum frequency, the flags must be valid at the beginning of the next cycle. However, because they can be updated by either edge of the read of write signal, they must be valid by one-half of a cycle. Cypress FIFOs meet this requirement; some competitors' FIFOs do not.

The reason why the flags are required to be valid by the next cycle is fairly complex. It has to do with the "effective pulse width violation" phenomenon, which can occur at the full and empty boundary conditions, if the flags are not properly used. The empty flag must be used to prevent reading from an empty FIFO and the full flag must be used to prevent writing into a full FIFO.

For example, consider an empty FIFO that is receiving read pulses. Because the FIFO is empty, the read pulses are ignored by the FIFO, and nothing happens. Next, a single word is written into the FIFO, with a signal that is asynchronous to the read signal. The (internal) state machine in the FIFO goes from empty to empty+1. However, it does this asynchronously with respect to the read signal, so that it cannot be determined what the effective pulse width of the read signal is, because the state machine does not look at the read signal until it goes to the empty+1 state. In a similar manner, the minimum write pulse width may be violated by attempting to write into a full FIFO, and asynchronously performing a read. The empty and full flags are used to avoid these effective pulse width violations, but in order to do this and operate at the maximum frequency, the flag must be valid at the beginning of the next cycle.

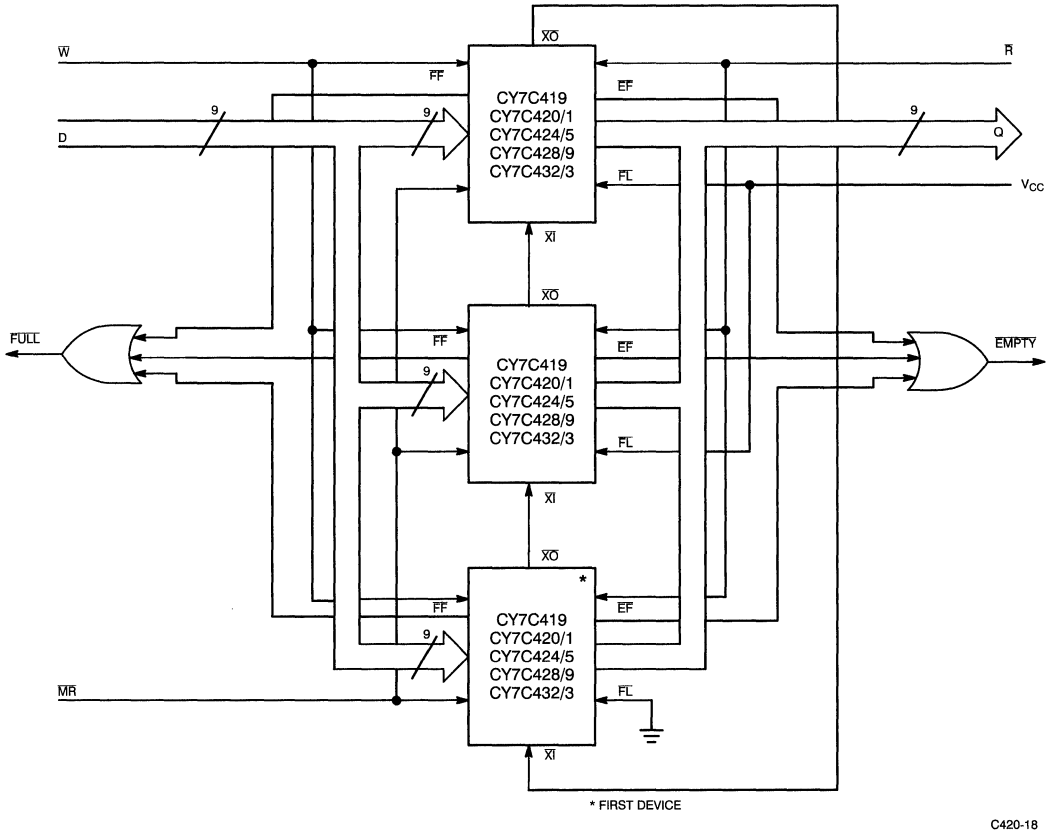


Figure 1. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C419–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C419–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C419–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C419–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C419–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C419–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–40VC	V21	28-Lead (300-Mil) Molded SOJ	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C419–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C419–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

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Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C420–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
25	CY7C420–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C420–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C420–30PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C420–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C420–40PC	P15	28-Lead (600-Mil) Molded DIP	Commerical
	CY7C420–40PI	P15	28-Lead (600-Mil) Molded DIP	Industry
	CY7C420–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C420–65PC	P15	28-Lead (600-Mil) Molded DIP	Commerical
	CY7C420–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C421–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C421–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C421–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C421–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C421–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C421-40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C421-65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421-40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421-65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421-65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421-65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421-65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421-65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C424-20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
25	CY7C424-25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424-25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424-25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C424-30PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424-30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424-30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C424-40PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424-40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424-40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C424-65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424-65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424-65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C425–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C425–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C425–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C425–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C425–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C425–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C425–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C428–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
25	CY7C428–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C428–30PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C428–40PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C428–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C429–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C429–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C429–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C429–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C429–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C429–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–40VC	V21	28-Lead (300-Mil) Molded SOJ	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C429–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C429–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C432–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
30	CY7C432–30PC	P15	28-Lead (600-Mil) Molded DIP	Commerical
	CY7C432–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C432–40PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C432–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C432–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C432–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C433–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C433–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C433–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C433–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C433–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C433–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C433–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{CC1}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

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CY7C4421/4201/4211/4221
CY7C4231/4241/4251

64/256/512/1K/2K/4K/8K x 9 Synchronous FIFOs

Features

- 64 x 9 (CY7C4421)
- 256 x 9 (CY7C4201)
- 512 x 9 (CY7C4211)
- 1K x 9 (CY7C4221)
- 2K x 9 (CY7C4231)
- 4K x 9 (CY7C4241)
- 8K x 9 (CY7C4251)
- **High-speed 100-MHz operation (10 ns read/write cycle time)**
- **Pin compatible and functionally equivalent to IDT72421, 72201, 72211, 72221, 72231, 72241**
- **Fully asynchronous and simultaneous read and write operation**
- **Four status flags: Empty, Full, and programmable Almost Empty/Almost Full**
- **Expandable in width**
- **Low operating power**
  I_{CC2} = 50 mA
- **Output Enable ($\overline{OE}$) pin**
- **32-pin PLCC/TQFP**

Functional Description

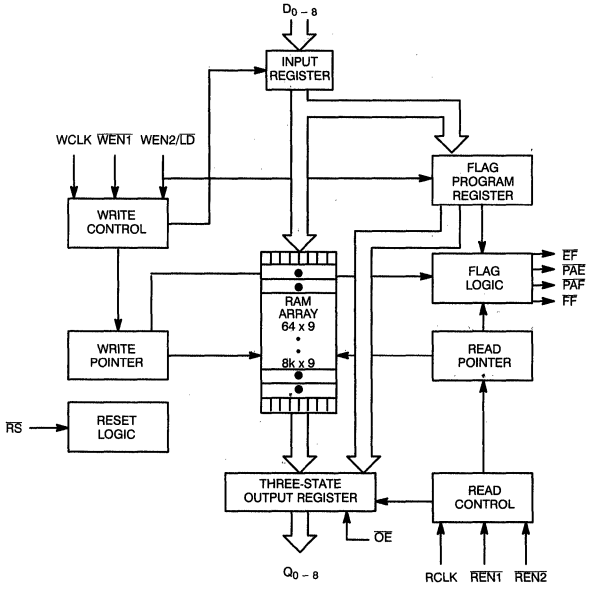
The CY7C42X1 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 9 bits wide. The CY7C42X1 are pin-compatible to IDT722X1. The CY7C42X1 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C42X1 has an output enable pin ($\overline{OE}$). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

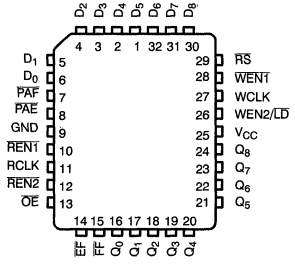
Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram

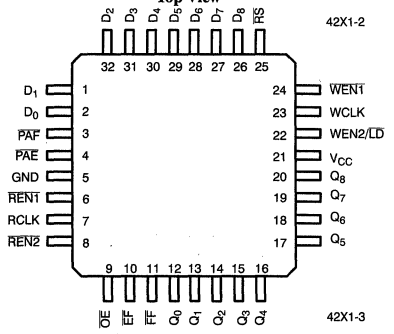


Pin Configuration

PLCC
Top View



TQFP
Top View



Functional Description (continued)

The CY7C42X1 provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty-7 and Full-7.

The flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.65µ N-Well CMOS technology. Input ESD protection is greater than 4001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C42X1–10	7C42X1–15	7C42X1–25	7C42X1–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Operating Current (I_{CC5}) (mA)	Commercial	50	50	50	50
	Industrial	70	70	70	70

	CY7C4421	CY7C4201	CY7C4211	CY7C4221	CY7C4231	CY7C4241	CY7C4251
Density	64 x 9	256 x 9	512 x 9	1K x 9	2K x 9	4K x 9	8K x 9

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	Data Inputs for 9-bit bus
Q_{0-8}	Data Outputs	O	Data Outputs for 9-bit bus
$\overline{WEN1}$	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2 Load	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or lead the programmable flag offsets.
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	Enables the device for Read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

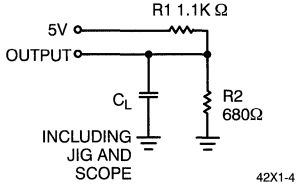
Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C42X1–10 Min.	7C42X1–10 Max.	7C42X1–15 Min.	7C42X1–15 Max.	7C42X1–25 Min.	7C42X1–25 Max.	7C42X1– 35 Min.	7C42X1– 35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{CC1}[4]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		150		130		75		60	mA
			Ind		170		150		95		80	mA
I_{CC2}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		50		50		50		50	mA
			Ind		70		70		70		70	mA
I_{SB}[6]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		28		25		22	mA
			Ind		40		38		35		35	mA

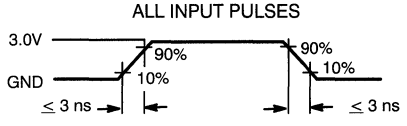
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[8, 9]

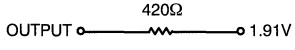


42X1-4



42X1-5

Equivalent to: THÉVENIN EQUIVALENT



Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Test no more than one output at a time for not more than one second.
4. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
5. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
6. All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
7. Tested initially and after any design or process changes that may affect these parameters.
8. C_L = 30 pF for all AC parameters except for t_{OHZ}.
9. C_L = 5 pF for t_{OHZ}.

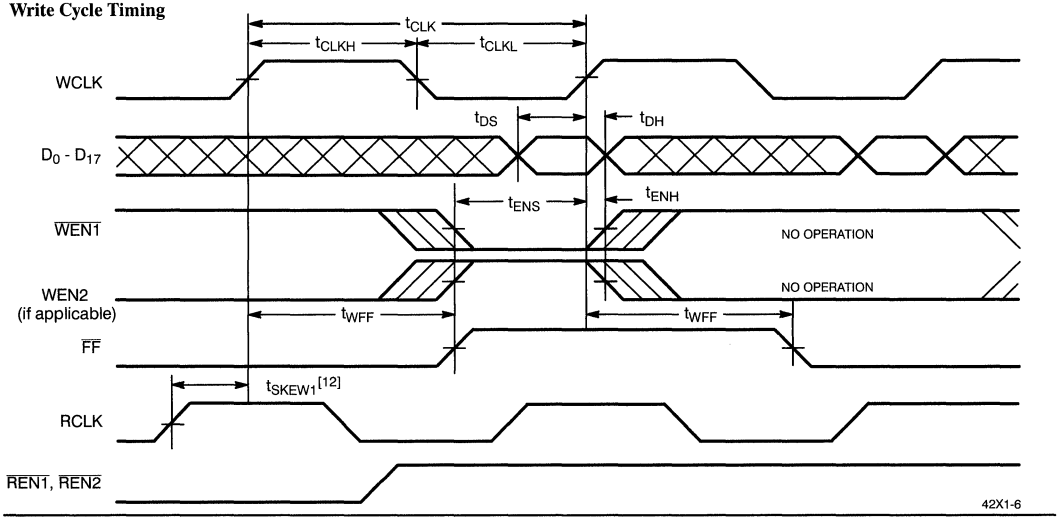
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X1–10		7C42X1–15		7C42X1–25		7C42X1–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	ns
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[10]	10		15		25		35		ns
t_{RSS}	Reset Set-Up Time	8		10		15		20		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{OLZ}	Output Enable to Output in Low Z[11]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[11]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	10		15		18		20		ns

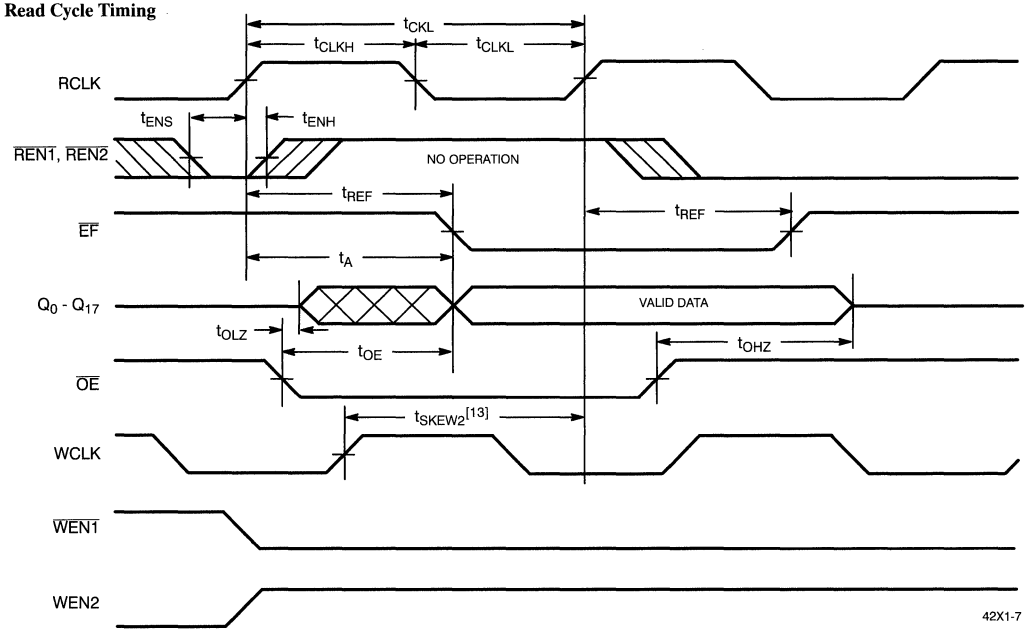
Notes:
10. Pulse widths less than minimum values are not allowed.
11. Values guaranteed by design, not currently tested.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

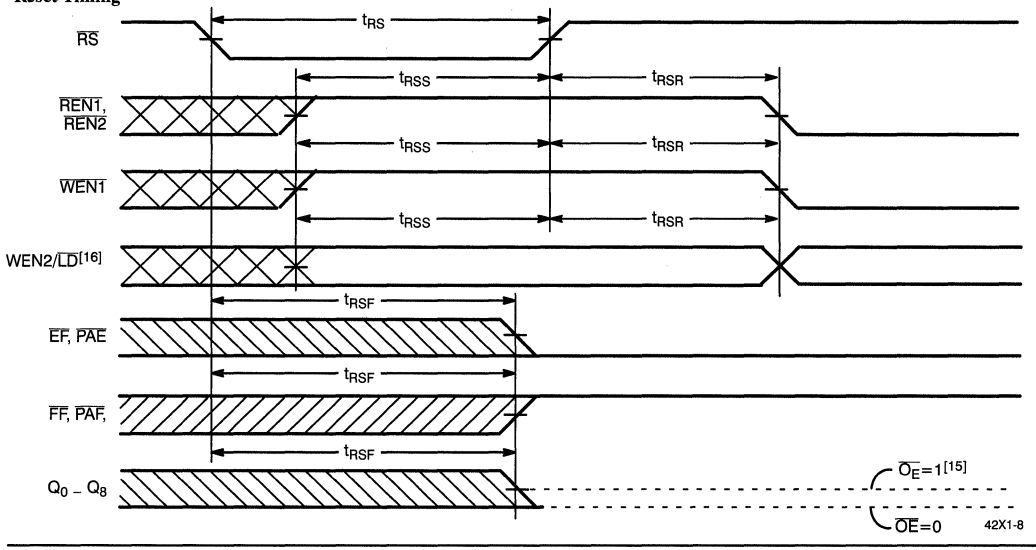


Notes:

12. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.
13. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Switching Waveforms (continued)

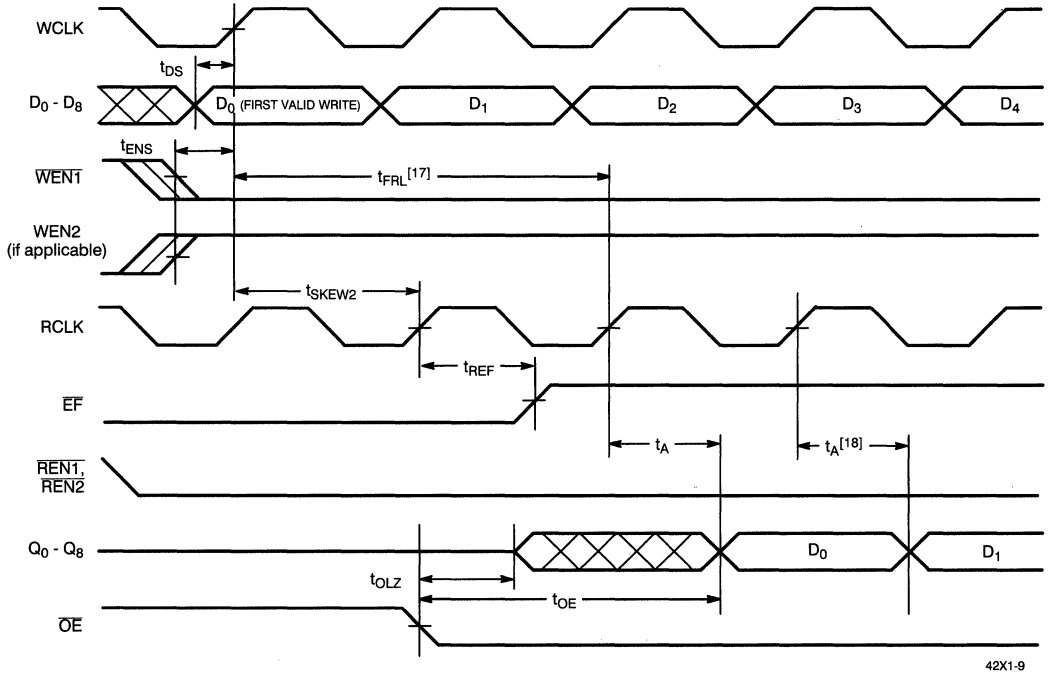
Reset Timing[14]



Notes:
14. The clocks (RCLK, WCLK) can be free-running during reset.
15. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
16. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

Switching Waveforms (continued)

First Data Word Latency after Reset with Simultaneous Read and Write

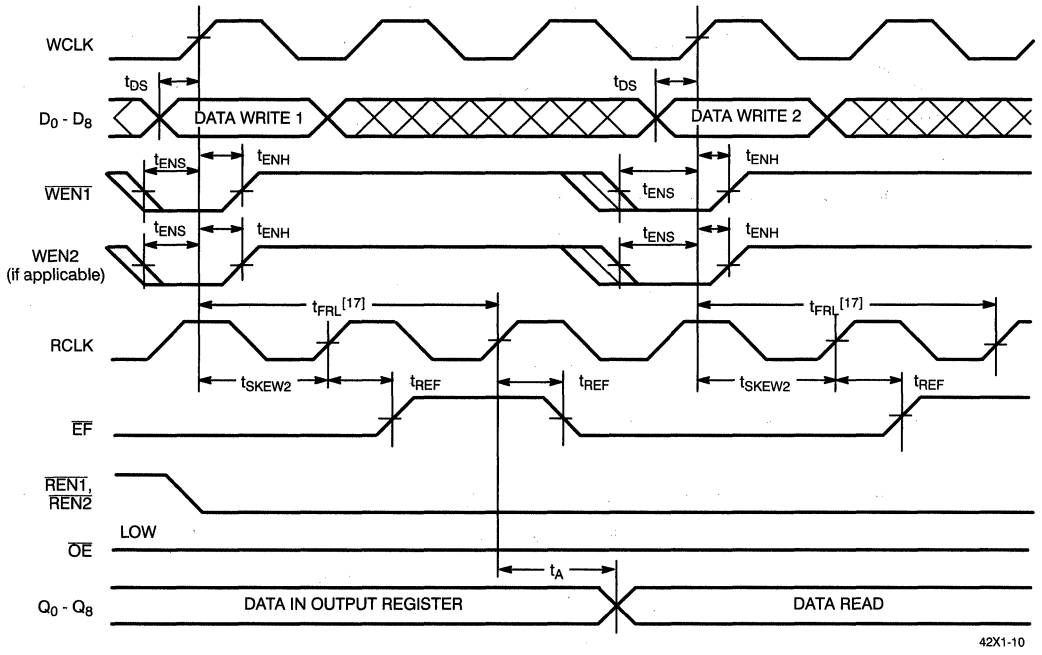


Notes:

17. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
18. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

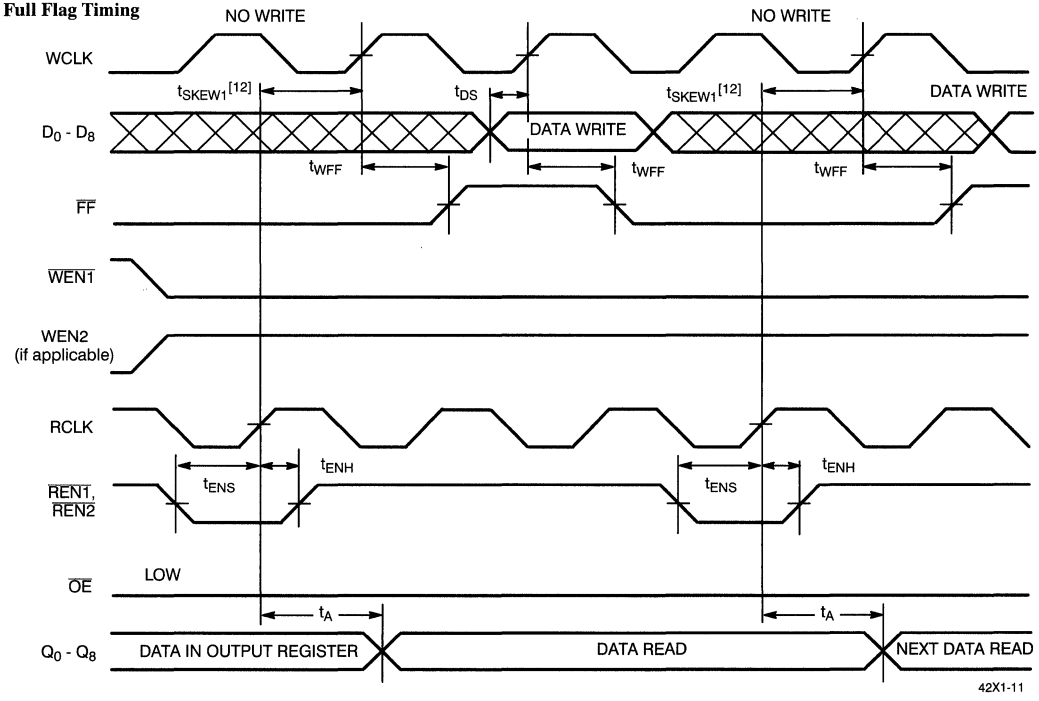
Switching Waveforms (continued)

Empty Flag Timing



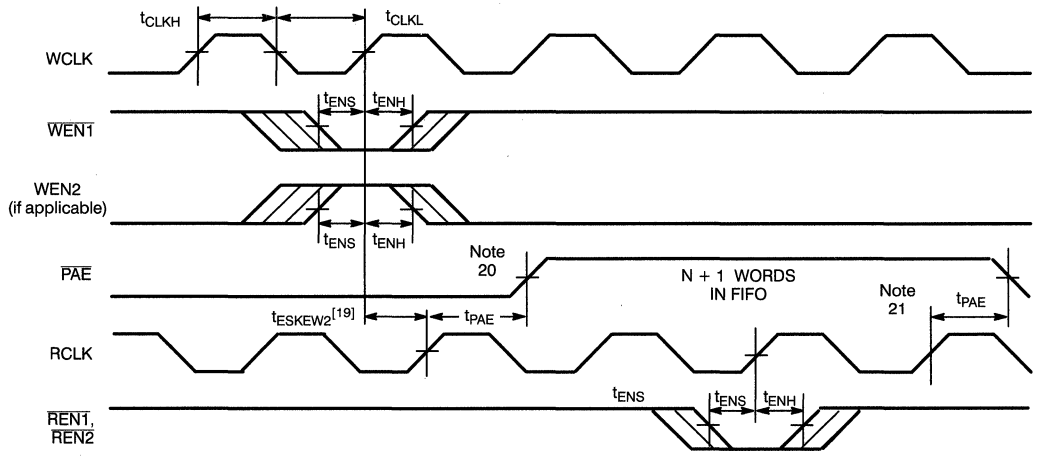
Switching Waveforms (continued)

Full Flag Timing

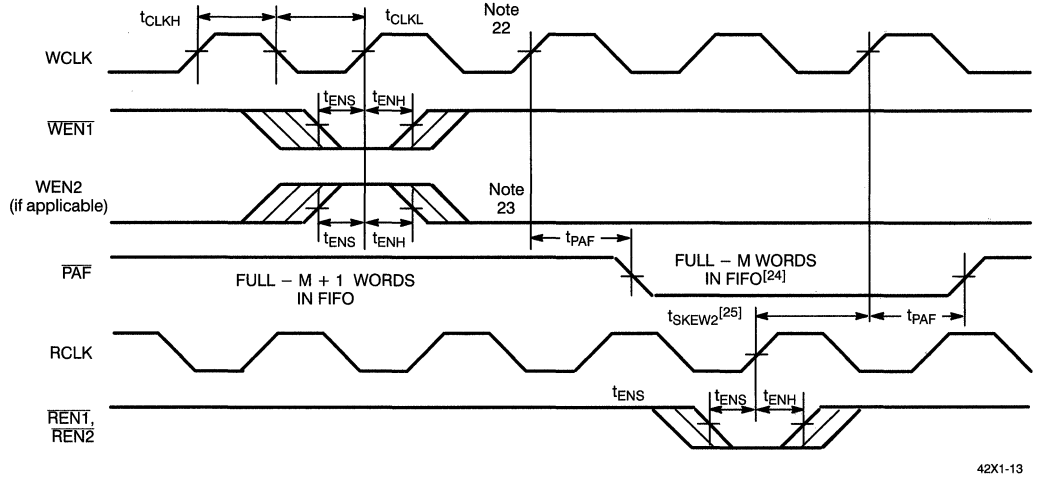


Switching Waveforms (continued)

Programmable Almost Empty Flag Timing



Programmable Almost Full Flag Timing

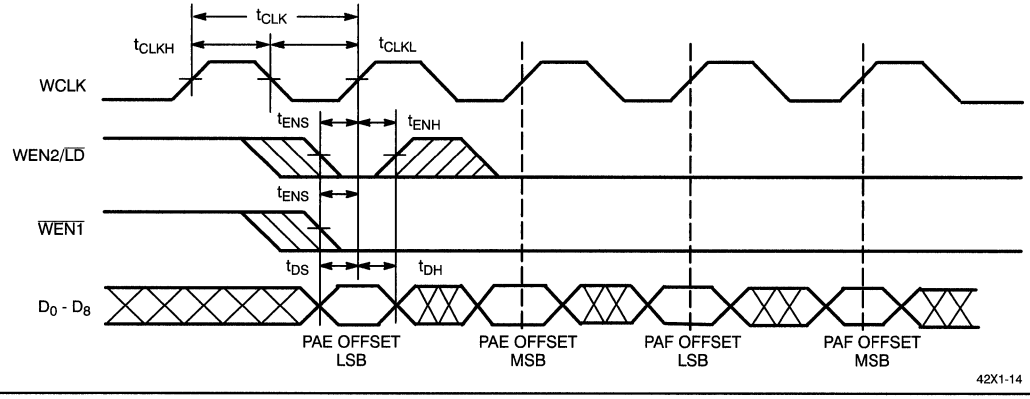


Notes:

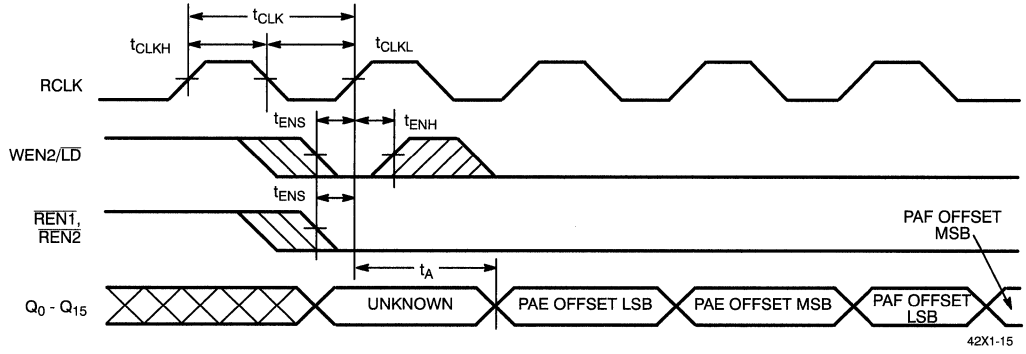
19. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
20. PAE offset – n.
21. If a read is preformed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
22. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
23. PAF offset = m.
24. 64–m words for CY7C4421, 256–m words in FIFO for CY7C4201, 512–m words for CY7C4211, 1024–m words for CY7C4221, 2048–m words for CY7C4231, 4096–m words for CY7C4241, 8192–m words for CY7C4251.
25. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising.

Switching Waveforms (continued)

Write Programmable Registers



Read Programmable Registers



Architecture

The CY7C42X5 consists of an array of 64 to 8K words of 9 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN1}$, $\overline{REN2}$, $\overline{WEN1}$, WEN2, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and $\overline{REN2}$ signals are active LOW, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN1}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-8} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$) – If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data

is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/$\overline{LD}$) – This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

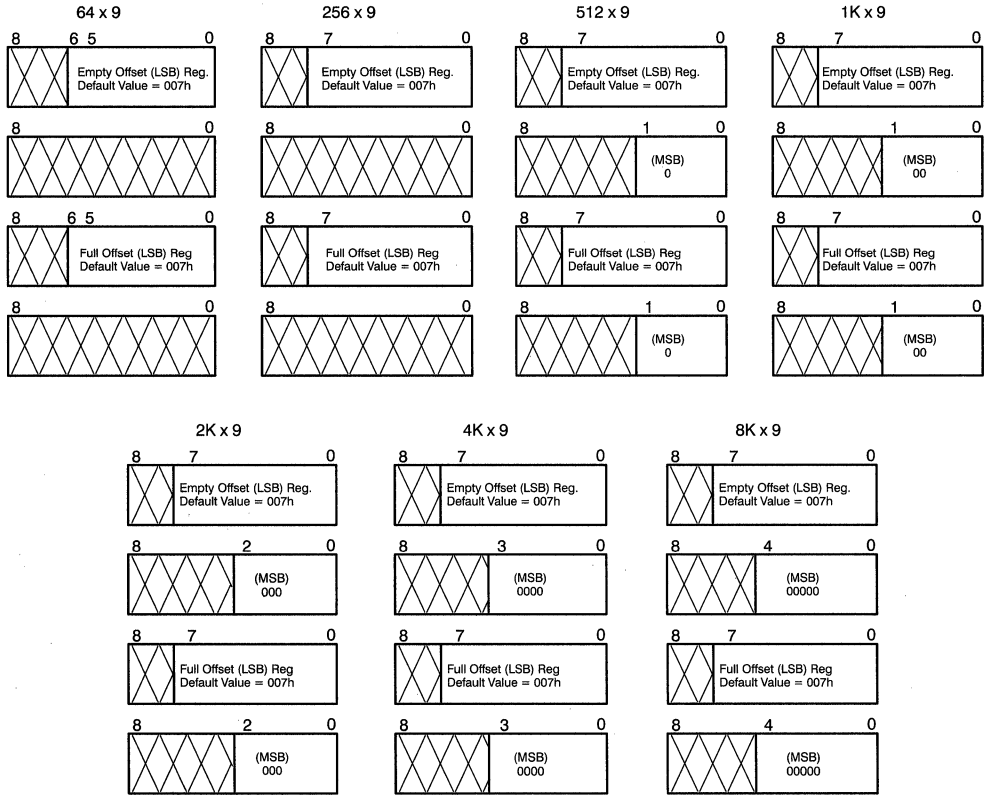


Figure 1. Offset Register Location and Default Values

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.

Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

$\overline{LD}$	$\overline{WEN}$	WCLK[26]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4421. (64−m), CY7C4201 (256−m), CY7C4211 (512−m), CY7C4221 (1K−m), CY7C4231 (2K−m), CY7C4241 (4K−m), and CY7C4251 (8K−m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 2. Status Flags

Number of Words in FIFO						
CY7C4421	CY7C4201	CY7C4211	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[27]	1 to n[27]	1 to n[27]	H	H	L	H
(n+1) to 32	(n+1) to 128	(n+1) to 256	H	H	H	H
33 to (64−(m+1))	129 to (256−(m+1))	257 to (512−(m+1))	H	H	H	H
(64−m)[28] to 63	(256−m)[28] to 255	(512−m)[28] to 511	H	L	H	H
64	256	512	L	L	H	H

Number of Words in FIFO							
CY7C4221	CY7C4231	CY7C4241	CY7C4251	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	H	H	L	L
1 to n[27]	1 to n[27]	1 to n[27]	1 to n[27]	H	H	L	H
(n+1) to 512	(n+1) to 1024	(n+1) to 2048	(n+1) to 4096	H	H	H	H
513 to (1024 −(m+1))	1025 to (2048 −(m+1))	2049 to (4096 −(m+1))	4097 to (8182 −(m+1))	H	H	H	H
(1024−m)[28] to 1023	(2048−m)[28] to 2047	(4096−m)[28] to 4095	(8182−m)[28] to 8181	H	L	H	H
1024	2048	4096	8182	L	L	H	H

Notes:

26. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
27. n = Empty Offset (n=7 default value).
28. m = Full Offset (m=7 default value).

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See *Figure 2*). In this configuration, the Write Enable 2/Load ($\overline{WEN2/LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full, $\overline{PAE}$, and $\overline{PAF}$ are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN1}$ and $\overline{WEN2/LD}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

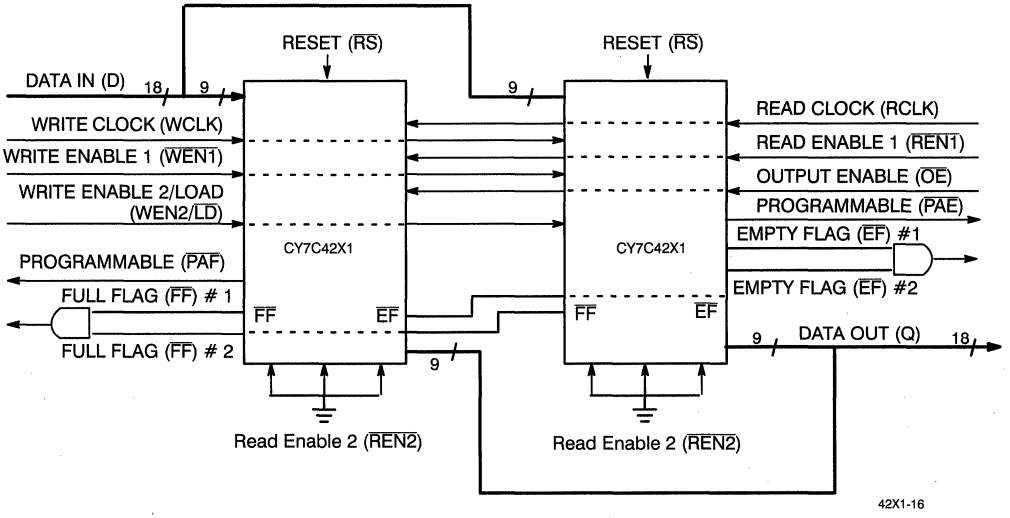


Figure 2. Block Diagram of 64 x 18/256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18/8192 x 18 Synchronous FIFO Memory Used in a Width Expansion Configuration

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4421-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4421-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4421-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4421-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4201-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4201-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4201-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4201-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4211–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4211–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4211–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4211–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4221–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4221–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4221–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4221–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4231–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4231–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4231–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4231–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4241–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4241–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4241–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4241–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4251–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4251–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4251–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4251–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Document #: 38–00419

CY7C4425/4205/4215
CY7C4225/4235/4245

64, 256, 512, 1K, 2K, 4K x 18 Synchronous FIFOs

Features

- 64 x 18 (CY7C4425)
- 256 x 18 (CY7C4205)
- 512 x 18 (CY7C4215)
- 1K x 18 (CY7C4225)
- 2K x 18 (CY7C4235)
- 4K x 18 (CY7C4245)
- **High-speed 100-MHz operation (10 ns read/write cycle time)**
- **Pin compatible and functional equivalent to IDT72425, 72205, 72215, 72225, 72235, 72245**
- **Additional features**
  - **— Retransmit**
  - **— Synchronous Almost Empty/Full flags**
- **Fully asynchronous and simultaneous read and write operation**
- **Five status flags: Empty, Full, Half Full, and programmable Almost Empty/Almost Full**
- **Low operating power**
  - **— I_{CC2} = 100 mA**
- **Output Enable ($\overline{OE}$) pin**
- **68-pin PLCC and 64-pin TQFP**

Functional Description

The CY7C42X5 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide and are pin/functionally compatible to IDT722x5LB. The CY7C42X5 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a write enable pin ($\overline{WEN}$).

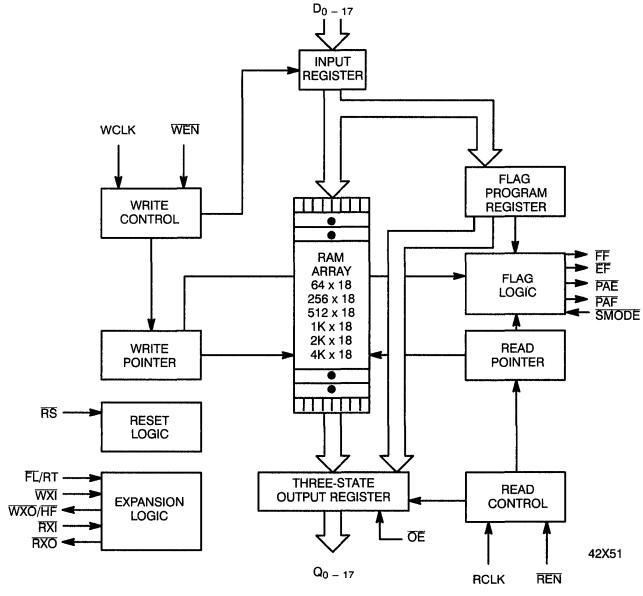
When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and a read enable pin ($\overline{REN}$). In addition, the CY7C42X5 have an output enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

Depth expansion is possible using the cascade input ($\overline{WXI}$, $\overline{RXI}$), cascade output ($\overline{WXO}$, $\overline{RXO}$), and First Load ($\overline{FL}$) pins. The $\overline{WXO}$ and $\overline{RXO}$ pins are connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the next device, and the $\overline{WXO}$ and $\overline{RXO}$ pins of the last device should be connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}.

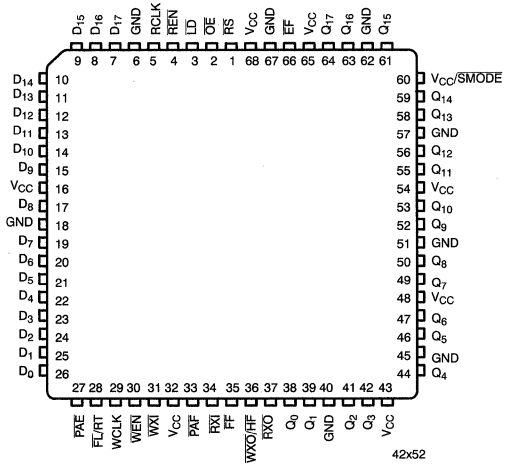
5

Logic Block Diagram

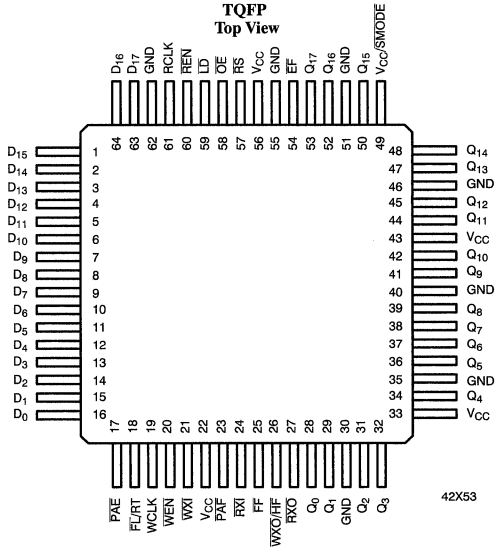


Pin Configurations

PLCC
Top View



TQFP
Top View



Functional Description (continued)

The CY7C42X5 provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see *Table 2*). The Half Full flag shares the $\overline{WXO}$ pin. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{WXO}$) information that is used to signal the next FIFO when it will be activated.

The Empty and Full flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags will remain valid from one clock cycle to the next. As mentioned previously, the Almost Empty/Almost Full flags become synchronous if the $V_{CC}/\overline{SMODE}$ is tied to V_{SS}. All configurations are fabricated using an advanced 0.65μ N-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C42X5–10	7C42X5–15	7C42X5–25	7C42X5–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Operating Current (I_{CC2}) (mA)	Commercial	100	100	100	100
	Industrial	120	120	120	120

	CY7C4425	CY7C4205	CY7C4215	CY7C4225	CY7C4235	CY7C4245
Density	64 x 18	256 x 18	512 x 18	1K x 18	2K x 18	4K x 18

Pin Definitions

Signal Name	Description	I/O	Function
D_{0-17}	Data Inputs	I	Data inputs for an 18-bit bus
Q_{0-17}	Data Outputs	O	Data outputs for an 18-bit bus
$\overline{WEN}$	Write Enable	I	Enables the WCLK input
$\overline{REN}$	Read Enable	I	Enables the RCLK input
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO/HF}$	Write Expansion Out/Half Full Flag	O	Dual-Mode Pin: Single device or width expansion – Half Full status flag. Cascaded – Write Expansion Out signal, connected to $\overline{WXI}$ of next device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, D_{0-17} (O_{0-17}) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}/RT$	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded – The first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC}. In standard mode of width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded – Tied to V_{SS}. Retransmit function is also available in standalone mode by strobing RT.
$\overline{WXI}$	Write Expansion Input	I	Cascaded – Connected to $\overline{WXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXI}$	Read Expansion Input	I	Cascaded – Connected to $\overline{RXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXO}$	Read Expansion Output	O	Cascaded – Connected to $\overline{RXI}$ of next device.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual-Mode Pin Asynchronous Almost Empty/Almost Full flags – tied to V_{CC}. Synchronous Almost Empty/Almost Full flags – tied to V_{SS}. (Almost Empty synchonized to RCLK, Almost Full synchronized to WCLK.)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

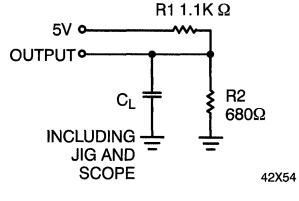
Electrical Characteristics Over the Operating Range[2]

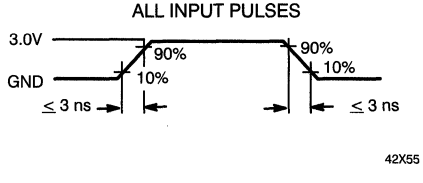
Parameter	Description	Test Conditions		7C42X5–10 Min.	7C42X5–10 Max.	7C42X5–15 Min.	7C42X5–15 Max.	7C42X5–25 Min.	7C42X5–25 Max.	7C42X5– 35 Min.	7C42X5– 35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[3]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[3]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{CC1}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		230		200		115		90	mA
			Ind		250		220		135		110	mA
I_{CC2}[6]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		100		100		100		100	mA
			Ind		120		120		120		120	mA
I_{SB}[7]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		28		25		25	mA
			Ind		40		38		35		35	mA

Capacitance[8]

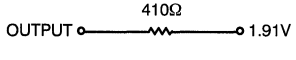
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[9, 10]





Equivalent to: THÉVENIN EQUIVALENT



Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
4. Test no more than one output at a time for not more than one second.
5. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
6. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
7. All input signals are connected to V_{CC}. All outputs are unloaded.
8. Tested initially and after any design or process changes that may affect these parameters.
9. C_L = 30 pF for all AC parameters except for t_{OHZ}.
10. C_L = 5 pF for t_{OHZ}.

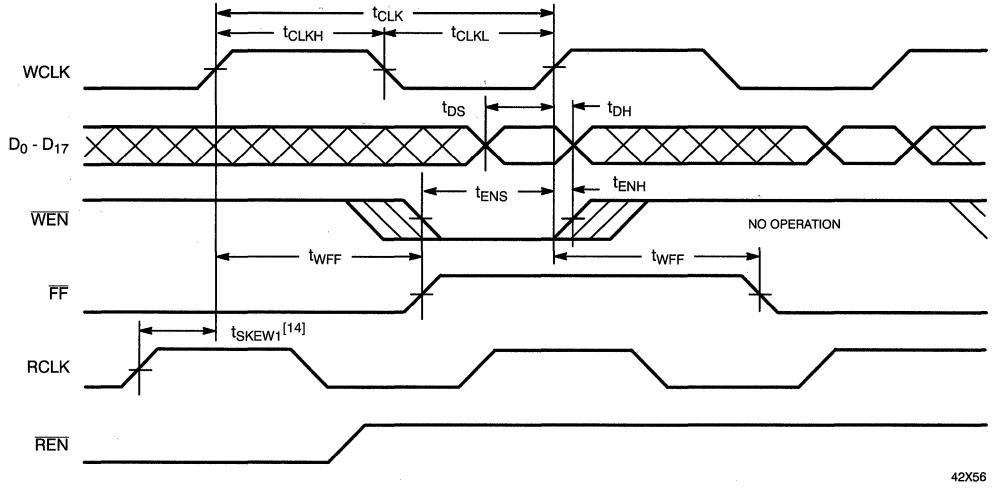
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X5–10		7C42X5–15		7C42X5–25		7C42X5–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	MHz
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[11]	10		15		25		35		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{PRT}	Retransmit Pulse Width	12		15		25		35		ns
t_{RTR}	Retransmit Recovery Time	12		15		25		35		ns
t_{OLZ}	Output Enable to Output in Low Z[12]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[12]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
$t_{PAFasynch}$	Clock to Programmable Almost-Full Flag[13] (Asynchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAFsynch}$	Clock to Programmable Almost-Full Flag (Synchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
$t_{PAEasynch}$	Clock to Programmable Almost-Empty Flag[13] (Asynchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAEsynch}$	Clock to Programmable Almost-Full Flag (Synchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
t_{HF}	Clock to Half-Full Flag		12		16		20		25	ns
t_{XO}	Clock to Expansion Out		7		10		15		20	ns
t_{XI}	Expansion in Pulse Width	3		6.5		10		14		ns
t_{XIS}	Expansion in Set-Up Time	4.5		5		10		15		ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	5		6		10		12		ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags.	10		15		18		20		ns

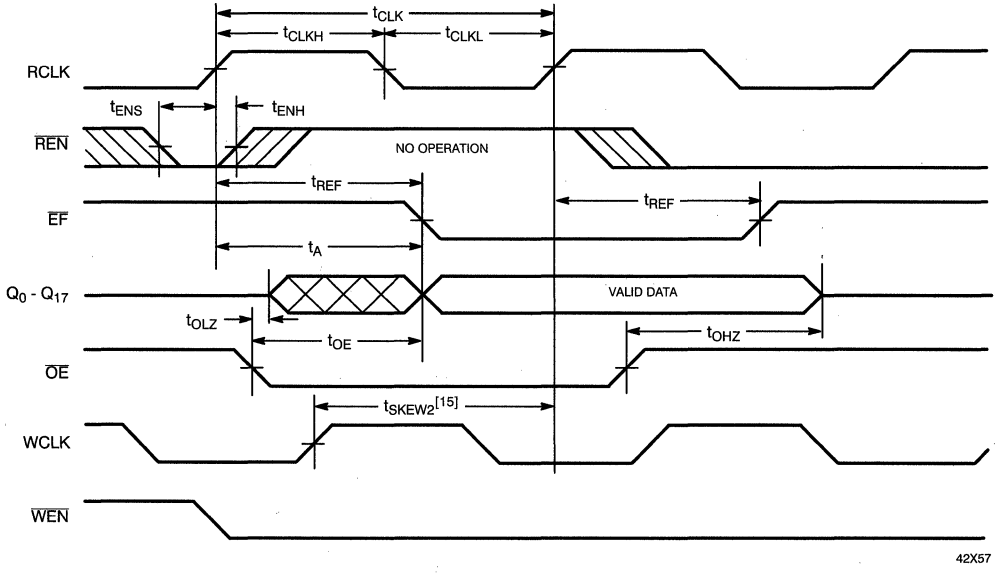
Notes:
11. Pulse widths less than minimum values are not allowed.
12. Values guaranteed by design, not currently tested.
13. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write will not be valid until 5 ns + $t_{PAF(E)}$.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

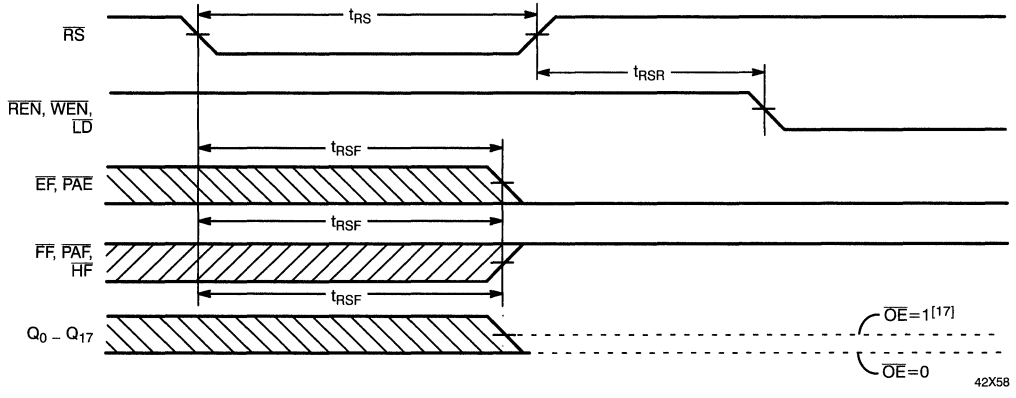


Notes:

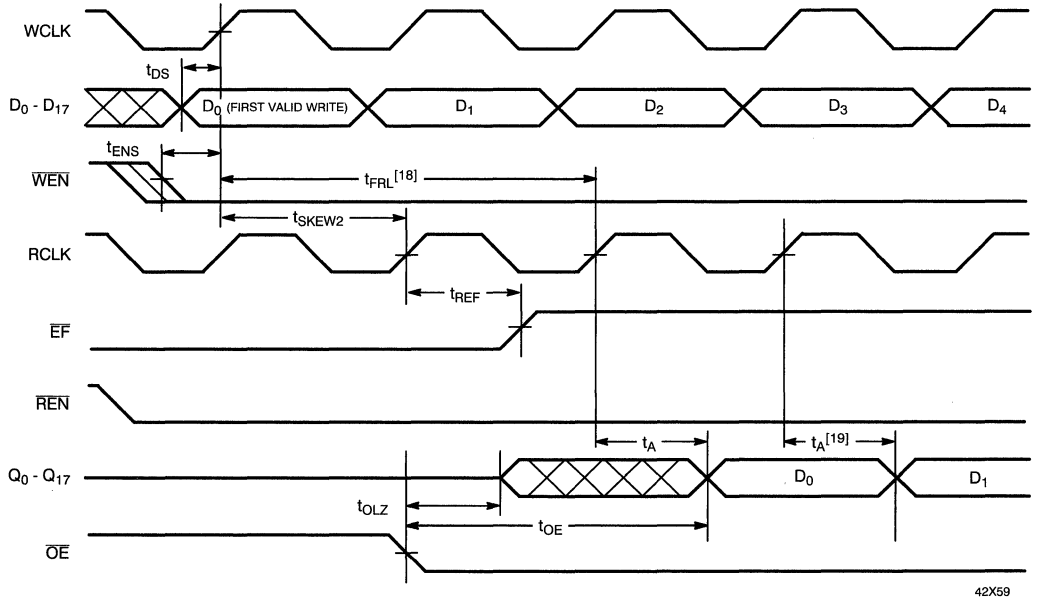
14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.
15. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Switching Waveforms (continued)

Reset Timing[16]



First Data Word Latency after Reset with Simultaneous Read and Write

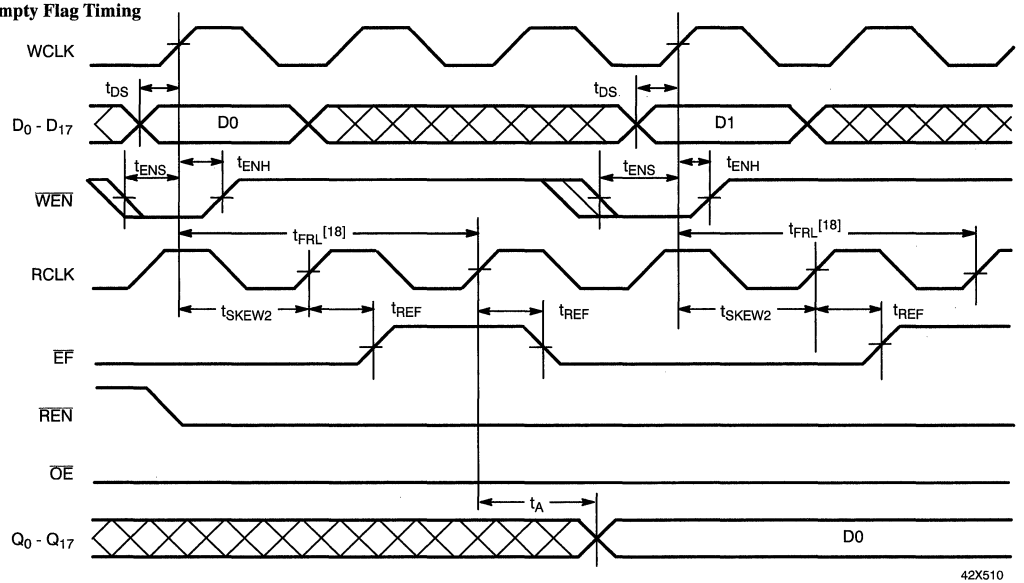


Notes:

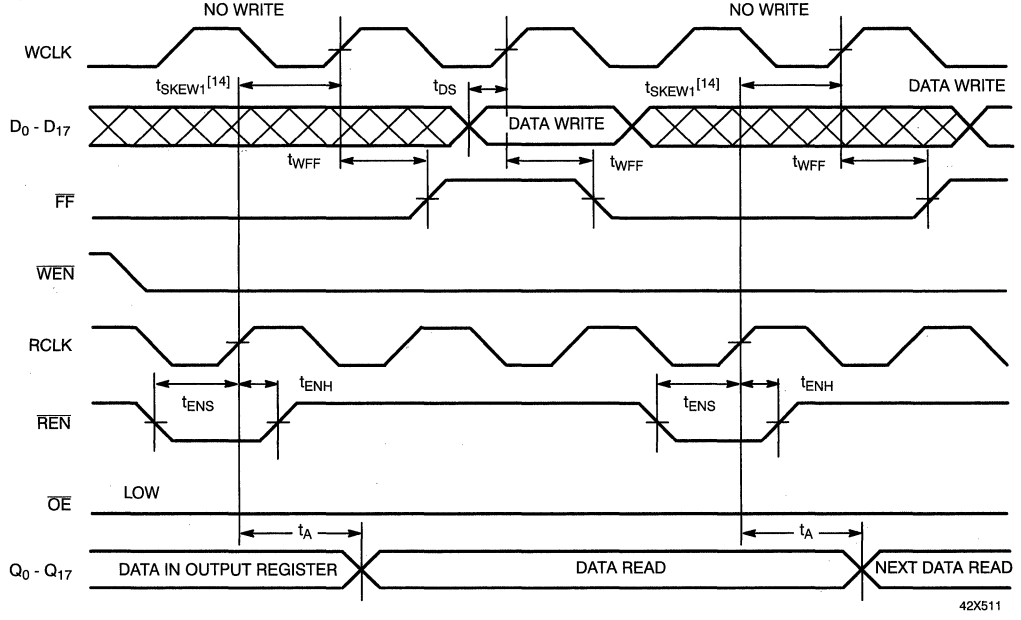
16. The clocks (RCLK, WCLK) can be free-running during reset.
17. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
18. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
19. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Switching Waveforms (continued)

Empty Flag Timing

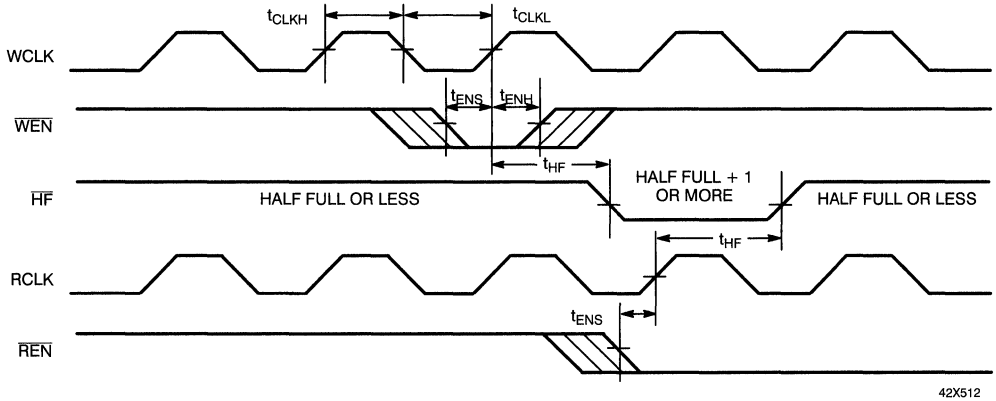


Full Flag Timing

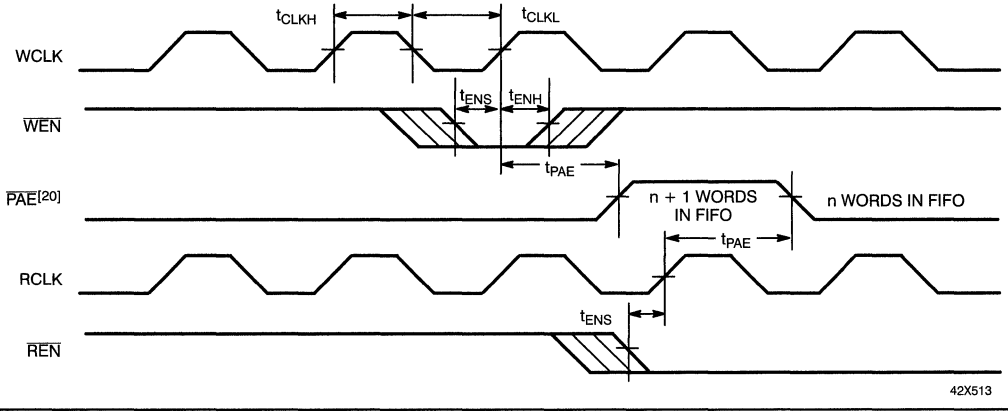


Switching Waveforms (continued)

Half-Full Flag Timing



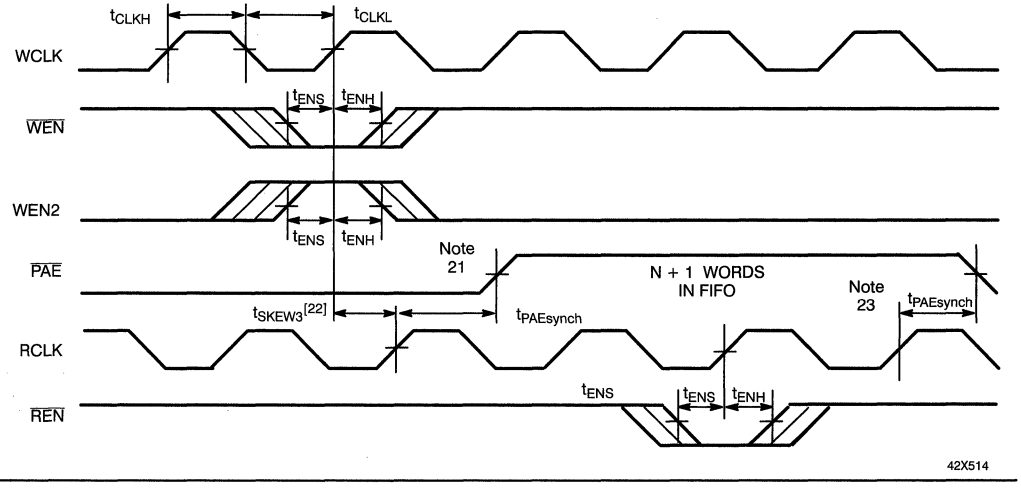
Programmable Almost Empty Flag Timing



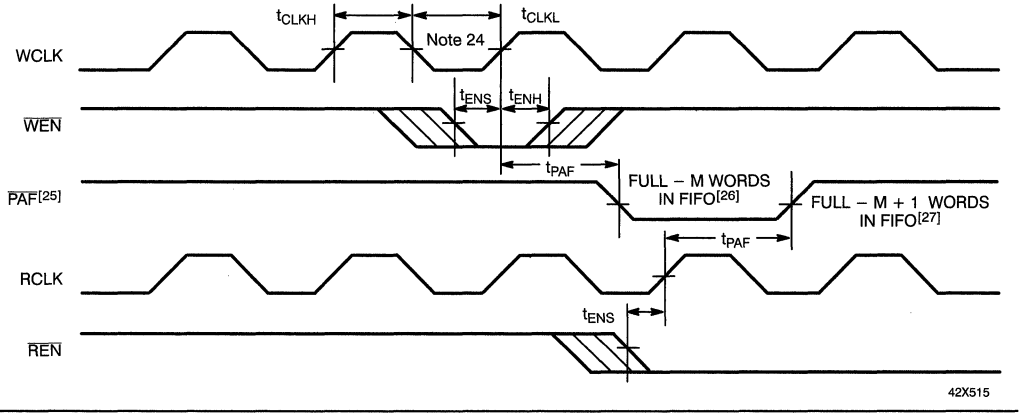
Note:
20. $\overline{PAE}$ is offset = n. Number of data words into FIFO already = n.

Switching Waveforms (continued)

Programmable Almost Empty Flag Timing (applies only in $\overline{\text{SMODE}}$ ($\overline{\text{SMODE}}$ is LOW))



Programmable Almost Full Flag Timing

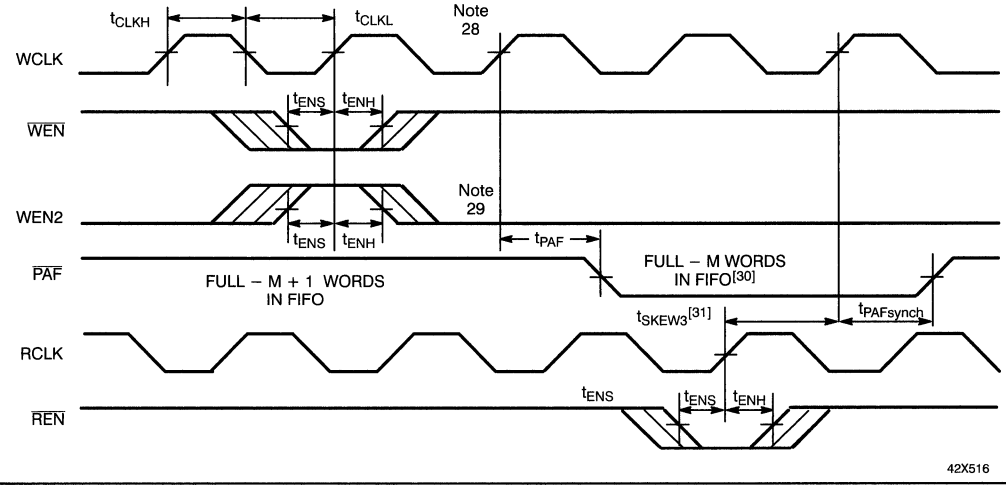


Notes:

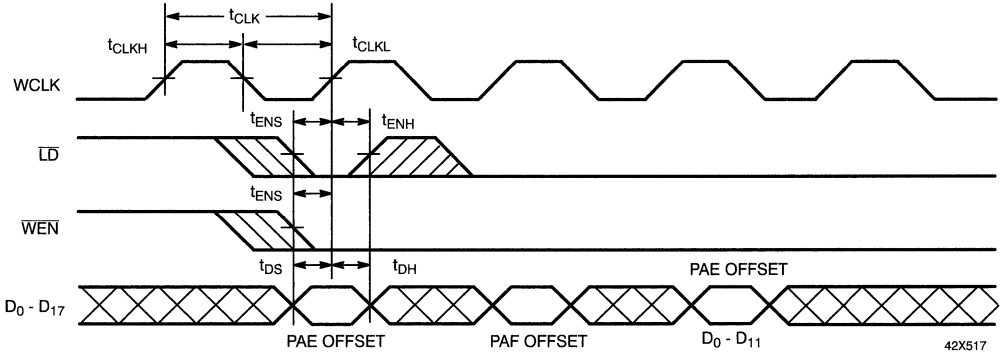
21. PAE offset – n.
22. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{\text{PAE}}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3}, then $\overline{\text{PAE}}$ may not change state until the next RCLK.
23. If a read is preformed on this rising edge of the read clock, there will be Empty + (n−1) words in the FIFO when $\overline{\text{PAE}}$ goes LOW.
24. PAF offset = m. Number of data words written into FIFO already = 64 – m + 1 for the CY7C4425, 256 – m + 1 for the CY7C4205, 512 – m + 1 for the CY7C4215. 1024 – m + 1 for the CY7C4225, 2048 – m + 1 for the CY7C4235, and 4096 – m + 1 for the CY7C4245.
25. PAF is offset = m.
26. 64 – m words in CY7C4425, 256 – m words inCY7C4205, 512 – m word in CY7C4215. 1024 – m words in CY7C4225, 2048 – m words in CY7C4235, and 4096 – m words in CY7C4245.
27. 64 – m + 1 words in CY7C4425, 256 – m + 1 words in CY7C4205, 512 – m + 1 words in CY7C4215. 1024 – m + 1 CY7C4225, 2048 – m + 1 words in CY7C4235, and 4096 – m + 1 words inCY7C4245.

Switching Waveforms (continued)

Programmable Almost Full Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))



Write Programmable Registers

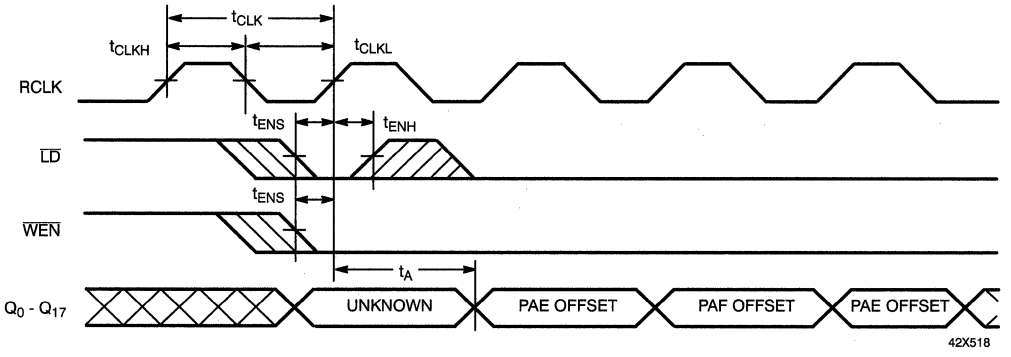


Notes:

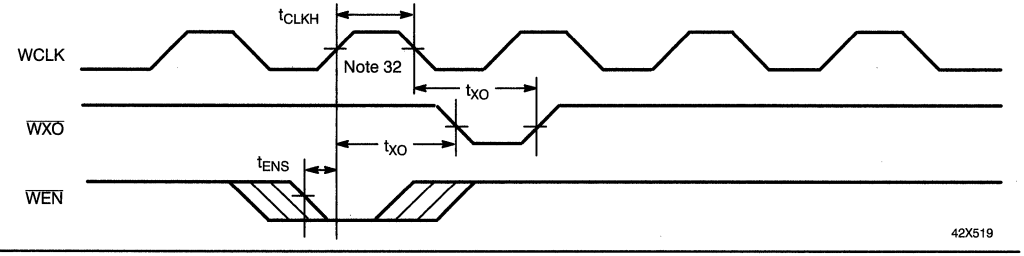
28. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
29. PAF offset = m.
30. 64 – m words in CY7C4425 , 256 – m words in FIFO for CY7C4205, 512 – m word in CY7C4215. 1024 – m words in CY7C4225, 2048 – m words in CY7C4235, and 4096 – m words in CY7C4245.
31. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{PAF}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

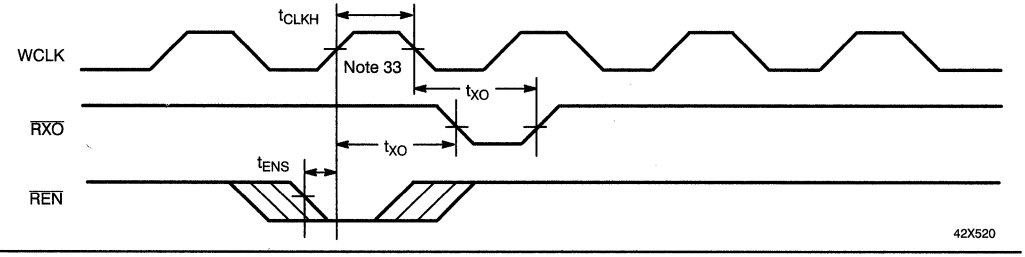
Read Programmable Registers



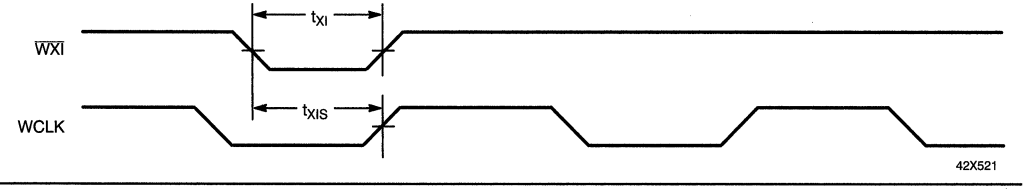
Write Expansion Out Timing



Read Expansion Out Timing



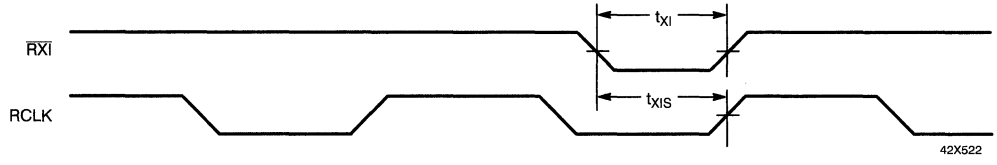
Write Expansion In Timing



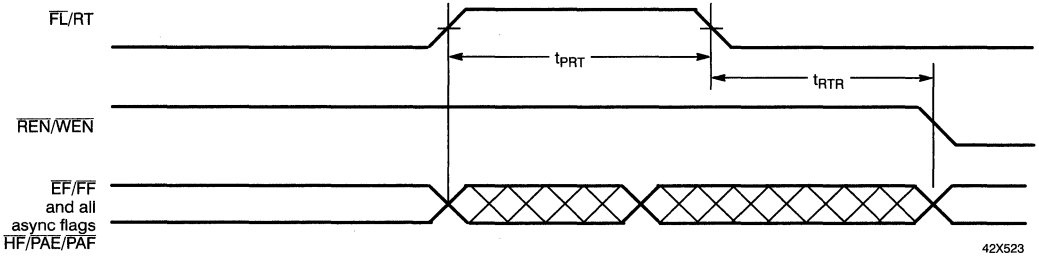
Notes:
32. Write to Last Physical Location.
33. Read from Last Physical Location.

Switching Waveforms (continued)

Read Expansion In Timing



Retransmit Timing[34, 35, 36]



Architecture

The CY7C42X5 consists of an array of 64 to 4K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN}$, $\overline{WEN}$, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, $\overline{FF}$). The CY7C42X5 also includes the control signals $\overline{WXI}$, $\overline{RXI}$, $\overline{WXO}$, $\overline{RXO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs go LOW after the falling edge of $\overline{RS}$ only if $\overline{OE}$ is asserted. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW.

FIFO Operation

When the $\overline{WEN}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ signal is active LOW, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN}$ is active LOW and $\overline{OE}$ is LOW. $\overline{REN}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN}$ must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is deasserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C42X5 devices contain two 12-bit offset registers. Data present on D_{0-11} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see *Table 2*). When the Load $\overline{LD}$ pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D_{0-11} is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register (see *Table 1*). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

Notes:

34. Clocks are free running in this case.
35. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
36. For the synchronous $\overline{PAE}$ and $\overline{PAF}$ flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Table 1. Write Offset Register

LD	WEN	WCLK[37]	Selection
0	0	↑	Writing to offset registers: Empty Offset Full Offset
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

Flag Operation

The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. $\overline{PAE}$ and $\overline{PAF}$ are synchronous if $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C42X5 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See *Table 2* for a description of programmable flags.

When the $\overline{SMODE}$ pin is tied LOW, the $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 2. Flag Truth Table

Number of Words in FIFO							
7C4425 – 64 x 18	7C4205 – 256 x 18	7C4215 – 512 x 18	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	H	L	L
1 to n[38]	1 to n[38]	1 to n[38]	H	H	H	L	H
(n+1) to 32	(n+1) to 128	(n+1) to 256	H	H	H	H	H
33 to (64−(m+1))	129 to (256−(m+1))	257 to (512−(m+1))	H	H	L	H	H
(64−m)[39] to 63	(256−m)[39] to 255	(512−m)[39] to 511	H	L	L	H	H
64	256	512	L	L	L	H	H

Number of Words in FIFO							
7C4225 – 1K x 18	7C4235 – 2K x 18	7C4245 – 4K x 18	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	H	L	L
1 to n[38]	1 to n[38]	1 to n[38]	H	H	H	L	H
(n+1) to 512	(n+1) to 1024	(n+1) to 2048	H	H	H	H	H
513 to (1024 −(m+1))	1025 to (2048 −(m+1))	2049 to (4096 −(m+1))	H	H	L	H	H
(1024−m)[39] to 1023	(2048−m)[39] to 2047	(4096−m)[39] to 4095	H	L	L	H	H
1024	2048	4096	L	L	L	H	H

Notes:

37. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.
38. n = Empty Offset (Default Values: CY7C4425 n = 7, CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/7C4235/7C4245 n = 127).
39. m = Full Offset (Default Values: CY7C4425 n = 7, CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/7C4235/7C4245 n = 127).

Width Expansion Configuration

The CY7C42X5 can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO. This technique will avoid ready data from the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. *Figure 1* demonstrates a 36-word width by using two CY7C42X5.

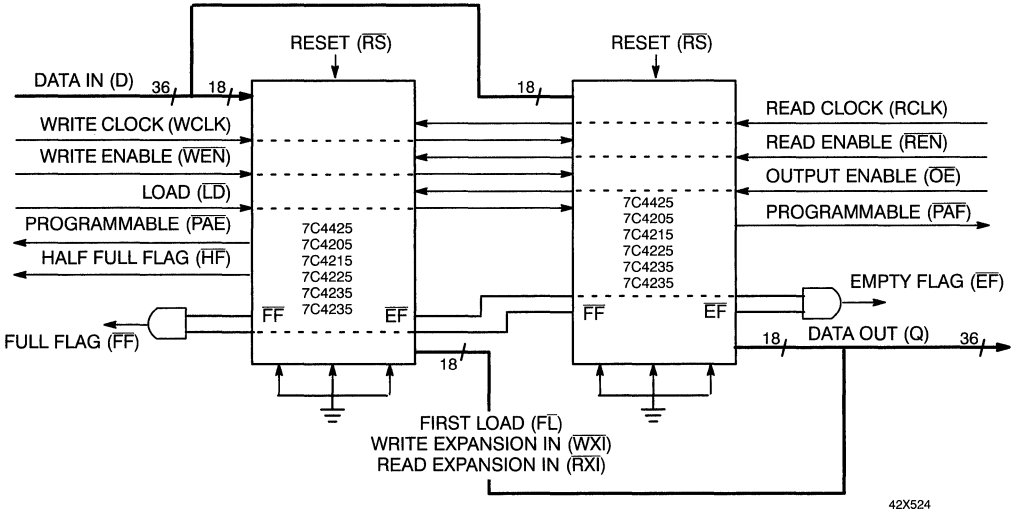


Figure 1. Block Diagram of 64 x 36/256 x 36/512 x 36/1024 x 36/2048 x 36/4096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

Depth Expansion Configuration (with Programmable Flags)

The CY7C42X5 can easily be adapted to applications requiring more than 64/256/512/1024/2048/4096 words of buffering. *Figure 2* shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together these respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

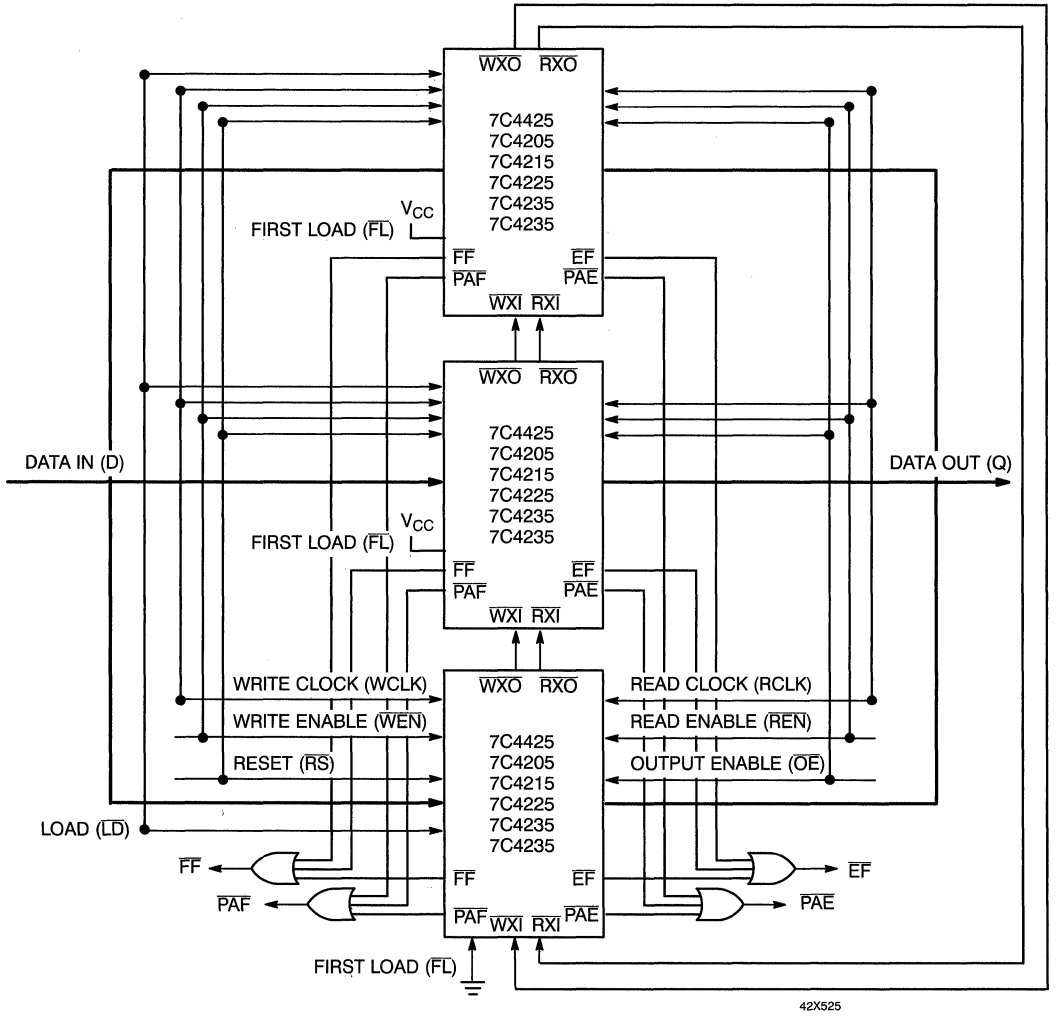


Figure 2. Block Diagram of 192 x 18/768 x 18/1536 x 18/3072 x 18/12288 x 18 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

Ordering Information

64 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4425–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4425–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4425–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4425–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

256 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4205–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4205–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4205–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4205–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

512 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4215–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4215–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4215–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4215–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

1K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4225–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4225–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4225–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4225–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

2K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4235-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235-10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235-10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4235-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235-15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4235-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4235-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235-35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235-35JI	J81	68-Lead Plastic Leaded Chip Carrier	

4K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4245-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245-10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245-10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4245-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245-15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4245-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4245-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245-35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245-35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Document #: 38-00420

CY7C439

Bidirectional 2K x 9 FIFO

Features

- **2048 x 9 FIFO buffer memory**
- **Bidirectional operation**
- **High-speed 28.5-MHz asynchronous reads and writes**
- **Simple control interface**
- **Registered and transparent bypass modes**
- **Flags indicate Empty, Full, and Half Full conditions**
- **5V ± 10% supply**
- **Available in 300-mil DIP, PLCC, LCC, and SOJ packages**
- **TTL compatible**

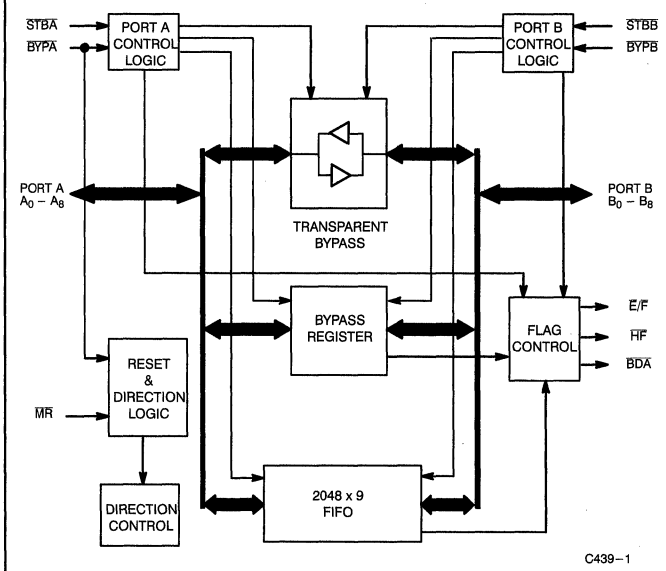
Functional Description

The CY7C439 is a 2048 x 9 FIFO memory capable of bidirectional operation. As the term first-in first-out (FIFO) implies, data becomes available to the output port in the same order that it was presented to the input port. There are two pins that indicate the amount of data contained within the FIFO block—$\overline{E}/\overline{F}$ (Empty/Full) and $\overline{HF}$ (Half Full). These pins can be decoded to determine one of four states. Two 9-bit data ports are provided. The direction selected for the FIFO determines the input and output ports. The FIFO direction can be programmed by the user at any time through the use of the reset pin ($\overline{MR}$) and the bypass/direction pin ($\overline{BYPA}$). There are no control or status registers on the CY7C439, making the part simple to use while meeting the needs of the majority of bidirectional FIFO applications.

FIFO read and write operations may occur simultaneously, and each can occur at up to 28.5 MHz. The port designated as the write port drives its strobe pin ($\overline{STBX}$, X = A or B) LOW to initiate the write operation. The port designated as the read port drives its strobe pin LOW to initiate the read operation. Output port pins go to a high-impedance state when the associated strobe pin is HIGH. All normal FIFO operations require the bypass control pin ($\overline{BYPX}$, X = A or B) to remain HIGH.

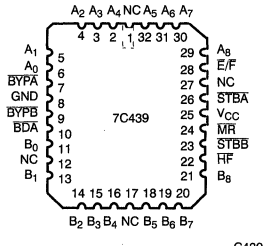
In addition to the FIFO, two other data paths are provided; registered bypass and transparent bypass. Registered bypass can be considered as a single-word FIFO in the reverse direction to the main FIFO. The

Logic Block Diagram



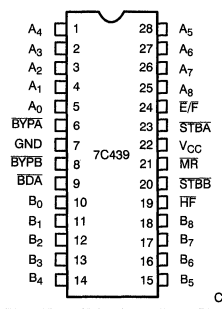
Pin Configurations

PLCC/LCC Top View



C439-2

DIP Top View



C439-3

Selection Guide

		7C439–25	7C439–30	7C439–40	7C439–65
Frequency (MHz)		28.5	25	20	12.5
Maximum Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	147	140	130	115
	Military		170	160	145

Functional Description (continued)

bypass register provides a means of sending a 9-bit status or control word to the FIFO-write port. The bypass data available pin ($\overline{BDA}$) indicates whether the bypass register is full or empty. The direction of the bypass register is always opposite to that of the main FIFO.

The port designated to write to the bypass register drives its bypass control pin ($\overline{BYPX}$) LOW. The other port detects the presence of data by monitoring $\overline{BDA}$ and reads the data by driving its bypass control pin ($\overline{BYPX}$) LOW. Registered bypass operations require that the associated FIFO strobe pin ($\overline{STBX}$) remains HIGH. Registered bypass operations do not affect data residing in the FIFO, or FIFO operations at the other port.

Transparent bypass provides a means of transferring a single word (9 bits) of data immediately in either direction. This feature allows the device to act as a simple 9-bit bidirectional buffer. This is useful for allowing the controlling circuitry to access a dumb peripheral for control/programming information.

For transparent bypass, the port wishing to send immediate data to the other side drives both its bypass and its strobe pins LOW simultaneously. This causes the buffered data to be driven out of the other port. On-chip circuitry detects conflicting use of the control pins and causes both data ports to enter a high-impedance state until the conflict is resolved.

Additionally, a Test mode is offered on the CY7C439. This mode allows the user to load data into the FIFO and then read it back out of the same port. Built-In Self Test (BIST) and diagnostic functions can take advantage of these features.

The CY7C439 is fabricated using an advanced 0.8µ N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPA}$ and $\overline{STBA}$
$B_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPB}$ and $\overline{STBB}$
$\overline{BYPA}$	I	Registered Bypass Mode Select for A Side
$\overline{BYPB}$	I	Registered Bypass Mode Select for B Side
$\overline{BDA}$	O	Bypass Data Available Flag
$\overline{STBA}$	I	Data Strobe for A Side
$\overline{STBB}$	I	Data Strobe for B Side
$\overline{E/F}$	O	Encoded Empty/Full Flag
$\overline{HF}$	O	Half Full Flag
$\overline{MR}$	I	Master Reset

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C439–25 Min.	7C439–25 Max.	7C439–30 Min.	7C439–30 Max.	7C439–40 Min.	7C439–40 Max.	7C439–65 Min.	7C439–65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
			Mil			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{STBX}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		147		140		130		115	mA
			Mil[4]				170		160		145	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		40		40		40		40	mA
			Mil				45		45		45	
I_{SB2}	Power-Down Current	All Inputs V_{CC} − 0.2V	Com'l		20		20		20		20	mA
			Mil				25		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90		−90	mA

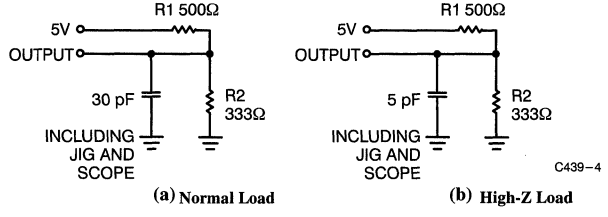
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

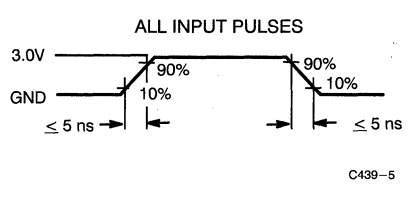
Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 115 mA + [($\bar{f}$ − 12.5) · 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 145 mA + [($\bar{f}$ − 12.5) · 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

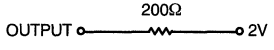
AC Test Loads and Waveform



(a) Normal Load (b) High-Z Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 7]

Parameter	Description	7C439–25		7C439–30		7C439–40		7C439–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_A	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[8, 9]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[8, 9]	Data Valid from Read HIGH	3		3		3		3		ns
t_{HZR}[8, 9]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[8, 9]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPS}	$\overline{STBX}$ HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RPBS}	$\overline{BYPA}$ to $\overline{MR}$ HIGH	10		10		15		20		ns
t_{RPBH}	$\overline{BYPA}$ Hold after $\overline{MR}$ HIGH	0		0		0		0		ns
t_{BDH}	$\overline{MR}$ LOW to $\overline{BDA}$ HIGH		35		40		50		80	ns
t_{BSR}	$\overline{STBX}$ HIGH to $\overline{BYPA}$ LOW	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{BRS}	$\overline{BYPX}$ HIGH to $\overline{STBX}$ LOW	10		10		10		15		ns
t_{REF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Read)		25		30		35		60	ns
t_{RFF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Read)		25		30		35		60	ns
t_{WEF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Write)		25		30		35		60	ns
t_{WFF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Write)		25		30		35		60	ns
t_{BDA}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ LOW (Write)		25		30		35		60	ns
t_{BDB}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ HIGH (Read)		25		30		35		60	ns
t_{BA}	$\overline{BYPX}$ LOW to Data Valid (Read)		30		30		40		60	ns
t_{BHZ}[8, 9]	$\overline{BYPX}$ HIGH to High Z (Read)		18		20		25		30	ns
t_{TSB}	$\overline{STBX}$ HIGH to $\overline{BYPX}$ LOW Set-Up	10		10		10		15		ns
t_{TBS}	$\overline{STBX}$ LOW after $\overline{BYPX}$ LOW	0	10	0	10	0	10	0	10	ns
t_{TSN}	$\overline{STBX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TSD}[8, 9]	$\overline{STBX}$ HIGH to Data High Z		18		20		25		30	ns
t_{TBN}	$\overline{BYPX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TBD}	$\overline{BYPX}$ HIGH to Data High Z		18		20		25		30	ns

Switching Characteristics Over the Operating Range[2, 7] (continued)

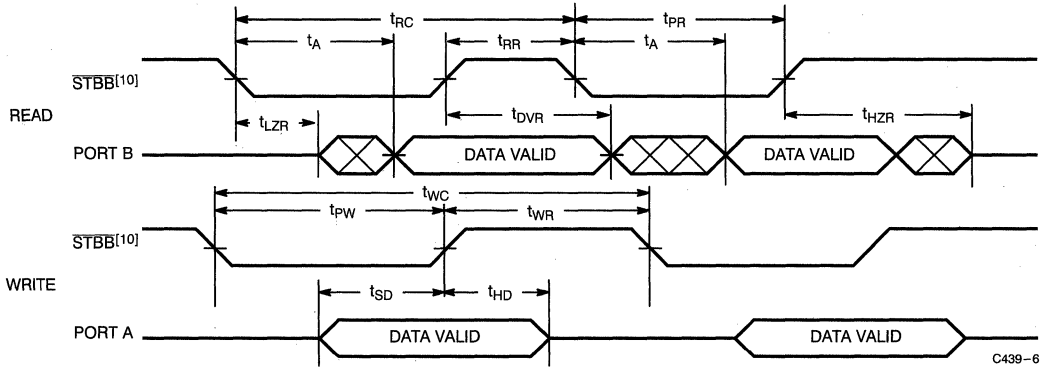
Parameter	Description	7C439–25		7C439–30		7C439–40		7C439–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{TPD}[8, 9]	$\overline{STBX}$ LOW to Data Valid		20		20		30		55	ns
t_{DL}	Transparent Propagation Delay		20		20		25		30	ns
t_{ESD}[8, 9]	$\overline{STBX}$ LOW to High Z		18		20		25		30	ns
t_{EBD}[8, 9]	$\overline{BYPX}$ LOW to High Z		18		20		25		30	ns
t_{EDS}	$\overline{STBX}$ HIGH to Low Z		18		20		25		30	ns
t_{EDB}	$\overline{BYPX}$ HIGH to Low Z		18		20		25		30	ns
t_{BPW}	$\overline{BYPX}$ Pulse Width (Trans.)	25		30		40		65		ns
t_{TSP}	$\overline{STBX}$ Pulse Width (Trans.)	20		20		30		55		ns
t_{BLZ}[8, 9]	$\overline{BYPX}$ LOW to Low Z (Read)	10		10		10		10		ns
t_{BDV}	$\overline{BYPX}$ HIGH to Data Invalid (Read)	3		3		3		3		ns
t_{WHF}	$\overline{STBX}$ LOW to $\overline{HF}$ LOW (Write)		35		40		50		80	ns
t_{RHF}	$\overline{STBX}$ HIGH to $\overline{HF}$ HIGH (Read)		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{E}/\overline{F}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{E}/\overline{F}$ HIGH	25		30		40		65		ns
t_{BSU}	Bypass Data Set-Up Time	15		18		20		30		ns
t_{BHL}	Bypass Data Hold Time	0		0		0		10		ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance as in part (a) of AC Test Loads, unless otherwise specified.
8. t_{DVR}, t_{BDV}, t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, t_{TSD}, t_{LZR}, t_{HWZ}, and t_{BLZ} use capacitance loading as in part (b) of AC Test Loads.
9. t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, and t_{TSD} transition is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}. t_{DVR} and t_{BDV} transition is measured at the 1.5V level. t_{LZR}, t_{HWZ}, and t_{BLZ} transition is measured at ±100 mV from the steady state.

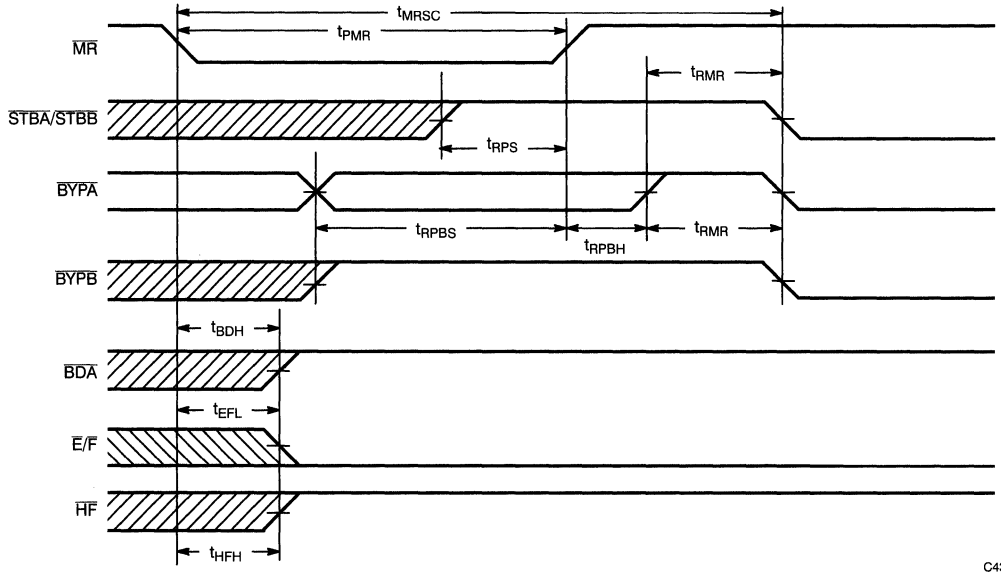
Switching Waveforms

Asynchronous Read and Write Timing Diagram

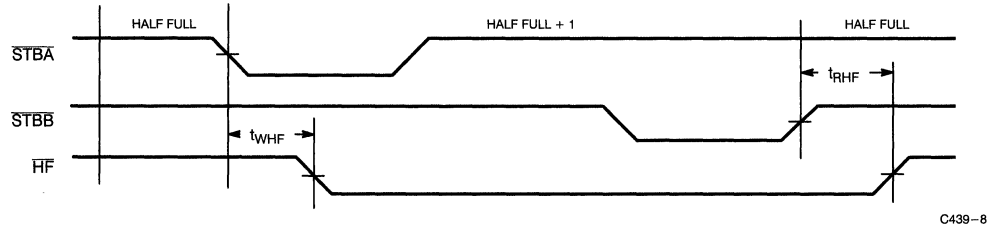


Switching Waveforms (continued)

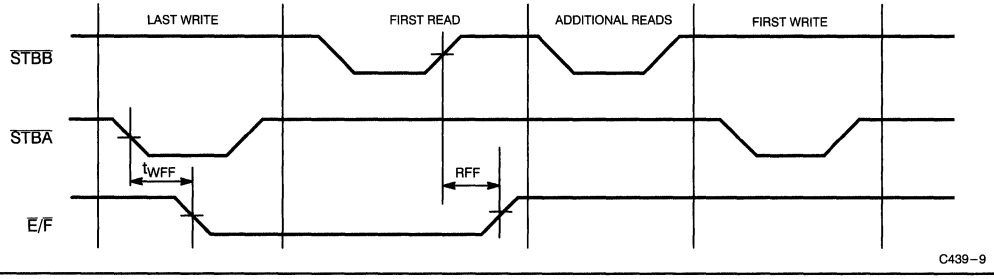
Master Reset Timing Diagram



Half-Full Flag Timing Diagram[11]



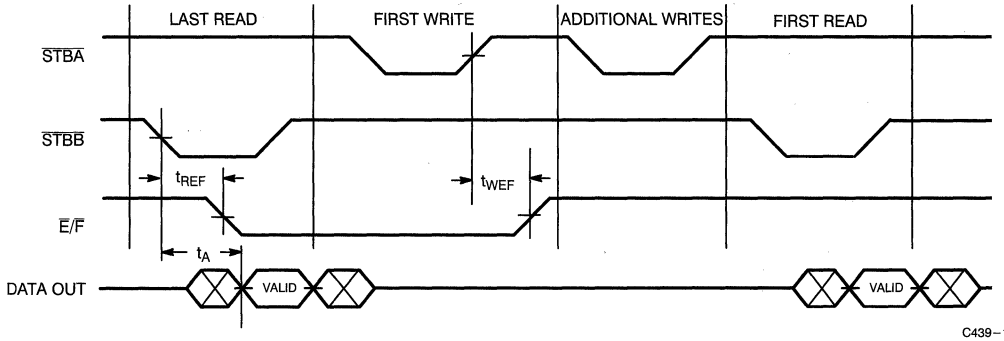
Last Write to First Read Empty/Full Flag Timing Diagram[11]



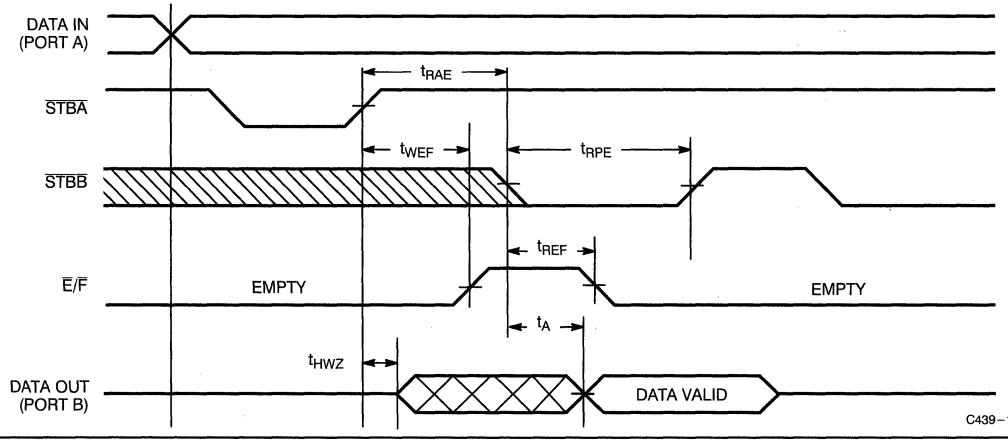
Notes:
10. Direction selected Port A to Port B.
11. Direction selected as A to B.

Switching Waveforms (continued)

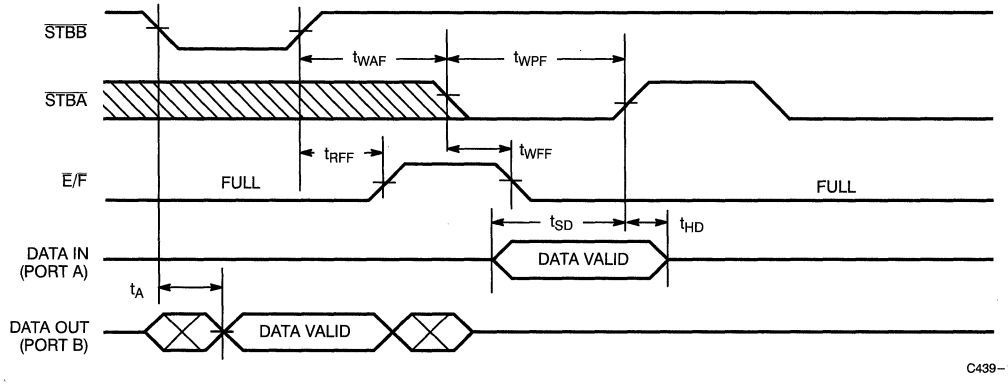
Last Read to First Write Empty/Full Flag Timing Diagram[11]



Empty/Full Flag and Read Bubble-Through Mode Timing Diagram[11]

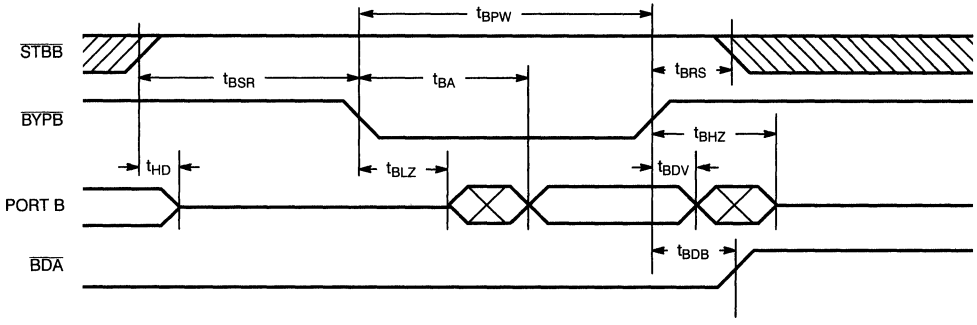


Empty/Full Flag and Write Bubble-Through Mode Timing Diagram[11]

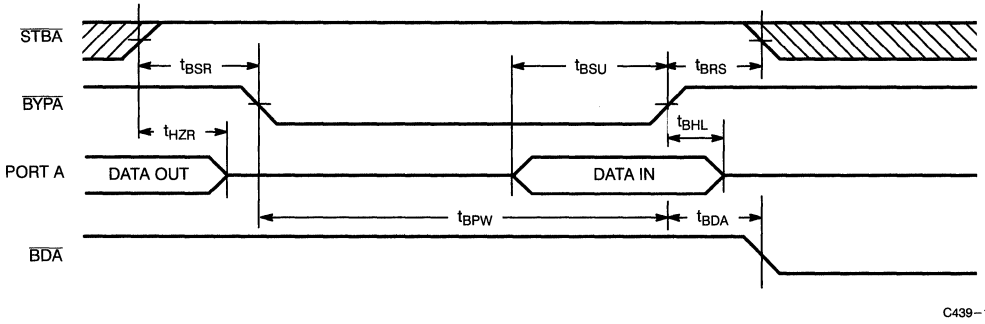


Switching Waveforms (continued)

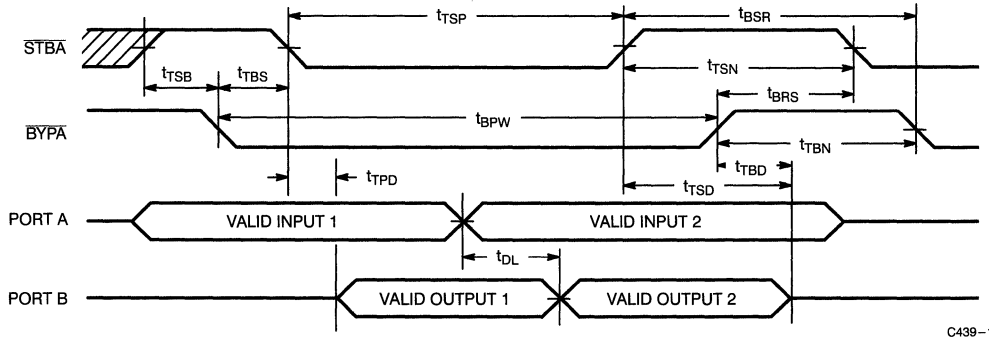
Registered Bypass Read Timing Diagram[12]



Registered Bypass Write Timing Diagram[13]



Transparent Bypass Read Timing Diagram[14]

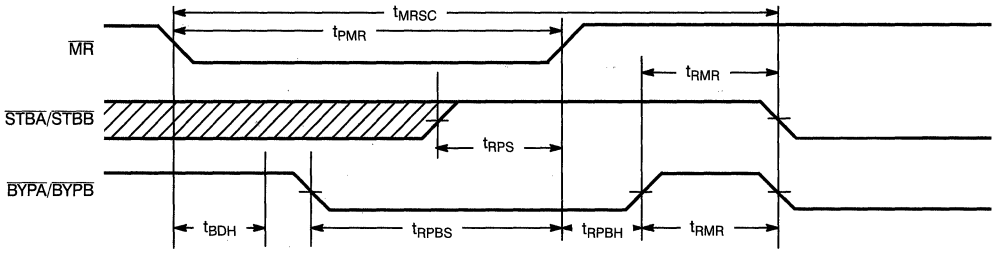


Notes:

12. Port B selected to read bypass register (FIFO direction Port B to Port A).
13. Port A selected to write bypass register (FIFO direction Port B to Port A.
14. Diagram shows transparent bypass initiated by Port A. Times are identical if initiated by Port B.

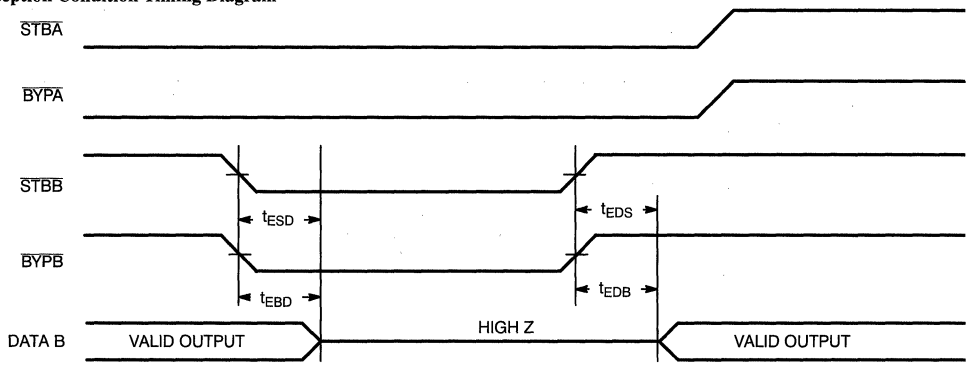
Switching Waveforms (continued)

Test Mode Timing Diagram



C439–16

Exception Condition Timing Diagram[14]



C439–17

Architecture

The CY7C439 consists of a 2048 by 9-bit dual-ported RAM array, a read pointer, a write pointer, data switching circuitry, buffers, a bypass register, control signals ($\overline{STBA}$, $\overline{STBB}$, $\overline{BYPA}$, $\overline{BYPB}$, $\overline{MR}$), and flags ($\overline{E}/\overline{F}$, $\overline{HF}$, $\overline{BDA}$).

Operation at Power-On

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. During an $\overline{MR}$ cycle, the user can initialize the device by choosing the direction of FIFO operation (see *Table 1*). There is a minimum LOW period for $\overline{MR}$, but no maximum time. The state of $\overline{BYPA}$ is latched internally by the rising edge of $\overline{MR}$ and used to determine the direction of subsequent data operations.

Resetting the FIFO

During the reset condition (see *Table 1*), the FIFO three-states the data ports, sets $\overline{BDA}$ and $\overline{HF}$ HIGH, $\overline{E}/\overline{F}$ LOW, and ignores the state of $\overline{BYPA}/B$ and $\overline{STBA}/B$. The bypass registers are initialized to zero. During this time the user is expected to set the direction of the FIFO by driving $\overline{BYPA}$ HIGH or LOW, and $\overline{BYPB}$, $\overline{STBA}$, and $\overline{STBB}$ HIGH. If $\overline{BYPA}$ is LOW (selecting direction B>A), the FIFO will then remain in a reset condition until the user terminates the reset operation by driving $\overline{BYPA}$ HIGH. If $\overline{BYPA}$ is HIGH (selecting direction A>B), the reset condition terminates after the rising edge of $\overline{MR}$. The entire reset phase can be accomplished in one cycle time of t_{RC}.

FIFO Operation

The operation of the FIFO requires only one control pin per port ($\overline{STBX}$). The user determines the direction of the FIFO data flow by initiating an $\overline{MR}$ cycle (see *Table 1*), which clears the FIFO and bypass register and sets the data path and control signal multiplexers. The bypass register is configured in the opposite direction to the FIFO data flow. The FIFO direction can be reversed at any time by initiating another $\overline{MR}$ cycle. Data is written into the FIFO on the rising edge of the input, $\overline{STBX}$, and read from the FIFO by a low level at the output, $\overline{STBX}$. The two ports are asynchronous and independent. If the user attempts to read the FIFO when it is empty, no action takes place (the read pointer is not incremented) until the other port writes to the FIFO. Then a bubble-through read takes place, in which the read strobe is generated internally and the data becomes available at the read port shortly thereafter if the read strobe ($\overline{STBX}$) is still LOW. Similarly, for an attempted write operation when the FIFO is full, no internal operation takes place until the other port performs a read operation, at which time the bubble-through write is performed if the write strobe ($\overline{STBX}$) is still LOW.

Registered Bypass Operation

The registered bypass feature provides a means of transferring one 9-bit word of data in the opposite direction to normal data flow without affecting either the FIFO contents or the FIFO write operations at the other port. The bypass register is configured during reset to provide a data path in the opposite direction to that of the FIFO (see *Table 1*). For example, if port A is writing data to the FIFO (hence port B is reading data from the FIFO) then $\overline{BYPB}$ is used to write to the bypass register at port B, and $\overline{BYPA}$ is used to read a single word from the bypass register at port A. The bypass data available flag ($\overline{BDA}$) is generated to notify port A that bypass data is available. $\overline{BDA}$ goes true on the trailing edge of the $\overline{BYPX}$ write operation and false upon the trailing edge of the $\overline{BYPX}$ read operation.

Data is written on the rising edge of $\overline{BYPX}$ into the bypass register for later retrieval by the other port, regardless of the state of $\overline{BDA}$. The bypass register is read by a low level at $\overline{BYPX}$, regardless of the state of $\overline{BDA}$.

Transparent Bypass Operation

The transparent bypass feature provides a means of sending immediate data "around" the FIFO in either direction. The FIFO contents are not affected by the use of transparent bypass, but the control signals for transparent bypass are shared with those of the normal FIFO operation. Hence there are limitations on the use of transparent bypass to ensure that data integrity and ease of use are preserved. The port wishing to send immediate data must ensure that the other port will not attempt a FIFO read or write during the transparent bypass cycle. If this is not possible, registered bypass or external circuitry should be used.

Transparent bypass mode is initiated by bringing both $\overline{BYPA}$ and $\overline{STBA}$ LOW together. Care should be taken to observe the following constraints on the timing relationships. Since $\overline{STBA}$ is used for normal FIFO operations, it must follow $\overline{BYPA}$ falling edge by t_{TBS} to prevent erroneous FIFO read or write operations. Since $\overline{BYPA}$ is used alone to initiate registered bypass read and write, it is internally delayed before initiating registered bypass. If $\overline{STBA}$ falls during this time, delay registered bypass is averted, and transparent bypass is initiated. Identical arguments apply to $\overline{BYPB}$ and $\overline{STBB}$.

If a transparent bypass sequence is successfully accomplished, data presented to the initiating port (port A in the above discussion) will be buffered to the other (port B) after t_{DL}. Either port can initiate a transparent bypass operation at any time, but if the control signals ($\overline{STBA}$/B, $\overline{BYPA}$/B) are in conflict (exception condition), internal circuitry will switch both ports to high-impedance until the conflict is resolved.

Test Mode Operation

The Test mode feature provides a means of reading the FIFO contents from the same port that the data was written to the FIFO. This feature is useful for Built-In Self Test (BIST) and diagnostic functions. To utilize this capability, initialize FIFO direction A to B and load data into the FIFO using normal write timing. In order to read data back out of the same port (port A), initiate a $\overline{MR}$ cycle with both $\overline{BYPA}$ and $\overline{BYPB}$ LOW (see Test Mode Timing diagram). After completing the cycle, the data can be read out of port A in FIFO order. Data will be inverted when read out of the device. Also, flags are not valid when reading data.

Flag Operation

There are two flags, Empty/Full ($\overline{E}/\overline{F}$) and Half Full ($\overline{HF}$), which are used to decode four FIFO states (see *Table 4*). The states are empty, 1–1024 locations full, 1025–2047 locations full, and full. Note that two conditions cause the $\overline{E}/\overline{F}$ pin to go LOW, Empty and Full, hence both flag pins must be used to resolve the two conditions.

Table 1. FIFO Direction Select Truth Table

$\overline{MR}$	$\overline{BYPA}$	$\overline{BYPB}$	$\overline{STBA}$	$\overline{STBB}$	Action
1	X	X	X	X	Normal Operation
⌐¬	1	1	1	1	FIFO Direction A to B, Registered Bypass Direction B to A
⌐¬	0	1	1	1	FIFO Direction B to A, Registered Bypass Direction A to B
0	X	X	X	X	Reset Condition

Table 2. Bypass Operation Truth Table

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
A⇕B	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at A, Read at B
A⇕B	1	⌐¬	⌐¬	1	Normal FIFO Read at B, Bypass Register Read at A
A⇕B	⌐¬	1	1	⌐¬	Normal FIFO Write at A, Bypass Register Write at B
B⇕A	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at B, Read at A
B⇕A	1	⌐¬	⌐¬	1	Normal FIFO Write at B, Bypass Register Write at A
B⇕A	⌐¬	1	1	⌐¬	Normal FIFO Read at A, Bypass Register Read at B
X	0	0	1	1	No FIFO Operations, Transparent Data A to B
X	1	1	0	0	No FIFO Operations, Transparent Data B to A

Table 3. Exception Conditions: Operation Not Defined

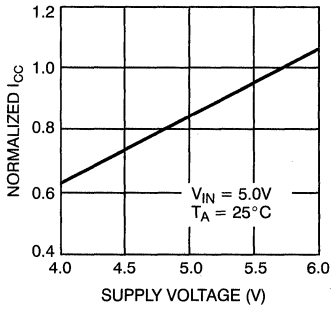
Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYBP}$	Action
X	0	1	0	0	Data Buses High Impedance
X	1	0	0	0	Data Buses High Impedance
X	0	0	0	0	Data Buses High Impedance
X	0	0	1	0	Data Buses High Impedance
X	0	0	0	1	Data Buses High Impedance

Table 4. Flag Truth Table

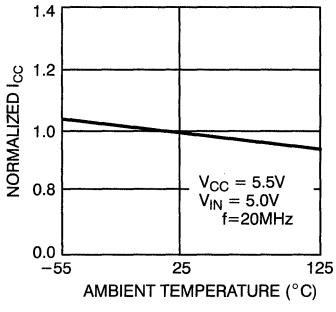
$\overline{E/F}$	$\overline{HF}$	State
0	1	Empty
1	1	1–1024 Locations Full
1	0	1025–2047 Locations Full
0	0	Full

Typical DC and AC Characteristics

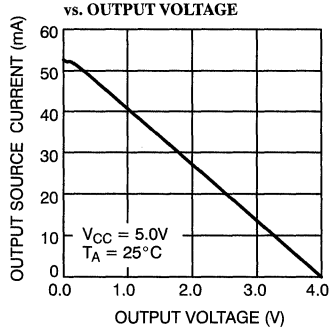
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



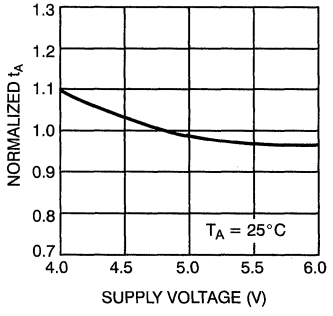
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



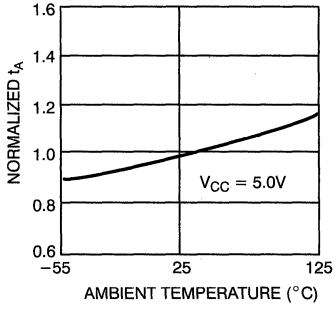
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



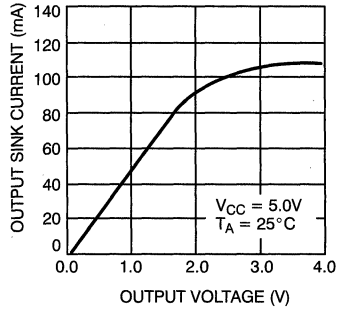
NORMALIZED t_A vs. SUPPLY VOLTAGE



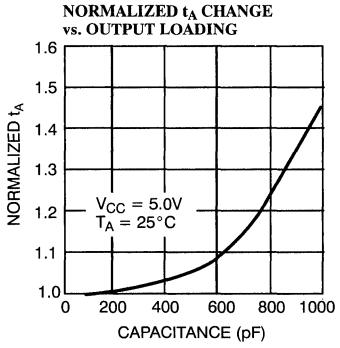
NORMALIZED t_A vs. AMBIENT TEMPERATURE

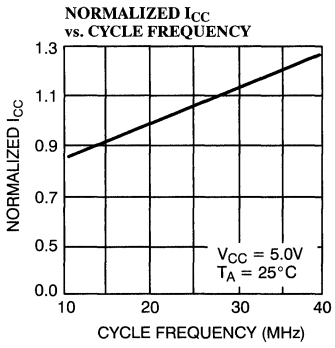


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)





Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C439–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–25PC	P21	28-Lead (300-Mil) Molded DIP	
30	CY7C439–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C439–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
6.5	CY7C439–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPS}	9, 10, 11
t_{RPBS}	9, 10, 11
t_{RPBH}	9, 10, 11
t_{BDH}	9, 10, 11
t_{BSR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{BRS}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11

Parameters	Subgroups
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{BSU}	9, 10, 11
t_{BHL}	9, 10, 11
t_{BDA}	9, 10, 11
t_{BDB}	9, 10, 11
t_{BA}	9, 10, 11
t_{BHZ}	9, 10, 11
t_{TSB}	9, 10, 11
t_{TBS}	9, 10, 11
t_{TSN}	9, 10, 11
t_{TSD}	9, 10, 11
t_{TBN}	9, 10, 11
t_{TBD}	9, 10, 11
t_{TPD}	9, 10, 11
t_{DL}	9, 10, 11
t_{ESD}	9, 10, 11
t_{EBD}	9, 10, 11
t_{EDS}	9, 10, 11
t_{EDB}	9, 10, 11
t_{BPW}	9, 10, 11
t_{TSP}	9, 10, 11
t_{BLZ}	9, 10, 11
t_{BDV}	9, 10, 11

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CY7C441
CY7C443

Clocked 512 x 9, 2K x 9 FIFOs

Features

- **512 x 9 (CY7C441) and 2,048 x 9 (CY7C443) FIFO buffer memory**
- **High-speed 70-MHz operation**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Almost Empty, and Almost Full status flags**
- **Fully asynchronous and simultaneous read and write operation**
- **Width expandable**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Available in 300-mil 28-pin DIP, PLCC, LCC, and SOJ packages**
- **Proprietary 0.8μ CMOS technology**
- **TTL compatible**
- **Low power – I_{CC}=70 mA**

Functional Description

The CY7C441 and CY7C443 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C441 has a 512 word by 9 bit memory array, while the CY7C443 has a 2048 word by 9 bit memory array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

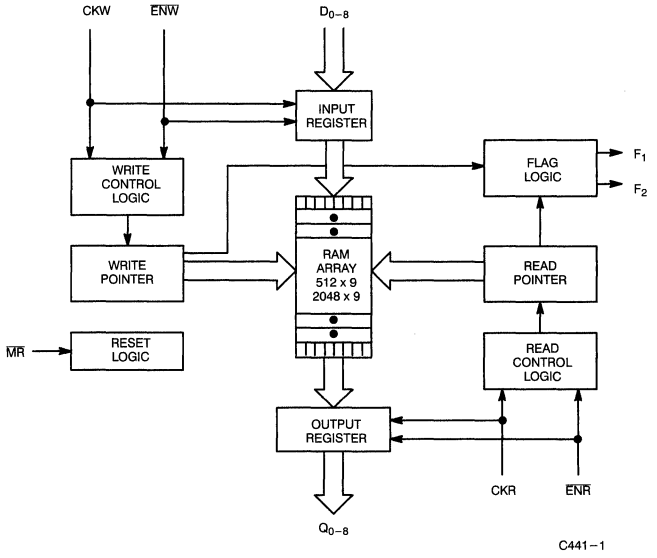
Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are acceptable.

The CY7C441 and CY7C443 clocked FIFOs provide two status flag pins (F1 and F2). These flags are decoded to determine one of four states: Empty, Almost Empty, Intermediate, and Almost Full (*Table 1*). The flags are synchronous; i.e., change state relative to either the read clock (CKR) or the write clock (CKW). The Empty and Almost Empty states are updated exclusively by the CKR while Almost Full is updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C441 and the CY7C443 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

5

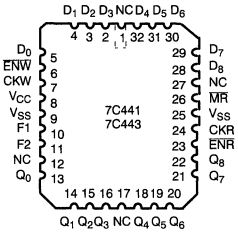
Logic Block Diagram



C441–1

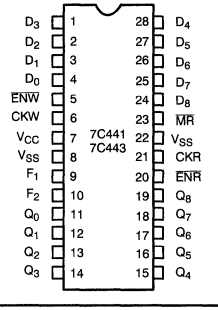
Pin Configurations

PLCC/LCC
Top View



C441–2

DIP/SOJ
Top View



C441–3

Selection Guide

		7C441–14 7C443–14	7C441–20 7C443–20	7C441–30 7C443–30
Maximum Frequency (MHz)		71.4	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: when the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_0 – D_8) into the FIFO's memory
Q_{0-8}	O	Data Outputs: when the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_0 – Q_8) out of the FIFO's memory
$\overline{ENW}$	I	Enable Write: enables the CKW input
$\overline{ENR}$	I	Enable Read: enables the CKR input
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW and updates the Almost Full flag state
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW and updates the Almost Empty and Empty flag states
F1	O	Flag 1: is used in conjunction with Flag 2 to decode which state the FIFO is in (see *Table 1*)
F2	O	Flag 2: is used in conjunction with Flag 1 to decode which state the FIFO is in (see *Table 1*)
$\overline{MR}$	I	Master Reset: resets the device to an empty condition

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C441–14 7C443–14 Min.	7C441–14 7C443–14 Max.	7C441–20 7C443–20 Min.	7C441–20 7C443–20 Max.	7C441–30 7C443–30 Min.	7C441–30 7C443–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	μA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		– 90		– 90		– 90		mA
I_{CC1}[4]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		120		100	mA
			Mil/Ind		150		130		110	mA
I_{CC2}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70	mA
			Mil/Ind		80		80		80	mA
I_{SB}[6]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
			Mil/Ind		30		30		30	mA

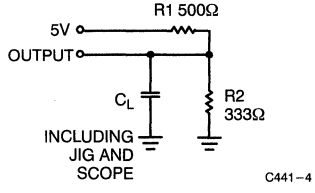
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

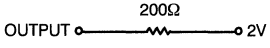
2. See the last page of this specification for Group A subgroup testing information.
3. Test no more than one output at a time and do not test any output for more than one second.
4. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
5. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
6. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
7. Tested initially and after any design or process changes that may affect these parameters.

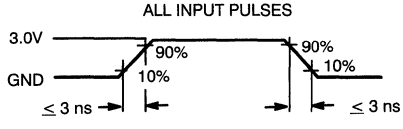
AC Test Loads and Waveform[8,9]



C441–4

Equivalent to: THÉVENIN EQUIVALENT





C441–5

Switching Characteristics Over the Operating Range[2,10]

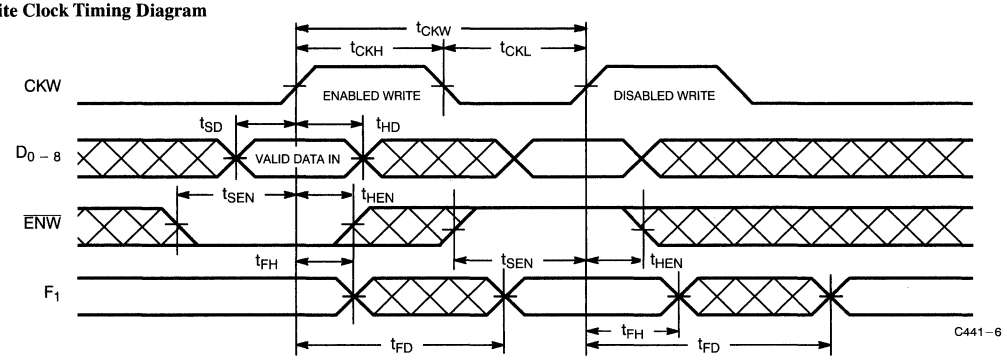
Parameter	Description	7C441–14 7C443–14		7C441–20 7C443–20		7C441–30 7C443–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A[11]	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	7		9		12		ns
t_{HD}	Data Hold	0		0		0		ns
t_{SEN}	Enable Set-Up	7		9		12		ns
t_{HEN}	Enable Hold	0		0		0		ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[12]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[13]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns

Notes:

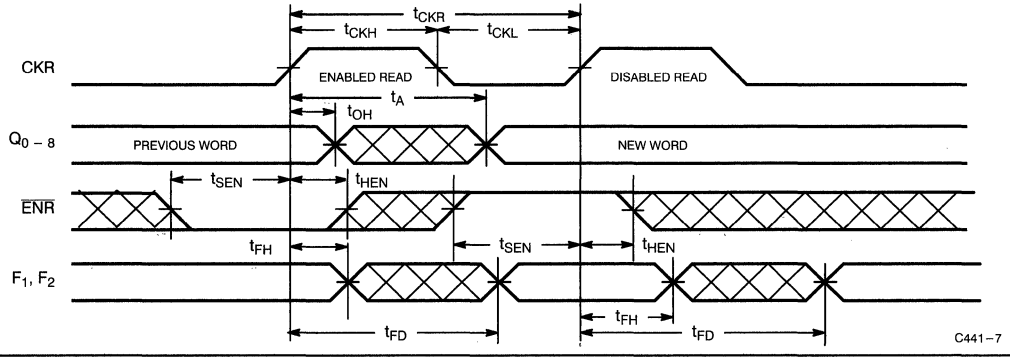
8. C_L = 30 pF for all AC parameters.
9. All AC measurements are referenced to 1.5V.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in the AC Test Loads and Waveforms and capacitance as in note NO TAG, unless otherwise specified.
11. Access time includes all data outputs switching simultaneously.
12. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full flag. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Almost Full flag, CKR is the clock for Empty and Almost Empty flags.
13. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is abritrary. See Note NO TAG for definition of clock and opposite clock.

Switching Waveforms

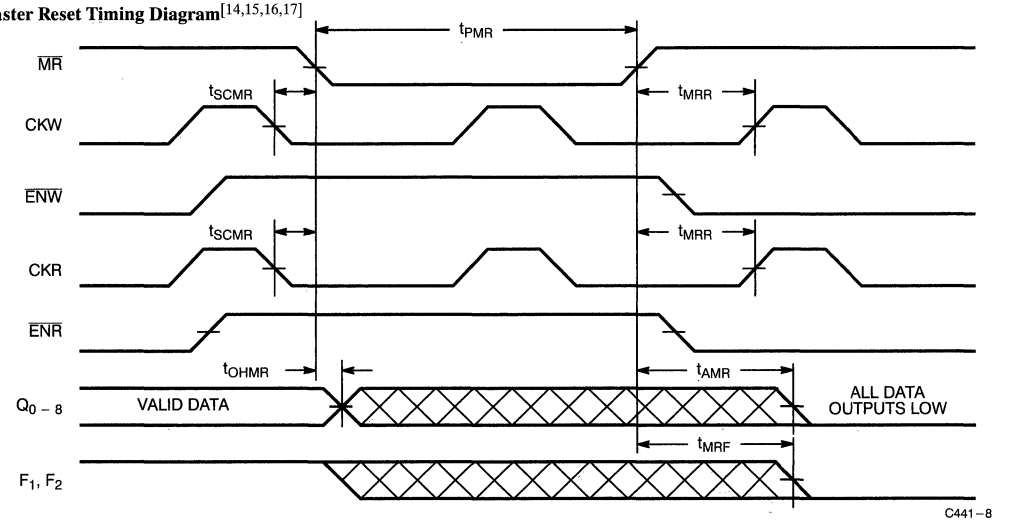
Write Clock Timing Diagram



Read Clock Timing Diagram

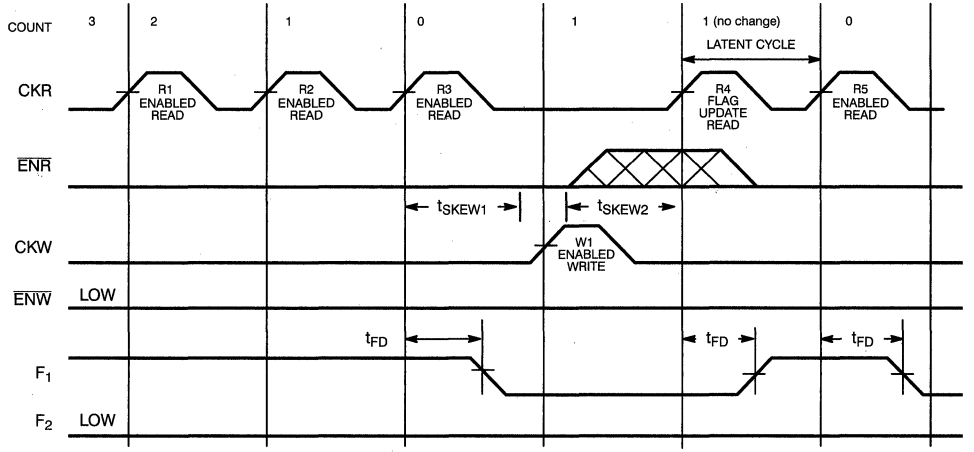


Master Reset Timing Diagram[14,15,16,17]



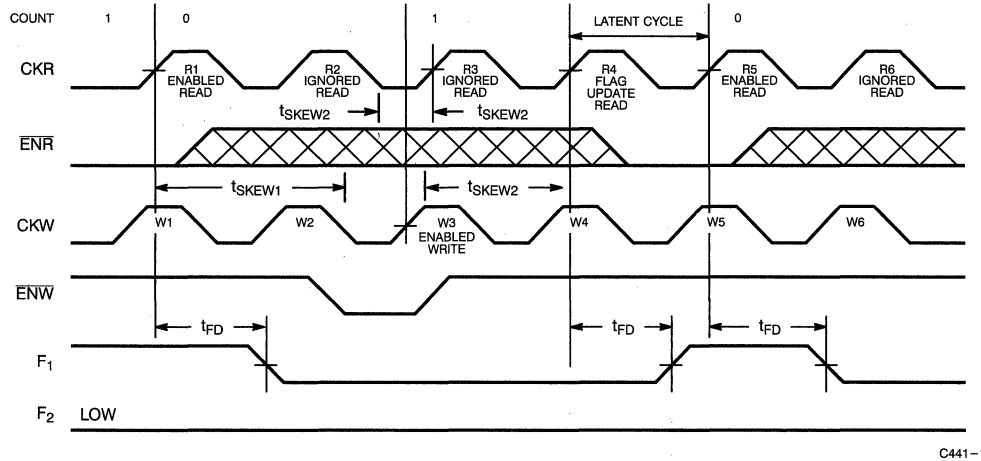
Switching Waveforms (continued)

Read to Empty Timing Diagram[18,19,20]



C441–9

Read to Empty Timing Diagram with Free-Running Clocks[18,19,21]



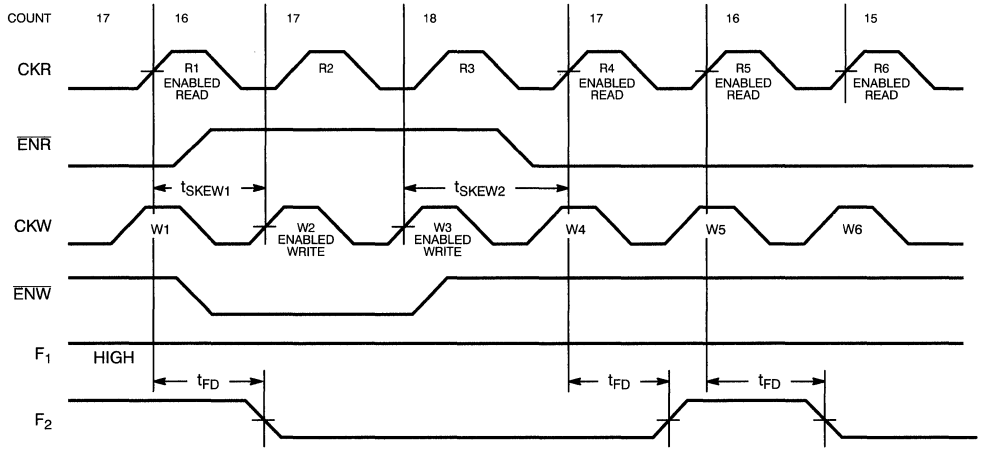
C441–10

Notes:

14. $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
15. $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
16. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$.
17. In this example, Q_{0-8} will remain valid until t_{OHMR} if the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.
18. "Count" is the number of words in the FIFO.
19. CKR is clock and CKW is opposite clock.
20. R3 updates the flags to the Empty state by bringing F1 LOW. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and therefore updates the FIFO to the Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status, regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.
21. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.

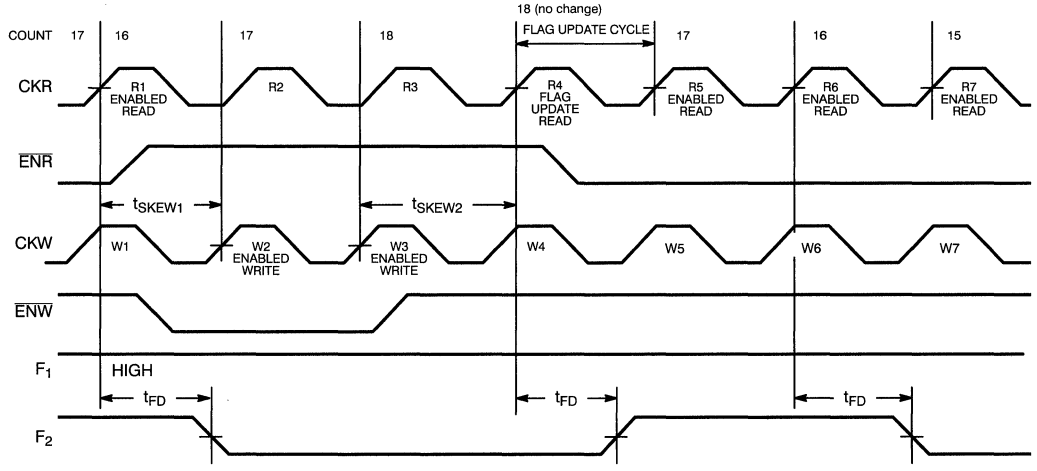
Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[18,19]



C441–11

Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[18,19,22,23]



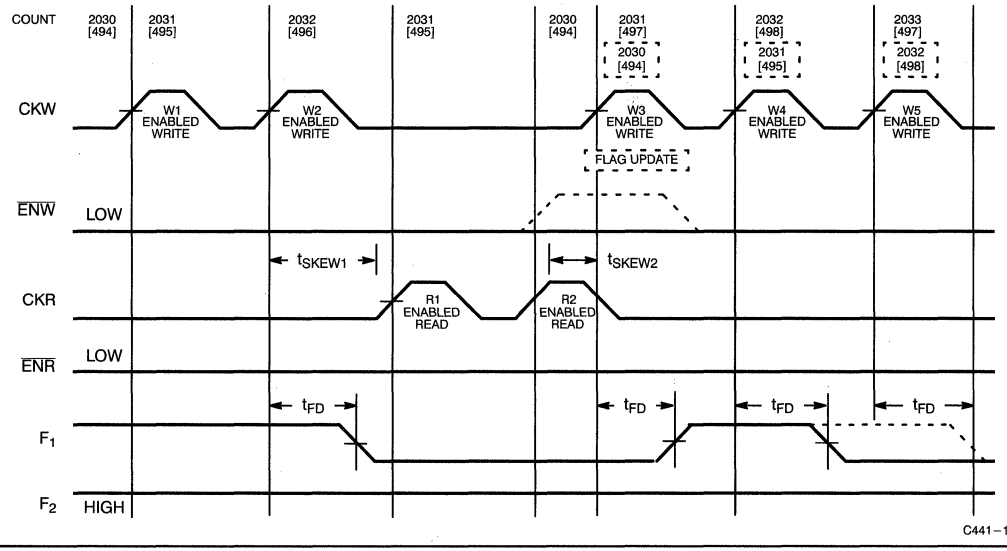
C441–12

Notes:

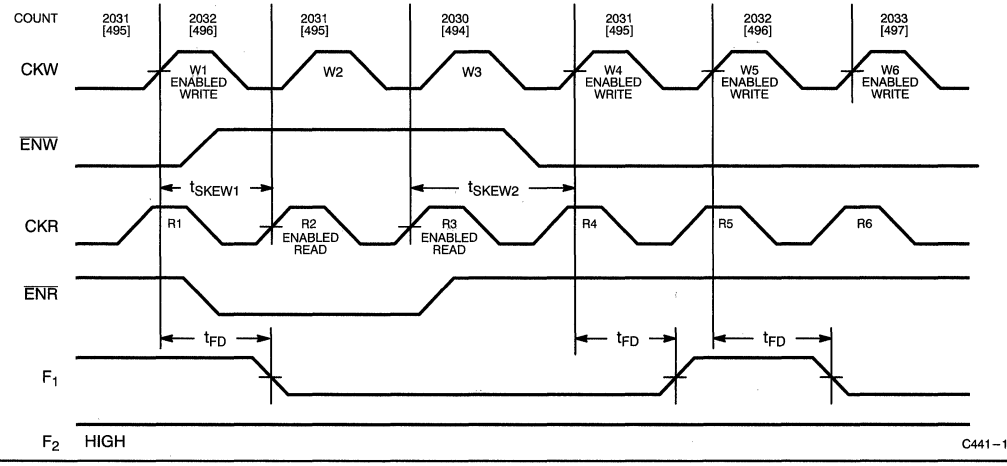
22. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
23. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧18; two enabled writes: W2, W3) before a read (R4) can update flags to the Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram[18,24,25,26,27]



Write to Almost Full Timing Diagram with Free-Running Clocks[18,24,25]

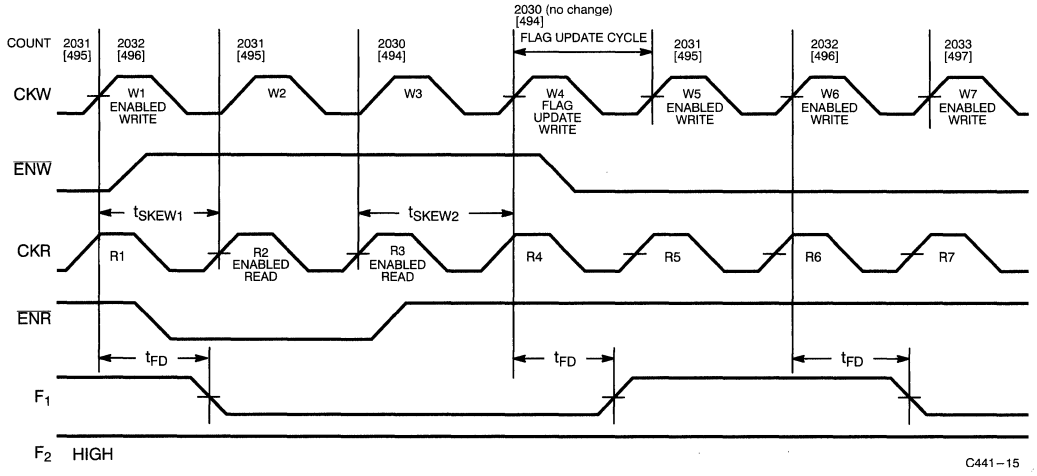


Notes:

24. CKW is clock and CKR is opposite clock.
25. Count = 2032 indicates Almost Full for CY7C443 and count = 496 indicates Almost Full for CY7C441. Values for the CY7C441 count are shown in brackets.
26. The dashed lines show W3 as flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.
27. W2 updates the flags to the Almost Full state by bringing F1 LOW. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
28. When making the transition from Almost Full to Intermediate, the count must decrease by two (2032 ◗ 2030; two enabled reads: R2, R3) before a write (W4) can update flags to Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clock[18,24,25,28]



Architecture

The CY7C441/443 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$), and flags (F1, F2).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by both flags F1 and F2 being LOW. All data outputs (Q_{0-8}) go LOW at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. F_1 and F_2 are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read duration. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Flag Operation

The CY7C441/3 provide two flags, F1 and F2, which are used to decode four FIFO states (see *Table 1*). All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate; see *Figure 1*). The synchronous architecture guarantees some minimum valid time for the flags.

The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the F1 and F2 pins to output a state signifying the Empty condition. The Almost Full flag is updated exclusively by the write clock (CKW). For example, if the CY7C443 FIFO contains 2031 words (2032 words or greater indicates Almost Full in the CY7C443), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the F1 and F2 pins to output the Almost Full state.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the Almost Full flag is only updated by the CKW, careful attention must be given to the flag operation. The user must be aware that if a flag boundary (Empty, Almost Empty, and Almost Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKR does not effect Almost Full), a flag update is necessary to represent the FIFO's new state. This signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for the Almost Full flag).

Table 1. Flag Truth Table

F1	F2	State	CY7C441 Number of Words in FIFO	CY7C443 Number of Words in FIFO
0	0	Empty	0	0
1	0	Almost Empty	1 – 16	1 – 16
1	1	Intermediate Range	17 – 495	17 – 2031
0	1	Almost Full or Full	496 – 512	2032 – 2048

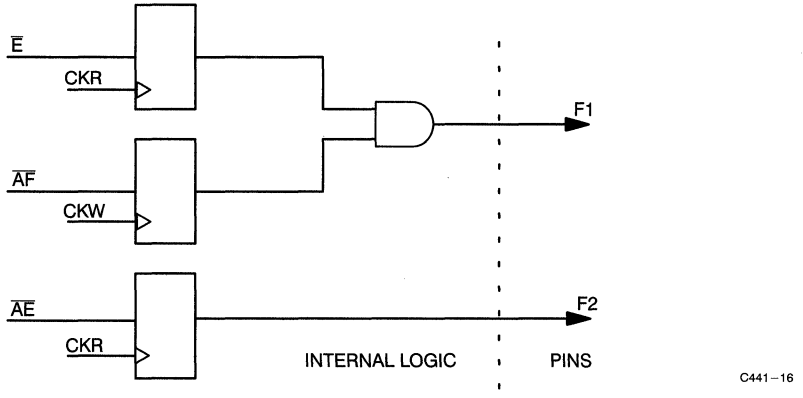


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Until the flag update cycle is executed, the synchronous flags do not show the true state of the FIFO. For example, if 2,040 writes are performed to an empty CY7C443 without a single read, F1 and F2 will still exhibit an Empty flag. This is because F2 is exclusively updated by the CKR, therefore, a single read (flag update cycle) is necessary to update flags to Almost Full state. It should be noted that this flag update read does not require $\overline{ENR}$ = LOW, so a free-running read clock will initiate the flag update cycle.

When updating the flags, the CY7C441/443 decide whether or not the opposite clock was recognized when a clock updates the flag. For example, if a write occurs at least t_{SKEW1} after a read when updating the Empty flag, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates the flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Almost Full) is different from that used to update the boundary flag (Empty). Both operations are described below.

Boundary Flag (Empty)

The Empty flag is synchronized to the CKR signal. The Empty flag can only be updated by a clock pulse on the CKR pin. An empty FIFO that is written to will be described with an Empty flag state until a clock pulse is presented on the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Intermediate or Empty to Almost Full), a clock cycle on the CKR is necessary to update the flags to the current state. Such a state (flags displaying empty even though data has been written to the FIFO) would require two read cycles to read data out of FIFO. The first read serves only to update the flags to the Almost Empty, Intermediate, or Almost Full state, and the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flags are updated regardless of the $\overline{ENR}$ state. Therefore the update occurs even when $\overline{ENR}$ is deasserted (HIGH) so that a valid read is not necessary to update the flags to correctly describe the FIFO. With a free-running clock connected to CKR, the flag updates with each cycle. *Table 2* shows sample operations that update the Empty flag.

Although a Full flag is not supplied externally on the CY7C441/CY7C443, a Full flag exists internally. The operation of the FIFO at the Full boundary is analogous to its operation at the Empty boundary. See the text section "Boundary Flags (Full)" in the CY7C451/CY7C453 datasheet.

Non-Boundary Flags (Almost Empty, Almost Full)

The flag status pins, F_1 and F_2, exhibit the Almost Empty status when both the CY7C441 and the CY7C443 contain 16 words or less. The Almost Full Flag becomes active when the FIFO contains 16 or less empty locations. The CY7C441 becomes Almost Full when it contains 496 words. The CY7C443 becomes Almost Full when it contains 2032 words. The Almost Empty flag (like the Empty flag) is synchronous to the CKR signal, whereas the Almost Full flag is synchronous to the CKW signal. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO state. For example, if the FIFO just reaches the Almost Empty state (16 words) and then two words are written, a read clock (CKR) will be required to update the flags to the Intermediate state. However, unlike the boundary (Empty) flag's update cycle, the state of the enable pin ($\overline{ENR}$ in this case) affects the operation. Therefore, ENR set-up (t_{SEN}) and hold (t_{HEN}) times must be met. If $\overline{ENR}$ is asserted ($\overline{ENR}$=LOW) during the latent cycle, the count and data update in addition to F1 and F2. If $\overline{ENR}$ is not active ($\overline{ENR}$=1) during the flag update cycle, only the flag is updated.

The same principles apply for updating the flags when a transition from the Almost Full to the Intermediate state occurs. If the CY7C443 just reaches the Almost Full state (2032 words) and then two words are read, a write clock (CKW) will be required to update the flag to the Intermediate state. If $\overline{ENW}$ is LOW during the flag update cycle, the count and data update in addition to the flags. If $\overline{ENW}$ is HIGH, only the flag is updated. Therefore, $\overline{ENW}$ set-up (t_{SEN}) and hold (t_{HEN}) times must be met. *Tables 3* and *4* show examples for a sequence of operations that affect the Almost Empty and Almost Full flags, respectively.

Width Expansion

The CY7C441/3 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode, all control inputs are common. When the FIFO is being read near

the Empty boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty condition on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width expanded devices (A and B), device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored).The first write occurs because a read within t_{SKEW2} of the first write is only guaranteed to be either recognized or ignored, but which of the two is not guaranteed. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to outpout "staggered" data assuming more data has been written to the FIFOs.

In the width expansion configuration, any of the devices' flags may be monitored for the composite Almost Full status.

Table 2. Empty Flag Operation Example [29]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Write ($\overline{ENW}$ = LOW)	Empty	0	0	2	Write
Empty	0	0	2	Read ($\overline{ENR}$ = HIGH)	AE	1	0	2	Flag Update
AE	1	0	2	Read ($\overline{ENR}$ = LOW)	AE	1	0	1	Read
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition for Almost Empty to Empty)
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	Flag Update
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition from Almost Empty to Empty)

Table 3. Almost Empty Flag Operation Example[29]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
AE	1	0	16	Write ($\overline{ENW}$ = LOW)	AE	1	0	17	Write
AE	1	0	17	Write ($\overline{ENW}$ = LOW)	AE	1	0	18	Write
AE	1	0	18	Read ($\overline{ENR}$ = LOW)	Intermediate	1	1	17	Flag Update and Read
Intermediate	1	1	17	Read ($\overline{ENR}$ = LOW)	AE	1	0	16	Read (Transition from Intermediate to Almost Empty)
AE	1	0	16	Read ($\overline{ENR}$ = HIGH)	AE	1	0	16	Ignored Read

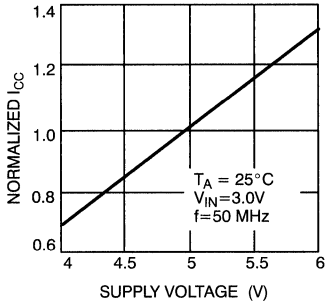
Table 4. Almost Full Flag Operation Example[30,31]

Status Before Operation						Next State of FIFO	Status After Operation				
Current State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Operation		F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Comments
AF	0	1	496	2032	Read ($\overline{ENR}$=LOW)	AF	0	1	495	2031	Read
AF	0	1	495	2031	Read ($\overline{ENR}$=LOW)	AF	0	1	494	2030	Read
AF	0	1	494	2030	Write ($\overline{ENW}$=HIGH)	Intermediate	1	1	494	2030	Flag Update
Intermediate	1	1	494	2030	Write ($\overline{ENW}$=LOW)	Intermediate	1	1	495	2031	Write
Intermediate	1	1	495	2031	Write ($\overline{ENW}$=LOW)	AF	0	1	496	2032	Write (Transition from Intermediate to Almost Full)

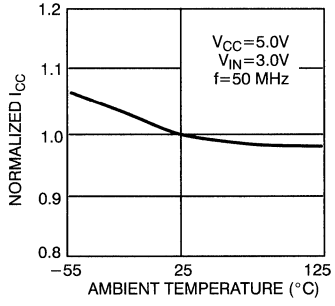
Notes:
29. Applies to both the CY7C441 and CY7C443 operations.
30. The CY7C441 Almost Full state is represented by 496 or more words.
31. The CY7C443 Almost Full state is represented by 2032 or more words.

Typical DC and AC Characteristics

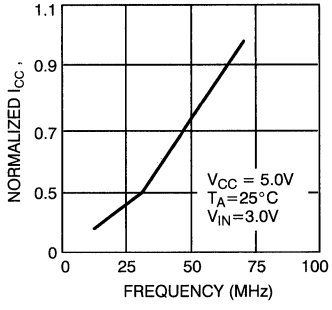
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



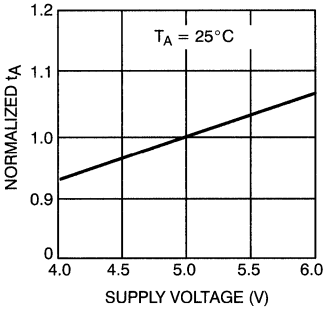
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



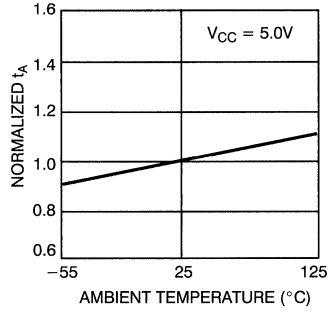
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



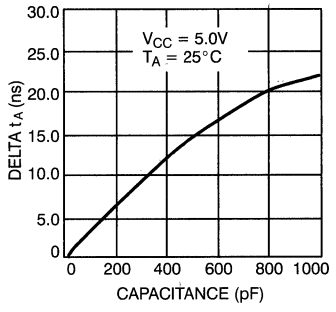
NORMALIZED t_A vs. SUPPLY VOLTAGE



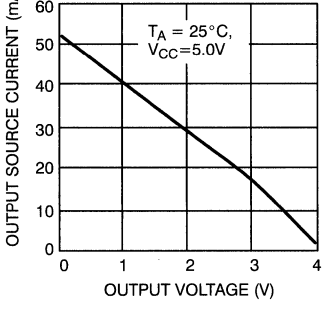
NORMALIZED t_A vs. AMBIENT TEMPERATURE



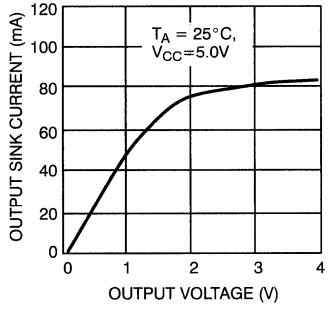
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C441–14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441–14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441–14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C441–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441–20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441–20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C441–30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441–30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441–30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C443–14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443–14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443–14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C443–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443–20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443–20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C443–30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443–30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443–30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{SB}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CKR}	9, 10, 11
t_{CKW}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{HENR}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11

Document #: 38–00124–F

CY7C451
CY7C453

512 x 9 Cascadable Clocked and 2K x 9 Cascadable Clocked FIFOs with Programmable Flags

Features

- **512 x 9 (CY7C451) and 2,048 x 9 (CY7C453) FIFO buffer memory**
- **Expandable in width and depth**
- **High-speed 70-MHz standalone; 50-MHz cascaded**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Almost Empty, Half Full, Almost Full, and Full status flags**
- **Programmable Almost Full/Empty flags**
- **Parity generation/checking**
- **Fully asynchronous and simultaneous read and write operation**
- **Output Enable ($\overline{OE}$)**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Available in 300-mil 32-pin DIP, PLCC, and LCC packages**
- **Proprietary 0.8μ CMOS technology**
- **Low power**
  — **I_{CC}=70 mA**

Functional Description

The CY7C451 and CY7C453 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C451 has a 512-word by 9-bit memory array, while the CY7C453 has a 2048-word by 9-bit memory array. Devices can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

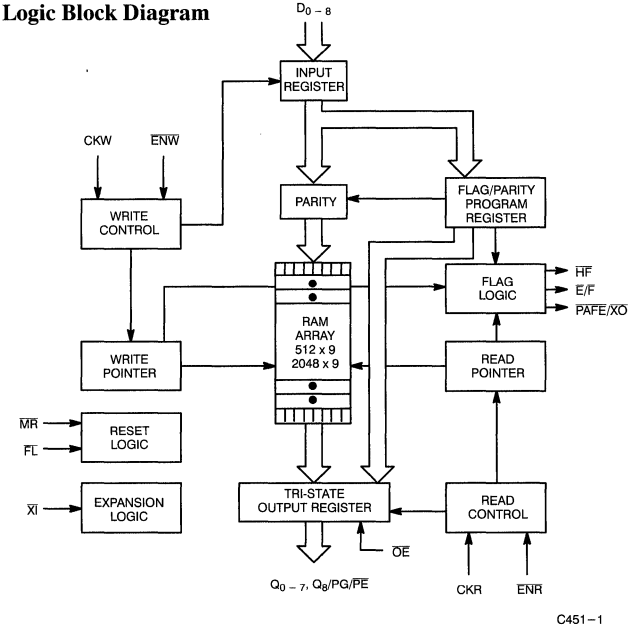
Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle.

The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are acceptable in the standalone configuration, and up to 50 MHz is acceptable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$) and cascade output ($\overline{XO}$). The $\overline{XO}$ signal is connected to the $\overline{XI}$ of the next device, and the $\overline{XO}$ of the last device should be connected to the $\overline{XI}$ of the first device. In standalone mode, the input ($\overline{XI}$) pin is simply tied to V_{SS}.

The CY7C451 and CY7C453 provide three status pins to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) and $\overline{XO}$ functions share the same pin. The Almost Empty/Full flag is

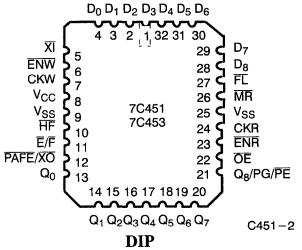
Logic Block Diagram



C451–1

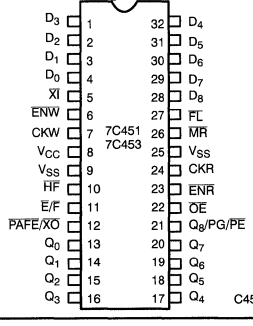
Pin Configurations

PLCC/LCC
Top View



C451–2

DIP
Top View



C451–3

Functional Description (continued)

valid in the standalone and width expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C451 and the CY7C453 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

Selection Guide

		7C451–14 7C453–14	7C451–20 7C453–20	7C451–30 7C453–30
Maximum Frequency (MHz)		71.4[1]	50	33.3
Maximum Cascadable Frequency		N/A[2]	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[3]	−55°C to +125°C	5V ± 10%

Notes:

1. 71.4-MHz operation is available only in the standalone configuration.
2. The −14 device cannot be cascaded.
3. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-8}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW then data is written into the FIFO's programming register. D_8 is ignored if the device is configured for parity generation.
Q_{0-7}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR then data is read from the programming register.
Q_8/PG/$\overline{PE}$	O	Function varies according to mode: Parity disabled – same function as Q_{0-7} Parity enabled, generation – parity generation bit (PG) Parity enabled, check – Parity Error Flag ($\overline{PE}$)
$\overline{ENW}$	I	Enable Write: enables the CKW input (for both non-program and program modes)
$\overline{ENR}$	I	Enable Read: enables the CKR input (for both non-program and program modes)
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag – synchronized to CKW.
$\overline{E}$/$\overline{F}$	O	Empty or Full Flag – $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW
$\overline{PAFE}$/$\overline{XO}$	O	Dual-Mode Pin: Not Cascaded – Programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR Cascaded – Expansion Out signal, connected to $\overline{XI}$ of next device
$\overline{XI}$	I	Not Cascaded – $\overline{XI}$ is tied to V_{SS} Cascaded – Expansion Input, connected to $\overline{XO}$ of previous device
$\overline{FL}$	I	First Load Pin: Cascaded – the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure2*) Not Cascaded – tied to V_{CC}
$\overline{MR}$	I	Master Reset: resets device to empty condition. Non-Programming Mode: program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of $\overline{CKW}$. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7} and Q_8/PG/$\overline{PE}$ pins

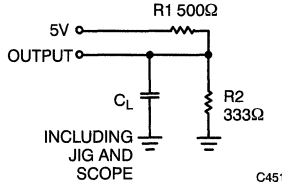
Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C451–14 7C453–14 Min.	7C451–14 7C453–14 Max.	7C451–20 7C453–20 Min.	7C451–20 7C453–20 Max.	7C451–30 7C453–30 Min.	7C451–30 7C453–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}[5]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[5]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	µA
I_{OS}[6]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+ 10	µA
I_{CC1}[7]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		120		100	mA
			Mil/Ind		150		130		110	mA
I_{CC2}[8]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70	mA
			Mil/Ind		80		80		80	mA
I_{SB}[9]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
			Mil/Ind		30		30		30	mA

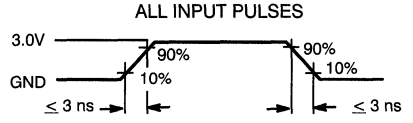
Capacitance[10]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms[11, 12, 13, 14, 15]

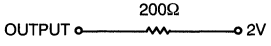


C451–4



C451–5

Equivalent to: THÉVENIN EQUIVALENT



Notes:

4. See the last page of this specification for Group A subgroup testing information.
5. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.
6. Test no more than one output at a time for not more than one second.
7. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
8. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
9. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
10. Tested initially and after any design or process changes that may affect these parameters.
11. C_L = 30 pF for all AC parameters except for t_{OHZ}.
12. C_L = 5 pF for t_{OHZ}.
13. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
14. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
15. t_{OHZ} is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}.

Switching Characteristics Over the Operating Range[4, 16]

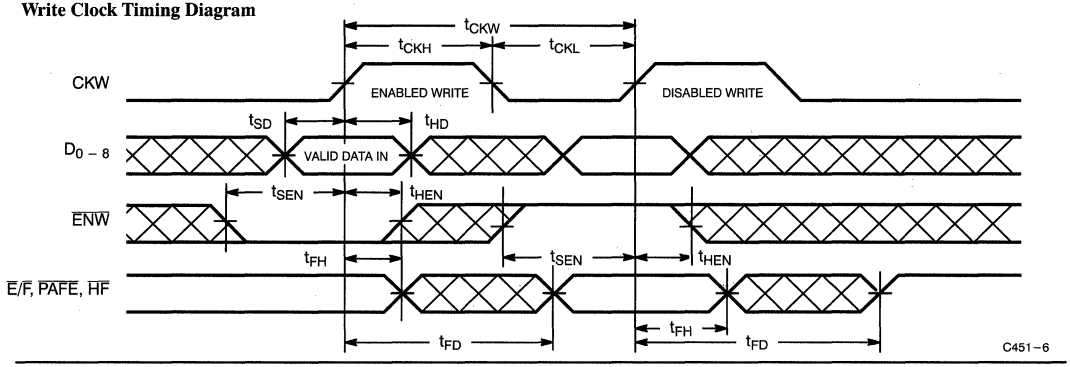
Parameter	Description	7C451–14 7C453–14		7C451–20 7C453–20		7C451–30 7C453–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A[17]	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	7		9		12		ns
t_{HD}	Data Hold	0		0		0		ns
t_{SEN}	Enable Set-Up	7		9		12		ns
t_{HEN}	Enable Hold	0		0		0		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		10		15		20	ns
t_{OLZ}[10, 18]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		ns
t_{OHZ}[10, 18]	$\overline{OE}$ HIGH to Output Data in High Z		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[19]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[20]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	10		15		25		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t_{AP}	Program Mode—Data Access Time		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		ns

Notes:

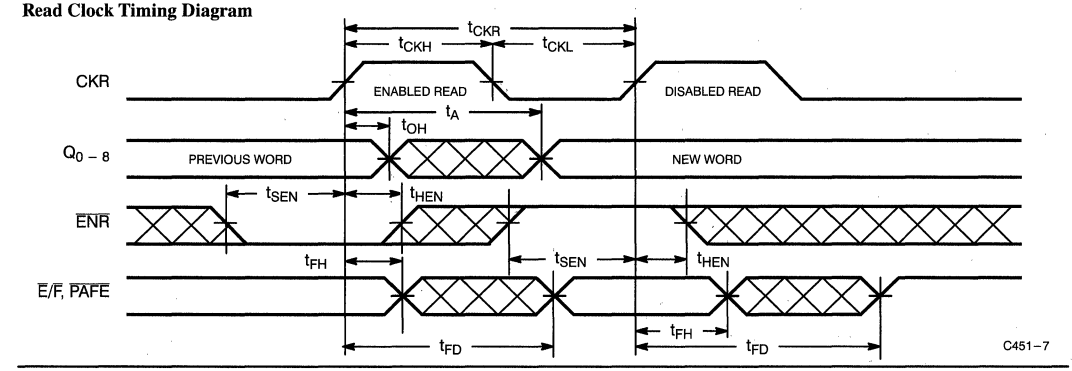
16. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 11 and 12, unless otherwise specified.
17. Access time includes all data outputs switching simultaneously.
18. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
19. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, CKR is the clock for Empty and Almost Empty flags.
20. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 19 for definition of clock and opposite clock.

Switching Waveforms

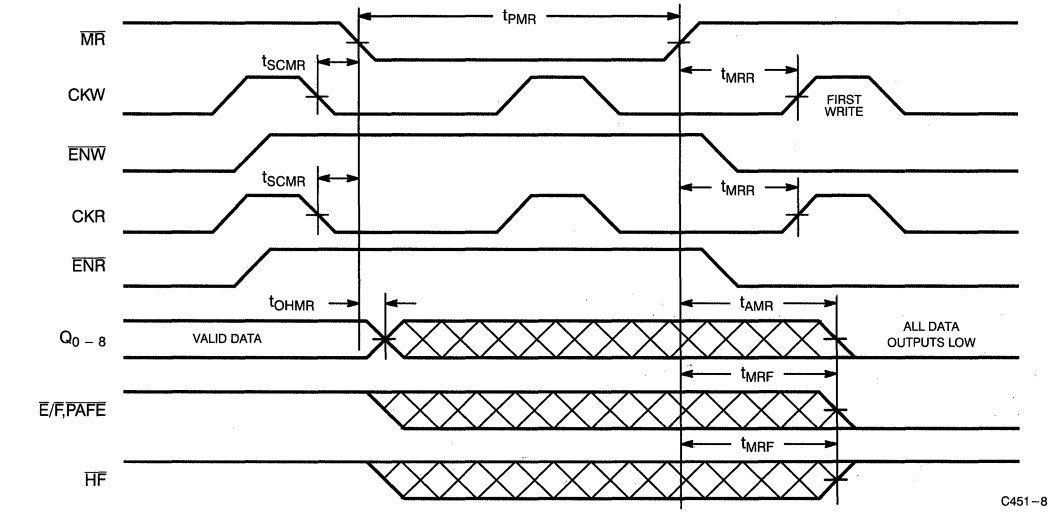
Write Clock Timing Diagram



Read Clock Timing Diagram

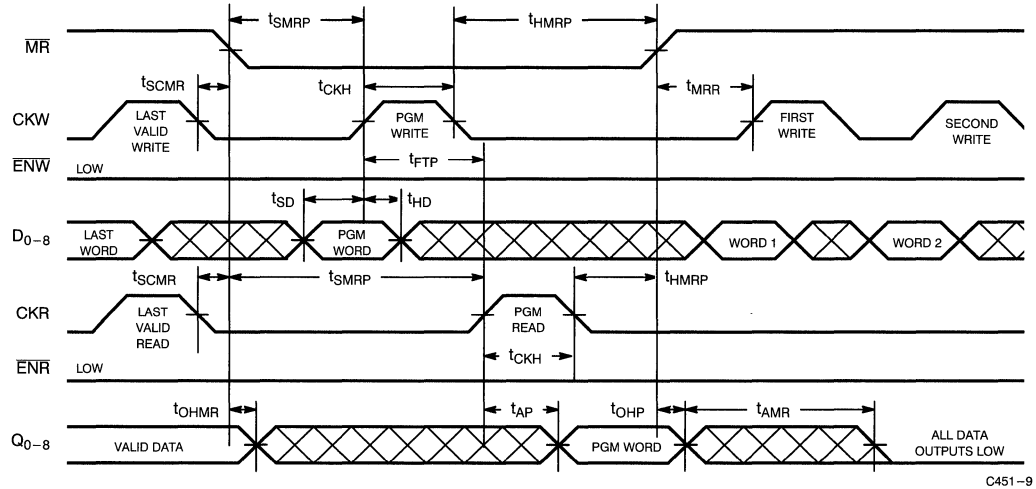


Master Reset (Default with Free-Running Clocks) Timing Diagram[21, 22, 23, 24]

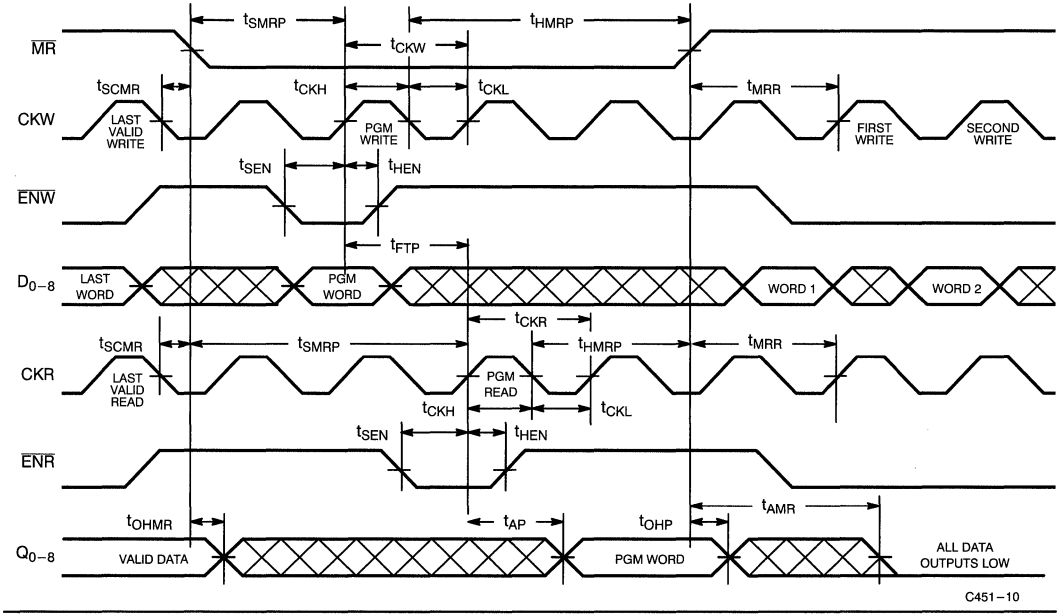


Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[23, 24]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[23, 24]

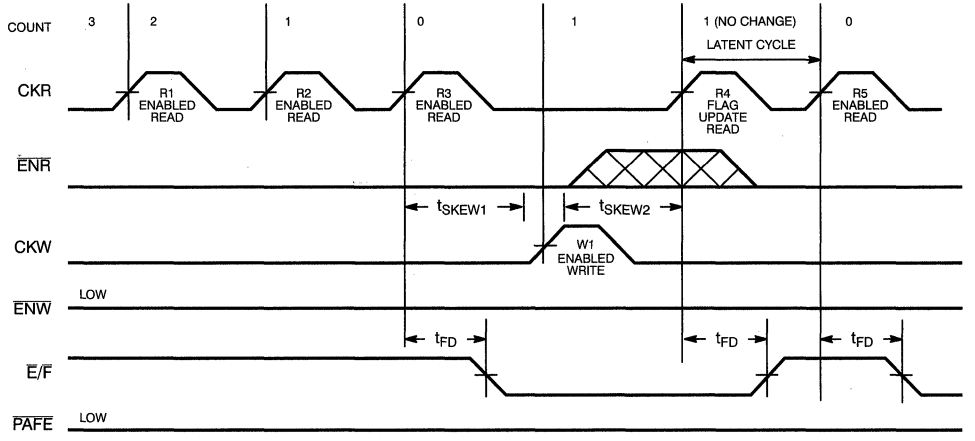


Notes:

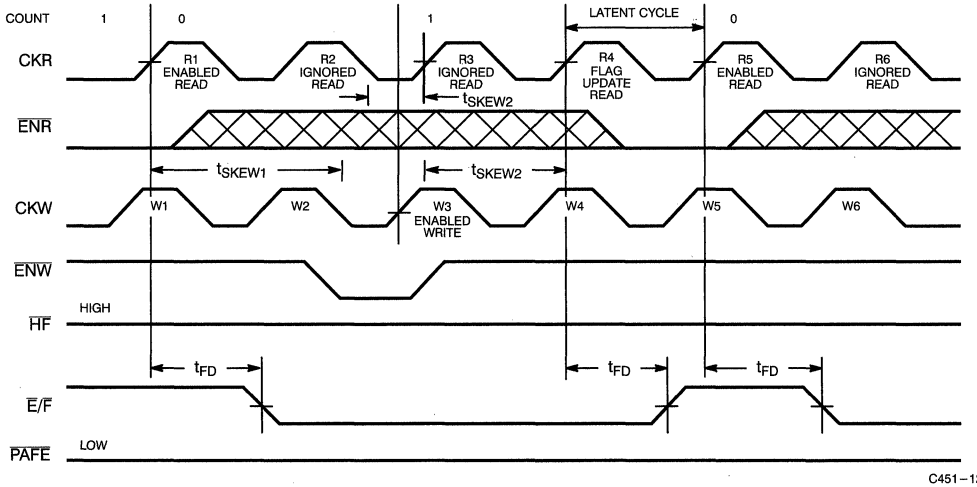
21. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
22. To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
23. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
24. In this example, Q_{0-8} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)

Read to Empty Timing Diagram[25, 28, 29]



Read to Empty Timing Diagram with Free-Running Clocks[25, 26, 27, 28]

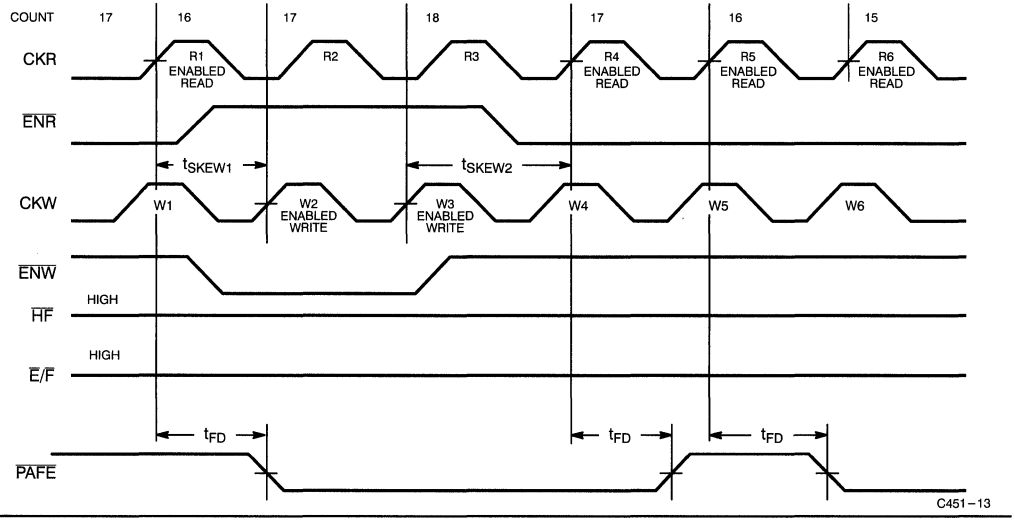


Notes:

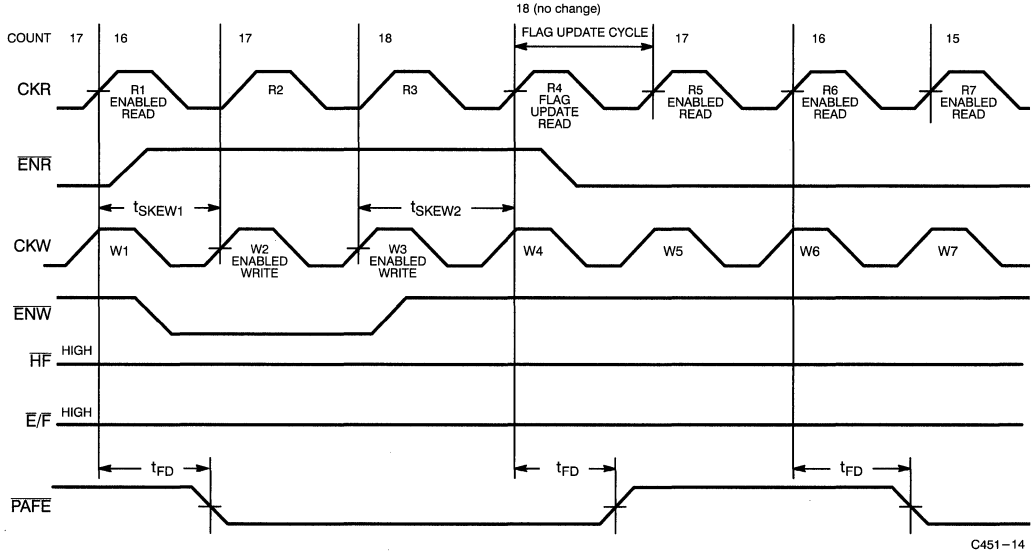
25. "Count" is the number of words in the FIFO.
26. The FIFO is assumed to be programmed with P > 0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
27. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
28. CKR is clock; CKW is opposite clock.
29. R3 updates the flag to the Empty state by asserting $\overline{E}/\overline{F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[25, 28, 30]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[25, 28, 30, 31, 32]

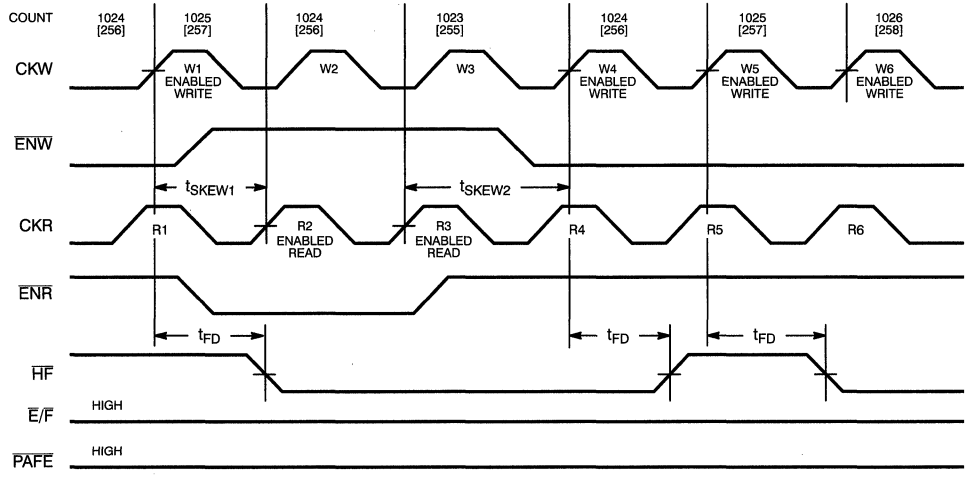


Notes:

30. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
31. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
32. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ⧫18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

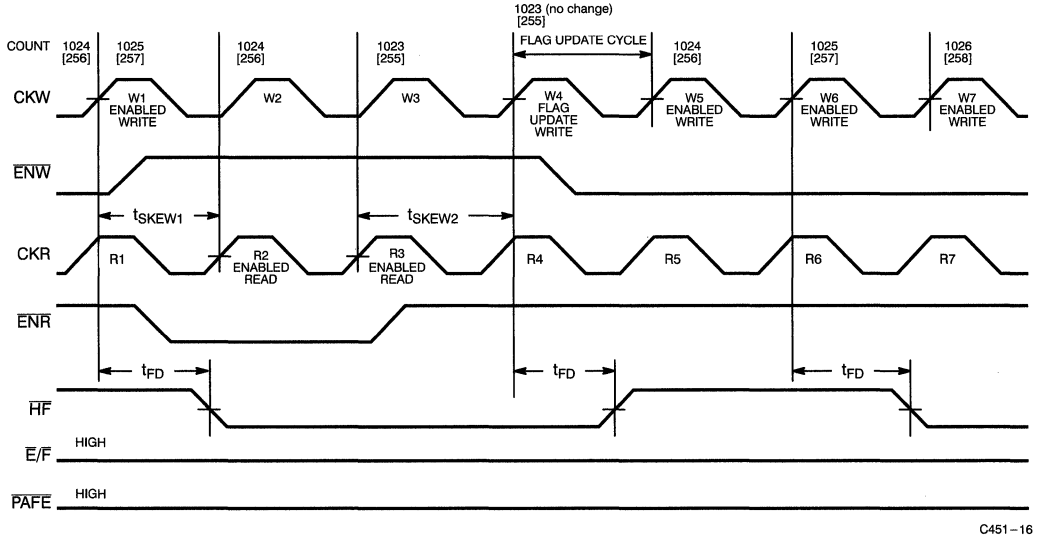
Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[25, 33, 34, 35]



C451–15

Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[25, 33, 34, 35, 36, 37]



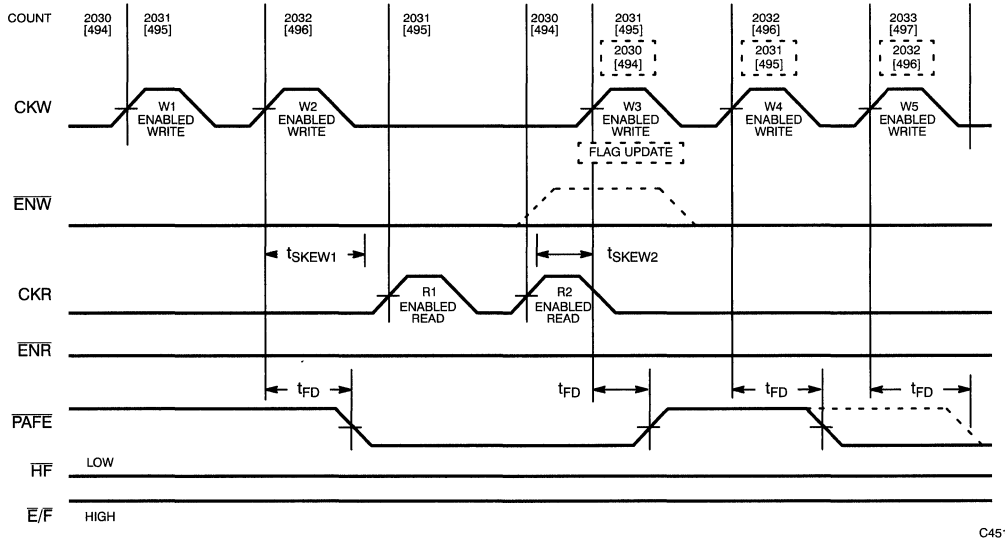
C451–16

Notes:

33. CKW is clock and CKR is opposite clock.
34. Count = 1,025 indicates Half Full for the CY7C453 and count = 257 indicates Half Full for the CY7C451. Values for CY7C451 count are shown in brackets.
35. When the FIFO contains 1,024 [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
36. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
37. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (1,025 ➧ 1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

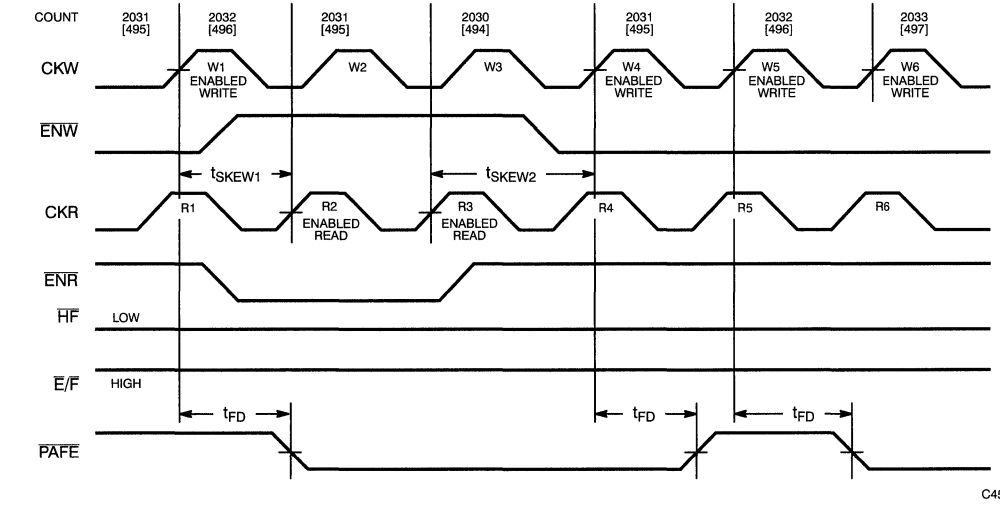
Switching Waveforms (continued)

Write to Almost Full Timing Diagram[25, 30, 33, 38, 39]



C451–17

Write to Almost Full Timing Diagram with Free-Running Clocks[25, 30, 33]



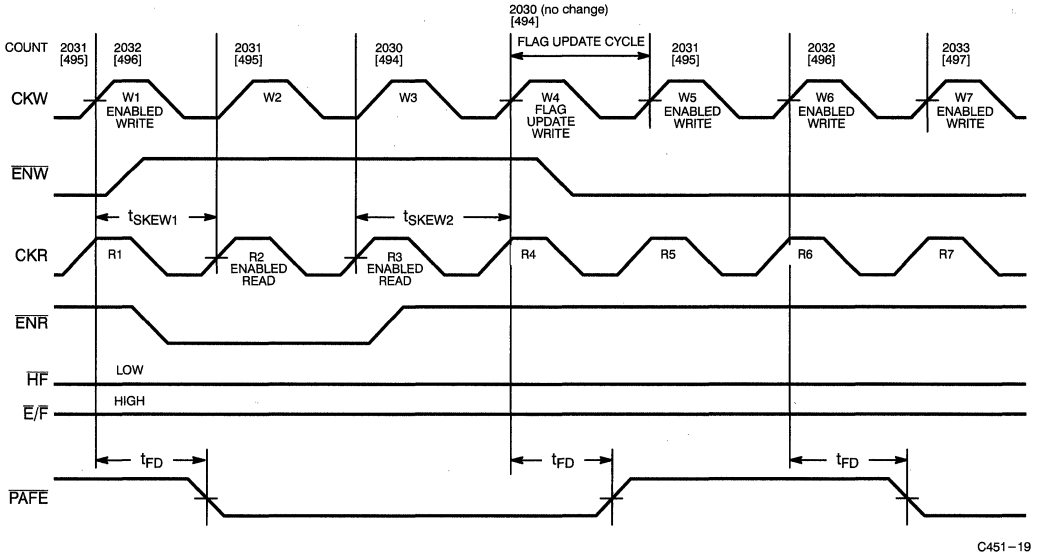
C451–18

Notes:

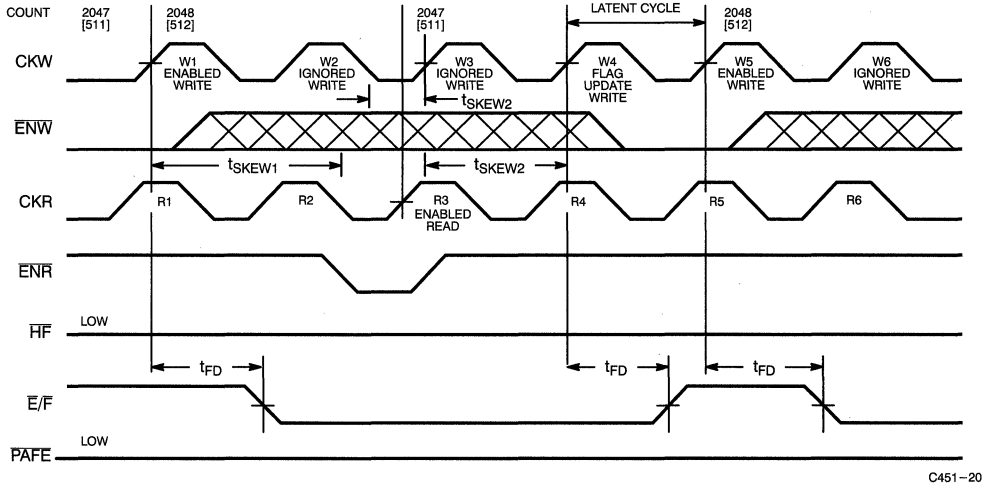
38. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
39. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[25, 30, 33]



Write to Full Flag Timing Diagram with Free-Running Clocks[25, 26, 33, 40]

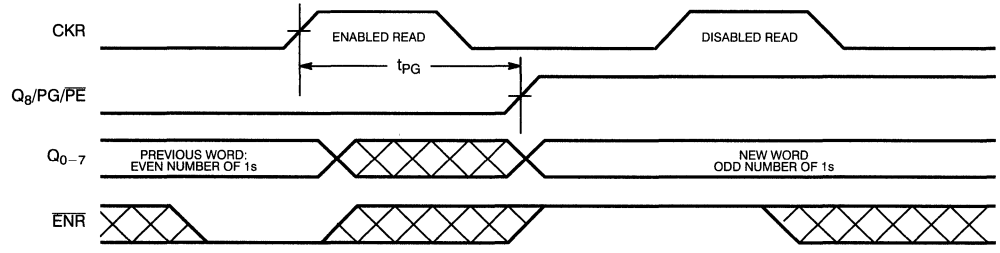


Note:

40. W2 is ignored because the FIFO is full (count = 2,048 [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

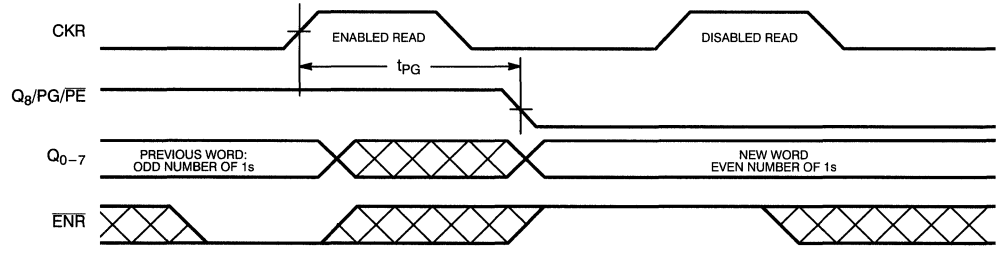
Switching Waveforms (continued)

Even Parity Generation Timing Diagram[41, 42]



C451–21

Even Parity Generation Timing Diagram[41, 43]



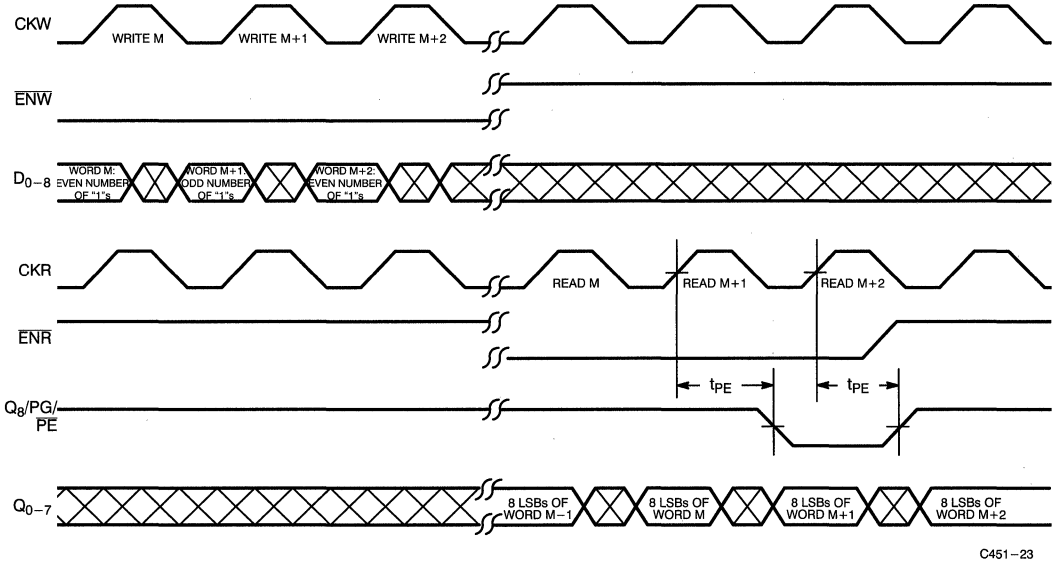
C451–22

Notes:

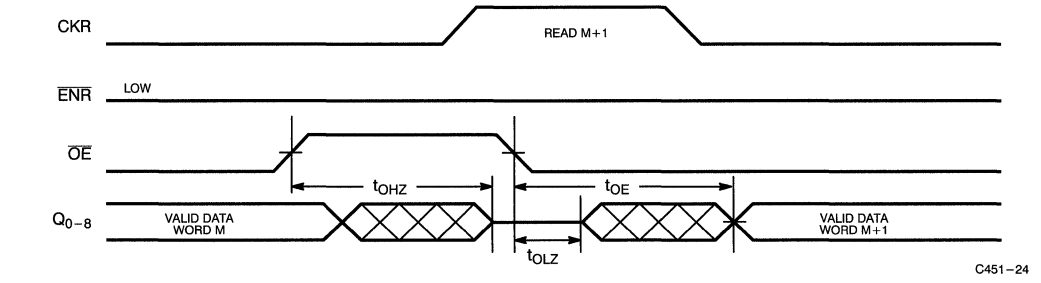
41. In this example, the FIFO is assumed to be programmed to generate even parity.
42. If Q_{0-7} "new word" also has an even number of 1s, then PG stays LOW.
43. If Q_{0-7} "new word" also has an odd number of 1s, then PG stays HIGH.

Switching Waveforms (continued)

Even Parity Checking[44]



Output Enable Timing[45, 46]



Notes:

44. In this example, the FIFO is assumed to be programmed to check for even parity.
45. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$.
46. If $\overline{ENR}$ was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

Architecture

The CY7C451 and CY7C453 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{CKR}$, $\overline{CKW}$, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$, $\overline{OE}$, $\overline{FL}$, $\overline{XI}$, $\overline{XO}$), and flags ($\overline{HF}$, $\overline{E/F}$, $\overline{PAFE}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{E/F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-8}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to tri-state the Q_{0-8} outputs when $\overline{OE}$ is not asserted. When $\overline{OE}$ is enabled, data in the output register will be available to Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Programming

The CY7C451 and CY7C453 are programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write D_{0-8} inputs into the programming register. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set–up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on D_{0-5} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in 1 refers to the decimal equivalent of the binary number represented by D_{0-5}. Programming options for the CY7C451 and CY7C453 are listed in *Table 5*. Programming resolution is 16 words for either device.

The programmable $\overline{PAFE}$ function is only valid when the CY7C451/453 are not cascaded. If the user elects not to program the FIFO's flags, the default (P=1) is as follows: Almost Empty condition (Almost Full condition) is activated when the CY7C451/453 contain 16 or less words (empty locations).

Parity is programmed with the D_{6-8} bits. See *Table 6* for a summary of the various parity programming options. Data present on D_{6-8} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-8} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C451/453 provide three status pins when not cascaded. The three pins, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when FIFOs are cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate. See *Figure 1.*). The synchronous architecture guarantees some minimum valid time for the flags. The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock (CKW). For example, if the CY7C453 FIFO contains 2047 words (2048 words indicate Full for the CY7C453), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Table 1. Flag Truth Table[47]

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State	CY7C451 512 x 9 Number of Words in FIFO	CY7C453 2K x 9 Number of Words in FIFO
0	0	1	Empty	0	0
1	0	1	Almost Empty	1 ➧ (16 • P)	1 ➧ (16 • P)
1	1	1	Less than or Equal to Half Full	(16 • P)+1 ➧ 256	(16 • P)+1 ➧ 1024
1	1	0	Greater than Half Full	257 ➧ 511 – (16 • P)	1025 ➧ 2047 – 16 • P
1	0	0	Almost Full	512 – (16 • P) ➧ 511	2048 – (16 • P) ➧ 2047
0	0	0	Full	512	2048

Note:

47. P is the decimal value of the binary number represented by D_{0-5}. When programming the CY7C451/53, P can have values from 0 to 15 for the CY7C451 and values from 0 to 63 for the CY7C453. See *Table 5* for D_{0-5} representation. P = 0 signifies Almost Empty state = Empty state.

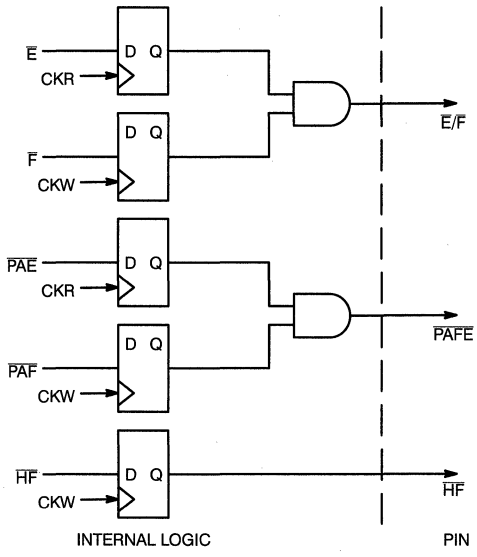


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the CY7C451/453 must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on the CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read cycles are required to read data out of FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is unasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on the CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C451/453 feature programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at a distance of up to 1008 words/locations for the CY7C453 (240 words/locations for the CY7C451) from the Empty/Full boundary. The programming resolution is 16 words/locations. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

The default distance (CY7C451/453 not programmed) from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Tables 3* and *4* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

Programmable Parity

The CY7C451/453 also features even or odd parity checking and generation. D_{6-8} are used during a program write to describe the parity option desired. *Table 6* gives a summary of programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on one multimode output pin (Q8/PG/$\overline{PE}$). The three possible modes are described in the following paragraphs. Regardless of the mode selected, the $\overline{OE}$ pin retains tri-state control of all 9 Q_{0-8} bits.

Parity Disabled (Q8 mode)

When parity is disabled (or user does not program parity option) the CY7C451/453 stores all 9 bits present on D_{0-8} inputs internally and will output all 9 bits on Q_{0-8}.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7}. D_8 input is ignored. The parity bit is stored internally as D_8 and during a subsequent read will be available on the PG pin along with the data word from which the parity was generated (Q_{0-7}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the CY7C451/453 is programmed for parity checking, the FIFO will compare the parity of D_{0-8} with the program register. If the expected parity is present, D_8 will be set HIGH internally. When this word is later read, $\overline{PE}$ will be HIGH. If a parity error occurs, D_8 will be set LOW internally. When this word is later read, $\overline{PE}$ will be LOW. For example, if parity check is set to odd and D_{0-8} have an even number of 1s, a parity error occurs. When that word is later read, $\overline{PE}$ will be asserted (LOW).

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. The CY7C451/453 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C451/453 can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with

$\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-8}, Q_{0-8}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-8} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-8} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-8} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C451/453 are cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-8} during a program read. Q_{0-8} of all other devices will remain in a high-impedance state to avoid bus contention.

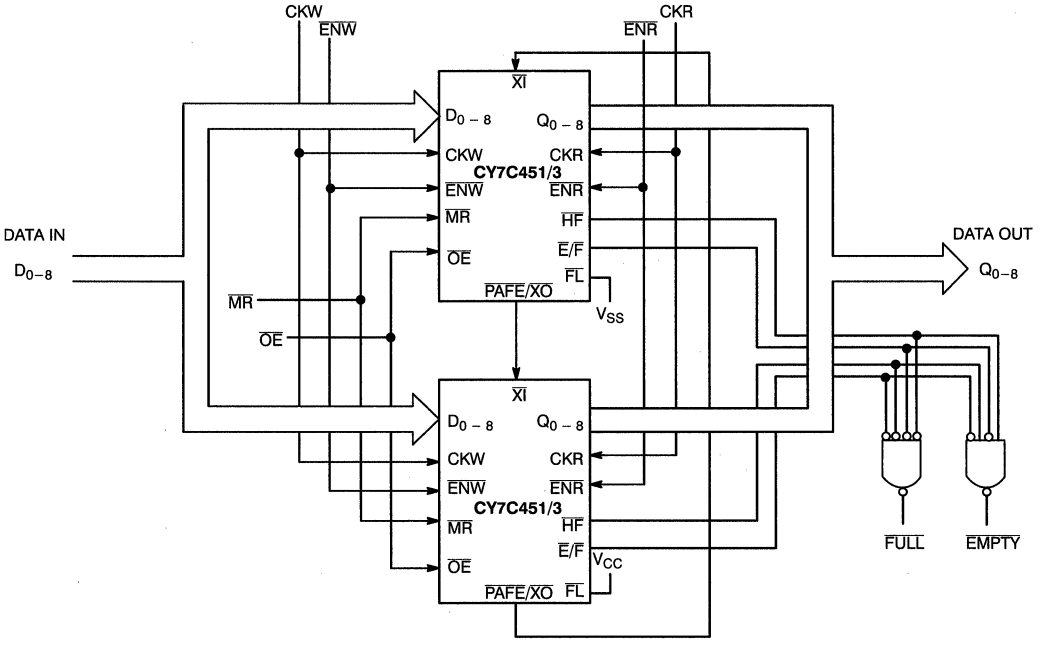


Figure 2. Depth Expansion with CY7C451/3

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[48]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (Transition from <HF to AE)

Table 4. Almost Full Flag Operation Example[49]

Status Before Operation							Status After Operation						
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453	Comments
AF	1	0	0	496	2032	Read ($\overline{ENR}$ = 0)	AF	1	0	0	495	2031	Read
AF	1	0	0	495	2031	Read ($\overline{ENR}$ = 0)	AF	1	0	0	494	2030	Read
AF	1	0	0	494	2030	Write ($\overline{ENW}$ = 1)	>HF	1	1	0	494	2030	Flag Update
>HF	1	1	0	494	2030	Write ($\overline{ENW}$ = 0)	>HF	1	1	0	495	2031	Write
>HF	1	1	0	495	2031	Write ($\overline{ENW}$ = 0)	AF	1	0	0	496	2032	Write (Transition from >HF to AF)

Notes:
48. Applies to both CY7C451 and CY7C453 operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.
49. Programmed so that Almost Full becomes active when the FIFO contains 16 or less empty locations.

Table 5. Programmable Almost Full/Almost Empty Options – CY7C451/CY7C453[50]

D5	D4	D3	D2	D1	D0	PAFE Active when CY7C451/453 is:	P[51]
0	0	0	0	0	0	Completely Full and Empty.	0
0	0	0	0	0	1	16 or less locations from Empty/Full (default)	1
0	0	0	0	1	0	32 or less locations from Empty/Full	2
0	0	0	0	1	1	48 or less locations from Empty/Full	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	1	1	1	0	224 or less locations from Empty/Full	14
0	0	1	1	1	1	240 or less locations from Empty/Full	15
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	992 or less locations from Empty/Full	62
1	1	1	1	1	1	1008 or less locations from Empty/Full	63

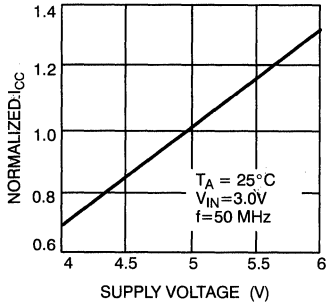
Table 6. Programmable Parity Options

D8	D7	D6	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

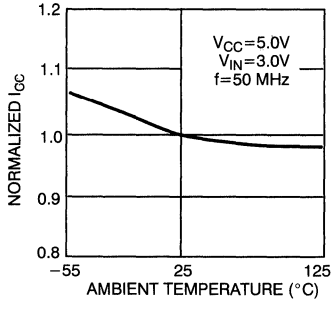
Notes:
50. D4 and D5 are don't care for CY7C451.
51. Referenced in *Table 1*.

Typical DC and AC Characteristics

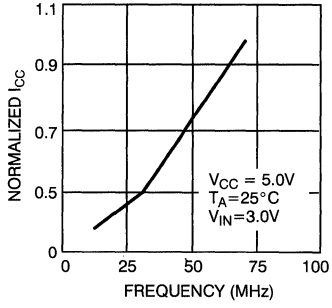
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



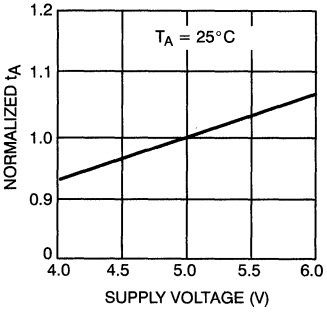
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



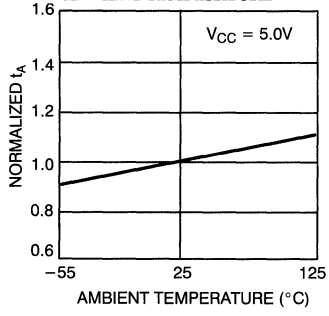
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



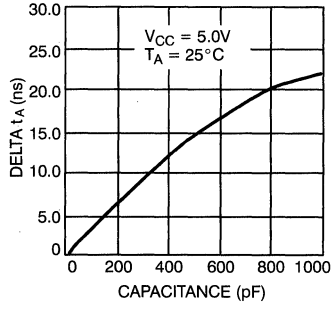
NORMALIZED t_A vs. SUPPLY VOLTAGE



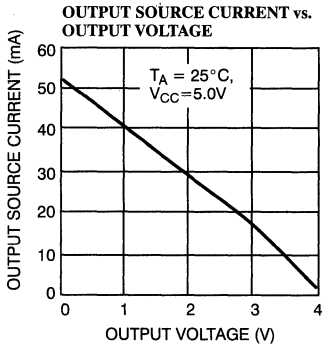
NORMALIZED t_A vs. AMBIENT TEMPERATURE



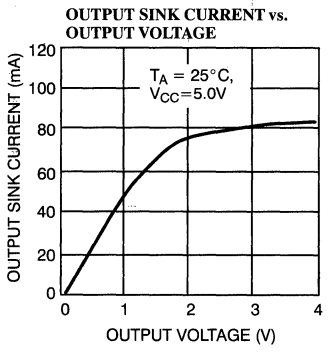
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C451–14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451–14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C451–20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C451–30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–30JI	D32	32-Lead (300-Mil) CerDIP	Industrial
	CY7C451–30DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

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	CY7C453–14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C453–20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C453–30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–30DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{SB}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CKW}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{OE}	9, 10, 11
t_{PG}	9, 10, 11
t_{PE}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11
t_{SMRP}	9, 10, 11
t_{HMRP}	9, 10, 11
t_{FTP}	9, 10, 11
t_{AP}	9, 10, 11
t_{OHP}	9, 10, 11

Document #: 38−00125−E

CY7C455
CY7C456
CY7C457

512 x 18, 1K x 18, and 2K x 18 Cascadable Clocked FIFOs with Programmable Flags

Features

- **512 x 18 (CY7C455), 1,024 x 18 (CY7C456), 2,048 x 18 (CY7C457) FIFO buffer memory**
- **Expandable in width**
- **Expandable in depth**
- **High-speed 70-MHz standalone; 50-MHz cascaded**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags**
- **Parity generation/checking**
- **Fully asynchronous and simultaneous read and write operation**
- **Output Enable ($\overline{OE}$) pin**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **52-pin PLCC and 52-pin PQFP**
- **Proprietary 0.8µ CMOS technology**
- **TTL compatible**

Functional Description

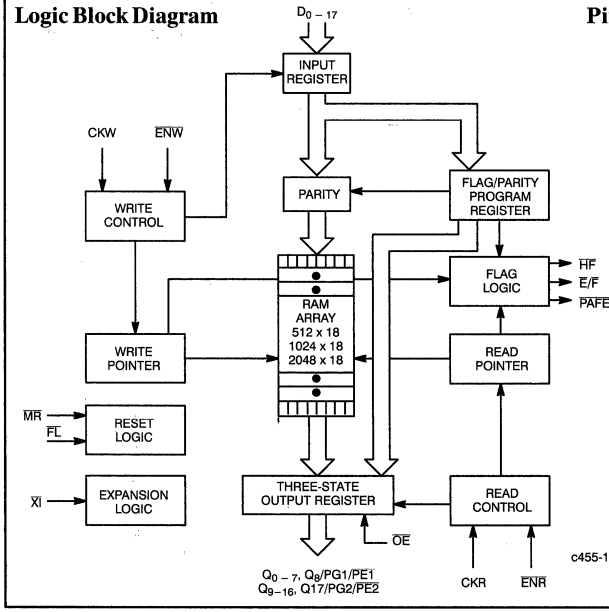
The CY7C455, CY7C456, and CY7C457 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C455 has a 512-word memory array, the CY7C456 has a 1,024-word memory array, and the CY7C457 has a 2,048-word memory array. The CY7C455, CY7C456, and CY7C457 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$).

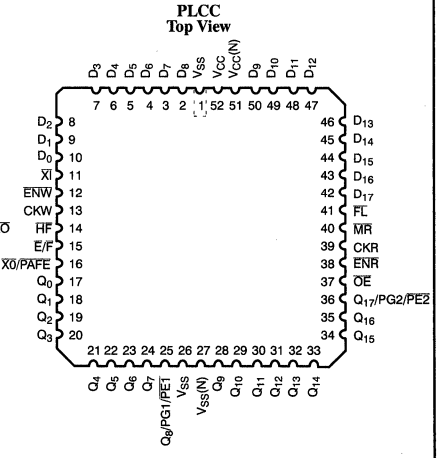
When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). In addition, the CY7C455, CY7C456, and CY7C457 have an output enable pin ($\overline{OE}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are achievable in the standalone configuration, and up to 50 MHz is achievable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$), cascade output ($\overline{XO}$), and First Load ($\overline{FL}$) pins. The $\overline{XO}$ pin is connected to the $\overline{XI}$ pin of the next device, and the $\overline{XO}$ pin of the last device should be connected to the $\overline{XI}$ pin of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS}.

Logic Block Diagram

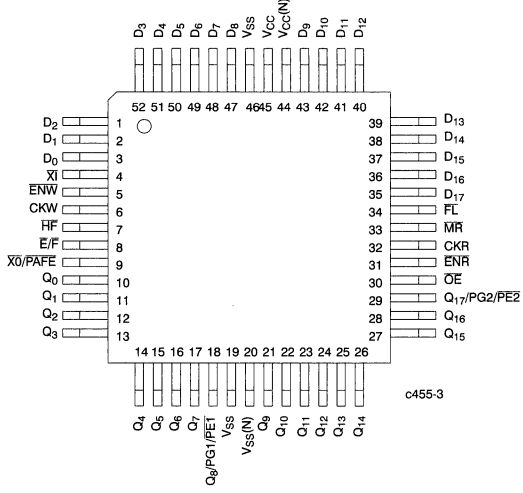


Pin Configuration



Pin Configurations (continued)

PQFP
Top View



Functional Description (continued)

The CY7C455, CY7C456, and CY7C457 provide three status pins. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) shares the $\overline{XO}$ pin on the CY7C455, CY7C456, and CY7C457. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time. This time is typically equal to approximately one cycle time.

The CY7C45X uses center power and ground for reduced noise. All configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings and a substrate bias generator.

5

Selection Guide

		7C45X–14	7C45X–20	7C45X–30
Maximum Frequency (MHz)		71.4[1]	50	33.3
Maximum Cascadable Frequency		N/A	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		5	7	9
Minimum Data or Enable Hold (ns)		1	1	1
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	160	140	120
	Industrial	180	160	140

	CY7C455	CY7C456	CY7C457
Density	512 x 18	1,024 x 18	2,048 x 18
$\overline{OE}$, Depth Cascadable	Yes	Yes	Yes
Package	52-Pin LCC/PLCC/PQFP	52-Pin LCC/PLCC/PQFP	52-Pin LCC/PLCC/PQFP

Note:
1. 71.4-MHz operation is available only in the standalone configuration.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	−40°C to +85°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-17}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-17}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW, data is written into the FIFO's programming register. $D_{8,17}$ are ignored if the device is configured for parity generation.
Q_{0-7} Q_{9-16}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}, Q_{9-16}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR, data is read from the programming register.
Q_8/PG1/$\overline{PE1}$ Q_{17}/PG2/$\overline{PE2}$	O	Function varies according to mode: Parity disabled − same function as Q_{0-7} and Q_{9-16} Parity enabled, generation − parity generation bit (PG_x) Parity enabled, check − Parity Error Flag ($\overline{PE_x}$)
$\overline{ENW}$	I	Enable Write: Enables the CKW input (for both non-program and program modes).
$\overline{ENR}$	I	Enable Read: Enables the CKR input (for both non-program and program modes).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag: Synchronized to CKW.
$\overline{E}$/$\overline{F}$	O	Empty or Full Flag: $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW.
$\overline{PAFE}$/$\overline{XO}$	O	Dual-Mode Pin: Not Cascaded − programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR. Cascaded − expansion out signal, connected to $\overline{XI}$ of next device.
$\overline{XI}$	I	Expansion-In Pin: Not Cascaded − $\overline{XI}$ is tied to V_{SS}. Cascaded − expansion Input, connected to $\overline{XO}$ of previous device.
$\overline{FL}$	I	First Load Pin: Cascaded − the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure 1*). Not Cascaded − tied to V_{CC}.
$\overline{MR}$	I	Master Reset: Resets device to empty condition. Non-Programming Mode: Program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of CKW. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7}, Q_{9-16}, Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$ pins.

Note:
2. T_A is the "instant on" case temperature.

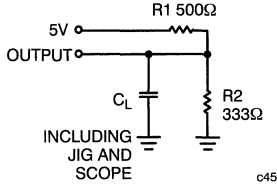
Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C45X–14 Min.	7C45X–14 Max.	7C45X–20 Min.	7C45X–20 Max.	7C45X–30 Min.	7C45X–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}[4]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[4]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	µA
I_{OS}[5]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{CC1}[6]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		160		140		120	mA
			Ind		180		160		140	mA
I_{CC2}[7]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		90		90	mA
			Ind		100		100		100	mA
I_{SB}[8]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		40		40		40	mA
			Ind		40		40		40	mA

Capacitance[9]

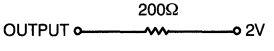
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

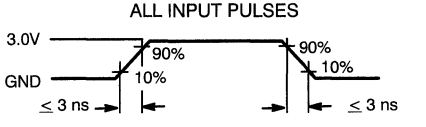
AC Test Loads and Waveforms[10, 11, 12, 13, 14]



c455-4

Equivalent to: THÉVENIN EQUIVALENT





c455-5

Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.
5. Test no more than one output at a time for not more than one second.
6. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
7. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
8. All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
9. Tested initially and after any design or process changes that may affect these parameters.
10. C_L = 30 pF for all AC parameters except for t_{OHZ}.
11. C_L = 5 pF for t_{OHZ}.
12. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
13. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
14. t_{OHZ} is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}.

Switching Characteristics Over the Operating Range[3, 15]

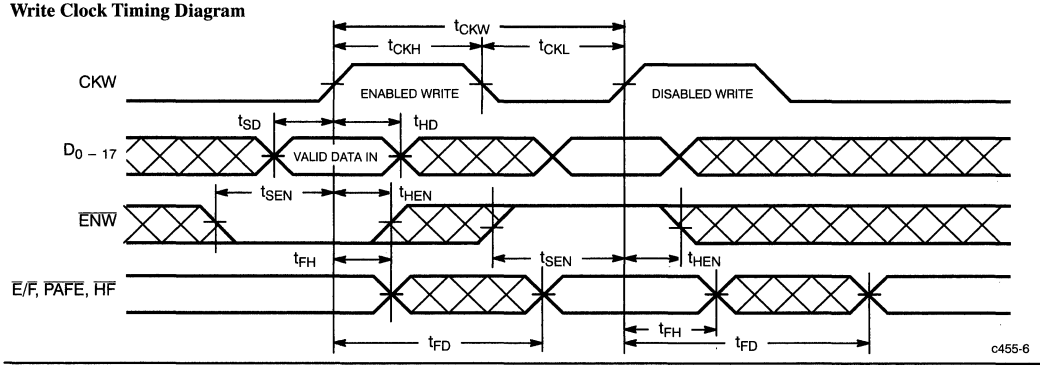
Parameter	Description	7C45X–14		7C45X–20		7C45X–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	5		7		9		ns
t_{HD}	Data Hold	1		1		1		ns
t_{SEN}	Enable Set-Up	5		7		9		ns
t_{HEN}	Enable Hold	1		1		1		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		10		15		20	ns
t_{OLZ}[9, 16]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		ns
t_{OHZ}[9, 16]	$\overline{OE}$ HIGH to Output Data in High Z		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[17]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[18]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	10		15		20		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t_{AP}	Program Mode—Data Access Time		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		ns

Notes:

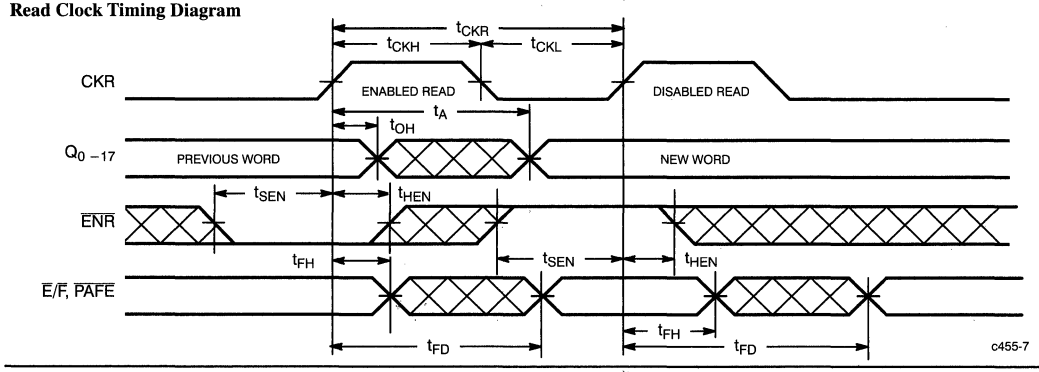
15. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 10 and 11, unless otherwise specified.
16. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
17. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, and CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, and CKR is the clock for Empty and Almost Empty flags.
18. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 17 for definition of clock and opposite clock.

Switching Waveforms

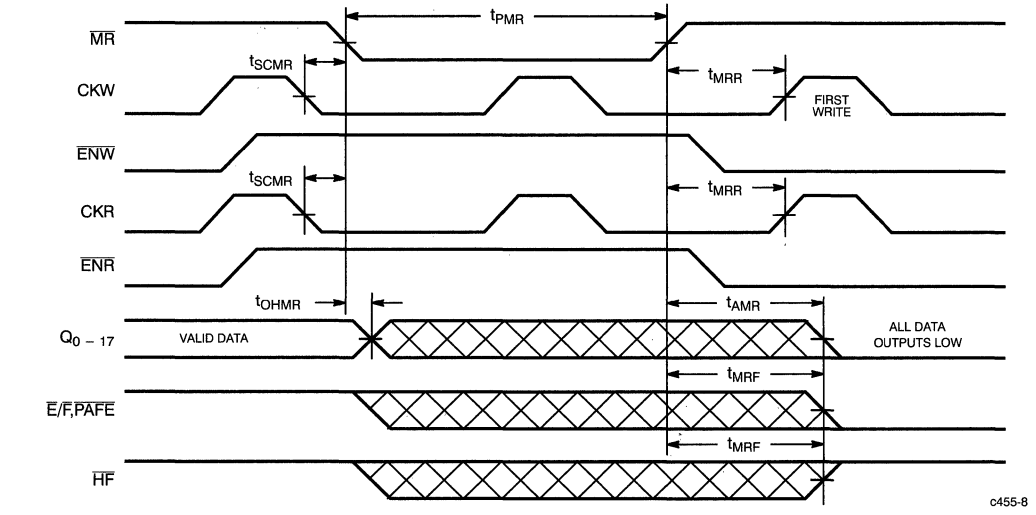
Write Clock Timing Diagram



Read Clock Timing Diagram

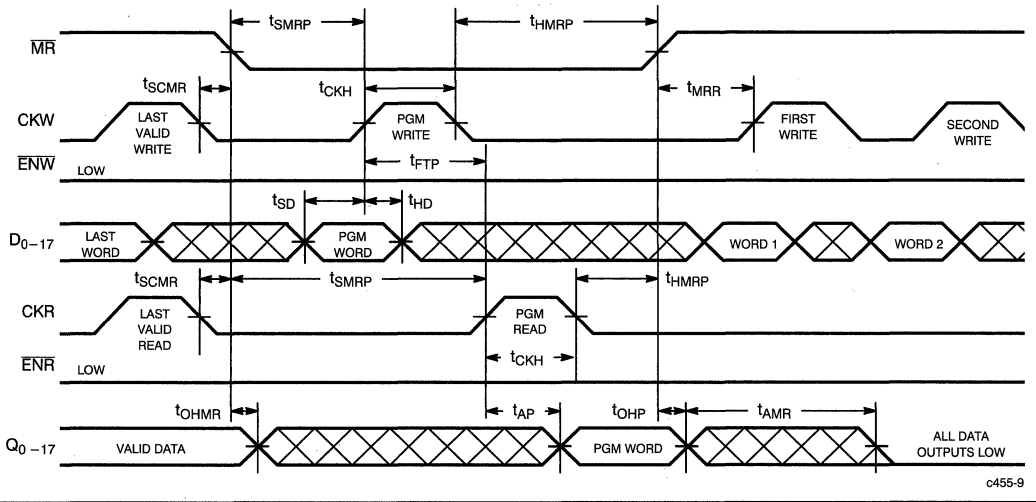


Master Reset (Default with Free-Running Clocks) Timing Diagram[19, 20, 21, 22]

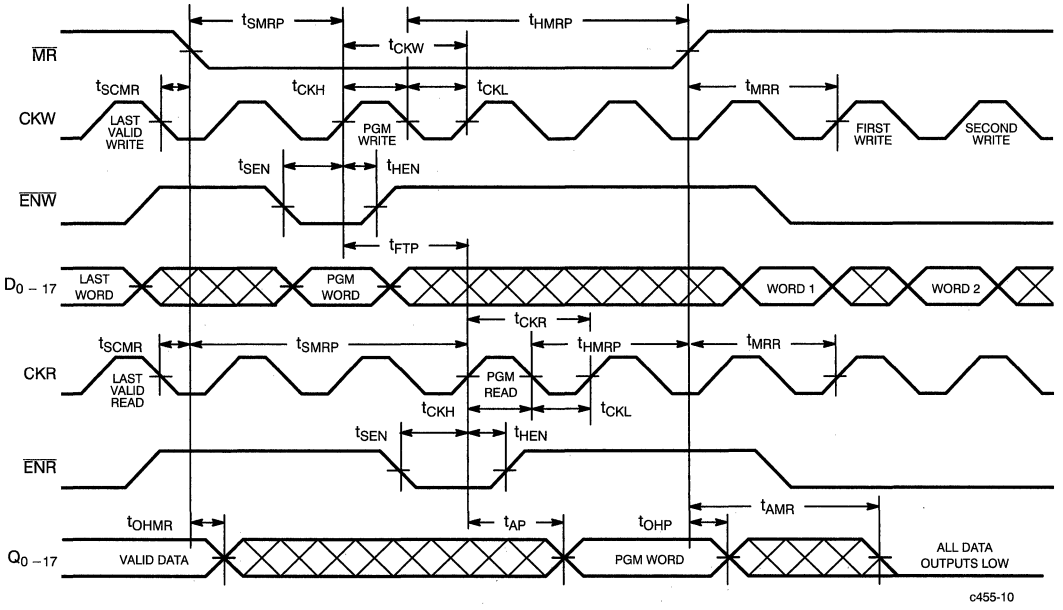


Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[21, 22]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[21, 22]

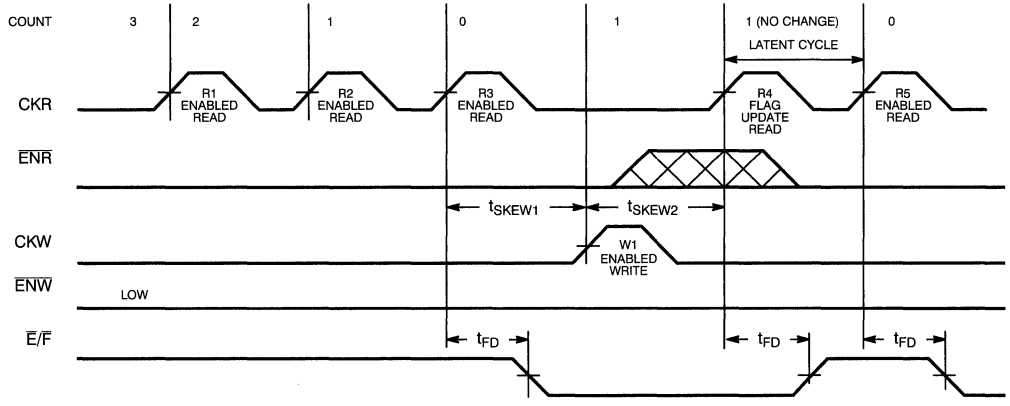


Notes:

19. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
20. To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
21. All data outputs (Q_{0-17}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
22. In this example, Q_{0-17} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

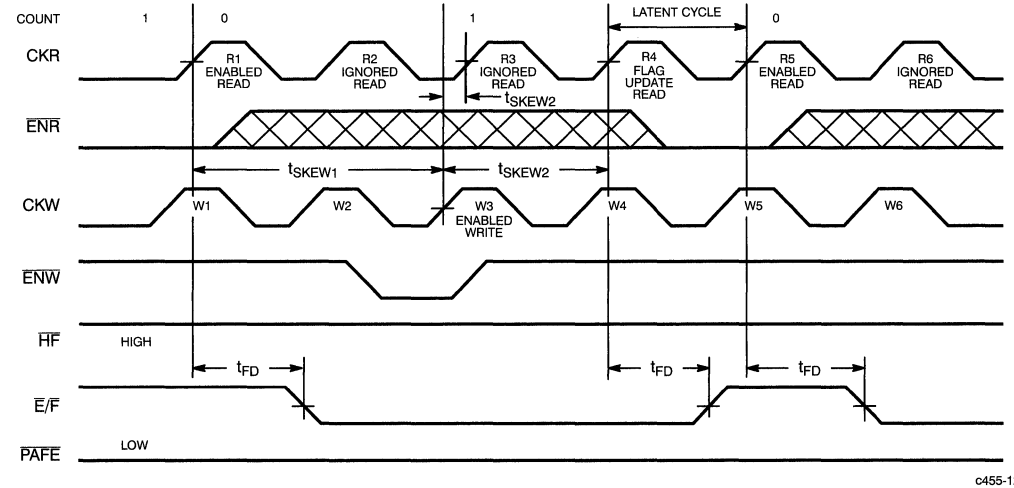
Switching Waveforms (continued)

Read to Empty Timing Diagram[23, 26, 27]



c455-11

Read to Empty Timing Diagram with Free-Running Clocks[23, 24, 25, 26]



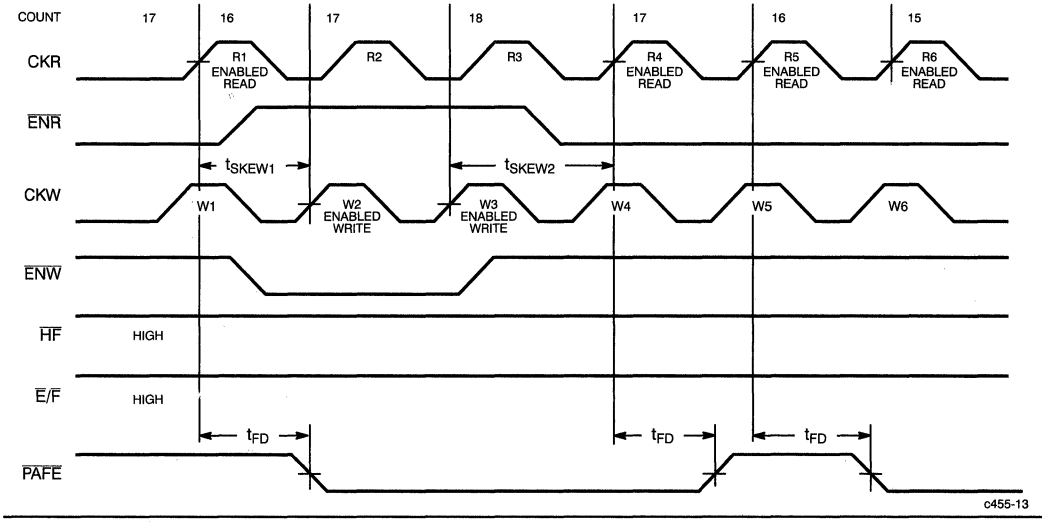
c455-12

Notes:

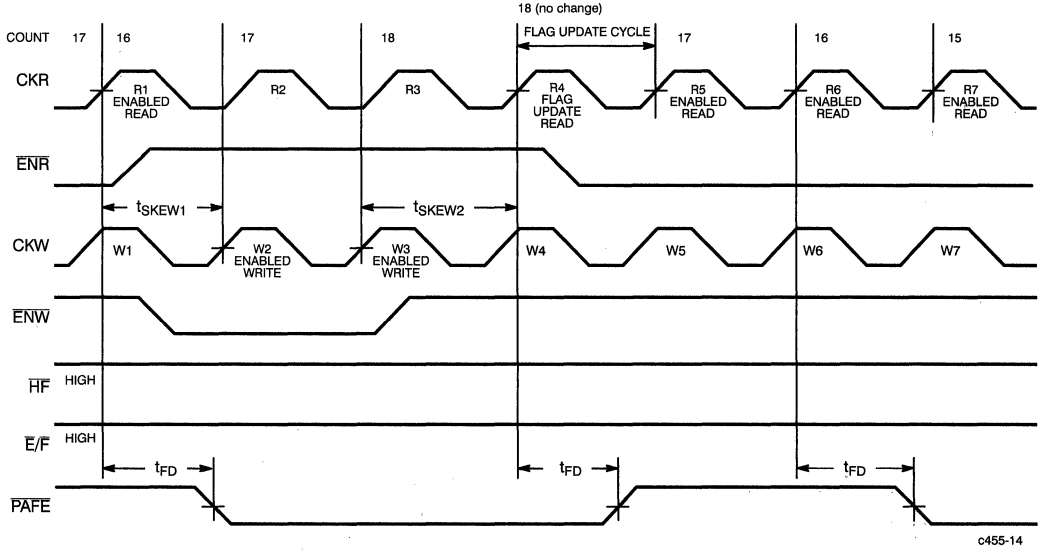
23. "Count" is the number of words in the FIFO.
24. The FIFO is assumed to be programmed with P>0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
25. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
26. CKR is clock and CKW is opposite clock.
27. R3 updates the flag to the Empty state by asserting $\overline{E/F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[23, 26, 28]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle with Free-Running Clocks[23, 26, 28, 29, 30]

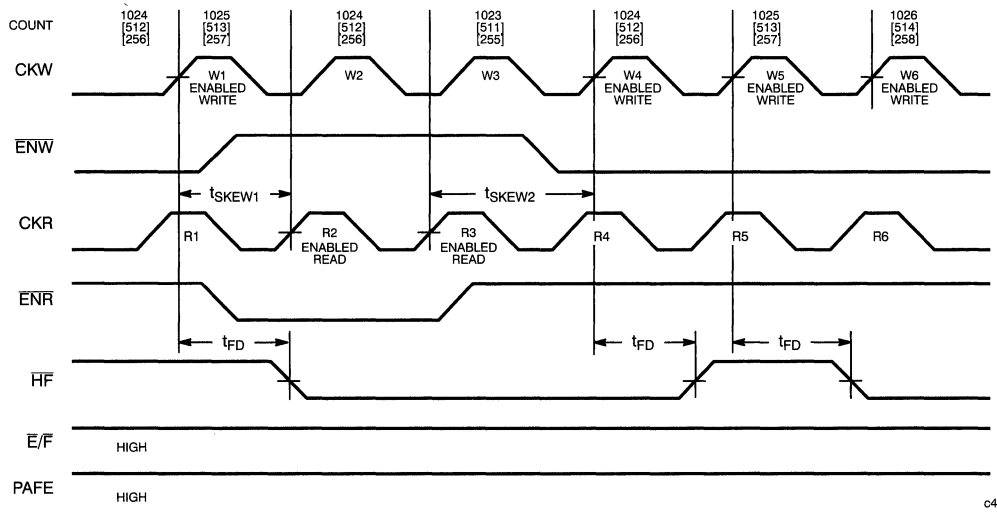


Notes:

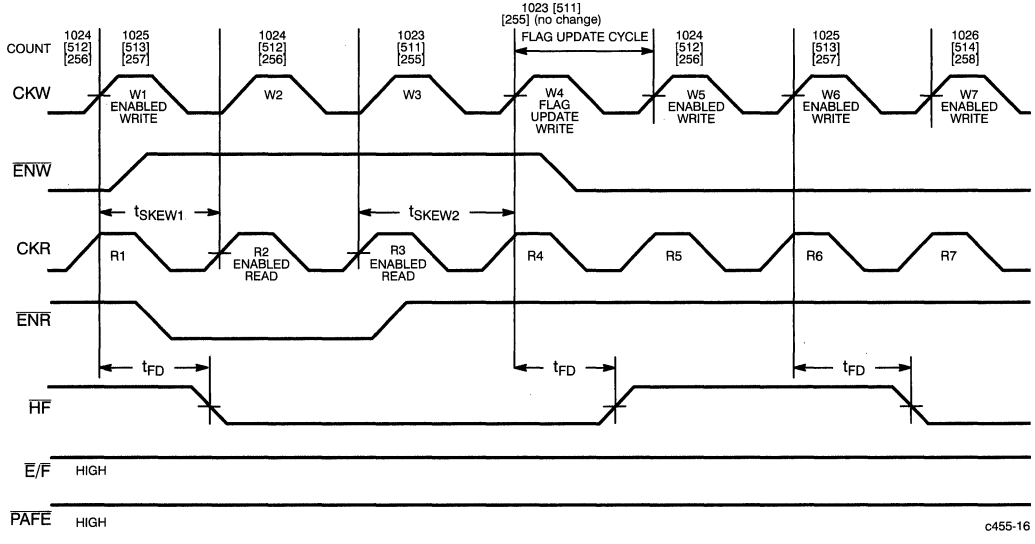
28. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
29. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
30. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[23, 31, 32, 33]



Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[23, 31, 32, 33, 34, 35]

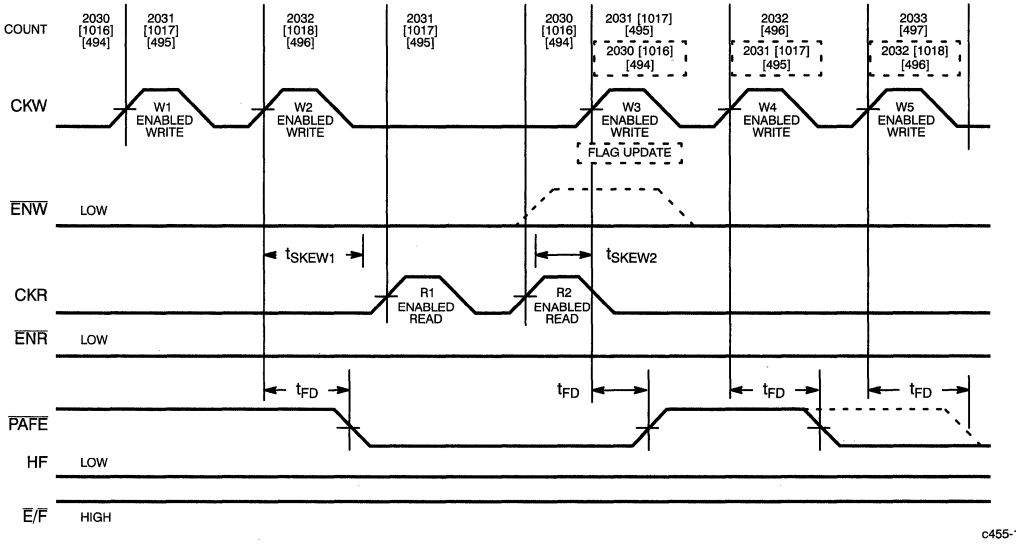


Notes:

31. CKW is clock and CKR is opposite clock.
32. Count = 1,025 indicates Half Full for the CY7C446 and CY7C456. Count = 513 indicates Half Full for the CY7C447 and CY7C457. Count = 257 indicates Half Full for the CY7C448 and CY7C458.
33. When the FIFO contains 1,024 [512] [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
34. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
35. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (i.e., 1,025 ♦1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

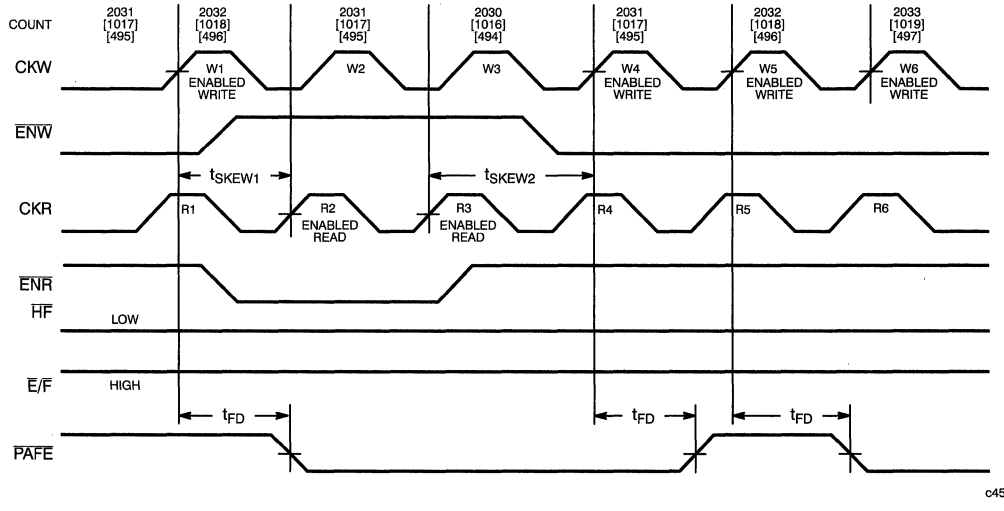
Switching Waveforms (continued)

Write to Almost Full Timing Diagram[23, 28, 31, 36, 37]



c455-17

Write to Almost Full Timing Diagram with Free-Running Clocks[23, 28, 31]



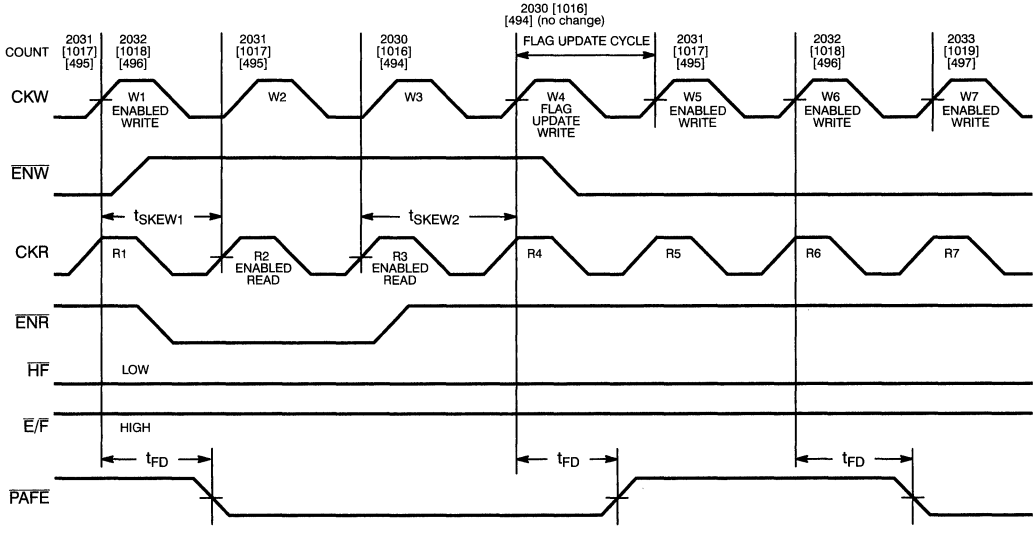
c455-18

Notes:

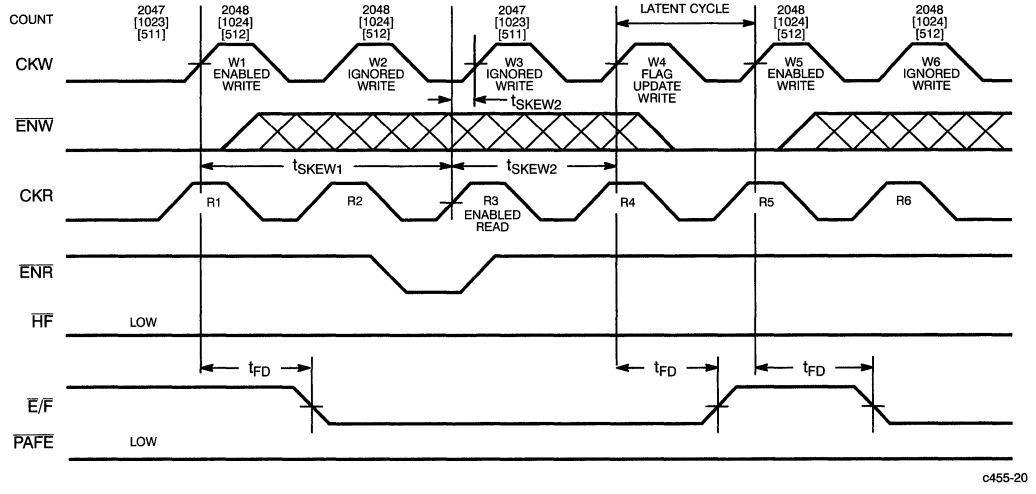
36. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
37. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is HIGH.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[23, 28, 31]



Write to Full Flag Timing Diagram with Free-Running Clocks[23, 31, 38]

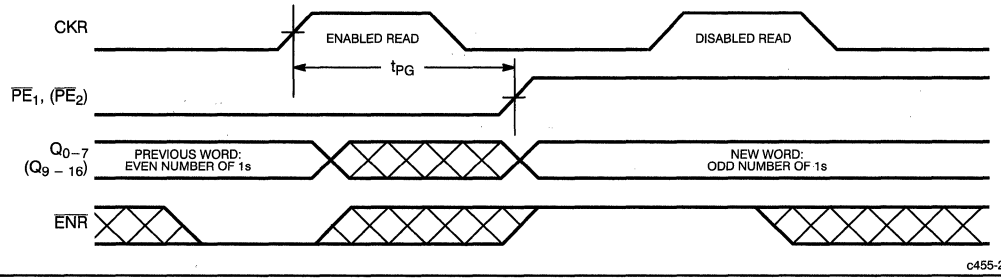


Note:

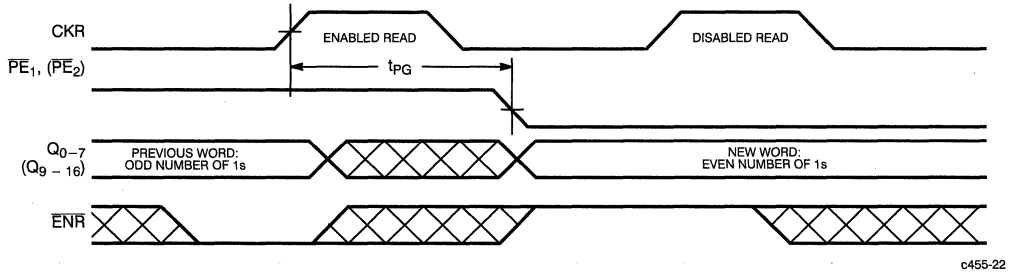
38. W2 is ignored because the FIFO is full (count = 2,048 [1,024] [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)

Even Parity Generation Timing Diagram[39, 40]



Even Parity Generation Timing Diagram[39, 41]

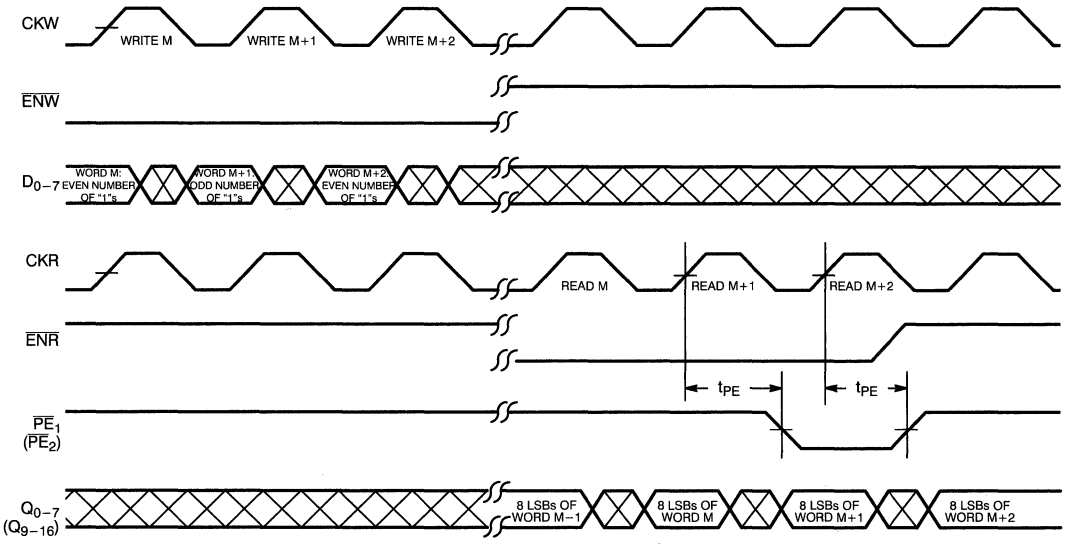


Notes:

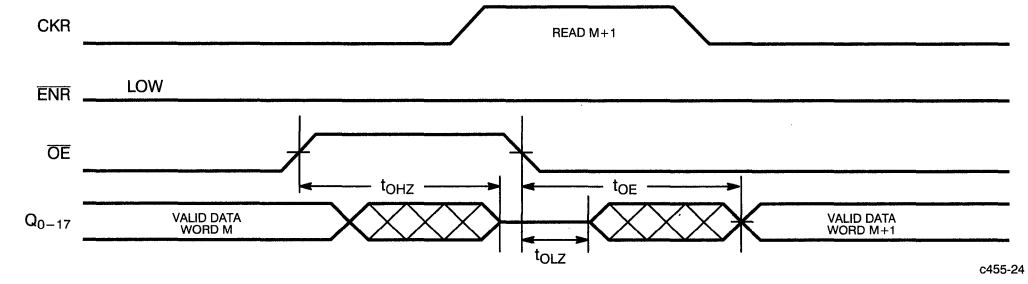
39. In this example, the FIFO is assumed to be programmed to generate even parity. The Q_{0-7} word is shown. The example is similar for the Q_{9-16} word.
40. If Q_{0-7} "new word" also has an even number of 1s, then PG1 stays LOW.
41. If Q_{0-7} "new word" also has odd number of 1s, then PG1 stays HIGH.

Switching Waveforms (continued)

Even Parity Checking[42]



Output Enable Timing[43, 44]



Notes:

42. In this example, the FIFO is assumed to be programmed to check for even parity. The Q_{0-7} word is shown.
43. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$. The Q_{0-7} word is shown.
44. If $\overline{ENR}$ was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

Architecture

The CY7C45X consists of an array of 512, 1,024, or 2,048 words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, and $\overline{MR}$), and flags ($\overline{HF}$, $\overline{E/F}$, $\overline{PAFE}$). The CY7C45X also includes the control signals $\overline{OE}$, $\overline{FL}$, $\overline{XI}$, and $\overline{XO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{E/F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-17}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the master reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (low), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C45X is programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write the $D_{0-9,10 \text{ or } 11}$ inputs into the programming register[45]. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on D_{0-9} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in *Table 1* refers to the decimal equivalent of the binary number represented by $D_{0-7,8 \text{ or } 9}$. Programming options for the CY7C45X are listed in *Table 4*.

The programmable $\overline{PAFE}$ function on the CY7C45X is only valid when not cascaded. If the user elects not to program the FIFO's flags, the default is as follows: the Almost Empty condition (Almost Full condition) is activated when the FIFO contains 16 or less words (empty locations).

Parity is programmed with the D_{15-17} bits. See *Table 4* for a summary of the various parity programming options. Data present on D_{15-17} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-7} and D_{9-16} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C45X provides three status pins when not cascaded. The three pins, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when the CY7C45X is cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate).[46] The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock

Table 1. Flag Truth Table[47]

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State	7C455 Words in FIFO	7C456 Words in FIFO	7C457 Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1 ⧫ P	1 ⧫ P	1 ⧫ P
1	1	1	Less than or Equal to Half Full	P + 1 ⧫ 256	P + 1 ⧫ 512	P + 1 ⧫ 1024
1	1	0	Greater than Half Full	257 ⧫ 511 − P	513 ⧫ 1023 − P	1025 ⧫ 2047 − P
1	0	0	Almost Full	512 − P ⧫ 511	1024 − P ⧫ 1023	2048 − P ⧫ 2047
0	0	0	Full	512	1024	2048

Notes:

45. CKW will write D_{0-9} into the programming register. CKR will read D_{0-9} during a programming register read.
46. The synchronous architecture guarantees the flags valid for approximately one cycle of the clock they are synchronized to.
47. P is the decimal value of the binary number represented by D_{0-7} for the CY7C455, D_{0-8} for the CY7C456, and D_{0-9} for the CY7C457. P = 0 signifies that the Almost Empty state = Empty state.

Flag Operation (continued)

(CKW). For example, if the CY7C457 contains 2,047 words (2,048 words indicate Full for the CY7C457), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the FIFO must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1} after or t_{SKEW2} before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read clock cycles are required to read data out of the FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is deasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C45X features programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at any distance from the Empty/Full boundary. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

The default distance from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Table 3* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

The CY7C45X also features even or odd parity checking and generation. D_{15-17} are used during a program write to describe the parity option desired. *Table 4* summarizes programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on two multi-mode output pins (Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$). The three possible modes are described in the following paragraphs.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Programmable Parity

Parity Disabled (Q_8/Q_{17} mode)

When parity is disabled (or the user does not program parity option) the FIFO stores all 18 bits present on D_{0-17} inputs internally and will output all 18 bits on Q_{0-17}.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7} and D_{9-16}. D_8 and D_{17} inputs are ignored. The parity bits are stored internally as D_8 and D_{17}, and during a subsequent read will be available on the PG1 and PG2 pins along with the data words from which the parity was generated (Q_{0-7} and Q_{9-16}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG1 will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the FIFO is programmed for parity checking, it will compare the parity of D_{0-8} and D_{9-17} with the program register. For example, D_8 and D_{17} will be set according to the result of the parity check on each word. When these words are later read, $\overline{PE_1}$ and $\overline{PE_2}$ will reflect the result of the parity check. If a parity error occurs in D_{0-8}, D_8 will be set LOW internally. When this word is later read, $\overline{PE1}$ will be LOW.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. These FIFOs can be expanded in width to provide word width greater than 18 in increments of 18. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C45X can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-17}, Q_{0-17}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-17} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-17} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-17} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C45X is cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-17} during a program read. Q_{0-17} of all other devices will remain in a high-impedance state to avoid bus contention.

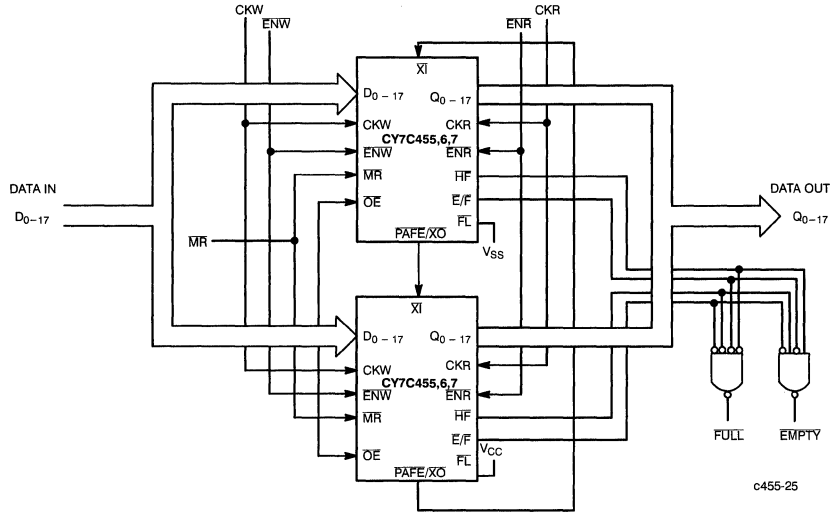


Figure 1. Depth Expansion with CY7C45X

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[48]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (transition from <HF to AE)

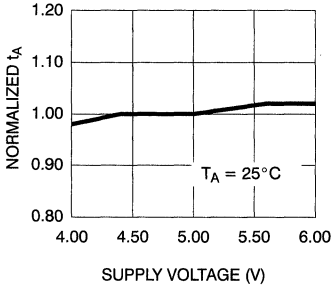
Table 4. Programmable Parity Options

D17	D16	D15	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

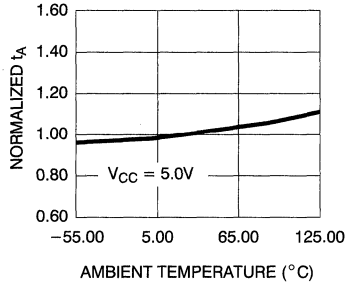
Note:
48. Applies to CY7C45X operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.

Typical AC and DC Characteristics

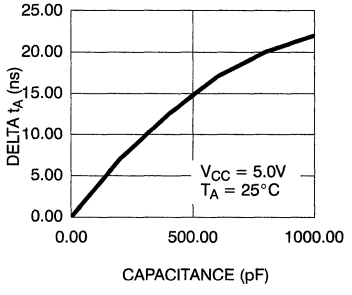
NORMALIZED t_A vs. SUPPLY VOLTAGE



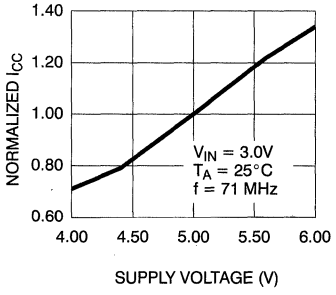
NORMALIZED t_A vs. AMBIENT TEMPERATURE



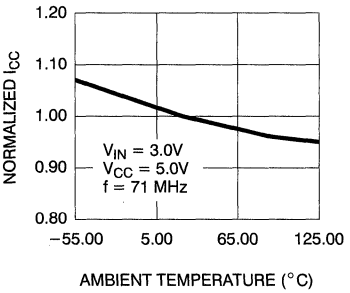
TYPICAL t_A CHANGE vs. OUTPUT LOADING



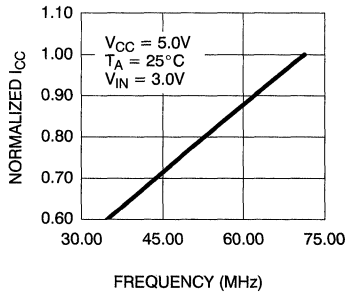
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



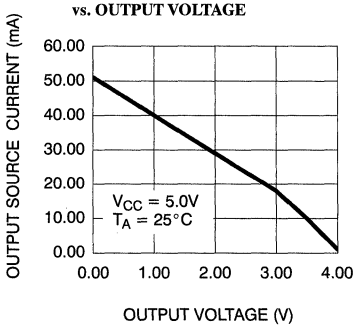
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



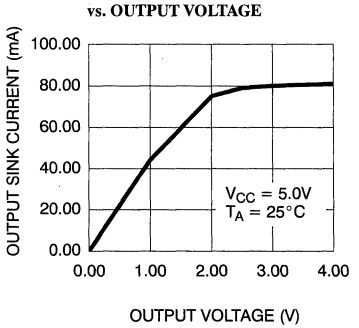
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C455–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C455–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C455–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C456–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C456–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C456–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C457–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C457–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C457–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Document #: 38–00211–C

CY7C460
CY7C462
CY7C464

Cascadable 8K x 9 FIFO
Cascadable 16K x 9 FIFO
Cascadable 32K x 9 FIFO

Features

- **8K x 9 FIFO (CY7C460)**
- **16K x 9 FIFO (CY7C462)**
- **32K x 9 FIFO (CY7C464)**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  — I_{CC} = 70 mA (max.)
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **5V ± 10% supply**
- **PLCC, LCC, and 600-mil DIP packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functionally equivalent to IDT7205, IDT7206**

Functional Description

The CY7C460, CY7C462, and CY7C464 are respectively, 8K, 16K, and 32K words by 9-bit wide first-in-first-out (FIFO) memories. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

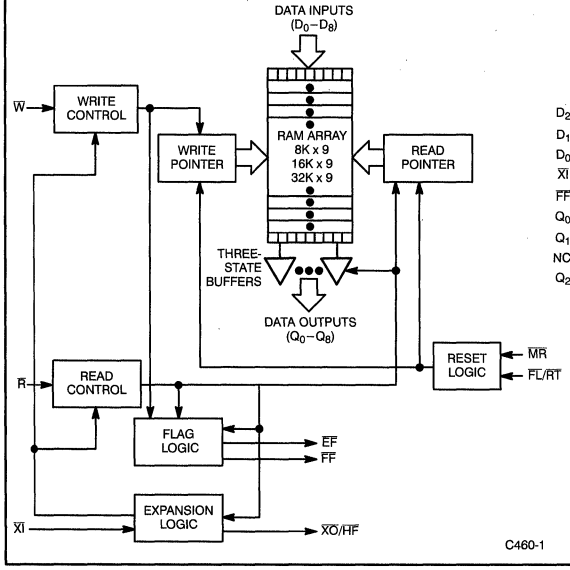
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone (single device) and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

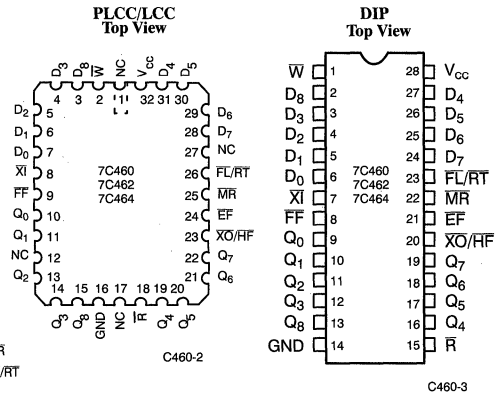
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

The CY7C460, CY7C462, and CY7C464 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

Logic Block Diagram



Pin Configurations



CYPRESS

Selection Guide

		7C460–15 7C462–15 7C464–15	7C460–20 7C462–20 7C464–20	7C460–25 7C462–25 7C464–25	7C460–40 7C462–40 7C464–40	7C460–65 7C462–65 7C464–65
Frequency (MHz)		33.3	33.3	28.5	20	12.5
Maximum Access Time (ns)		15	20	25	40	65
Maximum Operating Current (mA)	Commercial	105		90	70	70
	Military		110	95	75	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

5

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C460–15 7C462–15 7C464–15 Min.	7C460–15 7C462–15 7C464–15 Max.	7C460–20 7C462–20 7C464–20 Min.	7C460–20 7C462–20 7C464–20 Max.	7C460–25 7C462–25 7C464–25 Min.	7C460–25 7C462–25 7C464–25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2				2.2		V
			Mil/Ind			2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		105				90	mA
			Mil/Ind				110		95	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25				25	mA
			Mil/Ind				30		30	
I_{SB2}	Power-Down Current	All Inputs V_{CC} − 0.2V	Com'l		20				20	mA
			Mil/Ind				25		25	
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.

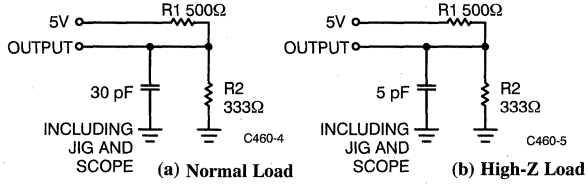
Electrical Characteristics Over the Operating Range (continued)[2]

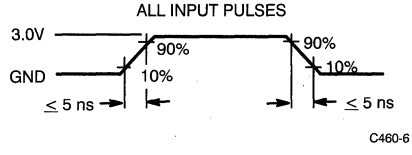
Parameter	Description	Test Conditions		7C460–40 7C462–40 7C464–40 Min.	7C460–40 7C462–40 7C464–40 Max.	7C460–65 7C462–65 7C464–65 Min.	7C460–65 7C462–65 7C464–65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2		2.2		V
			Mil/Ind	2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R} \ge V_{IH}$, $GND \le V_O \le V_{CC}$		−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70	mA
			Mil/Ind		75			
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil/Ind		30		30	
I_{SB2}	Power-Down Current	All Inputs V_{CC} − 0.2V	Com'l		20		20	mA
			Mil/Ind		25		25	
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA

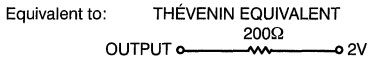
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms







Notes:
4. Tested initially and after any design or process changes that may affect these parameters.

CYPRESS

Switching Characteristics Over the Operating Range[2, 5]

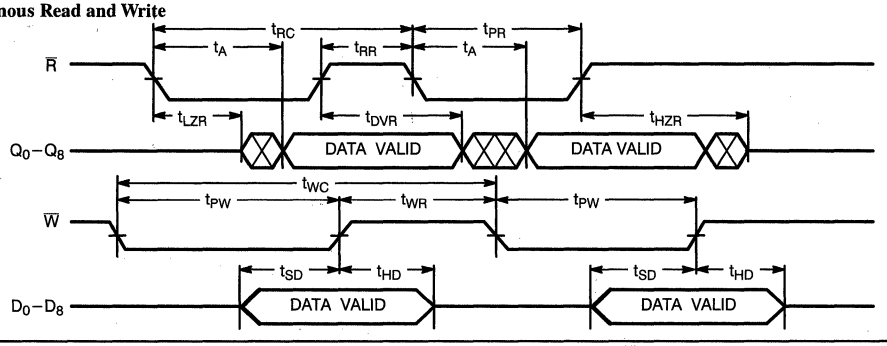
Parameter	Description	7C460–15 7C462–15 7C464–15		7C460–20 7C462–20 7C464–20		7C460–25 7C462–25 7C464–25		7C460–40 7C462–40 7C464–40		7C460–65 7C462–65 7C464–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	30		30		35		50		80		ns
t_A	Access Time		15		20		25		40		65	ns
t_{RR}	Read Recovery Time	15		10		10		10		15		ns
t_{PR}	Read Pulse Width	15		20		25		40		65		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		3		ns
t_{DVR}[6]	Data Valid After Read HIGH	3		3		3		3		3		ns
t_{HZR}[6]	Read HIGH to High Z		15		15		18		25		25	ns
t_{WC}	Write Cycle Time	30		30		35		50		80		ns
t_{PW}	Write Pulse Width	15		20		25		40		65		ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		5		5		ns
t_{WR}	Write Recovery Time	15		10		10		10		15		ns
t_{SD}	Data Set-Up Time	11		12		15		20		30		ns
t_{HD}	Data Hold Time	0		0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	30		30		35		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	15		20		25		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	15		10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	15		20		25		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	15		20		25		40		65		ns
t_{RTC}	Retransmit Cycle Time	30		30		35		50		80		ns
t_{PRT}	Retransmit Pulse Width	15		20		25		40		65		ns
t_{RTR}	Retransmit Recovery Time	15		10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		25		30		35		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		25		30		35		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		25		30		35		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		15		20		25		40		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		15		20		25		40		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		15		20		25		40		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		15		20		25		40		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		25		30		35		50		60	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		25		30		35		50		60	ns
t_{RAE}	Effective Read from Write HIGH		15		20		25		40		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	15		20		25		40		65		ns
t_{WAF}	Effective Write from Read HIGH		15		20		25		40		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	15		20		25		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		15		20		25		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		35		35		50		65	ns

Notes:

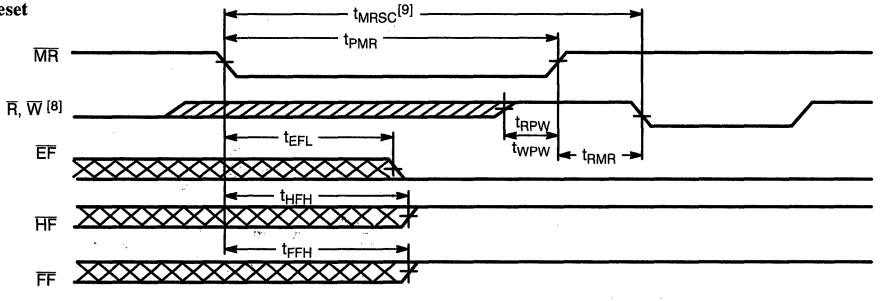
5. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load, unless otherwise specified.
6. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load.

Switching Waveforms[7]

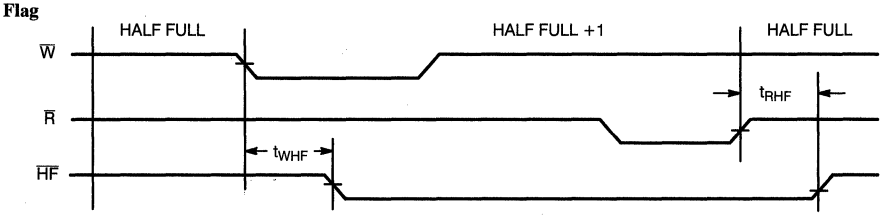
Asynchronous Read and Write



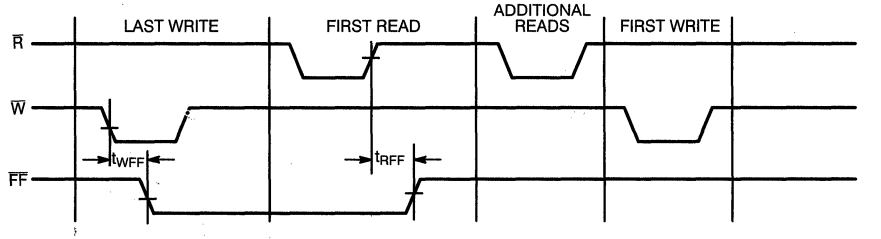
Master Reset



Half Full Flag



Last Write to First Read Full Flag

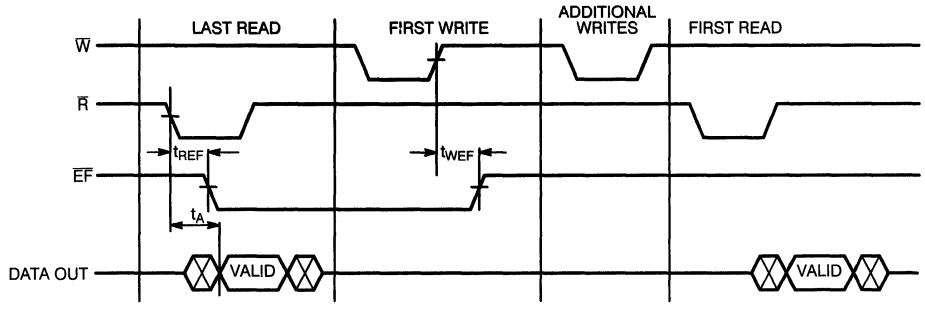


Notes:

7. A HIGH-to-LOW transition of either the write or read strobe causes a HIGH-to-LOW transition of the responding flag. Correspondingly, a LOW-to-HIGH strobe transition causes a LOW-to-HIGH flag transition.
8. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.
9. $t_{MRSC} = t_{PMR} + t_{RMR}$.

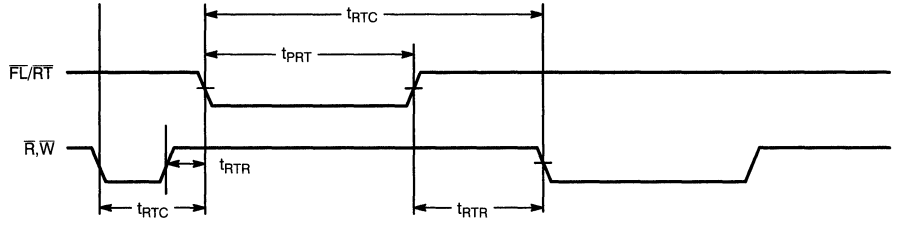
Switching Waveforms

Last READ to First WRITE Empty Flag



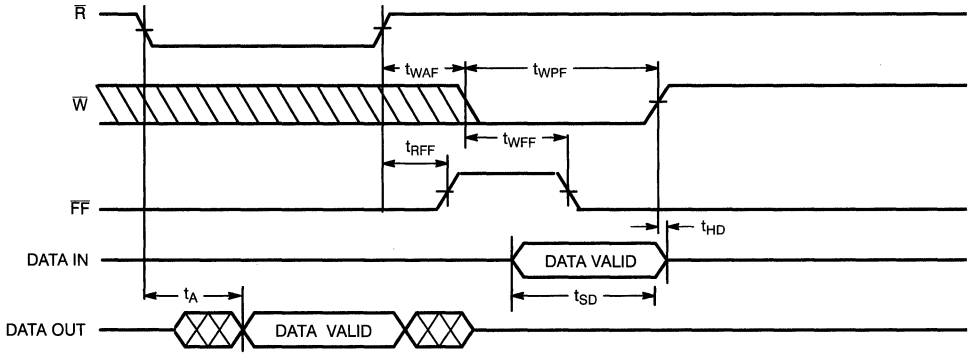
C460-11

Retransmit[10, 11]



C460-12

Full Flag and Write Data Flow-Through Mode



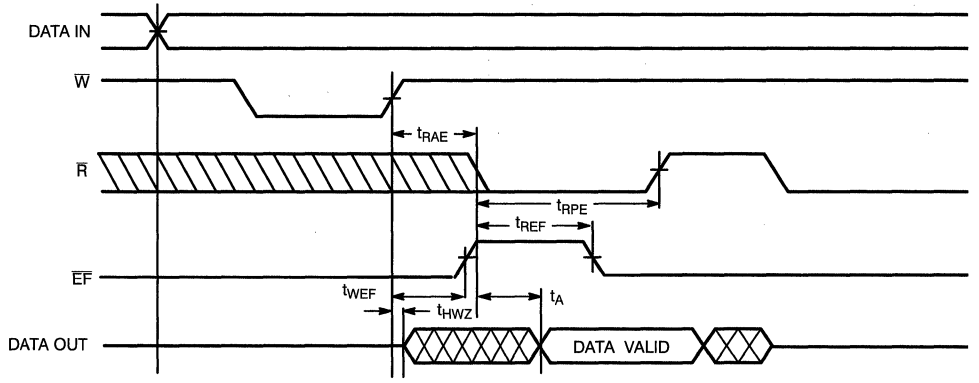
C460-13

Notes:

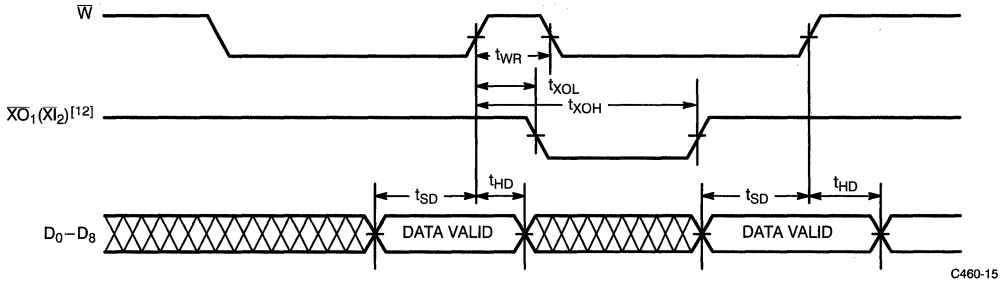
10. $t_{RTC} = t_{PRT} + t_{RTR}$.
11. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}, except for the CY7C46x–20 (Military), whose flags will be valid after t_{RTC} + 10 ns.

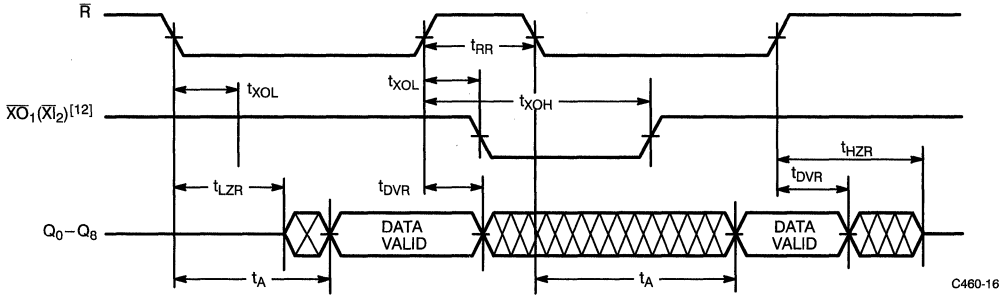
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



Expansion Timing Diagrams





Note:
12. Expansion out of device 1 ($\overline{XO}_1$) is connected to expansion in of device 2 ($\overline{XI}_2$).

Architecture

Resetting the FIFO

Upon power up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$), and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs ($D_0 - D_8$) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being half full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs ($Q_0 - Q_8$) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal-to-or-less-than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer incremented until equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding expansion in ($\overline{XI}$) and tying first load ($\overline{FL}$) to V_{CC} prior to a $\overline{MR}$ cycle. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (*see Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, expansion out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode, the first load ($\overline{FL}$) input, when grounded, indicates that this is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created with word widths in increments of nine. When expanding in depth, a composite $\overline{FF}$ is created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

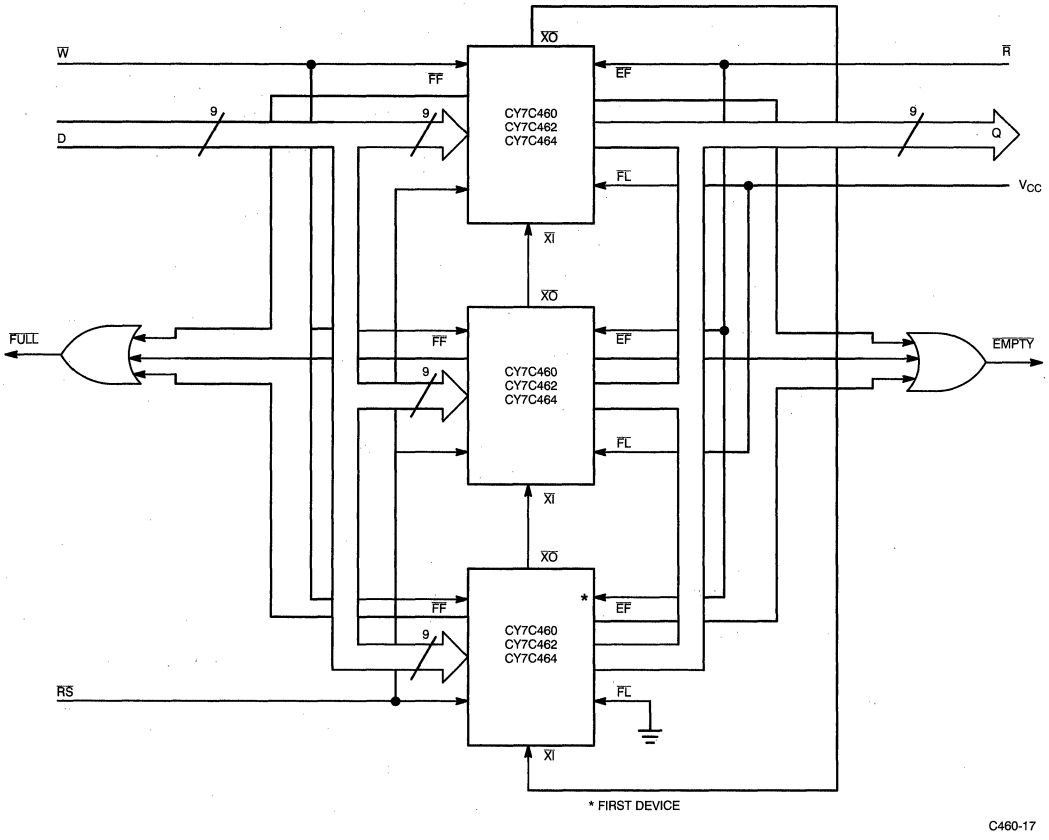
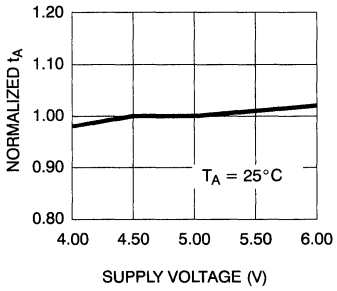


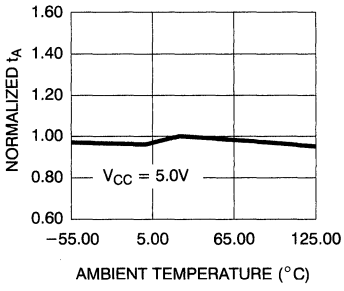
Figure 1. Depth Expansion

Typical AC and DC Characteristics

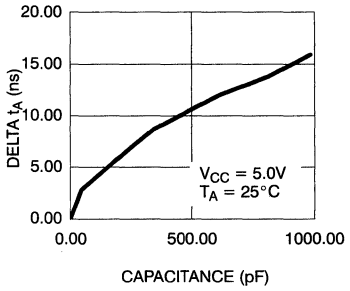
NORMALIZED t_A vs. SUPPLY VOLTAGE



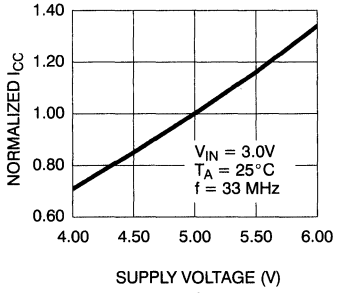
NORMALIZED t_A vs. AMBIENT TEMPERATURE



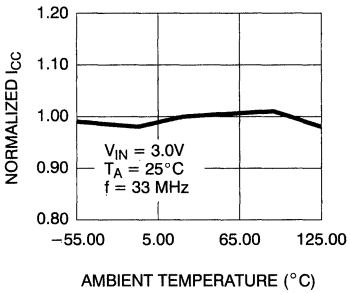
TYPICAL t_A CHANGE vs. OUTPUT LOADING



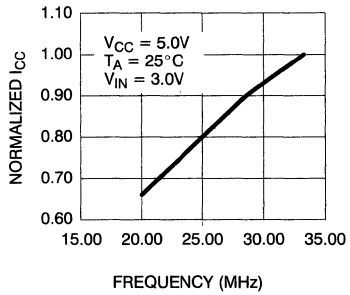
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



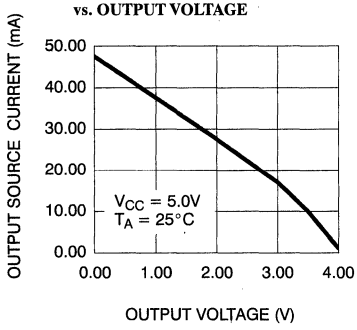
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



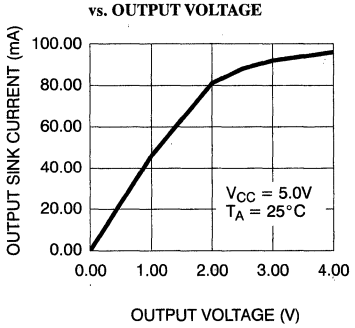
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C460–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C460–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C460–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C460–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C460–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C460–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C460–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C460–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C462–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C462–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C462–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C462–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C462–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C462–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C462–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C462–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

CYPRESS

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C464–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C464–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C464–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C464–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C464–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C464–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C464–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C464–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38-00141-G

CY7C470
CY7C472
CY7C474

8K x 9 FIFO, 16K x 9 FIFO, 32K x 9 FIFO with Programmable Flags

Features

- **8K x 9, 16K x 9, and 32K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  — I_{CC} (max.) = 70 mA
- **Programmable Almost Full/Empty flag**
- **Empty, Almost Empty, Half Full, Almost Full, and Full status flags**
- **Programmable retransmit**
- **Expandable in width**
- **5V ± 10% supply**
- **TTL compatible**
- **Three-state outputs**
- **Proprietary 0.8-micron CMOS technology**

Functional Description

The CYC47X FIFO series consists of high-speed, low-power, first-in first-out (FIFO) memories with programmable flags and retransmit mark. The CY7C470, CY7C472, and CY7C474 are 8K, 16K, and 32K words by 9 bits wide, respectively. They are offered in 600-mil DIP, PLCC, and LCC packages. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Three status pins—Empty/Full ($\overline{E/F}$), Programmable Almost Full/Empty ($\overline{PAFE}$), and Half Full ($\overline{HF}$)—are provided to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than Half Full, Greater than Half Full, Almost Full, and Full.

The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal goes LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go into a high-impedance state when $\overline{R}$ is HIGH.

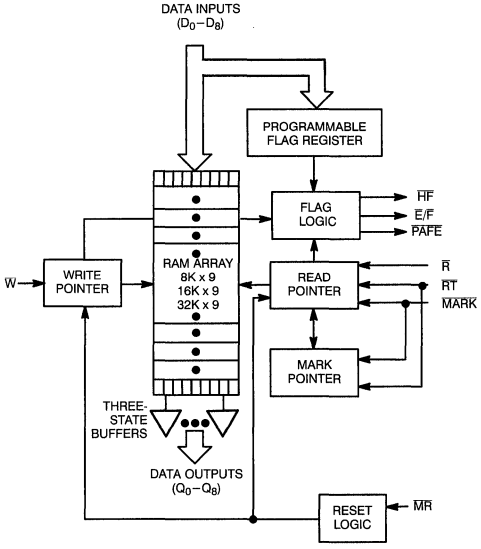
The user can store the value of the read pointer for retransmit by using the $\overline{MARK}$ pin. A LOW on the retransmit ($\overline{RT}$) input causes the FIFO to resend data by resetting the read pointer to the value stored in the mark pointer.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFO to resend the data. With the mark feature, retransmit can start from any word in the FIFO.

The CYC47X series is fabricated using a proprietary 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2001V and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

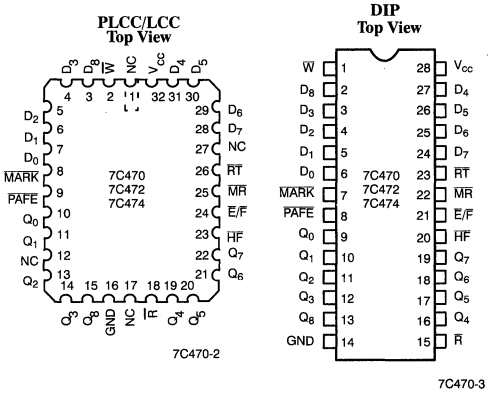
5

Logic Block Diagram



7C470-1

Pin Configurations



CYPRESS

Selection Guide

		7C470–15 7C472–15 7C474–15	7C470–20 7C472–20 7C474–20	7C470–25 7C472–25 7C474–25	7C470–40 7C472–40 7C474–40
Frequency (MHz)		33.3	33.3	28.5	20
Maximum Access Time (ns)		15	20	25	40
Maximum Operating Current (mA)	Commercial	105		90	70
	Military/Industrial		110	95	75

Maximum Ratings

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C470–15 7C472–15 7C474–15 Min.	Max.	7C470–20 7C472–20 7C474–20 Min.	Max.	7C470–25 7C472–25 7C474–25 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2				2.2		V
			Mil/Ind			2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		105				90	mA
			Mil/Ind				110		95	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25				25	mA
			Mil/Ind				30		30	
I_{SB2}	Power-Down Current	All Inputs = V_{CC} − 0.2V	Com'l		20				20	mA
			Mil/Ind				25		25	
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.

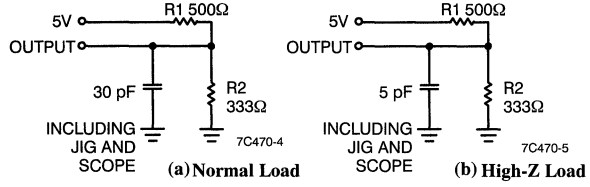
Electrical Characteristics Over the Operating Range[2] (continued)

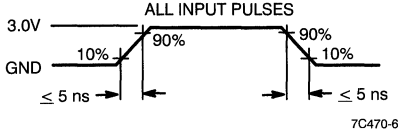
Parameter	Description	Test Conditions		7C470–40 7C472–40 7C474–40 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2		V
			Mil/Ind	2.2		
V_{IL}	Input LOW Voltage				0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70	mA
			Mil/Ind		75	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25	mA
			Mil/Ind		30	
I_{SB2}	Power-Down Current	All Inputs = V_{CC} − 0.2V	Com'l		20	mA
			Mil/Ind		25	
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−90	mA

Capacitance[4]

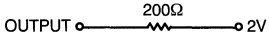
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Note:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5, 6]

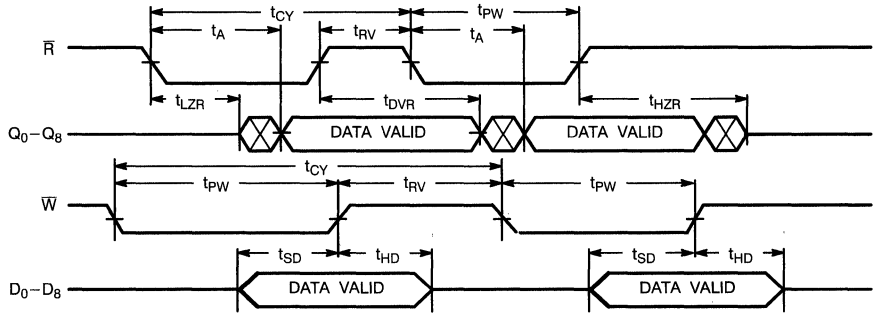
Parameter	Description	7C470–15 7C472–15 7C474–15		7C470–20 7C472–20 7C474–20		7C470–25 7C472–25 7C474–25		7C470–40 7C472–40 7C474–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	30		30		35		50		ns
t_A	Access Time		15		20		25		40	ns
t_{RV}	Recovery Time	15		10		10		10		ns
t_{PW}	Pulse Width	15		20		25		40		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		ns
t_{DV}[7]	Valid Data from Read HIGH	3		3		3		3		ns
t_{HZ}[7]	Read HIGH to High Z		15		15		18		25	ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		5		ns
t_{SD}	Data Set-Up Time	11		12		15		20		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{EFD}	$\overline{E}/\overline{F}$ Delay		15		20		25		40	ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		25		30		35		50	ns
t_{HFD}	$\overline{HF}$ Delay		25		30		35		50	ns
t_{AFED}	$\overline{PAFE}$ Delay		25		30		35		50	ns
t_{RAE}	Effective Read from Write HIGH	15		20		25		40		ns
t_{WAF}	Effective Write from Read HIGH	15		20		25		40		ns

Notes:

5. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
6. See the last page of this specification for Group A subgroup testing information.
7. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Loads. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.

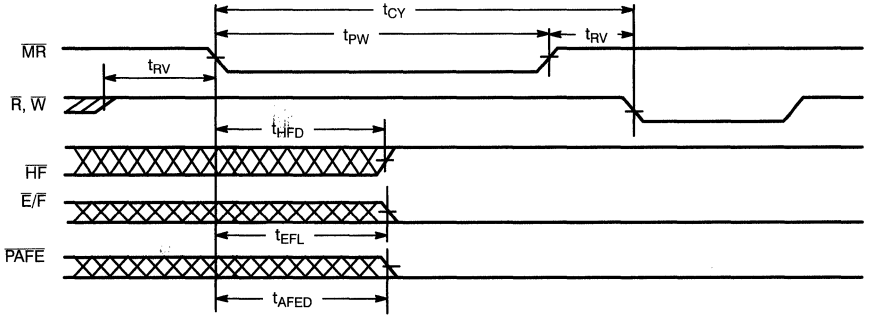
Switching Waveforms

Asynchronous Read and Write



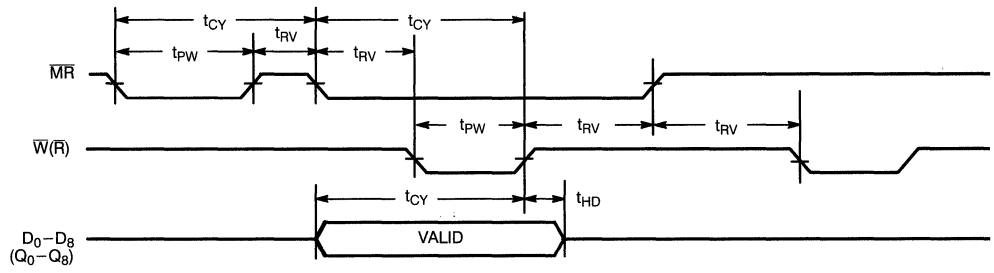
7C470-7

Master Reset (No Write to Programmable Flag Register)



7C470-8

Master Reset (Write to Programmable Flag Register)[8, 9]

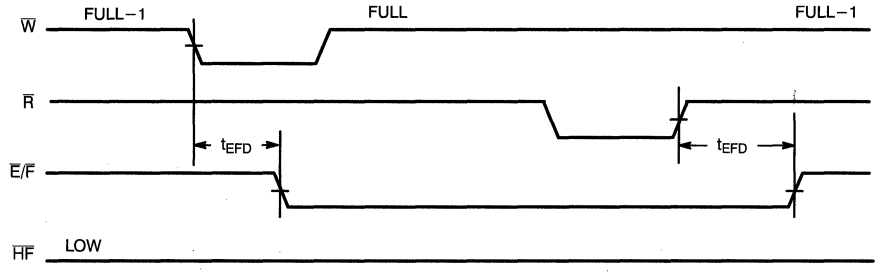


7C470-9

Note:
8. Waveform labels in parentheses pertain to writing the programmable flag register from the output port ($Q_0 - Q_8$).
9. Master Reset ($\overline{MR}$) must be pulsed LOW once prior to programming.

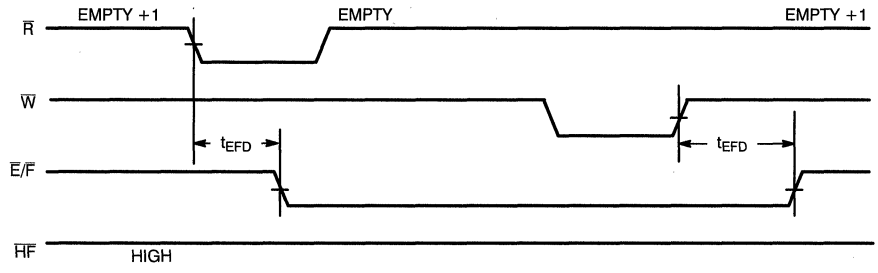
Switching Waveforms (continued)

$\overline{E}/\overline{F}$ Flag (Last Write to First Read Full Flag)



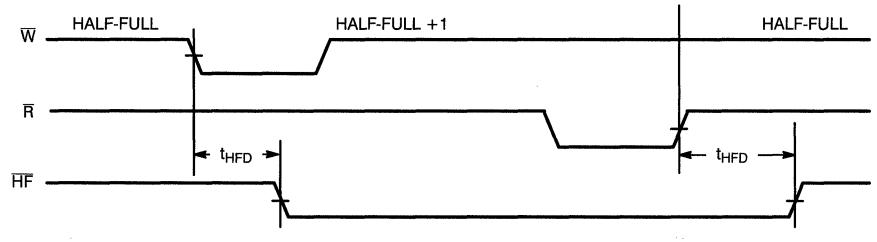
7C470-10

$\overline{E}/\overline{F}$ Flag (Last Read to First Write Empty Flag)



7C470-11

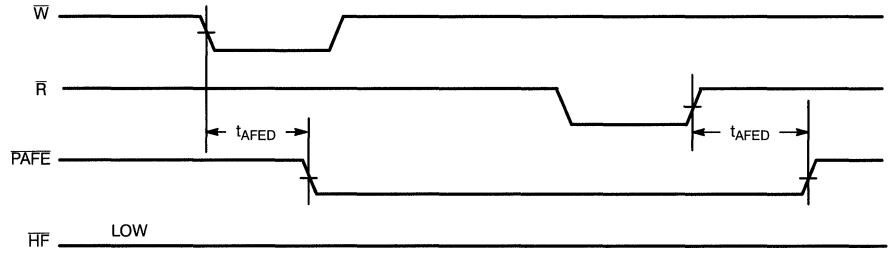
Half Full Flag



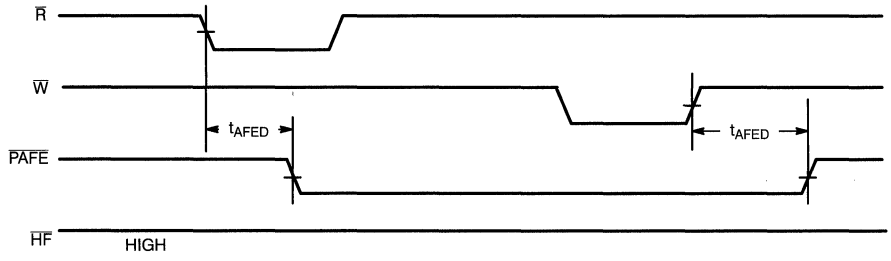
7C470-12

Switching Waveforms (continued)

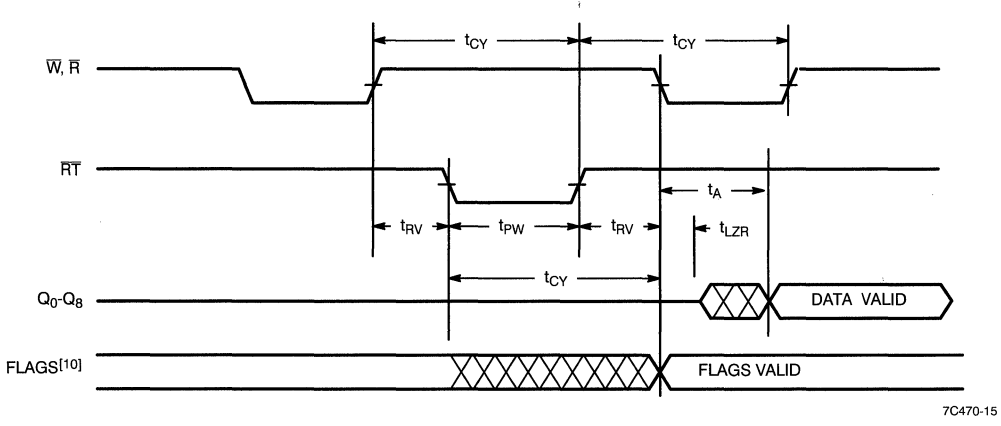
$\overline{PAFE}$ Flag (Almost Full)



$\overline{PAFE}$ Flag (Almost Empty)



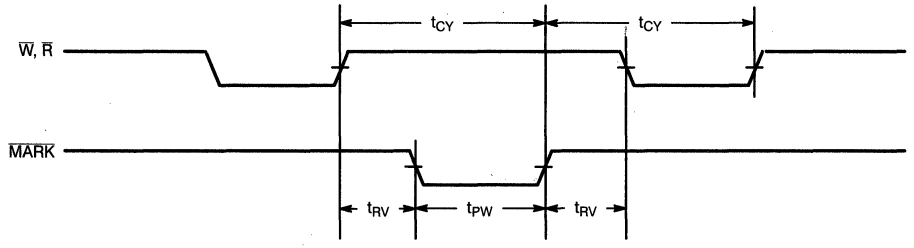
Retransmit[10]



Note:
10. The flags may change state during retransmit, but they will be valid a t_{CY} later, except for the CY7C47X–20 (Military), whose flags will be valid after t_{CY} + 10 ns.

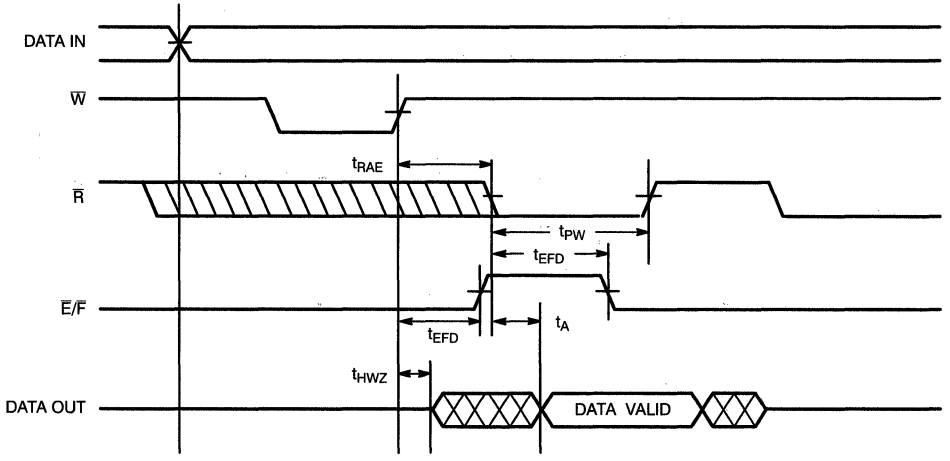
Switching Waveforms (continued)

Mark



7C470-16

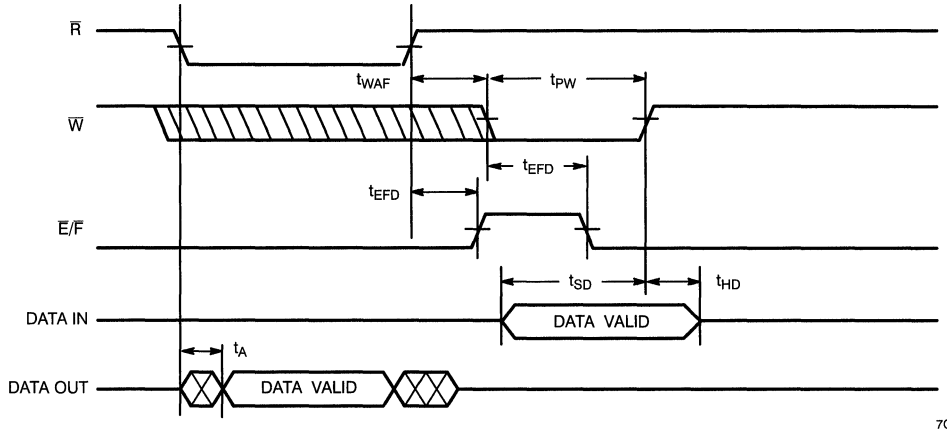
Empty Flag and Read Data Flow-Through Mode



7C470-17

Switching Waveforms (continued)

Full Flag and Write Data Flow-Through Mode



7C470-18

Architecture

The CY7C470, CY7C472, and CY7C474 FIFOs consist of an array of 8,192, 16,384, and 32,768 words of 9 bits each, respectively. The control consists of a read pointer, a write pointer, a retransmit pointer, control signals (i.e., write, read, mark, retransmit, and master reset), and flags (i.e., Empty/Full, Half Full, and Programmable Almost Full/Empty).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{E}/\overline{F}$) and Almost Full/Empty flag ($\overline{PAFE}$) being LOW, and Half Full flag ($\overline{HF}$) being HIGH. The read pointer, write pointer, and retransmit pointer are reset to zero. For a valid reset, Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before the falling edge and t_{RMR} after the rising edge of $\overline{MR}$.

Writing Data to the FIFO

Data can be written to the FIFO when it is not FULL[11]. A falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

Reading Data from the FIFO

Data can be read from the FIFO when it is not empty[12]. A falling edge of $\overline{R}$ initiates a read cycle. Data outputs (Q_0-Q_8) are in a high-impedance condition when the FIFO is empty and between read operations ($\overline{R}$ HIGH). The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a high-to-low transition of $\overline{E}/\overline{F}$, prohibiting any further read operations until t_{RFF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and resent if necessary. Retransmission can start from anywhere in the FIFO and be repeated without limitation.

The retransmit methodology is as follows: mark the current value of the read pointer, after an error in subsequent read operations return to that location and resume reading. This effectively resends all of the data from the mark point. When $\overline{MARK}$ is LOW, the current value of the read pointer is stored. This operation marks the beginning of the packet to be resent. When $\overline{RT}$ is LOW, the read pointer is updated with the mark location. During each subsequent read cycle, data is read and the read pointer incremented.

Care must be taken when using the retransmit feature. Use the mark function such that the write pointer does not pass the mark pointer, because further write operations will overwrite data.

Programmable Almost Full/Empty Flag

The CY7C470/2/4 offer a variable offset for the Almost Empty and the Almost Full condition. The offset is loaded into the programmable flag register (PFR) during a master reset cycle. While $\overline{MR}$ is LOW, the PFR can be loaded from Q_8-Q_0 by pulsing $\overline{R}$ LOW or from D_8-D_0 by pulsing $\overline{W}$ LOW. The offset options are listed in *Table 2*. See *Table 1* for a description of the six FIFO states. If the PFR is not loaded during master reset ($\overline{R}$ and $\overline{W}$ HIGH) the default offset will be 256 words from Full and Empty.

Notes:

11. When the FIFO is less than half full, the flags make a LOW-to-HIGH transition on the rising edge of $\overline{W}$ and make the HIGH-to-LOW transition on the falling edge of $\overline{R}$. If the FIFO is more than half full, the flags make the LOW-to-HIGH transition on the rising edge of $\overline{R}$ and HIGH-to-LOW transition on the falling edge of $\overline{W}$.
12. Full and empty states can be decoded from the Half-Full ($\overline{HF}$) and Empty/Full ($\overline{E}/\overline{F}$) flags.

Table 1. Flag Truth Table[13]

$\overline{HF}$	$\overline{E/F}$	$\overline{PAFE}$	State	CY77C470 (8K x 9) Number of Words in FIFO	CY77C472 (16K x 9) Number of Words in FIFO	CY77C474 (32K x 9) Number of Words in FIFO
1	0	0	Empty	0	0	0
1	1	0	Almost Empty	1 ➧ (P − 1)	1 ➧ (P − 1)	1 ➧ (P − 1)
1	1	1	Less than Half Full	P ➧ 4096	P ➧ 8192	P ➧ 16384
0	1	1	Greater than Half Full	4097 ➧ (8192 − P)	8193 ➧ (16384 − P)	16385 ➧ (32768 − P)
0	1	0	Almost Full	(8192 − P+1) ➧ 8191	(16384 − P+1) ➧ 16383	(32768 − P+1) ➧ 32767
0	0	0	Full	8192	16384	32768

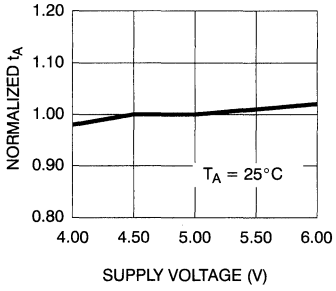
Table 2. Programmable Almost Full/Empty Options[14]

D3	D2	D1	D0	PAFE Active when:	P
0	0	0	0	256 or less locations from Empty/Full (default)	256
0	0	0	1	16 or less locations from Empty/Full	16
0	0	1	0	32 or less locations from Empty/Full	32
0	0	1	1	64 or less locations from Empty/Full	64
0	1	0	0	128 or less locations from Empty/Full	128
0	1	0	1	256 or less locations from Empty/Full (default)	256
0	1	1	0	512 or less locations from Empty/Full	512
0	1	1	1	1024 or less locations from Empty/Full	1024
1	0	0	0	2048 or less locations from Empty/Full	2048
1	0	0	1	4098 or less locations from Empty/Full[15]	4098
1	0	1	0	8192 or less locations from Empty/Full[16]	8192

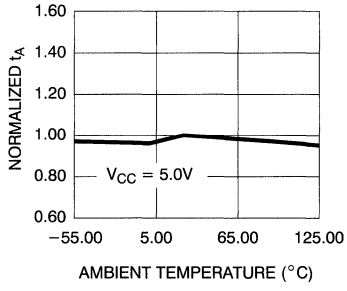
Notes:
13. See *Table 2* for P values.
14. Almost flags default to 256 locations from Empty/Full.
15. Only for CY7C472 and CY7C474.
16. Only for CY7C470.

Typical AC and DC Characteristics

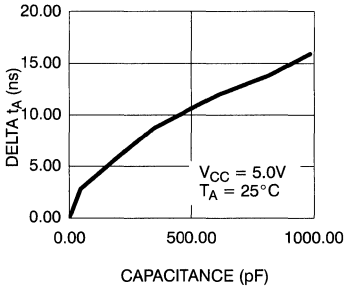
NORMALIZED t_A vs. SUPPLY VOLTAGE



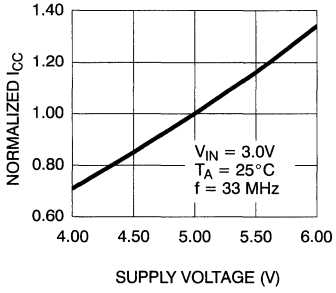
NORMALIZED t_A vs. AMBIENT TEMPERATURE



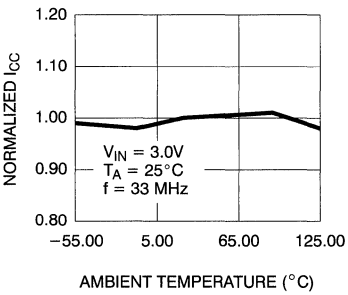
TYPICAL t_A CHANGE vs. OUTPUT LOADING



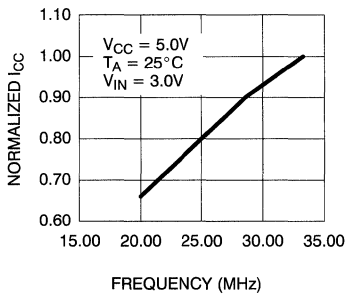
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



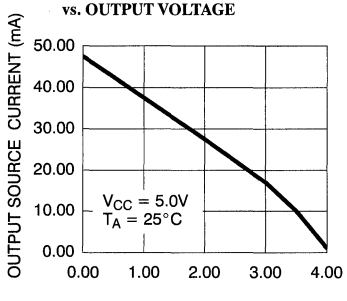
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



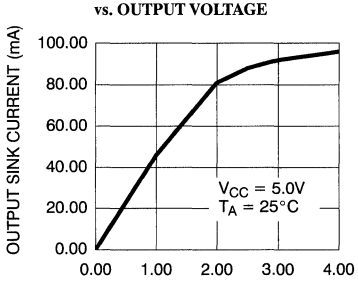
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



CYPRESS

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C470–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C470–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C470–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C470–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C470–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C470–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C470–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C472–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C472–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C472–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C472–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C472–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C472–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C472–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

CYPRESS

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C474–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C474–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C474–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C474–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C474–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C474–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C474–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C474–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C474–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

5

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CY}	9, 10, 11
t_{A}	9, 10, 11
t_{RV}	9, 10, 11
t_{PW}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{EFD}	9, 10, 11
t_{HFD}	9, 10, 11
t_{AFED}	9, 10, 11
t_{RAE}	9, 10, 11
t_{WAF}	9, 10, 11

Document #: 38–00142–H

Section Contents

Dual-Port Memories

CY7C006
CY7C016

16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **CMOS for optimum speed/power**
- **High-speed access**
  — 15 ns (commercial)
- **Low operating power: 140 mA (typ.)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin PLCC; 80-pin (7C016) and 64-pin (7C006) TQFP**
- **TTL compatible**
- **Capable of withstanding greater than 2001V ESD**
- **Pin compatible and functional equivalent to IDT7006 and IDT7016**

Functional Description

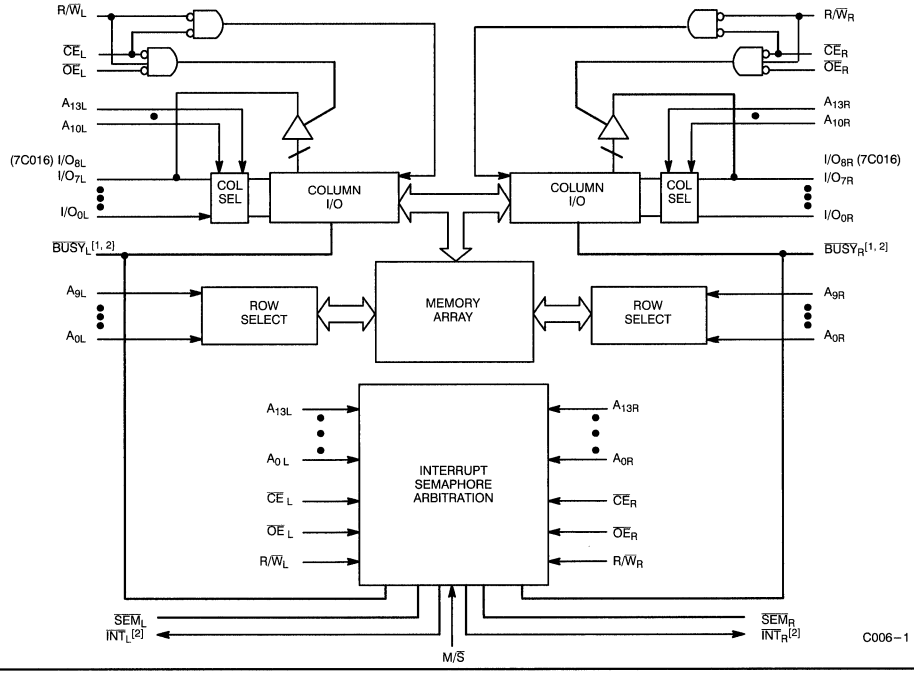
The CY7C006 and CY7C016 are high-speed CMOS 16K x 8 and 16K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7C006/016 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C006/016 can be utilized as a standalone 128-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16-/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16-/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7C006 and CY7C016 are available in 68-pin PLCCs, and 80-pin (7C016) TQFP and 64-pin (7C006) TQFP.

6

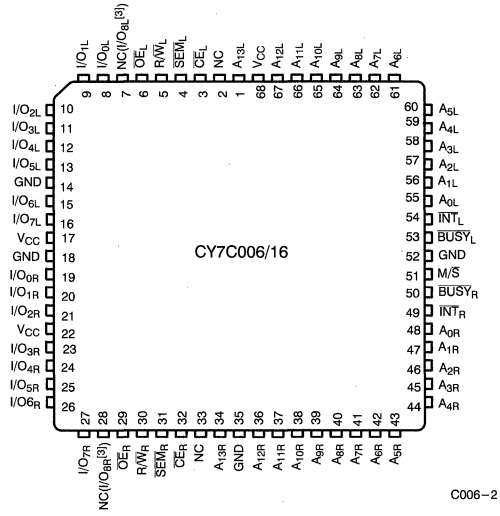
Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

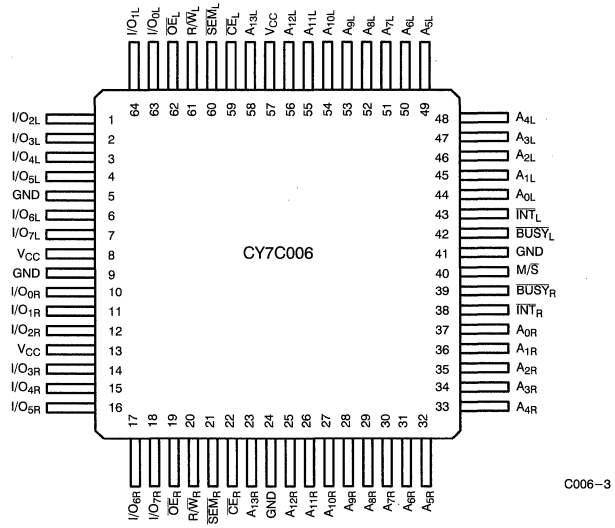
Pin Configurations

68-Pin LCC/PLCC
Top View



C006–2

64-Pin TQFP
Top View

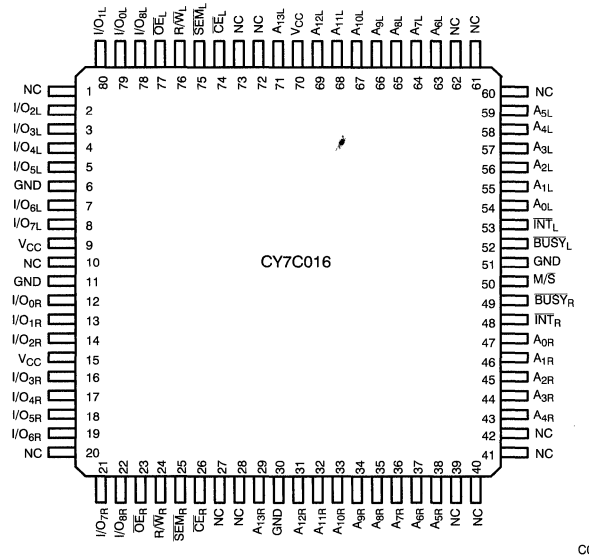


C006–3

Note:
3. I/O for 7C016 only.

Pin Configurations (continued)

80-Pin TQFP
Top View



C006–4

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-13L}	A_{0R-13R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 3FFE and is cleared when left port reads location 3FFE. $\overline{INT}_R$ is set when left port writes location 3FFF and is cleared when right port reads location 3FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

	7C006–15 7C016–15	7C006–25 7C016–25	7C006–35 7C016–35	7C006–55 7C016–55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	260	220	210	200
Maximum Standby Current for I_{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[4] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Note:
4. Pulse width < 20 ns.

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C006–15 7C016–15 Min.	Typ.	Max.	7C006–25 7C016–25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10		+10	−10		+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10		+10	−10		+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		170	260		160	220	mA
			Ind					160	270	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		50	70		40	60	mA
			Ind					40	75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		110	170		90	130	mA
			Ind					90	150	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[6]	Com'l		3	15		3	15	mA
			Ind					3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[6]	Com'l		100	150		80	120	mA
			Ind					80	130	

Parameter	Description	Test Conditions		7C006–35 7C016–35 Min.	Typ.	Max.	7C006–55 7C016–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10		+10	−10		+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10		+10	−10		+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		150	210		140	200	mA
			Ind		150	250		140	240	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		30	50		20	40	mA
			Ind		30	65		20	55	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		80	120		70	100	mA
			Ind		80	130		70	115	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[6]	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[6]	Com'l		70	100		60	90	mA
			Ind		70	110		60	95	

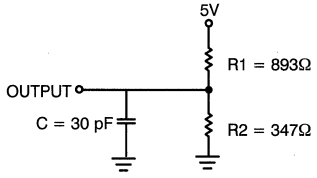
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance[7]

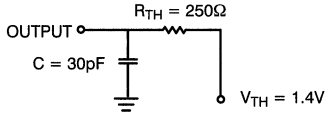
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



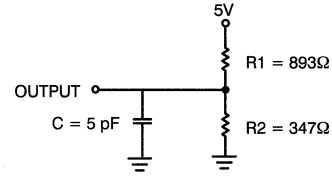
(a) Normal Load (Load 1)

C006–5



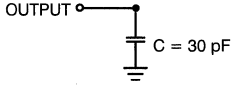
(b) Thévenin Equivalent (Load 1)

C006–6



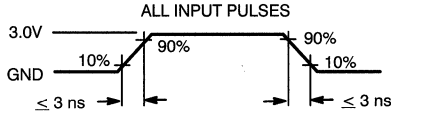
(c) Three-State Delay (Load 3)

C006–7



Load (Load 2)

C006–8



C006–9

Switching Characteristics Over the Operating Range[5, 8]

Parameter	Description	7C006–15 7C016–15 Min.	7C006–15 7C016–15 Max.	7C006–25 7C016–25 Min.	7C006–25 7C016–25 Max.	7C006–35 7C016–35 Min.	7C006–35 7C016–35 Max.	7C006–55 7C016–55 Min.	7C006–55 7C016–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		20		25	ns
t_{LZOE}[9,10]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[9,10]	$\overline{OE}$ HIGH to High Z		10		15		15		25	ns
t_{LZCE}[9,10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[9,10]	$\overline{CE}$ HIGH to High Z		10		15		15		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns

Notes:

7. Tested initially and after any design or process changes that may affect these parameters.
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.

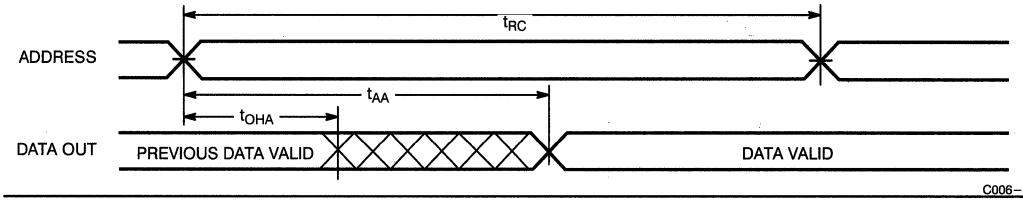
Switching Characteristics Over the Operating Range[5, 8] (continued)

Parameter	Description	7C006–15 7C016–15 Min.	7C006–15 7C016–15 Max.	7C006–25 7C016–25 Min.	7C006–25 7C016–25 Max.	7C006–35 7C016–35 Min.	7C006–35 7C016–35 Max.	7C006–55 7C016–55 Min.	7C006–55 7C016–55 Max.	Unit
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}[11]	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[12]	Write Pulse to Data Delay		30		50		60		80	ns
t_{DDD}[12]	Write Data Valid to Read Data Valid		25		30		35		60	ns
BUSY TIMING[13]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		17		25		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		17		25		30		ns
t_{BDD}[14]	$\overline{BUSY}$ HIGH to Data Valid		Note 14		Note 14		Note 14		Note 14	ns
INTERRUPT TIMING[13]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

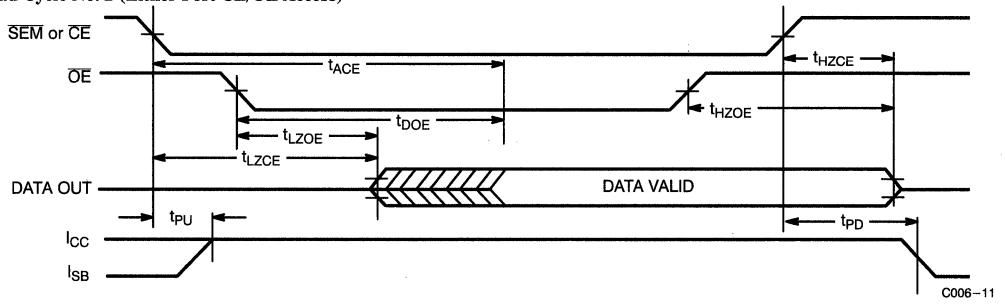
Notes:
11. Must be met by the device writing to the RAM under all operating conditions.
12. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
13. Test conditions used are Load 2.
14. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Switching Waveforms

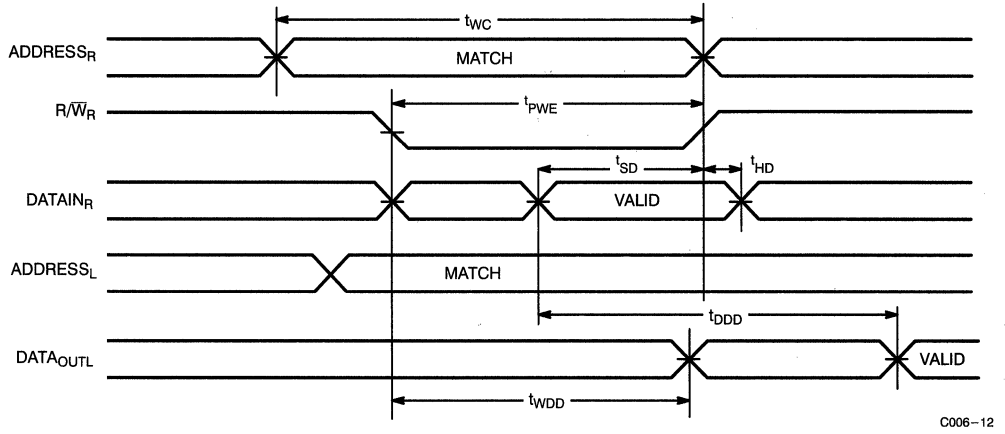
Read Cycle No. 1 (Either Port Address Access)[15, 16]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[15, 17, 18]



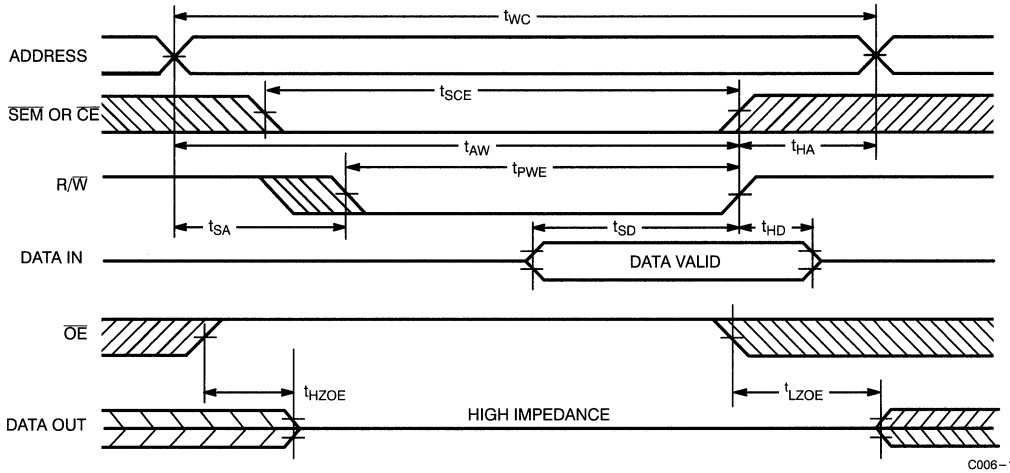
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[19, 20]



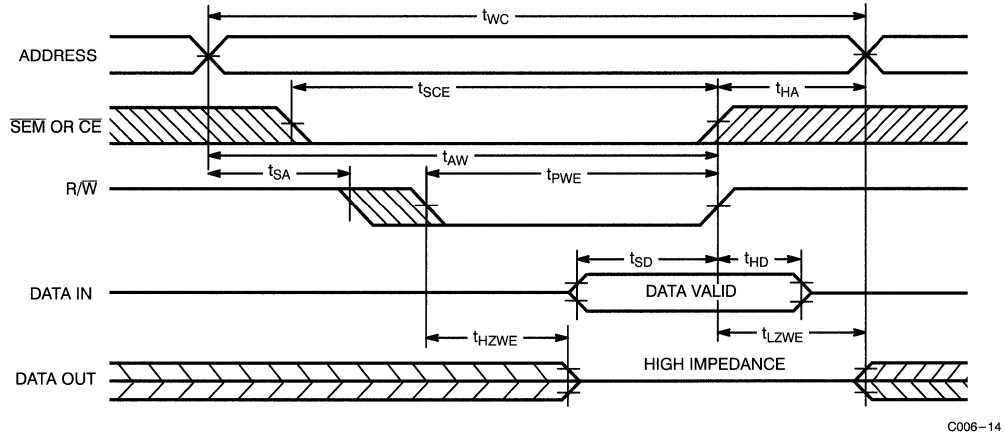
Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[21, 22, 23]



Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[21, 23, 24]

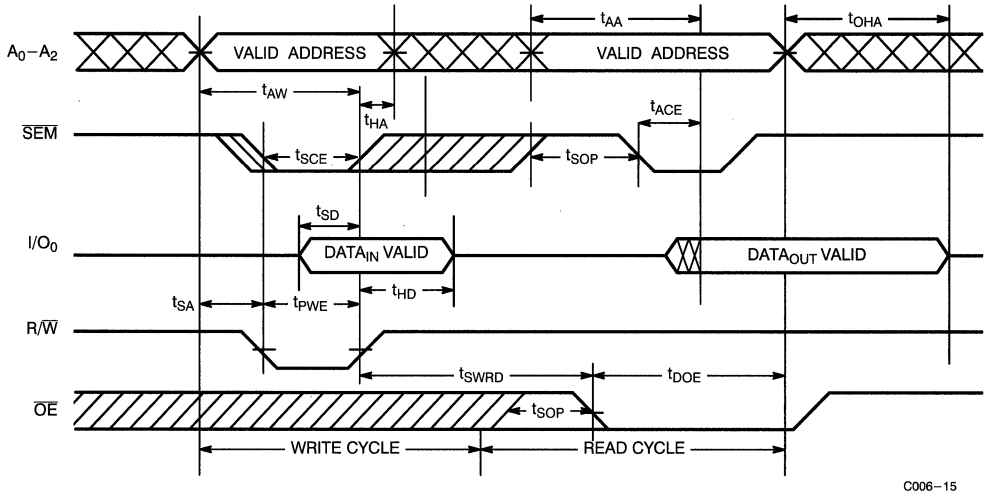


Notes:

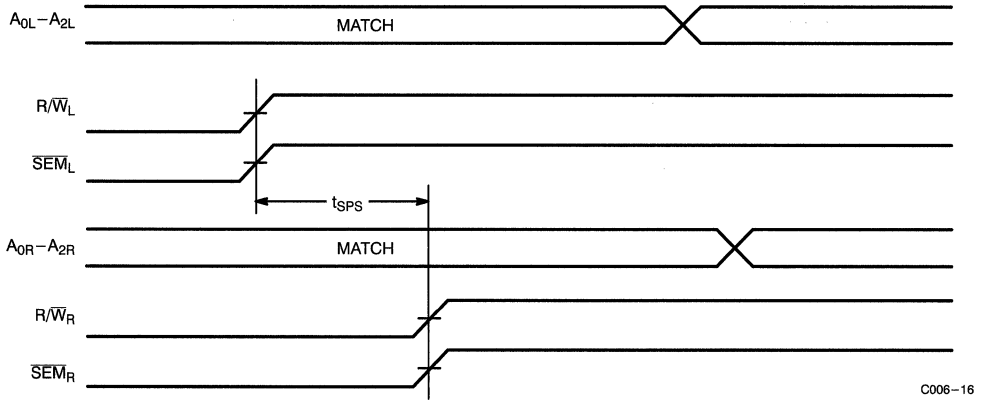
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.
24. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[25]



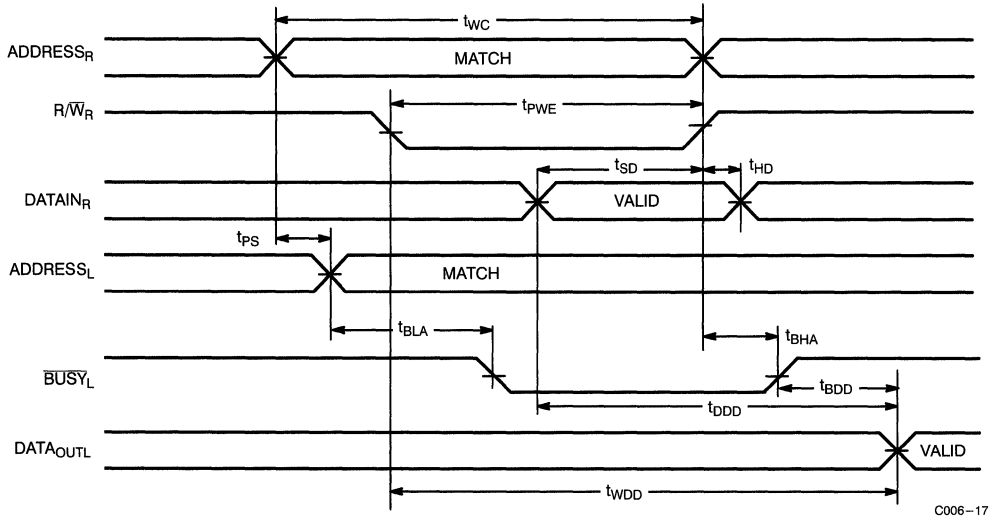
Semaphore Contention[26, 27, 28]



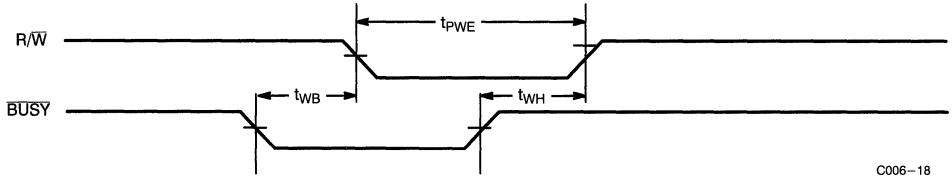
Notes:
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[20]



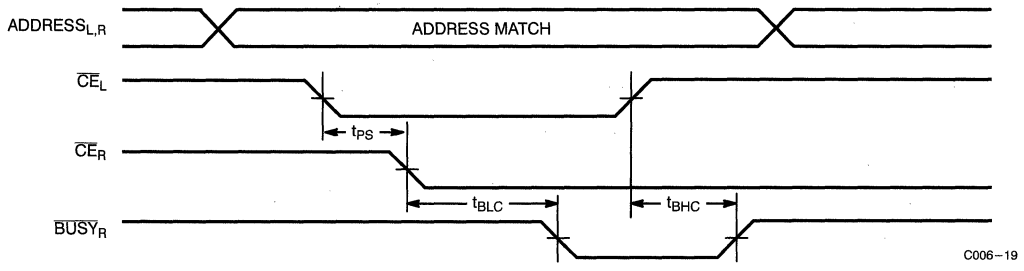
Write Timing with Busy Input (M/$\overline{S}$=LOW)



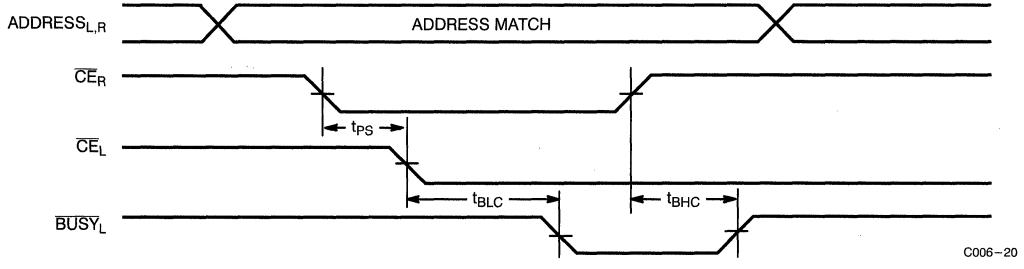
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[29]

$\overline{CE}_L$ Valid First:

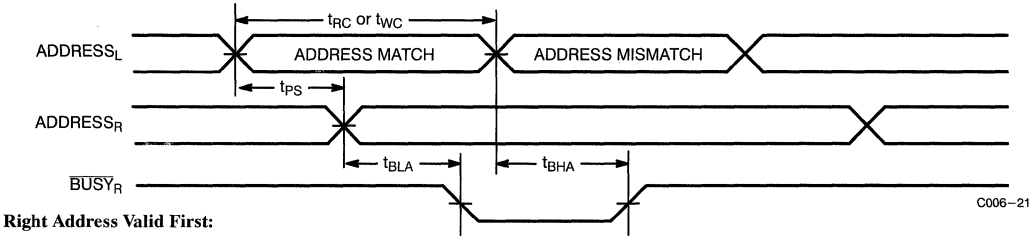


$\overline{CE}_R$ Valid First:

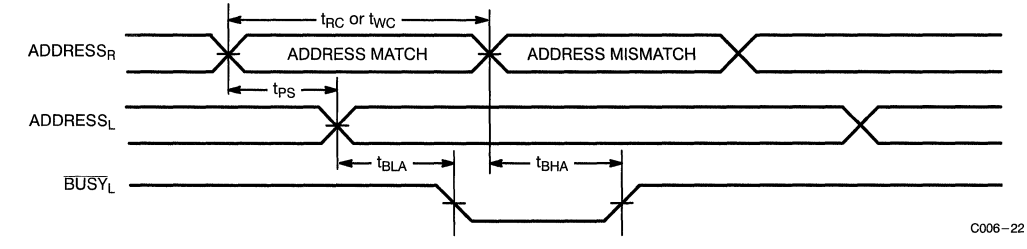


Busy Timing Diagram No. 2 (Address Arbitration)[29]

Left Address Valid First:



Right Address Valid First:



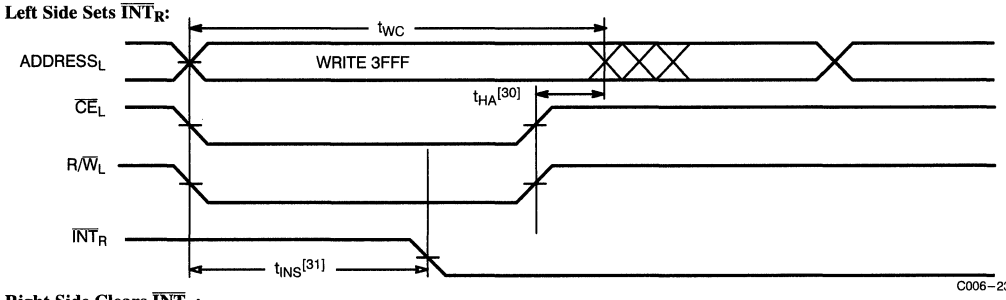
Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

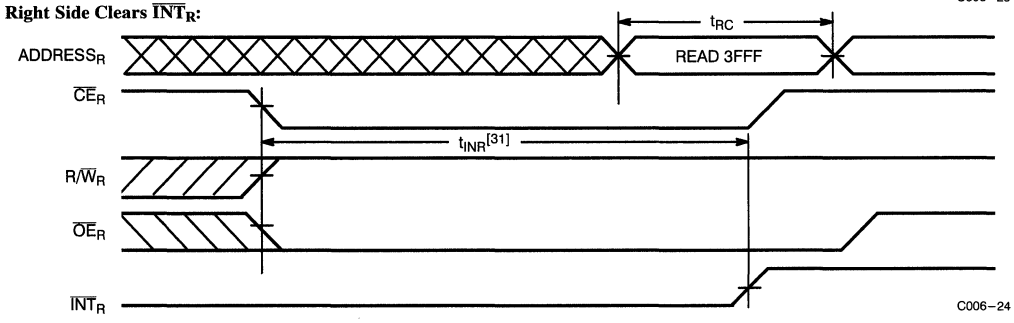
Switching Waveforms (continued)

Interrupt Timing Diagrams

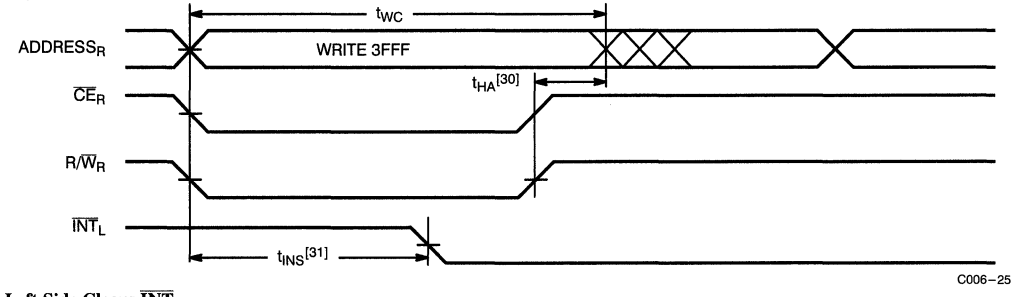
Left Side Sets $\overline{INT}_R$:



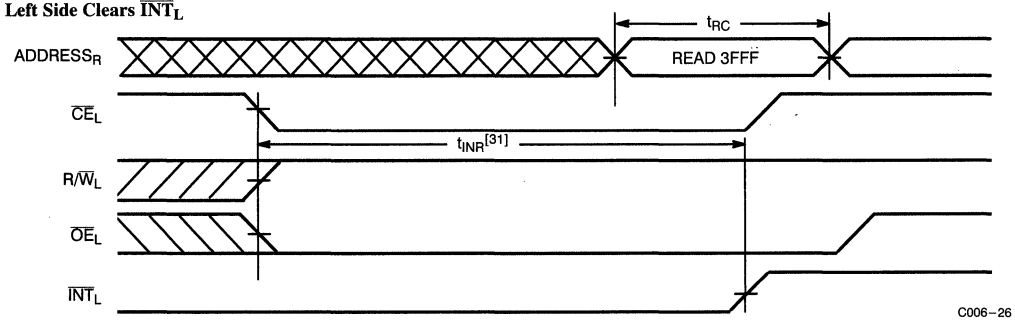
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Architecture

The CY7C006/016 consists of a an array of 16K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C006/016 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C006/016 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⎍	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7C006/016 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location 3FFE(HEX), the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location 3FFE(HEX). This flag is cleared when the left port reads location 3FFE(HEX). The message at 3FFE(HEX) is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C006/016 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006/016 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Table 2. Interrupt Operation Example (assumes $\overline{BUSY_L}$=$\overline{BUSY_R}$=HIGH)

	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0L-13L}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0R-13R}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	3FFE	X
Reset Left $\overline{INT}$	X	L	L	3FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	3FFE	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	3FFE	H

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and $R/\overline{W}$ are used in the same manner as a normal memory access.When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 3. Semaphore Operation Example

Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C006–15AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C006–25AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–25AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C006–35AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–35AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C006–55AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–55AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C016–15AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C016–25AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–25AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C016–35AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–35AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C016–55AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–55AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38–00163

CY7C024/0241
CY7C025/0251

4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with Sem, Int, Busy

Features

- **4K x 16 organization (CY7C024)**
- **4K x 18 organization (CY7C0241)**
- **8K x 16 organization (CY7C025)**
- **8K x 18 organization (CY7C0251)**
- **High-speed access**
  — 15 ns
- **Automatic power-down**
- **Low operating power**
  — I_{CC} = 150 mA (typ.)
- **Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device**
- **On chip arbitration logic**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Separate upper byte and lower byte control**
- **Pin select for Master or Slave**
- **Available in 84-pin PLCC and 100-pin TQFP**
- **Pin-compatible and functional equivalent to IDT7024/IDT7025**

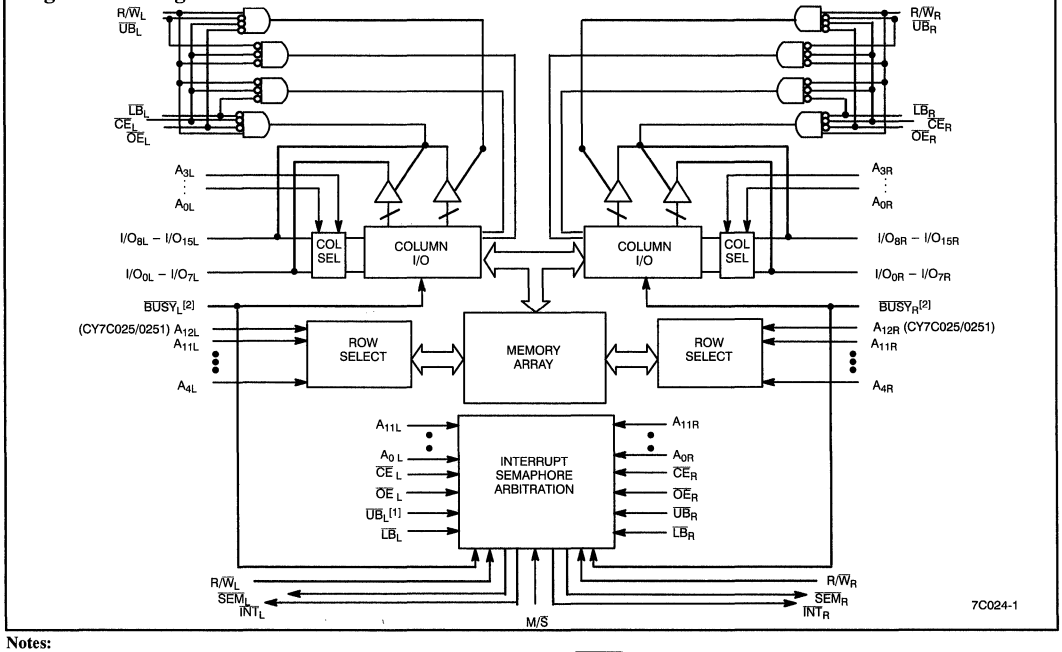
Functional Description

The CY7C024/0241 and CY7C025/0251 are low-power CMOS 4K x 16/18 and 8K x 16/18 dual-port static RAMs. Various arbitration schemes are included on the CY7C024/0241 and CY7C025/0251 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C024/0241 and CY7C025/0251 can be utilized as standalone 16-/18-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32-/36-bit or wider master/slave dual-port static RAM. An $\overline{M/S}$ pin is provided for implementing 32-/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip select ($\overline{CE}$) pin.

The CY7C024/0241 and CY7C025/0251 are available in 84-pin PLCCs (CY7C024 and CY7C025 only) and 100-pin Thin Quad Plastic Flatpack (TQFP).

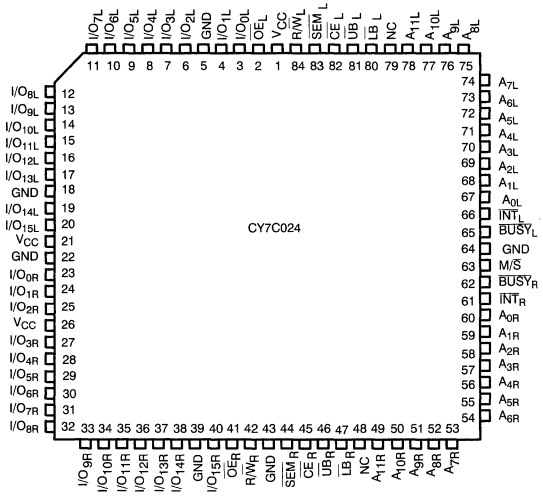
Logic Block Diagram



Notes:
1. LB=Lower Byte. UB=Upper Byte.
2. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

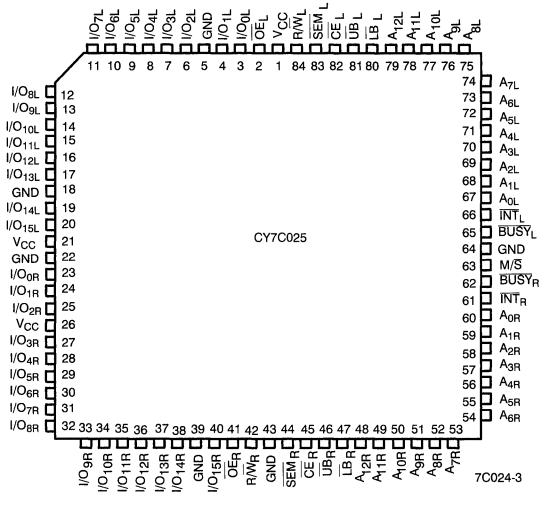
Pin Configurations

84-Pin PLCC
Top View



7C024-2

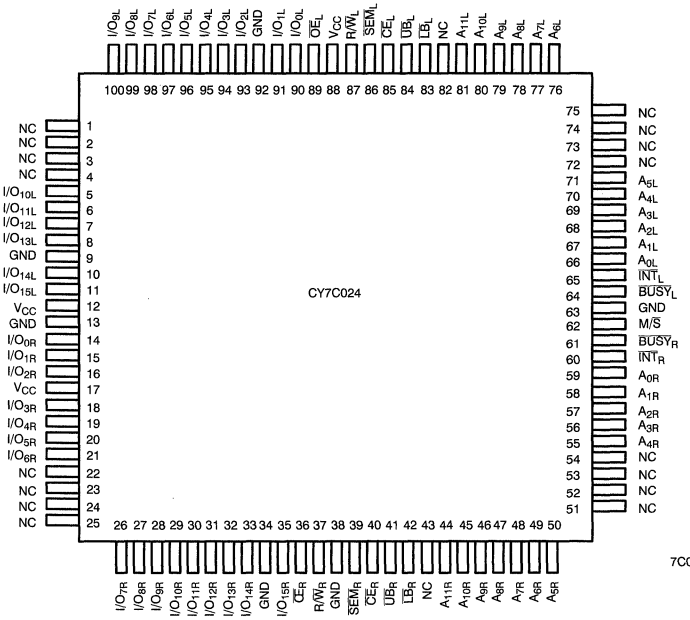
84-Pin PLCC
Top View



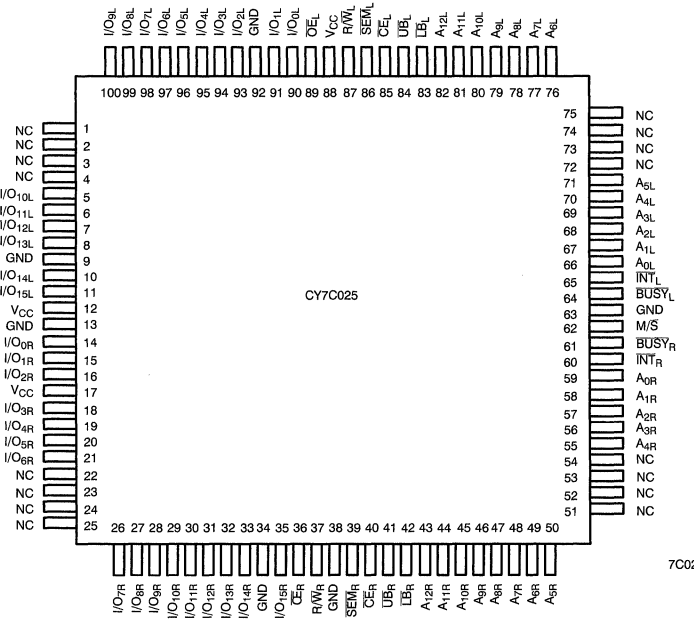
7C024-3

Pin Configurations (continued)

100-Pin TQFP
Top View



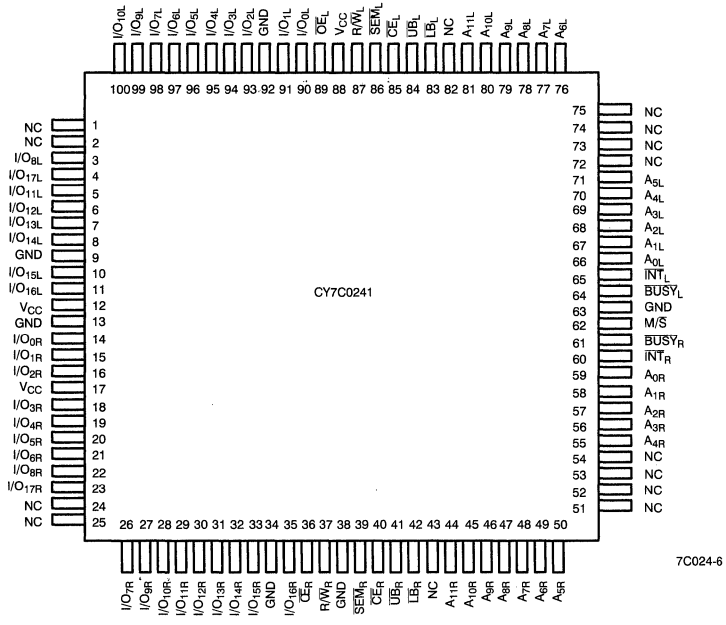
7C024-4



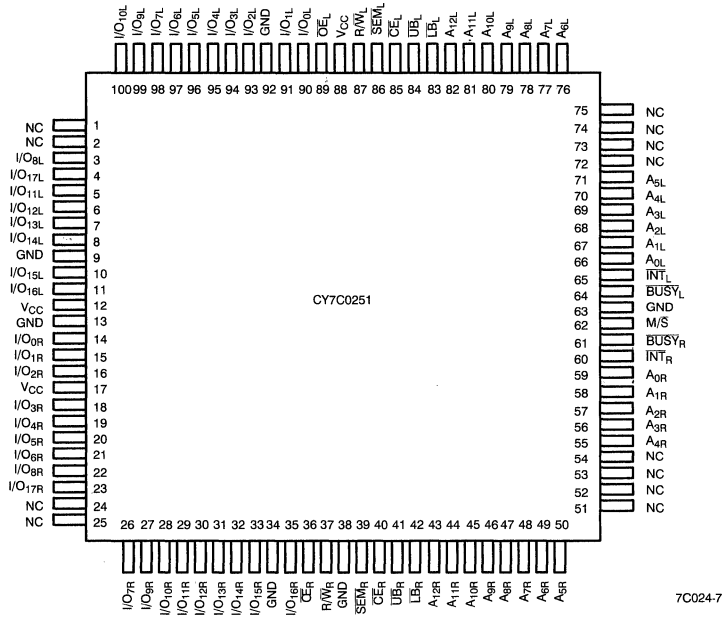
7C024-5

Pin Configurations (continued)

100-Pin TQFP
Top View



7C024-6



7C024-7

Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}-A_{12L}$	$A_{0R}-A_{12R}$	Address
$I/O_{0L}-I/O_{15L}$	$I/O_{0R}-I/O_{15R}$	Data Bus Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

	7C024/0241–15 7C025/0251–15	7C024/0241–25 7C025/0251–25	7C024/0241–35 7C025/0251–35	7C024/0241–55 7C025/0251–55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	280	250	230	220
Maximum Standby Current for I_{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to + 150°C

Ambient Temperature with Power Applied ..... −55°C to + 125°C

Supply Voltage to Ground Potential ..... −0.3V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to + 7.0V

DC Input Voltage[3] ..... −0.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Note:
3. Pulse width < 20 ns.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C024/0241–15 7C025/0251–15 Min.	Typ.	Max.	7C024/0241–25 7C025/0251–25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10		+10	−10		+10	μA
I_{OZ}	Output Leakage Current	Output Disabled, $GND \le V_O \le V_{CC}$		−10		+10	−10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		190	280		170	250	mA
			Ind					170	290	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[4]	Com'l		50	70		40	60	mA
			Ind						75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[4]	Com'l		120	180		100	140	mA
			Ind					100	160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0[4]	Com'l		3	15		3	15	mA
			Ind					3	15	
I_{SB4}	Standby Current (Both Ports CMOS Levels)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, Active Port Outputs, f = f_{MAX}[4]	Com'l		110	160		90	120	mA
			Ind					90	140	

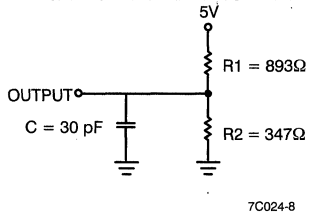
Parameter	Description	Test Conditions		7C024/0241–35 7C025/0251–35 Min.	Typ.	Max.	7C024/0241–55 7C025/0251–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10		+10	−10		+10	μA
I_{OZ}	Output Leakage Current	Output Disabled, $GND \le V_O \le V_{CC}$		−10		+10	−10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		160	230		150	220	mA
			Ind		160	260		150	250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[4]	Com'l		30	50		20	40	mA
			Ind		30	65		20	60	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[4]	Com'l		85	125		75	110	mA
			Ind		85	140		75	145	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0[4]	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
I_{SB4}	Standby Current (Both Ports CMOS Levels)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, Active Port Outputs, f = f_{MAX}[4]	Com'l		80	105		70	90	mA
			Ind		80	120		70	105	

Note:
4. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at $f = 1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

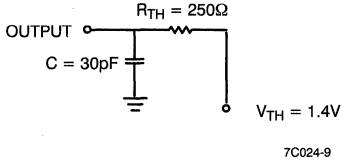
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

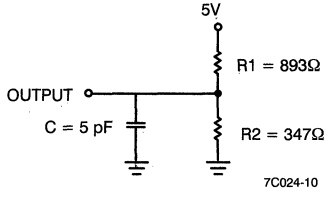
AC Test Loads and Waveforms



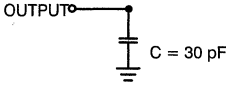
(a) Normal Load (Load 1)



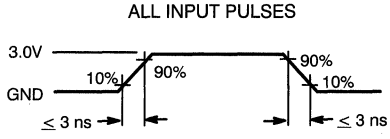
(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 3)



Load (Load 2)



Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C024/0241–15 7C025/0251–15 Min.	7C024/0241–15 7C025/0251–15 Max.	7C024/0241–25 7C025/0251–25 Min.	7C024/0241–25 7C025/0251–25 Max.	7C024/0241–35 7C025/0251–35 Min.	7C024/0241–35 7C025/0251–35 Max.	7C024/0241–55 7C025/0251–55 Min.	7C024/0241–55 7C025/0251–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}[7]	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		20		25	ns
t_{LZOE}[8, 9]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[8, 9]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[8, 9]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[8, 9]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		25			ns
t_{ABE}[7]	Byte Enable Access Time		15		25		35		55	ns

Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. To access RAM, $\overline{CE}$=L, $\overline{UB}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire t_{SCE} time.
8. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C024/0241–15 7C025/0251–15		7C024/0241–25 7C025/0251–25		7C024/0241–35 7C025/0251–35		7C024/0241–55 7C025/0251–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}[7]	$\overline{CE}$ LOW to Write End	12		20		30		35		ns
t_{AW}	Address Set-Up to Write End	12		20		30		35		ns
t_{HA}	Address Hold From Write End	0		0		0		0		ns
t_{SA}[7]	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		35		ns
t_{SD}	Data Set-Up to Write End	10		15		15		20		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[9]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[9]	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		ns
t_{WDD}[10]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[10]	Write Data Valid to Read Data Valid		25		35		35		45	ns
BUSY TIMING[11]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		40	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		40	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		35	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	13		20		30		40		ns
t_{BDD}[12]	$\overline{BUSY}$ HIGH to Data Valid		Note 12		Note 12		Note 12		Note 12	ns
INTERRUPT TIMING[11]										
t_{INS}	$\overline{INT}$ Set Time		15		20		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		20		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		12		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		10		10		15		ns
t_{SPS}	SEM Flag Contention Window	5		10		10		15		ns
t_{SAA}	SEM Address Access Time		15		25		35		55	ns

Notes:

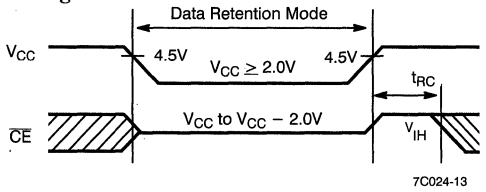
10. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
11. Test conditions used are Load 2.
12. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Data Retention Mode

The CY7C024/0241 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to V_{CC} − 0.2V.
2. $\overline{CE}$ must be kept between V_{CC} − 0.2V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{CC} reaches the minimum operating voltage (4.5 volts).

Timing

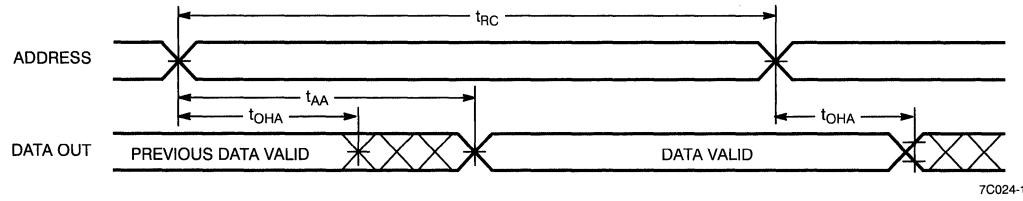


Parameter	Test Conditions[13]	Max.	Unit
ICC_{DR1}	@ VCC_{DR} = 2V	1.5	mA

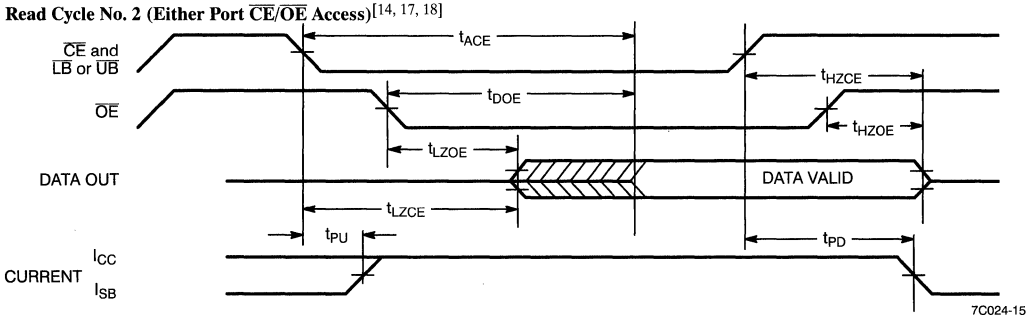
Note:
13. $\overline{CE}$ = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25°C. This parameter is guaranteed but not tested.

Switching Waveforms

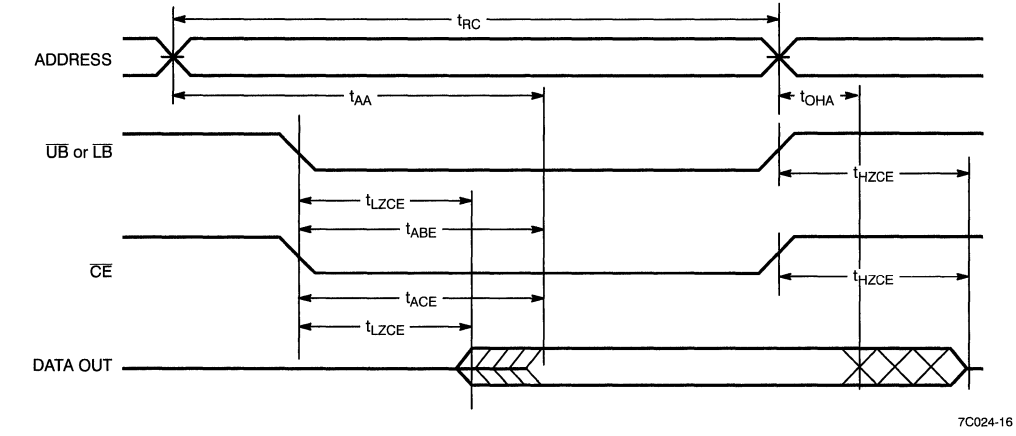
Read Cycle No. 1 (Either Port Address Access)[14, 15, 16]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[14, 17, 18]



Read Cycle No. 3 (Either Port)[14, 16, 17, 18]

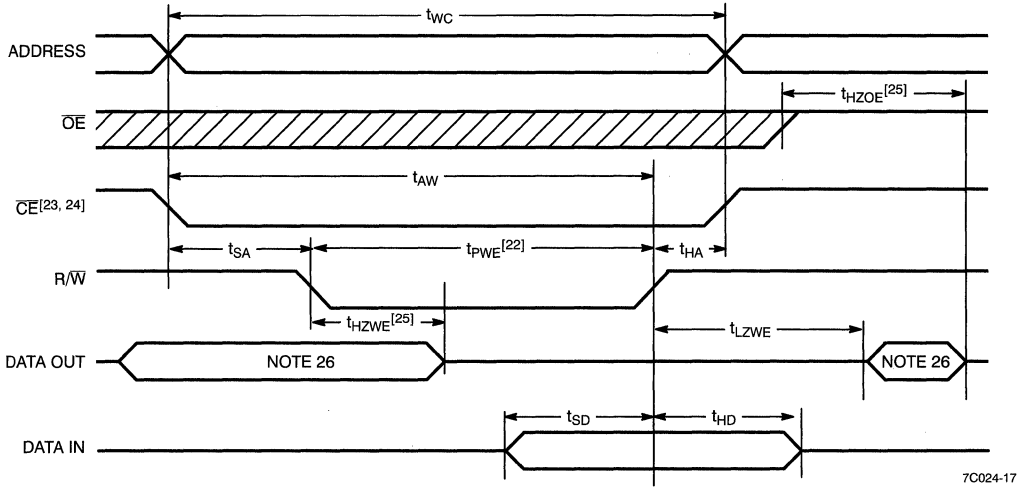


Notes:

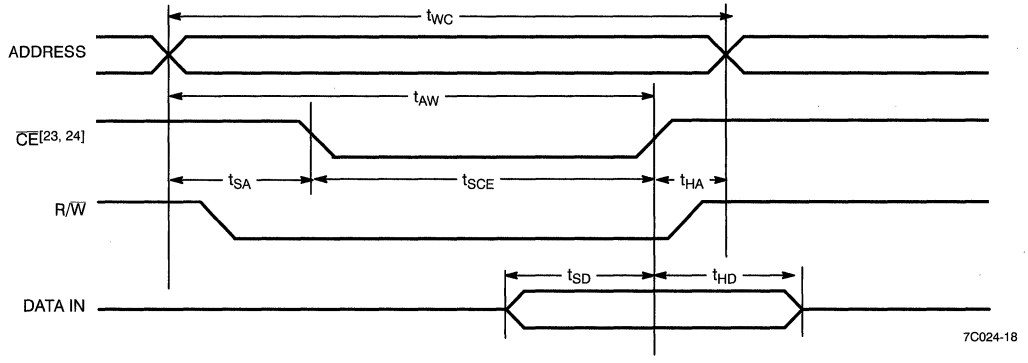
14. R/$\overline{W}$ is HIGH for read cycles.
15. Device is continuously selected $\overline{CE} = V_{IL}$ and $\overline{UB}$ or $\overline{LB} = V_{IL}$. This waveform cannot be used for semaphore reads.
16. $\overline{OE} = V_{IL}$.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. To access RAM, $\overline{CE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

Switching Waveforms (continued)

Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[19, 20, 21, 22]



Write Cycle No. 2: $\overline{CE}$ Controlled Timing[19, 20, 21, 27]

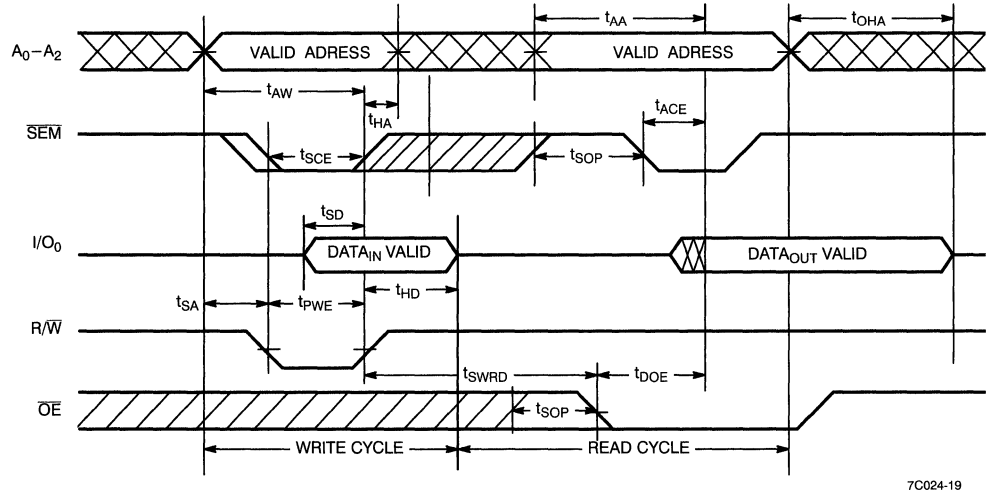


Notes:

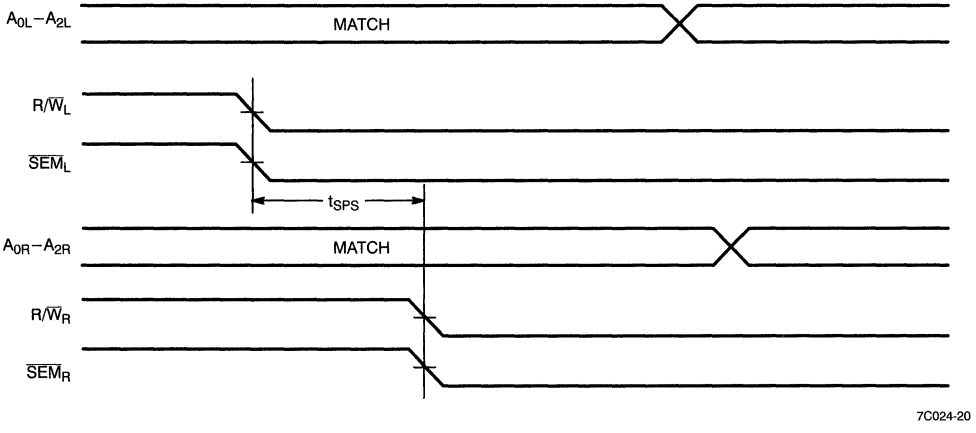
19. R/$\overline{W}$ must be HIGH during all address transitions.
20. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
21. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
24. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
25. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
26. During this period, the I/O pins are in the output state, and input signals must not be applied.
27. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[28]



Timing Diagram of Semaphore Contention[29, 30, 31]

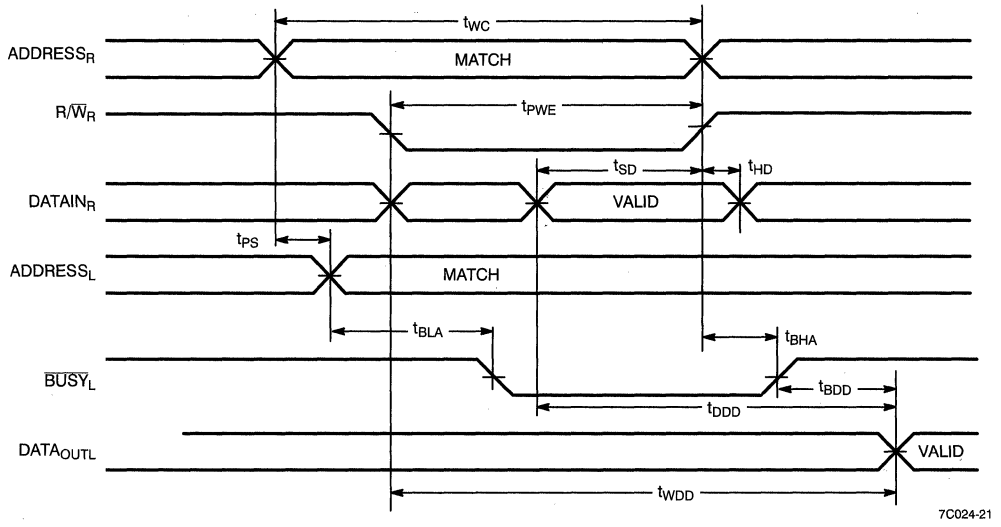


Notes:

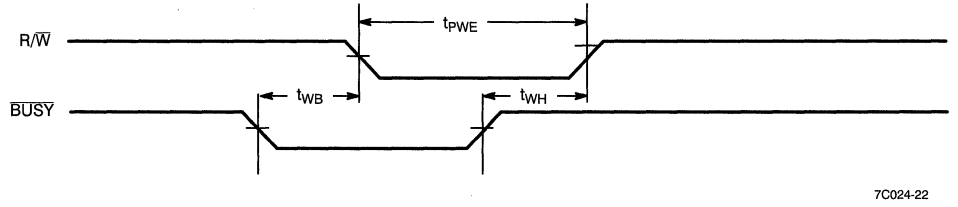
28. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
29. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
30. Semaphores are reset (available to both ports) at cycle start.
31. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[32]



Write Timing with Busy Input (M/$\overline{S}$=LOW)

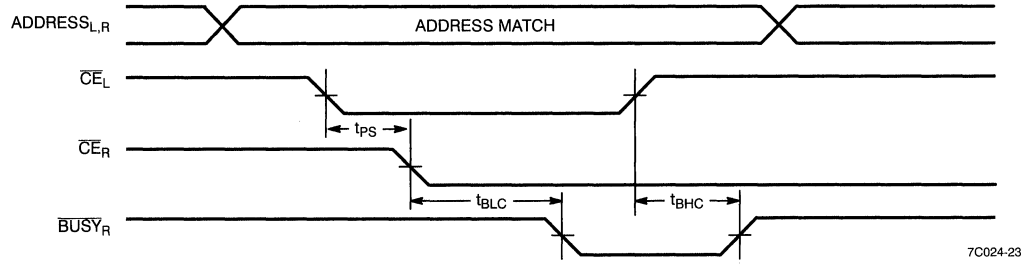


Note:
32. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

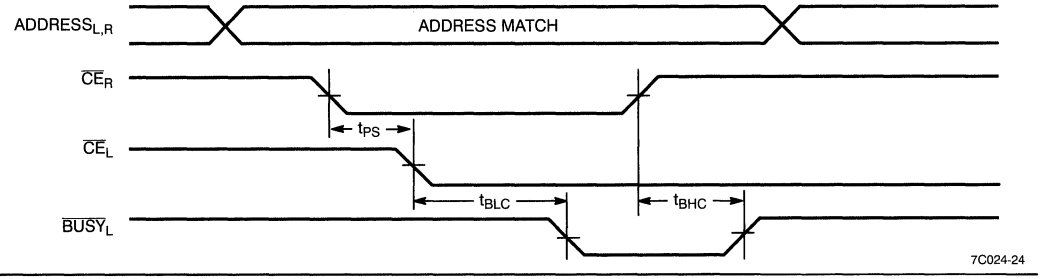
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[33]

$\overline{CE}_L$ Valid First:

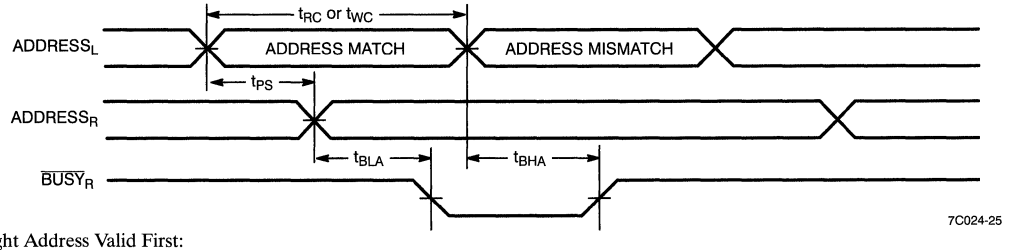


$\overline{CE}_R$ Valid First:

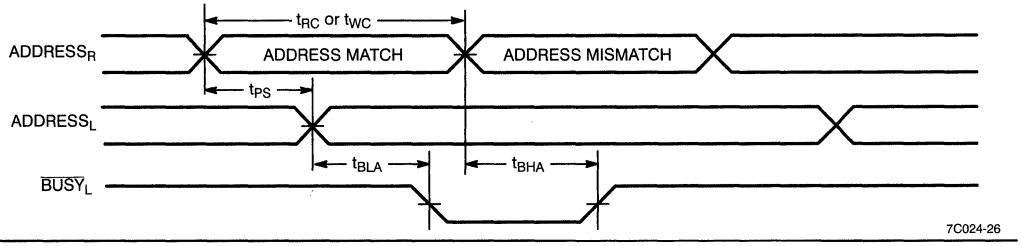


Busy Timing Diagram No. 2 (Address Arbitration)[33]

Left Address Valid First:



Right Address Valid First:

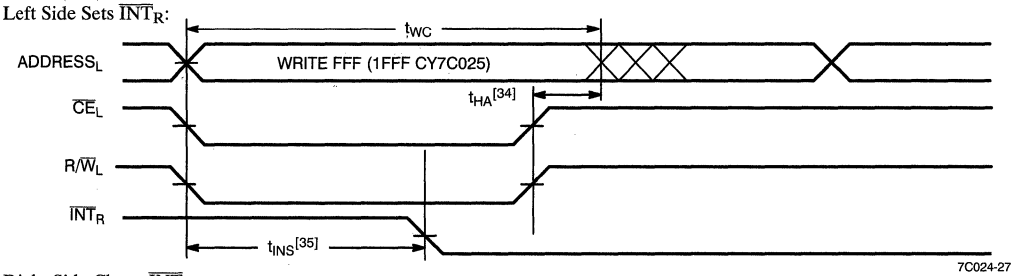


Note:
33. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

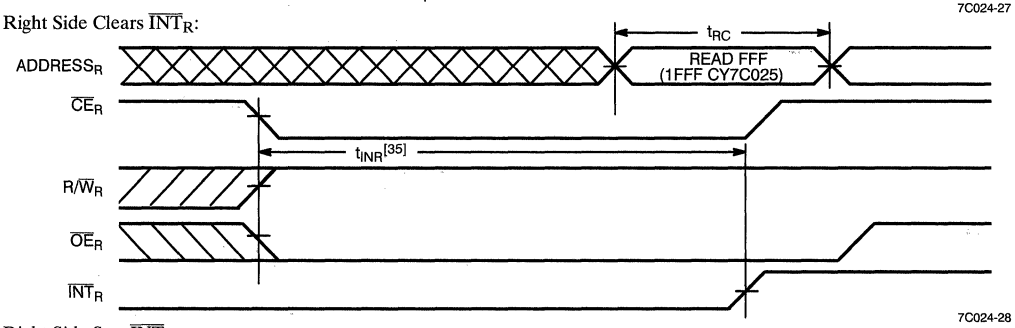
Switching Waveforms (continued)

Interrupt Timing Diagrams

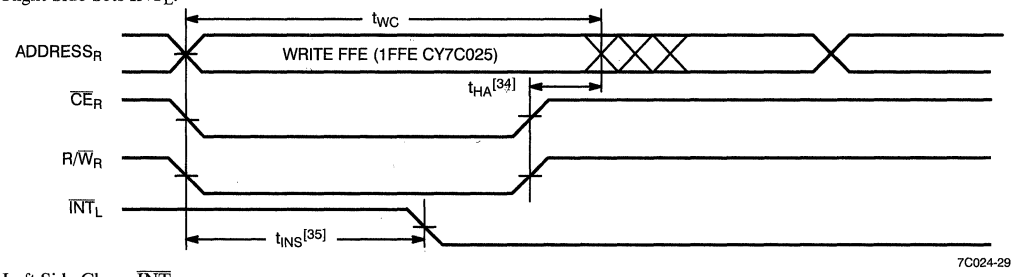
Left Side Sets $\overline{INT}_R$:



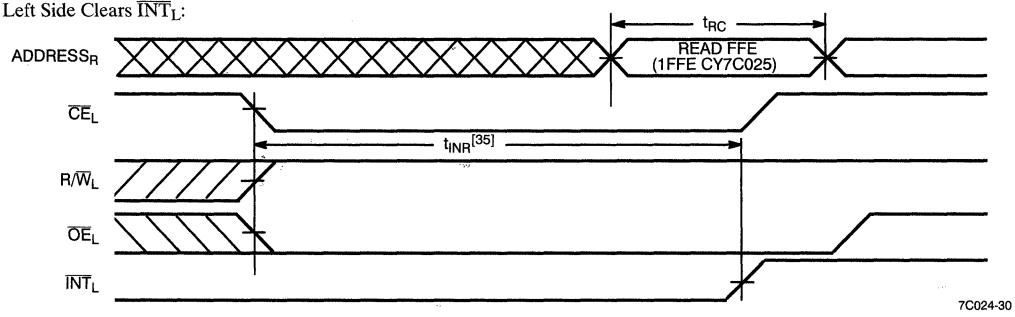
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes:

34. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
35. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7C024/0241 and CY7C025/0251 consist of an array of 4K words of 16/18 bits each and 8K words of 16/18 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C024/0241 and CY7C025/0251 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C024/0241 and CY7C025/0251 have an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}$ pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user of the CY7C024/0241 or CY7C025/0251 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C024/0241, 1FFF for the CY7C025/0251) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C024/0241, 1FFE for the CY7C025/0251) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and thus resetting the interrupt to it.

If your application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2*.

Busy

The CY7C024/0241 and CY7C025/0251 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but which one is not predictable. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C024/0241 and CY7C025/0251 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all sixteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write

Inputs						Outputs		Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	$I/O_8-I/O_{15}$	$I/O_0-I/O_7$	
H	X	X	X	X	H	High Z	High Z	Deselected: Power-Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	⎍	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	⎍	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L=\overline{BUSY}_R$=HIGH)[36]

	Left Port					Right Port				
Function	R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-11L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-11R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	(1)FFF	X	X	X	X	X	L[38]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	(1)FFF	H[37]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[37]	L	L	X	(1)FFE	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	(1)FFE	H[38]	X	X	X	X	X

Table 3. Semaphore Operation Example

Function	D_0-D_{15} Left	D_0-D_{15} Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore.
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes:
36. A_{0L-12L} and A_{0R-12R}, 1FFF/1FFE for the CY7C025.
37. If $\overline{BUSY}_R$=L, then no change.
38. If $\overline{BUSY}_L$=L, then no change.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C024–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–15JC	J83	84-Lead Plastic Leaded Chip Carrier	
25	CY7C024–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–25JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C024–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C024–25JI	J83	84-Lead Plastic Leaded Chip Carrier	
35	CY7C024–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–35JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C024–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C024–35JI	J83	84-Lead Plastic Leaded Chip Carrier	
55	CY7C024–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–55JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C024–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C024–55JI	J83	84-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C025–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–15JC	J83	84-Lead Plastic Leaded Chip Carrier	
25	CY7C025–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–25JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C025–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C025–25JI	J83	84-Lead Plastic Leaded Chip Carrier	
35	CY7C025–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–35JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C025–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C025–35JI	J83	84-Lead Plastic Leaded Chip Carrier	
55	CY7C025–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–55JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C025–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C025–55JI	J83	84-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0241–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0241–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
35	CY7C0241–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
55	CY7C0241–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0251–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0251–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
35	CY7C0251–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
55	CY7C0251–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Document #: 38–00255–A

CY7C130/CY7C131
CY7C140/CY7C141

1K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141**
- **$\overline{BUSY}$ output flag on CY7C130/CY7C131; $\overline{BUSY}$ input on CY7C140/CY7C141**
- **$\overline{INT}$ flag for port-to-port communication**
- **Pin compatible and functionally equivalent to IDT7130 and IDT7140**

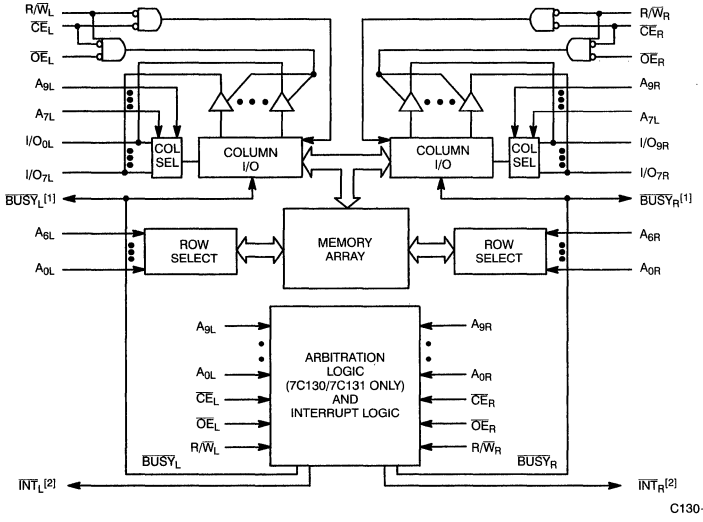
Functional Description

The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

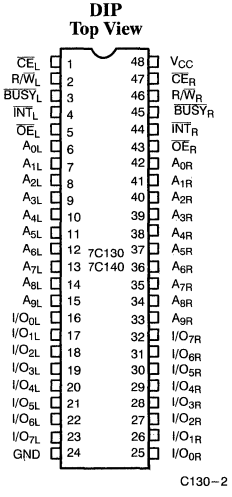
Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in 52-pin LCC, PLCC, and PQFP.

Logic Block Diagram



Pin Configurations

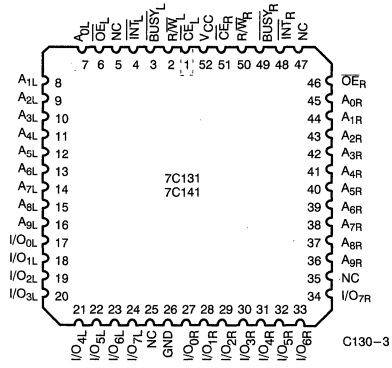


Notes:

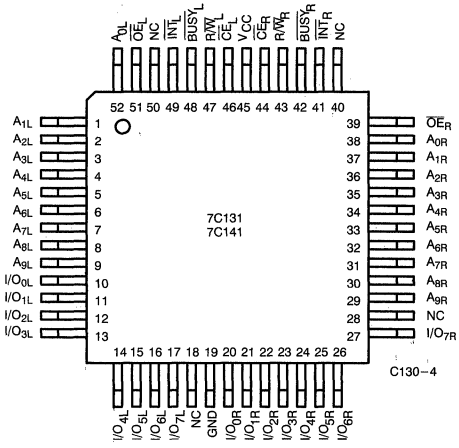
1. CY7C130/CY7C131 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs: pull-up resistor required.

Pin Configurations (continued)

LCC/PLCC
Top View



PQFP
Top View



Selection Guide

		7C130-25[3] 7C131-25 7C140-25 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available only in PLCC/PQFP packages.
4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

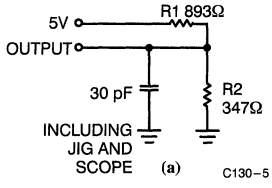
Parameter	Description	Test Conditions		7C130–25, 30[3] 7C131–25, 30 7C140–25, 30 7C141–25, 30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45, 55 7C131–45, 55 7C140–45, 55 7C141–45, 55		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[7, 8]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[9]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[9]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		105		85		70	mA
			Mil				105		85	

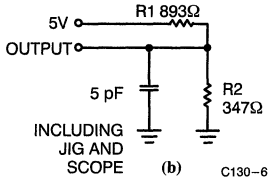
Capacitance[8]

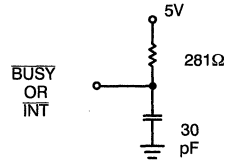
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. Tested initially and after any design or process changes that may affect these parameters.
9. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.

AC Test Loads and Waveforms



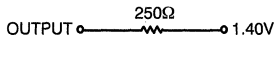




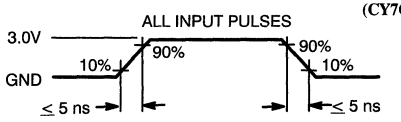
BUSY Output Load (CY7C130/CY7C131 ONLY)

C130-7

Equivalent to: THÉVENIN EQUIVALENT



C130-8



C130-9

Switching Characteristics Over the Operating Range[5, 10]

Parameter	Description	7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12, 13]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12, 13]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[13]		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[13]	0		0		0		0		0		ns

Notes:

10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
11. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[5, 10] (continued)

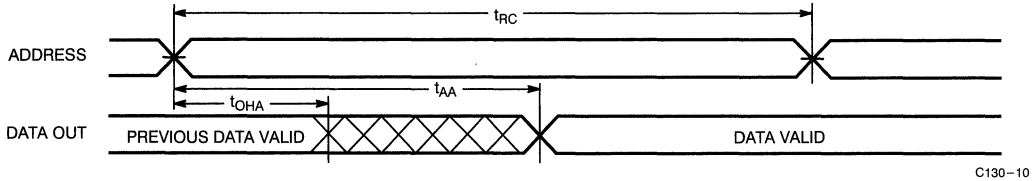
Parameter	Description	7C130–25[3] 7C131–25 7C140–25 7C141–25		7C130–30 7C131–30 7C140–30 7C141–30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45 7C131–45 7C140–45 7C141–45		7C130–55 7C131–55 7C140–55 7C141–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns

Notes:
15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C140/CY7C141 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address is toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
18. R/$\overline{W}$ is HIGH for read cycle.
19. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
21. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
22. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms

Read Cycle No. 1[18, 19]

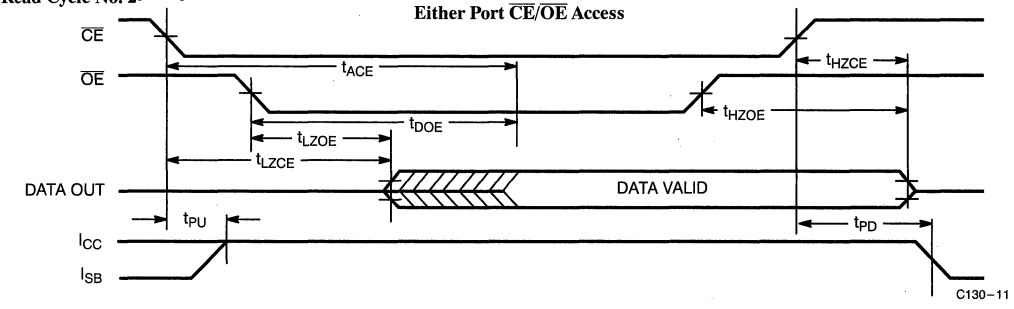
Either Port Address Access



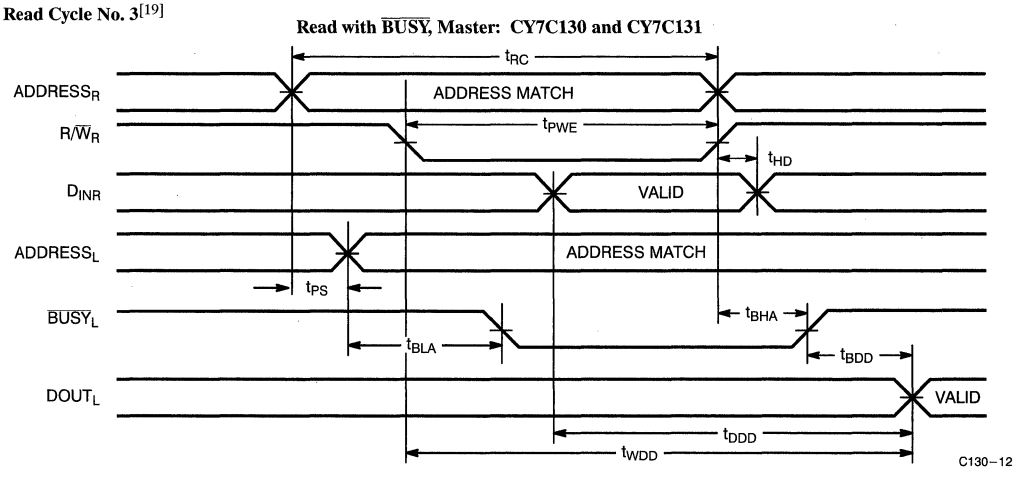
C130–10

Switching Waveforms (continued)

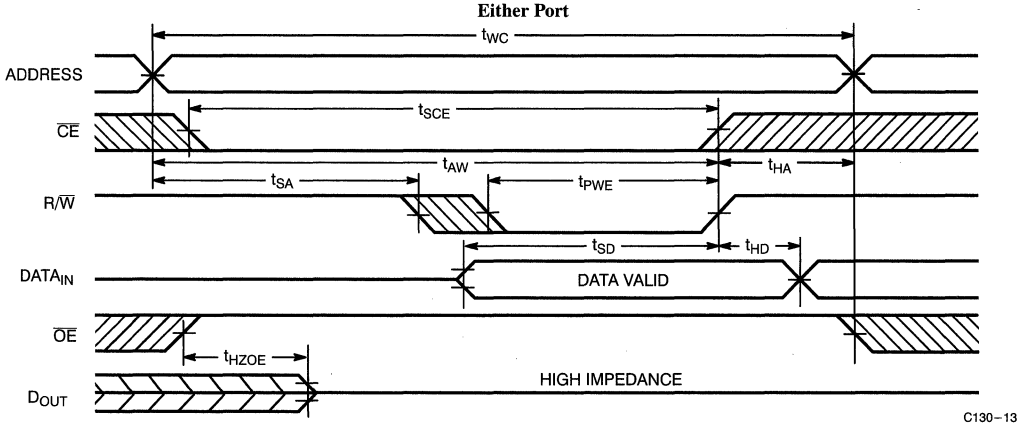
Read Cycle No. 2[18, 20]



Read Cycle No. 3[19]

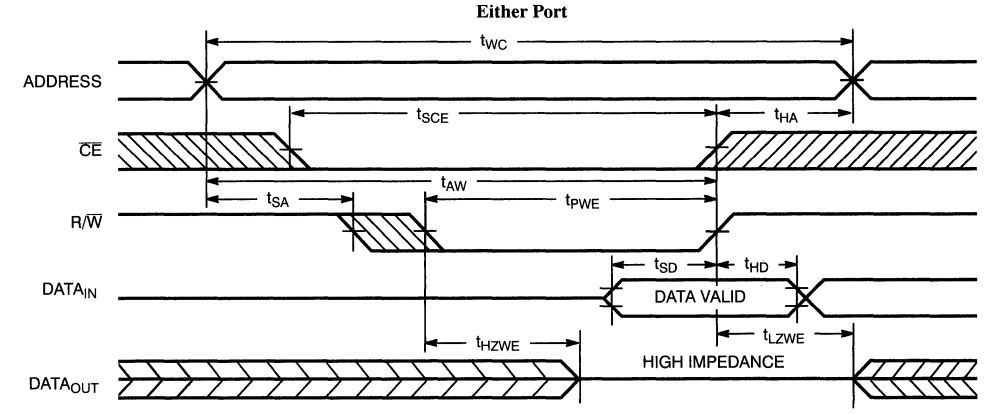


Write Cycle No.1 (OE Three-States Data I/Os – Either Port)[14, 21]



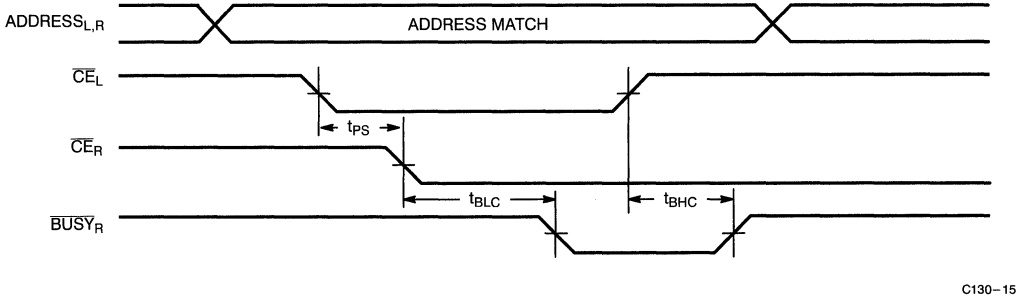
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[15, 22]

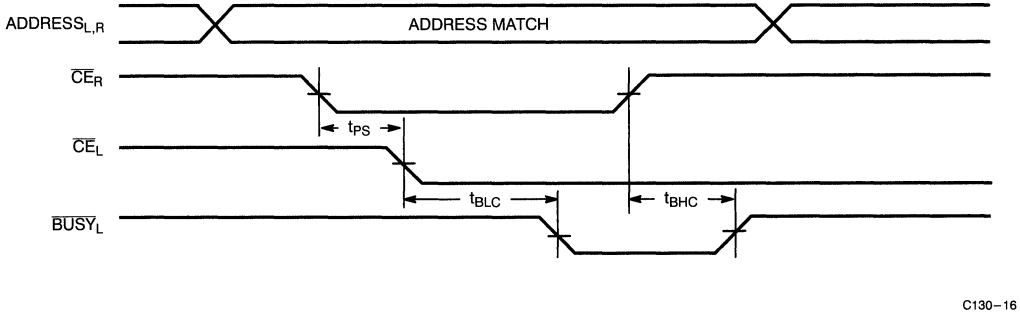


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



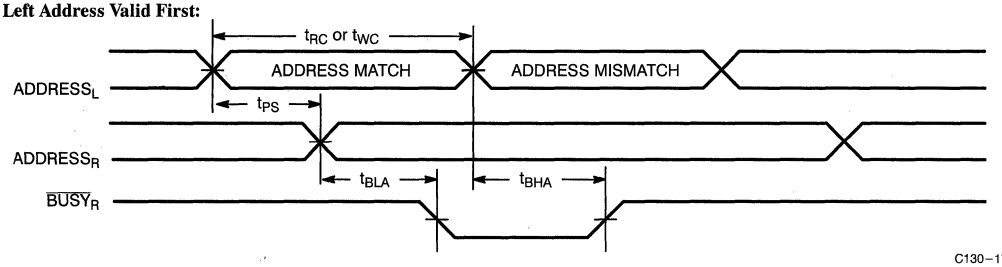
$\overline{CE}_R$ Valid First:



Switching Waveforms (continued)

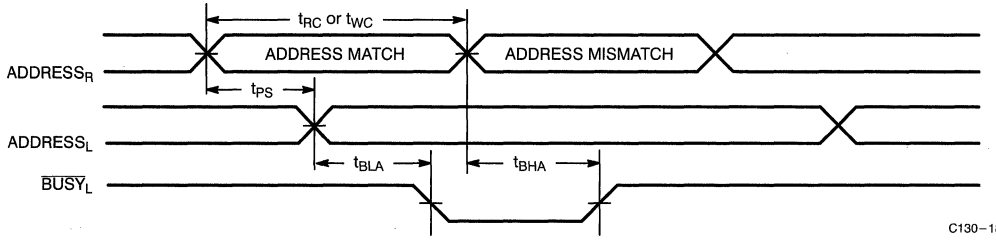
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



C130–17

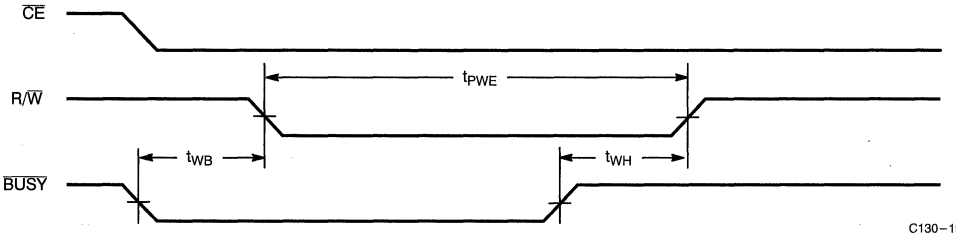
Right Address Valid First:



C130–18

Busy Timing Diagram No. 3

Write with $\overline{BUSY}$ (Slave: CY7C140/CY7C141)

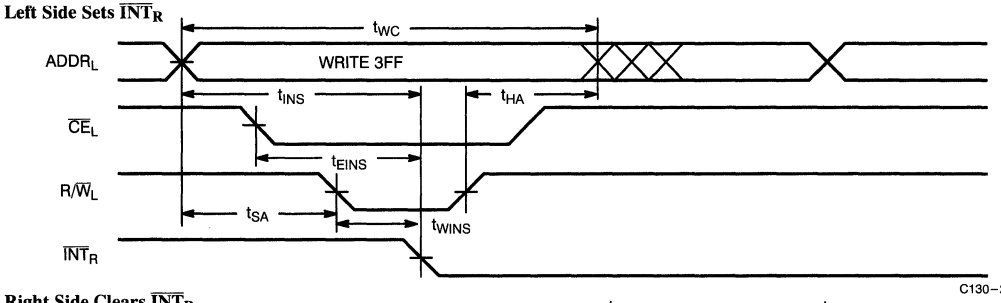


C130–19

Switching Waveforms (continued)

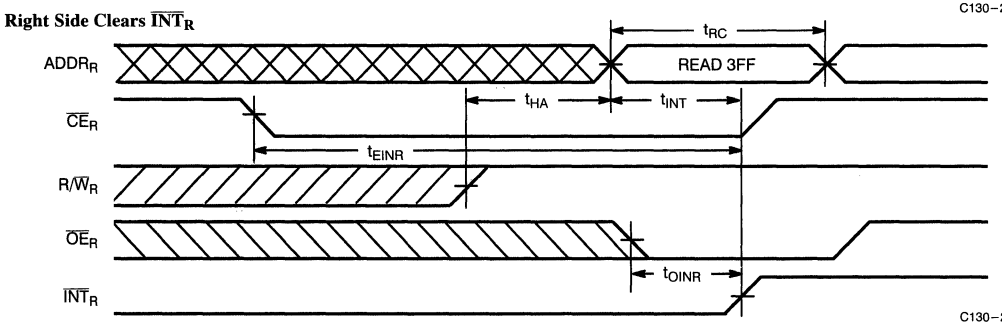
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$



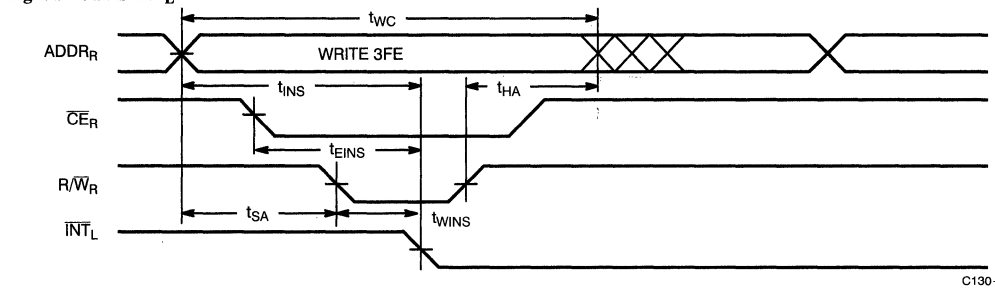
C130–20

Right Side Clears $\overline{INT}_R$



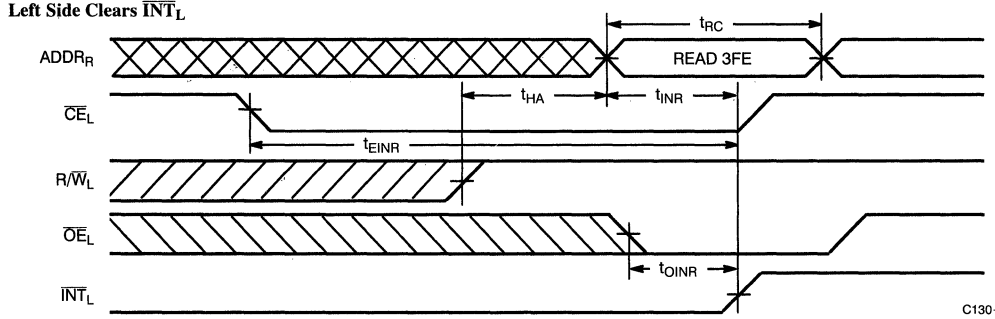
C130–21

Right Side Sets $\overline{INT}_L$



C130–22

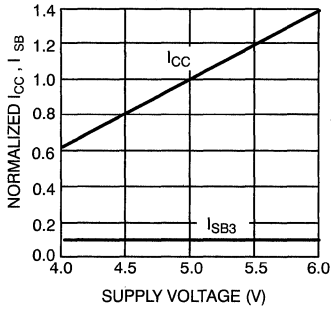
Left Side Clears $\overline{INT}_L$



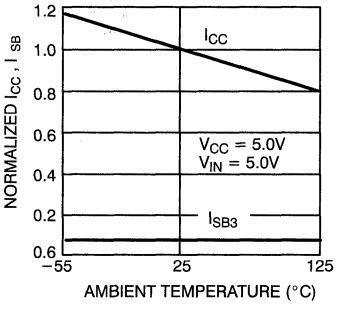
C130–23

Typical DC and AC Characteristics

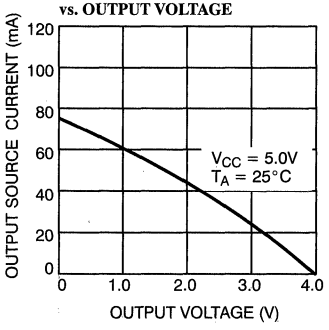
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



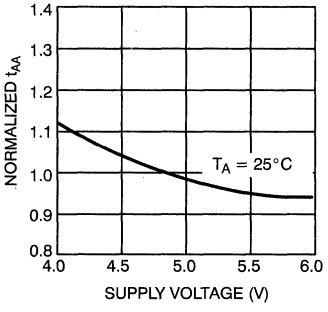
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



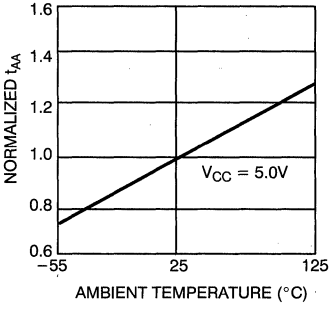
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



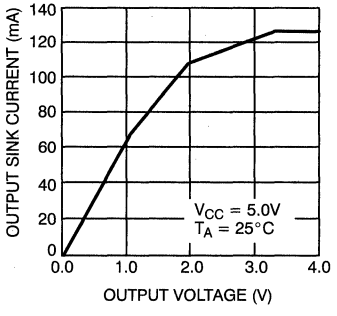
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



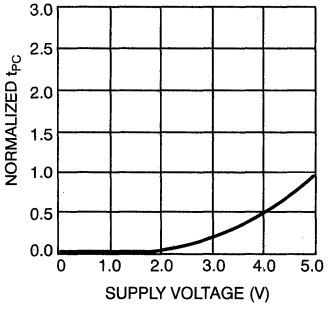
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



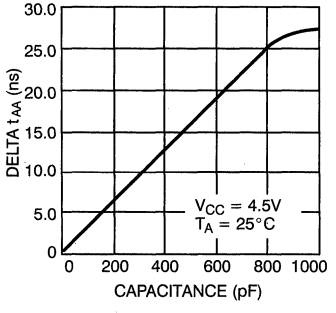
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



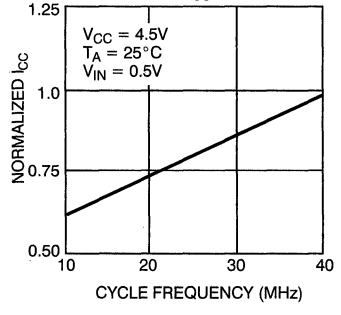
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C130–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C130–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C131–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–35NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C131–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–45NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C131–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–55LMB	L69	52-Square Leadless Chip Carrier	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C140–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C140–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C141–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–35NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C141–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–45NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C141–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–55LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[23]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
23. CY7C140/CY7C141 only.

Document #: 38−00027−K

CY7C132/CY7C136
CY7C142/CY7C146

2K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146**
- **$\overline{BUSY}$ output flag on CY7C132/CY7C136; $\overline{BUSY}$ input on CY7C142/CY7C146**
- **$\overline{INT}$ flag for port-to-port communication (52-pin LCC/PLCC/PQFP versions)**

Functional Description

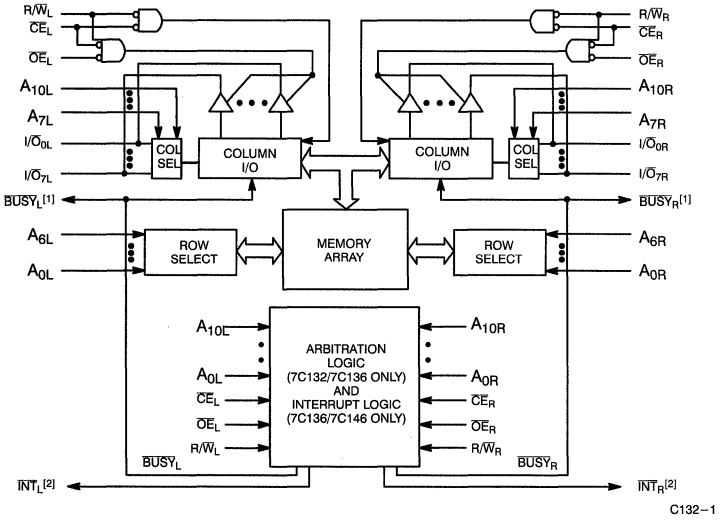
The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin LCC and PLCC versions. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

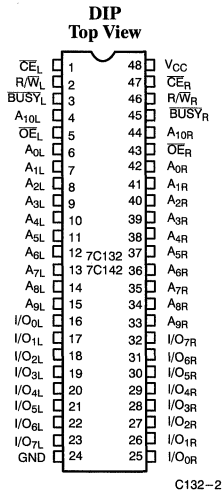
An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in 52-pin LCC, PLCC, and PQFP..

Logic Block Diagram



Pin Configuration



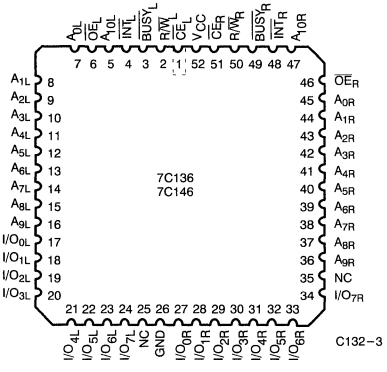
C132-2

Notes:

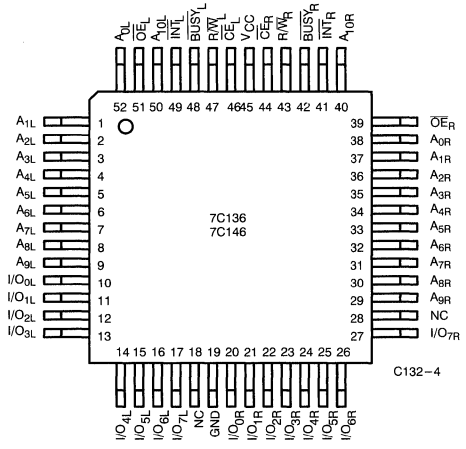
1. CY7C132/CY7C136 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C142/CY7C146 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs; pull-up resistor required.

Pin Configurations (continued)

LCC/PLCC
Top View



PQFP
Top View



Selection Guide

		7C132-25[3] 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available in PQFP and PLCC packages only.
4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C132–25, 30[3] 7C136–25, 30 7C142–25, 30 7C146–25, 30 Min.	Max.	7C132–35 7C136–35 7C142–35 7C146–35 Min.	Max.	7C132–45, 55 7C136–45, 55 7C142–45, 55 7C146–45, 55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[8]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		105		85		70	mA
			Mil				105		85	

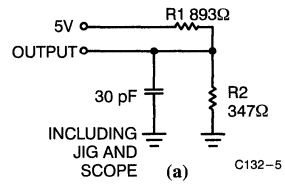
Capacitance[9]

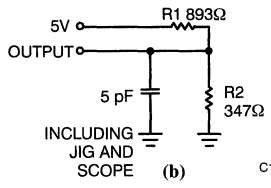
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

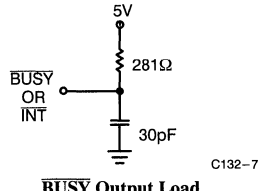
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
11. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms

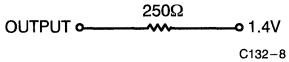


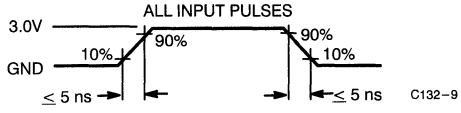




BUSY Output Load (CY7C132/CY7C136 ONLY)

Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[5, 10]

Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

Switching Characteristics Over the Operating Range[5, 10] (continued)

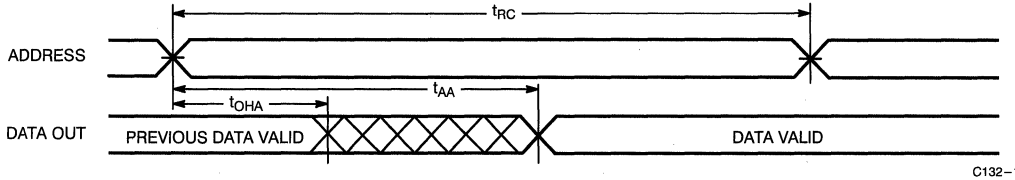
Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING[18]												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns

Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
18. 52-pin LCC/PLCC versions only.
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms

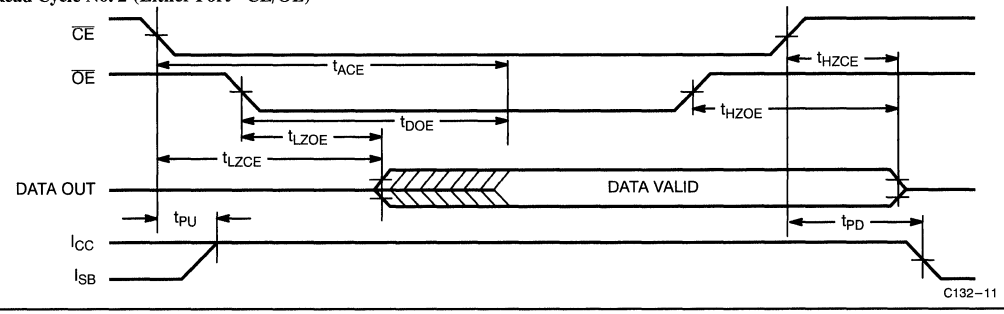
Read Cycle No. 1 (Either Port–Address Access[19, 20]



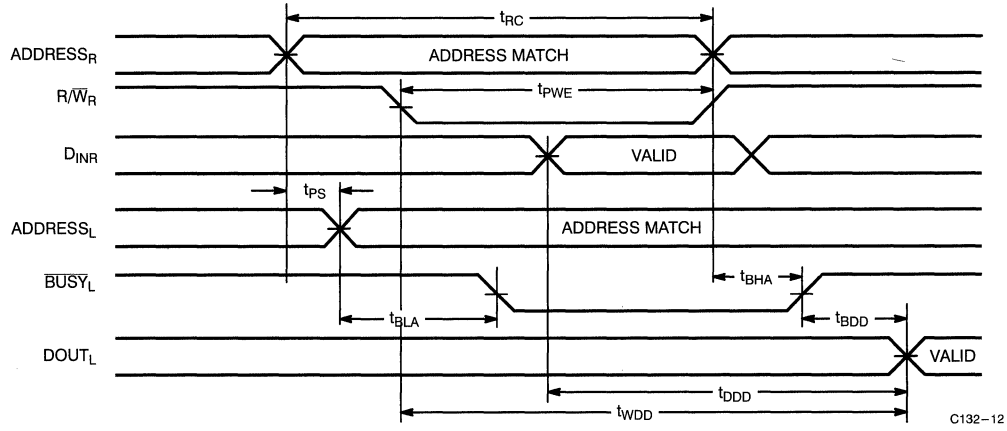
C132–10

Switching Waveforms (continued)

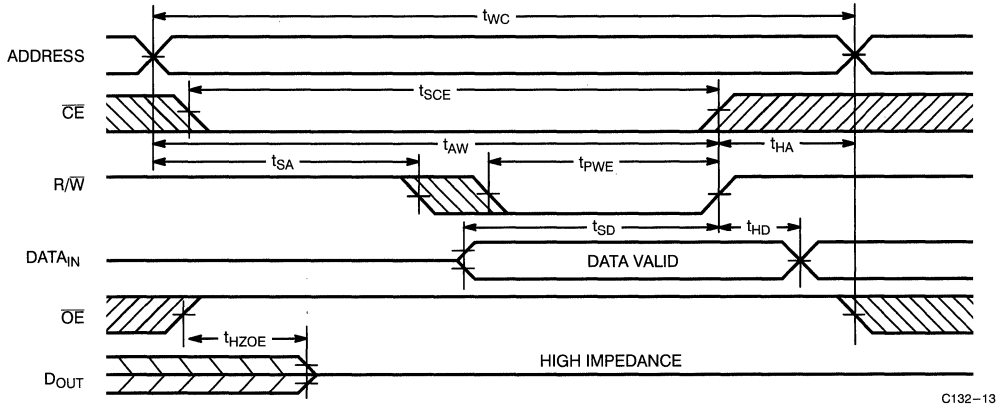
Read Cycle No. 2 (Either Port–$\overline{CE}/\overline{OE}$)[19, 21]



Read Cycle No. 3 (Read with $\overline{BUSY}$ Master: CY7C132 and CY7C136)

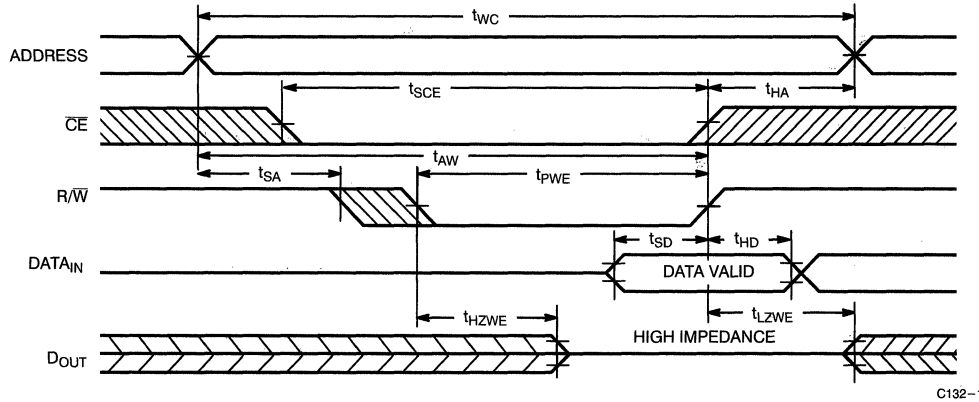


Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port) [14, 22]



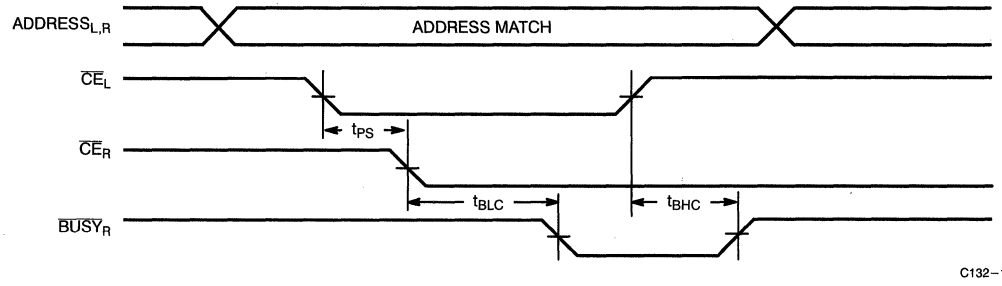
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[14, 23]

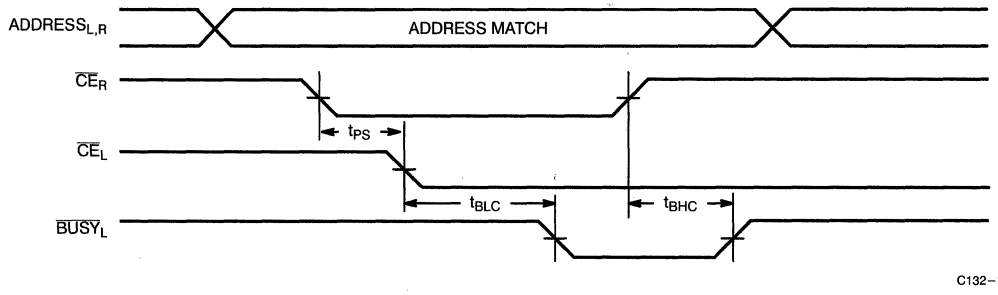


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



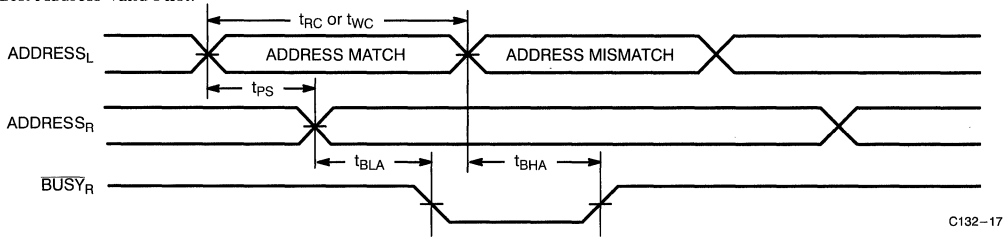
$\overline{CE}_R$ Valid First:



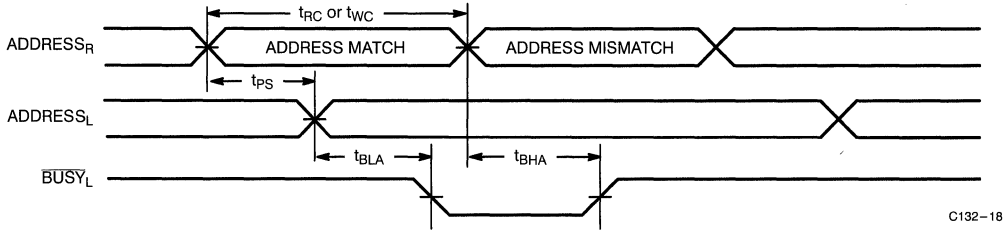
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

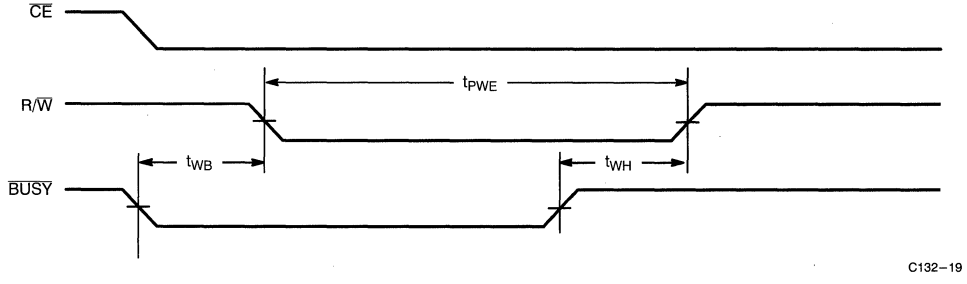
Left Address Valid First:



Right Address Valid First:

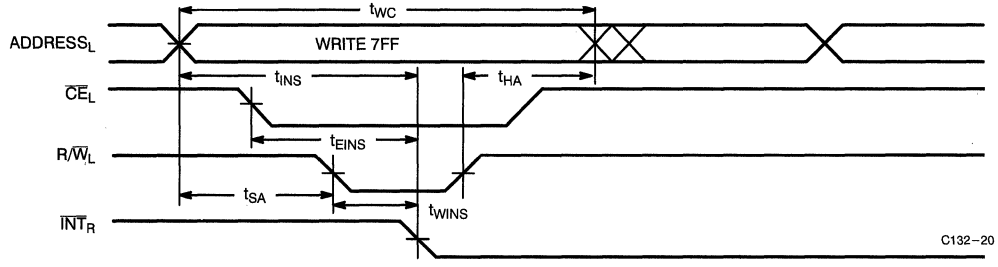


Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave: CY7C142/CY7C146)

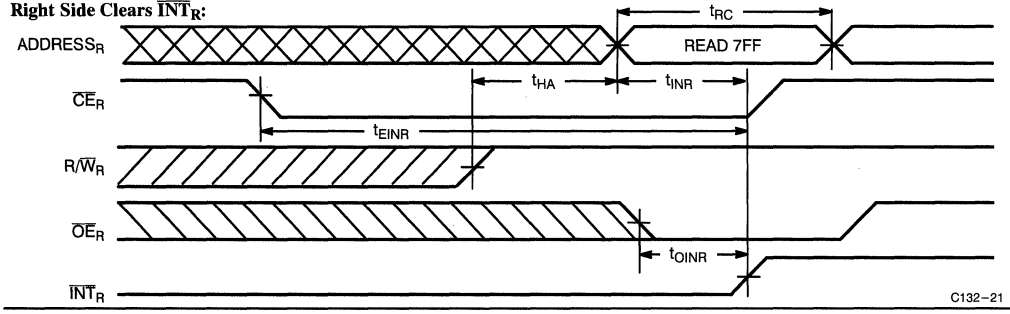


Interrupt Timing Diagrams[18]

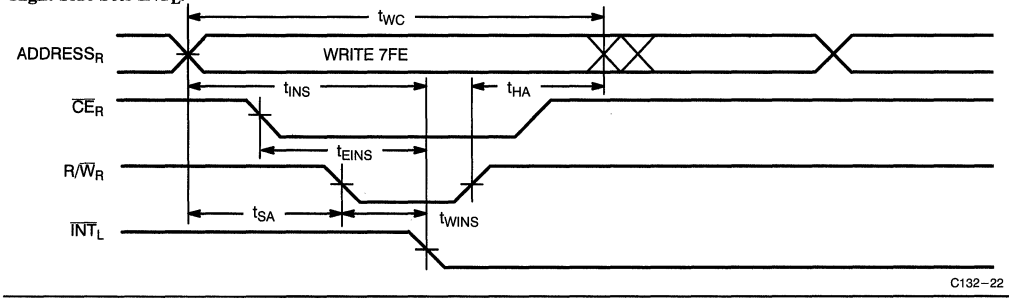
Left Side Sets $\overline{INT}_R$:



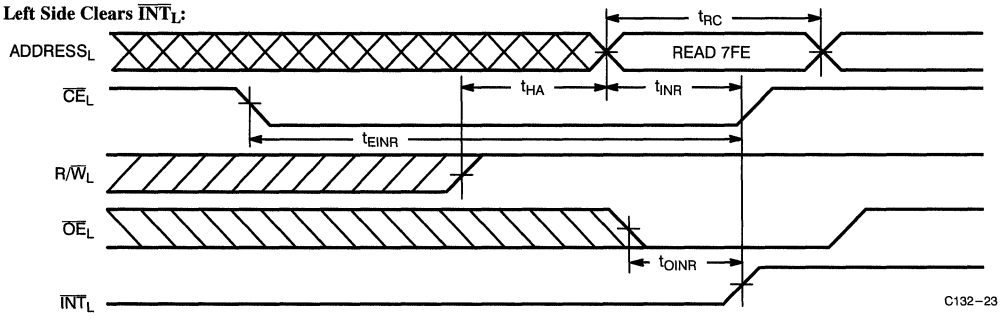
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:

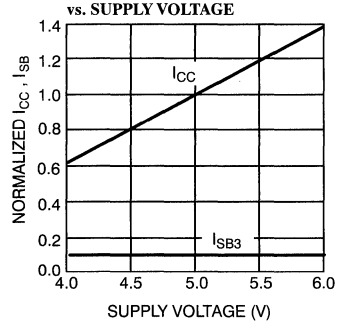


Left Side Clears $\overline{INT}_L$:

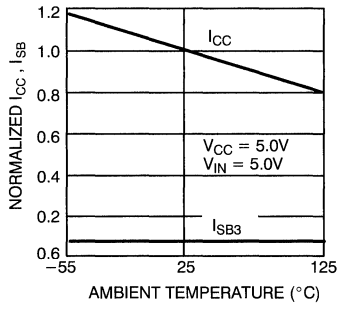


Typical DC and AC Characteristics

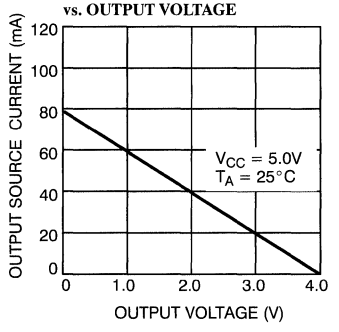
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



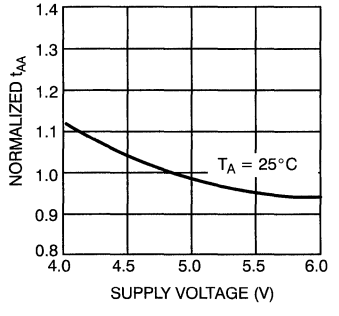
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



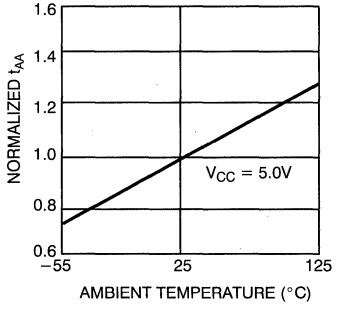
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



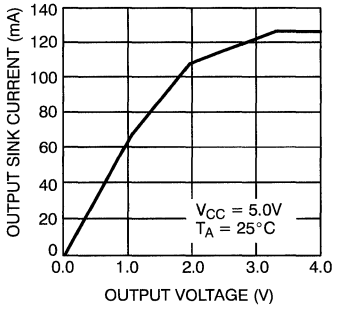
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



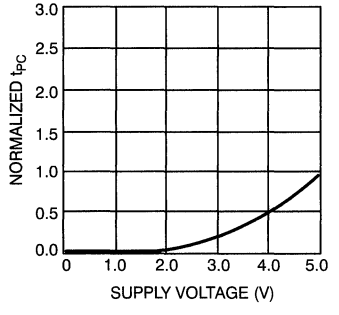
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



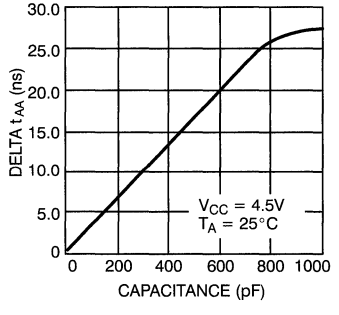
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



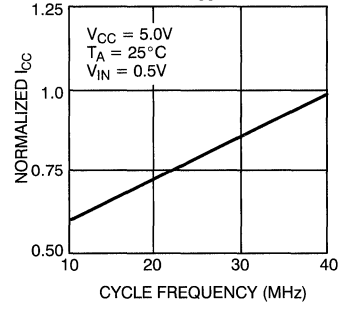
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C132–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C132–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C136–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C136–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–55LMB	L69	52-Square Leadless Chip Carrier	Military

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C142–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C142–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C146–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C146–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C146–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–55LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
24. CY7C142/CY7C146 only.

Document #: 38-00061-J

CY7C133
CY7C143

2K x 16 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed access: 25 ns**
- **Low operating power: I_{CC} = 170 mA (typ.)**
- **Automatic power-down**
- **TTL compatible**
- **Fully asynchronous operation**
- **Master CY7C133 easily expands data bus width to 32 or more bits using slave CY7C143**
- **$\overline{BUSY}$ output flag on CY7C133; $\overline{BUSY}$ input on CY7C143**
- **Available in 68-pin PLCC**
- **Pin compatible and functionally equivalent to IDT7133 and IDT7143**

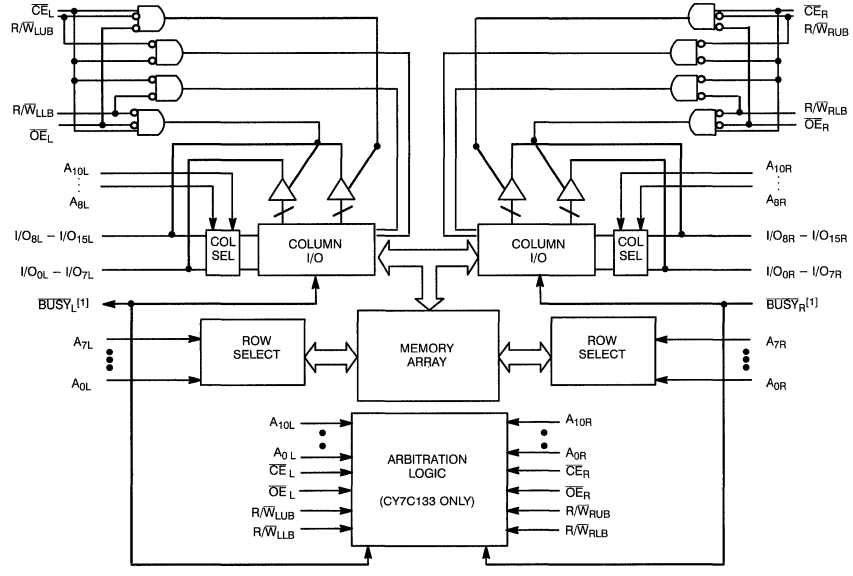
Functional Description

The CY7C133 and CY7C143 are high-speed CMOS 2K by 16 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C133 can be utilized as either a standalone 16-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C143 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($R/\overline{W}_{UB}$, $R/\overline{W}_{LB}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C133 and CY7C143 are available in 68-pin PLCC.

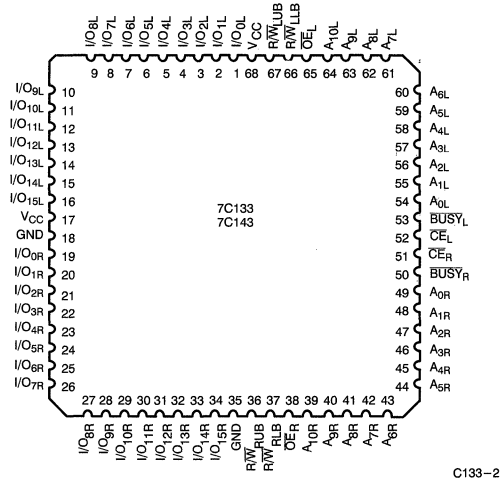
Logic Block Diagram



Note:
1. CY7C133 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C143 (Slave): $\overline{BUSY}$ is input.

Pin Configuration

68-Pin LCC/PLCC
Top View



C133–2

Selection Guide

	7C133–25 7C143–25	7C133–35 7C143–35	7C133–55 7C143–55
Maximum Access Time (ns)	25	35	55
Typical Operating Current I_{CC} (mA)	170	160	150
Typical Standby Current for I_{SB1} (mA)	40	30	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

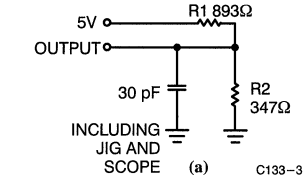
Parameter	Description	Test Conditions		7C133–25 7C143–25 Min.	Typ.	Max.	7C133–35 7C143–35 Min.	Typ.	Max.	7C133–55 7C143–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA				0.4			0.4			0.4	V
		I_{OL} = 16.0 mA[3]				0.5			0.5			0.5	
V_{IH}	Input HIGH Voltage			2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5		+5	−5		+5	−5		+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5		+5	−5		+5	−5		−5	µA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = GND				−200			−200			−200	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[6]	Com'l		170	250		160	230		150	220	mA
			Ind		170	290		160	260		150	250	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		40	60		30	50		20	40	mA
			Ind		40	75		30	65		20	55	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		100	140		85	125		75	110	mA
			Ind		100	160		85	140		75	125	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		3	15		3	15		3	15	mA
			Ind		3	15		3	15		3	15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		90	120		80	105		70	90	mA
			Ind		90	140		80	120		70	105	

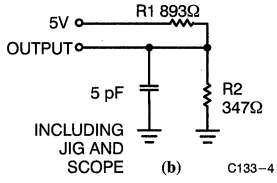
Capacitance[5]

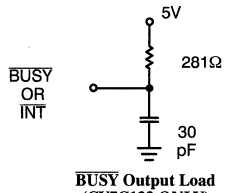
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. $\overline{BUSY}$ pin only.
4. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.

AC Test Loads and Waveforms



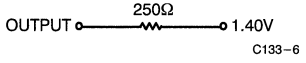




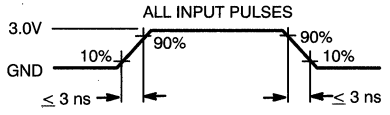
BUSY Output Load (CY7C133 ONLY)

C133-5

Equivalent to: THÉVENIN EQUIVALENT



C133-6



C133-7

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C133-25 7C143-25 Min.	7C133-25 7C143-25 Max.	7C133-35 7C143-35 Min.	7C133-35 7C143-35 Max.	7C133-55 7C143-55 Min.	7C133-55 7C143-55 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		55		ns
t_{AA}	Address to Data Valid[8]		25		35		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[8]		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[8]		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9, 10]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9, 10]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		25	ns
WRITE CYCLE[11]								
t_{WC}	Write Cycle Time	25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		40		ns
t_{AW}	Address Set-Up to Write End	20		25		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[10]		15		20		20	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[10]	0		0		0		ns

Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
8. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{LZCE} is less than t_{HZCE} and t_{LZOE} is less than t_{HZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

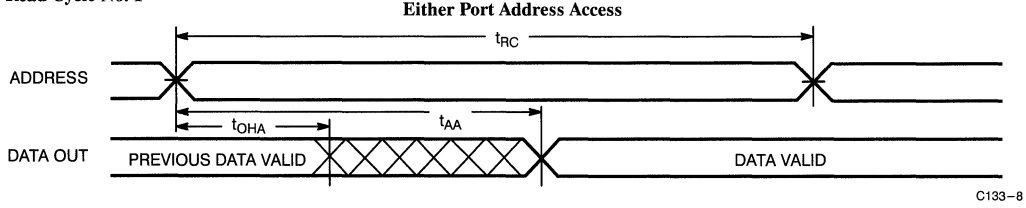
Switching Characteristics Over the Operating Range[2,7] (continued)

Parameter	Description	7C133–25 7C143–25		7C133–35 7C143–35		7C133–55 7C143–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING (For Master CY7C133)								
t_{BLA}	$\overline{BUSY}$ Low from Address Match		25		35		50	ns
t_{BHA}	$\overline{BUSY}$ High from Address Mismatch		20		30		40	ns
t_{BLC}	$\overline{BUSY}$ Low from $\overline{CE}$ Low		20		25		35	ns
t_{BHC}	$\overline{BUSY}$ High from $\overline{CE}$ High		20		20		30	ns
t_{WDD}	Write Pulse to Data Delay[12]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[12]		35		45		55	ns
t_{BDD}	$\overline{BUSY}$ High to Valid Data[13]		Note 13		Note 13		Note 13	ns
t_{PS}	Arbitration Priority Set Up Time[14]	5		5		5		ns
BUSY TIMING (For Slave CY7C143)								
t_{WB}	Write to $\overline{BUSY}$[15]	0		0		0		ns
t_{WH}	Write Hold After $\overline{BUSY}$[16]	20		25		30		ns
t_{WDD}	Write Pulse to Data Delay[17]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[17]		35		45		55	ns

6

Switching Waveforms

Read Cycle No. 1[18, 19]

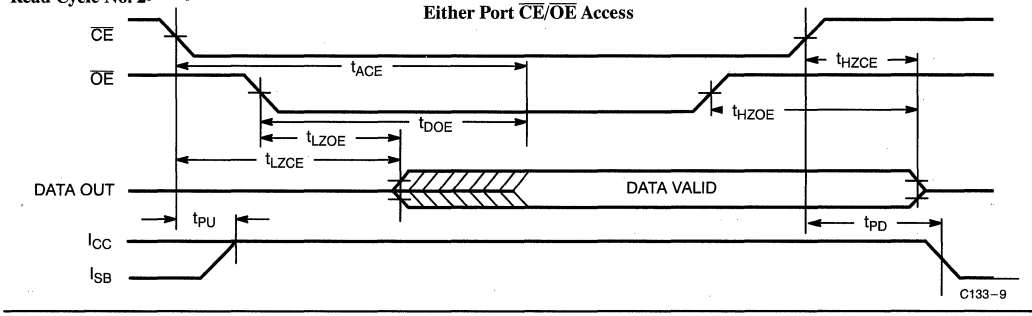


Notes:

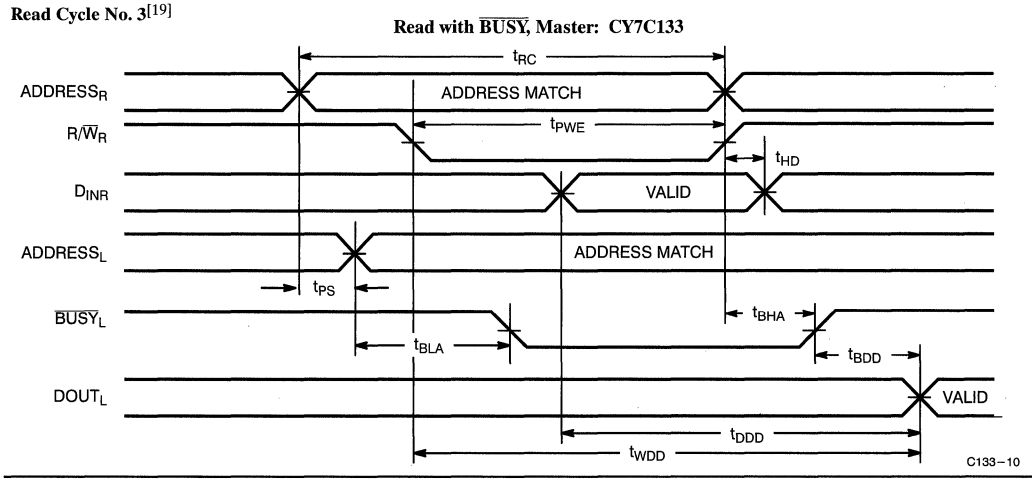
12. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with $\overline{BUSY}$, Master: CY7C133."
13. t_{BDD} is a calculated parameter and is greater of 0, $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).
14. To ensure that the earlier of the two ports wins.
15. To ensure that write cycle is inhibited during contention.
16. To ensure that a write cycle is completed after contention.
17. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with Port-to-port Delay."
18. R/$\overline{W}$ is HIGH for read cycle
19. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.

Switching Waveforms (continued)

Read Cycle No. 2[18,20]



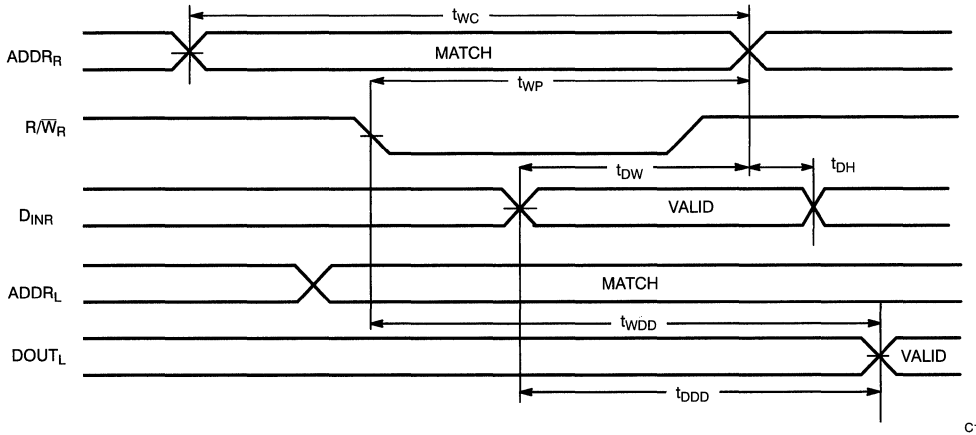
Read Cycle No. 3[19]



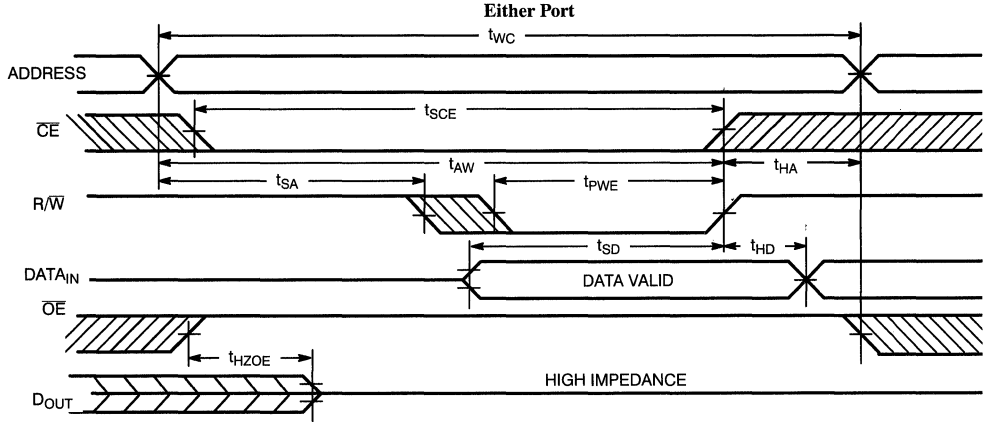
Notes:
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Timing Waveform of Read with Port-to-port Delay No. 4 (For Slave CY7C143)[21,22,23]



Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port)[14,24]

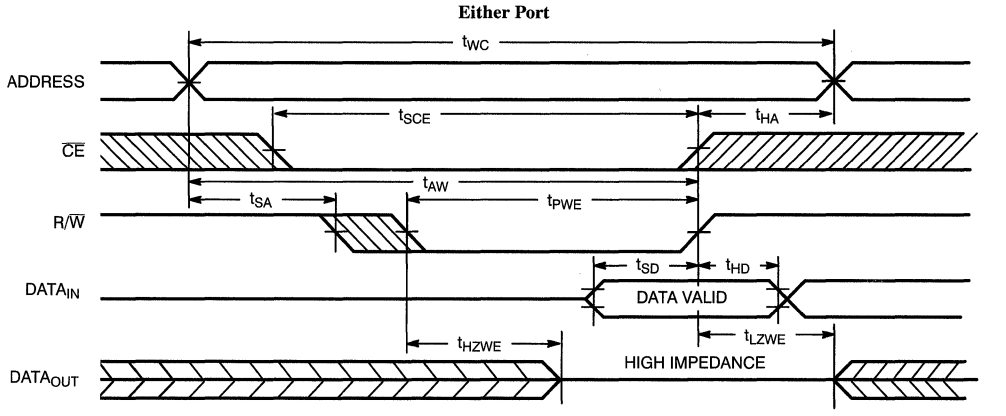


Notes:

21. Assume $\overline{BUSY}$ input at V_{IH} for the writing port and at V_{IL} for the reading port.
22. Write cycle parameters should be adhered to inorder to ensure proper writing.
23. Device is continuously enabled for both ports.
24. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

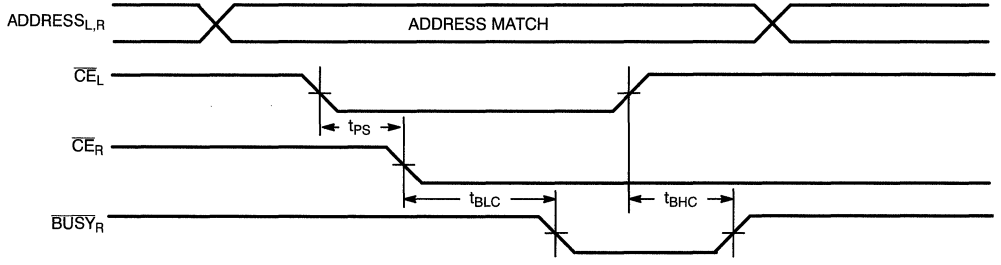
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[20,25]

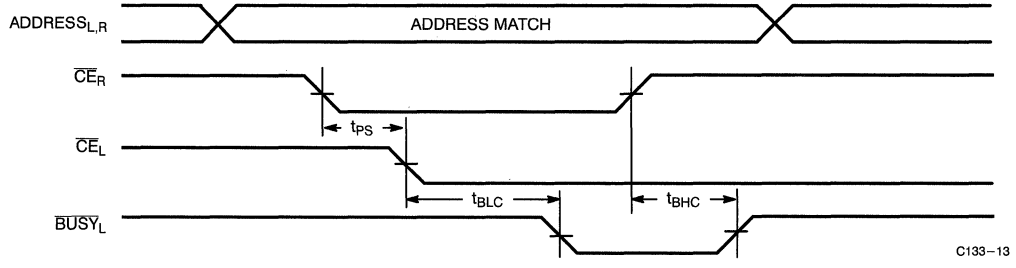


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:

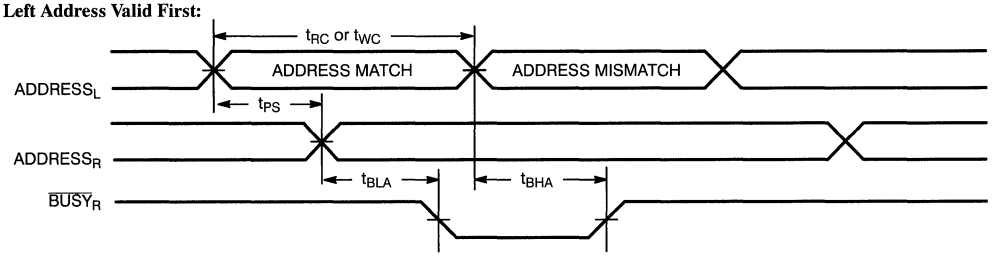


Note:
25. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

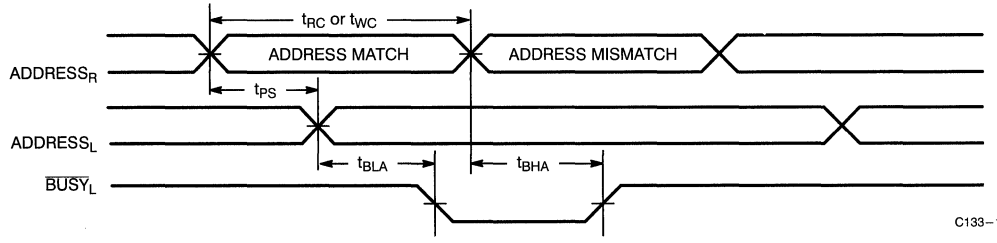
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



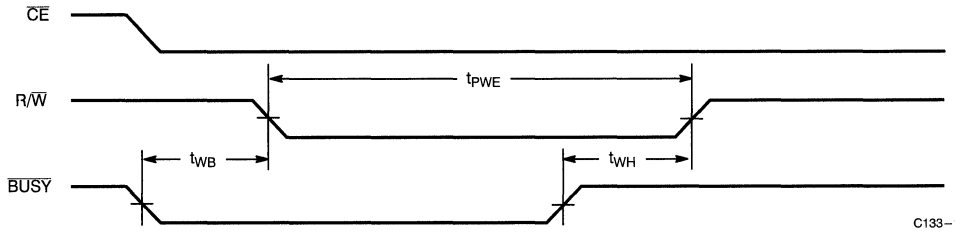
Right Address Valid First:



C133–15

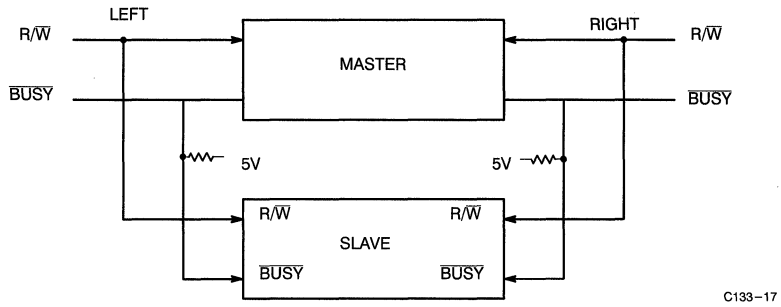
Busy Timing Diagram No. 3

Write with $\overline{BUSY}$ (Slave: CY7C143)



C133–16

32-Bit Master/Slave Dual-Port Memory Systems



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C133-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C133-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C133-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C143-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C143-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C143-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[26]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
26. CY7C143 only.

Document #: 38−00414

CY7B134
CY7B135
CY7B1342

4K x 8 Dual-Port Static RAMs and 4K x 8 Dual-Port Static RAM with Semaphores

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **7B1342 includes semaphores**
- **7B134 available in 48-pin DIP**
- **7B135/7B1342 available in 52-pin LCC/PLCC**

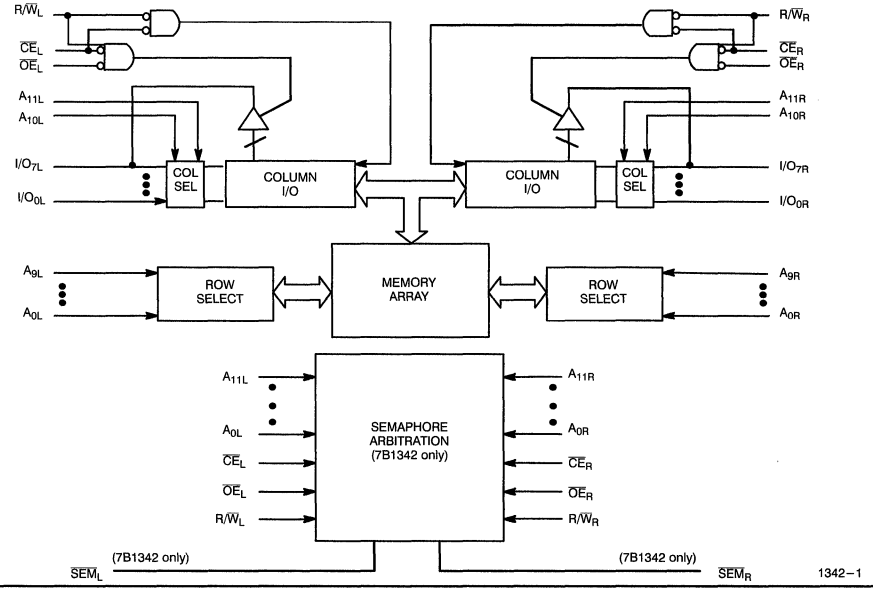
Functional Description

The CY7B134, CY7B135, and CY7B1342 are high-speed BiCMOS 4K x 8 dual-port static RAMs. The CY7B1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). The CY7B134/135 are suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7B1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin (CY7B1342 only).

The CY7B134 is available in 48-pin DIP. The CY7B135 and CY7B1342 are available in 52-pin LCC/PLCC.

Logic Block Diagram

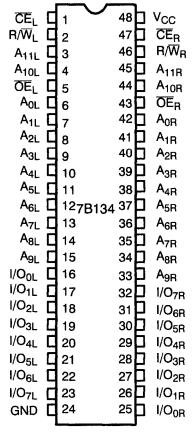


Selection Guide

		7B135–15 7B1342–15	7B134–20 7B135–20 7B1342–20	7B134–25 7B135–25 7B1342–25	7B134–35 7B135–35 7B1342–35	7B134–55 7B135–55 7B1342–55
Maximum Access Time (ns)		15	20	25	35	55
Maximum Operating Current (mA)	Commercial	260	240	220	210	210
	Military			260	250	250
Maximum Standby Current (mA)	Commercial	110	100	95	90	90
	Military			100	95	95

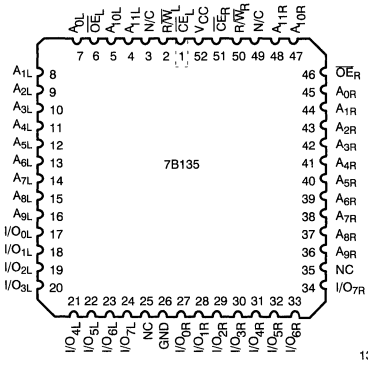
Pin Configurations

DIP
Top View



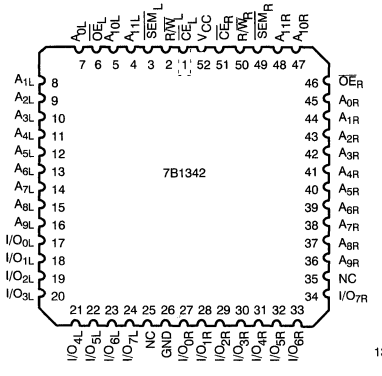
1342-2

LCC/PLCC
Top View



1342-3

LCC/PLCC
Top View



1342-4

Pin Definitions

Left Port	Right Port	Description
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$ (CY7B1342 only)	$\overline{SEM}_R$ (CY7B1342 only)	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −3.0V to +7.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B135−15 7B1342−15 Min.	7B135−15 7B1342−15 Max.	7B134−20 7B135−20 7B1342−20 Min.	7B134−20 7B135−20 7B1342−20 Max.	7B134−25 7B135−25 7B1342−25 Min.	7B134−25 7B135−25 7B1342−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, $GND \leq V_O \leq V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		260		240		220	mA
			Mil/Ind						260	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[4]	Com'l		110		100		95	mA
			Mil/Ind						100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[4]	Com'l		165		155		145	mA
			Mil/Ind						170	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R \geq$ V_{CC} − 0.2V, $V_{IN} \geq V_{CC}$ − 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4]	Com'l		15		15		15	mA
			Mil/Ind						30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq$ V_{CC} − 0.2V, $V_{IN} \geq V_{CC}$ − 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		160		150		140	mA
			Mil/Ind						160	

Notes:

1. Pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

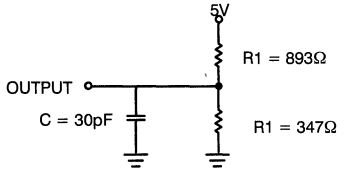
Electrical Characteristics Over the Operating Range[3](continued)

Parameter	Description	Test Conditions		7B134–35 7B135–35 7B1342–35 Min.	7B134–35 7B135–35 7B1342–35 Max.	7B134–55 7B135–55 7B1342–55 Min.	7B134–55 7B135–55 7B1342–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, $GND \leq V_O \leq V_{CC}$		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[4]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[4]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0[4]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs, f = f_{MAX}[4]	Com'l		130		130	mA
			Mil/Ind		140		140	

Capacitance[5]

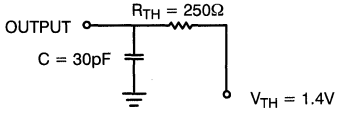
Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



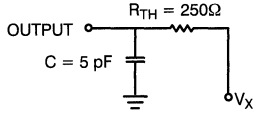
(a) Normal Load (Load 1)

1342–5



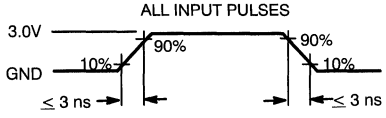
(b) Thévenin Equivalent (Load 1)

1342–6



(c) Three-State Delay (Load 3)

1342–7



1342–8

Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. For all packages except DIP and cerDIP (D26, P25), which have maximums of C_{IN} = 15 pF, C_{OUT} = 15 pF.

Switching Characteristics Over the Operating Range[7, 8]

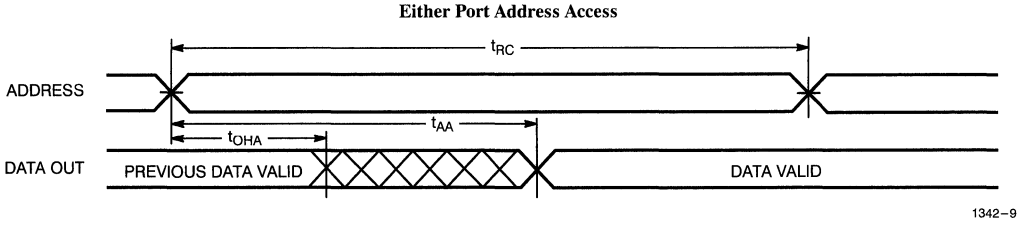
Parameter	Description	7B135–15 7B1342–15		7B134–20 7B135–20 7B1342–20		7B134–25 7B135–25 7B1342–25		7B134–35 7B135–35 7B1342–35		7B134–55 7B135–55 7B1342–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		55		ns
t_{AA}	Address to Data Valid		15		20		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		15		20		25	ns
t_{LZOE}[9, 10]	$\overline{OE}$ Low to Low Z	3		3		3		3		3		ns
t_{HZOE}[9, 10]	$\overline{OE}$ HIGH to High Z		10		13		15		20		25	ns
t_{LZCE}[9, 10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZCE}[9, 10]	$\overline{CE}$ HIGH to High Z		10		13		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		25		35		55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	15		20		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		30		50		ns
t_{AW}	Address Set-Up to Write End	12		15		20		30		50		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		15		20		25		50		ns
t_{SD}	Data Set-Up to Write End	10		13		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z		10		13		15		20		25	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		3		ns
t_{WDD}[11]	Write Pulse to Data Delay		30		40		50		60		70	ns
t_{DDD}[11]	Write Data Valid to Read Data Valid		25		30		30		35		40	ns
SEMAPHORE TIMING[12]												
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		15		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		5		ns

Notes:

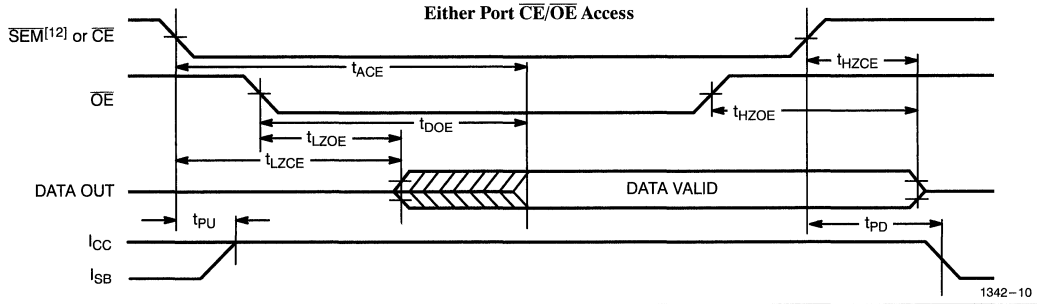
7. See the last page of this specification for Group A subgroup testing information.
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
12. Semaphore timing applies only to CY7B1342.

Switching Waveforms

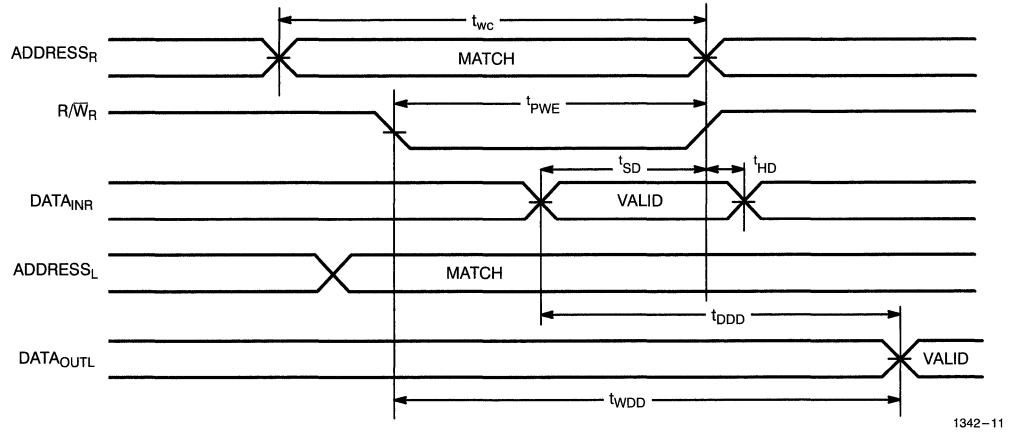
Read Cycle No. 1[13, 14]



Read Cycle No. 2[13, 15]



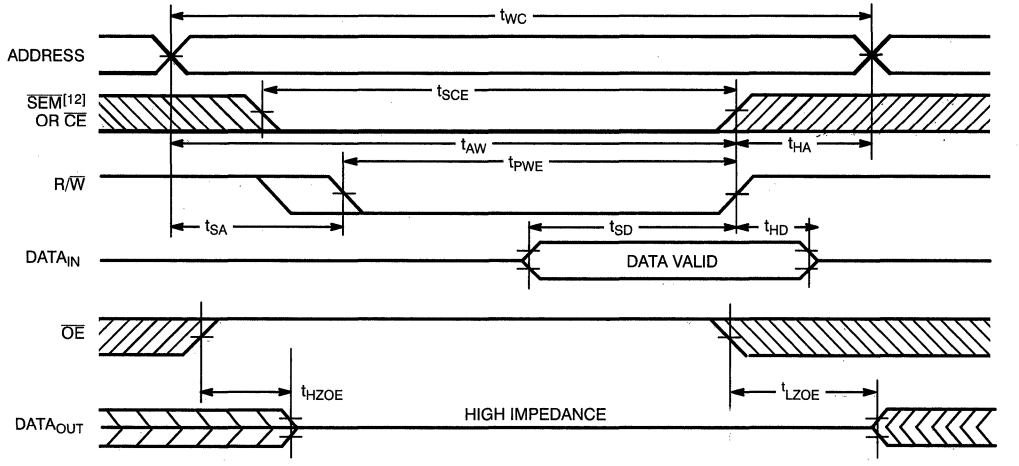
Read Timing with Port-to-Port Delay[16]



Notes:
13. R/$\overline{W}$ is HIGH for read cycle.
14. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. $\overline{CE}_L$ = $\overline{CE}_R$ =LOW; R/$\overline{W}_L$ = HIGH

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[17, 18, 19]

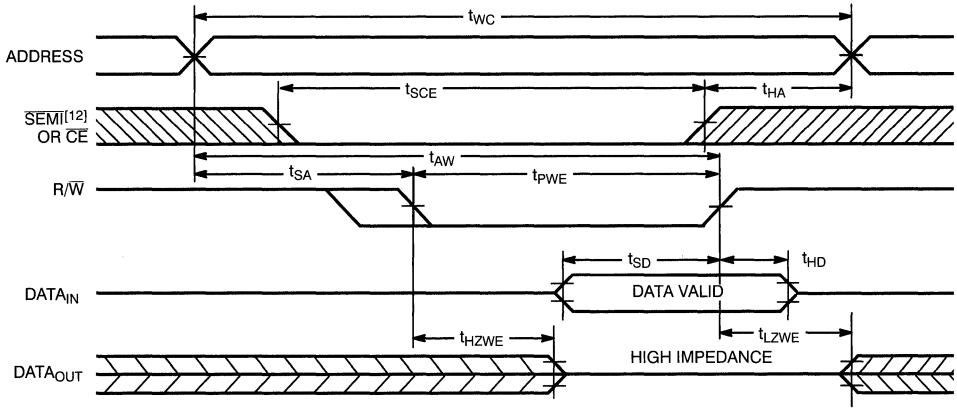


Notes:

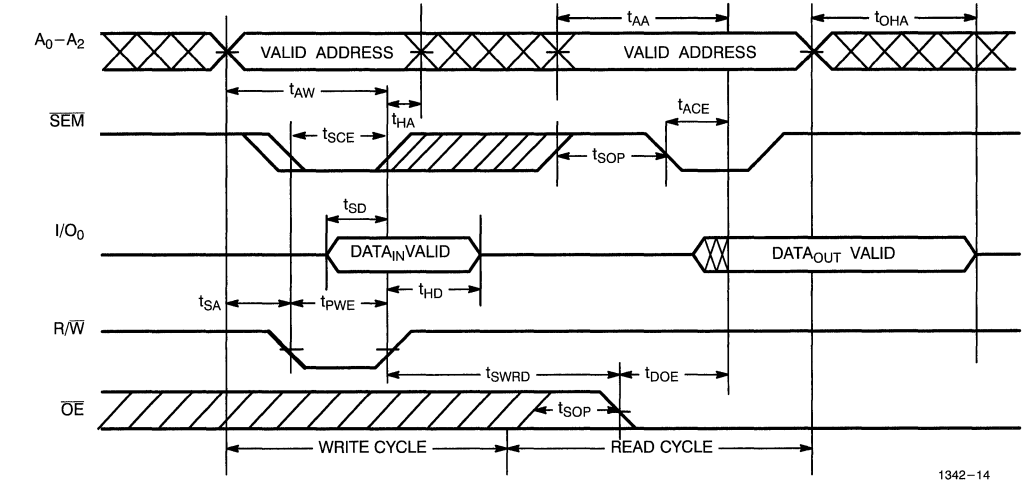
17. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. R/$\overline{W}$ must be HIGH during all address transactions.
19. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.

Switching Waveforms (continued)

Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[18, 20]



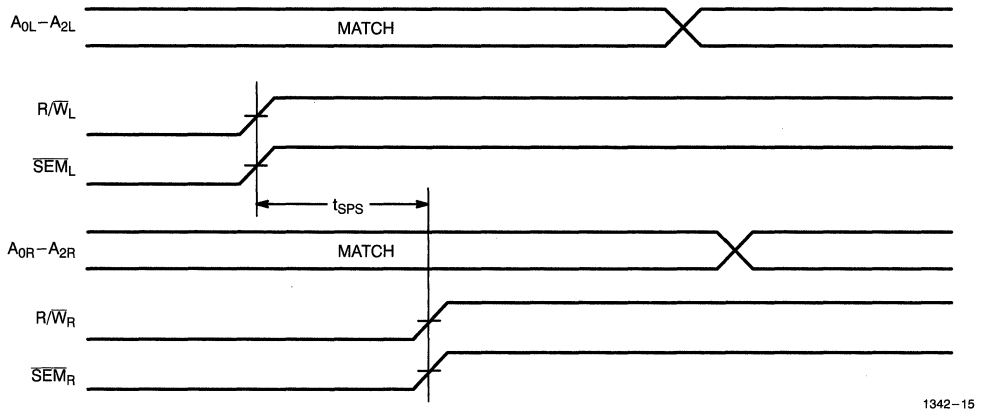
Semaphore Read After Write Timing, Either Side (CY7B1342 only)[21]



Notes:
20. Data I/O pins enter high-impedance when $\overline{OE}$ is held LOW during write.
21. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

Switching Waveforms (continued)

Timing Diagram of Semaphore Contention (CY7B1342 only)[22, 23, 24]



Notes:
22. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
23. Semaphores are reset (available to both ports) at cycle start.
24. If t_{SPS} is violated, it is guaranteed that only one side will gain access to the semaphore.

Architecture

The CY7B134 and CY7B135 consist of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). Two semaphore control pins exist for the CY7B1342 ($\overline{SEM}_{L/R}$).

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. Since there is no on-chip arbitration, the user must be sure that a specific location will not be accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 timing diagram) or the R/$\overline{W}$ pin (see Write Cycle No. 2 timing diagram). Data can be written t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for write operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B1342 wishes to access a semaphore, the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin. Required inputs for read operations are summarized in *Table 1*.

Semaphore Operation

The CY7B1342 provides eight semaphore latches which are separate from the dual port memory locations. Semaphores are used to reserve resources which are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches. $\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW. A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing a zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore. *Table 2* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports request a semaphore control by writing a 0 to a semaphore within t_{SPS} of each other, it is guaranteed that only one side will gain access to the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

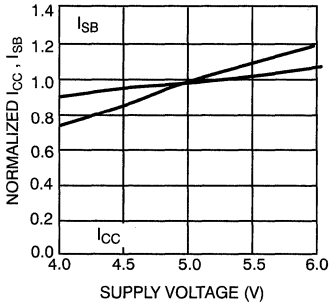
Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 - I/O_7$	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read $Data_{IN}$ Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Semaphore Operation Example

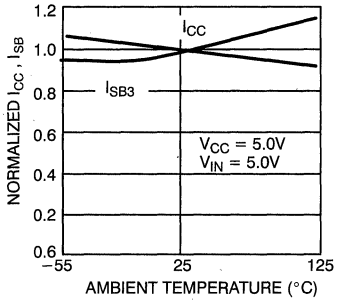
Function	I/O_0 Left	I/O_0 Right	Status
No Action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to Semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

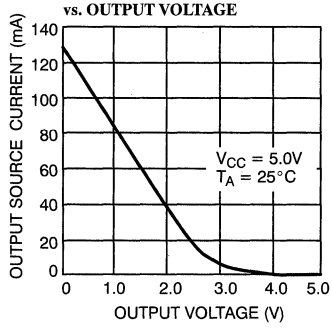
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



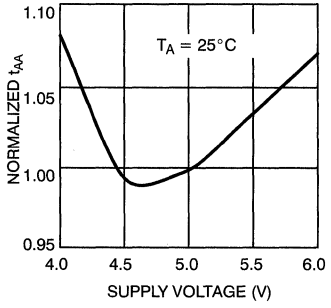
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



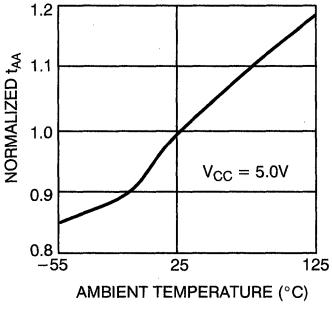
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



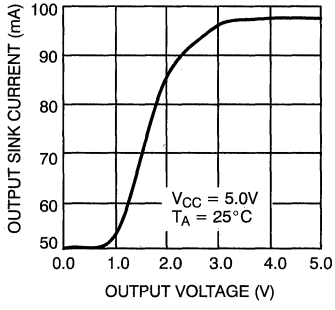
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



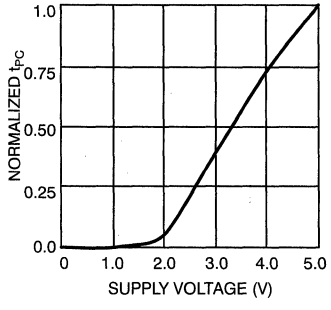
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



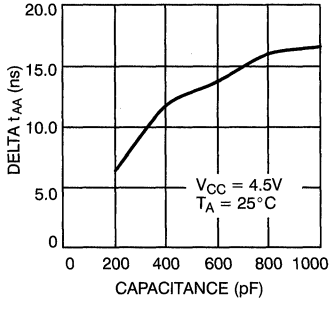
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



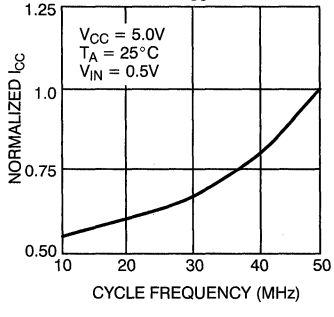
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7B134–20PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
25	CY7B134–25PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–25PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134–25DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
35	CY7B134–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7B134–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B135–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B135–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B135–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135–25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B135–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135–35LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7B135–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7B1342–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B1342–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B1342–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342–25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B1342–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342–35LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7B1342–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
SEMAPHORE CYCLE	
t_{SOD}	7, 8, 9, 10, 11
t_{SWRD}	7, 8, 9, 10, 11
t_{SPS}	7, 8, 9, 10, 11

Document #: 38−00161−D

CY7B138
CY7B139

4K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (com'l)**
  - **— 25 ns (mil)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master /Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC/PGA**
- **TTL compatible**

Functional Description

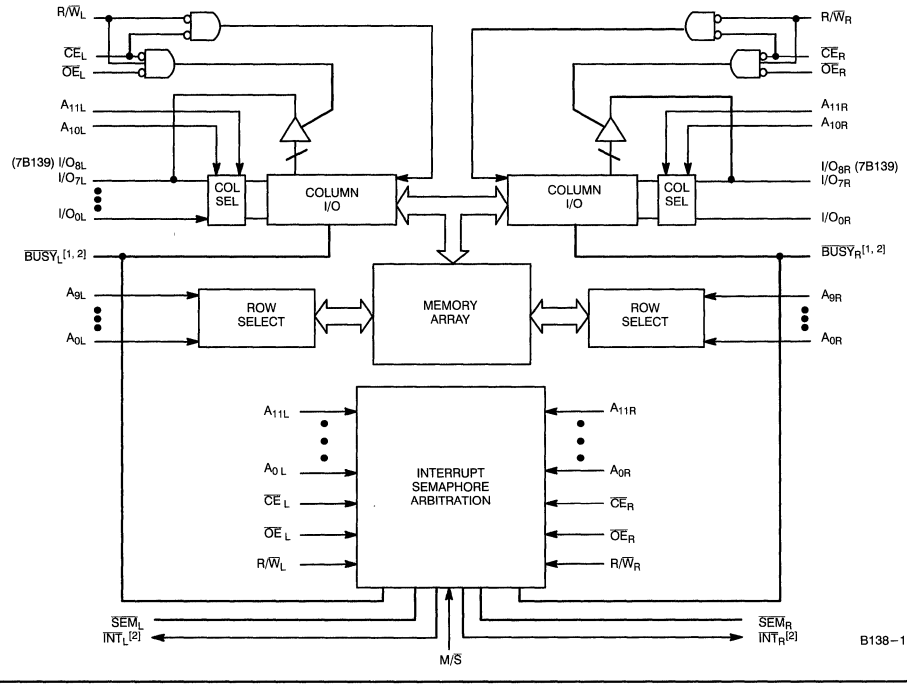
The CY7B138 and CY7B139 are high-speed BiCMOS 4K x 8 and 4K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B138/9 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B138/9 can be utilized as a stand-alone 32-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B138 and CY7B139 are available in 68-pin LCCs, and PLCCs.

6

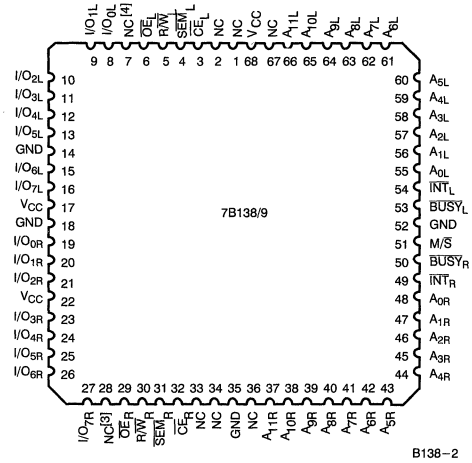
Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

Pin Configuration

68-Pin LCC/PLCC
Top View



B138–2

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location FFE and is cleared when left port reads location FFE. $\overline{INT}_R$ is set when left port writes location FFF and is cleared when right port reads location FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B138–15 7B139–15	7B138–25 7B139–25	7B138–35 7B139–35	7B138–55 7B139–55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military/Industrial		280	250	250
Maximum Standby Current for I_{SB1}(mA)	Commercial	110	95	90	90
	Military/Industrial		100	95	95

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[3] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7B138−15 7B139−15 Min.	7B138−15 7B139−15 Max.	7B138−25 7B139−25 Min.	7B138−25 7B139−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		260		220	mA
			Mil/Ind				280	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		110		95	mA
			Mil/Ind				100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		165		145	mA
			Mil/Ind				180	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[6]	Com'l		15		15	mA
			Mil/Ind				30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[6]	Com'l		160		140	mA
			Mil/Ind				160	

Notes:

3. Pulse width < 20 ns.
4. T_A is the "instant on" case temperature.
5. See the last page of this specification for Group A subgroup testing information.
6. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

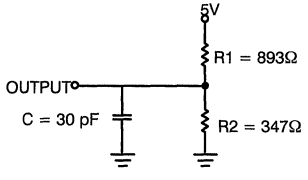
Electrical Characteristics Over the Operating Range[5] (continued)

Parameter	Description	Test Conditions		7B138–35 7B139–35 Min.	7B138–35 7B139–35 Max.	7B138–55 7B139–55 Min.	7B138–55 7B139–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[6]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[6]	Com'l		130		130	mA
			Mil/Ind		140		140	

Capacitance[7]

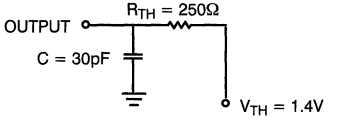
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

AC Test Loads and Waveforms



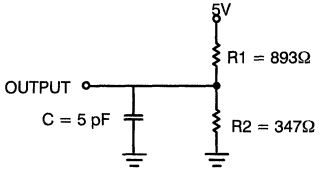
(a) Normal Load (Load 1)

B138–3



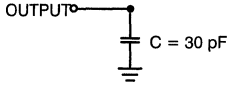
(b) Thévenin Equivalent (Load 1)

B138–4



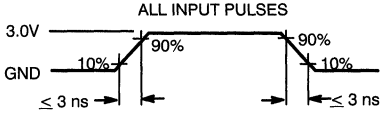
(c) Three-State Delay (Load 3)

B138–5



Load (Load 2)

B138–6



B138–7

Note:
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5, 8]

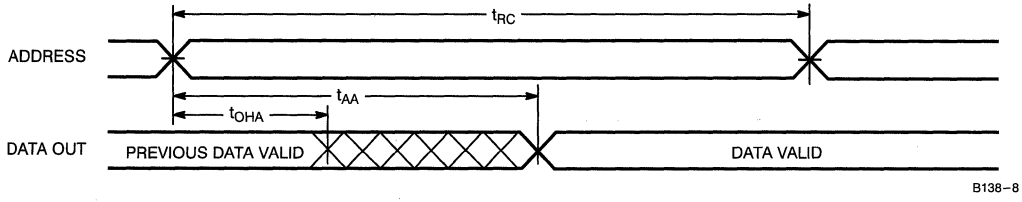
Parameter	Description	7B138–15 7B139–15 Min.	7B138–15 7B139–15 Max.	7B138–25 7B139–25 Min.	7B138–25 7B139–25 Max.	7B138–35 7B139–35 Min.	7B138–35 7B139–35 Max.	7B138–55 7B139–55 Min.	7B138–55 7B139–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		25	ns
t_{LZOE}[9, 10]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[9, 10]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[9, 10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[9, 10]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		40		ns
t_{AW}	Address Set-Up to Write End	12		20		30		40		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		15		15		20		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[11]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[11]	Write Data Valid to Read Data Valid		25		30		35		40	ns
BUSY TIMING[12]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		40	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		40	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		35	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		40		ns
t_{BDD}[13]	$\overline{BUSY}$ HIGH to Data Valid		Note 13		Note 13		Note 13		Note 13	ns
INTERRUPT TIMING[12]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

Notes:

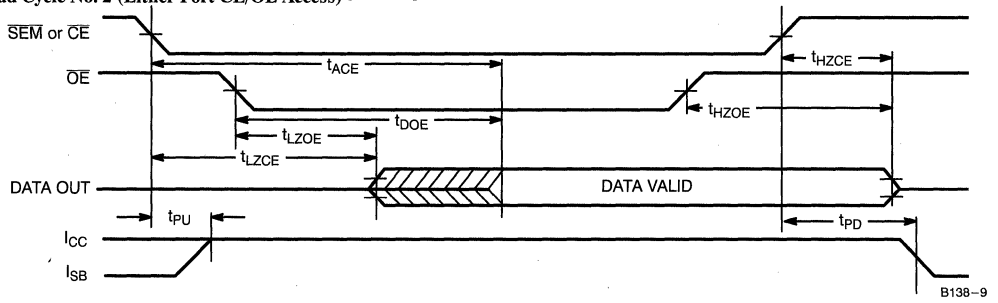
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
12. Test conditions used are Load 2.
13. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Switching Waveforms

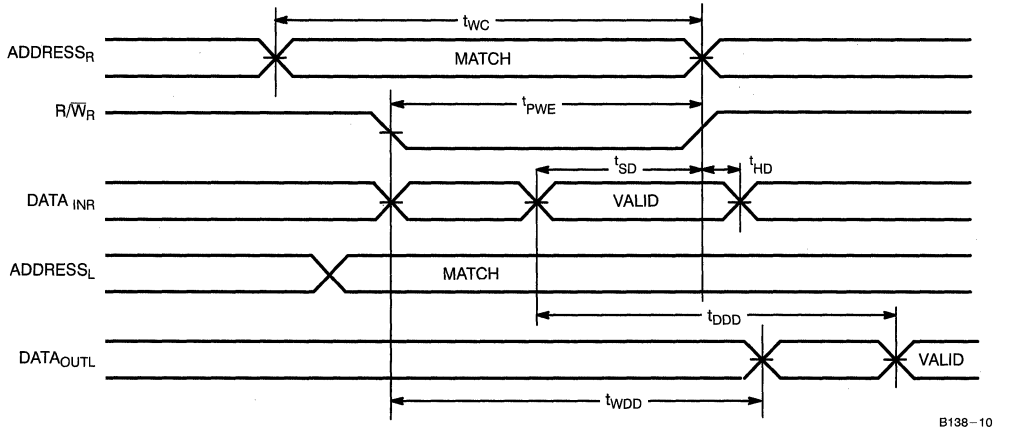
Read Cycle No. 1 (Either Port Address Access)[14, 15]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access) [14, 16, 17]



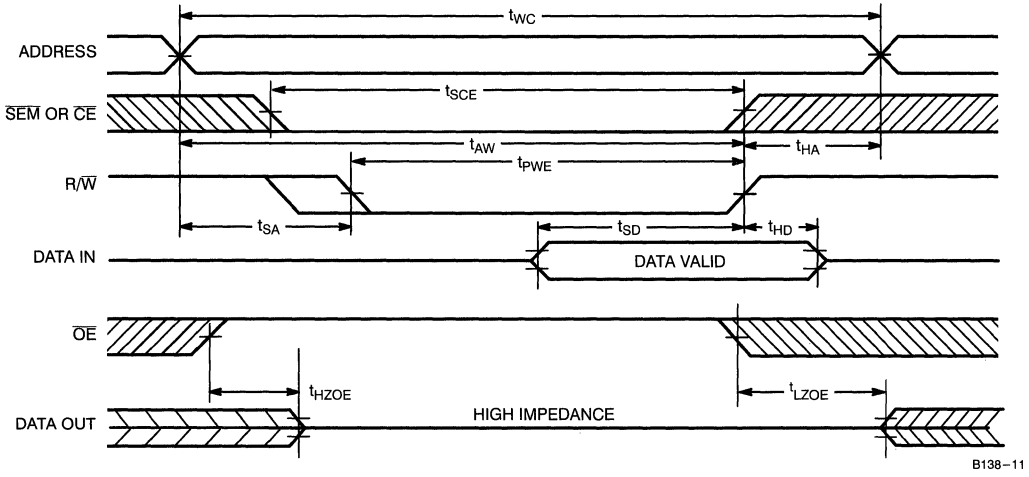
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[18, 19]



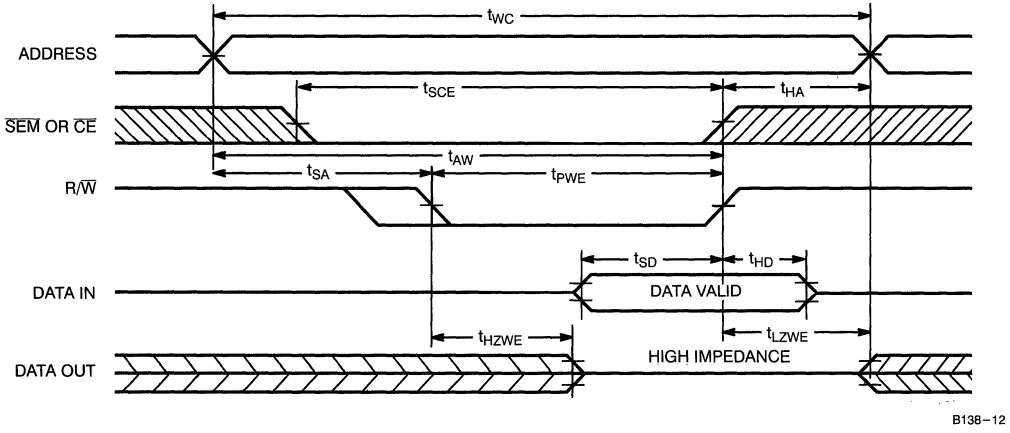
Notes:
14. R/$\overline{W}$ is HIGH for read cycle.
15. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
17. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
18. $\overline{BUSY}$ = HIGH for the writing port.
19. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[20, 21, 22]



Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[20, 22, 23]

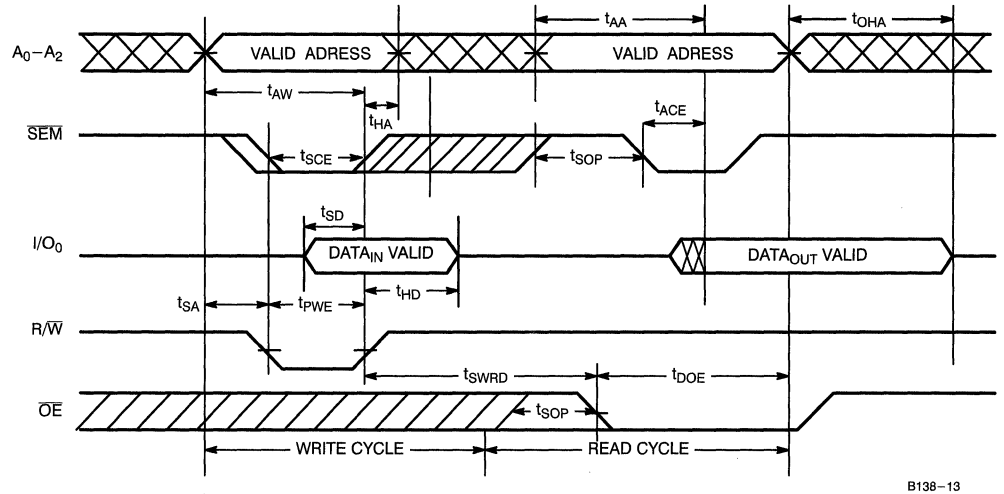


Notes:

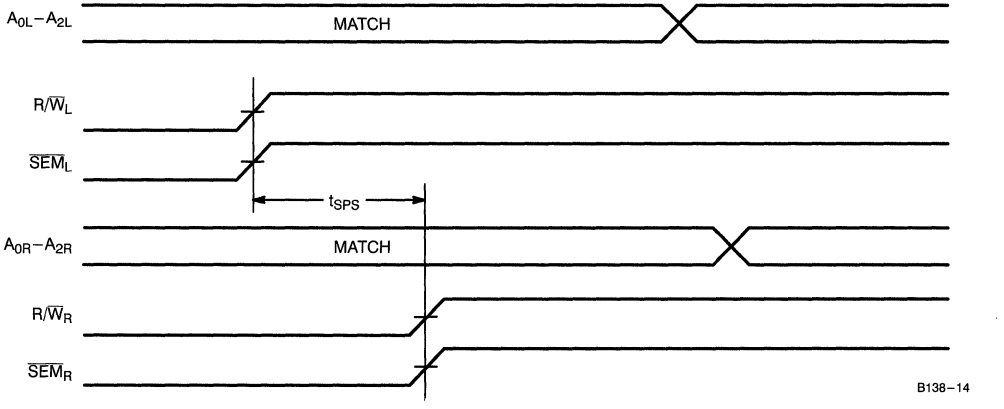
20. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
21. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
22. R/$\overline{W}$ must be HIGH during all address transitions.
23. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[24]



Timing Diagram of Semaphore Contention[25, 26, 27]

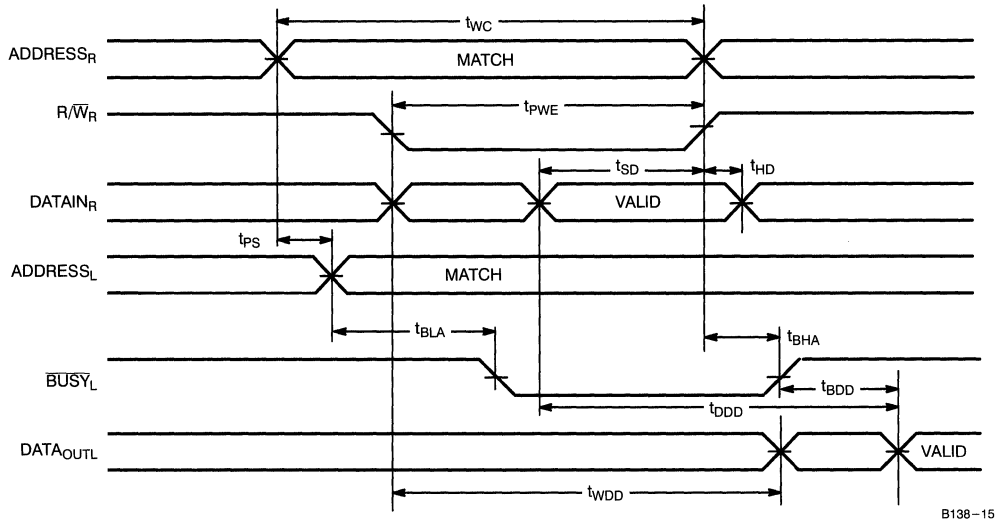


Notes:

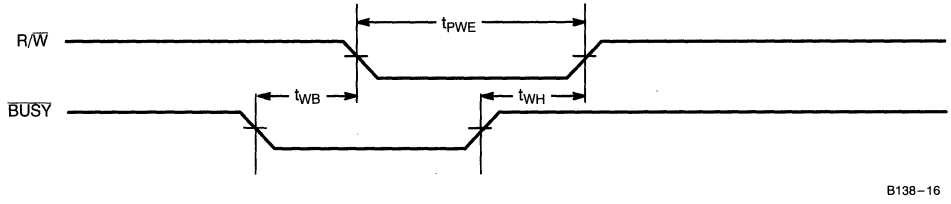
24. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
25. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
26. Semaphores are reset (available to both ports) at cycle start.
27. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[19]



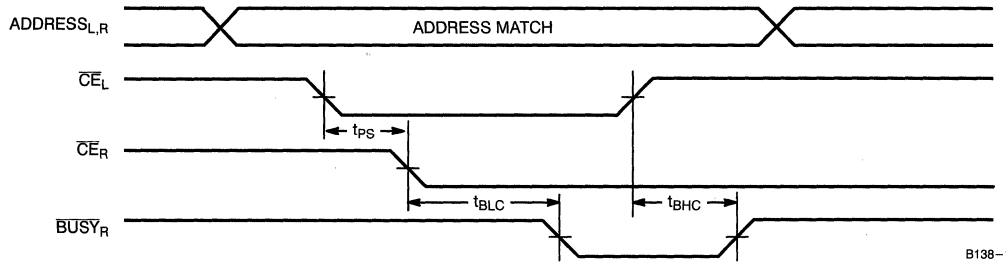
Write Timing with Busy Input (M/$\overline{S}$=LOW)



Switching Waveforms (continued)

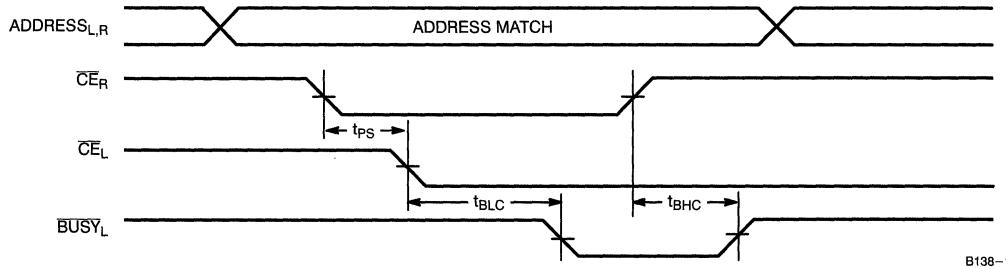
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[28]

$\overline{CE}_L$ Valid First:



B138–17

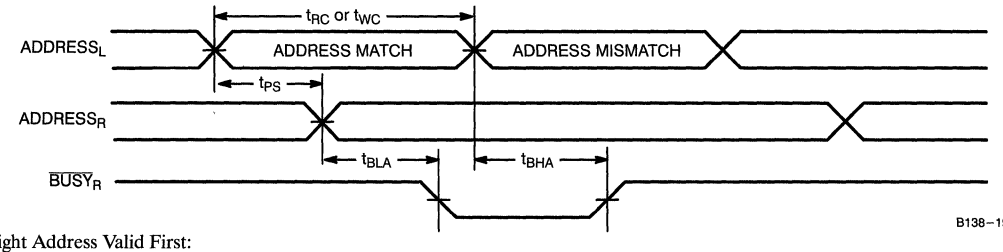
$\overline{CE}_R$ Valid First:



B138–18

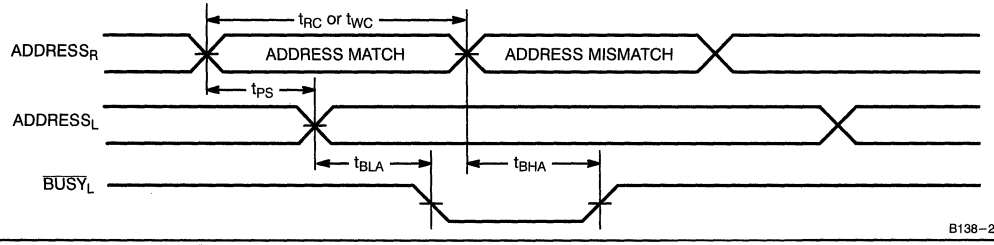
Busy Timing Diagram No. 2 (Address Arbitration)[28]

Left Address Valid First:



B138–19

Right Address Valid First:



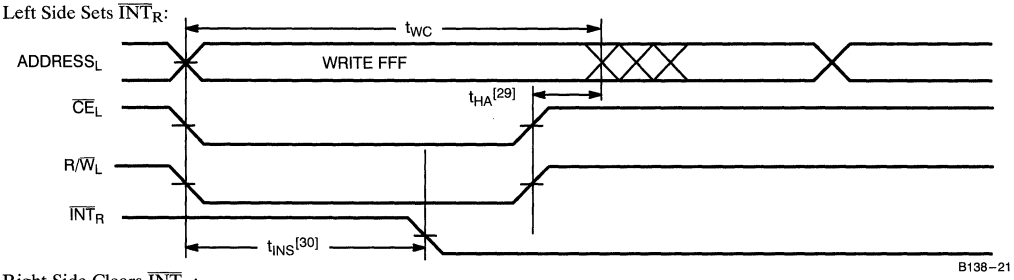
B138–20

Note:
28. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

Switching Waveforms (continued)

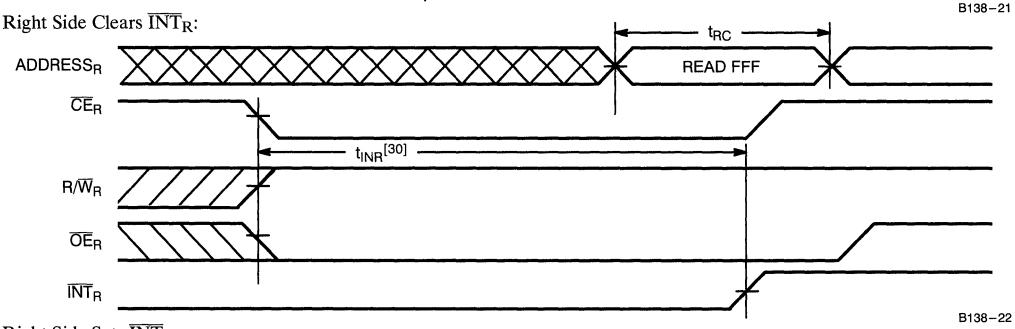
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$:



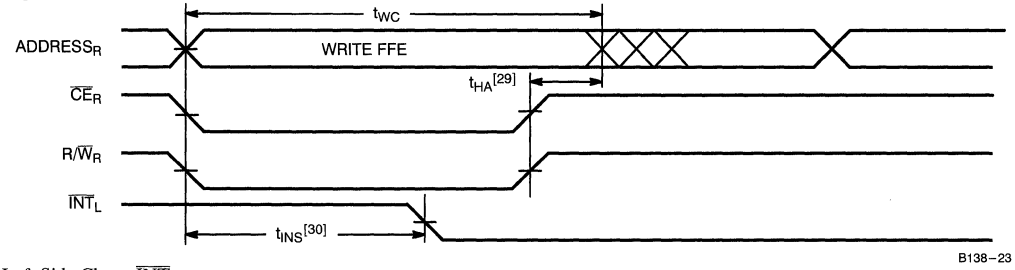
B138-21

Right Side Clears $\overline{INT}_R$:



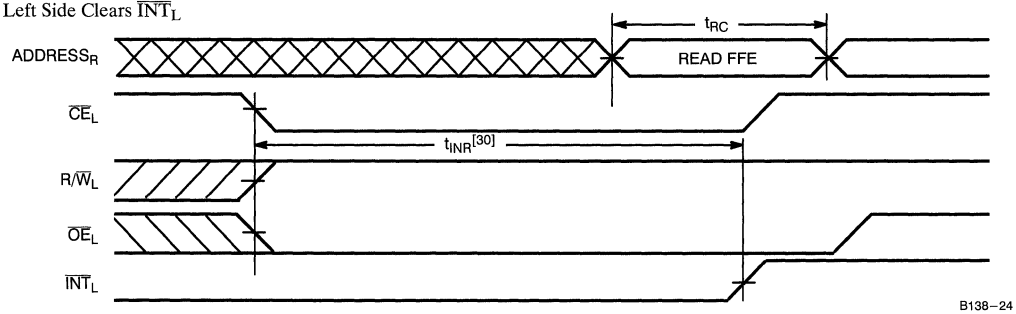
B138-22

Right Side Sets $\overline{INT}_L$:



B138-23

Left Side Clears $\overline{INT}_L$



B138-24

Notes:

29. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
30. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7B138/9 consists of an array of 4K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B138/9 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B138/9 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user of the CY7B138/9 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location FFF, the right port's interrupt flag ($\overline{INT}_R$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT}_L$) is accomplished when the right port writes to location FFE. This flag is cleared when the left port reads location FFE. The message at FFF or FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT}_R$ and $\overline{INT}_L$ are push-pull outputs and do not require pull-up resistors to operate. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B138/9 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented as a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B138/9 provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the a semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into themn at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

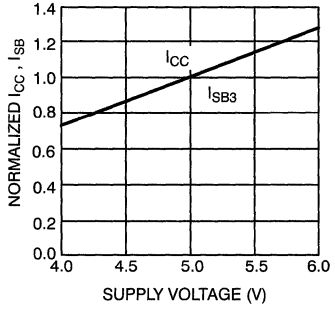
	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-11}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-11}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	FFE	X
Reset Left $\overline{INT}$	X	L	L	FFE	H	X	X	X	X	X
Set Right $\overline{INT}$	L	L	X	FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	FFF	H

Table 3. Semaphore Operation Example

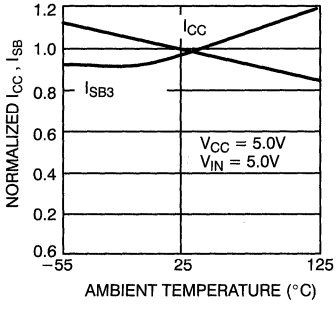
Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

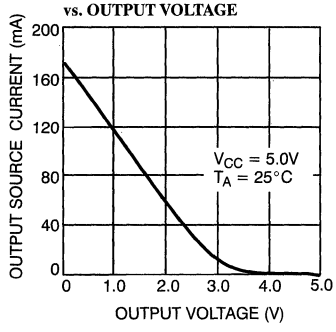
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



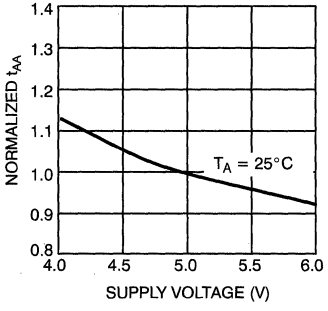
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



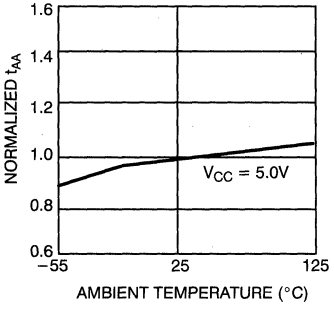
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



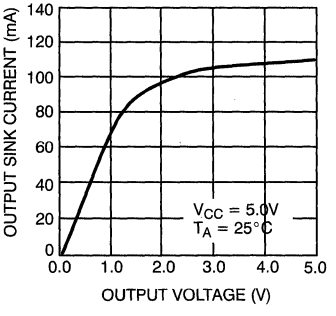
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



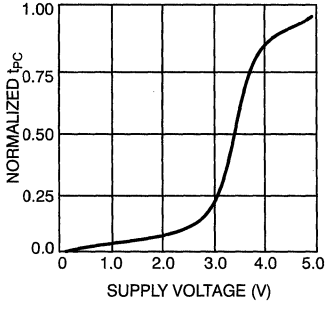
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



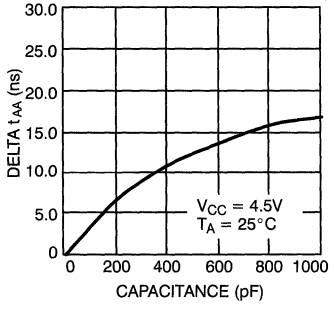
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



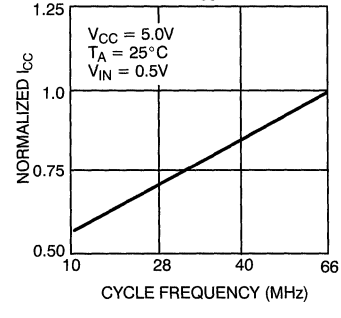
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B138–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B138–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B138–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B138–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B138–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B138–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B138–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B138–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B138–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7B139–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B139–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B139–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B139–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B139–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B139–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B139–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B139–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B139–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38−00162−G

CY7B144
CY7B145

8K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC, 64-pin and 80-pin TQFP**
- **TTL compatible**
- **Pin compatible and functionally equivalent to IDT7005 and IDT7015**

Functional Description

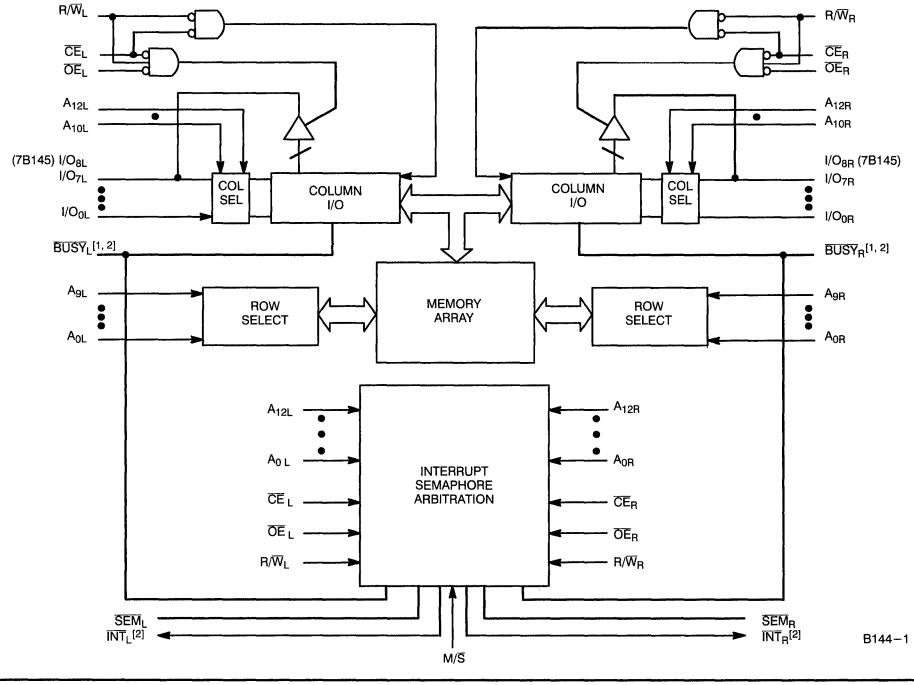
The CY7B144 and CY7B145 are high-speed BiCMOS 8K x 8 and 8K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B144/5 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B144/5 can be utilized as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B144 and CY7B145 are available in 68-pin LCCs, PLCCs, 64-pin (CY7B144) and 80-pin TQFP (CY7B145).

6

Logic Block Diagram

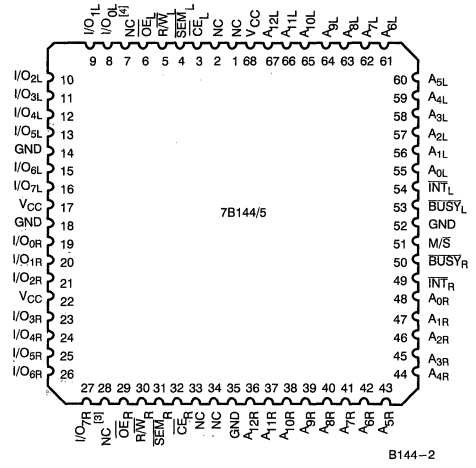


Notes:

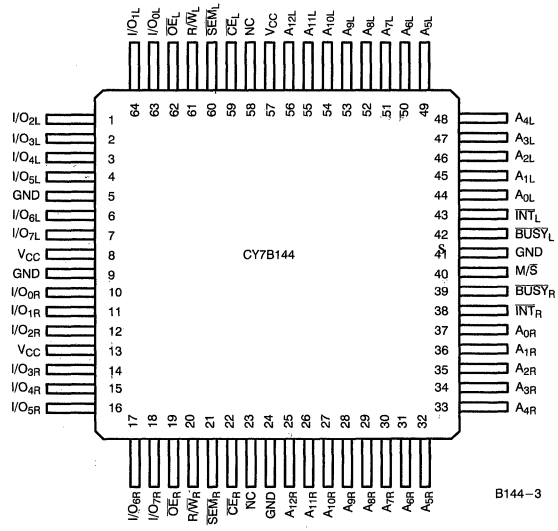
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

Pin Configurations

68-Pin LCC/PLCC
Top View



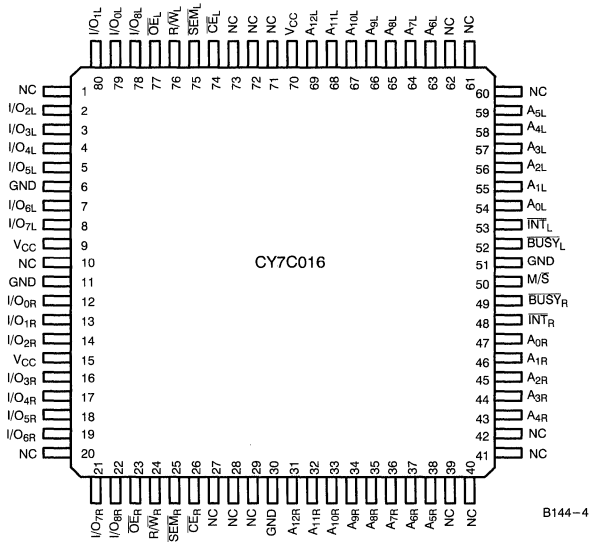
64-Pin TQFP
Top View



Notes:
3. I/O_{8R} on the CY7B145.
4. I/O_{8L} on the CY7B145.

Pin Configurations (continued)

80-Pin TQFP
Top View



Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data bus Input/Output
A_{0L-12L}	A_{0R-12R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. $\overline{INT}_R$ is set when left port writes location 1FFF and is cleared when right port reads location 1FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B144–15 7B145–15	7B144–25 7B145–25	7B144–35 7B145–35	7B144–55 7B145–55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military		280	250	
Maximum Standby Current for I_{SB1} (mA)	Commercial	110	95	90	90
	Military		100	95	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[5] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[6]	−55°C to +125°C	5V ± 10%

Notes:

5. Pulse width < 20 ns.

6. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		260		220	mA
			Mil/Ind				280	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		110		95	mA
			Mil/Ind				100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		165		145	mA
			Mil/Ind				180	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind				30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		160		140	mA
			Mil/Ind				160	

Parameter	Description	Test Conditions		7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	7B144–55 7B145–55 Min.	7B144–55 7B145–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		130		130	mA
			Mil/Ind		140		140	

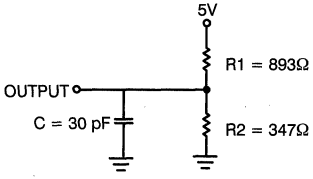
Notes:

7. See the last page of this specification for Group A subgroup testing information.
8. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance[9]

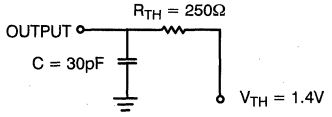
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

AC Test Loads and Waveforms



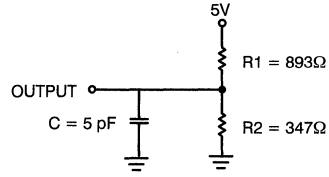
(a) Normal Load (Load 1)

B144–5



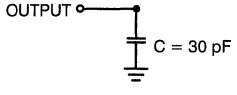
(b) Thévenin Equivalent (Load 1)

B144–6



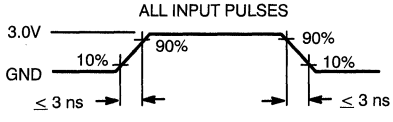
(c) Three-State Delay (Load 3)

B144–7



Load (Load 2)

B144–8



B144–9

Switching Characteristics Over the Operating Range[7, 10]

Parameter	Description	7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	7B144–55 7B145–55 Min.	7B144–55 7B145–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		25	ns
t_{LZOE}[11, 12]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[11, 12]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[11, 12]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[11, 12]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns

Notes:

9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
12. Test conditions used are Load 3.

Switching Characteristics Over the Operating Range[7, 10] (continued)

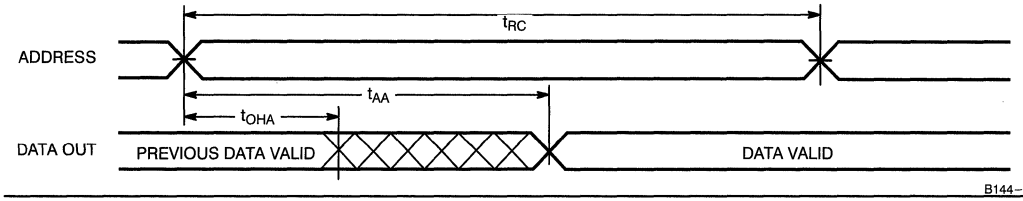
Parameter	Description	7B144–15 7B145–15		7B144–25 7B145–25		7B144–35 7B145–35		7B144–55 7B145–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[12]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[12]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[13]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[13]	Write Data Valid to Read Data Valid		25		30		35		40	ns
BUSY TIMING[14]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		30		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35		55	ns
INTERRUPT TIMING[14]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		35	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		35	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

Notes:

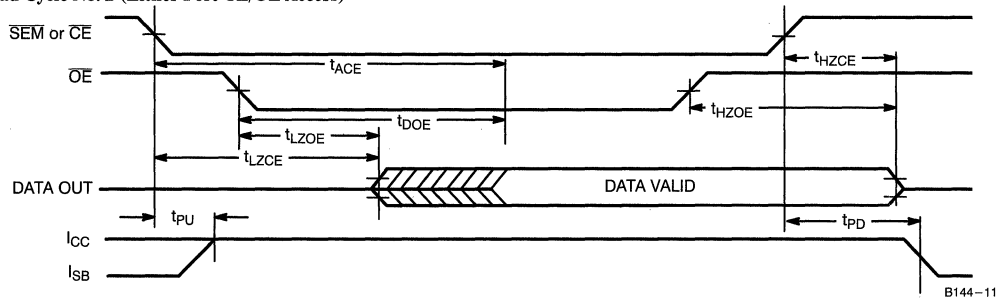
13. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
14. Test conditions used are Load 2.

Switching Waveforms

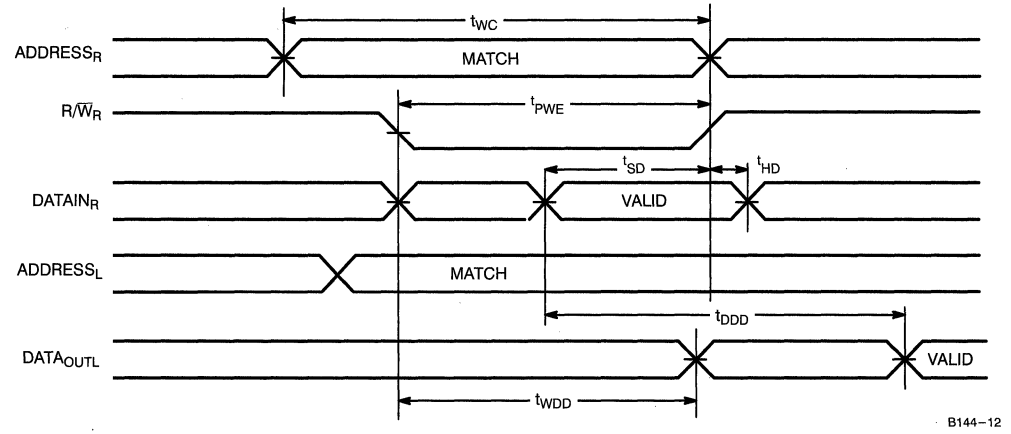
Read Cycle No. 1 (Either Port Address Access)[15, 16]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[15, 17, 18]



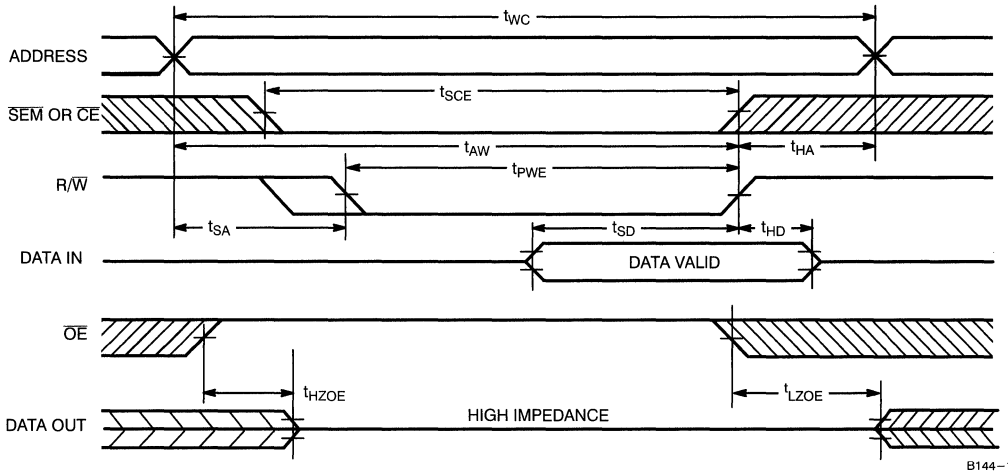
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[19, 20]



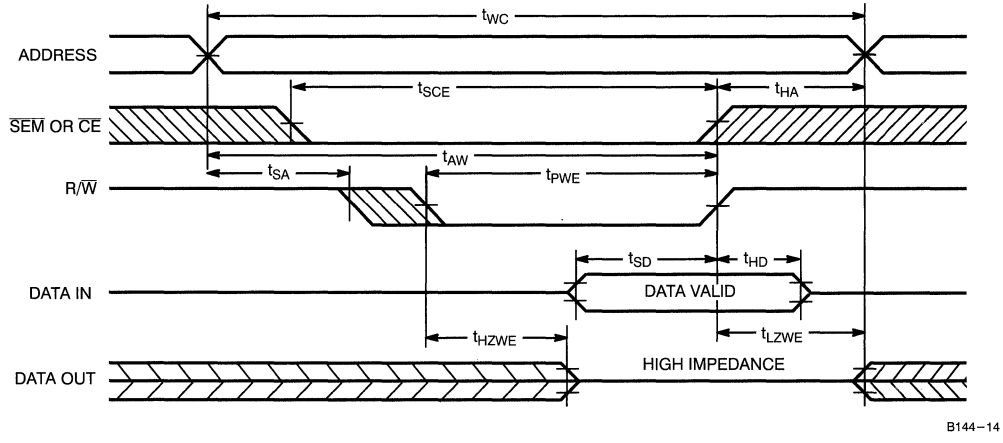
Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[21, 22, 23]



Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[21, 23, 24]

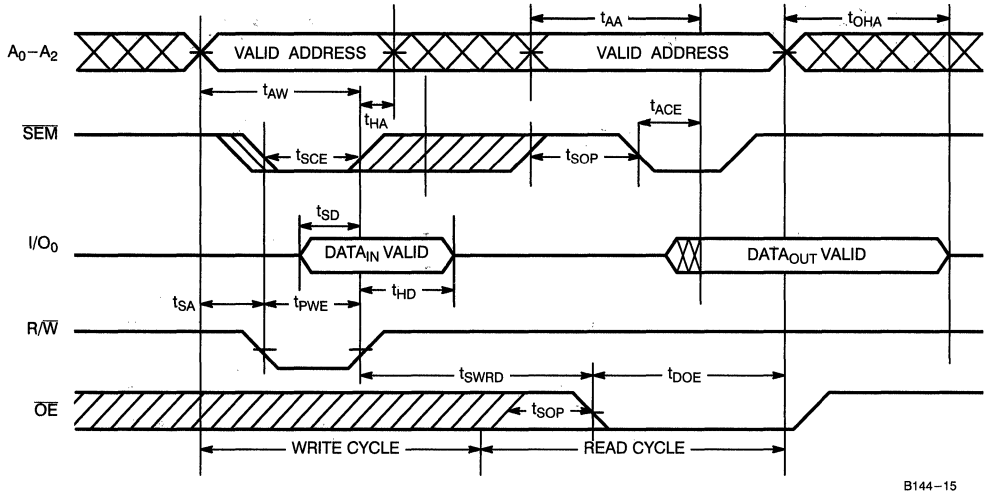


Notes:

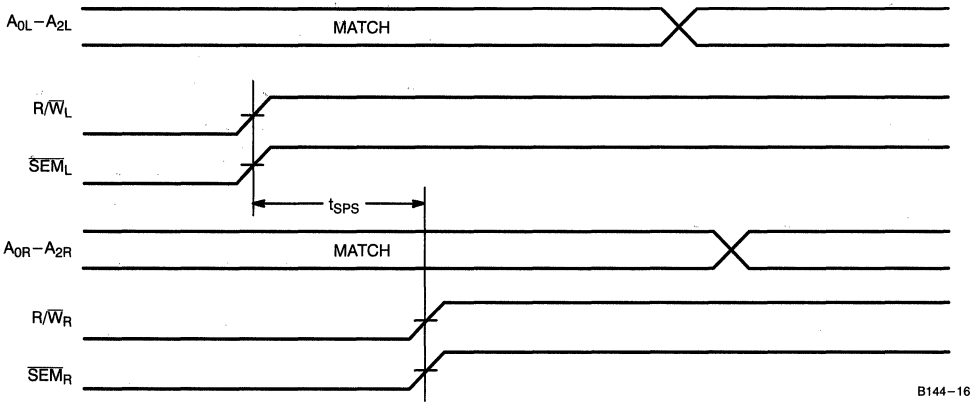
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.
24. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[25]



Semaphore Contention[26, 27, 28]

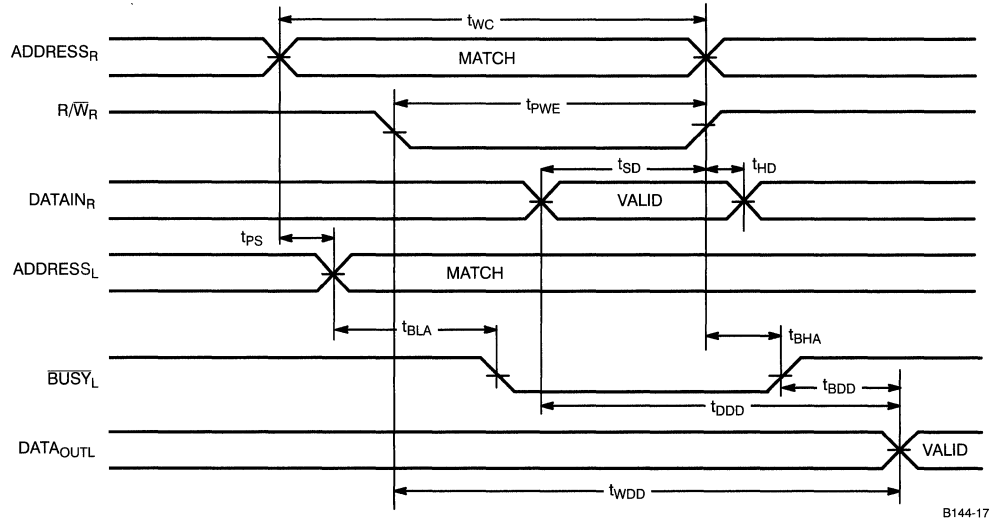


Notes:

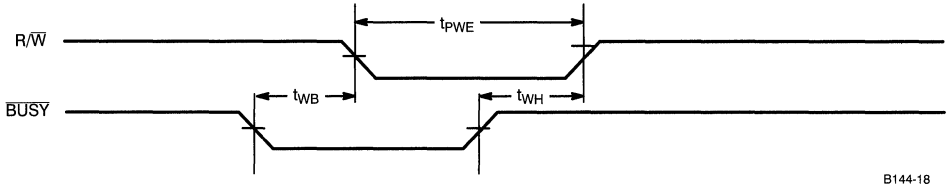
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[20]



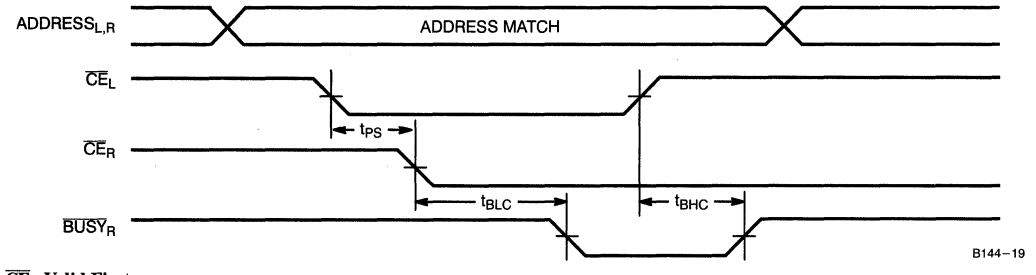
Write Timing with Busy Input (M/$\overline{S}$=LOW)



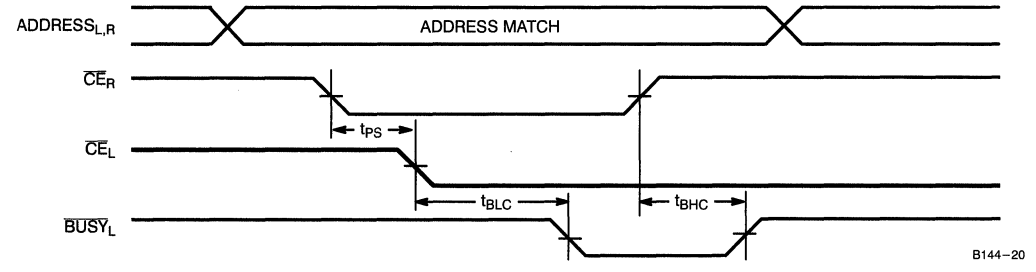
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[29]

$\overline{CE}_L$ Valid First:

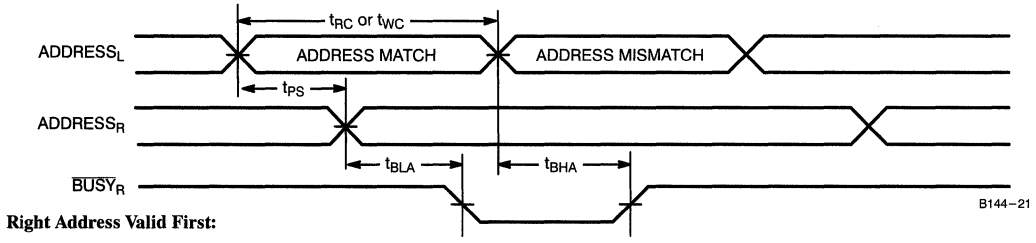


$\overline{CE}_R$ Valid First:

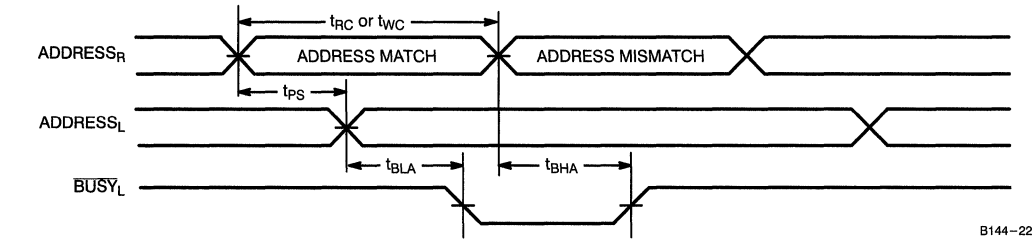


Busy Timing Diagram No. 2 (Address Arbitration)[29]

Left Address Valid First:



Right Address Valid First:



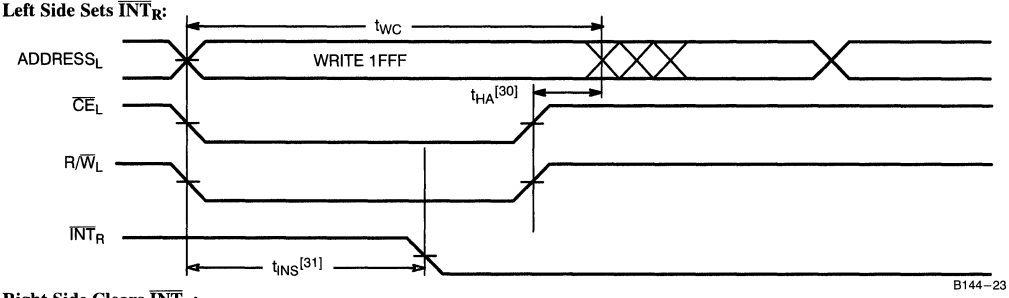
Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

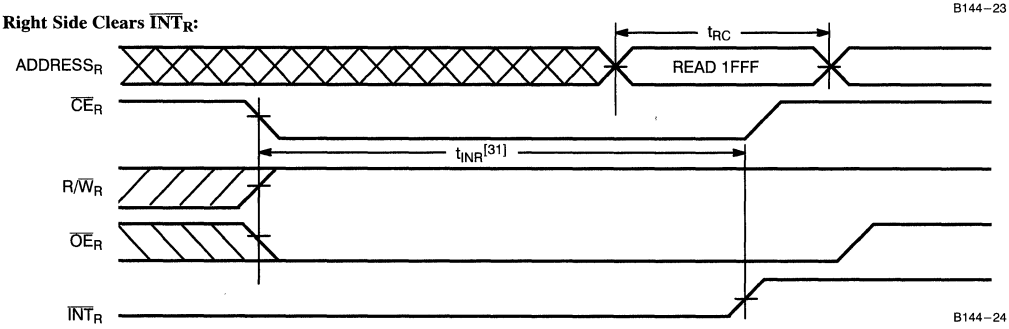
Switching Waveforms (continued)

Interrupt Timing Diagrams

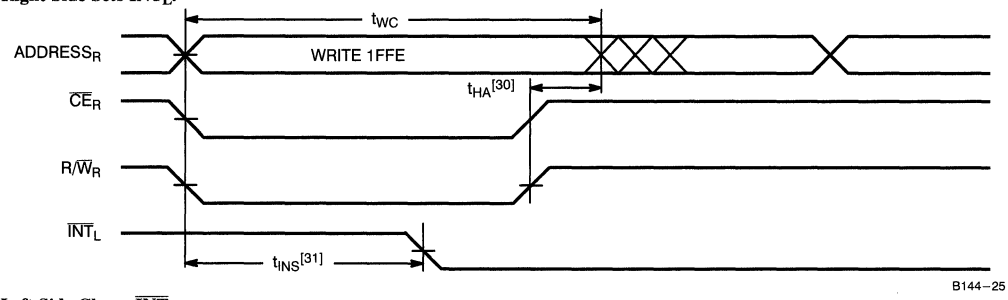
Left Side Sets $\overline{INT}_R$:



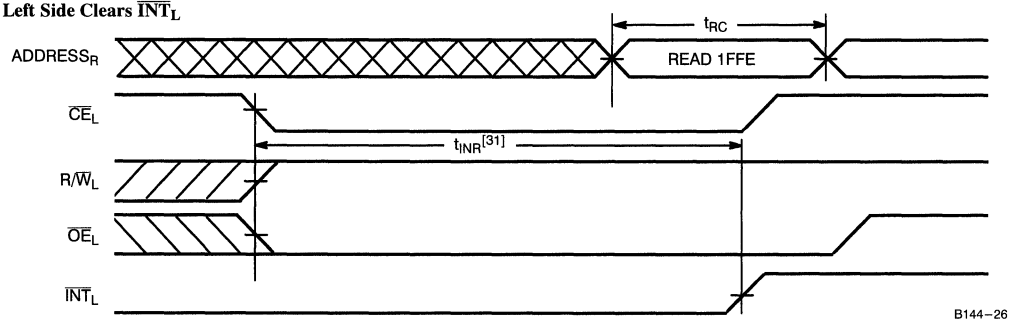
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Architecture

The CY7B144/5 consists of a an array of 8K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B144/5 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B144/5 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B144/5 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location 1FFF, the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. all Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

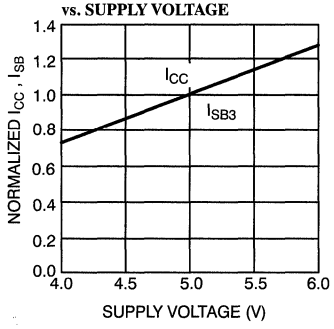
	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset Left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 3. Semaphore Operation Example

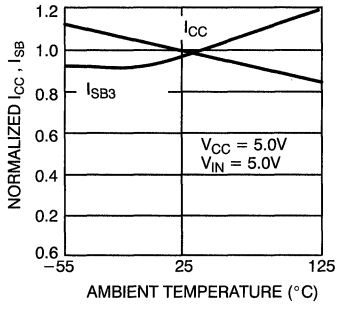
Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

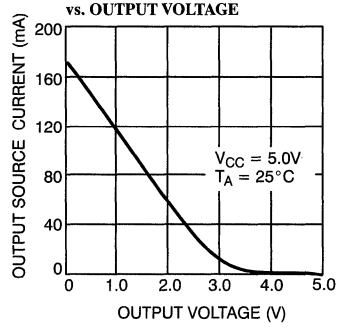
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



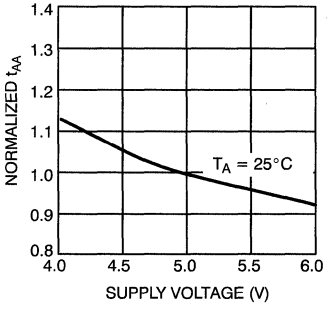
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



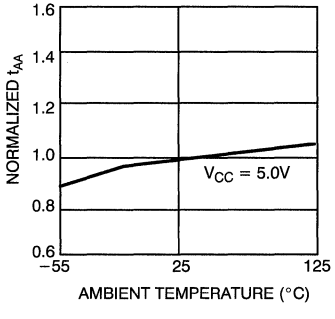
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



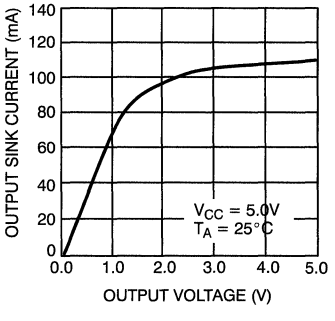
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



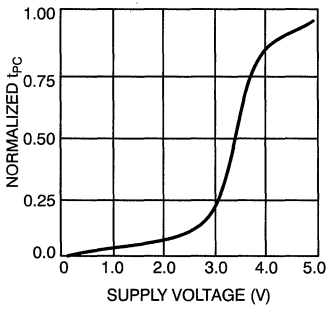
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



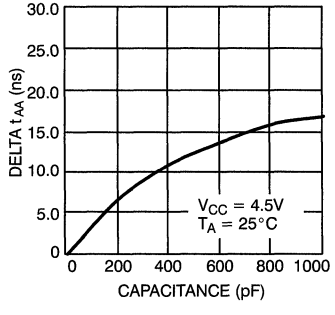
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



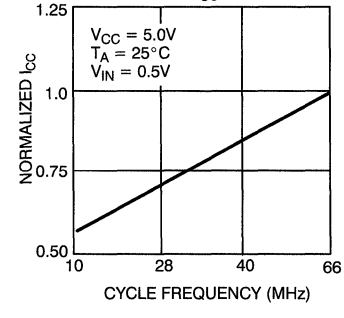
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B144–15AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B144–25AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B144–35AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B144–55AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–55AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B145–15AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B145–25AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B145–35AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B145–55AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–55AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38-00163-G

Section Contents

Data Communications Products

CY10E383
CY101E383

ECL/TTL/ECL Translator and High-Speed Bus Driver

Features

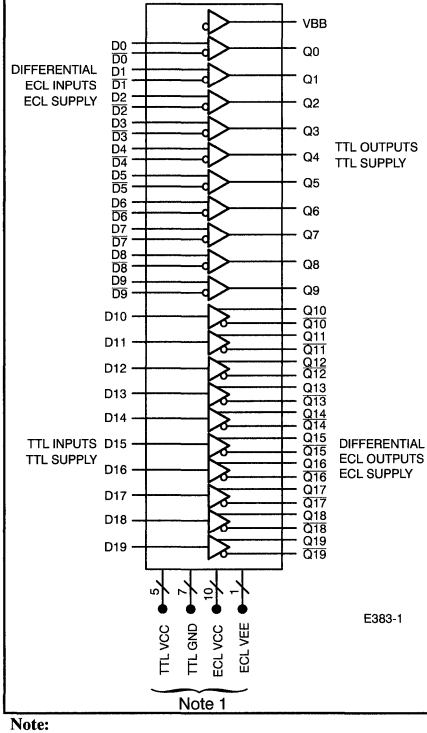
- **BiCMOS for optimum speed/power**
- **High speed (max.)**
  - **— 2.5 ns t_{PD} TTL-to-ECL**
  - **— 3.5 ns t_{PD} ECL-to-TTL**
- **Low skew < ± 1 ns**
- **Can operate on single +5V supply**
- **Full-duplex ECL/TTL data transmission**
- **Internal 2 kΩ ECL pull-down resistors on each ECL output**
- **80-pin PQFP package**
- **Surface-mount PLCC/CLCC package**
- **V_{BB} ECL reference voltage output**
- **Single- or dual-supply operation**
- **Capable of greater than 2001V ESD**
- **ECL cable/twisted pair driver**

Functional Description

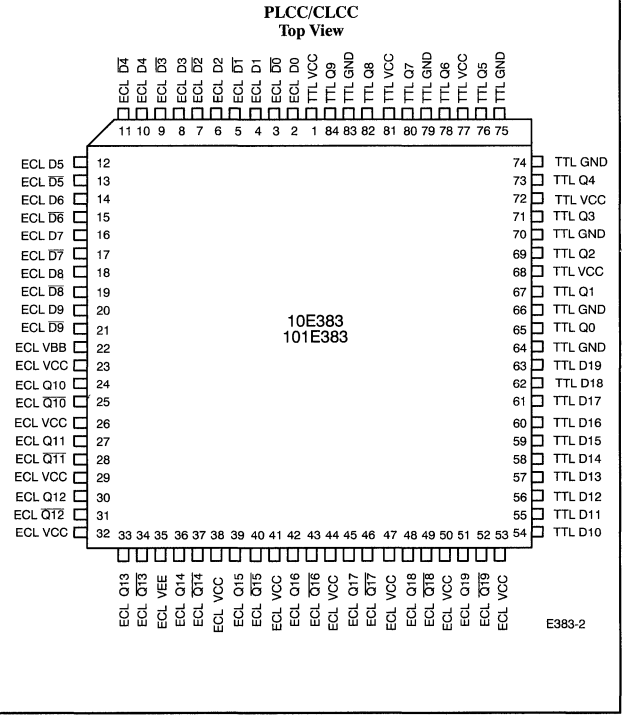
The CY10/101E383 is a new-generation TTL-to-ECL and ECL-to-TTL logic level translator designed for high-performance systems. The device contains ten independent TTL-to-ECL and ten independent ECL-to-TTL translators for high-speed full-duplex data transmission, mixed logic, and bus applications. The CY10/101E383 is especially suited to drive ECL backplanes between TTL boards. The CY10/101E383 is implemented with differential ECL I/O to provide balanced low noise operation over controlled impedance buses between TTL and/or ECL subsystems. In addition, the device has internal output 2 kΩ pull-down resistors tied to V_{EE} to decrease the number of external components. For system testing purposes or for driving light loads, the 2 kΩ is used as the only termination thereby eliminating up to 20 external resistors. The part meets standard 10K/10KH and 100K logic levels with the internal pull-down while driving 50Ω to −2V.

The device is designed with ample ground pins to reduce bounce, and has separate ECL and TTL power/ground pins to reduce noise coupling between logic families. The parts can operate in single- or dual-supply configurations while maintaining absolute 10K/10KH and 100K level swings. The translators are offered in standard 10K/10KH (10E) and 100K (101E) ECL-compatible versions with −5.2V or −4.5V power supply. The TTL I/O is fully TTL compatible. The CY10/101E383 is packaged in 84-pin surface-mountable PLCCs and CLCCs. To save board space, an 80-pin PQFP package with 25-mil-lead pitch is available.

Logic Block Diagram



Pin Configurations

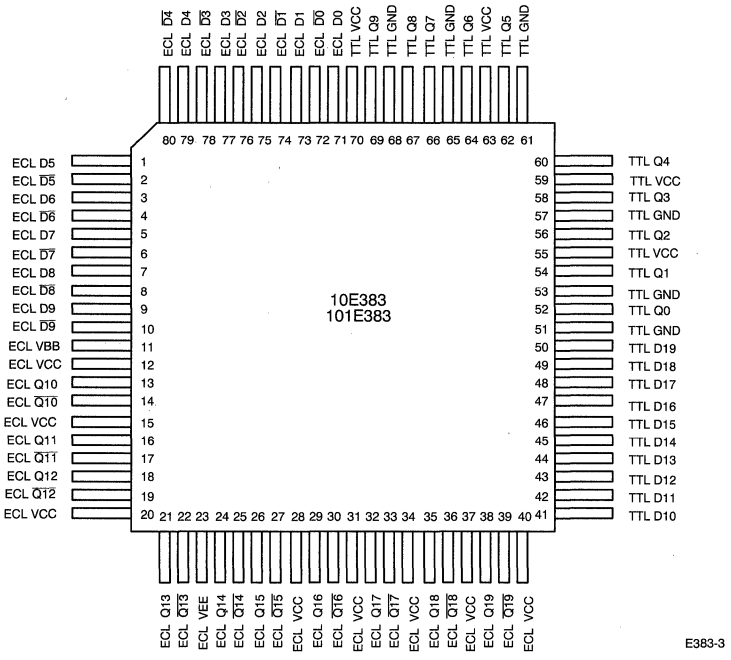


Note:

1. The PQFP package has one less each TTL V_{CC} and TTL GND pin and two less ECL V_{CC} pins.

Pin Configurations (continued)

PQFP
Top View



E383-3

Selection Guide

	10E383–2 101E383–2	10E383–3 101E383–3
Maximum Propagation Delay Time (ns) (TTL to ECL)	2.5	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	3.5	4
Maximum Operating Current (mA) Sum of I_{EE} and I_{CC}	270	270

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

TTL Supply Voltage to Ground Potential ... −0.5V to +7.0V

TTL DC Input Voltage ..... −3.0V to +7.0V

ECL Supply Voltage V_{EE} to ECL V_{CC} ..... −7.0V to +0.5V

ECL Input Voltage ..... V_{EE} to +0.5V

ECL Output Current ..... −50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	I/O	Version	Ambient Temperature	ECL V_{EE}	TTL V_{CC}
Commercial	10K 10KH	10E	0°C to +75°C	−5.2V ± 5%	5V ± 5%
Commercial	100K	101E	0°C to +85°C	−4.2V to −5.46V	5V ± 5%
Military	10K 10KH	10E	−55°C to +125°C case	−5.2V ± 5%	5V ± 5%

ECL Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	Temperature[3]	10E383 Min.	10E383 Max.	101E383 Min.	101E383 Max.	Unit
V_{OH}	Output HIGH Voltage	10E, R_L = 50Ω to −2V $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	T_C = −55°C	−1140	−900			mV
			T_A = 0°C	−1000	−840			mV
			T_A = +25°C	−960	−810			mV
			T_A = +75°C	−900	−735			mV
			T_C = +125°C	−880	−700			mV
		101E, R_L = 50Ω to −2V, $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	T_A = 0°C to 85°C			−1025	−880	mV
V_{OL}	Output LOW Voltage	10E, R_L = 50Ω to −2V $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	T_C = −55°C	−1920	−1670			mV
			T_A = 0°C	−1870	−1665			mV
			T_A = +25°C	−1850	−1650			mV
			T_A = +75°C	−1830	−1625			mV
			T_C = +125°C	−1830	−1610			mV
		101E, R_L = 50Ω to −2V, $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	T_A = 0°C to 85°C			−1810	−1620	mV
V_{IH}	Input HIGH Voltage	10E	T_C = −55°C	−1260	−900			mV
			T_A = 0°C	−1170	−840			mV
			T_A = +25°C	−1130	−810			mV
			T_A = +75°C	−1070	−720			mV
			T_C = +125°C	−1030	−700			mV
		101E	T_A = 0°C to 85°C			−1165	−880	mV
V_{IL}	Input LOW Voltage	10E	T_C = −55°C	−1950	−1540			mV
			T_A = 0°C	−1950	−1480			mV
			T_A = +25°C	−1950	−1475			mV
			T_A = +75°C	−1950	−1450			mV
			T_C = +125°C	−1950	−1450			mV
		101E	T_A = 0°C to 85°C			−1810	−1475	mV
V_{BB}	Output Reference Voltage	10E[4]	T_A = 0°C to 75°C	−1.37	−1.18			V
			T_C = −55°C	−1.46	−1.32			
			T_C = +125°C	−1.29	−1.14			
		101E[4]	T_A = 0°C to 85°C			−1.40	−1.23	
V_{CM}[5]	Common Mode Voltage	±V_{CM} with respect to V_{BB}			1.0		1.0	V
V_{DIFF}	Input Voltage Differential	Required for Full Output Swing		150		150		mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ Max.			220		220	µA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ Min.		−0.5	170	−0.5	170	µA
R_{PD}	Pull-Down Resistor	Connected from All ECL Outputs to V_{EE}	T_A = 0°C to 75°C	1.6	2.4			kΩ
			T_C = −55°C to +125°C	1.6	2.4			
			T_A = 0°C to 85°C			1.6	2.4	
I_{EE}	Supply Current (All inputs and outputs open)				−180		−180	mA

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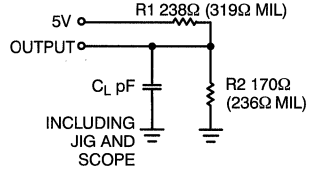
TTL Electrical Characteristics Over the Operating Range[2]

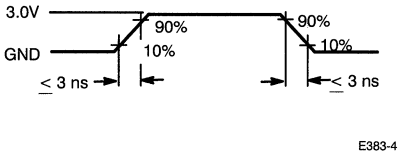
Parameter	Description	Test Conditions	10E383 101E383 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Max., I_{OL} = 16.0 mA		0.5	V
V_{IH}	Input HIGH Voltage[6]		2.0		V
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{CD}	Input Clamp Diode Voltage	I_{IN} = −10 mA	−1.5		V
I_{OS}[7]	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[8]	−180	−40	mA
I_{IX}	Input Load Current[9]	GND ≤ V_I ≤ V_{CC}	−250	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		90	mA

Capacitance[7]

Parameter	Description	Max.	Unit
C_{IN}	Input Capacitance	4	pF
C_{OUT}	Output Capacitance	5	pF

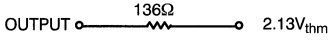
TTL AC Test Load and Waveform[10]



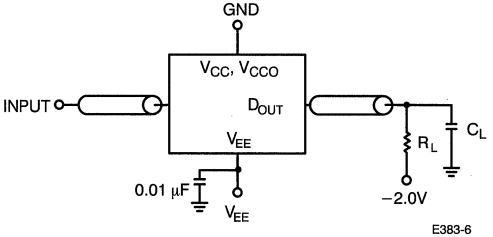


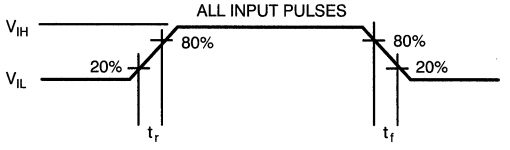
Equivalent to: THÉVENIN EQUIVALENT (Commercial)

THÉVENIN EQUIVALENT (Military)



ECL AC Test Load and Waveform[11, 12, 13, 14, 15, 16]





Notes:

2. See AC Test Load and Waveform for test conditions.
3. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
4. Max. I_{BB} = −1 mA.
5. The internal gain of the CY101/10E383 guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
6. These are absolute values with respect to device ground.
7. Characterized initially and after any design or process changes that may affect these parameters.
8. Not more than one output should be tested at a time. Duration of the short should not be more than one second.
9. I/O pin leakage is the worst case of I_{IX} (where X = H or L).
10. TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 10 pF.
11. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10KH version.
12. V_{IL} = −1.7V, V_{IH} = −0.9V on 101E version.
13. ECL R_L = 50Ω, C_L < 5 pF (includes fixture and stray capacitance).
14. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
15. t_r = t_f = 0.7 ns
16. All timing measurements are made from the 50% point of all waveforms.

ECL-to-TTL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	10E383–2 101E383–2		10E383–3 101E383–3		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	3	1	4	ns
t_{PHL}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	3	1	4	ns

TTL-to-ECL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	10E383–2 101E383–2		10E383–3 101E383–3		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	2.5	1	3	ns
t_{PHL}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	2.5	1	3	ns
t_R	Output Rise Time	20% to 80%	0.35	1.7	0.35	1.7	ns
t_F	Output Fall Time	20% to 80%	0.35	1.7	0.35	1.7	ns

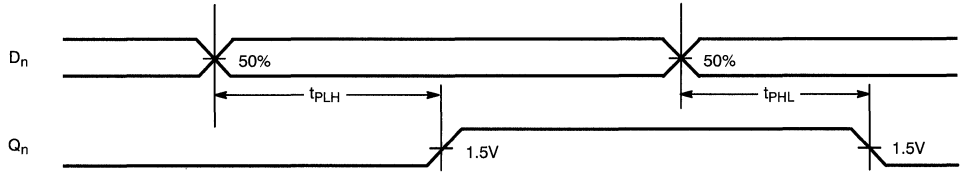
Skew Time Switching Characteristics[7] (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

Symbol	Characteristic	Test Conditions	Min.	Max.	Unit
t_{SKT}	Data Skew Time ECL-to-TTL	$TTLQ_n$ to $TTLQ_{n+m}$		1	ns
t_{SKE}	Data Skew Time TTL-to-ECL	$ECLQ_n$, $\overline{Q}_n$ to $ECLQ_{n+m}$, $\overline{Q}_{n+m}$		1	ns

7

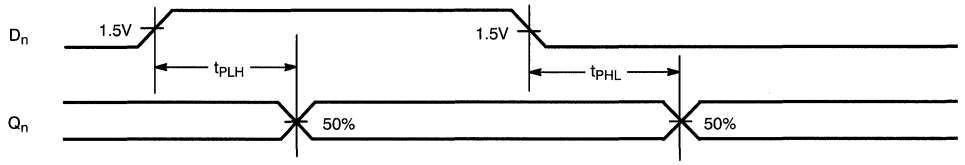
Switching Waveforms

ECL-to-TTL Timing



E383-8

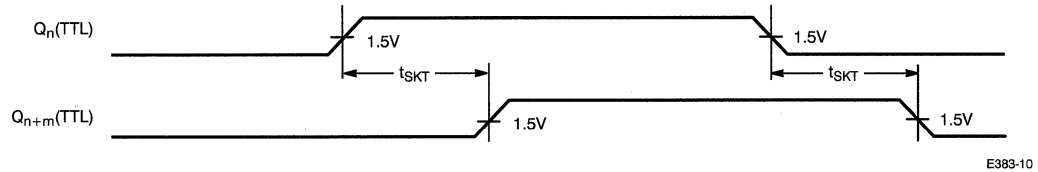
TTL-to-ECL Timing



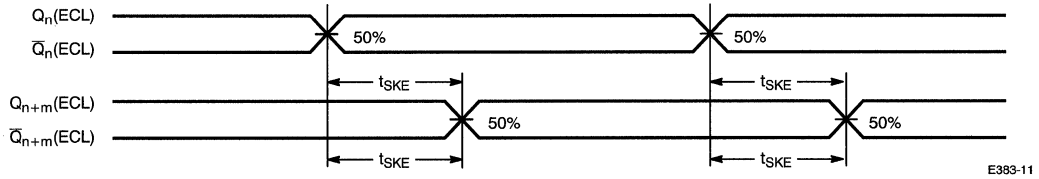
E383-9

Switching Waveforms (continued)

Skew Test (t_{SKT})
TTL_{Qn}-to-TTL_{Qn+m}



Skew Test (t_{SKE})
ECL_{Qn}, $\overline{Q}_n$-to-ECL_{Qn+m}, $\overline{Q}_{n+m}$



ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL $\overline{D}_n$	TTL Q_n
Open[17]	Open[17]	L
L	H	L
H	L	H

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL $\overline{Q}_n$
L	L	H
H	H	L

Nominal Voltages

The CY101/10E383 can be used in dual ±5V or single +5V supply systems. The supply pins should be connected as shown in *Tables 1* and *2*. This connection technique involves shifting up all ECL supply pins by 5V. When operating in single-supply systems, the ECL termination voltage level must also be shifted up by adding 5V. For example, if the termination is 50 ohms to −2V in a dual-supply system, the single +5V system should have 50 ohms to +3V. If the termination is a thévenin type, then the resistor tied to ground is now at +5V and the resistor tied to −5V is now at ground potential. Consideration should be given to the power supply so that adequate bypassing is made to isolate the ECL output switching noise from the supply. Having separate TTL and ECL +5V supply lines will help to reduce the noise. *Table 3* shows the CY10E383 nominal voltages applied in a 10K system.

Table 1. CY101E383 Nominal Voltages Applied in 100K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−4.5V

Table 2. CY101E383 Nominal Voltages Applied in 101K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−5.2V

Table 3. CY10E383 Nominal Voltages Applied in 10K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−5.2V

Note:
17. The ECL inputs will pull to a known logic level if left open.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
2.5	CY10E383–2JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY10E383–2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY10E383–3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY10E383–3NC	N80	80-Lead Plastic Quad Flatpack	
	CY10E383–3YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
2.5	CY101E383–2JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383–2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY101E383–3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383–3NC	N80	80-Lead Plastic Quad Flatpack	

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CY7B923
CY7B933

HOTLink™ Transmitter/Receiver

Features

- **Fibre Channel compliant**
- **IBM ESCON® compliant**
- **ATM-compliant**
- **8B/10B-coded or 10-bit unencoded**
- **160- to 330-Mbps data rate**
- **TTL synchronous I/O**
- **No external PLL components**
- **Triple PECL 100K serial outputs**
- **Dual PECL 100K serial inputs**
- **Low power: 350 mW (Tx), 650 mW (Rx)**
- **Compatible with fiber optic modules, coaxial cable, and twisted pair media**
- **Built-In Self-Test**
- **Single +5V supply**
- **28-pin SOIC/PLCC/LCC**
- **0.8μ BiCMOS**

Functional Description

The CY7B923 HOTLink™ Transmitter and CY7B933 HOTLink Receiver are point-to-point communications building blocks that transfer data over high-speed serial links (fiber, coax, and twisted pair) at 160 to 330 Mbits/second. *Figure 1* illustrates typical connections to host systems or controllers.

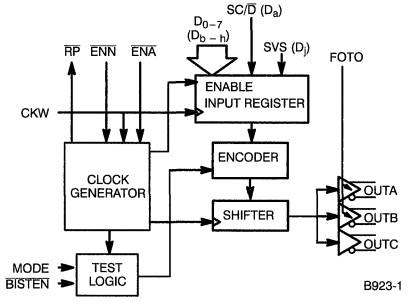
Eight bits of user data or protocol information are loaded into the HOTLink transmitter and are encoded. Serial data is shifted out of the three differential positive ECL (PECL) serial ports at the bit rate (which is 10 times the byte rate).

The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The bit stream is deserialized, decoded, and checked for transmission errors. Recovered bytes are presented in parallel to the receiving host along with a byte rate clock.

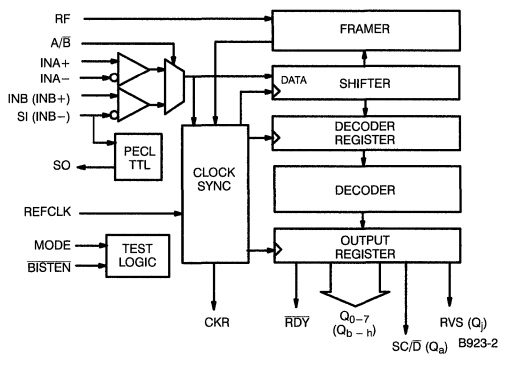
The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. I/O signals are available to create a seamless interface with both asynchronous FIFOs (i.e., CY7C42X) and clocked FIFOs (i.e., CY7C44X). A Built-In Self-Test pattern generator and checker allows testing of the transmitter, receiver, and the connecting link as a part of a system diagnostic check.

HOTLink devices are ideal for a variety of applications where a parallel interface can be replaced with a high-speed point-to-point serial link. Applications include interconnecting workstations, servers, mass storage, and video transmission equipment.

CY7B923 Transmitter Logic Block Diagram



CY7B933 Receiver Logic Block Diagram



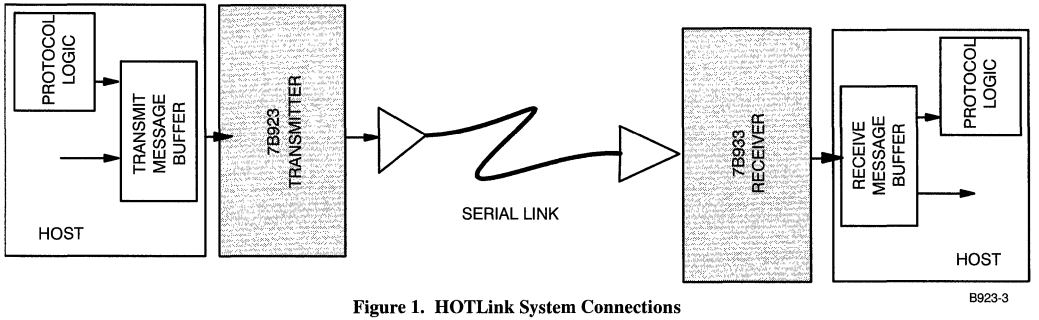
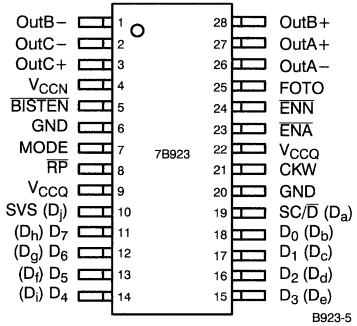


Figure 1. HOTLink System Connections

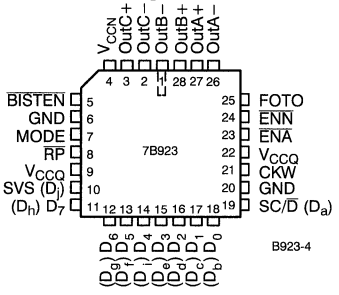
HOTLink is a trademark of Cypress Semiconductor Corporation.
ESCON is a registered trademark of IBM.

CY7B923 Transmitter Pin Configurations

SOIC
Top View

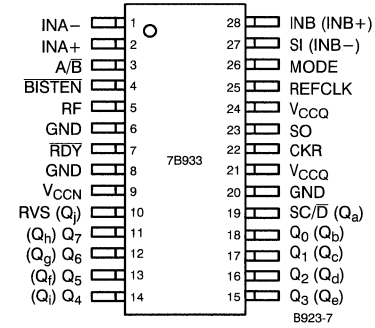


PLCC/LCC
Top View

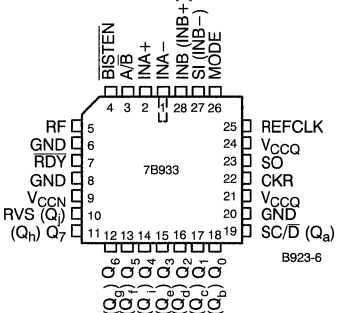


CY7B933 Receiver Pin Configurations

SOIC
Top View



PLCC/LCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into PECL outputs (HIGH) ..... −50 mA

Static Discharge Voltage ..... >4001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C Case Temperature	5V ± 10%

Pin Descriptions

CY7B923 HOTLink Transmitter

Name	I/O	Description
D_{0-7} (D_{b-h})	TTL In	Parallel Data Input. Data is clocked into the Transmitter on the rising edge of CKW if $\overline{ENA}$ is LOW (or on the next rising CKW with $\overline{ENN}$ LOW). If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, a Null character (K28.5) is sent. When MODE is HIGH, $D_{0,\,1,\,...7}$ become $D_{b,\,c,...h}$ respectively.
SC/$\overline{D}$ (D_a)	TTL In	Special Character/Data Select. A HIGH on SC/$\overline{D}$ when CKW rises causes the transmitter to encode the pattern on D_{0-7} as a control code (Special Character), while a LOW causes the data to be coded using the 8B/10B data alphabet. When MODE is HIGH, SC/$\overline{D}$ (D_a) acts as D_a input. SC/$\overline{D}$ has the same timing as D_{0-7}.
SVS (D_j)	TTL In	Send Violation Symbol. If SVS is HIGH when CKW rises, a Violation symbol is encoded and sent while the data on the parallel inputs is ignored. If SVS is LOW, the state of D_{0-7} and SC/$\overline{D}$ determines the code sent. In normal or test mode, this pin overrides the BIST generator and forces the transmission of a Violation code. When MODE is HIGH (placing the transmitter in unencoded mode), SVS (D_j) acts as the D_j input. SVS has the same timing as D_{0-7}.
$\overline{ENA}$	TTL In	Enable Parallel Data. If $\overline{ENA}$ is LOW on the rising edge of CKW, the data is loaded, encoded, and sent. If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the data inputs are ignored and the Transmitter will insert a Null character (K28.5) to fill the space between user data. $\overline{ENA}$ may be held HIGH/LOW continuously or it may be pulsed with each data byte to be sent. If $\overline{ENA}$ is being used for data control, $\overline{ENN}$ will normally be strapped HIGH, but can be used for BIST function control.
$\overline{ENN}$	TTL In	Enable Next Parallel Data. If $\overline{ENN}$ is LOW, the data appearing on D_{0-7} at the next rising edge of CKW is loaded, encoded, and sent. If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the data appearing on D_{0-7} at the next rising edge of CKW will be ignored and the Transmitter will insert a Null character to fill the space between user data. $\overline{ENN}$ may be held HIGH/LOW continuously or it may be pulsed with each data byte sent. If $\overline{ENN}$ is being used for data control, $\overline{ENA}$ will normally be strapped HIGH, but can be used for BIST function control.
CKW	TTL In	Clock Write. CKW is both the clock frequency reference for the multiplying PLL that generates the high-speed transmit clock, and the byte rate write signal that synchronizes the parallel data input. CKW must be connected to a crystal controlled time base that runs within the specified frequency range of the Transmitter and Receiver.
FOTO	TTL In	Fiber Optic Transmitter Off. FOTO determines the function of two of the three PECL transmitter output pairs. If FOTO is LOW, the data encoded by the Transmitter will appear at the outputs continuously. If FOTO is HIGH, OUTA± and OUTB± are forced to their "logic zero" state (OUT+ = LOW and OUT− = HIGH), causing a fiber optic transmit module to extinguish its light output. OUTC is unaffected by the level on FOTO, and can be used as a loop-back signal source for board-level diagnostic testing.
OUT A± OUT B± OUT C±	PECL Out	Differential Serial Data Outputs. These PECL 100K outputs (+5V referenced) are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. Unused pairs of outputs can be wired to V_{CC} to reduce power if the output is not required. OUTA± and OUTB± are controlled by the level on FOTO, and will remain at their "logical zero" states when FOTO is asserted. OUTC± is unaffected by the level on FOTO. (OUTA+ and OUTB+ are used as a differential test clock input while in Test mode, i.e., MODE=UNCONNECTED or forced to $V_{CC}/2$.)
MODE	3-Level In	Encoder Mode Select. The level on MODE determines the encoding method to be used. When wired to GND, MODE selects 8B/10B encoding. When wired to V_{CC}, data inputs bypass the encoder and the bit pattern on D_{a-j} goes directly to the shifter. When left floating (internal resistors hold the input at $V_{CC}/2$) the internal bit-clock generator is disabled and OUTA+/OUTB+ become the differential bit clock to be used for factory test. In typical applications MODE is wired to V_{CC} or GND.
$\overline{BISTEN}$	TTL In	Built-In Self-Test Enable. When $\overline{BISTEN}$ is LOW and $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the transmitter sends an alternating 1−0 pattern (D10.2 or D21.5). When either $\overline{ENA}$ or $\overline{ENN}$ is set LOW and $\overline{BISTEN}$ is LOW, the transmitter begins a repeating test sequence that allows the Transmitter and Receiver to work together to test the function of the entire link. In normal use this input is held HIGH or wired to V_{CC}. The BIST generator is a free-running pattern generator that need not be initialized, but if required, the BIST sequence can be initialized by momentarily asserting SVS while $\overline{BISTEN}$ is LOW. $\overline{BISTEN}$ has the same timing as D_{0-7}.
$\overline{RP}$	TTL Out	Read Pulse. $\overline{RP}$ is a 60% LOW duty-cycle byte-rate pulse train suitable for the read pulse in CY7C42X FIFOs. The frequency on $\overline{RP}$ is the same as CKW when enabled by $\overline{ENA}$, and duty cycle is independent of the CKW duty cycle. Pulse widths are set by logic internal to the transmitter. In BIST mode, $\overline{RP}$ will remain HIGH for all but the last byte of a test loop. $\overline{RP}$ will pulse LOW one byte time per BIST loop.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B933 HOTLink Receiver

Name	I/O	Description
Q_{0-7} (Q_{b-h})	TTL Out	Q_{0-7} Parallel Data Output. Q_{0-7} contain the most recently received data. These outputs change synchronously with CKR. When MODE is HIGH, $Q_{0,1,...7}$ become $Q_{b,c,...h}$ respectively.
SC/$\overline{D}$ (Q_a)	TTL Out	Special Character/Data Select. SC/$\overline{D}$ indicates the context of received data. HIGH indicates a Control (Special Character) code, LOW indicates a Data character. When MODE is HIGH (placing the receiver in Unencoded mode), SC/$\overline{D}$ acts as the Q_a output. SC/$\overline{D}$ has the same timing as Q_{0-7}.
RVS (Q_j)	TTL Out	Received Violation Symbol. A HIGH on RVS indicates that a code rule violation has been detected in the received data stream. A LOW shows that no error has been detected. In BIST mode, a LOW on RVS indicates correct operation of the Transmitter, Receiver, and link on a byte-by-byte basis. When MODE is HIGH (placing the receiver in Unedcoded mode), RVS acts as the Q_j output. RVS has the same timing as Q_{0-7}.
$\overline{RDY}$	TTL Out	Data Output Ready. A LOW pulse on $\overline{RDY}$ indicates that new data has been received and is ready to be delivered. A missing pulse on $\overline{RDY}$ shows that the received data is the Null character (normally inserted by the transmitter as a pad between data inputs). In BIST mode $\overline{RDY}$ will remain LOW for all but the last byte of a test loop and will pulse HIGH one byte time per BIST loop.
CKR	TTL Out	Clock Read. This byte rate clock output is phase and frequency aligned to the incoming serial data stream. $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS all switch synchronously with the rising edge of this output.
A/$\overline{B}$	PECL in	Serial Data Input Select. This PECL 100K (+5V referenced) input selects INA or INB as the active data input. If A/$\overline{B}$ is HIGH, INA is connected to the shifter and signals connected to INA will be decoded. If A/$\overline{B}$ is LOW INB is selected.
INA±	Diff In	Serial Data Input A. The differential signal at the receiver end of the communication link may be connected to the differential input pairs INA± or INB±. Either the INA pair or the INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternative data input selected by the state of A/$\overline{B}$.
INB (INB+)	PECL in (Diff In)	Serial Data Input B. This pin is either a single-ended PECL data receiver (INB) or half of the INB of the differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, INB becomes a single-ended PECL 100K (+5V referenced) serial data input. INB is used as the test clock while in Test mode.
SI (INB−)	PECL in (Diff In)	Status Input. This pin is either a single-ended PECL status monitor input (SI) or half of the INB of the differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, SI becomes a single-ended PECL 100K (+5V referenced) status monitor input, which is translated into a TTL-level signal at the SO pin.
SO	TTL Out	Status Out. SO is the TTL-translated output of SI. It is typically used to translate the Carrier Detect output from a fiber-optic receiver connected to SI. When this pin is normally connected and loaded (without any external pull-up resistor), SO will assume the same logical level as SI and INB will become a single-ended PECL serial data input. If the status monitor translation is not desired, then SO may be wired to V_{CC} and the INB± pair may be used as a differential serial data input.
RF	TTL In	Reframe Enable. RF controls the Framer logic in the Receiver. When RF is held HIGH, each SYNC (K28.5) symbol detected in the shifter will frame the data that follows. If is HIGH for 2,048 consecutive bytes, the internal framer switches to double-byte mode. When RF is held LOW, the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC characters to reframe the data erroneously.
REFCLK	TTL In	Reference Clock. REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream. REFCLK must be connected to a crystal-controlled time base that runs within the frequency limits of the Tx/Rx pair, and the frequency must be the same as the transmitter CKW frequency (within CKW±0.1%)
MODE	3-Level In	Decoder Mode Select. The level on the MODE pin determines the decoding method to be used. When wired to GND, MODE selects 8B/10B decoding. When wired to V_{CC}, registered shifter contents bypass the decoder and are sent to Q_{a-j} directly. When left floating (internal resistors hold the MODE pin at $V_{CC}/2$) the internal bit clock generator is disabled and INB becomes the bit rate test clock to be used for factory test. In typical applications, MODE is wired to V_{CC} or GND.
$\overline{BISTEN}$	TTL In	Built-In Self-Test Enable. When $\overline{BISTEN}$ is LOW the Receiver awaits a D0.0 (sent once per BIST loop) character and begins a continuous test sequence that tests the functionality of the Transmitter, the Receiver, and the link connecting them. In BIST mode the status of the test can be monitored with $\overline{RDY}$ and RVS outputs. In normal use $\overline{BISTEN}$ is held HIGH or wired to V_{CC}. $\overline{BISTEN}$ has the same timing as Q_{0-7}.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B923 HOTLink Transmitter Block Diagram Description

Input Register

The Input register holds the data to be processed by the HOTLink transmitter and allows the input timing to be made consistent with standard FIFOs. The Input register is clocked by CKW and loaded with information on the D_{0-7}, SC/$\overline{D}$, and SVS pins. Two enable inputs ($\overline{ENA}$ and $\overline{ENN}$) allow the user to choose when data is loaded in the register. Asserting $\overline{ENA}$ (Enable, active LOW) causes the inputs to be loaded in the register on the rising edge of CKW. If $\overline{ENN}$ (Enable Next, active LOW) is asserted when CKW rises, the data present on the inputs on the next rising edge of CKW will be loaded into the Input register. If neither $\overline{ENA}$ nor $\overline{ENN}$ are asserted LOW on the rising edge of CKW, then a SYNC (K28.5) character is sent. These two inputs allow proper timing and function for compatibility with either asynchronous FIFOs or clocked FIFOs without external logic, as shown in *Figure 5.*

In BIST mode, the Input register becomes the signature pattern generator by logically converting the parallel Input register into a Linear Feedback Shift Register (LFSR). When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

Encoder

The Encoder transforms the input data held by the Input register into a form more suitable for transmission on a serial interface link. The code used is specified by ANSI X3.230 (Fibre Channel) and the IBM ESCON channel (code tables are at the end of this datasheet). The eight D_{0-7} data inputs are converted to either a Data symbol or a Special Character, depending upon the state of the SC/$\overline{D}$ input. If SC/$\overline{D}$ is HIGH, the data inputs represent a control code and are encoded using the Special Character code table. If SC/$\overline{D}$ is LOW, the data inputs are converted using the Data code table. If a byte time passes with the inputs disabled, the Encoder will output a Special Character Comma K28.5 (or SYNC) that will maintain link synchronization. SVS input forces the transmission of a specified Violation symbol to allow the user to check error handling system logic in the controller or for proprietary applications.

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller. This bypass is controlled by setting the MODE select pin HIGH. When in bypass mode, D_{a-j} (note that bit order is specified in the Fibre Channel 8B/10B code) become the ten inputs to the Shifter, with D_a being the first bit to be shifted out.

Shifter

The Shifter accepts parallel data from the Encoder once each byte time and shifts it to the serial interface output buffers using a PLL multiplied bit clock that runs at ten (10) times the byte clock rate. Timing for the parallel transfer is controlled by the counter included in the Clock Generator and is not affected by signal levels or timing at the input pins.

OutA, OutB, OutC

The serial interface PECL output buffers (ECL100K referenced to +5v) are the drivers for the serial media. They are all connected to the Shifter and contain the same serial data. Two of the output pairs (OUTA± and OUTB±) are controllable by the FOTO input and can be disabled by the system controller to force a logical zero (i.e., "light off") at the outputs. The third output pair (OUTC±) is not affected by FOTO and will supply a continuous data stream suitable for loop-back testing of the subsystem.

OUTA± and OUTB± will respond to FOTO input changes within a few bit times. However, since FOTO is not synchronized with the transmitter data stream, the outputs will be forced off or turned on at arbitrary points in a transmitted byte. This function is intended to augment an external laser safety controller and as an aid for Receiver PLL testing.

In wire-based systems, control of the outputs may not be required, and FOTO can be strapped LOW. The three outputs are intended to add system and architectural flexibility by offering identical serial bit streams with separate interfaces for redundant connections or for multiple destinations. Unneeded outputs can be wired to V_{CC} to disable and power down the unused output circuitry.

Clock Generator

The clock generator is an embedded phase-locked loop (PLL) that takes a byte-rate reference clock (CKW) and multiplies it by ten (10) to create a bit rate clock for driving the serial shifter. The byte rate reference comes from CKW, the rising edge of which clocks data into the Input register. This clock must be a crystal referenced pulse stream that has a frequency between the minimum and maximum specified for the HOTLink Transmitter/Receiver pair. Signals controlled by this block form the bit clock and the timing signals that control internal data transfers between the Input register and the Shifter.

The read pulse ($\overline{RP}$) is derived from the feedback counter used in the PLL multiplier. It is a byte-rate pulse stream with the proper phase and pulse widths to allow transfer of data from an asynchronous FIFO. Pulse width is independent of CKW duty cycle, since proper phase and duty cycle is maintained by the PLL. The $\overline{RP}$ pulse stream will insure correct data transfers between asynchronous FIFOs and the transmitter input latch with no external logic.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic to properly select the data encoding. Test logic is discussed in more detail in the CY7B923 HOTLink Transmitter Operating Mode Description.

CY7B933 HOTLink Receiver Block Diagram Description

Serial Data Inputs

Two pairs of differential line receivers are the inputs for the serial data stream. INA± or INB± can be selected with the A/$\overline{B}$ input. INA± is selected with A/$\overline{B}$ HIGH and INB± is selected with A/$\overline{B}$ LOW. The threshold of A/$\overline{B}$ is compatible with the ECL 100K signals from PECL fiber optic interface modules. TTL logic elements can be used to select the A or B inputs by adding a resistor pull-up to the TTL driver connected to A/$\overline{B}$. The differential threshold of INA± and INB± will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 20 db ($V_{DIF} \geq 50$mv) or can be directly connected to fiber optic interface modules (any ECL logic family, not limited to ECL 100K). The common mode tolerance will accommodate a wide range of signal termination voltages. The highest HIGH input that can be tolerated is $V_{IN} = V_{CC}$, and the lowest LOW input that can be interpreted correctly is V_{IN} = GND+2.0V.

PECL-TTL Translator

The function of the INB(INB+) input and the SI(INB−) input is defined by the connections on the SO output pin. If the PECL/TTL translator function is not required, the SO output is wired to

V_{CC}. A sensor circuit will detect this connection and cause the inputs to become INB± (a differential line-receiver serial-data input). If the PECL/TTL translator function is required, the SO output is connected to its normal TTL load (typically one or more TTL inputs, but no pull-up resistor) and the INB+ input becomes INB (single-ended ECL 100K, serial data input) and the INB− input becomes SI (single-ended, ECL 100K status input).

This positive-referenced PECL-to-TTL translator is provided to eliminate external logic between an PECL fiber-optic interface module "carrier detect" output and the TTL input in the control logic. The input threshold is compatible with ECL 100K levels (+5V referenced). It can also be used as part of the link status indication logic for wire connected systems.

Clock Synchronization

The Clock Synchronization function is performed by an embedded phase-locked loop (PLL) that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit rate clock to the serial data transitions. This block contains the logic to transfer the data from the Shifter to the Decode register once every byte. The counter that controls this transfer is initialized by the Framer logic. CKR is a buffered output derived from the bit counter used to control the Decode register and the output register transfers.

Clock output logic is designed so that when reframing causes the counter sequence to be interrupted, the period and pulse width of CKR will never be less than normal. Reframing may stretch the period of CKR by up to 90%, and either CKR Pulse Width HIGH or Pulse Width LOW may be stretched, depending on when reframe occurs.

The REFCLK input provides a byte-rate reference frequency to improve PLL acquisition time and limit unlocked frequency excursions of the CKR when no data is present at the serial inputs. The frequency of REFCLK is required to be within ±0.1% of the frequency of the clock that drives the transmitter CKW pin.

Framer

Framer logic checks the incoming bit stream for the pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as a Special Character Comma (K28.5). When it is found, the free-running bit counter in the Clock Synchronization block is synchronously reset to its initial state, thus framing the data correctly on the correct byte boundaries.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a K28.5, and thus cause an erroneous data-framing error. The RF input prevents this by inhibiting reframing during times when normal message data is present. When RF is held LOW, the HOTLink receiver will deserialize the incoming data without trying to reframe the data to incoming patterns. When RF rises, $\overline{RDY}$ will be inhibited until a K28.5 has been detected, after which $\overline{RDY}$ will resume its normal function. While RF is HIGH, it is possible that an error could cause misframing, after which all data will be corrupted. Likewise, a K28.7 followed by D11.x, D20.x, or an SVS (C0.7) followed by D11.x will create alias K28.5 characters and cause erroneous framing. These sequences must be avoided while RF is HIGH.

If RF remains HIGH for greater than 2048 bytes, the framer converts to double-byte framing, requiring two K28.5 characters aligned on the same byte boundary within 5 bytes in order to reframe. Double-byte framing greatly reduces the possibility of erroneously reframing to an aliased K28.5 character.

Shifter

The Shifter accepts serial inputs from the Serial Data inputs one bit at a time, as clocked by the Clock Synchronization logic. Data is transferred to the Framer on each bit, and to the Decode register once per byte.

Decode Register

The Decode register accepts data from the Shifter once per byte as determined by the logic in the Clock Synchronization block. It is presented to the Decoder and held until it is transferred to the output latch.

Decoder

Parallel data is transformed from ANSI-specified X3.230 8B/10B codes back to "raw data" in the Decoder. This block uses the standard decoder patterns shown in the Valid Data Characters and Valid Special Character Codes and Sequences sections of this datasheet. Data patterns are signaled by a LOW on the SC/$\overline{D}$ output and Special Character patterns are signaled by a HIGH on the SC/$\overline{D}$ output. Unused patterns or disparity errors are signaled as errors by a HIGH on the RVS output and by specific Special Character codes.

Output Register

The Output register holds the recovered data (Q_{0-7}, SC/$\overline{D}$, and RVS) and aligns it with the recovered byte clock (CKR). This synchronization insures proper timing to match a FIFO interface or other logic that requires glitch free and specified output behavior. Outputs change synchronously with the rising edge of CKR.

In BIST mode, this register becomes the signature pattern generator and checker by logically converting itself into a Linear Feedback Shift Register (LFSR) pattern generator. When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized, it checks each byte in the Decoder with each byte generated by the LFSR and shows errors at RVS. Patterns generated by the LFSR are compared after being buffered to the output pins and then fed back to the comparators, allowing test of the entire receive function.

In BIST mode, the LFSR is initialized by the first occurrence of the transmitter BIST loop start code D0.0 (D0.0 is sent only once per BIST loop). Once the BIST loop has been started, RVS will be HIGH for pattern mismatches between the received sequence and the internally generated sequence. Code rule violations or running disparity errors that occur as part of the BIST loop will not cause an error indication. $\overline{RDY}$ will pulse HIGH once per BIST loop and can be used to check test pattern progress. The receiver BIST generator can be reinitialized by leaving and re-entering BIST mode.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic for the decoder. Test logic is discussed in more detail in the CY7B933 HOTLink Receiver Operating Mode Description.

CY7B923/CY7B933 Electrical Characteristics Over the Operating Range[1]

Parameter	Description	Test Conditions		Min.	Max.	Unit
TTL OUTs, CY7B923: $\overline{RP}$; CY7B933: Q_{0-7}, SC/$\overline{D}$, RVS, $\overline{RDY}$, CKR, SO						
V_{OHT}	Output HIGH Voltage	I_{OH} = − 2 mA		2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA			0.45	V
I_{OST}	Output Short Circuit Current	V_{OUT} =0V[2]		−15	− 90	mA
TTL INs, CY7B923: D_{0-7}, SC/$\overline{D}$, SVS, $\overline{ENA}$, $\overline{ENN}$, CKW, FOTO, BISTEN; CY7B933: RF, REFCLK, $\overline{BISTEN}$						
V_{IHT}	Input HIGH Voltage		Com'l & Mil	2.0	V_{CC}	V
			Mil (CKW and FOTO, only) .	2.2	V_{CC}	V
V_{ILT}	Input LOW Voltage			− 0.5	0.8	V
I_{IHT}	Input HIGH Current	V_{IN} = V_{CC}		− 10	+10	µA
I_{ILT}	Input LOW Current	V_{IN} = 0.0V			− 500	µA
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA−, OUTB+, OUTB−, OUTC+, OUTC−						
V_{OHE}	Output HIGH Voltage (V_{CC} referenced)	Load = 50 Ω to V_{CC} − 2V	Com'l	V_{CC}−1.03	V_{CC}−0.83	V
			Mil	V_{CC}−1.05	V_{CC}−0.83	V
V_{OLE}	Output LOW Voltage (V_{CC} referenced)	Load = 50 Ω to V_{CC} − 2V	Com'l	V_{CC}−1.86	V_{CC}−1.62	V
			Mil	V_{CC}−1.96	V_{CC}−1.62	V
V_{ODIF}	Output Differential Voltage |(OUT+) − (OUT−)|	Load = 50 ohms to V_{CC} − 2V		0.6		V
Receiver PECL-Compatible Input Pins: A/$\overline{B}$, SI, INB						
V_{IHE}	Input HIGH Voltage		Com'l	V_{CC}−1.165	V_{CC}	V
			Mil	V_{CC}−1.14	V_{CC}	V
V_{ILE}	Input LOW Voltage		Com'l	2.0	V_{CC}−1.475	V
			Mil	2.0	V_{CC}−1.50	V
I_{IHE}[3]	Input HIGH Current	V_{IN} = V_{IHE} Max.			+500	µA
I_{ILE}[3]	Input LOW Current	V_{IN} = V_{ILE} Min.		+0.5		µA
Differential Line Receiver Input Pins: INA+, INA−, INB+, INB−						
V_{DIFF}	Input Differential Voltage |(IN+) − (IN−)|			50		mV
V_{IHH}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILL}	Lowest Input LOW Voltage			2.0		V
I_{IHH}	Input HIGH Current	V_{IN} = V_{IHH} Max.			750	µA
I_{ILL}[4]	Input LOW Current	V_{IN} = V_{ILL} Min.		−200		µA
Miscellaneous				**Typ.**	**Max.**	
I_{CCT}[5]	Transmitter Power Supply Current	Freq. = Max.	Com'l	65	85	mA
			Mil	75	95	mA
I_{CCR}[6]	Receiver Power Supply Current	Freq. = Max.	Com'l	120	155	mA
			Mil	135	160	mA

Notes:

1. See the last page of this specification for Group A subgroup testing information.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Applies to A/$\overline{B}$ only.
4. Input currents are always positive at all voltages above V_{CC}/2.
5. Maximum I_{CCT} is measured with V_{CC} = Max., one PECL output pair loaded with 50 ohms to V_{CC} − 2.0V, and other PECL outputs tied to V_{CC}. Typical I_{CCT} is measured with V_{CC} = 5.0V, T_A = 25°C, one output pair loaded with 50 ohms to V_{CC} − 2.0V, others tied to V_{CC}, $\overline{BISTEN}$ = LOW. I_{CCT} includes current into V_{CCQ} (pin 9 and pin 22) only. Current into V_{CCN} is determined by PECL load currents, typically 30 mA with 50 ohms to V_{CC} − 2.0V. Each additional enabled PECL pair adds 5 mA to I_{CCT} and an additional load current to V_{CCN} as described. When calculating the contribution of PECL load currents to chip power dissipation, the output load current should be multiplied by 1V instead of V_{CC}.
6. Maximum I_{CCR} is measured with V_{CC} = Max., RF = LOW, and outputs unloaded. Typical I_{CCR} is measured with V_{CC} = 5.0V, T_A = 25°C, RF = LOW, $\overline{BISTEN}$ = LOW, and outputs unloaded. I_{CCR} includes current into V_{CCQ} (pins 21 and 24). Current into V_{CCN} (pin 9) is determined by the total TTL output buffer quiescent current plus the sum of all the load currents for each output pin. The total buffer quiescent current is 10mA max., and max. TTL load current for each output pin can be calculated as follows:

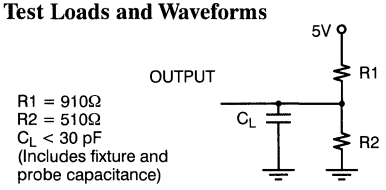
$$\frac{I_{CCN}}{TTLPin} = \left[\frac{0.95 + (V_{CCN} - 5) * 0.3}{R_L} + C_L * \left(\frac{V_{CCN}}{2} + 1.5\right) * F_{pin}\right] * 1.1$$

Where R_L=equivalent load resistance, C_L=capacitive load, and F_{pin}=frequency in MHz of data on pin. A derating factor of 1.1 has been included to account for worst process corner and temperature condition.

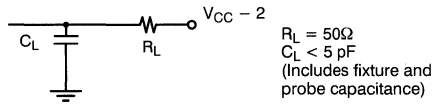
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 5.0V$	10	pF

AC Test Loads and Waveforms

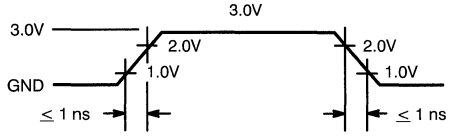


(a) TTL AC Test Load[8]



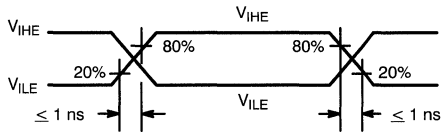
(b) PECL AC Test Load[8]

B923-8



(c) TTL Input Test Waveform

B923-9



(d) PECL Input Test Waveform

B923-10

Transmitter Switching Characteristics Over the Operating Range[1]

Parameter	Description	7B923 Min.	7B923 Max.	Unit
t_{CKW}	Write Clock Cycle	30.3	62.5	ns
t_B	Bit Time[9]	3.03	6.25	ns
t_{CPWH}	CKW Pulse Width HIGH	6.5		ns
t_{CPWL}	CKW Pulse Width LOW	6.5		ns
t_{SD}	Data Set-Up Time[10]	5		ns
t_{HD}	Data Hold Time[10]	0		ns
t_{SENP}	Enable Set-Up Time (to insure correct $\overline{RP}$)[11]	$6t_B + 8$		ns
t_{HENP}	Enable Hold Time (to insure correct $\overline{RP}$)[11]	0		ns
t_{PDR}	Read Pulse Rise Alignment[12]	−4	2	ns
t_{PPWH}	Read Pulse HIGH[12]	$4t_B-3$		ns
t_{PDF}	Read Pulse Fall Alignment[12]	$6t_B-3$		ns
t_{RISE}	PECL Output Rise Time 20–80% (PECL Test Load)[7]		1.2	ns
t_{FALL}	PECL Output Fall Time 80–20% (PECL Test Load)[7]		1.2	ns
t_{DJ}	Deterministic Jitter (peak-peak)[7, 13]		35	ps
t_{RJ}	Random Jitter (peak-peak)[7, 14]		175	ps
	Random Jitter (σ)[7, 14]		20	ps

Notes:

7. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
8. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
9. Transmitter t_B is calculated as $t_{CKW}/10$. The byte rate is one tenth of the bit rate.
10. Data includes D_{0-7}, SC/$\overline{D}$, SVS, $\overline{ENA}$, $\overline{ENN}$, and $\overline{BISTEN}$. t_{SD} and t_{HD} minimum timing assures correct data load on rising edge of CKW, but not $\overline{RP}$ function or timing.
11. t_{SENP} and t_{HENP} timing insures correct $\overline{RP}$ function and correct data load on the rising edge of CKW.
12. Loading on $\overline{RP}$ is the standard TTL test load shown in part (a) of AC Test Loads and Waveforms except C_L = 15 pF.
13. While sending continuous K28.5s, $\overline{Rp}$ unloaded, outputs loaded to 50Ω to $V_{CC}-2.0V$, over the operating range.
14. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to CKW input, over the operating range.

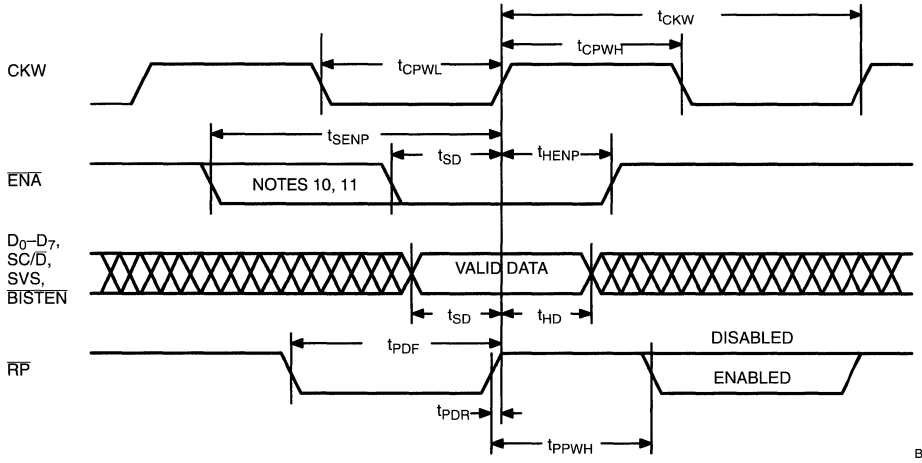
Receiver Switching Characteristics Over the Operating Range[1]

Parameter	Description	7B933		Unit
		Min.	Max.	
t_{CKR}	Read Clock Period (No Serial Data Input), REFCLK as Reference[15]	−1	+1	%
t_B	Bit Time[16]	3.03	6.25	ns
t_{CPRH}	Read Clock Pulse HIGH	$5t_B-3$		ns
t_{CPRL}	Read Clock Pulse LOW	$5t_B-3$		ns
t_{RH}	$\overline{RDY}$ Hold Time	t_B-3		ns
t_{PRF}	$\overline{RDY}$ Pulse Fall to CKR Rise	$5t_B-3$		ns
t_{PRH}	$\overline{RDY}$ Pulse Width HIGH	$4t_B-3$		ns
t_A	Data Access Time[17, 18]	$2t_B-2$	$2t_B+4$	ns
t_{ROH}	Data Hold Time[17, 18]	t_B-3		ns
t_H	Data Hold Time from CKR Rise [17, 18]	$2t_B-3$		ns
t_{CKX}	REFCLK Clock Period Referenced to CKW of Transmitter[19]	−0.1	+0.1	%
t_{CPXH}	REFCLK Clock Pulse HIGH	6.5		ns
t_{CPXL}	REFCLK Clock Pulse LOW	6.5		ns
t_{DS}	Propagation Delay SI to SO (note PECL and TTL thresholds)[20]		20	ns
t_{SA}	Static Alignment[7, 21]		100	ps
t_{EFW}	Error Free Window[7, 22]	$0.9t_B$		

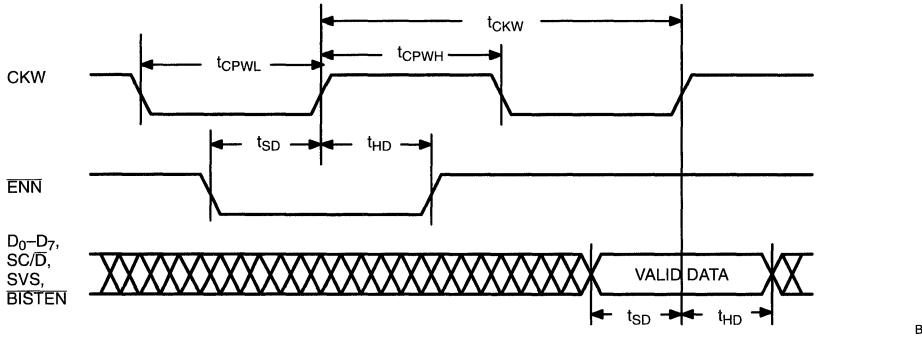
Notes:

15. The period of t_{CKR} will match the period of the transmitter CKW when the receiver is receiving serial data. When data is interrupted, CKR may drift to one of the range limits above.
16. Receiver t_B is calculated as $t_{CKR}/10$ if no data is being received, or $t_{CKW}/10$ if data is being received. See note 9.
17. Data includes Q_{0-7}, SC/$\overline{D}$, and RVS.
18. t_A, t_{ROH}, and t_H specifications are only valid if all outputs (CKR, $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS) are loaded with similar DC and AC loads.
19. REFCLK has no phase or frequency relationship with CKR and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within 0.1% of the transmitter CKW frequency, necessitating a ±500-PPM crystal.
20. The PECL switching threshold is the midpoint between the PECL–V_{OH}, and V_{OL} specification (approximately V_{CC} – 1.35V). The TTL switching threshold is 1.5V.
21. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a byte error occurs.
22. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.

Switching Waveforms for the CY7B923 HOTLink Transmitter

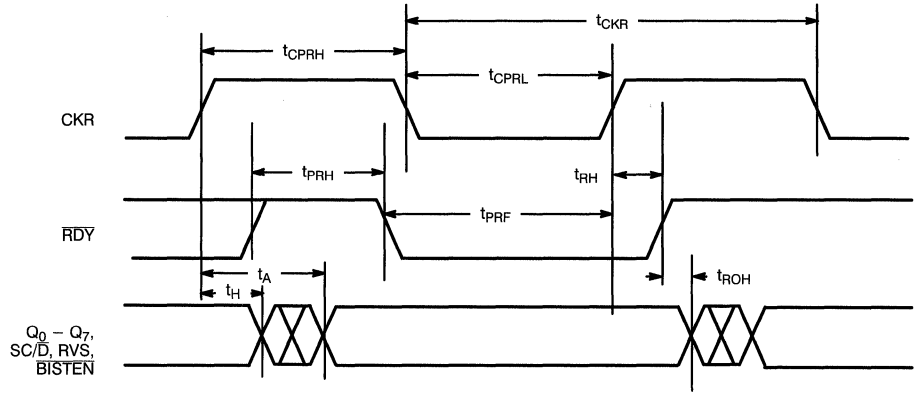


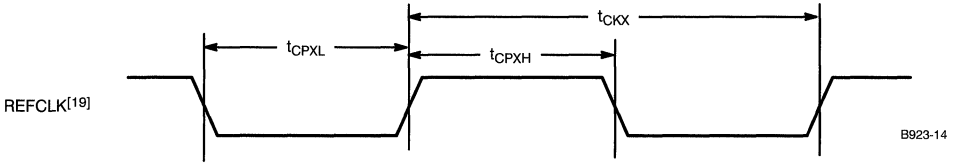
B923-11

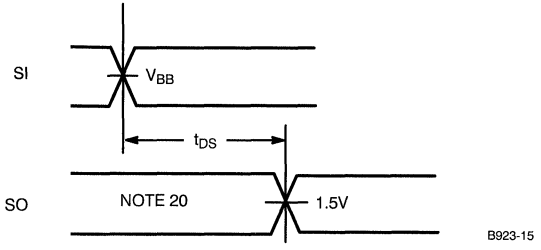


B923-12

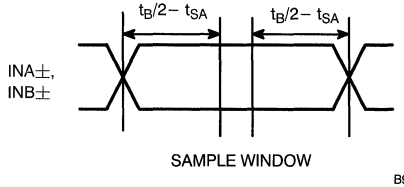
Switching Waveforms for the CY7B933 HOTLink Receiver



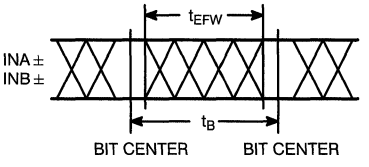




Static Alignment



Error-Free Window



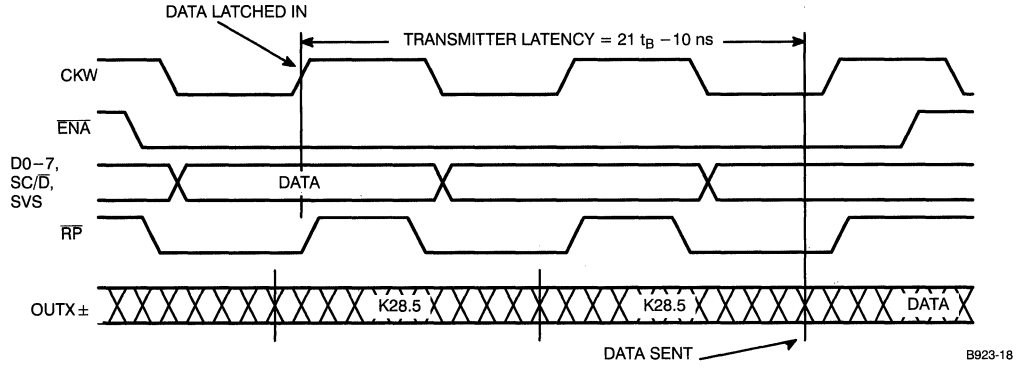


Figure 2. CY7B923 Transmitter Data Pipeline

HOTLink CY7B923 Transmitter and CY7B933 Receiver Operation

The CY7B923 Transmitter operating with the CY7B933 Receiver form a general purpose data communications subsystem capable of transporting user data at up to 33Mbytes per second over several types of serial interface media. *Figure 2* illustrates the flow of data through the HOTLink CY7B923 transmitter pipeline. Data is latched into the transmitter on the rising edge of CKW when enabled by $\overline{ENA}$ or $\overline{ENN}$. $\overline{RP}$ is asserted LOW with a 60% LOW/40% HIGH duty cycle when $\overline{ENA}$ is LOW. $\overline{RP}$ may be used as a read strobe for accessing data stored in a FIFO. The parallel data flows through the encoder and is then shifted out of the OUTx± PECL drivers. The bit-rate clock is generated internally from a multiply-by-ten PLL clock generator. The latency through the transmitter is approximately $21t_B$ − 10 ns over the operating range. A more complete description is found in the section *CY7B923 HOTLink Transmitter Operating Mode Description*.

Figure 3 illustrates the data flow through the HOTLink CY7B933 receiver pipeline. Serial data is sampled by the receiver on the INx± inputs. The receiver PLL locks onto the serial bit stream and generates an internal bit rate clock. The bit stream is deserialized, decoded and then presented at the parallel output pins. A byte rate clock (bit clock ÷ 10) sycnchronous with the parallel data is presented at the CKR pin. The $\overline{RDY}$ pin will be asserted to LOW to indicate that data or control characters are present on the outputs. $\overline{RDY}$ will not be asserted LOW in a field of K28.5s except for any single K28.5 or the last one in a continuous series of K28.5's. The latency through the receiver is approximately $24t_B$ + 10 ns over the operating range. A more complete description of the receiver is in the section *CY7B933 HOTLink Receiver Operating Mode Description*.

The HOTLink Receiver has a built−in byte framer that synchronizes the Receiver pipeline with incomming SYNC (K28.5) characters. *Figure 4* illustrates the HOTLink CY7B933 Receiver framing operation. The Framer is enabled when the RF pin is asserted HIGH. RF is latched into the receiver on the falling edge of CKR. The framer looks for K28.5 characters embedded in the serial data stream. When a K28.5 is found, the framer sets the parallel byte boundary for subsequent data to the the K28.5 boundary. While the framer is enabled, the $\overline{RDY}$ pin indicates the status of the framing operation.

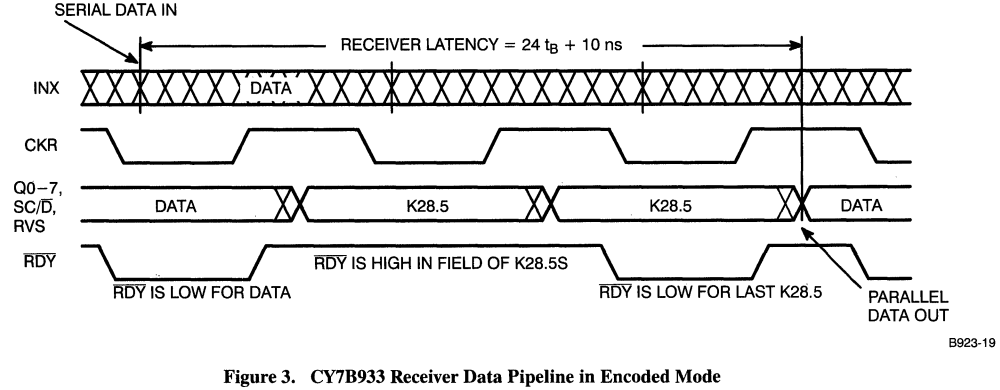


Figure 3. CY7B933 Receiver Data Pipeline in Encoded Mode

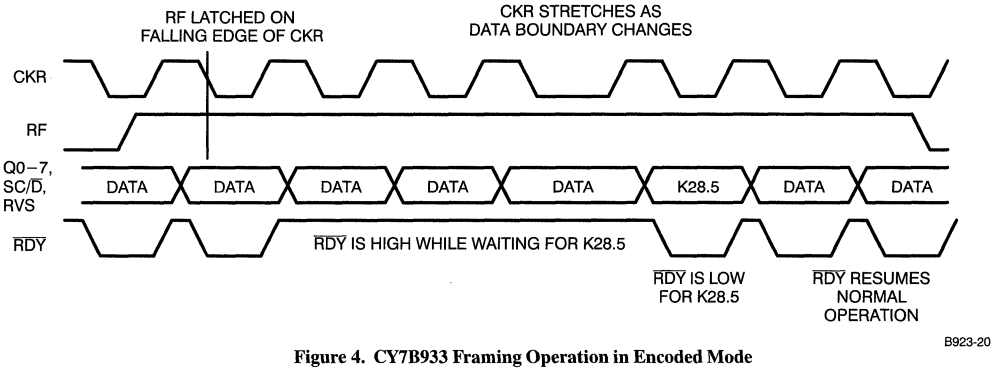


Figure 4. CY7B933 Framing Operation in Encoded Mode

When the RF pin is asserted HIGH, $\overline{RDY}$ leaves it normal mode of operation and is asserted HIGH while the framer searches the data stream for a K28.5 character. After the framer has synchronized to a K28.5 character, the Receiver will assert the $\overline{RDY}$ pin LOW when the K28.5 character is present at the parallel output. The $\overline{RDY}$ pin will then resume its normal operation as dictated by the $\overline{MODE}$ and $\overline{BISTEN}$ pins.

The normal operation of the $\overline{RDY}$ pin in encoded mode is to signal when parallel data is present at the output pins by pulsing LOW with a 60% LOW/40% HIGH duty cycle. $\overline{RDY}$ does not pulse LOW in a field of K28.5 characters; however, $\overline{RDY}$ does pulse LOW for the last K28.5 character in the field or for any single K28.5. In unencoded mode, the normal operation of the $\overline{RDY}$ pin is to signal when any K28.5 is at the parallel output pins.

The Transmitter and Receiver parallel interface timing and functionality can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by appropriately connecting signals (See *Figure 5*). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

The HOTLink Transmitter and Receiver serial interface provides a seamless interface to various types of media. A minimal number of external components are needed to properly terminate transmission lines and provide PECL loads. For proper power supply decoupling, a single 0.01 µF for each device is all that is required to bypass the V_{CC} and GND pins. *Figure 6* illustrates a HOTLink Transmitter and Receiver interface to fiber optic and copper media. More information on interfacing HOTLink to various media can be found in the *HOTLink Design Considerations* application note.

CY7B923 HOTLink Transmitter Operating Mode Description

In normal operation, the Transmitter can operate in either of two modes. The Encoded mode allows a user to send and receive eight (8) bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed in an external protocol controller.

In either mode, data is loaded into the Input register of the Transmitter on the rising edge of CKW. The input timing and functional response of the Transmitter input can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by an appropriate connection of input signals (See *Figure 5*). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

Encoded Mode Operation

In Encoded mode the input data is interpreted as eight bits of data ($D_0 - D_7$), a context control bit (SC/$\overline{D}$), and a system diagnostic input bit (SVS). If the context of the data is to be normal message data, the SC/$\overline{D}$ input should be LOW, and the data should be encoded using the valid data character set described in the Valid Data Characters section of this datasheet. If the context of the data is to be control or protocol information, the SC/$\overline{D}$ input will be HIGH, and the data will be encoded using the valid special character set described in the Valid Special Character Codes and Sequences section. Special characters include all protocol characters necessary to encode packets for Fibre Channel, ESCON, proprietary systems, and diagnostic purposes.

The diagnostic characters and sequences available as Special Characters include those for Fibre Channel link testing, as well as codes to be used for testing system response to link errors and timing. A Violation symbol can be explicitly sent as part of a user data packet (i.e., send C0.7; D_{7-0} = 111 00000 and SC/$\overline{D}$ = 1), or it can be sent in response to an external system using the SVS input. This will allow system diagnostic logic to evaluate the errors in an unambiguous manner, and will not require any modification to the transmission interface to force transmission errors for testing purposes.

Bypass Mode Operation

In Bypass mode the input data is interpreted as ten (10) bits (D_{b-h}), SC/$\overline{D}$ (D_a), and SVS (D_j) of pre-encoded transmission data to be serialized and sent over the link. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per 10 bit byte), and that it be compatible with the transmission media.

Data loaded into the Input register on the rising edge of CKW will be loaded into the Shifter on the subsequent rising edges of CKW. It will then be shifted to the outputs one bit at a time using the internal clock generated by the clock generator. The first bit of the transmission character (D_a) will appear at the output (OUTA±, OUTB±, and OUTC±) after the next CKW edge.

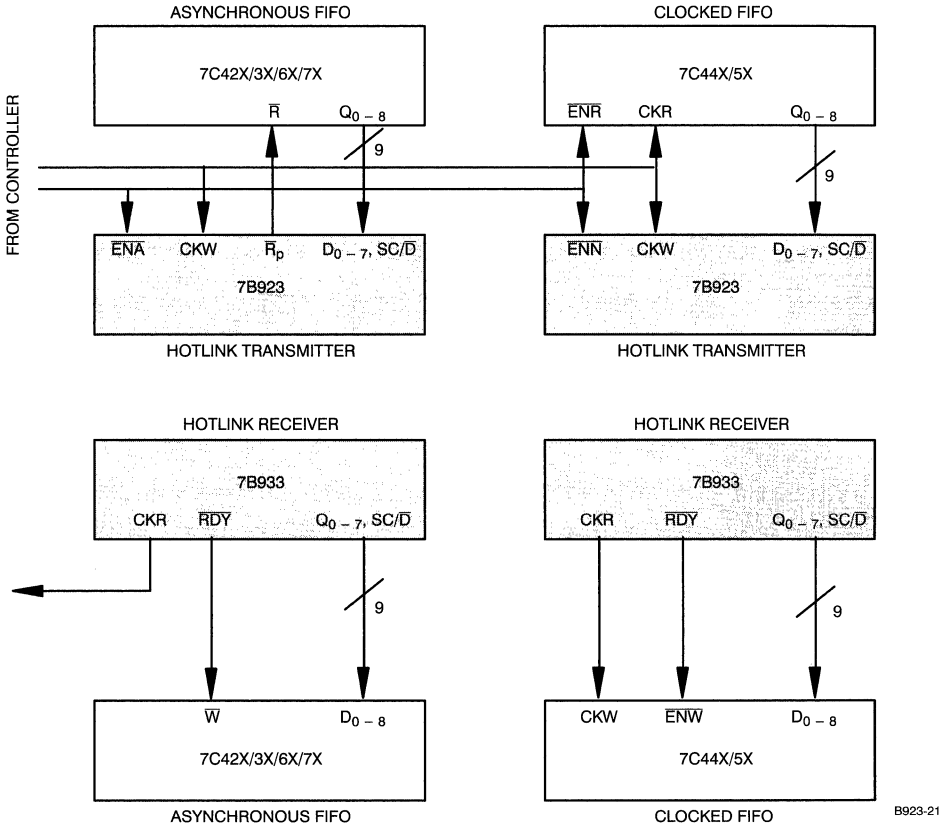


Figure 5. Seamless FIFO Interface

While in either the Encoded mode or Bypass mode, if a CKW edge arrives when the inputs are not enabled ($\overline{ENA}$ and $\overline{ENN}$ both HIGH), the Encoder will insert a pad character K28.5 (e.g., C5.0) to maintain proper link synchronization (in Bypass mode the proper sense of running disparity cannot be guaranteed for the first pad character, but is correct for all pad characters that follow). This automatic insertion of pad characters can be inhibited by insuring that the Transmitter is always enabled (i.e., $\overline{ENA}$ or $\overline{ENN}$ is hardwired LOW).

PECL Output Functional and Connection Options

The three pairs of PECL outputs all contain the same information and are intended for use in systems with multiple connections. Each output pair may be connected to a different serial media, each of which may be a different length, link type, or interface technology. For systems that do not require all three output pairs, the unused pairs should be wired to V_{CC} to minimize the power dissipated by the output circuit, and to minimize unwanted noise generation. An internal voltage comparator detects when an output differential pair is wired to V_{CC}, causing the current source for that pair to be disabled. This results in a power savings of around 5 mA for each unused pair.

In systems that require the outputs to be shut off during some periods when link transmission is prohibited (e.g., for laser safety functions), the FOTO input can be asserted. While it is possible to insure that the output state of the PECL drivers is LOW (i.e., light is off) by sending all 0's in Bypass mode, it is often inconvenient to insert this level of control into the data transmission channel, and it is impossible in Encoded mode. FOTO is provided to simplify and augment this control function (typically found in laser-based transmission systems). FOTO will force OUTA+ and OUTB+ to go LOW, OUTA− and OUTB− to go HIGH, while allowing OUTC± to continue to function normally (OUTC is typically used as a diagnostic feedback and cannot be disabled). This separation of function allows various system configurations without undue load on the control function or data channel logic.

Transmitter Serial Data Characteristics

The CY7B923 HOTLink Transmitter serial output conforms to the requirements of the Fibre Channel specification. The serial data output is controlled by an internal Phase-Locked Loop that multiplies the frequency of CKW by ten (10) to maintain the proper bit clock frequency. The jitter characteristics (including both PLL and logic components) are shown below:

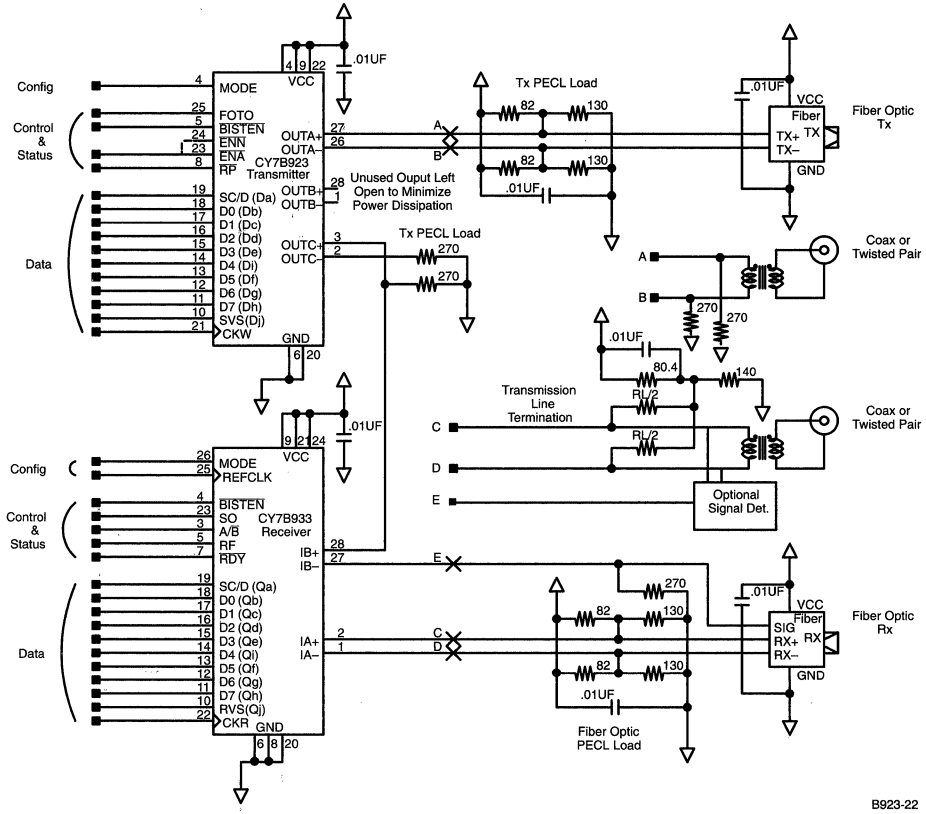


Figure 6. HOTLink Connection Diagram

Deterministic Jitter (D_j) < 35 ps (peak-peak). Typically measured while sending a continuous K28.5 (C5.0).

Random Jitter (R_j) < 175 ps (peak-peak). Typically measured while sending a continuous K28.7 (C7.0).

Transmitter Test Mode Description

The CY7B923 Transmitter offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver, and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in *Figure 7*.

BIST Mode

BIST mode functions as follows:

1. Set $\overline{\text{BISTEN}}$ LOW to begin test pattern generation. Transmitter begins sending bit rate ...1010...
2. Set either $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$ LOW to begin pattern sequence generation (use of the Enable pin not being used for normal FIFO or system interface can minimize logic delays between the controller and transmitter).
3. Allow the Transmitter to run through several BIST loops or until the Receiver test is complete. $\overline{\text{RP}}$ will pulse LOW once per BIST loop, and can be used by an external counter to monitor the number of test pattern loops.
4. When testing is completed, set $\overline{\text{BISTEN}}$ HIGH and $\overline{\text{ENA}}$ and $\overline{\text{ENN}}$ HIGH and resume normal function.

Note: It may be advisable to send violation characters to test the RVS output in the Receiver. This can be done by explicitly sending a violation with the SVS input, or allowing the transmitter BIST loop to run while the Receiver runs in normal mode. The BIST loop includes deliberate violation symbols and will adequately test the RVS function.

BIST mode is intended to check the entire function of the Transmitter (except the Transmitter input pins and the bypass function in the Encoder), the serial link, and the Receiver. It augments normal factory ATE testing and provides the designer with a rigorous test mechanism to check the link transmission system without requiring any significant system overhead.

While in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. MODE = HIGH and $\overline{\text{BISTEN}}$ = LOW causes the Transmitter to switch to Encoded mode and begin sending the BIST pattern, as if MODE = LOW. When $\overline{\text{BISTEN}}$ returns

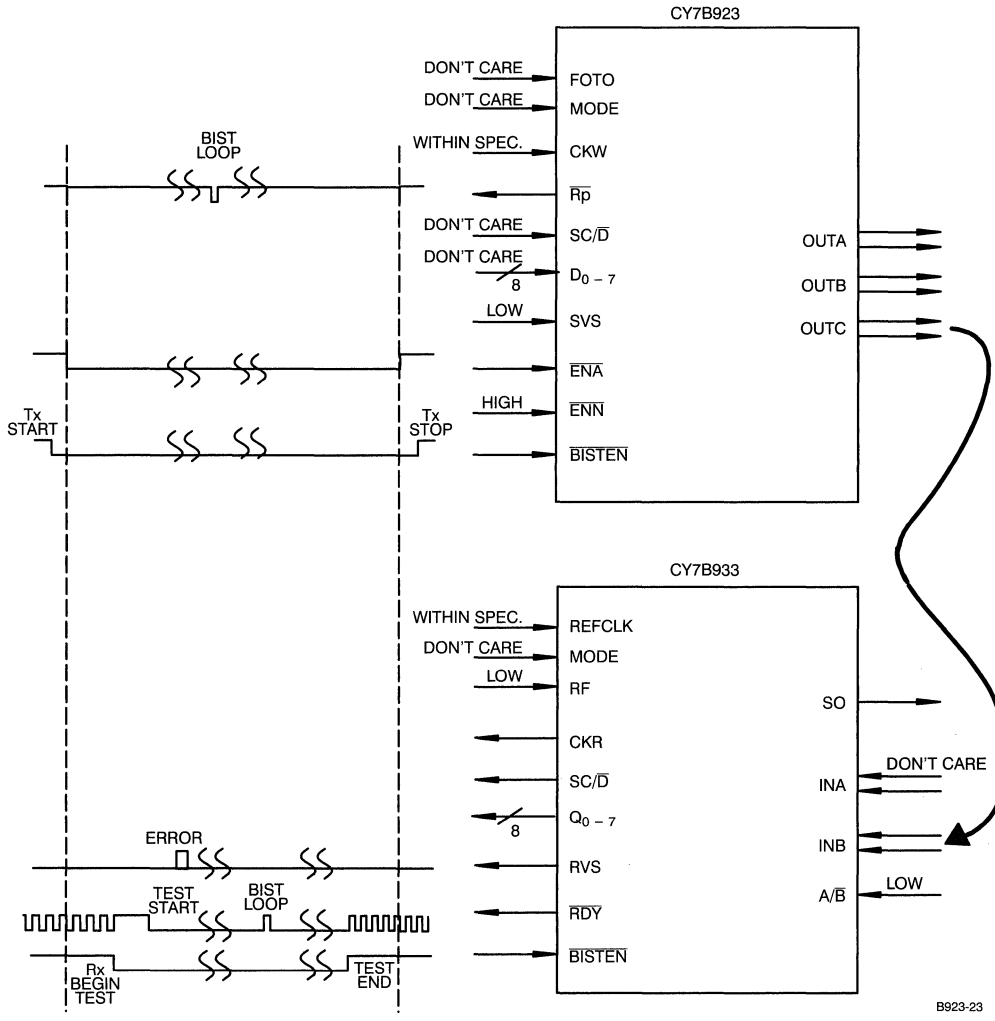


Figure 7. Built-In Self-Test Illustration

to HIGH, the Transmitter resumes normal Bypass operation. In Test mode the BIST function works as in the Normal mode. For more information on BIST, consult the "HOTLink Built-In Self-Test" Application Note.

Test Mode

The MODE input pin selects between three transmitter functional modes. When wired to V_{CC}, the $D_{(a-j)}$ inputs bypass the Encoder and load directly from the Input register into the Shifter. When wired to GND, the inputs D_{0-7}, SVS, and SC/$\overline{D}$ are encoded using the Fibre Channel 8B/10B codes and sequences (shown at the end of this datasheet). Since the Transmitter is usually hard wired to Encoded or Bypass mode and not switched between them, a third function is provided for the MODE pin. Test mode is selected by floating the MODE pin (internal resistors hold the MODE pin at $V_{CC}/2$). Test mode is used for factory or incoming device test.

Test mode causes the Transmitter to function in its Encoded mode, but with OutA+/OutB+ (used as a differential test clock input) as the bit rate clock input instead of the internal PLL-generated bit clock. In this mode, inputs are clocked by CKW and transfers between the Input register and Shifter are timed by the internal counters. The bit-clock and CKW must maintain a fixed phase and divide-by-ten ratio. The phase and pulse width of $\overline{RP}$ are controlled by phases of the bit counter (PLL feedback counter) as in Normal mode. Input and output patterns can be synchronized with internal logic by observing the state of $\overline{RP}$ or the device can be

initialized to match an ATE test pattern using the following technique:

1. With the MODE pin either HIGH or LOW, stop CKW and bit-clock.
2. Force the MODE pin to MID (open or $V_{CC}/2$) while the clocks are stopped.
3. Start the bit-clock and let it run for at least 2 cycles.
4. Start the CKW clock at the bit-clock/10 rate.

Test mode is intended to allow logical, DC, and AC testing of the Transmitter without requiring that the tester check output data patterns at the bit rate, or accommodate the PLL lock, tracking, and frequency range characteristics that are required when the HOTLink part operates in its normal mode. To use OutA+/OutB+ as the test clock input, the FOTO input is held HIGH while in Test mode. This forces the two outputs to go to an "PECL LOW," which can be ignored while the test system creates a differential input signal at some higher voltage.

CY7B933 HOTLink Receiver Operating Mode Description

In normal user operation, the Receiver can operate in either of two modes. The Encoded mode allows a user system to send and receive 8-bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed by an external protocol controller.

In either mode, serial data is received at one of the differential line receiver inputs and routed to the Shifter and the Clock Synchronization. The PLL in the Clock Synchronizer aligns the internally generated bit rate clock with the incoming data stream and clocks the data into the shifter. At the end of a byte time (ten bit times), the data accumulated in the shifter is transferred to the Decode register.

To properly align the incoming bit stream to the intended byte boundaries, the bit counter in the Clock Synchronizer must be initialized. The Framer logic block checks the incoming bit stream for the unique pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as "Special Character Comma" (K28.5). Once K28.5 is found, the free running bit counter in the Clock Synchronizer block is synchronously reset to its initial state, thus "framing" the data to the correct byte boundaries.

Since noise-induced errors can cause the incoming data to be corrupted, and since many combinations of error and legal data can create an alias K28.5, an option is included to disable resynchronization of the bit counter. The Framer will be inhibited when the RF input is held LOW. When RF rises, $\overline{RDY}$ will be inhibited until a K28.5 has been detected, and $\overline{RDY}$ will resume its normal function. Data will continue to flow through the Receiver while $\overline{RDY}$ is inhibited.

Encoded Mode Operation

In Encoded mode the serial input data is decoded into eight bits of data ($Q_0 - Q_7$), a context control bit (SC/$\overline{D}$), and a system diagnostic output bit (RVS). If the pattern in the Decode register is found in the Valid Data Characters table, the context of the data is decoded as normal message data and the SC/$\overline{D}$ output will be LOW. If the incoming bit pattern is found in the Valid Special Character Codes and Sequences table, it is interpreted as "control" or "protocol information," and the SC/$\overline{D}$ output will be HIGH. Special characters include all protocol characters defined for use in packets for Fibre Channel, ESCON, and other proprietary and diagnostic purposes.

The Violation symbol that can be explicitly sent as part of a user data packet (i.e., Transmitter sending C0.7; D_{7-0} = 111 00000 and SC/$\overline{D}$ = 1; or SVS = 1) will be decoded and indicated in exactly the same way as a noise-induced error in the transmission link. This function will allow system diagnostics to evaluate the error in an unambiguous manner, and will not require any modification to the receiver data interface for error-testing purposes.

Bypass Mode Operation

In Bypass mode the serial input data is not decoded, and is transferred directly from the Decode register to the Output register's 10 bits ($Q_{(a-j)}$). It is assumed that the data has been pre-encoded prior to transmission, and will be decoded in subsequent logic external to HOTLink. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per 10 bit byte) and that it be compatible with the transmission media.

The framer function in Bypass mode is identical to Encoded mode, so a K28.5 pattern can still be used to re-frame the serial bit stream.

Parallel Output Function

The 10 outputs (Q_{0-7}, SC/$\overline{D}$, and RVS) all transition simultaneously, and are aligned with $\overline{RDY}$ and CKR with timing allowances to interface directly with either an asynchronous FIFO or a clocked FIFO. Typical FIFO connections are shown in *Figure 5*.

Data outputs can be clocked into the system using either the rising or falling edge of CKR, or the rising or falling edge of $\overline{RDY}$. If CKR is used, $\overline{RDY}$ can be used as an enable for the receiving logic. A LOW pulse on $\overline{RDY}$ shows that new data has been received and is ready to be delivered. The signal on $\overline{RDY}$ is a 60%–LOW duty cycle byte-rate pulse train suitable for the write pulse in asynchronous FIFOs such as the CY7C42X, or the enable write input on Clocked FIFOs such as the CY7C44X. HIGH on $\overline{RDY}$ shows that the received data appearing at the outputs is the null character (normally inserted by the transmitter as a pad between data inputs) and should be ignored.

When the Transmitter is disabled it will continuously send pad characters (K28.5). To assure that the receive FIFO will not be overfilled with these dummy bytes, the $\overline{RDY}$ pulse output is inhibited during fill strings. Data at the Q_{0-7} outputs will reflect the correct received data, but will not appear to change, since a string of K28.5s all are decoded as Q_{7-0} =000 00101 and SC/$\overline{D}$ = 1 (C5.0). When new data appears (not K28.5), the $\overline{RDY}$ output will resume normal function. The "last" K28.5 will be accompanied by a normal $\overline{RDY}$ pulse.

Fill characters are defined as any K28.5 followed by another K28.5. All fill characters will not cause $\overline{RDY}$ to pulse. Any K28.5 followed by any other character (including violation or illegal characters) will be interpreted as usable data and will cause $\overline{RDY}$ to pulse.

As noted above, $\overline{RDY}$ can also be used as an indication of correct framing of received data. While the Receiver is awaiting receipt of a K28.5 with RF HIGH, the $\overline{RDY}$ outputs will be inhibited. When $\overline{RDY}$ resumes, the received data will be properly framed and will be decoded correctly. In Bypass mode with RF HIGH, $\overline{RDY}$ will pulse once for each K28.5 received. For more information on the $\overline{RDY}$ pin, consult the "HOTLink CY7B933 $\overline{RDY}$ Pin Description" application note.

Code rule violations and reception errors will be indicated as follows:

	RVS	SC/$\overline{D}$	Qouts	Name
1. Good Data code received with good Running Disparity (RD)	0	0	00–FF	D0.0–31.7
2. Good Special Character code received with good RD	0	1	00–0B	C0.0–11.0
3. K28.7 immediately following K28.1 (ESCON Connect_SOF)	0	1	27	C7.1
4. K28.7 immediately following K28.5 (ESCON Passive_SOF)	0	1	47	C7.2
5. Unassigned code received	1	1	E0	C0.7
6. −K28.5+ received when RD was +	1	1	E1	C1.7
7. +K28.5− received when RD was −	1	1	E2	C2.7
8. Good code received with wrong RD	1	1	E4	C4.7

Receiver Serial Data Requirements

The CY7B933 HOTLink Receiver serial input capability conforms to the requirements of the Fibre Channel specification. The serial data input is tracked by an internal Phase-Locked Loop that is used to recover the clock phase and to extract the data from the serial bit stream. Jitter tolerance characteristics (including both PLL and logic component requirements) are shown below:

Deterministic Jitter tolerance (D_j) >40% of t_B. Typically measured while receiving data carried by a bandwidth-limited channel (e.g., a coaxial transmission line) while maintaining a Bit Error Rate (BER) $<10^{-12}$.

Random Jitter tolerance (R_j) > 90% of t_B. Typically measured while receiving data carried by a random-noise-limited channel (e.g., a fiber-optic transmission system with low light levels) while maintaining a Bit Error Rate (BER) $<10^{-12}$.

Total Jitter tolerance >90% of t_B. Total of $D_j + R_j$.

PLL-Acquisition time <500-bit times from worst-case phase or frequency change in the serial input data stream, to receiving data within BER objective of 10^{-12}. Stable power supplies within specifications, stable REFCLK input frequency and normal data framing protocols are assumed. Note: Acquisition time is measured from worst-case phase or frequency change to zero phase and frequency error. As a result of the receiver's wide jitter tolerance, valid data will appear at the receiver's outputs a few byte times after a worst-case phase change.

Receiver Test Mode Description

The CY7B933 Receiver offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in *Figure 7.*

BIST Mode

BIST Mode function is as follows:

1. Set $\overline{\text{BISTEN}}$ LOW to enable self-test generation and await $\overline{\text{RDY}}$ LOW indicating that the initialization code has been received.
2. Monitor RVS and check for any byte time with the pin HIGH to detect pattern mismatches. $\overline{\text{RDY}}$ will pulse HIGH once per BIST loop, and can be used by an external counter to monitor test pattern progress. Q_{0-7} and SC/$\overline{D}$ will show the expected pattern and may be useful for debug purposes.
3. When testing is completed, set $\overline{\text{BISTEN}}$ HIGH and resume normal function.

Note: A specific test of the RVS output may be required to assure an adequate test. To perform this test, it is only necessary to have the Transmitter send violation (SVS = HIGH) for a few bytes before beginning the BIST test sequence. Alternatively, the Receiver could enter BIST mode after the Transmitter has begun sending BIST loop data, or be removed before the Transmitter finishes sending BIST loops, each of which contain several deliberate violations and should cause RVS to pulse HIGH.

BIST mode is intended to check the entire function of the Transmitter, serial link, and Receiver. It augments normal factory ATE testing and provides the user system with a rigorous test mechanism to check the link transmission system, without requiring any significant system overhead.

When in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. MODE = HIGH and $\overline{\text{BISTEN}}$ = LOW causes the Receiver to switch to Encoded mode and begin checking the decoded received data of the BIST pattern, as if MODE = LOW. When $\overline{\text{BISTEN}}$ returns to HIGH, the Receiver resumes normal Bypass operation. In Test mode the BIST function works as in the normal mode.

Test Mode

The MODE input pin selects between three receiver functional modes. When wired to V_{CC}, the Shifter contents bypass the Decoder and go directly from the Decoder latch to the Q_{a-j} inputs of the Output latch. When wired to GND, the outputs are decoded using the 8B/10B codes shown at the end of this datasheet and become Q_{0-7}, RVS, and SC/$\overline{D}$. The third function is Test mode, used for factory or incoming device test. This mode can be selected by leaving the MODE pin open (internal circuitry forces the open pin to $V_{CC}/2$).

Test mode causes the Receiver to function in its Encoded mode, but with INB (INB+) as the bit rate Test clock instead of the Internal PLL generated bit clock. In this mode, transfers between the Shifter, Decoder register and Output register are controlled by their normal logic, but with an external bit rate clock instead of the PLL (the recovered bit clock). Internal logic and test pattern inputs can be synchronized by sending a SYNC pattern and allowing the Framer to align the logic to the bit stream. The flow is as follows:

1. Assert Test mode for several test clock cycles to establish normal counter sequence.
2. Assert RF to enable reframing.
3. Input a repeating sequence of bits representing K28.5 (Sync).
4. $\overline{\text{RDY}}$ falling shows the byte boundary established by the K28.5 input pattern.
5. Proceed with pattern, voltage and timing tests as is convenient for the test program and tester to be used.

(While in Test mode and in BIST mode with RF HIGH, the Q_{0-7}, RVS, and SC/$\overline{D}$ outputs reflect various internal logic states and not the received data.)

Test mode is intended to allow logical, DC, and AC testing of the Receiver without requiring that the tester generate input data at the bit rate or accommodate the PLL lock, tracking and frequency

range characteristics that are required when the part operates in its normal mode.

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character Comma) that assists a Receiver in achieving word alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation)

```
FC-2  45
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```
Data Byte Name  D5.2
                Bits: ABCDE FGH
                      10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
Bits: abcdei  fghj
      101001  0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and the SC/$\overline{D}$ pin is LOW) or a Special Character (c is set to K, and the SC/$\overline{D}$ pin is HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

Note: This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code" *IBM Journal of Research and Development*, 27, No. 5: 440–451 (September, 1983).

U.S. Patent 4,488,739. Peter A. Franaszek and Albert X. Widmer. "Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code" (December 4, 1984).

Fibre Channel Physical and Signaling Interface (dpANS X3.230–199X ANSI FC–PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22–7202).

8B/10B Transmission Code

The following information describes how the tables shall be used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit "a" shall be transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i shall be transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity ("Current RD–" or "Current RD+"). Running disparity is a binary parameter with either the value negative (–) or the value positive (+).

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter shall calculate a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver shall decide whether the Transmission Character is valid or invalid according to the following rules and tables and shall calculate a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity shall be used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character shall be calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks shall be calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in the table shall be found for the Valid Data byte or the Special Character byte for which a Transmission Character is to be generated (encoded). The current value of the Transmitter's running disparity shall be used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity shall be calculated. This new value shall be used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 1* shows naming notations and examples of valid transmission characters.

Table 1. Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	000101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity shall be searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character shall be used to calculate a new value of running disparity. The new value shall be used as the Receiver's current running disparity for the next received Transmission Character.

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 2* shows an example of this behavior.

Table 2. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Valid Data Characters (SC/$\overline{D}$ = LOW)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.2	010	11111	101011	0101	010100	0101

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.4	100	00110	011001	1101	011001	0010
D7.4	100	00111	111000	1101	000111	0010
D8.4	100	01000	111001	0010	000110	1101
D9.4	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

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Valid Special Character Codes and Sequences (SC/$\overline{D}$ = HIGH)[23, 24]

S.C. Byte Name	S.C. Code Name		Bits HGF	Bits EDCBA	Current RD− abcdei	Current RD− fghj	Current RD+ abcdei	Current RD+ fghj
K28.0	C0.0	(C00)	000	00000	001111	0100	110000	1011
K28.1	C1.0	(C01)	000	00001	001111	1001	110000	0110
K28.2	C2.0	(C02)	000	00010	001111	0101	110000	1010
K28.3	C3.0	(C03)	000	00011	001111	0011	110000	1100
K28.4	C4.0	(C04)	000	00100	001111	0010	110000	1101
K28.5	C5.0	(C05)	000	00101	001111	1010	110000	0101
K28.6	C6.0	(C06)	000	00110	001111	0110	110000	1001
K28.7	C7.0	(C07)	000	00111	001111	1000	110000	0111
K23.7	C8.0	(C08)	000	01000	111010	1000	000101	0111
K27.7	C9.0	(C09)	000	01001	110110	1000	001001	0111
K29.7	C10.0	(C0A)	000	01010	101110	1000	010001	0111
K30.7	C11.0	(C0B)	000	01011	011110	1000	100001	0111
Idle	C0.1	(C20)	001	00000	-K28.5+,D21.4,D21.5,D21.5,repeat[25]			
R_RDY	C1.1	(C21)	001	00001	-K28.5+,D21.4,D10.2,D10.2,repeat[26]			
EOFxx	C2.1	(C22)	001	00010	-K28.5,Dn.xxx0[27]		+K28.5,Dn.xxx1[27]	
	Follows K28.1 for ESCON Connect-SOF (Rx indication only)							
C-SOF	C7.1	(C27)	001	00111	001111	1000	110000	0111
	Follows K28.5 for ESCON Passive-SOF (Rx indication only)							
P-SOF	C7.2	(C47)	010	00111	001111	1000	110000	0111
					Code Rule Violation and SVS Tx Pattern			
Exception	C0.7	(CE0)	111	00000	100111	1000[28]	011000	0111[28]
-K28.5	C1.7	(CE1)	111	00001	001111	1010[29]	001111	1010[29]
+K28.5	C2.7	(CE2)	111	00010	110000	0101[30]	110000	0101[30]
					Running Disparity Violation Pattern			
Exception	C4.7	(CE4)	111	00100	110111	0101[31]	001000	1010[31]

Notes:

23. All codes not shown are reserved.
24. Notation for Special Character Byte Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn=the specified value between 00 and FF).
25. C0.1 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmitter begins sending the repeating transmit sequence −K28.5+, D21.4, D21.5, D21.5, (repeat all four bytes)... defined in X3.230 as the primitive signal "Idle word." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

Notes (continued):

26. C1.1 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmitter begins sending the repeating transmit sequence −K28.5+, D21.4, D10.2, D10.2,(repeat all four bytes)... defined in X3.230 as the primitive signal "Receiver_Ready (R_RDY)." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7 and the subsequent bytes are decoded as data.

27. C2.1 = Transmit either −K28.5+ or +K28.5− as determined by Current RD and modify the Transmission Character that follows, by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (−) the LSB becomes 1. This modification allows construction of X3.230 "EOF" frame delimiters wherein the second data byte is determined by the Current RD.

    For example, to send "EOFdt" the controller could issue the sequence C2.1−D21.4− D21.4−D21.4, and the HOTLink Transmitter will send either K28.5−D21.4−D21.4−D21.4 or K28.5−D21.5−D21.4−D21.4 based on Current RD. Likewise to send "EOFdti" the controller could issue the sequence C2.1−D10.4−D21.4−D21.4, and the HOTLink Transmitter will send either K28.5−D10.4−D21.4−D21.4 or K28.5−D10.5−D21.4− D21.4 based on Current RD.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

28. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. Transmission of this Special Character has the same effect as asserting SVS = HIGH.

    The receiver will only output this Special Character if the Transmission Character being decoded is not found in the tables.

29. C1.7 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD.

    The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if −K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.

30. C2.7 = Transmit Positive K28.5 (+K28.5−) disregarding Current RD.

    The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD−, otherwise K28.5 is decoded as C5.0 or C1.7.

31. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation.

    The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This might indicate that an error occurred in a prior byte.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B923−JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B923−SC	S21	28-Lead (300-Mil) SOIC	
CY7B923−JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
CY7B923−LMB	L64	28-Square Leadless Chip Carrier	Military

Ordering Code	Package Name	Package Type	Operating Range
CY7B933−JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B933−SC	S21	28-Lead (300-Mil) SOIC	
CY7B933−JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
CY7B933−LMB	L64	28-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroup
V_{OHT}	1, 2, 3
V_{OLT}	1, 2, 3
V_{OHE}	1, 2
V_{OLE}	1, 2, 3
V_{ODIF}	1, 2, 3
I_{OST}	1, 2, 3
V_{IHT}	1, 2, 3
V_{ILT}	1, 2, 3
V_{IHE}	1, 2, 3
V_{ILE}	1, 2, 3
I_{IHT}	1, 2, 3
I_{ILT}	1, 2, 3
I_{IHE}	1, 2, 3
I_{ILE}	1, 2, 3
I_{CC}	1, 2, 3
V_{DIFF}	1, 2, 3
V_{IHH}	1, 2, 3
V_{ILL}	1, 2, 3

Switching Characteristics

Parameter	Subgroup
t_{CKW}	9, 10, 11
t_{B}	9, 10, 11
t_{CPWH}	9, 10, 11
t_{CPWL}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SENP}	9, 10, 11
t_{HENP}	9, 10, 11
t_{PDR}	9, 10, 11
t_{PPWH}	9, 10, 11
t_{PDF}	9, 10, 11
t_{RISE}	9, 10, 11
t_{FALL}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CPRH}	9, 10, 11
t_{CPRL}	9, 10, 11
t_{RH}	9, 10, 11
t_{PRF}	9, 10, 11
t_{PRH}	9, 10, 11
t_{A}	9, 10, 11
t_{ROH}	9, 10, 11
t_{CKX}	9, 10, 11
t_{CPXH}	9, 10, 11
t_{CPXL}	9, 10, 11
t_{DS}	9, 10, 11

Document #: 38−00189−F

CY7B951

SST™
SONET/SDH Serial Transceiver

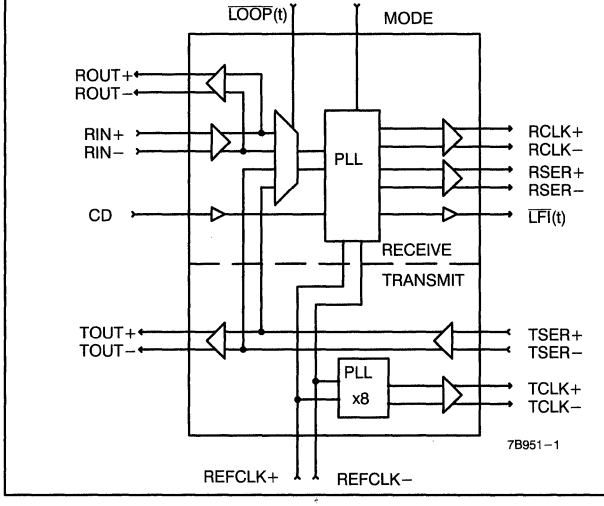
Features

- SONET/SDH and ATM Compatible
- Compatible with PMC–Sierra PM5345 SUNI™
- Clock and data recovery from 51.84- or 155.52-MHz datastream
- 155.52-MHz clock multiplication from 19.44-MHz source
- 51.84-MHz clock multiplication from 6.48-MHz source
- ±1% frequency agility
- Line Receiver Inputs: No external buffering required
- Differential output buffering
- 100K ECL compatible I/O
- No output clock "drift" without data transitions
- Link Status Indication
- Loop-back testing
- Single +5V supply
- 24-pin SOIC
- Compatible with fiberoptic modules, coaxial cable, and twisted pair media
- No external PLL components
- Power-down options to minimize power or crosstalk
- Low operating current: <65 mA
- 0.8μ BiCMOS

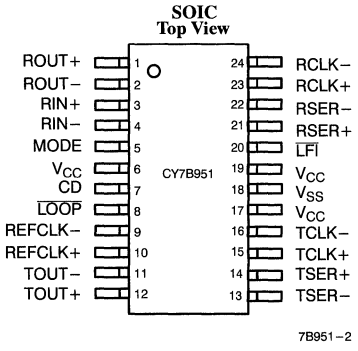
Functional Description

The SONET/SDH Serial Transceiver (SST) is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ or NRZI serial data stream and to provide differential data buffering for the Transmit side of the system.

Logic Block Diagram



Pin Configuration



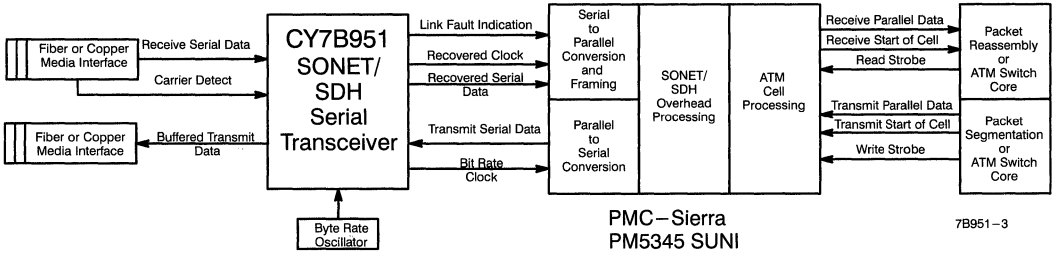


Figure 1. SONET/SDH and ATM Interface

SST is a trademark of Cypress Semiconductor Corporation
SUNI is a trademark of PMC–Sierra, Incorporated

Pin Descriptions

Name	I/O	Description
RIN±	Differential In	Receive Input. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embedd clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the RIN± inputs are not being used, connect RIN+ to V_{CC} and RIN− to V_{SS}.
ROUT±	ECL Out	Receive Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the input data stream (RIN±). This output pair can be used for Receiver input data equalization in copper based systems, reducing the system impact of data dependent jitter. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
RSER±	ECL Out	Recovered Serial Data. These ECL 100K outputs (+5V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.
RCLK±	ECL Out	Recovered Clock. These ECL 100K outputs (+5V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V_{CC} or left unconnected, the entire Receive PLL will be powered down.
CD	TTL/ECL In	Carrier Detect. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK×8 frequency. Also, the Link Fault Indicator ($\overline{LFI}$) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN). When the CD input is at a TTL LOW, the internal transitions detection circuitry is disabled.
$\overline{LFI}$	TTL Out	Link Fault Indicator. This output indicates the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the $\overline{LFI}$ output will be HIGH. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the $\overline{LFI}$ output will be LOW. If CD is at a TTL LOW then the $\overline{LFI}$ output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.
TSER±	Differential In	Transmit Serial Data. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the $\overline{LOOP}$ pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the TSER± inputs are not being used, connect RIN+ to V_{CC} and RIN− to V_{SS}.
TOUT±	ECL Out	Transmit Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low impedance copper media.
REFCLK±	Diff/TTL In	Reference Clock. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK− is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.
TCLK±	ECL Out	Transmit Clock. These ECL 100K outputs (+5V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
$\overline{LOOP}$	TTL In	Loop Back Select. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the $\overline{LOOP}$ input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When $\overline{LOOP}$ is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

Pin Descriptions (continued)

Name	I/O	Description
MODE	3-Level In	Frequency Mode Select. This three-level input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH the two PLLs operate at the SONET (SDH) STS−3 (STM−1) line rate of 155.52 MHz. When this input is held LOW the two PLLs operate at the SONET STS−1 line rate of 51.84 MHz. The REFCLK± frequency in both operating modes is 1/8 the PLL operating frequency. When the MODE input is left floating or held at $V_{CC}/2$ the TSER± inputs substitute for the internal PLL VCO for use in factory testing.
V_{CC}		Power.
V_{SS}		Ground.

Description

The CY7B951 Serial SONET/SDH Transceiver (SST) is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit clock, from a byte rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system (see *Figure 1*). This device is compliant with all relevant SONET/SDH specifications including ANSI T1X1.6/91−022, ANSI T1X1.3/ 93−006R1 Draft and CCITT G958.

Operating Frequency

The SST operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. The MODE input has three different functional selections. When MODE is connected to V_{CC}, the highest operating range of the device is selected. A 19.44-MHz ±1% source must drive the REFCLK input and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48-MHz ±1% source must drive the REFCLK inputs and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84 MHz ±1%. When the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test mode.

Transmit Functions

The transmit section of the SST contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK×8) to produce a PECL (Pseudo ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE pin as explained above. The SST Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter as shown in *Figure 1*.

The REFCLK± input can be configured three ways. When both REFCLK+ and REFCLK− are connected to a differential 100K-compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK− or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the SST yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the receiver is to recover clock (RCLK±) and data (RSER±) from the incoming differential PECL data stream (RIN±) without the need for external buffering. These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2.5V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK×8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin as explained earlier. To insure accurate data and clock recovery, REFCLK×8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK×8 frequency accuracy be within 20−100 ppm.

The differential input serial data (RIN±) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT±. This output pair can be used as part of the transmission line interface circuit for base line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) output is a TTL-level output that indicates the status of the receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{\text{LFI}}$ is controlled by the Carrier Detect input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW (≤2.5V Max.), the $\overline{\text{LFI}}$ output will transition LOW and the Receiver PLL will align itself with the REFCLK×8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN).

In addition, the SST has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transition can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive media coupling. The SST will detect a quiet link by counting the

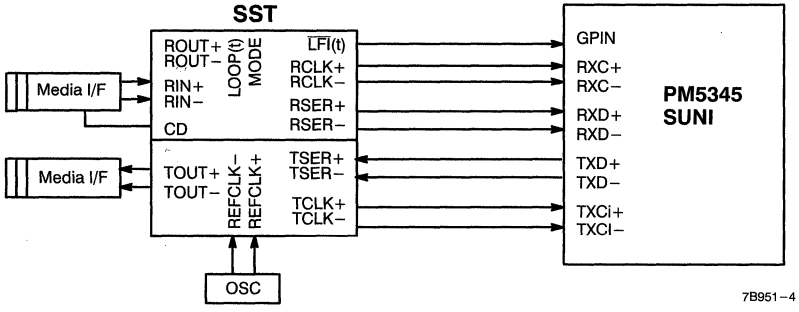


Figure 2. SST to PMC−Sierra PM5345 SUNI Connection Diagram

number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 256 bit times have passed without a data transition on RIN±, $\overline{LFI}$ will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. $\overline{LFI}$ will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 256 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW (≤0.8V). When CD is pulled to a TTL LOW the $\overline{LFI}$ will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLK×8 frequency. $\overline{LFI}$ LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

Loop Back Testing

The TTL level $\overline{LOOP}$ pin is used to perform loop-back testing. When $\overline{LOOP}$ is asserted (held LOW) the Transmitter serial input (TSER±) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{LOOP}$ input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{LOOP}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{LOOP}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power Down Modes

There are several power-down features on the SST. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC}, the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the Link Fault Indicator ($\overline{LFI}$) will still reflect the state of the Carrier Detect (CD) input. This feature can be used for aggressive power management.

Applications

The SST can be used in SONET/SDH and ATM applications. The operating frequency of the 7B951 is centered around the SONET/SDH STS−1 rate of 51.84 MHz and the SONET/SDH STS−3/STM−1 rate of 155.52 MHz. This device can also be used in data mover and Local Area Network (LAN) applications that operate at these frequencies.

The SST can provide clock and data recovery as well as output buffering for physical layer protocol engines such as the SONET/SDH and ATM processing application shown in *Figures 1* and *2* and SONET/SDH overhead termination and 155Mb/s serial to parallel conversion as shown in *Figure 3*.

Figure 1 shows the SST in a ATM system that uses the PMC−Sierra SUNI device. The SST will recover clock and data from the input serial data stream and pass it to the PM5345 SUNI. The SUNI device will perform serial to parallel conversion, SONET/SDH overhead processing and ATM cell processing and then pass ATM cells to an ATM packet reassembly engine. On the Transmit side, a segmentation engine will divide long packets of data such as Ethernet packets into 53 byte cells and pass them to the SUNI. The SUNI device will then perform ATM cell processing, such as header generation, SONET/SDH overhead processing and parallel to serial conversion. This serial data will then be passed to the SST which will buffer this data stream and pass it along to the transmission media.

The SST provides the necessary clock and data recovery function to the PM5345. These differential PECL clock and data signals interface directly with the RXD± and RXC± inputs of the SUNI device as show in *Figure 2*. In addition, the SST provides transmit data output buffering for direct drive of cable transmission media. Lastly, the SST provides a bit rate reference clock to the SUNI transmitter by multiplying a local clock by eight allowing an inexpensive crystal oscillator to be used for the local reference.

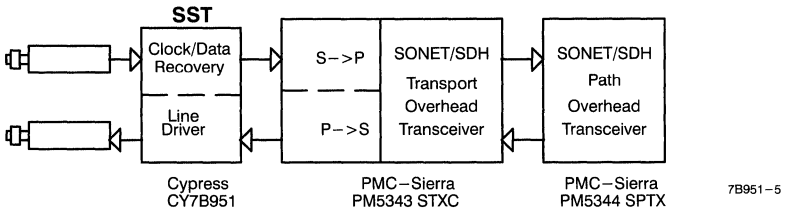


Figure 3. SONET/SDH Overhead Processing Application

Figure 3 shows the SST in a more generic telecommunications system. In this system, the SST is used to provide clock recovery for a pure SONET/SDH system such as a SONET/SDH switch. The SST provides the recovered clock and data to a serial to parallel converter and SONET/SDH Transport Overhead Processor such as the PMC-Sierra PM5343 STXC. The parallel data is then passed to a SONET/SDH Path Overhead Processor such as the PMC-Sierra PM5344 SPTX.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into ECL Outputs (HIGH) ..... −50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

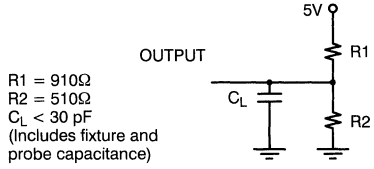
Electrical Characteristics Over the Operating Range

Parameter	Description		Test Condition	Min.	Max.	Unit
TTL Compatible Input Pins (LOOP, REFCLK+, REFCLK−)						
V_{IHT}	Input HIGH Voltage			2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage			−0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK	$V_{IN}=V_{CC}$	+0.5	+200	µA
		LOOP	$V_{IN}=V_{CC}$	−10	+10	µA
I_{ILT}	Input LOW Current	REFCLK	$V_{IN}=0.0V$	−50	+50	µA
		LOOP	$V_{IN}=0.0V$	−500		µA
TTL Compatible Output Pins ($\overline{LFI}$)						
V_{OHT}	Output HIGH Voltage		$I_{OH}=-2$ mA	2.4		V
V_{OLT}	Output LOW Voltage		$I_{OL}=4$ mA		0.45	V
I_{OST}	Output Short Circuit Current		$V_{OUT}=0V$[2]	−15	−90	mA
ECL Compatible Input Pins (REFCLK+/−, CD, TSER+/−, RIN+/−)						
I_{IHE}	ECL Input HIGH Current		$V_{IN}=V_{IHE(MAX)}$		+250	µA
		TSER/RIN	$V_{IN}=V_{IHE(MAX)}$		+750	µA
I_{ILE}[3]	ECL Input LOW Current		$V_{IN}=V_{ILE(MIN)}$	+0.5		µA
		TSER/RIN	$V_{IN}=V_{ILE(MIN)}$	−200		µA
V_{IDIFF}	Input Differential Voltage	TSER/RIN		50	1200	mV
		REFCLK		100	1200	mV
V_{IHE}	Input High Voltage	TSER/RIN			V_{CC}	V
		REFCLK		3.0	V_{CC}	V
		CD		$V_{CC}-1.165$	V_{CC}	V
V_{ILE}	Input LOW Voltage			2.0		V
		REFCLK		2.5		V
		CD (ECL)		2.5	$V_{CC}-1.475$	V
		CD (Disable)		−0.5	0.8	V
ECL Compatible Output Pins (ROUT+/−,RCLK+/−,RSER+/−,TOUT+/−,TCLK+/−)						
V_{OHE}	ECL Output HIGH Voltage		Commercial	$V_{CC}-1.03$	$V_{CC}-0.83$	V
			Industrial[4]	$V_{CC}-1.08$	$V_{CC}-0.83$	
V_{OLE}	ECL Output LOW Voltage		T > 0°C	$V_{CC}-1.86$	$V_{CC}-1.62$	V
V_{ODIFF}	Output Differential Voltage			0.6		V
Three-Level Input Pins (MODE)						
V_{IHH}	Three-Level Input HIGH			$V_{CC}-1.0$	V_{CC}	V
V_{IMM}	Three-Level Input MID			$V_{CC}/2-0.5$	$V_{CC}/2+0.5$	V
V_{ILL}	Three-Level Input LOW			0.0	1.0	V
Operating Current[5]						
I_{CCS}	Static Operating Current				30	mA
I_{CCR}	Receiver Operating Current				50	mA
I_{CCT}	Transmitter Operating Current				13	mA
I_{CCE}	ECL Pair Operating Current				7.0	mA
I_{CC5}	Additional Current at 51.84 MHz				7.0	mA
I_{CCO}	Additional Current $\overline{LFI}$=LOW				3	mA

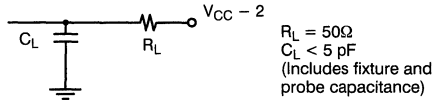
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 5.0V$	10	pF

AC Test Loads and Waveforms

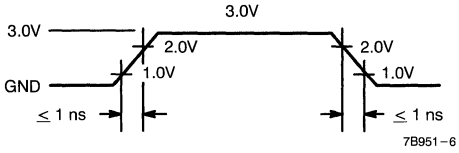


(a) TTL AC Test Load[7]

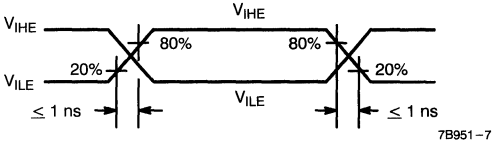


(b) ECL AC Test Load[7]

7B951–8



(c) TTL Input Test Waveform



(d) ECL Input Test Waveform

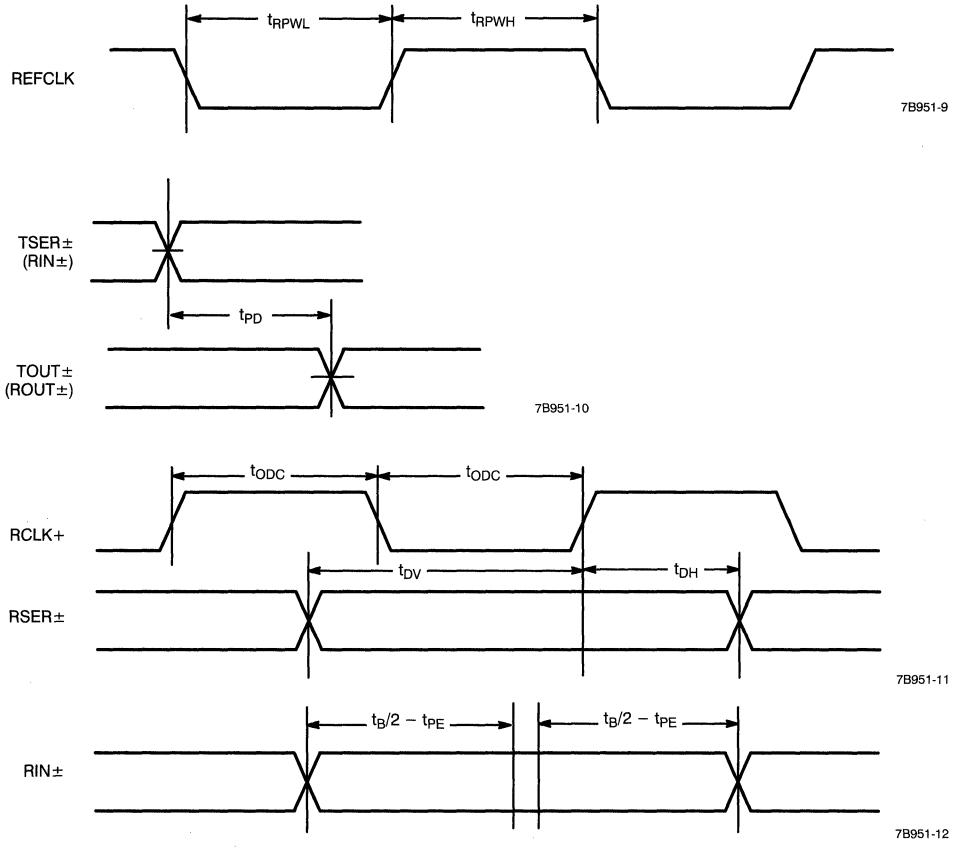
Switching Characteristics Over the Operating Range

Parameter	Description		Min.	Max.	Unit
f_{REF}	Reference Frequency	MODE=LOW	6.41	6.55	MHz
		MODE=HIGH	19.24	19.64	MHz
f_B	Bit Time[8]	MODE=LOW	19.5	19.1	ns
		MODE=HIGH	6.50	6.40	ns
t_{PE}	Receiver Static Phase Error[6]	MODE=LOW		100	ps
		MODE=HIGH		200	ps
t_{ODC}	Output Duty Cycle (TCLK±, RCLK±)[6]		48	52	%
t_{RF}	Output Rise/Fall Time[6]		0.4	1.2	ns
t_{LOCK}	PLL Lock Time (RIN transition density 25%)			0.5	ms
t_{RPWH}	REFCLK Pulse Width HIGH		10		ns
t_{RPWL}	REFCLK Pulse Width LOW		10		ns
t_{DV}	Data Valid		3		ns
t_{DH}	Data Hold		1		ns
t_{PD}	Propagation Delay (RIN to ROUT, TSER to TOUT)[9]			10	ns

Notes:

2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Input currents are always positive at all voltages above $V_{CC}/2$.
4. Specified only for temperatures below 0°C.
5. Total Receiver operating current (assuming that the Transmitter is not activated) can be found by adding $I_{CCS} + I_{CCR} + x * I_{CCE}$; where x is 2 if the ROUT± outputs are not activated and 3 if they are activated.
   Total Transmitter operating current (assuming that the Receiver is not activated) can be found by adding $I_{CCS} + I_{CCT} + x * I_{CCE}$; where x is 1 if the TOUT± outputs are not activated and 2 if they are activated.
   Total device power (assuming that the Transmitter and the Receiver are activated) can be found by adding $I_{CCS} + I_{CCR} + I_{CCT} + x * I_{CCE}$; where x represents the number of ECL output pairs activated.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
8. f_B is calculated a $1/(f_{REF \times 8})$.
9. The ECL switching threshold is the differential zero crossing (i.e., the place where + and − signals cross).

Switching Waveforms for the CY7B951 SONET/SDH Serial Transceiver



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7B951–SC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY7B951–SI	S13	24-Lead (300-Mil) Molded SOIC	Industrial

Document #: 38–00358–C

100BASE-T4/10BASE-T Fast Ethernet Transceiver (CAT 3)

Features

- **Complies with IEEE 802.3u draft standard**
- **Three operating modes:**
  - **— 100BASE-T4**
  - **— 10BASE-T Full Duplex**
  - **— 10BASE-T**
- **Media Independent Interface (MII)**
  - **— Three-state receive port**
  - **— Serial management port**
- **Auto-Negotiation**
- **On-chip transmit wave shaper**
- **Receive filter and adaptive equalization**
- **PMA Interface for repeater applications**
- **Jam function for hub applications**
- **LED status indicators: TX, RX, Link**
- **Loopback mode for PHY integrity testing**
- **Auto-polarity correction**
- **Low-power CMOS**
- **80-pin PQFP**

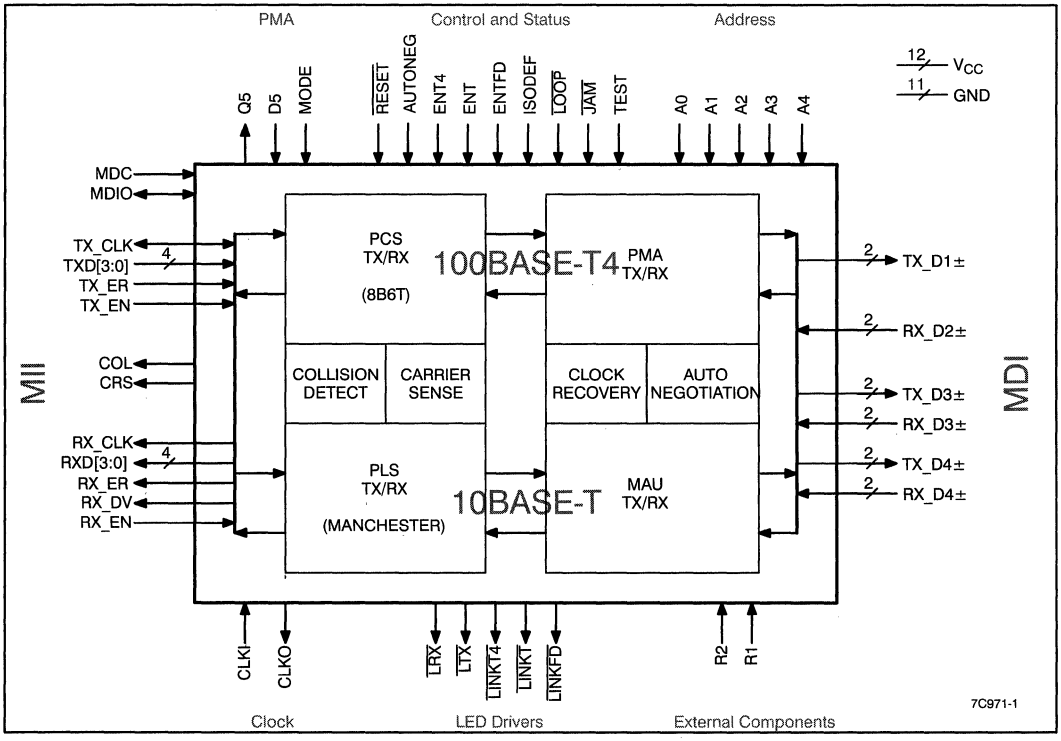
Functional Description

The CY7C971 is a full featured physical layer transceiver (PHY) device supporting both 100BASE-T4 (Fast Ethernet) and 10BASE-T Local Area Network (LAN) standards. The CY7C971 complies with IEEE 802.3 100BASE-T4, 10BASE-T, MII, and Auto-Negotiation standards for twisted pair interfaces.

The CY7C971 interfaces to category 3, 4, or 5 unshielded twisted-pair cable through its Media Dependent Interface (MDI). The Media Independent Interface (MII) attaches directly to Media Access Control (MAC) layer devices.

The CY7C971 performs the Physical Coding Sublayer (PCS), Physical Layer Signalling (PLS), Physical Media Attachment (PMA), and Media Attachment Unit (MAU) functions defined in the 802.3 standard. Ethernet frames are transferred from the MAC to the CY7C971 over the MII interface. The data is encoded in the PCS or PLS encoder (8B6T for 100BASE-T4 or Manchester for 10BASE-T) and then passed to the PMA or MAU where the encoded data is shifted bitwise on to the twisted-pair media. Collision and Carrier Sense signals are generated by the CY7C971 and passed to the MAC over the MII.

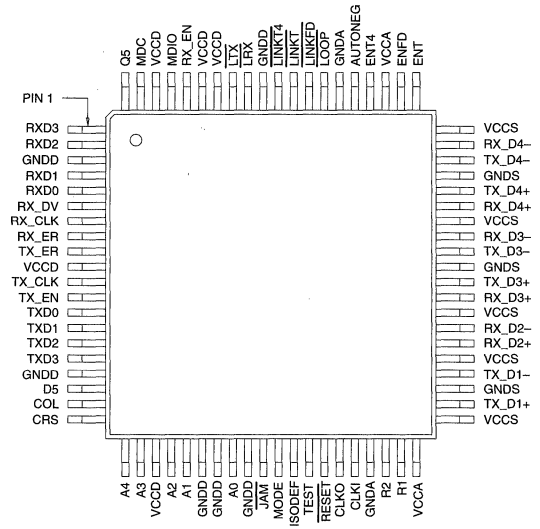
The CY7C971 PHY uses 802.3 standard Auto Negotiation to configure the link. The PHY includes a direct interface to the PMA layer for repeater applications.



Pin Configuration

80-Lead Plastic Quad Flatpack

(Top View)



7C971-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Pin Descriptions

Media Independent Interface (MII)

Name	I/O	Description
TXD[3:0] (D[3:0])	Input (TTL)	Transmit Data. TXD[3:0] are the data signals that carry the Ethernet transmit frame data from the MAC to the PHY on a nibble basis. TXD[3:0] are sampled on the rising edge of TX_CLK when TX_EN is asserted HIGH. In PMA mode, these pins become the D[3:0] pins used for passing binary encoded 8B6T symbols to the PMA sublayer.
TX_EN	Input (TTL)	Transmit Enable. When asserted HIGH, TX_EN indicates that the MAC is presenting data to the TXD[3:0] inputs of the PHY. TX_EN should be asserted HIGH with the first nibble of the preamble and remain HIGH for the duration of the frame. TX_EN should be deasserted on the first cycle following the final nibble of the frame. In PMA mode, TX_EN is asserted HIGH in order to latch D[5:0] into the transmitter.
TX_CLK	Output (TTL, Three State)	Transmit Clock. In MII Mode (MODE = HIGH), TX_CLK is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TX_EN, and TX_ER from the MAC. The nominal frequency of TX_CLK is 25 MHz in 100-Mb/s mode and 2.5 MHz in 10-Mb/s mode.
TX_ER (D4)	Input (TTL)	Transmit Coding Error. When asserted HIGH while TX_EN is HIGH, the PHY will transmit an error code word . TX_ER is sampled on the rising edge of TX_CLK. In PMA mode, this pin becomes the D4 pin used for passing binary encoded 8B6T symbols to the PMA sublayer.
RXD[3:0] (Q[3:0])	Output (TTL, Three State)	Receive Data. RXD[3:0] are the data signals that carry the received Ethernet frame data from the PHY to the MAC on a nibble basis. RXD[3:0] are driven synchronous to RX_CLK. In PMA mode, these pins become the Q[3:0] pins used for transferring binary encoded 8B6T symbols from the PMA sublayer.
RX_DV	Output (TTL, Three State)	Receive Data Valid. When asserted HIGH, RX_DV indicates that the PHY is presenting recovered and decoded nibbles on the RXD[3:0] lines and that RX_CLK has been synchronized to the recovered data. RX_DV is first driven HIGH when RXD[3:0] contains the SFD and is held HIGH for the duration of the frame. RX_DV makes transitions synchronous to RX_CLK. In PMA Mode, RX_DV is driven high when Q2–3 contains the first data symbol.
RX_CLK	Output (TTL, Three State)	Receive Clock. RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER signals from the PHY to the MAC. When RX_DV is HIGH, RX_CLK is recovered from the received data. When RX_DV is LOW, RX_CLK is sourced from the PHY's nominal frequency. Transition between nominal frequency and recovered frequency is made while RX_DV is LOW. In 100-Mb/s mode, the nominal clock frequency is 25 MHz,and in 10-Mb/s the nominal frequency is 2.5 MHz.
RX_EN[1]	Input (TTL)	Receiver Output Enable. RX_EN enables the RXD[3:0], COL, Q5, RX_ER, and RX_DV signal drivers. RX_EN allows the receive data signals to bussed together for multiple PHY applications.
RX_ER	Output (TTL, Three State)	Receive Error. RX_ER is asserted HIGH to indicate to the MAC that a fault condition was detected during the frame presently being transferred from the PHY to the MAC. RX_ER is driven synchronously with RX_CLK.
COL (Q4)	Output (TTL, Three State)	Collision Detect. COL is asserted HIGH to indicate that a collision has occurred on the media. COL is asserted asynchronously and with minimum delay from the start of the collision. In PMA Mode, this pin becomes the Q4 pin used for transferring binary encoded 8B6T symbols from the PMA sublayer.
CRS	Output (TTL, Three State)	Carrier Sense. CRS is asserted HIGH by the PHY to indicate the detection of a non-idle condition on the media. CRS is asserted asynchronously and with minimum delay from the detection of the non-idle condition. CRS is asserted HIGH throughout the duration of a collision condition.
MDC	Input (TTL)	Management Data Clock. MDC is sourced from the station management entity (STA) to the PHY as a timing reference for the transfer of management information on the MDIO signal.
MDIO	Bidirectional (TTL, Three State)	Management Data Input/Output. MDIO is a bidirectional signal between the PHY and the station management entity (STA) used to transfer control and status information. Control information is driven from STA to the PHY synchronously with MDC and sampled on the rising edge of MDC. The PHY drives status information to the STA synchronously with MDC. The STA samples the data on the rising edge of MDC.

Note:
1. RX_EN is not specified in the 802.3 MII standard.

Pin Descriptions (continued)

Media Dependent Interface

Name	I/O	Description
TX_D1+ TX_D1−	Differential Output	Transmit Data. TX_D1± are differential line drivers for data transmission. In 10BASE-T mode TX_D1± transmit Manchester encoded data with a nominal period of 100 ns. In 100BASE-T4 mode TX_D1± transmit 8B6T ternary symbols with a nominal period of 40 ns. TX_D1± also participate in the Link Integrity function.
RX_D2+ RX_D2−	Differential Input	Receive Data. RX_D2± are differential line receivers for data reception. In 100-Mb/s mode, RX_D2± receives 8B6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D2± receives Manchester encoded bits with a nominal period of 100ns. RX_D2± also participates in the Link Integrity function.
TX_D3+ TX_D3−	Differential Output	Transmit Data. TX_D3± are differential line drivers for data transmission. In 100-Mb/s mode, TX_D3± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D3± are not used.
RX_D3+ RX_D3−	Differential Input	Receive Data. RX_D3± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D3± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D3± are not used.
TX_D4+ TX_D4−	Differential Output	Transmit Data. TX_D4± are differential line drivers used for data transmission. In 100-Mb/s mode, TX_D4± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D4± are not used.
RX_D4+ RX_D4−	Differential Input	Receive Data. RX_D4± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D4± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D4± are not used.

Physical Media Attachment Interface

Name	I/O	Description
MODE	Input (TTL)	Mode. When MODE is tied HIGH, the transceiver is in normal mode. Received and tranmitted data will move through the PMA and the PCS sublayers. Asserting MODE LOW exposes the 100BASE-T4 PMA service interface and disables 10BASE-T. The PCS is bypassed and the binary coded 6T serial data is presented at the MII and PMA interface pins.
D5	Input (TTL)	PMA Input Data. D5 is an input signal to the PMA transmit sublayer when MODE is asserted LOW.
Q5	Output (TTL, Three State)	PMA Output Data. Q5 is an output signal from the PMA receive sublayer when MODE is asserted LOW. Q5 is high-impedence when RX_EN is HIGH.

Control and Status

Name	I/O	Description
$\overline{\text{RESET}}$	Input (TTL)	Reset. When $\overline{\text{RESET}}$ is asserted LOW, the PHY is placed in the reset state and the transmit and receive functions are disables. The MII registers are placed in their default states.
AUTONEG	Input (TTL)	Auto-Negotiation Enable. When asserted HIGH, Auto-Negotation capability is enabled by setting the Status Register bit 1.3. Auto-Negotation is controlled through the MII management registers. When asserted LOW, Auto-Negotation capability is disabled. AUTONEG is sampled on the rising edge of $\overline{\text{RESET}}$.
ENT4	Input (TTL)	Enable 100BASE-T4. ENT4 enables 100BASE-T4 operation by setting the Status Register bit 1.15. When ENT4 is HIGH, bit 1.15 is forced HIGH, enabling 100BASE-T4 operation. When ENT4 is LOW, bit 1.15 is forced LOW, disabling 100BASE-T4. ENT4 is latched on the rising edge of $\overline{\text{RESET}}$.
ENT	Input (TTL)	Enable 10BASE-T. ENT enables 10BASE-T operation by setting the Status Register bit 1.11. When ENT is HIGH, bit 1.11 is forced HIGH, enabling 10BASE-T operation. When ENT4 is LOW, bit 1.11 is forced LOW, disabling 10BASE-T. ENT is latched on the rising edge of $\overline{\text{RESET}}$.
ENTFD	Input (TTL)	Enable 10BASE-T Full Duplex. ENTFD enables 10BASE-T Full Duplex operation by setting the Status Register bit 1.12. When ENTFD is HIGH, bit 1.12 is forced HIGH, enabling 10BASE-T Full Duplex operation. When ENTFD is LOW, bit 1.12 is forced LOW, disabling 10BASE-T Full Duplex. ENTFD is latched on the rising edge of $\overline{\text{RESET}}$.
ISODEF	Input (TTL)	Isolate Default. ISODEF determines the default state of Isolate Bit 0.10 in the Control Register. When ISODEF is HIGH, the default value for 0.10 is 1. When ISODEF is LOW, the default value for 0.10 is 0. ISODEF is latched on the rising edge of $\overline{\text{RESET}}$.
$\overline{\text{LOOP}}$	Input (TTL)	Loopback Enable. When asserted LOW, the transmitter bit stream is looped back to the receiver for diagnostic testing. When $\overline{\text{LOOP}}$ is HIGH, the Loopback function is controlled by the Loopback bit in the control register.

Pin Descriptions (continued)

Control and Status (continued)

Name	I/O	Description
$\overline{JAM}$	Input (TTL)	100BASE-T4 Jam Generation. When $\overline{JAM}$ is LOW in 100BASE-T4 mode and a carrier is present, the PHY will enter the collision state and generate the Jam pattern. The jam condition will persist for a minimum of 512 bit times.
TEST	Input (TTL)	Test. This pin is used for factory testing and should be tied LOW for normal operation.

Address

Name	I/O	Description
A[4:0]	Input (TTL)	PHY Address. These pins assign the management address to the PHY. A0 is least significant bit and A4 is the most significant bit. A4 is the first address bit received by the PHY in the management frame. The address is latched on the rising edge of $\overline{RESET}$.

LED Drivers

Name	I/O	Description
$\overline{LRX}$	Output (Open Drain, Weak Pull-Up)	Receive LED Indicator. $\overline{LRX}$ is driven LOW when the transceiver is receiving. An internal 20KΩ resistor will pull $\overline{LRX}$ HIGH when the transceiver is not receiving.
$\overline{LTX}$	Output (Open Drain, Weak Pull-Up)	Transmit LED Indicator. $\overline{LTX}$ is driven LOW when the transceiver is transmitting. An internal 20KΩ resistor will pull $\overline{LTX}$ HIGH when the transceiver is not transmitting.
$\overline{LINKT4}$	Output (Open Drain, Weak Pull-Up)	100BASE-T4 Link Pass LED Indicator. $\overline{LINKT4}$ is driven LOW when the 100BASE-T4 transceiver is in the Link Pass State. An internal 20KΩ resistor will pull $\overline{LINKT4}$ HIGH when the transceiver is not in the 100BASE-T4 Link Pass State.
$\overline{LINKT}$	Output (Open Drain, Weak Pull-Up)	10BASE-T Link Pass LED Indicator. $\overline{LINKT}$ is driven LOW when the 10BASE-T transceiver is in the Link Pass State. An internal 20KΩ resistor will pull $\overline{LINKT}$ HIGH when the transceiver is not in the 100BASE-T Link Pass State.
$\overline{LINKFD}$	Output (Open Drain, Weak Pull-Up)	10BASE-T Full Duplex Link Pass LED Indicator. $\overline{LINKFD}$ is driven LOW when 10BASE-T Full Duplex has been negotiated or chosen as the operating mode and the 10BASE-T transceiver is in the Link Pass State. An internal 20KΩ resistor will pull $\overline{LINTFD}$ HIGH when the transceiver is not in the 100BASE-T Link Pass State.

Clock

Name	I/O	Description
CLKI	Input	Reference Clock Input. In MII Mode (MODE=HIGH), the 25-MHz signal is used as a timing reference for TX_CLK and analog circuits. This pin should be connected to either to a 25-MHz crystal or a crystal-controlled TTL-level clock source. In PMA mode (MODE = LOW), CLKI is an input and is used as a timing reference for the PMA interface and analog circuits.
CLKO	Output	Reference Clock Output. This pin connects to a 25 MHz crystal or is left open if a TTL clock is used with CLKI. In PMA mode, CLKO should be left open.

External Components

Name	I/O	Description
R1	Passive	10K ±1% External resistor.
R2	Passive	10K ±1% External resistor.

Power and Ground

Name	I/O	Description
V_{CCD}	Digital Power	Positive Voltage Supply. V_{CC} requires a 5V±10% supply.
V_{CCA}	Analog Power	Positive Voltage Supply. V_{CC} requires a 5V±10% supply.
V_{CCS}	Serial MDI Power	Positive Voltage Supply. V_{CC} requires a 5V±10% supply.
GNDD	Digital Ground	Ground.
GNDA	Analog Ground	Ground.
GNDS	Serial MDI Ground	Ground.

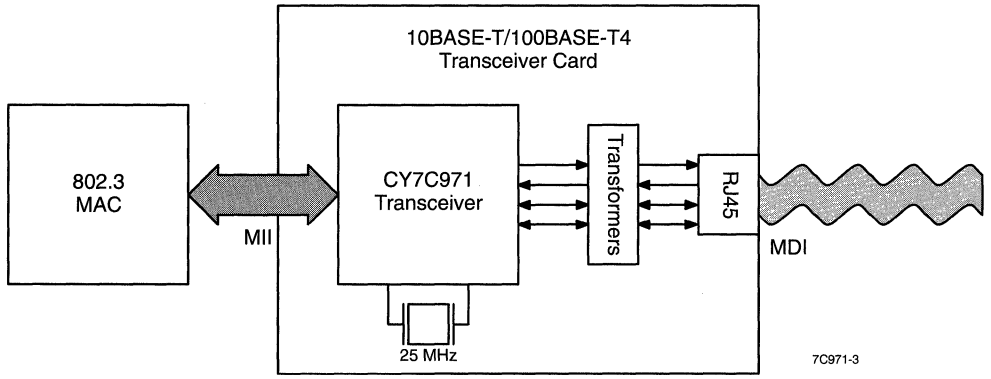


Figure 1. Transceiver Card Block Diagram

CY7C971 Description

100BASE-T4

The CY7C971 provides a physical layer interface (PHY) for dual speed IEEE 802.3 100BASE-T4 and 10BASE-T CSMA/CD local area networks. 100BASE-T4 offers increased performance over existing 10BASE-T networks while maintaining compatibility with the existing Ethernet Media Access Control (MAC) specification. The 100BASE-T4 PHY interfaces to 4 pairs of category 3, 4, or 5 cable. The 100BASE-T4 PHY is comprised of the Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Media Independent Interface (MII), and Media Dependent Interface (MDI). A typical 100BASE-T4 transceiver card application is shown in *Figure 1*.

Transmitter

The transmitter is comprised of the Physical Coding Sublayer (PCS) and the Physical Media Attachment (PMA). *Figure 2* shows a block diagram of the T4 transmitter.

Transmit Physical Coding Sublayer (PCS)

The PCS takes nibble-wide data from the MII and accumulates them into 8-bit octets in the TXD1 and TXD2 registers. The octets are then encoded using the 8B6T ternary code according to the 802.3 standard. The encoded 8B6T code groups are then loaded in binary form to the shift registers.

Three shift registers convert the parallel 8B6T code groups to serial form. When the transmitter is active, a shift register is loaded on every other TX_CLK cycle. The first 8B6T code group of the frame is loaded into TX_shift1. The second group is loaded into TX_shift2 and the third into TX_shift3. The 4th group will be loaded into TX_shift1. This sequence continues until all of the 8B6T code groups comprising the frame have been transmitted.

At the start of the transmit frame, TX_shift2 and TX_shift3 will be loaded with a pad sequence aligned with first 8B6T code group in TX_shift1. The pad sequence aides the receiver with clock recovery and pair alignment. The preamble is generated automatically and follows the pad sequence.

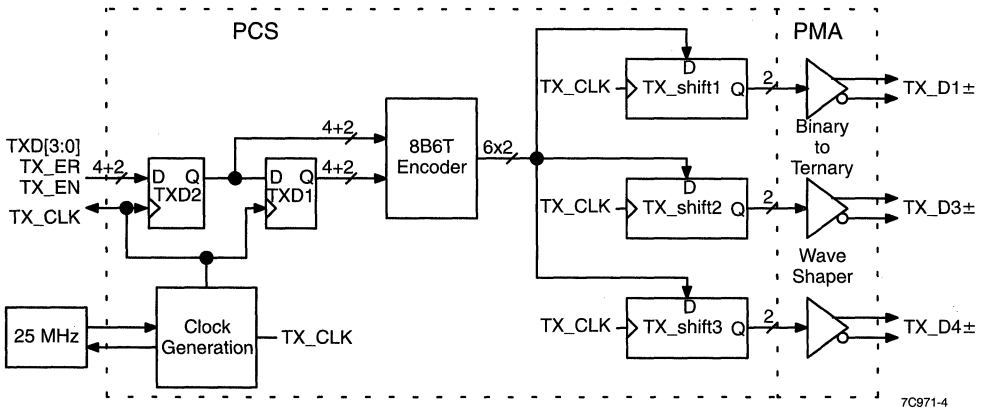


Figure 2. T4 Transmitter Block Diagram

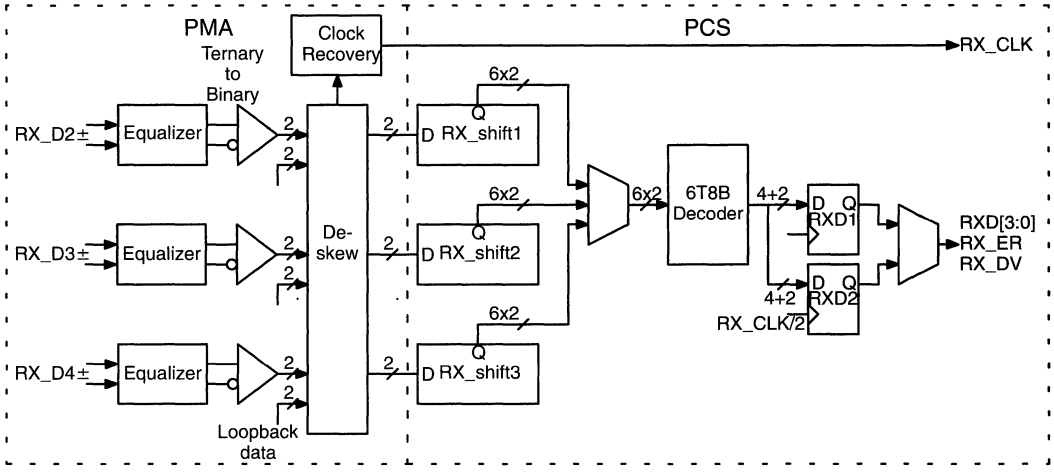


Figure 3. T4 Receiver Block Diagram

Transmit Physical Media Attachment (PMA)

The Transmit PMA converts the serial encoded 6T bits from the transmit PCS to their corresponding ternary waveforms. The waveshaper Digial to Analog Converter (DAC) generates high precision raised cosine waveforms on each transmission pair. The waveforms conform to the 100BASE-T4 output template specification. No external filters are required. The PMA output drivers interface to the media through external termination resistors and isolation transformers.

Receiver

The T4 receiver is comprised of the PCS and the PMA. *Figure 3* shows a block diagram of the receiver

Receive Physical Media Attachment (PMA)

The PMA receives serial 8B6T symbols from the twisted-pair interface and presents them to the PCS. The T4 receiver media interface features three adaptive equalizers. The equalizers compensate for the attentuation of high-frequency signals by up to 100 meters of category 3, 4, or 5 twisted-pair cable. The equalized waveforms are converted to binary form and passed to the clock recovery and data alignment blocks. The clock recovery circuit aligns the frequency and phase of RX_CLK with that of the received serial data. The data alignment block deskews the three receive channels.

Receive Physical Coding Sublayer (PCS)

The PCS accepts serial 8B6T symbols from the PMA, deserializes them, and then decodes the 8B6T code groups. Three shift registers convert the serial data back to parallel form. The first 8B6T code group is shifted into RX_shift1. The second 6T symbol group is shifted into RX_shift2 and the third into RX_shift3. The fourth code group is then shifted into RX_shift1. This process continues until the entire frame has been deserialized. The parallel 8B6T data are converted to 8-bit octets and latched into registers RXD1 and RXD2 on every other RX_CLK. The data is then presented at the MII interface in nibble form. RX_DV indicates that received data is present on the RXD[3:0] pins. RX_ER indicates that a receiver fault has occured.

Carrier Sense

The carrier sense function detects activity on the media using a smart squelch function similiar to 10BASE-T. The CRS signal is asserted HIGH when a valid carrier is detected on the pair RX_D2 according to the 10BASE-T4 draft standard. After detecting a valid carrier, an eop1 code group or seven consecutive zeros on RX_D2 must be detected before CRS is deasserted.

Collision Detection

A collision is detected when the transmitter is active simultaneously with the detection of a valid carrier by the carrier sense function. The MII COL signal will be asserted HIGH to signal the presence of a collision. When a collision is detected the TX_D2 and TX_D3 pair drivers turn off.

Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotation and normal operation.

10BASE-T

The CY7C971 provides a 10BASE-T physical layer interface for compatibility with existing 10-Mb/s Ethernet networks. 10BASE-T operation is automatically selected if Auto-Negotation established 10BASE-T as the highest common operating mode. The 10BASE-T transceiver can also be enabled manually by disabling Auto-Negotation and clearing the Speed Selection (0.13) bit in the MII Control Register. The $\overline{\text{LINKT}}$ pin indicates when 10BASE-T is the selected mode of operation and the 10BASE-T transceiver is in the link pass state. *Figure 4* shows a block diagram of the 10BASE-T transceiver.

During 10BASE-T operation, transmit and receive data are transfered over the MII interface in nibble wide groups. The TX_CLK and RX_CLK clocks are sourced from the PHY with a 2.5-MHz nominal clock rate. TX_EN qualifies incoming transmit data,and RX_DV qualifies receive data. In this mode, the MII complies with the IEEE MII specification for a 10-Mb/s interface.

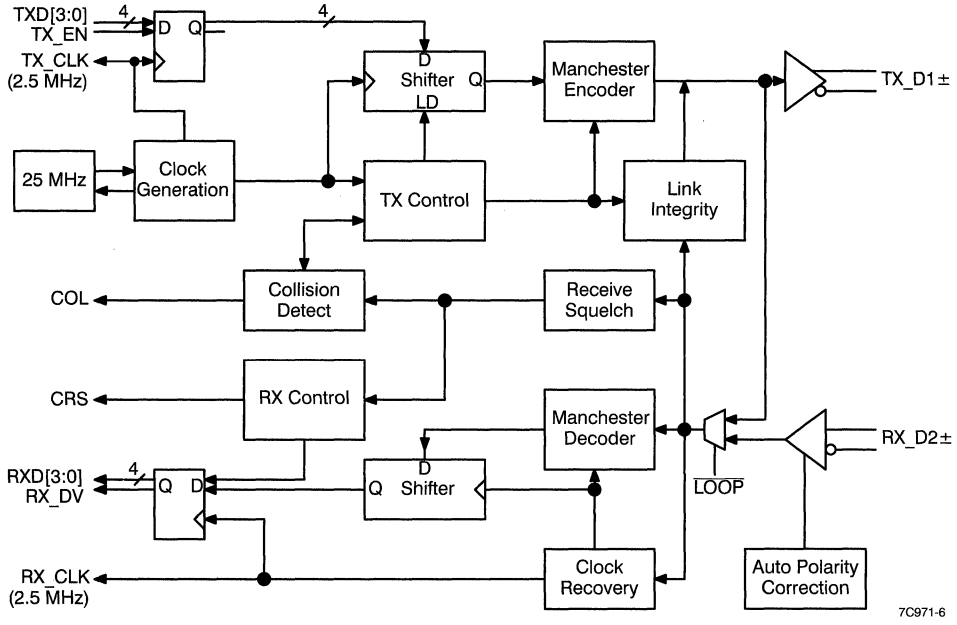


Figure 4. 10BASE-T Transmitter & Receiver Block Diagram

Full Duplex

The CY7C971 supports Full Duplex operation in 10BASE-T mode. 10BASE-T Full Duplex operation is automatically selected if Auto-Negotation established 10BASE-T Full Duplex as the highest common operating mode. The 10BASE-T Full Duplex operation can also be selected manually by disabling Auto-Negotation and clearing the Speed Selection (0.13) bit and setting the Duplex Mode Bit (0.8) in the MII Control Register. 10BASE-T Full Duplex mode cannot be enabled through Auto-Negotation or manually unless the the ENTFD pin is HIGH. The $\overline{\text{LINKFD}}$ pin indicates when 10BASE-T Full Duplex is the selected mode of operation and the 10BASE-T transceiver is in the Link Pass State. During full duplex operation, the collision pin (COL) is LOW.

Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotation and normal operation.

Media Independent Interface (MII)

The MII provides a connection between the PHY and the MAC and between the PHY and the station management (STA) entity. The MII is capable of supporting 100- and 10-Mb/s operation.

Data transfer is accomplished over nibble-wide dedicated transmit and receive channels. When TX_EN is asserted HIGH, data on TXD[3:0] channel is latched into the PHY on the rising edge of TX_CLK and passed to the PCS. If TX_ER is asserted HIGH, an 8B6T code violation word will be sent in place of the transmit data. TX_CLK provides a continuous clock that is sourced from the PHY.

When recovered data is available from the PCS, the RX_DV signal is asserted HIGH simultaneously with the first Start of Frame Delimiter (SFD) nibble on RXD[3:0]. The RX_DV signal remains HIGH continuously through the final recovered nibble of the frame. If an error is detected in the frame by the PHY, the RX_ER signal is driven HIGH synchronously with RX_CLK.

RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER from the PHY to the MAC. RX_CLK is sourced from the PHY. While RX_DV is deasserted, RX_CLK will run at the PHY's nominal frequency. When RX_DV is asserted, the frequency and phase of RX_CLK is recovered from the received data. During the transition from nominal to recovered frequency, the period of RX_CLK may extend by up to one cycle. RX_CLK stretching prevents logic failures from occuring in downstream logic while the clock makes it transition.

When a carrier is detected, the CRS signal is asserted HIGH. A collision is signaled by asserting COL HIGH. CRS is asserted throughout a collision condition.

Access to the management facilities are provided throught the MII with the MDC and MDIO pins. These pins provide a serial interface to the management control and status registers. The MDC signal is driven to the PHY from the management station (STA) as a timing reference for transfer of information on the MDIO signal. The MDIO signal is a bidirectional signal between the PHY and the STA. Control information is driven by the STA to the PHY. Status information is driven from the PHY to the STA.

Media Dependent Interface

The Media Interface is comprised of four communications channels. A dedicated transmit channel, TX_D1±, transmits 100BASE-T4 and 10BASE-T signals. RX_D2± is a dedicated receive channel for both 100BASE-T4 and 10BASE-T signals. The two bidirectional channels for 100BASE-T4 are formed from TX_D3±, RX_D3± and TX_D4±, RX_D4±.

The MDI pins interface to the medium through external resistors and isolation transformers. No external filters are required. The transmit drivers use class AB differential drivers to help reduce power consumption while providing ample drive capability. The drivers have a common mode control circuit to help reduce common mode emissions.

Management

The management facilities are used to control and indicate the status of the PHY resources. The management facilities and MII management interface is compliant with the IEEE 802.3 MII draft specification.

MII Management Interface

The management facilities are accessed through the MII management pins MDC and MDIO. The management facilities respond to register accesses that match the PHY address. The PHY address is assigned with the A[4:0] pins. The value of these pins are latched into the internal PHY address register on the rising edge of $\overline{\text{RESET}}$.

Register accesses are perfomed by transferring an opcode, address, and register number to the PHY management facility. If the address transferred matches the PHY address at the A0–A4 pins, the PHY responds to the access. During a read access, 16 bits of data from the selected register are transferred from the PHY to the STA on the MDIO pin. During a write, 16 bits of data are transferred from the STA to the PHY and written into the selected register.

Control and Status Registers

Control and status information are stored in two 16-bit registers. The Control register is assigned address 0 and the Status register is assigned address 1. *Table 1* shows a map of the Control register and *Table 2* shows the Status register.

Table 1. MII Control Register Definition[2]

Control Register (Register 0)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
0.15	Reset	1 = PHY Reset 0 = Normal Operation	R/W S/C	0	Resets the status and control registers to their default states. Reset is self clearing.
0.14	Loopback	1 = Loopback Mode 0 = Normal Operation	R/W	0	Loopback connects the transmit data path to the receive data path.
0.13	Speed Selection	1 = 100 Mb/s 0 = 10 Mb/s	R/W	1	When Auto-Negotiation is disabled, Speed Select determines the speed of the PHY.
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotation 0 = Disable Auto-Negotiation	R/W	1	This bit enables the Auto-Negotiation function.
0.11	Power Down	1 = Power Down 0 = Normal operation	R/W	0	Power down shuts off the internal PLLs and core logic.
0.10	Isolate[3]	1 = Isolate PHY from MII 0 = Normal Operation	R/W	0, 1	Isolate places the receiver MII channel in high impedence, and the MII transmiter channel does not respond to MII activity.
0.9	RestartAuto-Negotiation	1 = Restart Auto-Negotiation 0 = Normal Operation	R/W S/C	0	Restart Auto-Negotiation breaks the link and restarts the Auto-Negotiation process.
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	0	Duplex Mode selects between full and half duplex operation for 10BASE-T.
0.7	Collision Test	1 = Test COL Signal 0 = Normal Operation	R/W	0	Collision test causes the COL signal to be asserted when TX_EN is asserted.
0.6:0	Reserved			0	

Notes:
2. R/W = Read/Write
   SC = Self Cleaning
   RO = Read Only
   LH = Latched HIGH
3. Isolate default is set by the ISODEF pin.

Table 2. MII Status Register Definition

Status Register (Register 1)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
1.15[4]	100BASE-T4	1 = 100BASE-T4 Able 0 = 100BASE-T4 Able	RO	1,0	When set, this bit indicates that the PHY is 100BASE-T4 capable.
1.14	100BASE-TX Full Duplex	0 = 100BASE-TX Full Duplex Not Supported	RO	0	This bit is always set to zero.
1.13	100BASE-TX Half Duplex	0 = 100BASE-TX Half Duplex Not Supported	RO	0	This bit is always set to zero.
1.12[5]	10BASE-T Full Duplex	1 = 10BASE-T Full Duplex Able 0 = 10BASE-T Full Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T full duplex capable.
1.11[6]	10BASE-T Half Duplex	1 = 10BASE-T Half Duplex Able 0 = 10BASE-T Half Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T half duplex capable.
1.10:6	Reserved	0 = Default	RO	0	
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation Complete 0 = Auto-Negotiation Incomplete	RO	0	This bit is set when NWAY has completed the auto negotiation process.
1.4	Remote Fault	1 = Remote Fault Condition 0 = No Remote Fault Condition	RO	0	This bit is set when Auto Negotiation detects a remote fault.
1.3[7]	Auto Negotiation Ability	1 = PHY is Able to Perform Auto Negotiation	RO	1,0	PHY supports Auto-Negotiation.
1.2	Link Status	1 = Link Is Up 0 = Link Is Down	RO	0	Link Status indicates that the PHY is in the Link Pass State.
1.1	Jabber Detect	1 = Jabber Condition Detected 0 = No Jabber Condition Detected	RO LH	0	Jabber Detect indicates that a jabber condition has been detected for 10BASE-T.
1.0	Extended Capabilities	1 = Extended Register Capable	RO	1	OUI and Auto-Negotiation Extended Registers 2–7 are present.

Vendor and Product ID Registers

Vendor and Product identification codes are stored in management ID registers 2 and 3. These registers contain the Cypress Semiconductor Corporation unique identifier and the CY7C971 product and revision number. *Table 3* explains the ID registers.

Auto-Negotation Registers

The Auto-Negotation process is managed through the Auto-Negotation registers. Register 4 is the Auto-Negotation Advertisement register. This register contains the 16-bit code word that is advertised to the remote link partner. Register 5 is the Auto-Negotation Link Partner Ability register for base and next pages. This register holds the 16-bit code word that the Auto-Negotation function receives from the remote link partner. Register 6 is the Auto-Negotation Expansion register and is used to monitor the negotiation process. Register 7 is the Auto-Negotation Next Page Transmit register. The function of the Auto-Negotation register bits are defined in *Tables 4* through 7.

Auto-Negotation

The IEEE Auto-Negotation function provides remote capability detection and automatic speed selection. Auto-Negotation is fully compatible with existing 10BASE-T only devices.

Auto-Negotation advertises the capabilities of the PHY by transmitting a sequence of fast link pulses (FLPs) that form a standard 16-bit code word. The advertised code word is contained in the Auto-Negotation Advertisement register (Register 4). Auto-Negotation receives 16-bit code words and stores them in the Auto-Negotation Partner Ability register (Register 5). Once the code words have been sent and acknowledged, Auto-Negotation selects the highest common operating mode as the current mode of operation. The highest common mode of operation is determined by the Priority Resolution Table specified in the Auto-Negotation standard. When a mode of operation is selected, Auto-Negotation enables the transition to the selected mode's Link Pass state.

The Auto-Negotation process is controlled and monitored through the MII management registers. Auto-Negotation may be disabled in the MII control register or by asserting the AUTONEG pin HIGH.

The Auto-Negotation is capable of transmitting and receiving code word pages in addition to the base pages. The next page process is controlled through the MII registers.

Notes:
4. 100BASE-T4 Default is set by the ENT4 pin.
5. 10BASE-T FD Default is set by the ENTFD pin.
6. 10BASE-T HD Default is set by he ENT pin.
7. Auto-Negotiation Default is set by the AUTONEG pin.

Table 3. MII PHY ID Register Definition

PHY Identifier (Register 2 and 3)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
2.15:0	OUI PHY Identifier	16 Most Significant OUI Bits	RO	0028h	This field contains 16 bits of the Cypress Organizationally Unique Identifier (OUI).
3.15:10	OUI PHY Identifier	6 Least Significant OUI Bits	RO	02h	This field contains 6 bits of the Cypress Organizationally Unique Identifier (OUI).
3.9:4	Model Number	CY7C971 Model Number	RO	01h	This field contains a 6-bit model number.
3.3:0	Revision Number	CY7C971 Revision Number	RO	–	This field contains a 4-bit revision number.

Table 4. MII Auto-Negotation Advertisement Register Definition

Auto-Negotation Advertisement Register (Register 4)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
4.15	Next Page	1 = Next Page to be Transmitted 0 = No Next Page	R/W	0	When set, this bit will cause the PHY to advertise Next Page capability.
4.14	Reserved		RO	0	Reserved.
4.13	Remote Fault	1 = Fault Indication 0 = No Fault	R/W	0	When set, this bit will cause the PHY to advertise a Remote Fault has occured.
4.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.9[8]	Technology Ability Field 100BASE-T4	1 = Advertise 100BASE-T4 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 100BASE-T4 capability. This bit may only be set if 100BASE-T4 is enabled.
4.8	Technology Ability Field 100BASE-TX Full Duplex	0 = 100BASE-TX FD Not Supported	RO	0	This bit will always be zero. 100BASE-TX FD is not supported.
4.7	Technology Ability Field 100BASE-TX	0 = 100BASE-TX Not Supported	RO	0	This bit will always be zero. 100BASE-TX is not supported.
4.6[9]	Technology Ability Field 10BASE-T Full Duplex	1 = Advertise 10BASE-T FD 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 10BASE-T FD capability. This bit may only be set if 10BASE-T FD is enabled.
4.5[10]	Technology Ability Field 10BASE-T	1 = Advertise 10BASE-T 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 10BASE-T capability. This bit may only be set if 10BASE-T is enabled.
4.4:0	Selector Field	Indicates IEEE 802.3 LAN	RO	01h	This field is permanently set to 0001 to advertise IEEE 802.3 CSMA/CD LAN.

Notes:
8. 100BASE-T4 Advertised Ability default is set by the ENT4 pin.
9. 10BASE-T FD Advertised Ability default is set by the ENTFD pin.
10. 10BASE-T Advertised Ability default is set by the ENT pin.

Table 5. MII Auto-Negotation Link Partner Ability Register Definition

Auto-Negotation Link Partner Ability Register (Register 5)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
5.15	Remote Next Page	1 = Next Page to be Transmitted 0 = No Next Page	RO	0	When set, this bit indicates the remote PHY has a Next Page to send.
5.14	Remote Acknowledge	1 = Remote Acknowledge 0 = No Acknowledge	RO	0	When set, this bit indicates that the remote PHY has acknowledged receipt of a page.
5.13	Remote Fault	1 = Fault Indication 0 = No Fault	RO	0	When set, this bit indicates that a fault has ocurred in the remote PHY.
5.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.9	Technology Ability Field 100BASE-T4	1 = 100BASE-T4 Able 0 = Not 100BASE-T4 Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-T4 capability.
5.8	Technology Ability Field 100BASE-TX Full Duplex	1 = 100BASE-TX FD Able 0 = Not 100BASE-TX FD Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX FD capability.
5.7	Technology Ability Field 100BASE-TX	1 = 100BASE-TX Able 0 = Not 00Base-TX Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX capability.
5.6	Technology Ability Field 10BASE-T Full Duplex	1 = 10BASE-T FD Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T FD capability.
5.5	Technology Ability Field 10BASE-T	1 = 10BASE-T Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T capability.
5.4:0	Selector Field	Indicates LAN Type	RO	00h	This field indicates the type of LANs being advertised by the remote PHY.

Table 6. MII Auto-Negotation Expansion Register Definition

Auto Negotiation Expansion Register (Register 6)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
6.15:5	Reserved	Reserved	RO	0	Reserved.
6.4	Parallel Detection Fault	1 = Parallel Detection Fault 0 = No Parallel Detection Fault	RO LH	0	When set, this bit indicates that local Auto-Negotation has detcted more than one valid link.
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is Not Next Page Able	RO	0	When set, this bit indicates that the remote PHY supports Next Page capability
6.2	Next Page Able	1 = Next Page Able	RO	1	This bit indicates that local Auto-Negotation supports Next Page capability.
6.1	Page Received	1 = 3 Identical Code Words Received 0 = 3 Identical Code Words Have Not Been Received	RO LH	0	When set, this bit indicates that local Auto-Negotation has received three consecutive and identical code words.
6.0	Link Partner Auto Negotiation Able	1 = Link Partner is Auto-Negotiation Able 0 = Link Partner is Not Auto-Negotiation Able	RO	0	When set, this bit indicates that the remote PHY has Auto-Negotation capability.

Table 7. MII Auto-Negotation Next Page Transmit Register Definition

Auto-Negotation Next Page Transmit Register (Register 7)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
7.15	Next page	1 = More Pages Follow 0 = Last Page	R/W	0	When set, this bit indicates that more pages follow. When clear, it indicates that the last page is being sent.
7.14	Reserved		RO	0	
7.13	Message Page	1 = Message Page 0 = Unformatted Page	R/W	0	When set, this bit indicates that the next page being sent is formatted as a message page.
7.12	Acknowledge 2	1 = Will Comply 0 = Cannot Comply	RO	1	When set, this bit indicates that the device can comply with the received message.
7.11	Toggle	1 = Previous Toggle Was Zero 0 = Previous Toggle Was One	RO	0	This bit is used to ensure synchronization with the link partner during next page exchange.
7.10:0	Message/Unformatted Code Field	Eleven-Bit Field	R/W	000h	This field contains the message/unformatted bits for the next page.

Loopback

In Loopback Mode, the transmit PMA circuits are isolated from the media and are connected to the receive PMA circuits. Transmit data flows from the MII through the PCS and into the PMA. The serial data is then looped back through the Receiver PMA and PCS to the MII interface. Loopback Mode is useful for checking the integrity of the PHY and MAC operations.

Loopback Mode is enabled by either setting the Loopback bit in the Management Control register to one or by asserting the $\overline{\text{LOOP}}$ pin LOW.

PMA Mode

When the MODE pin is LOW, the CY7C971 is in 100BASE-T4 PMA mode. This mode of operation is intended for use in repeater applications. In PMA mode, the PCS is bypassed exposing the PMA sublayer. Binary encoded 6T symbols are transfered directly over the PMA interface pins. This reduces the transmitter latency for use in class 1 and class 2 repeaters. A block diagram of the PMA interface is shown in *Figure 5*. 10BASE-T is disabled in the Status register.

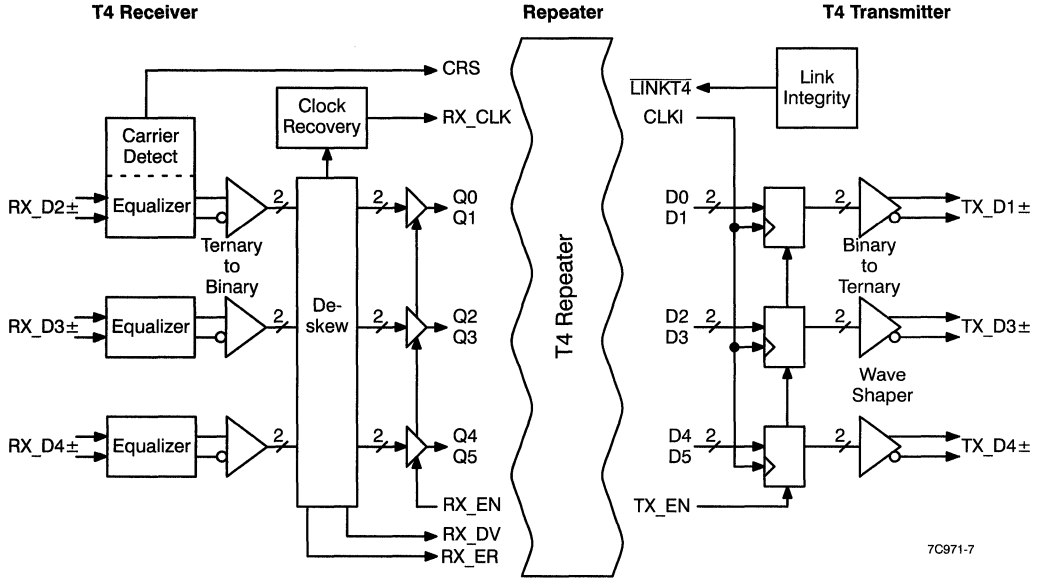


Figure 5. T4 Transmitter & Receiver PMA Interface and Block Diagram (MODE = LOW)

Serial 6T data from the three PMA circuits are transferred over the PMA interface pins in binary form. The Receiver aligns and converts the line signals to their 6T binary representation and drives them to the Q[5:0] pins. The transmitter latches the three 6T symbol streams on its D[5:0] input pins on the rising edge of TX_CLK. The 6T symbols are loaded into the waveshaper DAC and converted to their corresponding ternary waveforms. *Table 8* shows the mapping of binary PMA signals to ternary waveforms.

Table 8. PMA Binary to Ternary Map[11]

PMA Q1–0, Q3–2, Q5–4 D1–0, D3–2, D5–4	Transmitter	Receiver
00	CS0	CS0
10	CS1	CS1
01	CS–1	CS–1
11	CS0	–

Notes:
11. CS0 is a waveform which conveys the ternary symbol 0.
CS1 is a waveform which conveys the ternary symbol 1.
CS–1 is a waveform which conveys the ternary symbol –1.

The RX_DV signal indicates when the first data symbol after sosb is present on the Q0–5 PMA interface pins. RX_DV will remain HIGH throughout the transfer of data symbols across the PMA interface. RX_DV is LOW when there is no carrier present. RX_ER HIGH indicates a pair alignment error. The RX_EN input pin enables the Q0–5, RX_DV, and RX_ER drivers. RX_EN LOW places the drivers in the high-impedence state.

The transmit PMA interface is synchronous to the CLKI input clock signal. The TX_EN HIGH causes data on the PMA D0–5 pins to be loaded into the transmit PMA waveshaper on the rising edge of CLKI. When TX_EN is LOW, the output drivers transmit the CSO idle symbols.

Applications

The CY7C971 is a flexible physical-layer device that fits into any Ethernet application including network interface cards, transceiver cards, repeaters, hubs and switches. *Figure 6* shows a schematic of the CY7C971 configured for a transceiver card application with an exposed MII port.

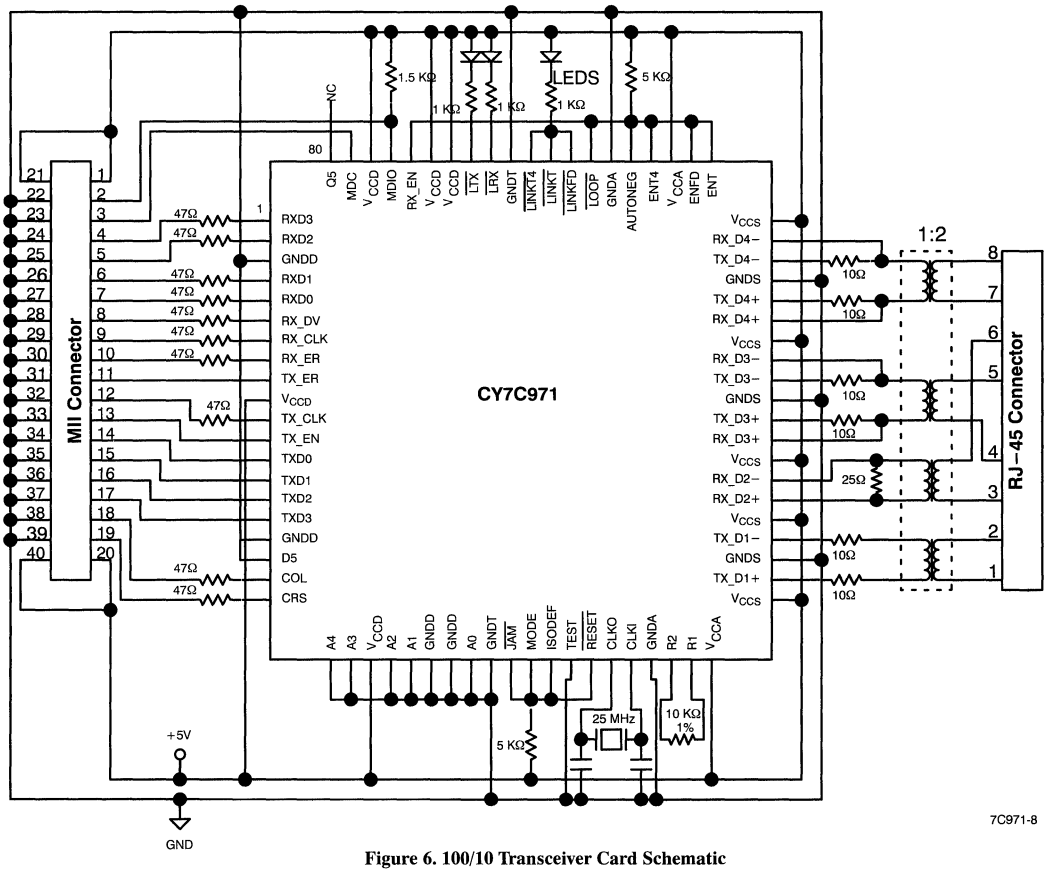


Figure 6. 100/10 Transceiver Card Schematic

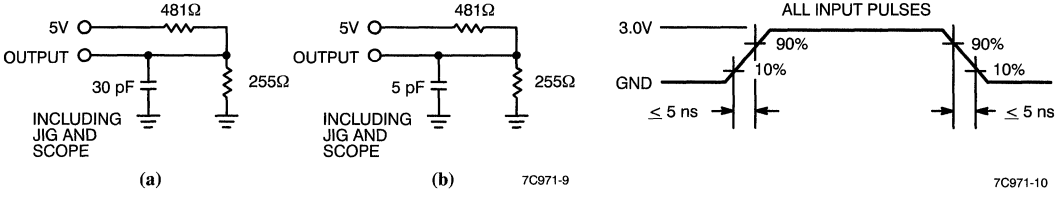
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
TTL Pins					
V_{OHT}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OLT}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IHT}	Input HIGH Voltage		2.0	6.0	V
V_{ILT}	Input LOW Voltage		−3.0	0.8	V
I_{IXT}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_{OZT}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	+50	μA
I_{OST}	Output Short Circuit Current[12]	V_{CC} = Max., V_{OUT} = GND		−350	mA
Open Drain LED Pins					
V_{OLD}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4	V
Miscellaneous					
I_{CC1}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, 100BASE-T4 transmitting		300	mA
I_{CC2}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, 100BASE-T4 not transmitting		100	mA
I_{SB}	Power-Down Current	Max. V_{CC}		TBD	mA

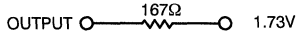
Capacitance[13]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:
12. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
13. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	Min.	Max.	Unit
MII Timing				
$t_{TCPWHT4}$	TX_CLK Pulse Width HIGH (T4)	14	26	ns
$t_{TCPWLT4}$	TX_CLK Pulse Width LOW (T4)	14	26	ns
t_{TCPWHT}	TX_CLK Pulse Width HIGH (T)	194	206	ns
t_{TCPWLT}	TX_CLK Pulse Width LOW (T)	194	206	ns
t_{TDS}	TXD Set Up	10		ns
t_{TDH}	TXD Hold	0		ns
t_{TMIIT4}	Transmit Latency (T4)		110	ns
t_{TMIIT}	Transmit Latency (T)		500	ns
$t_{TCRSHT4}$	Transmit Path CRS Assert (T4)		20	ns
t_{TCRSHT}	Transmit Path CRS Assert (T)		20	ns
$t_{TCRSLT4}$	Transmit Path CRS Deassert (T4)		320	ns
t_{TCRSLT}	Transmit Path CRS Deassert (T)		100	ns
$t_{RCPWHT4}$[15]	RX_CLK Pulse Width HIGH	14	26	ns
$t_{RCPWLT4}$[15]	RX_CLK Pulse Width LOW	14	26	ns
t_{RCPWHT}[15]	RX_CLK Pulse Width HIGH	194	206	ns
t_{RCPWLT}[15]	RX_CLK Pulse Width LOW	194	206	ns
t_{RDV}	RXD Valid from Clock		18	ns
t_{RDH}	RXD Hold from Clock	10		ns
t_{RXDVT4}	RXD Valid Latency (T4)		870	ns
t_{RXDVT}	RXD Valid Latency (T)		500	ns
$t_{RXDATAT4}$	RXD Latency (T4)		950	ns
$t_{RXDATAT}$	RXD Latency (T)		8700	ns
t_{RHZD}	RX_EN HIGH to Valid Data		15	ns
t_{RDHZ}	RX_EN LOW to High Impedance		20	ns
100BASE-T4 CRS and COL				
t_{CRSH}[16]	CRS Assert Latency for Preamble	110	140	ns
t_{CRSLC}[17]	CRS Deassert Latency for EOC		370	ns
t_{CRSLE}[18]	CRS Deassert Latency for EOP		370	ns
t_{COLH1}[19]	COL Assert Latency from TX_EN HIGH		20	ns
t_{COLL1}[20]	COL Deassert Latency from TX_EN LOW		20	ns
t_{COLH2}[21]	COL Assert Latency from Preamble		190	ns
t_{COLL2}[22]	COL Deassert Latency from EOC or EOP		370	ns

Notes:

14. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
15. During clock transition, clock max time could be as long as an entire cycle.
16. t_{CRSH} is measured from the rising edge of the latest arriving signal of the three pair that meets the 100BASE-T4 squelch criterion to the rising edge of CRS. The rising and falling edges of CRS are guarenteed to meet the fairness timing specification defined in the 100BASE-T4 standard.
17. t_{CRSLC} is measured from the end of the last data symbol on RX_D2 to the falling edge on CRS. Seven consecutive zeros must be received on RX_D2 in order for the PMA to recognize loss of carrier.
18. t_{CRSLE} is measured from the begining of the first symbol of EOP1 on any RX_Dx MDI pair accounting for skew to the falling edge on CRS. Detection of a properly framed EOP1 will cause the PCS to recognize loss of carrier.
19. t_{COLH1} is measured from the rising edge of TX_CLK while TX_EN is HIGH to the rising edge of COL.
20. t_{COLL1} is measured from the rising edge of TX_CLK while TX_EN is LOW to the falling edge of COL.
21. t_{COLH2} is measured from the rising edge of the signal on RX_D2 that meets the 100BASE-T4 unsquelch criterion to the rising edge of COL.
22. t_{COLL2} is measured from the first symbol of the EOP or EOC sequences to the falling edge of COL.

Switching Characteristics Over the Operating Range (continued)

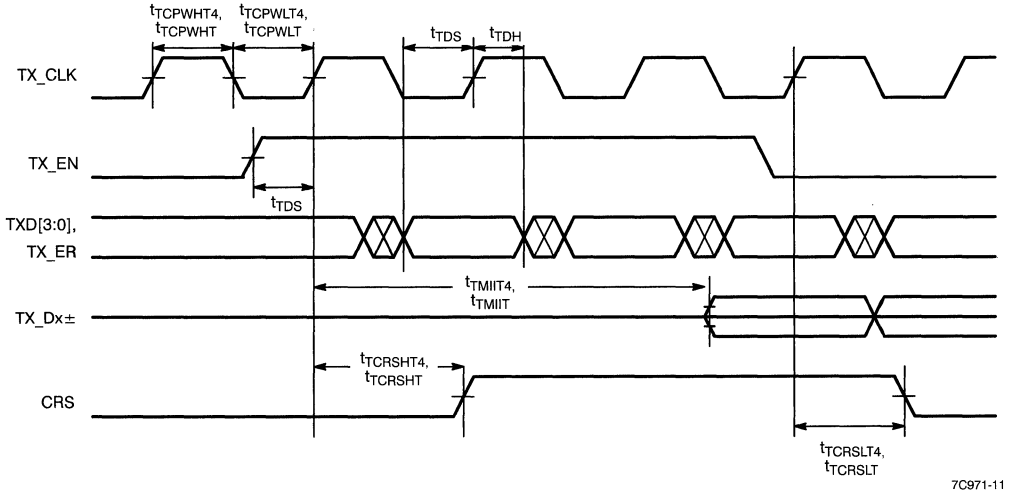
Parameter	Description	Min.	Max.	Unit
10BASE-T CRS and COL				
t_{CRSH3}[23]	CRS Assert Latency		500	ns
t_{CRSL3}[24]	CRS Deassert Latency		500	ns
Management Timing				
t_{MCPWH}	MDC Pulse Width HIGH	25		ns
t_{MCPWL}	MDC Pulse Width LOW	25		ns
f_M	MDC Frequency		12.5	MHz
t_{MDS}	MDIO Set-Up	10		ns
t_{MDH}	MDIO Hold	0		ns
t_{MDO}	MDIO Valid from Clock		40	ns
t_{MDOH}	MDIO Hold from Clock	0		ns
t_{MDHZ}	MDC to High Impedance		40	ns
t_{MDLZ}	MDC to Low Impedance	0	20	ns
Control and Status Timing				
t_{RL}	Reset Pulse Width LOW	5		µs
t_{RS}	Control Input Set-Up	100		ns
PMA Interface Timing				
t_{TPMA}	PMA Transmit Latency		40	ns
t_{TDS}	PMA Transmit Data Set Up	10		ns
t_{TDH}	PMA Transmit Data Hold	0		ns
$t_{PMACRSH}$	PMA CRS Assert Latency	110	140	ns
$t_{PMACRSL}$	PMA CRS Deassert Latency		650	ns
$t_{PMADATA}$	PMA Receiver Data Latency		800	ns
Clock Timing				
t_{CPWH}	Reference Clock Pulse Width HIGH	16	24	ns
t_{CPWL}	Reference Clock Pulse Width LOW	16	24	ns
f_C	Reference Clock Frequency	25 − 100 ppm	25 + 100 ppm	MHz

Notes:

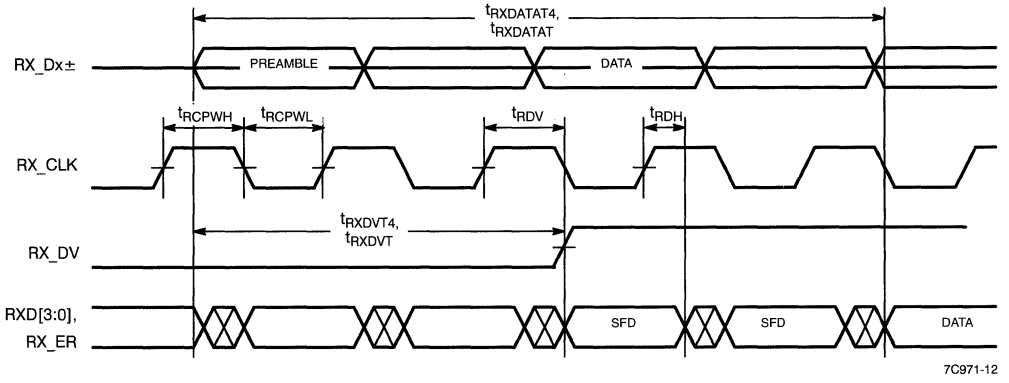
23. t_{CRSH3} is measured from the rising edge of the signal on RX_D2 that meets the 10BASE-T carrier criterion to the rising edge of $\overline{CRS}$.
24. t_{CRSL3} is measured from th eend of the last data symbol on RX_D2 to the falling edge of CRS.

Switching Waveforms

MII Transmit Port Data Timing[25]



MII Receive Port Data Timing[26, 27]

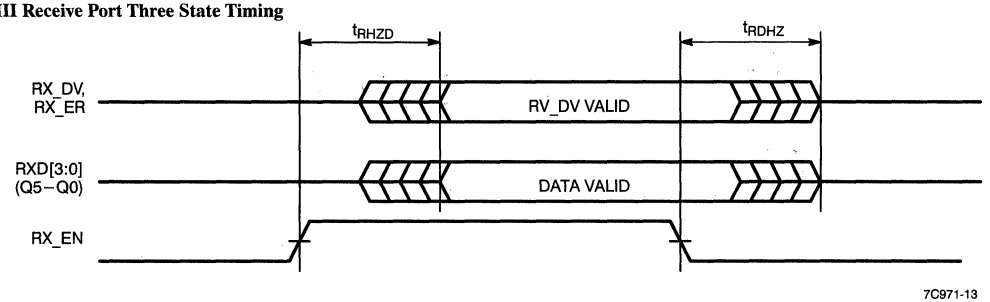


Notes:

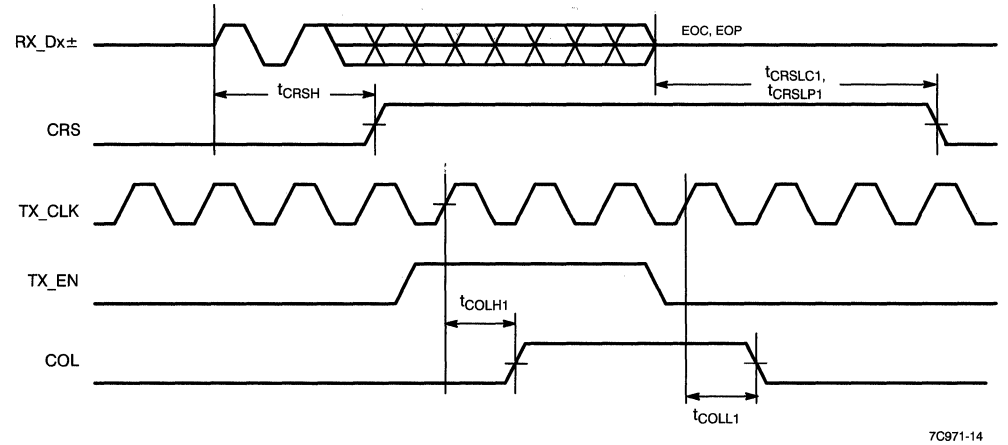
25. t_{MII} is measured from the rising edge of TX_CLK to the 50% point of the TX_Dx± outputs at the MDI pins.
26. t_{RXDV} is measured from the first rising edge of the preamble at the MDI input pins to the rising edge of RX_DV. This includes up to 64 bits of preamble and SFD plus the latency of the receive circuitry.
27. t_{RXDATA} is measured from the first rising edge of the preamble at the MDI input pins to the rising edge of valid data at the RXD pins. This includes up to 64 bits of preamble and SFD plus the first 8 bits of data and the latency of the receive circuitry.

Switching Waveforms (continued)

MII Receive Port Three State Timing

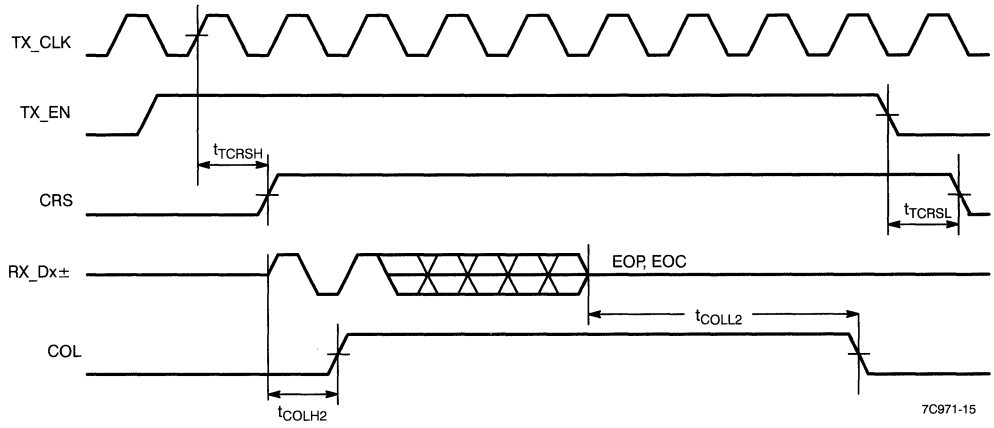


MII Carrier Sense and Collision (100BASE-T4)

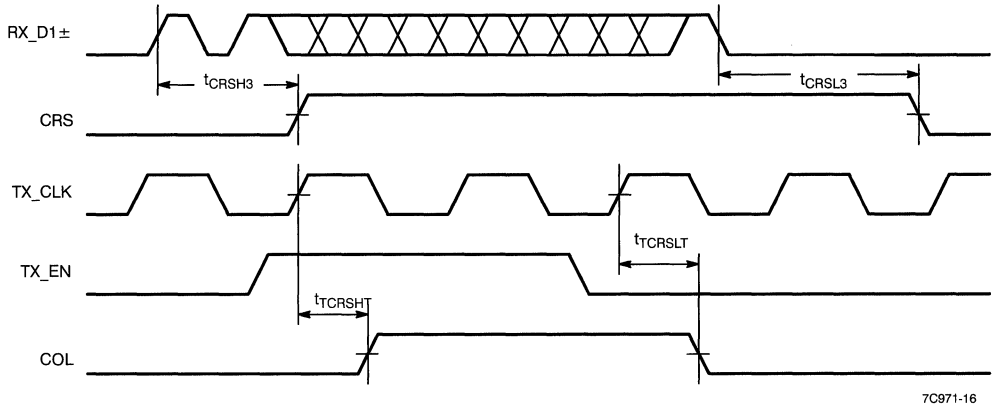


Switching Waveforms (continued)

MII Carrier Sense and Collision (100BASE-T4)



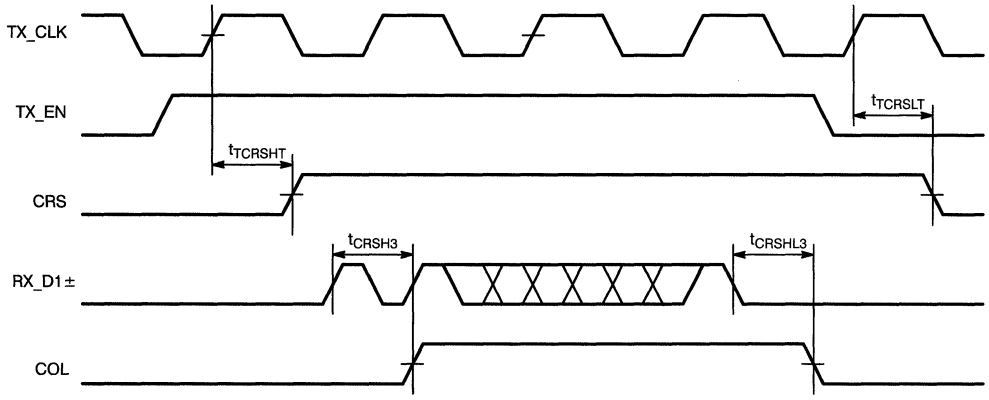
MII Carrier Sense and Collision (10BASE-T) [28]



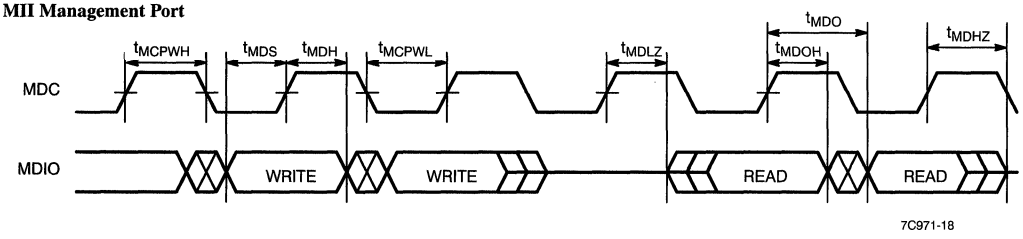
Notes:
28. Switching waveforms show CRS and COL timing for a colision that is started and terminated by the transmit path (TX_EN HIGH).

Switching Waveforms (continued)

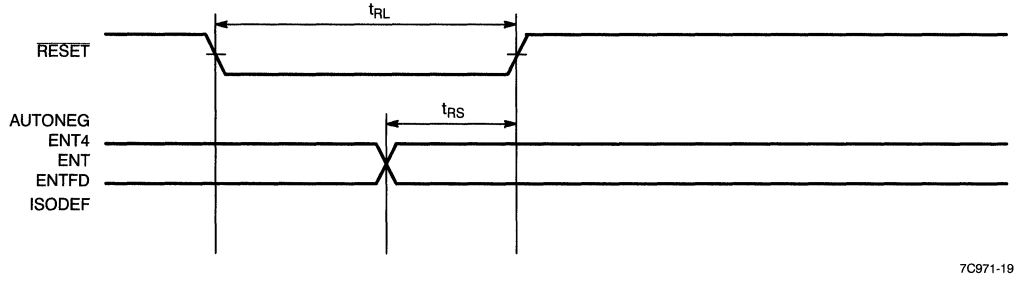
MII Carrier Sense and Collision (10BASE-T) [29]



MII Management Port



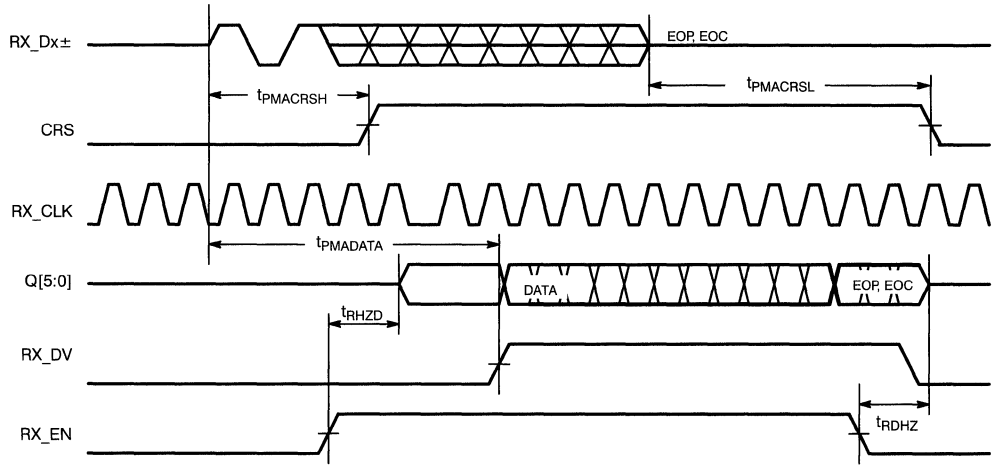
Control and Status Pins



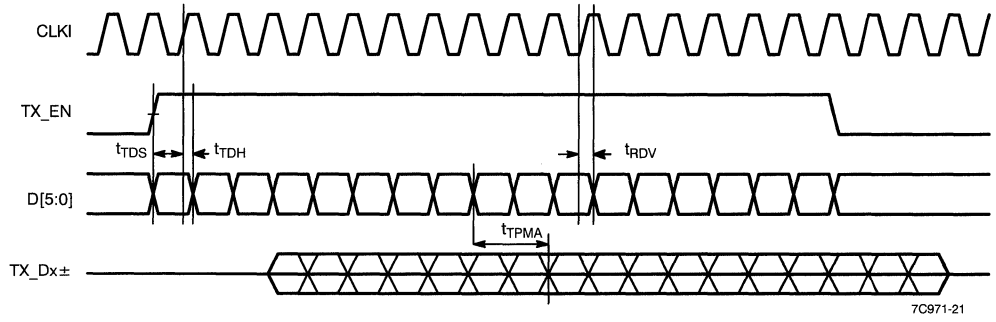
Notes:
29. Switching waveforms show CRS and COL timing for a collision that is started and terminiated by activity on the receive path.

Switching Waveforms (continued)

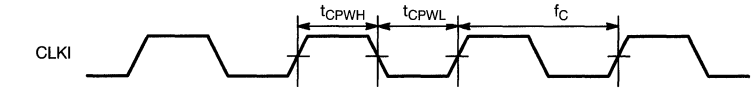
PMA Receiver Interface (MODE = LOW)



PMA Transmitter Interface (MODE = LOW)



Reference Clock Pins



Document #: 38−00415

100BASE-TX/10BASE-T Fast Ethernet Transceiver

Features

- **Complies with IEEE 802.3u standard**
- **Four Operating Modes:**
  - **—100BASE-TX**
  - **—100BASE-TX Full Duplex**
  - **—10BASE-T**
  - **—10BASE-T Full Duplex**
- **Media Independent Interface (MII)**
  - **—Three-state receive port**
  - **—Serial management port**
- **Auto-Negotiation**
- **MLT-3 Transmitter/Receiver for 100BASE-TX**
- **Cat. 5 twisted-pair adaptive equalizer for 100BASE-TX**
- **PMA interface for repeater applications**
- **LED status indicators: TX, RX, Link**
- **Loopback mode for PHY integrity testing**
- **80-pin PQFP**

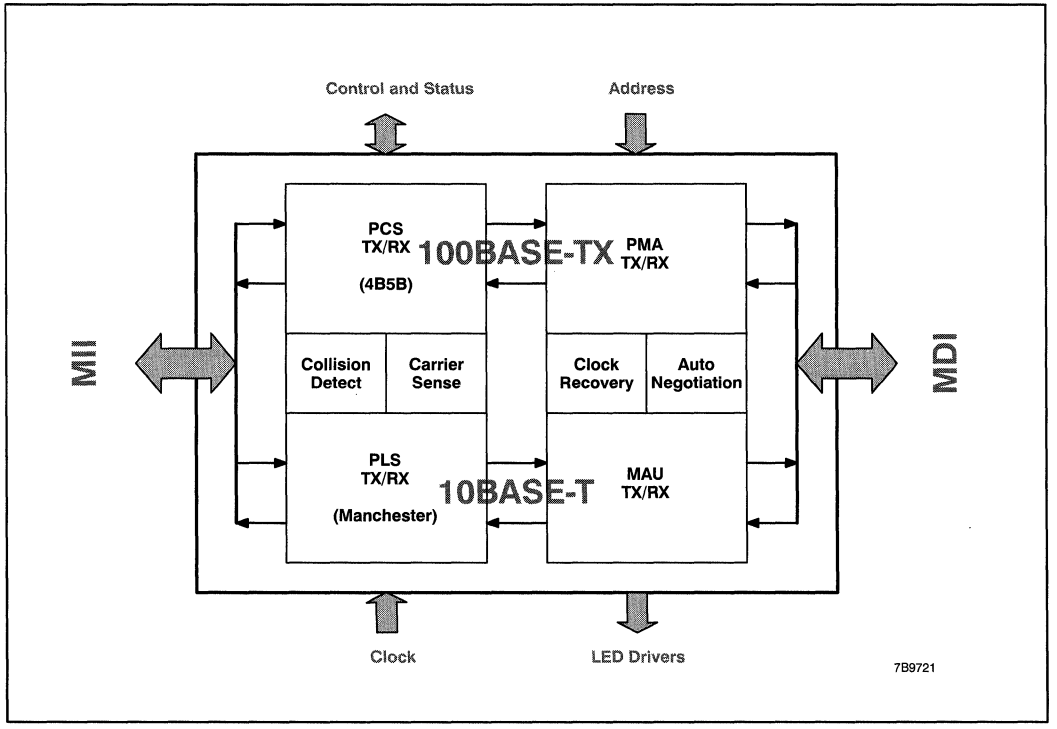
Functional Description

The CY7B972 is a full featured physical layer transceiver (PHY) device supporting both 100BASE-TX (Fast Ethernet) and 10BASE-T Local Area Network (LAN) standards. The CY7B972 complies with IEEE 802.3 100BASE-TX, 10BASE-T, Auto-Negotiation and MII standards.

The CY7B972 interfaces to two pair of category 5 unshielded twisted-pair cable or fiber. The Media Independent Interface (MII) attaches directly to 802.3 Media Access Control (MAC) layer devices.

The CY7B972 performs the Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Physical Layer Signalling (PLS), and Media Attachment Unit (MAU) functions defined in the 802.3 standard for 100BASE-X and 10BASE-T. Ethernet frames are transferred from the MAC to the CY7B972 over the MII interface. The data is encoded in the PCS or PLS encoder (4B5B for 100BASE-TX or Manchester for 10BASE-T) and then passed to the PMA or MAU where the serial encoded data is shifted bitwise on to the twisted pair media. Collision and Carrier Detect signals are generated by the CY7B972 and passed to the MAC over the MII.

The CY7B972 PHY uses 802.3 standard Auto-Negotiation to configure the twisted-pair link. The CY7B972 also includes a direct interface to the PMA layer for repeater applications.



Document #: 38–00453

Ethernet Coax Transceiver Interface

Features

- **Compliant with IEEE 802.3 10BASE5 and 10BASE2**
- **Pin compatible with the popular 8392**
- **Internal squelch circuit to eliminate input noise**
- **Receive/transmit mode collision detect for extended distance**
- **Automatic AUI port isolation when coaxial connector is not present**
- **Low power BiCMOS design**

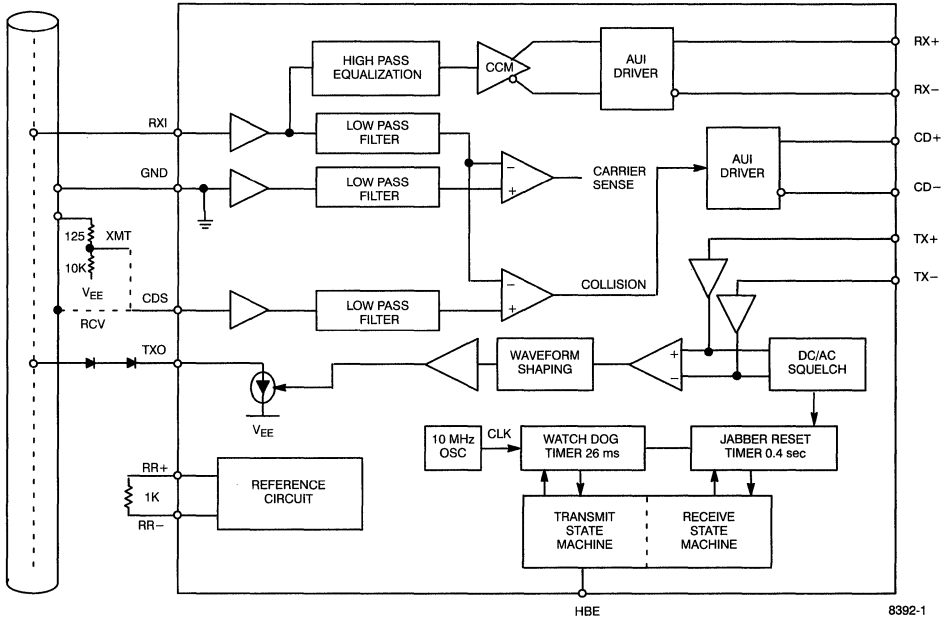
Functional Description

The CY7B8392 is a low power coaxial transceiver for Ethernet 10BASE5 and 10BASE2 applications. The device contains all the circuits required to perform transmit, receive, collision detection, heartbeat generation, jabber timer and attachment unit interface (AUI) functions. In addition, the 7B8392 can also be used in a transmit collision detect mode.

The transmitter output is connected directly to a double terminated 50Ω cable.

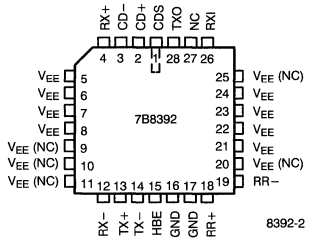
The CY7B8392 is fabricated with an advanced low power BiCMOS process. Typical standby current during idle is 25 mA.

Logic Block Diagram

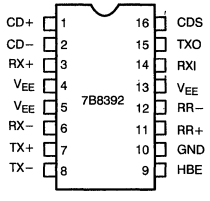


Pin Configurations

PLCC
Top View



DIP
Top View



Pin Description

Pin Number		Pin Name	Description
16-Pin DIP	28-Pin PLCC		
1 2	2 3	CD+ CD−	AUI Collision Output pins. Differential driver that transmit a 10-MHz signal during collision events, jabber and CD Heartbeat conditions. Also referred to as CI port.
3 6	4 12	RX+ RX−	AUI Receive Output pins. Differential driver that outputs the signal receive from the line. Also referred to as DI port.
7 8	13 14	TX+ TX−	AUI Transmit Input pins. Differential receiver that inputs the signal for transmission onto the cable.
9	15	HBE	Heartbeat Enable Pin. When this pin is grounded, the heartbeat is enabled. When the pin is connected to V_{EE}, the heartbeat is disabled.
11 12	18 19	RR+ RR−	External Resistor. A 1K 1% resistor should be connected between these pins to establish proper internal operation current.
14	26	RXI	Receive Input. This pin is connected directly to the coaxial cable.
15	28	TXO	Transmitter Output. This pin is connected directly (10BASE2 thin wire) or through a diode to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to prevent ground drops from altering the receive mode collision detect threshold.
10	16,17	GND	Positive Power Supply Pin.
4,5,13	5−11 20−25	V_{EE}	Negative Power Supply Pin.

CY7B8392 Description

Transmitter

The CY7B8392 transfers Manchester-encoded data from the AUI port of the DTE (TX+ and TX−) to the coaxial cable. The output waveform is wave shaped to meet IEEE 802.3 specifications. For Ethernet compatible applications (10BASE5), an external isolation diode may be added to further reduce the coax load capacitance.

The AUI squelch circuit prevents signals with less than 15 ns pulse width or smaller than 175 mV average dc level from reaching the output driver. The squelch circuit also turns the transmitter off at the end of the packet if the average of the dc level of the signal stays greater than 175 mV for more than 190 ns.

Receiver

The CY7B8392 receiver transfers the serial data from the coaxial cable to the DTE via the balanced differential output (RX+ and RX−). The received signal is amplified and equalized by the on chip equalizer.

The device also contains an internal squelch function that discriminates noise from valid data. A 4-pole Bessel filter is used to extract the DC level of the received signal. If the DC level of the received signal is lower than an internally set squelch threshold, the CY7B8392 receive function will not be activated.

Collision Detection

The collision detection circuit monitors the signal level on the coax cable. This signal voltage level is compared against the collision voltage threshold V_{CD}. When the measured signal level is more negative than V_{CD}, a collision condition is declared by the CY7B8392 by sending a 10-MHz signal over the CD+/CD− pair.

Long Cable Application

The IEEE 802.3 standard is designed for 500 meters of Ethernet cable and 185 meters of thin coax cable (RG58A/U). To extend the cable segment to 1000 meters and 300 meters of Ethernet cable and thin coaxial cable respectively, transmit collision detection mode is required. The disadvantage of the transmit collision detection mode is that it will detect collision only when the station is transmitting; it will not be able to detect collision of two far-end stations when it is not transmitting. Note that transmit mode collision detection is not allowed in repeater applications.

Implementation of transmit mode collision detection with CY7B8392 is simple. By connecting an external resistor divider to the CDS pin; R1 to 150 ohms and R2 to 10 Kohms, the device is now in transmit collision detection mode.

The CY7B8392 utilizes a combination receive and transmit mode collision detection. When the device is idle it enters into receive collision detection mode, and when it is transmitting it is in the transmit collision detection mode.

Heartbeat Test Function

The Heartbeat Test Function is enabled when the HBE pin is tied to ground. When enabled, a 10-MHz collision signal is transmitted to the MAC over the CD+/CD− pair after the transmission of a packet for 10±5BT[1]. The Heartbeat function should be disabled by tying the HBE pin to V_{EE} for repeater applications.

Note:
1. BT = Bit Time = 100 ns.

Jabber Function

The on-chip watchdog timer prevents the DTE from locking up a network by transmitting continuously. When the transmission exceeds the jabber time limit, the Jabber function disables the transmitter and sends a 10-MHz signal over the CD± pair. Once the transmitter is in the jabber state, it must remain in the idle state for 500 ms before it will exit the jabber state.

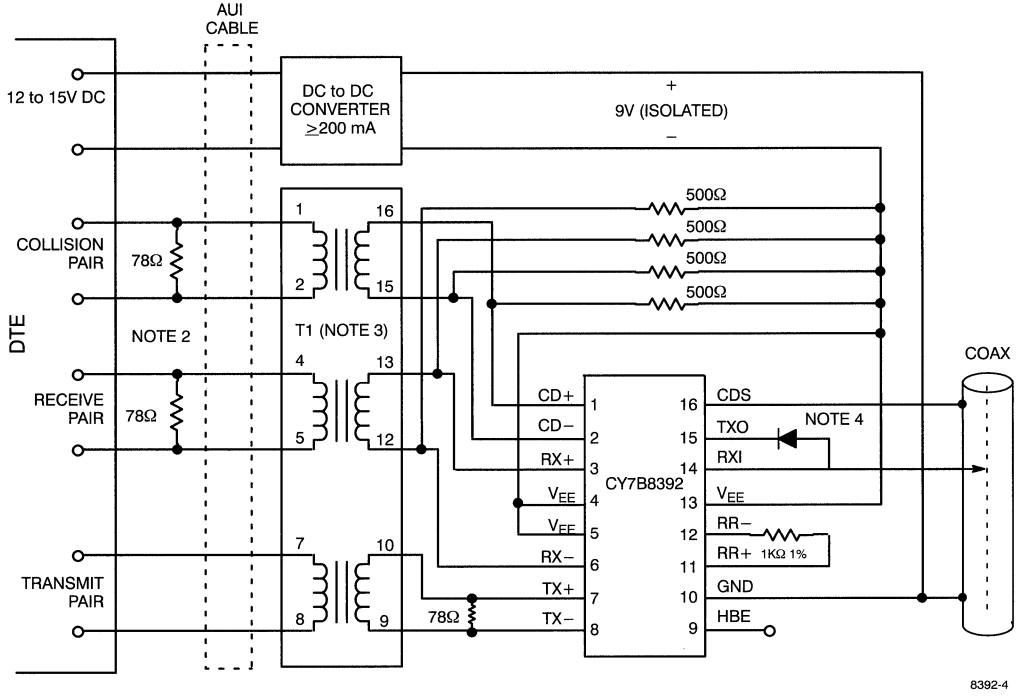
Auto AUI Selection Function

Initially, during power-up the CI and DI ports of the AUI are high impedance. If the RXI port is not connected to a coaxial segment, the AUI port will remain in high impedance. The AUI port will only be activated when RXI is connected to a coaxial segment.

When the connector is removed from the CY7B8392 (after power-up), a 10-MHz signal is transmitted over the CI circuit for 800 ms with the DI port disabled. After the transmission of the 10-MHz signal, the CI port is disabled.

This function allows multiple MAUs to be connected to a single AUI port without having to turn off the coaxial transceiver manually.

Connection Diagram for Standard CY7B8392 Applications



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage ..... −12V

Input Voltage ..... GND+0.3V to V_{EE}−0.3V

Operating Range

Range	Ambient Temperature	V_{EE}
Commercial	0°C to +70°C	−9V ± 5%

Notes:

2. 78Ω resistors not required if AUI cable not present.
3. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100 µH.
4. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

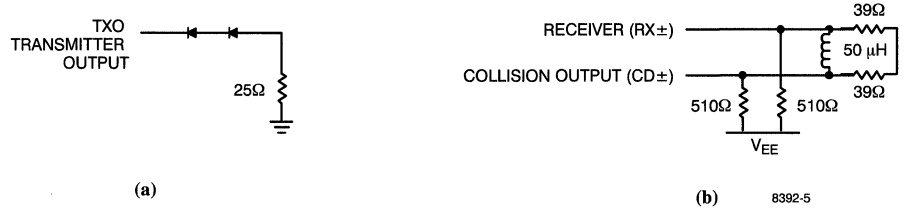
Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Min.	Typ.	Max.	Unit
V_{EE}	Supply Voltage	−8.55	−9.0	−9.45	V
I_{EE1}	(V_{EE} to GND) Non-transmitting		−25	−35	mA
I_{EE2}	(V_{EE} to GND) Transmitting		−70	−80	mA
I_{RXI}	Input Bias Current (RXI pin)	−2		25	µA
I_{TDC}	Transmitter Output DC Current	37	41	45	mA
I_{TAC}	Transmitter AC Current	±28			mA
V_{CD}	Collision Threshold	−1.45	−1.53	−1.62	V
V_{CS}	Carrier Sense Threshold	−0.38	−0.45	−0.52	V
RX, C, D	Differential Output Voltage	±500		±1500	mV
V_{OC}	Common Mode Voltage[6]	−1		−3	V
V_{TS}	Transmitter Squelch Threshold[7]	−175	−225	−300	mV
R_{RXI}	Shunt Resistance—Non-transmitting	100			KΩ
T_{TXO}	Shunt Resistance—Transmitting	10			KΩ

Capacitance

Parameter	Description	Test Conditions	Typ.	Unit
C_X	Input Capacitance		1.5	pF

AC Test Loads and Waveforms



Notes:
5. Testing is done under test load as defined in AC Test Loads and Waveforms.
6. During idle, V_{OC} is pulled down to V_{EE} to minimize the power dissipation across the load resistors connected to RX± and CD±.
7. For a minimum pulse width of >40 ns.

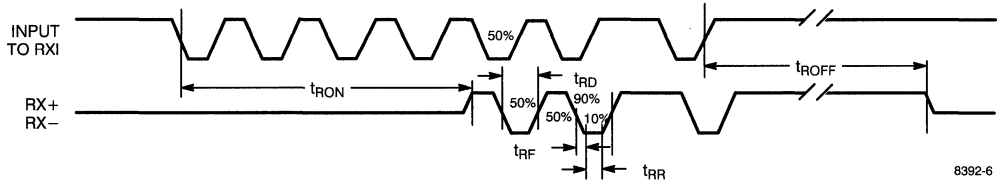
Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Typ.	Max.	Unit
t_{RON}	Receiver Start-Up Delay		2.5	5	bits
t_{RD}	Receiver Propagation Delay		25	50	ns
t_{RR}	Differential Output Rise Time (RX±, CD±)		4	7	ns
t_{RF}	Differential Output Fall Time (RX±, CD±)		4	7	ns
t_{RJ}	Receiver and Cable Total Jitter		±2		ns
t_{TST}	Transmitter Start-Up Delay		1	2	bits
t_{TD}	Transmitter Propagation Delay		25	50	ns
t_{TR}	Transmitter Output Rise Time (TXO)	20	25	30	ns
t_{TF}	Transmitter Fall Time (TXO)	20	25	30	ns
t_{TM}	t_{TR} and t_{TF} Mismatch		±0.5	±3	ns
t_{TS}	Transmit Skew (TXO)		±0.5	±2	ns
t_{TON}	Transmit Turn-On Pulse Width at V_{TS} (TX±)[8]	10	20	40	ns
t_{TOFF}	Transmit Turn-Off Delay	130	200	300	ns
t_{CON}	Collision Turn-On Delay		7	13	bits
t_{COFF}	Collision Turn-Off Delay			20	bits
f_{CD}	Collision Frequency	8.5	10	12.5	MHz
t_{CD}	Collision Pulse Width	40	50	69	ns
t_{HON}	CD Heartbeat Delay	0.6	1.1	1.6	µs
t_{HW}	CD Heartbeat Duration	0.5	1.0	1.5	µs
t_{JA}	Jabber Activation Delay	20	26	32	ms
t_{JR}	Jabber Reset Time Out	300	420	550	ms

Note:
8. For a minimum pulse amplitude of >300 mV.

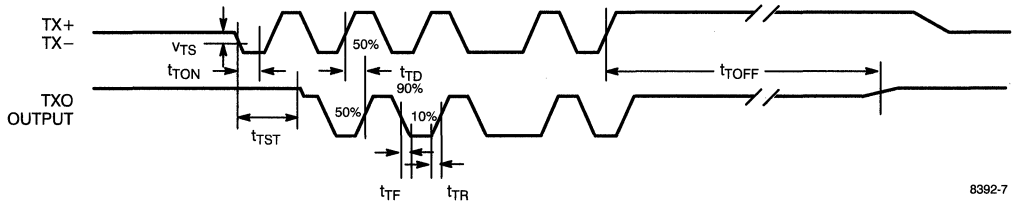
Switching Waveforms

Receiver Timing

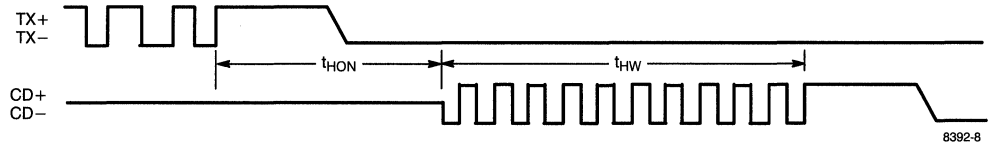


Switching Waveforms (continued)

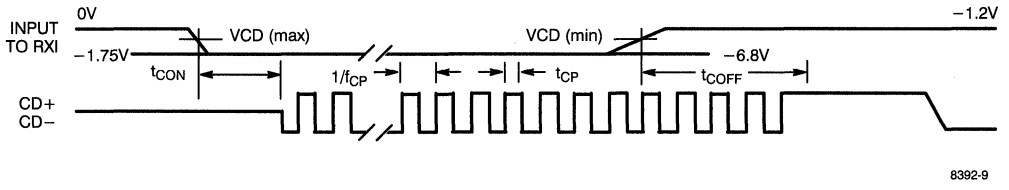
Transmit Timing



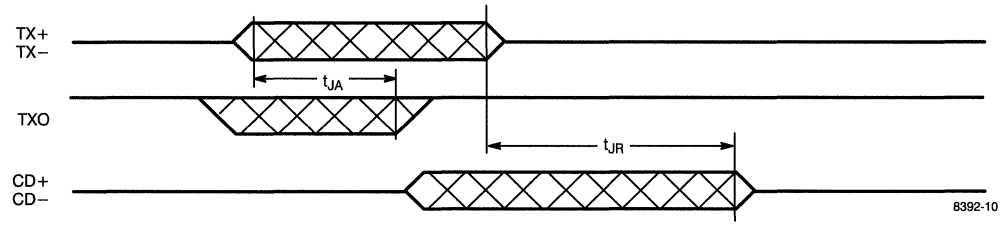
Heartbeat Timing



Collision Timing



Jabber Timing



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B8392−JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B8392−PC	P1	16-Lead (300-Mil) Molded DIP	

Document #: 38−00430

PRELIMINARY

HOTLink™ Evaluation Board

Features

- 160 to 330 Mbps point-to-point serial data link
- Parallel-to-serial and serial-to-parallel I/O
- 10-bit-wide 8B/10B encode, decode or unencoded
- Full system diagnostics with Built-In-Self-Test (BIST)
- Compliant with ESCON®, Fiber Channel and ATM standards
- Compatible with Fiber Channel FC–0 specification (CY9266–C/T):
  - —25–TV–EL–S
  - —25–MI–EL–S
  - —25–TP–EL–S
- Compatible with Fiber Channel FC–0 specification (CY9266–F):
  - —25–M6–LE–I
- Development tool for proprietary networks
- Two-digit error display for BER analysis
- Multiple host interface:
  - —48-pin connector (IBM OLC–266™ compatible)
  - —60-pin edge connector
  - —60-pin two-row right-angle connector
- Easy to use for applications development

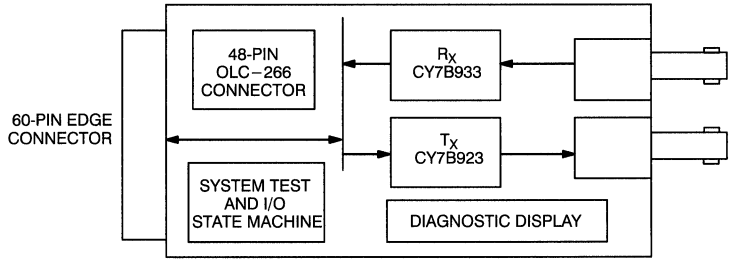


Figure 1. Copper Media Interface Evaluation Board CY9266–C

9266–1

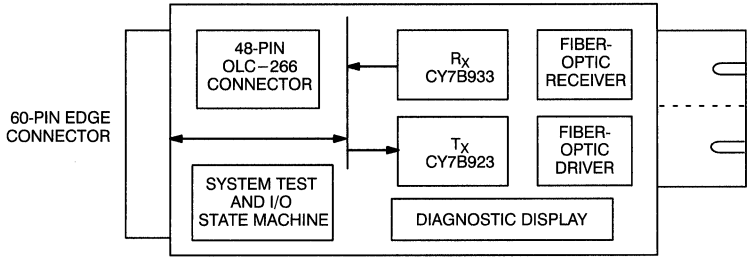


Figure 2. Fiber-Optic Interface Evaluation Board CY9266–F

9266–2

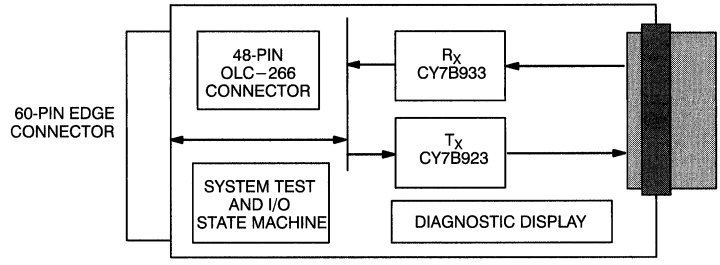


Figure 3. Twisted-Pair Interface Evaluation Board CY9266–T

9266–3

7

Functional Description

The HOTLink Evaluation Board (CY9266) is a system development tool that facilitates the design and evaluation of the Cypress HOTLink transmitter (CY7B923) and receiver (CY7B933) devices. The CY9266 Evaluation Board is offered with three serial media interface options: CY9266–C (copper), CY9266–F (fiber), and CY9266–T (twisted pair). The CY9266–C offers a low cost 1/4″ coaxial connection, the CY9266–F interfaces with a longwave (1300 nm) LED optical transceiver and SC fiberoptics connector, and the CY9266–T is configured to support shielded twisted pair or twin axial cable that attaches through a 9-pin D-sub connector.

The CY9266 accepts data and control commands from the host via the parallel interface ports (available in three connectors). The 48-pin header connector allows interoperability with the IBM OLC–266 interface. The two 60-pin connectors are functionally equivalent. The vertical pin connector is used for probing and monitoring the appropriate signals, while the edge connector can be connected to a flat ribbon cable as a direct host communication interface.

In a typical point-to-point link, the host downloads parallel data to the CY9266 Evaluation Board. Parallel data can be formatted as pre-encoded 10-bit patterns or 8-bit data/special characters to be encoded by the HOTLink transmitter. The data is then encoded (optionally) and serialized by CY7B923 HOTLink Transmitter. Serial data is then transmitted via coax, twisted pair, or fiber.

In the receive operation, serial data is sent from a remote source (via copper/fiber/twisted pair) and transferred to the CY7B933 HOTLink receiver. The serialized data is converted to parallel and then optionally decoded. Parallel data is transferred to the host system along with various status and synchronizing signals. All I/O operations are performed between the host and the Evaluation Board using simple handshakes.

The CY9266 Evaluation Board can also operate in self-diagnostic mode and indicate errors in the serial transmission stream using a built-in two-digit, seven-segment LED display.

Typical Applications for the Evaluation Board include:

- HOTLink system development
- Telecommunication
- Remote data acquisition
- Processor-to-disk/peripheral communication
- Backplane extender
- Point-to-point video/image communications
- Point-to-point CPU/server communications
- High-speed data switching (TI Multiplier, etc.)
- Similar in function to IBM OLC-266 (single channel) and HP HOLC-0266™

Specification

Board Dimensions	3.0″ x 4.0″ (approx., plus media connector)
Two media types:	
CY9266–C	Coax connectors—BNC for transmit, TNC for receive
CY9266–F	Fiber optic module, single row or 4 row modules
CY9266–T	Twisted pair connector, 9-pin D-sub
Power Supply	+5V ± 5%
Maximum Clock Rate	33 MHz
Maximum Data Rate	330 Mbps
Parallel I/O	TTL
Serial I/O	Coax or twisted pair (CY9266–C/T) or Fiber optic with SC connector (CY9266–F)

Ordering Information

Ordering Code	Media Type
CY9266–C	Copper
CY9266–F	Fiber
CY9266–T	Twisted Pair
CY9266–FX	Fiber w/o optic module

Document #: 38–00236–A

Section Contents

Bus Interface Products

VIC64

VMEbus Interface Controller with D64 Functionality

Features

- **An enhanced VIC068A**
  - **64-bit MBLT operation**
  - **Higher transfer rate**
- **Complete VMEbus interface controller and arbiter**
  - **58 internal registers for configuration control and VMEbus and local operations status**
  - **Drives arbitration, interrupt, address modifier, utility, strobe, address line A[7:1], and data line D[7:0] directly. and provides control signals to drive remaining address and data lines**
  - **Direct connection to 68K family and mappable to non-68K processors**
- **Complete master/slave capability**
  - **Supports read, write, write posting, and block transfers**
  - **Accommodates VMEbus timing requirements with internal digital delay line with half-clock granularity**
  - **Programmable metastability delay**
  - **Programmable data acquisition delays**
  - **Provides programmable timeout timers for local bus and VMEbus transactions**
- **Interleaved block transfers**
  - **D64 block transfer capability in conformance with VME64 proposal**
  - **Can act as DMA master on local bus**
  - **Programmable burst counter, transfer length, and interleave period**
  - **Allows master and slave transfer to occur during interleave period**
  - **Also supports local module-based DMA**
- **Arbitration support**
  - **Supports single-level, priority, and round-robin arbitration**
  - **Support fair request option as requester**
- **Interrupt support**
  - **Complete support for the VMEbus interrupts; interrupters and interrupt handler**
  - **Seven local interrupt lines**
  - **8-level interrupt priority encoded**
  - **Total of 29 interrupts mapped through the VIC64**
- **Miscellaneous features**
  - **Refresh option for local DRAM**
  - **Four broadcast location monitors**
  - **Four module-specific location monitors**
  - **Eight interprocessor communication registers**
- **See the *VIC64/7C964 Design Notes* for more information**

Functional Description

Cypress's VIC64 VMEbus Interface Controller with D64 functionality is a single chip designed to minimize the cost and board area requirements and to maximize the performance of a VMEbus master/slave module. Data transfers of 70 Mbyte/sec are possible between boards using VIC64.

In addition to D8, D16 and D32 operations, the VIC64 performs D64 data transfer. On-chip output buffers are used to provide direct connection to address and data lines.

The VIC64 is based on the industry-standard VIC068A. For most applications, the VIC64 is fully software and plug compatible with the VIC068A. (As VIC64 uses register bits that are unassigned in VIC068A, user code may require simple rework to insure compatibility.)

The local bus interface of the VIC64 emulates Motorola's family of 32-bit 68K processor interfaces. Other processors can easily be adapted to interface to the VIC64 using appropriate logic.

Resetting the VIC64

The VIC64 can be reset by any of three distinct reset conditions:

- Internal Reset. This reset is the most common means of resetting the VIC64. It resets selected register values and logic within the device.
- System Reset. This reset provides a means of resetting the VIC64 through the VMEbus backplane. The VIC64 may also initiate a system reset by writing a configuration register.
- Global Reset. This provides the most complete reset of the VIC64. It resets all of the VIC64's configuration registers.

All three reset options are implemented in a different manner and have different effect on the VIC64 configuration registers.

VIC64 VMEbus System Controller

The VIC64 is capable of operating as the VMEbus system controller. It provides VMEbus arbitration functions, including:

- Priority, round-robin, and single-level arbitration schemes
- Driving IACK daisy-chain
- Driving BGiOUT daisy-chain (all four levels)
- Driving SYSCLK output
- VMEbus arbitration timeout timer

The system controller functions are enabled by the SCON pin of the VIC64. This pin is sampled during Reset and if LOW, VIC64 performs as system controller. After Reset the pin becomes an output signifying a D64 transfer.

VIC64 VMEbus Master Cycles

The VIC64 is capable of becoming the VMEbus master in response to a request from local resources. In this situation, the local resource requests a VMEbus transfer. The VIC64 makes a request for the VMEbus. When the VMEbus is granted to the VIC64, it then performs the transfer and acknowledges the local resource and the cycle is complete. The VIC64 is capable of all four VMEbus request levels. In addition, the following release modes are supported:

- Release On Request (ROR)
- Release When Done (RWD)
- Release On Clear (ROC)
- Release Under RMC Control
- Bus Capture And Hold (BCAP)

Pin Configurations

Pin Grid Array (PGA)
Bottom View

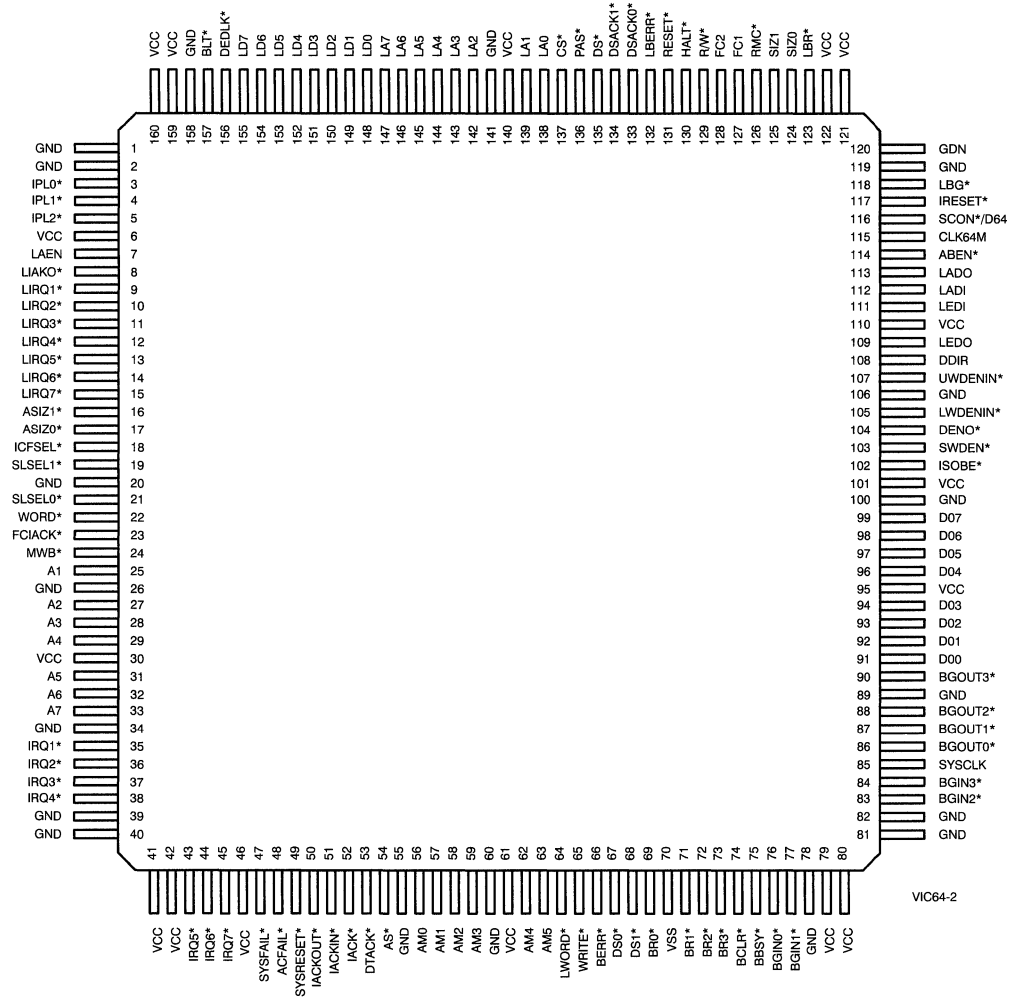
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
GND	IPL2*	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1	ASIZ0	SLSEL1*	WORD*	FCIACK*	A02	A04	VCC	GND	IRQ4*	1
LD6	BLT*	IPL1*	VCC	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
LD2	LD5	DEDLK*	IPL0*	LAEN	LIRQ3*	LIRQ7*	GND	SLSEL0*	GND	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VCC	IACKOUT*	4
LA7	LD0	LD4										SYSFAIL*	SYSRESET*	DTACK*	5
LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
LA2	LA4	GND										GND	AS*	AM1	7
LA1	LA0	VCC										GND	AM2	AM3	8
CS*	DSACK1*	DS*										VCC	LWORD*	AM4	9
PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
FC2	SIZ0	SCON*/D64	CLK64M	LADI	GND	VCC	GND	VCC	D00	BGOUT1*	BGIN2*	BGIN0*	BR3*	GND	13
SIZ1	IRESET*	LADO	LEDI	DDIR	LWDENIN*	DENO*	D06	D03	D01	GND	BGOUT0*	BGIN3*	BGIN1*	BCLR*	14
LBG*	ABEN*	VCC	LEDO	UWDENIN*	SWDEN*	ISOBE*	D07	D05	D04	D02	BGOUT3*	BGOUT2*	SYSCLK	GND	15

VIC64-1

Pin Configurations (continued)

160-Pin Quad Flatpack (QFP)

Top View

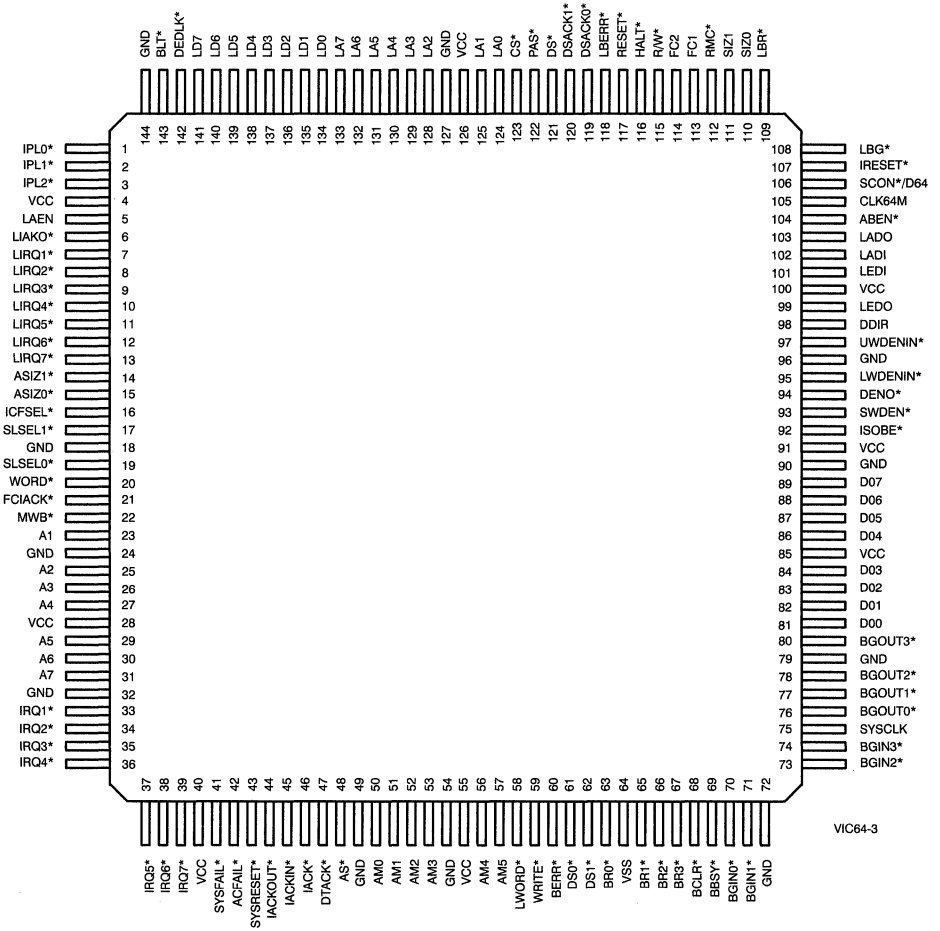


VIC64-2

Pin Configurations (continued)

144-Pin Thin Quad Flatpack (TQFP)

Top View



VIC64-3

Functional Description (continued)

The VIC64 supports A32, A24, and A16, as well as user-defined address spaces.

Master Write-Posting

The VIC64 is capable of performing master write-posting (bus decoupling). In this situation, the VIC64 acknowledges the local resource immediately after the request to the VIC64 is made, thus freeing the local bus. The VIC64 latches the local data to be written and performs the VMEbus transfer without the local resource having to wait for VMEbus arbitration.

Indivisible Cycles

Read-modify-write cycles and indivisible multiple-address cycles (IMACs) are easily performed using the VIC64. Significant control is allowed for:

- Requesting the VMEbus on the assertion of RMC independent of MWB* (this prevents any slave access from interrupting local indivisible cycles)
- Stretching the VMEbus AS*
- Making the above behaviors dependent on the local SIZi signals

Deadlock

If a master operation is attempted when a slave operation to the same module is in progress, a deadlock condition occurs. The VIC64 signals a deadlock condition by asserting the DEDLOCK* signal. This should be used by the local resource requesting the VMEbus to try the transfer after the slave access has completed.

Self-Access

If the VIC64, while it is VMEbus master, has a slave select signaled, a self-access has occurred. The VIC64 asserts BERR* and LBERR*.

VIC64 VMEbus Slave Cycles

The VIC64 is capable of operating as a VMEbus slave controller. The VIC64 contains a highly programmable environment to allow for a wide variety of slave configurations. The VIC64 allows for:

- D64, D32, D16, or D8 configuration
- A32, A24, A16, or user-defined address spaces
- Programmable block transfer support including:
  - — DMA-type block transfer (PAS* and DSACKi* held asserted)
  - — Non DMA-type block transfer (toggle PAS&* and DSACKi*)
  - — No support for block transfer
- Programmable data acquisition delays
- Programmable PAS* and DS* timing
- Restricted slave accesses (supervisory accesses only)

When a slave access is required, the VIC64 requests the local bus. When local bus mastership is obtained, the VIC64 reads or writes the data to/from the local resource and asserts the DTACK* signal to complete the transfer.

Slave Write-Posting

The VIC64 is capable of performing a slave write-post operation (bus decoupling). When enabled, the VIC64 latches the data to be written, and acknowledges the VMEbus (asserts DTACK*) immediately thereafter. This prevents the VMEbus from having to wait for local bus access.

Address Modifier (AM) Codes

The VIC64 encodes and decodes the VMEbus address modifier codes. For VMEbus master accesses, the VIC64 encodes the appropriate AM codes through the VIC64 FCi and ASIZi signals, as well as the block transfer status. For slave accesses, the VIC64 decodes the AM codes and checks the slave select control registers to see if the slave request is to be supported with regard to address spaces, supervisory accesses, and block transfers. The VIC64 also supports user-defined AM codes; that is, the VIC64 can be made to assert and respond to user-defined AM codes.

VIC64 VMEbus Block Transfers

The VIC64 is capable of both master and slave block transfers. The master VIC64 performs a block transfer in one of two modes:

- The Master Block Transfer with Local DMA (D16, D32, and D64)
- The MOVEM-type Block Transfer (D16 and D32)

In addition to these VMEbus block transfers, the VIC64 is also capable of performing block transfers from one local resource to another in a DMA-like fashion. This is referred to as a module-based DMA transfer.

For D32 block transfers, the VMEbus specification restricts block transfers from crossing 256-byte boundaries without toggling the address strobe, in addition to restricting the maximum length of the transfer to 256 bytes. The VIC64 allows for easy implementation of block transfers that exceed the 256-byte restriction by releasing the VMEbus at the appropriate time and re-arbitrating for the bus at a programmed time later (this in-between time is referred to as the interleave period), while at the same time holding both the local and VMEbus addresses with internal latches. All of this is performed without processor/software intervention until the transfer is complete. For D64 block transfers, the VMEbus specification allows for bursts of up to 2048 bytes.

The VIC64 contains two separate address counters for the VMEbus and local address buses. In addition, a separate address counter is provided for slave block transfers. The VIC64 address counters are 8-bit up-counters that provide for transfers up to 256 bytes. For transfers that exceed the 256 byte limit, the external counters and latches are required.

The VIC64 is capable of performing A32/A16:D64/D32/D16 master block transfers. For D64 transfers, external logic is required for the multiplexing of the data and address signals for the upper 24 address/data lines. The CY7C964 is specifically designed for this purpose. Multiplexing for the lower 8 bits is done within the VIC64.

The VIC64 allows slave accesses to occur during the interleave period. Master accesses are also allowed during interleave with programming and external logic. This is referred to as the dual-path option.

MOVEM Master Block Transfer

This mode of block transfer provides the simplest implementation of VMEbus block transfers. For this mode, the local resource simply configures the VIC64 for a MOVEM block transfer and proceeds with the consecutive-address cycles (such as a 68K MOVEM instruction). The local resource continues as the local bus master in this mode.

Master Block Transfers with Local DMA

In this mode, the VIC64 becomes the local bus master and reads or writes the local data in a DMA-like fashion. This provides a much faster interface than the MOVEM block transfer, but with less control and fault tolerance.

D64 block transfers are not supported by MOVEM protocol.

VIC64 Slave Block Transfer

The VIC64 is capable of decoding the address modifier codes to determine that a slave block transfer is desired. In this mode, the VIC64 captures the VMEbus address, and latches it into internal counters. For subsequent cycles, the VIC64 simply increments this counter for each transfer. The local protocol for slave block transfers can be configured in a full handshake mode by toggling both PAS* and DS* and expecting DSACKi* to toggle, or in an accelerated mode in which only DS* toggles and PAS* is asserted throughout the cycle.

For D64 slave block transfers, the SCON*/D64 signal is asserted to indicate a D64 transfer is in progress. External logic is required to de-multiplex the data from the VMEbus address bus for the upper 24 address/data lines. The lower 8 bits are done within the VIC64.

Module-Based DMA Transfers

The VIC64 can act as a DMA controller between two local resources. This mode is similar to that of master block transfers with local DMA, with the exception that the VMEbus is not the source or destination.

VIC64 Interrupt Generation and Handling Facilities

The VIC64 can generate and handle a seven-level prioritized interrupt scheme similar to that used by the Motorola 68K processors. These interrupts include:

- 7 VMEbus interrupts
- 7 local interrupts
- 5 VIC64 error/status interrupts
- 8 interprocessor communication interrupts.

The VIC64 can be configured to act as handler for any of the seven VMEbus interrupts. The VIC64 can generate the seven VMEbus interrupts as well as supplying a user-defined status/ID vector. The local priority level (IPL) for VMEbus interrupts is programmable. When configured as the system controller, the VIC64 drives the IACK* daisy chain.

The local interrupts can be configured with the following:

- User-defined local interrupt priority level (IPL)
- Option for VIC64 to provide the status/ID vector
- Edge or level sensitivity
- Polarity (rising/falling edge, active HIGH/LOW)

The VIC64 is also capable of generating local interrupts on certain error or status conditions. These include:

- ACFAIL* asserted
- SYSFAIL* asserted
- Failed master write-post (BERR* asserted)
- Local DMA completion for block transfers
- Arbitration timeout
- VMEbus interrupter interrupt

The VIC64 can also interrupt on the setting of a module or global switch in the interprocessor communication facilities.

Interprocessor Communication Facilities

The VIC64 includes interprocessor registers and switches that can be written and read through VMEbus accesses. These are the only such registers that are directly accessible from the VMEbus. Included in the interprocessor communication facilities are:

- Four general-purpose 8-bit registers
- Four module switches
- Four global switches
- VIC64 version/revision register (read-only)
- VIC64 reset/halt condition (read-only)
- VIC64 interprocessor communication register semaphores

When set through a VMEbus access, these switches can interrupt a local resource. The VIC64 includes module switches that are intended for a single module, and global switches which are intended to be used as a broadcast.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC64/CY7C964 Design Notes
VIC068A/VAC068A User's Guide

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VIC64−AC	A144	144-Lead Thin Quad Flatpack	Commercial
VIC64−BC	B144	145-Pin Plastic Pin Grid Array	
VIC64−GC	G145	145-Pin Ceramic Pin Grid Array	
VIC64−NC	N160	160-Lead Plastic Quad Flatpack	
VIC64−GI	G145	145-Pin Pin Grid Array	Industrial
VIC64−GM	G145	145-Pin Ceramic Pin Grid Array	Military Temp. Commercial
VIC64−GMB	G145	145-Pin Ceramic Pin Grid Array	MIL-STD-883
VIC64−UMB	U162	160-Lead Ceramic Quad Flatpack	MIL-STD-883
VIC64−UM	U162	160-Lead Ceramic Quad Flatpack	Military Temp. Commercial

Document #: 38−00196−B

VIC068A

VMEbus Interface Controller

Features

- **Complete VMEbus interface controller and arbiter**
  - **— 58 internal registers provide configuration control and status of VMEbus and local operations**
  - **— Drives arbitration, interrupt, address modifier utility, strobe, address lines A07through A01 and data lines D07 through D00 directly, and provides signals for control logic to drive remaining address and data lines**
  - **— Direct connection to 68xxx family and mappable to non-68xxx processors**
- **Complete master/slave capability**
  - **— Supports read, write, write posting, and block transfers**
  - **— Accommodates VMEbus timing requirements with internal digital delay line (½-clock granularity)**
  - **— Programmable metastability delay**
  - **— Programmable data acquisition delays**
  - **— Provides timeout timers for local bus and VMEbus transactions**
- **Interleaved block transfers over VMEbus**
  - **— Acts as DMA master on local bus**
  - **— Programmable burst count, transfer length, and interleaved period interval**
  - **— Supports local module-based DMA**
- **Arbitration support**
  - **— Supports single-level, priority and round robin arbitration**
  - **— Supports fair request option as requester**
- **Interrupt support**
  - **— Complete support for the VMEbus interrupts: interrupter and interrupt handler**
  - **— Seven local interrupt lines**
  - **— 8-level interrupt priority encode**
  - **— Total of 29 interrupts mapped through the VIC068A**
- **Miscellaneous features**
  - **— Refresh option for local DRAM**
  - **— Four broadcast location monitors**
  - **— Four module-specific location monitors**
  - **— Eight interprocessor communications registers**
  - **— PGA or QFP packages**
  - **— Compatible with IEEE Specification 1014, Rev. C**
  - **— Supports RMC operations**
- **See the *VIC068A/VAC068A User's Guide* for more information**

Functional Description

The VMEbus interface controller (VIC068A) is a single chip designed to minimize the cost and board area requirements and to maximize performance of the VMEbus interface of a VMEbus master/slave module. This can be implemented on VIC068Aeither a 8-bit, 16-bit, or 32-bit VMEbus system. The VIC068A performs all VMEbus system controller functions plus many others, which simplify the development of VIC068Aa VMEbus interface. The VIC068A utilizes patented on-chip output buffers. These CMOS high-drive buffers provide direct connection to the address and data lines. In addition to these signals, the VIC068A connects directly to the arbitration, interrupt, address modifier, utility and strobe lines. Signals are provided which control data direction and latch functions needed for a 32-bit implementation.

The VIC068A was developed through the efforts of a consortium of board vendors, under the auspices of the VMEbus International Trade Association (VITA). The VIC068A thus insures compatibility between boards designed by different manufacturers.

Pin Configurations

Pin Grid Array (PGA)
Bottom View

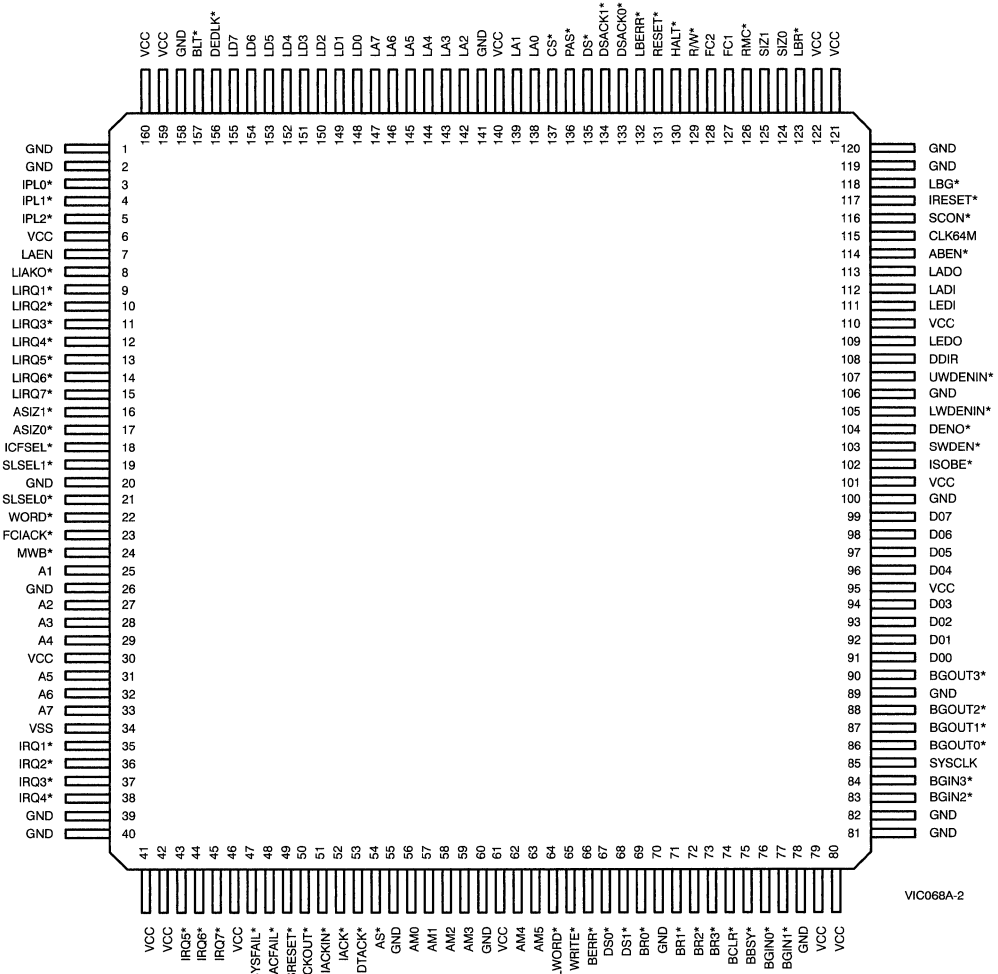
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
GND	IPL2*	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1	ASIZ0	SLSEL1*	WORD*	FIACK*	A02	A04	VCC	GND	IRQ4*	1
LD6	BLT*	IPL1*	VCC	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
LD2	LD5	DEDLK*	IPL0*	LAEN	LIRQ3*	LIRQ7*	GND	SLSEL0*	GND	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VCC	IACKOUT*	4
LA7	LD0	LD4										SYSFAIL*	SYSRESET*	DTACK*	5
LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
LA2	LA4	GND										GND	AS*	AM1	7
LA1	LA0	VCC										GND	AM2	AM3	8
CS*	DSACK1*	DS*										VCC	LWORD*	AM4	9
PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
FC2	SIZ0	SCON*	CLK64M	LADI	GND	VCC	GND	VCC	D00	BGOUT1*	BGIN2*	BGIN0*	BR3*	GND	13
SIZ1	IRESET*	LADO	LEDI	DDIR	LWDENIN*	DENO*	D06	D03	D01	GND	BGOUT0*	BGIN3*	BGIN1*	BCLR*	14
LBG*	ABEN*	VCC	LEDO	UWDENIN*	SWDEN*	ISOBE*	D07	D05	D04	D02	BGOUT3*	BGOUT2*	SYSCLK	GND	15

VIC068A-1

Pin Configurations (continued)

160-Pin Quad Flatpack (QFP)

Top View

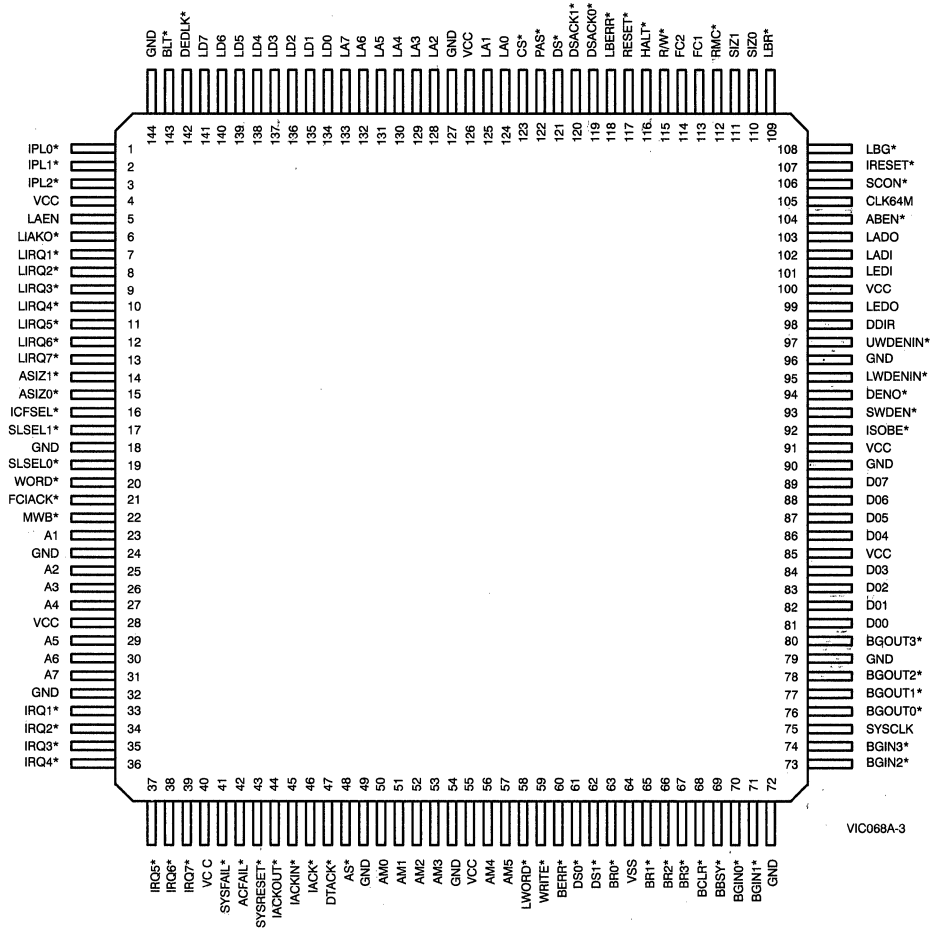


VIC068A-2

Pin Configurations (continued)

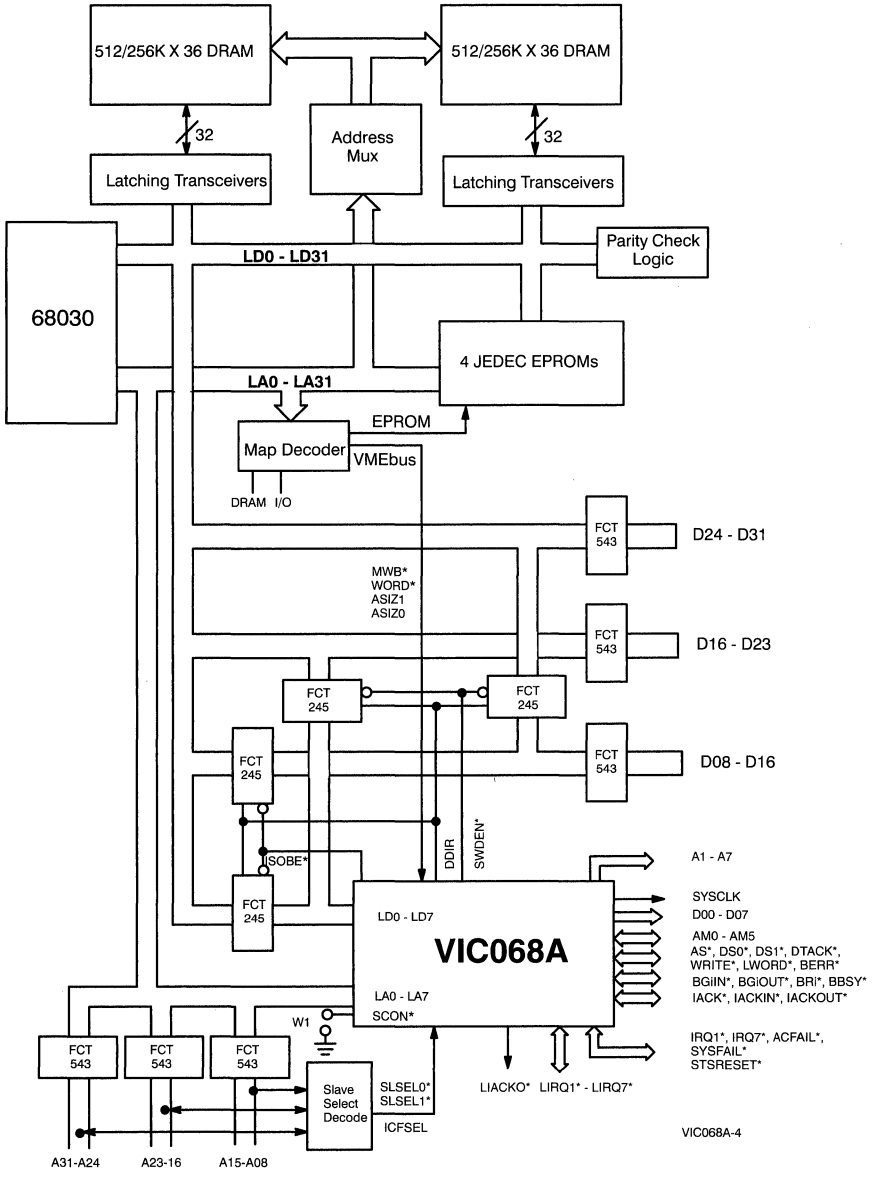
144-Pin Thin Quad Flatpack (TQFP)

Top View



VIC068A-3

VIC068A on 68030 Board



Theory of Operation

The VIC068A is an interface between a local CPU bus and the VMEbus. The local bus interface of the VIC068A emulates Motorola's family of 32-bit CISC processor interfaces. Other processors can easily be adapted to interface to the VIC068A using the appropriate logic.

Resetting the VIC068A

The VIC068A can be reset by any of three distinct reset conditions:

Internal Reset. This reset is the most common means of resetting the VIC068A. It resets select register values and all logic within the device.

System Reset. This reset provides a means of resetting the VIC068A through the VMEbus backplane. The VIC068A may also signal a SYSRESET* by writing a configuration register.

Global Reset. This provides a complete reset of the VIC068A. This reset resets all of the VIC068A's configuration registers. This reset should be used with caution since SYSCLK is not driven while a global reset is in progress.

All three reset options are implemented in a different manner and have different effects on the VIC068A configuration registers.

VIC068A VMEbus System Controller

The VIC068A is capable of operating as the VMEbus system controller. It provides VMEbus arbitration functions, including:

- Priority, round-robin, and single-level arbitration schemes
- Driving IACK* Daisy-Chain
- Driving BGiOUT* Daisy-Chain (All four levels)
- Driving SYSCLK output
- VMEbus arbitration timeout timer

The System controller functions are enabled by the SCON* pin of the VIC068A. When strapped LOW, the VIC068A functions as the VMEbus system controller.

VIC068A VMEbus Master Cycles

The VIC068A is capable of becoming the VMEbus master in response to a request from local resources. In this situation, the local resource requests that a VMEbus transfer is desired. The VIC068A makes a request for the VMEbus. When the VMEbus is granted to the VIC068A, it then performs the transfer and acknowledges the local resource and the cycle is complete. The VIC068A is capable of all four VMEbus request levels. The following release modes are supported:

- Release on request (ROR)
- Release when done (RWD)
- Release on clear (ROC)
- Release under RMC* control
- Bus capture and hold (BCAP)

The VIC068A supports A32, A24, and A16, as well as user-defined address spaces.

Master Write-Posting

The VIC068A is capable of performing master write-posting (bus decoupling). In this situation, the VIC068A acknowledges the local resource *immediately* after the request to the VIC068A is made, thus freeing the local bus. The VIC068A latches the local data to be written and performs the VMEbus transfer without the local resource having to wait for VMEbus arbitration.

Indivisible Cycles

Read-modify-write cycles and indivisible multiple-address cycles (IMACs) are easily performed using the VIC068A. Significant control is allowed to:

- Requesting the VMEbus on the assertion of RMC* independent of MWB* (this prevents any slave access from interrupting local indivisable cycles)
- Stretching the VMEbus AS*
- Making the above behaviors dependent on the local SIZi signals

Deadlock Condition

If a master operation is attempted when a slave operation to the same module is in progress, a deadlock condition has occurred. The VIC068A will signal a deadlock condition by asserting the DEDLK* signal. This should be used by the local resource requesting the VMEbus to try the transfer after the slave access has completed.

Self-Access Condition

If the VIC068A, while it is VMEbus master, has a slave select signaled, a self access is said to have occurred. The VIC068A will issue a BERR*, which in turn will cause a LBERR* to be asserted.

VIC068A VMEbus Slave Cycles

The VIC068A is capable of operating as a VMEbus slave controller. The VIC068A contains a highly programmable environment to allow for a wide variety of slave configurations. The VIC068A allows for:

- D32, D16, or D8 configuration
- A32, A24, A16, or user-defined address spaces
- Programmable block transfer support including:
  - — DMA-type block transfer (PAS* and DSACKi* held asserted)
  - — non–DMA-type block transfer (toggle PAS* and DSACKi*)
  - — No support for block transfer
- Programmable data acquisition delays
- Programmable PAS* and DS* timing
- Restricted slave accesses (supervisory accesses only)

When a slave access is required, the VIC068A will request the local bus. When local bus mastership is obtained, the VIC068A will read or write the data to/from the local resource and assert the DTACK* signal to complete the transfer.

Slave Write-Posting

The VIC068A is capable of performing a slave write-post operation (bus decoupling). When enabled, the VIC068A latches the data to be written and acknowledge the VMEbus (asserts DTACK*) immediately thereafter. This prevents the VMEbus from having to wait for local bus access.

Address Modifier (AM) Codes

The VIC068A encodes and decodes the VMEbus address modifier codes. For VMEbus master accesses, the VIC068A encodes the appropriate AM codes through the VIC068A FCi and ASIZi signals, as well as the block transfer status. For slave accesses, the VIC068A decodes the AM codes and checks the slave select control registers to see if the slave request is to be supported with regard to address spaces, supervisory accesses, and block transfers. The VIC068A also supports user-defined AM codes; that is, the

VIC068A can be made to assert and respond to user-defined AM codes.

VIC068A VMEbus Block Transfers

The VIC068A is capable of both master and slave block transfers. The master VIC068A performs a block transfer in one of two modes:

- MOVEM-type Block Transfer
- Master Block Transfer with Local DMA

In addition to these VMEbus block transfers, the VIC068A is also capable of performing block transfers from one local resource to another in a DMA-like fashion. This is referred to as a Module-based DMA transfer.

The VMEbus specification restricts block transfers from crossing 256-byte boundaries without toggling the address strobe, in addition to restricting the maximum length of the transfer to 256 bytes. The VIC068A allows for easy implementation of block transfers that exceed the 256-byte restriction by releasing the VMEbus at the appropriate time and rearbitrating for the bus at a programmed time later (this in-between time is referred to as the interleave period), while at the same time holding both the local and VMEbus addresses with internal latches. All of this is performed without processor/software intervention until the transfer is complete.

The VIC068A contains two seperate address counters for the VMEbus and the local address buses. In addition, a seperate address is counter-provided for slave block transfers. The VIC068A address counters are 8-bit up-counters that provide for transfers up to 256 bytes. For transfers that exceed the 256-byte limit, the Cypress CY7C964 or external counters and latches are required.

The VIC068A allows slave accesses to occur during the interleave period. Master accesses are also allowed during interleave with programming and external logic. This is referred to as the "dual path" option.

MOVEM Master Block Transfer

This mode of block transfer provides the simplest implementation of VMEbus block transfers. For this mode, the local resource simply configures the VIC068A for a MOVEM block transfer and proceeds with the consecutive-address cycles (such as a 680X0 MOVEM instruction). The local resource continues as the local bus master in this mode.

Master Block Transfers with Local DMA

In this mode, the VIC068A becomes the local bus master and reads or writes the local data in a DMA-like fashion. This provides a much faster interface than the MOVEM block transfer, but with less control and fault tolerence.

VIC068A Slave Block Transfer

The process of receiving a block transfer is referred to as a slave block transfer. The VIC068A is capable of decoding the address modifier codes to determine that a slave block transfer is desired. In this mode, the VIC068A captures the VMEbus address, and latches them into internal counters. For subsequent cycles, the VIC068A simply increments this counter for each transfer. The local protocol for slave block transfers can be configured in a full handshake mode by toggling both PAS* and DS* and expecting DSACKi* to toggle, or in an accelerated mode in which only DS* toggles and PAS* is asserted throughout the cycle.

Module-Based DMA Transfers

The VIC068A is capable of acting as a DMA controller between two local resources. This mode is similar to that of master block transfers with local DMA, with the exception that the VMEbus is not the second source or destination.

VIC068A Interrupt Generation and Handling Facilities

The VIC068A is capable of generating and handling a seven-level prioritized interrupt scheme similar to that used by the Motorola CISC processors. These interrupts include the seven VMEbus interrupts, seven local interrupts, five VIC068A error/status interrupts, and eight interprocessor communication interrupts.

The VIC068A can be configured to act as handler for any of the seven VMEbus interrupts. The VIC068A can generate the seven VMEbus interrupts as well as supplying a user-defined status/ID vector. The local priority level (IPL) for VMEbus interrupts is programmable. When configured as the system controller, the VIC068 will drive the IACK daisy-chain.

The local interrupts can be configured with the following:

- User-defined local interrupt priority level (IPL)
- Option for VIC068A to provide the status/ID vector
- Edge or level sensitivity
- Polarity (rising/falling edge, active HIGH/LOW)

The VIC068A is also capable of generating local interrupts on certain error or status conditions. These include:

- ACFAIL* asserted
- SYSFAIL* asserted
- Failed master write-post (BERR* asserted)
- Local DMA completion for block transfers
- Arbitration timeout
- VMEbus interrupter interrupt

The VIC068A can also interrupt on the setting of a module or global switch in the interprocessor communication facilities.

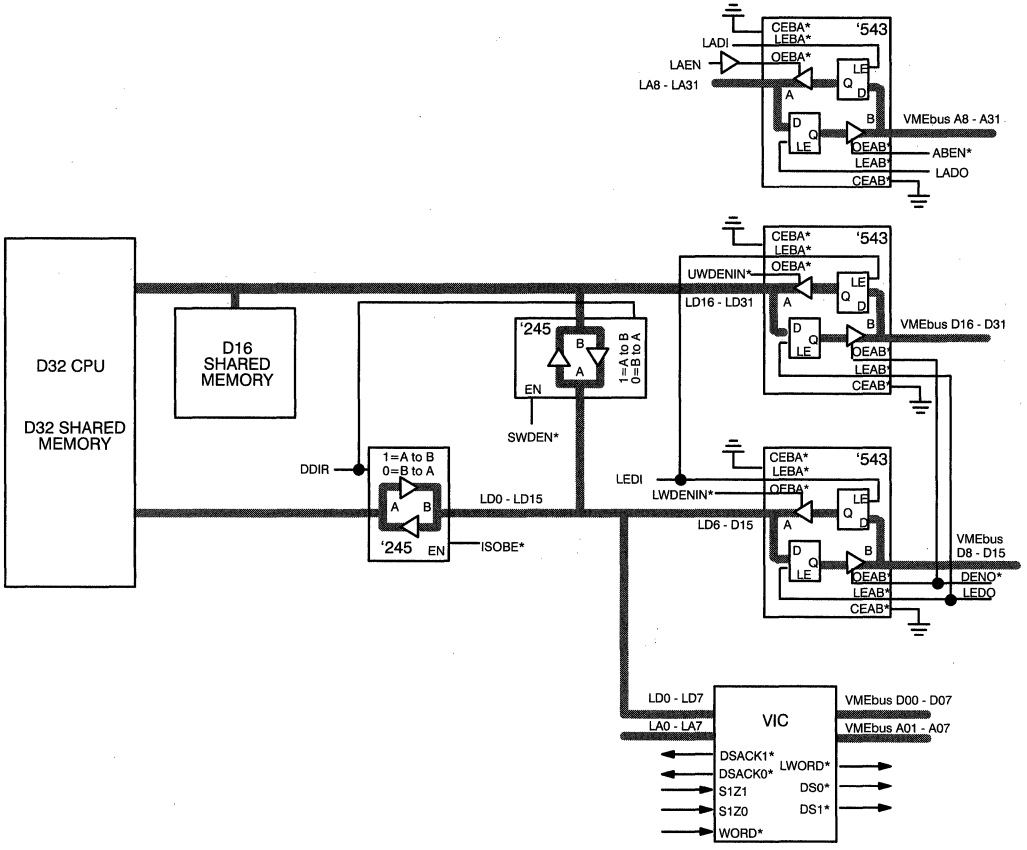
Interprocessor Communication Facilities

The VIC068A includes interprocessor registers and switches that can be written and read through VMEbus accesses. These are the only such registers that are directly accessible from the VMEbus. Included in the interprocessor communication facilities are:

- Four general purpose 8-bit registers
- Four module switches
- Four global switches
- VIC068A version/revision register (read-only)
- VIC068A Reset/Halt condition (read-only)
- VIC068A interprocessor communication register semaphores

When set through a VMEbus access, these switches can interrupt a local resource. The VIC068A includes module switches that are intended for a single module, and global switches which are intended to be used as a broadcast.

Buffer Control Signal for Shared Memory Implementation[1]



Note:
1. This configuration can support Slave Block Transfers and Master and Slave Write-Post Operation. This buffer configuration cannot support block transfers with DMA.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC068A/VAC068A User's Guide
VIC64/CY7C964 Design Notes

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VIC068A−AC	A144	144-Pin Thin Quad Flatpack	Commercial
VIC068A−BC	B144	145-Pin Plastic Pin Grid Array	
VIC068A−GC	G145	145-Pin Ceramic Pin Grid Array	
VIC068A−NC	N160	160-Lead Plastic Quad Flatpack	
VIC068A−GI	G145	145-Pin Ceramic Pin Grid Array	Industrial
VIC068A−GMB	G145	145-Pin Ceramic Pin Grid Array	MIL-STD-883
VIC068A−UM	U162	160-Lead Ceramic Quad Flatpack	Military Temp. Commercial
VIC068A−UMB	U162	160-Lead Ceramic Quad Flatpack	MIL-STD-883

Document #: 38−00167−C

VAC068A

VMEbus Address Controller

Features

- **Optional companion part to VIC068A**
- **Implements master/slave VMEbus interface in conjunction with the VIC068A**
- **Complete VMEbus and I/O DMA capability for a 32-bit CPU**
- **Complete local and VMEbus memory map decoding**
  - **— Separate segments on local side available for DRAM, VME subsystem bus (VSB), shared resources, VMEbus, local I/O, and EPROM**
  - **— Separate segments for the VMEbus address decode for slave select 0, slave select 1, and interprocessor communication facilities**
  - **— 64-Kbyte resolution for both local and VMEbus memory maps**
- **Supports block transfers over 256 byte boundaries**
  - **— Address counters for both VMEbus A(31–8) and local LA(31–8)**
  - **— Supports dual-path mode**
  - **— Supports implementation of VSB interface with DMA capability**
- **Dual UART channels on board**
  - **— Double-buffered on transmit, quint-buffered on receive**
  - **— Baud rate programmable**
- **Miscellaneous features**
  - **— Pin grid array or quad flatpack packages**
  - **— Supports unaligned transfers**
  - **— Programmable DSACKi for local I/O**
  - **— Programmable timer and interrupt controller**
  - **— Programmable I/O (PIO)**
- **See the *VIC068A/VAC068A User's Guide* for more information**

Functional Description

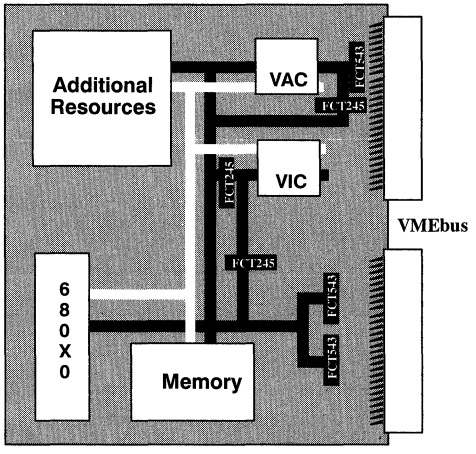
The VMEbus address controller (VAC068A) is a programmable memory map address controller. In conjunction with the VIC068A (VMEbus interface controller), the VAC068A maximizes the VMEbus interface performance of a master/slave module.

The VAC068A contains programmable registers to allow the user to easily define memory maps for both the local and VMEbus address regions. The VAC068A also contains the address counters and handshaking signals to allow easy implementation of block-level transfers over 256-byte boundaries. Additional features include dual internal UART channels, redirection control on the local bus to VSB (VME subsystem bus) or shared resource area, data swapping for unaligned transfers, programmable DSACKi, programmable timer and interrupt controller.

The VAC068A connects directly to the local bus and the VIC068A. VMEbus address lines A8 through A31 are driven directly. The VAC068A output drivers feature patented high-drive outputs and TTL-compatible inputs.

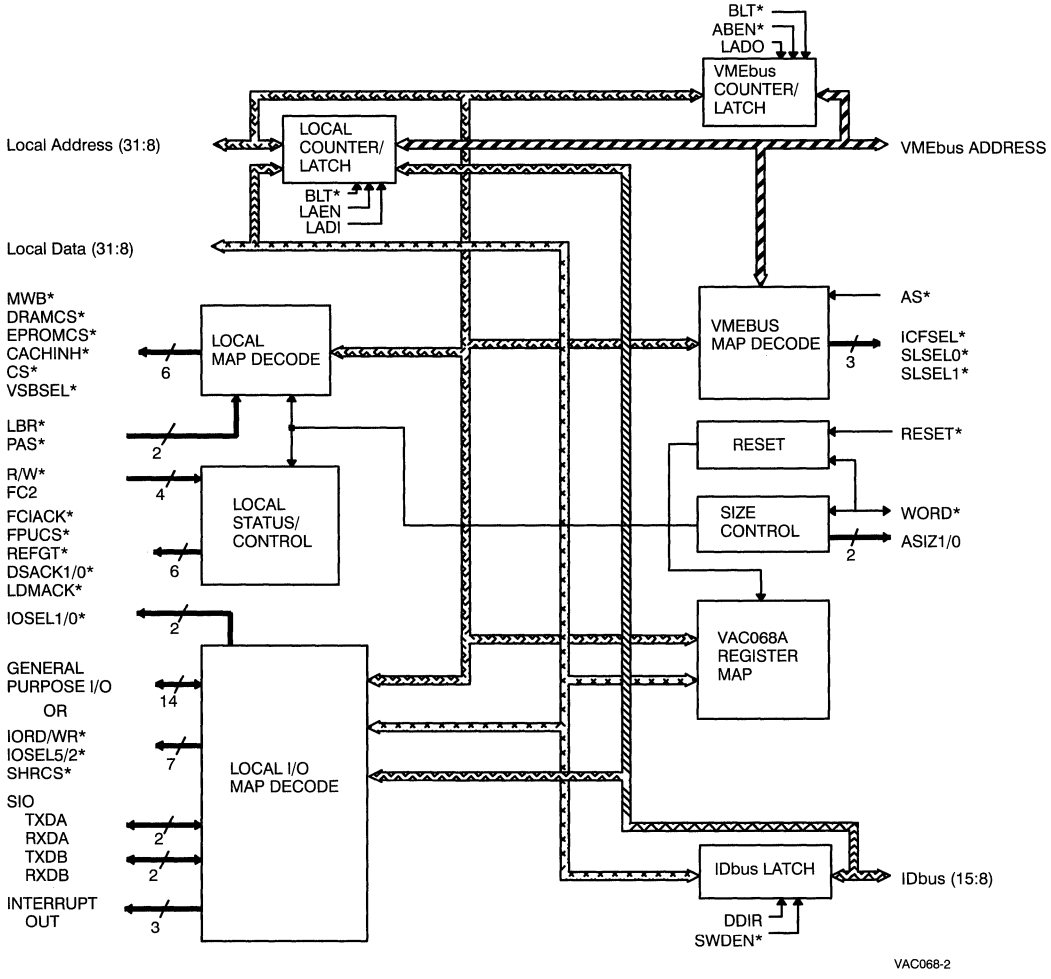
The VAC068A is available in pin grid array (with 122 active signals, 22 power and ground pins, and 1 locator pin) and quad flatpack.

Sample Board Design



VAC068-1

Block Diagram



Pin Configurations

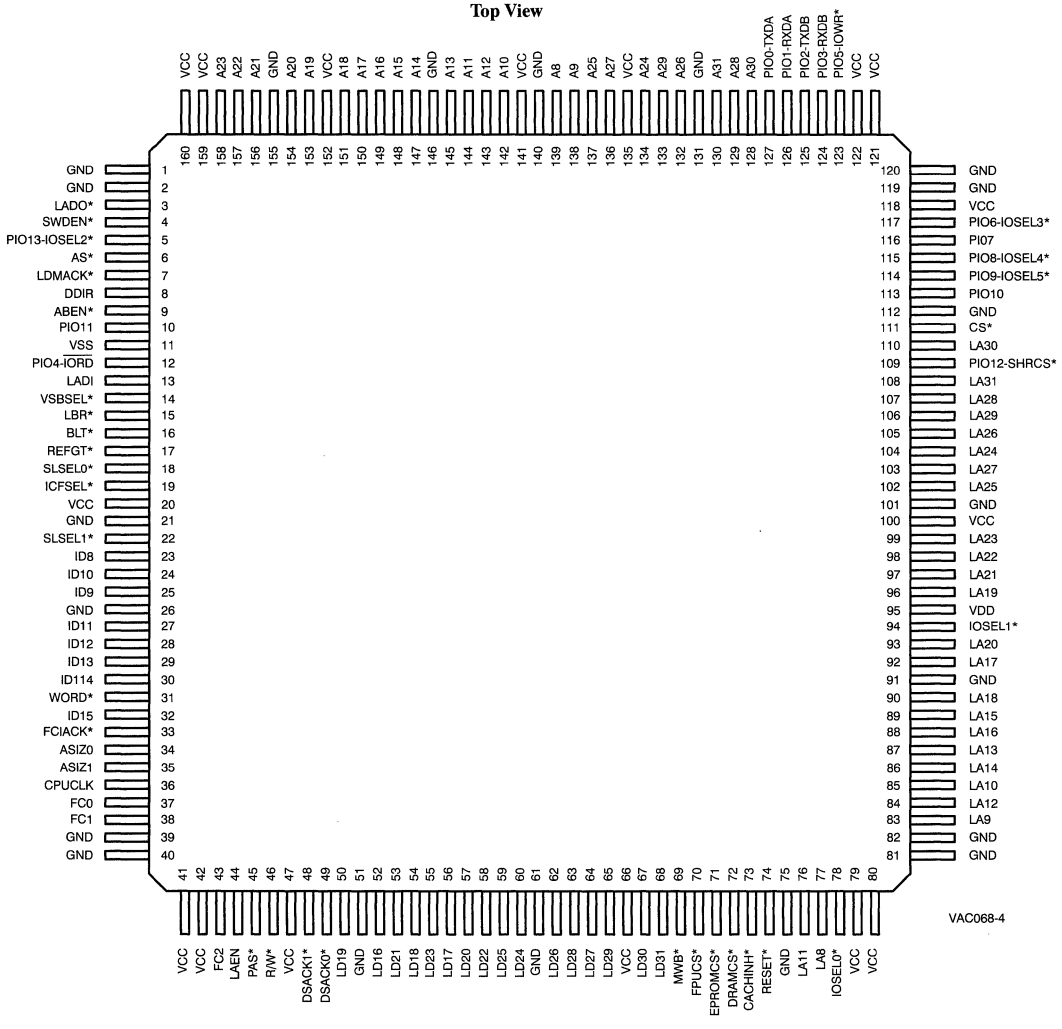
Pin Grid Array (PGA)
Bottom View

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
A23	PIO13/ IOSEL2*	DDIR	PIO11	LADI	BLT*	REFGT*	ICFSEL*	SLSEL1*	ID8	ID11	ID13	ID14	ASIZ0	FC1	1
A20	A22	SWDEN*	VAS*	ABEN*	PIO4/ IORD*	VSBSEL*	SLSEL0*	IDI0	ID9	ID12	WORD*	FCIACK*	FC0	PAS*	2
A17	A19	A21	LADO	LDMACK*	GND	LBR*	VCC	GND	GND	ID15	ASIZ1	CPUCLK	LAEN	DSACK1*	3
A16	A18	GND	LOCATOR PIN									FC2	R/W*	LD19	4
A14	A15	VCC										VCC	DSACK0*	LD21	5
A12	A13	GND										GND	LD16	LD17	6
A10	A11	VCC										LD23	LD18	LD20	7
A08	A09	GND										LD24	LD22	LD25	8
A25	A24	VCC										GND	LD27	LD26	9
A27	A26	GND										VCC	LD29	LD28	10
A29	A28	PIO0/ TXDA										DRAMCS*	LD31	LD30	11
A31	PIO1/ RXDA	PIO5/ IOWR*										GND	EPROMCS*	MWB*	12
A30	PIO3/ RXDB	PIO7	PIO8/ IOSEL4*	GND	LA29	GND	VCC	VCC	GND	LA13	LA9	LA11	CACHINH*	FPUCS*	13
PIO2/ TXDB	PIO6/ IOSEL3*	PIO10	CS*	LA31	LA26	LA24	LA22	IOSEL1*	LA17	LA15	LA14	LA12	LA8	RESET*	14
VCC	PIO9/ IOSEL5*	LA30	PIO12/ SHRCS*	LA28	LA27	LA25	LA23	LA21	LA19	LA20	LA18	LA16	LA10	IOSEL0*	15

VAC068-3

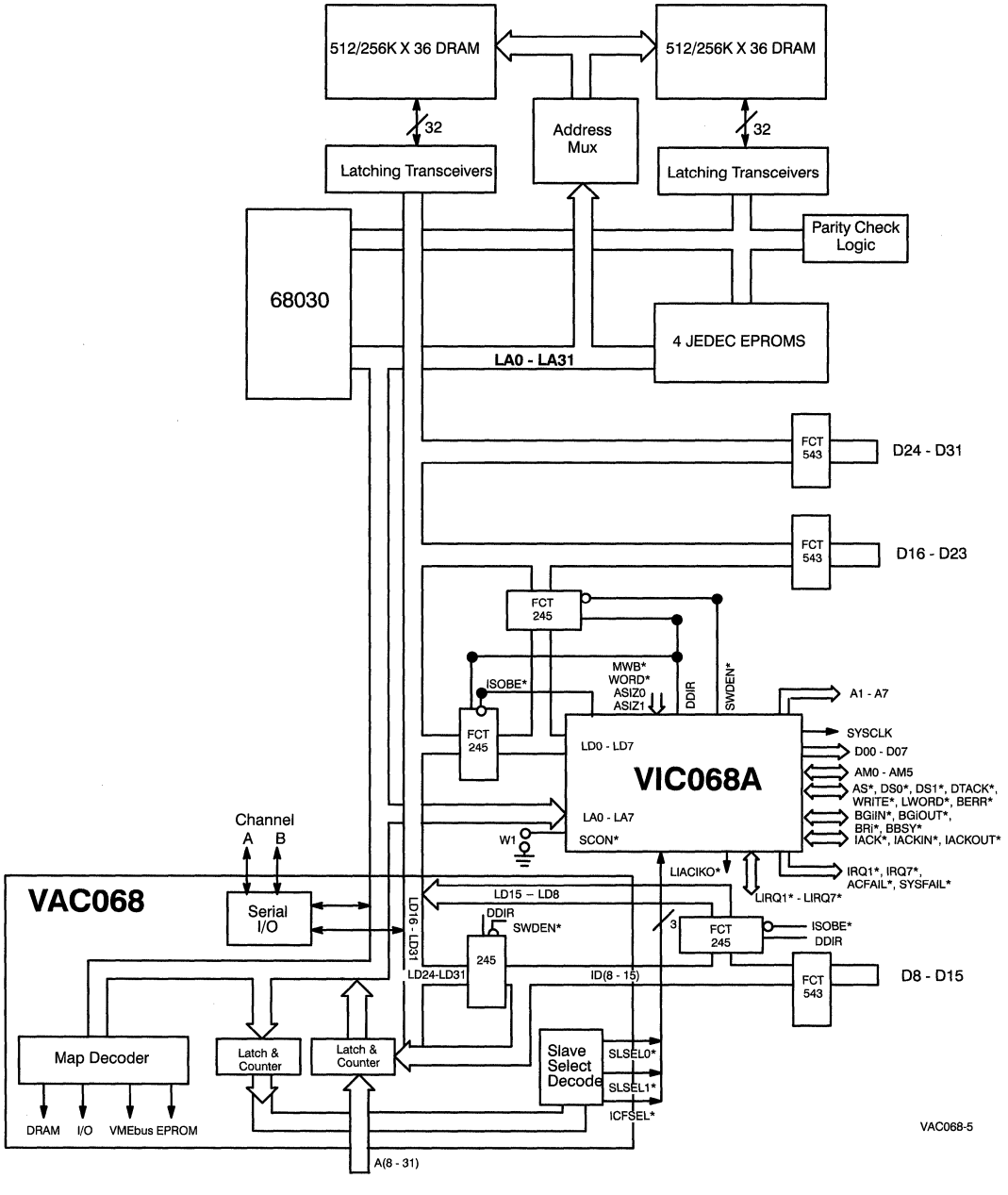
Pin Configurations (continued)

Quad Flatpack (QFP)
Top View



VAC068-4

VIC068A/VAC068A on 68030 Board



Operating Range

Range	Ambient Temperature	VCC
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC068A/VAC068A User's Guide
VIC64/CY7C964 Design Notes

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VAC068A−BC	B144	145-Pin Plastic Pin Grid Array	Commercial
VAC068A−GC	G145	145-Pin Ceramic Pin Grid Array	
VAC068A−NC	N160	160-Lead Plastic Quad Flatpack	
VAC068A−GI	G145	145-Pin Ceramic Pin Grid Array	Industrial
VAC068A−GM	G145	145-Pin Ceramic Pin Grid Array	Military Temp. Commercial
VAC068A−GMB	G145	145-Pin Ceramic Pin Grid Array	MIL-STD-883
VAC068A−UM	U162	160-Lead Ceramic Quad Flatpack	Military Temp. Commercial
VAC068A−UMB	U162	160-Lead Ceramic Quad Flatpack	MIL-STD-883

Document #: 38−00169−C

CY7C960
CY7C961

Slave VMEbus Interface Controller Family

Features

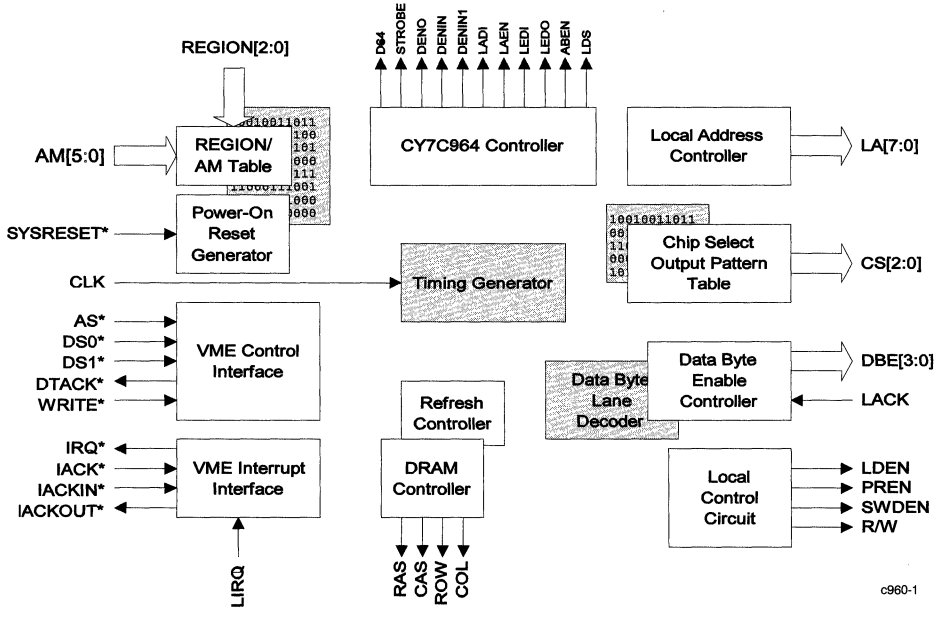
- **80 Mbyte per second block transfer rates**
- **All VME64 transactions provided, including A64/D64, A40/MD32 transfers**
- **Auto Slot ID**
- **CR/CSR space**
- **All standard (rev C) VMEbus transactions implemented**
- **VMEbus Interrupter**
- **No local CPU required**
- **Programmable from VMEbus or serial PROM**
- **DRAM controller, including refresh**
- **On-chip DMA controller (CY7C961)**
- **Local I/O controller**
- **Flexible VMEbus address scheme**
- **User-configured VMEbus response**
- **64-pin TQFP, 10x10mm (CY7C960)**
- **100-pin TQFP, 14x14mm (CY7C961)**

Functional Description

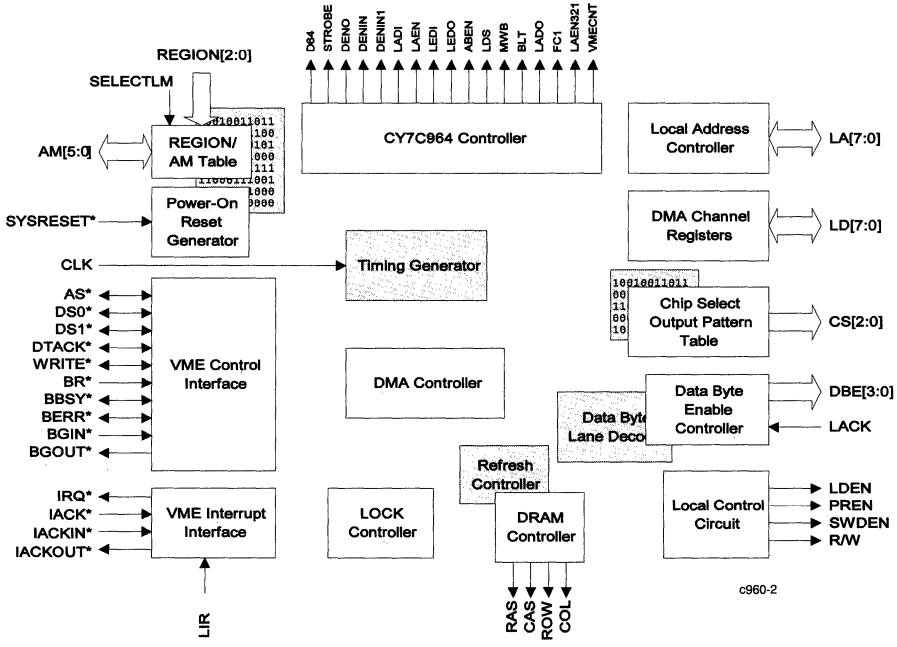
The CY7C960 Slave VMEbus Interface Controller provides the board designer with an integrated, full-featured VME64 interface. This 64-pin device can be programmed to handle every transaction defined in the VME64 specification. The CY7C961 is based upon the CY7C960: additional features include Remote Master capability whereby the CY7C961 can be commanded to move data as a VMEbus master. The CY7C961 is packaged in a 100-pin outline.

The CY7C960 contains all the circuitry needed to control large DRAM arrays and local I/O circuitry without the intervention of a local CPU. There are no registers to read or write, no complex command blocks to be constructed in memory. The CY7C960 simply fetches its own configuration parameters during the power-on reset period. After reset the CY7C960 responds appropriately to VMEbus activity and controls local circuitry transparently.

CY7C960 Logic Block Diagram

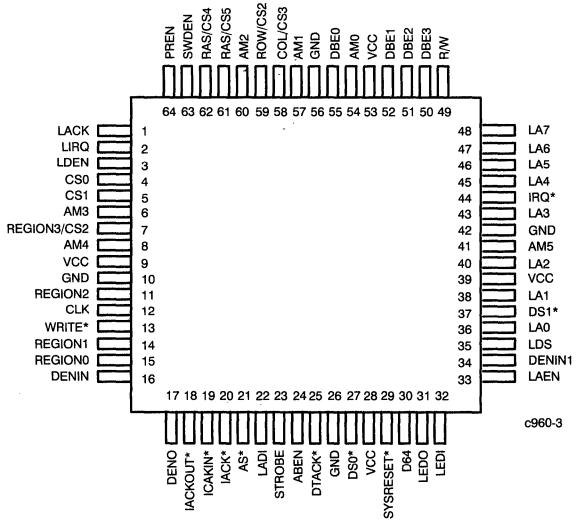


CY7C961 Logic Block Diagram

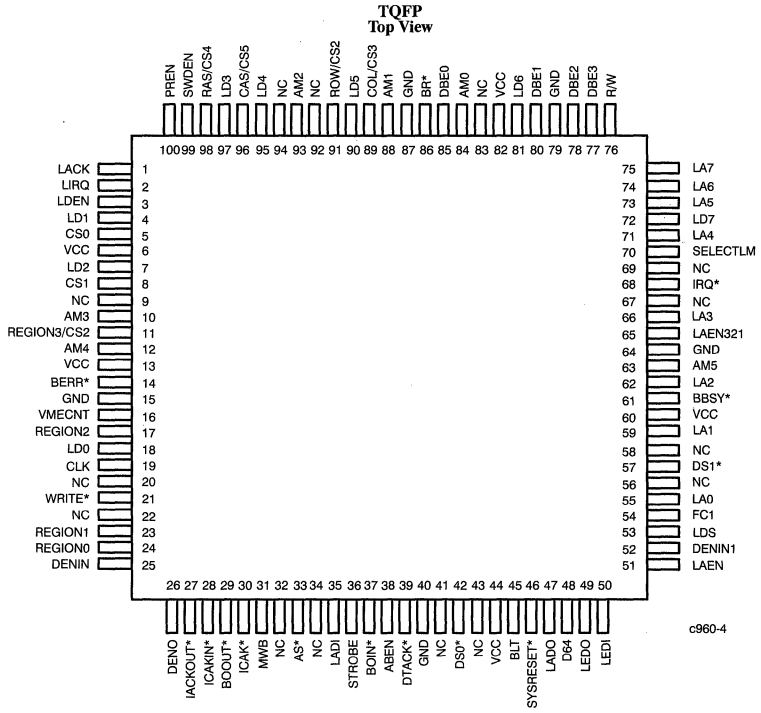


CY7C960 Pin Configuration

TQFP
Top View



CY7C961 Pin Configuration



Functional Description (continued)

The CY7C960 controls a bridge between the VMEbus and local DRAM and I/O. Once programmed, the CY7C960 provides activities such as DRAM refresh and local I/O handshaking in a manner that requires no additional local circuitry. The VMEbus control signals are connected directly to the CY7C960. The VMEbus address and data signals are connected to companion address/data transceivers which are controlled by the CY7C960. The CY7C964 VMEbus Interface Logic Circuit is an ideal companion device: the CY7C964 provides a slice of data and address logic that has been optimized for VME64 transactions. In addition to providing the specified drive strength and timing for VME64 transactions, the CY7C964 contains all the circuitry needed to multiplex the address/data bus for multiplexed VMEbus transactions. It contains counters and latches needed during BLT operations. And it also contains address comparators which can be used in the board's Slave Address Decoder. For a 6U or 9U application, four CY7C964 devices are controlled by a single CY7C960. For 3U applications, the CY7C960 controls two CY7C964 devices and an address latch.

The design of the CY7C960 makes it unnecessary to know the details of the VMEbus transaction timing and protocol. The complex VMEbus activities are translated by CY7C960 to simple local cycles involving a few familiar control signals. Similarly, it is not necessary to understand the operation of the companion device, CY7C964: all control sequences for the part are generated automatically by the CY7C960 in response to VMEbus or local activity. If more information is desired, consult the CY7C964 chapter in the *VIC64 Design Notes* (available separately).

VMEbus transactions supported by the CY7C960 include D8, D16, D32 (incl. UAT), MD32, D64, A16, A24, A32, A40, A64 single-cycle and block-transfer reads and writes, Read-Modify-Write cycles (incl. multiplexed), and Address-only (with or without Handshake). The CY7C960 functions as a VMEbus Interrupter, and supports the new Auto Slot ID standard and CR/CSR space. The CY7C960 also handles LOCK cycles, although full LOCK support is not possible within the constraints of the CY7C960 pinout. Full LOCK support is provided by the CY7C961.

On the local side, no CPU is needed to program the CY7C960, nor to manage transactions. All programmable parameters are initialized through the use of either the VMEbus or a serial PROM. As the CY7C960 incorporates a reliable power-on reset circuit, parameters are self-loaded by the device at power-up or after a system reset. If the VMEbus is used to provide parameters, a VMEbus Master provides the programming information using a protocol, described in the User's Guide, which is compliant with the Auto Slot ID protocol from the new VME64 specification.

To assist in generating the configuration file, a Windows-based program is available which guides the user through the process of

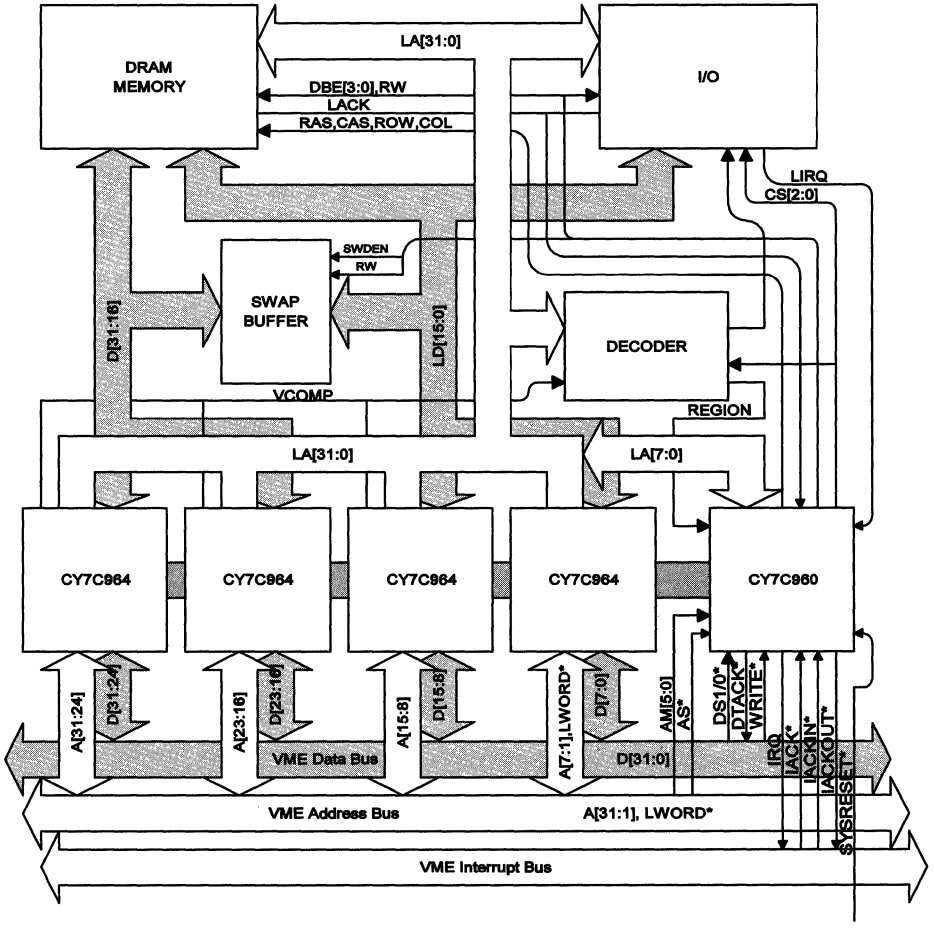
selecting appropriate options. Contact your Sales Office for further details.

The CY7C961 is a true superset of the CY7C960. Signal pins have been added to control CY7C964 DMA functions. Existing VMEbus input pins have been changed to bidirectional and augmented to complete a master interface. A data port and chip select signal (SELECTLM) complete the pin additions. As a VMEbus Slave, the CY7C961 behaves in every respect like the CY7C960. It simply has more pins, a master block transfer facility, and (because of the addition of the BBSY* connection) full lock cycle support.

From a system perspective, the CY7C961 master block transfer capability can be viewed as a DMA channel that resides on the slave card, but is controlled over the VMEbus by one or more VMEbus masters. The channel is programmed by VMEbus master accesses to the slave's DMA channel control registers. Once programmed, the CY7C961 acquires the VMEbus and transfers the data in one of 20 user-selected protocols.

The CY7C961 master block facility provides "block transfer on demand" capability for slave cards built around the Cypress CY7C961/CY7C964 chip set. This facility allows one or many VMEbus masters to write short series of commands to the slave card, telling it how much data to move, where to get it from, where to put it, and what transfer protocol to use while moving it. Blocks can be moved over the VMEbus as indivisible single cycles or BLTs. The protocol menu includes D8, D16, D32, MD32, or D64. A16, A24, A32, A40, and A64 address spaces can be specified. Burst lengths from 16 bytes to 8 megabytes can be requested. Eight registers accessible from the VMEbus make the facility simple to configure and simple to control. The facility has a busy semaphore, a VMEbus Interrupt on completion feature with a programmable Status/Id byte, and a built in requester and bus grant daisychain.

System Diagram Using the CY7C960



Related Documents

CY7C960 Family User's Guide

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C960–AC	A64	10x10 mm body Plastic Thin Quad Flat Pack	Commercial
CY7C960–NC	N65	14x14 mm body Plastic Quad Flat Pack	

Ordering Code	Package Name	Package Type	Operating Range
CY7C961–NC	A100	14x14 mm body Plastic Thin Quad Flat Pack	Commercial

Document #: 38–00250

CY7C964

Bus Interface Logic Circuit

Features

- **Comparators, counters, latches, and drivers minimize logic requirements for a variety of multiplexed and non-multiplexed buses**
- **Directly drives VMEbus address and data signals**
- **8-bit comparator for slave address decoding**
- **Flexible interface optimized for VMEbus applications**
- **Companion device to Cypress VMEbus family of components**
- **Replaces multiple SSI/MSI components**
- **Cascadable**
- **64-pin QFP and 68-pin PGA packages**
- **See the *VIC64/7C964 Design Notes* for more information**

Functional Description

The CY7C964 integrates several space-consuming functions into one small package, freeing board space for the implementation of added-value board features. It contains counters, comparators, latches, and drivers configured to be of value to implementors of any backplane interface with address and data buses, particularly VMEbus interfaces. The on-chip drivers are suitable for driving the VMEbus directly. The CY7C964 is ideal in applications where high-performance and real estate are primary concerns.

Although having many applications, the Bus Interface Logic Circuit is an ideal companion part to Cypress's VMEbus family of components, the VIC068A, VIC64, the CY7C960, and CY7C961. It is intended to drive the address and data buses, so three or four of these small devices are needed per controller. In every case, the controllers provide the control and timing signals to the Bus Interface Logic Circuit as it acts as a bridge between the VMEbus and the Local bus.

Application with VMEbus Architecture

Use with Cypress VMEbus Controllers

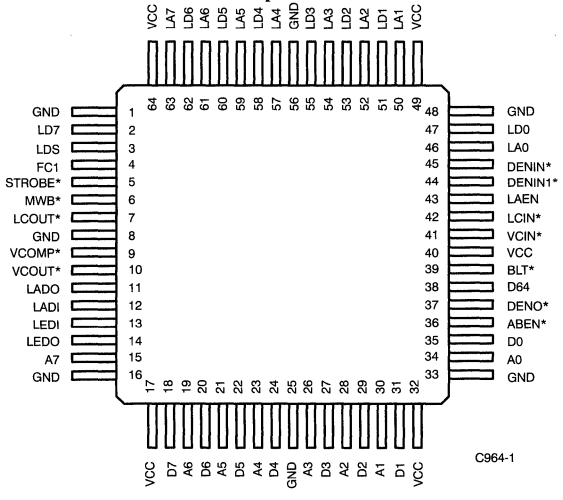
The CY7C964 Bus Interface Logic Circuit is a seamless interface between the VIC068A/VIC64 and the VMEbus signals. The device functions equally well in the established 32-bit VMEbus arena and the new 64-bit VMEbus standard. The device contains three 8-bit counters to fulfill the functions of Block counters, and DMA counters as implied by the D64 portion of the VMEbus specification. It also contains the necessary multiplexing logic to allow the 64-bit-wide VMEbus path to be funnelled to and from the 32-bit local bus. Control circuitry is included to manage the switching of the 32-bit address bus during normal (32-bit) operations, and during MBLT (64-bit) operations. The on-chip drivers are capable of driving the VMEbus directly (48 mA).

Use in Other VMEbus Controller Implementations

The CY7C964 circuitry is designed to be of use to designers of VMEbus circuitry, including VSB (VME subsystem bus) and designs not requiring the features of the Cypress VIC068A, VIC64, CY7C960, and CY7C961. The logic diagram includes general-purpose blocks of comparators, counters, and latches that can be controlled using the flexible control interface to allow many different options to be implemented. Although the device is packaged in a small 64-pin package, the use of multiplexed input and output pins provides access to the many internal functions, thus saving external circuitry.

Pin Configuration

PQFP/CQFP/TQFP
Top View



C964-1

Pin Configuration (continued)

68-Pin Ceramic PGA
Bottom View

11	10	9	8	7	6	5	4	3	2	1	
	A0	ABEN*	D64	V_{CC}	LCIN*	DENIN1*	LA0	GND	V_{CC}		A
GND	GND	D0	DENO*	BLT*	VCIN*	LAEN	DENIN*	LD0	V_{CC}	LA1	B
V_{CC}	D1								LD1	LA2	C
A1	D2								LD2	LA3	D
A2	D3								LD3	GND	E
A3	GND								LA4	LD4	F
D4	A4								LA5	LD5	G
D5	A5								LA6	LD6	H
D6	A6								LA7	V_{CC}	J
D7	V_{CC}	A7	LEDI	LADO	VCOMP*	LCOUT*	STROBE*	LDS	GND	V_{CC}	K
	GND	GND	LEDO	LADI	VCOUT*	GND	MWB*	FC1	LD7		L

Index Mark On Top

C964-2

Application with Other Bus Architectures

The CY7C964 is optimized for applications requiring wide buffers and high-performance multiplexing operations. The architecture can be configured to provide functions such as 16-bit bidirectional three-state latch and 16-bit comparator with mask register, or more complex functions such as 16-to-8 pipelined bidirectional multiplexer with address counter/comparator circuitry. The device can be cascaded to generate counters and comparators suitable for multiple byte address/data buses. The on-chip 48 mA drivers can be directly connected to many standard backplane buses.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C964–AC	A64	64-Pin Thin Quad Flatpack	Commercial
CY7C964–NC	N65	64-Pin Plastic Quad Flatpack	
CY7C964–GM	G68	68-Pin Ceramic PGA	Military Temp. Commercial
CY7C964–GMB	G68	68-Pin Ceramic PGA	MIL-STD-883
CY7C964–UM	U65	64-Pin Ceramic Quad Flatpack	Military Temp. Commercial
CY7C964–UMB	U65	64-Pin Ceramic Quad Flatpack	MIL-STD-883

Related Documents

VIC64/CY7C964 Design Notes
VIC068A/VAC068A User's Guide
CY7C690 and CY7C961 User's Guide

Document #: 38–00197–B

Section Contents

FCT Logic Products

FCT Logic Products (continued)

Parameter Measurement Information

Features

- **Function, pinout, speed, and drive compatible with F Logic**
- **Meets requirements of FCT Logic JEDEC Standard No. 18A**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature on all families**
- **Matched rise and fall times**
- **CMOS for low power consumption – typically 1/3 of the fastest advanced Schottky TTL logic**
- **Inputs and outputs interface directly with TTL, NMOS, and CMOS devices**
- **Typically 64 mA Sink and 32 mA Source Drive Capability**
- **Three-state outputs on most devices**
- **Operational over the full commercial and military temperature ranges (Octal)**
- **Extended commercial temperature range of −40°C to +85°C (16-bit family)**
- **Products available to latest revision of MIL-STD-8833 class B compliance**

Functional Description

Overview

FCT-T, FCT2-T, and FCT16-T are logic families consisting of high-performance, low power, CMOS integrated circuits that either meet or exceed the speed and drive capability of their popular functional equivalents. These families represent a technology crossover point that occurred when the performance achieved using CMOS technology matched that of bipolar technology at one-third the power.

All logic families are TTL compatible, which means that they conform to the industry-standard TTL voltage levels and threshold point, and operate from a 5V V_{CC} power source. The TTL threshold point is 1.5V. All inputs have hysteresis. The benefit to the user is increased static and dynamic noise immunity, as well as less sensitivity to noise superimposed on slowly rising or falling inputs.

The outputs of the original FCT family swing rail-to-rail, i.e., from V_{OL}=0.4V to V_{OH}=V_{CC}−0.2V. The datasheets specify V_{OH} minimum as 2.4V when sourcing 15 mA and typical as 4.3. The output pull-up transistor is a p-channel device. Typical unloaded output signal rise and fall times are one nanosecond.

The new FCT-T logic families feature output buffers that use n-channel pullup transistors and controlled rise and fall time edge rates. Typical unloaded output signal rise and fall times are two nanoseconds. The maximum unloaded output high voltage, V_{OH}, is V_{CC} minus the n-channel threshold, V_T. The transistor drain is connected to V_{CC}, so V_T is approximately one volt. The loaded V_{OH} is typically 3.3 Volts when sourcing 15 mA with a V_{CC} of 5.0V.

The reduced output voltage swing of FCT-T results in lower crosstalk. The controlled edge rates reduce crosstalk as well as ground bounce.

The FCT2-T logic family is identical to the FCT-T logic family, except that the FCT2-T devices have a 25-Ohm resistor in series with the output. The purpose of the resistor is to provide series damping when driving a transmission line. These products with series damping resistors should be used only when driving lumped (or single) loads, and should not be used for driving multiple or distributed loads. For a description of series damping, see the application note "System Design Considerations When Using Cypress CMOS Circuits" in the *Cypress Applications Handbook.*

The FCT16-T logic family is a 16-bit version of the FCT-T family. The commercial temperature range of the family has been extended to −40°C to +85°C and Vcc tolerance has been loosened to ±10%. Multiple power and grounds have been added to reduce typical ground bounce to below 1.0V.

The FCT162-T logic family is a 24 mA balanced drive version of the FCT16-T family and is intended for use in driving transmission lines.

CMOS Process Technology

All products are manufactured using the Logic 2.7 process and are fabricated in a Class 1 facility on six inch wafers. The minimum drawn channel length is 0.65 microns. The process uses one layer of polysilicon and two layers of metal. There is no substrate bias generator. In addition to providing high density, the technology assures latch-up protection, single event upset protection, and excellent ESD protection.

Switching Characteristics

The circuit of *Figure 1* is used to load each output for specifying and measuring device propagation delays. It is a de facto industry standard and does not represent device behavior in any application.

The switch is open for all measurements except those having to do with the outputs entering or leaving the high impedance state as a result of a control input changing.

These conditions are illustrated in *Figures 7* and *8*. The parameter t_{PZL} is the amount of time it takes an output to go from the high-impedance state to a low state. The parameter t_{PLZ} is the amount of time it takes an output to go from the LOW state to the high-impedance state: defined as 300 mV above V_{OL}. The parameter t_{PZH} is the amount of time it takes an output to go from a high-impedance state to the HIGH state. The parameter t_{PHZ} is the amount of time it takes an output to go from a HIGH state to the high-impedance state; defined as 300 mV below V_{OH}.

Figures 2 through *9* illustrate the various propagation delay, set-up times, and hold times that are referred to in the Switching Characteristics section of the various datasheets. Note that except for entering the high impedance state, all measurements are made between the 1.5V amplitude voltage levels.

The input waveform amplitude levels recommended for AC testing of Cypress logic products are illustrated in *Figure 10*. Input signals should have maximum rise and fall times of 2.5 ns and signal swings of zero to three volts. Input signals with rise and fall times of one nanosecond should be used for testing minimum pulse width or maximum frequency.

When performing AC tests, care must be taken to insure that the input signals do not return to the transition region due to signal overshoot or undershoot. It is recommended that the load capacitor be a leaderless chipcap. If this is not possible, keep the leads as short as possible in order to avoid signal overshoot and undershoot due to lead inductance. The same reasoning applies to the load resistors and power supply decoupling and filtering capacitors. Solid grounding is required and a ground plane is recommended.

Power Specifications

Cypress logic devices do not use a substrate bias generator. As a result, the quiescent or standby current is typically a few microamperes when the voltage at the inputs are either less than 0.2V or greater than $V_{CC}-0.2V$. On the datasheet this current is described as Quiescent Power Supply Current, given the symbol I_{CC}, and specified on a per IC basis. No inputs are switching and all outputs are open, and if possible, disabled.

When the input signal transitions between the logic levels, both the p-channel pull-up transistor and the n-channel pulldown transistor in the input TTL to CMOS translator are partially turned on, which creates a low-impedance path between V_{CC} and ground. On the datasheet this current is described as "Quiescent Power Supply Current (TTL inputs)," given the symbol ΔI_{CC}, and specified on a per input basis. One input is at $V_{IN}=3.4V$ and other inputs at either V_{CC} or 0 Volts, and all outputs are open, and if possible, disabled.

The Dynamic Power Supply Current, given the symbol I_{CCD}, is not measured directly, but is provided so that the user can calculate total current. It is specified in mA per Megahertz at 50% duty cycle, with one input toggling and one output toggling (enabled) but open (unloaded).

Note that the preceding three currents are specified with the outputs open. The AC CVf current required to charge and discharge parasitic capacitances (e.g., other inputs being driven by the outputs), as well as any DC load currents must be calculated separately.

Total supply current, I_C, is specified on the data sheet for several different conditions. The inputs are switched between ground and either TTL (3.4V) or CMOS ($V_{CC}-0.2V$) levels with rise and fall times of 2.5 ns. Slow rise and fall times can cause the dynamic current to increase, because the input signals are within the transition region for longer times. A characterization curve of normalized ($I_{CC}/\Delta I_{CC}$) currents versus V_{IN} is shown in *Figure 14*.

Total device current can be estimated by using the following formula to calculate the total current. This equation implies calculating the current associated with each input and adding them up. The same procedure must be followed to calculate the CVf current required to charge and discharge the load capacitances.

$$I_C=I_{CC}+\Delta I_{CC} D_H N_T+I_{CCD} (f_{cp}/2+f_n N_n)$$

Where:

I_{CC} = Quiescent Current
I_{CC} = Power Supply Current for a TTL HIGH input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f_{CP} = Clock frequency for registered devices, otherwise zero
f_n = Input signal frequency
N_n = Number of inputs changing at Fn

ESD (Electrostatic Discharge) Precautions

Large electrical fields can damage the thin gate oxides of MOS transistors. Special input protection circuits are used at every input pin of all Cypress products to provide protection against ESD. This circuitry has been designed to withstand repeated applications of high voltages without failure or performance degradation. This is accomplished by preventing the high voltage (ESD) from reaching the thin gate oxides of the internal transistors. For a description of the ESD protection circuit and an explanation of its operation, please see the application note titled "Input/Output Characteristics of Cypress Circuits" in the *Cypress Applications Handbook.*

Precautions should be taken by persons handling CMOS devices. It is recommended that individuals wear a grounded wrist strap or ankle strap when handling Cypress FCT-T devices.

Maximum Ratings[1, 2]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range FCT-T, FCT2-T

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, BT	−40°C to +85°C	5V ± 5%
Military[3]	All	−55°C to +125°C	5V ± 10%

Operating Range FCT16-T

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

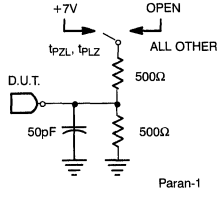


Figure 1. Test Load

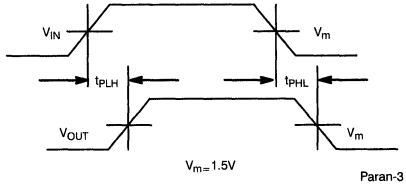


Figure 3. Waveform for Non-Inverting Functions

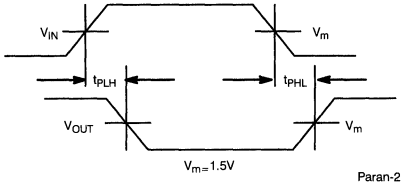


Figure 2. Waveform for Inverting Functions

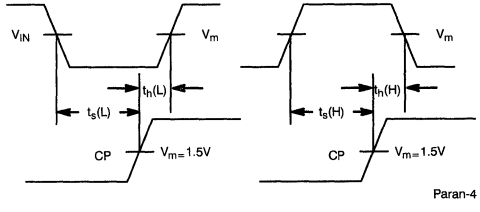


Figure 4. Set-Up and Hold Times, Rising-Edge Clock

Notes:

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. T_A is the "instant on" case temperature.

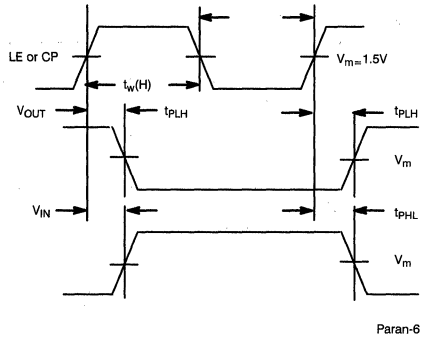


Figure 5. Propagation Delays from Rising-Edge Clock or Enable

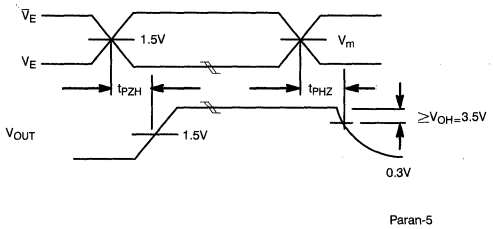


Figure 8. Three-State Output HIGH Enable and Disable Times

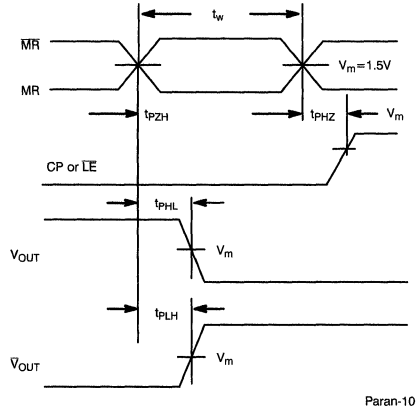


Figure 6. Asynchronous Reset, Active Rising-Edge Clock or Active LOW Enable

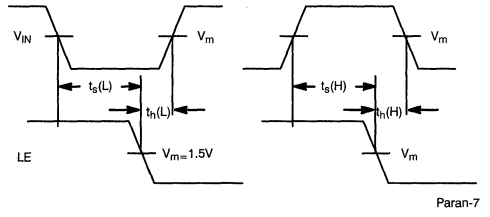


Figure 9. Set-Up and Hold Times to Active HIGH Enable or Parallel Load

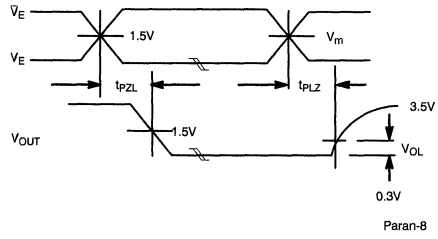


Figure 7. Three-State Output LOW Enable and Disable Times

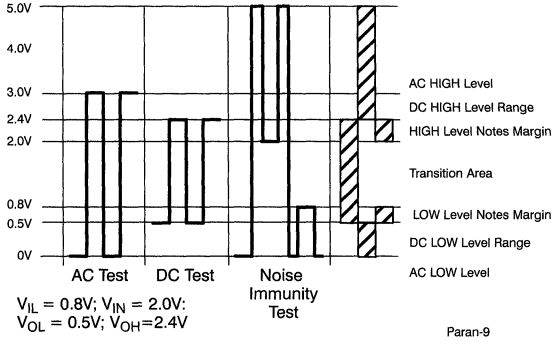


Figure 10. Input Signal Levels

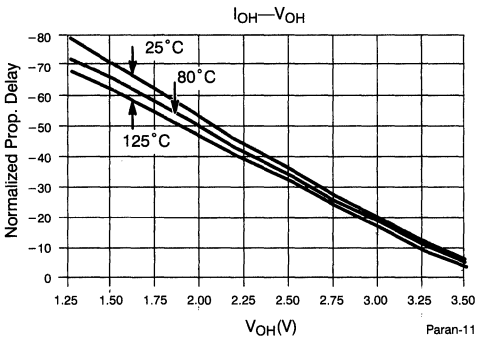


Figure 11. Output Source Current vs. Output Voltage

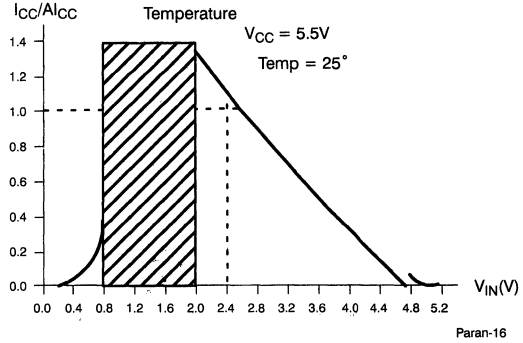


Figure 14. Normalized Current vs. Input Voltage

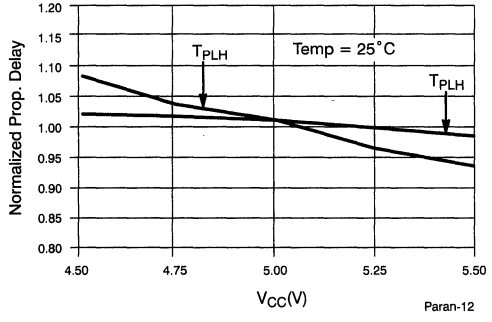


Figure 12. Normalized Propagation Delay vs. V_{CC}

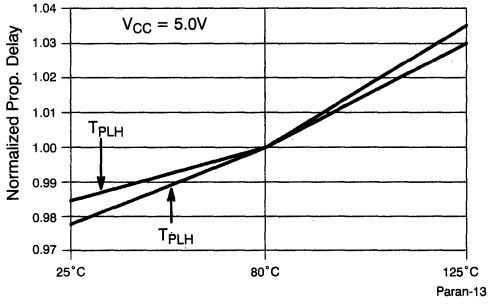


Figure 15. Normalized Propagation Delay vs. Temperature

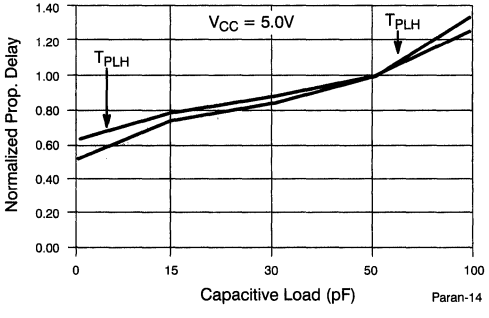


Figure 13. Normalized Propagation Delay vs. Output Loading

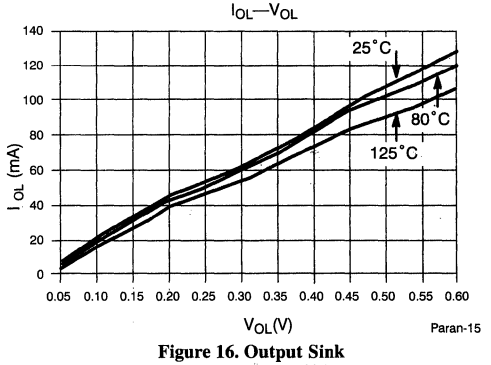


Figure 16. Output Sink Current vs. Output Voltage

CY29FCT52T

8-Bit Registered Transceiver

Features

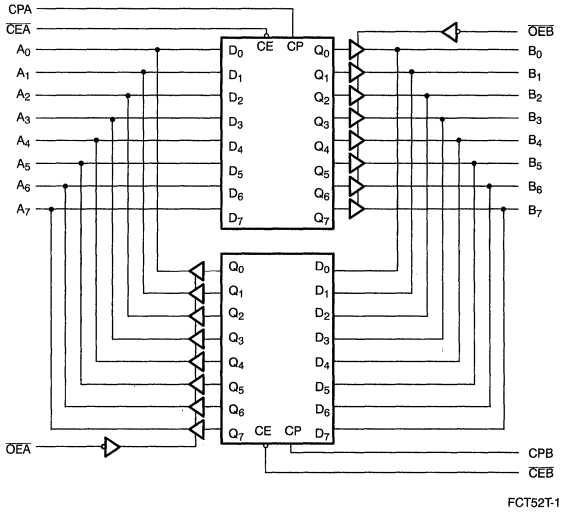
- **Function, pinout, and drive compatible with FCT, F Logic and AM2952**
- **FCT-C speed at 6.3 ns max. (Com'l) FCT-B speed at 7.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **ESD > 2000V**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink Current 64 mA (Com'l), 48 mA (Mil)**
- **Source Current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

The CY29FCT52T has two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Separate clock, clock enable, and three-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64 mA.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

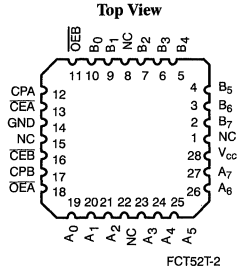
Logic Block Diagram



FCT52T-1

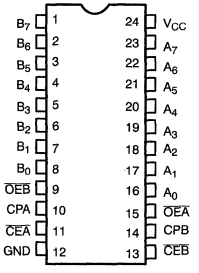
Pin Configurations

LCC
Top View



FCT52T-2

DIP/SOIC/QSOP
Top View



FCT52T-3

Function Table[1]

Inputs				
D	CP	$\overline{CE}$	Internal Q	Function
X	X	H	NC	Hold Data
L	⌐	L	L	Load Data
H	⌐	L	H	

Output Control

$\overline{OE}$	Internal Q	Y-Outputs	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Pin Description

Name	Description
A	A register inputs or B register outputs.
B	B register inputs or A register outputs.
CPA	Clock for the A register. When $\overline{CEA}$ is LOW, data is entered into the A register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	Clock Enable for the A register. When $\overline{CEA}$ is LOW, data is entered into the A register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A register holds its contents regardless of CPA signal transitions.
$\overline{OEA}$	Output Enable for the A register. When $\overline{OEA}$ is LOW, the A register outputs are enabled onto the B lines. When $\overline{OEA}$ is HIGH, the B outputs are in the high impedance state.
CPB	Clock for the B register. When $\overline{CEB}$ is LOW, data is entered into the B register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	Clock Enable for the B register. When $\overline{CEB}$ is LOW, data is entered into the B register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B register holds its contents regardless of CPA signal transitions.
$\overline{OEB}$	Output Enable for the B register. When $\overline{OEB}$ is LOW, the B register outputs are enabled onto the A lines. When $\overline{OEB}$ is HIGH, the A outputs are in the high impedance state.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.

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Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEA}$ or $\overline{OEB}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_i N_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	29FCT52AT				29FCT52BT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CPA, $\overline{CPB}$ to A, B	2.0	11.0	2.0	10.0	2.0	8.0	2.0	7.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	13.0	1.5	10.5	1.5	8.5	1.5	8.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		2.5		2.5		ns	4
t_H	Hold Time HIGH or LOW, A, B to CPA, CPB	2.0		2.0		1.5		1.5		ns	4
t_S	Set-Up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	3.0		3.0		3.0		3.0		ns	4
t_H	Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0		2.0		2.0		2.0		ns	4
t_W	Pulse Width,[6] HIGH or LOW, CPA or CPB	3.0		3.0		3.0		3.0		ns	5

Parameter	Description	29FCT52CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to A, B	2.0	7.3	2.0	6.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PHZ} t_{PHZ}	Output Disable Time, $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		ns	4
t_H	Hold Time HIGH or LOW, A, B to CPA, CPB	1.5		1.5		ns	4
t_S	Set-Up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	3.0		3.0		ns	4
t_H	Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0		2.0		ns	4
t_W	Pulse Width,[6] HIGH or LOW, CPA or CPB	3.0		3.0		ns	5

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY29FCT52CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY29FCT52CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY29FCT52BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY29FCT52BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY29FCT52ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY29FCT52ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52ATLMB	L64	28-Square Leadless Chip Carrier	

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CY29FCT520T

Multi-Level Pipeline Register

Features

- **Function, pinout, and drive compatible with FCT, F Logic, and AM29520**
- **FCT-C speed at 6.0 ns max. (Com'l) FCT-B speed at 7.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-Off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Single and dual pipeline operation modes**
- **Multiplexed data inputs and outputs**

Functional Description

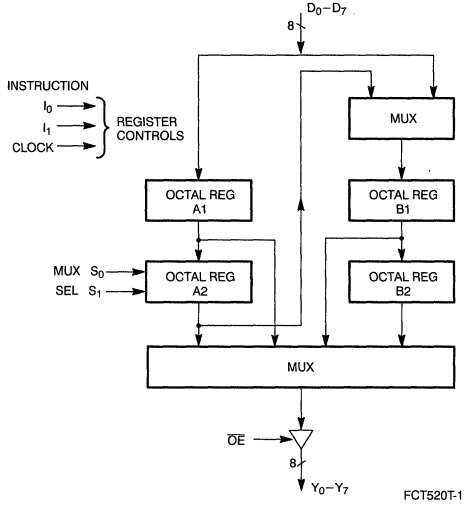
The FCT520T is a multi-level 8-bit-wide pipeline register. The device consists of four registers, A1, A2, B1, and B2, which are configured by the instruction inputs I_0, I_1 as a single 4-level pipeline or as two two-level pipelines. The contents of any register may be read at the multiplexed output at any time by using the mux-selection controls S_0 and S_1.

The pipeline register is positive edge triggered and data is shifted by the rising edge of the clock input. Instruction I=0 selects the four-level pipeline mode. Instruction I=1 selects the two-level B pipeline while I=2 selects the two-level A pipeline. I=3 is the HOLD instruction; no shifting is performed by the clock in this mode.

In the two-level operation mode, the FCT520T data is shifted from level 1 to level 2 and new data is loaded into level 1.

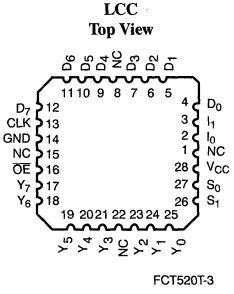
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

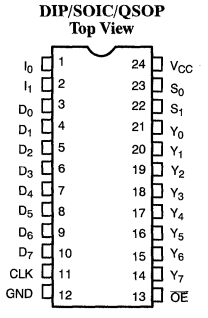


FCT520T-1

Pin Configurations



FCT520T-3



FCT520T-2

Pipeline Instruction Table

I = 0		I = 1		I = 2		I = 3	
I_1= 0	I_0= 0	I_1= 0	I_0= 1	I_1= 1	I_0= 0	I_1= 1	I_0= 1
A1 → A2 B1 → B2		A1 → A2 B1 → B2		A1 → A2 B1		A1 B1 → B2	
Single four-level		Dual two-level				Hold	

Output Selection Mux Table

Inputs		Output
S_1	S_0	
1	1	A1
1	0	A2
0	1	B1
0	0	B2

Maximum Ratings[1, 2]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[3]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[5]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[5]

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. T_A is the "instant on" case temperature.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[7] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[10]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	5.1	14.3[10]	mA

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT520AT				FCT520BT				Unit	Fig. No.[12]
		Military		Commercial		Military		Commercial			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Data Output	2.0	16.0	2.0	14.0	2.0	8.0	2.0	7.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Data Output	2.0	15.0	2.0	13.0	2.0	8.0	2.0	7.5	ns	1, 5
t_S	Set-Up Time Input Data to Clock	6.0		5.0		2.8		2.5		ns	4
t_H	Hold Time Input Data to Clock	2.0		2.0		2.0		2.0		ns	4
t_S	Set-Up Time Instruction (Reg. Enable) to Clock	6.0		5.0		4.5		4.0		ns	4
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0		2.0		2.0		2.0		ns	4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	13.0	1.5	12.0	1.5	7.5	1.5	7.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time	1.5	16.0	1.5	15.0	1.5	8.0	1.5	7.5	ns	1, 7, 8
t_W	Clock Pulse Width,[5] HIGH or LOW	8.0		7.0		6.0		5.5		ns	5

Parameter	Description	FCT520CT				Unit	Fig. No.[12]
		Military		Commercial			
		Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Data Output	2.0	7.0	2.0	6.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Data Output	2.0	7.0	2.0	6.0	ns	1, 5
t_S	Set-Up Time Input Data to Clock	2.8		2.5		ns	4
t_H	Hold Time Input Data to Clock	2.0		2.0		ns	4
t_S	Set-Up Time Instruction (Reg. Enable) to Clock	4.5		4.0		ns	4
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0		2.0		ns	4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	6.0	1.5	6.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time	1.5	7.0	1.5	6.0	ns	1, 7, 8
t_W	Clock Pulse Width,[5] HIGH or LOW	6.0		5.5		ns	5

Notes:
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT520CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT520CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.0	CY29FCT520CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT520CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY29FCT520BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT520BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY29FCT520BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT520BTLMB	L64	28-Square Leadless Chip Carrier	
14.0	CY29FCT520ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT520ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
16.0	CY29FCT520ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT520ATLMB	L64	28-Square Leadless Chip Carrier	

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CY29FCT818T

Diagnostic Scan Register

Features

- **Function, pinout and drive compatible with FCT, F Logic and AM29818**
- **FCT-C speed at 6.0 ns max. (Com'l) FCT-B speed at 7.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 20 mA (Mil)**
  Source current 32 mA (Com'l), 3 mA (Mil)
- **8-Bit pipeline and shadow register**
- **ESD > 2000V**

Functional Description

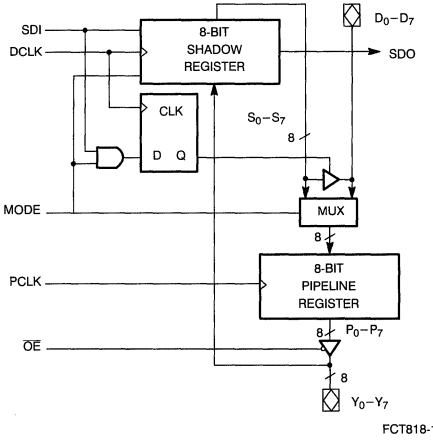
The FCT818T contains a high-speed 8-bit general-purpose data pipeline register and a high-speed 8-bit shadow register. The general-purpose register can be used in an 8-bit wide data path for a normal system application. The shadow register is designed for applications, such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

The shadow registers can load data from the output of the FCT818T, and can be used as a right-shift register with bit-serial input SDI and output SDO, using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins using PCLK. Note that data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register provided set-up and hold time requirements are satisfied with respect to the two independent clock inputs.

In a typical application, the general-purpose register in the FCT818T replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxillary bit-serial loop which is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxillary diagnostic loop to make it accessible to the diagnostics controller. This data is then compared with the expected value to diagnose faulty operation of the sequential circuit.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

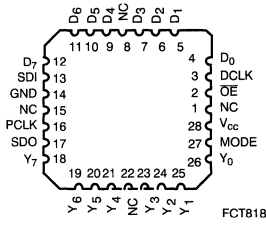
Logic Block Diagram



FCT818-1

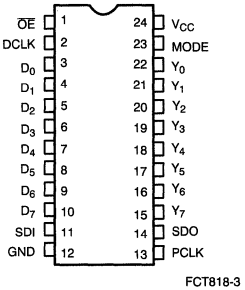
Pin Configurations

LCC
Top View



FCT818-2

DIP, SOIC, QSOP
Top View



FCT818-3

Function Table[1]

Inputs			Inputs		Shadow Register	Pipeline Register	Operation
MODE	SDI	DCLK	PCLK	SDO			
L	X	↓	X	S_7	$S_0 \leftarrow SDI$ $S_i \leftarrow S_{i-1}$	NA	Serial Shift; D_7-D_0 Output Disabled
L	X	X	↓	S_7	NA	$P_i \leftarrow D_i$	Load Pipeline Register from Data Input
H	L	↓	X	L	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y Output
H	H	↓	X	H	Hold	NA	Hold Shadow Register; D_7-D_0 Output Enabled
H	X	X	↓	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT, BT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−3 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=20 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. NA = Not Applicable
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$		0.25	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$		5.3	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND		7.3	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, f_1=5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$		17.8[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND		30.8[11]	mA

Note:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	FCT818T				FCT818AT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PD}	Propagation Delay										
	PCLK to Y		18		13		12		9	ns	5
	MODE to SDO		18		16		18		16	ns	6
	SDI to SDO		18		16		18		15	ns	3
	DCLK to SDO		30		25		30		25	ns	5
t_S	Set-Up Time										
	D to PCLK	10		8		6		4		ns	
	MODE to PCLK	15		15		15		15		ns	
	Y to DCLK	5		5		5		5		ns	
	MODE to DCLK	12		12		12		12		ns	4
	SDI to DCLK	10		10		10		10		ns	
	DCLK to PCLK	15		15		15		15		ns	
	PCLK to DCLK	45		40		45		40		ns	
t_H	Hold Time										
	D to PCLK	2		2		2		2		ns	
	MODE to PCLK	0		0		0		0		ns	
	Y to DCLK	5		5		5		5		ns	4
	MODE to DCLK	5		2		5		2		ns	
	SDI to DCLK	0		0		0		0		ns	
t_{PLZ}	Output Disable Time LOW										
	$\overline{OE}$ to Y		20		15		20		15	ns	7
	DCLK to D		45		45		45		45	ns	5
t_{PHZ}	Output Disable Time HIGH										
	$\overline{OE}$ to Y		30		25		30		25	ns	8
	DCLK to D		90		85		90		80	ns	5
t_{PZL}	Output Enable Time LOW										
	$\overline{OE}$ to Y		20		15		20		15	ns	7
	DCLK to D		35		30		35		25	ns	5
t_{PZH}	Output Enable Time HIGH										
	$\overline{OE}$ to Y		20		15		20		15	ns	8
	DCLK to D		30		25		30		25	ns	5
t_W	Pulse Width										
	PCLK (HIGH and	15		15		15		10		ns	5
	LOW)	25		25		25		15		ns	5
	DCLK (HIGH and LOW)										

Notes:

12. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information Section".
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.

Switching Characteristics Over the Operating Range[12] (continued)

Parameter	Description	FCT818BT				FCT818CT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PD}	Propagation Delay										
	PCLK to Y		9.0		7.5		7.6		6.0	ns	5
	MODE to SDO		10.5		9.0		8.9		7.2	ns	6
	SDI to SDO		10.5		9.0		8.9		7.1	ns	3
	DCLK to SDO		10.5		9.0		8.9		7.2	ns	5
t_S	Set-Up Time										
	D to PCLK	4.5		3.0		3.0		2.0		ns	
	MODE to PCLK	6.5		5.0		5.0		3.5		ns	
	Y to DCLK	4.5		3.0		3.0		2.0		ns	
	MODE to DCLK	6.5		5.0		5.0		3.5		ns	4
	SDI to DCLK	6.5		5.0		5.0		3.5		ns	
	DCLK to PCLK	6.5		5.0		5.0		3.5		ns	
	PCLK to DCLK	12.5		11.0		11.0		8.5		ns	
t_H	Hold Time										
	D to PCLK	2.0		2.0		2.0		1.5		ns	
	MODE to PCLK	0		0		0		0		ns	
	Y to DCLK	3.0		2.0		3.0		1.5		ns	4
	MODE to DCLK	3.0		2.0		3.0		1.5		ns	
	SDI to DCLK	0		0		0		0		ns	
t_{PLZ}	Output Disable Time LOW										
	$\overline{OE}$ to Y		8.5		7.0		7.0		5.5	ns	7
	DCLK to D		8.5		7.0		7.0		5.5	ns	5
t_{PHZ}	Output Disable Time HIGH										
	$\overline{OE}$ to Y		10.5		9.0		9.0		8.0	ns	8
	DCLK to D		10.5		9.0		9.0		8.0	ns	5
t_{PZL}	Output Enable Time LOW										
	$\overline{OE}$ to Y		11.5		10.0		10.0		8.0	ns	7
	DCLK to D		11.5		10.0		10.0		9.0	ns	5
t_{PZH}	Output Enable Time HIGH										
	$\overline{OE}$ to Y		11.5		10.0		10.0		8.5	ns	8
	DCLK to D		12.5		11.0		11.0		9.0	ns	5
t_W	Pulse Width										
	PCLK (HIGH and	7.0		6.0		6.0		5.0		ns	5
	LOW)	7.0		6.0		6.0		5.0		ns	5
	DCLK (HIGH and LOW)										

9

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT818CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY29FCT818BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.6	CY29FCT818CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818CTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY29FCT818ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
	CY29FCT818BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818BTLMB	L64	28-Square Leadless Chip Carrier	
12.0	CY29FCT818ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818ATLMB	L64	28-Square Leadless Chip Carrier	
13.0	CY29FCT818TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818TQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818TSOC	S13	24-Lead (300-Mil) Molded SOIC	
18.0	CY29FCT818TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818TLMB	L64	28-Square Leadless Chip Carrier	

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CY54/74FCT138T

1-of-8 Decoder

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.0 ns max. (Com'l) FCT-A speed at 5.8 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**
- **Dual 1-of-8 decoder with enables**

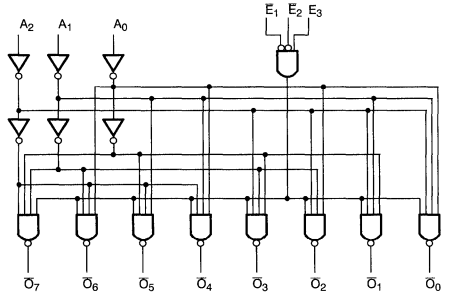
Functional Description

The FCT138T is a 1-of-8 decoder. The FCT138T accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0 - \overline{O}_7$). The FCT138T features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3).

All inputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four FCT138T devices and one inverter.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

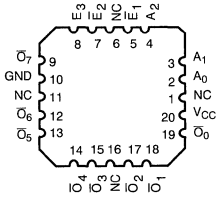
Logic Block Diagram



FCT138T-1

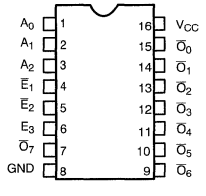
Pin Configurations

LCC
Top View



FCT138T-2

DIP/SOIC/QSOP
Top View



FCT138T-3

Pin Description

Name	Description
A	Address Inputs
$\overline{E}_1 - \overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}$	Outputs

Function Table[1]

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, Toggle $\overline{E}_1$, $\overline{E}_2$, or E_3, One Output Toggling, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, Toggle $\overline{E}_1$, $\overline{E}_2$, or E_3, One Output Toggling, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT138T				FCT138AT				Unit	Fig. No.[12]
		Military		Commercial		Military		Commercial			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to $\overline{O}$	1.5	12.0	1.5	9.0	1.5	7.8	1.5	5.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}$	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}$	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	ns	1, 5

Parameter	Description	FCT138CT				Unit	Fig. No.[12]
		Military		Commercial			
		Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to $\overline{O}$	1.5	6.0	1.5	5.0	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}$	1.5	6.1	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}$	1.5	6.1	1.5	5.0	ns	1, 5

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.0	CY74FCT138CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY74FCT138ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT138CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.8	CY54FCT138ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138ATLMB	L61	20-Pin Square Leadless Chip Carrier	
9.0	CY74FCT138TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138TSOC	S1	16-Lead (300-Mil) Molded SOIC	
12.0	CY54FCT138TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138TLMB	L61	20-Pin Square Leadless Chip Carrier	

Notes:
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information Section.

Document #: 38-00297-A

Quad 2-Input Multiplexers

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 4.3 ns max. (Com'l) FCT-A speed at 5.0 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

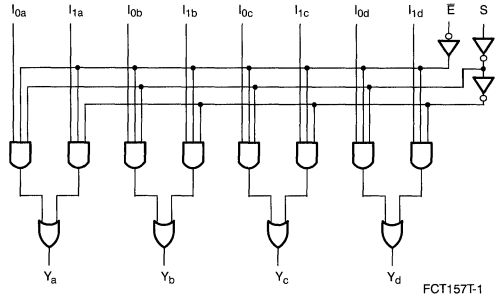
The FCT157T and FCT158T are quad two-input multiplexers that select four bits of data from two sources under the control of a common data Select input (S). The Enable input ($\overline{E}$) is Active LOW. When ($\overline{E}$) is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the FCT157T and FCT158T. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the sixteen different functions of two variables with one variable common.

These devices are logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The outputs of the FCT157T are non-inverting whereas the FCT158T has inverting outputs.

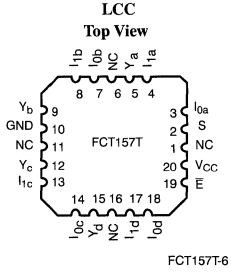
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram, FCT157T

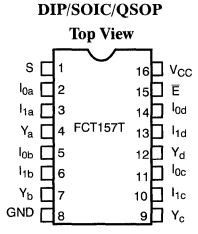


FCT157T-1

Pin Configurations

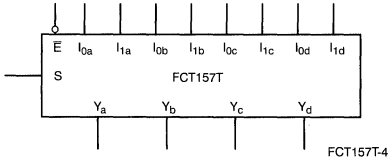


FCT157T-6



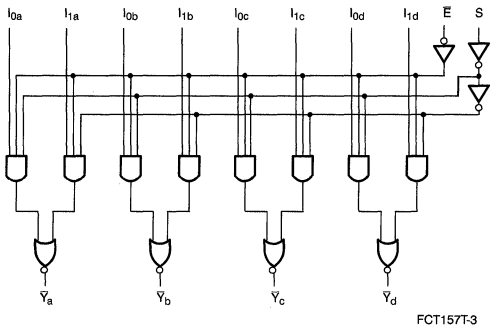
FCT157T-5

Logic Symbol



FCT157T-4

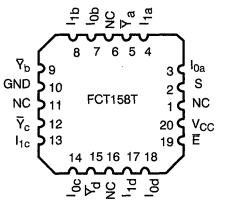
Logic Block Diagram, FCT158T



FCT157T-3

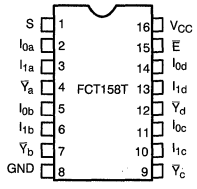
Pin Configurations

LCC
Top View



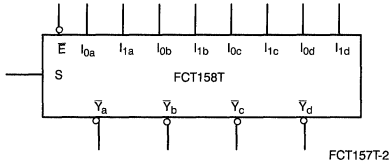
FCT157T-5

DIP/SOIC/QSOP
Top View



FCT157T-4

Logic Symbol



FCT157T-2

Pin Description

Name	Description
S	Common Select Input
$\overline{E}$	Enable Inputs (Active LOW)
I_0	Data Inputs from Source 0
I_1	Data Inputs from Source 1
Y	Non-Inverted Output (FCT157T)
$\overline{Y}$	Inverted Output (FCT158T)

Function Table[1]—FCT157T

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	H
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Function Table[1]—FCT158T

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f_1=10 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f_1=10 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.7	5.4[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT157T				FCT157AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to Y	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Y	1.5	12.0	1.5	10.5	1.5	7.4	1.5	6.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	ns	1, 3

Parameter	Description	FCT157CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to Y	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Y	1.5	5.9	1.5	4.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.5	6.0	1.5	5.2	ns	1, 3

Switching Characteristics Over the Operating Range

Parameter	Description	FCT158T				FCT158AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to $\overline{Y}$	1.5	7.5	1.5	6.5	1.5	6.3	1.5	5.5	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Y}$	1.5	12.5	1.5	11.0	1.5	7.9	1.5	6.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Y}$	1.5	12.5	1.5	11.0	1.5	8.6	1.5	7.5	ns	1, 2

Parameter	Description	FCT158CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to $\overline{Y}$	1.5	5.5	1.5	4.3	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Y}$	1.5	6.4	1.5	4.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Y}$	1.5	6.5	1.5	5.2	ns	1, 2

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information—FCT157T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT157CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT157CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT157CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT157ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT157ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT157ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT157CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT157CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.8	CY54FCT157ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT157ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.0	CY74FCT157TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT157TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT157TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT157TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT157TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT158T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT158CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT158CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT158CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.5	CY74FCT158ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT158ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT158ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.5	CY54FCT158CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT158CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.3	CY54FCT158ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT158ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT158TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT158TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT158TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT158TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT158TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38–00288–A

CY54/74FCT163T

4-Bit Binary Counter

Features

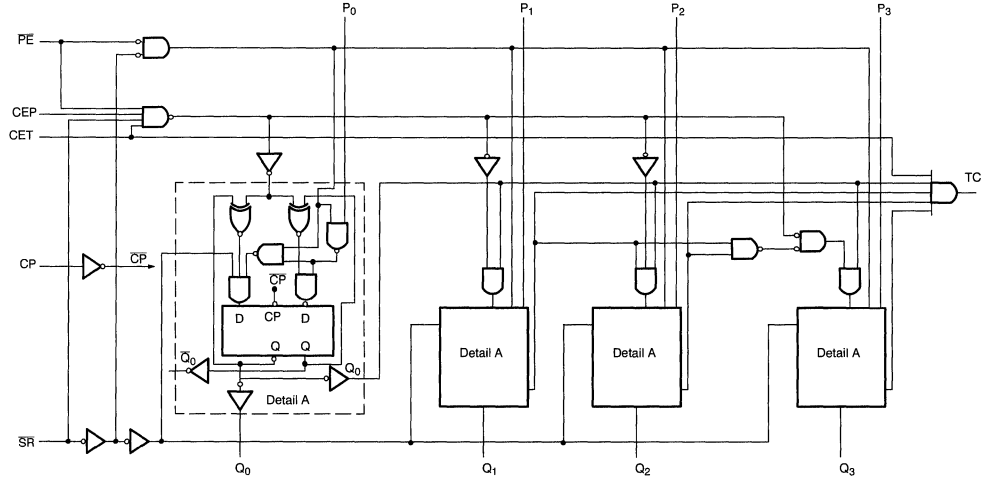
- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.8 ns max. (Com'l) FCT-A speed at 7.2 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current** 64 mA (Com'l), 32 mA (Mil)
- **Source current** 32 mA (Com'l), 12 mA (Mil)

Functional Description

The FCT163T is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The FCT163T has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

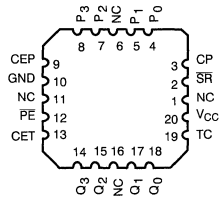
Logic Block Diagram



FCT163T-1

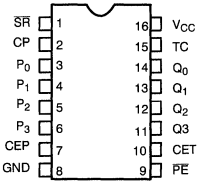
Pin Configurations

LCC
Top View



FCT163T-2

DIP/SOIC/QSOP
Top View



FCT163T-3

Function Table[1]

Inputs				Action on the Rising Clock Edge(s)
$\overline{SR}$	$\overline{PE}$	CET	CEP	
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Incremental)
H	H	L	X	No Charge (Hold)
H	H	X	L	No Charge (Hold)

Pin Description

Name	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SR}$	Synchronous Reset Input (Active LOW)
P	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q	Flip-Flop Outputs
TC	Terminal Count Output

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.2	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, Load Mode, 50% Duty Cycle, Outputs Open, $\overline{CEP}$=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEP}$=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, CEP=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, $\overline{CEP}$=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, CEP=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	2.9	8.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT163T				FCT163AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q ($\overline{PE}$ Input HIGH)	2.0	11.5	1.5	11.0	2.0	7.5	1.5	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC ($\overline{PE}$ Input LOW)	2.0	10.0	1.5	9.5	2.0	6.5	1.5	6.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC	2.0	16.5	1.5	15.0	2.0	10.8	1.5	9.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CET to TC	1.5	9.0	1.5	8.5	1.5	5.9	1.5	5.5	ns	1, 5
t_S	Set-Up Time, HIGH or LOW P to CP	5.5		4.0		4.5		4.0		ns	4
t_H	Hold Time, HIGH or LOW P to CP	2.0		1.5		2.0		1.5		ns	4
t_{SU}	Set-Up Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	13.5		9.5		11.5		9.5		ns	4
t_H	Hold Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5		1.5		1.5		1.5		ns	4
t_{SU}	Set-Up Time HIGH or LOW CEP or CET to CP	13.0		9.5		11.0		9.5		ns	4
t_H	Hold Time HIGH or LOW CEP or CET to CP	0		0		0		0		ns	4
t_W	Clock Pulse Width (Load) HIGH or LOW	5.0		4.0		4.0		4.0		ns	5
t_W	Clock Pulse Width(Count) HIGH or LOW	8.0		6.0		7.0		6.0		ns	5

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	FCT163CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q ($\overline{PE}$ Input HIGH)	1.5	6.1	1.5	5.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC ($\overline{PE}$ Input LOW)	1.5	5.5	1.5	5.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC	1.5	8.7	1.5	7.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CET to TC	1.5	4.8	1.5	4.4	ns	1, 5
t_S	Set-Up Time, HIGH or LOW P to CP	3.9		3.5		ns	4
t_H	Hold Time, HIGH or LOW P to CP	2.0		1.5		ns	4
t_{SU}	Set-Up Time, HIGH or LOW$\overline{PE}$ or $\overline{SR}$ to CP	9.0		7.6		ns	4
t_H	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5		1.0		ns	4
t_{SU}	Set-Up Time, HIGH or LOW CEP or CET to CP	8.8		7.6		ns	4
t_H	Hold Time, HIGH or LOW CEP or CET to CP	0		0		ns	4
t_W	Clock Pulse Width (Load) HIGH or LOW	4.0		4.0		ns	5
t_W	Clock Pulse Width (Count) HIGH or LOW	6.0		5.0		ns	5

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT163CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163CTQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.1	CY54FCT163CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163CTLMB	L61	20-Square Leadless Chip Carrier	
7.2	CY74FCT163ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163ATQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT163ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163ATLMB	L61	20-Square Leadless Chip Carrier	
11.0	CY74FCT163TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163TQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163TSOC	S1	16-Lead (300-Mil) Molded SOIC	
11.5	CY54FCT163TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163TLMB	L61	20-Square Leadless Chip Carrier	

Document #: 38−00285−A

CY54/74FCT191T

4-Bit Up/Down Binary Counter

Features

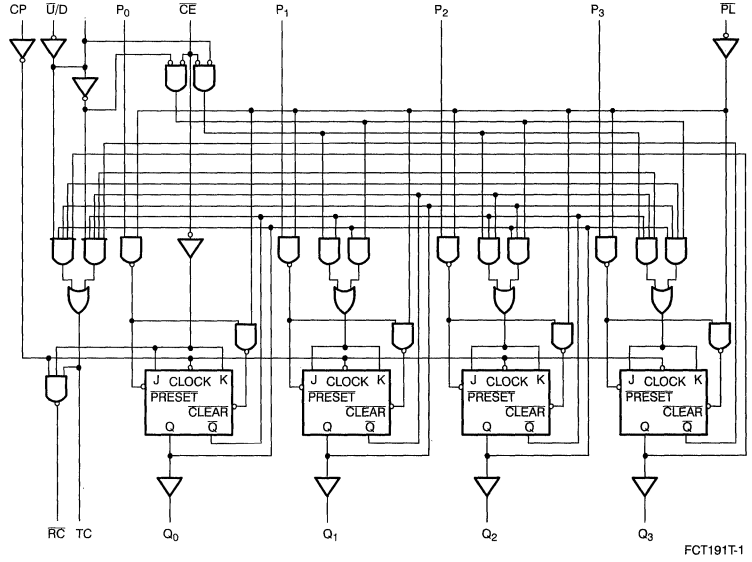
- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 6.2 ns max. (Com'l) FCT-A speed at 7.8 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Three-State outputs**

Functional Description

The FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

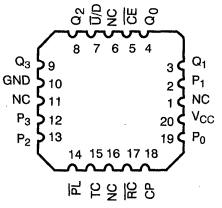
Logic Block Diagram



FCT191T-1

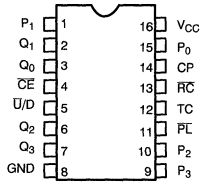
Pin Configurations

LCC
Top View



FCT191T-3

DIP/SOIC/QSOP
Top View



FCT191T-2

Pin Description

Name	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}$/D	Up/Down Count Control Input
Q	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output

$\overline{RC}$ Function Table[1]

Inputs		Outputs	
$\overline{CE}$	CP	T[2]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

Mode Select[1]

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	U/$\overline{D}$	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[5]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[7]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[7]

Parameter	Description	Typ.[6]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ⌐ = LOW-to-HIGH clock transition. ⊓ = Low Pulse.
2. TC is generated internally.
3. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. T_A is the "instant on" case temperature.
6. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
7. This parameter is guaranteed but not tested.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[9] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Bit Toggling, Preset Mode, 50% Duty Cycle, Outputs Open, $\overline{MR}=V_{CC}=\overline{SR}$, $\overline{PL}=\overline{CE}=U/\overline{D}=CP=GND$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{PL}=\overline{CE}=U/\overline{D}=CP=GND$, $V_{IN}=V_{CC}$, V_{IN}=GND	0.4	0.8	mA
		V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, V_{IN}=3.4V or V_{IN}=GND	0.7	1.8	mA
		V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, $\overline{PL}=\overline{CE}=U/\overline{D}=CP=GND$, $V_{IN}=V_{CC}$, V_{IN}=GND	1.3	2.6[12]	mA
		V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, $\overline{PL}=\overline{CE}=U/\overline{D}=CP=GND$, V_{IN}=3.4V or V_{IN}=GND	2.3	6.6[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT191T				FCT191AT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	1.5	16.0	1.5	12.0	1.5	10.5	1.5	7.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	2.0	16.0	1.5	14.0	2.0	12.2	1.5	11.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	1.5	12.5	1.5	8.5	1.5	10.0	1.5	8.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	2.0	8.5	1.5	8.0	2.0	8.0	1.5	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	4.0	22.5	1.5	20.0	4.0	14.7	1.5	13.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{TC}$	3.0	13.0	1.5	11.0	3.0	8.5	1.5	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	1.5	16.0	1.5	14.0	1.5	10.4	1.5	9.1	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.0	14.0	2.0	13.0	3.0	9.1	2.0	8.5	ns	1, 5
t_{SU}	Set-Up Time HIGH or LOW P_n to $\overline{PL}$	6.0		5.0		5.0		4.0		ns	4
t_H	Hold Time HIGH or LOW P_n to $\overline{PL}$	1.5		1.5		1.5		1.5		ns	4
t_{SU}	Set-Up Time LOW $\overline{CE}$ to CP	10.5		10.0		9.5		9.0		ns	4
t_H	Hold Time LOW $\overline{CE}$ to CP	0		0		0		0		ns	4
t_{SU}	Set-Up Time HIGH or LOW $\overline{U}/D$ to CP	12.0		12.0		10.0		10.0		ns	4
t_H	Hold Time HIGH or LOW $\overline{U}/D$ to CP	0		0		0		0		ns	4
t_W	$\overline{PL}$ Pulse Width LOW	8.5		6.0		8.0		5.5		ns	5
t_W	Clock Pulse Width[6] HIGH or LOW	7.0		5.0		6.0		4.0		ns	5
t_{REM}	Recovery Time $\overline{PL}$ to CP	7.5		6.0		6.5		5.0		ns	6

Notes:
13 Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.

9

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	FCT191CT				Unit	Fig. No.[14]
		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	1.5	8.4	1.5	6.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC	1.5	9.8	1.5	9.4	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	1.5	7.9	1.5	6.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	1.5	6.4	1.5	6.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	2.5	11.7	1.5	11.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC	1.5	6.8	1.5	6.1	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	1.5	8.3	1.5	7.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	2.0	7.3	2.0	7.2	ns	1, 5
t_{SU}	Set-Up Time, HIGH or LOW, P_n to $\overline{PL}$	4.0		3.5			4
t_H	Hold Time, HIGH or LOW, P_n to $\overline{PL}$	1.5		1.0		ns	4
t_{SU}	Set-Up Time LOW, $\overline{CE}$ to CP	7.6		7.2		ns	4
t_H	Hold Time LOW, $\overline{CE}$ to CP	0		0		ns	4
t_{SU}	Set-Up Time, HIGH or LOW, $\overline{U}$/D to CP	8.5		8.0		ns	4
t_H	Hold Time, HIGH or LOW, $\overline{U}$/D to CP	0		0		ns	4
t_W	$\overline{PL}$ Pulse Width LOW	6.0		5.0		ns	5
t_W	Clock Pulse Width[6] HIGH or LOW	5.0		4.0		ns	5
t_{REM}	Recovery Time $\overline{PL}$ to CP	5.0		4.5		ns	6

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.2	CY74FCT191CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT191CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT191CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
8.4	CY54FCT191CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT191CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.8	CY74FCT191ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT191ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT191ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
10.5	CY54FCT191ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT191ATLMB	L61	20-Pin Square Leadless Chip Carrier	
12.0	CY74FCT191TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT191TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT191TSOC	S1	16-Lead (300-Mil) Molded SOIC	
16.0	CY54FCT191TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT191TLMB	L61	20-Pin Square Leadless Chip Carrier	

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CY54/74FCT240T
CY54/74FCT244T

8-Bit Buffers/Line Drivers

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.8 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current** 64 mA (Com'l), 48 mA (Mil)
  Source current 32 mA (Com'l), 12 mA (Mil)

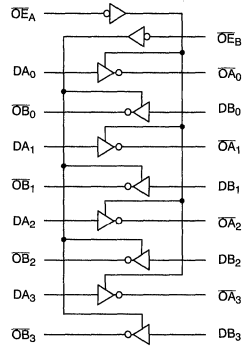
Functional Description

The FCT240T and FCT244T are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

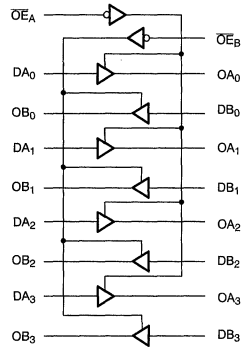
Logic Block Diagram

FCT240T



FCT240T-1

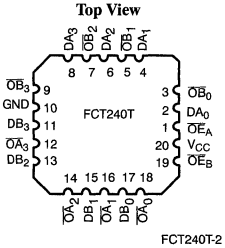
FCT244T



FCT240T-4

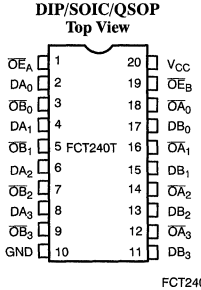
Pin Configurations

LCC
Top View



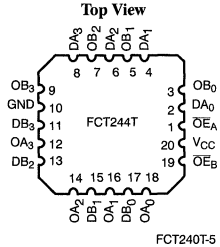
FCT240T-2

DIP/SOIC/QSOP
Top View



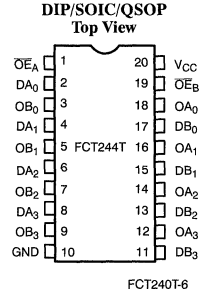
FCT240T-3

LCC
Top View



FCT240T-5

DIP/SOIC/QSOP
Top View



FCT240T-6

Function Table FCT240T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT244T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Speed	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1=\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT240T				FCT240AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT240CT				FCT240DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	4.7	1.5	4.3	1.5	3.6	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.7	1.5	5.0	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	4.6	1.5	4.5	1.5	4.0	ns	1, 7, 8

Parameter	Description	FCT244T				FCT244AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	7.0	1.5	6.5	1.5	5.1	1.5	4.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.5	1.5	8.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT244CT				FCT244DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	4.6	1.5	4.1	1.5	3.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	1.5	4.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information—FCT240T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT240DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT240DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.3	CY74FCT240CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240CTQC	Q5	20-Lead (150-Mil) QSOP	
4.7	CY54FCT240CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT240CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT240ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240ATQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT240ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT240ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT240TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240TSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240TQC	Q5	20-Lead (150-Mil) QSOP	
9.0	CY54FCT240TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT240TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT244T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT244DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT244DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT244CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244CTQC	Q5	20-Lead (150-Mil) QSOP	
4.6	CY54FCT244CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.6	CY74FCT244ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244ATQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT244ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT244TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244TSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244TQC	Q5	20-Lead (150-Mil) QSOP	
7.0	CY54FCT244TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38–00259–A

CY54/74FCT245T

8-Bit Transceiver

Features

- **Function, pinout, and drive compatible with FCT, F logic**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.6 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current** **64 mA (Com'l), 48 mA (Mil)**
  Source current **32 mA (Com'l), 12 mA (Mil)**

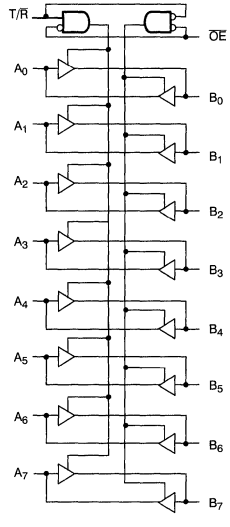
Functional Description

The FCT245T contains eight non-inverting bidirectional buffers with three-state outputs and is intended for bus oriented applications. For the FCT245T, current sinking capability is 64 mA at the A and B ports.

The Transmit/Receiver ($T/\overline{R}$) input determines the direction of data flow through bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports. The output enable ($\overline{OE}$), when HIGH, disables both the A and B ports by putting them in a High Z condition.

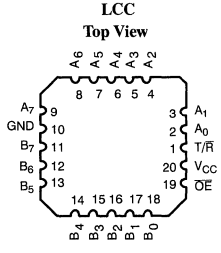
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

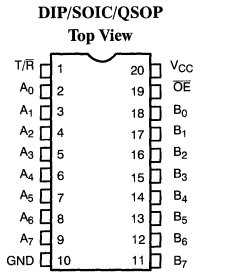


FCT245T-1

Pin Configurations



FCT245T-2



FCT245T-3

Function Table[1]

$\overline{OE}$	$T/\overline{R}$	Operation
L	L	B Data to Bus A
L	H	A Data to Bus B
H	X	High Z State

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	μA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	μA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	μA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	μA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, T/$\overline{R}$ or $\overline{OE}$=GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, T/$\overline{R}$ or $\overline{OE}$=GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, T/$\overline{R}$ or $\overline{OE}$=GND and V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, T/$\overline{R}$ or $\overline{OE}$=GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, T/$\overline{R}$ or $\overline{OE}$=GND and V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT245T				FCT245AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	1.5	7.5	1.5	7.0	1.5	4.9	1.5	4.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	10.0	1.5	9.5	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	ns	1, 7, 8

Switching Characteristics Over the Operating Range

Parameter	Description	FCT245CT				FCT245DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	1.5	4.5	1.5	4.1	1.5	3.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	6.2	1.5	5.8	1.5	5.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	5.2	1.5	4.8	1.5	4.3	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT245DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT245DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT245CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT245CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT245CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.5	CY54FCT245CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT245CTLMB	L61	20-Square Leadless Chip Carrier	
4.6	CY74FCT245ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT245ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT245ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.9	CY54FCT245ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT245ATLMB	L61	20-Square Leadless Chip Carrier	
7.0	CY74FCT245TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT245TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT245TSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT245TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT245TLMB	L61	20-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38−00318−A

CY54/74FCT257T

Quad 2-Input Multiplexer

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 4.3 ns max. (Com'l) FCT-A speed at 5.0 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

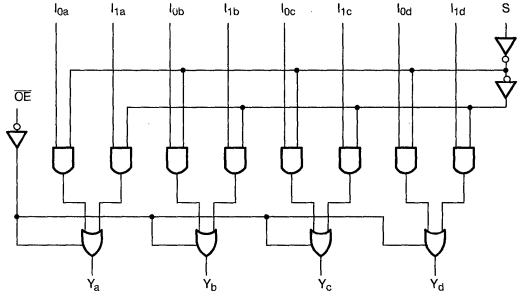
The FCT257T has four identical two-input multiplexers which select four bits of data from two sources under the control of a common data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT257T.

The FCT257T is a logic implementation of a four-pole, two position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedence "OFF" state when the Output Enable input ($\overline{OE}$) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

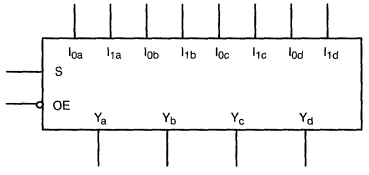
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



FCT257T-1

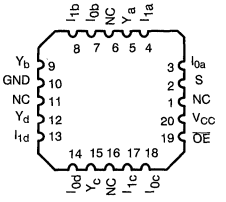
Logic Symbol



FCT257T-4

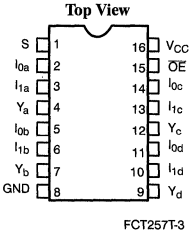
Pin Configurations

LCC
Top View



FCT257T-2

DIP/SOIC/QSOP
Top View



FCT257T-3

Pin Description

Name	Description
I	Data Inputs
S	Common Select Input
$\overline{OE}$	Enable Inputs (Active LOW)
Y	Data Outputs

Function Table[1]

Inputs				Output
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Note:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High impedence (OFF) state

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Inputt Toggling at f_1=10 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Input Toggling at f_1=10 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.7	5.4[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT257T				FCT257AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to $\overline{Y}$	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay S to O	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.0	1.5	8.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	6.0	1.5	5.8	1.5	5.5	ns	1, 7, 8

Parameter	Description	FCT257CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to $\overline{Y}$	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay S to O_n	1.5	6.0	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.8	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.3	1.5	5.0	ns	1, 7, 8

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

9

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT257CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT257CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.0	CY74FCT257ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY54FCT257ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.0	CY74FCT257TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT257TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT257TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT257TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT257TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38–00289–A

CY54/74FCT273T

8-Bit Register

Features

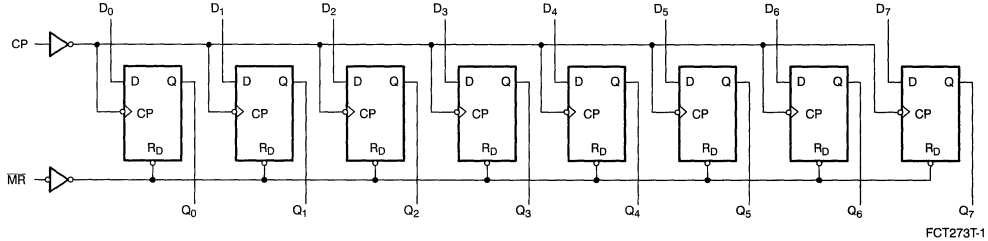
- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.8 ns max. (Com'l) FCT-A speed at 7.2 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Buffered common clock**
- **Buffered, asynchronous master reset**
- **Edge-triggered D flip-flops**
- **CMOS for low-power consumption, typically one-third of FAST Bipolar Logic**

Functional Description

The FCT273T consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset (MR) load and reset all flip-flops simultaneously. The FCT273T is an edge-triggered register. The state of each D input (one set-up time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flop's Q output. All outputs will be forced LOW by a low voltage level on the $\overline{MR}$ input.

The outputs are designed with a power-off disable eature to allow for live insertion of boards.

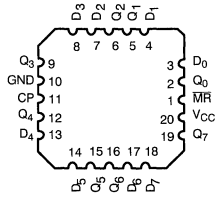
Logic Block Diagram



FCT273T-1

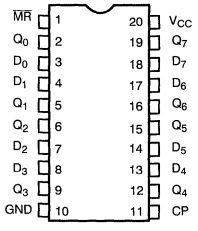
Pin Configurations

LCC
Top View



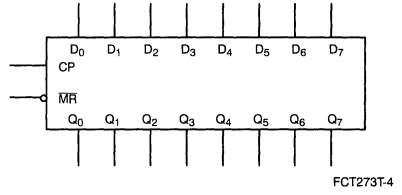
FCT273T-2

DIP/SOIC/QSOP
Top View



FCT273T-3

Logic Symbol



FCT273T-4

Function Table[1]

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D	Q
Reset (clear)	L	X	X	L
Load '1'	H	⌐	h	H
Load '0'	H	⌐	l	L

Note:
1. H = HIGH Voltage Level steady state
   h = HIGH Voltage Level one set-up time prior to LOW-to-HIGH clock transition
   L = LOW Voltage Level steady state
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH transition
   X = Don't Care
   ⌐ = LOW-to-HIGH clock transition

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{MR}=V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{MR}=V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{MR}=V_{CC}$, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{MR}=V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{MR}=V_{CC}$, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_i N_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT273T				FCT273AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 6
t_S	Set-Up Time HIGH or LOW D to Clock	3.5		2.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW D to Clock	2.0		1.5		1.5		1.5		ns	4
t_W	Clock Pulse Width HIGH or LOW	7.0		6.0		6.0		6.0		ns	5
t_W	$\overline{MR}$ Pulse Width LOW	7.0		6.0		6.0		6.0		ns	6
t_{REC}	Recovery Time $\overline{MR}$ to Clock	5.0		2.0		2.5		2.0		ns	6

Parameter	Description	FCT273CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	6.5	2.0	5.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	2.0	6.8	2.0	6.1	ns	1, 6
t_S	Set-Up Time HIGH or LOW D to Clock	2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW D to Clock	1.5		1.5		ns	4
t_W	Clock Pulse Width HIGH or LOW	6.0		6.0		ns	5
t_W	$\overline{MR}$ Pulse Width LOW	6.0		6.0		ns	6
t_{REC}	Recovery Time $\overline{MR}$ to Clock	2.5		2.0		ns	6

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT273CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT273CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT273CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.5	CY54FCT273CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT273CTLMB	L61	20-Square Leadless Chip Carrier	
7.2	CY74FCT273ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT273ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT273ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.3	CY54FCT273ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT273ATLMB	L61	20-Square Leadless Chip Carrier	
13.0	CY74FCT273TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT273TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT273TSOC	S5	20-Lead (300-Mil) Molded SOIC	
15.0	CY54FCT273TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT273TLMB	L61	20-Square Leadless Chip Carrier	

Document #: 38−00380

CY54/74FCT373T
CY54/74FCT573T

8-Bit Latches

Features

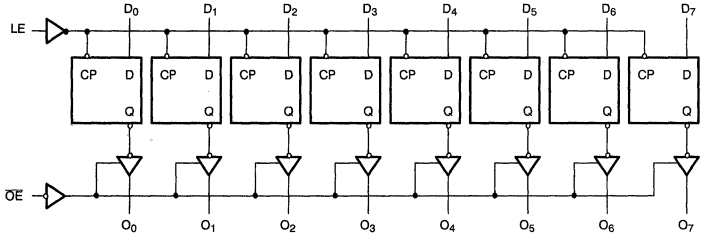
- **Function, pinout and drive compatible with the fastest bipolar logic**
- **FCT-C speed at 4.2 ns max. (Com'l) FCT-A speed at 5.2 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink Current** 64 mA (Com'l), 32 mA (Mil)
  Source Current 32 mA (Com'l), 12 mA (Mil)

Functional Description

The FCT373T and FCT573T consist of eight latches with three-state outputs for bus organized system applications. When latch enable (LE) is HIGH, the flip-flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable ($\overline{OE}$) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data may be entered into the latches. The FCT573T is identical to FCT373T except for flow-through pinout, which simplifies board design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

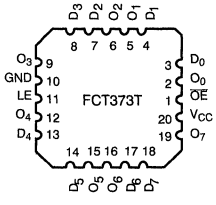
Logic Block Diagram



FCT373T-1

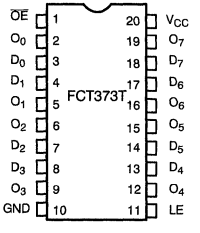
Pin Configurations

LCC
Top View



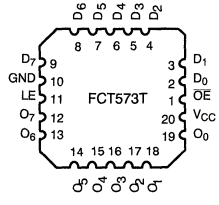
FCT373T-5

DIP/SOIC/QSOP
Top View



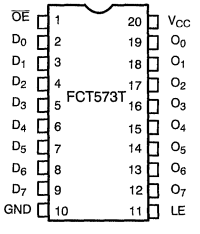
FCT373T-6

LCC
Top View



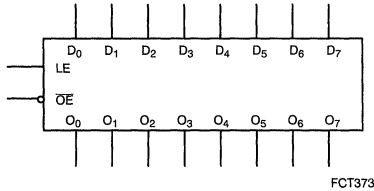
FCT373T-7

DIP/SOIC/QSOP
Top View



FCT373T-8

Logic Symbol



FCT373T-9

Function Table[1]

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T,AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   Q_n = Previous state of flip flops (Q_{n-1})
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	6	10	pF
C_{OUT}	Output Capacitance	8	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.6	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, LE=V_{CC} $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, LE=V_{CC} V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, LE=V_{CC} $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, LE=V_{CC} V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT373T/FCT573T				FCT373AT/FCT573AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	15.0	2.0	13.0	2.0	9.8	2.0	8.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	13.5	1.5	12.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	7.5	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_S	Set-Up Time HIGH to LOW D to LE	2.0		2.0		2.0		2.0		ns	9
t_H	Set-Up Time HIGH to LOW D to LE	1.5		1.5		1.5		1.5		ns	9
t_W	LE Pulse Width HIGH	6.0		6.0		6.0		5.0		ns	5

Parameter	Description	FCT373CT/FCT573CT				FCT373DT/ FCT573DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	5.1	1.5	4.2	1.5	3.8	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	8.0	2.0	5.5	2.0	4.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.3	1.5	5.5	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.9	1.5	5.0	1.5	4.0	ns	1, 7, 8
t_S	Set-Up Time, HIGH to LOW D to LE	2.0		2.0		1.5		ns	9
t_H	Set-Up Time, HIGH to LOW D to LE	1.5		1.5		1.0		ns	9
t_W	LE Pulse Width HIGH	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information—FCT373T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT373DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT373DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT373CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT373CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT373CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT373ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT373ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT373ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT373TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT373TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT373TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT573T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT573DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT573DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT573CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573CTQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT573CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT573CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT573ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT573ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT573ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT573ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT573TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT573TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT573TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT573TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38–00272–A

CY54/74FCT374T
CY54/74FCT574T

8-Bit Registers

Features

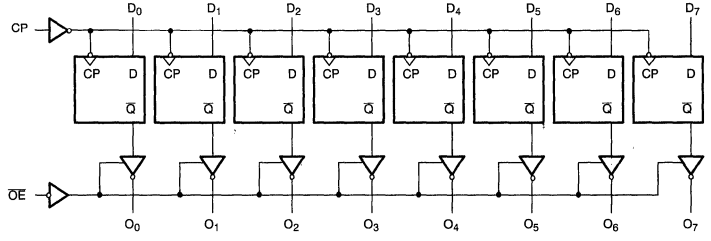
- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.2 ns max. (Com'l) FCT-A speed at 6.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink Current 64 mA (Com'l), 32 mA (Mil)**
  Source Current 32 mA (Com'l), 12 mA (Mil)
- **Edge-triggered D-type inputs**
- **250 MHz typical toggle rate**

Functional Description

The FCT374T and FCT574T are high-speed low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have three-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The FCT574T is identical to FCT374T except for flow-through pinout to simplify board design. The eight flip-flops contained in the FCT374T and FCT574T will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high-impedence state. The state of output enable does not affect the state of the flip-flops.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

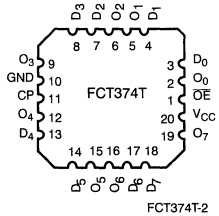
Logic Block Diagram



FCT374T-1

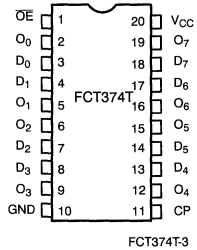
Pin Configurations

LCC
Top View



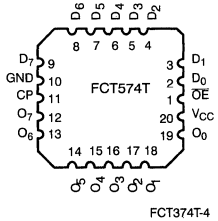
FCT374T-2

DIP/SOIC/QSOP
Top View



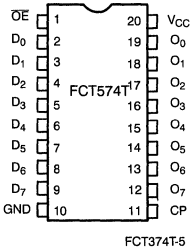
FCT374T-3

LCC
Top View



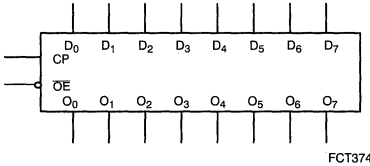
FCT374T-4

DIP/SOIC/QSOP
Top View



FCT374T-5

Logic Symbol



FCT374T-6

Function Table[1]

Inputs			Outputs
D	CP	$\overline{OE}$	O
H	⎍	L	H
L	⎍	L	L
X	X	H	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   ⎍ = LOW-to-HIGH clock transition
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	FCT374T/FCT574T				FCT374AT/FCT574AT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t_W	Clock Pulse Width[15] HIGH or LOW	7.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT374CT/FCT574CT				FCT374DT/ FCT574DT		Unit	Fig. No.[14]
		Military		Commercial		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	6.2	2.0	5.2	2.0	4.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.2	1.5	5.5	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.7	1.5	5.0	1.5	4.0	ns	1, 7, 8
t_S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		ns	4
t_H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		ns	4
t_W	Clock Pulse Width[15] HIGH or LOW	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. AC Characteristics guaranteed with C_L=50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information Section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. With one data channel toggling, $t_W(L)=t_W(H)$=4.0 ns and $t_r=t_f$=1.0 ns.

Ordering Information—FCT374T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT374DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT374CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT374CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT374ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT374ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT374TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT374TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT574T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT574DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT574CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT574CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT574CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT574ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT574ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT574ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT574TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT574TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT574TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38–00278–A

CY54/74FCT377T

8-Bit Register

Features

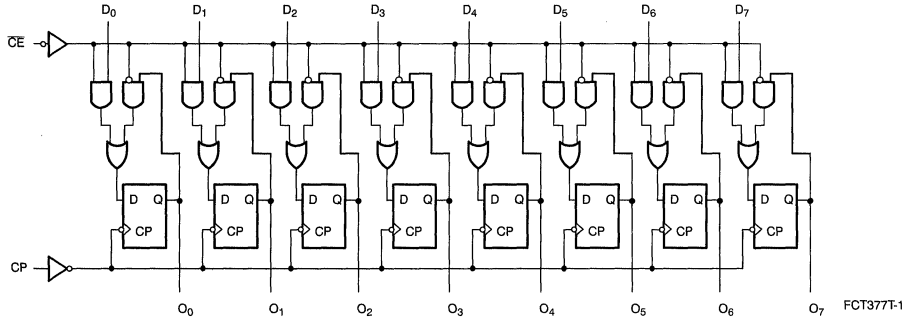
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 5.2 ns max. (Com'l) FCT-A speed at 7.2 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Clock Enable for address and data synchronization application**
- **Eight edge-triggered D flip-flops**

Functional Description

The FCT377T has eight triggered D-type flip-flops with individual D inputs. The common buffered clock inputs (CP) loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

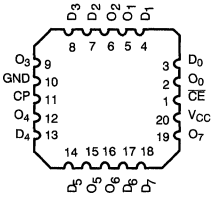
Logic Block Diagram



FCT377T-1

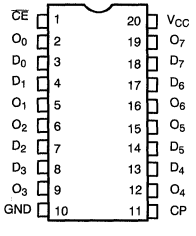
Pin Configurations

LCC
Top View



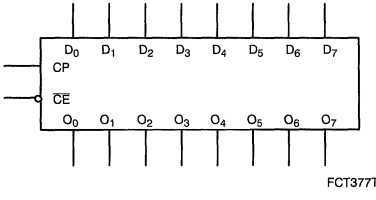
FCT377T-2

DIP/SOIC/QSOP
Top View



FCT377T-3

Logic Symbol



FCT377T-4

Function Table[1]

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	⌐	l	h	H
Load "0"	⌐	l	l	L
Hold	⌐	h	X	No Change
	X	H	X	No Change

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V., V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one set-up fime prior to the LOW-to-HIGH Clock Transition
   X = Don't Care
   Z = HIGH Impedance
   ⌐ = LOW-to-HIGH clock transition
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{CE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{CE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{CE}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	FCT377T				FCT377AT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 5
t_S	Set-Up Time HIGH or LOW Data to CP	3.0		2.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW Data to CP	2.5		1.5		1.5		1.5		ns	4
t_W	Set-Up Time HIGH or LOW $\overline{CE}$ to CP	4.0		3.5		3.5		3.5		ns	4
t_W	Set-Up Time HIGH or LOW $\overline{CE}$ to CP	1.5		1.5		1.5		1.5		ns	4
t_W	Clock Pulse Width[15] HIGH or LOW	7.0		6.0		7.0		6.0		ns	6

Parameter	Description	FCT377CT				Unit	Fig. No.[14]
		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	5.5	2.0	5.2	ns	1, 5
t_S	Set-Up Time, HIGH or LOW, Data to CP	2.0		2.0		ns	4
t_H	Hold Time, HIGH or LOW, Data to CP	1.5		1.5		ns	4
t_W	Set-Up Time, HIGH or LOW, $\overline{CE}$ to CP	3.5		3.5		ns	4
t_W	Set-Up Time HIGH or LOW, $\overline{CE}$ to CP	1.5		1.5		ns	4
t_W	Clock Pulse Width[15] HIGH or LOW	7.0		6.0		ns	6

Notes:

12. AC Characteristics guaranteed with C_L=50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information Section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. With one data channel toggling, $t_W(L)=t_W(H)=4.0$ ns and $t_r=t_f=1.0$ ns.

9

Ordering Information—FCT377T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT377CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT377CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT377CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.5	CY54FCT377CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT377CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.2	CY74FCT377ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT377ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT377ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.3	CY54FCT377ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT377ATLMB	L61	20-Pin Square Leadless Chip Carrier	
13.0	CY74FCT377TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT377TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT377TSOC	S5	20-Lead (300-Mil) Molded SOIC	
15.0	CY54FCT377TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT377TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38−00279−A

CY54/74FCT399T

Quad 2-Input Register

Features

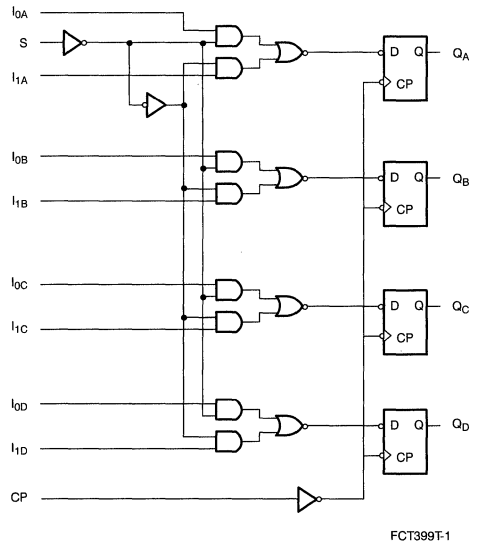
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 6.1 ns max. (Com'l) FCT-A speed at 7.0 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

The FCT399T is a high-speed quad dual-port register that selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation. The FCT399T offers true outputs.

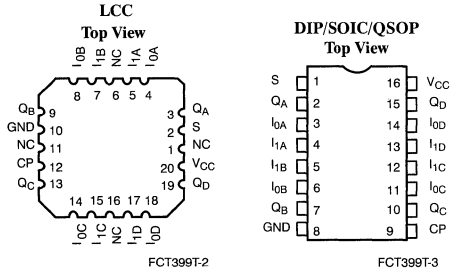
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



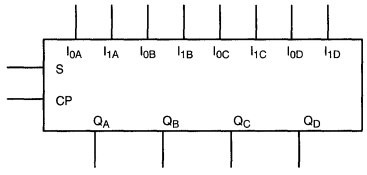
FCT399T-1

Pin Configurations



FCT399T-2 FCT399T-3

Logic Symbol



FCT399T-4

Pin Description

Name	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
I_0	Data Inputs from Source 0
I_1	Data Inputs from Source 1
Q	Register True Outputs

Function Table[1]

Inputs			Outputs
S	**I_0**	**I_1**	**Q**
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

Note:

1. H = HIGH Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH Clock Transition
   X = Don't Care

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques is preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1=5 MHz, S=Steady State $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1=5 MHz, S=Steady State V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Four Inputs Toggling at f_1=5 MHz, S=Steady State $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Four Inputs Toggling at f_1=5 MHz, S=Steady State V_{IN}=3.4V or V_{IN}=GND	2.9	8.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT399T				FCT399AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q	3.0	11.5	3.0	10.0	2.5	7.5	2.5	7.0	ns	1, 5
t_S	Set-Up Time HIGH or LOW I_n to CP	4.5		3.5		4.0		3.5		ns	4
t_H	Hold Time HIGH or LOW I_n to CP	1.5		1.0		1.0		1.0		ns	4
t_S	Set-Up Time HIGH or LOW S to CP	9.5		8.5		9.0		8.5		ns	4
t_H	Hold Time HIGH or LOW S to CP	0		0		0		0		ns	4
t_W	Clock Pulse Width[6] HIGH or LOW	7.0		5.0		6.0		5.0		ns	5

Parameter	Description	FCT399CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q	2.5	6.6	2.5	6.1	ns	1, 5
t_S	Set-Up Time, HIGH or LOW, I_n to CP	4.0		3.5		ns	4
t_H	Hold Time, HIGH or LOW, I_n to CP	1.0		1.0		ns	4
t_S	Set-Up Time, HIGH or LOW, S to CP	9.0		8.5		ns	4
t_H	Hold Time, HIGH or LOW, S to CP	0		0		ns	4
t_W	Clock Pulse Width[6] HIGH or LOW	6.0		5.0		ns	5

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.1	CY74FCT399CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT399CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT399CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.6	CY54FCT399CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT399CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.0	CY74FCT399ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT399ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT399ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT399ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT399ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT399TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT399TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT399TSOC	S1	16-Lead (300-Mil) Molded SOIC	
11.5	CY54FCT399TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT399TLMB	L61	20-Pin Square Leadless Chip Carrier	

Document #: 38−00280−A

CY54/74FCT480T

Dual 8-Bit Parity Generator/Checker

Features

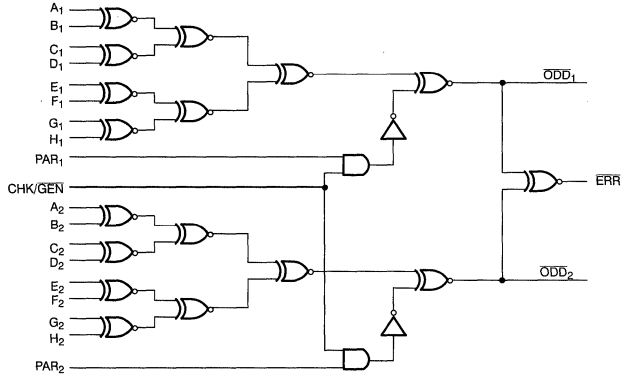
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-A speed at 7.5 ns max. (Com'l) FCT-B speed at 5.6 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink Current 64 mA (Com'l), 32 mA (Mil)**
  Source Current 32 mA (Com'l), 12 mA (Mil)
- **Two 8-bit parity generator/checkers**
- **Open drain Active LOW parity error output**
- **Expandable for larger word widths**

Functional Description

The FCT480T is a high-speed dual 8-bit parity generator/checker. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a sum and parity error output. The FCT480T can be used in ODD parity systems. The parity error output is open-drain, designed for easy expansion of the word width by a wired-OR connection of several FCT480T type devices. Since additional logic is not needed, the parity generation or checking times remain the same as for an individual FCT480T device.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

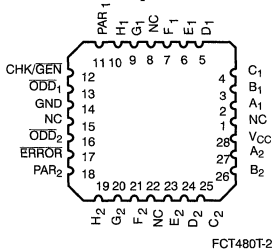
Logic Block Diagram



FCT480T-1

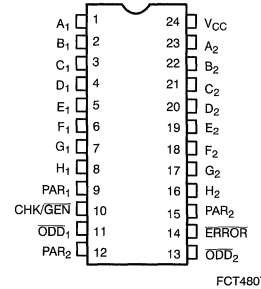
Pin Configurations

LCC
Top View



FCT480T-2

DIP/SOIC/QSOP
Top View



FCT480T-3

Function Table

Inputs					Outputs		
A_1 to H_1	A_2 to H_2	CHK/$\overline{GEN}$	PAR_1	PAR_2	$\overline{ODD}_1$	$\overline{ODD}_2$	$\overline{ERROR}$
Number of A_1 to H_1 Inputs HIGH is EVEN	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L
	Number of Inputs HIGH A_2 to H_2 is ODD	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
Number of A_1 to H_1 Inputs HIGH is ODD	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
	Number of A_2 to H_2 Inputs HIGH is ODD	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H

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Maximum Ratings[1, 2]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	BT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[3]	All	−55°C to +125°C	5V ± 10%

Notes:

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[5]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[5]

Parameter	Description	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[7] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=2.5 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=2.5 MHz, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling at f_1=2.5 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.5	5.0[10]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling at f_1=2.5 MHz, V_{IN}=3.4V or V_{IN}=GND	6.5	21.0[10]	mA

Switching Characteristics Over the Operating Range

	Description	FCT480T		FCT480AT		FCT480BT		Unit
		Military	Com'l	Military	Com'l	Military	Com'l	
t_{PLH} t_{PHL}	Propagation Delay A to EVEN/ODD	17.0 16.0	13.0 13.0	9.5 9.0	7.5 7.0	7.0 6.6	5.6 5.6	ns
t_{PLH}[11] t_{PHL}	Propagation Delay A to $\overline{ERROR}$	17.0 20.0	13.0 16.0	9.0 10.5	7.0 8.5	7.0 8.1	5.6 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay CHK/$\overline{GEN}$ to EVEN/ODD	15.0 18.0	12.0 15.0	8.5 10.0	6.5 7.5	6.3 7.4	5.9 5.9	ns
t_{PLH}[11] t_{PHL}	Propagation Delay CHK/$\overline{GEN}$ to $\overline{ERROR}$	17.0 16.0	14.0 13.0	9.5 9.0	7.5 7.0	7.1 6.9	5.7 5.5	ns

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_i = Input signal frequency
   N_i = Number of inputs changing at f_i
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. t_{PLH} is measured up to $V_{OUT}=V_{OL}+0.3V$

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.6	CY74FCT480BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT480BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480BTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT480ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
9.5	CY54FCT480ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480ATLMB	L64	28-Square Leadless Chip Carrier	
13.0	CY74FCT480TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480TSOC	S13	24-Lead (300-Mil) Molded SOIC	
17.0	CY54FCT480TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT480TLMB	L64	28-Square Leadless Chip Carrier	

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CY54/74FCT540T
CY54/74FCT541T

8-Bit Buffers/Line Drivers

Features

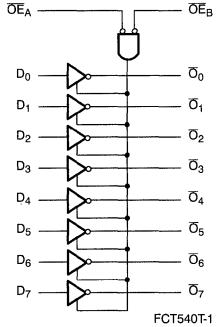
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.8 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 48 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Three-state outputs**

Functional Description

The FCT540T inverting buffer/line driver and the FCT541T non-inverting buffer/line driver are designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

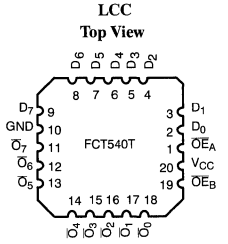
Logic Block Diagram—FCT540T



FCT540T-1

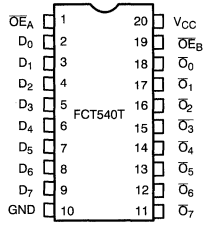
Pin Configurations

LCC
Top View



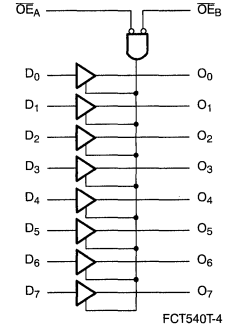
FCT540T-4

DIP/SOIC/QSOP
Top View



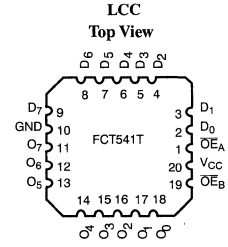
FCT540T-5

Logic Block Diagram—FCT541T



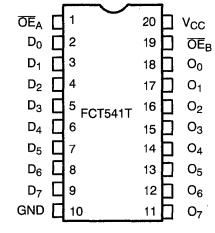
FCT540T-4

LCC
Top View



FCT540T-2

DIP/SOIC/QSOP
Top View



FCT540T-3

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Function Table FCT540T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT541T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}= Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max,. V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedence
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parametric tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Test Conditions	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT540T/FCT541T				FCT540AT/FCT541AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT540)	1.5	9.5	1.5	8.5	1.5	5.1	1.5	4.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT541)	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT540CT/FCT541CT				FCT540DT/ FCT541DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT540)	1.5	4.7	1.5	4.1	1.5	3.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT541)	1.5	4.6	1.5	4.1	1.5	3.3	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	1.5	5.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	1.5	5.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Ordering Information—FCT540T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT540DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT540DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT540CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.7	CY54FCT540CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT540ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT540ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.5	CY74FCT540TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.5	CY54FCT540TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT541T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT541DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT541DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT541CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY54FCT541CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT541ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT541ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT541TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT541TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00260-A

CY54/74FCT543T

8-Bit Latched Registered Transceiver

Features

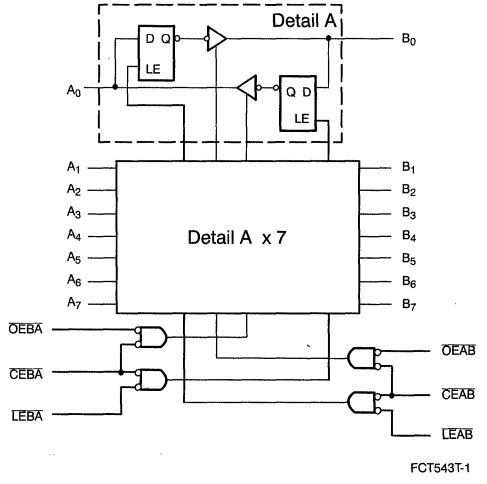
- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.3 ns max. (Com'l) FCT-A speed at 6.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 48 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Separation controls for data flow in each direction**
- **Back to back latches for storage**

Functional Description

The FCT543T octal latched transceiver contains two sets of eight D-type latches with separate latch enable ($\overline{LEAB}$, $\overline{LEBA}$) and output enable ($\overline{OEAB}$, $\overline{OEBA}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B enable ($\overline{CEAB}$) input must be LOW in order to enter data from A or to take data from B, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-stage B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs.

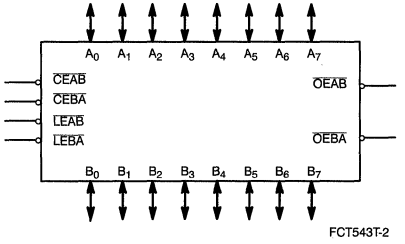
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Functional Block Diagram



FCT543T-1

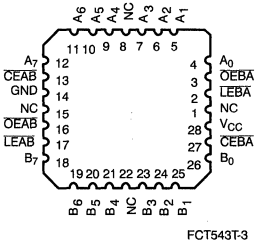
Logic Block Diagram



FCT543T-2

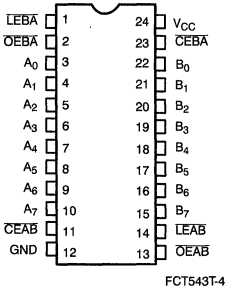
Pin Configurations

LCC
Top View



FCT543T-3

DIP/SOIC/QSOP
Top View



FCT543T-4

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1, 2]

Inputs			Latch	Outputs
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B[3]	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs

Maximum Ratings[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[6]	All	−55°C to +125°C	5V ± 10%

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
3. Before $\overline{LEAB}$ LOW-to-HIGH Transition.
4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
6. T_A is the "instant on" case temperature.

9

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[8]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[8]

Parameter	Description	Typ.[7]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:
7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[10] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ = 10 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ = 10 MHz, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ = 10 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[13]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ = 10 MHz, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT543T				FCT543AT				Unit	Fig. No.[15]
		Military		Commercial		Military		Commercial			
		Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A $\overline{LEAB}$ to B	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	3.0		2.0		2.0		2.0		ns	9
t_H	Hold Time HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	2.0		2.0		2.0		2.0		ns	9
t_W	Pulse Width LOW[6] $\overline{LEBA}$ or $\overline{LEAB}$	5.0		5.0		5.0		5.0		ns	5

Parameter	Description	FCT543CT				FCT543DT		Unit	Fig. No.[15]
		Military		Commercial		Commercial			
		Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.5	6.1	2.5	5.3	1.5	4.4	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	2.5	8.0	2.5	7.0	1.5	5.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	9.0	2.0	8.0	1.5	5.4	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	7.5	2.0	6.5	1.5	4.3	ns	1, 7, 8
t_S	Set-Up Time, HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	2.0		2.0		1.5		ns	9
t_H	Hold Time, HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	2.0		2.0		1.5		ns	9
t_W	Pulse Width LOW $\overline{LEBA}$ or $\overline{LEAB}$[6]	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT543DTSOC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT543DTQC	Q13	24-Lead (150-Mil) QSOP	
5.3	CY74FCT543CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT543CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT543CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.1	CY54FCT543CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT543CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY74FCT543ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT543ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT543ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT543ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT543ATLMB	L64	28-Square Leadless Chip Carrier	
8.5	CY74FCT543TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT543TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT543TSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY54FCT543TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT543TLMB	L64	28-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38−00264−A

CY54/74FCT646T
CY54/74FCT648T

8-Bit Registered Transceivers

Features

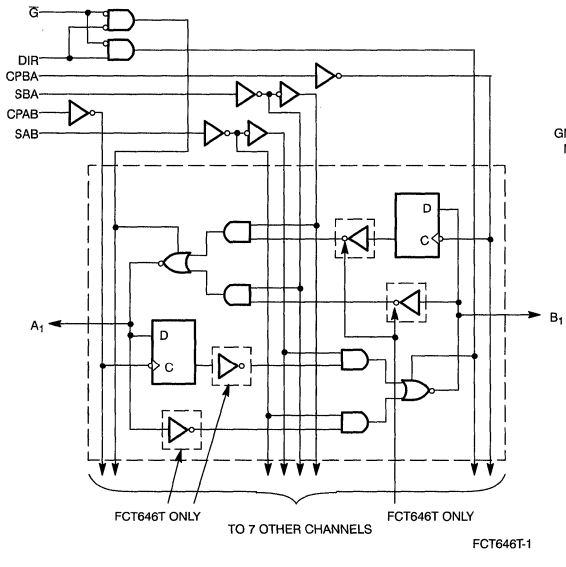
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 5.4 ns max. (Com'l) FCT-A speed at 6.3 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 48 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Independent register for A and B buses**
- **Three-state output**

Functional Description

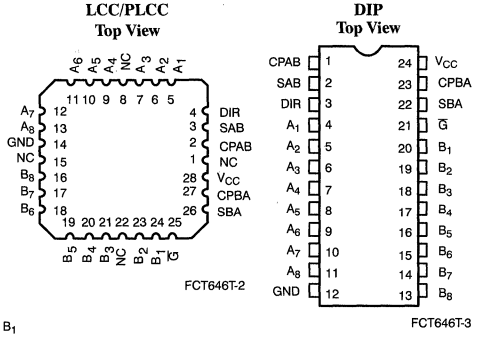
The FCT646T and FCT648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

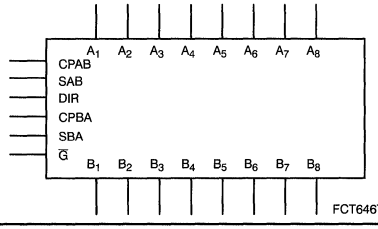
Function Block Diagrams



Pin Configurations

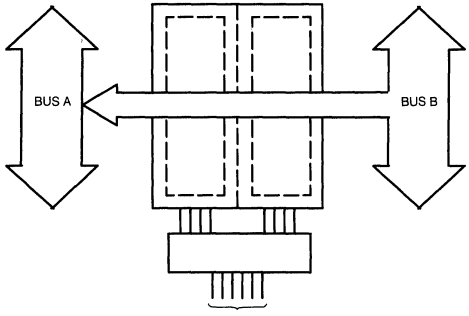


Logic Block Diagram



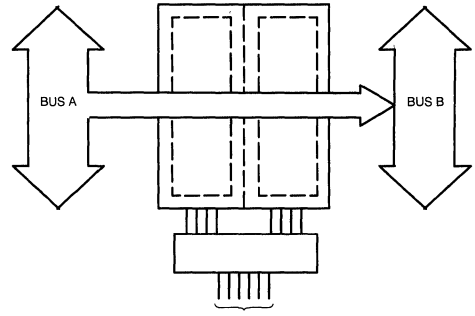
Pin Description

Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs



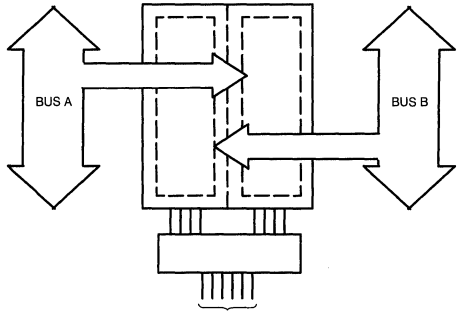
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



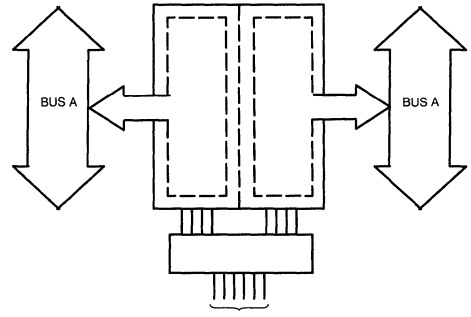
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	⌐	X	X	X
L	L	X	⌐	X	X
X	H	⌐	⌐	X	X

Storage from
A and/or B



DIR[1]	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data
to A and/or B

9

Function Table[2]

Inputs						Data I/O[3]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	FCT646T	FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	⌐	⌐	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

Notes:
1. Cannot transfer data to A bus and B bus simultaneously.
2. H = HIGH Voltage Level, L = LOW Voltage Level, ⌐ = LOW-to-HIGH Transition, X = Don't Care.
3. The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

Maximum Ratings[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[6]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[8]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[8]

Parameter	Description	Typ.[7]	Max.	Unit
C_{IN}	Input Capacitance	6	10	pF
C_{OUT}	Output Capacitance	8	12	pF

Notes:

4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
6. T_A is the "instant on" case temperature.
7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[10] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[13]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range

Parameter	Description	FCT646T/FCT648T				FCT646AT/FCT648AT				Unit	Fig. No.[15]
		Military		Commercial		Military		Commercial			
		Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A_n or B_n	2.0	15.0	1.5	14.0	2.0	10.5	1.5	9.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR toBus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	2.0	7.0	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	2.0	8.4	1.5	7.7	ns	1, 5
t_S	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t_W	Pulse Width,[6] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT646CT/FCT648CT				Unit	Fig. No.[15]
		Military		Commercial			
		Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A_n or B_n	1.5	8.9	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR toBus	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
t_S	Set-Up Time, HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
t_H	Hold Time, HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
t_W	Pulse Width,[6] HIGH or LOW	5.0		5.0		ns	5

Notes:
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.

Ordering Information – FCT646T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT646CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT646CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT646CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT646CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT646CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT646ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT646ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT646ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT646ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT646ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT646TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT646TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT646TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT646TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT646TLMB	L64	28-Square Leadless Chip Carrier	

Ordering Information—FCT648T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT648CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT648CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT648CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT648CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT648CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT648ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT648ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT648ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT648ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT648ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT648TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT648TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT648TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT648TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT648TLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38–00267–A

CY54/74FCT652T

8-Bit Registered Transceiver

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.4 ns max. (Com'l) FCT-A speed at 6.3 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 48 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **ESD > 2000V**
- **Independent register for A and B buses**
- **Multiplexed real-time and stored data transfer**

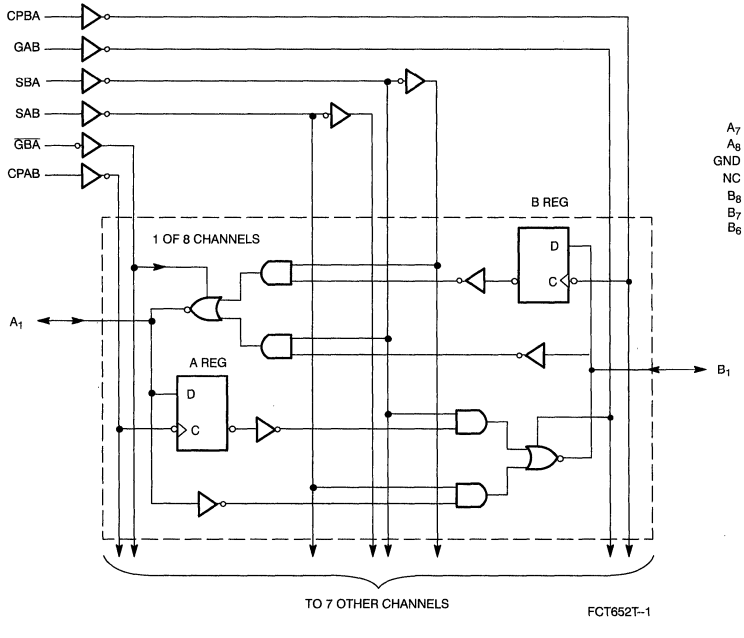
Functional Description

The FCT652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

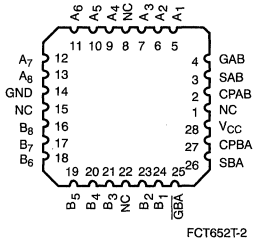
Logic Block Diagram



FCT652T-1

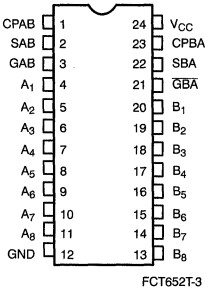
Pin Configurations

LCC
Top View

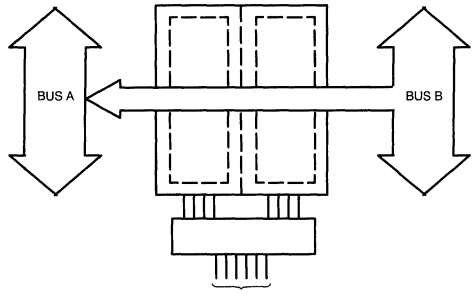


FCT652T-2

DIP/SOIC/QSOP
Top View

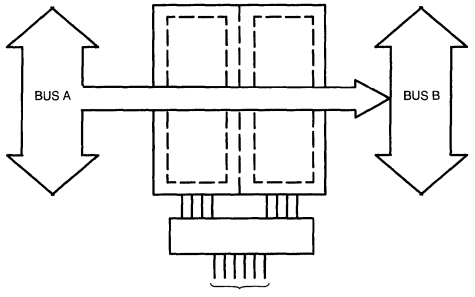


FCT652T-3



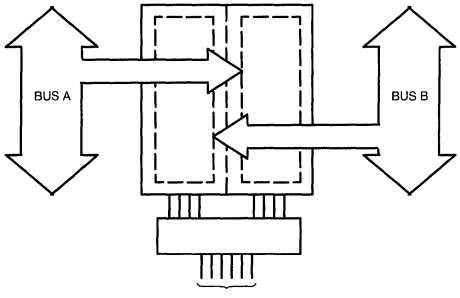
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



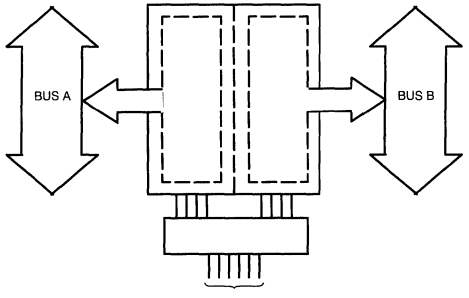
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Real-Time Transfer
Bus A to Bus B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
X	H	↓	X	X	X
L	X	X	↓	X	X
L	H	↓	↓	X	X

Store Data from A and/or B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Transferred Stored Data
to A and/or B

Function Table[1]

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	
L L	H H	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X[1]	X X	Input Input	Unspecified[2] Output	Store A, Hold B Store A in both registers
L L	X L	H or L ↓	↓ ↓	X X	X X[1]	Unspecified[2] Output	Input Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

1. Select control=L: clocks can occur simultaneously.
   Select control=H: clocks must be staggered in order to load both registers. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. ↓ = LOW-to-HIGH Transition.
2. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[5]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[7]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[7]

Parameter	Description	Typ.[6]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

3. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. T_A is the "instant on" case temperature.
6. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
7. This parameter is guaranteed but not tested.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[9] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, GAB=GND, $\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, GAB=GND, $\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, GAB=GND, $\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, GAB=$\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[12]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, GAB=$\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics[13] Over the Operating Range

Parameter	Description	FCT652T				FCT652AT				Unit	Fig. No.[15]
		Military		Commercial		Military		Commercial			
		Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	2.0	15.0	1.5	14.0	2.0	10.5	1.5	9.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	2.0	7.0	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	2.0	8.4	1.5	7.7	ns	1, 5
t_S	Set-Up Time HIGH or LOW Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t_W	Clock Pulse Width,[16] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT652CT				FCT652DT		Unit	Fig. No.[15]
		Military		Commercial		Commercial			
		Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	1.5	4.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	1.5	8.9	1.5	7.8	1.5	5.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	1.5	7.7	1.5	6.3	1.5	4.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	1.5	4.4	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	1.5	5.0	ns	1, 5
t_S	Set-Up Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	1.5		1.5		1.0		ns	4
t_W	Pulse Width,[16] HIGH or LOW	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

13. AC Characteristics guaranteed with $C_L=50$ pF as shown in Figure 1 of "Parameter Measurement Information" in the General Information section.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.
16. With one data channel toggling, $t_W(L)=t_W(H)=4.0$ ns and $t_r=t_f=1.0$ ns.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT652DTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT652DTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.4	CY74FCT652CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT652CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT652CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT652CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT652CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT652ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT652ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT652ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT652ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT652ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT652TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT652TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT652TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT652TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT652TLMB	L64	28-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

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9

CY54/74FCT821T
CY54/74FCT823T
CY54/74FCT825T

8-/9-/10-Bit Bus Interface Registers

Features

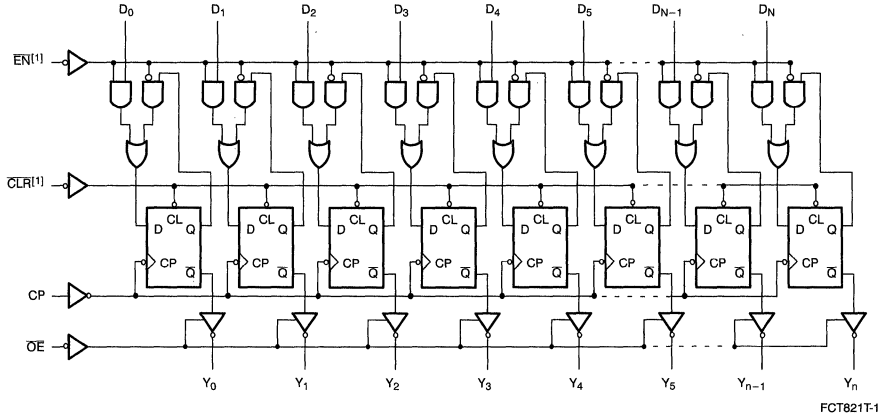
- **Function, pinout and drive compatible with FCT, F, and Am29821/23/25 logic**
- **FCT-C speed at 6.0 ns max. (Com'l) FCT-B speed at 7.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Buffered common clock enable ($\overline{EN}$) and asynchronous clear input ($\overline{CLR}$)**

Functional Description

These bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T is a buffered, 10-bit wide version of the popular FCT374 function. The FCT823T is a 9-bit wide buffered register with clock enable ($\overline{EN}$) and clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The FCT825T is an 8-bit buffered register with all the FCT823T controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

These devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

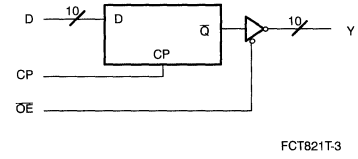
Logic Block Diagram



Note:
1. Not on FCT821.

Logic Diagrams

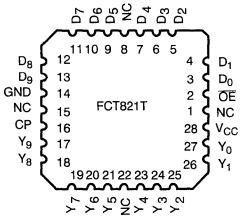
FCT821T (10-Bit Register)



FCT821T-3

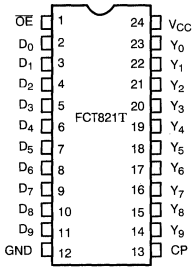
Pin Configurations

LCC/PLCC
Top View



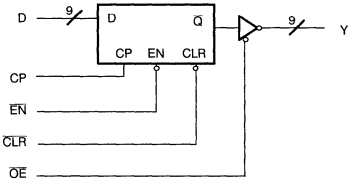
FCT821T-5

DIP
Top View



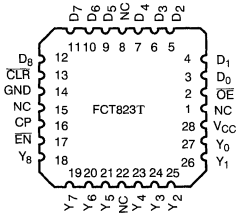
FCT821T-6

FCT823T (9-Bit Register)



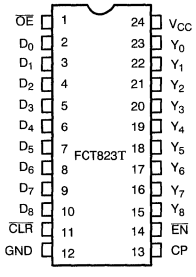
FCT821T-2

LCC/PLCC
Top View



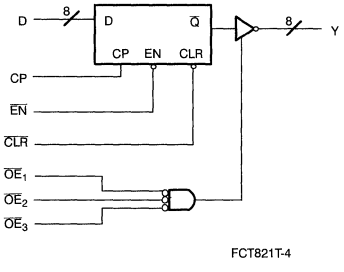
FCT821T-7

DIP
Top View



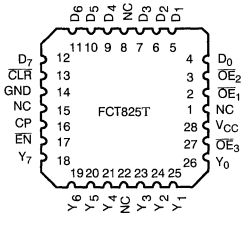
FCT821T-8

FCT825T (8-Bit Register)



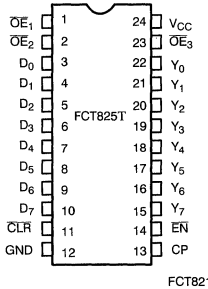
FCT821T-4

LCC/PLCC
Top View



FCT821T-9

DIP
Top View



FCT821T-10

Pin Description

Name	I/O	Description
D	I	The D flip-flop data inputs.
$\overline{CLR}$	I	When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the Q outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When $\overline{EN}$ is LOW, data on the D input is transferred to the Q output on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the Q outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the TRUE register data is present at the Y outputs.

Function Table[2]

Inputs					Internal Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D	CP	Q	Y	
H	H	L	L	⌐	L	Z	High Z
H	H	L	H	⌐	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	⌐	L	Z	Load
H	H	L	H	⌐	H	Z	
L	H	L	L	⌐	L	L	
L	H	L	H	⌐	H	H	

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[5]	All	−55°C to +125°C	5V ± 10%

Notes:

2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, ⌐ = LOW-to-HIGH Transition, Z = HIGH Impedance.
3. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[7]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[7]

Parameter	Description	Typ.[6]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:
6. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
7. This parameter is guaranteed but not tested.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[9] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=$\overline{EN}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=$\overline{EN}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=$\overline{EN}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=$\overline{EN}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=$\overline{EN}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Param.	Description	Test Load	FCT821AT/FCT823AT/ FCT825AT				FCT821BT/FCT823BT/ FCT825BT				Unit	Fig. No.[14]
			Military		Commercial		Military		Commercial			
			Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Y ($\overline{OE}$=LOW)	C_L=50 pF R_L=500Ω		11.5		10.0		8.5		7.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to Y ($\overline{OE}$=LOW)[7]	C_L=300 pF R_L=500Ω		20.0		20.0		16.0		15.0	ns	1, 5
t_{PLH}	Propagation Delay $\overline{CLR}$ to Y	C_L=50 pF R_L=500Ω		15.0		14.0		9.5		9.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω		13.0		12.0		9.0		8.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[7]	C_L=300 pF R_L=500Ω		25.0		23.0		16.0		15.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y [7]	C_L=5 pF R_L=500Ω		8.0		7.0		7.0		6.5	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω		9.0		8.0		8.0		7.5	ns	1, 7, 8
t_{SU}	Data to CP Set-Up Time	C_L=50 pF R_L=500Ω	4.0		4.0		3.0		3.0		ns	4
t_H	Data to CP Hold Time		2.0		2.0		1.5		1.5		ns	4
t_{SU}	Enable $\overline{EN}$ to CP Set-Up Time		4.0		4.0		3.0		3.0		ns	4
t_H	Enable $\overline{EN}$ to CP Hold Time		2.0		2.0		0.0		0.0		ns	4
t_{REM}	Clear Recovery Time $\overline{CLR}$ to CP		7.0		6.0		6.0		6.0		ns	6
t_W	Clock Pulse Width		7.0		7.0		6.0		6.0		ns	5
t_W	$\overline{CLR}$ Pulse Width LOW		7.0		6.0		6.0		6.0		ns	5

Notes:
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information".

9

Switching Characteristics Over the Operating Range (continued)

Param.	Description	Test Load	FCT821CT/FCT823CT/FCT825CT				Unit	Fig. No.[14]
			Military		Commercial			
			Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Y ($\overline{OE}$=LOW)	C_L=50 pF R_L=500Ω		7.0		6.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to Y ($\overline{OE}$=LOW)[6]	C_L=300 pF R_L=500Ω		13.5		12.5	ns	1, 5
t_{PLH}	Propagation Delay $\overline{CLR}$ to Y_1	C_L=50 pF R_L=500Ω		8.5		8.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω		8.0		7.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[6]	C_L=300 pF R_L=500Ω		13.5		12.5	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y[6]	C_L=5 pF R_L=500Ω		6.2		6.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω		6.5		6.5	ns	1, 7, 8
t_{SU}	Data to CP Set-Up Time	C_L=50 pF R_L=500Ω	3.0		3.0		ns	4
t_H	Data to CP Hold Time		1.5		1.5		ns	4
t_{SU}	Enable $\overline{EN}$ to CP Set-Up Time		3.0		3.0		ns	4
t_H	Enable $\overline{EN}$ to CP Hold Time		0.0		0.0		ns	4
t_{REM}	Clear Recovery Time $\overline{CLR}$ to CP		6.0		6.0		ns	6
t_W	Clock Pulse Width		6.0		6.0		ns	5
t_W	$\overline{CLR}$ Pulse Width LOW		6.0		6.0		ns	5

Ordering Information – FCT821T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT821CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY54FCT821CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT821CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT821BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY54FCT821BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT821BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY74FCT821ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT821ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT821ATLMB	L64	28-Square Leadless Chip Carrier	

Ordering Information – FCT823T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT823CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY54FCT823CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT823CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT823BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY54FCT823BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT823BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY74FCT823ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT823ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT823ATLMB	L64	28-Square Leadless Chip Carrier	

Ordering Information—FCT825T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT825CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT825CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT825BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT825BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825BTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT825ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT825ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825ATLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38−00282−A

CY54/74FCT827T

10-Bit Buffers

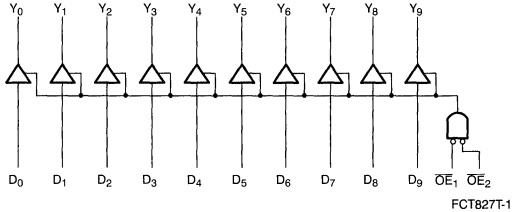
Features

- **Function, pinout and drive compatible with FCT, F, and AM29827 logic**
- **FCT-C speed at 4.4ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

The FCT827T 10-bit bus driver provides high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility. The FCT827T is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All outputs are designed for low-capacitance bus loading in the high-impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

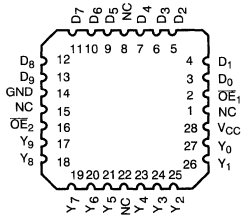
Logic Block Diagram



FCT827T-1

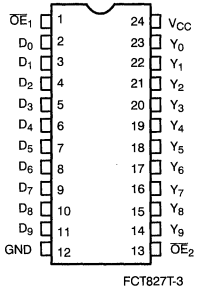
Pin Configurations

LCC/PLCC
Top View



FCT827T-2

DIP
Top View



FCT827T-3

Function Table[1]

Inputs			Outputs	
$\overline{OE_1}$	$\overline{OE_2}$	D	Y	Function
L L	L L	L H	L H	Transparent
H X	X H	X X	Z Z	Three-State

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	4.1	13.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range[12]

Parameter	Description	Test Load	FCT827AT Military Min.	FCT827AT Military Max.	FCT827AT Commercial Min.	FCT827AT Commercial Max.	FCT827BT Military Min.	FCT827BT Military Max.	FCT827BT Commercial Min.	FCT827BT Commercial Max.	Unit	Fig. No.[13]
t_{PLH} t_{PHL}	Propagation Delay D to Y	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	8.0	1.5	6.5	1.5	5.0	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay D to Y[6]	C_L=300 pF R_L=500Ω	1.5	17.0	1.5	15.0	1.5	14.0	1.5	13.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	13.0	1.5	12.0	1.5	9.0	1.5	8.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[6]	C_L=300 pF R_L=500Ω	1.5	25.0	1.5	23.0	1.5	16.0	1.5	15.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time- $\overline{OE}$ to Y[6]	C_L=5 pF R_L=500Ω	1.5	9.0	1.5	9.0	1.5	7.0	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.0	ns	1, 7, 8

Parameter	Description	Test Load	FCT827CT Military Min.	FCT827CT Military Max.	FCT827CT Commercial Min.	FCT827CT Commercial Max.	Unit	Fig. No.[13]
t_{PLH} t_{PHL}	Propagation Delay D to Y	C_L=50 pF R_L=500Ω	1.5	5.0	1.5	4.4	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay D to Y[6]	C_L=300 pF R_L=500Ω	1.5	11.0	1.5	10.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[6]	C_L=300 pF R_L=500Ω	1.5	15.0	1.5	14.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y[6]	C_L=5 pF R_L=500Ω	1.5	6.7	1.5	5.7	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	7.0	1.5	6.0	ns	1, 7, 8

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT827CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT827CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT827CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT827BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT827BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT827BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT827CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT827CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY54FCT827BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT827BTLMB	L64	28-Square Leadless Chip Carrier	
8.0	CY74FCT827ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT827ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT827ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT827ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT827ATLMB	L64	28-Square Leadless Chip Carrier	

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CY54/74FCT841T

10-Bit Latch

Features

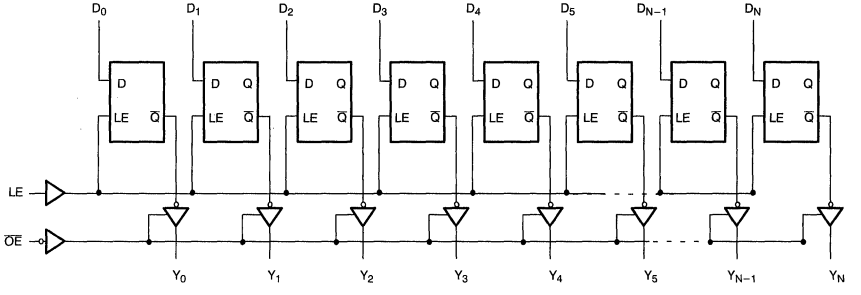
- **Function, pinout and drive compatible with FCT, F, and AM29841 logic**
- **FCT-C speed at 5.5ns max. (Com'l) FCT-B speed at 6.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **High-speed parallel latches**
- **Buffered common latch enable input**

Functional Description

The FCT841T bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The FCT841T is a buffered 10-bit wide version of the FCT373 function.

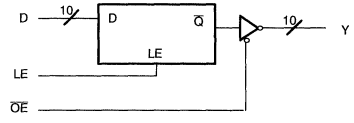
The FCT841T high-performance interface is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

Functional Block Diagram



FCT841T-1

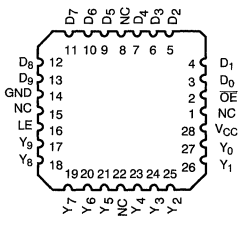
Logic Block Diagram



FCT841T-2

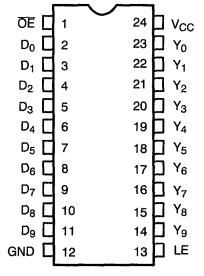
Pin Configurations

LCC/PLCC
Top View



FCT841T-3

DIP
Top View



FCT841T-4

Pin Description

Name	I/O	Description
D	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When the $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_1 are in the high impedance (off) state.

Function Table[1]

Inputs			Internal Outputs		Function
$\overline{OE}$	LE	D	O	Y	
H	X	X	X	Z	High Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, Z = High Impedance
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.

9

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)[8]	V_{CC}=Max., V_{IN}=3.4V, f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, LE=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, LE=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, LE=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, LE=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.0	3.2[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, LE=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	4.1	13.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	Test Load	FCT841AT				FCT841BT				Unit	Fig. No.[13]
			Military		Commercial		Military		Commercial			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_1 to Y_1 (LE=HIGH)	C_L=50 pF R_L=500Ω	1.5	10.0	1.5	9.0	1.5	7.5	1.5	6.5	ns	1, 3
	Propagation Delay D_1 to Y_1 (LE=HIGH)	C_L=300 pF R_L=500Ω	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	ns	1, 3
t_{SU}	Data to LE Set-Up Time	C_L=50 pF R_L=500Ω	2.5		2.5		2.5		2.5		ns	9
t_H	Data to LE Hold Time	C_L=50 pF R_L=500Ω	3.0		2.5		2.5		2.5		ns	9
t_{PLH} t_{PHL}	Propagation Delay LE to Y_1	C_L=50 pF R_L=500Ω	1.5	13.0	1.5	12.0	1.5	10.5	1.5	8.0	ns	1, 3
	Propagation Delay LE to Y_1 [6]	C_L=300 pF R_L=500Ω	1.5	20.0	1.5	16.0	1.5	18.0	1.5	15.5	ns	1, 3
t_W	LE Pulse Width (HIGH)	C_L=50 pF R_L=500Ω	5.0		4.0		4.0		4.0		ns	5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L=50 pF R_L=500Ω	1.5	13.0	1.5	11.5	1.5	8.5	1.5	8.0	ns	1, 7, 8
	Output Enable Time $\overline{OE}$ to Y_1[6]	C_L=300 pF R_L=500Ω	1.5	25.0	1.5	23.0	1.5	15.0	1.5	14.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_1[6]	C_L=5 pF R_L=500Ω	1.5	9.0	1.5	7.0	1.5	6.5	1.5	6.0	ns	1, 7, 8
	Output Disable Time $\overline{OE}$ to Y_1	C_L=50 pF R_L=500Ω	1.5	10.0	1.5	8.0	1.5	7.5	1.5	7.0	ns	1, 7, 8

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Switching Characteristics Over the Operating Range[12] (continued)

Parameter	Description	Test Load	FCT841CT				Unit	Fig. No.[13]
			Military		Commercial			
			Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_1 to Y_1 (LE=HIGH)	C_L=50 pF R_L=500Ω	1.5	6.3	1.5	5.5	ns	1, 3
	Propagation Delay D_1 to Y_1 (LE=HIGH)	C_L=300 pF R_L=500Ω	1.5	15.0	1.5	13.0	ns	1, 3
t_{SU}	Data to LE Set-Up Time	C_L=50 pF R_L=500Ω	2.5		2.5		ns	9
t_H	Data to LE Hold Time	C_L=50 pF R_L=500Ω	3.0		2.5		ns	9
t_{PLH} t_{PHL}	Propagation Delay LE to Y_1	C_L=50 pF R_L=500Ω	1.5	6.8	1.5	6.4	ns	1, 3
	Propagation Delay LE to Y_1[6]	C_L=300 pF R_L=500Ω	1.5	16.0	1.5	15.0	ns	1, 3
t_W	LE Pulse Width (HIGH)	C_L=50 pF R_L=500Ω	4.0		4.0		ns	5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L=50 pF R_L=500Ω	1.5	7.3	1.5	6.5	ns	1, 7, 8
	Output Enable Time $\overline{OE}$ to Y_1[6]	C_L=300 pF R_L=500Ω	1.5	13.0	1.5	12.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_1[6]	C_L=5 pF R_L=500Ω	1.5	6.0	1.5	5.7	ns	1, 7, 8
	Output Disable Time $\overline{OE}$ to Y_1	C_L=50 pF R_L=500Ω	1.5	6.3	1.5	6.0	ns	1, 7, 8

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT841CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT841CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT841CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.3	CY54FCT841CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT841CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY74FCT841BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT841BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT841BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT841BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT841BTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT841ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT841ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT841ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY54FCT841ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT841ATLMB	L64	28-Square Leadless Chip Carrier	

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CY54/74FCT2240T
CY54/74FCT2244T

8-Bit Buffers/Line Drivers

Features

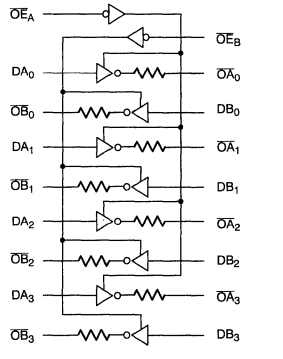
- **Function and pinout compatible with FCT and F logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.8 ns max. (Com'l)**
- **TTL output level versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA (Com'l), 12 mA (Mil)**
- **Source current 15 mA (Com'l), 12 mA (Mil)**
- **Three-state outputs**

Functional Description

The FCT2240T and FCT2244T are octal buffers and line drivers that include on-chip 25Ω terminating resistors at each of the outputs, to minimize noise resulting from reflections or standing waves in high-performance applications. The on-chip resistors reduce overall board space and component count. Designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers, these devices provide speed and drive capabilities commensurate with their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without the need for external components.

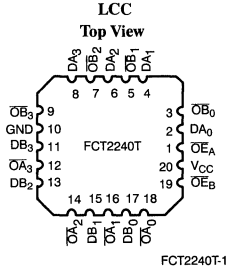
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram FCT2240T

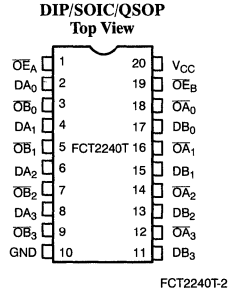


FCT2240T-1

Pin Configurations

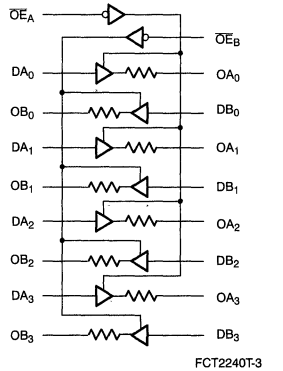


FCT2240T-1

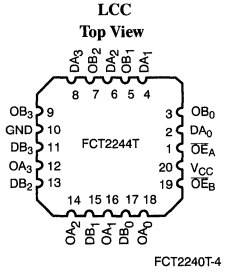


FCT2240T-2

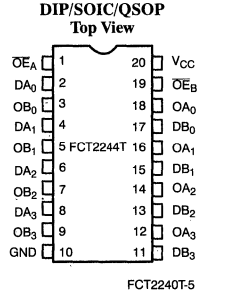
Logic Block Diagram FCT2244T



FCT2240T-3



FCT2240T-4



FCT2240T-5

Function Table FCT2240T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT2244T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1=\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1=\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics FCT2240T Over the Operating Range[12]

Parameter	Description	FCT2240T				FCT2240AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT2240CT		Unit	Fig. No.[13]
		Commercial			
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	4.1	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.2	ns	1, 7, 8

Switching Characteristics FCT2244T Over the Operating Range[12]

Parameter	Description	FCT2244T				FCT2244A				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	7.0	1.5	6.5	1.5	5.1	1.5	4.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.5	1.5	8.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT2244CT		FCT2244DT		Unit	Fig. No.[13]
		Commercial		Commercial			
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Input	1.5	4.1	1.5	3.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.8	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.2	1.5	4.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT2240CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2240CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2240CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.8	CY74FCT2240ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2240ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2240ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2240ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2240ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2240TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2240TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2240TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT2240TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2240TLMB	L61	20-Pin Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT2244DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2244DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.3	CY74FCT2244CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2244CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2244CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY74FCT2244ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2244ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2244ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2244ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2244ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT2244TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2244TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2244TSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT2244TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2244TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38−00341−A

CY54/74FCT2245T

8-Bit Transceiver

Features

- **Function and pinout compatible with FCT and F logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.6 ns max. (Com'l)**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current** **12 mA (Com'l), 12 mA (Mil)**
  Source current **15 mA (Com'l), 12 mA (Mil)**
- **Three-state outputs**

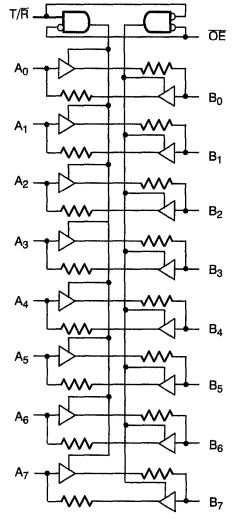
Functional Description

The FCT2245T contains eight non-inverting, bidirectional buffers with three-state outputs intended for bus oriented applications. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. For this reason, the FCT2245T can be used in an existing design to replace the FCT245T. The FCT2245T current sinking capability is 12 mA at the A and B ports.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports; receive (Active LOW) enables data from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both the A and B ports by putting them in a High Z condition.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

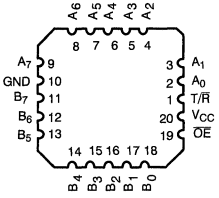
Logic Block Diagram



FCT2245T-1

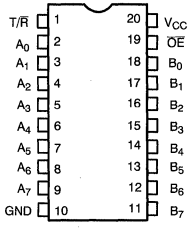
Pin Configurations

LCC
Top View



FCT2245T-2

DIP/SOIC/QSOP
Top View



FCT2245T-3

Function Table [1]

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Test Conditions	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $T/\overline{R}=\overline{OE}=GND$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $T/\overline{R}=\overline{OE}=GND$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $T/\overline{R}=\overline{OE}=GND$, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $T/\overline{R}=\overline{OE}=GND$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $T/\overline{R}=\overline{OE}=GND$, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2245T				FCT2245AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	7.5	1.5	7.0	1.5	4.9	1.5	4.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.0	1.5	9.5	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	ns	1, 7, 8

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	FCT2245CT		FCT2245DT		Unit	Fig. No.[13]
		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	4.1	1.5	3.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.8	1.5	5.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	4.5	1.5	4.3	ns	1, 7, 8

Ordering Information—FCT2245T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT2245DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2245DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT2245CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2245CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2245CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY74FCT2245ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2245ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2245ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.9	CY54FCT2245ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2245ATLMB	L61	20-Pin Square Leadless Chip Carrier	
7.0	CY54FCT2245TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2245TLMB	L61	20-Pin Square Leadless Chip Carrier	
7.5	CY74FCT2245TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2245TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2245TSOC	S5	20-Lead (300-Mil) Molded SOIC	

Shaded areas contain preliminary information.

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Document #: 38–00349

CY54/74FCT2257T

Quad 2-Input Multiplexer

Features

- **Function and pinout compatible with FCT and F logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.3 ns max. (Com'l) FCT-A speed at 5.0 ns max. (Com'l)**
- **TTL output level versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current** **12 mA (Com'l), 12 mA (Mil)**
  Source current **15 mA (Com'l), 12 mA (Mil)**
- **Three-state outputs**

Functional Description

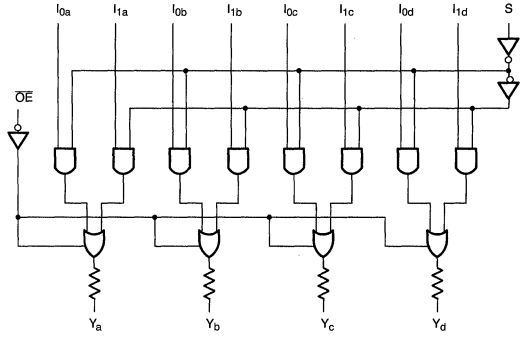
The FCT2257T has four identical two-input multiplexers that select four bits of data from two sources under the control of a common data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT2257T. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2257T can be used to replace the FCT257T to reduce noise in an existing design

The FCT2257T is a logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedence "OFF" state when the Output Enable input ($\overline{OE}$) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

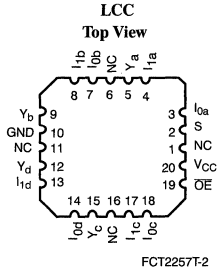
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

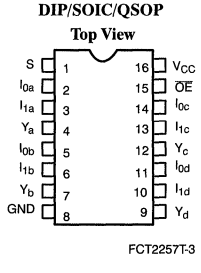


FCT2257T-1

Pin Configurations



FCT2257T-2



FCT2257T-3

Pin Description

Name	Description
I	Data Inputs
S	Common Select Input
$\overline{OE}$	Enable Inputs (Active LOW)
Y	Data Outputs

Function Table[1]

Inputs				Output
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High impedence (OFF) state

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	μA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	μA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	μA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	μA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	μA

Capacitance[6]

Parameter	Description	Test Conditions	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.7	5.4[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2257T				FCT2257AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Y	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay S to O	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.0	1.5	8.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	6.0	1.5	5.8	1.5	5.5	ns	1, 7, 8

Parameter	Description	FCT2257CT		Unit	Fig. No.[13]
		Commercial			
		Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Y	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay S to O	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.0	ns	1, 7, 8

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT2257CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2257CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT2257CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT2257ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2257ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT2257ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY54FCT2257ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT2257ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.0	CY74FCT2257TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2257TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT2257TSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT2257TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT2257TLMB	L61	20-Pin Square Leadless Chip Carrier	

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

Document #: 38–00340

CY54/74FCT2373T
CY54/74FCT2573T

8-Bit Latches

Features

- **Function and pinout compatible with the fastest bipolar logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.7 ns max. (Com'l) FCT-A speed at 5.2 ns max. (Com'l)**
- **Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current** 12 mA (Com'l), 12 mA (Mil)
- **Source current** 15 mA (Com'l), 12 mA (Mil)

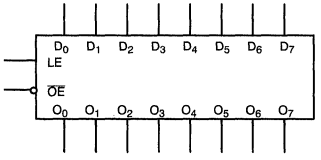
Functional Description

The FCT2373T and FCT2573T are 8-bit, high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25Ω termination resistors have been added to the outputs to reduce system noise caused by reflections. FCT2373T can be used to replace FCT373T, and FCT2573T to replace FCT573T to reduce noise in an existing design.

When latch enable (LE) is HIGH, the flip-flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable ($\overline{OE}$) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data can still be entered into the latches.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

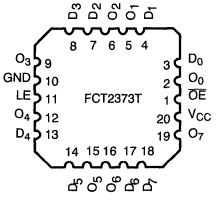
Logic Symbol



FCT2373T-1

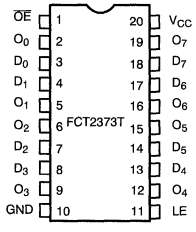
Pin Configurations

LCC
Top View



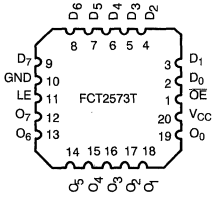
FCT2373T-4

DIP/SOIC/QSOP
Top View



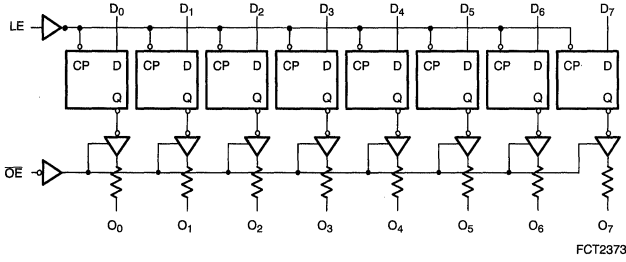
FCT2373T-5

LCC
Top View



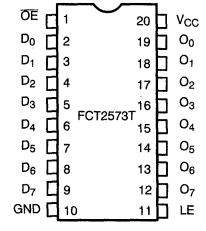
FCT2373T-6

Logic Block Diagram



FCT2373T-8

DIP/SOIC/QSOP
Top View



FCT2373T-7

Function Table[1]

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	28	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   Q_n = Previous state of flip flops (Q_{n-1})
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance	6	10	pF
C_{OUT}	Output Capacitance	8	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, LE=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}$=GND, LE=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, LE=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, LE=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2373T/FCT2573T				FCT2373AT/FCT2573AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	14.0	2.0	13.0	2.0	9.8	2.0	8.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	12.5	1.5	11.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.5	1.5	7.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_S	Set-Up Time, HIGH to LOW D to LE	2.0		2.0		2.0		2.0		ns	9
t_H	Hold Time, HIGH to LOW D to LE	1.5		1.5		1.5		1.5		ns	9
t_W	LE Pulse Width HIGH	6.0		6.0		6.0		5.0		ns	5

Parameter	Description	FCT2373CT/FCT2573CT				FCT2373DT/ FCT2573DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	5.1	1.5	4.2	1.5	3.8	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	8.0	2.0	5.5	2.0	4.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.3	1.5	5.5	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.9	1.5	5.0	1.5	4.0	ns	1, 7, 8
t_S	Set-Up Time, HIGH to LOW, D to LE	2.0		2.0		1.5		ns	9
t_H	Hold Time, HIGH to LOW, D to LE	1.5		1.5		1.0		ns	9
t_W	LE Pulse Width HIGH	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.

9

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT2373DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2373DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT2373CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2373CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT2373ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT2373ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2373TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT2373TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT2573DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2573DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT2573CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2573CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT2573ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT2573ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2573TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT2573TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38−00338−A

CY54/74FCT2374T
CY54/74FCT2574T

8-Bit Registers

Features

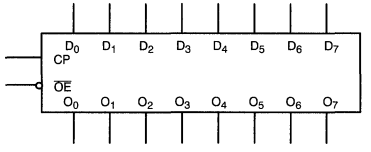
- **Function and pinout compatible with FCT and F logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 5.2 ns max. (Com'l) FCT-A speed at 6.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 12 mA (Com'l), 12 mA (Mil)**
  Source current 15 mA (Com'l), 12 mA (Mil)
- **Edge-triggered D-type inputs**
- **250 MHz typical toggle rate**

Functional Description

The FCT2374T and FCT2574T are high-speed low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2374T and FCT2574T can be used to replace the FCT374T and FCT574T to reduce noise in an existing design. Both devices have three-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The FCT2574T is identical to FCT2374T except that all the outputs are on one side of the package and inputs on the other side. The flip-flops contained in the FCT2374T and FCT2574T will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high-impedence state. The state of output enable does not affect the state of the flip-flops.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

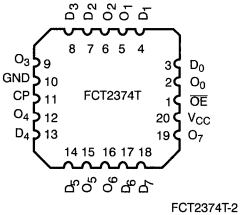
Logic Symbol



FCT2374T-1

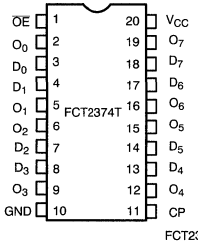
Pin Configurations

LCC
Top View



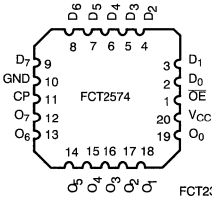
FCT2374T-2

DIP/SOIC/QSOP
Top View



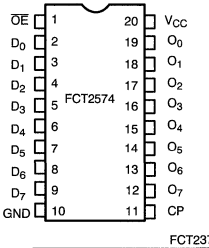
FCT2374T-3

LCC
Top View



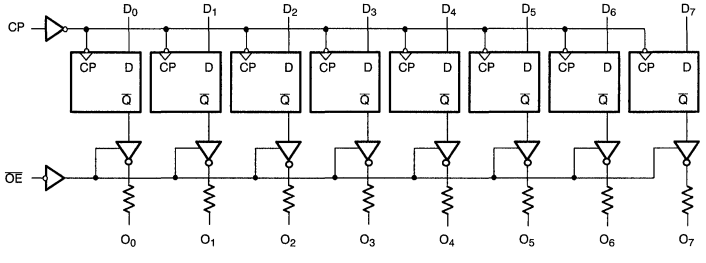
FCT2374T-4

DIP/SOIC/QSOP
Top View



FCT2374T-5

Logic Block Diagram



FCT2374T-2

9

Function Table[1]

Inputs			Outputs
D	CP	$\overline{OE}$	O
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   ⌐ = LOW-to-HIGH clock transition
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Test Conditions	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, f_0=10 MHz $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, f_0=10 MHz $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, Fo=10 MHz, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, Fo=10 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_i N_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2374T/FCT2574T				FCT2374AT/FCT2574AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t_H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t_W	Clk Pulse Width HIGH or LOW	6.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT2374CT/FCT2574CT				FCT2374DT/ FCT2574DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	6.5	2.0	5.2	2.0	4.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.9	1.5	6.2	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	6.5	1.5	5.0	1.5	4.0	ns	1, 7, 8
t_S	Set-Up Time, HIGH or LOW D to CP	2.0		1.5		2.0		ns	4
t_H	Hold Time, HIGH or LOW D to CP	1.0		1.0		1.0		ns	4
t_W	Clk Pulse Width HIGH or LOW	5.0		4.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT2374DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2374DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT2374CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2374CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2374CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2374CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2374CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT2374ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2374ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2374ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT2374ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2374ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT2374TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2374TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2374TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2374TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2374TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT2574DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2574DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT2574CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2574CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2574CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2574CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2574CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT2574ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2574ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2574ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT2574TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2574ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT2574TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2574TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2574TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2574TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2574TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38–00345

CY54/74FCT2541T

8-Bit Buffer/Line Driver

Features

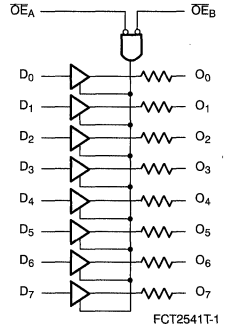
- **Function and pinout compatible with FCT and F logic**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.8 ns max. (Com'l)**
- **25Ω output series to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA (Com'l), 12 mA (Mil)**
  Source current 15 mA (Com'l), 12 mA (Mil)
- **Three-state outputs**

Functional Description

The FCT2541T is an octal buffer and line driver designed to be employed as a memory address driver, clock driver, and bus-oriented transmitter/receiver. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2541T can be used to replace the FCT541T to reduce noise in an existing design. The speed of the FCT2541T is comparable to bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

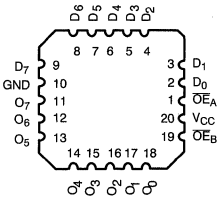
Logic Block Diagram



FCT2541T-1

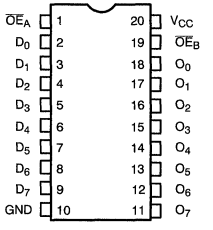
Pin Configurations

LCC
Top View



FCT2541T-1

DIP/SOIC/QSOP
Top View



FCT2541T-2

Function Table[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Note:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedence

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				15	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−15	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}_A=\overline{OE}_B$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_A=\overline{OE}_B$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_A=\overline{OE}_B$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_A=\overline{OE}_B$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_A=\overline{OE}_B$=GND, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2541T				FCT2541AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT2541CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	4.6	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	ns	1, 7, 8

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT2541CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2541CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2541CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY54FCT2541CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2541CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT2541ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2541ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2541ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2541ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2541ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2541TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2541TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2541TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT2541TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2541TLMB	L61	20-Pin Square Leadless Chip Carrier	

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Document #: 38–00342–A

CY54/74FCT2543T

8-Bit Latched Transceiver

Features

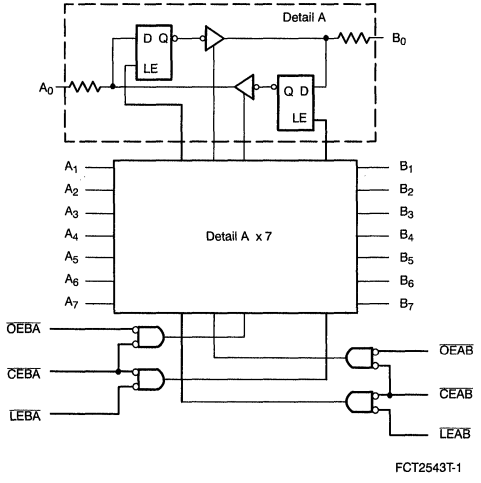
- **Function and pinout compatible with FCT and F logic**
- **FCT-C speed at 5.3 ns max. (Com'l) FCT-A speed at 6.5 ns max. (Com'l)**
- **25W output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA (Com'l), 12 mA (Mil)**
  Source current 15 mA (Com'l), 12 mA (Mil)
- **Separation controls for data flow in each direction**
- **Back to back latches for storage**
- **ESD > 2000V**

Functional Description

The FCT2543T Octal Latched Tranceiver contains two sets of eight D-type latches. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) permits each latch set to have independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW to enter data from A or to take data from B, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2543T can be used to replace the FCT543T to reduce noise in an existing design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

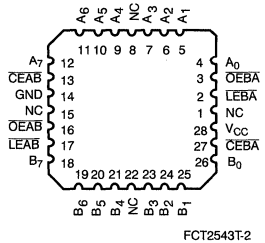
Functional Block Diagram



FCT2543T-1

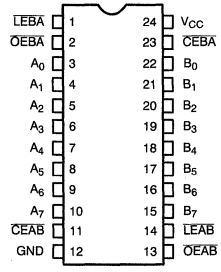
Pin Configurations

LCC
Top View



FCT2543T-2

DIP/SOIC/QSOP
Top View



FCT2543T-3

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1,2]

Inputs			Latch	Outputs
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B[3]	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs

Maximum Ratings[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[6]	All	−55°C to +125°C	5V ± 10%

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. A-to-B data flow shown: B-to-A is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
3. Before $\overline{LEAB}$ LOW-to-HIGH transition.
4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
6. T_A is the "instant on" case temperature.

9

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[8]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				15	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−15	µA
I_{OS}	Output Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[8]

Parameter	Description	Test Conditions	Typ. [7]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[10] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	1.2	mA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ =10 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ =10 MHz, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ =10 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[13]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0=\overline{LEAB}$ =10 MHz, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2543T Military Min.[14]	FCT2543T Military Max.	FCT2543T Commercial Min.[14]	FCT2543T Commercial Max.	FCT2543AT Military Min.[14]	FCT2543AT Military Max.	FCT2543AT Commercial Min.[14]	FCT2543AT Commercial Max.	Unit	Fig. No.[15]
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A $\overline{LEAB}$ to B	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	3.0		2.0		2.0		2.0		ns	9
t_H	Hold Time HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	2.0		2.0		2.0		2.0		ns	9
t_W	Pulse Width LOW $\overline{LEBA}$ or $\overline{LEAB}$	5.0		5.0		5.0		5.0		ns	5

Parameter	Description	FCT2543CT Military Min.[14]	FCT2543CT Military Max.	FCT2543CT Commercial Min.[14]	FCT2543CT Commercial Max.	FCT2543DT Commercial Min.[14]	FCT2543DT Commercial Max.	Unit	Fig. No.[15]
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.5	6.1	2.5	5.5	1.5	4.4	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	2.5	8.0	2.5	7.0	1.5	5.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	9.0	2.0	8.0	1.5	5.4	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	2.0	7.5	2.0	6.5	1.5	4.3	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	2.0		2.0		1.5		ns	9
t_H	Hold Time HIGH or LOW, A or B to $\overline{LEBA}$ or $\overline{LEAB}$	2.0		2.0		1.5		ns	9
t_W	Pulse Width LOW $\overline{LEBA}$ or $\overline{LEAB}$	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT2543DTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT2543DTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.3	CY74FCT2543CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2543CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2543CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.1	CY54FCT2543CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2543CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY74FCT2543ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2543ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2543ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT2543ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2543ATLMB	L64	28-Square Leadless Chip Carrier	
8.5	CY74FCT2543TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2543TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2543TSOC	S13	24-Lead (300-Mil) Molded SOIC	
10	CY54FCT2543TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2543TLMB	L64	28-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38−00348−A

CY54/74FCT2646T
CY54/74FCT2648T

8-Bit Registered Transceivers

Features

- **Function and pinout compatible with FCT and F logic**
- **FCT-C speed at 5.4 ns max. (Com'l) FCT-A speed at 6.3 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA (Com'l), 12 mA (Mil)**
- **Source current 15 mA (Com'l), 12 mA (Mil)**
- **Independent register for A and B buses**
- **Three-state output**

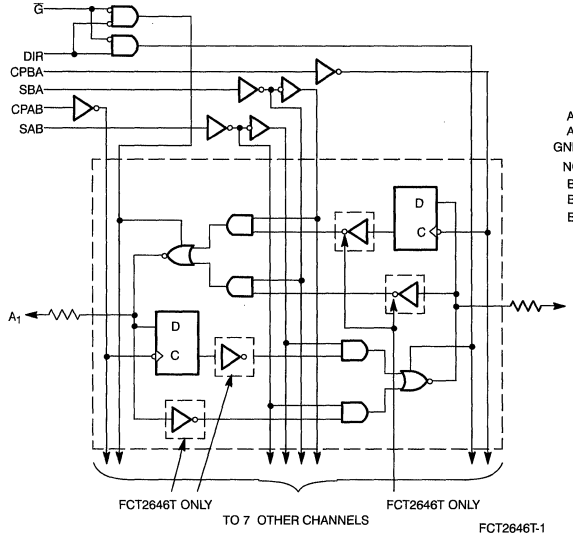
Functional Description

The FCT2646T and FCT2648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections so that the FCT2646T and the FCT2648T can be used to replace the FCT646T and the FCT648T, respectively, in an existing design.

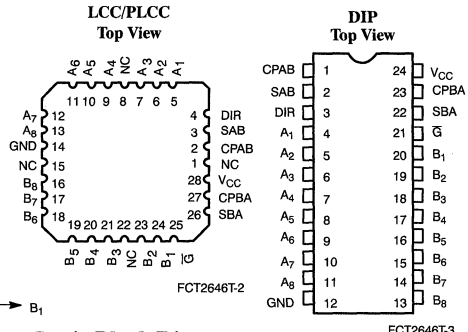
In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. Select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

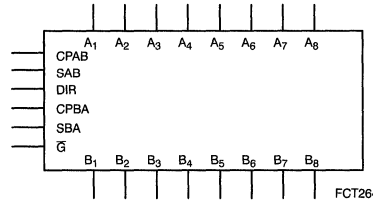
Functional Block Diagram



Pin Configurations

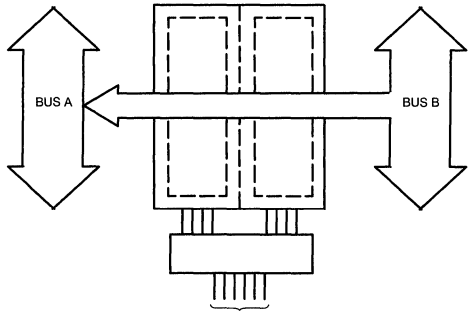


Logic Block Diagram



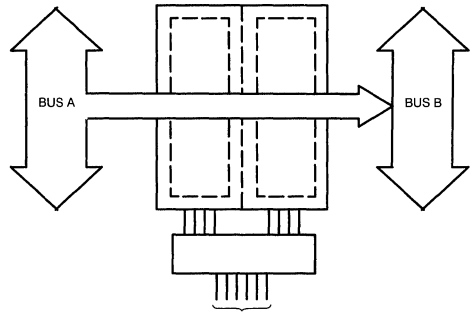
Pin Description

Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs



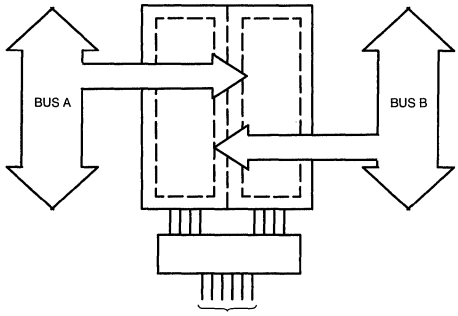
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	X

Real-Time Transfer
Bus B to Bus A



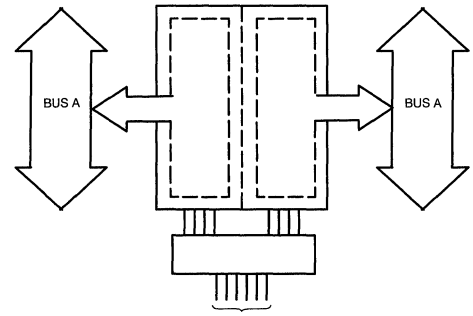
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	↓	X	X	X
L	L	X	↓	X	X
X	H	↓	↓	X	X

Storage from
A and/or B



DIR[1]	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data
to A and/or B

Function Table[2]

Inputs						Data I/O[3]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	FCT2646T	FCT2648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↓	↓	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

Notes:
1. Cannot transfer data to A bus and B bus simultaneously.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
3. The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

Maximum Ratings[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[6]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[8]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[8]

Parameter	Description	Typ. [7]	Max.	Unit
C_{IN}	Input Capacitance	6	10	pF
C_{OUT}	Output Capacitance	8	12	pF

Notes:

4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
6. T_A is the "instant on" case temperature.
7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[10] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[13]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT2646T/FCT2648T				FCT2646AT/FCT2648AT				Unit	Fig. No.[15]
		Military		Commercial		Military		Commercial			
		Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A_n or B_n	1.5	15.0	1.5	14.5	1.5	10.5	1.5	9.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	10.0	1.5	9.0	1.5	7.0	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	12.0	1.5	11.0	1.5	8.4	1.5	7.7	ns	1, 5
t_S	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t_W	Pulse Width,[6] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT2646CT/FCT2648CT				Unit	Fig. No.[15]
		Military		Commercial			
		Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A_n or B_n	1.5	8.9	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR to Bus	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
t_S	Set-Up Time HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
t_W	Pulse Width,[6] HIGH or LOW	5.0		5.0		ns	5

Notes:
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT2646CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2646CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2646CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2646CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2646CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT2646ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2646ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2646ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT2646ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2646ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT2646TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2646TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2646TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2646TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2646TLMB	L64	28-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT2648CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2648CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2648CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2648CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2648CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT2648ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2648ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2648ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT2648ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2648ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT2648TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2648TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2648TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2648TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2648TLMB	L64	28-Square Leadless Chip Carrier	

Document #: 38−00346

CY54/74FCT2652T

8-Bit Registered Transceiver

Features

- **Function and pinout compatible with FCT and F logic**
- **FCT-C speed at 5.4 ns max. (Com'l) FCT-A speed at 6.3 ns max. (Com'l)**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current** 12 mA (Com'l), 12 mA (Mil)
  Source current 15 mA (Com'l), 12 mA (Mil)
- **ESD > 2000V**
- **Independent register for A and B buses**
- **Multiplexed real-time and stored data transfer**

Functional Description

The FCT2652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

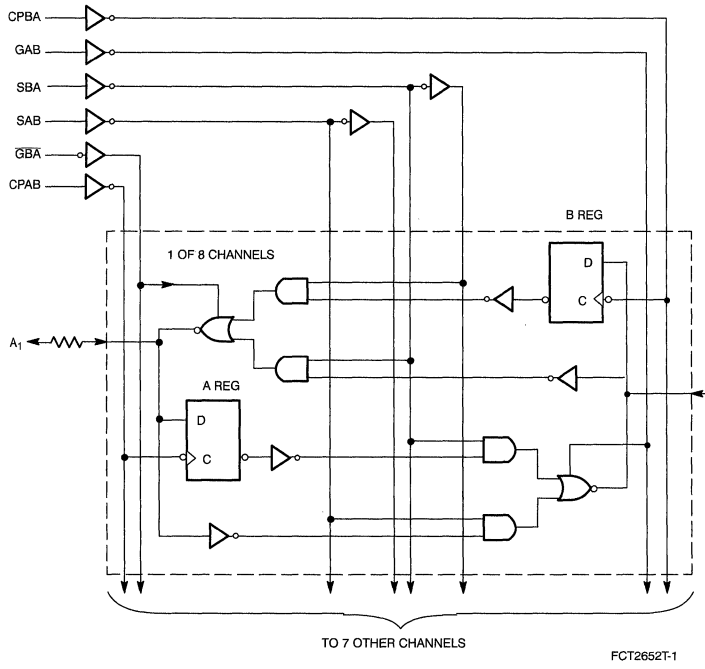
On-chip termination resistors are added to the outputs to reduce system noise caused by reflections. The FCT2652T can replace the FCT652T to reduce noise in an existing design.

The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

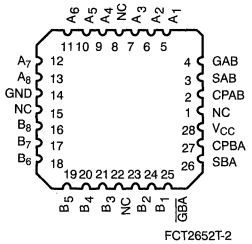
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



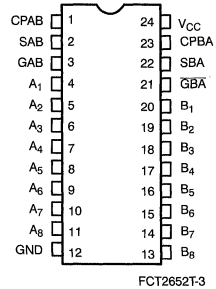
Pin Configurations

LCC
Top View

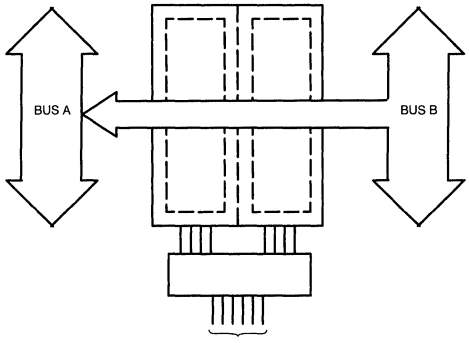


FCT2652T-2

DIP/SOIC/QSOP
Top View

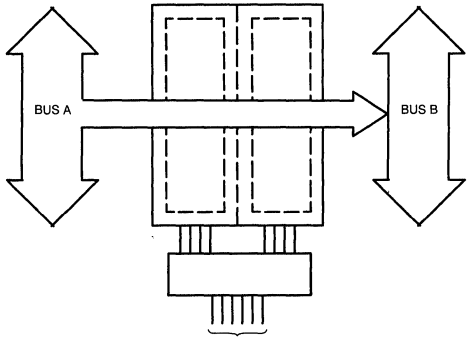


FCT2652T-3



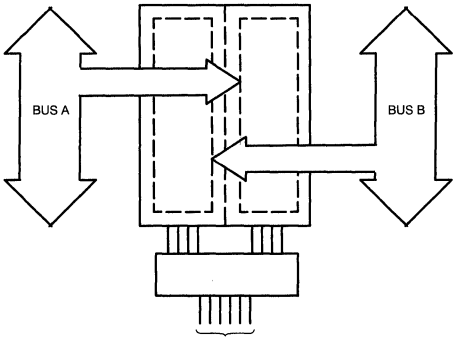
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



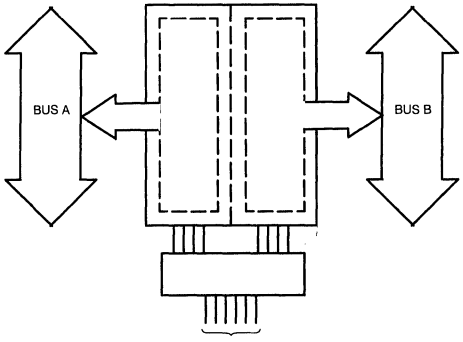
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Real-Time Transfer
Bus A to Bus B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Store Data from A and/or B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Transferred Stored Data
to A and/or B

9

Function Table[1]

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	
L L	H H	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X[1]	X X	Input Input	Unspecified[2] Output	Store A, Hold B Store A in both registers
L L	X L	H or L ↓	↓ ↓	X X	X X[1]	Unspecified[2] Output	Input Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[5]	All	−55°C to +125°C	5V ± 10%

Notes:

1. Select control=L: clocks can occur simultaneously.
   Select control=H: clocks must be staggered in order to load both registers. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[7]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[7]

Parameter	Description	Test Conditions	Typ. [6]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

6. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
7. This parameter is guaranteed but not tested.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[9] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, GAB=GND, $\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, GAB=GND, $\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, GAB=GND, $\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, GAB=$\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[12]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, GAB=$\overline{GBA}$=GND, SAB=CPAB=GND, SBA=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics[13] Over the Operating Range

Parameter	Description	FCT2652T				FCT2652AT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[15]	Max.	Min.[15]	Max.	Min.[15]	Max.	Min.[15]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	1.5	15.0	1.5	14.0	1.5	10.5	1.5	9.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	10.0	1.5	9.0	1.5	7.0	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	12.0	1.5	11.0	1.5	8.4	1.5	7.7	ns	1, 5
t_S	Set-Up Time HIGH or LOW Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t_W	Clock Pulse Width,[16] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT2652CT				FCT2652DT		Unit	Fig. No.[14]
		Military		Commercial		Commercial			
		Min.[15]	Max.	Min.[15]	Max.	Min.[15]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	1.5	4.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	1.5	8.9	1.5	7.8	1.5	5.0	ns	1, 3
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	1.5	7.7	1.5	6.3	1.5	4.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	1.5	4.4	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	1.5	5.0	ns	1, 5
t_S	Set-Up Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	1.5		1.5		1.0		ns	4
t_W	Pulse Width,[16] HIGH or LOW	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

13. AC Characteristics guaranteed with $C_L = 50$ pF as shown in Figure 1 in "Parameter Measurement Information" in the General Information Section..
14. See "Parameter Measurement Information" in the General Information Section.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. With one data channel toggling, $t_W(L) = t_W(H) = 4.0$ ns and $t_r = t_f = 1.0$ ns.

9

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT2652DTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT2652DTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.4	CY74FCT2652CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2652CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2652CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2652CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2652CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT2652ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2652ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2652ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT2652ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2652ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT2652TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2652TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2652TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2652TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2652TLMB	L64	28-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

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Features

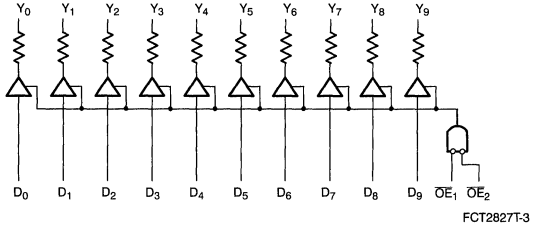
- **Function and pinout compatible with FCT, F, and AM29827 logic**
- **FCT-C speed at 5.0 ns max. (Com'l), FCT-A speed at 8.0 ns max. (Com'l)**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA (Com'l), 12 mA (Mil)**
- **Source current 15 mA (Com'l), 12 mA (Mil)**

Functional Description

The FCT2827T 10-bit bus driver provides high-performance bus interface buffering for wide data/address paths or buses carrying parity. This 10-bit buffer has NAND-ed output enables for maximum control flexibility. The FCT2827T is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2827T can be used to replace the FCT827T to reduce noise in an existing design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

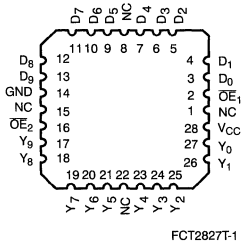
Logic Block Diagram



FCT2827T-3

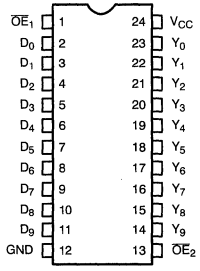
Pin Configurations

LCC/PLCC
Top View



FCT2827T-1

DIP
Top View



FCT2827T-2

Function Table[1]

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D	Y	Function
L L	L L	L H	L H	Transparent
H X	X H	X X	Z Z	Three-State

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=12 mA	Mil		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
		V_{CC}=Min., I_{OL}=12 mA	Mil		25		Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	μA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	μA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	μA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	μA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				−10	μA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	μA

Capacitance[6]

Parameter	Description	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	4.1	13.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Param.	Description	Test Load	FCT2827AT				FCT2827BT				Unit	Fig. No.[12]
			Military		Commercial		Military		Commercial			
			Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Y	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	8.0	1.5	6.5	1.5	5.0	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay D to Y[6]	C_L=300 pF R_L=500Ω	1.5	17.0	1.5	15.0	1.5	14.0	1.5	13.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	13.0	1.5	12.0	1.5	9.0	1.5	8.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[6]	C_L=300 pF R_L=500Ω	1.5	25.0	1.5	23.0	1.5	16.0	1.5	15.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y[6]	C_L=5 pF R_L=500Ω	1.5	10.0	1.5	9.0	1.5	7.0	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	10.0	1.5	9.0	1.5	8.0	1.5	7.0	ns	1, 7, 8

Param.	Description	Test Load	FCT2827CT				Unit	Fig. No.[12]
			Military		Commercial			
			Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Y	C_L=50 pF R_L=500Ω	1.5	5.0	1.5	4.4	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay D to Y[6]	C_L=300 pF R_L=500Ω	1.5	11.0	1.5	10.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[6]	C_L=300 pF R_L=500Ω	1.5	15.0	1.5	14.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y[6]	C_L=5 pF R_L=500Ω	1.5	6.7	1.5	5.7	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	7.0	1.5	6.0	ns	1, 7, 8

Notes:

12. See "Parameter Measurement Information" in the General Information section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT2827CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2827CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2827CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT2827BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2827BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2827BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.0	CY54FCT2827CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2827CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY54FCT2827BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2827BTLMB	L64	28-Square Leadless Chip Carrier	
8.0	CY74FCT2827ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2827ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2827ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT2827ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2827ATLMB	L64	28-Square Leadless Chip Carrier	

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CY74FCT16240T
CY74FCT162240T

16-Bit Buffers/Line Drivers

Features

- **Low power, pin compatible replacement for ABT functions**
- **FCT-C speed at 4.3 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16240T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162240T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

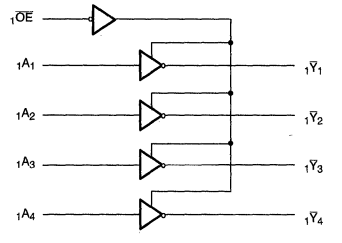
Functional Description

These 16-bit buffer/line drivers are used in memory driver, clock driver, or other bus interface applications, where high speed and low power are required. With flow-through pinout and small shrink packaging, board layout is simplified. The three-state controls are designed to allow 4-, 8-, or 16-bit operation. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

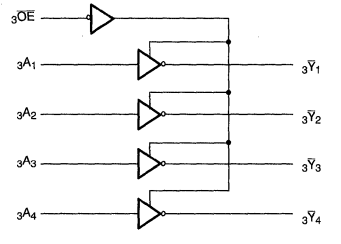
The CY74FCT16240T is ideally suited for driving high capacitance loads and low-impedance backplanes.

The CY74FCT162240T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162240T is ideal for driving transmission lines.

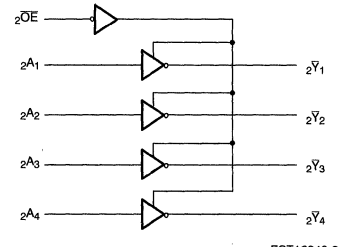
Logic Block Diagrams



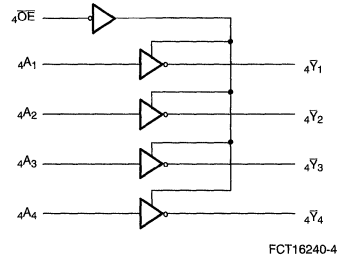
FCT16240-1



FCT16240-3



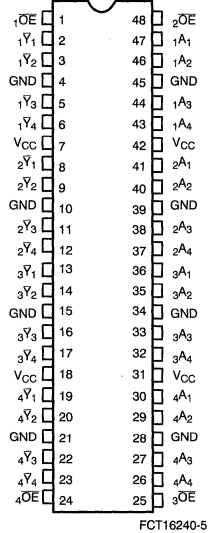
FCT16240-2



FCT16240-4

Pin Configuration

SSOP/TSSOP
Top View



FCT16240-5

Pin Summary

Name	Description
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs
$\overline{Y}$	Three-State Outputs

Function Table[1]

Inputs		Outputs
$\overline{OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16240T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162240T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Notes:

2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[7]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	60	100	µA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.4	4.5[10]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[10]	mA

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16240T CY74FCT162240T		CY74FCT16240AT CY74FCT162240AT		CY74FCT16240CT CY74FCT162240CT		Unit	Fig. No.[12]
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	8.0	1.5	4.8	1.5	4.3	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.0	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	9.5	1.5	5.6	1.5	5.2	ns	1, 7, 8
$t_{SK(O)}$	Output Skew[13]		0.5		0.5		0.5	ns	—

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = $I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information Section.
13. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information CY74FCT16240

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT16240CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16240CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16240ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16240ATPVC	O48	48-Lead (300-Mil) SSOP	
8.0	CY74FCT16240TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16240TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162240

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT162240CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162240CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162240ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162240ATPVC	O48	48-Lead (300-Mil) SSOP	
8.0	CY74FCT162240TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162240TPVC	O48	48-Lead (300-Mil) SSOP	

Document #: 38−00395

CY74FCT16244T/2244T
CY74FCT16444T/2H244T

16-Bit Buffers/Line Drivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 4.1 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16244T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162244T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

CY74FCT16444T Features:

- **64 mA sink current, 32 mA source current**
- **Reduced system loading**

CY74FCT162H244T Features:

- **Bus hold on data inputs**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

These 16-bit buffers/line drivers are designed for use in memory driver, clock driver, or other bus interface applications, where high-speed and low power are required. With flow-through pinout and small shrink packaging board layout is simplified. The three-state controls are designed to allow 4-bit, 8-bit or combined 16-bit operation. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

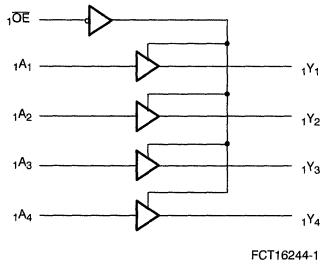
The CY74FCT16244T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162244T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162244T is ideal for driving transmission lines.

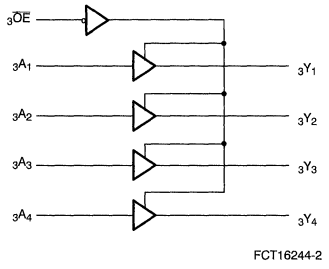
The CY74FCT16444 is designed for 16-bit operation, reducing control lines from four $\overline{OE}$ to one $\overline{OE}$ reduce input loading.

The CY74FCT162H244T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

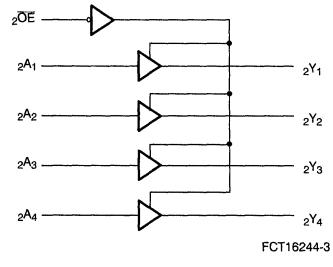
Logic Block Diagrams CY74FCT16244T, CY74FCT162244T, CY74FCT162H244T



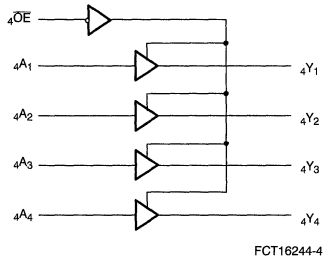
FCT16244-1



FCT16244-2



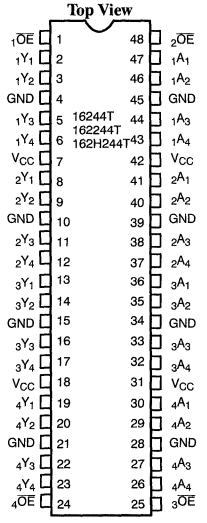
FCT16244-3



FCT16244-4

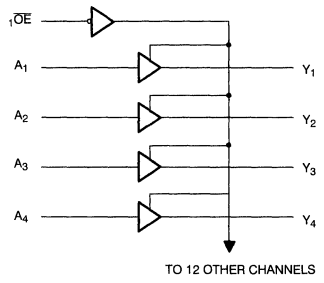
Pin Configuration

SSOP/TSSOP
Top View



FCT16244-5

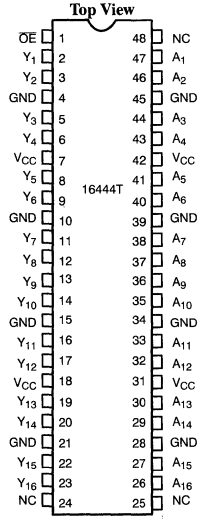
Logic Block Diagram CY74FCT16444T



FCT16244-6

Pin Configuration

SSOP/TSSOP
Top View



FCT16244-7

Pin Description

Name	Description
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs[1]
Y	Three-State Outputs

Function Table[2]

Inputs		Outputs
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Notes:

1. On CY74FCT162H244T these pins have "bus hold."
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[6]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[7]		V_{CC}=Min.	V_I=2.0V	−50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[7]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[8]		V_{CC}=Max., V_{OUT}=GND		−80	−140	−200	mA
I_O	Output Drive Current[6]		V_{CC}=Max., V_{OUT}=2.5V		−50		−180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V				±1	µA

Output Drive Characteristics for CY74FCT16244T, CY74FCT16444T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162244T, CY74FCT162H244T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Note:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Pins with bus hold are described in Pin Description.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[9]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	60	100	µA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.4	4.5[12]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[12]	mA

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16244T CY74FCT162244T CY74FCT16444T CY74FCT162H244T		CY74FCT16244AT CY74FCT162244AT CY74FCT16444AT CY74FCT162H244AT		CY74FCT16244CT CY74FCT162244CT CY74FCT16444CT CY74FCT162H244CT		Unit	Fig. No.[14]
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	6.5	1.5	4.8	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.0	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.0	1.5	5.6	1.5	5.2	ns	1, 7, 8
$t_{SK(O)}$	Output Skew[15]		0.5		0.5		0.5	ns	—

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information CY74FCT16244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16244TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162244TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT16444

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16444CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT16444ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16444TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16444TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H244

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162H244CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244CTPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT162H244ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244ATPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162H244TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H244TPVC	O48	48-Lead (300-Mil) SSOP	

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CY74FCT16245T/2245T
CY74FCT16445T/2H245T

16-Bit Transceiver

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 4.1 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16245T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162245T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C**

CY74FCT16445T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Reduces system loadling**

CY74FCT162H245T Features:

- **Bus hold on data inputs**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

These 16-bit transceivers are designed for use in bidirectional synchronous communication between two buses, where high speed and low power are required. With the exception of the CY74FCT16245T, these devices can be operated either as two independent octals or a single 16-bit transceiver. Direction of data flow is controlled by (DIR), the Output Enable ($\overline{OE}$) transfers data when LOW and isolates the buses when HIGH. The output buffers are designed with power off disable capability to allow for live insertion of boards.

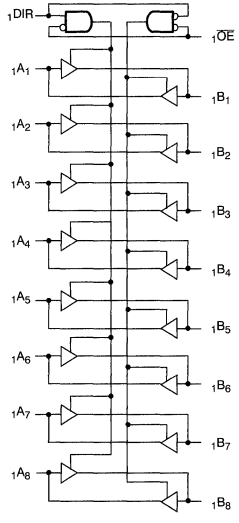
The CY74FCT16245T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162245T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and povides for minimal undershoot and reduced ground bounce. The CY74FCT162245T is ideal for driving transmission lines.

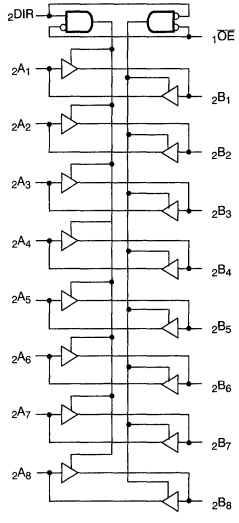
The CY74FCT16445T is designed for 16-bit operation, reducing control lines from two $\overline{OE}$ and two DIR pins to one $\overline{OE}$ and one DIR pin to reduce loading.

The CY74FCT162H245T is a 24-mA balanced output part that has bus hold on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Logic Block Diagrams CY74FCT16245T, CY74FCT162245T, CY74FCT162H245T



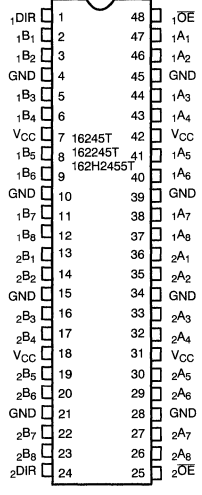
FCT16245-1



FCT16245-2

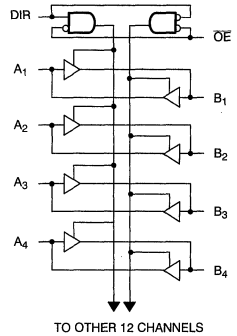
Pin Configuration

SSOP/TSSOP
Top View



FCT16245-3

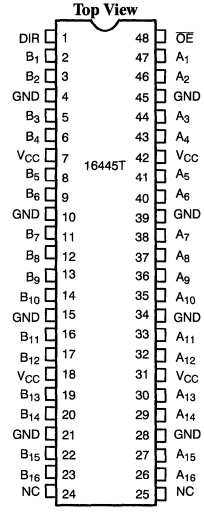
Logic Block Diagram CY74FCT16445T



FCT16245-4

Pin Configuration

SSOP/TSSOP
Top View



FCT16245-5

Pin Description

Name	Description
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
DIR	Direction Control
A	Inputs or Three-State Outputs[1]
B	Inputs or Three-State Outputs[1]

Function Table[2]

Inputs		Outputs
$\overline{OE}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Notes:

1. On CY74FCT162H245T these pins have bus hold.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[6]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[7]		V_{CC}=Min.	V_I=2.0V	−50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[7]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[8]		V_{CC}=Max., V_{OUT}=GND		−80	−140	−200	mA
I_O	Output Drive Current[6]		V_{CC}=Max., V_{OUT}=2.5V		−50		−180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V				±1	µA

Output Drive Characteristics for CY74FCT16245T, CY74FCT16445T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162245T, CY74FCT162H245T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Notes:
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Pins with bus hold are described in Pin Decription.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[9]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=DIR=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	60	100	µA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=DIR=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=DIR=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.4	4.5[12]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	74FCT16245T 74FCT162245T 74FCT16445T 74FCT162H245T		74FCT16245AT 74FCT162245AT 74FCT16445AT 74FCT162H245AT		74FCT16245CT 74FCT162245CT 74FCT16445CT 74FCT162H245CT		Unit	Fig. No.[14]
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output A to B, B to A	1.5	7.0	1.5	4.5	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B	1.5	9.5	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B	1.5	7.5	1.5	5.0	1.5	4.8	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time DIR to A or B	1.5	9.5	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A or B	1.5	7.5	1.5	5.0	1.5	4.8	ns	1, 7, 8
$t_{SK(O)}$	Output Skew[15]		0.5		0.5		0.5	ns	—

Notes:
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

9

Ordering Information CY74FCT16245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16245CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16245CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16245ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16245ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16245TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16245TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162245CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162245CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT162245ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162245ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162245TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162245TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT16445

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16445CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16445CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16445ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16445ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16445TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16445TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162H245CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H245CTPVC	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT162H245ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H245ATPVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162H245TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H245TPVC	O48	48-Lead (300-Mil) SSOP	

Document #: 38–00389

CY74FCT16373T
CY74FCT162373T

16-Bit Latches

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 4.2 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16373T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162373T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

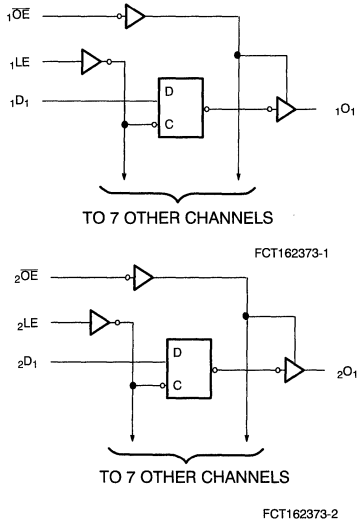
Functional Description

CY74FCT16373T and CY74FCT162373T are 16-bit D-type latches designed for use in bus applications requiring high speed and low power. These devices can be used as two independent 8-bit latches or as a single 16-bit latch by connecting the Output Enable ($\overline{OE}$) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with power-off disable feature that allows llive insertion of boards.

The CY74FCT16373T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

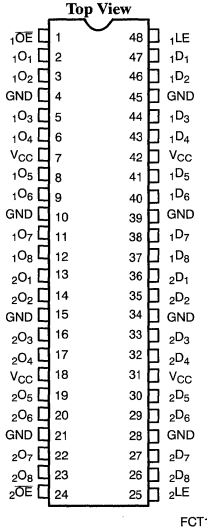
The CY74FCT162373T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162373T is ideal for driving transmission lines.

Logic Block Diagrams



Pin Configuration

SSOP/TSSOP
Top View



FCT162373-3

Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Inputs (Active HIGH)
$\overline{OE}$	Output Enable Inputs (Active LOW)
O	Three-State Outputs

Function Table[1]

Inputs			Outputs
D	LE	$\overline{OE}$	O
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level.
   X = Don't Care. Z = High Impedance.
   Q_0=Previous state of flip-flop.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16373T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162373T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Notes:

2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[7]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	60	100	µA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND, LE=V_{CC}	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND, LE=V_{CC}	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.4	4.5[10]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[10]	mA

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16373T CY74FCT162373T		CY74FCT16373AT CY74FCT162373AT		CY74FCT16373CT CY74FCT162373CT		Unit	Fig. No.[12]
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	8.0	1.5	5.2	1.5	4.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	13.0	2.0	6.7	2.0	5.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	12.0	1.5	6.1	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	5.5	1.5	5.0	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to LE	2.0		2.0		2.0		ns	9
t_H	Hold Time HIGH or LOW, D to LE	1.5		1.5		1.5		ns	9
t_W	LE Pulse Width HIGH	6.0		3.3		3.3		ns	5
$t_{SK(O)}$	Output Skew[13]		0.5		0.5		0.5	ns	—

Ordering Information CY74FCT16373

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16373CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16373CTPVC	O48	48-Lead (300-Mil) SSOP	
5.2	CY74FCT16373ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16373ATPVC	O48	48-Lead (300-Mil) SSOP	
8.0	CY74FCT16373TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16373TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162373

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT162373CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162373CTPVC	O48	48-Lead (300-Mil) SSOP	
5.2	CY74FCT162373ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162373ATPVC	O48	48-Lead (300-Mil) SSOP	
8.0	CY74FCT162373TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162373TPVC	O48	48-Lead (300-Mil) SSOP	

Notes:
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information Section.
13. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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CY74FCT16374T
CY74FCT162374T

16-Bit Registers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.2 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16374T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162374T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

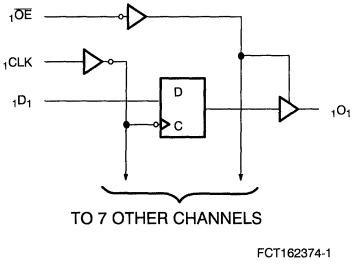
Functional Description

CY74FCT16374T and CY74FCT162374T are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be usedas two independent 8-bit registers or as a signle 16-bit register by connecting the output Enable (OE) and Clock (CLK) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with power-off disable feature that allows live insertion of boards.

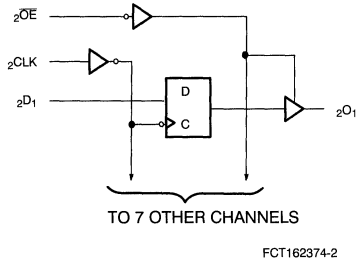
The CY74FCT16374T is ideally suited for driving high capacitance loads and low-impedance backplanes.

The CY74FCT162374T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162374T is ideal for driving transmission lines.

Logic Block Diagrams



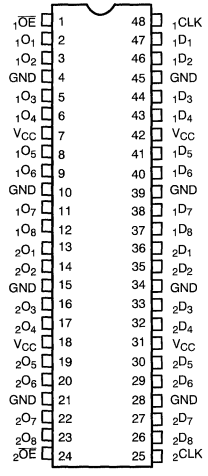
FCT162374-1



FCT162374-2

Pin Configuration

SSOP/TSSOP
Top View



FCT162374-3

Function Table[1]

Inputs			Outputs	
D	CLK	$\overline{OE}$	O	Function
X	L	H	Z	High-Z
X	H	H	Z	
L	⌐	L	L	Load Register
H	⌐	L	H	
L	⌐	H	Z	
H	⌐	H	Z	

Pin Description

Name	Description
D	Data Inputs
CLK	Clock Inputs
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ⌐ = LOW-to-HIGH Transition.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Output Drive Characteristics for CY74FCT16374T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162374T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[7]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	60	100	μA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., f_0=10 MHz, f_1=5 MHz 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	1.1	3.0	mA
		V_{CC}=Max., f_0=10 MHz,, f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	3.0	5.5[10]	mA
			V_{IN}=3.4V or V_{IN}=GND	7.5	19.0[10]	mA

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT16374T CY74FCT162374T		CY74FCT16374AT CY74FCT162374AT		CY74FCT16374CT CY74FCT162374CT		Unit	Fig. No.[12]
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CLK to O	2.0	10.0	2.0	6.5	2.0	5.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	12.5	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	5.5	1.5	5.0	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW, D to CLK	1.5		1.5		1.5		ns	4
t_W	CLK Pulse Width HIGH or LOW	5.0		5.0		3.3		ns	5
$t_{SK(O)}$	Output Skew[13]		0.5		0.5		0.5	ns	

Ordering Information CY74FCT16374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT16374CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374CTPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16374ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374ATPVC	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT16374TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374TPVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT162374CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374CTPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162374ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374ATPVC	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT162374TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374TPVC	O48	48-Lead (300-Mil) SSOP	

Notes:
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information Section.
13. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38–00391

CY74FCT16500T
CY74FCT162500T

18-Bit Registered Transceivers

Features

- **Low power, pin compatible replacement for ABT functions**
- **FCT-C speed at 4.6 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16500T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162500T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

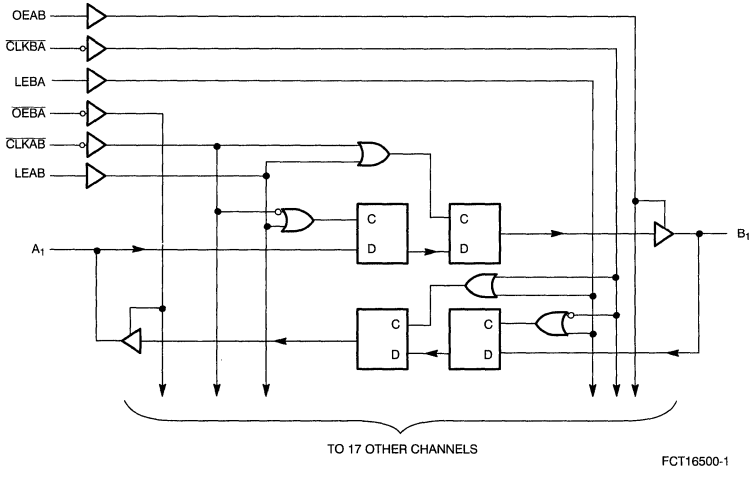
Functional Description

These 18-bit universal bus transceivers can be operated in transparent, latched, or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and $\overline{\text{LEBA}}$), and clock inputs ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{\text{CLKAB}}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{\text{CLKAB}}$. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output buffers are designed with power-off disable feature that allows live insertion of boards.

The CY74FCT16500T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

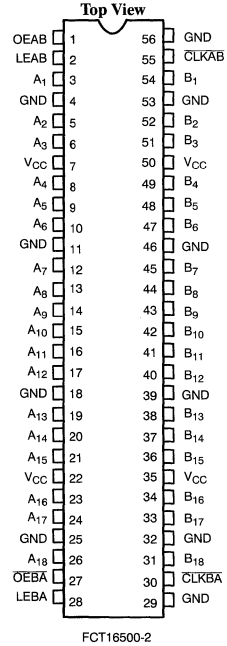
The CY74FCT162500T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162500T is ideal for driving transmission lines.

Logic Block Diagram



Pin Configuration

SSOP/TSSOP
Top View



FCT16500-2

Pin Summary

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1, 2]

Inputs				Outputs
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B[3]
H	L	L	X	B[4]

Maximum Ratings[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[8]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND.			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[9]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ↓ = HIGH-to-LOW Transition.
2. A-to-B data flow is shown, B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
5. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
6. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Output Drive Characteristics for CY74FCT16500T

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162500T

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[8] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN}\le$0.2V, $V_{IN}\ge V_{CC}$−0.2V	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[10]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEAB}$=$\overline{OEBA}$=V_{CC} or GND	V_{IN}=V_{CC} or V_{IN}=GND	75	120	µA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz ($\overline{CLKAB}$), f_1=5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OEAB}$=$\overline{OEBA}$=V_{CC} LEAB=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	1.3	3.2	mA
		V_{CC}=Max., f_0=10 MHz, f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, $\overline{OEAB}$=$\overline{OEBA}$=V_{CC} LEAB=GND	V_{IN}=V_{CC} or V_{IN}=GND	3.8	6.5[13]	mA
			V_{IN}=3.4V or V_{IN}=GND	8.5	20.8[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_i N_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description		CY74FCT16500AT/ CY74FCT162500AT Min.[14]	CY74FCT16500AT/ CY74FCT162500AT Max.	CY74FCT16500CT/ CY74FCT162500CT Min.[14]	CY74FCT16500CT/ CY74FCT162500CT Max.	Unit	Fig. No.[15]
f_{MAX}	$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency			150		150	MHz	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	5.1	1.5	4.6	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.6	1.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLKBA}$ to A, $\overline{CLKAB}$ to B		1.5	5.6	1.5	5.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to A, OEAB to B		1.5	6.0	1.5	5.4	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to A, OEAB to B		1.5	5.6	1.5	5.2	ns	1, 7, 8
t_{SU}	Set-Up Time, HIGH or LOW A to $\overline{CLKAB}$, B to $\overline{CLKBA}$		3.0		3.0		ns	9
t_H	Hold Time, HIGH or LOW A to $\overline{CLKAB}$, B to $\overline{CLKBA}$		0		0		ns	9
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0		ns	4
		Clock LOW	1.5		1.5		ns	4
t_H	Hold Time, HIGH or LOW A to LEAB, B to LEBA		1.5		1.5		ns	4
t_W	LEAB or LEBA Pulse Width HIGH		3.0		2.5		ns	5
t_W	$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW		3.0		3.0		ns	5
$t_{SK(O)}$	Output Skew[16]			0.5		0.5	ns	

Ordering Information CY74FCT16500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16500CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16500CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16500ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16500ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162500CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162500CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162500ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162500ATPVC	O56	56-Lead (300-Mil) SSOP	

Notes:
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.
16. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38–00381

CY74FCT16501T
CY74FCT162501T
CY74FCT162H501T

18-Bit Registered Transceivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 4.6 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6 mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16501T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162501T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

CY74FCT162H501T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

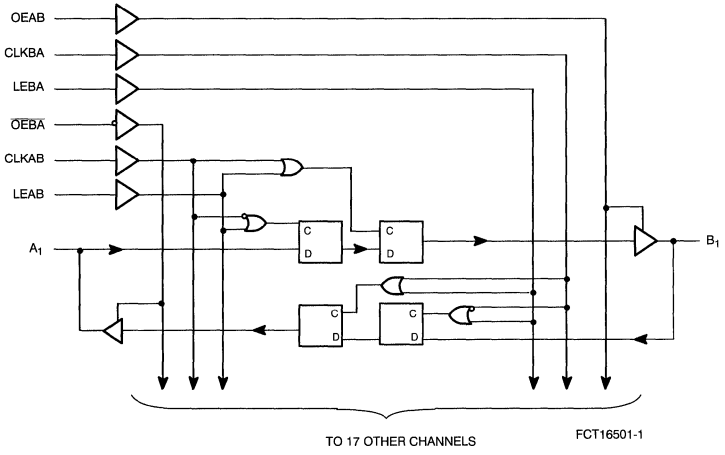
These 18-bit universal bus transceivers can be operated in transparent, latched or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock inputs (CLKAB and CLKBA). For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by $\overline{OEBA}$, LEBA, and CLKBA. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

The CY74FCT16501T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

THE CY74FCT162501T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162501T is ideal for driving transmission lines.

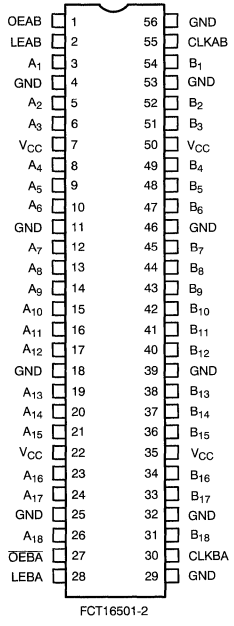
The CY74FCT162H501T is a 24-mA balanced output part, that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Functional Block Diagram



Pin Configuration

SSOP/TSSOP
Top View



9

Pin Description

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[1]

Function Table[2, 3]

Inputs				Outputs
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	⌐	L	L
H	L	⌐	H	H
H	L	L	X	B[4]
H	L	H	X	B[5]

Maximum Ratings[6, 7]

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Notes:

1. On the 74FCT162H501T these pins have bus hold.
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ⌐ = LOW-to-HIGH Transition
4. Output level before the indicated steady-state input conditions were established.
5. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
6. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
7. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[9]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[10]		V_{CC}=Min.,	V_I=2.0V	−50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[7]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[11]		V_{CC}=Max., V_{OUT}=GND		−80	−140	−200	mA
I_O	Output Drive Current[11]		V_{CC}=Max., V_{OUT}=2.5V		−50		−180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V				±1	µA

Output Drive Characteristics for CY74FCT16501T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162501T, CY74FCT162H501T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
I_{ODL}	Output LOW Current[11]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[11]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[9] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[8]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:
8. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
9. This parameter is guaranteed but not tested.
10. Pins with bus hold are described in Pin Description.
11. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Sym.	Parameter	Test Conditions[12]		Min.	Typ.[8]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current TTL inputs HIGH	V_{CC}= Max., V_{IN} = 3.4V[13]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[14]	V_{CC}=Max., Outputs Open OEAB=$\overline{OEBA}$=V_{CC} or GND One Input Toggling, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[15]	V_{CC}=Max., Outputs Open f_0 =10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB = GND, One Bit Toggling f_1 = 5MHz, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max., Outputs Open f_0 = 10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB=GND Eighteen Bits Toggling f_1=2.5MHz, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.8	6.5 [16]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.5	20.8[16]	

Notes:

12. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
13. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply.
15. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description		74FCT16501AT 74FCT162501AT 74FCT162H501AT		74FCT16501CT 74FCT162501CT 74FCT162H501CT		Unit	Fig. No.[17]
			Min.[18]	Max.	Min.[18]	Max.		
f_{MAX}	CLKAB or CLKBA frequency[19]		—	150	—	150	MHz	—
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	5.1	1.5	4.6	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.6	1.5	5.3	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay CLKBA to A, CLKAB to B		1.5	5.6	1.5	5.3	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to A, $\overline{OEAB}$ to B		1.5	6.0	1.5	5.6	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to A, $\overline{OEAB}$ to B		1.5	5.6	1.5	5.2	ns	1,7,8
t_{SU}	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA		3.0	—	3.0	—	ns	4
t_H	Hold Time HIGH or LOW A to CLKAB, B to CLKBA		0	—	0	—	ns	4
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock LOW	3.0	—	3.0	—	ns	4
		Clock HIGH	1.5	—	1.5	—	ns	4
t_H	Hold Time, HIGH or LOW, A to LEAB, B to LEBA		1.5	—	1.5	—	ns	4
t_W	LEAB or LEBA Pulse Width HIGH[19]		3.0	—	3.0	—	ns	5
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[19]		3.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew[20]		—	0.5	—	0.5	ns	—

Notes:
17. See "Parameter Measurement Information" in the General Information Section.
18. Minimum limits are guaranteed, but not tested, on propagation delays.
19. This parameter is guaranteed but not tested.
20. Skew between any two outputs of the same package switching in the same direction. This parameter guaranteed by design.

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Ordering Information CY74FCT16501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16501ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162501ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162H501CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162H501ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H501ATPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38−00382

CY74FCT16543T
CY74FCT162543T

16-Bit Latched Transceivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.1 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16543T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162543T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C**

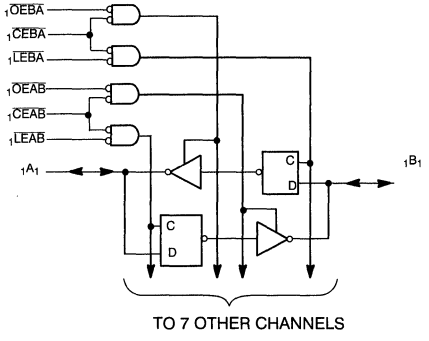
Functional Description

The CY74FCT16543T and CY74FCT162543T are 16-bit, high-speed, low power latched transceivers that are organized as two independent 8-bit D-type latched transceivers containing twosets of eight D-type latches with separate Latch Enable ($\overline{LEAB}$, $\overline{LEAB}$) and Output Enabe ($\overline{OEAB}$, $\overline{OEAB}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B input Enable ($\overline{CEAB}$) must be LOW in order to enter data from A or to take data from B as indicated in the truth table. With $\overline{CAEB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) makes the A-to-B latchestransparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs flow-through pinout and small shrink packaging and in simplifying board design. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

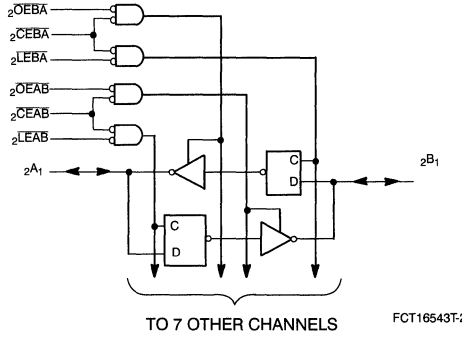
The CY74FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162543T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162543T is ideal for driving transmission lines.

Logic Block Diagrams



FCT16543T-1

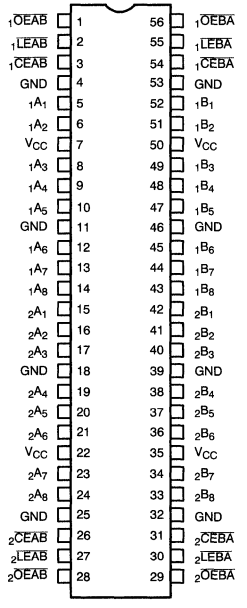


FCT16543T-2

Pin Configuration

Top View

SSOP/TSSOP



FCT16543T-3

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1]

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs[2]

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Ambient Temperature with
Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

Static Discharge Voltage ..... >2001V
(per MIL-STD-883, Method 3015)

Notes:

1. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, LEBA, and $\overline{OEBA}$.
2. Data prior to $\overline{LEAB}$ LOW-to-HIGH Transition.
   H = HIGH Voltage Level. L = LOW Voltage Level.
   X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16543T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162543T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[7] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[8]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. This parameter is guaranteed but not tested.
8. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[8]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[9]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	60	100	µA/ MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.4	4.5[12]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	Conditions[13]	74FCT16543T 74FCT162543T		74FCT16543AT 74FCT162543AT		74FCT16543CT 74FCT162543CT		Unit	Fig. No.[15]
			Min.[14]	Max.	Min.[14]	Max.	Min.[14]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	C_L=50pF R_L=500Ω	1.5	8.5	1.5	6.5	1.5	5.1	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B		1.5	12.5	1.5	8.0	1.5	5.6	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B		1.5	12.0	1.5	9.0	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B		1.5	9.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{SU}	Set-up Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$		2.0	—	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$		2.0	—	2.0	—	2.0	—	ns	4
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		4.0	—	4.0	—	4.0	—	ns	5
$t_{SK(O)}$	Output Skew[16]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
13. See test circuits and waveforms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.
16. Skew between any two outputs of the same package switching in the same directional. This parameter is guaranteed by design.

9

Ordering Information CY74FCT16543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT16543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT16543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT16543TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543TPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT162543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT162543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT162543TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543TPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38−00388

CY74FCT16646T
CY74FCT162646T

16-Bit Registered Transceivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.4 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16646T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162646T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

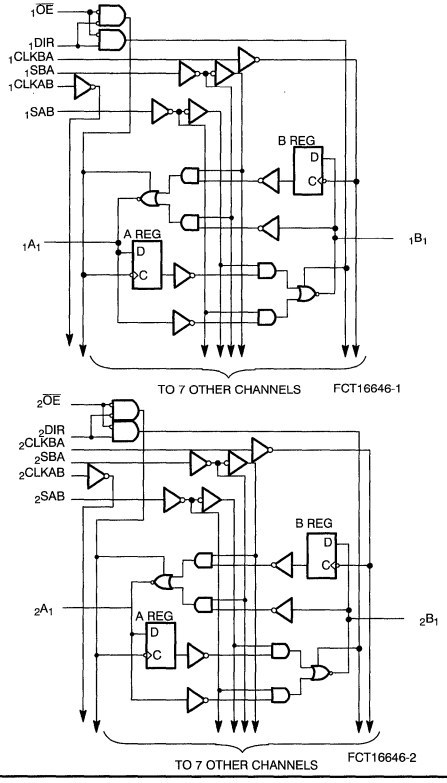
Functional Description

The CY74FCT16646T and CY74FCT162646T 16-bit transceivers are three-state, D-type registers, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Output Enable ($\overline{OE}$) and direction pins (DIR) are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the Output Enable ($\overline{OE}$) is Active LOW. In the isolation mode (Output Enable ($\overline{OE}$) HIGH), A data may be stored in the B register and/or B data may be stored in the A register. The output buffers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16646T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

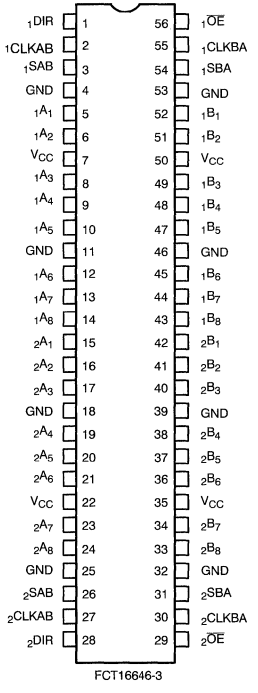
The CY74FCT162646T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162646T is ideal for driving transmission lines.

Logic Block Diagrams



Pin Configuration

SSOP/TSSOP
Top View



FCT16646-3

9

Pin Description

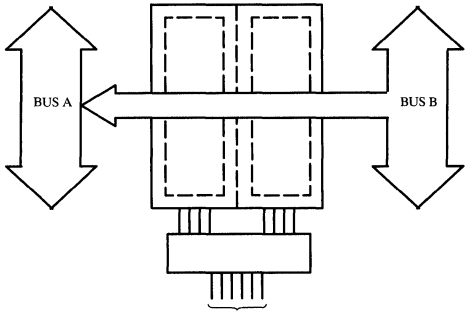
Pin Names	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR	Direction
$\overline{OE}$	Output Enable (Active LOW)

Function Table[1]

Inputs						Data I/O[2]		Function
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A	B	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

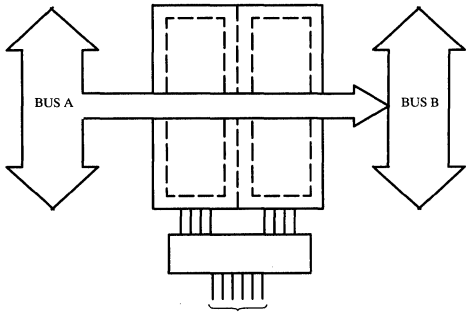
Notes:

1. H = High Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ⌐ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.



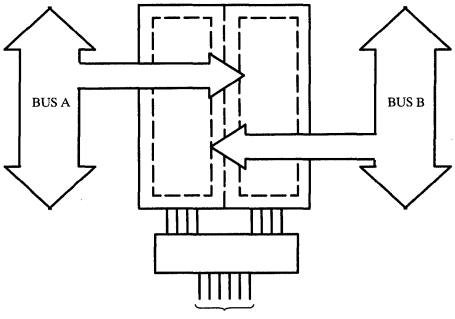
DIR	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



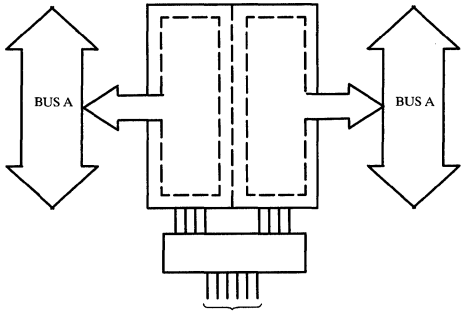
DIR	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



DIR	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
H	L	⌐	X	X	X
L	L	X	⌐	X	X
X	H	⌐	⌐	X	X

Storage from
A and/or B



DIR[3]	$\overline{OE}$	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data
to A and/or B

Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Notes:

3. Cannot transfer data to A-bus and B-bus simultaneously.
4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	μA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	μA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	μA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	μA
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[7]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	μA

Output Drive Characteristics for CY74FCT16646T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162646T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Description[8]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} =0V	5.5	8.0	pF

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Parameter	Description	Test Conditions[9]		Min.	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN}=3.4V[10]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max. Outputs Open DIR=OE=GND One-Bit Toggling 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND One-Bit Toggling f_1=5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND Sixteen-Bits Toggling f_1=2.5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.8	6.5[13]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.3	20.0[13]	

Notes:

9. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range

Parameter	Description	Cond.	74FCT16646T 74FCT162646T		74FCT16646AT 74FCT162646AT		74FCT16646CT 74FCT162646CT		Unit	Fig. No.[14]
			Min.[15]	Max.	Min.[15]	Max.	Min.[15]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time DIR or $\overline{OE}$ to Bus		1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time DIR or $\overline{OE}$ to Bus		1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		1.5	11.0	1.5	7.7	1.5	6.2	ns	1,5
t_{SU}	Set-Up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	5.0	—	ns	6
$t_{SK(O)}$	Output Skew[16]		—	0.5	—	0.5	—	0.5	ns	—

Ordering Information CY74FCT16646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16646CTPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646CTPVC	O56	48-Lead (300-Mil) SSOP	
6.3	CY74FCT16646ATPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646ATPVC	O56	48-Lead (300-Mil) SSOP	
9.0	CY74FCT16646TPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646TPVC	O56	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT162646CTPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646CTPVC	O56	48-Lead (300-Mil) SSOP	
6.3	CY74FCT162646ATPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646ATPVC	O56	48-Lead (300-Mil) SSOP	
9.0	CY74FCT162646TPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646TPVC	O56	48-Lead (300-Mil) SSOP	

Notes:

14. See "Parameter Measurement Information" in the General Information Section.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. Skew any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38−00383

CY74FCT16652T
CY74FCT162652T

16-Bit Registered Transceivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.4 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16652T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162652T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

Functional Description

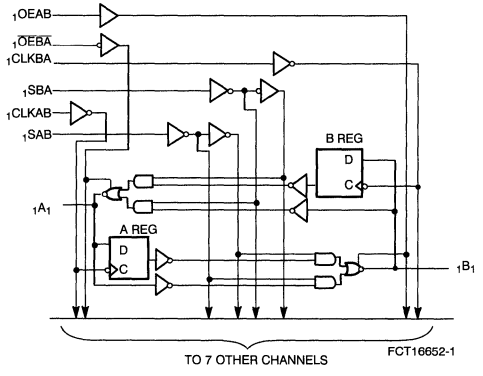
These16-bit, high-speed, low-power, registered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and $\overline{OEBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

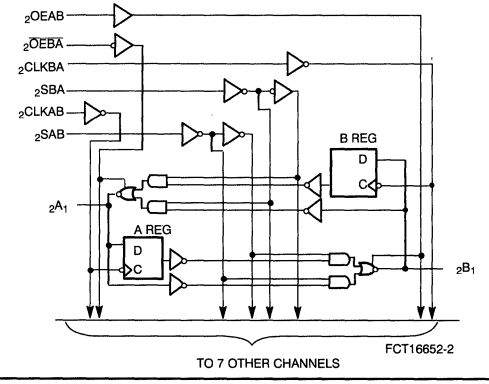
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. The output buffers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal underhsoot and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.

Logic Block Diagrams

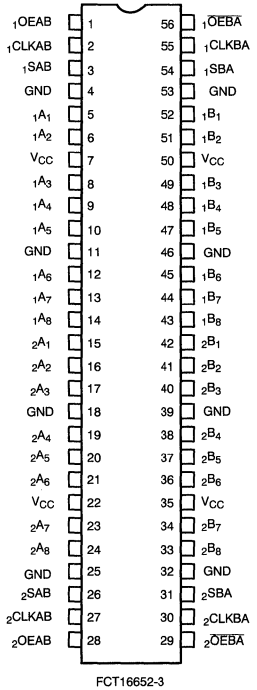




Pin Configuration

SSOP/TSSOP

Top View



FCT16652-3

9

Pin Description

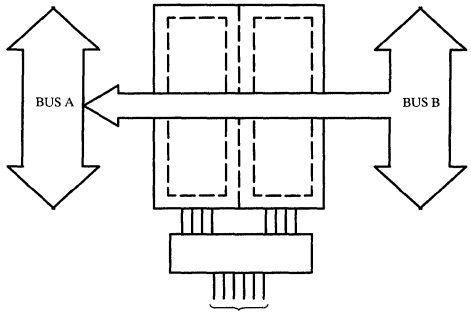
Name	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Function Table[1]

Inputs						Data I/O[2]		
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A	B	Operation or Function
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	⌐	⌐	X	X			Store A and B Data
X	H	⌐	H or L	X	X	Input	Unspecified[2]	Store A, Hold B
H	H	⌐	⌐	X[3]	X	Input	Output	Store A in Both Registers
L	X	H or L	⌐	X	X	Unspecified[2]	Input	Hold A, Store B
L	L	⌐	⌐	X	X[3]		Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and
								Stored B Data to A Bus

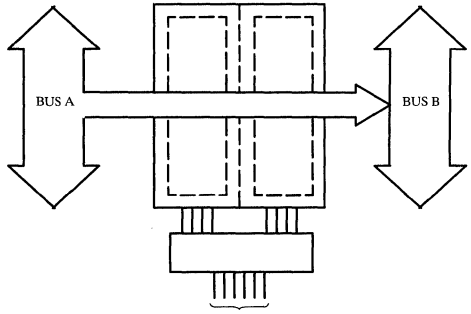
Notes:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ⌐ =LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Select control=L; clocks can occur simultaneously.
   Select control=H; clocks must be staggered to load both registers.



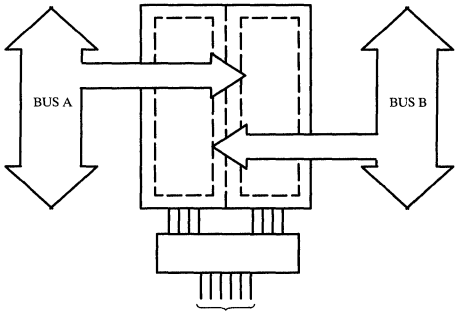
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



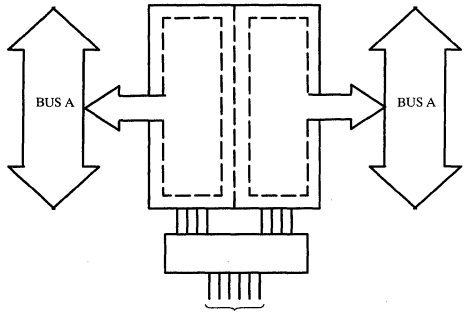
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↓	X	X	X
L	X	X	↓	X	X
L	H	↓	↓	X	X

Storage from
A and/or B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

Transfer Stored Data
to A and/or B

Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with
Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V
(per MIL-STD-883, Method 3015)

Note:

4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V_H	Input Hysteresis			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current[7]	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current[7]	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output[7] Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output[7] Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current	V_{CC}=Max., V_{OUT}=GND[8]	−80	−140	−200	mA
I_O	Output Drive Current	V_{CC}=Max., V_{OUT}=2.5V[8]	−50		−180	mA
I_{OFF}	Power-Off Disable[7]	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16652T

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA[9]	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162652T

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V[8]	60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V[8]	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance (T_A = +25°C, f = 1.0 MHz)

Parameter	Description[10]	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:
5. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{CC}=5.0V, +25°C ambient.
7. The test limit for this parameter is +5mA at T_A=−55°C.
8. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
9. Duration of the condition cannot exceed one second.
10. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Param.	Description	Test Conditions[11]		Min.	Typ.[12]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	—	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN}=3.4V[13]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[14]	V_{CC}=Max. Outputs Open $\overline{OEAB}$=$\overline{OEBA}$=GND One Input Toggling 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	μA/ MHz
I_C	Total Power Supply Current[15]	V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle $\overline{OEAB}$=$\overline{OEBA}$=GND One-Bit Toggling f_1=5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle $\overline{OEAB}$=$\overline{OEBA}$=GND Sixteen Bits Toggling f_1=2.5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.8	6.5[16]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.3	20.0[16]	

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Typical values are at V_{CC}=5.0V +25° ambient.
13. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range

Parameter	Description	Cond.[17]	74FCT16652T 74FCT162652T		74FCT16652AT 74FCT162652AT		74FCT16652CT 74FCT162652CT		Unit	Fig. No.[18]
			Min.[19]	Max.	Min.[19]	Max.	Min.[19]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 3
t_{PZH} t_{PHL}	Output Enable Time OEAB or $\overline{OEBA}$ to Bus		1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEAB or $\overline{OEBA}$ to Bus		1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		1.5	11.0	1.5	7.7	1.5	6.2	ns	1, 5
t_{SU}	Set-Up time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	5.0	—	ns	5
$t_{SK(O)}$	Output Skew[20]		—	0.5	—	0.5	—	0.5	ns	

Notes:

17. See test circuits and waveforms.
18. See "Parameter Measurement Information" in the General Information Section.
19. Minimum limits are guaranteed, but not tested, on propagation delays.
20. Skew between any two outputs of the same package switching in the same direction. This parameter guaranteed by design.

Ordering Information CY74FCT16652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16652CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16652CTPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT16652ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16652ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT16652TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16652TPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT162652CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162652CTPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT162652ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162652ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT162652TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162652TPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38−00384

CY74FCT16823T
CY74FCT162823T

18-Bit Registers

Features

- **Low power, pin compatible replacement for ABT functions**
- **FCT-C speed at 6.0 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16823T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162823T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

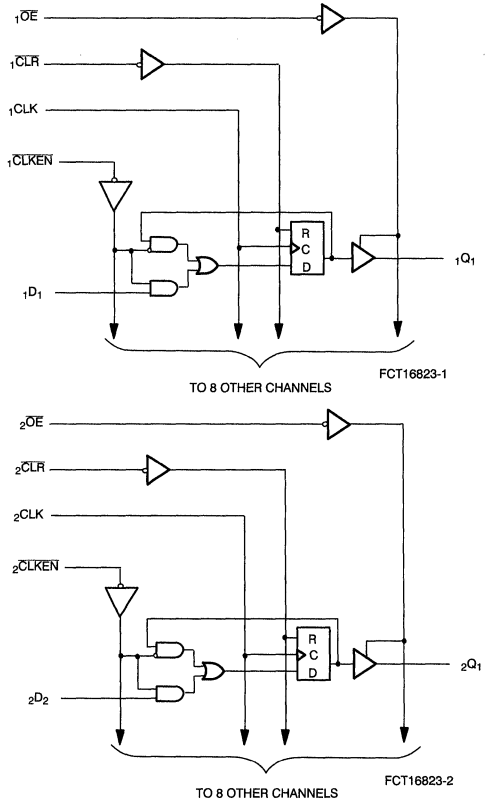
Functional Description

The CY74FCT16823T and the CY74FCT162823T 18-bit bus interface register are designed for use in high-speed, low-power systems needing wide registers and parity. 18-bit operation is achieved by connecting the control lines of the two 9-bit registers. Flow-through pinout and small shrink packaging aids in simplifying board layout. The outputs are designed with a power-off disable feature to allow live insertion of boards.

The CY74FCT16823T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162823T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and redced ground bounce. The CY74FCT162823T is ideal for driving transmission lines.

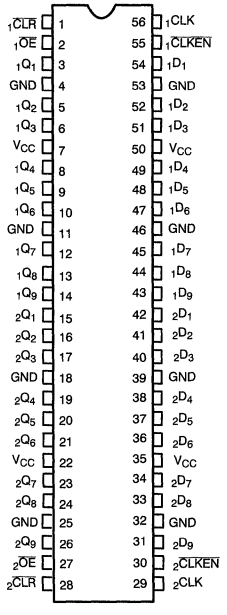
Logic Block Diagrams



Pin Configuration

SSOP/TSSOP

Top View



FCT16823-3

Pin Description

Name	Description
D	Data Inputs
CLK	Clock Inputs
$\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$\overline{CLR}$	Asynchronous Clear Inputs (Active LOW)
$\overline{OE}$	Output Enable Inputs (Active LOW)
Q	Three-State Outputs

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   Z = HIGH Impedance.
   ⌐ = LOW-to-HIGH transition.
2. Output level before indicated steady-state input conditions were established.

Function Table[1]

Inputs						Outputs
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q[2]	Hold
H	H	L	⌐	L	Z	Load
H	H	L	⌐	H	Z	
L	H	L	⌐	L	L	
L	H	L	⌐	H	H	

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

9

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			1	µA

Output Drive Characteristics for CY74FCT16823T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162823T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
I_{ODL}	Output LOW Voltage[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Voltage[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[7] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[8]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

5. This input is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. This parameter is guaranteed but not tested.
8. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

Power Supply Characteristics

Parameter	Description	Test Conditions[9]		Min.	Typ.[8]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[10]	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=$\overline{CLKEN}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=$\overline{CLKEN}$=GND at f_1=5 MHz	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max., at f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, $\overline{OE}$=$\overline{CLKEN}$=GND f_0=10 MHz	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	4.2	7.1[13]	
			V_{IN}=3.4V or V_{IN}=GND	—	9.2	22.1[13]	

Notes:

9. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range

Parameter	Description	Condition[14]	74FCT16823AT 74FCT162823AT		74FCT16823BT 74FCT162823BT		74FCT16823CT 74FCT162823CT		Unit	Fig. No.[16]
			Min.[15]	Max.	Min.[15]	Max.	Min.[15]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CLK to Q	C_L=50 pF R_L=500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns	1, 5
		C_L=300 pF[17] R_L=500Ω	1.5	20.0	1.5	15.0	1.5	12.5		
t_{PHL}	Propagation Delay $\overline{CLR}$ to Q	C_L=50 pF R_L=500Ω	1.5	14.0	1.5	9.0	1.5	6.1	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Q	C_L=50 pF R_L=500Ω	1.5	12.0	1.5	8.0	1.5	5.5	ns	1, 7, 8
		C_L=300 pF[17] R_L=500Ω	1.5	23.0	1.5	15.0	1.5	12.5		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q	C_L=5 pF[17] R_L=500Ω	1.5	7.0	1.5	6.5	1.5	5.2	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	8.0	1.5	7.5	1.5	6.5		
t_{SU}	Set-Up Time HIGH or LOW D to CLK	C_L=50 pF R_L=500Ω	3.0	—	3.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW D to CLK		1.5	—	1.5	—	1.5	—	ns	4
t_{SU}	Set-Up Time HIGH or LOW $\overline{CLKEN}$ to CLK		3.0	—	3.0	—	3.0	—	ns	9
t_H	Hold Time HIGH or LOW $\overline{CLKEN}$ to CLK		0	—	0	—	0	—	ns	9
t_W	CLK Pulse Width HIGH or LOW		6.0	—	6.0	—	3.3	—	ns	5
t_W	$\overline{CLR}$ Pulse Width LOW		6.0	—	6.0	—	3.3	—	ns	5
t_{REM}	Recovery Time $\overline{CLR}$ to CLK		6.0	—	6.0	—	6.0	—	ns	6
$t_{SK(O)}$	Output Skew[18]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
14. See test circuit and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. See "Parameter Measurement Information" in the General Information Section.
17. These limits are guaranteed but not tested.
18. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information CY74FCT16823

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY74FCT16823CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16823CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT16823BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16823BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT16823ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16823ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162823

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY74FCT162823CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162823CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162823ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162823ATPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162823TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162823TPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38–00385

CY74FCT16827T
CY74FCT162827T

20-Bit Buffers

Features

- **Low power, pin compatible replacement for ABT functions**
- **FCT-C speed at 4.2 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16827T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162827T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C**

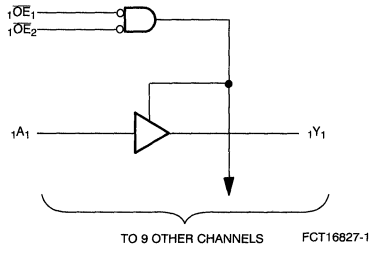
Functional Description

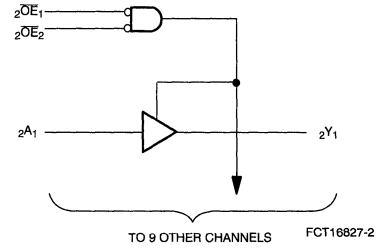
The CY74FCT16827T 20-bit buffer/line driver and the CY74FCT162827T 20-bit buffer/line driver provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. These parts can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed $\overline{OE}$ for increased flexibility. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16827T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162827T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162827T is ideal for driving transmission lines.

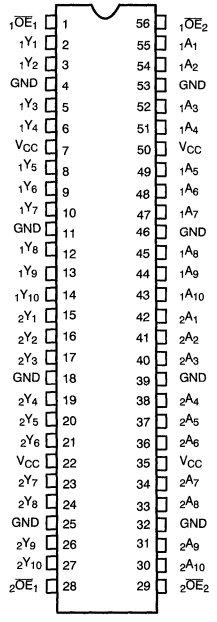
Logic Block Diagrams





Pin Configuration

SSOP/TSSOP
Top View



FCT16827-3

Pin Description

Name	Description
$\overline{OE}$	Output Enable Inputs (Active LOW)
A	Data Inputs
Y	Three-State Outputs

Function Table[1]

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   Z = HIGH Impedance.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

9

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162827T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[7]	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE_1}=\overline{OE_2}$=GND,	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE_1}=\overline{OE_2}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	—	0.9	2.3	
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, $\overline{OE_1}=\overline{OE_2}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.0	5.5[10]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.0	20.5[10]	

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_i N_i)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_i = Input signal frequency
   N_i = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Switching Characteristics Over the Operating Range

Parameter	Description	Condition[11]	74FCT16827AT 74FCT162827AT		74FCT16827BT 74FCT162827BT		74FCT16827CT 74FCT162827CT		Unit	Fig. No.[13]
			Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to Y	C_L=50 pF R_L=500Ω	1.5	8.0	1.5	5.0	1.5	4.2	ns	1, 3
		C_L=300 pF[3] R_L=500Ω	1.5	15.0	1.5	13.0	1.5	10.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	12.0	1.5	8.0	1.5	5.6	ns	1, 7, 8
		C_L=300 pF[3] R_L=500Ω	1.5	23.0	1.5	15.0	1.5	14.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y	C_L=5 pF[3] R_L=500Ω	1.5	9.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	10.0	1.5	7.0	1.5	6.0		
$t_{SK(O)}$	Output Skew[14]		—	0.5	—	0.5	—	0.5	ns	—

Ordering Information CY74FCT16827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16827CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827CTPVC	O56	56-Lead (300-Mil) SSOP	
5.0	CY74FCT16827BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827BTPVC	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT16827ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT162827CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827CTPVC	O56	56-Lead (300-Mil) SSOP	
5.0	CY74FCT162827BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827BTPVC	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT162827ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827ATPVC	O56	56-Lead (300-Mil) SSOP	

Notes:
11. See test circuit and waveforms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Document #: 38−00393

CY74FCT16841T
CY74FCT162841T

20-Bit Latches

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.5 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16841T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162841T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

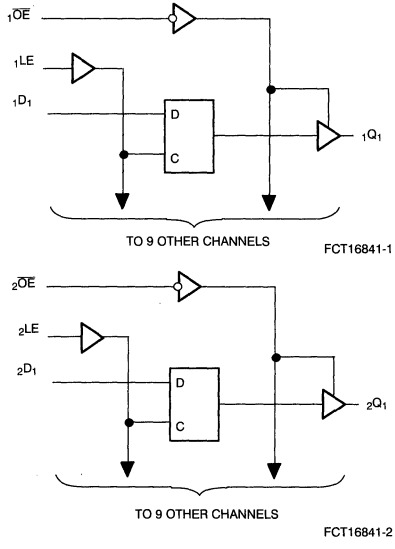
Functional Description

The CY74FCT16841T and CY74FCT162841T are 20-bit D-type latches deisgned for use in bus applications requiring high speed and low power. These devices can be used as two independent 10-bit latches, or as a single 10-bit latch, or as a single 20-bit latch by connecting the Output Enable ($\overline{OE}$) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

The CY74FCT16841T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162841T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162841T is ideal for driving transmission lines.

Logic Block Diagrams

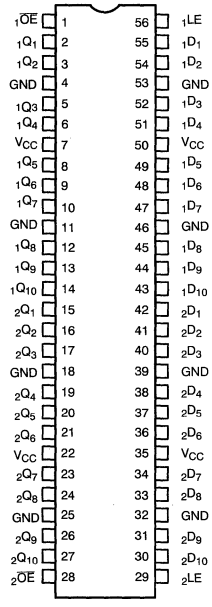


FCT16841-1

FCT16841-2

Pin Configuration

SSOP/TSSOP
Top View



FCT16841-3

Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O	Three-State Outputs

Function Table[1]

Inputs			Outputs
D	LE	$\overline{OE}$	Q
H	H	L	H
L	H	L	L
X	L	L	Q[2]
X	X	H	Z

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[7]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   Z = HIGH Impedance.
2. Output level before LE HIGH-to-LOW Transition.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Output Drive Characteristics for CY74FCT16841T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162841T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Symbol	Description	Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V V_{IN}≥V_{CC}−0.2V	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.,	V_{IN}=3.4V[8]	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	—	60	100	µA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND LE = V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	—	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	—	0.9	2.3	
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, $\overline{OE}$=GND LE = V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	—	3.0	5.5[11]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.0	20.5[11]	

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C=I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC}=Quiescent Current with CMOS input levels
    ΔI_{CC}=Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H =Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 =Clock frequency for registered devices, otherwise zero
    f_1 =Input signal frequency
    N_1 =Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	Condition[12]	74FCT16841AT 74FCT162841AT		74FCT16841BT 74FCT162841BT		74FCT16841CT 74FCT162841CT		Unit	Fig. No.[14]
			Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Q (LE=HIGH)	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns	1, 5
		C_L=300 pF[15] R_L=500Ω	1.5	13.0	1.5	13.0	1.5	13.0		
t_{PLH} t_{PHL}	Propagation Delay LE to Q	C_L=50 pF R_L=500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns	1, 5
		C_L=300 pF[15] R_L=500Ω	1.5	16.0	1.5	15.5	1.5	15.0		
t_{PHZ} t_{PZL}	Output Enable Time $\overline{OE}$ to Q	C_L=50 pF R_L=500Ω	1.5	11.5	1.5	8.0	1.5	6.5	ns	1, 7, 8
		C_L=300 pF[15] R_L=500Ω	1.5	23.0	1.5	14.0	1.5	12.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q	C_L=5 pF[15] R_L=500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	8.0	1.5	7.0	1.5	6.0		
t_{SU}	Set-Up Time HIGH or LOW, D to LE	C_L=50 pF R_L=500Ω	2.5	—	2.5	—	2.0	—	ns	9
t_H	Hold Time HIGH or LOW, D to LE		2.5	—	2.5	—	1.5	—	ns	9
t_W	LE Pulse Width HIGH		4.0[16]	—	4.0[16]	—	4.0[16]	—	ns	5
$t_{SK(O)}$	Output Skew[17]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
12. See test circuit and waveform.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.
15. These conditions are guaranteed but not tested.
16. These limits are guaranteed but not tested.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information for CY74FCT16841T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT16841CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16841CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT16841ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16841ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT16841TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16841TPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162841T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT162841CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162841CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT162841ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162841ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT162841TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162841TPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38−00387

CY74FCT16952T
CY74FCT162952T
CY74FCT162H952T

16-Bit Registered Transceivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 6.3 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16952T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162952T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25°C**

CY74FCT162H952T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

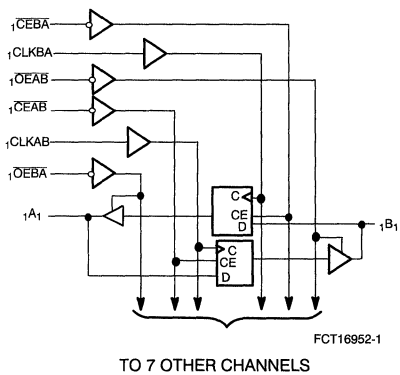
These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B, $\overline{CEAB}$ must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when $\overline{OEAB}$ is LOW. Control of data from B-to-A is similar and is controlled by using the $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$ inputs. The output buffers are designed with a power-off disable feature to allow for live insertion of boards.

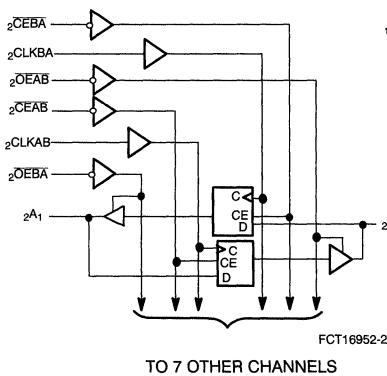
The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

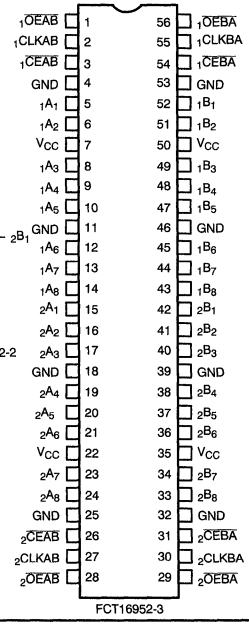
Logic Block Diagrams





Pin Configuration

SSOP/TSSOP
Top View



FCT16952-3

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[1]

Function Table[2, 3]

For A-to-B (Symmetric with B-to-A)

Inputs				Outputs
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B[4]
X	L	L	X	B[4]
L	⌐	L	L	L
L	⌐	L	H	H
X	X	H	X	Z

Maximum Ratings[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Notes:

1. On the CY74FCT162H952T these pins have bus hold.
2. A-to-B data flow is shown: B-to-A data flow is similar but uses, $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
3. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   ⌐ = LOW-to-HIGH Transition.
   Z = HIGH Impedance.
4. Level of B before the indicated steady-state input conditions were established.
5. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
6. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

9

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[10]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[7]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[8]		V_{CC}=Min.	V_I=2.0V	−50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[7]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[9]		V_{CC}=Max., V_{OUT}=GND		−80	−140	−200	mA
I_O	Output Drive Current[9]		V_{CC}=Max., V_{OUT}=2.5V		−50		−180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V				±1	µA

Output Drive Characteristics for CY74FCT16952T

Parameter	Description	Test Conditions	Min.	Typ.[10]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T

Parameter	Description	Test Conditions	Min.	Typ.[10]	Max.	Unit
I_{ODL}	Output LOW Current[9]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[9]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[7] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[10]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

7. This parameter is guaranteed but not tested.
8. Pins with bus hold are described in the Pin Description.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
10. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

Power Supply Characteristics

Parameter	Description	Test Conditions[11]		Typ.[10]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[12]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[13]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEAB}$ or $\overline{OEBA}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	75	120	µA/ MHz
I_C	Total Power Supply Current[14]	V_{CC}=Max., F_1=5 MHz, F_0 = 10 MHz (CLKAB) $\overline{OEAB}$ = $\overline{CEAB}$ = GND $\overline{OEBA}$ = V_{CC} 50% Duty Cycle, Outputs Open, One Bit Toggling	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	1.3	3.2	
		V_{CC}=Max., f_0=10 MHz (CLKAB) f_1=2.5 MHz, $\overline{OEAB}$ = $\overline{CEAB}$ = GND $\overline{OEBA}$ = V_{CC} 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	$V_{IN}=V_{CC}$ or V_{IN}=GND	3.8	6.5[15]	
			V_{IN}=3.4V or V_{IN}=GND	8.3	20.0[15]	

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
14. I_C = $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
15. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	Conditions[16]	74FCT16952AT 74FCT162952AT 74FCT162H952AT		74FCT16952BT 74FCT162952BT 74FCT162H952BT		74FCT16952CT 74FCT162952CT 74FCT162H952CT		Unit	Fig. No.[18]
			Min.[17]	Max.	Min.[17]	Max.	Min.[17]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CLKAB, CLKBA to B, A	C_L=50 pF R_L=500Ω	2.0	10.0	2.0	7.5	2.0	6.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$, $\overline{OEAB}$ to A, B		1.5	10.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$, $\overline{OEAB}$ to A, B		1.5	10.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{SU}	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA		2.5	—	2.5	—	2.5	—	ns	4
t_H	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA		2.0	—	1.5	—	1.5	—	ns	4
t_{SU}	Set-Up Time, HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CLKAB, CLKBA		3.0	—	3.0	—	3.0	—	ns	4
t_H	Hold Time, HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CLKAB, CLKBA		2.0	—	2.0	—	2.0	—	ns	4
t_W	Pulse Width HIGH or LOW CLKAB or CLKBA[19]		3.0	—	3.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew[20]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
16. See test circuits and waveforms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. See "Parameter Measurement Information" in the General Information Section.
19. This parameter is guaranteed but not tested.
20. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information CY74FCT16952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT16952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT16952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT16952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT162952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT162H952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162H952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162H952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952ATPVC	O56	56-Lead (300-Mil) SSOP	

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CYBUS3384
CYBUS3L384

Dual 5-Bit Bus Switches

Features

- **Zero propagation delay**
- **2Ω switches connect inputs to outputs**
- **Direct bus connection when switches are ON**
- **High (>500 Meg Ω) resistance when switch is OFF**
- **Performs bidirectional translator function between 3.3V and 5.0V power supplies**
- **CMOS for low power dissipation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Inputs and outputs interface with 5.0V CMOS, TTL, or 3.3V CMOS**
- **ESD>2000 V**
- **Power-off disable**

CYBUS3L384

- **Low power version**

Functional Description

The CYBUS3384 and CYBUS3L384 are ten-bit, two-port bidirectional bus switches that allow one bus to be connected directly to, or isolated from, another without introducing additional propagation delay or ground noise. The input and output voltage levels allow direct interface with TTL and CMOS devices. Two bus enable signals, $\overline{BE}_1$ and $\overline{BE}_2$, turn on the upper and lower five bits, respectively.

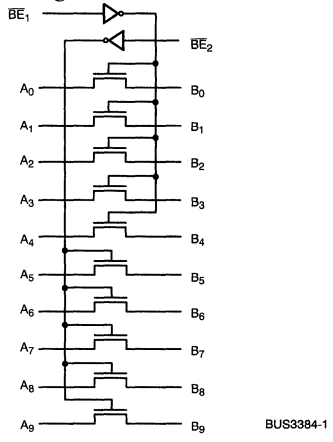
Designed with a low resistance of 2Ω, the CYBUS3384 and CYBUS3L384 are ideal for use in VME or other high DC drive applications.

The power-off disable feature enables modules and cards to be either inserted or withdrawn from operating equipment without shutting down power. Additionally, they facilitate bidirectional interfacing between 3.3V and 5V systems by placing a single diode in series with the 5V V_{CC} line and a resistor from pin 24 to ground.

The CYBUS3384 and CYBUS3L384 are also suitable for small signal analog application where crosstalk and off isolation performance of −66 dB at 50 MHz is required.

The CYBUS3L384 is a low-power version of the CYBUS3384 with a typical I_{CC} of 0.2 μA.

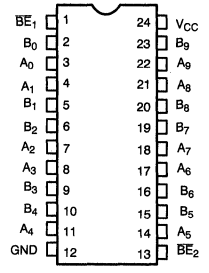
Logic Block Diagram



BUS3384-1

Pin Configurations

DIP/SOIC/QSOP
Top View



BUS3384-2

Pin Description

Name	Description
A	Bus A, Inputs or Outputs
B	Bus B, Inputs or Outputs
$\overline{BE}_1$, $\overline{BE}_2$	Bus Switch Enable

Function Table[1]

Inputs				
$\overline{BE}_1$	$\overline{BE}_2$	B_{0-4}	B_{5-9}	Function
H	H	High-Z	High-Z	Non-connect
L	H	A_{0-4}	High-Z	Connect
H	L	High-Z	A_{5-9}	Connect
L	L	A_{0-4}	A_{5-9}	Connect

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +165°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

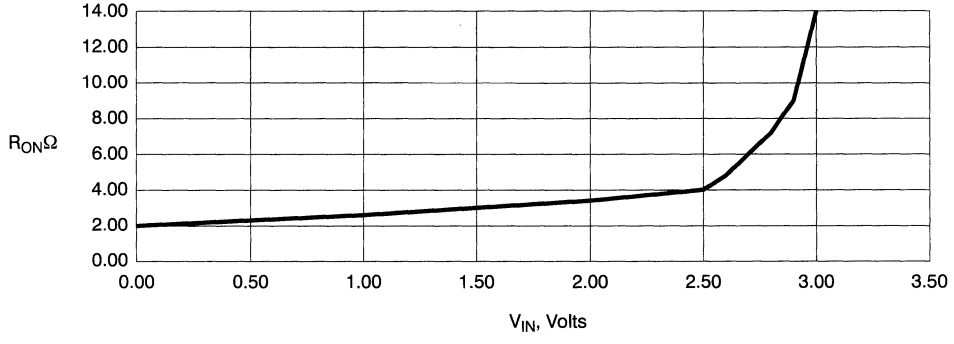
Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	4.0V to 5.5V
Military	−55°C to +125°C	4.0V to 5.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage	Control Inputs Only	2.0			V
V_{IL}	Input LOW Voltage	Control Inputs Only			0.8	V
V_H	Hysteresis[5]	Control Inputs Only		0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
R_{ON}	Switch On Resistance[6]	V_{CC}=4.75V, V_{IN}=0.0V, I_{ON}=30 mA		2	4	Ω
		V_{CC}=4.75V, V_{IN}=2.4V, I_{ON}=15 mA		4	8	Ω
I_{IN}	Input Leakage Current	V_{CC}=Max., V_{IN}=V_{CC}			±1	µA
I_{OZ}	Off State Current (High-Z)	V_{CC}=Max., V_{OUT}=0.5V		0.001	±1	µA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V, V_{IN}=V_{CC}			±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		100		mA

On Resistance vs. V_{IN} @ 4.75 V_{CC}



Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on pin A or pin B.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	3	4	pF
C_{OUT}	Output Capacitance	7	8	pF

Power Supply Characteristics

Parameter	Description	Test Conditions[8]		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le$ GND or V_{CC}, f=0	3384	0.1	0.2	mA
			3L384	0.2	3.0	μA
ΔI_{CC}	Quiescent Power Supply Current (Input HIGH)[9]	V_{CC}=Max., V_{IN}=3.4V, f=0, Per Control Input			2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., Control Input Toggling, @ 50% Duty Cycle, A & B Pins Open			0.12	mA/ MHz
I_C	Total Power Supply Current[11, 12]	V_{CC}=Max., Two Control Inputs Toggling, @ 50% Duty Cycle, f_1=10 MHz, V_{IN}=3.4V	3384		4.6	mA
			3L384		4.4	mA

Notes:

8. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
9. Per TTL driven input (V_{IN}=3.4V); A and B pins do not contribute to I_{CC}. All other inputs at V_{CC} or GND.
10. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
12. Note that activity on A or B inputs do not contribute to I_C. The switches merely connect and pass through activity on these pins.

Switching Characteristics Over the Operating Range

Parameter	Description	Military		Commercial		Unit
		Min.[13]	Max.	Min.[13]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B[14, 15]		0.25		.25	ns
t_{PZH} t_{PZL}	Switch Turn On Delay, $\overline{BE}_1$, $\overline{BE}_2$ to A, B[13]	1.5	7.5	1.5	6.5	ns
t_{PHZ} t_{PHZ}	Switch Turn Off Delay, $\overline{BE}_1$, $\overline{BE}_2$ to A, B[13, 14]	1.5	6.5	1.5	5.5	ns
$\lvert Q_{ci} \rvert$	Charge Injection, Typical[16, 17]		1.5		1.5	pC

Ordering Information CYBUS3384

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
0.25	CYBUS3384PC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CYBUS3384QC	Q13	24-Lead (150-Mil) QSOP	
	CYBUS3384SOC	S13	24-Lead (300-Mil) Molded SOIC	
0.25	CYBUS3384DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CYBUS3384LMB	L64	28-Square Leadless Chip Carrier	

Ordering Information CYBUS3L384

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
0.25	CYBUS3L384PC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CYBUS3L384QC	Q13	24-Lead (150-Mil) QSOP	
	CYBUS3L384SOC	S13	24-Lead (300-Mil) Molded SOIC	

Notes:

13. See test Circuit and Waveform. Minimum limits are guaranteed but not tested.
14. This parameter is guaranteed by design but not tested.
15. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
16. Measured at switch turn off, A to C, load=50 pF in parallel with 10 meg scope probe, V_{IN} at A=0.0V.
17. Tested initially and after any design change which may affect this parameter.

9

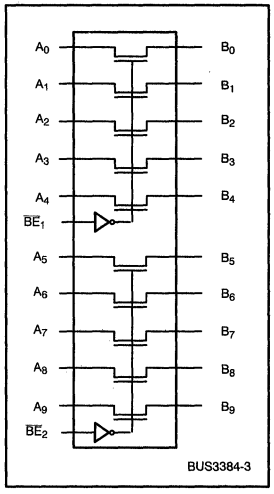


Figure 1. CYBUS3384

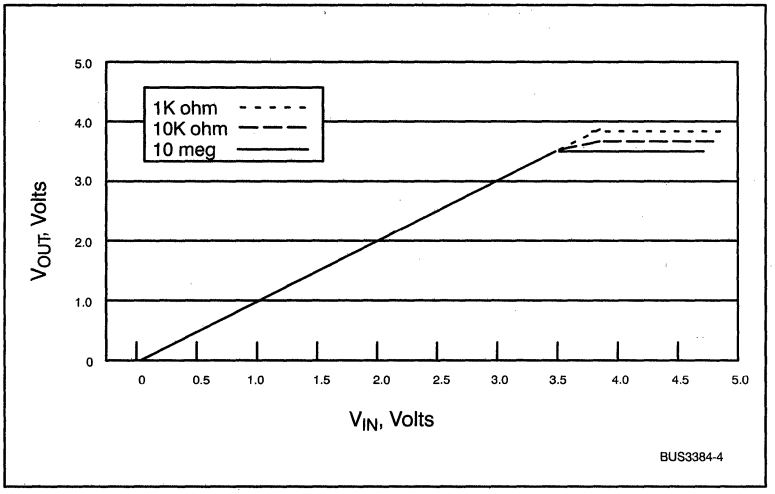


Figure 2. V_{OUT} vs. Volts

Application Information

The CYBUS3384 is a ten-channel bidirectional solid state bus switch with a "near zero" propagation delay.

The CYBUS3384 is organized into two groups of five N-Channel MOSFETs. Each group has an independent control input for output enable (see *Figure 1*). Because the N-channel MOSFET is physically symmetric, the device pin can act as an input or an output.

The two enable input ($\overline{BE}_1$ and $\overline{BE}_2$) sense TTL level signals and drive the gates of the N-channel MOSFETs to V_{CC}. With the gate at V_{CC}, the output voltage will follow the input voltage up to V_{CC} minus the threshold voltage. At this point the N-channel MOSFET begins to turn off, rapidly increasing the effective resistance (R_{ON}) such that further increases to input voltage no longer increase the output voltage (see *Figure 2*).

When either the input or output of the CYBUS3384 is near zero volts and the gate is at V_{CC}, the device is fully on, (low resistance) and available to pass large currents in either direction. In this condition, the CYBUS3384 inputs are directly connected to the outputs.

The CYBUS3384 provides no signal drive itself. As a result the rise and fall times of the CYBUS3384 outputs are determined by the device driving the CYBUS3384 inputs rather than the CYBUS3384 itself.

The propagation delay contributed by the CYBUS3384 is essentially zero when the N-channel gate is at V_{CC}.

When the device is unpowered, the CYBUS3384 draws no current from the I/O or control inputs, and there is no current path from the I/O or control to the power pins. There are no back power or current drain problems when the device is unpowered.

The CYBUS3384 provides an ideal interface between 5V and 3.3V components, since the CYBUS3384 provides no signal drive, the I_{CC} demands are small, limited to AC switching of the N-channel gates, control circuitry, and a minute amount of I/O leakage. Due to the low current demands of the CYBUS3384, it is possible to lower the CYBUS3384 V_{CC} from a standard 5.0V supply with a small, inexpensive diode and a resistor to provide a low-current full-bidirectional signal compatibility between 5V logic family signals and 3.3V logic family signals.

By adding a small, inexpensive diode and a resistor, the CYBUS3384 V_{CC} supply voltage can be shifted to 4.3V as shown in *Figure 3*. 5V signals will then be limited to 3.3V as they pass through the CYBUS3384. 3.3V signals will pass back through the CYBUS3384 unaltered and provide compatibility with 5V TTL input requirements. Note that the conversion is bedirectional and is limited to 3.3V independent of which side is driven to 5V. The CYBUS3384 could convert 5V signals for use on a 3.3V bus of convert a 5V bus to signals compatibile with 3.3V components.

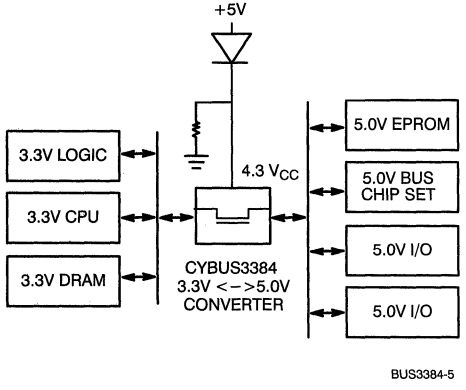


Figure 3. System with CYBUS3384 as 5V TTL to 3V Converter

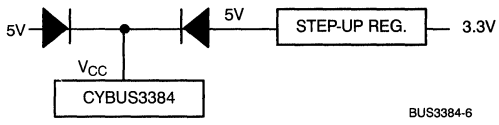


Figure 4. 3.3V/5V Supply Switch

3.3V/5V Supply Operation

In certain system applications, the CYBUS3384 must operate from either a 5V or 3.3V power supply, depending on the state of the system. If this occurs, the circuit shown in *Figure 4* can be added to step the 3.3V supply up to a nominal 5V level. The low-cost, high-efficiency Step Up regulator shown in the figure is available for Linear Technology, Maxim, and other suppliers. The diode arrangement will automatically select the active supply. Standard silicon diodes can be used because the CYBUS3384 V_{CC} is specified at 4.0V.

Low Power Bus Isolation

Modern battery-operated systems rely on internal power management schemes to disconnect power from subsystems not in use. Usually the subsystem bus input ESD protection circuits consist of a pair of clamp diodes to limit input voltage excursions to a maximum of $V_{CC}+Vt$ and $-Vt$ (see *Figure 5*). Removing power from these causes the V_{CC} ESD clamp diode to connect the dead circuit inputs to GND, often significantly increasing bus loading and power dissipation (see *Figure 6*). The CYBUS3384 placed on the input of the load to be disconnected effectively prevents bus loading and its associated problems.

High Speed Dual Port RAM

As shown in *Figure 7*, a high-speed, dual-port memory is implemented using a combination of commodity SRAM, a simple arbitration circuit, and the CYBUS3384. Processor 1 is the system host processor while Processor 2 is dedicated peripheral processor (such as a DSP for acquisitioning and manipulating data). Either processor can own the SRAM by first reading the BUSY bit to determine if the SRAM is available. If so, the requesting processor takes control by writing the OWN bit (which redirects

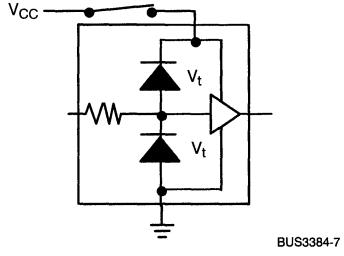


Figure 5. Gate Input (Power ON)

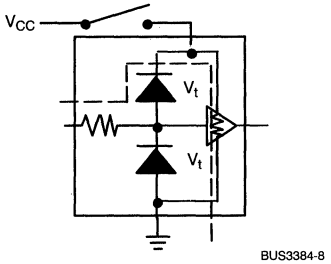


Figure 6. Gate Input (Power OFF)

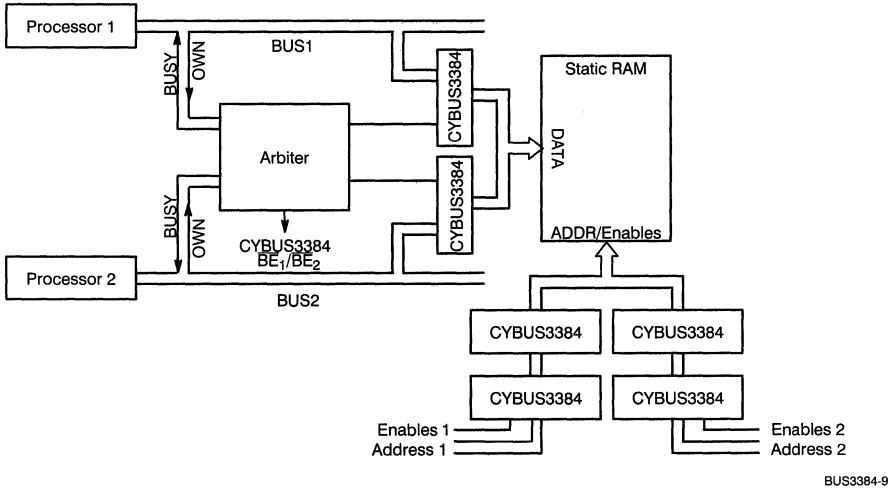


Figure 7. High Speed Dual Port RAM

the bus through the CYBUS3384s and sets the BUSY bit notifying the other bus the SRAM is not available). Processor 1 owns the bus and may now access the SRAM as needed. When finished, Processor 1 resets the OWN bit releasing the SRAM. The SRAM access sequence is identical for Processor 2. In this application, the CYBUS3384 saves 10 ns compared to using an F244 address buffer and an F245 data bus transceiver. This, in turn, allows the use of a slower, more available SRAM, resulting in lower system cost and power savings.

Selectable Termination Loads

In some applications, it is desirable to vary the characteristic termination impedance as the system configuration changes. This is a common problem in automatic test equipment applications. Because of their low ON resistance, miniature relays are often used to switch termination loads. A single CYBUS3384 can replace as many as 10 such relays resulting in faster switching operation, lower power, and significant cost savings.

Fast Latch

Figures 8 and *9* show variations of a latch having a sub 1-ns propagational delay time using the CYBUS3384 in combination with other components. This circuit has the advantage of being four

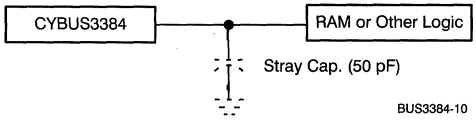


Figure 8. Latch Variation with Stray Capacitance

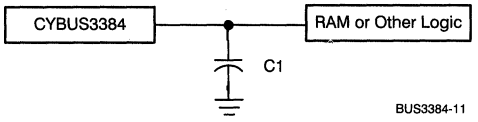


Figure 9. Latch Variation with Physical Capacitor

to ten times faster than an equivalent implementation using a 373 latch—and with no added noise. *Figure 8* relies on the stray capacitance of the bus to maintain data when the CYBUS3384 opens. Assuming 50-pF stray capacitance at room temperature and a 1 microampere input leakage current, a 1 volt "droop" from the initial voltage level would take 50 microseconds. *Figure 9* shows the addition of a physical capacitor if there is insufficient stray capacitance. *Figure 10* shows an active bus termination capable of sustaining the programmed logic for an indefinite period of time in the presence of V_{CC}.

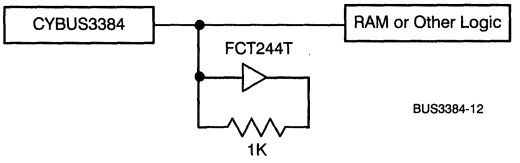


Figure 10. Active Bus Termination

Document #: 38–00355

Section Contents

Timing Technology Products

Pentium™ Processor Compatible Clock Synthesizer/Driver

Features

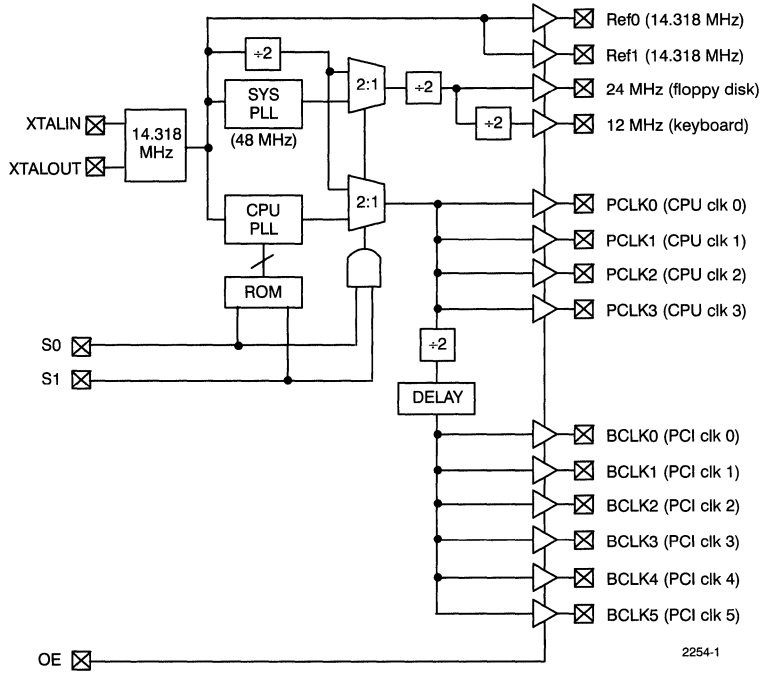
- **Compatible with Intel Triton™ chipset requirements**
- **Multiple clock outputs to meet requirements of most motherboards using Pentium™ processors**
  - **Four CPU clocks @ 66.66 MHz, 60 MHz, and 50 MHz, pin selectable**
  - **Six PCI clocks (CPUCLK/2)**
  - **One Floppy clock @ 24 MHz**
  - **One Keyboard Controller clock @ 12 MHz**
  - **Two Ref. clocks @ 14.318 MHz**
  - **Ref. 14.318 MHz Xtal oscillator input**
- **CPU clock jitter ≤ 200 ps cycle-to-cycle**
- **Low skew outputs**
  - **≤ 250 ps between CPU clocks (PCLK)**
  - **≤ 500 ps between PCI clocks (BCLK)**
  - **+1 ns min. to +5 ns max. skew between CPU and PCI Clocks (CPU leads PCI)**
- **Freq. stability = 0.01 % (max.)**
- **Output duty cycle 40% min. to 60% max.**
- **Test mode support**
- **3.3V operation**

Functional Description

The CY2254 is a Clock Synthesizer/Driver chip for the Intel® Pentium processor based PC. The part outputs multiple clocks, to serve the requirements of most motherboards. The CY2254 has low-skew outputs (≤ 250 ps between the CPU Clocks, ≤ 500 ps between the PCI Clocks). In addition, the CY2254 CPU clock outputs have less than 200 ps cycle-to-cycle RMS jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of the Pentium-based system.

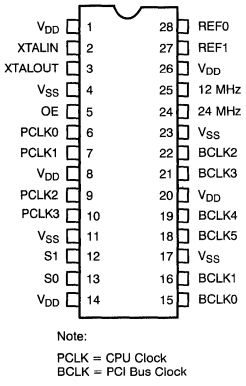
The CY2254 accepts a 14.318 MHz reference signal as its input. The CY2254 has 2 PLLs, one of which generates the CPU and PCI clocks, and the other generates the Floppy Disk and Keyboard Controller clocks. The CY2254 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration

Top View
SOIC



Note:
PCLK = CPU Clock
BCLK = PCI Bus Clock

2254-2

Pin Summary

Name	Number	Description
V_{DD}	1	Digital voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
OE	5	Output Enable, Active HIGH
PCLK0	6	CPU output clock
PCLK1	7	CPU output clock
V_{DD}	8	Digital voltage supply
PCLK2	9	CPU output clock
PCLK3	10	CPU output clock
V_{SS}	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V_{DD}	14	Digital voltage supply
BCLK0	15	PCI output clock
BCLK1	16	PCI output clock
V_{SS}	17	Ground
BCLK5	18	PCI output clock
BCLK4	19	PCI output clock
V_{DD}	20	Digital voltage supply
BCLK3	21	PCI output clock
BCLK2	22	PCI output clock
V_{SS}	23	Ground
24 MHz	24	Floppy disk output clock (24 MHz)
12 MHz	25	Keyboard controller clock (12 MHz)
V_{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Function Table

OE	S0	S1	XTALIN Input	PCLK	BCLK	Ref. Clock Output	24 MHz	12 MHz
0	X	X	14.31818 MHz	High-Z	High-Z	High-Z	High-Z	High-Z
1	0	0	14.31818 MHz	50 MHz	PCLK/2	14.31818 MHz	24 MHz	12 MHz
1	0	1	14.31818 MHz	60 MHz	PCLK/2	14.31818 MHz	24 MHz	12 MHz
1	1	0	14.31818 MHz	66 MHz	PCLK/2	14.31818 MHz	24 MHz	12 MHz
1	1	1	TCLK[2]	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

PCI Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... −65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_C	Temperature of Case	0	70	°C
C_L	Max. Capacitive Load on PCLK BCLK 24 MHz 12 MHz REF0 REF1		 20 30 20 20 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Notes:
2. TCLK is a test clock on the XTAL1 input during test mode.
3. Electrical parameters are guaranteed with these operating conditions.

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Electrical Characteristics V_{DD} = 3.3V ±5%, T_C = 0°C to +70°C

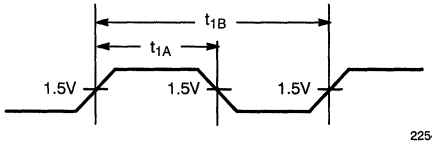
Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = 6 mA	PCLK	2.4		V
			I_{OH} = 12 mA	BCLK, REF0			
			I_{OH} = 4 mA	24, 12 MHz			
			I_{OH} = 8 mA	REF1			
V_{OL}	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 6 mA	PCLK		0.4	V
			I_{OL} = 12 mA	BCLK, REF0			
			I_{OL} = 4 mA	24, 12 MHz			
			I_{OL} = 8 mA	REF1			
I_{IH}	Input High Current	V_{IH} = V_{DD} − 0.5V			−5	+5	µA
I_{IL}	Input Low Current	V_{IL} = 0.5V			−5	+5	µA
I_{OZ}	Output Leakage Current	Three-state			−10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.465, V_{IN} = 0 or V_{DD}				90	mA

Switching Characteristics[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	40%	60%	
t_2	PCLK, BCLK	Output Slew Rate	0.4−2.4V	1		V/ns
t_3	REF, 24, 12 MHz	Rise Time	0.4−2.4V		4	ns
t_4	REF, 24, 12 MHz	Fall Time	2.4−0.4V		4	ns
t_5	PCLK	CPU Skew	CPU-CPU clock skew		250	ps
t_6	BCLK	PCI Skew	PCI-PCI clock skew		500	ps
t_7	PCLK, BCLK	CPU-PCI Skew	CPU to PCI clock skew (CPU leads)	1	5	ns
t_8	PCLK	Cycle-Cycle Clock Jitter	RMS clock jitter		200	ps

Switching Waveforms

Duty Cycle Timing

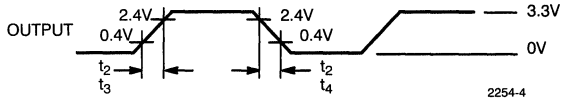


2254-3

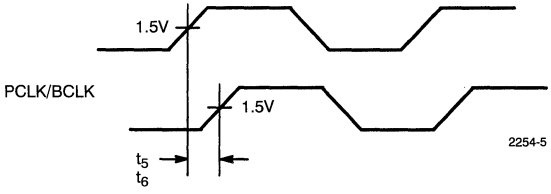
Notes:
4. All parameters specified with outputs fully loaded.
5. Duty cycle is measured at 1.5V.

Switching Waveforms (continued)

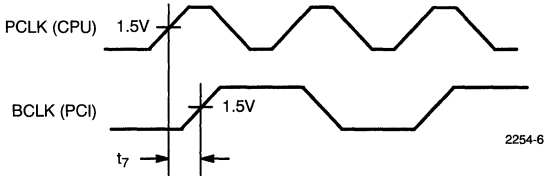
All Outputs Rise/Fall Time



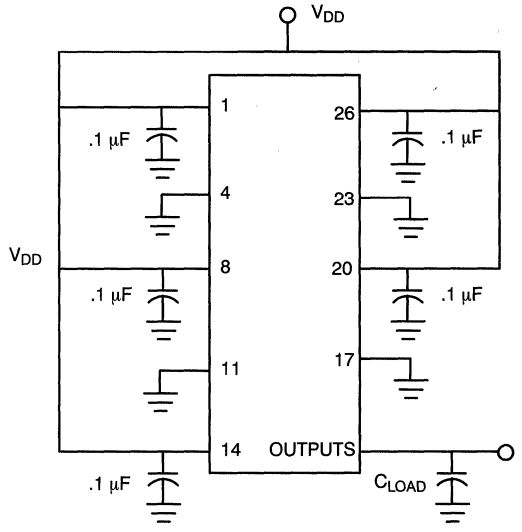
Clock Skew



CPU-PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2254	S21	28-Pin SOIC	Commercial

Document #: 38–00426

Pentium™ Processor Compatible Clock Synthesizer/Driver for OPTi Viper™ Chipset

Features

- **Multiple clock outputs to meet requirements of OPTi Viper™ chipset**
  - **Five CPU clocks @ 66.66 MHz, 60 MHz, and 50 MHz, pin selectable**
  - **One Early clock, leads CPU clocks by 2 to 5 ns**
  - **Six PCI clocks (CPUCLK/2)**
  - **Two Ref. clocks @ 14.318 MHz**
  - **Ref. 14.318 MHz Xtal oscillator input**
- **CPU clock jitter ≤ 250 ps cycle-to-cycle**
- **Low skew outputs**
  - **≤ 250 ps between CPU clocks**
  - **≤ 500 ps between PCI clocks**
  - **≤ 750 ps between CPU clocks and PCI clocks**
- **Freq. stability = 0.01 % (max.)**
- **Output duty cycle 40% min. to 60% max.**
- **Test mode support**
- **3.3V operation**
- **CMOS technology**

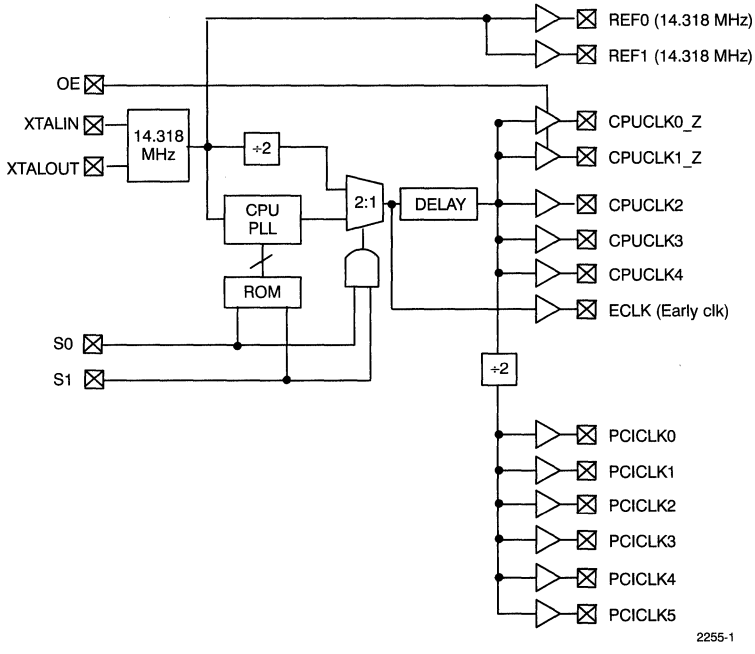
Functional Description

The CY2255 is a Clock Synthesizer/Driver chip with multiple output clocks, for the OPTi Viper™ chipset. The CY2255 outputs six CPU clocks at pin-selectable frequencies of 50, 60, and 66.66 MHz. One CPU clock leads the rest by 2 to 5 ns, and is denoted as Early Clock (ECLK). Two of the remaining five CPU clocks are three-stateable, controlled by an active-HIGH Output Enable (OE) pin. The CY2255 has six synchronous PCI clock outputs, each having a frequency of CPUCLK/2. The CY2255 also outputs two copies of the Reference clock.

The CY2255 has low-skew outputs (≤ 250 ps between the CPU Clocks, ≤ 500 ps between the PCI Clocks). In addition, the CY2255 CPU clock outputs have less than 250 ps cycle-to-cycle RMS jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of a Pentium™ processor–based system.

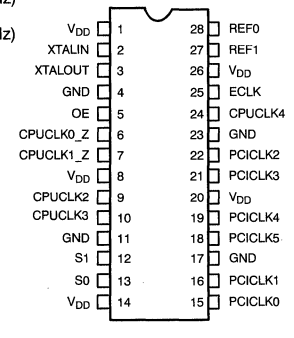
The CY2255 accepts a 14.318 MHz reference signal as its input, and uses it to generate the CPU and PCI clocks from a single PLL. The CY2255 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration

Top View
SOIC



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Viper is a trademark of OPTi.

Pin Summary

Name	Number	Description
V_{DD}	1	Digital voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
GND	4	Ground
OE	5	Output Enable, Active HIGH
CPUCLK0_Z	6	CPU clock output, three-stateable by OE
CPUCLK1_Z	7	CPU clock output, three-stateable by OE
V_{DD}	8	Digital voltage supply
CPUCLK2	9	CPU clock output
CPUCLK3	10	CPU clock output
GND	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V_{DD}	14	Digital voltage supply
PCICLK0	15	PCI clock output
PCICLK1	16	PCI clock output
GND	17	Ground
PCICLK5	18	PCI clock output
PCICLK4	19	PCI clock output
V_{DD}	20	Digital voltage supply
PCICLK3	21	PCI clock output
PCICLK2	22	PCI clock output
GND	23	Ground
CPUCLK4	24	CPU clock output
ECLK	25	Early clock output, leads CPU clocks by 2 to 5 ns
V_{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Function Table

OE	S0	S1	XTALIN Input	CPUCLK_Z [0:1]	ECLK, CPUCLK [2:4]	PCICLK	Ref. Clock Output
0	0	0	14.318 MHz	High-Z	50 MHz	CPUCLK/2	14.318 MHz
0	0	1	14.318 MHz	High-Z	60 MHz	CPUCLK/2	14.318 MHz
0	1	0	14.318 MHz	High-Z	66.66 MHz	CPUCLK/2	14.318 MHz
0	1	1	TCLK[2]	High-Z	TCLK/2	TCLK/4	TCLK
1	0	0	14.318 MHz	50 MHz	50 MHz	CPUCLK/2	14.318 MHz
1	0	1	14.318 MHz	60 MHz	60 MHz	CPUCLK/2	14.318 MHz
1	1	0	14.318 MHz	66.66 MHz	66.66 MHz	CPUCLK/2	14.318 MHz
1	1	1	TCLK[2]	TCLK/2	TCLK/2	TCLK/4	TCLK

PCI/CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... −65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Range

Ambient Temperature	V_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	3.3V ± 5%

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Temperature	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK REF0 REF1		 20 30 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Notes:

2. TCLK is a test clock on the XTALIN input during test mode.
3. Electrical parameters are guaranteed with these operating conditions.

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Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	HIGH-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I_{OH} = 6 mA	CPUCLK, ECLK	2.4		V
			I_{OH} = 12 mA	PCICLK, REF0			
			I_{OH} = 8 mA	REF1			
V_{OL}	LOW-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I_{OL} = 6 mA	CPUCLK, ECLK		0.4	V
			I_{OL} = 12 mA	PCICLK, REF0			
			I_{OL} = 8 mA	REF1			
V_{IH}	HIGH-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	LOW-level Input Voltage	Except Crystal Inputs				0.8	V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD} - 0.5V$			−5	+5	µA
I_{IL}	Input LOW Current	$V_{IL} = 0.5V$			−5	+5	µA
I_{OZ}	Output Leakage Current	Three-state outputs			−10	+10	µA
I_{DD}	Power Supply Current	$V_{DD} = 3.465$, $V_{IN} = 0$ or V_{DD}				90	mA

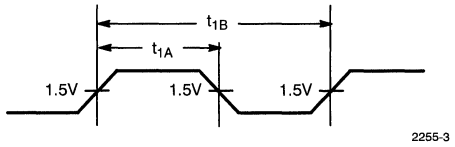
Switching Characteristics[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	40%	60%	
t_2	CPUCLK, ECLK, PCICLK	Output Slew Rate	0.4–2.4V	1		V/ns
t_3	REF0	Rise Time	20% – 80% of V_{DD}		2.5	ns
t_3	REF1	Rise Time	20% – 80% of V_{DD}		4	ns
t_4	REF0	Fall Time	20% – 80% of V_{DD}		2.5	ns
t_4	REF1	Fall Time	20% – 80% of V_{DD}		4	ns
t_5	CPUCLK	CPU Skew	CPU-CPU clock skew		250	ps
t_6	ECLK, CPUCLK	ECLK Skew	Early-CPU clock skew (ECLK leads)	2	5	ns
t_7	PCICLK	PCI Skew	PCI-PCI clock skew		500	ps
t_8	CPUCLK, PCICLK	CPU-PCI Skew	CPU to PCI clock skew (CPU leads)		750	ps
t_9	CPUCLK	Cycle-Cycle Clock Jitter	Clock jitter		250	ps

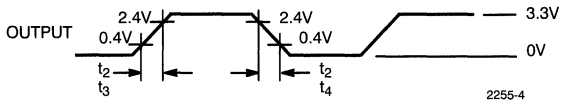
Notes:
4. All parameters specified with outputs fully loaded.
5. Duty cycle is measured at 1.5V.

Switching Waveforms

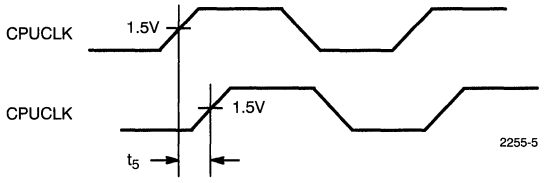
Duty Cycle Timing



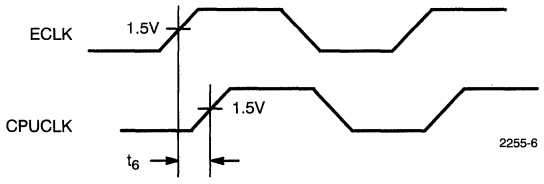
All Outputs Rise/Fall Time



CPU-CPU Clock Skew

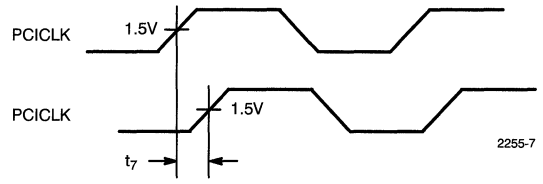


Early-CPU Clock Skew

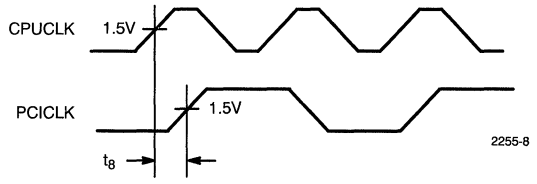


Switching Waveforms (continued)

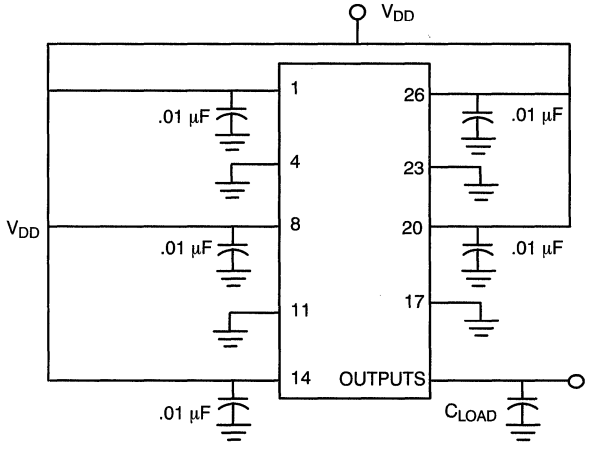
PCI-PCI Clock Skew



CPU-PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2255	S21	28-Pin SOIC	Commercial

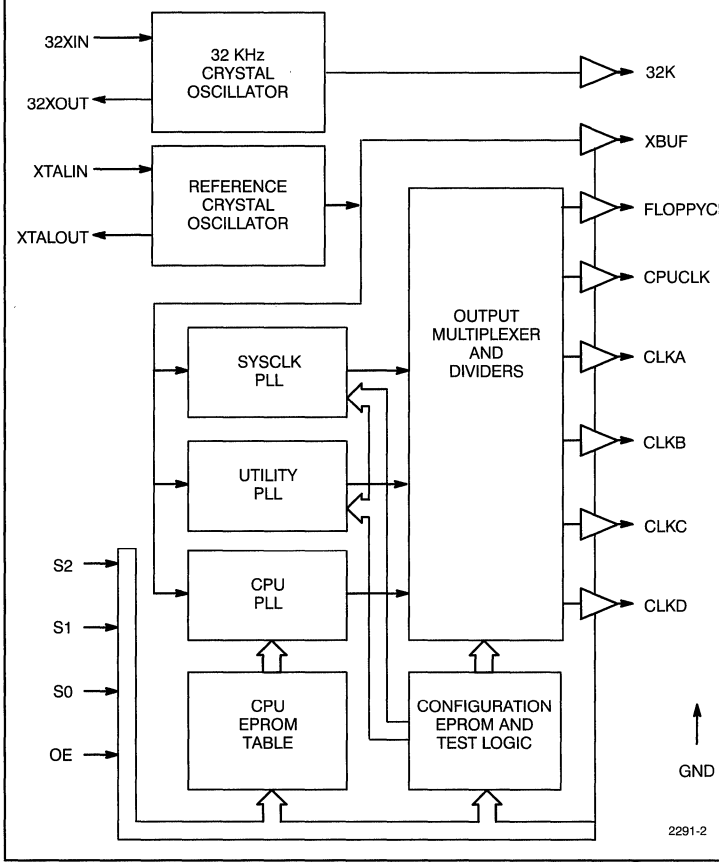
Document #: 38−00442

Three-PLL Clock Generator

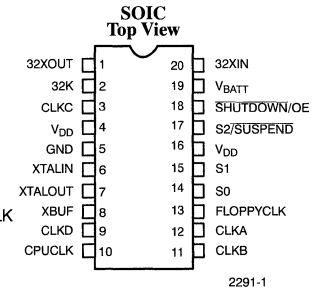
Features

- Pin compatible with ICD2028 (20-pin, 300-mil SOIC). Upward compatible with 2023 (without serial channel), and all versions of 2028
- Three PLLs provide all necessary clocks for modern motherboards and other synchronous systems
- Eight outputs including 32 kHz, FLOPPYCLK, XBUF, CPUCLK, and four configurable clocks
- Each configurable clock can choose 1 of 30 frequency options
- Low skew (500 ps) between related signals available on any or all configurable outputs
- Supports 10-MHz to 25-MHz reference clock
- Configuration includes permanent shutdown options for unused PLLs and configurable clocks
- Suspend feature allows shutting down a factory configurable set of PLLs and outputs with the S2 pin
- Smooth frequency transitions on CPUCLK from 4 MHz to 100 MHz (80 MHz at 3.3V)
- $\overline{\text{SHUTDOWN}}$/OE pin three-states outputs and powers down part. OE available as an option. Power-down current draw of less than 50 µA, plus 15 µA max. for 32 kHz subsystem
- Factory EPROM programmable for fast turnaround times
- Weak pulldowns in outputs pull signals low when three-stated
- Compatible with 486 and Pentium™ processor clock specifications
- 3.3V or 5V operation
- Capable of withstanding greater than 2000V static discharge

Logic Block Diagram



Pin Configuration



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Pin Summary

Name	Number	Description
32XOUT	1	32.768 kHz crystal feedback
32K	2	32.768 kHz output (always active if V_{BATT} is present)
CLKC	3	Configurable clock output C
V_{DD}	4	Voltage supply to I/O
GND	5	Ground
XTALIN[1, 2]	6	Reference crystal input
XTALOUT[1, 2]	7	Reference crystal feedback
XBUF	8	Buffered reference clock output
CLKD	9	Configurable clock output D
CPUCLK	10	CPU frequency clock output
CLKB	11	Configurable clock output B
CLKA	12	Configurable clock output A
FLOPPYCLK	13	Floppy clock output (24 or 32 MHz)
S0	14	CPU clock select input, bit 0
S1	15	CPU clock select input, bit 1
V_{DD}	16	Analog voltage supply to core
S2/$\overline{\text{SUSPEND}}$	17	CPU clock select input, bit 2. Optionally enables suspend feature when LOW.
$\overline{\text{SHUTDOWN}}$/OE	18	Places outputs in three-state[3] condition and shuts down chip when LOW. Optionally, only places outputs in three-state[3] condition and does not shut down chip when LOW.
V_{BATT}	19	Battery supply for 32.768 kHz circuit
32XIN	20	32.768 kHz crystal input

Operation

The CY2291 is a third-generation Clock Generator, upwardly compatible with the industry standard ICD2023 and ICD2028. The CY2291 continues the tradition of these parts by providing a high level of customizable features to meet the diverse clock generation needs of modern multi-function motherboards and other synchronous systems.

The CY2291 provides a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same frequency will have low (≤500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2291 includes two independent power-saving modes for Green PC or laptop applications. Shutdown mode, controlled by the $\overline{\text{SHUTDOWN}}$/OE pin, shuts down all of the active circuitry on the chip except for the 32 kHz oscillator. The resulting current draw on the V_{DD} pins is typically less than 10 μA. Suspend mode, controlled by the S2/$\overline{\text{SUSPEND}}$ pin, shuts down a customizable set of outputs and/or PLLs when they are not needed. In addition to these two modes, most configurations support disabling unused outputs and PLLs.

The CY2291 can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing factory configuration for operation at non-standard frequencies. The reference oscillator has been designed for 10 MHz to 25 MHz crystals, providing additional flexibility. All configurations are factory programmable, providing short sample and production lead times.

Output Configuration

The CY2291 has five independent frequency sources on chip. These are the 32 kHz oscillator, the reference oscillator, and three Phase Locked Loops (PLLs). Each PLL has a specific function. The SYSCLK PLL drives the FLOPPYCLK output and provides the fixed frequencies on the configurable outputs. The CPU PLL responds to the select inputs (S0–S2) to provide eight user selectable frequencies with smooth slewing between frequencies. The Utility PLL is available to provide miscellaneous frequencies not provided by the other frequency sources.

The CY2291 has four fixed frequency outputs (32K, XBUF, FLOPPYCLK, and CPUCLK) and four configurable outputs (CLKA–CLKD). Each of these configurable outputs has an identical set of 30 output frequency options. The list of frequency options includes frequencies derived from four of the five sources on the chip. Please refer to the application note "Understanding the 2291" for information on configuring the part.

Notes:

1. For best accuracy, use a parallel-resonant crystal.
2. Assume $C_{LOAD} \approx 17$ pF.
3. The CY2291 has weak pull-downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

Power Saving Features

The SHUTDOWN/OE input three-states the outputs when pulled LOW (the 32-kHz clock output is not affected). If system shutdown is enabled (the default), a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 50 µA (plus 15 µA max. for the 32-kHz subsystem) and is typically 10 µA. After leaving shutdown mode, the PLLs will have to re-lock. All outputs except 32K have a weak pull-down so that the outputs do not float when three-stated.[3]

The S2/SUSPEND input can be configured to shut off a customizable set of outputs and/or PLLs when LOW. All PLLs and any of the outputs except 32K can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.[3]

The CPUCLK on the CY2291 can slew (transition) smoothly between 4 MHz and 100 MHz (80 MHz at 3.3V). This feature is extremely useful in "Green" PC and laptop applications, where reducing the frequency of operation can result in considerable power savings. This feature meets all 486 and Pentium processor slewing requirements.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Storage Temperature ..... −65°C to +150°C

Max. Soldering Temperature (10 sec) ..... 260°C

Junction Temperature ..... 150°C

Package Power Dissipation ..... 750 mW

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[4]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5.0V (3.3V) operation	4.5 (3.0)	5.5 (3.6)	V
V_{BATT}	Battery Backup Voltage	2.0	5.5	V
T_C	Operating Temperature of Case	0	70	°C
C_{LOAD}	Max. Load Capacitance		25 (15)	pF
f_{REF}	Reference Frequency	10.0	25.0	MHz

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA	2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{OH-32}	32.768 kHz HIGH-Level Output Voltage	I_{OH} = 0.5 mA	V_{BATT}−0.5			V
V_{OL-32}	32.768 kHz LOW-Level Output Voltage	I_{OL} = 0.5 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[5]	Except crystal pins	2.0			V
V_{IL}	LOW-Level Input Voltage[5]	Except crystal pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}−0.5V		< 1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V		< 1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs			250	µA
I_{DD}	V_{DD} Supply Current[6]	V_{DD} = V_{DD} max., 5V (3.3V) operation		75(50)	100(65)	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[6]	Shutdown active, excluding V_{BATT}		10	50	µA
I_{BATT}	V_{BATT} Power Supply Current	V_{BATT} = 3.0V		5	15	µA

Notes:

4. Electrical parameters are guaranteed with these operating conditions.
5. Xtal inputs have CMOS thresholds.
6. Load = Max., V_{IN} = 0V or V_{DD}, Standard (−000) configuration, CPU = 66 MHz. Other configurations will vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.03\bullet(F_{CPLL}+F_{UPLL}+2\bullet F_{SPLL})+0.27\bullet(F_{CLKA}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CPU}+F_{FLOPPY}+F_{XBUFF})$

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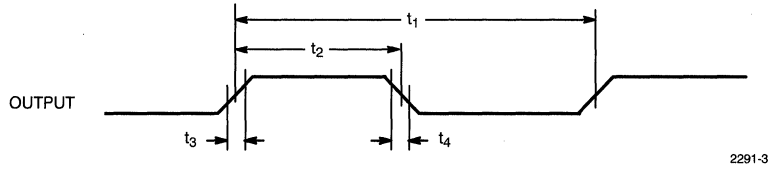
Switching Characteristics[7]

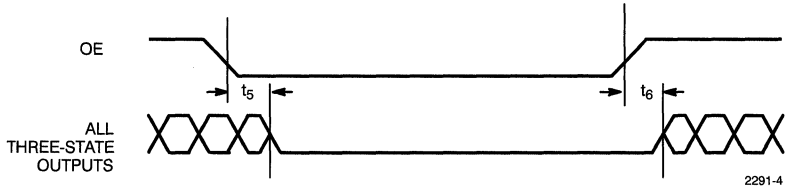
Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	10 (100 MHz)		5000 (200 KHz)	ns
t_1	Output Period	Clock output range, 3.3V operation	12.5 (80 MHz)		5000 (200 KHz)	ns
	Output Duty Cycle[8]	Duty cycle for outputs, defined as $t_2 \div t_1$[9]	40%	50%	60%	
t_3	Rise time	Output clock rise time[10]			5	ns
t_4	Fall time	Output clock fall time[10]			4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after $\overline{\text{SHUTDOWN}}$/OE goes LOW			15	ns
t_6	Output	Time for output to leave three-state mode after $\overline{\text{SHUTDOWN}}$/OE goes HIGH			15	ns
t_7	Skew	Skew delay between any identical or related outputs, as measured @ TTL V_{th}[11]		< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate	2.0		20.0	MHz/ ms
t_{9A}	Clock Jitter	Peak-to-peak period jitter (t_{9A} max. − t_{9A} min.) percent of clock period		< 2	5	%
t_{9B}	Clock Jitter	Peak-to-peak period jitter ($f_{OUT} \geq 16$ MHz)			700	ps
t_{9C}	Clock Jitter	±3σ jitter (CPUCLK @ ≥ 50 MHz)			250	ps
t_{10}	Lock Time	Time for VCO to settle between changes		5	50	ms
	Slew Limits		4		100 (5V) 80 (3.3V)	MHz

Switching Waveforms

All Outputs Duty Cycle and Rise/Fall Time



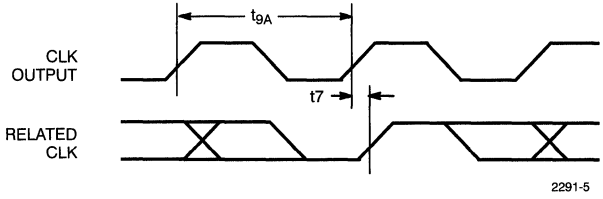
Output Three-State Timing[3]



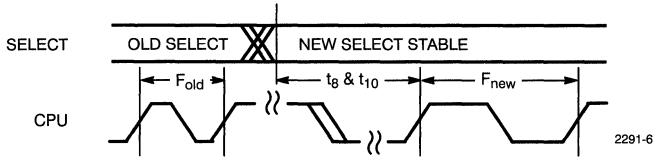
Note:
7. Guaranteed by design, not 100% tested.
8. XBUF duty cycle depends on XTALIN duty cycle.
9. Measured at 1.4V.
10. Measured between 0.4V and 2.4V.
11. "Related" outputs are defined as having identical sources internally. Generally they are multiples of each other. To meet the skew guarantee, outputs must have identical capacitive loads.

Switching Waveforms (continued)

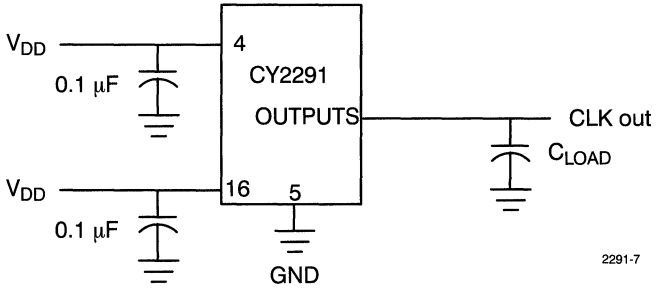
CLK Outputs Jitter and Skew



CPU Frequency Change



Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2291	S5	20-Pin SOIC	Commercial[12]

Note:
12. 0°C to +70°C

Document #: 38-00410

CY2291 CONFIGURATION REQUEST FORM

Customer_____ Contact_____ FAE/Sales_____

Phone # _____ Fax # _____ Date _____

1. OPERATING VOLTAGE (circle one) 3.3V 5.0V

2. INPUT REFERENCE FREQUENCY
Default reference = 14.318 MHz. If a different reference is desired, please enter value between 10 and 25 MHz.

3. PLL FREQUENCIES
Harmonics will result at the outputs if two or more PLLs run at frequencies which are integral multiples of each other.
Note: "Off" is a valid frequency for any PLL.

	Select S2 S1 S0	Requested	Actual	
CPLL (CPU PLL) *If suspend option chosen, then request frequencies only for S2 = 1*	0 0 0			*shaded areas for Cypress use only*
	0 0 1			
	0 1 0			
	0 1 1			
	1 0 0			
	1 0 1			
	1 1 0			
	1 1 1			
UPLL (UTILITY PLL)				*shaded areas for Cypress use only*
SPLL (SYSCLK PLL) *Default frequency is 96 MHz @ 5V, 48 MHz @ 3.3V*				*shaded areas for Cypress use only*

4. OUTPUT CONFIGURATION

Available Output Options

1. Ref	6. CPLL/2	11. UPLL/4	16. SPLL/4	21. SPLL/12	26. SPLL/40
2. Ref/2	7. CPLL/4	12. UPLL/8	17. SPLL/5	22. SPLL/13	27. SPLL/48
3. Ref/4	8. CPLL/8	13. SPLL	18. SPLL/6	23. SPLL/20	28. SPLL/52
4. Ref/8	9. UPLL	14. SPLL/2	19. SPLL/8	24. SPLL/24	29. SPLL/96
5. CPLL	10. UPLL/2	15. SPLL/3	20. SPLL/10	25. SPLL/26	30. SPLL/104

CLKA (select 1–30, off) _____
CLKB (select 1–30, off) _____
CLKC (select 1–30, off) _____
CLKD (select 1–30, off) _____
for CLKD, Ref/8 is replaced with Ref/3

CPUCLK (select 5 or off) _____
FLOPPYCLK (select 14, 15, 16, or off) _____
XBUF (select 1 or off) _____

5. SHUTDOWN OPTION (circle one) Y N

6. SUSPEND OPTION (circle one) Y N
If Yes, assign resources by circling any of the following:
Suspending a PLL automatically suspends its outputs.

CPLL	XBUF	CLKA
UPLL	CPUCLK	CLKB
SPLL	FLOPPYCLK	CLKC
		CLKD

7. FOR CYPRESS / IC DESIGNS USE ONLY

Customer Configuration	Marking
Date	Quantity

PC Motherboard Clock Generator

Features

- **Seven independent clock outputs handle all clocking requirements for personal computer motherboards**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Programmable frequency range: 10 MHz to 80 MHz with 50% duty cycle**
- **Ideally suited for PC desktop and laptop computer applications**
- **Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Battery input maintains 32.768 kHz clock during power-down**
- **Three-state oscillator control disables outputs for test purposes**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

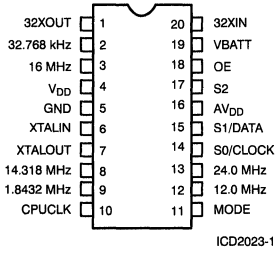
Functional Description

A modern personal computer motherboard often requires as many as seven different crystal can oscillators. The System Logic family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2023 PC Motherboard Clock Generator offers two oscillators, two phase-locked loops and seven different outputs in a single package. Six of the outputs are of a fixed value while the seventh output is fully user-programmable and may be changed on-the-fly to any desired frequency value between 10 MHz and 80 MHz. The ICD2023 is ideally suited for use in both existing designs (since it requires no support from the motherboard chip set and outputs seven frequencies concurrently) and new designs which can utilize the programmable nature of this device.

Pin Configurations

SOIC
Top View



ICD2023-1

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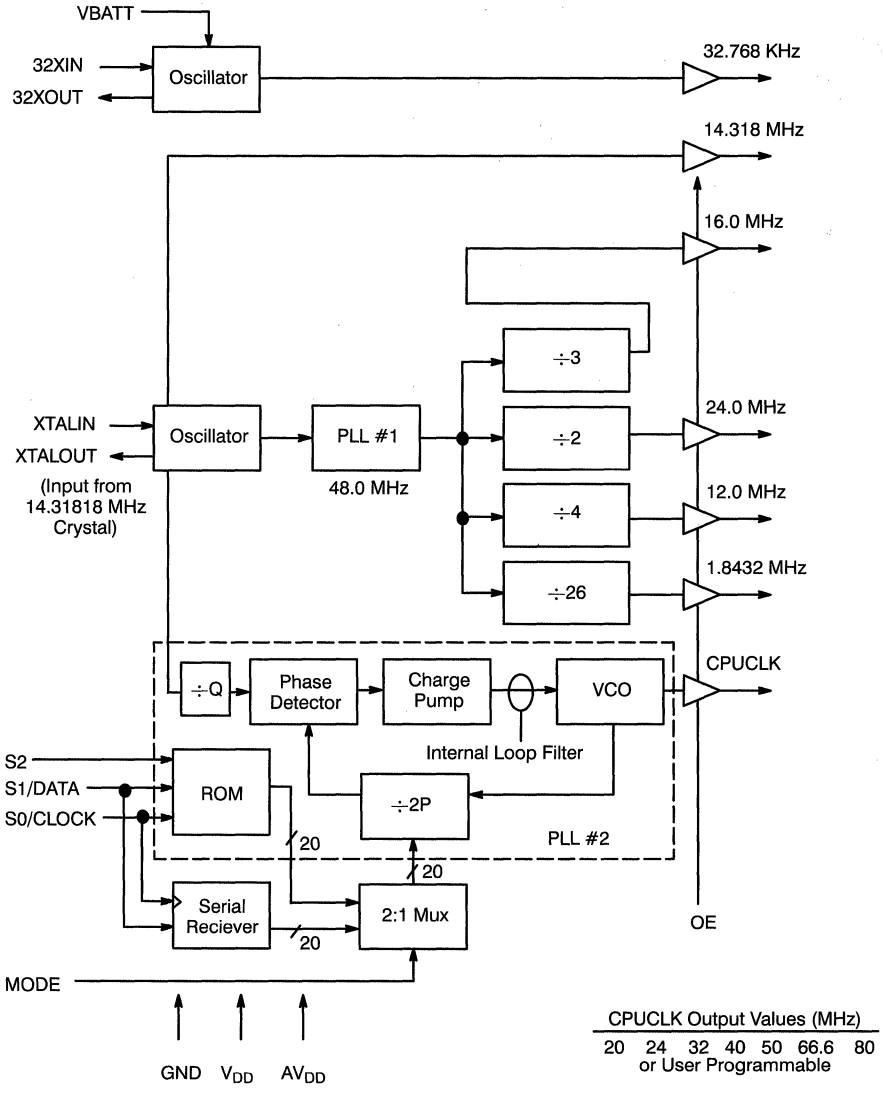
Logic Block Diagram



Pin Summary

Name	Number	Description
32XOUT[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 KHz Output
16 MHz	3	16 MHz Output
V_{DD}	4	+5V
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal.
14.318 MHz	8	14.318 MHz Output
1.8432 MHz	9	1.8432 MHz Output
CPUCLK	10	CPUCLK clock output (See *Table 2.*)
MODE	11	MODE=0, CPUCLK is in programmable mode MODE=1, CPUCLK depends on S2, S1, and S0
12.0 MHz	12	12.0 MHz Output
24.0 MHz	13	24.0 MHz Output
S0/CLOCK	14	MODE=0, S0 is serial clock input line for CPUCLK MODE=1, S0 is select line for CPUCLK (Internal pull-up)
S1/DATA	15	MODE=0, S1 is serial data input line for CPUCLK MODE=1, S1 is select line for CPUCLK (Internal pull-up)
AV_{DD}	16	+5V to Analog Core
S2	17	MODE=0 and S2 =1; CPUCLK=(14.31818 MHz) reference frequency MODE=1, S2 is select line for CPUCLK (Internal pull-up)
OE	18	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V_{BATT}	19	Battery backup voltage
32XIN[1]	20	Oscillator input from a 32.768 kHz parallel-resonant crystal.

General Considerations

Fixed Frequency Oscillator Operation

Table 1 describes each output.

Table 1. Fixed Frequency Oscillator Operation

Output Clock Function	Desired Frequency (MHz)	Actual Frequency (MHz)	PPM Error
Real-Time Clock[2]	32.768 kHz	32.768 kHz	0
System Bus[3]	14.318	14.318	0
Int. Bus Clock[4]	16.000	15.983	1058
Keyboard Clock[5]	12.000	11.987	1058
Floppy Disk Clock[6]	24.000	23.975	1058
Serial Port[7]	1.843	1.844	543

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.
2. Pass-through 32.768 kHz XTAL.
3. Pass-through 14.31818 MHz XTAL.
4. Output = 47.94295/3.
5. Output = 47.94295/4.
6. Output = 47.94295/2.
7. Output = 47.94295/26.

CPUCLK Programmable Oscillator: Selection Mode

CPUCLK offers a programmable output based on two modes of operation. The first mode uses three select lines to select one of eight different preset frequencies, while the other mode allows the user to program any desired frequency between 10 MHz and 80 MHz. The two different modes are controlled by the MODE signal.

When MODE=1, the select lines can be changed to choose different frequencies. When this occurs, PLL #2 will immediately seek the newly selected frequency as shown in the following table. During the transition period, the CPUCLK output will not glitch.

Table 2. CPUCLK Output with MODE=1

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error
0	0	0	20.000	20.0454	2272
0	0	1	24.000	23.9746	1058
0	1	0	32.000	32.0455	1422
0	1	1	40.000	40.0909	2272
1	0	0	50.000	49.9923	154
1	0	1	66.667	66.5962	57
1	1	0	80.000	80.1818	2272
1	1	1	100.000[8]	99.8182	1818

CPUCLK Programmable Oscillator: Serial Mode

When MODE=0, CPUCLK enters its programmable mode. Signals S0 (clock) and S1 (data) become a serial interface, allowing a 20-bit number to be shifted in. In ICD2023 programmable oscillator (CPUCLK) requires a 20-bit programming word (W). This word contains 4 fields:

Table 3. Programming Word Bit Fields

Field	# of Bits
Index (I)[9]	4
P Counter value (P)	7
Mux (M)	3
Q Counter Value (Q)[10]	6

If a signal S2=1 and MODE=0, then the reference frequency (14.31818 MHz) is multiplexed to the CPUCLK output. This enables a glitch-free transition to the reference frequency while the VCO stabilizes.

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P'=P-3 \quad Q'=Q-2$$
$$f_{(VCO)}=2 \times f_{(REF)} \times P/Q$$

where $f_{(REF)}$=Reference frequency=14.31818 MHz.

The value of $f_{(VCO)}$ should be kept between 40 MHz and 80 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. The mux bits allow a post-divide of the higher VCO to bring the output to those desired values below 40 MHz.

Table 4. Mux Bits M_0-M_1

M_1	M_0	Divisor
0	0	16
0	1	4
1	0	2
1	1	1

The M2 mux bit is used to select which one of the two Phase-Locked Loops is to be utilized in the CPUCLK output. Normally, the PLL #2 section (see Logic Block Diagram) is used. However, if the desired output frequency requires $f_{(VCO)}$ to be set to 48 MHz, then PLL #1 section should be used. This both reduces power consumption (since only one VCO is activated) and eliminates the possibility of jitter which can arise when two VCOs of the same frequency beat (heterodyne) against each other.

Table 5. Mux Bits M_2

M_1	CPUCLK
0	PLL #2
1	PLL #1 (48 MHz)

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be should be chosen from *Table 6*. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

Table 6. Index Field (I)

I	$f_{(VCO)}$ MHz
0001	40.0–47.5
0010	47.5–52.2
0011	52.2–56.3
0100	56.3–61.9
0101	61.9–65.0
0110	65.0–68.1
0111	68.1–80.0
1111	Turn off VCO

If the desired VCO frequency lies on a boundary in the table (if it is exactly the upper limit of one entry and the lower limit of the next) then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. Contact your local Cypress representative for more information.

Notes:

8. Duty cycle specs not guaranteed above 80 MHz.
9. MSB (Most Significant Bits).
10. LSB (Least Significant Bits).

Programming Constraints

There are five primary programming constraints the user must be aware of:

Table 7. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	14.31818 MHz	14.31818 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	40 MHz	80 MHz
Q	3	65
P	4	130

The constraints have to do with trade-offs between optimum speed and lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the *BitCalc* program all of these constraints become transparent.

ICD2023 Programming Example

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz<40 MHz, double it to 79.0 MHz. Set M2, M1 and M0 to 0, 1 and 0, respectively. Set I to 0111. The result:

$$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$$
$$P/Q=2.7857$$

Several choices of P and Q are available:

Table 8. P and Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 ppm).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

and the full programming word, W is:

W=I, P', M, Q'=0111, 1001101, 010, 011011
=01111001101010011011 (79a9bH)

A LOW-to-HIGH transition on S0 is used to shift the programming word W into S1 as a serial bit stream, LSB first. (See the set-up and hold timing specifications elsewhere in this datasheet.) If more than 20 shifts are performed, only the last 20 data bits received will be retained.

Output Frequency Accuracy

The accuracy of the ICD2023 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2023 are an integral fraction of the input reference frequency:

$$f_{(OUT)}=2 \times f_{(REF)} \times P/Q$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2023 normally produces an output frequency within 0.1% of the target frequencies listed. This is more than sufficient to meet standard motherboard requirements. Specifics regarding accuracy are available from the output of the *BitCalc* program.

Three-State Output Operation

The OE signal, when pulled LOW, will three-state all the clock output lines (except 32.768 kHz). This supports wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

V_{BATT}

The V_{BATT} input powers the Real-Time Clock Oscillator (RTC). The back-up power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable. If the 32 kHz output is not used, all related inputs and outputs and V_{BATT} should be grounded.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical=3.0 Volts	2.0	5.0	V
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{OH-32}	32.768 kHz Output HIGH				V
V_{OL-32}	32.768 kHz Output LOW				V
V_{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD}-0.5V$		150	µA
I_{IL}	Input LOW Current	V_{IL} = +0.5V		−250.0	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Supply Current	V_{DD} = Max., fully loaded output, typical = 40[11]	25	65.0	mA
I_{BATT}	Backup Battery Current	V_{BATT} = 3V, fully loaded output, typical = 8 µA		50	µA

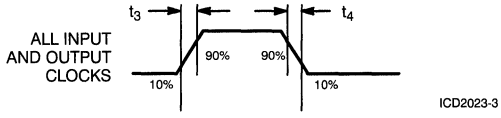
Switching Characteristics Over the Operating Range[12]

Parameter	Description	Test Conditions	Min.	Max.	Unit
	CPUCLK	Clock Output	10	80	MHz
t_1	Ref Frequency	Reference Oscillator nominal value		14.318	MHz
t_2	Duty Cycle	Duty cycle for the outputs defined as $t_{2A} \div t_{2B}$	40%	60%	
t_3	Rise Time	Rise time for the outputs into a 25 pF load		4	ns
t_4	Fall Time	Fall time for the outputs into a 25 pF load		4	ns
t_5	Set-Up Time	Delay required after MODE goes LOW prior to starting the S0 clock line		0	ns
t_6	Cycle Time	Minimum cycle time for the S0 clock	200		ns
t_7	Set-Up Time	Time required for the data to be valid prior to the rising edge of S0/CLOCK	10		ns
t_8	Hold Time	Time required for the data to remain valid prior to the rising edge of S0/CLOCK	5		ns
t_9	Clk Unstable	Time CPUCLK remains valid after MODE signal goes LOW		0	ns
t_{10}	Clk Stable	Time required for the CPUCLK to become valid after last S0/clock edge		10	msec
t_{11}	Clk Unstable	Time the output oscillators remain valid after the S0, S1 or S2 select signals change value		0	ns
t_{12}	Clk Stable	Time required for the outputs to become valid after the S0, S1, or S2 signals change value		10	msec
t_{13}	Three-State	Time for the outputd to go into three-state mode after OE signal assertion		12	ns
t_{14}	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH		12	ns

Notes:
11. CPUCLK = 66 MHz and inputs at GND or V_{DD}.
12. Input capacitance is typically 10 pF, except for the crystal pads.

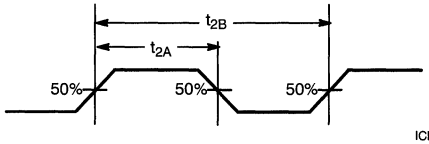
Switching Waveforms

Rise and Fall Times



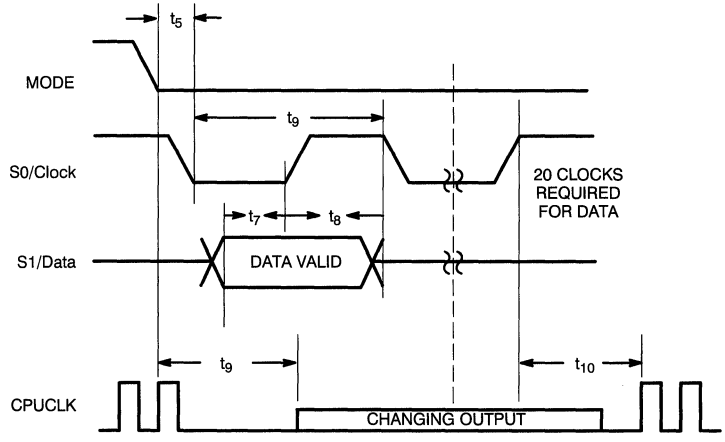
ICD2023-3

Duty Cycle Timing



ICD2023-4

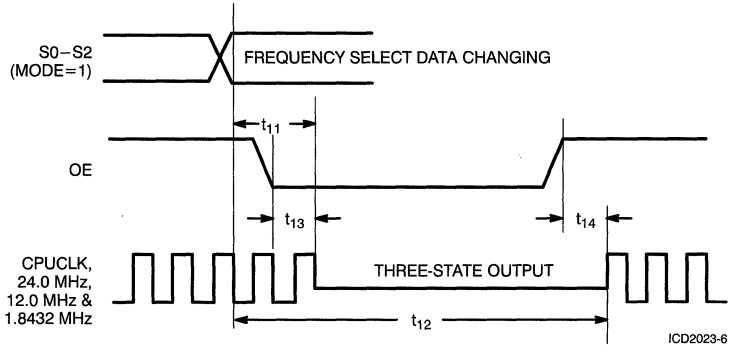
Serial Programming Timing



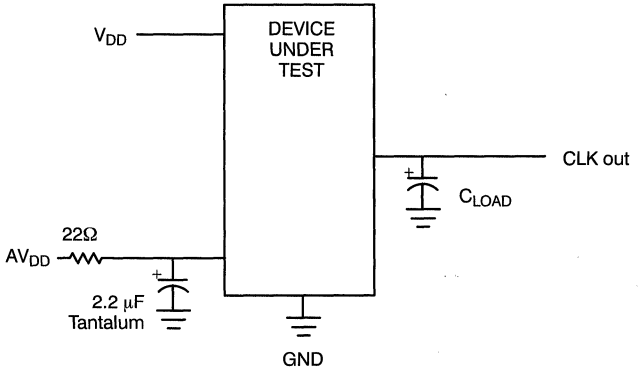
ICD2023-5

Switching Waveforms (continued)

State Timing



Test Circuit



Ordering Information[13]

Ordering Code	Package Name	Package Type	Operating Range
ICD2023	S5	20-Pin SOIC	Commercial[14]

Note:
13. Please contact your local Cypress representative.
14. 0°C to +70°C

Document #: 38–00397

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ICD2025

Motherboard Clock Generator

Features

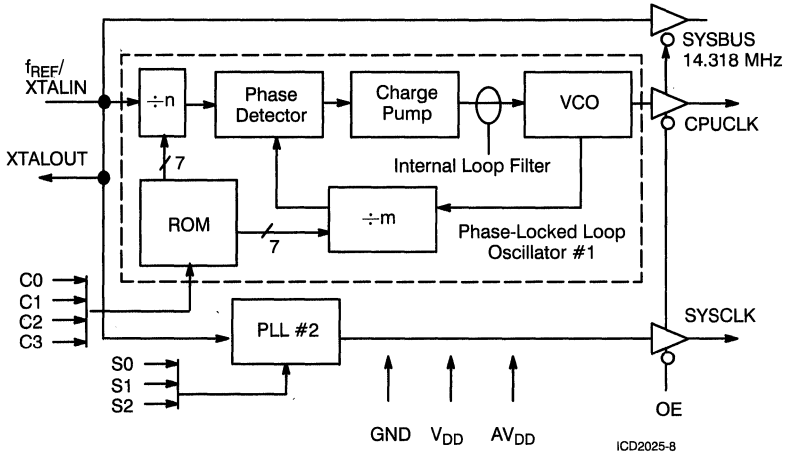
- **Three independent clock outputs: separate CPUCLK, SYSCLK and Buffered Reference Clock**
- **Ideally suited for 386/486 motherboard applications**
- **Phase-locked loop output range of 1.843 MHz – 100 MHz**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Three-state oscillator control disables outputs for test purposes**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package**

Functional Description

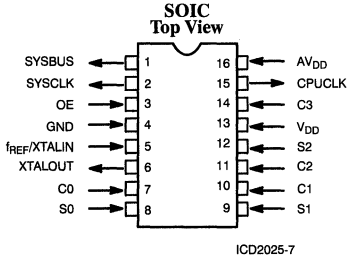
A modern personal computer motherboard often requires many different crystal can oscillators. The System Logic family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit borad space required.

The ICD2025 is a low-cost approach to the generation of the 3 necessary clocks required by any PC motherboard.

Logic Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
SYSBUS	1	Buffered 14.31818 MHz crystal output (z)
SYSCLK	2	System clock output (see *Table 2*)
OE	3	Output Enable three-states output when signal is LO. (pin has internal pull-up)
GND	4	Ground
f_{REF}/ XTALIN[1]	5	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	6	Oscillator output to a reference crystal.
C0	7	CPUCLK Select signal—Bit 0 (internal pull-up)
S0	8	SYSCLK Clock Select signal—Bit 0 (internal pull-up)
S1	9	SYSCLK Select signal—Bit 1 (internal pull-up)
C1	10	CPUCLK Select signal—Bit 1 (internal pull-up)
C2	11	CPUCLK Select signal—Bit 2 (internal pull-up)
S2	12	SYSCLK Select signal—Bit 2 (internal pull-up)
VDD	13	+5V to I/O Ring
C3	14	CPUCLK Select signal—Bit 3 (internal pull-down)
CPUCLK	15	CPU Clock Output (See CPUCLK Selection Table)
AVDD	16	+5V to Analog Core

Available Frequencies (MHz)

SYSCLK	CPUCLK
1.843	16.000
3.686	20.000
8.000	25.000
12.000	32.000
18.432	33.333
20.000	40.000
24.000	50.000
32.000	66.667
	80.000
	100.000

Note:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

General Considerations

CPU and System Clock Oscillator Selection

The frequency value of the CPU clock output (CPUCLK) is selected by the four CPU clock select inputs: C0, C1, C2, and C3. This feature allows the ICD2025 to support different CPU speeds. The frequency value of the system clock output (SYSCLK) is selected by the three system clock selection inputs: S0, S1, and S2. The selection tables are shown in *Tables 1* and *2*.

At any time during operation, the select lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the 14.31818 MHz reference signal until the PLL settles to the new frequency. The timing for this transition is shown in AC Characteristics.

Table 1. CPUCLK Selection

C3	C2	C1	C0	Word	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	0	0	40.000	39.812	4734
0	0	0	1	1	80.000	79.623	4734
0	0	1	0	2	33.333	33.322	320
0	0	1	1	3	66.667	66.645	335
0	1	0	0	4	25.000	25.000	0
0	1	0	1	5	50.000	50.000	0
0	1	1	0	6	16.000	15.923	4848
0	1	1	1	7	32.000	31.846	4848
1	0	0	0	8	20.000	19.906	4734
1	0	0	1	9	100.000	99.840	1600
1	0	1	0	10	40.000	39.812	4734
1	0	1	1	11	80.000	79.623	4734
1	1	0	0	12	33.333	33.322	320
1	1	0	1	13	66.667	66.645	335
1	1	1	0	14	25.000	25.000	0
1	1	1	1	15	50.000	50.000	0

Table 2. SYSCLK Selection

S2	S1	S0	Word	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	0	18.432	18.431	62
0	0	1	1	20.000	20.003	167
0	1	0	2	24.000	23.998	80
0	1	1	3	1.843	1.843	144
1	0	0	4	12.000	11.999	80
1	0	1	5	8.000	8.001	167
1	1	0	6	3.686	3.687	144
1	1	1	7	32.000	32.005	167

Output Frequency Accuracy

The accuracy of the ICD2025 output frequencies depends on the target output frequencies. The tables within this document contain target frequencies that differ from the actual frequencies produced by the clock synthesizer.

The output frequencies of the ICD2025 are an integral fraction of the input (reference) frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times {}^{P}/_{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2025 always produces an output frequency within 0.1% of the target frequencies listed, which is more than sufficient to meet standard system logic requirements. (Actual values are given in the tables.)

Three-State Output Operation

The OE signal, when pulled LOW, will three-state the SYSCLK, CPUCLK, and SYSBUF output lines. This supports procedures such as automated testing, where the clock must be disabled. The OE signal contains an internal pull-up but should be tied to V_{DD} if not used.

Short-term stability (also called bit-jitter) is a manifestation of the frequency synthesis process. The Cypress/IC Designs frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the dance of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC Designs families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough for system logic applications.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	ICD2025 Min.	ICD2025 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Wxcept crystal inputs		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IL} = 0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	Inputs @ V_{DD} or GND		60	mA
I_{ADD}	Analog Power Supply Current			6	mA

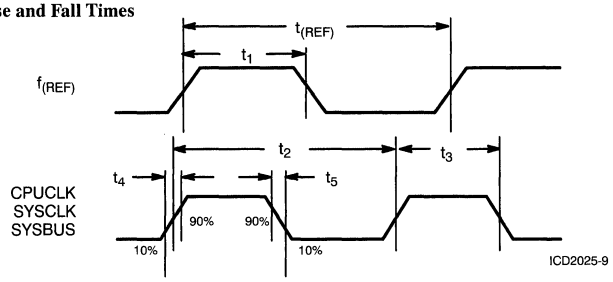
Switching Characteristics Over the Operating Range[2]

Parameter	Name	Drscription	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value	4	14.318	26	MHz
$t_{(REF)}$	Ref Clock Period	1 ÷ $f_{(REF)}$	38.5	69.8	2500	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_1 \div t_{(REF)}$	25%	50%	75%	
t_2	Output Period	CPUCLK output value	10 100 MHz		544 1.84 MHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs defined as $t_3 \div t_2$ (measured at 2.5V)	40%		60%	
t_4	Rise Time	Rise time for the outputs into a 25 pF load			4	ns
t_5	Fall Time	Fall time for the outputs into a 25 pF load			4	ns
t_6	Three-State	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_7	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_{MUXREF}	Clk Stable	Time required for the outputs to become valid after C0−C3 or S0−S2 select signals change value	3.4	5	6.9	msec
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_8	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3\frac{t_{(REF)}}{2}$	ns
t_9	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3\frac{t_{freq2}}{2}$	ns

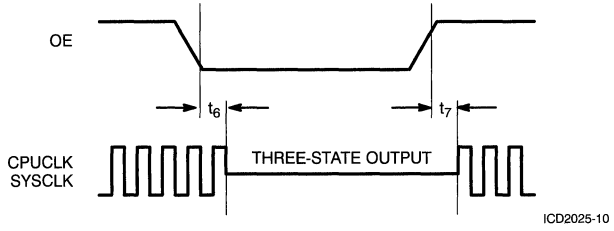
Note:
2. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

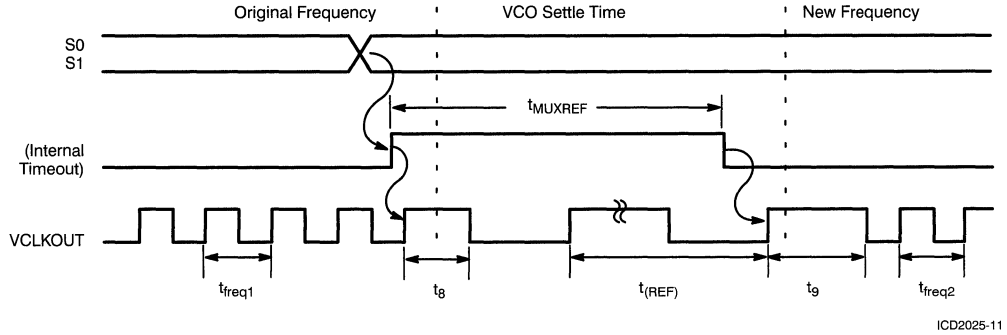
Rise and Fall Times



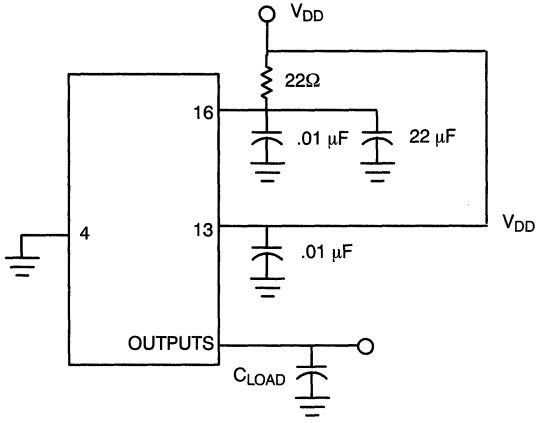
Three-State Timing



Selection Timing



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information[3]

Ordering Code	Package Name	Package Type	Operating Range
ICD2025	S1	16-Pin SOIC	Commercial[4]

Note:
3. Contact your local Cypress representative.
4. 0°C to +70°C

Example: order ICD2025SC for the ICD2025, 16-pin plastic SOIC, commercial temperature range device.

Document #: 38–00398

PC Motherboard Clock Generator

Features

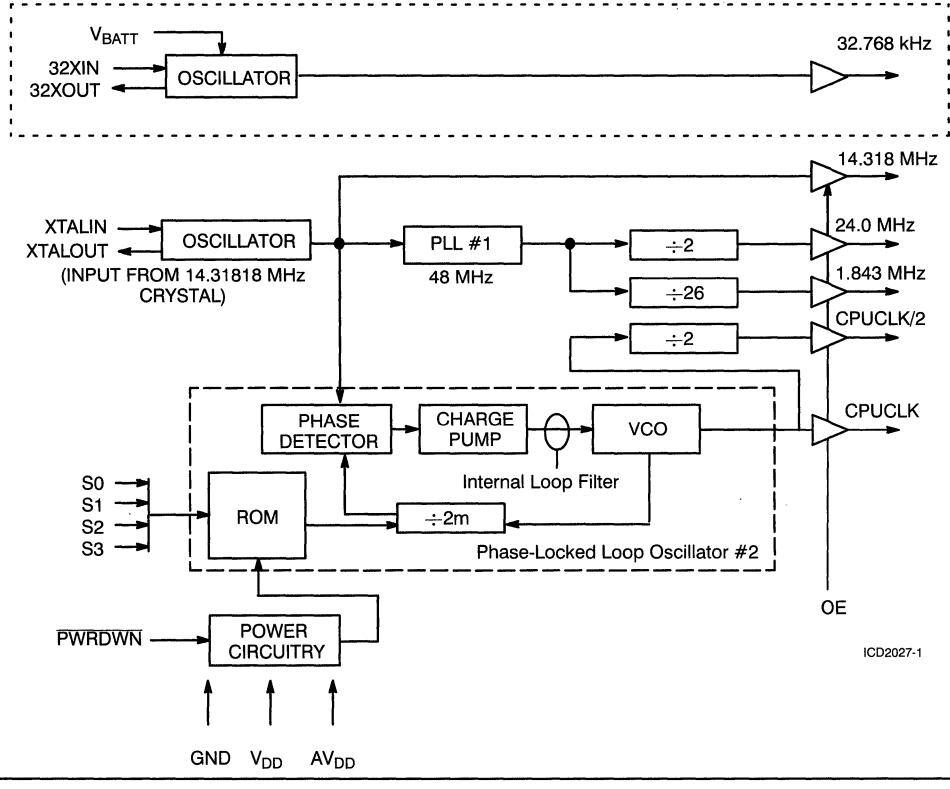
- **Six clock outputs handle all clocking requirements for personal computer motherboards**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Frequency range: 760 kHz to 100 MHz with 50% duty cycle**
- **Two power-down modes—hardware pin and software programmable**
- **Concurrent and low skew ÷1 and ÷2, CPUCLK outputs**
- **Ideally suited for desktop PC, laptop, and notebook applications**
- **Battery input maintains 32.768 kHz clock during power-down**
- **Three-state oscillator control disables outputs for test purposes**
- **Sophisticated internal loop-filter requires no external components**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

Functional Description

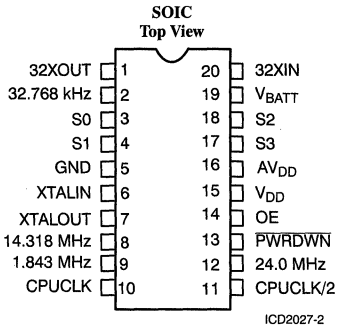
A modern personal computer motherboard often requires as many as seven different crystal can oscillators per printed circuit board. A new family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2027 PC Motherboard Clock Generator offers two oscillators, two phase-locked loops, and six different outputs in a single package. Four of the outputs are of a fixed value, while the other two may be changed "on the fly" to any one of 16 preset frequency values between 760 kHz and 100 MHz. The ICD2027 is ideally suited for use in laptop/notebook designs due to its dual power-down modes. The ICD2027 also requires no support from the motherboard chip set and outputs all six frequencies concurrently.

Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
32XOUT[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 kHz clock output
S0	3	Input select line 0 for CPUCLK (pin has internal pull-down)
S1	4	Input select line 1 for CPUCLK (pin has internal pull-down)
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal.
14.318 MHz	8	14.31818 MHz clock output
1.8432 MHz	9	1.8432 MHz clock output
CPUCLK	10	CPUCLK programmable clock output (See *Table 1* for values.)
CPUCLK/2	11	Half the frequency of CPUCLK. Output is phase-coherent with the CPUCLK output.
24.0 MHz	12	24.0 MHz clock output
$\overline{\text{PWRDWN}}$	13	Puts device in Power-Down mode when signal is pulled LOW (pin has internal pull-down)
OE	14	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V_{DD}	15	+5V to I/O ring
AV_{DD}	16	+5V to analog core
S3	17	Input select line 3 for CPUCLK (pin has internal pull-down)
S2	18	Input select line 2 for CPUCLK (pin has internal pull-down)
V_{BATT}	19	+2 to +5V for battery backup operation
32XIN[1]	20	Oscillator input from 32.768 kHz crystal

Note:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

General Considerations

CPUCLK Selection

CPUCLK is the selectable output. It uses four select lines (S0, S1, S2, S3) to select 1 of 16 different preset frequencies, as shown in *Table 1* (Reference Frequency = 14.31818 MHz).

Table 1. CPUCLK ROM Selection Outputs[2]

S3	S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	0	0.7950[3]	$f_{(REF)}/18$	0
0	0	0	1	0.7950	$f_{(REF)}/18$	0
0	0	1	0	33.3000	33.2981	57
0	0	1	1	0.7600	0.7599	75
0	1	0	0	2.0000	2.0003	167
0	1	0	1	3.0000	2.9968	1057
0	1	1	0	8.0000	8.0013	167
0	1	1	1	10.0000	10.0227	2273
1	0	0	0	20.0000	20.0455	2273
1	0	0	1	24.0000	23.9747	1057
1	0	1	0	32.0000	32.0053	167
1	0	1	1	40.0000	40.0909	2273
1	1	0	0	50.0000	50.0000	0
1	1	0	1	66.6000	66.5962	57
1	1	1	0	80.0000	80.1818	2273
1	1	1	1	100.0000	99.8182	1818

Fixed Frequency Operation

Table 2 describes each output.

Table 2. Fixed Frequency Oscillators

Output Clock Function	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
Real-Time Clock[4]	32.768 kHz	32.768 kHz	0
System Bus[5]	14.31818	14.31818	0
Floppy Disk Clock	24.00000	23.97470	1058
Serial Port	1.84320	1.84420	1058

Notes:
2. The select lines have internal pull-downs so that in a system power-down situation, the power-down mode is chosen in the CPUCLK table as the default. Therefore, upon power-up, one of the select lines must be pulled HIGH.
3. Soft power-down mode.
4. Pass-through 32.768 kHz XTAL.
5. Pass-through 14.31818 MHz XTAL.

Power-Down Operation

There are two power-down modes within the ICD2027. The first is the hardware mode. When Pin 13 is pulled LOW ($\overline{PWRDWN}$=0), the part is immediately forced into its lowest power mode. This shuts down everything but the 32.768-kHz oscillator and its output. All power is now supplied by the V_{BATT} input. For minimum power consumption in power-down mode, all select lines should be set LOW and OE should be set HIGH

The second mode is a programmable soft power-down mode. This mode shuts down the two phase-locked loops and all outputs except for the CPUCLK output, which runs at 795 kHz—a frequency sufficient to refresh dynamic RAMs (see *Table 3*).

Table 3. Soft Power-Down Mode (S0−S3=0000)

Output Signal	Status
32.768 kHz	32.768 kHz
CPUCLK	795.00 kHz
CPUCLK/2	(shutdown)
14.318 MHz	(shutdown)
1.8432 MHz	(shutdown)
24.000 MHz	(shutdown)

Three-State Output Operation

The OE signal, when pulled LOW, will three-state all the clock output lines (except 32.768 kHz). This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required.

Skew-Free ÷2 on CPUCLK/2

The CPUCLK/2 output is available concurrently as a ÷2 of the desired CPUCLK output. The ÷2 output is also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 1 ns of skew between the two outputs, with 2 ns guaranteed worst case.

V_{BATT}

The V_{BATT} input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable. If the 32-kHz output is not used, all related inputs and outputs and V_{BATT} should be grounded.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical = 3.0V	2.0	5.0	V
V_{IH}	Input HIGH Voltage	Except Crystal Inputs	2.0		V
V_{IL}	Input LOW Voltage	Except Crystal Inputs		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
I_{IH}	Input HIGH Current	V_{IH} = 5.25V		150	µA
I_{IL}	Input LOW Current	V_{IL} = 0V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	Inputs @ V_{DD} or GND	20	65	mA
I_{DD-PD}	Soft Power-Down Current			7.5	mA
I_{BATT}	Backup Battery Current	Typical = 5 µA		15	µA

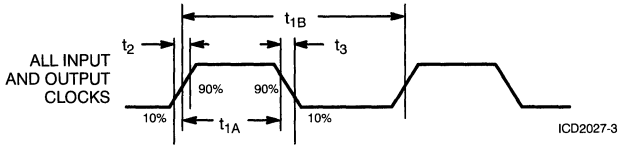
Switching Characteristics[6]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
f_{REF}	Reference Frequency	Reference input normal value		14.318		MHz
$t_{(REF)}$	Reference Period	$1 \div f_{(REF)}$		69.8		ns
t_1	Duty Cycle	Duty cycle for the output clock defined as $t_{1A} \div t_{1B}$	40%		60%	
t_2	Rise Time	Rise time for the outputs into a 25-pF load			4	ns
t_3	Fall Time	Fall time for the outputs into a 25-pF load			4	ns
t_4	Three-state	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_5	clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_6	CPUCLK/2 Skew	Skew delay between CPUCLK and CPUCLK/2 outputs		1	2	ns
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_7	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
t_8	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_{MUXREF}		Time for VCO to settle between changes			6.2	msec

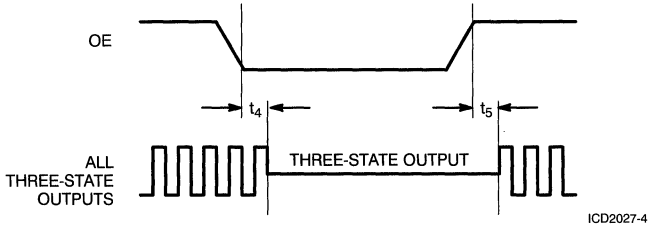
Note:
6. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

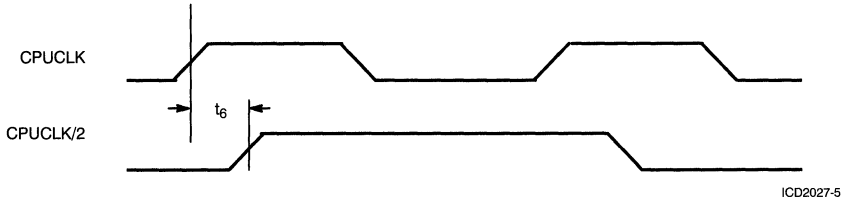
Rise and Fall Times



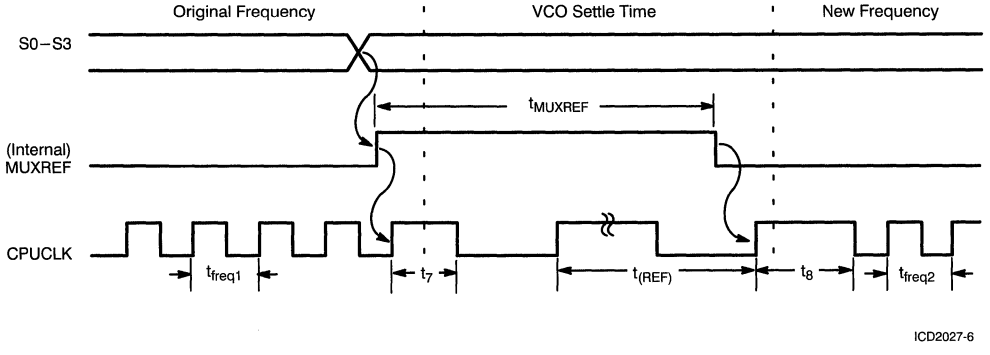
Three-State Timing



CPUCLK Skew



Select Timing



Ordering Information

Ordering Code	Package Name	Package Type	Temperature Range	CPUCLK ROM Option
ICD2027	S5	20-Pin SOIC	C=Commercial=0°C to +70°C	1

Example: Order ICD2027SC−1 for the ICD2027, 20-pin plastic SOIC, commercial temperature range device which uses the standard CPUCLK ROM Option 1 table of frequency decodes. Custom CPUCLK ROM decodes are available by special order. Please call your local Cypress representative.

Document #: 38−00399

ICD2028

PC Motherboard Clock Generator

Features

- **Eight independent clock outputs handle all clocking requirements for personal computer motherboards**
- **CPU clock frequency range: 10 MHz to 100 MHz with user-defined duty cycle**
- **Four user-configurable outputs**
- **Skew-free CPU clock, CPU clock ÷2, and buffered CPU clock options on configurable outputs**
- **Ideally suited for desktop PCs**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Sophisticated internal loop-filter requires no external components**
- **Battery input maintains 32.768 kHz clock during power-down**
- **Three-state oscillator control disables outputs for test purposes**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

Functional Description

A modern personal computer motherboard often requires as many as seven different crystal can oscillators. The System Logic family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2028 is a second-generation PC Motherboard Clock Generator built on the foundation of the industry-standard and most widely-used ICD2023. The ICD2028 offers most of the features of the ICD2023, as well as some important enhancements:

- An additional VCO
- An additional clock output
- Four customer-configured outputs which can be configured to have
  - — A skew-free divided-by-two CPU clock
  - — An additional skew-free CPU clock
- User-definable CPUCLK output duty cycle

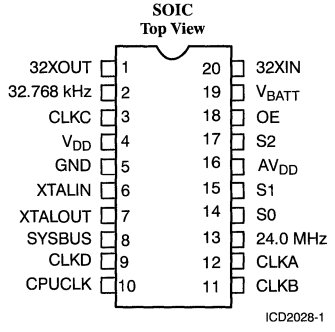
Because today's desktop PCs must support a myriad of new requirements, and each company's implementation tends to be unique, the most important new feature of the ICD2028 is its ability to tailor four of the outputs to the individual needs of today's system logic design engineer, and to configure the CPUCLK duty cycle for special microprocessor needs.

The ICD2028 was specifically designed to support such demanding clock requirements as:

- 486 and Pentium™ microprocessors both with and without clock doublers
- New single-chip system logic chip sets
- Super I/O combo chips
- New high-density floppy disk drive controllers

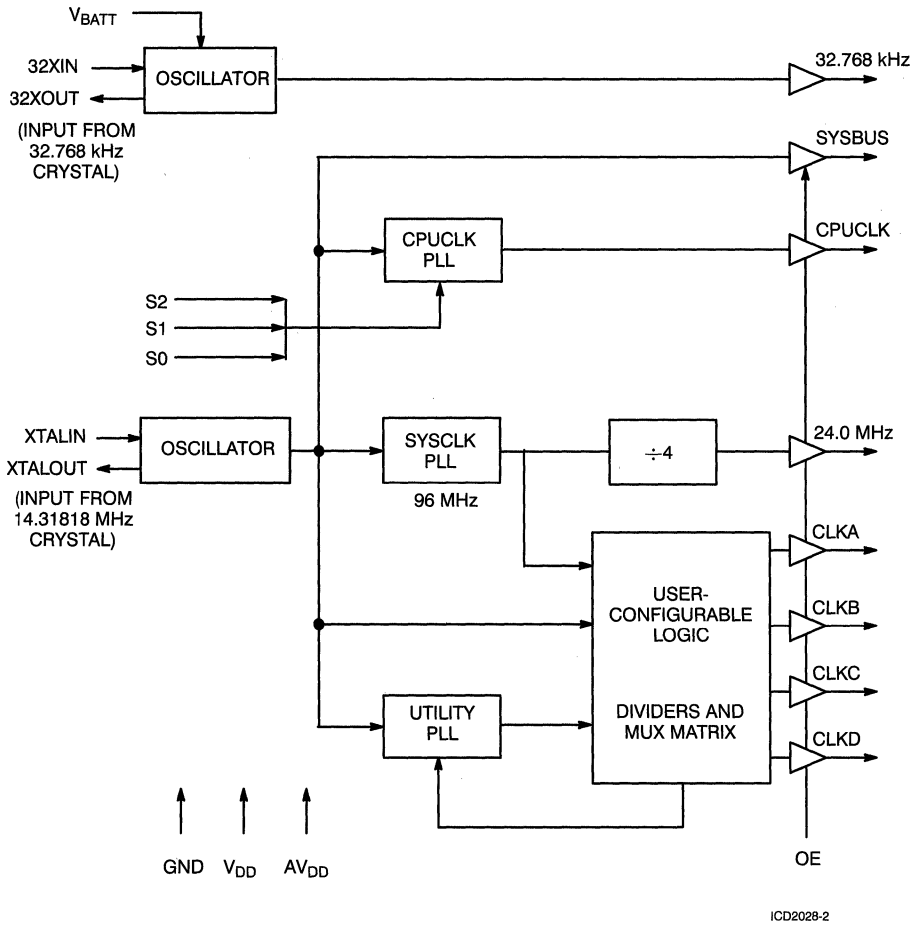
The ICD2028 consists of two crystal-controlled oscillators, three phase-locked loops, and eight different outputs in a single package. To sum up, the greatest asset of the ICD2028 lies in its ability to serve as the single source of all clocking requirements in modern desktop PCs.

Pin Configuration



Pentium is a trademark of Intel Corporation.

Block Diagram



Pin Summary

Name	Number	Description
32XOUT[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 kHz clock output
CLKC	3	User-configurable clock output (See *User-Selectable Clock Options* for values.)
V_{DD}	4	+5V
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal.
SYSBUS	8	Buffered 14.31818 MHz crystal output
CLKD	9	User-configurable clock output (See *User-Selection Clock Options* for values.)
CPUCLK	10	CPUCLK clock output (See *CPU Clock Selection* for values.)
CLKB	11	User-configurable clock output (See *User-Selection Clock Options* for values.)
CLKA	12	User-configurable clock output (See *User-Selection Clock Options* for values.)
24.0 MHz	13	24.0 MHz clock output
S0	14	Input select line 0 for CPUCLK (pin has internal pull-down)
S1	15	Input select line 1 for CPUCLK (pin has internal pull-down)
AV_{DD}	16	+5V to analog core
S2	17	Input select line 2 for CPUCLK (pin has internal pull-down)
OE	18	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V_{BATT}	19	+2 to +5V for battery backup operation; powers 32.768 kHz oscillator.
32XIN[1]	20	Oscillator input from a 32.768 kHz parallel-resonant crystal.

Note:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

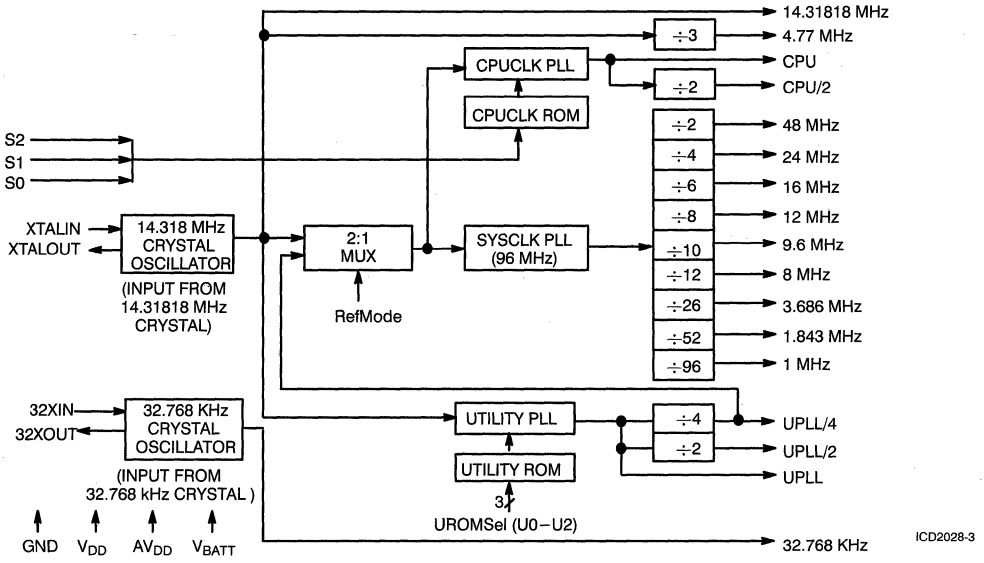


Figure 1. Inputs

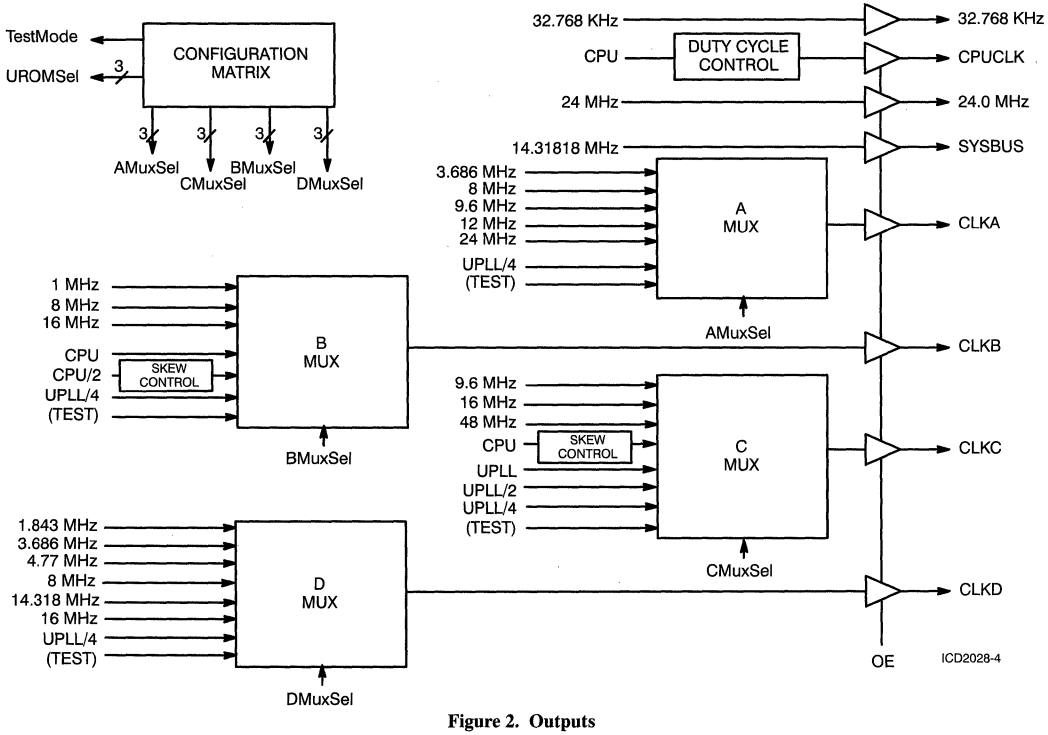


Figure 2. Outputs

User-Selectable Clock Options

System and Utility Clock Selection

The heart of the ICD2028 is the rich set of frequencies which are generated internally, encompassing most known system logic motherboard requirements. From this set of outputs, the user may select four output frequencies.

Through a proprietary technique, Cypress/IC Designs can quickly configure samples of any desired output pin configuration. The configuration process involves no NRE (non-recurring engineering) charges or prototype delays, as are commonly associated with masked ROM changes. Samples of user-configured ICD2028s can generally be made available in 24 hours.

Tables 1 and *2* list all the available internally generated system clocks on the CLKA, CLKB, CLKC, and CLKD outputs, as well as the Utility PLL output.

Table 1. System Clock Options

Clock Function	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)	Clock Source	Available on Pin (s)					
					CLKA	CLKB	CLKC	CLKD	SYSBUS	24.0 MHz
SYSCLK PLL	96.000	95.870	1361	SYSCLK						
	48.000	47.935	1361	SYSCLK/2			X			
Super Floppy	32.000	31.957	1361	SYSCLK/3	X	X				
Floppy Disk	24.000	23.967	1361	SYSCLK/4	X					X
Internal Bus	16.000	15.978	1361	SYSCLK/6		X	X	X		
System Bus	14.318	14.318	0	f_{REF}				X	X	
Keyboard	12.000	11.984	1361	SYSCLK/8	X					
	9.600	9.587	1361	SYSCLK/10	X		X			
Bus Clock	8.000	7.989	1361	SYSCLK/12	X	X		X		
	4.770	4.773	572	$f_{REF}/3$				X		
Alt. Comm. Port	3.686	3.687	242	SYSCLK/26		X		X		
Serial Port	1.843	1.844	242	SYSCLK/52				X		
Special CLK	1.000	0.999	1361	SYSCLK/96		X				

Table 2. Utility PLL Options

Clock Function	ROM Source[2]	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)	Clock Source[3]	Available on Pin (s)			
						CLKA	CLKB	CLKC	CLKD
Alt. Comm. Port	A & B	18.432	18.431	62	Utility PLL/4	X	X	X	X
	A & B	36.864	36.862	62	Utility PLL/2			X	
	A & B	73.728	73.723	62	Utility PLL			X	
Custom	A & B	14.746	14.748	144	Utility PLL/4	X	X	X	X
	A & B	29.492	29.495	144	Utility PLL/2			X	
	A & B	58.984	58.991	144	Utility PLL			X	
Custom	A & B	19.200	19.199	32	Utility PLL/4	X	X	X	X
	A & B	38.400	38.399	32	Utility PLL/2			X	
	A & B	76.800	76.798	32	Utility PLL			X	
Super I/O−1	B	32.000	31.997	102	Utility PLL/4	X	X	X	X
	B	64.000	63.994	102	Utility PLL/2			X	
	B	128.000	127.987	102	Utility PLL			X	
Super I/O−2	B	16.000	16.003	167	Utility PLL/4	X	X	X	X
	B	32.000	32.005	167	Utility PLL/2			X	
	B	64.000	64.011	167	Utility PLL			X	
Shut VCO	A & B	–	–	–	–				
	A & B	–	–	–	–				
	A & B	–	–	–	–				

Notes:
2. Refers to the two currently available ROM Options: A and B.
3. Each clock function outputs three separate frequencies: UPLL, UPLL/2 and UPLL/4.

CPU Clock Selection

The output frequency of the CPU clock oscillator (CPUCLK) is selected by the Clock Selection Inputs S0–S2. This lets the ICD2028 support different microprocessor speed configurations. There are two ROM options available, shown in *Table 3* and *Table 4*.

The selection lines can be changed at any time to select a new frequency. When this occurs, the internal phase-locked loop immediately seeks the new frequency. During the transition period (about 5 msec), the clock output is multiplexed glitch-free to the reference signal (14.318 MHz) until the PLL settles to the new frequency. The timing for this transition is shown in Electrical Characteristics.

Table 3. CPUCLK Output—ROM Option A

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	20.000	20.045	2272
0	0	1	24.000	23.967	1361
0	1	0	32.000	32.045	1422
0	1	1	40.000	40.091	2272
1	0	0	50.000	49.992	154
1	0	1	66.600	66.596	1058
1	1	0	80.000	80.182	2272
1	1	1	100.000	99.818	1822

Table 4. CPUCLK Output—ROM Option B

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	20.000	20.003	167
0	0	1	24.000	23.967	1359
0	1	0	60.000	59.974	429
0	1	1	40.000	40.007	167
1	0	0	50.000	50.000	0
1	0	1	66.600	66.645	331
1	1	0	80.000	80.013	167
1	1	1	100.000	99.840	1600

Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the equation I = C x V x f, where I=current, C=load capacitance (max. 25 pF), V=output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and f=output frequency in MHz.

To calculate total operating current, sum the following:

32.768 KHz –> C_{32} x V x .032 x 10^{-3} mA
14.318 MHz –> C_{14} x V x 14.318 x 10^{-3} mA
24.0 MHz –> C_{24} x V x 24 x 10^{-3} mA
CPUCLK –> C_{CPUCLK} x V x f_{CPUCLK} x 10^{-3} mA
CLKA –> C_{CLKA} x V x f_{CLKA} x 10^{-3} mA
CLKB –> C_{CLKB} x V x f_{CLKB} x 10^{-3} mA
CLKC –> C_{CLKC} x V x f_{CLKC} x 10^{-3} mA
CLKD –> C_{CLKD} x V x f_{CLKD} x 10^{-3} mA
Internal –> 17 mA

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5–10 pF loading, depending on the package type.

Some typical values are displayed in *Table 5*.

Table 5. Operating Current Typical Values

Frequency	Capacitive Load	Current (in mA)
		V_{DD}=5V
LOW	LOW	20
HIGH	LOW	35
HIGH	HIGH	65

General Considerations

V_{BATT}

The V_{BATT} input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable. If the 32-kHz output is not used, all related inputs and outputs and V_{BATT} should be grounded.

Three-State Output Operation

The OE signal, when pulled LOW, will three-state all the clock output lines (except 32.768 kHz). This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required.

Device Specifications

Standard Configurations

While the ICD2028 can easily be configured to the user's unique requirements, there are a few standard configurations available. These are defined in *Table 6*.

Table 6. Standard Configurations[4]

Signal Name	Pin #	−2 Configuration	−4 Configuration	−5 Configuration
Reference Crystal	–	14.318 MHz	14.318 MHz	14.318 MHz
Utility PLL	–	(Off)	(Off)	32.000 MHz
CPUCLK Duty Cycle	–	50%	50%	50%
ROM Option	–	A	B	B
CPUCLK	10	Available	Available	Available
SYSBUS	8	Available	Available	Available
24.0 MHz	13	Available	Available	Available
CLKA	12	12.000 MHz	12.000 MHz	12.000 MHz
CLKB	11	CPUCLK/2	CPUCLK/2	CPUCLK/2
CLKC	3	16.000 MHz	16.000 MHz	32.000 MHz (UPLL/4)
CLKD	9	1.843 MHz	1.843 MHz	1.843 MHz
32.768 kHz	2	Available	Available	Available

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C
Power dissipation ..... 750 mW

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical = 3.0 Volts	2.0	5.25	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	V_{DD}−0.5		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{OH-32}	32.768 kHz Output HIGH	I_{OH} = −0.5 mA	V_{BATT}−0.5		V
V_{OL-32}	32.768 kHz Output LOW	I_{OL} = 0.5 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	Except crystal inputs	−0.3	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	V_{DD} = Max., fully loaded output, typical = 35[5]	20	85	mA
I_{BATT}	Backup Battery Current	V_{BATT} = 3V, fully loaded output, typical = 5 µA		15	µA

Notes:

4. −2 Compatible with most 486 chip sets, while adding skew-free CPUCLK/2 support.
   −4 Supports Pentium™ processor requirements.
   −5 Provides 486 support and Super I/O (32 MHz) support.
5. CPUCLK = 66 MHz and inputs at GND or V_{DD}.

Pentium is a trademark of Intel Corporation.

Switching Characteristics[6]

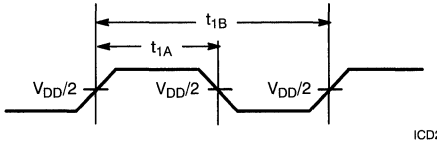
Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference input normal value		14.318		MHz
t_1	Input Duty Cycle	Duty cycle for the input oscillator defined as $t_1 = t_{1A} \div t_{1B}$	25%	50%	75%	
t_2	Output Period	Output frequency/period ranges (see tables under *User-Selectable Clock Options* for details)	8.3 100 MHz		2857 350 KHz	ns
t_3	Output Duty Cycle[7]	Duty cycle for the outputs, measured @ CMOS V_{TH} of $V_{DD} \div 2$	40%		60%	
t_4	Rise Times	Rise time for the outputs into a 25-pF load			4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load			4	ns
t_6	Three-state	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_7	clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_8	Buffered CPUCLK Skew	Skew delay between CPUCLK and buffered CPUCLK outputs, as measured @ CMOS V_{TH} of $V_{DD} \div 2$		<.25	1	ns
t_9	CPUCLK/2 Skew	Skew delay between CPUCLK and CPUCLK/2 outputs, as measured @ CMOS V_{TH} of $V_{DD} \div 2$		<.25	1	ns
t_A	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
t_B	t_{freq2} Mux Time[8]	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_{MUXREF}		Time for VCO to settle between changes		5		msec

Notes:

6. Input capacitance is typically 10 pF, except for the crystal pads.
7. Custom CPUCLK duty cycle may be special ordered. Contact your local Cypress representative for more information.
8. t_{freq2} dependent on frequency selected. freq1 and freq2 are frequencies on CPUCLK output before and after change in S0–S2.

Switching Waveforms

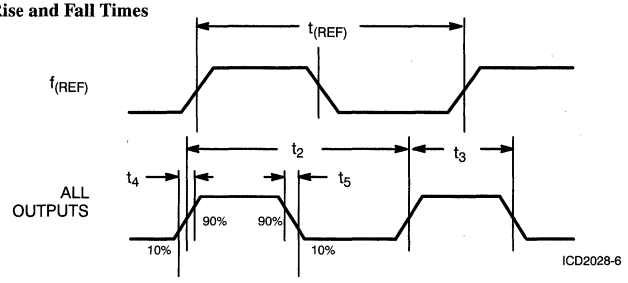
Duty Cycle Timing



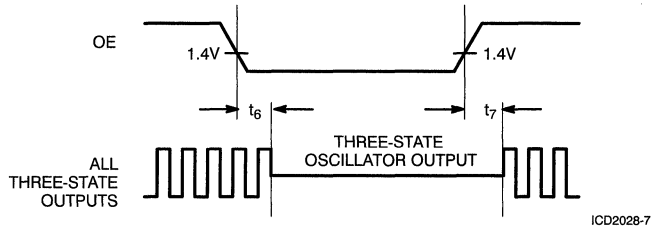
ICD2028-5

Switching Waveforms (continued)

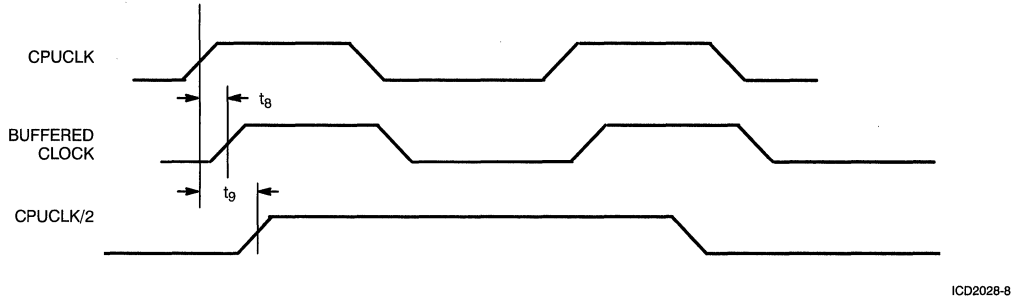
Rise and Fall Times



Three-State Timing

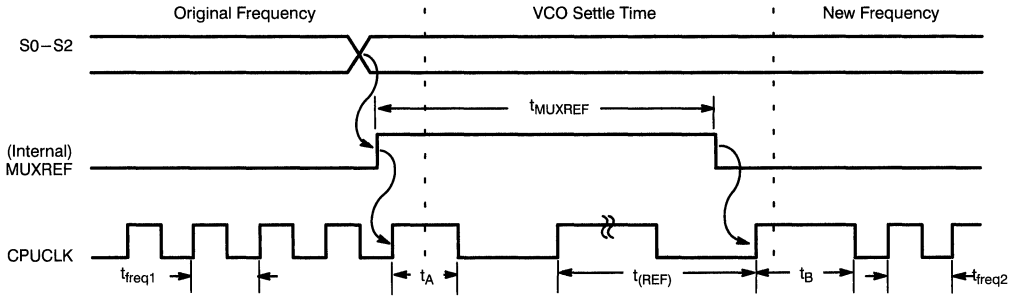


CPUCLK Skew



Switching Waveforms (continued)

Selection Timing



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
ICD2028	S5	20-Pin SOIC	C=0°C to +70°C @ V_{DD}=5V

Example: Order ICD2028SC–2 for the ICD2028, 20-pin plastic SOIC, 5V operating range device which uses the standard configuration code –2 (486 compatibility with CPUCLK/2 support). See *Table 6* for details on the standard configurations.

Standard packaging is in a surface-mount configuration. The ICD2028 is also available in a through-hole DIP configuration by special order. Please contact your Cypress representative for current availability and lead times.

Document #: 38–00400

ICD2028 Custom Configuration Order Form

Company Name _____ Contact _____

Telephone _____ Fax _____

Output Signals

(All frequencies in MHz unless otherwise noted)

(Circle one in each line, or fill in the blanks.)

Operating Voltage (V_{DD} & AV_{DD}): 5V

Dedicated Pins: 32.768 KHz 24.000

Reference Xtal & SYSBUS Output: 14.31818

CPUCLK (Select desired ROM Option line below.)

ROM Opt. A	[20.0	24.0	32.0	40.0	50.0	66.6	80.0	100.0]
ROM Opt. B	[20.0	24.0	60.0	40.0	50.0	66.6	80.0	100.0]

CPUCLK: Duty Cycle _____ % (default) (50%) Load _____ pF (25 pF) Frequency _____ MHz (10–100 MHz)

UtilityPLL/4	18.432	14.746	20.000	19.2000	32.000	16.000[1]	OFF
CLKA	3.692	8.000	9.600	12.000	24.000	–	UPLL/4
CLKB	1.000	8.000	16.000	–	CPU[2]	CPU/2[2]	UPLL/4
CLKC	9.600	16.000	48.000	CPU[2]	UPLL	UPLL/2	UPLL/4
CLKD	1.843	3.686	4.770	8.000	14.318	16.000	UPLL/4

IC Designs Assignment Configuration Code _____
(For IC Designs use only)

Notes:
1. Only available with ROM Option B.
2. Skew-controlled to CPUCLK output.

ICD2042A

Dual VGA Clock Generator

Features

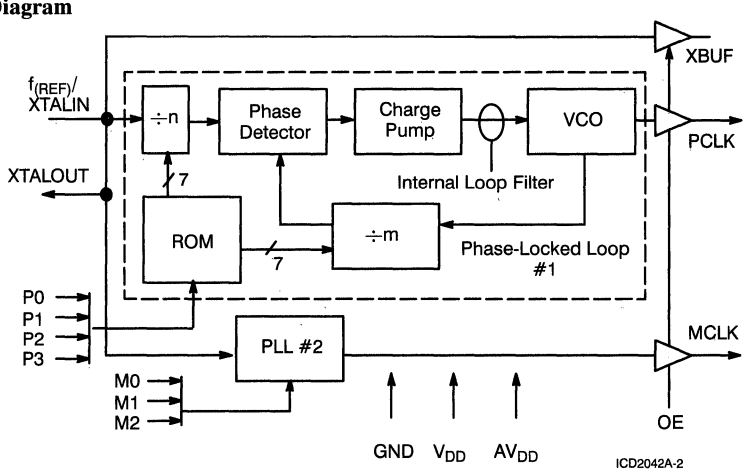
- **Three independent clock outputs: separate pixel and memory clocks and buffered reference clock**
- **Phase-locked loop output range of 1350 kHz – 120 MHz**
- **Phase-locked loop oscillator input derived from PC system bus or from single 14.318 MHz crystal**
- **Ideally suited for VGA, XGA, and 8514 graphics applications**
- **Sophisticated internal loop-filter requires no external components**
- **Three-state output control disables outputs for test purposes**
- **Change-on-the-fly frequency selection supports most popular VGA/8514 chip sets**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package**

Functional Description

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from Cypress/IC Designs replaces the large number of these oscillators required to build such multi-function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

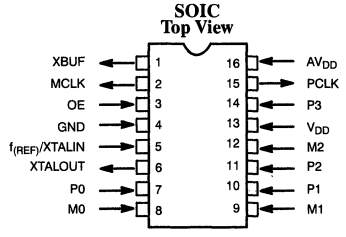
The ICD2042A Dual VGA Clock Generator supports new designs using the newer graphics chip sets which generate output frequency select information. The ICD2042A features two independent clock outputs for the pixel clock and the memory clock which are chosen via select lines. Additional features include three-stateable outputs and direct support for popular graphics chip set selection decodes.

Logic Block Diagram



ICD2042A-2

Pin Configuration



ICD2042A-1

Pin Summary

Name	Number	Description
XBUF	1	Buffered reference frequency output (14.318 MHz)
MCLK	2	Memory Clock output (see *Table 1*)
OE	3	Output Enable, three-states output when signal is LOW (pin has internal pull-up)
GND	4	Ground
$f_{(REF)}$/ XTALIN[1]	5	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.318-MHz crystal).
XTALOUT[1]	6	Oscillator output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
P0	7	Pixel Clock Select input—Bit 0 (internal pull-up)
M0	8	Memory Clock Select input—Bit 0 (internal pull-up)
M1	9	Memory Clock Select input—Bit 1 (internal pull-up)
P1	10	Pixel Clock Select input—Bit 1 (internal pull-up)
P2	11	Pixel Clock Select input—Bit 2 (internal pull-up)
M2	12	Memory Clock Select input—Bit 2 (internal pull-up)
V_{DD}	13	+5V to I/O Ring
P3	14	Pixel Clock Select input—Bit 3 (internal pull-down)
PCLK	15	Pixel Clock Output
AV_{DD}	16	+5V to Analog Core (special order: bond V_{DD} to AV_{DD} internally)

General Considerations

Design Recommendations

The ICD2061A, with its ability to program the output frequencies, is recommended for designs in which a fixed ROM would be inconvenient and/or the desired volume does not warrant a custom ROM.

The ICD2042A is currently a custom order only.

Pixel and Memory Clock Oscillator Selection

The output frequency value of the Pixel clock oscillator (PCLK) is selected by the four Pixel clock selection inputs: P0, P1, P2, and P3. This feature allows the ICD2042A to support different video configurations. The output frequency value of the Memory clock oscillator (MCLK) is selected by the three Memory clock selection inputs: M0, M1, and M2. The selection table is shown in *Table 1*.

At any time during operation, the select lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the reference signal until the PLL settles to the new frequency.

Normally, the MCLK select lines are hard-wired during manufacturing to correspond to the desired memory speed. A different memory clock frequency output may be generated by changing the memory select lines of the ICD2042A. The timing for this transition is shown in AC Characteristics.

Note:

1. For best accuracy, use a parallel-resonant crystal, asume C_{LOAD} = 17 pF.

Table 1. Memory Clock ROM Decode Options

M2	M1	M0	Word	2042–23	2042–24	2042–27
				Frequencies in MHz		
0	0	0	0	48.000	48.000	40.000
0	0	1	1	39.800	39.800	41.000
0	1	0	2	66.000	66.000	41.500
0	1	1	3	50.000	50.000	42.000
1	0	0	4	56.644	56.644	42.500
1	0	1	5	32.200	32.000	43.000
1	1	0	6	44.000	44.000	44.000
1	1	1	7	39.800	39.800	48.000

Three-State Output Operation

The OE signal, when pulled LOW, will three-state the MCLK, PCLK, and XBUF output lines. This supports procedures such as automated testing, where the clock must be disabled. The OE signal contains an internal pull-up but should be tied to V_{DD} if not used.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0mA	V_{DD}−0.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IL}= 0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	Inputs @ V_{DD} and GND		60	mA
I_{ADD}	Analog Power Supply Current			6	mA

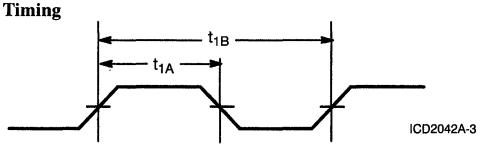
Switching Characteristics Over the Operating Range[2]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value[3]	4	14.318	25	MHz
$t_{(REF)}$	Ref Clock Period	1 ÷ $f_{(REF)}$	40	69.8	250	ns
t_1	Input Duty Cycle	Duty cycle for the input oscillators defined as t_{1A} ÷ t_{1B}	25%	50%	75%	
t_2	Output Period	Clock output time period	8.3 120 MHz		2857 350 KHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs defined as t_{1A} ÷ t_{1B} (measured at 2.5V)	40%		60%	
t_4	Rise Time	Rise time for the outputs into a 25 pF load			4	ns
t_5	Fall Time	Fall time for the outputs into a 25 pF load			4	ns
t_6	Three-State	Time for the outputs to go into three-state mode after OE signal deassertion			12	ns
t_7	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_{MUXREF}	Clk Stable	Time required for the outputs to become valid after P0−P3 or M0−M2 select signals change value	3.4	5	6.9	msec
t_8	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)})/2$	ns
t_9	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3(t_{freq2})/2$	ns

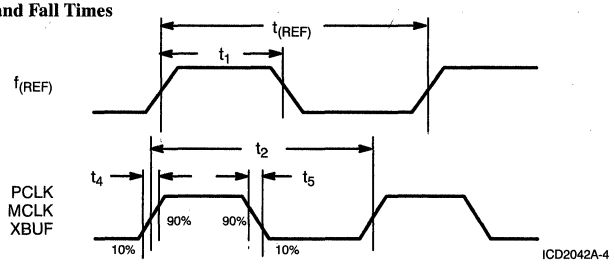
Notes:
2. Input capacitance is typically 10 pF, except for the crystal pads.
3. Different reference frequencies require a custom ROM; standard parts use 14.31818 MHz, unless otherwise stated.

Switching Waveforms

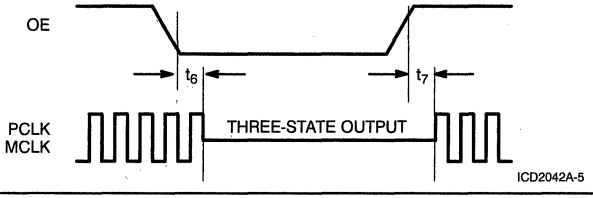
Duty Cycle Timing



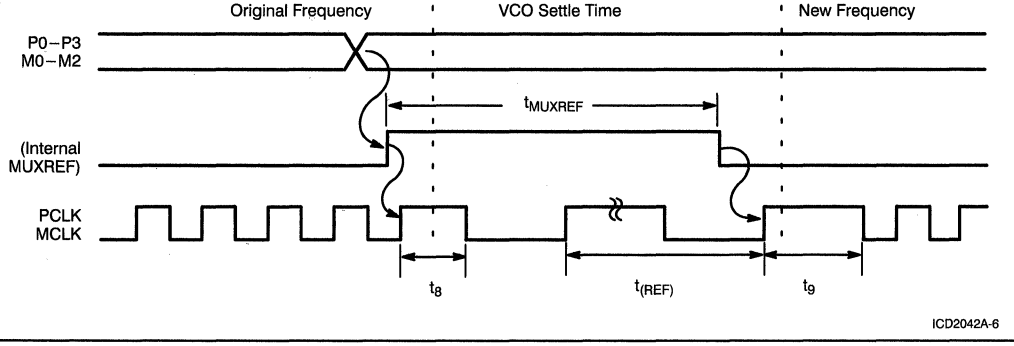
Rise and Fall Times



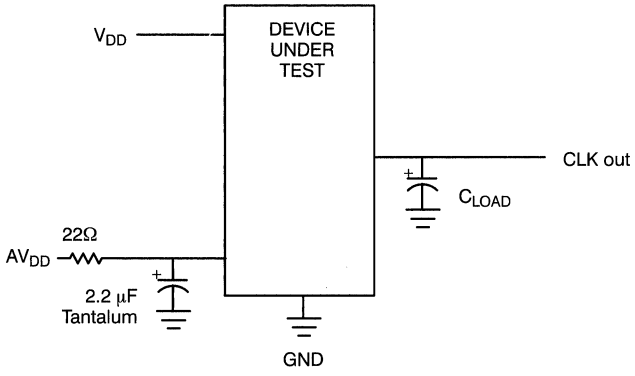
Three-State Timing



Selection Timing



Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
ICD2042A	S1	16-Pin SOIC	Commercial[4]

Note:
12. 0°C to +70°C

Document #: 38−00402

ICD2051

Dual Programmable Clock Generator

Features

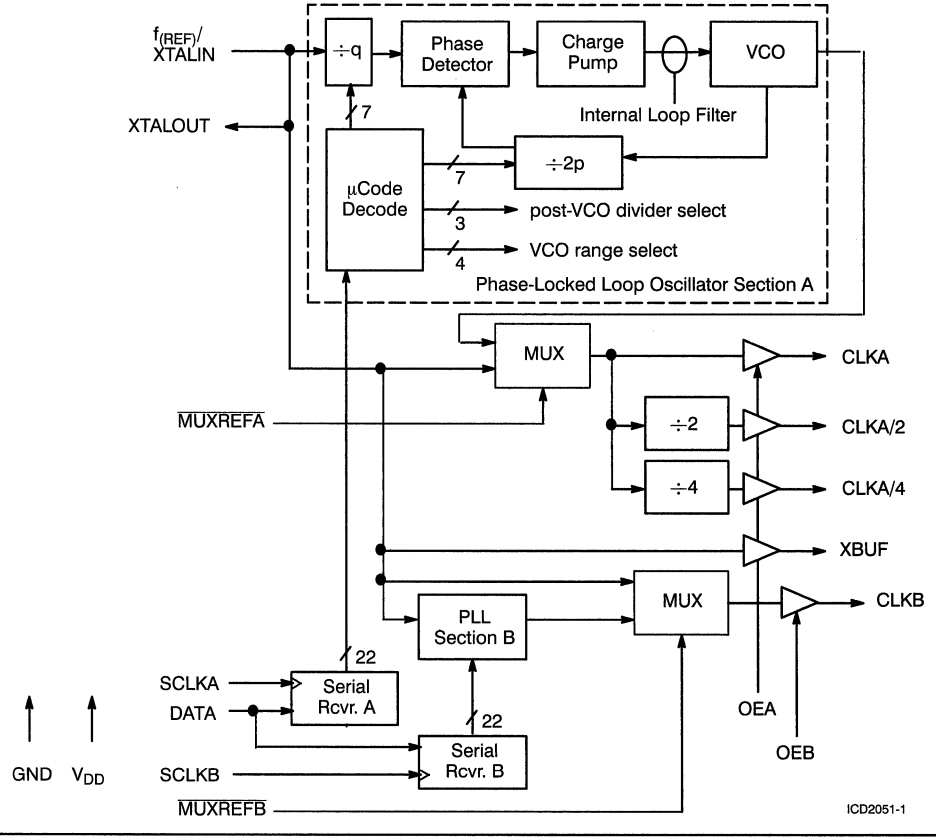
- **Two independent clock outputs ranging from 320 kHz to 100 MHz**
- **Individually programmable PLLs use 22-bit serial word**
- **Low-skew ÷1, ÷2, and ÷4 CLKA outputs**
- **Phase-locked loop oscillator input derived from external low-frequency reference clock (1 MHz – 25 MHz) or external crystal (2 MHz – 24 MHz)**
- **Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Three-state control disables outputs for test purposes (optional)**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package**

Functional Description

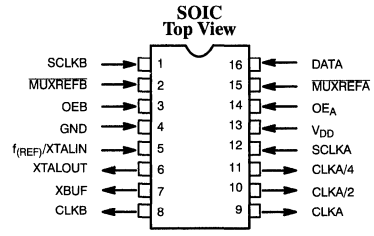
The ICD2051 Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 320 kHz and 100 MHz. The ICD2051 is ideally suited for any design where one or more multiple or varying frequencies are required, thus replacing more expensive metal can oscillators.

The capability to dynamically change the output frequency adds a whole new degree of freedom for the electrical engineer. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example ±10%) allows worst case evaluations.

Logic Block Diagram



Pin Configuration



ICD2051-2

Pin Summary

Name	Number	Description
SCLKB	1	Serial clock input line for CLKB
$\overline{\text{MUXREFB}}$	2	$\overline{\text{MUXREFB}}$ = 0, CLKB equals input reference frequency $\overline{\text{MUXREFB}}$ = 1, CLKB equals programmed frequency This is used if glitch-free frequency changes are required.
OEB	3	Three-states CLKB outputs when pulled LOW. (Internal pull-up allows for no-connect if three-state operation is not needed.)
GND	4	Ground
f_{REF}/ XTALIN[1]	5	Reference Oscillator input for all internal phase-locked loops
XTALOUT[1]	6	Oscillator output to a reference crystal.
XBUF	7	Buffered Crystal Oscillator Output
CLKB	8	CLKB Programmable Output
CLKA	9	CLKA Programmable Output
CLKA/2	10	CLKA divided by 2 (low skew)
CLKA/4	11	CLKA divided by 4
SCLKA	12	Serial clock input line for CLKA.
V_{DD}	13	+5V
OEA	14	Three-states CLKA outputs when pulled LOW. (Internal pull-up allows for no-connect if three-state operation is not needed.)
$\overline{\text{MUXREFA}}$	15	$\overline{\text{MUXREFA}}$ = 0, CLKA equals input reference frequency $\overline{\text{MUXREFA}}$ = 1, CLKA equals programmed frequency This is used if glitch-free frequency changes are required.
DATA	16	Serial data input line for both programmable PLLs

Note:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

10

General Considerations

Programming the ICD2051

The desired output frequency is defined via a serial interface, with a 22-bin number shifted in. The ICD2051 has two programmable PLLs (CLKA and CLKB), requiring a 22-bit programming word (W) to be loaded into each channel independently. This word contains 5 fields:

Table 1. Programming Word Bit Fields

Field	# of bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Reserved (R)	1	normally set to logic 1
Mux (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$P'=P-3$

$Q'=Q-2$

$f_{(VCO)}=2 \times f_{(REF)} \times P/Q$

where $f_{(REF)}$=Reference frequency (between 1 MHz – 25 MHz)

The value of $f_{(VCO)}$ must remain between 40 MHz and 120 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Table 2. Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be should be chosen from *Table 3*. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

Table 3. Index Field (I)

I	$f_{(VCO)}$ (MHz)
0000	40.0 – 42.5
0001	42.5 – 471.5
0010	47.5 – 53.5
0011	53.5 – 58.5
0100	58.5 – 62.5
0101	62.5 – 68.5
0110	68.5 – 69.0
0111	69.0 – 82.0
1000	82.0 – 87.0
1001	87.0 – 92.0
1010	92.0 – 92.1
1011	92.1 – 105.0
1100	105.0 – 115.0
1101	115.0 – 120.0
1110	115.0 – 120.0
1111	115.0 – 120.0

If the desired VCO frequency lies on a boundary in the table (if it is exactly the upper limit of one entry and the lower limit of the next) then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies. The software also assembles the program words for control and power-down registers. Contact your local Cypress representative for more information.

Programming Constraints

There are five primary programming constraints the user must be aware of:

Table 4. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	25 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	40 MHz	120 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed and lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the *BitCalc* program all of these constraints become transparent.

ICD2051 Programming Example

The following is an example of the calculations *BitCalc* performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz<40 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0111. The result:

$$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$$
$$P/Q=2.7857$$

Several choices of P and Q are available:

Table 5. P and Q Value Candidates

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 ppm).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

The programming word, W is generated by concatenating I=0111, P'=1001101, R=1, M=001, Q'=0011011 to obtain

W=01111001101100100110 11 (1e6c9bH)

A LOW-to-HIGH transition on SCLKA/SCLKB (depending on appropriate channel) is used to shift the programming word W into DATA as a serial bit stream, LSB first. (See the set-up and hold timing specifications later in this datasheet.) If more than 22 shifts are performed, only the last 22 data bits received will be retained.

Glitch-Free Frequency-Modification Procedure

When changing to a new frequency, there is a period of time when the output signal will be in transition and may glitch due to changes in the post divider. For applications where it is critical that the output clock not glitch and always maintain some known value, the $\overline{\text{MUXREFA}}$ and $\overline{\text{MUXREFB}}$ inputs must be used. Under normal operation, $\overline{\text{MUXREF(X)}}$ is HIGH and the output clocks are at the programmed value. When $\overline{\text{MUXREF(X)}}$ is brought LOW, the reference clock is now multiplexed to the associated output clock. The output remains at this fixed frequency while the programmed frequency seeks its new value.

When programming the ICD2051, use the MUXREF inputs in the following manner:

4. Set $\overline{\text{MUXREF(X)}}$ to a LOW state. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See the timing specifications.)
5. Shift in the desired output frequency value via a 22-bit word (as defined above) using the appropriate SCLK and DATA lines.
6. After the last bit is shifted in, the VCO will settle to the new state (within .01% of the actual output frequency) within 10 msec.
7. Set $\overline{\text{MUXREF(X)}}$ to a HIGH state. This will set the output to the new programmed frequency. This transition is guaranteed to be glitch-free. (See Serial Programming Timing in the Switching Waveforms section of this datasheet.)

Skew-Controlled ÷2 on CLKA

The CLKA output is available concurrently as ÷1, ÷2, and ÷4 values of the desired output. The ÷1 and ÷2 outputs are also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 2 ns of skew between the two outputs, with 1 ns or less available as an order option.

Output Frequency Accuracy

The accuracy of the ICD2051 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2051 are integrally related to the input reference frequency:

$$f_{(OUT)}=2 \times f_{(REF)} \times P/Q$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2051 normally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (ppm) are given for any desired output frequency as part of the *BitCalc* program output.

Three-State Output Operation

The OEA or OEB signal, when pulled LOW, will three-state the clock output line (CLKA or CLKB respectively). This supports wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signals contain internal pull-ups; they can be left unconnected if three-state operation is not required.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I=C•V•f, where I=current, C=load capacitance (max. 25 pF), V=output voltage (usually 5V), and f=output frequency (in MHz).

To calculate total operating current, sum the following:

XBUF	⇒	$C \bullet V \bullet f_{(REF)}$
CLKA	⇒	$C \bullet V \bullet f_{(CLKA)}$
CLKA/2	⇒	$C \bullet V \bullet f_{(CLKA/2)}$
CLKA/4	⇒	$C \bullet V \bullet f_{(CLKA/4)}$
CLKB	⇒	$C \bullet V \bullet f_{(CLKB)}$
Internal	⇒	12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5−10 pF loading, depending on package type.

Typical values:

Table 6. Typical Load Current Values

Frequency	Load	Current (mA)
low	none	15
high	none	40
high	high	100

10

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C
Package power dissipation ..... 525 mWatts

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5.25	V
T_A	Ambient Operating Temperature	0	70	°C
C_L	Load Capacitance		25	pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except XTALIN pins	2.0		V
V_{IL}	Input LOW Voltage	Except XTALIN pins		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25V		150	µA
I_{IL}	Input LOW Current	V_{IN} = 0V		−250	µA
I_{OZ}	Output Leakage Current	Three-state outputs		10	µA
I_{DD}	Power Supply Current	V_{DD} = V_{DD} max., 100 MHz, V_{IN} = V_{DD} or 0V	15	100	mA

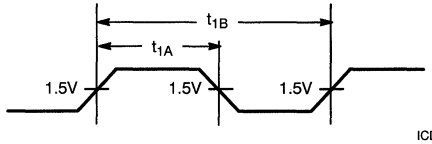
Switching Characteristics Over the Operating Range[2]

Parameter	Name	Description	Min.	Max.	Unit
	Output Frequency		0.320	100	MHz
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value	1	25	MHz
$t_{(REF)}$	Reference Clock Period	$t_{(REF)} = 1/f_{(REF)}$	40	1000	ns
	Duty Cycle	Duty cycle for the output oscillators defined as $t_{1A} \div t_{1B}$	40%	60%	
t_2	Output Rise Time	Rise time for the outputs into a 25-pF load		3	ns
t_3	Output Fall Time	Fall time for the outputs into a 25-pF load		3	ns
t_4	CLKA/2/4 skew	Skew delay between the CLKA output and the CLKA/2 and CLKA/4 outputs		2	ns
t_5	MUXREF Set-Up Time	Delay required after MUXREF goes LOW prior to starting the SCLK clock line	t_{freq1}		ns
t_6	SCLK Cycle Time	Minimum cycle time for the SCLK clock	$2*t_{(REF)}$		ns
t_{6H}	SCLK HIGH Time	Minimum HIGH time for the SCLK clock	$t_{(REF)}$		ns
t_{6L}	SCLK LOW Time	Minimum LOW time for the SCLK clock	$t_{(REF)}$		ns
t_7	Output Clock Stable Time	Time required for CLKA or CLKB output to become valid after last SCLK clock		10	msec
t_8	Data Set-Up Time	Time required for the data to be valid prior to the rising edge of SCLK	10		ns
t_9	Data Hold Time	Time required for the data to remain valid after the rising edge of SCLK	5		ns
t_{10}	Transition Time	Time for CLKA or CLKB to go HIGH after assertion of MUXREF	0	t_{freq1}	ns
t_{11}	Transition Time	Delay of CLKA or CLKB prior to valid $t_{(REF)}$ signal at output	$t_{(REF)}/2$	$3(t_{(REF)}/2)$	ns
t_{12}	Transition Time	Time for CLKA or CLKB to go HIGH after release of MUXREF	0	$t_{(REF)}$	ns
t_{13}	Transition Time	Delay of CLKA or CLKB prior to valid new frequency at output	$t_{freq2}/2$	$3(t_{freq2}/2)$	ns
t_{14}	Output Disable Time	Time for the outputs to go into three-state mode after OE signal assertion		12	ns
t_{15}	Output Enable Time	Time for the outputs to recover from three-state mode after OE signal goes HIGH		12	ns

Note:
2. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

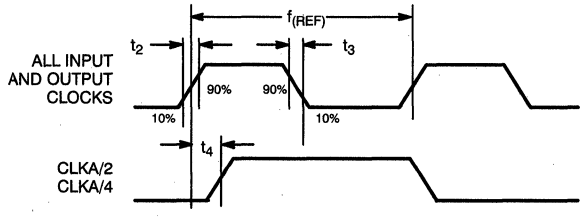
Duty Cycle Timing



ICD2051-3

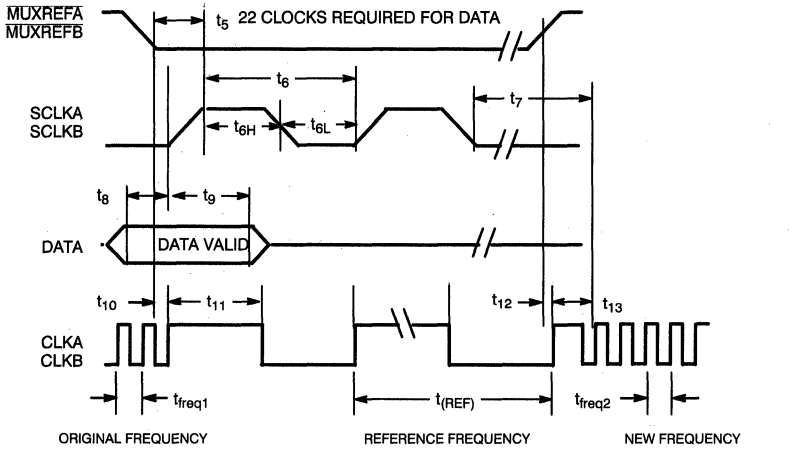
Switching Waveforms (continued)

Rise and Fall Times



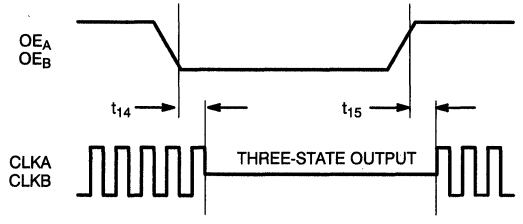
ICD2051-4

Serial Programming Timing



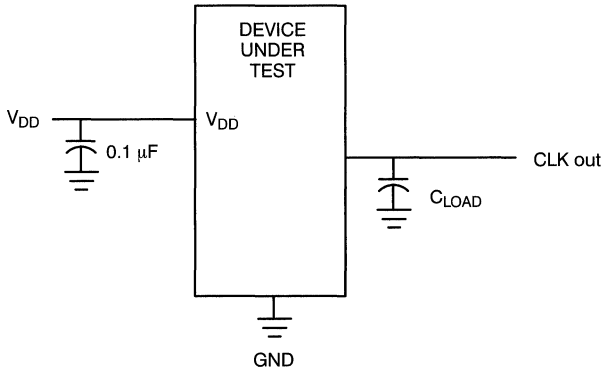
ICD2051-5

Three-State Timing



ICD2051-6

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
ICD2051	S1	16-Pin SOIC	Commercial[3]

Note:
3. 0°C to +70°C

Document #: 38−00402

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ICD2053B

Programmable Clock Generator

Features

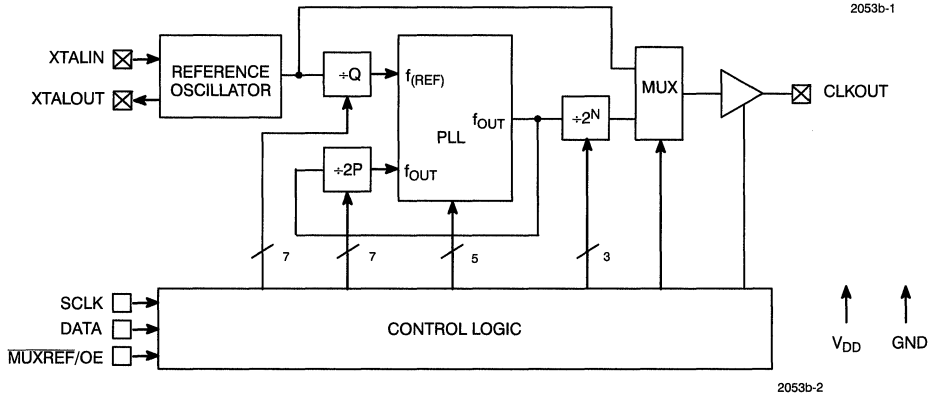
- **Clock outputs ranging from 391 kHz to 100 MHz (TTL levels) or 90 MHz (CMOS levels)**
- **2-wire serial interface facilitates programmable output frequency**
- **Phase-Locked Loop oscillator input derived from external reference clock (1 MHz to 25 MHz) or External Crystal (2 MHz to 24 MHz)**
- **Three-State output control disables output for test purposes**
- **Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Low power consumption makes device ideal for power- and space-critical applications**
- **8-pin 150-mil packaging achieves minimum footprint for space-critical applications**
- **5V operation**
- **High-speed CMOS technology**

Functional Description

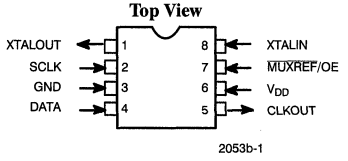
The ICD2053B Programmable Clock Generator offers a fully user-programmable phase-locked loop in a single 8-pin package. The output may be changed "on the fly" to any desired frequency value between 391 kHz and 100 MHz (90 MHz at CMOS levels). The ICD2053B is ideally suited for any design in which package size, power, and/or frequency programmability are important design issues.

The ability to dynamically change the output frequency adds a whole new degree of freedom for the designer. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption; graphics board dot clocks to allow dynamic synchronization of different brands of monitors or display formats; on-board test strategies where the ability to skew a system's desired frequency (e.g., ±10%) allows worst-case evaluation.

Logic Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
XTALOUT[1, 2]	1	Reference crystal feedback
SCLK	2	Serial clock input line for programming purposes
GND	3	Ground
DATA	4	Serial data input line for programming purposes
CLKOUT	5	Programmable clock output
V_{DD}	6	+5 volts
$\overline{\text{MUXREF}}$/OE	7	If bit 3 (Pin 7 Usage) in the Control register is set to 1, this input pin controls the multiplexed reference frequency function. The operation is defined in *Table 1* If bit 3 (Pin 7 Usage) in the Control Register is set to 0, this input pin controls the three-state output function. The operation is defined in *Table 1* On power-up, pin 7 implements the OE function. An internal pull-up allows pin to be not-connected.
XTALIN[1, 2]	8	Reference crystal input or external reference input ($f_{(REF)}$)

ICD2053B Registers

The ICD2053B contains two registers, Control and Program.

These registers are written using a protocol which uses a Protocol word = 011110 to distinguish Control register data from Program register data. This Protocol word is recognized by the four sequential 1s; therefore, all other data sent must have a 0 bit stuffed in after each sequence of three sequential 1s (whether originally followed by a 1 or a 0). This is called bit-stuffing.

Please see the example under "Program Register Example" and the "Frequency Modification Procedure" section. Following is a bit-stuffing example (read right to left, LSB to MSB):

To send this programming data: 1111 0111 1110 111111
Transmit this serial bit stream: 10111 00111 01110 01110111

All serial words are shifted in bit-serially starting with the LSB. A low-to-high transition on SCLK is used to shift data. Whenever the Protocol word is detected, the preceding 8 bits are transferred into the Control register. The control command is then immediately executed.

Control Register

The Control register is used to control the non-frequency setting aspects of the ICD2053B. It is an 8-bit register, which is defined as shown in *Figure 1* and *Table 1.*

At power-up, the Control register is loaded with 0000 0100. This means that the MUXREF Control field is set to 1, forcing the CLKOUT to equal the reference frequency. Additionally, the other fields in the Control register specify that the Program register is disabled from loading, and the internal three-state is disabled.

7	6	5	4	3	2	1	0
0 (Reserved)	0 (Reserved)	Duty Cycle Adjust (Set to 1)	0 (Reserved)	Pin 7 Usage	MUXREF Control	OE Control	Enable Program Word

Figure 1. Control Register

Notes:
1. For best accuracy, use a parallel-resonant crystal.
2. Assume $C_{LOAD} \approx 17$ pF.

Table 1. Control Register

Bit	Definition
RESERVED	For future use. Set to 0.
Duty Cycle Adjust	Set to 1 to reduce duty cycle by approximately 0.7 ns. Normally set to 1.
Pin 7 Usage	Definition of whether pin 7 is $\overline{\text{MUXREF}}$ or OE input pin 0 = Pin 7 is OE input (default) 1 = Pin 7 is $\overline{\text{MUXREF}}$ input
MUXREF Control	Allows internal control of MUXREF. If enabled, this feature automatically multiplexes the reference frequency to the CLKOUT output. This is used to change output glitch-free to new frequencies. 0 = CLKOUT is VCO frequency 1 = CLKOUT is $f_{(REF)}$ (default)
OE Control	Forces the CLKOUT output into a three-state mode 0 = CLKOUT is VCO frequency or $f_{(REF)}$ (default)(depending on current MUXREF state) 1 = CLKOUT is three-stated
Enable Program Word	Enable Program word loading into Program register. When enabled, the Program word may be shifted in. This permits changing the Control register without disturbing Program register data. 0 = Program register is disabled from loading (default) 1 = Program register is enabled to receive data

Program Register

The Program register can be loaded with a 22-bit programming word, the fields of which are defined in *Table 2.*

Table 2. Program Register

Field	# of Bits	Notes
P Counter value (P')	7	MSB (Most Significant Bits)
Duty Cycle Adjust Up (D)	1	Set to logic 1 to increase duty cycle by approx. 0.7 ns. Normally set to 1.
Mux (M)	3	
Q Counter value (Q')	7	
Index (I)	4	LSB (Least Significant Bits)

The VCO frequency, $f_{(VCO)}$, is determined by the following relation:

$f_{(VCO)} = (2 * f_{(REF)} * P/Q)$

where $P' = P - 3$

$Q' = Q - 2$

$f_{(REF)}$ = Reference frequency (1 MHz to 25 MHz)

The value of $f_{(VCO)}$ must remain between 50 MHz and 150 MHz. Therefore, for output frequencies below 50 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 3.* (Note that this table is referenced to the VCO frequency $f_{(VCO)}$ rather than to the desired output frequency and that only the MSB is significant.)

Table 3. Index Field (I)

I	$f_{(VCO)}$ @ 5V
0000	50 to 80 MHz
1000	80 to 150 MHz

To assist with these calculations, Cypress/IC Designs provides the BITCALC program. BITCALC is a Windows™ program for the IBM PC which automatically generates the appropriate programming word from the user's reference input and desired output frequencies.

VCO Programming Constraints

There are seven primary programming constraints the user must be aware of:

Table 4. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	25 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	50 MHz	150 MHz
divisor	1	128
f_{OUT}	50 MHz/128	100 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the above-mentioned BITCALC program, these constraints become transparent.

PROGRAM Register Example

The following is an example of the calculations BITCALC performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 50 MHz, double it to 79.0 MHz. Set M to 001 to post divide by 2. Set I to 1000. The result:

$f_{(VCO)} = 79.0 = (2 * 14.31818 * P/Q)$

$P/Q = 2.7587$

Several choices of P and Q are available for this example:

P	Q	$f_{(VCO)}$	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9969	419

Normally, one would choose (P,Q) = (80,29) for the best accuracy (40 PPM). However, we will choose (P,Q) = (91,33) as it illustrates bit stuffing.

Therefore:

P' = P − 3 = 91 − 3 = 88 = 1011000
Q' = Q − 2 = 33 − 2 = 31 = 0011111

The programming word, W, is generated by first creating the non-bit-stuffed word W' by concatenating P'=1011000, D=1, M=001, Q'=0011111, I=1000, and then bit-stuffing.

W' = 1011000 1 001 001 0011111 1000
W = 10110001001000111011100 0

Zeros were stuffed in two places in this example.

Output Frequency Accuracy

The accuracy of the ICD2053B output frequency depends on the target output frequency and reference frequency. As stated previously, the output frequency of the ICD2053B is mathematically related to the input reference frequency:

$f_{(OUT)} = (2 * f_{(REF)} * P/Q) \div 2^n$, n = 0...7.

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2053B generally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (in ppm) are given for any desired output frequency in the BITCALC program output.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
Input Voltage ..... −0.5V to V_{DD}+0.5
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Max. Soldering Temperature (10 sec) ..... +260°C
Junction Temperature ..... +125°C

Note:
3. Static sensitive <2000V.

Frequency Modification Procedure

When changing to a new frequency, there is a period of time during which the output signal will be in transition and could jump in frequency, or glitch due to changes in the post divider. For applications in which it is critical that the output clock not glitch and always maintain some known value, the MUXREF feature in the Control register should be used. MUXREF causes the reference clock to be multiplexed, glitch-free, to the output clock. The output will remain at this fixed frequency while the VCO seeks its new programmed value.

The procedure for programming the ICD2053B to an initial or new frequency is as follows:

1. Load the Control register to enable MUXREF and enable loading of the Program register. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See timing specifications.) Note that the Protocol Word must precede the Control register data. Also note that all data is shifted in LSB (Least Significant Bit) first.

   Control word = 0 1 1 1 1 0 0 0 0 0 X 1 0 1 ← LSB
   Protocol Word Control Reg. Data

   The state of the Pin 7 Usage bit is defined by the user, and so is denoted as X.
2. Shift in the desired output frequency value computed via a 22-bit data word (as defined above), plus any bit-stuffs (as defined above). Remember to bit-stuff a 0 after any three sequential 1s.
3. Load the Control register to enable MUXREF and disable loading of the Program register. This loads the Program word bits into the Program register and keeps the output set to the reference frequency while the new frequency settles.

   Control word = 0 1 1 1 1 0 0 0 0 0 X 1 0 0
   Protocol Word Control Reg. Data
4. Wait for VCO to settle in the new state (10 ms to within 0.1% of the new frequency).
5. Load the Control register to enable new frequency output. The transition is guaranteed to be glitch-free. (See the timing specifications.)

   Control word = 0 1 1 1 1 0 0 0 0 0 X 0 0 0
   Protocol Word Control Reg. Data

Package Power Dissipation ..... 400 mW
Static Discharge Voltage ..... Class 1[3] (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature	0	70	°C
C_L	Load Capacitance		25	pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	HIGH-level Output Voltage	I_{OH} = 4.0 mA	2.4		V
V_{OL}	LOW-level Output Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	HIGH-level Input Voltage	Except XTALIN pins	2.0		V
V_{IL}	LOW-level Input Voltage	Except XTALIN pins		0.8	V
V_{IH}	HIGH-level Reference Input Voltage, when DC coupled[4]	XTALIN pin only	$V_{DD}-0.8$		V
V_{IL}	LOW-level Reference Input Voltage, when DC coupled[4]	XTALIN pin only		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.0V, except SCLK		100	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V, except SCLK		−250	µA
I_{IH}	Input HIGH Current	V_{IN} = 5.0V, SCLK only		250	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V, SCLK only		−100	µA
I_{OZ}	Output Leakage Current	Three-state		10	µA
I_{DD}	Power Supply Current	$V_{DD}=V_{DD}$ max., 100 MHz, $V_{IN}=V_{DD}$ or 0V	13	50	mA

Capacitance

Parameter	Description	Max.	Unit
C_{IN}	Input Capacitance, except XTALIN pin	10	pF
C_{IN}	Input Capacitance, XTALIN pin	34	pF

Switching Characteristics Over the Operating Range

Parameter	Name	Description		Min.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value[4]		1	25	MHz
$t_{(REF)}$	Reference Clock Period	$t_{(REF)} = 1/f_{(REF)}$		40	1000	ns
t_1	Reference Clock HIGH Time	Input pulse width HIGH for reference. Measured at $V_{DD}/2$, DC coupled.[4]		16		ns
t_2	Output Period	CLKOUT period (frequency), TTL levels		10 (100 MHz)	2560 (391 kHz)	ns
		CLKOUT period (frequency), CMOS levels		11.1 (90 MHz)	2560 (391 kHz)	
t_3	Output Duty Cycle (t_0/t_2)	Duty cycle of CLKOUT measured at 1.4V (TTL) threshold	$f_{(OUT)}$ < 50 MHz AND post-divide ≥ 2	45%	55%	
			$f_{(OUT)}$ > 50 MHz OR post-divide = 1	40%	60%	
		Duty cycle of CLKOUT measured at $V_{DD}/2$ (CMOS) threshold	post-divide ≥ 2	45%	55%	
			post-divide = 1	40%	60%	
t_4	Rise Time	Rise time for the clock output into a 25 pF load	TTL 0.4V to 2.4V		3	ns
			CMOS, $0.1V_{DD}$ to $0.9V_{DD}$		6	

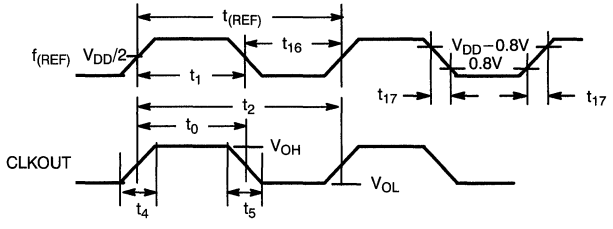
Note:
4. See *Externally Driven Crystal Oscillator* Application Note. For AC coupling, use an input duty cycle near 50%.

Switching Characteristics Over the Operating Range (continued)

Parameter	Name	Description		Min.	Max.	Unit
t_5	Fall Time	Fall time for the clock output into a 25 pF load	TTL 0.4V to 2.4V		3	ns
			CMOS, 0.1V_{DD} to 0.9V_{DD}		6	
t_6	SCLK Cycle Time	Minimum cycle time for the SCLK clock		2 * $t_{(REF)}$		ns
t_7	Clock Valid	Time required for the CLKOUT oscillator to become valid after last SCLK clock[5]		$t_{(REF)}$	3 * $t_{(REF)}$ + 25	ns
t_8	Serial Data Set-up	Time required for the data to be valid prior to the rising edge of SCLK		15		ns
t_9	Hold	Time required for the data to remain valid after the rising edge of SCLK		0		ns
t_{10}	Delay, MUXREF[6] Asserted to CLKOUT HIGH	Time for CLKOUT to go HIGH after assertion of MUXREF[6]		0	t_{old} + 25	ns
t_{11}	Transition, $f_{(OLD)}$ to $f_{(REF)}$	Delay of first falling edge of $f_{(REF)}$ signal at output		t_{13}	$t_{(REF)}$ + 25	ns
t_{12}	Reference Output High Time	Output during MUXREF[6], reference DC coupled		t_{16} − 10	t_{16} + 10	ns
t_{13}	Reference Output Low Time	Output during MUXREF[6], reference DC coupled		t_1 − 10	t_1 + 10	ns
t_{14}	Transition, $f_{(REF)}$ to $f_{(NEW)}$	Time for CLKOUT to go HIGH after release of MUXREF[6]		0	$t_{(REF)}$ + 25	ns
t_{15}	Transition, MUXREF[6] released to CLKOUT LOW	Delay of first falling edge of $f_{(NEW)}$ signal at output		t_{new}/2	t_{new} * 3/2 + 25	ns
t_{16}	Reference Clock Low Time	Input pulse width low for reference. Measured at V_{DD}/2, DC coupled[4]		18		ns
t_{17}	Reference Input Rise/Fall	Rise/fall time for DC coupled reference input[4]			$t_{(REF)}$/10	ns
t_{18}	Output Enable Delay	Delay from Output Enable HIGH to Output Valid		0	20	ns
t_{19}	Output Disable Delay	Delay from Output Enable LOW to Output Floating		0	20	ns
t_{old}	Original Period	Output period before reprogramming, $1/f_{(OLD)}$				
t_{new}	New Period	Output period after reprogramming, $1/f_{(NEW)}$				
t_{lock}	VCO Lock Time	Time for VCO to lock onto new $f_{(VCO)}$ within 0.1%			10	msec

Switching Waveforms

Rise and Fall Times

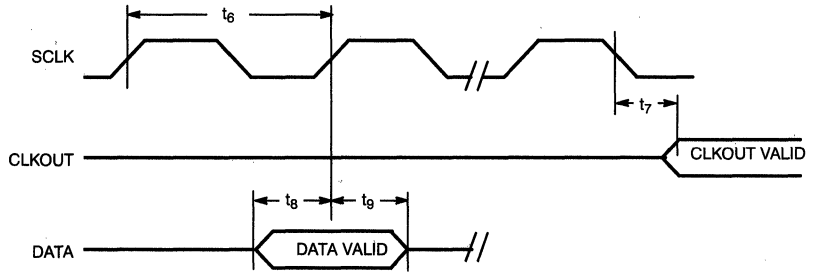


2053b-3

Notes:
5. This is the time for the serial word shifted in to take effect, including the Control Word output enable bit. The VCO stabilization time is separate.
6. Pin or internal bit.

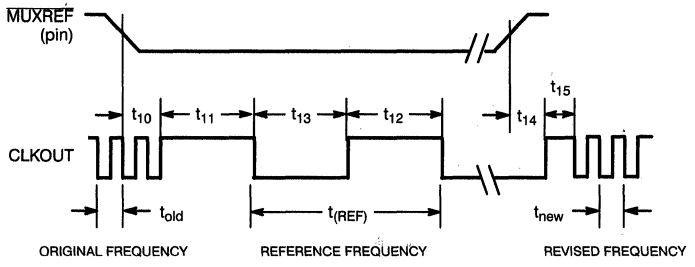
Switching Waveforms (continued)

Serial Programming Timing



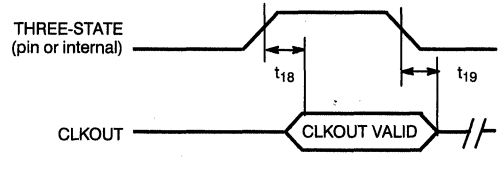
2053b-4

MUXREF Timing[7]



2053b-5

Three-State Timing



2053b-6

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
ICD2053B	S8	8-Pin (150-Mil) SOIC	Commercial[8]

Notes:
7. Identical behavior is exhibited when the internal MUXREF bit in the Control register is HIGH.
8. 0°C to +70°C

Document #: 38–00412

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ICD2061A

Dual Programmable Graphics Clock Generator

Features

- **Second generation dual oscillator graphics clock generator**
- **2 independent clock outputs from 390 kHz to 100 MHz**
- **Individually programmable oscillators using a highly reliable, Manchester-encoded, 21-bit serial data word**
- **2-pin serial programming interface allows direct connection to most graphics chip sets with no external hardware required**
- **2 advanced power-down capabilities**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.318 MHz crystal**
- **Sophisticated internal loop-filter requires no external components or manufacturing "tweaks" as commonly required with external filters**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package configuration**

Functional Description

The ICD2061A Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2061A offers the selection ease of ROM-based clock chips, while also offering the versatility of serially programmable frequency synthesizers. It features advanced power-down capabilities, making it ideally suited for the portable computer market. The ICD2061A has extended frequency range and improved voltage/temperature stability when compared to first-generation frequency synthesizers.

The ICD2061A Dual Programmable Graphics Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 390 kHz and 100 MHz. The ICD2061A is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators.

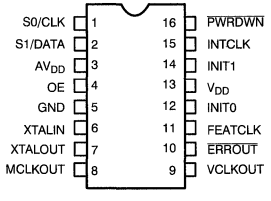
Being able to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer which was previously unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2061A makes it ideal wherever two variable, yet highly accurate clock sources are required.

10

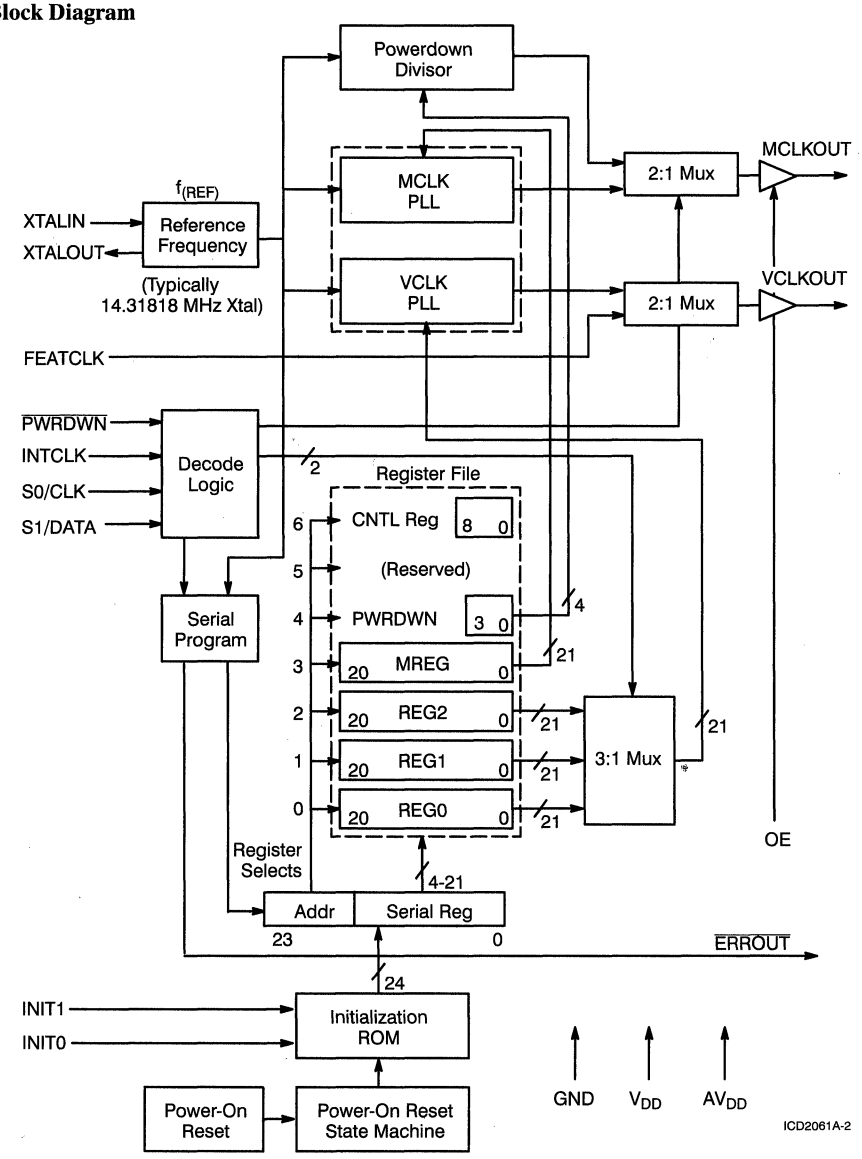
Pin Configuration

SOIC
Top View



ICD2061A-1

Logic Block Diagram



Pin Summary

Name	Number	Description
S0/CLK	1	Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
S1/DATA	2	Bit 1 (MSB) of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
AV_{DD}	3	+5V to Analog Core
OE	4	Output Enable. Three-states output when pulled LOW. (Internal pull-up allows no connect.)
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
MCLKOUT	8	Memory Clock output
VCLKOUT	9	Video Clock output
$\overline{ERROUT}$	10	Error Output: a LOW signals an error during serial programming.
FEATCLK	11	External clock input (Feature Clock) (Internal pull-up allows no-connect.)
INIT0	12	Select power-up initial conditions (LSB) (Internal pull-down allows no-connect.)
V_{DD}	13	+5V to I/O Ring
INIT1	14	Select power-up initial conditions (MSB) (Internal pull-down allows no-connect.)
INTCLK	15	Selects the Feature Clock external clock input as VCLKOUT output (Internal pull-up allows no-connect.)
$\overline{PWRDWN}$	16	Power-down pin (active LOW) (Internal pull-up allows no-connect if power-down operation not required. See *Power Management Issues* for specific details concerning the use of this pin.)

Register Definitions

Register File

The Register File consists of the following registers and their selection addresses:

Table 1. Register Addressing[2]

Address	Register	Usage
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory or I/O Timing Clock
100	PWRDWN	Divisor for Power-Down mode
101	(Reserved)	
110	CNTL Reg	Control Register

Power-On Reset and Register Initialization

The ICD2061A Clock Synthesizer has all of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three VGA registers and the Memory Clock register are initialized based on the state of the INIT1 and INIT0 pins at power-up.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with V_{DD} if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as follows in *Table 2* (all frequencies in MHz).

Table 2. Register Initialization—ROM Option 1

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD}=17 pF.
2. All register values are preserved in power-down mode.

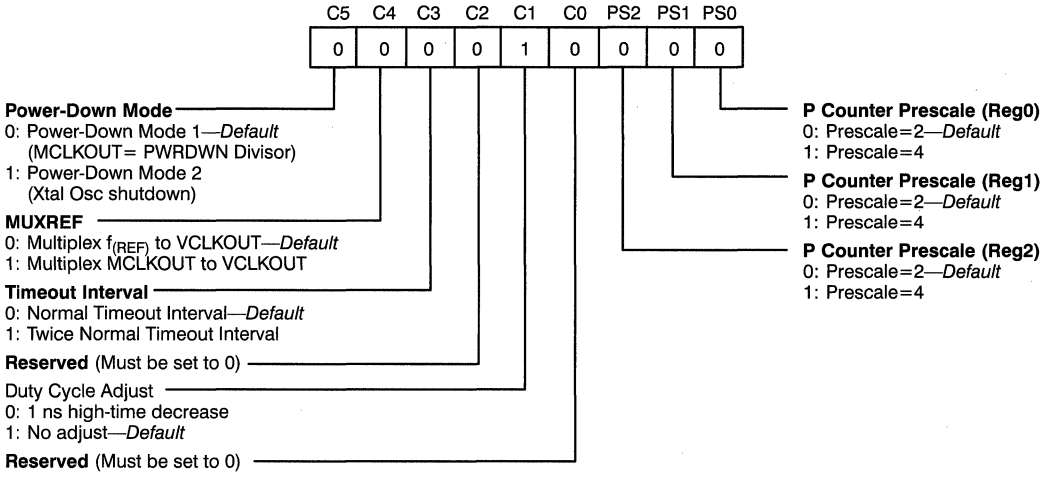


Figure 1. Control Register Definition ICD2061A-3

Register Selection

The Video Clock output is controlled not only by the S0 and S1 bits, but also by the $\overline{\text{PWRDWN}}$ and OE signals. Additionally, the clock synthesizer is multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. *Table 3* shows the VCLKOUT selection criteria.

Table 3. VCLKOUT Selection

OE	PWRDWN	INTCLK	S1	S0	VCLKOUT
0	X	X	X	X	High-Z
1	0	X	X	X	Forced High
1	1	X	0	0	REG0
1	1	X	0	1	REG1
1	1	0	1	0	FEATCLK
1	1	1	1	X	REG2
1	1	X	1	1	REG2

The Memory Clock output is controlled by the $\overline{\text{PWRDWN}}$ and OE signals as indicated in *Table 4*.

Table 4. MCLKOUT Selection

OE	PWRDWN	MCLKOUT
0	X	High-Z
1	1	MREG
1	0	PWRDWN[3]

Note:

3. Power-Down Mode (1 or 2) is determined by the setting of bit C5 in the CNTL Reg. See *1.* Control Register Definition.

The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval to give the VCO time to settle to its new value. [The timeout interval in both cases is approximately 5 msec—see the timeout interval spec in *Switching Characteristics*.]

When a new frequency is being set for MCLK, or if the active VCLK register is programmed, a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *Switching Characteristics* for further details).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1.*

Duty Cycle Adjust—This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the threshold voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

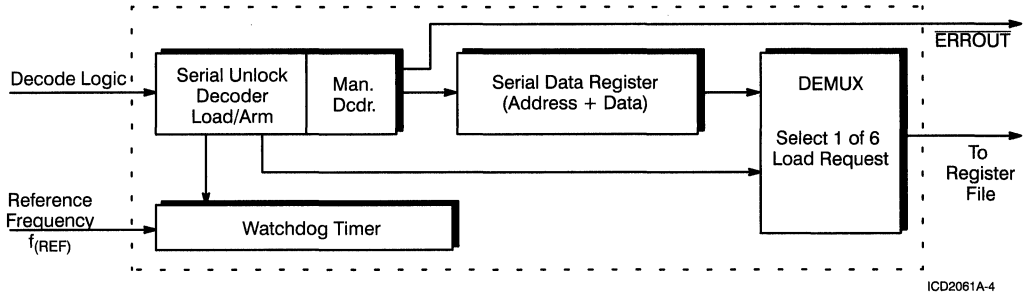


Figure 2. Serial Programming Block Diagram—Detail

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics*. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

MUXREF—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Power-Down Mode—This control bit determines which Power-Down Mode the $\overline{\text{PWRDWN}}$ pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section entitled *Power Management Issues*.

P Counter Prescale (REG0, REG1, REG2)—These control bits determine whether or not to prescale the P Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail in various sections of this datasheet.

Serial Programming Architecture

The ICD2061A programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See ICD2061A Logic Block Diagram) contains several components: a Serial Unlock Decoder (containing the unlocking mechanism and Manchester decoder), a watchdog timer, the Serial Data register (Serial Reg) and a Demultiplexer to the Register File (see *Figure 2*).

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in *Figure 3*.

The initial unlock sequence consists of at least five LOW-to-HIGH transitions of CLK with DATA HIGH, followed immediately by a single LOW-to-HIGH transition of CLK with DATA LOW. Following this unlock sequence, the encoded serial data is clocked into the Serial Data register (Serial Reg).

Note that the ICD2061A may not be serially programmed when in Power-Down Mode.

Watchdog Timer

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. Throughout the entire programming process, the watchdog timer ensures that successive edges of CLK or DATA do not violate the timeout specification (of 2 msec—see *Switching Characteristics*.) If a timeout does occur, the lock mechanism is rearmed and the current data in the Serial Data register (Serial Reg) is ignored.

Since the VCLK registers are selected by the S0 or S1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of S0 or S1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.

Serial Data Register

The serial data is clocked into the Serial Data register (Serial Reg) in the following order shown in *Figure 4*.

The serial data is sent using a modified Manchester-encoded data format. This is defined as:

1. An individual data bit is sampled on the rising edge of CLK.

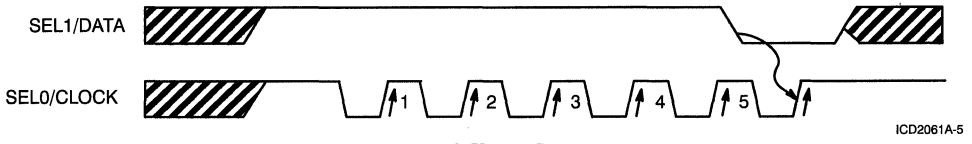


Figure 3. Unlock Sequence

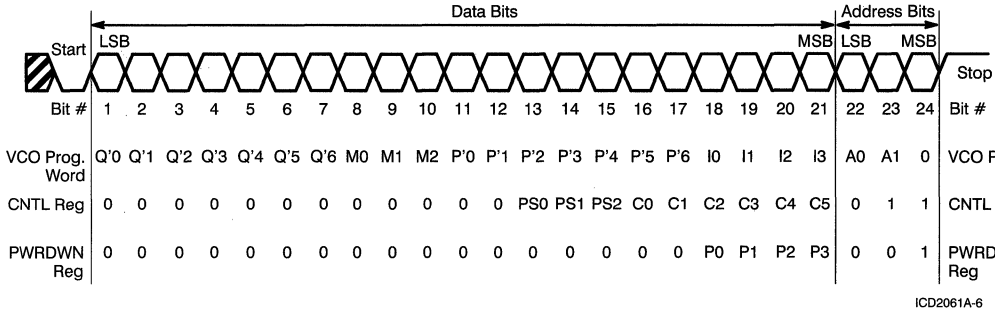


Figure 4. Serial Data Timing

2. The complement of the data bit must be sampled on the previous falling edge of CLK.
3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the "Serial Programming Timing" section in the switching waveforms..

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10]=P'; D[9:7]=Mux; D[6:0]=Q'. (See the *Programming the ICD2061A* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (PWRDWN, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing data HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register (Serial Reg) that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

$\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to report when a program error has been detected internally by the ICD2061A. The signal stays active until the next unlock sequence.

Figure 5 shows the basic mechanism used to detect valid and erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

Note that if there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

Programming the ICD2061A

The desired output frequency is defined via a serial interface, with a 24-bit number shifted in. The ICD2061A has two programmable oscillators, requiring a 24-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

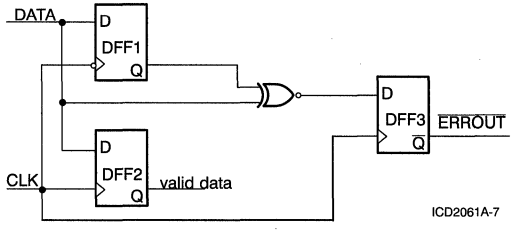


Figure 5. Serial Data Timing

Table 5. Programming Word Bit Fields

Field	# of Bits
Address (A)	3
Index (I)	4[4]
P Counter value (P)	7
Div (D)	3
Q Counter Value (Q)	7[5]

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P'=P-3 \quad Q'=Q-2$$
$$f_{(VCO)}=(2 \times f_{(REF)} \times P/Q)$$

where $f_{(REF)}$=Reference frequency (between 1 MHz–25 MHz; typically 14.31818 MHz)

Note that if a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between 50 MHz and 120 MHz inclusive. Therefore, for output frequencies below 50 MHz $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO divisor is selected by setting the values of the div field (D). See *Table 6*.

Table 6. Post-VCO Divisor

D	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index Field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (This table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running.

When the Index Field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one does want the clocks to run at 2^n (n=0, 1, 2 .. 7) multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

Table 7. Index Field (I)

I	VCLK f_{VCO} (MHz)	MCLK f_{VCO} (MHz)
0000	50.0 – 51.0	50.0 – 51.0
0001	51.0 – 53.2	51.0 – 53.2
0010	53.2 – 58.5	53.2 – 58.5
0011	58.5 – 60.7	58.5 – 60.7
0100	60.7 – 64.4	60.7 – 64.4
0101	64.4 – 66.8	64.4 – 66.8
0110	66.8 – 73.5	66.8 – 73.5
0111	73.5 – 75.6	73.5 – 75.6
1000	75.6 – 80.9	75.6 – 80.9
1001	80.9 – 83.2	80.9 – 83.2
1010	83.2 – 91.5	83.2 – 91.5
1011	91.5 – 100.0	91.5 – 100.0
1100	100.0 – 120.0	100.0 – 120.0
1101	100.0 – 120.0	100.0 – 120./0
1110	Turn off VCLK	100.0 – 120.0
1111	Mux MCLK to VCLK	100.0 – 120.0

If the desired VCO frequency lies on a boundary in the table—in other words, if it is exactly the upper limit of one entry and the lower limit of the next—then either index value may be used (since both limits are tested).

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program that automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers.

Programming Constraints

There are five primary programming constraints of which the user must be aware:

Table 8. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	60 MHz
$f_{(REF)}$ + Q	200 kHz	1 MHz
$f_{(VCO)}$	VCLK: 65 MHz MCLK: 52 MHz	VCLK: 165 MHz MCLK: 120 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the *BitCalc* program, these constraints become transparent.

Notes:
4. MSB (Most Significant Bits)
5. LSB (Least Significant Bits)

Programming Example—Prescaling=2 (default)

The following is an example of the calculations *BitCalc* performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz<50 MHz, double it to 79.0 MHz. Set D to 001. Set I to 1000. The result:

$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$
$P/Q = 2.7587$

Table 9. P&Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

and the full programming word, W is:

W=I, P', M, Q'=1000, 1001101, 001, 0011011
=10001001101001001101 1 (11349bH)

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the Serial Programming Scheme section.

Programming Example—Prescaling=4

Assume the desired VCLKOUT frequency is 100 MHz. *Table 10* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 10. Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	Error (PPM)
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0-2 (corresponding to REG0-2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

Power Management Issues

Power-Down Mode 1

The ICD2061A contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling, the $\overline{\text{PWRDWN}}$ signal low and having the proper CNTL Reg bit set to zero), both VCOs are shut down, the VCLKOUT output is forced high, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The power-down MCLKOUT value is determined by the following equation:

$MCLKOUT_{Power\text{-}Down}=f_{(REF)} \div$ (PWRDWN Reg Divisor Value)

The Power-Down register divisor is determined according to the following 4-bit word programmed into the PWRDWN register. (See *Table 11.*)

Table 11. PWRDWN Register Programming

PWRDWN bits				PWRDWN Register Value	Power-Down Divisor	MCLKOUT Power-Down ($f_{(REF)}$=14.31818 MHz)
P3	P2	P1	P0			
0	0	0	0	0	N/A	N/A
0	0	0	1	1	32	447.4 KHz
0	0	1	0	2	30	477.3 KHz
0	0	1	1	3	28	511.4 KHz
0	1	0	0	4	26	550.7 KHz
0	1	0	1	5	24	596.6 KHz
0	1	1	0	6	22	650.8 KHz
0	1	1	0	7	20	715.9 KHz
1	**0**	**0**	**0**	**8**	**18 (default)**	**795.5 KHz**
1	0	0	1	9	16	894.9 KHz
1	0	1	0	A	14	1.023 MHz
1	0	1	1	B	12	1.193 MHz
1	1	0	0	C	10	1.432 MHz
1	1	0	1	D	8	1.790 MHz
1	1	1	0	E	6	2.386 MHz
1	1	1	1	F	4	3.580 MHz

On power-up, the value of the PWRDWN Register is loaded with a default value of 8 (1000 binary), which yields an MCLKOUT frequency of 795 KHz (14.31818/18). The default mode is Power-Down Mode 1.

Note that the ICD2061A may not be serially programmed when in Power-Down Mode.

Power-Down Mode 2

If there is no need for any output during power-down operation, then an alternate Power-Down Mode is available, which will completely shut down all outputs and the reference oscillator, yet still preserve all register contents. This results in the absolute least power consumption.

Power-Down Mode 2 is invoked by first programming the power-down bit in the CNTL Reg, and then pulling the $\overline{\text{PWRDWN}}$ pin LOW.

The $\overline{\text{PWRDWN}}$ Pin

This pin has a standard internal pull-up during normal operation. When the user pulls it down to invoke Power-Down Mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which significantly reduces power consumption. If, after pulling this pin LOW, the pin is allowed to float, the weak pull-up will gradually cause the signal to rise, enabling the normal pull-up, and will eventually turn the device back on.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I=C x V x f, where:

I=current (in mA)
C=Load capacitance (max., 25pF)
V=output voltage (usually 5V)
f=output frequency (in MHz)

To calculate total operating current, sum the following terms:

VCLKOUT −−>C x V x f(VCLK)
MCLKOUT−−> C x V x f(MCLK)
Internal −−>12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5 to 10pF loading, depending on package type.

Table 12. Typical Values

Frequency	Capacitive Load	Current (mA)
LOW	LOW	15
HIGH	LOW	40
HIGH	HIGH	65

When in Power-Down Mode 1, and using a 14.31818 MHz reference crystal, the power consumption should not exceed 7.5 mA. In Power-Down Mode 2, the power consumption should not exceed 50 µA.

Output Enable Pin

When the OE pin is asserted (active LOW), all the output pins except XTALOUT and $\overline{\text{ERROUT}}$ enter a high-impedance mode, to support automated board testing.

External Clock Input (Feature Connector Compatibility)

To maintain backward compatibility to the VGA feature connector standard, the video clock output VCLKOUT can multiplex between the clock synthesizer output and the external clock input FEATCLK. This multiplexing is controlled by the INTCLK input signal and appropriate decode of selection signals (SEL0, SEL1). See the section on Register Definitions for more information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V
V_{IL}	Input LOW Voltage	Except on Crystal Pins		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5		105.0	µA
I_{IL}	Input LOW Current	V_{IL} = +0.5V		−250.0	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Supply Current	Inputs @ V_{DD} and GND	15	85.0	mA
I_{ADD}	Analog Power Supply Current			10	mA
I_{PD1}	Power-Down Current (Mode 1)			7.5	mA
I_{PD2}	Power-Down Current (Mode 2)			50	µA

Note:
6. Input capacitance is typically 10 pF, except for the crystal pins.

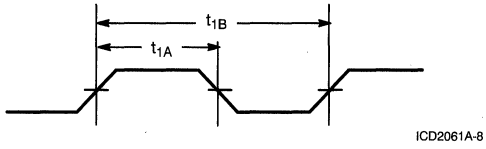
Switching Characteristics Over the Operating Range

Parameter	Name	Description	Min.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value	1	25	MHz
$t_{(REF)}$	Reference Clock Period	$t_{(REF)} = 1/f_{(REF)}$	40	1000	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_{1A} \div t_{1B}$	25%	75%	
t_2	Output Clock Periods	Output values	10	2564	ns
t_3	Output Duty Cycle	Duty cycle for the outputs defined as $t_{2A} \div t_2$[7]	40	60	%
t_4	Rise Times	Rise time for the outputs into a 25-pF load		4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load		4	ns
t_{freq1}	freq1 Output	Old frequency output			
t_{freq2}	freq2 Output	New frequency output			
t_A	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$	$3(t_{(REF)}/2)$	ns
$t_{timeout}$	Timeout Interval	Internal interval for serial programming and for VCO changes to settle[8]	2	10	msec
t_B	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$	$3/(t_{freq2}/2)$	ns
t_6	Three-state	Time for the outputs to go into three-state mode after OE signal assertion	0	12	ns
t_7	CLK Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH	0	12	ns
t_8	Power-Down	Time for Power-Down Mode of operation to take effect		12	ns
t_9	Power-Up	Time for recovery from Power-Down Mode of operation		12	ns
t_{10}	MCLKOUT HIGH	Time for MCLKOUT to go HIGH after $\overline{PWRDWN}$ is asserted HIGH	0	$t_{PWR-DWN}$	ns
t_{11}	MCLKOUT delay	Delay of MCLKOUT prior to f_{MCLK} signal at output	$t_{MCLK}/2$	$3/(t_{MCLK}/2)$	ns
t_{serclk}		Clock period of serial clock	$2 \times t_{(REF)}$	2	msec
t_{HI}		Minimum HIGH time	$t_{(REF)}$		ns
t_{LO}		Minimum LOW time	$t_{(REF)}$		ns
t_{SU}		Set-Up time	20		ns
t_{HD}		Hold time	10		ns
t_{ldcmd}		Load command	0	$t_{(REF)}+30$	ns

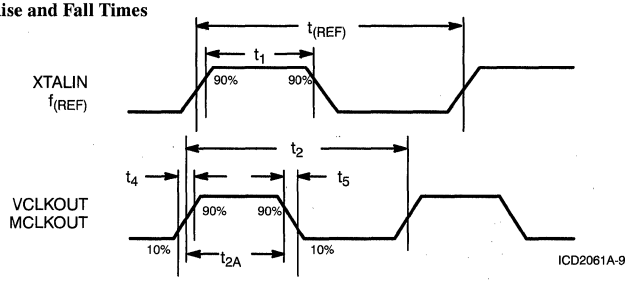
Notes:
7. Duty cycle is measured at CMOS threshold levels. At 5V, $V_{TH}=2.5V$.
8. If the interval is too short, see the Timeout Interval paragraph.

Switching Waveforms

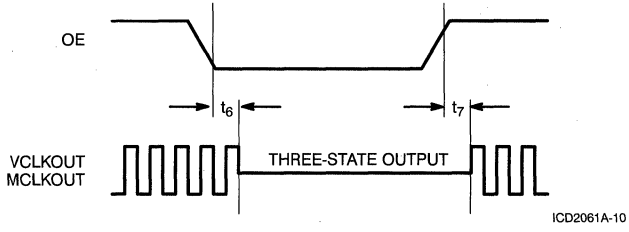
Duty Cycle Timing



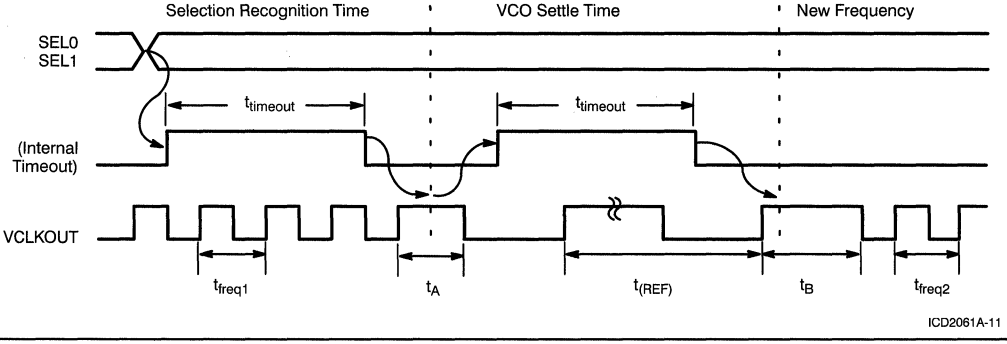
Rise and Fall Times



State Timing

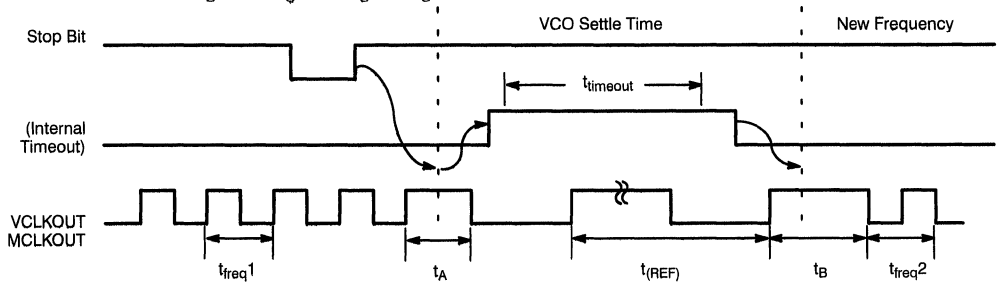


Selection Timing

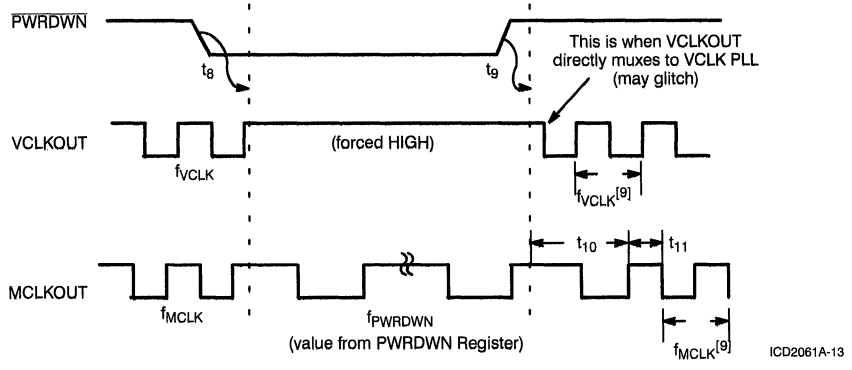


Switching Waveforms (continued)

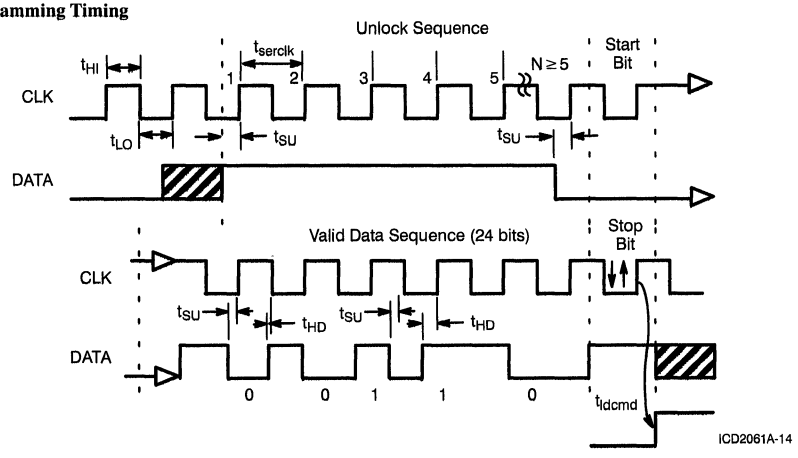
MCLK and Active VCLK Register Programming Timing



Soft Power-Down Timing (Mode 2)

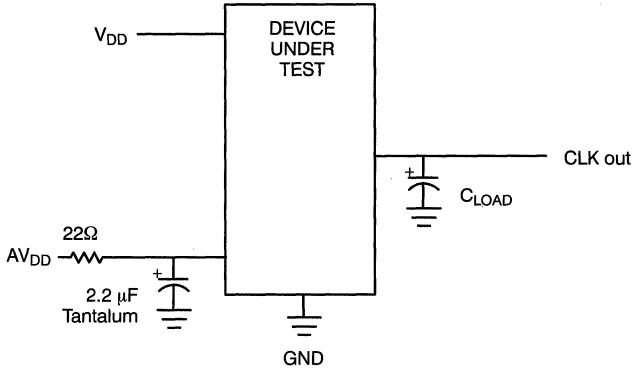


Serial Programming Timing



Note:
9. It takes 2 to 10 msec after Soft Power-Down to guarantee lock of VCLKOUT and MCLKOUT PLLs

Test Circuit



Ordering Information[10]

Ordering Code	Package Name	Package Type	Operating Range
ICD2061A	S1	16-Pin SOIC	Commercial[11]

Notes:
10. Please call your local Cypress representative.
11. 0°C to +70°C

Example: order ICD2061ASC-1 for the ICD2061A, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in *Table 2.*

Document #: 38–00403

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Dual Programmable ECL/TTL Clock Generator

Features

- **Second generation dual oscillator graphics clock generator**
- **PECL Video Outputs: 508 kHz to 165 MHz**
- **TTL Outputs: 508 kHz to 120 MHz**
- **Individually programmable PLLs using a highly reliable, Manchester-encoded, 21-bit serial data word**
- **2-pin serial programming interface allows direct connection to most graphics chip sets with no external hardware required**
- **Programmable video clock dividers allow for easy interface to most RAMDACs and VRAMs**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.318 MHz crystal**
- **Sophisticated internal loop-filter requires no external components**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

Functional Description

The ICD2062B is a clock generator for high-resolution video displays. It uses a low-frequency, low-cost reference crystal to produce the following: a 10 K compatible complementary ECL output signal for high-speed video RAMDACs, a high-speed TTL output signal for video RAMs and system logic operation, and the requisite load, control, and clock signals to control the loading of data between the CRT controller, VRAM, and RAMDACs.

The ICD2062B Dual Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value in the range 508 kHz to 165 MHz (VCLKOUT) and 508 kHz to 120 MHz (MCLKOUT). The ICD2062B is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators, particularly where the application requires expensive complementary ECL oscillators.

The Video Clock output may be programmatically divided—by 1, 2, 3, 4, 5, or 8—in order to generate the Load Signal, which is further divided by 2 and 4 for clocking video timing logic. A second Load Signal may be synchronously gated in order to enable starting and stopping the clocking of video RAMs. The ICD2062B can also configure the pipeline delay of certain RAMDACs (such as the Bt457/458) to a fixed pipeline delay.

Some examples of the uses for this device include: graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

ICD2062A vs. ICD2062B

The ICD2062B revision of the ICD2062A is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following points detail the differences between the two versions.

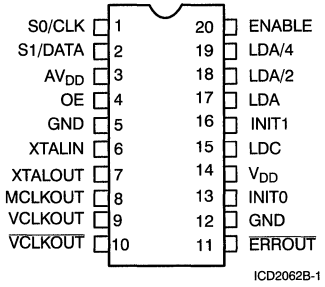
The ICD2062B offers the following new features:

- **New VCO**—The primary difference between the A and B versions is the design of the internal VCO. The ICD2062B video VCO has been redesigned to support frequencies up to 165 MHz (see above);
- **Higher Upper Frequency Limit (VCLKOUT)**—165 MHz;
- **New Register Initialization ROM**—A new ROM allows the ICD2062B to be initialized to higher default frequencies;
- **More Load Clock divisors**—The ICD2062B Load Clock divisors of 1, 2, 3, 4, 5, and 8.

10

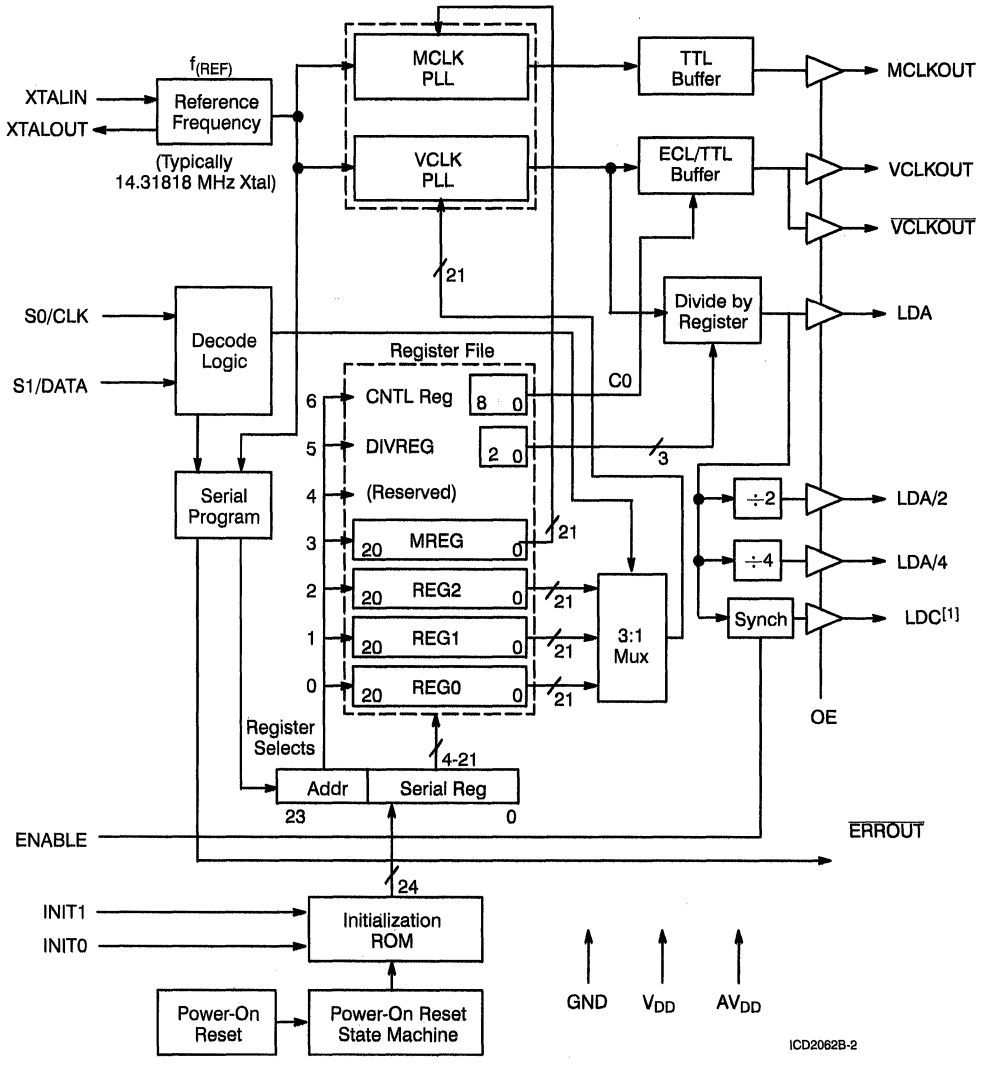
Pin Configuration

SOIC
Top View



ICD2062B-1

Logic Block Diagram



Note:
1. If ENABLE =1, then LDC = synch. copy of LDA, else LDC = 0.

Pin Summary

Name	Number	Description
S0/CLK	1	Bit 0 (LSB) of frequency select logic, used to select output frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
S1/DATA	2	Bit 1 (MSB) of frequency select logic, used to select output frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
AV_{DD}	3	+5V to Analog Core
OE	4	Output Enable three-states output when signal is LOW (pin has internal pull-up.)
GND	5	Ground
XTALIN[2]	6	Reference Oscillator input for all phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[2]	7	Oscillator Output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
MCLKOUT	8	Memory Clock output
VCLKOUT	9	Differential clock outputs. Connect directly to RAMDAC CLOCK inputs. Can drive 4 RAMDACs.
$\overline{\text{VCLKOUT}}$	10	Output levels equivalent to 10 K ECL circuit operating from single supply. $\overline{\text{VCLKOUT}}$ is skew-free.
$\overline{\text{ERROUT}}$	11	Error Output: a LOW signals an error during serial programming.
GND	12	Ground
INIT0	13	Select power-up initial conditions (LSB) (Internal pull-down allows no-connect.)
V_{DD}	14	+5V to I/O Ring
LDC	15	Load output (TTL compatible). When ENABLE is HIGH, has same timing as LDA output. Can drive up to 4 capacitive loads without buffering.
INIT1	16	Select power-up initial conditions (MSB) (Internal pull-down allows no-connect.)
LDA	17	Skew-free Load Outputs (TTL compatible). Generated by dividing VCLKOUT by Div Register (1, 2, 3, 4, 5, or 8). Each output can drive up to 4 capacitive loads without buffering.
LDA/2	18	Generated by dividing LDA by two.
LDA/4	19	Generated by dividing LDA by four.
ENABLE	20	Synchronous load enable input. Internally synched to LDA, used to start/stop LDC output synchronously. If ENABLE is LOW, LDC is held LOW; when HIGH, LDC is free-running.

Register Definitions

Register File

The Register File consists of the following registers and their selection addresses:

Table 1. Register Addressing

Address	Register	Usage
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory or I/O Timing Clock
100	(Reserved)	
101	DIVREG	Load Divisor Register
110	CNTL Reg	Control Register

Note:
2. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD}=17 pF.

Register Selection

The Video Clock output is controlled not only by the S0 and S1 bits, but also by the OE signal as shown in *Table 2*.

Table 2. VCLKOUT Selection

OE	S1	S0	VCLKOUT
0	X	X	High-Z
1	0	0	REG0
1	0	1	REG1
1	1	X	REG2

The Memory Clock output is controlled by the OE signal as indicated in *Table 3*.

Table 3. MCLKOUT Selection

OE	VCLKOUT
0	High-Z
1	MREG

The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval toallow the VCO to settle to its new value. (The timeout interval in both cases is approximately 5 msec—see the timeout interval spec in *Switching Characteristics*.)

When a new frequency is being set for MCLK, or if the active VCLK register is being programmed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *Switching Characteristics* for further details).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1*.

MUXREF—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphics controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics*. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

RAMDAC Reset—This control bit, when set, will cause the ICD2062B to issue a RAMDAC reset sequence, which is required by some specific RAMDACs (such as the Bt457/458). For more specifics on this operation, refer to the section *Internal RESET Sequence*. NOTE: This operation will only take place the first time this bit is set.

Duty Cycle Adjust—This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the threshold voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

VCLKOUT Pad—This control bit determines whether the VCLKOUT Pad is at ECL or TTL levels. The default is ECL levels. When in TTL mode, the $\overline{\text{VCLKOUT}}$ Pad is nonfunctional, and remains three-stated.

P Counter Prescale (REG0, REG1, REG2)—These control bits determine whether or not to prescale the P Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail later in this datasheet.

Divide Register Definition

The output signals LDA, LDA/2, LDA/4, and LDC are all a function of the VCLK VCO value divided by the division factor stored in the Divide Register (DIVREG). The maximum LDA and LDC output is 100 MHz.

Table 4. DIVREG Division Factors

D2	D1	D0	Division Factor	Clock LOW (cycles)	Clock HIGH (cycles)	Device Version
1	0	X	÷1	1/2	1/2	A&B
1	1	X	÷2	1	1	A&B
0	0	0	÷3	1	2	B
0	0	1	÷4	2	2	B[3]
0	1	0	÷5	2	3	B
0	1	1	÷8	4	4	B

Note:
3. Default on power-up.

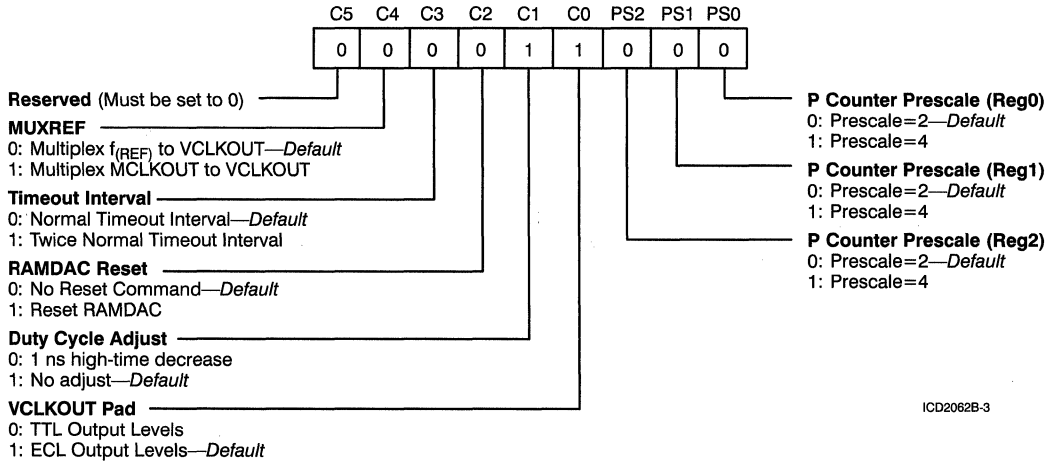


Figure 1. Control Register Definition

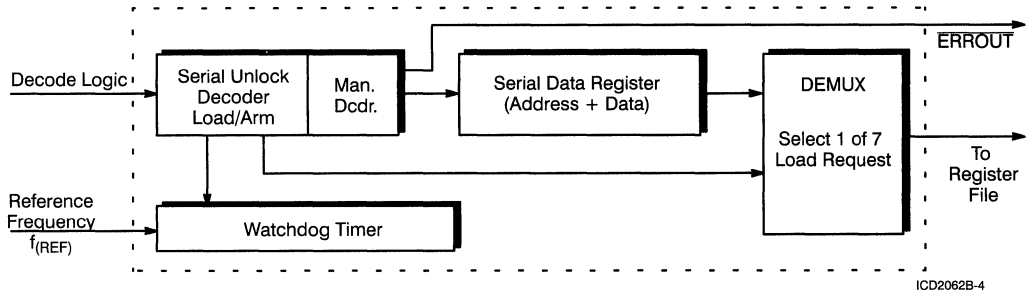


Figure 2. Serial Programming Block Diagram—Detail

Register Initialization

The ICD2062B Clock Synthesizer has all of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three pixel clock registers and the Memory Clock register are initialized based on the state of the INIT1 and INIT0 pins at power-up.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with V_{DD} if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as shown in *Table 5* (all frequencies in MHz).

Table 5. Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	110.000	135.000	165.000
1	1	56.644	110.000	135.000	185.000

Serial Programming Architecture

The ICD2062B programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (see *Figure 2*) contains several components: a Serial Unlock Decoder (containing the unlocking mechanism and Manchester decoder), a watchdog timer, the Serial Data register and a Demultiplexer to the Register File.

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in *Figure 3*.

The initial unlock sequence consists of at least five LOW-to-HIGH transitions of CLK with DATA HIGH, followed immediately by a single LOW-to-HIGH transition of CLK with DATA LOW. Following this unlock sequence, the encoded serial data is clocked into the Serial Data register (Serial Reg).

Watchdog Timer

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. Throughout the entire programming process, the watchdog timer ensures that successive edges of CLK or DATA do not violate the timeout specification (of 2 msec—see *Switching Characteristics*.) If a timeout does occur, the lock mechanism is rearmed and the current data in the Serial Data register is ignored.

Since the VCLK registers are selected by the S0 or S1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of S0 or S1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.

Serial Data Register

Serial data is clocked into the Serial Data register in the order shown in *Figure 4*.

The serial data is sent using a modified Manchester-encoded data format. This is defined as:

1. An individual data bit is sampled on the rising edge of CLK.
2. The complement of the data bit must be sampled on the previous falling edge of CLK.

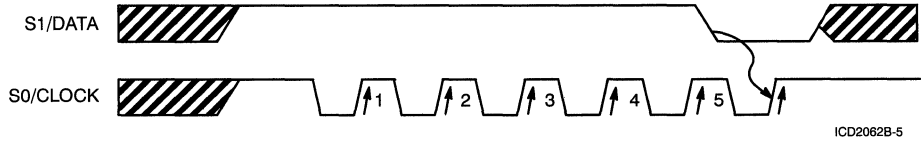


Figure 3. Unlock Sequence

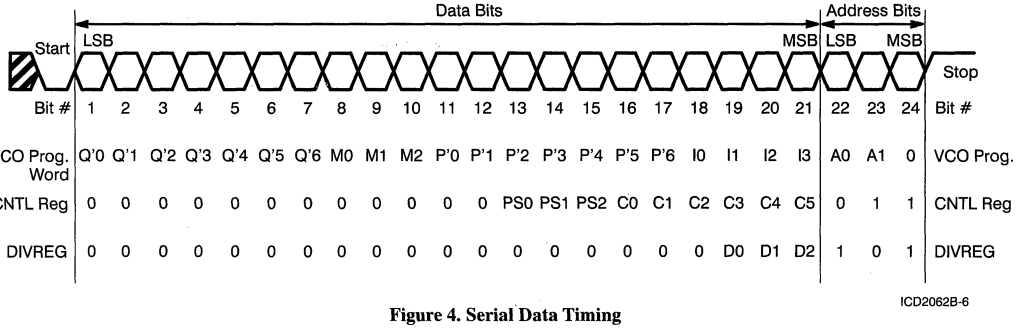


Figure 4. Serial Data Timing

3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the "Serial Programming Timing" section in the switching waveforms..

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10]=P'; D[9:7]=Mux; D[6:0]=Q'. (See the *Programming the ICD2062B* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (DIVREG, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing DATA HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Data Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

$\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to announce when a program error has been detected internally by the ICD2062B. The signal remains LOW until the next unlock sequence.

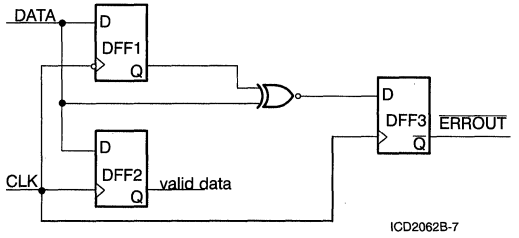


Figure 5. Modified Manchester Decoder Circuit

Figure 5 shows the basic mechanism used to detect erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect start bit, incorrect Manchester encoding; incorrect length of data word; incorrect stop bit.

Note that if there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming success.

Programming the ICD2062B

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2062B has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields, as shown in *Table 6*.

Table 6. Programming Word Bit Fields

Field	# of bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Mux (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P'=P-3$$
$$Q'=Q-2$$
$$f_{(VCO)}=(2 \times f_{(REF)} \times P/Q)$$

where $f_{(REF)}$=Reference frequency (typically 14.31818 MHz)

Note that if a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between a minimum and maximum frequency. These limits vary depending on the clock (MCLK or VCLK). See *Table 4* for the actual boundary frequencies in each case. For output frequencies below the minimum, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO divisor is selected by setting the values of the Mux field (M). See *Table 7*.

Table 7. Post-VCO Divisor

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index Field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 8*. (This table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running.

When the Index Field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, the two VCOs should not run at integral multiples of each other; therefore, to allow the output clocks to run at 2^n (n=0, 1, 2 .. 7) multiples of each other, turn off the VCLK VCO and multiplex the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

If the desired VCO frequency lies on a boundary in the table—in other words, if it is exactly the upper limit of one entry and the lower limit of the next—then either index value may be used (since both limits are tested) but the higher value should be used.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program that automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers.

Table 8. Index Field (I)

I	VCLK f_{VCO} (MHz)	MCLK f_{VCO} (MHz)
0000	65.0 – 70.7	Reserved
0001	70.7 – 77.8	52.0 – 55.0
0010	77.8 – 85.6	55.0 – 60.0
0011	85.6 – 88.0	60.0 – 68.0
0100	88.0 – 94.2	68.0 – 70.0
0101	94.2 – 96.8	70.0 – 75.0
0110	96.8 – 106.5	75.0 – 80.0
0111	106.5 – 111.7	80.0 – 84.5
1000	111.7 – 117.2	84.5 – 90.0
1001	117.2 – 122.8	90.0 – 95.0
1010	122.8 – 135.1	95.0 – 100.0
1011	135.1 – 148.6	100.0 – 104.0
1100	148.6 – 160.0	104.0 – 110.0
1101	160.0 – 165.0	110.0 – 120.0
1110	Turn off VCLK	110.0 – 120.0
1111	Mux MCLK > VCLK	110.0 – 120.0

Programming Constraints

There are five primary programming constraints of which the user must be aware:

Table 9. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	60 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	VCLK: 65 MHz MCLK: 52 MHz	VCLK: 165 MHz MCLK: 120 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the *BitCalc* program, these constraints become transparent.

Programming Example—Prescaling=2 (default)

The following is an example of the calculations *BitCalc* performs:

Derive the proper programming word for a 39.5 MHz VCLK output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz<50 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0010. The result:

$$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$$
$$P/Q = 2.7587$$

Table 10. P&Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

and the full programming word, W is obatined by concatenating:

I=0010, P'=1001101, M=001, Q'=0011011
=00101001101001011011 (05349bH)

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the Serial Programming Architecture section.

Programming Example—Prescaling=4

Assume the desired VCLKOUT frequency is 100 MHz. *Table Table 10* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 11. Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	Error (PPM)
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0−2 (corresponding to REG0−2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: The results will be unpredictable at best, and it could cause the VCO to go out of lock.

RAMDAC/VRAM Interface

Interfacing to the RAMDAC

Figure 6 shows how to interface the ICD2062B to a RAMDAC. The part should be located as close to the RAMDAC as possible. Termination resistors are needed on the VCLKOUT outputs, and should be located as close as possible to the RAMDAC. For specific information, please refer to the Cypress/IC Designs application note *ECL Outputs*.

The ICD2062B may drive the CLOCK inputs of up to four RAMDACs, if they are located physically adjacent to each other. In this case, only 2 sets of termination resistors should be used, and these should be located closest to the farthest RAMDAC from the ICD2062B.

Typical ICD2062B Usage

The DIVREG register holds the divisor, which can be 1, 2, 3, 4, 5, or 8, by which the pixel clock is divided to generate the load signals: LDA, LDA/2, and LDA/4.

The ENABLE input is synchronized internally to LDA; it may be used to start and stop the LDC output synchronously. When ENABLE is LOW, LDC is held LOW. When ENABLE is HIGH, then LDC will be free-running and in phase with LDA. This allows the video DRAM shift registers to be non-clocked during the retrace intervals. Note that for fanouts greater than 4, LDC needs to be buffered.

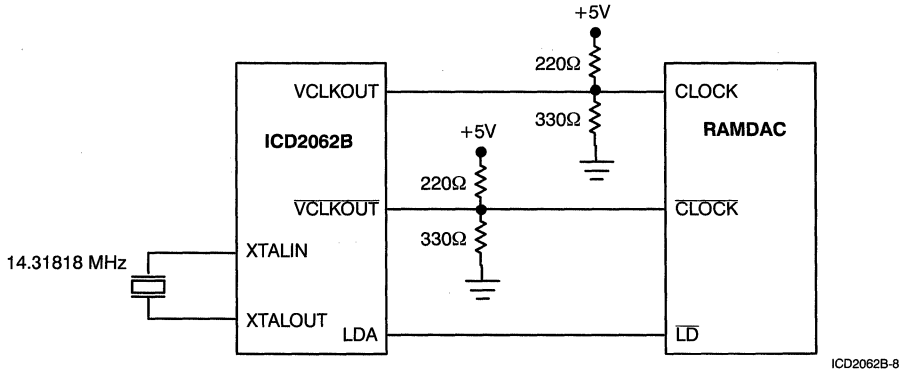


Figure 6. ICD2062B to RAMDAC Interface Example

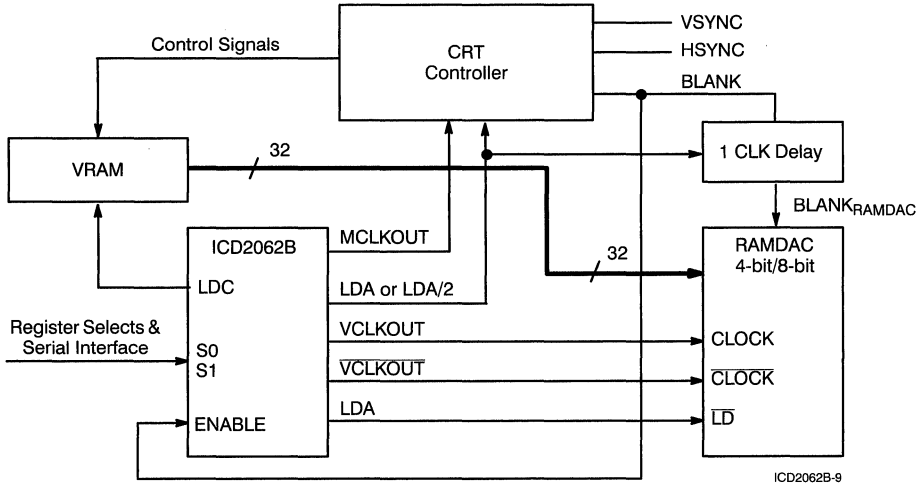


Figure 7. ICD2062B Typical Interface Circuit

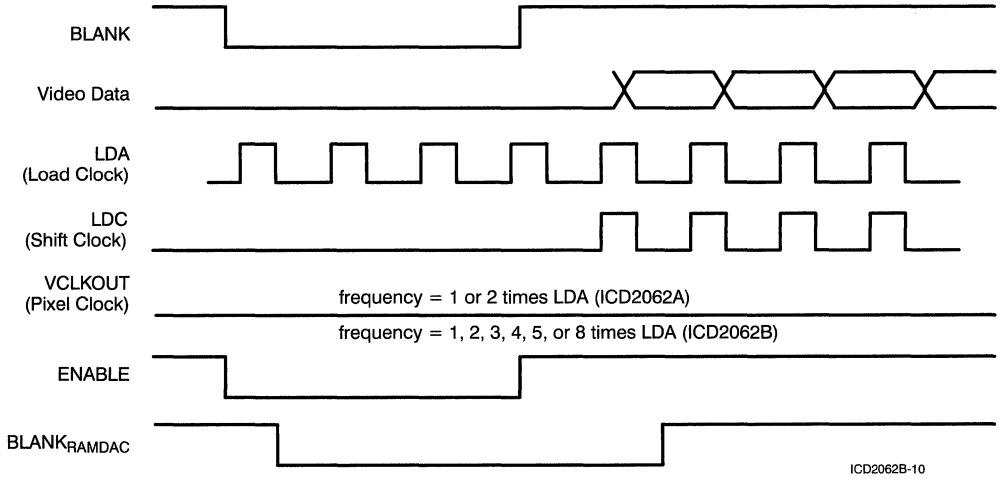


Figure 8. Timing Diagram for Interface Circuit

Internal RESET Sequence

The internal RESET signal allows the ICD2062B to set the RAMDAC pipeline delay to a specific cycle count, depending on the RAMDAC. Reset takes place the first time the Control Register's Reset Bit is set. Following the rising edge of LDA/4 after the Reset Bit is set, the VCLKOUT and $\overline{\text{VCLKOUT}}$ outputs are stopped HIGH and LOW, respectively; at the next rising edge of LDA/4, these outputs are again allowed to be free-running. *Figure 9* shows the operation of the internal RESET signal.

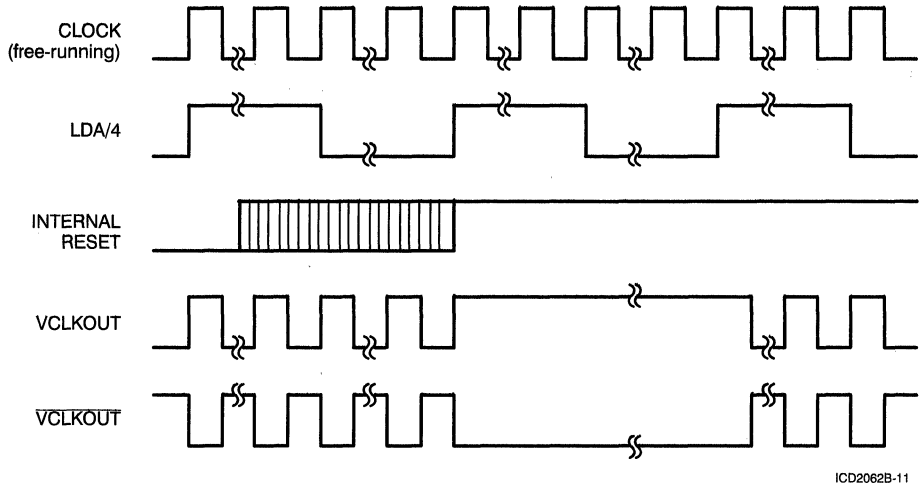


Figure 9. Internal RESET Timing

Power Management Issues

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I=C \bullet V \bullet f$, where

I=current,
C=load capacitance (max. 25 pF),
V=output voltage (usually 5V for TTL pads, 1.5V for ECL pads),
f=output frequency (in MHz).

To calculate total operating current, sum the following:

MCLKOUT ⇒ $C \bullet V \bullet f_{(MCLKOUT)}$
VCLKOUT ⇒ $C \bullet V \bullet f_{(VCLKOUT)}$; (ECL pad, V=1.5V)
$\overline{VCLKOUT}$ ⇒ $C \bullet V \bullet f_{(VCLKOUT)}$; (ECL pad, V=1.5V)
LDA ⇒ $C \bullet V \bullet f_{(LDA)}$
LDA/2 ⇒ $C \bullet V \bullet f_{(LDA/2)}$
LDA/4 ⇒ $C \bullet V \bullet f_{(LDA/4)}$
LDC ⇒ $C \bullet V \bullet f_{(LDC)}$
Internal ⇒ 12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5 to 10 pF loading, depending on package type.

Table 12. Typical Values

Frequency	Capacitive Load	Current (mA)
LOW	LOW	15
HIGH	LOW	50
HIGH	HIGH	100

Output Enable Pin

When the OE pin is asserted (active HIGH), all the output pins except XTALOUT and $\overline{ERROUT}$ enter a high-impedance mode, to support automated board testing.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{OH(ECL)}$	ECL Output HIGH Voltage[5]		V_{DD}−1.0	V_{DD}−0.8	V
$V_{OL(ECL)}$	ECL Output LOW Voltage		V_{DD}−2.0	V_{DD}−1.6	V
$V_{OH(TTL)}$	TTL Output HIGH Voltage[6]	I_{OH} = −4.0mA	2.4		V
$V_{OL(TTL)}$	TTL Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V
V_{IL}	Input LOW Voltage	Except on Crystal Pins		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IL} = 0.5V		−250	µA
I_{OZ}	Output Leakage Current	Three-state outputs		10	µA
I_{DD}	Power Supply Current	A/B, Inputs @ V_{DD} and GND	15	150/200	mA
I_{DD-TYP}	Power Supply Current	Typical= 45, @ 60 MHz			mA
$C_{OUT(ECL)}$	ECL Output Capacitance			10	pF

Note:
4.. Input capacitance is typically 10 pF, except for the crystal pins.
5. ECL outputs: VCLKOUT, $\overline{\text{VCLKOUT}}$.
6. TTL outputs: MCLKOUT, LDA, LDA/2, LDA/4, LDC, $\overline{\text{ERROUT}}$.

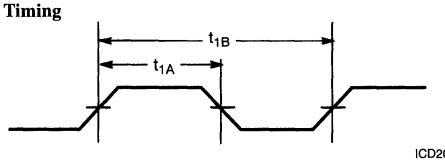
Switching Characteristics Over the Operating Range

Parameter	Name	Description		Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value (Note: for references of other than 14.318 MHz, the pre-loaded ROM frequencies will not be accurate.)		1	14.318	25	MHz
$t_{(REF)}$	Reference Clock Period	$1 \div f_{(REF)}$		40		1000	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_{1A} \div t_{1B}$		25%	50%	75%	
t_2	Output Clock Periods	Output values	ECL	6.1 165 MHz		1970 508 kHz	ns
			TTL	8.3 120 MHz		1970 508 kHz	
t_3	Output Duty Cycle	Duty cycle for the outputs[7]		40%		60%	
t_4	Rise Times	Rise time for the outputs into a 25-pF load				4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load				4	ns
$t_{skew\text{-}ECL}$		Skew between the VCLKOUT complementary outputs				1	ns
t_{freq1}	freq1 Output	Old frequency output					
t_{freq2}	freq2 Output	New frequency output					
t_A	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency		$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
$t_{timeout}$	Timeout Interval	Internal interval for serial programming and for VCO changes to settle[8]		2	5	10	msec
t_B	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value		$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_6	Three-state	Time for the outputs to go into three-state mode after OE signal assertion		0		12	ns
t_7	CLK Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH		0		12	ns
t_{LD}	Load Clock Period	Maximum LDA and LDC period		10			ns
$t_{SKEW\text{-}LDA}$		VCLKOUT to LDA output skew		2		6	ns
$t_{SKEW\text{-}LDA/2}$		LDA to LDA/2 output skew		0	1	2	ns
$t_{SKEW\text{-}LDA/4}$		LDA to LDA/4 output skew		0	1	2	ns
$t_{SKEW\text{-}LDC}$		LDA to LDC output skew		0	1	2	ns
$t_{EN\text{-}SU}$		ENABLE set-up time to LDA		12			ns
$t_{EN\text{-}HD}$		ENABLE hold time to LDA		0			ns
t_{serclk}		Clock period of serial clock		$2 \times t_{(REF)}$		2	msec
t_{HI}		Minimum HIGH time of serial clock		$t_{(REF)}$			ns
t_{LO}		Minimum LOW time of serial clock		$t_{(REF)}$			ns
t_{SU}		Set-Up time		20			ns
t_{HD}		Hold time		10			ns
t_{ldcmd}		Load command		0		t_1+30	ns

Notes:
7. For non-ECL outputs, duty cycle is measured at CMOS threshold levels. At 5V, V_{TH}=2.5V.
8. If the interval is too short, see the Timeout Interval section in the Control register definition.

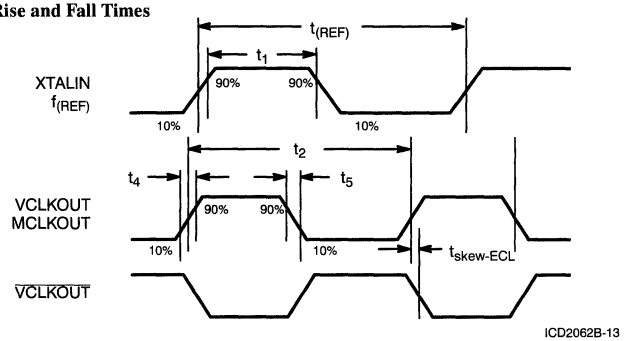
Switching Waveforms

Duty Cycle Timing



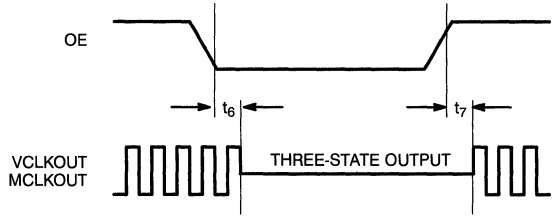
ICD2062B-12

Rise and Fall Times



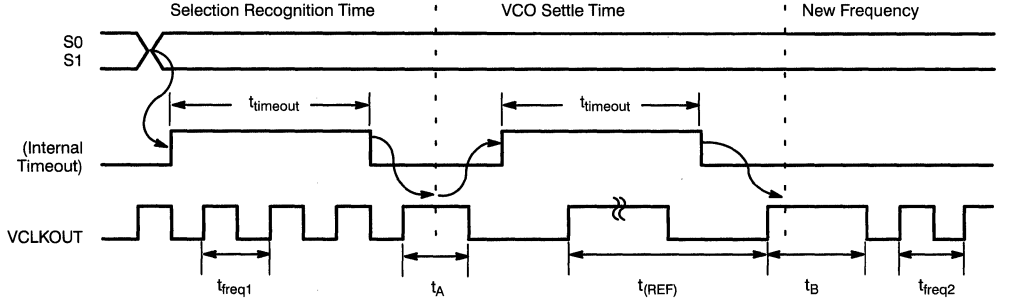
ICD2062B-13

Three-State Timing



ICD2062B-14

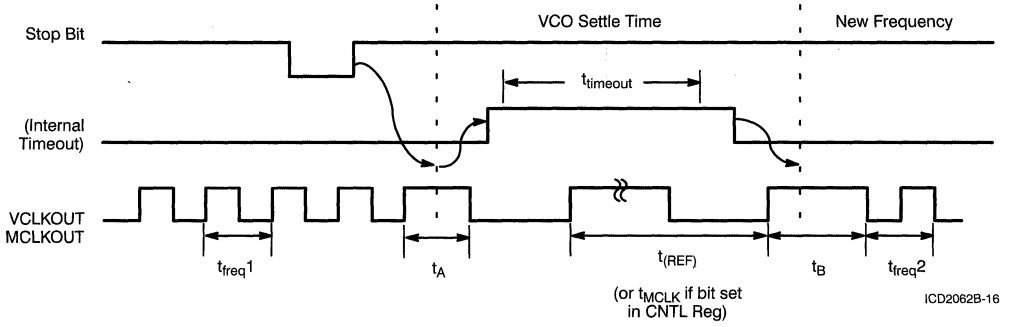
Selection Timing



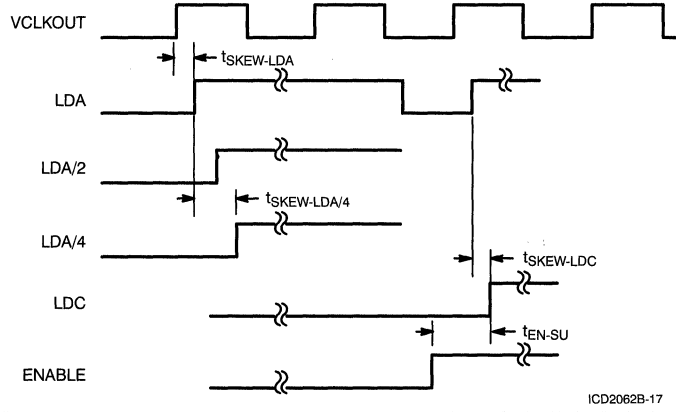
ICD2062B-15

Switching Waveforms (continued)

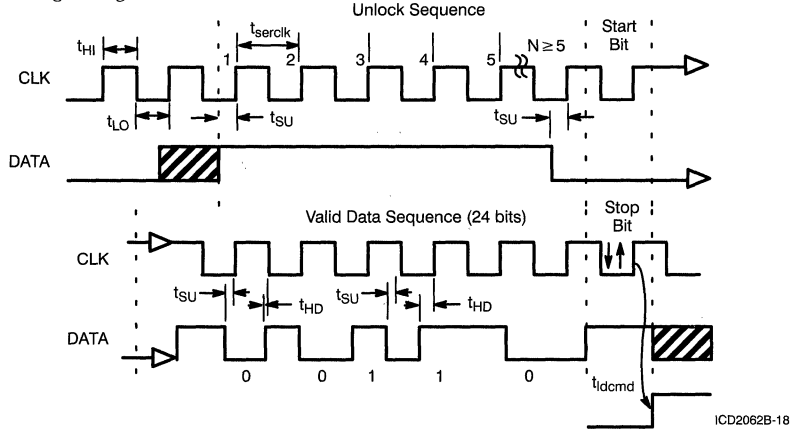
MCLK and Active VCLK Register Programming Timing



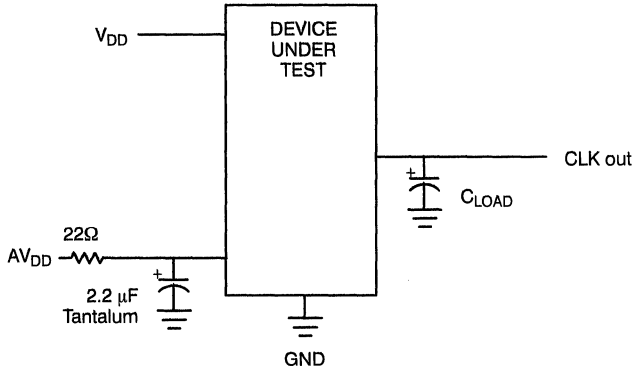
RAMDAC/VRAM Interface Timing



Serial Programming Timing



Test Circuit



Ordering Information[9]

Ordering Code	Package Name	Package Type	Operating Range
ICD2062B	S5	20-Pin SOIC	Commercial[10]

Notes:
9. Please call your local Cypress representative.
10. 0°C to +70°C

Example: order ICD2062BSC–2 for the ICD2062B, 20-pin plastic SOIC, commercial temperature range device with a top Video Clock frequency range of 165 MHz.

Document #: 38–00404

ICD2063

Programmable Graphics Clock Generator

Features

- **Second generation dual PLL graphics clock generator**
- **Compatible with the ICD2061A**
- **2 independent clock outputs:**
  - **—VCLK Output— 390 kHz – 135 MHz (100 MHz at 3.3V)**
  - **—MCLK Output 312 kHz – 100 MHz (80 MHz at 3.3V)**
- **Individually programmable PLLs using a highly reliable, Manchester-encoded, 21-bit serial data word**
- **2-pin serial programming interface allows direct connection to most graphics chip sets with no external hardware required**
- **2 advanced power-down capabilities**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.318 MHz crystal**
- **3.3V and 5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package configuration**

Functional Description

The ICD2063 Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2063 offers the selection ease of ROM-based clock chips and the versatility of serially programmable frequency synthesizers. It features both 3.3V and 5V operation with advanced power-down capabilities, making it ideally suited for the portable computer market.

The ICD2063 Dual Programmable Graphics Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between limits which depend on selected modes and operating voltage. The ICD2063 is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators or less functional ROM-based clock synthesizers.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2063 makes it ideal wherever two variable, yet highly accurate clock sources are required.

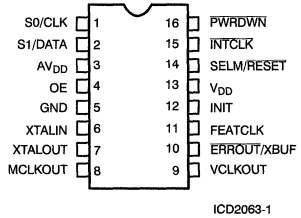
ICD2063 Changes from the ICD2061A

The ICD2063 revision of the ICD2061A is a complete mask redesign which includes many feature enhancements. The following major modifications have been implemented:

- **3.3V Operation**—The ICD2063 supports 3.3V operation in addition to 5V operation.
- **Expanded Register Set**—There are now 4 Video registers and 2 Memory registers. This allows better support for Windows NT drivers.
- **Expanded VCO Range**—The upper frequency limit has been increased to 135 MHz.
- **No Index Field Required**—The Serial Word now treats the Index Field (Mode Field) as a "Don't Care" bit region, for complete software compatibility with the ICD2061A.
- **Buffered Crystal Output** (Optional)—XBUF Output may be specified, replacing the $\overline{\text{ERROUT}}$ signal.
- **Smooth Frequency Transition**—The two phase-locked loops now transition smoothly from one frequency to another.
- **No MUXREF Required**—The necessity for the MUXREF procedure has been eliminated by the smooth frequency transition. For compatibility with the ICD2061A, there is an option which multiplexes a known output during frequency transitions. New to the ICD2063 is that the VCLK VCO is multiplexed to the MCLK output. See the *MUXREF Option* section for details.
- **Very High Frequency Resolution**—The MCLK Phase-Locked Loop Output can be multiplexed to the VCLK PLL Reference Input, thus enabling very high frequency resolution, at the expense of slightly higher jitter. See the *Extended VCLK Frequency Precision* section.
- **Reduced Register Initialization ROM**—The former INIT2 pin now selects between the 2 memory registers MREG0 and MREG1.
- **Hardware Reset** (Optional)—A hardware reset is available as an option, replacing the memory selection signal.

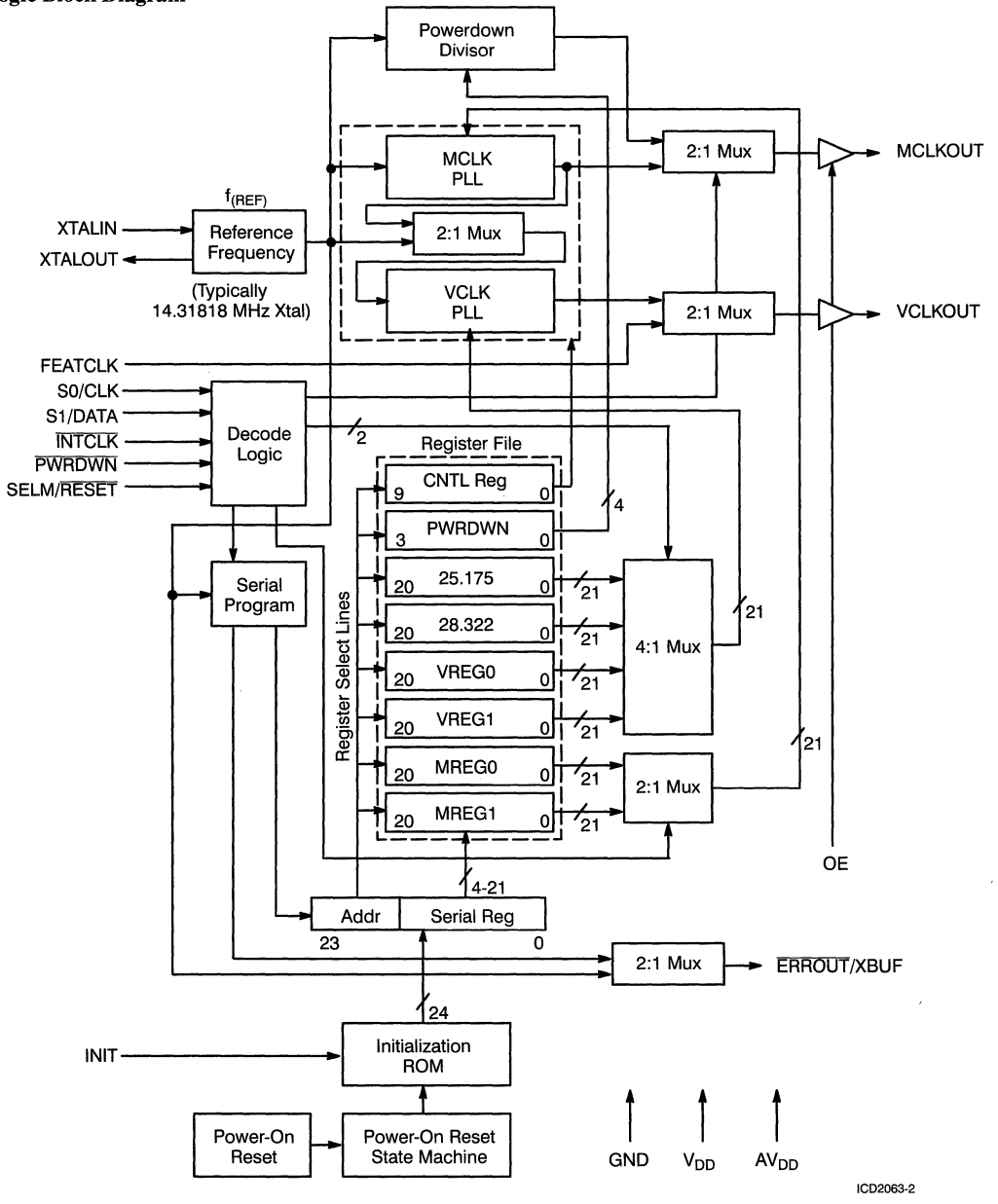
Pin Configuration

SOIC
Top View



ICD2063-1

Logic Block Diagram



Pin Summary

Name	Number	Description
S0/CLK	1	Bit 0 (LSB) of frequency select logic, used to select PLL frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
S1/DATA	2	Bit 1 (MSB) of frequency select logic, used to select PLL frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
AV_{DD}	3	+5V or 3.3V to Analog Core
OE	4	Output Enable. Three-states output when pulled LOW. (Internal pull-up allows no connect.)
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
MCLKOUT	8	Memory Clock output
VCLKOUT	9	Video Clock output
$\overline{\text{ERROUT}}$/ XBUF	10	Error Output: a LOW signals an error during serial programming –OR– Buffered Crystal Reference Output (selectable via configuration option)
FEATCLK	11	External clock input (Feature Clock) (Internal pull-up allows no-connect.)
INIT	12	Selects state of initialization ROM during power-up. See *Table 2.* (This pin has no internal pull-up or pull-down; it *must* be tied HIGH or LOW externally.)
V_{DD}	13	+5V or 3.3V to I/O Ring
SELM/$\overline{\text{RESET}}$	14	Selectable via configuration option: SELM—Selects 1 of 2 Memory Clock Output (MCLKOUT) frequencies (see *Register Selection* subsection *MCLKOUT*) $\overline{\text{RESET}}$—Hardware RESET control signal (see the *Power-On Reset, RESET, and Register Initialization* section)
$\overline{\text{INTCLK}}$	15	Selects the Feature Clock external clock input as VCLKOUT output (Internal pull-up allows no-connect.) (See *Table 3.*)
$\overline{\text{PWRDWN}}$	16	Power-down pin (active LOW) (Internal pull-up allows no-connect if power-down operation not required. See *Power Management Issues* for specific details concerning the use of this pin.)

Register Definitions

Register File

The Register File consists of the following registers and their respective addresses in the Serial Data register:

Table 1. Register Addressing[2]

A2	A1	A0	Register	Usage
0	0	0	25.175 MHz	Fixed Video Clock Frequency
0	0	1	28.322 MHz	Fixed Video Clock Frequency
0	1	0	VREG0	Programmable Video Clock Register 0
0	1	1	MREG0	Programmable Memory Clock Register 0
1	0	0	PWRDWN	Divisor for Power-Down mode
1	0	1	VREG1	Programmable Video Clock Register 1
1	1	0	CNTL	Control Register
1	1	1	MREG1	Programmable Memory Clock Register 1

Notes:

1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD}=17 pF.
2. All register values are preserved in power-down mode.

Power-On Reset, $\overline{\text{RESET}}$, and Register Initialization

On power-up the ICD2063 Clock Generator initializes all of its registers to a known state upon power-up. This is implemented by the Power-On initialization circuitry. Two Video Clock registers and two Memory Clock registers are initialized based on the state of the INIT pin at power-up.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pin must be strapped to V_{DD} or GND.

If the $\overline{\text{RESET}}$ option on pin 14 is chosen, then this pin, when pulled LOW, forces the equivalent of a Power-On Reset operation: the registers are reloaded with the contents of the initialization ROM (depending on the state of the INIT pin).

The various registers are initialized as shown in *Table 2* (all frequencies in MHz).

Table 2. Register Initialization ROM

INIT Pin	25.175	28.322	VREG0	VREG1	MREG0	MREG1
0	25.175	28.322	36.000	44.900	40.000	40.000
1	25.175	28.322	40.000	65.000	45.000	45.000

Register Selection

VCLKOUT

The Video Clock output is controlled not only by the S0, S1, and $\overline{\text{INTCLK}}$ pins, but also by the $\overline{\text{PWRDWN}}$ and OE inputs. Additionally, the clock generator may be multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. *Table 3* shows the VCLKOUT selection criteria.

Table 3. VCLKOUT Selection

OE	PWRDWN	$\overline{\text{INTCLK}}$	S1	S0	VCLKOUT
0	X	X	X	X	High-Z
1	0	X	X	X	Forced LOW
1	1	X	0	0	25.175 MHz
1	1	X	0	1	28.322 MHz
1	1	0	1	0	FEATCLK
1	1	1	1	0	VREG0
1	1	X	1	1	VREG1

The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming functionality. If serial programming was not started at the end of the timeout interval, new register selection occurs, at which point the frequency changes to a new value. See the *Serial Programming Architecture* section for selection and transition details.

MCLKOUT

The Memory Clock output (MCLKOUT) is selected by $\overline{\text{PWRDWN}}$, OE, and by—depending on which configuration is chosen—either the SELM input or the S0 and S1 inputs, as shown in *Tables 4* and *5*.

If the Memory Select option on pin 14 is chosen, then the SELM input is available to set MCLKOUT and the decode is defined as shown in *Table 4*.

Table 4. MCLKOUT Selection (Memory Select Mode)

OE	PWRDWN	SELM	MCLKOUT
0	X	X	High-Z
1	0	X	PWRDWN or LOW (depending on mode)
1	1	0	MREG0
1	1	1	MREG1

If the $\overline{\text{RESET}}$ option is chosen, the MCLKOUT and VCLKOUT are both selected using the S0 and S1 pins (MREG1 can *only* be selected when VREG1 is selected).

See the *Frequency Transition Options* section for more specifics.

Table 5. MCLKOUT Selection (Reset Mode)

OE	PWRDWN	$\overline{\text{INTCLK}}$	S1	S0	VCLKOUT	MCLKOUT
0	X	X	X	X	High-Z	High-Z
1	0	X	X	X	Forced LOW	PWRDWN or LOW (depending on mode)
1	1	X	0	0	25.175 MHz	MREG0
1	1	X	0	1	28.322 MHz	MREG0
1	1	0	1	0	FEATCLK	MREG0
1	1	1	1	0	VREG0	MREG0
1	1	X	1	1	VREG1	MREG1

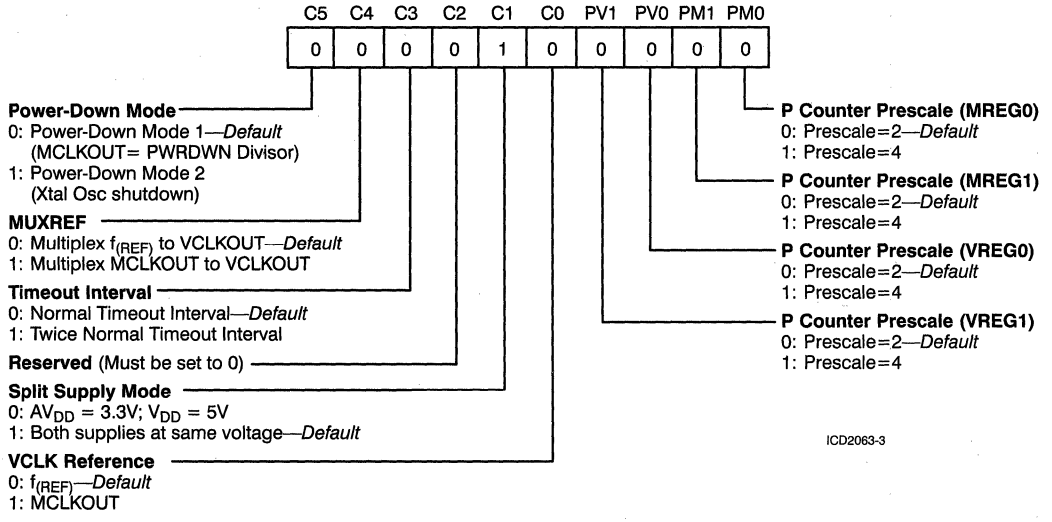


Figure 1. Control Register Definition

Control Register Definition

The Control Register (CNTL) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1.*

VCLK Reference—This control bit determines whether the VCLK VCO uses $f_{(REF)}$ or the MCLK output as a reference. Refer to the *Extended VCLK Frequency Precision* section for more details.

Split Supply Mode—This control bit allows mixing 3.3V (AV_{DD}) and 5V (V_{DD}) supplies. The default is for both to be the same (5V or 3.3V). The alternative is AV_{DD} = 3.3V, V_{DD} = 5V. See the *3.3 Volt and 5 Volt Issues* section for more details. The purpose is to maintain duty cycle 50%.

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics*. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

MUXREF (MUXREF Mode only)—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Power-Down Mode—This control bit determines which Power-Down Mode the $\overline{PWRDWN}$ pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section entitled *Power Management Issues*.

P Counter Prescale (VREG0, VREG1, MREG0, MREG1)—These control bits determine whether or not to prescale the P Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail in the *Prescaling* section.

Serial Programming Architecture

The ICD2063 programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See ICD2063 Logic Block Diagram) contains several components: a Serial Unlock Decoder (containing the unlocking mechanism and Manchester decoder), a watchdog timer, the Serial Data register and a Demultiplexer to the Register File (see *Figure 2*).

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in *Figure 3*.

The initial unlock sequence consists of at least five LOW-to-HIGH transitions of CLK with DATA HIGH, followed immediately by a single LOW-to-HIGH transition of CLK with DATA LOW. Following this unlock sequence, the encoded serial data is clocked into the Serial Data register.

Note that the ICD2063 may not be serially programmed when in Power-Down Mode.

Watchdog Timer

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. Throughout the entire programming process, the watchdog timer ensures that there is a transition on CLK or DATA within the timeout specification (of 2 msec—see *Switching Characteristics*.) If a timeout does occur, the lock mechanism is rearmed and the current data in the Serial Data register is ignored.

Since the VCLK registers are selected by the S0 or S1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted

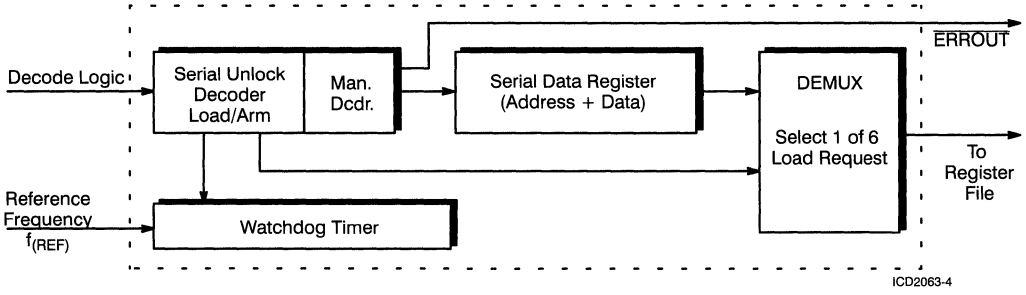


Figure 2. Serial Programming Block Diagram

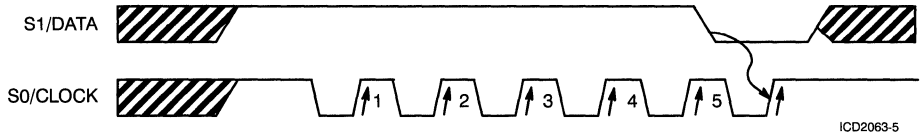


Figure 3. Unlock Sequence

to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of S0 and S1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. Note that there is a latency amounting to the duration of the Watchdog Timer before any new register selections take effect.

Serial Data Register

The serial data is clocked into the Serial Data register in the order shown in *Figure 4*.

The serial data is sent using a modified Manchester-encoded data format. This is defined as:

1. An individual data bit is sampled on the rising edge of CLK.
2. The complement of the data bit must be sampled on the previous falling edge of CLK.
3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the "Serial Programming Timing" section in the switching waveforms..

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (VREG0–1, MREG0–1), the data is made up of 4 fields: D[20:18] = Mode (formerly Index); D[17:11]=P'; D[10:8]=Post-VCO Divider; D[7:1]=Q'. (See the *Programming the ICD2063* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (PWRDWN, CNTL), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is

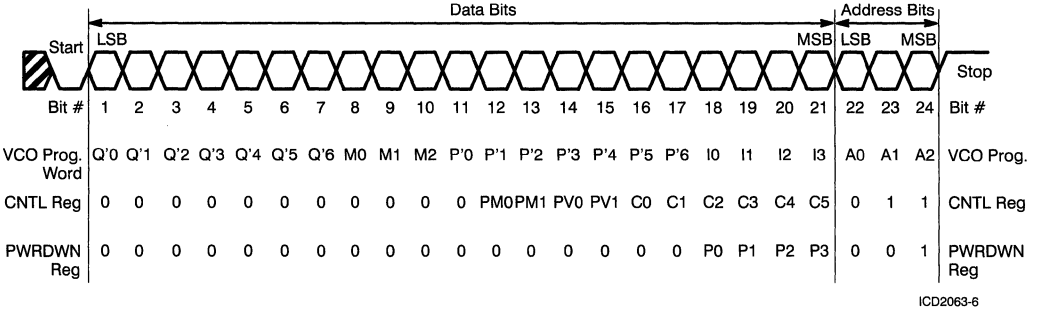


Figure 4. Serial Data Timing

issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing data HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Data register contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

$\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to report when a program error has been detected internally by the ICD2063. The signal stays active until the next unlock sequence.

Figure 5 shows the basic mechanism used to detect valid and erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect start bit, incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

Note that if there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

Note also that the $\overline{\text{ERROUT}}$ signal is an order option. If the XBUF option is chosen instead, then $\overline{\text{ERROUT}}$ is not available, and the user may want to implement the above technique to verify that the desired programming did indeed take place.

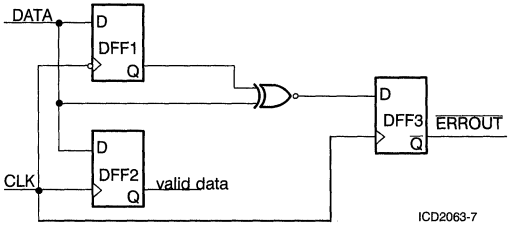


Figure 5. Serial Data Timing

Programming the ICD2063

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2063 has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

Table 6. Programming Word Bit Fields

Field	# of bits	Notes
Mode (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Post-VCO Divisor (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P'=P-3$$
$$Q'=Q-2$$
$$f_{(VCO)}=(\text{Prescale} \times f_{(REF)} \times P/Q)$$

where $f_{(REF)}$=Reference frequency (between 1 MHz–60 MHz; typically 14.31818 MHz) and Prescale=2 or 4 (default is 2, defined by CNTL Reg).

Note that if a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

Table 7 lists the various limits for $f_{(VCO)}$.

Table 7. VCO Frequency Ranges

	5 Volt Operation	3.3 Volt Operation
VCLK PLL	50 MHz – 135 MHz	50 MHz – 100 MHz
MCLK PLL	40 MHz – 100 MHz	40 MHz – 80 MHz

For lower output frequencies, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO divisor is selected by setting the values of the Post-VCO Divider field (M). See *Table 8*.

Table 8. Post-VCO Divider (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Mode Field (I), formerly the Index Field, is included for historical reasons to preserve software compatibility with the ICD2061A. In the ICD2063, it is only used for a few special circumstances, as detailed in the following paragraphs.

Table 9. Index Field (I)

I	VCLK VCO	MCLK VCO
0000	50.0 – 51.0	50.0 – 51.0
0001	51.0 – 53.2	51.0 – 53.2
0010	53.2 – 58.5	53.2 – 58.5
0011	58.5 – 60.7	58.5 – 60.7
0100	60.7 – 64.4	60.7 – 64.4
0101	64.4 – 66.8	64.4 – 66.8
0110	66.8 – 73.5	66.8 – 73.5
0111	73.5 – 75.6	73.5 – 75.6
1000	75.6 – 80.9	75.6 – 80.9
1001	80.9 – 83.2	80.9 – 83.2
1010	83.2 – 91.5	83.2 – 91.5
1011	91.5 – 100.0	91.5 – 100.0
1100	100.0 – 120.0	100.0 – 120.0
1101	100.0 – 120.0	100.0 – 120./0
1110	VCLK VCO is turned off and output is forced LOW	Ignored[3]
1111	VCLK is turned off and both channels run from the same MCLK VCO	Ignored[3]

The Mode Field was included to allow turning off the VCLK VCO and optionally multiplexing the MCLK VCO, then dividing down to the desired frequency. This will significantly reduce heterodyne jitter and is useful if the frequencies are 2^n multiples.

When the Index Field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, do not run the two VCOs at integral multiples of each other. Hence, to obtain output clocks which are integral multiples of each other, multiplex the MCLK VCO to VCLKOUT and divide down to the desired frequency.

The MCLK VCO completely ignores the Mode Field values. For new designs, Cypress/IC Designs recommends the setting the Mode Field to 0000.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program that automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers.

Programming Constraints

Table 10 shows the primary programming constraints of which the user must be aware:

Note:

3. In MUXREF mode, the memory clock cannot be changed—neither by the selects nor by reprogramming—because the VCLK is shut down and the MCLK is multiplexed to VCLK..

Table 10. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	60 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$ (VCLK)	5V: 50 MHz 3.3V: 50 MHz	5V: 135 MHz 3.3V: 100 MHz
$f_{(VCO)}$ (MCLK)	5V: 40 MHz 3.3V: 40 MHz	5V: 100 MHz 3.3V: 80 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the *BitCalc* program, these constraints become transparent.

Programming Example

The following is an example of the calculations *BitCalc* performs. This example assumes that Prescaling = 2, which is the default value.

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency and V_{DD} = 5:

Since 39.5 MHz<50 MHz, double it to 79.0 MHz. Set M to 001. Since I is a "Don't Care," set it to 0000. The result:

$$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$$
$$P/Q = 2.7587$$

Several choices of P and Q are available:

Table 11. P&Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

and by concatenating I=0000, P'=1001101, M=001, Q'=0011011, we obtain the programming word

W=00001001101001001101 1 (01349bH)

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the *Serial Programming Architecture* section.

Prescaling Example

For most users, the resolution of the ICD2063 in its default modes is sufficient. For those demanding greater precision, Prescale can be set to 4. This section provides an example.

Assume the desired VCLKOUT frequency is 100 MHz. *Table 12* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 12. Effects of Prescaling

Prescale	Desired Freq. (MHz)	Actual Freq. (MHz)	P	Q	Error (PPM)
2	100	99.84028	129	37	1600
4	100	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before. However, if it is desired to program a new frequency without prescaling, a new Control Word must first be loaded with the proper bits set, with the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: The results will be unpredictable at best, and it could cause the VCO to go out of lock.

Extended VCLK Frequency Precision

An optional mode set in the CNTL register allows the VCLK PLL to use the MCLK PLL as its reference frequency instead of $f_{(REF)}$. The advantage is that, by proper tuning of the input reference, *very* fine frequency control is possible on the output of VCLK.

Just about any desired value can be achieved with worst-case precision of less than 5 ppm.

The reference frequency oscillator is used to drive the MCLK PLL, which is then fed internally to the VCLK PLL to generate the desired signal. However, please note the following:

- **No usable MCLK output**—This method essentially uses two PLLs to derive a single output, so that the MCLK output will probable be meaningless. Therefore, this method is probably not suited to normal VGA graphics applications.
- **Some increased jitter**—The trade-off associated with deriving the VCLK PLL reference from another PLL is that the MCLK+VCLK combination will tend to exhibit more jitter than a single PLL with a crystal-controlled reference—but the jitter should stay below 1 ns.
- **More challenging programming model**—Another trade-off of having 21 bits each to define both the reference frequency and the output is that it makes finding the optimum 2 programming words an iterative process. To aid in these calculations, Cypress/IC Designs strongly recommends using *BitCalc*, a utility designed to help in this analysis.

Power Management Issues

Power-Down Mode 1

The ICD2063 contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the $\overline{PWRDWN}$ signal LOW and having the proper CNTL register bit set to zero), both VCOs are shut down, the VCLKOUT output is forced LOW, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The power-down MCLKOUT value is determined by the following equation:

$MCLKOUT_{Power\text{-}Down} = f_{(REF)} \div$ (PWRDWN Reg Divisor Value)

The Power-Down register divisor is determined according to the following 4-bit word programmed into the PWRDWN register. (See *Table Table 11.*)

Table 13. PWRDWN Register Programming

PWRDWN bits				PWRDWN Register Value (Hex)	Power-Down Divisor	$MCLKOUT_{Power\text{-}Down}$ ($f_{(REF)}$=14.31818 MHz)
P3	P2	P1	P0			
0	0	0	0	0	N/A	N/A
0	0	0	1	1	32	447.4 kHz
0	0	1	0	2	30	477.3 kHz
0	0	1	1	3	28	511.4 kHz
0	1	0	0	4	26	550.7 kHz
0	1	0	1	5	24	596.6 kHz
0	1	1	0	6	22	650.8 kHz
0	1	1	1	7	20	715.9 kHz
1	**0**	**0**	**0**	**8**	**18 (default)**	**795.5 kHz**
1	0	0	1	9	16	894.9 kHz
1	0	1	0	A	14	1.023 MHz
1	0	1	1	B	12	1.193 MHz
1	1	0	0	C	10	1.432 MHz
1	1	0	1	D	8	1.790 MHz
1	1	1	0	E	6	2.386 MHz
1	1	1	1	F	4	3.580 MHz

On power-up, the value of the PWRDWN register is loaded with a default value of 8 (1000 binary), which yields an MCLKOUT frequency of 795 kHz (14.31818/18). The default mode is Power-Down Mode 1.

Note that the ICD2063 may not be serially programmed when in Power-Down Mode.

Power-Down Mode 2

If there is no need for any output during power-down operation, then an alternate Power-Down Mode is available, which will completely shut down all outputs and the reference oscillator, yet still preserve all register contents. This results in the absolute least power consumption.

Power-Down Mode 2 is invoked by first programming the power-down bit in the CNTL register, and then pulling the $\overline{\text{PWRDWN}}$ pin LOW.

The XTALIN pin is forced LOW; therefore if an external reference clock is used instead of a crystal, it must be stopped LOW.

The $\overline{\text{PWRDWN}}$ Pin

This pin has a standard internal pull-up during normal operation. When the user pulls it down to invoke Power-Down Mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which significantly reduces power consumption. If, after pulling this pin LOW, the pin is allowed to float, the weak pull-up will gradually cause the signal to rise, enabling the normal pull-up, and will eventually turn the device back on.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I=C \bullet V \bullet f$, where:

I=current (in mA)
C=Load capacitance (max., 25 pF)
V=output voltage (usually 5V or 3.3V)
f=output frequency (in MHz)

To calculate total operating current, sum the following terms:

$I_{(VCLKOUT)} \Rightarrow C \bullet V \bullet f_{(VCLK)}$
$I_{(MCLKOUT)} \Rightarrow C \bullet V \bullet f_{(MCLK)}$
$I_{(XBUF)}$ (if used) $\Rightarrow C \bullet V \bullet f_{(REF)}$
$I_{(Internal)} \Rightarrow$ 12 mA @ 5V; 8 mA @ 3.3V

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5 to 10 pF loading, depending on package type.

Table 14. Typical Current Drain Values

Frequency	Capacitive Load	Current (mA)	
		5 Volts	3.3 Volts
LOW	LOW	15	10
HIGH	LOW	40	26
HIGH	HIGH	65	44

When in Power-Down Mode 1, and using a 14.31818 MHz reference crystal, the power consumption will not exceed 7.5 mA @ 5V or 5 mA @ 3.3V. In Power-Down Mode 2, the power consumption will not exceed 50 µA @ 5V or 35 µA @ 3.3V.

3.3 Volt and 5 Volt Issues

The ICD2063 can function in mixed 5V/3.3V systems. The following discussion will attempt to address the various issues involved in mixed supply usage of the ICD2063.

V_{DD} and AV_{DD}

The ICD2063 has two isolated power leads: V_{DD} and AV_{DD}. Each supply may be independently run at either 3.3V or 5V. The V_{DD} rail supplies power to the I/O pad ring and core. All outputs and inputs are referenced to this voltage input. The device has a 4-Volt Detector which determines the pin's operating voltage and adjusts the threshold for the input pins. This guarantees that at either voltage, the inputs maintain TTL compatibility. If the voltage dynamically changes on the V_{DD} line (for instance going from 5V to 3.3V), the thresholds will be maintained properly.

The AV_{DD} pin supplies power to the VCO core. Since the VCO needs to know what the supply voltage is, a second 4-Volt Detector is placed on AV_{DD} to set the VCO operation properly. If the voltage dynamically changes on the AV_{DD} line (again, say from 5V to 3.3V), the VCOs will lose lock momentarily when the 4-Volt Detector triggers, and will re-lock to the desired value after a brief settling time. (See *Figure 6.*) This time should be less than 5 msec. This period of instability could cause a glitch in the output.

If a system requires dynamically changing from 5V to 3.3V and back (for example, some docking stations), and proper glitch-free output must be maintained during the transition period, then the AV_{DD} supply line should remain at 3.3 Volts while the V_{DD} pin can float to the desired levels. If this split mode is to be used, then the Split Supply Mode bit should be properly set in the Control register. (See the *Control Register Definition* section for more details.) Also note that, in this mode, the frequency range is limited to the narrower 3.3V values

Mixed Voltage Interfaces

The other issue which must be addressed is interfacing the ICD2063 into mixed-voltage systems. *Tables 15* and *16* depict the various configurations.

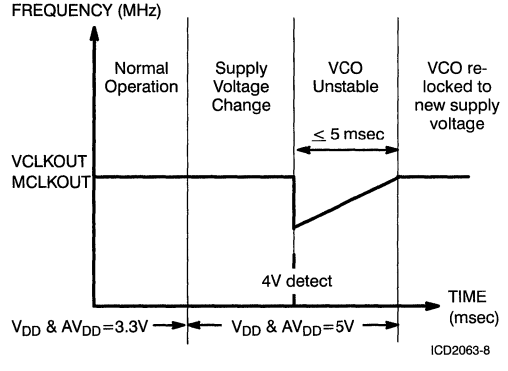


Figure 6. Effect of Supply Voltage Change to Clock Output

Table 15. Driving other Devices with the ICD2063

ICD2063 → Other Device		Status
5V	5V	OK
3.3V	5V	OK if driving TTL inputs; if driving CMOS inputs, then ICD2063 output will appear to have a low duty cycle.
5V	3.3V	Potential latch-up problems with other devices; will work if other device's input will accept $V_{IH}=V_{DD}+2V$.
3.3V	3.3V	OK

Table 16. Driving the ICD2063 with Other Devices

Other Device → ICD2063		Status
5V	5V	OK
3.3V	5V	OK
5V	3.3V	TTL outputs only; input to ICD2063 must not exceed $V_{DD}+0.3V$
3.3V	3.3V	OK

Frequency Transition Options

The ICD2063 may be configured for one of two frequency transition options: the Smooth Transition Option or the MUXREF Option (for compatibility with the ICD2061A).

Smooth Transition Option

Upon changing VCLK or MCLK, either by reprogramming the active register or by selecting a new register, the output will transition in one of two basic ways, depending on the post-divide values (Post-divide is used to divide down the VCO output to frequencies below the normal VCO operating range):

- **Normal Operation**—If the post-divide value (M) is the same for both frequencies (original and target), then the output will transition smoothly and linearly from the original to the target frequency, with no overshoot (see *Figure 7*).
- **Post-Divide Operation**—If the post-divide value (M) differs between the original and target frequencies, then the output behaves somewhat differently, but will never exceed the greater of the original and target frequencies.
  1. If the post-divide value decreases then, first, a smooth transition occurs to an intermediate frequency (equal to target frequency ÷ post divider value); second, the post-divide is changed to the new value, resulting in an instantaneous transition to the target frequency (see *Figure 8*).
  2. If the post-divide value increases then, first, the post-divide value is changed to the new value, resulting in an instantaneous transition to an intermediate frequency (equal to the target frequency ÷ post divider value); second there is a smooth transition from this frequency to the target frequency (see *Figure 9*).

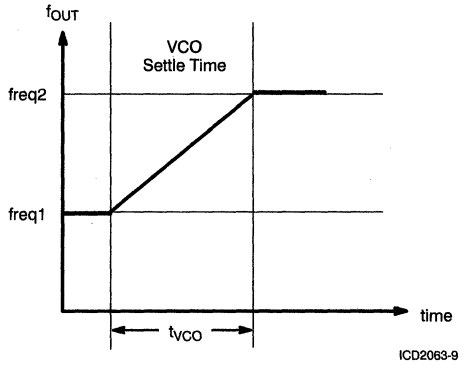


Figure 7. Frequency Transition—Smooth Mode: Normal Operation

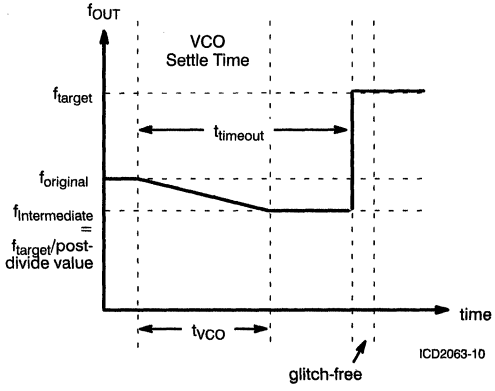


Figure 8. Frequency Transition—Post-Divide Value Decreases

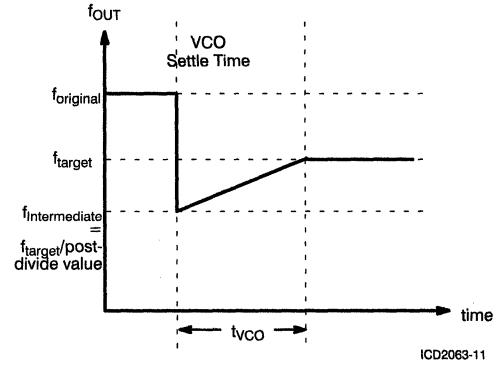


Figure 9. Frequency Transition—Post-Divide Value Increases

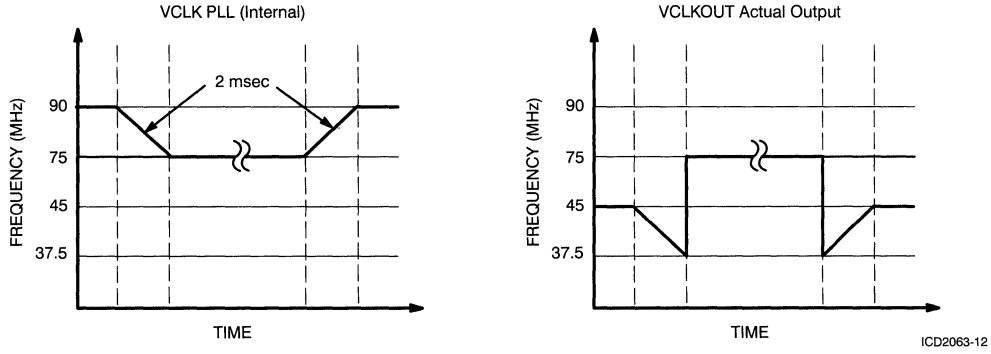


Figure 10. Smooth Frequency Transition Example

MUXREF Option

The other option for frequency transition is to multiplex the output of the VCO undergoing change to some alternate stable frequency until the VCO has settled to the new frequency value. This option preserves compatibility with the earlier ICD2061A.

In general, any changes to the VCLK VCO will result in the Reference Frequency ($f_{(REF)}$) being multiplexed to the output. However, since most video controllers now use the MCLK output as their principal clock source, and since an $f_{(REF)}$ of 14.31818 MHz is in many cases too slow for proper operation of the VGA chip, changes to the MCLK VCO will result in the VCLKOUT signal being multiplexed to the MCLK output.

The following five cases detail specifics about operation with the MUXREF option during frequency transitions.

Case 1: MCLK PLL Transition—Reprogramming of the Active Register

When a new frequency is being set for the active MCLK register, then a glitch-free multiplexing to the VCLKOUT signal is performed. For more details, see the *Active MCLK and VCLK Register Programming Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 2: VCLK PLL Transition—Reprogramming of the Active Register

When a new frequency is being set for the active VCLK register, then a glitch-free multiplexing to the reference signal $f_{(REF)}$ is performed. For more details, see the *Active MCLK and VCLK Register Programming Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 3: MCLK PLL Transition—Changing Register Selects

When a new MCLK frequency is being set by the register selects, then a glitch-free multiplexing to the VCLKOUT signal is performed. For more details, see the *Selection Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 4: VCLK PLL Transition—Changing Register Selects

When a new VCLK frequency is being set by the register selects, then a glitch-free multiplexing to the reference signal $f_{(REF)}$ is performed. For more details, see the *Selection Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 5: VCLK and MCLK PLL Transition—Changing Register Selects

If the Reset Option is configured and the select sequence is chosen which results in a coincident change in both MCLK and VCLK registers (i.e., selects go *from* being 11 or go *to* being 11), then first a new MCLK frequency is set with a glitch-free multiplexing to the current VCLKOUT signal, followed by the new VCLK frequency being set with a glitch-free multiplexing to the reference signal $f_{(REF)}$ being performed. For more details, see the *VCLK and MCLK Selection Timing* waveform in the *Switching Waveforms* section.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5% 3.3V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD} & AV_{DD}	Supply Voltage Relative to GND[5] 390 kHz – 100 MHz 390 kHz – 120 MHz 390 kHz – 135 MHz	VCLK specs shown (MCLK low end = 312 kHz)	 3.0 4.5 4.75		 3.6 5.5 5.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0mA	V_{DD}−0.5			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	Except on Crystal Pins	−0.3		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5			150	µA
I_{IL}	Input LOW Current	V_{IL} = +0.5V			−250	µA
I_{OZ}	Output Leakage Current	(Three-state)			10	µA
I_{DD}	Power Supply Current	5V/3.3V, Inputs @ V_{DD} or GND	15/10		65/44	mA
I_{DD-TYP}	Power Supply Current	5V/3.3V (60 MHz)		35/24	80/50	mA
I_{ADD}	Analog Power Supply Current				10	mA
I_{PD1}	Power-Down Current (Mode 1)	5V/3.3V		6/4	7.5/5.0	mA
I_{PD2}	Power-Down Current (Mode 2)	5V/3.3V		25/20	50/35	µA

Notes:
4. Input capacitance is typically 10 pF, except for the crystal pins.
5. For transition between 3.3V and 5V operation, refer to the *3.3 Volt and 5 Volt Issues* section.

Switching Characteristics Over the Operating Range

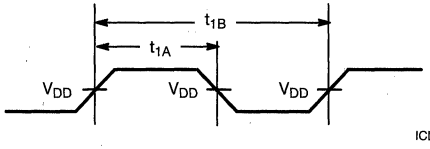
Parameter	Name	Description		Min.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value Typical = 14.318[6]		1	60	MHz
$t_{(REF)}$	Reference Clock Period	$t_{(REF)} = 1/f_{(REF)}$		16.6	1000	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_{1B} \div t_{1A}$		25%	75%	
t_2	Output Clock Periods	VCLK Output values	V_{DD}=5V	7.41 (135 MHz)	2564 (390 kHz)	ns
			V_{DD}=3.3V	10.0 (100 MHz)		
		MCLK Output values	V_{DD}=5V	10.0 (100 MHz)	3205 (312 kHz)	
			V_{DD}=3.3V	12.5 (80 MHz)		
t_3	Output Duty Cycle	Duty cycle for the outputs defined as $t_{1A} \div t_{1B}$[7]		40	60	%
t_4	Rise Times	Rise time for the outputs into a 25-pF load			4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load			4	ns
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_A	$f_{(REF)}$ Mux Time	Time clock output remains LOW while output muxes to reference frequency		$t_{(REF)}/2$	$3(t_{(REF)}/2)$	ns
$t_{timeout}$	Timeout Interval	Internal interval for special programming and for VCO changes to settle[8]		2	10	msec
t_B	t_{freq2} Mux Time	Time clock output remains LOW while output muxes to new frequency value		$t_{freq2}/2$	$3/(t_{freq2}/2)$	ns
t_6	Three-state Time	Time for the outputs to go into three-state mode after OE signal assertion		0	12	ns
t_7	CLK Valid Time	Time for the outputs to recover from three-state mode after OE signal goes HIGH		0	12	ns
t_8	Power-Down Delay	Time for Power-Down Mode of operation to take effect			12	ns
t_9	Power-Up Delay	Time for recovery from Power-Down Mode of operation			12	ns
t_{10}	MCLKOUT HIGH	Time for MCLKOUT to go LOW after $\overline{\text{PWRDWN}}$ is asserted HIGH		0	$1/t_{PWR\text{-}DWN}$	ns
t_{11}	MCLKOUT delay	Delay of MCLKOUT prior to f_{MCLK} signal at output		$t_{MCLK}/2$	$3/(t_{MCLK}/2)$	ns
t_{serclk}		Clock period of serial clock		$2 \times t_{(REF)}$	2	msec
t_{HI}		Minimum HIGH time		$t_{(REF)}$		ns
t_{LO}		Minimum LOW time		$t_{(REF)}$		ns
t_{SU}		Set-Up time		20		ns
t_{HD}		Hold time		10		ns
t_{ldcmd}		Load command		0	$t_{(REF)}+30$	ns

Notes:

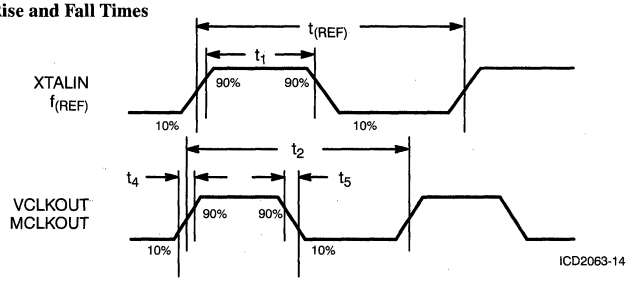
6. For references other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.
7. Duty cycle is measured at CMOS threshold levels ($V_{DD} \div 2$). At 5V, V_{TH}=2.5V.
8. If the interval is too short, see the Timeout Interval paragraph of the *Control Register Definition* section..

Switching Waveforms

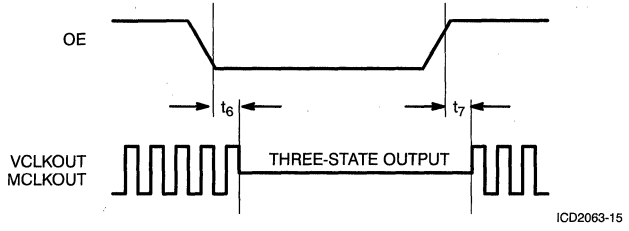
Duty Cycle Timing



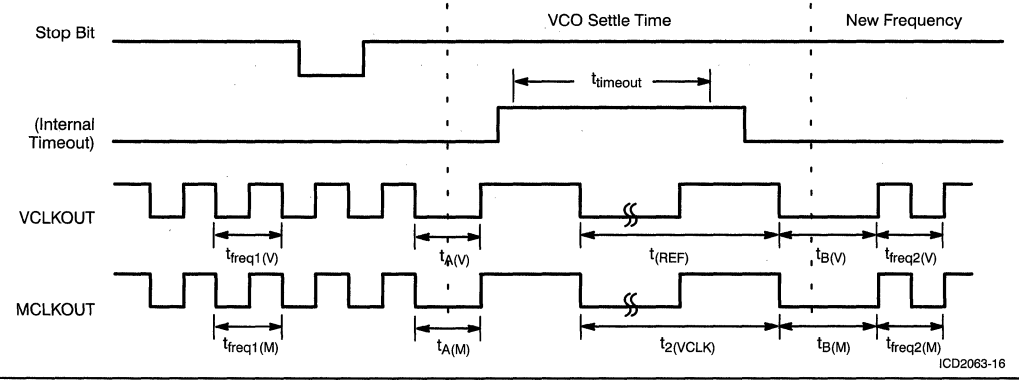
Rise and Fall Times



Three-State Timing

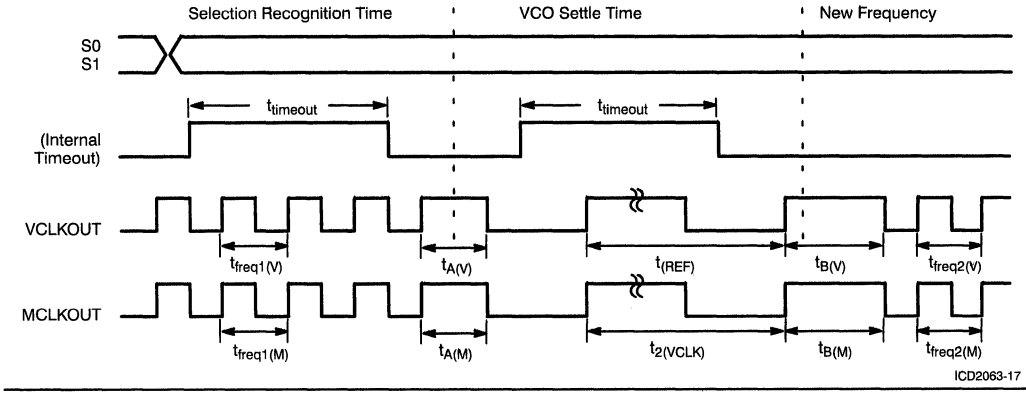


Active MCLK and VCLK Register Programming Timing (MUXREF Mode)

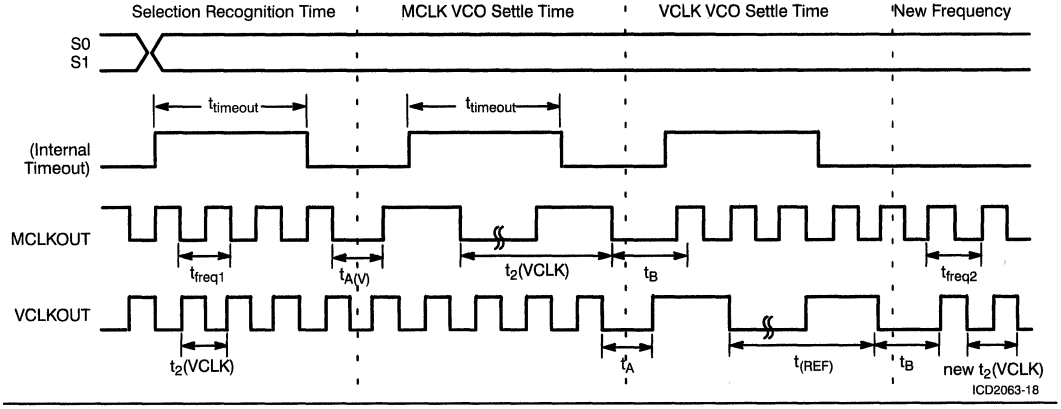


Switching Waveforms (continued)

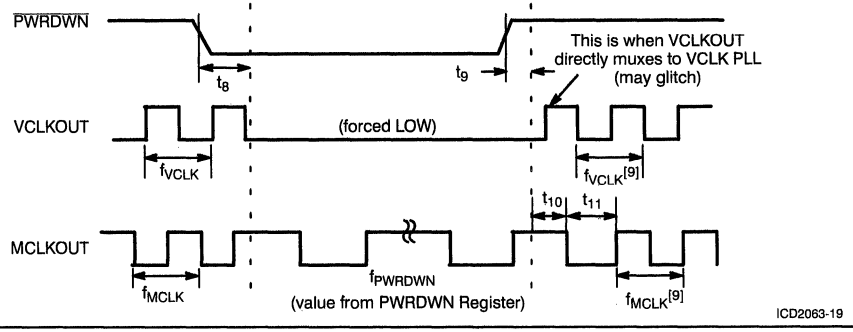
Selection Timing (MUXREF Mode)



VCLK and MCLK Selection Timing (Concurrent Change)



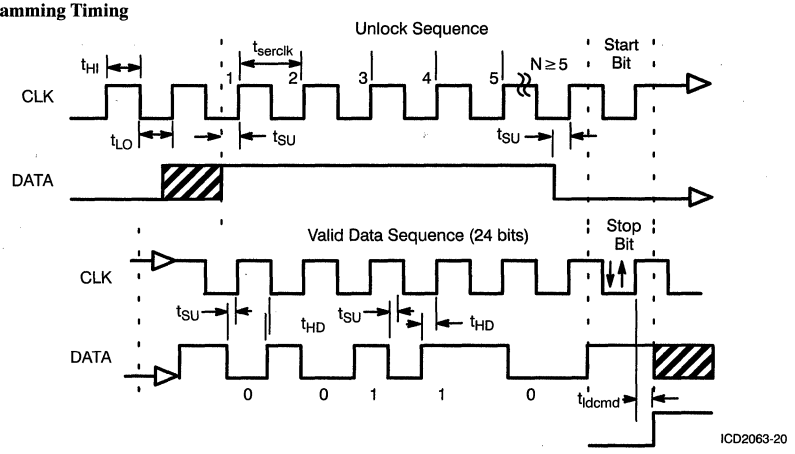
Soft Power-Down Timing (Mode 2)



Note:
9. It takes 5 msec after Soft Power-Down to guarantee lock of VCLKOUT and MCLKOUT PLLs.

Switching Waveforms (continued)

Serial Programming Timing



Configuration Options

Option	Choices	−1	−2	−3
Pin 10 Function	$\overline{\text{ERROUT}}$ or XBUF	XBUF	$\overline{\text{ERROUT}}$	$\overline{\text{ERROUT}}$
Pin 14 Function	$\overline{\text{RESET}}$ or SELM	SELM	$\overline{\text{RESET}}$	SELM
Frequency Transition	Smooth or MUXREF	Smooth	MUXREF	Smooth

Ordering Information[10]

Ordering Code	Package Name	Package Type	Operating Range	Chip Options
ICD2063	S1	16-Pin SOIC	Commercial[11]	−1, −2, −3

Notes:
10. Please call your local Cypress representative.
11. 0°C to +70°C

Example: order ICD2063SC−1 for the ICD2063, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in *Table 3.*

Document #: 38−00405

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"Super Buffer" Clock Generator

Features

- **Selectable CPU clock provides eight 2X or 1X outputs which handle all 486 processor clocking requirements**
- **Less than 250 ps total skew between Hi-Drive (48 mA) , Hi-Load (50 pF) CPU clock outputs**
- **Four fixed outputs: 14.31818 MHz (2), 16 MHz, and 24 or 32 MHz handle all other system clocking requirements**
- **CPU clock frequency range: 10 MHz to 100 MHz with 50% duty cycle**
- **Optional power-down mode**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Sophisticated internal loop-filter requires no external components**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 24-pin SOIC package configuration**

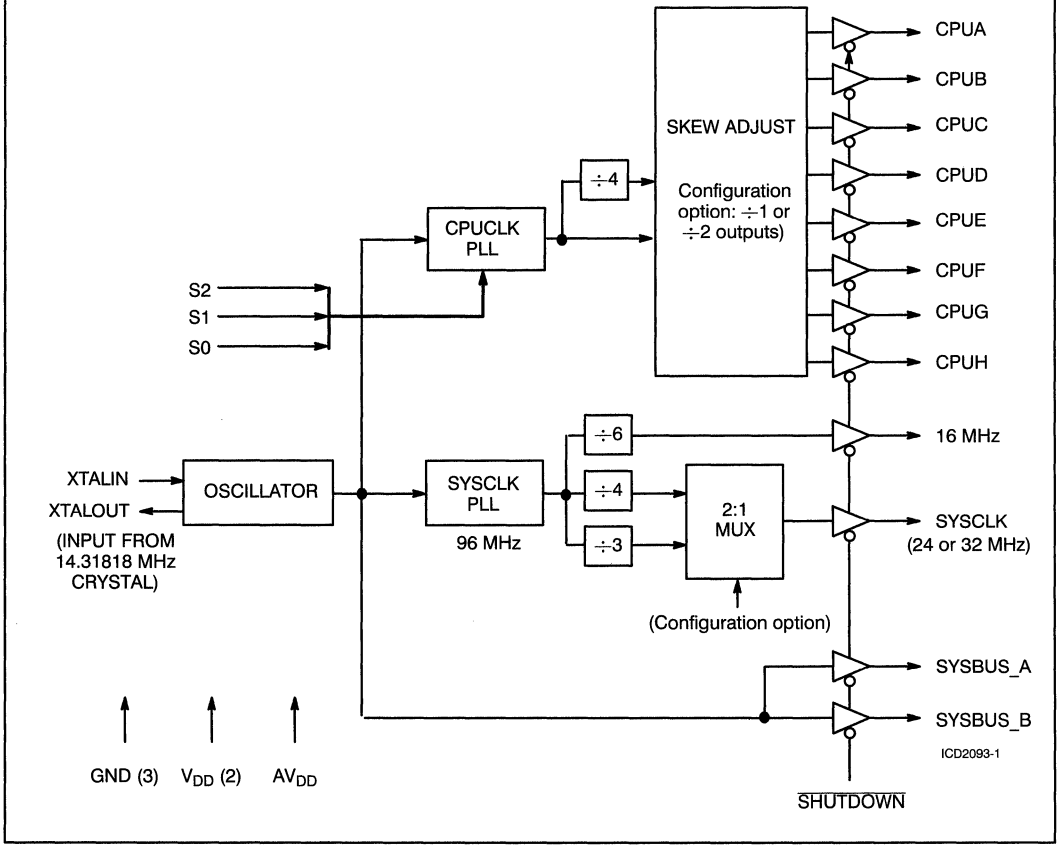
Functional Description

Today's high-end personal computers require a CPU system clock which exhibits a large drive capability (high fanout) without degradation in rise and fall times. The classical solution has been to distribute and buffer this clock. The ICD2093 alleviates this problem by providing eight 1X or 2X Clock outputs with extremely low skew between outputs.

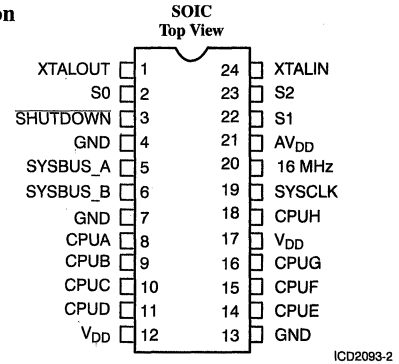
The ICD2093 also supplies other clocks required in a high-performance system: the system I/O and bus clocks.

The ICD2093 consists of one crystal controlled oscillator, two phase-locked loops, and twelve different outputs in a single package.

Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
XTALOUT[1]	1	Oscillator output to a 14.318 MHz parallel-resonant crystal
S0	2	CPU Clock ROM Select Line—Bit 0 (LSB)
$\overline{\text{SHUTDOWN}}$ (OE)	3	When pulled LOW, shuts down oscillator, PLL, and all dynamic logic. Can be made three-state Output Enable via configuration option. Internal pull-up allows for no-connect if shutdown operation is not needed.
GND	4	Ground
SYSBUS_A	5	14.31818 MHz Output
SYSBUS_B	6	14.31818 MHz Output
GND	7	Ground
CPUA	8	CPU Clock Output A (1X or 2X)[2]
CPUB	9	CPU Clock Output B (1X or 2X)[2]
CPUC	10	CPU Clock Output C (1X or 2X)[2]
CPUD	11	CPU Clock Output D (1X or 2X)[2]
V_{DD}	12	+5V to I/O Ring
GND	13	Ground
CPUE	14	CPU Clock Output E (1X or 2X)[2]
CPUF	15	CPU Clock Output F (1X or 2X)[2]
CPUG	16	CPU Clock Output G (1X or 2X)[2]
V_{DD}	17	+5V to I/O Ring
CPUH	18	CPU Clock Output H (1X or 2X)[2]
SYSCLK	19	24 MHz or 32 MHz Output (factory configurable)
16 MHz	20	16 MHz Output
AV_{DD}	21	+5V to Analog Core
S1	22	CPU Clock ROM Select Line—Bit 1
S2	23	CPU Clock ROM Select Line—Bit 2 (MSB)
XTALIN[1]	24	Oscillator input from a 14.31818 MHz crystal

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.
2. All the CPU outputs can be 1X, 2X, or any mix of the two (the outputs of each type are contiguous).

Clock Operation

CPUCLK PLL

The output frequency of the CPU clock PLL (CPUCLK) is selected by the Clock Selection Inputs S0–S2. This lets the ICD2093 support different microprocessor speed configurations.

The selection lines can be changed at any time to select a new frequency. When this occurs, the internal phase-locked loop immediately seeks the new frequency in the 33.333-MHz to 80-MHz range.

Table 1. CPUCLK ROM Selection Outputs

S2	S1	S0	Desired Freq. (MHz)	Actual CPUCLK (MHz)	Actual CPU/2 (MHz)	VCO Freq. (MHz)	Error (PPM)
0	0	0	20.000	20.003	10.002	80.013	167
0	0	1	33.333	33.322	16.661	66.645	331
0	1	0	60.000	60.000	30.000	120.000	0
0	1	1	40.000	40.006	20.003	80.013	167
1	0	0	50.000	50.114	25.057	100.227	2267
1	0	1	66.667	66.818	33.409	133.636	2270
1	1	0	80.000	80.013	40.006	160.026	167
1	1	1	100.000	100.227	50.114	100.227	2267

Fixed Frequency Oscillator Operation

Table 2 lists the available fixed frequency outputs.

Table 2. CPUCLK ROM Selection Outputs

Desired Frequency (MHz)	Actual Frequency (MHz)		Error (PPM)	
	Option –1	Option –2	Option –1	Option –2
24.000	23.993	23.967	1359	307
32.000	31.990	31.957	1359	307

Design Considerations

Skew Issues

The ICD2093 offers eight CPUCLK ÷1 or ÷2 outputs, CPUA–CPUH. These outputs have been optimized to minimize skew between any two CPUA–CPUH outputs.

The standard drive on all CPU outputs is 48 mA, with a 3-ns rise and fall time when driving 50 pF.

To minimize skew, output loads should be balanced and the printed circuit board trace lengths should be equal. The high-performance output driver of the ICD2093 requires the engineer to observe proper transmission line techniques, including termination, when designing for the ICD2093. (See the *Termination* section for suggestions on proper termination.)

Table 3 estimates the incremental skew (in addition to worst-case specification) caused by unbalanced loading. The table includes data for driving both TTL loads and CMOS threshold loads. There are two normalized measurements given: all loads normalized to 0 pF, and all loads at 30 pF (the latter being a more realistic operating assumption).

Table 3. CPUCLK ROM Selection Outputs

Load	Threshold Volts	Rising Edge (ns)		Falling Edge (ns)	
		Normalized at 0 pF	Normalized at 30 pF	Normalized at 0 pF	Normalized at 30 pF
50 pF	2.5	1.10	0.38	1.03	0.33
	1.4	0.72	0.22	1.31	0.44
40 pF	2.5	0.92	0.20	0.88	0.18
	1.4	0.62	0.12	1.09	0.22
30 pF	2.5	0.72	0.00	0.70	0.00
	1.4	0.50	0.00	0.87	0.00
20 pF	2.5	0.52	–0.20	0.50	–0.20
	1.4	0.35	–0.15	0.62	–0.25
10 pF	2.5	0.30	–0.42	0.28	–0.42
	1.4	0.20	–0.30	0.32	–0.55
0 pF	2.5	0.00	–0.72	0.00	–0.70
	1.4	0.00	–0.50	0.00	–0.87

Termination

The ICD2093 provides fast rise and fall times on its outputs to drive large loads, which require the PCB designer to observe proper transmission line techniques. There are three principal techniques for proper termination. The optimum choice depends on individual requirements.

Series Termination

The main drawback of this technique is that C_L adversely affects rise and fall times (see *Figure 1*).

Parallel Termination

The main drawback of this technique is that it consumes power.

$V_T = V_{DD} \div 2$ for minimum power. (Note that V_T should not equal receiver threshold. TTL systems often set V_T at 3V using Thévenin equivalent circuit.) See example divider in *Figure 2*.

AC Termination

The main drawback of this technique is that it is not as good at high frequencies (see *Figure 3*).

Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the

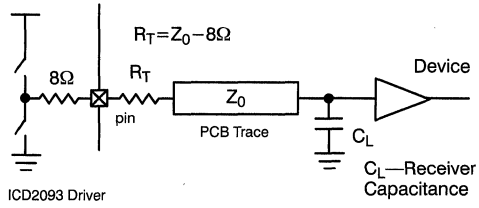
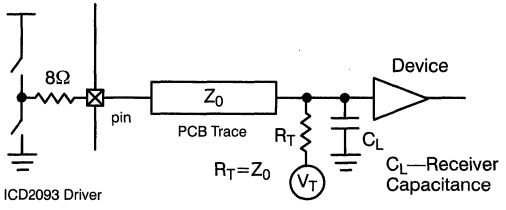


Figure 1. Series Termination



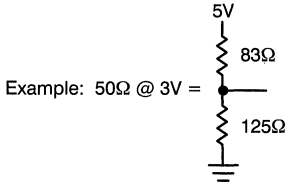


Figure 2. Parallel Termination

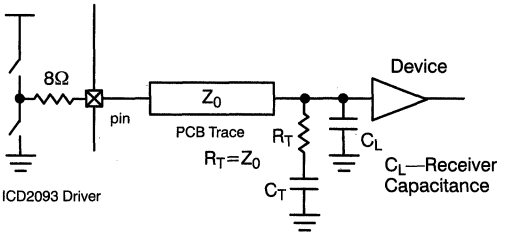


Figure 3. AC Termination

equation I = C • V • f, where I=current, C=load capacitance, V=output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and f=output frequency in MHz.

To calculate total operating current, sum the following:

$I_{SYSBUS\_A} \Rightarrow C_{14} \bullet V \bullet 14.318$
$I_{SYSBUS\_B} \Rightarrow C_{24} \bullet V \bullet 14.318$
$I_{CPUA} \Rightarrow C_{CLKA} \bullet V \bullet f_{CLKA}$
$I_{CPUB} \Rightarrow C_{CLKB} \bullet V \bullet f_{CLKB}$
$I_{CPUC} \Rightarrow C_{CLKC} \bullet V \bullet f_{CLKC}$
$I_{CPUD} \Rightarrow C_{CLKD} \bullet V \bullet f_{CLKD}$
$I_{CPUE} \Rightarrow C_{CLKE} \bullet V \bullet f_{CLKE}$
$I_{CPUF} \Rightarrow C_{CLKF} \bullet V \bullet f_{CLKF}$
$I_{CPUG} \Rightarrow C_{CLKG} \bullet V \bullet f_{CLKG}$
$I_{CPUH} \Rightarrow C_{CLKH} \bullet V \bullet f_{CLKH}$
$I_{(Internal)} \Rightarrow .06$ A (60 mA)

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5–10 pF loading, depending on the package type.

Some typical values are displayed in *Table 5*.

Table 4. Operating Current Typical Values

Frequency	Capacitive Load	Current (in mA)
66.6 MHz	30 pF	115

General Considerations

Power-Down Operation

In the power-down state, the oscillator, PLL, and all dynamic logic is shut down.

Note that, during shutdown, the internal PLLs are turned off. Upon restarting, there will be a 5-msec interval during which the VCOs stabilize. See *Power-Down Timing* in the *Switching Waveforms* section for further timing information.

Three-State Output Operation

If the OE configuration is chosen, then the $\overline{\text{SHUTDOWN}}$ pin becomes an OE pin, which, when pulled LOW, will three-state all the clock output lines. This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required. The output pads contain weak pull-down resistors.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 140°C
Package power dissipation ..... 1000 mW

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −48 mA[3]	V_{DD}−0.5		V
V_{OL}	Output LOW Voltage	I_{OL} = 48 mA[3]		0.5	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)	−10	150	µA
I_{DDA}	Power Supply to Core	1 CPU @ 66 MHz 7 CPU @ 33 MHz Inputs @ V_{DD} or GND		18	mA
I_{DD}	Power Supply Current			130	mA
C_L	Total Cap. Load/CPU Output			50[3, 4]	pF

Notes:
3. Option −2 has half the output drive capability: I_{OH}=−24 mA, I_{OL}=24 mA, C_L=25 pF.
4. Maximum load on all CPU outputs can exceed the maximum specifications.

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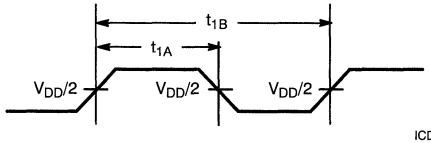
Switching Characteristics[5]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference input normal value		14.318		MHz
$t_{(REF)}$	Reference Clock Period	$1 \div f_{(REF)}$		69.84		ns
t_1	Input Duty Cycle	Duty cycle for the input oscillator defined as $t_1 = t_{1A} \div t_{1B}$	25%	50%	75%	
t_2	Output Period		10 100 MHz		100 10 MHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs, measured @ CMOS V_{TH} of $V_{DD} \div 2$ (special screening required for 100 MHz) $t_3 = t_{1A} \div t_{1B}$	40%		60%	
t_4	Rise Times	Rise time of clock outputs (50-pF load @ 10 MHz)			3.5	ns
t_5	Fall Times	Fall time of clock outputs (50-pF load @ 10 MHz)			4	ns
t_6	Skew	Leading edge skew between 1X and 2X outputs and C_L=50 pF			500	ps
t_8	Skew	Leading edge skew between 1X and 1X or 2X and 2X outputs and C_L=50 pF			250	ps
t_{VCO}	VCO Settle Time	Time for VCO to transition smoothly and monotonically from the original to the new frequency			3	msec
t_{10}	Three-state Time	Time for the outputs to go into three-state mode after OE signal goes LOW			20	ns
t_{11}	Clock Enable Time	Time for the outputs to recover from three-state mode after OE signal goes HIGH			20	ns
t_{12}	SYSBUS Skew	Leading edge skew between SYSBUS outputs			500	ps
t_{13}	SYSBUS Skew	Trailing edge skew between SYSBUS outputs			500	ps
t_{14}	Power-Down	Time to invoke power-down option			20	ns
t_{15}	Power-Up	Time to revoke power-down option			20	ns

Note:
5. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

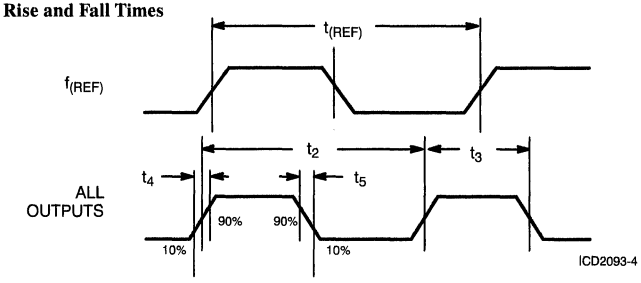
Duty Cycle Timing



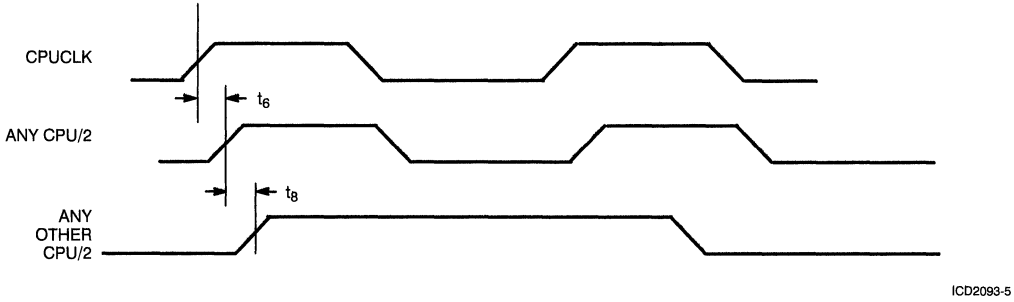
ICD2093-3

Switching Waveforms (continued)

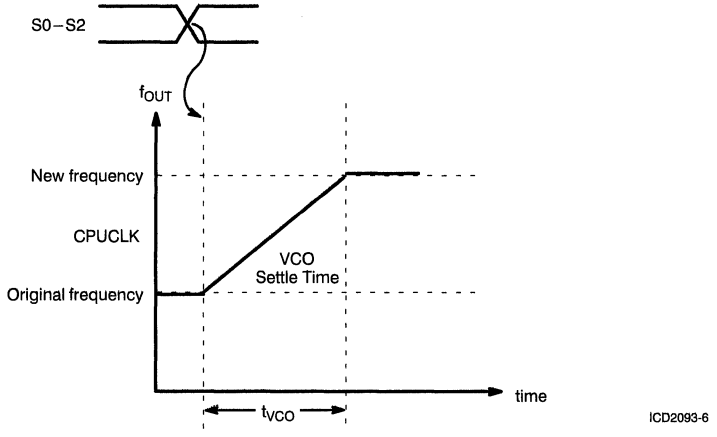
Rise and Fall Times



CPUCLK Skew



Selection Timing

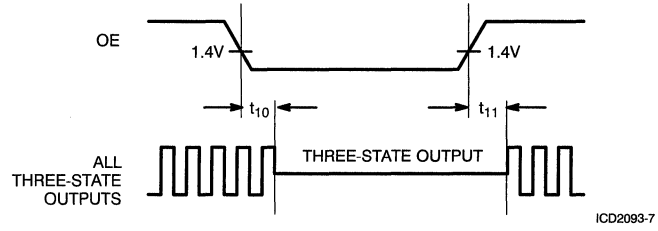


(Valid for all transitions except CPUCLK = 10 MHz ⇒ 100 MHz)

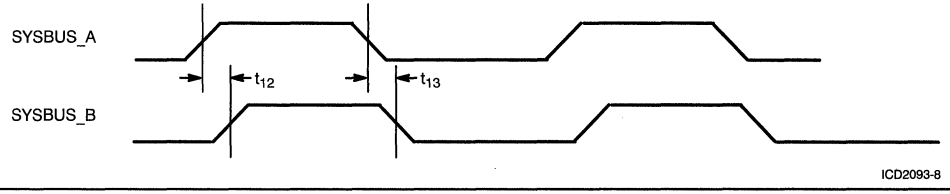
10

Switching Waveforms (continued)

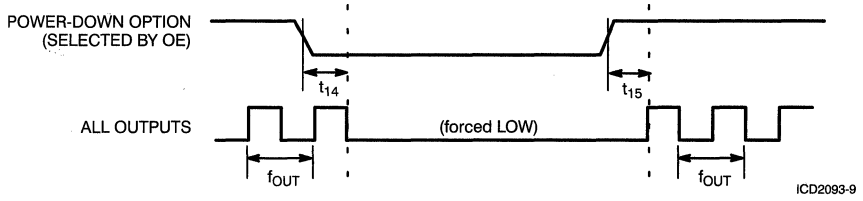
Three-State Timing



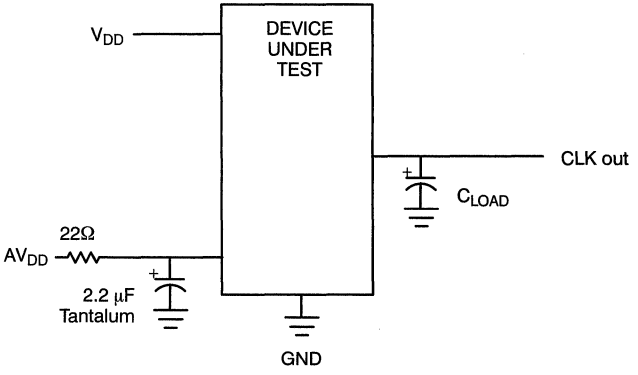
SYSBUS Skew



Power-Down Timing

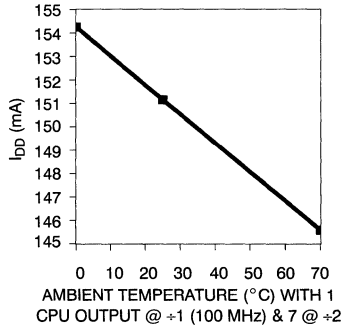


Test Circuit

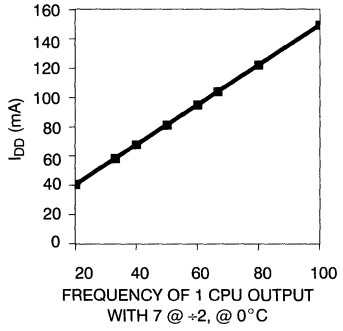


Typical AC and DC Characteristics

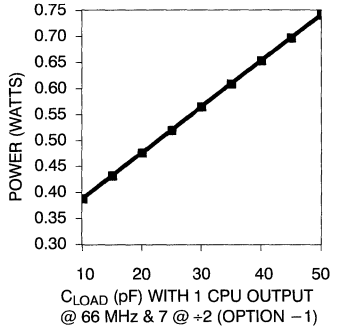
I TOTAL



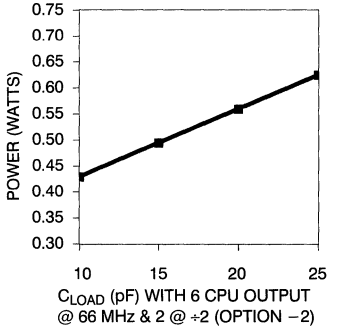
I TOTAL



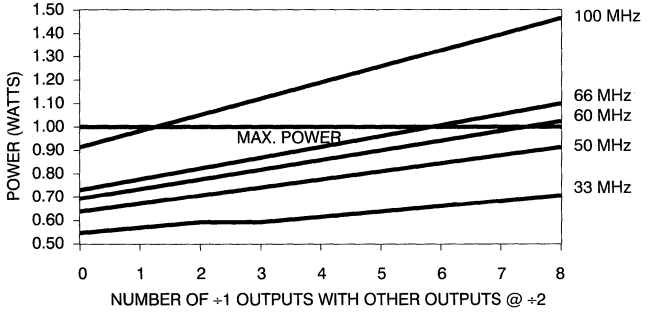
CALCULATED POWER DISSIPATION



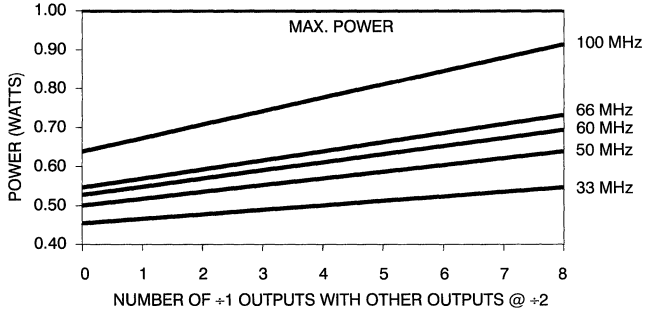
CALCULATED POWER DISSIPATION



WORST-CASE POWER, V_{DD}=5.25V, C_{LOAD}=50 pF (SIMILAR TO −1 OPTION)



WORST-CASE POWER, V_{DD}=5.25V, C_{LOAD}=25 pF (SIMILAR TO −2 OPTION)



Configuration Options

Signal/Pin	Option −1	Option −2
CPUA	÷2	÷2
CPUB	÷2	÷2
CPUC	÷2	÷1
CPUD	÷2	÷1
CPUE	÷2	÷1
CPUF	÷2	÷1
CPUG	÷2	÷1
CPUH	÷1	÷1
Pin 3	OE	$\overline{\text{SHUTDOWN}}$
SYSCLK	24 MHz	24 MHz

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Clock Output Options
ICD2093	S13	24-Pin SOIC	C=0°C to +70°C @ V_{DD}=5V	Standard Configuration −1

Example: Order ICD2093SC−1 for the ICD2093, 24-pin plastic SOIC, commercial temperature range device which uses the standard configuration code −1 (SYSCLK=24 MHz, Power-Down not enabled, one ÷1 CPU clock and seven ÷2 CPU clocks).

Custom configurations are also available. To order a custom configuration, please contact your Cypress representative.

Document #: 38−00401

ICD6233

One-Time-Programmable Clock Oscillator

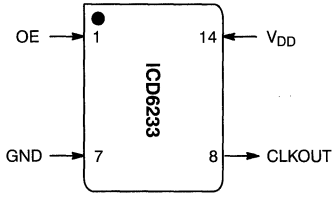
Features

- **Industry standard 14-pin package footprint**
- **Frequency can be programmed one time to values in a wide frequency range (937 kHz to 90 MHz)**
- **Programmable option allows output to meet both CMOS and TTL duty cycle requirements**
- **Example applications:**
  - **— Replace custom-frequency metal can oscillators to reduce time to market**
  - **— Allows prototyping with custom frequencies**
  - **— Reduces inventory needs**
- **Output can be three-stated**
- **Output enabled if pin 1 left floating**
- **Grounded metal cover reduces EMI**
- **Internal bypass capacitors—no external components required**
- **Sophisticated PLL technology with Internal Loop-Filter**
- **5V operation in CMOS technology**

Functional Description

The ICD6233 is a pin-for-pin-compatible metal can oscillator that allows the user to customize the output frequency. The ICD6233 may be programmed one time for an output in the range of 937 KHz to 90 MHz. At manufacturing time, the desired output frequency is programmed using a popular third-party programer like Data I/O Unisite or SMS.

Pin Configurations



ICD6233-1

Pin Names

Name	Number	Description
OE	1	Three-State Output Enable; internal pull-up allows no-connect
GND	7	Ground
CLKOUT	8	Programmable Clock Output
V_{DD}	14	+5 Volts

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −55°C to +125°C
Max soldering temperature (10 sec) ..... 260°C
Junction Temperature ..... +125°C

Operating Range

Ambient Temperature	V_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 10%
C_L 25 pF max.	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DD}	Supply Current	V_{DD} = Max., Output <90 MHz CE = V_{DD}		55.0	mA
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5V		100.0	µA
I_{IL}	Input LOW Current	V_{IL} = +0.5V		−250.0	µA

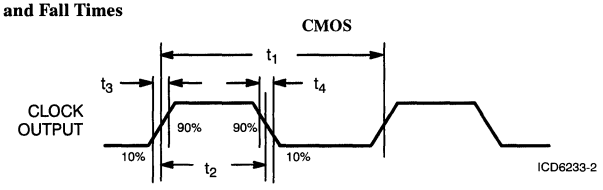
Switching Characteristics Over the Operating Range[1]

Parameter	Description	Test Conditions	Min.	Max.	Unit
t_1	Output Period	5V Operation	11.1 90 MHz	1066.7 937.5 kHz	ns
	Output Duty Cycle	Duty cycle for output pads, define as $t_1 \div t_2$	40	60	%
t_3	Rise Time	Clock output rise time		4	ns
t_4	Fall Time	Clock output fall time		4	ns
t_5	Power-Up	Time for output to become valid		15	msec
t_6	Three-State	Time for output oscillator to enter three-state mode after OE goes LOW		12	ns
t_7	CLK Valid	Time for output oscillator to enter three-state mode after OE goes HIGH		12	ns

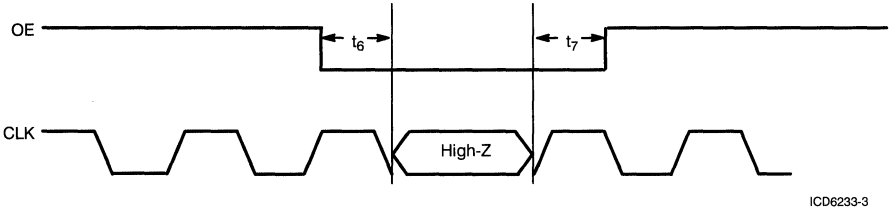
Note:
1. Input capacitance is typically 10pF.

Switching Waveforms

Rise and Fall Times



OE Timing



Ordering Information[2]

Ordering Code	Package Name	Package Type	Operating Range
ICD6233	M	14-Pin Metal Can	Commercial[3]

Note:
2. Call Cypress's IC Designs division at (800) 669-0557 and specify frequency (937.5 KHz to 90 MHz) and output duty cycle (TTL or CMOS).
3. 0°C to +70°C

Document #: 38–00407

CY7B991
CY7B992

Programmable Skew Clock Buffer (PSCB)

Features

- **Output pair skew <100 ps typical (250 max.)**
- **All outputs skew <250 ps typical (500 max.)**
- **3.75- to 80-MHz output operation**
- **User-selectable output functions**
  - **— Selectable skew to 18 ns**
  - **— Inverted and non-inverted**
  - **— Operation at ½ and ¼ input frequency**
  - **— Operation at 2x and 4x input frequency (input as low as 3.75 MHz)**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **32-pin PLCC/LCC package**
- **Jitter < 200 ps peak-to-peak (< 25 ps RMS)**
- **Compatible with a Pentium™-based processor**

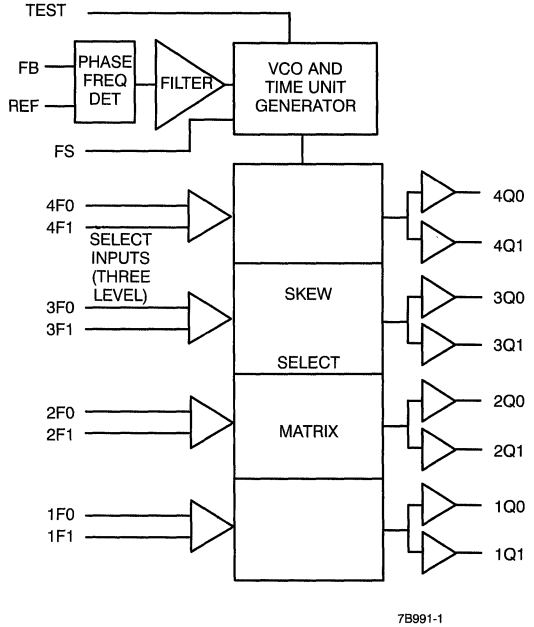
Functional Description

The CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB) offer user-selectable control over system clock functions. These multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B991 TTL or CY7B992 CMOS).

Each output can be hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency with outputs able to skew up to ±6 time units from their nominal "zero" skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. When this "zero delay" capability of the PSCB is combined with the selectable output skew functions, the user can create output-to-output delays of up to ±12 time units.

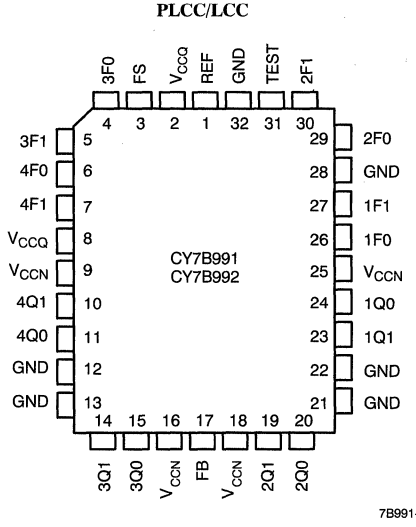
Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

Logic Block Diagram



7B991-1

Pin Configuration



7B991-2

Pentium is a trademark of Intel Corporation.

Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three-level frequency range select. See *Table 1.*
1F0, 1F1	I	Three-level function select inputs for output pair 1 (1Q0, 1Q1). See *Table 2.*
2F0, 2F1	I	Three-level function select inputs for output pair 2 (2Q0, 2Q1). See *Table 2.*
3F0, 3F1	I	Three-level function select inputs for output pair 3 (3Q0, 3Q1). See *Table 2.*
4F0, 4F1	I	Three-level function select inputs for output pair 4 (4Q0, 4Q1). See *Table 2.*
TEST	I	Three-level select. See test mode section under the block diagram descriptions.
1Q0, 1Q1	O	Output pair 1. See *Table 2.*
2Q0, 2Q1	O	Output pair 2. See *Table 2.*
3Q0, 3Q1	O	Output pair 3. See *Table 2.*
4Q0, 4Q1	O	Output pair 4. See *Table 2.*
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in *Table 1.*

Table 1. Frequency Range Select and t_U Calculation[1]

FS[2, 3]	f_{NOM} (MHz) Min.	f_{NOM} (MHz) Max.	$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. *Table 2* below shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 2. Programmable Skew Configurations[1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Note:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see *Table 2*). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} has reached 4.3V.

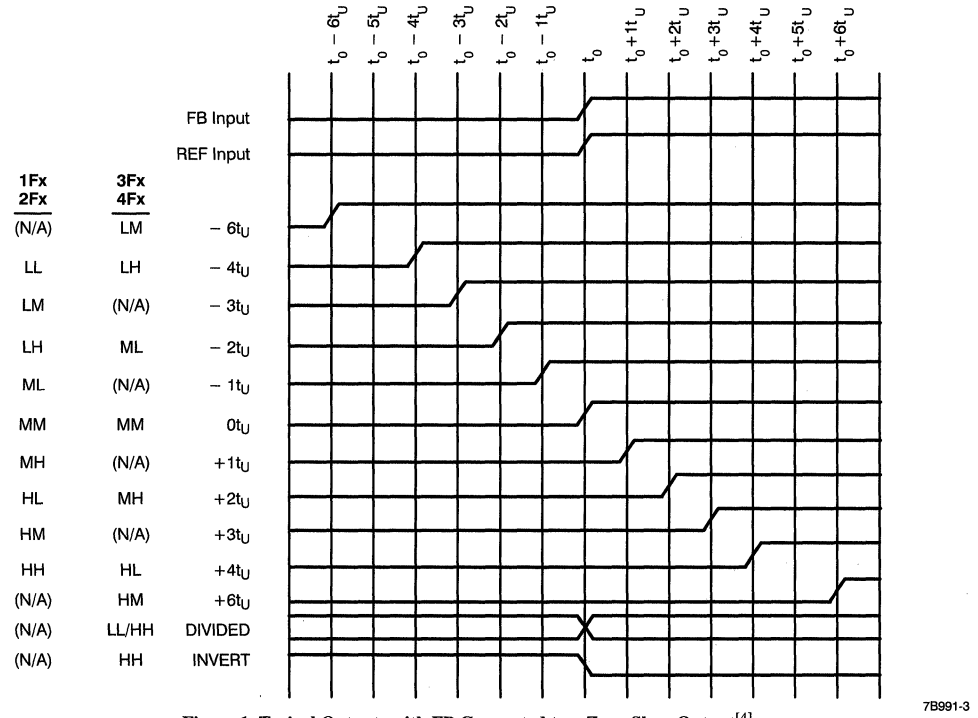


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output[4]

Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B991/CY7B992 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

4 FB connected to an output selected for "zero" skew (i.e., xF1 = xF0 = MID).

5. Indicates case temperature.

Electrical Characteristics Over the Operating Range[6]

Parameter	Description	Test Conditions	CY7B991 Min.	CY7B991 Max.	CY7B992 Min.	CY7B992 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 16 mA	2.4				V
		V_{CC} = Min., I_{OH} = − 40 mA			V_{CC} − 0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} = 46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} − 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		− 0.5	0.8	− 0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS, xFn)[7]	Min. ≤ V_{CC} ≤ Max.	V_{CC} − 1V	V_{CC}	V_{CC} − 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS, xFn)[7]	Min. ≤ V_{CC} ≤ Max.	$V_{CC}/2$ − 500 mV	$V_{CC}/2$ + 500 mV	$V_{CC}/2$ − 500 mV	$V_{CC}/2$ + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS, xFn)[7]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	− 500		− 500		µA
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = $V_{CC}/2$	− 50	50	− 50	50	µA
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		− 200		− 200	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC} = Max., V_{OUT} = GND (25°C only)		− 250		N/A	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open — Com'l		85		85	mA
		Mil/Ind		90		90	
I_{CCN}	Output Buffer Current per Output Pair[9]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}		14		19	mA
PD	Power Dissipation per Output Pair[10]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}		78		104[11]	mW

Capacitance[12]

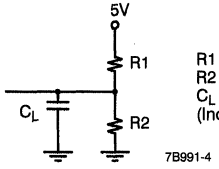
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

6. See the last page of this specification for Group A subgroup testing information.
7. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
8. CY7B991 should be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B992 outputs should not be shorted to GND. Doing so may cause permanent damage.
9. Total output current per output pair can be approximated by the following expression that includes device current plus load current:
   CY7B991:
   I_{CCN} = [(4 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N] x 1.1
   CY7B992:
   I_{CCN} = [(3.5+ .17F) + [((1160 − 2.8F)/Z) + (.0025FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F * C
10. Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
    CY7B991:
    PD = [(22 + 0.61F) + [((1550 − 2.7F)/Z) + (.0125FC)]N] x 1.1
    CY7B992:
    PD = [(19.25+ 0.94F) + [((700 + 6F)/Z) + (.017FC)]N] x 1.1
    See note NO TAG for variable definition.
11. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
12. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

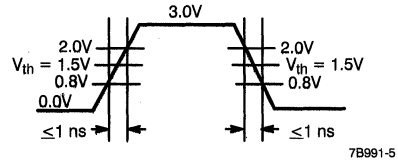
10

AC Test Loads and Waveforms

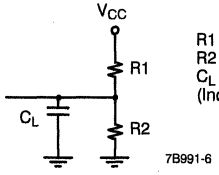


R1 = 130
R2 = 91
C_L = 50 pF (C_L = 30pF for −5 devices)
(Includes fixture and probe capacitance)

TTL AC Test Load (CY7B991)

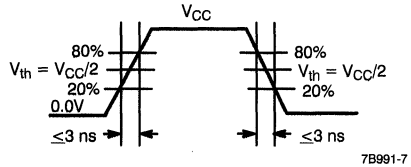


TTL Input Test Waveform (CY7B991)



R1 = 100
R2 = 100
C_L = 50 pF (C_L = 30pF for −5 devices)
(Includes fixture and probe capacitance)

CMOS AC Test Load (CY7B992)



CMOS Input Test Waveform (CY7B992)

Switching Characteristics Over the Operating Range[2, 13]

Parameter	Description		CY7B991−5 Min.	CY7B991−5 Typ.	CY7B991−5 Max.	CY7B992−5 Min.	CY7B992−5 Typ.	CY7B992−5 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2, 3]	40		80	40		80[14]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[15, 16]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[15, 17]			0.25	0.5		0.25	0.5	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[15, 18]			0.6	0.7		0.6	0.7	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[15, 18]			0.5	1.0		0.6	1.2	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[15, 18]			0.5	0.7		0.5	0.7	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[15, 18]			0.5	1.0		0.6	1.3	ns
t_{SKEW5}	Device-to-Device Skew[19, 25]				0.2			0.2	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.5	0.0	+0.5	− 0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[20]		− 1.0	0.0	+1.0	− 1.0	0.0	+1.0	ns
t_{PWH}	Output HIGH Time Deviation from 50%[21, 22]				2.5			3.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[21, 22]				3			3.5	ns
t_{ORISE}	Output Rise Time[21, 23]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{OFALL}	Output Fall Time[21, 23]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{LOCK}	PLL Lock Time[24]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[25]			25			25	ps
		Peak-to-Peak[25]			200			200	ps

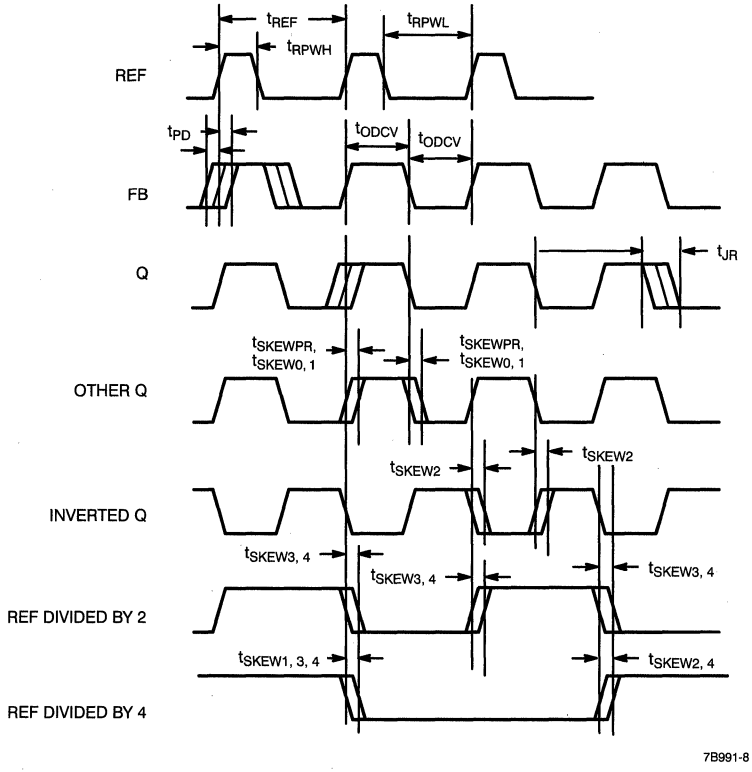
Switching Characteristics Over the Operating Range[2, 13] (continued)

Parameter	Description		CY7B991–7 Min.	CY7B991–7 Typ.	CY7B991–7 Max.	CY7B992–7 Min.	CY7B992–7 Typ.	CY7B992–7 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2]	40		80	40		50	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[15, 16]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[15, 17]			0.3	0.75		0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[15, 18]			0.6	1.0		0.6	1.0	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[15, 18]			1.0	1.5		1.0	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[15, 18]			0.7	1.2		0.7	1.2	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[15, 18]			1.2	1.7		1.2	1.7	ns
t_{SKEW5}	Device-to-Device Skew[19, 25]				0.2			0.2	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.7	0.0	+0.7	− 0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[20]		− 1.2	0.0	+1.2	− 1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50%[21, 22]				3			5.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[21, 22]				3.5			5.5	ns
t_{ORISE}	Output Rise Time[21, 23]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[21, 23]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[24]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[25]			25			25	ps
		Peak-to-Peak[25]			200			200	ps

Notes:

13. Test measurement levels for the CY7B991 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B992 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
14. Except as noted, all CY7B992−5 timing parameters are specified to 80-MHz with a 30-pF load.
15. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
16. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
17. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
18. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
19. t_{SKEW5} is the output-to-output skew between the outputs used as the FB input of two or more devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.). The maximum variation between two pins on different parts is t_{SKEW5} plus the skews associated with each part.
20. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
21. Specified with outputs loaded with 30 pF for the CY7B99X−5 devices and 50 pF for the CY7B99X−7 devices. Devices are terminated through 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
22. t_{PWH} is measured at 2.0V for the CY7B991 and 0.8 V_{CC} for the CY7B992. t_{PWL} is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
23. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or 0.8V_{CC} and 0.2V_{CC} for the CY7B992.
24. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
25. Tested initially and after any design or process changes that may affect these parameters.

AC Timing Diagrams



Operational Mode Descriptions

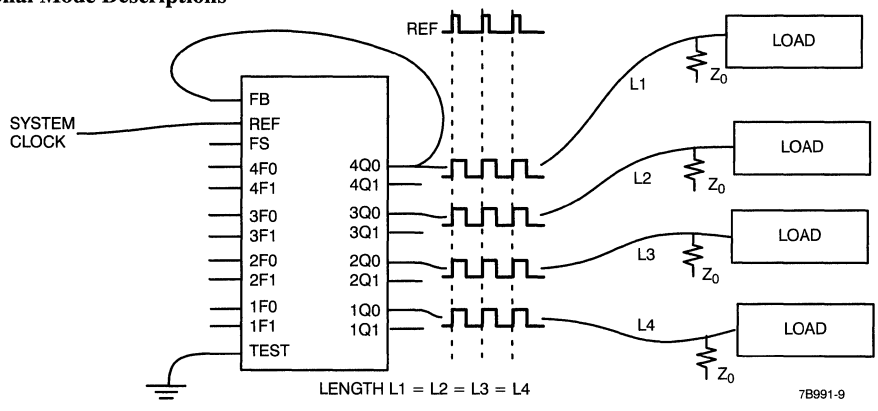


Figure 2. Zero-Skew and/or Zero-Delay Clock Driver

Figure 2 shows the PSCB configured as a zero-skew clock buffer. In this mode the 7B991/992 can be used as the basis for a low-skew clock distribution tree. When all of the function select inputs (xF0, xF1) are left open, the outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

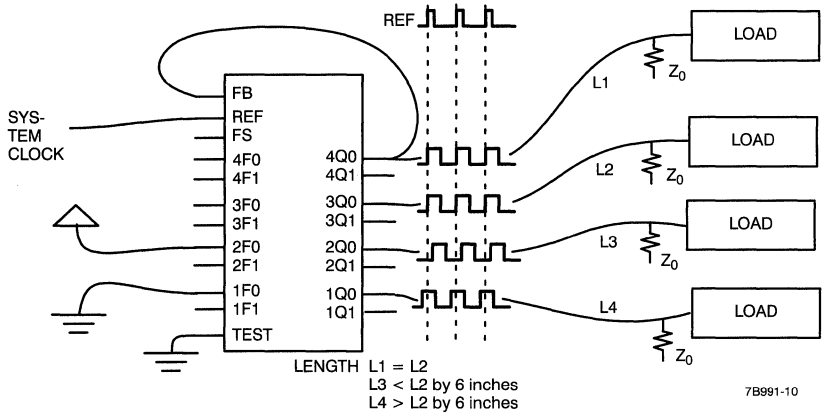


Figure 3. Programmable-Skew Clock Driver

Figure 3 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the PSCB can be programmed to stagger the timing of its outputs. The four groups of output pairs can each be programmed to different output timing. Skew timing can be adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is fed back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads can receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0-ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to insure that all outputs have precise phase alignment.

Clock skews can be advanced by ±6 time units (t_U) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since "Zero Skew", $+t_U$, and $-t_U$ are defined relative to output groups, and since the PLL aligns the rising edges of REF and FB, it is possible to create wider output skews by proper selection of the xFn inputs. For example a $+10\ t_U$ between REF and 3Qx can be achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at $-4\ t_U$ and 3Qx skews to $+6\ t_U$, a total of $+10\ t_U$ skew is realized.) Many other configurations can be realized by skewing both the output used as the FB input and skewing the other outputs.

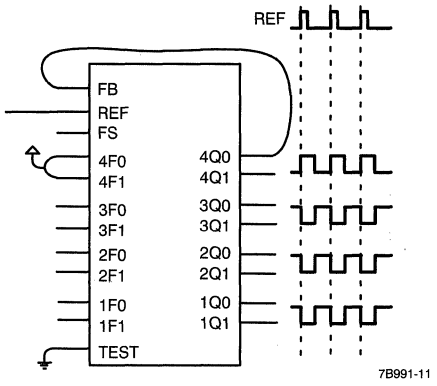


Figure 4. Inverted Output Connections

Figure 4 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the "inverted" outputs with respect to the REF input. By selecting which output is connect to FB, it is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs. The correct configuration would be determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 5 illustrates the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, which results in a 40-MHz waveform at these outputs. Note that the 20- and 40-MHz clocks fall simultaneously and are out of phase on their rising edge. This will allow the designer to use the rising edges of the ½ frequency and ¼ frequency outputs without concern for rising-edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80-MHz operation because that is the frequency of the fastest output.

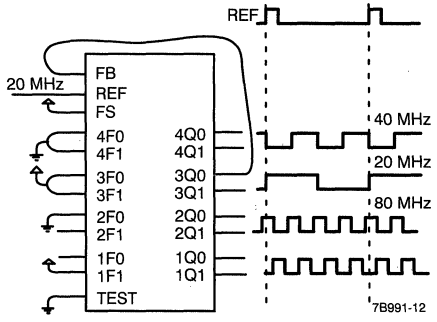


Figure 5. Frequency Multiplier with Skew Connections

Figure 6 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This allows use of the rising edges of the ½ frequency and ¼ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15- to 30-MHz range since the highest frequency output is running at 20 MHz.

Figure 7 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function allows the two subsystems to each be clocked 180 degrees out of phase, but still to be aligned within the skew spec.

The divided outputs offer a zero-delay divider for portions of the system that need the clock to be divided by either two or four, and still remain within a narrow skew of the "1X" clock. Without this feature, an external divider would need to be added, and the propagation delay of the divider would add to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the PSCB to multiply the clock rate at the REF input by either two or four. This mode will enable the designer to distribute a low-frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low-skew characteristics of the clock driver. The PSCB can perform all of the functions described above at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

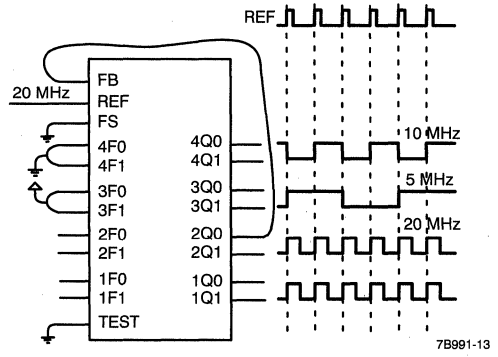


Figure 6. Frequency Divider Connections

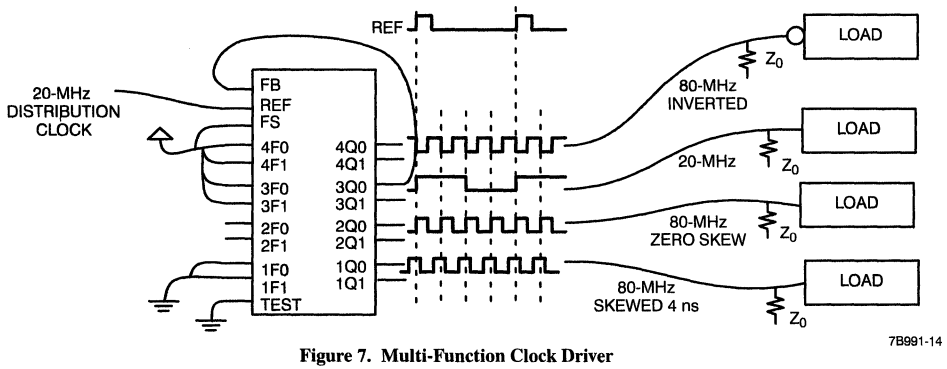


Figure 7. Multi-Function Clock Driver

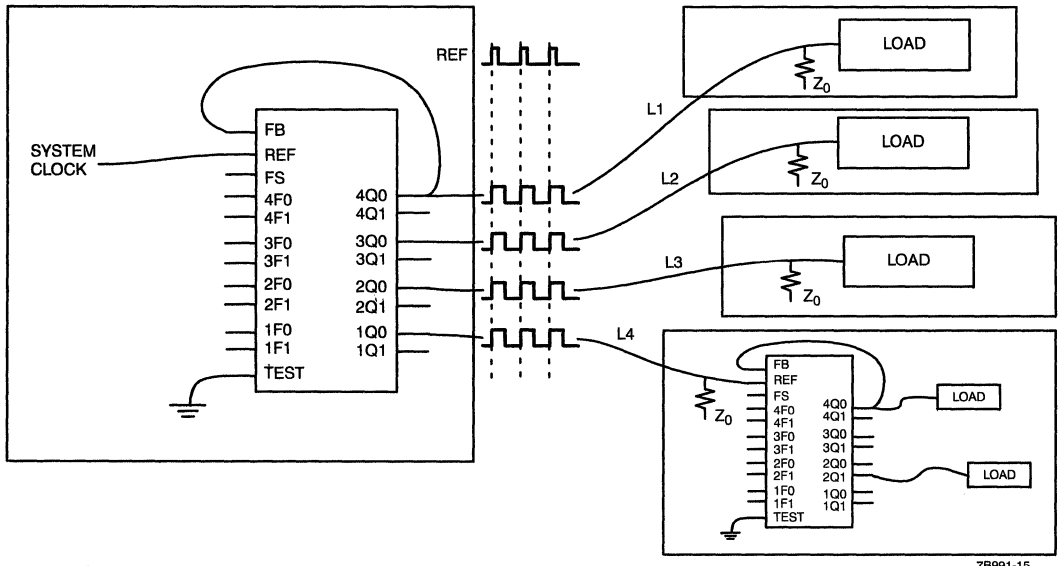


Figure 8. Board-to-Board Clock Distribution

Figure 8 shows the CY7B991/992 connected in series to construct a zero-skew clock distribution tree between boards. Delays of the downstream clock buffers can be programmed to compensate for the wire length (i.e., select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero-delay clock tree. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is recommended that not more than two clock buffers be connected in series.

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B991–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
750	CY7B991–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B991–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
500	CY7B992–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
750	CY7B992–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B992–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{IHH}	1, 2, 3
V_{IMM}	1, 2, 3
V_{ILL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{IHH}	1, 2, 3
I_{IMM}	1, 2, 3
I_{ILL}	1, 2, 3
I_{CCQ}	1, 2, 3
I_{CCN}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
t_{NOM}	9, 10, 11
t_{RPWH}	9, 10, 11
t_{RPWL}	9, 10, 11
t_{U}	9, 10, 11
t_{SKEWPR}	9, 10, 11
t_{SKEW0}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{SKEW3}	9, 10, 11
t_{SKEW4}	9, 10, 11
t_{PD}	9, 10, 11
t_{ODCV}	9, 10, 11
t_{PWH}	9, 10, 11
t_{PWL}	9, 10, 11
t_{QRISE}	9, 10, 11
t_{QFALL}	9, 10, 11
t_{LOCK}	9, 10, 11

CY7B9910
CY7B9920

Low Skew Clock Buffer

Features

- **All outputs skew <250 ps typical (500 max.)**
- **15- to 80-MHz output operation**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **24-pin SOIC package**
- **Jitter: <200 ps peak to peak, <25 ps RMS**
- **Compatible with Pentium™ -based processors**

Functional Description

The CY7B9910 and CY7B9920 Low Skew Clock Buffers offer low-skew system clock distribution. These multiple-output clock drivers optimize the timing of high-performance computer systems. Eight individual drivers can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B9910 TTL or CY7B9920 CMOS).

The completely integrated PLL allows "zero delay" capability. External divide capability, combined with the internal PLL, allows distribution of a low-frequency clock that can be multiplied by virtually any factor at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO

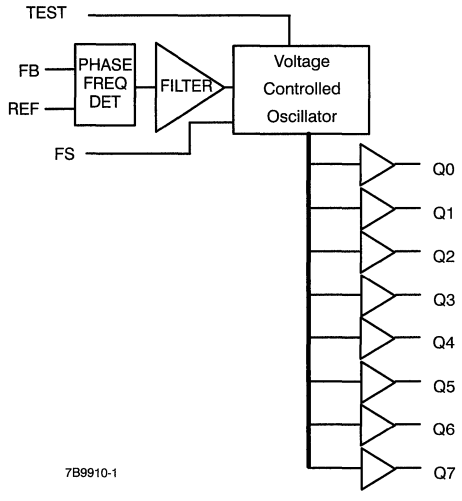
The VCO accepts analog control inputs from the PLL filter block and generates a frequency. The operational range of the VCO is determined by the FS control pin.

Test Mode

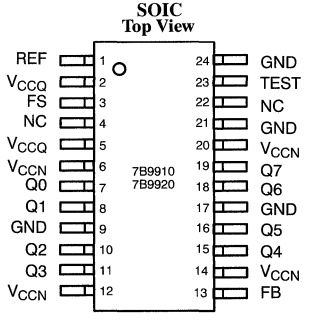
The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910/CY7B9920 to operate as explained above. (For testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase-locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

Logic Block Diagram



Pin Configuration



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Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS[1, 2, 3]	I	Three-level frequency range select. See *Table 1.*
TEST	I	Three-level select. See Test Mode section.
Q[0..7]	O	Clock outputs.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY7B9910		CY7B9920		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −16 mA	2.4				V
		V_{CC} = Min., I_{OH} = −40 mA			V_{CC}−0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} =46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} − 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		−0.5	0.8	−0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	V_{CC} − 1V	V_{CC}	V_{CC} − 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	−500		−500		µA
I_{IHH}	Input HIGH Current (Test, FS)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS)	V_{IN} = V_{CC}/2	−50	50	−50	50	µA
I_{ILL}	Input LOW Current (Test, FS)	V_{IN} = GND		−200		−200	µA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		CY7B9910 Min.	CY7B9910 Max.	CY7B9920 Min.	CY7B9920 Max.	Unit
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND (25°C only)			−250		N/A	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open	Com'l		85		85	mA
			Mil/Ind		90		90	
I_{CCN}	Output Buffer Current per Output Pair[3]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}			14		19	mA
PD	Power Dissipation per Output Pair[4]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}			78		104[5]	mW

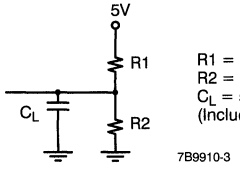
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

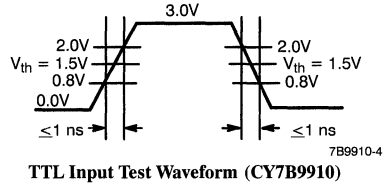
1. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B9920 outputs are not short circuit protected.
3. Total output current per output pair can be approximated by the following expression that includes device current plus load current:
   CY7B9910:
   I_{CCN} = [(4 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N] x 1.1
   CY7B9920:
   I_{CCN} = [(3.5+ .17F) + [((1160 − 2.8F)/Z) + (.0025FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F * C
4. Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   CY7B9910:
   PD = [(22 + 0.61F) + [((1550 − 2.7F)/Z) + (.0125FC)]N] x 1.1
   CY7B9920:
   PD = [(19.25+ 0.94F) + [((700 + 6F)/Z) + (.017FC)]N] x 1.1
   See note 3 for variable definition.
5. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
6. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

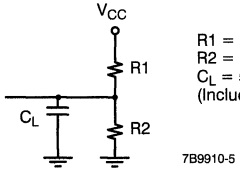


R1 = 130
R2 = 91
C_L = 50 pF (C_L = 30 pF for −5 devices)
(Includes fixture and probe capacitance)

TTL AC Test Load (CY7B9910)

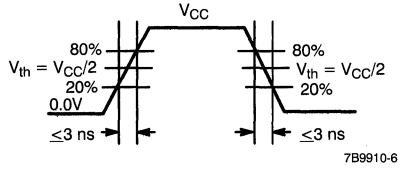


TTL Input Test Waveform (CY7B9910)



R1 = 100
R2 = 100
C_L = 50 pF (C_L = 30 pF for −5 devices)
(Includes fixture and probe capacitance)

CMOS AC Test Load (CY7B9920)



CMOS Input Test Waveform (CY7B9920)

Switching Characteristics Over the Operating Range[7]

Parameter	Description		CY7B9910–5 Min.	Typ.	Max.	CY7B9920–5 Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[8, 9]	15		30	15		30	MHz
		FS = MID[8, 9]	25		50	25		50	
		FS = HIGH[8,9,10]	40		80	40		80[11]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[12, 13]			0.25	0.5		0.25	0.5	ns
t_{DEV}	Device-to-Device Skew[14, 15]				1.0			1.0	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.5	0.0	+0.5	− 0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[16]		− 1.0	0.0	+1.0	− 1.0	0.0	+1.0	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak[15]			200			200	ps
		RMS[15]			25			25	ps

Parameter	Description		CY7B9910–7 Min.	Typ.	Max.	CY7B9920–7 Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[8, 9]	15		30	15		30	MHz
		FS = MID[8, 9]	25		50	25		50	
		FS = HIGH[8,9,10]	40		80	40		50	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[12, 13]			0.3	0.75		0.3	0.75	ns
t_{DEV}	Device-to-Device Skew[14, 15]				1.5			1.5	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.7	0.0	+0.7	− 0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[16]		− 1.2	0.0	+1.2	− 1.2	0.0	+1.2	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak[15]			200			200	ps
		RMS[15]			25			25	ps

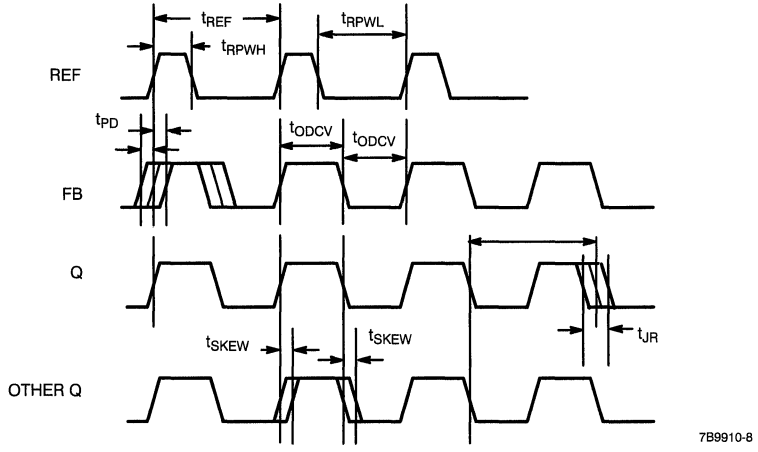
Notes:

7. Test measurement levels for the CY7B9910 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B9920 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions asume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
8. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
9. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be f_{NOM}/X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
10. When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} has reached 4.3V.
11. Except as noted, all CY7B9920–5 timing parameters are specified to 80-MHz with a 30-pF load.
12. SKEW is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
13. t_{SKEW} is defined as the skew between outputs.
14. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.).
15. Tested initially and after any design or process changes that may affect these parameters.
16. t_{ODCV} is the deviation of the output from a 50% duty cycle.
17. Specified with outputs loaded with 30 pF for the CY7B99X0–5 devices and 50 pF for the CY7B99X0–7 devices. Devices are terminated through 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
18. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B9910 or $0.8V_{CC}$ and $0.2V_{CC}$ for the CY7B9920.
19. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Table 1. Frequency Range Select

FS	f_{NOM} (MHz)	
	Min.	Max.
LOW	15	30
MID	25	50
HIGH	40	80

AC Timing Diagrams



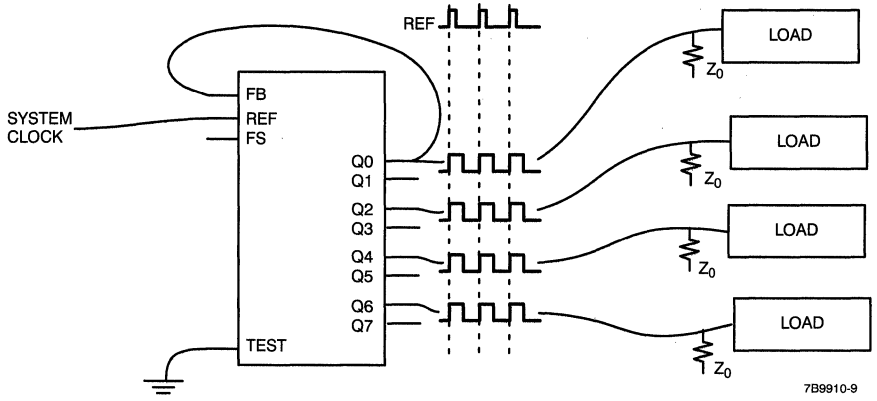


Figure 1. Zero-Skew and/or Zero-Delay Clock Driver

Operational Mode Descriptions

Figure 1 shows the device configured as a zero-skew clock buffer. In this mode the 7B9910/9920 can be used as the basis for a low-skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

Figure 2 shows the CY7B9910/9920 connected in series to construct a zero-skew clock distribution tree between boards. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is not recommended that more than two clock buffers be connected in series.

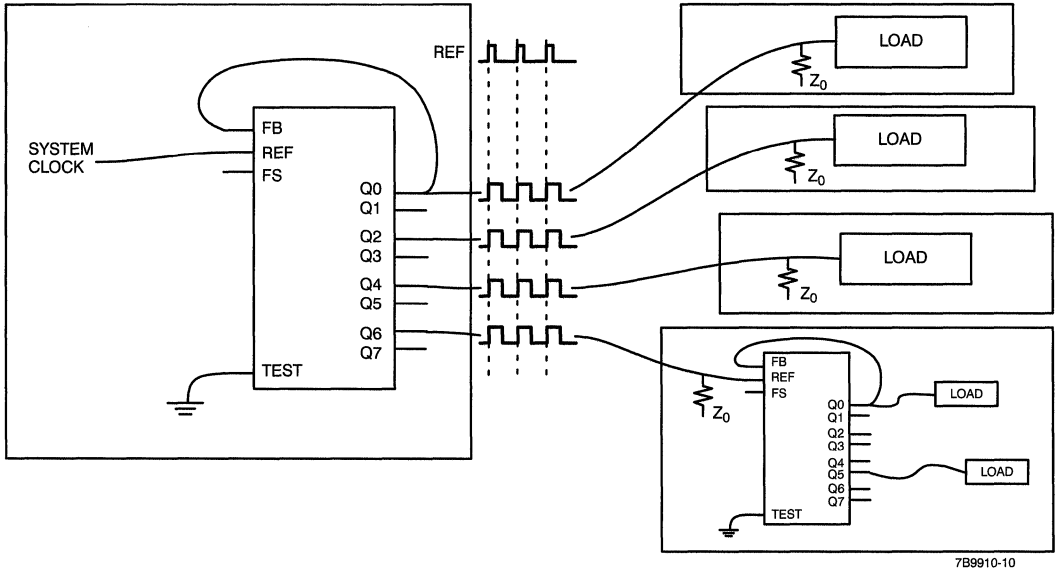


Figure 2. Board-to-Board Clock Distribution

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
500	CY7B9910–5SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9910–5SI	S13	24-Lead Small Outline IC	Industrial
	CY7B9920–5SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–5SI	S13	24-Lead Small Outline IC	Industrial
750	CY7B9910–7SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9910–7SI	S13	24-Lead Small Outline IC	Industrial
	CY7B9920–7SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–7SI	S13	24-Lead Small Outline IC	Industrial

Document #: 38–00437

Section Contents

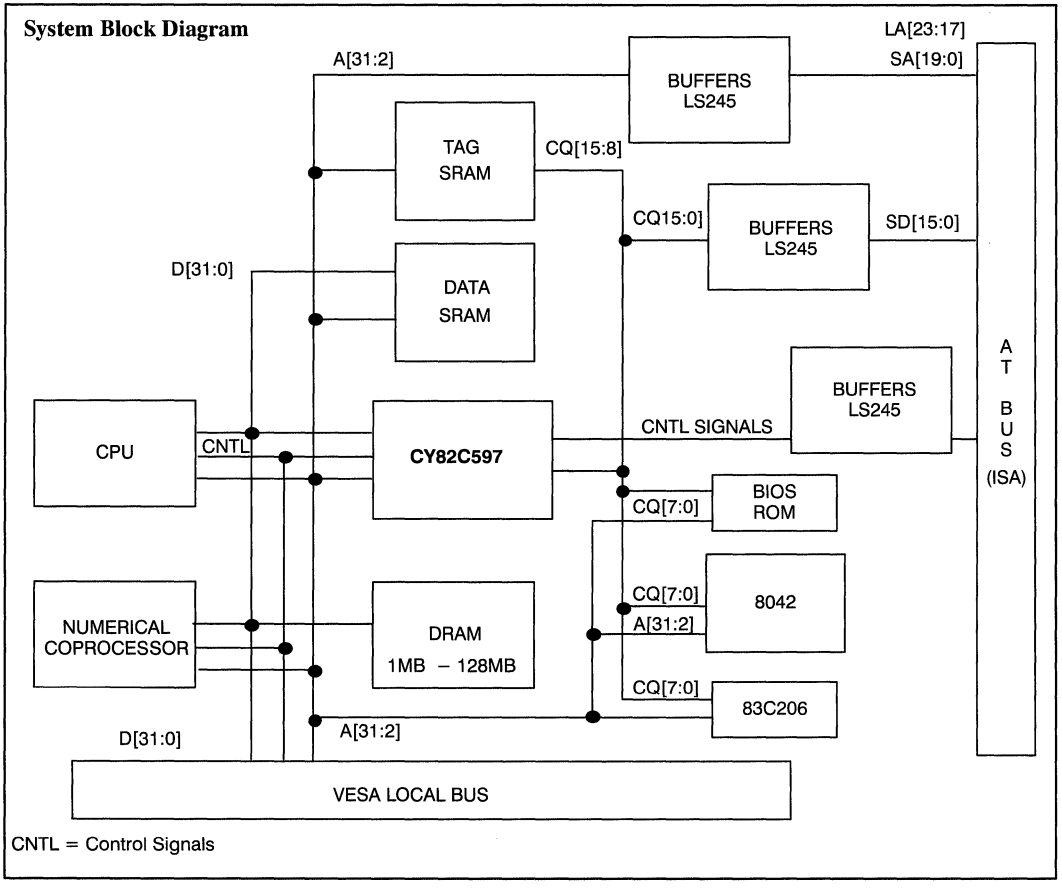
PC Chipsets

386/486 Green Chipset

Features

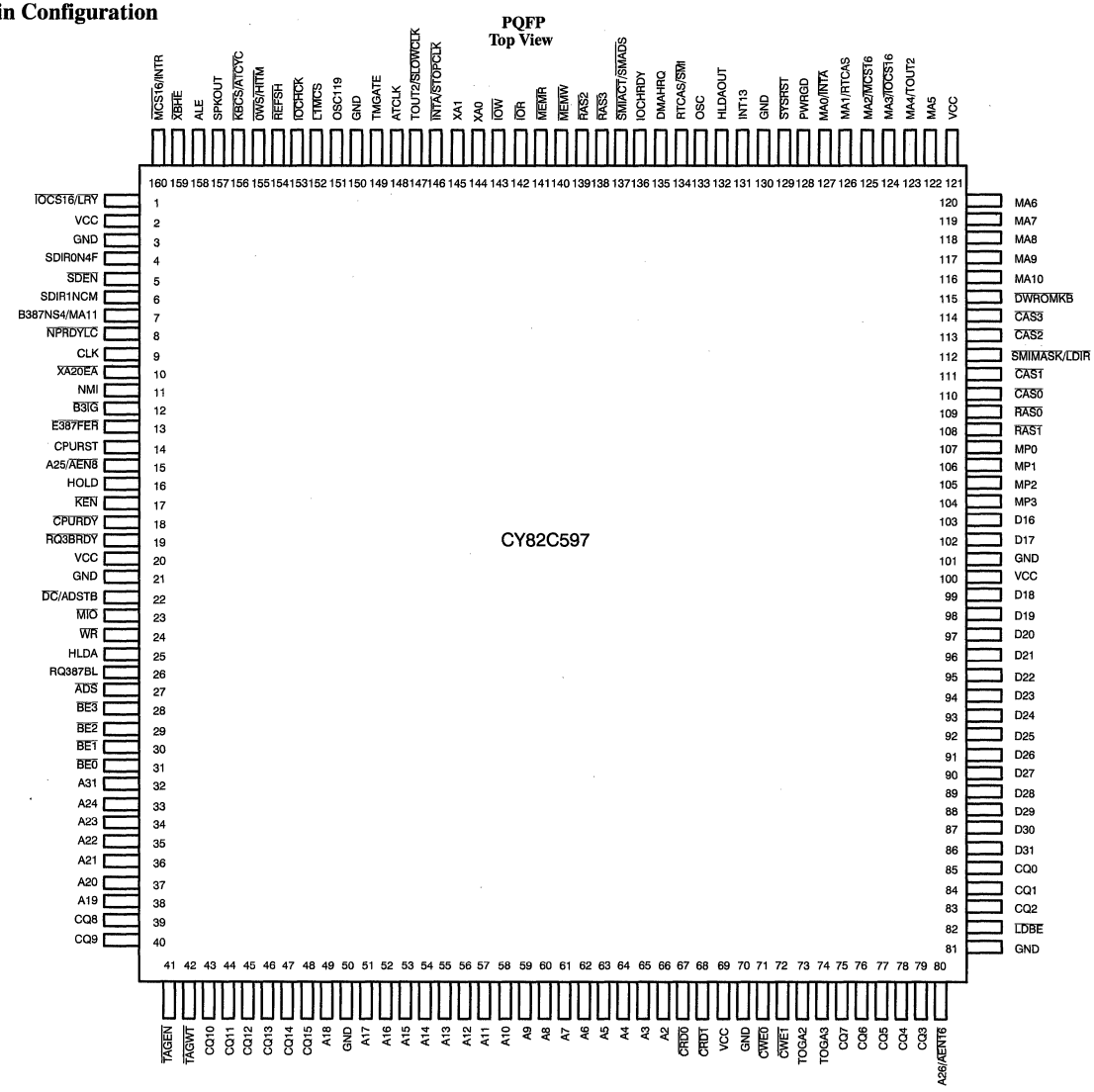
- 160-Pin single chip PQFP
- Supports PC/AT compatible systems at 25/33/40/50 MHz
- Supports AMD, Cyrix level 1 write-back CPU
- Write-Back/Write-Through cache with 32KB/64KB/128KB/256KB/512KB/1MB cache size
- Non-cachable memory range support
- Full VESA Local Bus support. No PAL needed for VESA master mode
- Built-in tag address comparator for lower cost and performance enhancement
- Page mode DRAM controller supports mixture of 256KB/512KB/1MB/2MB/4MB/16MB devices
- Additional DRAM memory can be supported on the AT bus or VESA bus
- Supports up to 128MB of DRAM on the motherboard
- Shadow RAM support
- Memory A,B,D, and E (256KB total) can be remapped to the top of the memory space
- Deep Green support – hardware or software Power-down mode
- Unlimited system state: full speed, stand-by, suspend and any number of user-defined states
- Microsoft® APM support
- 11 event detectors and 5 user-defined timers
- Standard AT refresh and hidden refresh support
- Hardware/software TURBO speed control
- Fast GATEA20, Fast Reset support
- Supports modular design – one motherboard for 386/486/486SX
- Supports Intel/AMD/Cyrix 386DX CPU
- Supports Intel 486DX/DX2/DX4/SL/SX/P24T, Cyrix Cx486, AMD Am486 CPUs

System Block Diagram



CNTL = Control Signals

Pin Configuration



82C597-1

Functional Description

The CY82C597 is a third-generation single chip PC/AT chipset featuring:

- **Single 160-pin gate array – means lower cost**
- **Higher performance – Write-back cache gives you true 0 wait state read/write support.**
- **VESA and AT bus support**
- **Supports Intel, AMD, Cyrix processors**

When combined with the 83C206, the CY82C597 can provide a highly integrated, high-performance, low cost solution for 25/33/40/50 MHz PC/AT systems.

Functional Blocks

The CY82C597 consists of the following functional blocks:

1. Reset and shutdown logic
2. Clock generation logic
3. Bus arbitration logic
4. Turbo speed control logic
5. Level 1 write-back CPU support
6. Write-back/Write-through cache controller
7. Page mode DRAM controller
8. Shadow RAM logic
9. DMA/MASTER access to DRAM
10. Refresh logic
11. VESA local bus logic
12. AT bus interface logic
13. Support logic for various processors
14. Data bus conversion logic
15. Parity generation and checking logic
16. Numerical coprocessor interface logic
17. Keyboard emulation logic
18. Port B, Port70H and NMI logic
19. Power management logic

1. Reset and Shutdown Logic

The CPURST, $\overline{\text{SYSRST}}$, and 387 reset ($\overline{\text{NPRLD}}$) are derived from either the $\overline{\text{PWRGD}}$ signal from the power supply or the reset switch. CPURST is used to reset the CPU and $\overline{\text{SYSRST}}$ is used to reset all AT bus devices. $\overline{\text{NPRLD}}$ is used to reset the 387 coprocessor. Only CPURST is activated when performing a shutdown cycle or a software reset through the keyboard. The 387 reset signal is generated through pin 80 ($\overline{\text{NPRLD}}$). A write to Port F1H will also activate the 387 reset.

2. Clock Generation Logic

For 386 systems, a 2x clock signal should be connected to the CLK pin of the CY82C597. For 486 systems, a 1x clock should be connected to the CLK pin of the CY82C597. ATCLK is generated from CLK divided by a number specified by bit [1:0] of register 10. The desired target for the ATCLK is 8 MHz. Please refer to *Tables 1* and *2* for the recommended clock divisors and ATCLK speeds.

Table 1. 486 Clock Divisors

CPU Speed	Recommended Clock Divisor	ATCLK Speed
33 MHz	4	8.2 MHz
40 MHz	5	8.0 MHz
50 MHz	6	8.3 MHz

Table 2. 386 Clock Divisors

CPU Speed	CLK input to the CY82C597 (CPUCLKx2)	Recommended Clock Divisor	ATCLK Speed
25 MHz	*50 MHz*	*6*	*8.33 MHz*
33 MHz	*66 MHz*	*8*	*8.25 MHz*
40 MHz	*80 MHz*	*10*	*8.00 MHz*

In addition, ATCLK can be fixed at 7.159 MHz (14.31818 MHz/2). The clock source for the 8042 keyboard controller is the same as the ATCLK.

The CY82C597 can also generate a 14.318MHz divided by 12 clock (OSC119 at 1.19 MHz) for system use.

3. Bus Arbitration Logic

The CPU will relinquish control of its bus when a HOLD request is issued by any other device. For DMA and ISA Bus Master cycles, DMAHRQ is generated by the 83C206 causing a HOLD request signal to be sent to the CPU by the CY82C597. The CPU will respond by asserting HLDA and releasing the bus to the requesting device. The CY82C597 will then send an acknowledgement to the 83C206, allowing the DMA/MASTER cycle to be performed. Upon completion of the transaction, the CY82C597 will deassert the hold request, allowing the CPU to access the bus again.

When the CPU performs a master cycle on its local bus, it starts by asserting $\overline{\text{ADS}}$ and a valid address. If the target is motherboard DRAM/SRAM, the DRAM controller inside the CY82C597 will start to access DRAM/SRAM memory and will terminate the cycle with the appropriate signal ($\overline{\text{RDY}}$ or $\overline{\text{BRDY}}$). If the target is a VESA bus device, the device will assert the $\overline{\text{LDEV}}$ (local bus device) signal which will cause the CY82C597 to ignore the cycle and not respond. In this case, it is the responsibility of the VESA target to provide the data and $\overline{\text{RDY}}$ or $\overline{\text{BRDY}}$ acknowledgement to the CPU. If the target is on the AT bus, the CY82C597 will issue an AT bus cycle and complete the CPU bus transaction when the data is available.

4. Turbo Speed Control Logic

The CY82C597 supports both software and hardware Turbo speed control. Software TURBO mode is controlled by bit 2 of register 10H. The hardware TURBO switch should be connected to the 8042 keyboard controller. When the TURBO pin of the 8042 is active, the system software should enable TURBO mode within the CY82C597 (Register 10H bit 2 should be set to 0).

The CY82C597 will assert a HOLD request every 3 µs out of a 4 µs period if bit 2 of register 10H is set to 1 (TURBO mode disabled). When the 8042 TURBO pin is tied non-active, software should disable TURBO mode. The CY82C597 controls

the arbitration between Refresh, DMA and non-TURBO hold request.

5. Level 1 Write-back CPU Support

In order to improve system performance and reduce bus bandwidth requirements, some CPUs (from Intel, AMD, Cyrix, etc.) implement an internal, level 1, write-back cache. Write-back CPUs must snoop (by way of inquiry transactions) all memory transactions. The CY82C597 will generate an inquiry cycle by asserting $\overline{EADS}$, which will be monitored by the CPU, whenever there is an ISA DMA/MASTER memory cycle. During VESA master memory cycles, the VESA master must assert $\overline{EADS}$ along with $\overline{ADS}$. For PCI master memory cycles, the CY82C599 will assert $\overline{EADS}$.

Upon seeing $\overline{EADS}$ asserted, a write-back CPU will check the status of its internal cache. If the CPU's cache contains the line and it is marked modified (the data in the level 1 cache is more up-to-date than the data in main memory), the cpu will assert the $\overline{HITM}$ signal. If the CY82C597 sees $\overline{HITM}$ asserted, it will relinquish the bus to the CPU and will not respond to the original access until the CPU first copies the cache data back to system memory (this is referred to as a write-back cycle). Write-backs consist of burst write cycles (the CY82C597 will handle burst writes to memory), The CY82C597 will wait until the CPU has completed the write-back transaction before allowing any bus master to access the modified memory location.

The CY82C597 has an inquiry filter to reduce the overhead of unnecessary snoop cycles. Every time a bus master attempts to access system memory, the CY82C597 will check to see if the address was previously used for an inquiry cycle. If the address was "snooped" in the previous transaction, the CY82C597 will not generate an inquiry cycle (for ISA/DMA MASTER cycles) or will ignore the results of the inquiry cycle (for VESA/PCI Bus Master cycles) and will allow the transaction to pass directly to system memory.

6. Write-back/Write-through Cache Controller

Write-back Operation

The CY82C597 implements a Burst mode, write-back cache controller. It monitors TAGA[6:0] and compares it with the CPU TAG address. If the cache is enabled and the Tag address matches the CPU address, a "cache hit" is detected. During a read hit, the CY82C597 will burst four double words to the CPU by alternating $\overline{CRD0}$ and $\overline{CRD1}$ (2 Banks of cache) or strobing $\overline{CRD0}$ four times (1 Bank of cache).

In the case of a write hit, the CPU data will be written to the cache RAMs by asserting $\overline{CWE0}$ or $\overline{CWE1}$. DRAM data is not updated.

During a read miss, the DIRTY bit will be checked before reading in new data from the DRAMs. If DIRTY=1, the displaced data from the SRAMs is copied to the DRAMs before the line fill. In the case of a write miss, data will only be written to DRAM.

The CY82C597 also supports an 8-bit tag size (TAGA[7:0]) without a DIRTY bit. All lines are considered dirty. On a cache read miss, the line in the cache is automatically written back to memory before the new line in memory is read. In the case of a write miss, data will only be written to DRAM memory.

Write-through Operation

The CY82C597 also supports write-through cache operation. During a write hit, the CY82C597 writes data to both the SRAMs and the DRAMs. Additional wait states are required especially when a DRAM page miss occurs. For a write miss, data is written to DRAM memory only. Only the 8-bit tag configuration is supported in write-through mode.

The selection between write-through or write-back cache policies is controlled by bit 6 of register 11.

DMA/ISA Master Transactions

When a DMA/MASTER memory read hit occurs, data will be supplied from the cache SRAMs instead of the DRAMs. On a memory read miss, data is supplied by the DRAMs. In the case of a DMA/MASTER memory write hit cycle, data will be written into the DRAMs and SRAMs. A DMA/MASTER write miss cycle will only write data into the DRAMs.

Tag RAM/Data RAM Configurations

The CY82C597 supports 32KB, 64KB, 128KB, and 256KB cache sizes for the 386, and 64KB, 128KB, 256KB, 512KB, and 1MB cache sizes for the 486. In write-back mode, the CY82C597 combines the DIRTY RAM with the Tag RAM, thereby saving one SRAM for cache systems. The dirty bit can be replaced by a tag address in order to increase the cachable range. See *Tables 3, 4,* and *5.* Dirty bit support vs. more cachable memory is controlled through bit 4 of control register 16.

Table 3. Tag RAM/Data RAM Requirements without a Dirty Bit

Cache Size	Tag RAM	Tag Address	Tag Field	Cachable Size[1]
32KB	2K x 8	A14 – A4	A22 – A15	8 MB
64KB	4K x 8	A15 – A4	A23 – A16	16 MB
128KB	8K x 8	A16 – A4	A24 – A17	32 MB
256KB	16K x 8	A17 – A4	A25 – A18	64 MB
512KB	32K x 8	A18 – A4	A26 – A19	128 MB
1MB	64K x 8	A19 – A4	A26 – A20	128 MB

Note:
1. 128MB is the maximum DRAM size supported.

Table 4. Cache with Dirty Bit (TAGA7 will serve as dirty bit)[2, 3, 4, 5]

Cache Size	Tag RAM	Tag Address	Tag Field	Cachable Size
32KB	2K x 8	A14 – A4	A21 – A15	4 MB
64KB	4K x 8	A15 – A4	A22 – A16	8 MB
128KB	8K x 8	A16 – A4	A23 – A17	16 MB
256KB	16K x 8	A17 – A4	A24 – A18	32 MB
512KB	32K x 8	A18 – A4	A25 – A19	64 MB
1MB	64K x 8	A19 – A4	A26 – A20	128 MB

Notes:
2. For 386 cache systems, the cache data RAMs need to be: 32KB cache: 1 bank (4 pieces) 8K x 8 SRAM, 64KB cache: 2 bank (8 pieces) 8K x 8 SRAM, 128KB cache: 1 bank (4 pieces) 32K x 8 SRAM, 256KB cache: 2 bank (8 piece) 32K x 8 SRAM.
3. For 486 cache systems, the cache data RAMs need to be: 32KB cache: 1 bank (4 pieces) 8K x 8 SRAM, 64KB cache: 2 bank (8 pieces) 8K x 8 SRAM, 128KB cache: 1 bank (4 pieces) 32K x 8 SRAM, 256KB cache: 2 bank (8 piece) 32K x 8 SRAM., 512KB: 1 bank (4 pieces) 128K x 8 SRAM, 1MB cache: 2 banks (8 pieces) 128K x 8 SRAM.
4. Cache line size is fixed at 16 bytes.
5. Cachable range is handled automatically by hardware.

Table 5. Tag RAM/Data RAM speed[2, 3]

CPU Speed	Tag RAM Speed	Data RAM Speed (Single Bank)	Data RAM Speed Interleaved (Dual Bank)
25 MHz (386+486)	20 ns	20 ns	25 ns
33 MHz (386+486)	15 ns	20 ns	25 ns
40 MHz (386)	15 ns	15 ns	20 ns
50 MHz (486) 3222 mode	20 ns	20 ns	25 ns

7. Page Mode DRAM Controller

Introduction

A pure Page mode DRAM controller is used in this design. No Interleaving is required. The CY82C597 can support mixed DRAM sizes. The starting address of each DRAM bank is calculated by internal hardware. The user can configure DRAM memory from 1MB to 128MB, as long as the memory stays continuous. The DRAM controller supports up to four banks of DRAM memory. Four RAS and four CAS signals (for three and four bank systems) or two RAS and four CAS signals (for one and two bank systems) are the allowed options. The DRAM controller also provides the multiplexed row and column addresses for the DRAMs. The address split is configurable, and the supported DRAM splits are given in the following tables.

DRAM Row/Column Address

The DRAM row address is listed as follows:

Address Split		DRAM	Row Address											
Row	Col.	Type	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11
9	9	256KB	A12	A13	A14	A15	A16	A17	A18	A19	A11	X	X	X
9	10	512KB	A12	A13	A14	A15	A16	A17	A18	A19	A20	X	X	X
10	10	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	X	X
11	9	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A11	X
12	8	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A11	A10
11	10	2MB	A22	A13	A14	A15	A16	A17	A18	A19	A20	A21	A12	X
12	9	2MB	A22	A13	A14	A15	A16	A17	A18	A19	A20	A21	A12	A11
11	11	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	X
12	10	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A12
16	6	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	X
12	12	16MB	A23	A24	A14	A15	A16	A17	A18	A19	A20	A21	A22	A25

The DRAM column address is listed as follows: [6]

Address Split			Column Address											
Row	Col.	DRAM TYPE	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11
9	9	256KB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	X	X	X
9	10	512KB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
10	10	1MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
11	9	1MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	X	X	X
12	8	1MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	X	X	X	X
11	10	2MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
12	9	2MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	X	X	X
11	11	4MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	X
12	10	4MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
16	6	4MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	X
12	12	16MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	$\overline{A13}$

Notes:
6. The column address lines are inverted from the CPU address.

DRAM Speed

Table 6. DRAM Speed/Wait States (Based on Page Mode DRAMs)

CPU Speed	DRAM Speed	DRAM Wait States (READ, WRITE)
25 MHz	100 ns	(R1WT, W0WT)
	80 ns	(R1WT, W0WT)
33 MHz	100 ns	(R2WT, W0WT)
	80 ns	(R2WT, W0WT)
40 MHz	100 ns	(R2WT, W1WT)
	80 ns	(R2WT, W1WT)
50 MHz	100 ns	(R3WT, W1WT)
	80 ns	(R3WT, W1WT)

8. Shadow RAM Logic

DRAM accesses are generally much faster than accesses to ROM or EPROM. The CY82C597 provides shadow RAM support to speed up system ROM and adapter ROM access time. ROM code can be moved into a reserved RAM space (Shadowed). After the move, the RAM area will be protected (set to read-only). All subsequent accesses to ROM are automatically routed to the protected RAM area. By moving ROM code to DRAM, performance can be improved dramatically. Shadow RAM on blocks C and F can also be configured as cachable or non-cachable (the default is non-cachable).

9. DMA/Master Access to DRAM

DMA cycles are controlled by the 83C206. DMA and ISA MASTER cycles are treated similarly. The arbitration for DMA and ISA MASTER cycles are coordinated through the 83C206. The ISA card will issue a DMA request to the 83C206. The 83C206 will assert DMAHRQ (DMA hold request) to the CY82C597. The CY82C597 will immediately issue a HOLD request to the CPU. Upon receipt of the HLDA (hold acknowledge) from the CPU, the CY82C597 will issue a DMA hold acknowledge to the 83C206 allowing the DMA or ISA MASTER cycle to commence. Once the internal arbitration logic grants a DMA/MASTER cycle, it will monitor the internal cache hit signals, $\overline{\text{MEMR}}$, and $\overline{\text{MEMW}}$. If the cycle is a memory read hit, the CY82C597 will provide data from the SRAMs. A memory read miss cycle will cause data to be accessed from the DRAMs. In the case of a memory write hit cycle, data will be written into both DRAM and SRAM memory. For a write miss cycle, data will be written into DRAM memory only.

10. Refresh Logic

The CY82C597 has an internal counter to generate a refresh request signal every 15.6 µs. Once the internal refresh request signal goes active, the refresh logic will check to see if it is an AT or Hidden refresh (Register 16, bit 6). In the case of an AT refresh, a HOLD request will be issued to the CPU. After receiving HLDA from the CPU, the arbitration logic will grant the refresh cycle. Refresh logic will start the cycle by sending the refresh address and 2 staggered $\overline{\text{RAS}}$ signals to the DRAMs. At the same time, the CY82C597 will send a refresh address and $\overline{\text{REFSH}}$ to the ISA bus. If hidden refresh is programmed, the CY82C597 will not send out a CPU HOLD signal. Instead, the CY82C597 will grant a refresh cycle to the refresh logic if the AT state machine is not busy. If the CPU tries to access the AT bus or DRAM during a hidden refresh, wait states will be inserted into the cycle until the refresh completes.

11. VESA Local Bus Logic

The CY82C597 supports VESA Local Bus devices by monitoring pin 8 ($\overline{\text{NPRDYLC}}$) at the end of T2 (2-1-1-1 mode) or the end of the second T2 (3-1-1-1/3-2-2-2 mode). All VESA $\overline{\text{LDEV}}$ signals should be externally ANDed together to provide the $\overline{\text{NPRDYLC}}$ signal. If a local device cycle is detected ($\overline{\text{NPRDYLC}}$ asserted LOW by any local device), the CY82C597 will allow the local device to fully control the bus.

The CY82C597 can also perform the arbitration for up to 2 VESA masters. The arbitration is fixed priority (device 1 has a higher VESA priority than device 2). When the CY82C597 detects a local request from a VESA master, it immediately issues a HOLD request to the CPU. Upon receiving HLDA from the CPU, the CY82C597 will grant the VESA bus to the highest priority master (provided that a refresh request is not pending). The CY82C597 will release the grant to the VESA master when its request is deactivated.

12. AT Bus Interface Logic

An AT bus cycle begins when the CPU wants to access an AT bus device. When ALE is generated, the AT state machine monitors $\overline{\text{MCS16}}$, $\overline{\text{IOCS16}}$, $\overline{\text{0WS}}$ and IOCHRDY from the AT bus and generates the command and control signals to the AT bus. The current AT bus cycle is terminated when a ready signal ($\overline{\text{CPURDY}}$) is returned to the CPU.

In order to support DMA/MASTER accesses, the CY82C597 will generate $\overline{\text{ADS}}$, M/$\overline{\text{IO}}$, and W/$\overline{\text{R}}$, after detecting HOLDA from the CPU.

13. Support for Various Processors via Modular Design

Modular design means all common components reside on the motherboard with the CPU and the cache memory socketed for easy upgrade. With this technology, the user can build a 386, 486, or 486SX cache/non-cache system using the same motherboard.

The CY82C597 supports various processors. When pin 7 ($\overline{\text{B387S4}}$) is pulled to V_{CC} through a 10 KΩ resistor, a 386 processor is selected. If pin 7 is pulled down to V_{SS}, the CY82C597 will consider the processor to be a 486. With this feature, the user can build one motherboard to support 386 cache/non-cache, and 486DX/SX cache/non-cache system.

14. Data Bus Conversion Logic

As the 486 CPU bus is 32 bits wide and the ISA bus has 8 and 16 bit residents, the CY82C597 performs data bus conversion for the following cycles: (1) CPU accesses 8- or 16-bit devices on the CQ bus through 16/32-bit instructions, (2) DMA/MASTER cycles from AT devices to local DRAM, cache memory, or on-board I/O devices (8/16 bit device translation to a 32/16 bit CPU bus).

During the conversion, the CY82C597 automatically provides all the necessary control signals to the external bidirectional data buffers.

15. Parity Generation and Checking Logic

For local DRAM write cycles from both the CPU and DMA/MASTER devices, the CY82C597 generates byte parity bits MP[3:0]. The parity bits are stored in the local DRAM along with the data.

During the local DRAM read cycle, the data and parity bits are read from the DRAMs into the CY82C597. Parity checking logic compares the parity bits with the parity generated from the read data. If a mismatch is detected and the system memory parity check is enabled, an NMI will be asserted by the CY82C597, if NMI reporting in enabled.

16. Numerical Coprocessor Interface Logic

The CY82C597 supports the Weitek 4167 Numerical Coprocessor (486SX systems), the Weitek 3167, and the Intel 387 Numerical Coprocessor (386 systems) without any external logic.

For 486SX systems, INT13 will be asserted when either $\overline{FERR}$ or WTINTR is activated. As soon as the $\overline{FERR}$ is asserted, the interrupt service routine will handle the error and clear the interrupt by executing a dummy write to I/O port F0H. The $\overline{IGNNE}$ signal is also activated by writing to the I/O port F0H.

For 386 systems, $\overline{BUSY386}$ is asserted when $\overline{BUSY387}$ is active to signal the 386 that the coprocessor is currently executing an instruction. If $\overline{BUSY387}$ is active when $\overline{ERR387}$ is active, the $\overline{BUSY387}$ will be latched and IRQ will be generated. The latched $\overline{BUSY387}$ can be cleared by performing a write to I/O port F0H. If the Weitek 3167 is being used and the interrupt signal (WTINTR) is active, IRQ will be asserted. The $\overline{ERR386}$ signal is asserted after system reset if a 387 is present. It will stay active until the first CPU cycle begins.

17. Keyboard Emulation Logic

I/O Port 60H and 64H are used to implement keyboard controller emulation. The keyboard emulation is enabled by programming register 10, bit 3 to a 0. When fast GA20 is enabled, writing D1H to Port 64H followed by DDH to Port 60H, A20 will be forced LOW in a 386 system. For a 486 system, the $\overline{A20M}$ pin should be connected to the 8042 and E386NGT functions as the A25 input. If the system is designed to support 32 MB of main memory or less, the E386NGT signal can be connected to the $\overline{A20M}$ signal on the 486 for fast GATEA20 operation.

The CY82C597 also performs fast RESET by intercepting the keyboard reset command sequence and performing the reset directly. The CY82C597 can be programmed to wait for a HALT instruction before asserting reset to the CPU.

18. Port B (61H), NMI, and Port 70H

When a parity error is detected by the CY82C597 , an NMI will be generated to the CPU if NMI reporting is enabled. NMI reporting can be enabled by setting bit 7 of Port 70H to 0. The CY82C597 provides access to the Port B register defined for a PC/AT. The chart below illustrates the bit definition for Port B (61H):

Address	Bit	Access	Description
61H	7	Read Only	System memory parity check
	6	Read Only	I/O channel check
	5	Read Only	Timer 2 output
	4	Read Only	Refresh detection
	3	Read/Write	0: Enable I/O channel check 1: Disable I/O channel check
	2	Read/Write	0: Enable system memory parity check. 1: Disable system memory parity check
	1	Read/Write	Speaker data
	0	Read/Write	Timer 2 gate

19. Power Management Logic

The CY82C597 implements flexible power management logic. When used with the CY82C599 (for a full VESA/ISA/PCI system), most of the power management functions are performed by the CY82C599. The CY82C597 will only perform the SMM memory mapping. All other power management functions in the CY82C597 are disabled. For VESA/ISA-only systems, the CY82C597 provides all of the chipset power management.

There are eleven event detectors and five user-programmable timers in the CY82C597 allowing it to support full hardware power management (for CPUs that do not support SMM, System Management Mode) and software power management (through SMM).

Monitored Events

The CY82C597 allows the following events to be monitored:

1. VESA master request
2. Keyboard command
3. Serial Port command
4. Parallel Port command
5. Hard Disk command
6. DMA/MASTER request from the ISA bus
7. Non-motherboard memory access
8. Video memory access
9. A specific I/O address
10. A specific memory range
11. A specific I/O range

When events are detected, the CY82C597 will transition to different power-down states.

Hardware Power Management

For hardware power management, the CY82C597 supports Full-speed/Stand-by/Suspend/Off states. In Stand-by state, the CY82C597 will assert the $\overline{SLOWCLK}$ signal that can be used by the system to slow down the CPU's clock frequency. In the Suspend state, the CY82C597 will assert the $\overline{STOPCLK}$ signal. $\overline{STOPCLK}$ can be used to stop the CPU's clock or turn off the monitor and other supported peripherals.

In the Full-speed state, the CY82C597 will monitor all stand-by events. Any monitored event will reset the stand-by timer. If no events occur within the period specified by the stand-by timer, the CY82C597 will enter the Stand-by state and assert the $\overline{SLOWCLK}$ signal. Once Stand-by state has been entered, the CY82C597 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C597 will assert $\overline{STOPCLK}$ and enter the Suspend state. In the Suspend state, the assertion of $\overline{STOPCLK}$ can be used to stop the CPU's clock or power-down any supported peripherals. If any monitored event is detected, the CY82C597 will return to the Full-speed state and $\overline{STOPCLK}$/$\overline{SLOWCLK}$ will be deasserted.

Any interrupt will temporarily cause the $\overline{STOPCLK}$ signal (and optionally the $\overline{SLOWCLK}$ signal) to be deasserted (allowing the CPU to service the interrupt). If the interrupt timer expires before a monitored event occurs, the CY82C597 will automatically return to the power-down state it was in prior to the interrupt (with the appropriate signal asserted).

Software Power Management

For software power management, the CY82C597 can fully utilize Intel's, AMD's, and Cyrix's power management modes to reduce system power requirements.

In the Full-speed state, the CY82C597 will monitor all stand-by events. If no events occur within the period specified by the stand-by timer, the CY82C597 will enter the Stand-by state and assert the $\overline{SMI}$ signal. In Stand-by state, the system clock can be slowed down by the assertion of the $\overline{SLOWCLK}$ signal. $\overline{SLOWCLK}$ is controlled through software (See Register 64). Once Stand-by state has been entered, the CY82C597 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C597 will assert $\overline{SMI}$ and enter the Suspend state. In the Suspend state, software assertion of $\overline{STOPCLK}$ (See register 64) can be used to stop the CPU's clock, the monitor can be turned off using a software driver, or the hard disk can be spun down. Please note that the assertion/deassertion of $\overline{STOPCLK}$ and $\overline{SLOWCLK}$ is fully software controlled and can be implemented in any power-down state (Stand-by and Suspend are customary).

The Suspend timer is fully reprogrammable. In the Suspend state, the Suspend timer can be disabled, the timer value changed, and the timer reenabled. After the new timer value has expired, $\overline{SMI}$ will once again be activated to allow for a user-defined power management mode.

The CY82C597 also contains three independent timers that can be used during the power-down control period. Different events and different time periods can be specified for each timer. Each timer will cause $\overline{SMI}$ to be asserted after the specified time period has expired. The three timers allow for more user-defined, power-down system states.

In order to identify the source of the $\overline{SMI}$ (System Management Interrupt), the CY82C597 maintains a status register (register 58) that keeps track of which event caused $\overline{SMI}$ to be asserted. Power-management software should read the status register before determining a course of action. The CPU and peripherals can be individually powered-down based on the source of the System Management Interrupt.

If any specified event is detected during Stand-by, Suspend, or any other power-down state, the CY82C597 will automatically return to the Full-speed state (with the stand-by timer reset). If the system is using software power management, the CY82C597 will assert $\overline{SMI}$ and within the $\overline{SMI}$ handler, software should bring all of the system clocks to their full-speed, full-power states through the deassertion of $\overline{STOPCLK}/\overline{SLOWCLK}$.

The CY82C597 supports SMM (System Management Mode) memory. If $\overline{SMACT}$ (Intel) or $\overline{SMADS}$ (Cyrix, AMD) is seen asserted, all memory accesses will be sent to a protected memory space (physical DRAM blocks A and B). The SMI handler and SMM data must be stored in the protected space. If software power management is used, ROM or video RAM cannot be shadowed in blocks A and B.

CY82C597 Control Registers

The control registers for the CY82C597 are defined in this section. The registers can be accessed through I/O Ports 22H and 23H. To access each register, the user must first write the index number of the register into Port 22, which forces the internal decoding logic to point to the selected register. Data can be accessed by then reading/writing to/from Port 23.

Register 10: AT Bus Control, Index: 10

Bit	Function	Default
7	486 speed indicator: 0: 20/25 MHz 1: 33/40/50 MHz	0
6	Parity check disable: [7] 0: Enable parity checking 1: Disable parity checking	0
5	386 speed indicator: 0: 40 MHz 1: 33 MHz (or any speed below 33 MHz)	0
4	Reserved, BIOS should set to 1.	0
3	Fast Gate A20 Emulation Control (386 only): 0: Enable 1: Disable	0
2	Turbo speed control: 0: Enable turbo speed (high speed) 1: Enable low speed	0
1:0	ATCLK control: Bits 01 486 system: (pin 4 tied to V_{CC} through a 51KΩ resistor) 00: CLK/4 01: CLK/6 10: CLK/8 11: CLK/5 Bits 01 486 system: (pin 4 tied to V_{SS} through a 1KΩ resistor) 00: CLK/2 01: CLK/3 10: CLK/4 11: CLK/2.5 Bits 01 386 system: 00: CLK/4 01: CLK/6 10: CLK/8 11: CLK/10	00

Notes:

7. If parity checking is disabled, the parity bits are used as VESA local bus request and grant signals (see pin description). If parity is required in the system, an external PAL must be used to control VESA local arbitration signals (if bus mastership from the VESA slots is allowed).

Register 11: Cache Control, Index: 11

Bit	Function	Default
7	486 Burst control mode: [8] 0: 3111 Burst Mode. For 33/40/50 MHz systems. 1: 2111 Burst Mode. For 20/25/33 MHz systems. For 386 systems, this bit should be set to 1 by the BIOS.	0
6	486 external cache type control: 0: Write-back cache. 1: Write-through cache. For 386 systems, only write-back cache is supported. This bit is ignored.	0
5	SRAM write wait states: 0: 1 wait 1: 0 wait	0
4	Direct SRAM access control: 0: Disable 1: Enable	0
3:2	Cache size: [9] Bits 32 Size (386 system): 00: 32KB; 01: 64KB; 10: 128KB; 11: 256KB Bits 32 Size (486 system): 00: 64KB; 01: 128KB; 10: 256KB; 11: 512KB	00
1	Cache hit/miss control: 0: All cache accesses are forced to miss 1: Normal cache access	0
0	Cache enable control: 0: Disable cache 1: Enable cache	0

Before enabling direct SRAM access, the cache should be disabled. After direct SRAM access is enabled, all CPU accesses to address 40000H to 7FFFFH will be forced to SRAM when the cache size is smaller than 512KB. If the cache size is 512KB, or larger, addresses from 20000H to 9FFFFH will be forced to SRAM. This feature can be used to debug/test cache memory.

Register 12: DRAM Type, Index: 12

Bit	Function	Default
7	Reserved, BIOS should set to 0.	0
6	Reserved, BIOS should set to 0.	0
5	Reserved, BIOS should set to 1.	0
4	0: Enable Flash write[10] 1: Disable Flash write	0
3:2	Bank 1: [11] Bits 32 Type: 00: Disabled; 01: 256KB; 10: 1MB; 11: 4MB	00
1:0	Bank 0: [12] Bits 10 Type: 00: 256KB; 01: 1MB; 10: 4MB; 11: Disabled	00

Notes:
8. See register 1B, bit 6.
9. See register 1A, bit 1.
10. If Flash write is disabled, writes into ROM space will not be executed.
11. See register 1A, bit 7.
12. See register 1A, bit 5.

Register 13: DRAM Wait State and Cachable Range Control, Index: 13[13]

Bit	Function	Default
7:4	Bits: 7654 Range 0000: 0–128MB 0001: 0–8MB 0010: 0–16MB 0011: 0–24MB 0100: 0–32MB 0101: 0–40MB 0110: 0–48MB 0111: 0–56MB 1000: 0–64MB 1001: 0–72MB 1010: 0–80MB 1011: 0–88MB 1100: 0–96MB 1101: 0–104MB 1110: 0–112MB 1111: 0–128MB	0000
3	Reserved, BIOS should set to 1.	0
2	DRAM write wait states: 0: 1 wait state 1: 0 wait states	0
1:0	DRAM read wait states: Bits 10 # of wait states 00: 3 01: 2 10: 1 11: 0	00

Notes:
13. The CY82C597 will take care of the cachable range. Bits [7:4] are for custom memory configurations.

Register 14: DRAM Wait State and Cachable Range Control, Index: 14

Bit	Function	Default
7	CPU reset control: 0: CPU reset will not wait for HALT instruction 1: CPU reset will wait for HALT instruction.	0
6	RAS precharge time:[14] 0: 3 clocks 1: 2 clocks	0
5	Reserved, BIOS should set to 0	0
4:0	Remap location: Bits 43210 Location 00000: Disable remap 00001: 1M 00010: 2M 00100: 4M 00101: 5M 01000: 8M 10000: 16M 10001: 17M 10100: 20M	00000

If blocks A, B, D, E on the local bus are not used for shadowing peripheral ROM, they can be remapped to the top of the memory space. By doing this, a 4-MB memory space can become 4MB +256KB. The physical location of the remapped 256KB are in DRAM blocks A, B, D, and E. If any of blocks A, B, D, and E are being used to shadow peripheral ROM, remapping is not allowed.

Register 15: Shadow RAM Block C, F Control, Index: 15

Bit	Function	Default
7	Block F RAM access control (F0000H–FFFFFH): 0: Write only 1: Read only	0
6	Block F RAM enable control: 0: Disable. Access on board ROM. 1: Enable. Access RAM	0
5	Shadow RAM at CC000H–CFFFFH control: 0: Disable. Will access AT bus memory. 1: Enable.	0
4	Shadow RAM at C8000H–CBFFFH control: 0: Disable. Will access AT bus memory. 1: Enable.	0
3	Shadow RAM at C4000H–C7FFFH control: 0: Disable. Will access AT bus memory. 1: Enable	0
2	Shadow RAM at C0000H–C3FFFH control: 0: Disable. Will access AT bus memory. 1: Enable.	0
1	Block C RAM access control (C0000H–CFFFFH): 0: Write only. 1: Read only.	0
0	Block C RAM/ROM control: 0: Access RAM. If RAM is disabled, access will go to AT bus memory. 1: Access on board ROM.	0

Notes:
14. When DRAM read wait states are set to 3, the RAS precharge time will be forced to 4 clocks (50 MHz system).

Shadowing Instructions

To shadow system BIOS (Block F), you must:

1. Set register 15, bit 6 to "0" to enable ROM access.
2. Read ROM data into the CPU register.
3. Set register 15, bit 6 to "1" to enable RAM access.
4. Set register 15, bit 7 to "0" to enable RAM write.
5. Write the data stored in the CPU register to RAM.
6. Go to step 1 if not done. Else, go to step 7.
7. Set register 15, bit 7 to "1" to enable shadow RAM read access and write protect it.

Shadowing on-board ROM is similar to shadowing system ROM. The following example is used to shadow Block C from on-board ROM:

1. Set register 15, bit 0 to "1" to enable ROM access.
2. Read ROM data into the CPU register.
3. Set register 15, bit 0 to "0" to enable RAM access.
4. Set register 15, bit 1 to "0" to enable RAM write.
5. Write the data stored in the CPU register to RAM.
6. Go to step 1 if not done. Else, go to step 7.
7. Set register 15, bit 1 to "1" to enable shadow RAM read access and write protect it.

Shadowing AT bus ROM is slightly different than shadowing on-board ROM. The following example is used to shadow Block C from AT bus ROM:

1. Set register 15, bit 0 to 0 to disable on-board ROM access.
2. Set register 15, bits 2, 3, 4, and 5 to 0 to disable RAM access. All access to Block C will go to the AT bus.
3. Read AT ROM data into CPU register.
4. Set register 15, bits 2, 3, 4, and 5 to 1 to enable RAM access.
5. Set register 15, bit 1 to 0 to enable RAM write.
6. Write the data stored in CPU register to RAM.
7. Go to step 1 if not done. Else, go to step 8.
8. Set register 15, bit 1 to 1 to enable shadow RAM read access and write protect it.

Register 16: Miscellaneous Control 1 Register, Index: 16

Bit	Function	Default
7	SRAM $\overline{TAGWT}$ delay control: 0: For 1 wait state SRAM 1: For 0 wait state SRAM	0
6	Hidden Refresh Control: 0: AT refresh 1: Hidden refresh.	0
5	DRAM $\overline{RAS}$ to MA [10:0], MA [10:0] to $\overline{CAS}$ delay. 0: 2 clocks. 1: 1 clock.	0
4	Dirty bit enable control: 0: Disable. No dirty bit (8 bit tag). 1: Enable. TAGA7 becomes the dirty bit (7 bit tag).	0
3	DRAM 15–16 MB disable control: 0: Normal. 1: Address 15–16 MB will not be on the motherboard.	0
2	Non-cachable block dual-function control: (for register 18, 19, and 1A) 0: For non-cachable block. 1: Non-cachable block becomes a non-local memory block.	0
1	Reserved, BIOS should set to 0.	0
0	Reserved, BIOS should set to 0.	0

Register 17: Miscellaneous Control 2 Register, Index: 17

Bit	Function	Default
7	Block F(F0000H–FFFFFH) Cachable control: 0: Non-cachable. 1: Cachable.	0
6	Block C(C0000H–CFFFFH) Cachable control: 0: Non-cachable. 1: Cachable.	0
5	Reserved, BIOS should set to 1.	0
4	Reserved, BIOS should set to 0.	0
3	Reserved, BIOS should set to 0.	0
2	Reserved, BIOS should set to 1.	0
1	Reserved, BIOS should set to 1.	0
0	$\overline{EADS}$ control: 0: $\overline{EADS}$ is a dedicated output. 1: $\overline{EADS}$ is three-state.	0

Register 18: Non-Cachable/non-local Block 0 Starting Address, Index: 18[15, 16, 17]

Bit	Function								Default
7:0	Bits								00000000
	7	6	5	4	3	2	1	0	
	A23	A22	A21	A20	A19	A18	A17	A16	

Notes:
15. Bits 0, 1, 2, 3, 4, and 5 may not be needed. Please see note on Register 19.
16. A24 of the non-cachable/non-local Block 0 starting address is bit 0 of Register 19.
17. A25 and A26 of the non-cachable/non-local Block 0 starting address are bits 2 and 3 of Register 1A.

Register 19: Non-cachable Block 0 Starting Address and Size, Index: 19[18]

Bit	Function	Default
7	Slow DRAM select: 0: Fast page mode DRAM supported. 1: Fast page mode DRAM not supported	0
6	486 Single bank SRAM select: 0: Support interleaved SRAMs (2 banks of SRAMs). 1: Support 1 bank of SRAMs. This is for 128KB cache using 32Kx8 SRAMs and 512KB cache using 128Kx8 SRAMs.	0
5	Reserved, BIOS should set to 0.	0
4	Non-cachable Block 0 control: 0: Disable. 1: Enable.	0
3:1	Non-cachable size Bits: 321 Size 000: 64KB 010: 128KB 100: 256KB 110: 512KB 001: 1MB 011: 2MB	000
0	Non-cachable/non-local Block 0 starting address A24.	0

Note:

18. For 64KB non-cachable size, the starting address is bound by A24–A16 from the configuration registers.
For 128KB non-cachable size, the starting address is bound by A24–A17 from the configuration registers.
For 256KB non-cachable size, the starting address is bound by A24–A18 from the configuration registers.
For 512KB non-cachable size, the starting address is bound by A24–A19 from the configuration registers.
For 1MB non-cachable size, the starting address is bound by A24–A20 from the configuration registers.
For 2MB non-cachable size, the starting address is bound by A24–A21 from the configuration registers.

Please note that the non-cachable size is independent of cache size. The non-cachable starting address and non-cachable size are used to define an address range that will not be cached.

When Register 16, bit 2 is set to 1, the non-cachable block will be changed to a non-local block. All addresses within this block will not be on the motherboard, i.e., they will go to the AT bus or VESA bus.

For 386 systems, 32KB/128KB cache is fixed to 1 bank of SRAMs. 64KB/256KB is fixed to 2 banks of SRAMs. For 486 systems, 64KB/128KB/256KB/512KB/1MB can be either 1 or 2 banks of SRAMs.

Register 1A: Control Register, Index: 1A

Bit	Function	Default
7:6	Bank 1 DRAM size modification:[19] Bits 00: Bank 1 size is determined by Register 12, bit [3:2] 01: 512KB DRAM 10: 16MB DRAM 11: 2MB DRAM	00
5:4	Bank 0 DRAM size modification: [20] Bits 00: Bank 0 size is determined by register 12, bit [1:0] 01: 512KB DRAM 10: 16MB DRAM 11: 2MB DRAM	00
3:2	Non-cachable/non-local Block 0 starting address (See register 18): 3=A26 2=A25	0
1	Bits 1: 1MB cache size 0: Refer to Register 11, but [3:2]	0
0	Reserved, BIOS should set to 0.	0

Register 1B: Miscellaneous Control Register 3, Index: 1B

Bit	Function	Default
7	Reserved, BIOS should set to 0.	0
6	Additional cache speed control: 0: No additional delay. 1: Additional delay, 3222 mode for 50 MHz. Once set, it will overwrite register 11, bit 7, which is used to control cache SRAM 2111 or 3111 burst sequence.	0
5	Reserved, BIOS should set to 1.	0
4	Reserved, BIOS should set to 0.	0
3:2	Reserved, BIOS should set to 11.	00
1:0	Reserved, BIOS should set to 00.	00

Notes:

19. If Bank 1 is selected for 512KB/16MB/2MB operation, the value in register 12, bits [3:2], will be ignored.
20. If Bank 0 is selected for 512KB/16MB/2MB operation, the value in register 12, bits [1:0], will be ignored.

Register 1C: Miscellaneous Control Register, Index: 1C

Bit	Function	Default
7	Bits 0: Symmetrical 4MB DRAM 1: Special 4MB DRAM with 16 row addresses and 6 column addresses	0
6	Bits 0: Symmetrical 4MB DRAM 1: Special 4MB DRAM with 12 row addresses and 10 column addresses	0
5	Bits 0: Normal mode (For 40/50 MHz systems, this bit should be set to 0) 1: Fast write at 25/33 MHz	0
4	Reserved, BIOS must set to 1.	0
3	Bits 0: Keyboard soft reset will not generate NPRST 1: Keyboard soft reset will generate NPRST	0
2	Reserved, BIOS should be set to 0.	0
1	Bits 0: ATCLK controlled by register 10, bit [1:0] 1: ATCLK fixed at 7.159 MHz	0
0	Bits 0: Normal mode (no additional IDLE AT CYCLES between AT command cycles) 1: Add one extra IDLE AT CYCLE between AT command cycles	0

Register 1D: Miscellaneous Control Register, Index: 1D

Bit	Function	Default
7	Bits 0: Normal mode (enable upper DRAM) 1: Upper 64KB or 1KB DRAM memory will be disabled	0
6	Bits 0: Upper 64K of DRAM will be disabled if bit 7=1 1: Upper 1K of DRAM will be disabled if bit 7=1	0
5	Reserved, BIOS should set to 0.	0
4	Bits 0: Add one SYSCLK cycle of delay before AT cycle detection 1: Add two SYSCLK cycles of delay before AT cycle detection	0
3	Fast DRAM write, BIOS should set to 1.	0
2	Reserved, BIOS should be set to 0.	0
1	Bits 0: AT cycle detection at end of T2 if register 11, bit 7=1 (2111 mode) AT cycle detection at end of second T2 if register 11, bit 7=0 (3111/3222 mode) 1: Add extra delay on AT cycle detection, extra delay based on register 1D, bit 4 setting	0
0	Reserved, BIOS should set to 0.	0

Registered 1E: Power Management Stand-by Timer and Event Control Register 1, Index: 1E

Bit	Function	Default
7	Reserved	0
6	Bits 0: Do not monitor VESA master request 1: Monitor VESA master request	0
5	Stand-by mode timer control, please see BIT (3:1): If Bit 5=0: 000: 30 sec., 001: 3.8 min., 010: 7.5 min., 011: 15 min., 100: 30 min., 101: 60 min., 110: 120 min., 111: 240 min. If Bit 5=1: 000: 0.2 sec., 001: 0.4 sec., 010: 1 sec., 011: 1.8 sec., 100: 3.5 sec., 101: 7 sec., 110: 14 sec., 111: 30 sec.	0
4	Reserved	0
3:1	Stand-by mode timer (Values for bits 3:1 are given in bit 5 definition)	000
0	Bits 0: Disable power management mode 1: Enable power management mode	0

Register 1F: Stand-by Mode Event Control, Index: 1F

Bit	Function	Default
7	Bits 0: Disable keyboard detection 1: Enable keyboard detection	0
6	Bits 0: Disable serial port detection 1: Enable serial port detection	0
5	Bits 0: Disable parallel port detection 1: Enable parallel port detection	0
4	Bits 0: Disable hard disk detection 1: Enable hard disk detection	0
3	Bits 0: Disable DMA/ISA MASTER detection 1: Enable DMA/ISA MASTER detection	0
2	Bits 0: Disable non-motherboard memory detection 1: Enable non-motherboard memory detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) detection 1: Enable video memory (Block A,B) detection	0

Register 60: I/O Address (for Address Detection), Index: 60

Bit	Function	Default
7:0	Bits 7:0 I/O Address to be Monitored	00000000

Register 61: I/O Address Detection and Miscellaneous Control, Index: 61

Bit	Function	Default
7	Bits 0: VESA/AT only mode (82C597 stand-alone) 1: 82C599 PCI bridge is present in the system	0
6	Bits 0: NMI output is non three-state 1: NMI output is three-state	0
5	Reserved	0
4	Reserved	0
3	Bits 0: Disable I/O address detection 1: Enable I/O address detection	0
2	Reserved, must be 0.	0
1:0	I/O address (9:8).	00

Register 62: Suspend Timer and Interrupt Timer Control, Index: 62

Bit	Function	Default
7:4	Bits (Suspend Timer Period) 0000: 3.8 min. 0001: 7.5 min. 0010: 15 min. 0011: 30 mins. 0100: 60 mins. 0101: 120 mins. 0110: 240 mins. 0111: 480 mins. 0000: 1 sec. 1001: 1.8 sec. 1010: 3.5 sec. 1011: 7 sec. 1100: 14 sec. 1101: 28 sec. 1110: 56 sec. 1111: 2 min.	0000
3:0	Bits (Interrupt Timer Period) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 54 µsec. 0110: 107 µsec. 0111: 215 µsec. 0000: 430 µsec. 1001: 860 µsec. 1010: 1.7 msec. 1011: 3.4 msec. 1100: 7 msec. 1101: 14 msec. 1110: 28 msec. 1111: 55 msec.	0000

The suspend timer is enabled when register 64 bit 1=0. When enabled, the suspend timer always follows the stand-by timer (i.e., it will not start counting until the stand-by timer has reached its terminal count. For hardware Power-down mode, the 82C597 will assert $\overline{\text{STOPCLK}}$ after the suspend timer has reached its terminal count. For software Power-down mode, the 82C597 will generate an $\overline{\text{SMI}}$ after its terminal count. $\overline{\text{STOPCLK}}$ and other power-down features can be implemented in $\overline{\text{SMI}}$ subroutines.

The interrupt timer is used for interrupt service routines. When the INTR input becomes active, the 82C597 will deassert $\overline{\text{STOPCLK}}$ and start the interrupt timer. After the interrupt timer reaches its terminal count, the 82C597 will assert $\overline{\text{STOPCLK}}$ again (if no event occurs during the interrupt period). This timer is used for both hardware and software Power-down modes and is enabled by register 63, Bit 2.

Register 63: Power-down Mode and DRAM Non-cachable Control, Index: 63

Bit	Function	Default
7	Bits 0: Disable hardware Power-down mode 1: Enable hardware Power-down mode	0
6	Bits 0: Disable software Power-down mode 1: Enable software Power-down mode	0
5	Bits 0: Disable interrupt input (INTR) 1: Enable interrupt input (INTR) Should be 1 when Power-down mode is enabled	0
4	Should be 0.	0
3	Bits 0: $\overline{\text{SLOWCLK}}$ does not change when input INTR active 1: $\overline{\text{SLOWCLK}}$ will be inactive when input INTR active	0
2	Bits 0: Enable interrupt timer (default) 1: Disable interrupt timer	0
1	0: Top 128K DRAM is not cachable 1: Top 128K DRAM is cachable	0
0	Must have the same value as bit 6.	

Hardware Power-down mode allows $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ to be controlled by the 82C597 hardware. Software Power-down mode will use System Management Mode ($\overline{\text{SMM}}$) subroutines to implement power-down control.

Register 64: Power-Down Mode Control, Index: 64

Bit	Function	Default
7	Bits Software initial $\overline{\text{SMI}}$ 0: Normal 1: Writing an 1 to this bit will generate an $\overline{\text{SMI}}$ to CPU. After a 1 is written, software should write a 0 to this bit.	0
6	Bits $\overline{\text{SMI}}$ inactive control 0: Normal 1: Writing a 1 to this bit will deassert the $\overline{\text{SMI}}$ signal. This is the only way to cause the 82C597 to deassert $\overline{\text{SMI}}$. After a 1 is written, 0 should be written to this bit.	0
5	Bits $\overline{\text{STOPCLK}}$ Active Control 0: Normal 1: Writing a 1 to this bit will assert $\overline{\text{STOPCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{STOPCLK}}$ to be deasserted.	0
4	Bits Software $\overline{\text{STOPCLK}}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{\text{STOPCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{STOPCLK}}$ to be asserted.	0
3	Bits Software $\overline{\text{SLOWCLK}}$ Active Control 0: Normal 1: Writing a 1 will assert $\overline{\text{SLOWCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{SLOWCLK}}$ to be deasserted.	0
2	Bits Software $\overline{\text{SLOWCLK}}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{\text{SLOWCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{SLOWCLK}}$ to be asserted.	0
1	Bits Suspend Timer Control 0: Enable suspend timer (default) 1: Disable suspend timer The 82C597 allows a second Suspend mode to be started after current suspend timer has reached its terminal count (i.e. When the current suspend timer expires, it will assert $\overline{\text{SMI}}$.) Within the $\overline{\text{SMI}}$ subroutine, the suspend timer can be disabled and the suspend timer reenabled. After the new terminal count has been reached, the 82C597 will initiate another $\overline{\text{SMI}}$.	0
0	Bits Disable Software Reset Mask 0: Normal 1: Force 82C597 to activate pin 153. This bit should be set to 1, then set to 0 before leaving the SMI subroutine.	0

Register 65: Power Management Control, Index: 65

Bit	Function	Default
7	Bits 0: Disable $\overline{\text{SMIACT}}$/$\overline{\text{SMADS}}$ input signal 1: Enable $\overline{\text{SMIACT}}$/$\overline{\text{SMADS}}$ input signal	0
6	Bits 0: INTEL SMM mode 1: Cyrix/AMD SMM mode	0
5	Bits 0: Disable quick power-down mode 1: Enable quick power-down mode when power-down key is pushed.	0
4	Reserved, must be 0	0
3:0	Reserved	0000

Register 66: Special Memory and I/O Event Detection, Index; 66

Bit	Function	Default
7:0	Memory cycle: memory address A31, A26, A25, A24, A23, A22, A21, A20 detection. I/O cycle: I/O address A7, A6, A5, A4, A3, A2, A1, A0 detection.	00000000

Register 67: Special Memory and I/O Event Detection, Index: 67

Bit	Memory Cycle	I/O Cycle	Default
7	Mask A31	A15	0
6	Mask A26	A14	0
5	Mask A25	A13	0
4	Mask A24	A12	0
3	Mask A23	A11	0
2	Mask A22	A10	0
1	Mask A21	A9	0
0	Mask A20	A8	0

Register 68: Special Memory and I/O Event Detection, Index: 68

Bit	Function	Default
7	Bits 0: Disable special memory I/O detection 1: Enable special memory I/O detection	0
6	Bits 0: Detect I/O cycle 1: Detect memory cycle	0
5	Bits 0: No write cycle detection 1: Detect write cycles	0
4	Bits 0: No read cycle detection 1: Detect ready cycles	0
3	I/O address A19	0
2	I/O address A18	0
1	I/O address A17	0
0	I/O address A16	0

Registers 66, 67, and 68 allow for special memory or I/O event detection. For memory detection, address A31, A26, A25, A24, A23, A22, A21, and A20 are monitored. Memory detection can also be limited to read cycles or write cycles. Certain memory addresses can also be masked. (Register 67) If the corresponding mask bit (e.g., mask A20) is set, then address (A20) will not be decoded. For I/O detection, addresses A19–A0 can be monitored. I/O detection can also be limited to read-only or write-only. I/O detection does not allow for address masking.

Register 69: Scratch Pad Register, Index: 69

Bit	Function	Default
7:0	This register is readable/writable and can be used by BIOS as a scratch register.	00000000

Register 6A: 82C597 Status Register, Index: 6A

Read Cycle:	Set A	Set B
Bit 7=1	SMI caused by start of stand-by mode	SMI caused by timer 5 reaching its terminal count
Bit 6=1	SMI caused by end of stand-by mode	SMI caused by timer 5 reset by an event
Bit 5=1	SMI caused by suspend timer reaching its terminal count	82C597 is in power-down mode (stand-by or suspend mode)
Bit 4=1	SMI caused by register 64, bit 7	82C597 is in suspend mode. Once in suspend mode, this bit will stay 1 unless any suspend event becomes active, or power-down mode is disabled
Bit 3=1	SMI caused by timer 3 reaching its terminal count	$\overline{\text{STOPCLK}}$ pin is active
Bit 2=1	SMI caused by timer 3 reset by an event	$\overline{\text{SLOWCLK}}$ pin is active
Bit 1=1	SMI caused by timer 4 reaching its terminal count	Suspend timer has reached its terminal count. It will be 0 if register 64, bit 1 is set to 1 later
Bit 0=1	SMI caused by timer 4 reset by an event	$\overline{\text{SMI}}$ pin is active

The CY82C597 has two status registers (16 bits total) that can be read through register 6A. Writing a 0 into bit 7 will cause A status set to be read on a read cycle. Writing a 1 into bit 7 will cause B status set to be read on a read cycle.

Register 6A contains the source of an $\overline{\text{SMI}}$ and some internal status. The status can be used to power-down/power-up individual system devices (monitor, CPU, hard disk, etc.).

Register 6B: DRAM Bank 2/3 Control, Index: 6B

Bit	Function	Default
7	Reserved	0
6:4	Bits 000: Disable Bank 3 001: Bank 3 is 256KB 010: Bank 3 is 1MB 011: Bank 3 is 4MB 100: Reserved 101: Bank 3 is 512KB 110: Bank 3 is 16MB 111: Bank 3 is 2MB	000
3	Bits 0: Disable Bank 2 and 3 1: Enable Bank 2 and 3	0
2:0	Bits 000: Disable Bank 2 001: Bank 2 is 256KB 010: Bank 2 is 1MB 011: Bank 2 is 4MB 100: Reserved 101: Bank 2 is 512KB 110: Bank 2 is 16MB 111: Bank 2 is 2MB	000

Register 6C: DRAM Bank Remap Register, Index: 6C

Bit	Function	Default
7:6	00: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS3}$	11
5:4	00: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS3}$	10
3:2	00: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS3}$	01
1:0	00: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS3}$	00

By allowing any DRAM logical bank to be remapped to any physical bank, DRAM modules can be installed in any empty socket. There are no limitations on the order of DRAM banks.

Register 6D: First Level Write-back (L1WB) CPU Control, Index: 6D

Bit	Function	Default
7	Bits 0: Update inquiry filter on memory read cycles 1: Update inquiry filter on memory read/write cycles	0
6	Bits 0: For 82C597 PCI mode (82C597 and 82C596) 1: For 82C597 VESA mode (82C597, only) and register 6D, Bit (0)=1	0
5	Reserved	0
4	$\overline{HITM}$ detection control 0: Normal 1: Delay $\overline{HITM}$ detection by 1 cycle (for AMD write-back CPUs)	0
3	Reserved, must be 0	0
2	Bits 0: Disable inquiry filter 1: Enable inquiry filter	0
1	Bits 0: Disable CPU bus burst-write support 1: Enable CPU bus burst-write support	0
0	Bits 0: Disable L1WB CPU support logic 1: Enable L1WB CPU support logic	0

Register 6E: Shadow RAM Block D, C Control, Index: 6E

Bit	Function	Default
7	Register 15, Bit 1 control (Block C RAM R/W control): Bits 0: Enable Register 15, Bit 1 1: Disable Register 15, Bit 1 (Replaced by Register 6E, Bit 6)	0
6	Block C RAM enable control (see Bit 7): Bits 0: Read or Write 1: Read only	0
5	Shadow RAM at DC000H–DFFFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
4	Shadow RAM at D8000H–DBFFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
3	Shadow RAM at D4000H–D7FFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
2	Shadow RAM at D0000H–D3FFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
1	Block D RAM access control (D0000H–DFFFFH): Bits 0: Read or Write 1: Read only	0
0	Block D RAM/ROM control: Bits 0: Access RAM. For those disabled RAM, access will go to AT Bus memory. 1: Access on board ROM.	0

Register 6F: Shadow RAM Block E Control, Index: 6F

Bit	Function	Default
7	Block D cachable control Bits 0: Non-cachable 1: Cachable	0
6	Block E cachable control: Bits 0: Non-cachable 1: Cachable	0
5	Shadow RAM at EC000H–EFFFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
4	Shadow RAM at E8000H–EBFFFH control: Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
3	Shadow RAM at E4000H–E7FFFH control: 0: Disable. Will access AT Bus memory 1: Enable.	0
2	Shadow RAM at E000H–E3FFFH control: 0: Disable. Will access AT Bus memory 1: Enable.	0
1	Block E RAM access control (E0000H–EFFFFH): 0: Read or Write 1: Read only	0
0	Block E RAM/ROM control: 0: Access RAM. When RAM is disabled, accesses will go to AT Bus memory. 1: Access on board ROM.	0

Register 70: DRAM and Miscellaneous Control, Index: 70

Bit	Function	Default
7	Bits 0: Normal 1: Enable 2MB DRAM with 11 row address and 10 column address	0
6	Bits 0: Normal 1: Enable 2MB DRAM with 12 row address and 9 column address	0
5	Bits 0: Normal 1: Enable 1MB DRAM with 11 row address and 9 column address	0
4	Bits 0: Normal 1: Enable 1MB DRAM with 12 row address and 8 column address	0
3	Reserved	0
2	Bits 0: Normal 1: Remap address Block 0004XXXX to 000AXXXX, remap address Block 0005XXXX to 000BXXXX.	0
1	Reserved	0
0	Reserved	0

Register 71: Timer 3 Event Detection Control, Index: 71

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 72: Timer 3 Control, Index: 72

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0
3	Bits 0: Disable timer 3 1: Enable timer 3	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (please see registers 60 and 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 73: Timer 4 Event Detection Control, Index: 73

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 74: Timer 4 Control, Index: 74

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0000
3	Bits 0: Disable timer 4 1: Enable timer 4	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (Please see register 60, 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 75: Timer 5 Event Detection Control, Index: 75

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 76: Timer 5 Control, Index: 76

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0000
3	Bits 0: Disable timer 5 1: Enable timer 5	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (Please see register 60, 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 77: Power-Down Control, Index: 77

Bit	Function	Default
7	Bits Timer 5 event control 0: Normal 1: Timer 5 will ignore all events (once enabled, timer 5 will start counting until it reaches the specified terminal count. No events will reset the timer.).	0
6	Bits Timer 4 event control 0: Normal 1: Timer 4 will ignore all events (once enabled, timer 4 will start counting until it reaches the specified terminal count. No events will reset the timer.).	0
5	Bits SMI retry timer 0: Disable SMI retry timer 1: Enable SMI retry timer	0
4:3	Bits SMI retry timer terminal count 00: 55 msec. 01: 0.2 msec 10: 1 sec. 11: 3.5 sec Once the SMI retry timer is enabled and any system management interrupt ($\overline{SMI}$) is active longer than the value specified by $\overline{SMI}$ retry timer, the 82C597 will generate a new $\overline{SMI}$.	00
2	Bits $\overline{STOPCLK}$ timer control 0: Disable $\overline{STOPCLK}$ timer 1: Enable $\overline{STOPCLK}$ timer	0
1:0	Bits $\overline{STOPCLK}$ timer 00: 430 µsec. 01: 860 µsec. 10: 1.7 msec. 11: 7 msec. In software power-down mode, the assertion of $\overline{STOPCLK}$ can be delayed. The delay time is determined by $\overline{STOPCLK}$ timer.	00

Register 78: Non-Cachable/Non-Local Block 1 Starting Address, Index: 78[21, 22, 23]

Bit	Function								Default
7:0	Bits								00000000
	7	6	5	4	3	2	1	0	
	A23	A22	A21	A20	A19	A18	A17	A16	

Notes:
21. Bits 0, 1, 2, 3, 4, and 5 may not be needed. Please see note on Register 79.
22. A24 of the non-cachable/non-local Block 1 starting address is bit 0 of Register 79.
23. A25 and A26 of the non-cachable/non-local Block 1 starting address are bits 6 and 7 of Register 79.

Register 79: Non-Cachable Block 1 Starting Address and Size, Index: 79[24]

Bit	Function	Default
7	Non-cachable/non-local Block 1 starting address A26.	0
6	Non-cachable/non-local Block 1 starting address A25.	0
5	Non-cachable Block 1 dual Functions control: 0: For non-cachable Block 1: For non-local memory Block	0
4	Non-cachable non-local Block 1 control: 0: Disable. 1: Enable.	0
3:1	Non-cachable size Bits 321 Size 000: 64KB 010: 128KB 100: 256KB 110: 512KB 001: 1MB 011: 2MB	000
0	Non-cachable/non-local Block 1 starting address A24.	0

Register 7B: Miscellaneous Control Register, Index: 7B

Bit	Function	Default
7	Reserved	0
6	Reserved	0
5	1: Enable Non-turbo speed set-up 0: Disable Non-turbo speed set-up	0
4	1: Non-turbo speed 0: Normal speed	0
3	1: Disable OSC119 output 0: Enable OSC119 output	0
2	1: Enable 0 ws input 0: Disable 0 ws input	0
1:0	Reserved	00

Register 7C: Reserved, Index: 7C

Bit	Function	Default
7:4	Not implemented	0
3	Reserved	0
2	Reserved, BIOS shall set to 1	0
1	Reserved, BIOS shall set to 1	0
0	Reserved	0

Note:

24. For 64KB non-cachable size, the starting address is bound by A24–A16 from the configuration registers.
For 128KB non-cachable size, the starting address is bound by A24–A17 from the configuration registers.
For 256KB non-cachable size, the starting address is bound by A24–A18 from the configuration registers.
For 512KB non-cachable size, the starting address is bound by A24–A19 from the configuration registers.
For 1MB non-cachable size, the starting address is bound by A24–A20 from the configuration registers.
For 2MB non-cachable size, the starting address is bound by A24–A21 from the configuration registers.

Please note that the non-cachable size is independent of cache size. The non-cachable starting address and non-cachable size are used to define an address range that will not be cached.

When Register 79, bit 4 is set to 1, the non-cachable block will be changed to a non-local block. All addresses within this block will not be on the motherboard, i.e., they will go to the AT bus, VESA bus, or PCI bus.

CY82C597 Pin Descriptions

Clock and Reset

Name	I/O	Pin Number	Description
CLK	I	9	Clock input for internal state machines. A 386 system needs a 2x clock, a 486 system needs a 1x clock.
ATCLK	O	148	Clock signal to the AT bus. Frequency is controlled by register 10, bit [0:1].
OSC	I	133	This input should be connected to a 14.318 MHz oscillator. It is used to generate OSC119.
OSC119	O	151	14.318 MHz divided by 12 output (1.19 MHz). This signal should be connected to the timer clock input (TMRCLK) of the 83C206.
PWRGD	I	128	Power good signal from the power supply or reset key. When LOW, it will activate CPURST, $\overline{\text{SYSRST}}$, and 387 reset ($\overline{\text{NPRLD}}$).
CPURST	O	14	This is an active HIGH signal to reset the CPU. When PWRGD is LOW, keyboard reset is active, or there is a shutdown, CPURST will be activated.
$\overline{\text{SYSRST}}$	O	129	This is an active LOW signal. It is asserted when PWRGD is LOW. This signal is used to reset all ISA peripheral cards.
A26/$\overline{\text{AEN16}}$	I/O	80	This is the CPU A26 input signal during CPU cycles and the $\overline{\text{AEN16}}$ input signal during DMA cycles.

Numerical Coprocessor Interface

Name	I/O	Pin Number	Description
$\overline{\text{NPRDYLC}}$	I	8	A dual function pin. During numerical coprocessor cycles, it is the numerical processor ready input ($\overline{\text{NPRDY}}$). During local bus cycles, it is the local bus device input ($\overline{\text{LOCAL}}$). Each $\overline{\text{LDEV}}$ signal from the VESA slots should be ANDed together to provide $\overline{\text{LOCAL}}$. The $\overline{\text{NPRDY}}$ and $\overline{\text{LOCAL}}$ should be ANDed externally and connected to this pin.
B387NS4/MA11	I	7	A dual function pin that is latched by the rising edge of PWRGD. For a 386 system, this pin should be tied HIGH through a 10KΩ resistor. After the power-up sequence, this pin operates as the $\overline{\text{BUSY387}}$, a signal from the 387 numerical coprocessor that indicates the 387 is still performing an operation. For a 486 system, this pin should be tied to Ground (V_{SS}) through a 1KΩ resistor. After power-up, this pin becomes the MA11 output.
$\overline{\text{B3IG}}$	O	12	A dual function pin. For 486 systems, it is an output ($\overline{\text{IGNNE}}$) to tell the 486 to ignore numerical errors and continue executing non-control floating point instructions. For 386 systems, it is an output ($\overline{\text{BUSY386}}$) that tells the 386 that the 387 is still busy.
$\overline{\text{E387FER}}$	I	13	A dual function pin. For 486 systems, it is an input ($\overline{\text{FERR}}$) from the 486 that indicates that there is a floating point error. For 386 systems, it is an input ($\overline{\text{ERR387}}$) that indicates that a 387 error has occurred.
INT13	O	131	Numerical coprocessor interrupt request to the 83C206.

CPU Control

Name	I/O	Pin Number	Description
A31	I	32	CPU address line 31.
A[24:21]	I	33–36	CPU address lines [24:21].
A20	I/O	37	CPU address line 20. Output during DMA/MASTER cycles for 386 systems.
A19	I	38	CPU address line 19.
A18	I	49	CPU address line 18.
A17	I	51	CPU address line 17.
A[16:2]	I/O	52–66	CPU address lines [16:2]. Outputs during DMA/MASTER cycles.
BE[3:0]	I/O	28–31	Byte enable [3:0]. Inputs during CPU cycles. Outputs during DMA/MASTER.
$\overline{ADS}$	I/O	27	CPU address strobe. Output during DMA/MASTER accesses on the VESA local bus.
$\overline{MIO}$	I/O	23	CPU memory I/O cycle status. Output during DMA/MASTER accesses on the VESA local bus cycles.
$\overline{DC}$/ADSTB	I	22	This pin is the CPU data/code status input during CPU cycles and the ADSTB signal during DMA cycles.
$\overline{WR}$	I/O	24	CPU write/read status. Output during DMA/MASTER accesses on VESA local bus.
$\overline{CPURDY}$	I/O	18	Ready output to terminate CPU cycle. During local bus/numerical processor cycles, the CY82C597 monitors this signal to see when the cycle has ended.
D[31:18]	I/O	86–99	CPU data bus for read/write data.
D[17:16]	I/O	102–103	CPU data bus for read/write data.
CQ[15:10]	I/O	48–43	Contaq bus or CQ bus [15:10]. The CQ bus sits between the CPU data bus and the AT SD bus. Used also as TAGA[7:2].
CQ[9:8]	I/O	40–39	CQ bus [9:8]. Used also as TAGA[1:0].
CQ[7:3]	I/O	75–79	CQ bus [7:3].
CQ[2:0]	I/O	83–85	CQ bus [2:0].
NMI	O	11	Non-maskable interrupt output to the CPU. When active, it indicates the CY82C597 has detected either a local memory or AT memory parity error.

Bus Arbitration

Name	I/O	Pin Number	Description
DMAHRQ	I	135	DMA hold request from the 83C206.
HOLD	O	16	Hold request to the CPU. Hold goes active due to a refresh request or a de-turbo request.
HLDA	I	25	Hold acknowledge from the CPU.
HLDAOUT	O	132	DMA/MASTER cycle hold acknowledge output to the 83C206. After receiving this signal, the DMA/MASTER can begin its cycle.
$\overline{REFSH}$	I/O	154	$\overline{REFRESH}$, an active LOW signal. An output to the AT bus during non-master cycles. An input during MASTER cycles.

DRAM Control

Name	I/O	Pin Number	Description
$\overline{\text{DWROMKB}}$	O	115	A dual function pin. In the 82C597 PCI mode, this signal is the $\overline{\text{DWE}}$ (DRAM write enable) during DRAM write cycles and the $\overline{\text{ROMCS}}$ (ROM chip select) signal during ROM access cycles. When the 82C597 is used without a CY82C599 present in the system, this signal is used as $\overline{\text{DWE}}$, $\overline{\text{ROMCS}}$, and $\overline{\text{KBCS}}$ (keyboard controller chip select) during keyboard controller accesses.
$\overline{\text{RAS[1:0]}}$	O	108–109	DRAM bank 1,0 row address strobe.
$\overline{\text{CAS0}}$	O	110	DRAM bank 0,1 column address strobe 0.
$\overline{\text{CAS1}}$	O	111	DRAM bank 0,1 column address strobe 1.
$\overline{\text{CAS2}}$	O	113	DRAM bank 0,1 column address strobe 2.
$\overline{\text{CAS3}}$	O	114	DRAM bank 0,1 column address strobe 3.
MA10	I/O	116	DRAM address line 10. When this pin is pulled down through a 1KΩ resistor, CY82C597 will use MP[3:0] as VESA Bus Master arbitration signals. This pin is an input only during system reset.
MA9	I/O	117	DRAM address line 9. This pin must be pulled down through a 1KΩ resistor for 128-MB of DRAM.
MA8	I/O	118	DRAM address line 8.
MA[7:6]	O	119–120	During power on, tying MA[7:6] HIGH or LOW through pull-up/pull-down resistors sets different internal 82C597 modes according to the following table: MA7 MA6 0 0 82C597 stand-alone. 0 1 82C597 PCI mode (in conjunctions with an 82C599). 1 X 82C596 emulation mode. During normal operation, MA[7:6] are used as DRAM address lines [7:6]. When the CY82C597 is configured for 596 mode, it can support 2 banks of DRAM up to 128 MB total. Please see the CY82C596 spec for 596 mode configuration.
MA5	I/O	122	DRAM address bit 5.
MA4/TOUT2	I/O	123	DRAM address line 4. In 597 mode, this pin is also used as the TOUT2 input signal during AT cycles.
MA3/$\overline{\text{IOCS16}}$	I/O	124	DRAM address line 3. In 597 mode, this pin is also used as the $\overline{\text{IOCS16}}$ input signal during AT cycles.
MA2/$\overline{\text{MCS16}}$	I/O	125	DRAM address line 2. In 597 mode, this pin is also used as the $\overline{\text{MCS16}}$ input signal during AT cycles.
MA1/RTCAS	I/O	126	DRAM address line 1. In 597 mode, this pin is also used as the RTCAS input signal during AT cycles.
MA0/$\overline{\text{INTA}}$	I/O	127	DRAM address line 0. In 597 mode, this pin is also used as the $\overline{\text{INTA}}$ input signal during AT cycles.
MP[3:0]	I/O	104–107	DRAM parity bits [3:0]. During DRAM read cycles, they are inputs. The CY82C597 will generate byte parity bits from D[31:0] and compare them with MP[3:0]. If a mismatch occurs and NMI reporting is enabled, the CY82C597 will generate an NMI to the CPU. During DRAM write cycles, the CY82C597 will generate byte parity bits from D[31:0] and put them on MP[3:0] and write them into the DRAM. When register 10, bit 6=1 and MA10 is pulled down through a 1KΩ resistor, these 4 signals are used as VESA bus master arbitration signals: MP0 =VESA bus master 2 request to CY82C597 MP1 =VESA bus master 1 request to CY82C597 MP2 = VESA bus master 2 grant from CY82C597 MP3 = VESA bus master 1 grant from CY82C597 If parity and VESA bus master capability are both required, an external PAL is needed to handle the VESA arbitration.

DRAM Control (continued)

Name	I/O	Pin Number	Description
$\overline{\text{L1MCS}}$	O	152	Indicates the current address is below 1 MB.

Cache Control

Name	I/O	Pin Number	Description
$\overline{\text{CRD0}}$	O	67	Cache read for the even bank of SRAMs. Connected to $\overline{\text{OE}}$ of Bank 0 cache data SRAMs.
$\overline{\text{CRD1}}$	O	68	Cache read for the odd bank of SRAMs. Connected to $\overline{\text{OE}}$ of Bank 1 cache data SRAMs.
$\overline{\text{CWE0}}$	O	71	Cache write enable for the even bank of SRAMs.
$\overline{\text{CWE1}}$	O	72	Cache write enable for the odd bank of SRAMs.
TOGA2	O	73	A dual function pin. For 386 systems, it is used to toggle CPU address A2 during cache accesses. For 486 systems with 1 bank of SRAMs, it is address 2 to bank 0. For 486 systems with 2 banks of SRAMs, it is address 3 input to bank 0.
TOGA3	O	74	A dual function pin. For 386 systems, it is used to toggle CPU address A3 during cache accesses. For 486 systems with 1 bank of SRAM, it is address 3 to bank 0. For 486 systems with 2 banks of SRAMs, it is address 3 input to bank 1.
$\overline{\text{TAGWT}}$	O	42	Tag RAM write enable, active LOW. It is active during a cache write hit or cache move in cycle.
$\overline{\text{TAGEN}}$	O	41	An active LOW signal. When active, it will enable the CY82C597 to read/write the Tag RAM.
$\overline{\text{XA20EA}}$	I/O	10	This is a dual function pin. For 486 systems, it is $\overline{\text{EADS}}$ to invalidate a 486 internal cache line. It is active during DMA/MASTER memory write hit cycles. For 386 systems, the CPU is from CYRIX, this pin is the $\overline{\text{EADS}}$ output to invalidate the CPU's cache line during DMA/MASTER memory write cycles. If Intel or AMD, this pin the SA20 output or input for DMA/MASTER cycles.
A25/$\overline{\text{AEN8}}$	I/O	15	This is the CPU A25 input signal during CPU cycles and the $\overline{\text{AEN8}}$ input signal during DMA cycles.
$\overline{\text{KEN}}$	O	17	$\overline{\text{KEN}}$ to the 486 to indicate that the cycle is cachable. It can also be connected to C&T 38605 and CYRIX CPU $\overline{\text{KEN}}$ pins making an external PAL unnecessary.
$\overline{\text{RQ3BRDY}}$	I/O	19	A dual function pin. For 486 systems, it is an I/O pin, $\overline{\text{BRDY}}$. During VESA local cycles, it is an input that monitors $\overline{\text{BRDY}}$ from the local device and determines when the cycle has terminated. During local memory cycles, it is an output that terminates the burst transfer. For 386 systems, it is an output connected to PEREQ of the 386.
RQ387BL	I	26	A dual function pin. For 486 systems, it is an input signal ($\overline{\text{BLAST}}$) from the 486. When active, it tells the CY82C597 that the next cycle will be the last burst cycle. For 386 systems, it is an input from the 387 (PRQ387) that requests a data operand to be transferred to/from memory by the 386.

AT Control

Name	I/O	Pin Number	Description
XA0	I/O	144	System address line 0. It is an input during MASTER and 8 bit DMA cycles, otherwise it is an output.
XA1	I/O	145	System address line 1. It is an input during DMA/MASTER cycles, otherwise it is an output.
$\overline{\text{MEMR}}$	I/O	141	AT memory read command. It is an input during DMA/MASTER cycles, otherwise it is an output.
$\overline{\text{MEMW}}$	I/O	140	AT memory write command. It is an input during DMA/MASTER cycles, otherwise it is an output.

AT Control (continued)

Name	I/O	Pin Number	Description
$\overline{IOR}$	I/O	142	AT I/O read command. It is an input during DMA/MASTER cycles, otherwise it is an output.
$\overline{IOW}$	I/O	143	AT I/O write command. It is an input during DMA/MASTER cycles, otherwise it is an output.
ALE	O	158	AT bus address latch enable. Indicates the start of an AT bus cycle.
$\overline{IOCS16}$/LRDY	I	1	In 597 mode, this is the ready input signal from the local bus. In 597 PCI mode, this is the signal from the AT bus to indicate a 16-bit AT I/O cycle.
$\overline{MCS16}$/INTR	I	160	In 597 mode, this is the interrupt request signal for the 83C206. In 597 PCI mode, this is the signal from the AT bus to indicate a 16-bit AT memory cycle.
$\overline{0WS}$/$\overline{HITM}$	I	155	This pin is the $\overline{HITM}$ input signal when the CY82C597 interfaces to a CPU that has a level 1, write-back cache. Otherwise, it is the AT bus 0WS (zero wait states) input signal.
$\overline{XBHE}$	I/O	159	AT bus byte high indicator. It is an input during DMA/MASTER cycles, otherwise it is an output.
IOCHRDY	I/O	136	AT bus I/O channel ready input. It is an output during numerical coprocessor reset.
$\overline{IOCHCK}$	I	153	AT bus I/O channel parity check. When active, it indicates that AT memory has a parity error.
$\overline{INTA}$/$\overline{STOPCLK}$	O	146	In 597 mode, this is the $\overline{STOPCLK}$ signal to CPU. In 597 PCI mode, this is the interrupt acknowledge pulse to the interrupt controller in the 83C206.
TOUT2/$\overline{SLOWCLK}$	I/O	147	In 597 mode, this is the $\overline{SLOWCLK}$ output signal. In 597 PCI mode, this is an input from the 83C206 timer 2 output that is used to generate a speaker tone.
TMGATE	O	149	Timer 2 gate control. It is used to enable /disable the tone to the speaker.
RTCAS/$\overline{SMI}$	I/O	134	In 597 mode, this is the system management interrupt signal. In 597 PCI mode, this is the real-time clock address strobe connected to the 83C206.
$\overline{KBCS}$/$\overline{ATCYC}$	O	156	In 597 stand-alone mode, this is an output signal that indicates that a cycle is bound for the AT bus. In 597 PCI mode, this is the keyboard controller chip select signal when an access is targeted for the keyboard controller.
SPKOUT	O	157	Output to speaker.
$\overline{SMIACT}$/$\overline{SMADS}$	I	137	This signal indicates that the processor is operating in system management mode (SMM) when the CY82C597 is interfaced to an Intel CPU. It is the SMI address strobe input signal when using a Cyrix or AMD CPU.
$\overline{RAS2}$	I/O	139	DRAM bank 2 row address strobe.
$\overline{RAS3}$	I/O	138	DRAM bank 3 row address strobe.
$\overline{SDEN}$	O	5	An active LOW system data bus enable to turn on/off bidirectional buffers between SD[15:0] and CQ [15:0] bus.
SDIR0N4F	I/O	4	A dual function pin. During 486 power-on reset, if this pin is pulled HIGH by a 51KΩ resistor, ATCLK will be CLK divided by 4/6/8/5 according to register 10, bit 1,0. If this pin is pulled LOW during power-on reset, ATCLK will be changed to CLK divided by 2/3/4/2.5. After power-on reset, this pin becomes SDIR0, which is used to control the LOW byte bus direction: SDIR0=0: for SD[7:0] to CQ[7:0] transfer. SDIR0=1: for CQ[7:0] to SD[7:0] transfer.
SDIR1NCM	I/O	6	A dual function pin. During 386 power-on reset, if this pin is pulled HIGH by 51KΩ resistor, the CY82C597 will know that the CPU manufacturer is Intel or AMD. If this pin is pulled LOW during power-on reset, the CY82C597 will recognize the CPU manufacturer as C&T or CYRIX. After power-on reset, this pin becomes SDIR1, which is used to control the HIGH byte bus direction. SDIR1=0: for SD[15:8] to CQ[15:8] transfer. SDIR1=1: for CQ[15:8] to SD[15:8] transfer.

AT Control (continued)

Name	I/O	Pin Number	Description
$\overline{LDBE}$	O	82	An active LOW system data bus enable signal to turn on/off the bidirectional buffer between D[15:0] bus and CQ[15:0] bus.
SMIMASK/$\overline{LDIR}$	I/O	112	In 597 mode, this pin is an output that controls the Data bus to CQ bus buffer direction. In 597 PCI mode, this pin is an input that masks out SMI generation during the reset period.

Ground and V_{CC}

Name	I/O	Pin Number	Description
GND	I	3, 21, 50, 70, 81, 101, 130, and 150	Ground
V_{CC}	I	2, 20, 69, 100, and 121	+5V

CY82C597 DC Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... +6.5 V

Ambient Operating Temperature ..... −25°C to +70°C

Ambient Storage Temperature ..... −40°C to 125°C

DC Voltage Applied to Outputs ..... −0.5V to +5.5V

DC Input Voltage ..... −0.5V to +5.5V

Electrical Characteristics Over the Operating Range (0°C to 70°C, V_{CC} = +5V ± 5%)

Parameter	Description		CY82C597 Min.	CY82C597 Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{OL}	Output LOW Voltage			0.4	V
V_{OH}	Output HIGH Voltage		2.4		V
I_{IL}	Input Leakage Current			10	µA
I_{OZ}	Three-state Leakage Current			10	µA
C_{IN}	Input Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
I_{CC}	Power Supply Current	33 MHz		150	mA
		50 MHz		200	mA

Switching Characteristics

Parameter	Description	CY82C597 Min.	CY82C597 Max.	Unit
CLOCK RESET AND TIMING				
T_{100}	CLK period	20		ns
T_{101}	CLK HIGH time at 2.0V	7		ns
T_{102}	CLK LOW time at 0.8V	7		ns
T_{103}	CLK rise time		2	ns
T_{104}	CLK fall time		2	ns
T_{105}	CPURST active delay from CLK	5	15	ns
T_{106}	CPURST inactive delay from CLK	5	15	ns
T_{107}	NPRST active delay from CLK	5	15	ns
T_{108}	NPRST inactive delay from CLK	5	15	ns
AT/DMA ARBITRATION/REFRESH TIMING				
T_{110}	$\overline{ADS}$ set-up time to CLK	5		ns
T_{111}	$\overline{CPURDY}$ active delay from CLK HIGH	5	16	ns
T_{112}	$\overline{CPURDY}$ inactive delay from CLK HIGH	5	14	ns
T_{113}	HOLD active delay from CLK HIGH	5	15	ns
T_{114}	HOLD inactive delay from CLK HIGH	5	15	ns
T_{115}	HLDAOUT active delay from HLDA HIGH	5	20	ns
T_{116}	HLDAOUT inactive delay from HLDA HIGH	5	20	ns
T_{117}	$\overline{REFSH}$ active delay from HLDA HIGH	5	20	ns
T_{118}	$\overline{REFSH}$ inactive delay from ATCLK HIGH	5	20	ns
T_{119}	$\overline{MEMR}$ active delay from ATCLK HIGH	5	20	ns
T_{120}	$\overline{MEMR}$ inactive delay from ATCLK LOW	5	20	ns
T_{121}	$\overline{RAS0}$ to $\overline{RAS1}$ active delay	5	10	ns
T_{122}	$\overline{RAS0}$ to $\overline{RAS1}$ inactive delay	5	10	ns
T_{123}	$\overline{MEMR}$ inactive delay from ATCLK HIGH	5	20	ns
CACHE/DRAM TIMING				
T_{306}	CLK LOW to $\overline{CWE}$ active delay	4	14	ns
T_{307}	CLK HIGH to $\overline{CWE}$ inactive delay	4	14	ns
T_{307A}	CLK LOW to $\overline{CWE}$ inactive delay	4	14	ns
T_{308}	CLK LOW to $\overline{TAGWT}$ active delay	4	14	ns
T_{309}	CLK HIGH to $\overline{TAGWT}$ inactive delay	5	16	ns
T_{310}	CLK HIGH to $\overline{TAGEN}$ active delay	4	14	ns
T_{311}	CLK HIGH to $\overline{TAGEN}$ inactive delay	5	16	ns
T_{312}	CLK LOW to $\overline{CPURDY}$ active delay	4	12	ns
T_{313}	CLK HIGH to $\overline{CPURDY}$ inactive delay	7	16	ns
T_{314}	CLK HIGH to $\overline{CPURDY}$ active delay	5	15	ns
T_{315}	CLK LOW to $\overline{TAGWT}$ inactive delay	5	16	ns
T_{316}	$\overline{BLAST}$ set-up to CLK HIGH	7		ns

Switching Characteristics (continued)

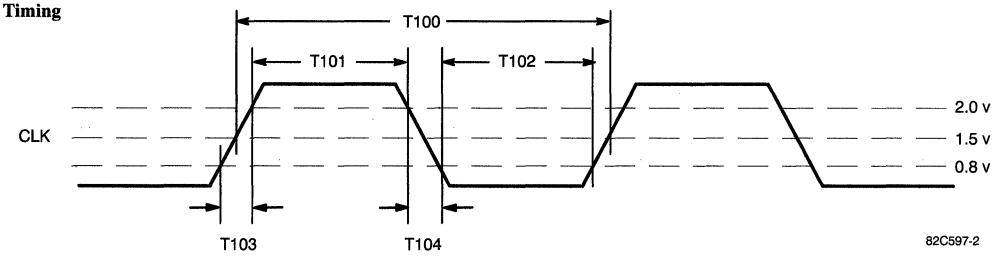
Parameter	Description	CY82C597		Unit
		Min.	Max.	
T_{320}	TAGA[7:0] set-up time to CLK LOW	15		ns
T_{321}	$\overline{CRD}$ active delay from CLK HIGH	5	15	ns
T_{322}	$\overline{CRD}$ inactive delay from CLK HIGH	6	13	ns
T_{323}	TOGA2/TOGA3 delay from CLK HIGH	3	15	ns
T_{324}	$\overline{BRDY}$ active delay from CLK LOW	4	15	ns
T_{325}	$\overline{BRDY}$ inactive delay from CLK HIGH	4	13	ns
T_{330}	CLK HIGH to $\overline{DWROMKB}$ active delay	5	18	ns
T_{331}	CLK HIGH to $\overline{DWROMKB}$ inactive delay	4	14	ns
T_{332}	CLK LOW to $\overline{CAS}$ active delay	6	18	ns
T_{333}	CLK LOW to $\overline{CAS}$ inactive delay	4	15	ns
T_{334}	CLK HIGH to $\overline{CAS}$ active delay	6	18	ns
T_{335}	CLK HIGH to $\overline{CAS}$ inactive delay	4	17	ns
T_{336}	A[31:2] to MA[10:0] delay	5	18	ns
T_{337}	CLK HIGH to $\overline{RAS}$ inactive delay	5	20	ns
T_{338}	CLK HIGH to $\overline{RAS}$ active delay	5	18	ns
T_{339}	CLK HIGH to MA[10:0] delay	5	18	ns
T_{340}	CLK HIGH to $\overline{CRD}$ active delay	4	15	ns
T_{341}	CLK LOW to $\overline{CRD}$ inactive delay	4	13	ns
T_{342}	A[31:3] to TOGA2/TOGA3 delay	5	16	ns
T_{343}	CLK HIGH to TOGA2/TOGA3 valid delay	5	16	ns
T_{344}	CLK HIGH to $\overline{CPURDY}$ active delay	4	16	ns
T_{345}	CLK HIGH to $\overline{CPURDY}$ inactive delay	4	14	ns
T_{346}	CLK LOW to $\overline{TAGWT}$ active delay	4	14	ns
T_{347}	CLK LOW to $\overline{TAGWT}$ inactive delay	4	14	ns
T_{348}	CLK LOW to $\overline{CWE}$ active delay	5	15	ns
T_{349}	CLK LOW to $\overline{CWE}$ inactive	4	13	ns
T_{350}	CLK LOW to $\overline{TAGEN}$ active		18	ns
T_{351}	CLK LOW to CQ[15:8]		18	ns
DMA/MASTER TIMING				
T_{360}	COMMAND active to $\overline{RAS}$ active delay	9	25	ns
T_{361}	COMMAND inactive to $\overline{RAS}$ inactive	9	25	ns
T_{362}	CLK HIGH to MA[10:0] delay	5	18	ns
T_{363}	CLK HIGH to $\overline{CAS}$ active delay	5	20	ns
T_{364}	COMMAND inactive to $\overline{CAS}$ inactive delay	5	22	ns
T_{365}	COMMAND active $\overline{CRD}$ active delay	5	16	ns
T_{366}	COMMAND inactive to $\overline{CRD}$ inactive delay	6	18	ns
T_{367}	COMMAND active to $\overline{DWROMKB}$ active delay	5	20	ns
T_{368}	COMMAND inactive to $\overline{DWROMKB}$ inactive	5	18	ns

Switching Characteristics (continued)

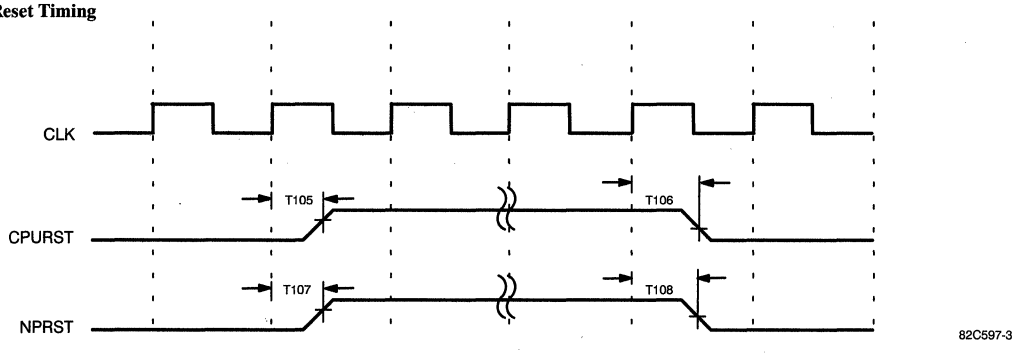
Parameter	Description	CY82C597		Unit
		Min.	Max.	
T_{369}	CLK HIGH to $\overline{CWE}$ active delay	5	19	ns
T_{370}	CLK HIGH to $\overline{CWE}$ inactive delay	5	19	ns
T_{371}	HLDA to $\overline{RAS}$ inactive delay	9	30	ns
DATA CONVERSION TIMING				
T_{400}	CQ[15:0] valid from D[31:0]	5	18	ns
T_{401}	CQ[15:0] hold time to D[31:0]	5	18	ns
T_{406}	D[31:0] valid from CQ[15:0]	5	18	ns
T_{407}	D[31:0] hold time to CQ[15:0]	5	18	ns
NUMERICAL COPROCESSOR TIMING				
T_{500}	IRQ asserted from $\overline{FERR}$ LOW	4	14	ns
T_{501}	IRQ deasserted from CNTL HIGH	4	12	ns
T_{502}	IRQ asserted from WTINTR HIGH	4	14	ns
T_{503}	IRQ deasserted from WTINTR LOW	4	12	ns
T_{504}	$\overline{IGNNE}$ asserted from CNTL HIGH	4	14	ns
T_{505}	$\overline{IGNNE}$ deasserted from $\overline{FERR}$ HIGH	3	12	ns
POWER MANAGEMENT TIMING				
T_{601}	$\overline{SMI}$ delay from CLK HIGH	8	15	ns
T_{602}	$\overline{SMIACT}$ setup to CLK HIGH	5		ns
T_{603}	$\overline{SLOWCLK}$ delay from CLK HIGH	8	15	ns
T_{604}	$\overline{STOPCLK}$ delay from CLK HIGH	8	15	ns

Switching Waveforms

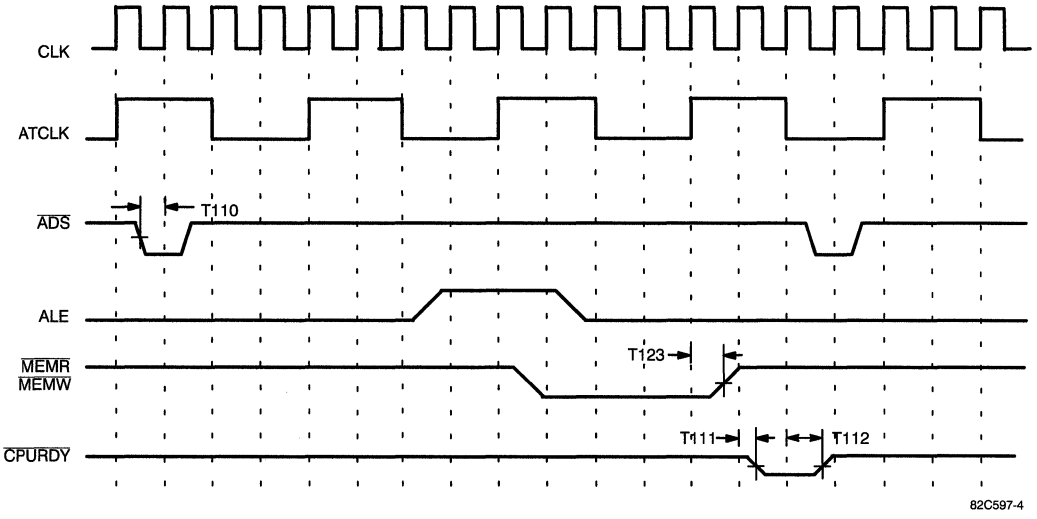
Clock Timing



Reset Timing

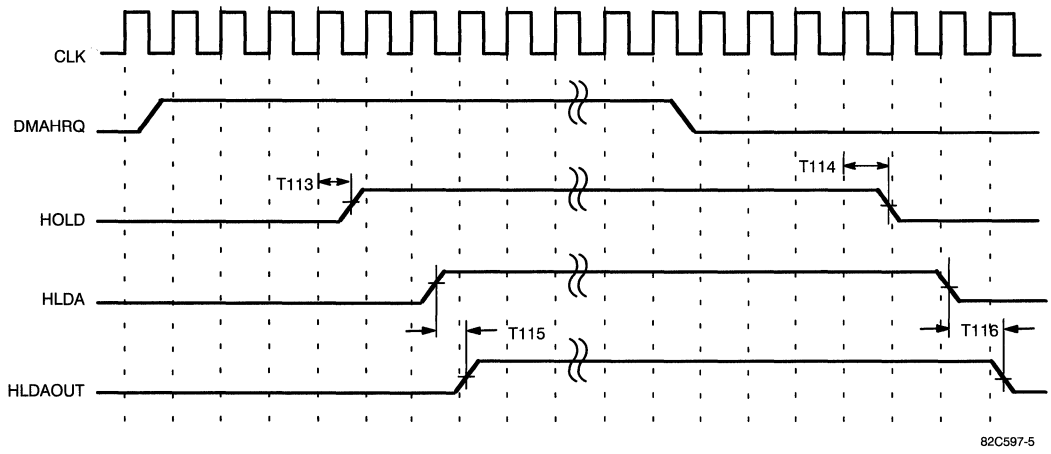


AT Cycle Timing

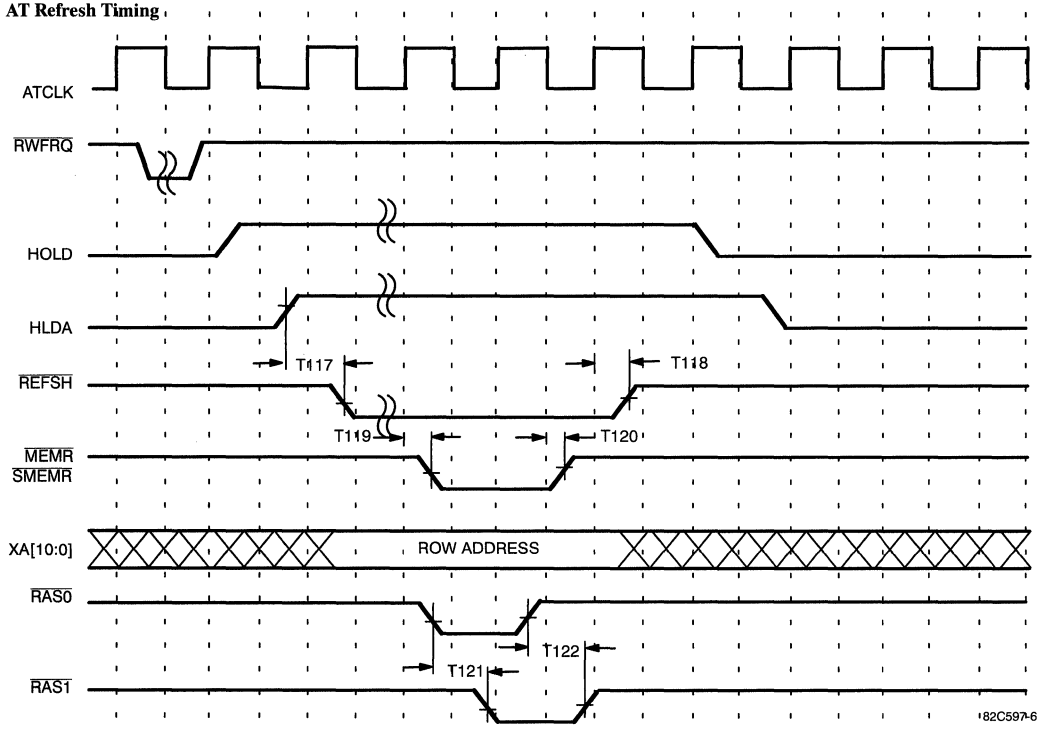


Switching Waveforms (continued)

DMA Arbitration Timing

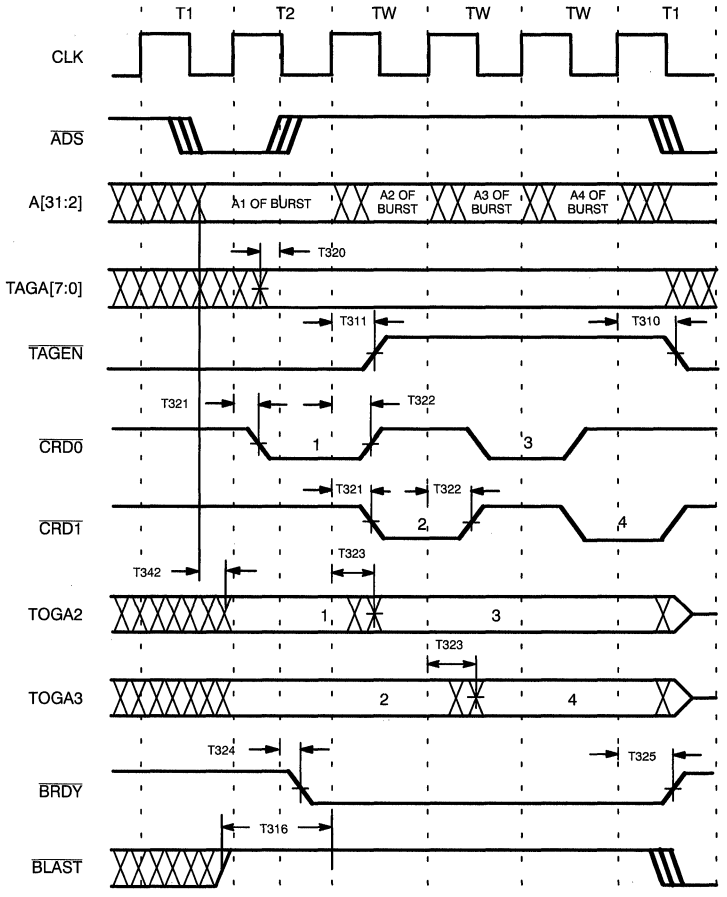


AT Refresh Timing



Switching Waveforms (continued)

486 Cache Read Hit (2-1-1-1 Burst Mode), 2 Banks of Cache, Interleaved



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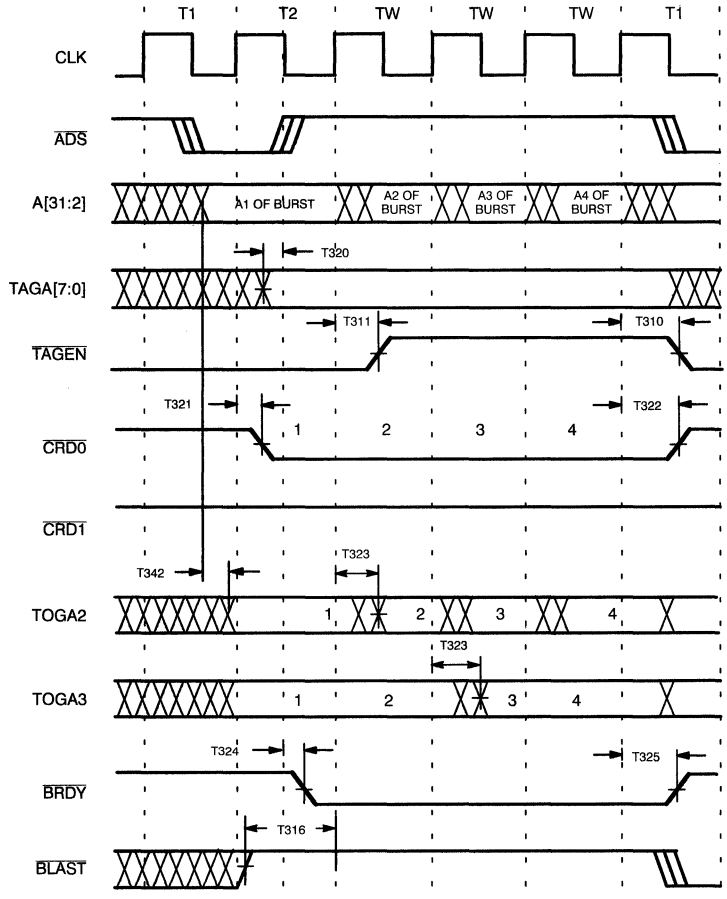
Switching Waveforms (continued)

486 Cache Read Hit (2-1-1-1 Burst Mode), 1 Bank of Cache



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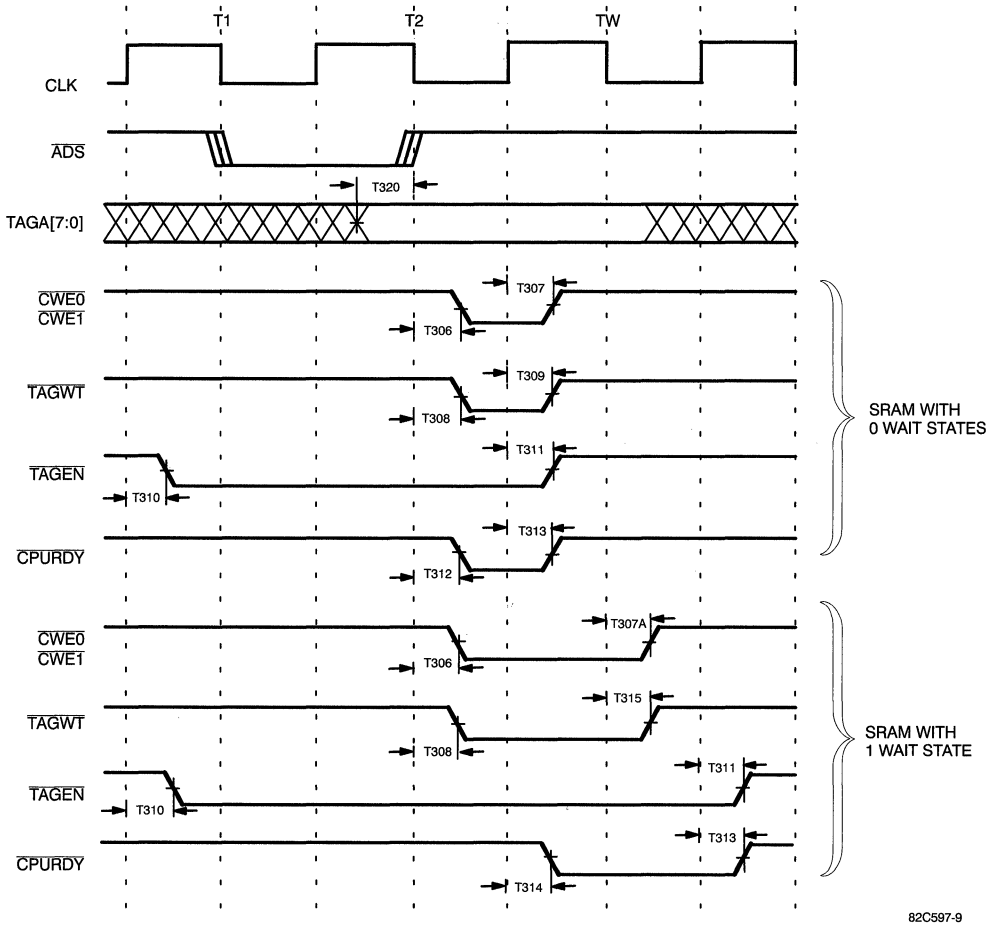
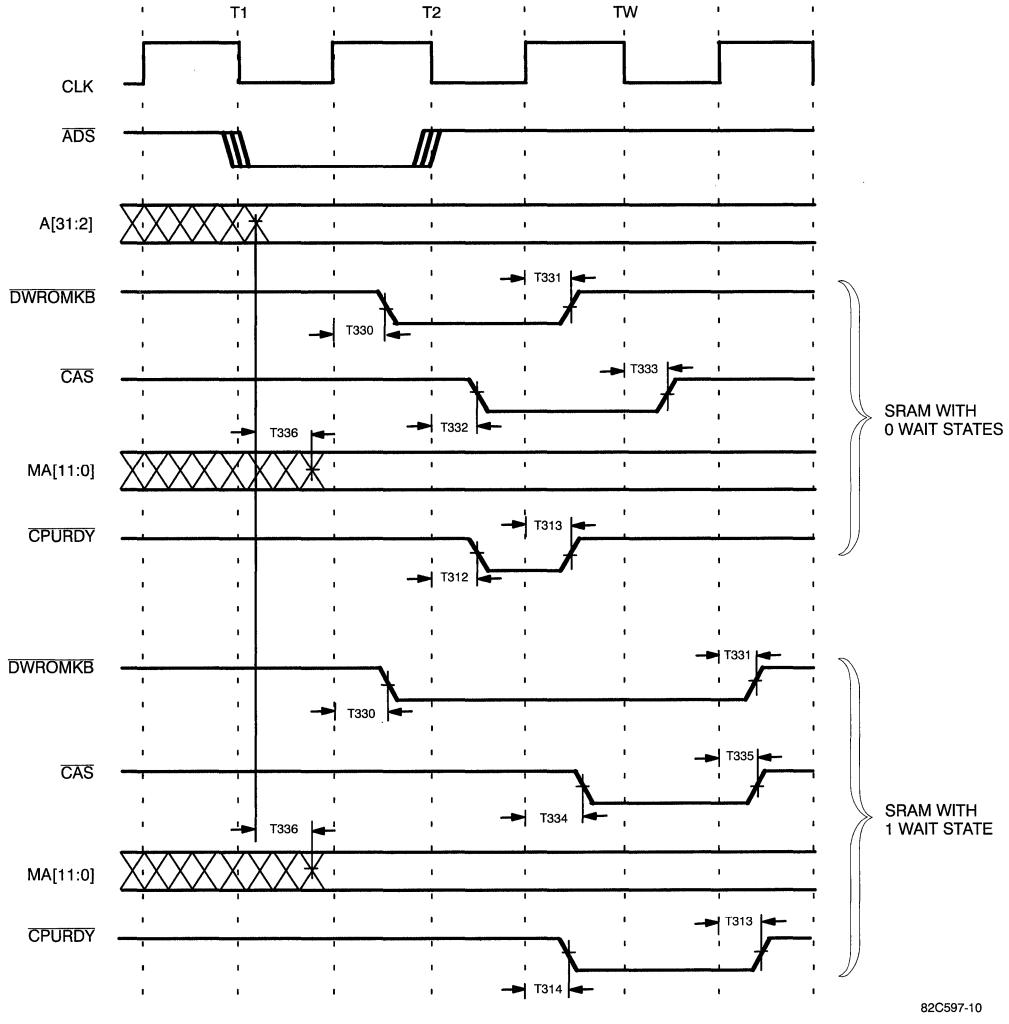
Switching Waveforms (continued)

Cache Write Hit Cycle (Write-Back)



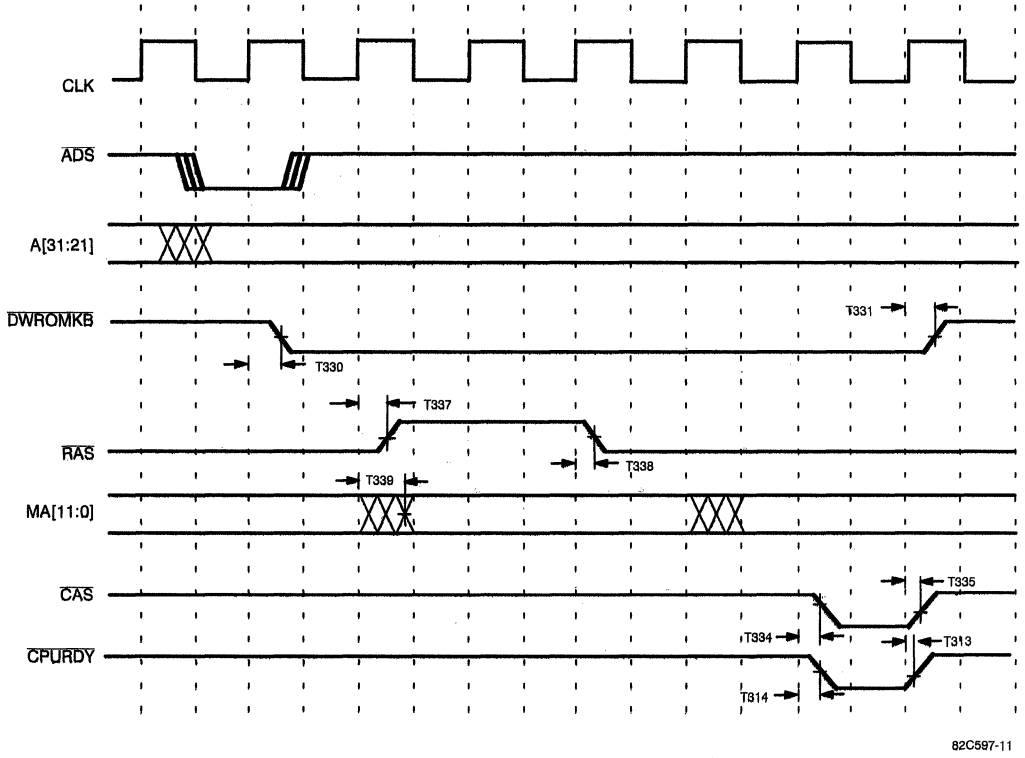
Switching Waveforms (continued)

Cache Write Miss, Page Hit Cycle



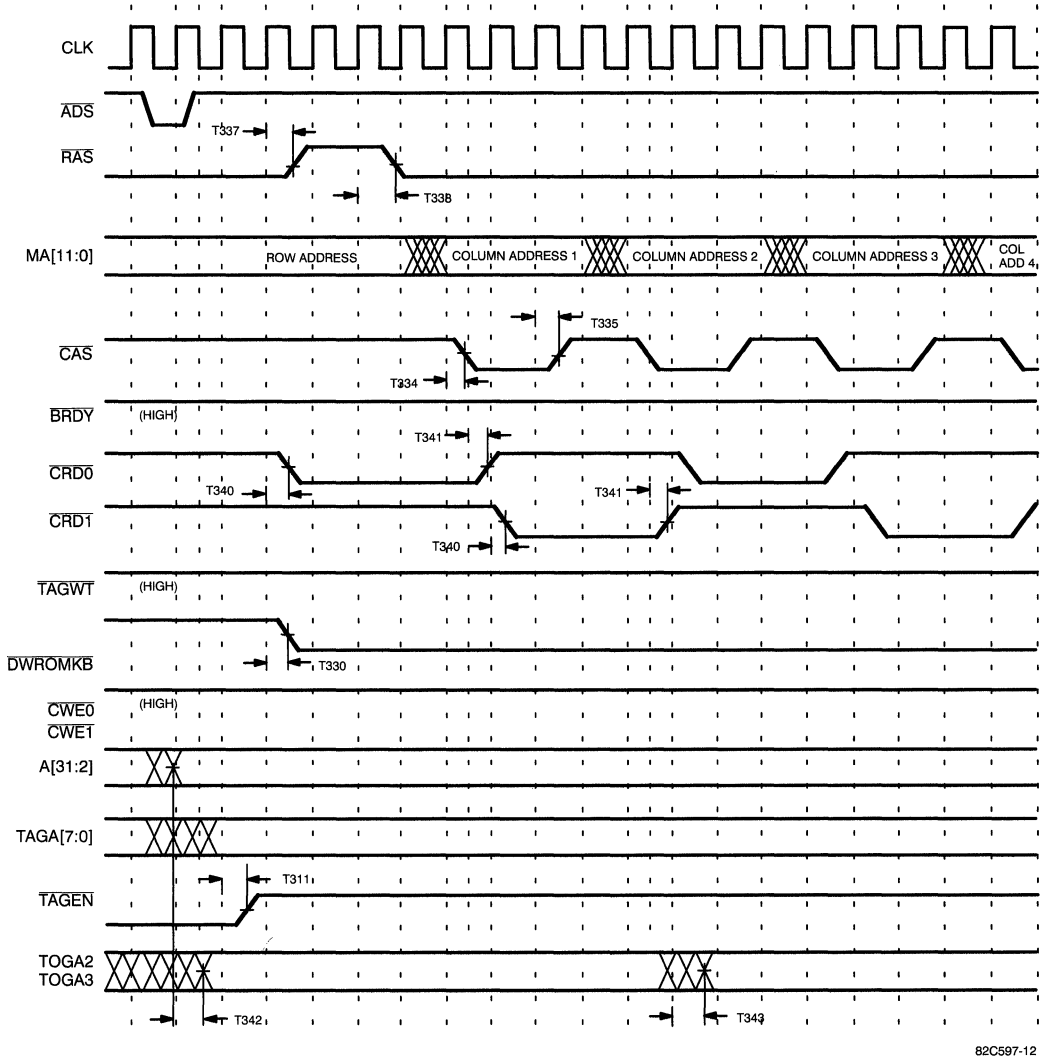
Switching Waveforms (continued)

Cache Write Miss, Page Miss Cycle



Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 1 of 3)



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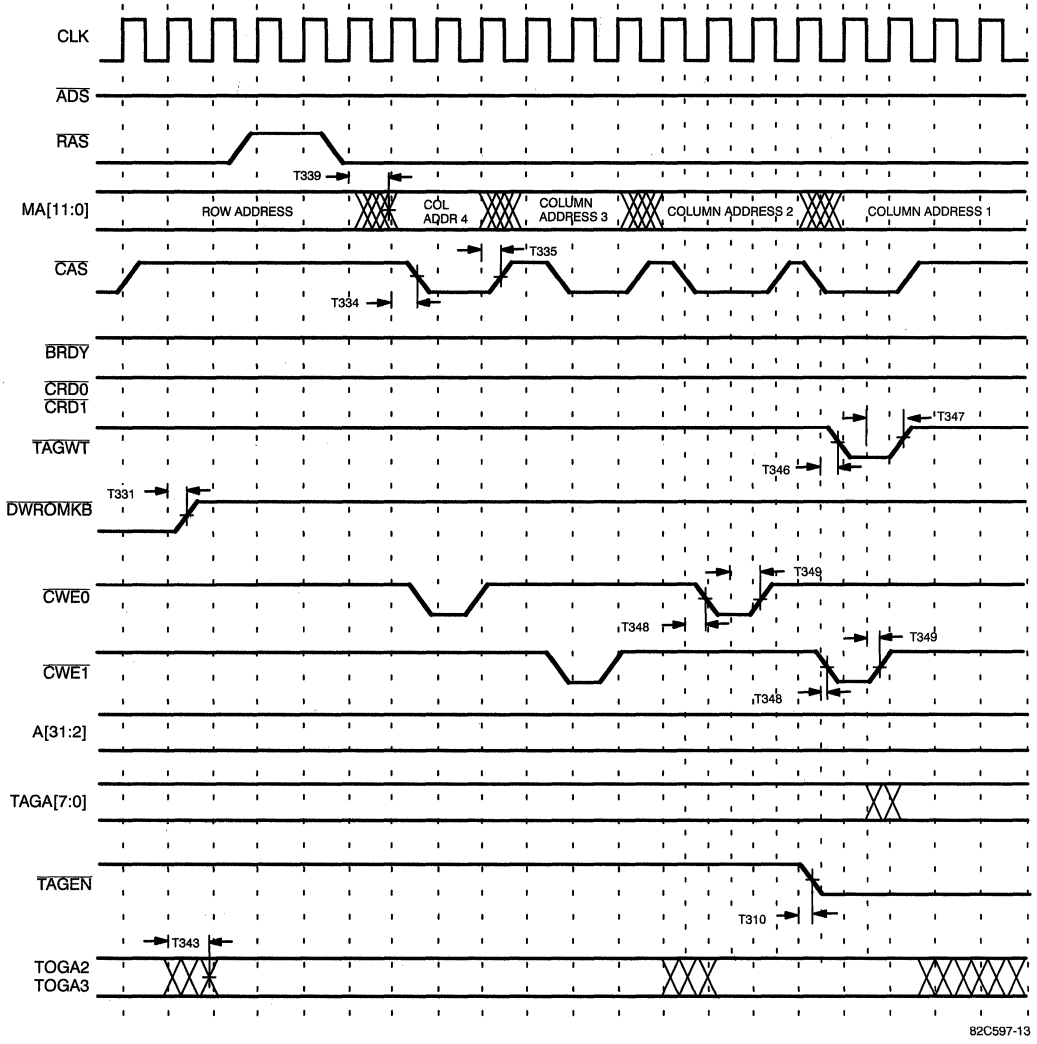
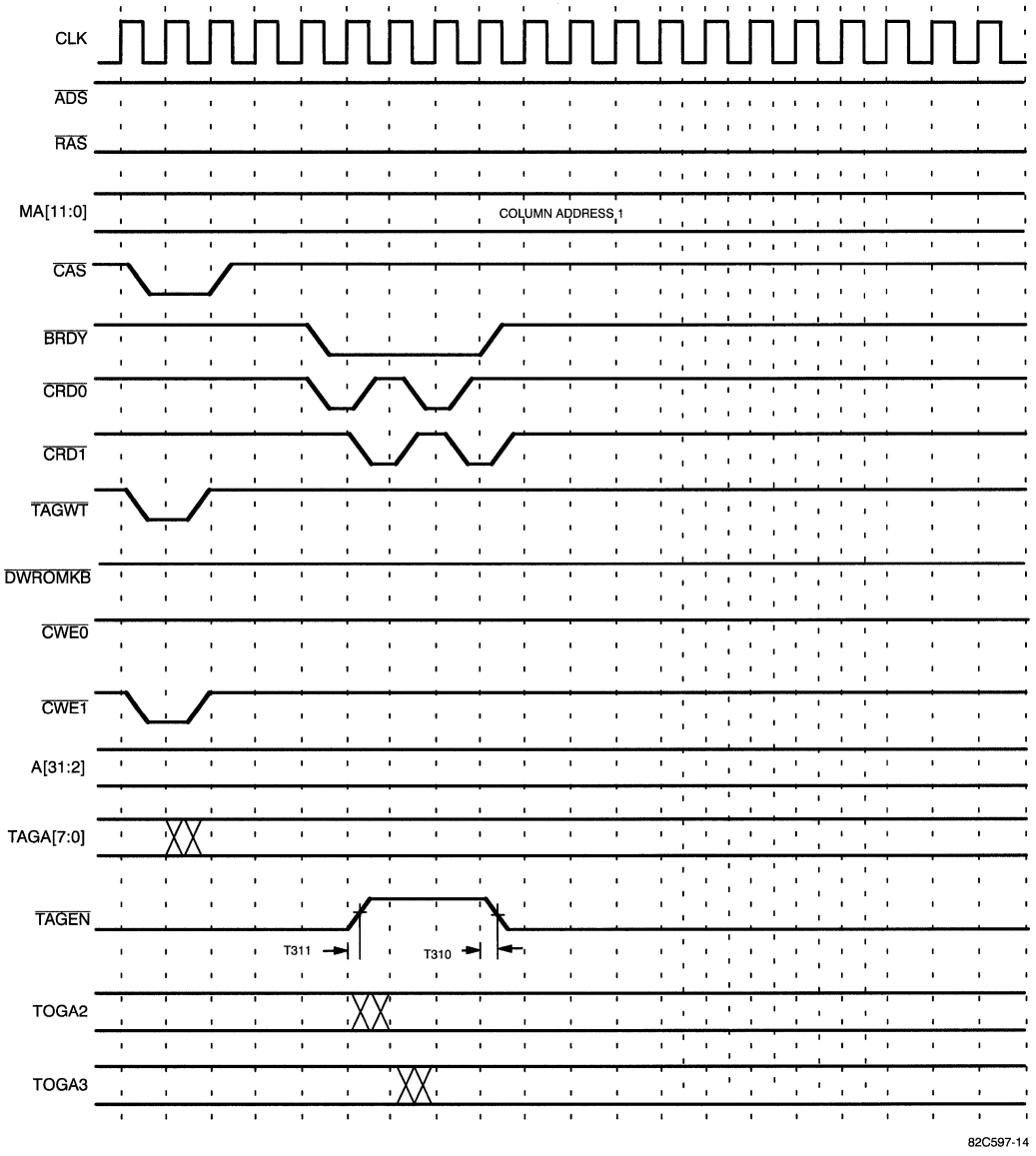
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 2 of 3)



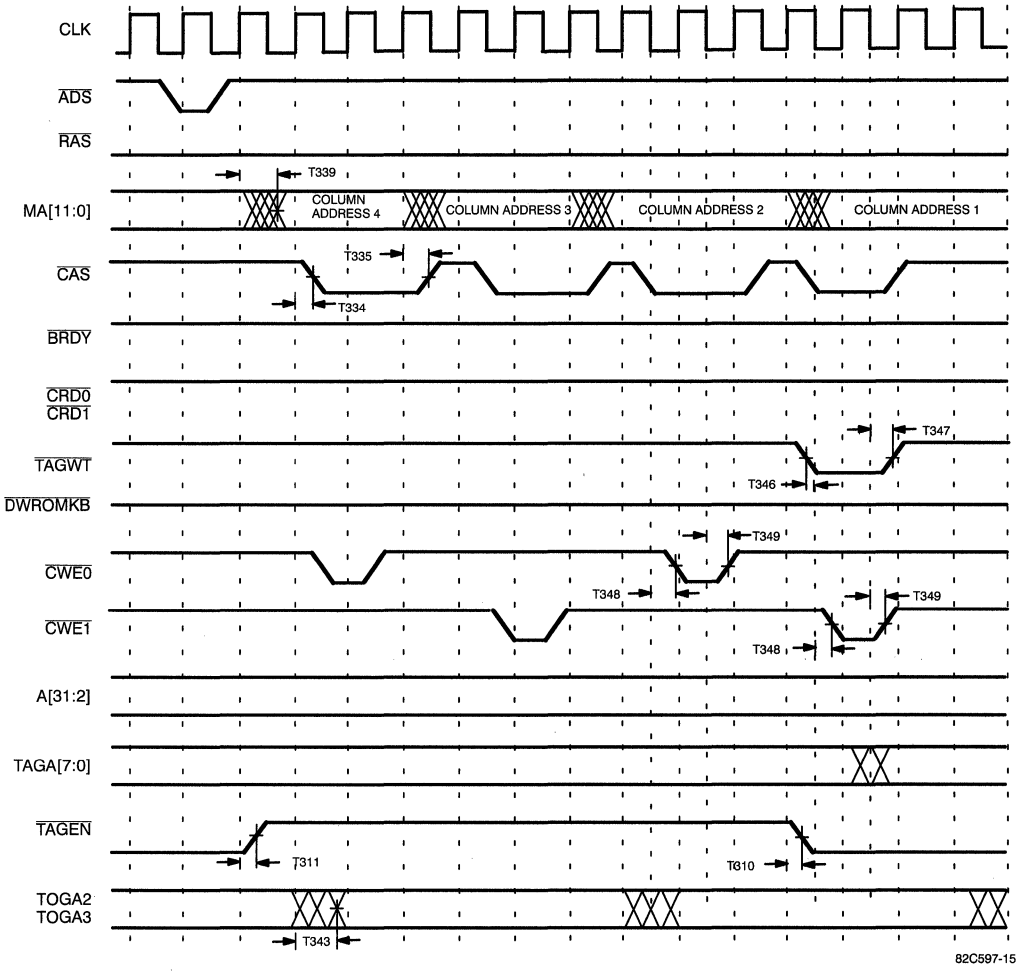
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 3 of 3)



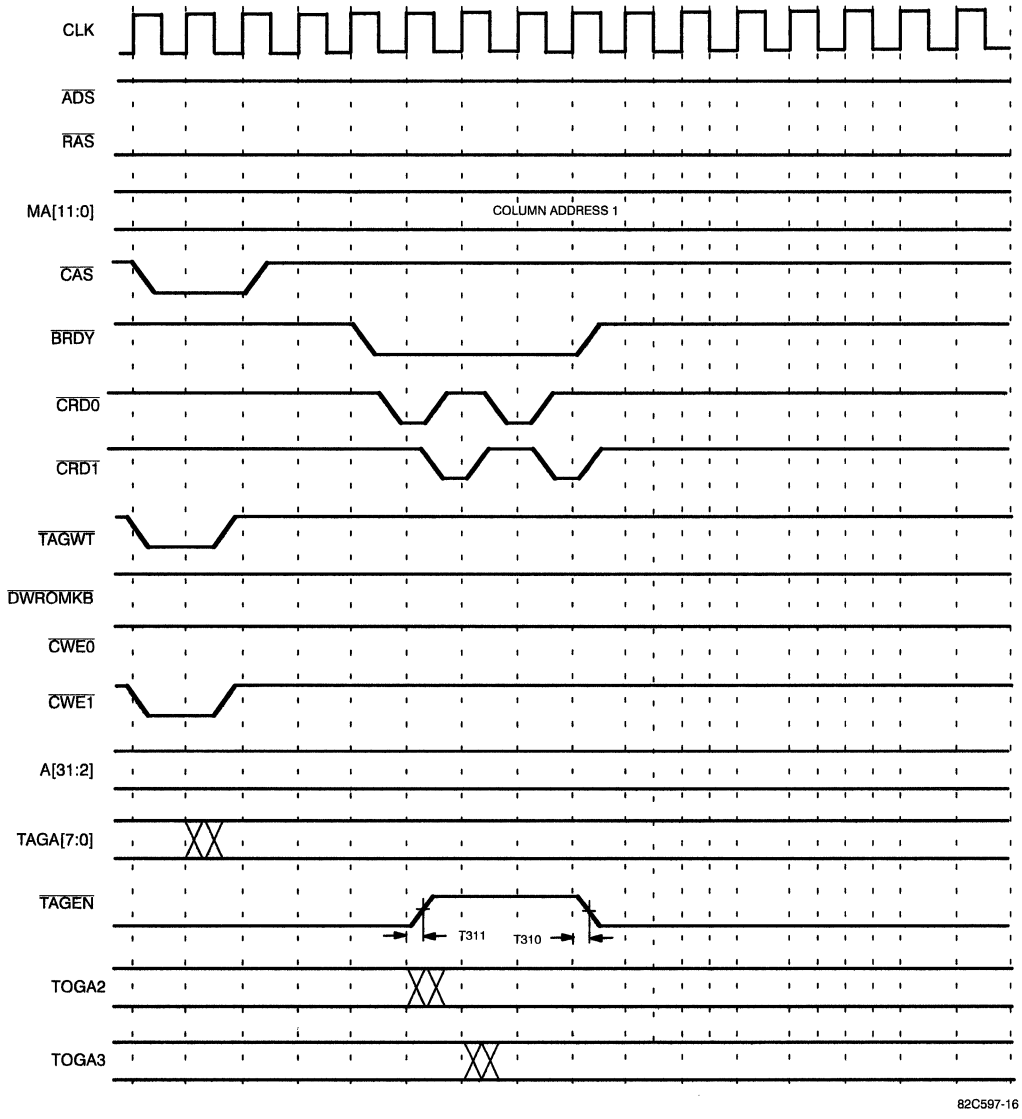
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Hit, Dirty = 0, DRAM R1WT Cycle (Page 1 of 2)



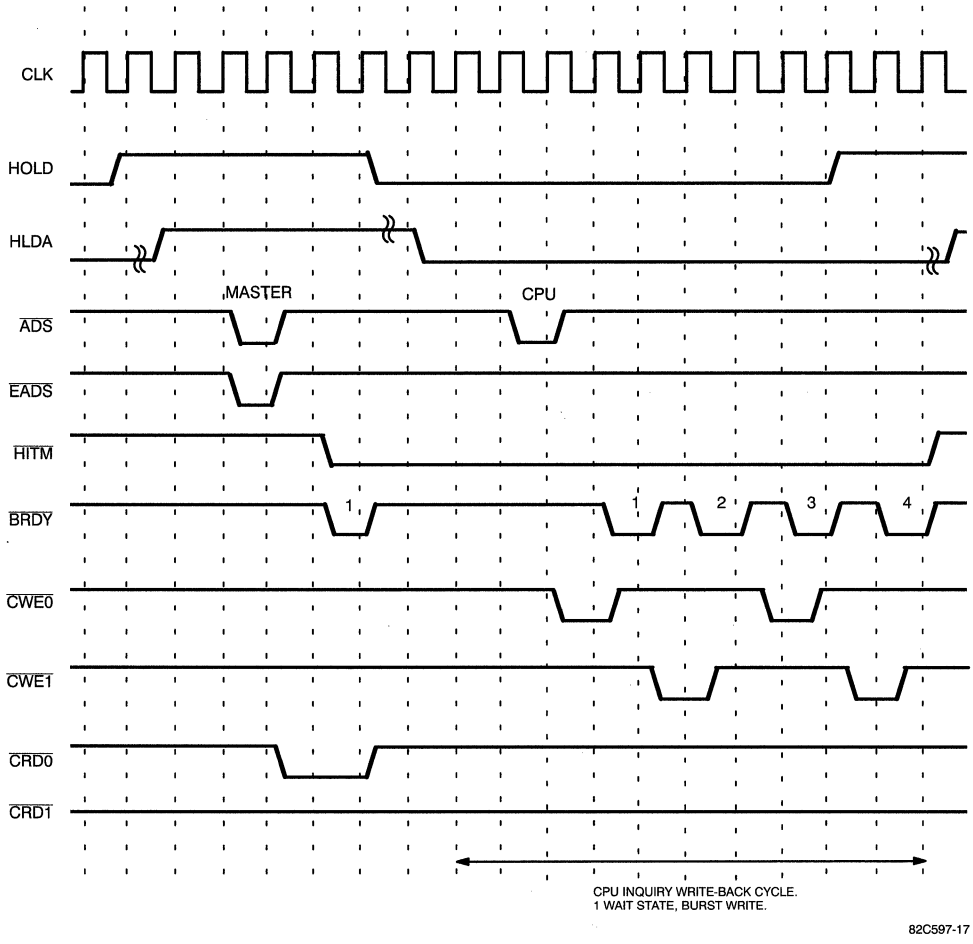
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Hit, Dirty = 0, DRAM R1WT Cycle (Page 2 of 2)



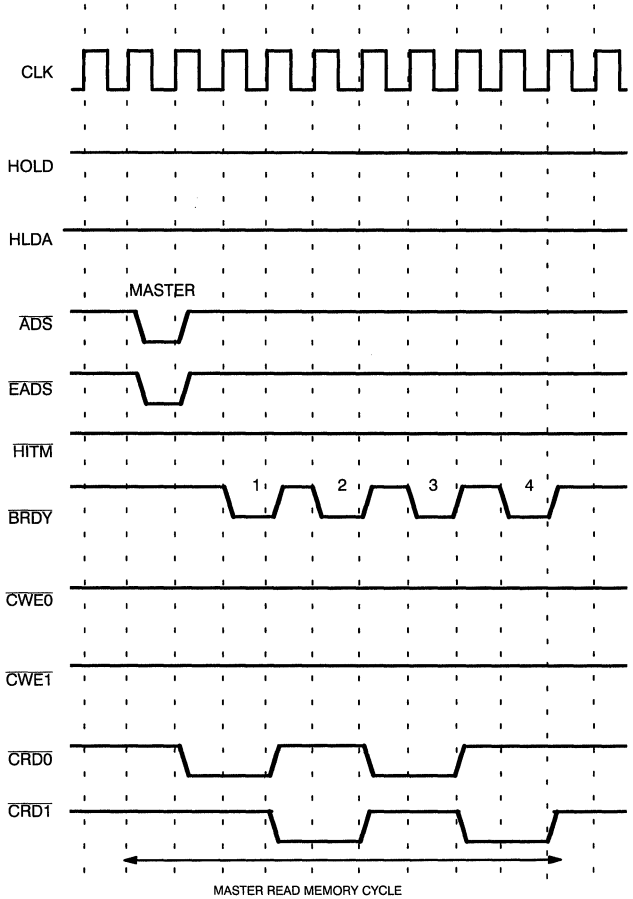
Switching Waveforms (continued)

VESA/PCI Master Read Memory Cycle with Inquiry Hit and Dirty ($\overline{HITM}$=0) (Part 1 of 2)



Switching Waveforms (continued)

VESA/PCI Master Read Memory Cycle with Inquiry Hit and Dirty ($\overline{HITM}$=0) (Part 2 of 2)



MASTER READ MEMORY CYCLE
CACHE HIT, 3222 MODE

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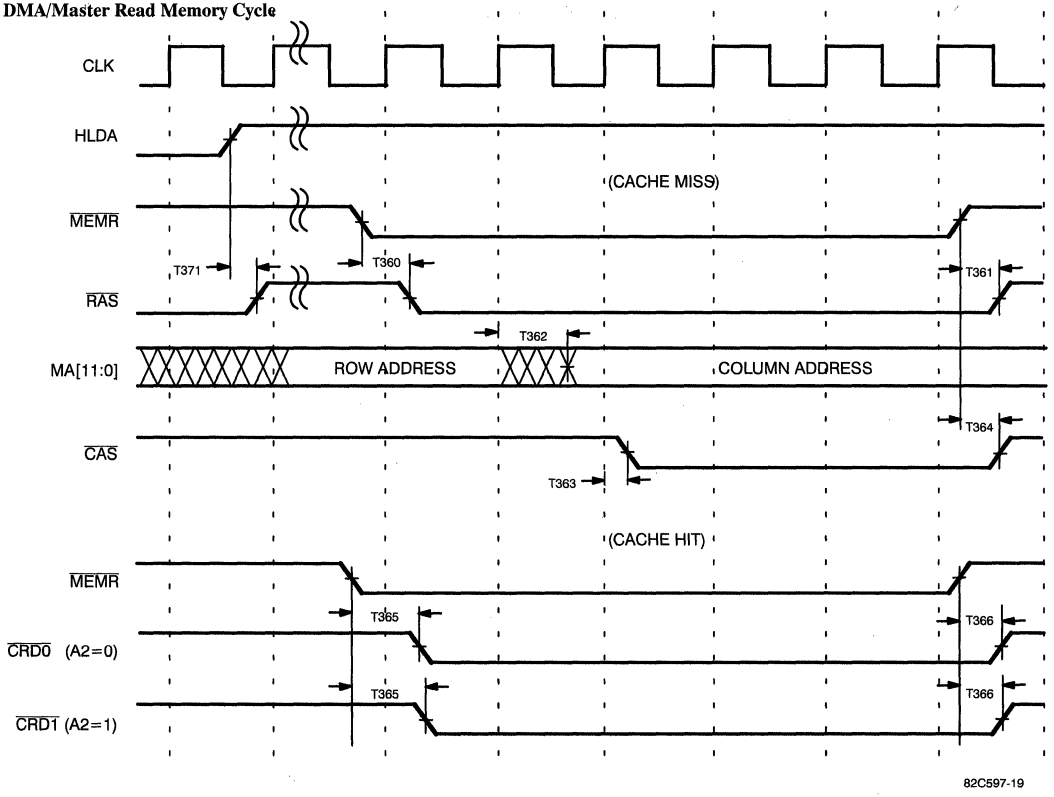
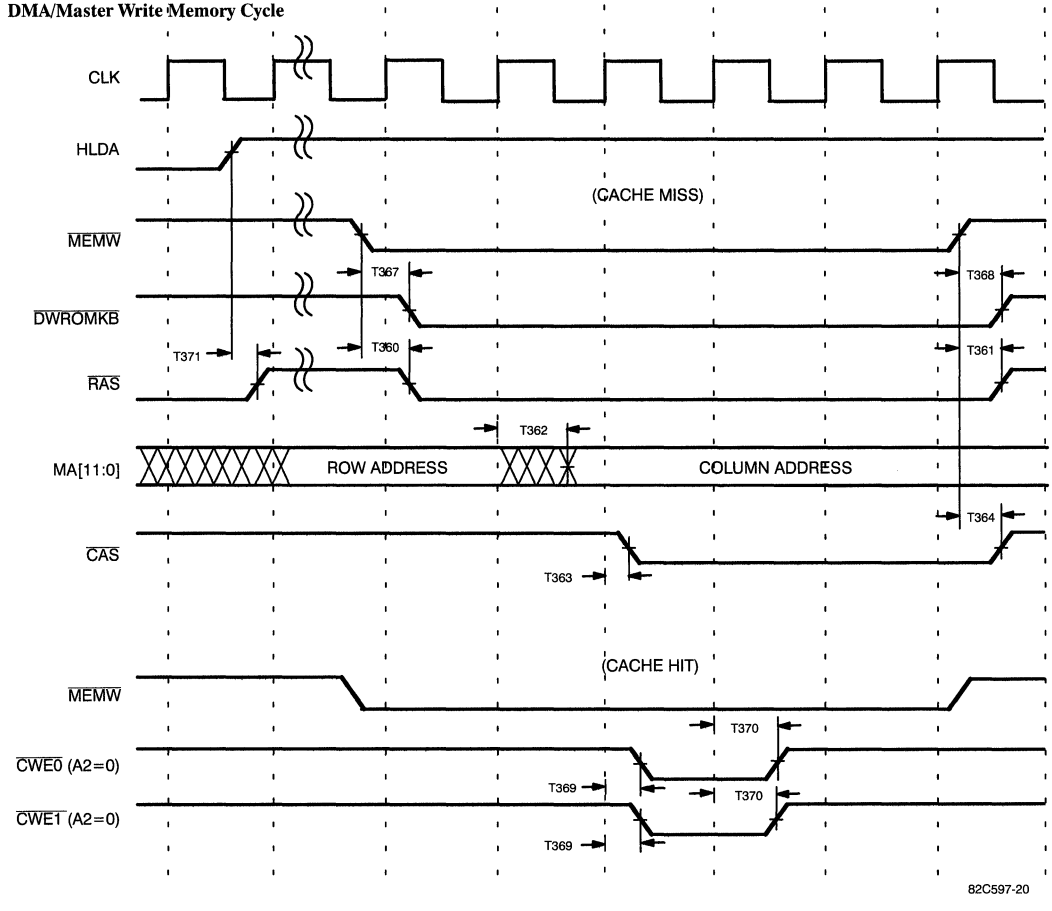
Switching Waveforms (continued)

DMA/Master Read Memory Cycle



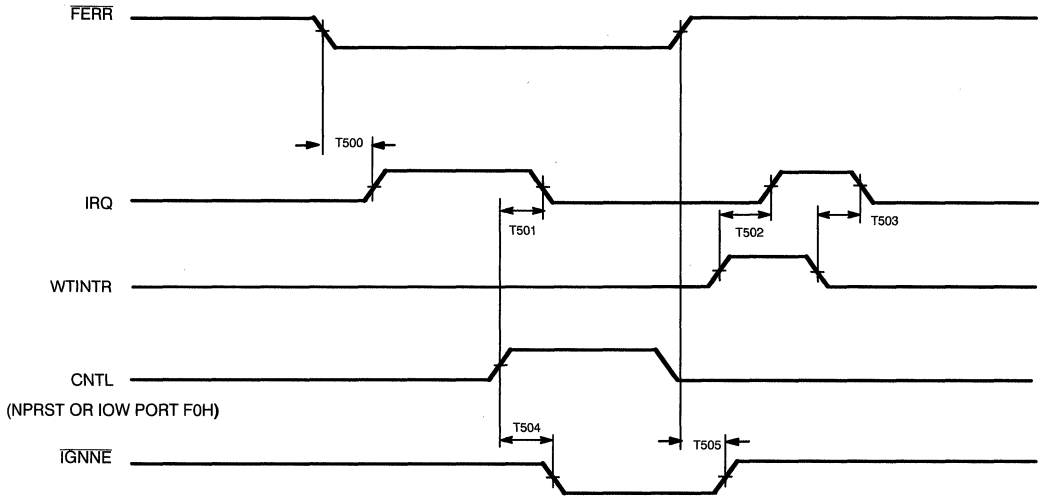
Switching Waveforms (continued)

DMA/Master Write Memory Cycle



Switching Waveforms (continued)

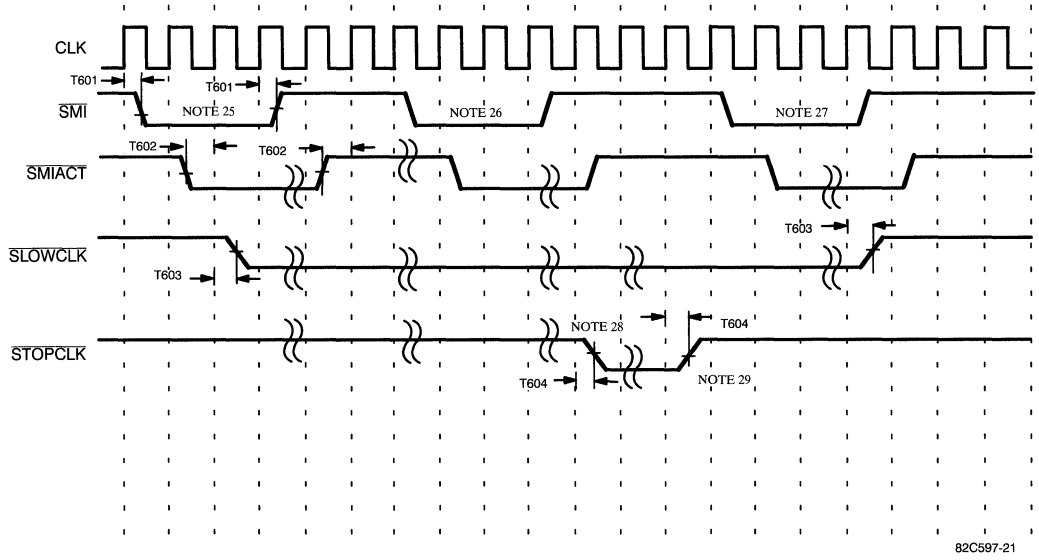
Numerical Coprocessor Interface Timing



82C597-21

Switching Waveforms (continued)

Software Power-Down (Through $\overline{SMI}$)

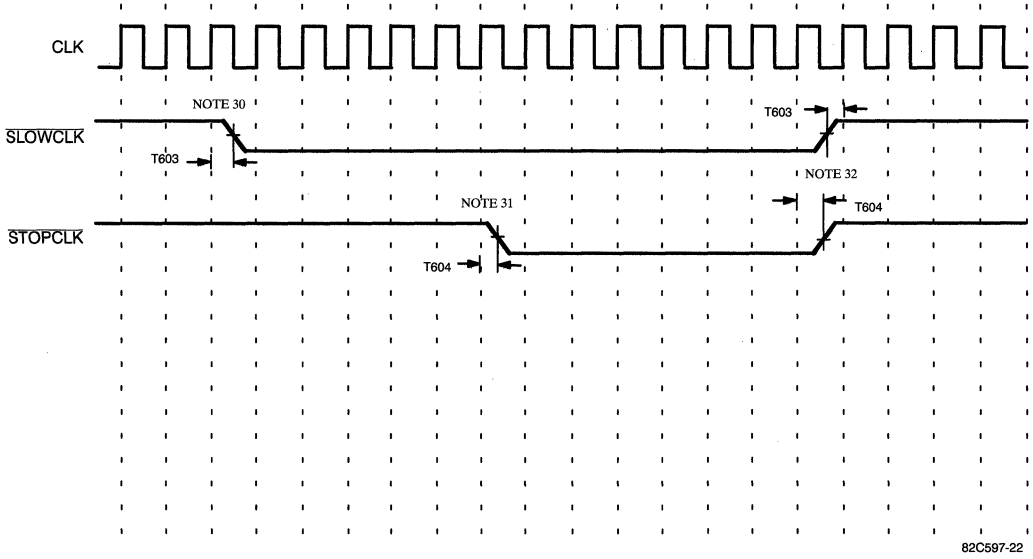


Notes:

25. $\overline{SMI}$ (System Management Interrupt) assertion caused by the standby timer reaching its terminal count with no detected events.
26. $\overline{SMI}$ (System Management Interrupt) assertion caused by the suspend timer reaching its terminal count with no detected events.
27. $\overline{SMI}$ (System Management Interrupt) assertion caused by the detection of one of the monitored events.
28. $\overline{STOPCLK}$ will go active when Register 64 bit 6 is set to 1 and the STOPCLK timer has expired.
29. $\overline{STOPCLK}$ will be deasserted when a monitored event is detected.

Switching Waveforms (continued)

Hardware Power-Down



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY82C597-NC	N160	160-Lead Plastic Quad Flatpack	Commercial

Notes:

30. The assertion of $\overline{\text{SLOWCLK}}$ caused by the stand-by timer reaching its terminal count with no detected events.
31. The assertion of $\overline{\text{STOPCLK}}$ caused by the suspend timer reaching its terminal count with no detected events.
32. $\overline{\text{SLOWCLK}}$ and $\overline{\text{STOPCLK}}$ deassertion caused by the detection of one of the monitored events.

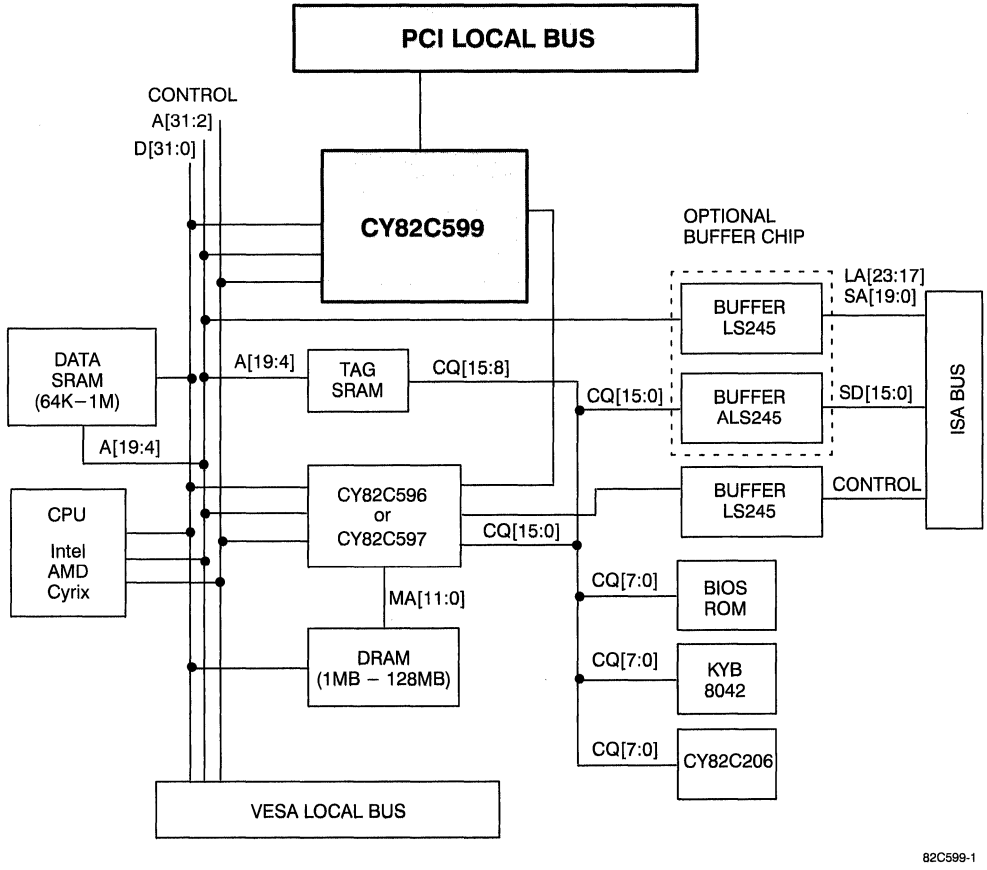
Document #: 38–00411

Intelligent PCI Bus Controller

Features

- Provides an interface between the PCI Local Bus and the CPU bus
- PCI Bus Rev. 2.0 compliant
- Supports Intel® 486DX, 486DX2, 486SX, 486SL, P24T, AMD AM486 and Cyrix Cx486S2 (M6/M7) CPUs
- Interfaces with Cypress CY82C596 or CY82C297 Core Logic devices to form a complete PC solution supporting PCI, VESA, and ISA buses
- Supports 4 PCI Masters
- Supports burst mode PCI accesses to memory space
- PCI pre-read support with 4-double-word-deep FIFO, each double-word is 32 Data bits wide
- PCI post-write support with 4-double-word-deep FIFO, each double-word is 32 Data bits wide
- Synchronous/Asynchronous PCI bus support
- Standby mode slows down CPU clock
- Power management timers
- SMI generation support for Intel, AMD, Cyrix CPUs
- Provides I/O trap for peripheral device power control
- Packaged in 160-pin PQFP

System Block Diagram



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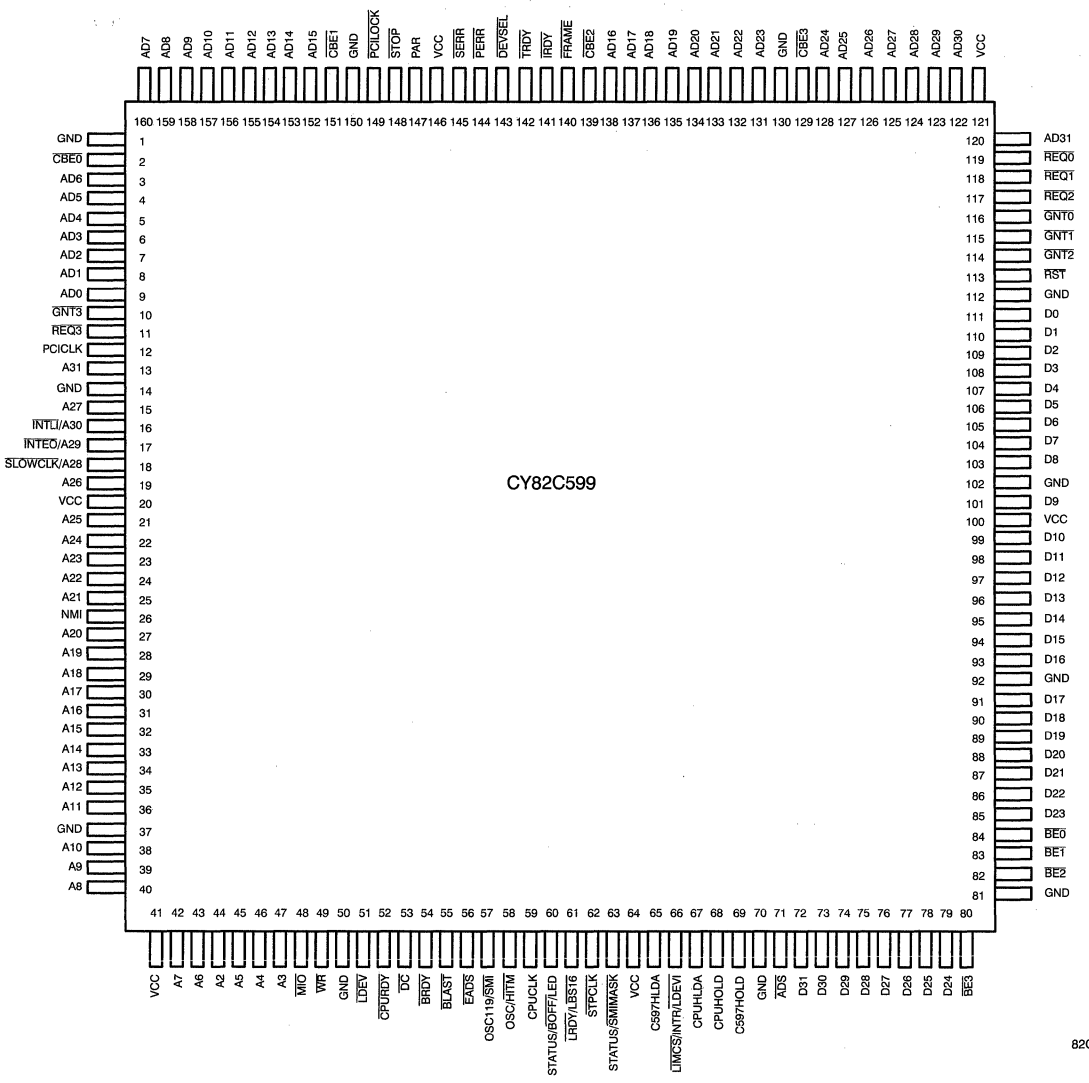
Pin Configurations

PQFP
Top View



82C599-2-

1.0 Introduction

The CY82C599 Intelligent PCI Bus Interface chip is designed to eliminate the ISA Bus I/O bottleneck by providing a glueless path to the high-performance PCI Local Bus. This chip connects the PCI Bus to the VESA Bus and the CPU simultaneously, allowing system designers to take advantage of the PCI Bus's high through-put while maintaining access to the large selection of ISA and VESA local bus expansion cards.

No TTL components are required to connect the CY82C599 to the PCI Bus. However, in applications with heavy loading on the Address/Data lines, buffers may be necessary to distribute the load. The CY82C599 simplifies the interface design by providing buffer control signals.

The CY82C599, along with the CY82C596 PC/AT Core Logic chip or the CY82C597 Green PC/AT Core Logic chip, implements a sophisticated and cost-effective 486-based PCI/VESA/ISA system.

2.0 Functional Overview

The CY82C599 provides the required functions in PCI Specification Revision 2.0 including bus arbitration, bus grant, master support, bus lock support and interrupt support. It supports all the CPU and bus commands except INTA and dual address cycles. INTA cycles are routed to the interrupt controller on the ISA bus. Dual address cycles are reserved for 64-bit addressing and they are ignored by the CY82C599.

The CY82C599 supports bursting in both CPU mode and PCI master mode. It also supports post-write buffering and pre-read buffering with a 4-word-deep bidirectional FIFO. Each word in the FIFO is 64 bits wide (32-bits address, 32-bits data). In addition, fast back-to-back write cycles are supported to enhance system performance.

The central arbiter of the CY82C599 supports two levels of arbitration. The first level arbiter arbitrates bus requests between the VESA and the PCI Buses. The second level arbiter handles bus requests from four PCI master channels. Both levels of arbitration can have either fixed or rotating priority. Optionally, a hold request on the ISA bus (for a refresh, DMA/MASTER, or VESA transactions) can prematurely terminate a PCI transaction.

The CY82C599 has built-in interrupt logic that can convert a level-sensitive interrupt signal to an edge-triggered interrupt signal. This feature enables the usage of popular interrupt controllers such as the 8259 or 83C206.

The preferred PCI Configuration Mechanism #1 is supported in the CY82C599 that allows PCI configuration cycles to be generated by software. To support hierarchical PCI buses, both Type 0 and Type 1 configuration access are implemented. BIOS support is available from AMI & AWARD.

3.0 PCI Bus

The purpose of this section is to give an overview of PCI, the motivation behind it, and its features. Basic transfers and rules are discussed. How the CY82C599 handles inter-bus transfers is discussed in later sections. For a detailed description of the PCI bus, all of the rules and requirements, see the PCI Specification 2.0.

The PCI Bus was defined in order to satisfy the growing need for a standardized high-speed local bus that is independent of the processors, operating system, and CPU bus speed. New generations of computers incorporating I/O intensive software will require bandwidth that cannot be satisfied with the traditional I/O architectures. The PCI specification 2.0 addresses these requirements and provides an upgrade path for future requirements. Some of the PCI features include:

- **Processor Independent**
- **Multiplexed, Burst Mode Operation**
- **120 MBytes/sec usable throughput (32-bit data path)**
- **Three physical address spaces**
  - **Memory**
  - **I/O**
  - **Configuration**
- **Hidden Arbitration**

PCI is defined as a synchronous bus that can operate from 0 to 33MHz. All transfers take place on the rising edge of the clock (PCICLK). The basic data transfer in PCI is a burst. A burst transfer consists of an address phase, followed by one or more data phases. The address phase is defined as the first rising edge of the clock where $\overline{\text{FRAME}}$ is asserted (LOW). During the Address phase, the Master (also referred to as the initiator) asserts the appropriate address on the address/data lines (AD[31:0]) while also asserting the appropriate command on the Command/Byte Enable C/$\overline{\text{BE}}$[3:0] lines. With the information transferred during the address phase, all PCI devices, including the slave (or Target), can determine: 1) Whether the transaction falls within its designated address range, 2) The kind of transfer that will take place (e.g. a read or write to memory, I/O, or configuration space), and 3) How to respond to that particular command.

Once a device recognizes that it is the target for the transaction, it claims the transactions by asserting Device Select ($\overline{\text{DEVSEL}}$) LOW. $\overline{\text{DEVSEL}}$ must be asserted LOW in order for any information is be transferred.

The address phase is followed by one or more data phases. Whether the initial data phase occurs on the subsequent clock edge is determined by the type of transaction and the ability of either agent to provide/accept the data within the appropriate time period. Since the address and data lines are multiplexed, a normal read operation requires a 'turn-around' cycle to avoid bus contention. During this cycle, control of the Address/Data lines is transferred from the master to the slave, who must now use these lines to drive out the requested information. During a write operation, this 'turn-around' cycle is not required since the master is providing the write data and does not have to relinquish control of the bus. PCI also allows that both the master and slave have the ability to insert wait states should either require additional cycles in order to properly participate in the transfer. This is accomplished with the Initiator Ready signal ($\overline{\text{IRDY}}$) and the Target Ready signal ($\overline{\text{TRDY}}$) for the Initiator and Target, respectively. Either of these signals being de-asserted (HIGH) during the data phase of the transaction will insert a wait state, thereby preventing data from being transferred during that cycle. The data presented on the AD[31:0] lines is transferred during a data phase on the rising edge of the clock when ALL of the following signals are active (LOW): $\overline{\text{DEVSEL}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, and $\overline{\text{FRAME}}$ (except during the final data phase, when $\overline{\text{FRAME}}$ is HIGH, which is explained later). The bytes containing meaningful information are controlled by the C/$\overline{\text{BE}}$[3:0] signals. During the data phase, these signals behave as byte enable lines.

Transactions are normally terminated by the Master by de-asserting $\overline{\text{FRAME}}$ HIGH on the clock prior to the last data

phase. By doing so, all of the agents on the bus, including the Target and the Arbiter, recognize that the current transaction is coming to an end. This advanced notice allows the Arbiter to grant ownership of the bus to the next requesting agent. This is referred to as Hidden Arbitration since no additional clock cycles are consumed. The new Master will not start to drive the bus until the current transaction is actually completed. The Target has the ability to abort the transaction prematurely should the need arise, although this is not the typical method of termination.

Arbitration in PCI is access based instead of time slot based. This is accomplished through a simple request–grant handshaking scheme through a central arbiter. Each agent has dedicated request and grant lines to the arbiter. A bus Master must request and be granted bus ownership each time a transaction is desired.

PCI defines three different physical address spaces; memory, I/O, and configuration space. Each of these address spaces has its own characteristics. Therefore, transactions to each space are handled differently, particularly in regards to AD[0:1]. The memory and I/O address spaces are customary, but the configuration address space has been defined by PCI in order to support hardware configuration.

4.0 Address Space

The purpose of this section is to explain the memory and I/O address space mapping used by the CY82C599.

The CY82C599 recognizes two different physical address spaces, memory and I/O. Transactions to these two address spaces are handled differently, and therefore need to be distinguished from one another. The CY82C599 differentiates these two different type of transactions by monitoring the M/$\overline{IO}$ signal coming from the CPU bus, or the C/$\overline{BE}$ signals coming from the PCI bus. In order to recognize the destination of each transaction, each address space needs to be divided (or mapped) into the different target areas (ISA, PCI, VESA, or Local Memory). Each address map, memory and I/O, is discussed below.

4.1 I/O Address Space

Although the I/O address space can extend the full 32 bits (a possible 4 GB of I/O address space), x86 CPUs limit I/O transactions to the lower 64KB (0000h–FFFFh). The remaining address locations are not valid I/O address space. In addition, the lower 1KB (0000h–03FFh) of I/O space has been assigned as AT I/O space. Within the lower 1KB (AT space) resides numerous predefined I/O blocks that can be assigned to PCI or ISA/VESA through configuration registers. The remaining I/O address locations (0400h–FFFFh) can be mapped using three 100% user defined I/O blocks. The base address, block size, and bus location (e.g. PCI, VESA, or ISA) of these I/O blocks are determined by the configuration registers during boot-up (see configuration registers). If an I/O address area is excluded from the user defined blocks mentioned above, it is considered to be in an 'unknown' I/O location. 'Unknown' I/O address locations are handled on a priority basis (see the I/O access priority sections for further details). Although the PCI base address can be placed anywhere within the lower 64KB using one of the three 100% user defined I/O blocks, it is recommended that the PCI base address be placed at 8000h or above to avoid contention with VESA devices. VESA and PCI devices should never occupy the same I/O address location. Doing so will cause a bus contention condition. How the CY82C599 responds to each I/O transaction is discussed in the following sections.

4.2 Memory Address Space

The CY82C599 supports up to 256MB of local memory space (128MB when used with the CY82C596/7). The full 4GB memory space can be mapped over the PCI, VESA, or ISA regions (see configuration registers). This mapping allows the CY82C599 to determine the destination of the transaction and respond appropriately. A minimum of 64KB (0000h–FFFFh) of memory address space is reserved for system usage. Up to 256MB can be defined as local memory. The Local memory ending address is user defined through configuration registers 20h and 21h. The CY82C599 also supports 4 user defined memory block. Blocks 0 & 1 can be mapped over the entire address space by defining the base address, block size, and bus location. Blocks 2 & 3 are simply enabled/disabled (through register 46h) and can only be mapped to PCI. With these memory blocks the user can define the memory map of the system. As with I/O address space, some memory areas can be excluded from the memory map, and are therefore defined as 'unknown'. These 'unknown' locations are handled on a priority basis that is discussed in memory priority sections. How the CY82C599 responds to each transaction is discussed in each of the following sections.

4.3 PCI Configuration Space

The CY82C599 supports the preferred PCI Configuration Mechanism #1 that allows PCI configuration cycles to be generated by software. Both Type 0 and Type 1 configurations accesses are also supported. All required fields within the Configuration Header Space are also supported.

5.0 Device Operation

The purpose of this section is to describe the basic operation of the CY82C599 Intelligent PCI Bus Interface. The CY82C599 functional block diagram is shown in the functional block diagram. The core functionality of the CY82C599 is controlled by the Central Arbiter and the surrounding four state machines. These four state machines communicate with one another in order to properly conduct and synchronize all transactions. Supporting functions are conducted through control logic, interface and synchronization logic (PCI and CPU buses), configuration registers, and an internal bidirectional FIFO. The following sections describes the functionality of each of these major blocks within the CY82C599.

5.1 Central Arbiter

The Central Arbiter is responsible for delegating control of the CY82C599 Intelligent PCI Bus Interface. In addition, the Central Arbiter also performs the general arbitration on the PCI bus. The Central Arbiter monitors incoming requests from both the CPU and PCI buses and grants control of the Interface to either the PP (PCI Master Controlling PCI bus) or CC (CPU Master Controlling CPU bus) state machines. Once a request has been granted, control of the Interface is transferred to that particular state machine. Once the transaction is complete, the arbiter delegates control of the bridge to the next requesting agent. Should there be no pending requests, the default owner of the bridge is the CC (CPU Master Controlling CPU bus) state machine. When servicing a CPU master bus cycle, the Central Arbiter will not grant a PCI agent control of the PCI bus (although CY82C599 to PCI transfers are permitted during CPU to memory bus transactions due to Post-Write Operations). Also, when servicing a PCI agent, a CPU hold is established (HOLD asserted and HLDA acknowledged) prior to the PCI $\overline{GNT}$ signal

being asserted. The PCI arbitration algorithm is user selectable through register 30h, and can be either fixed or rotating priority.

5.1.1 PCI Arbitration

Arbitration on the PCI bus is controlled by the Central Arbiter within the CY82C599. PCI arbitration is conducted through a request-grant handshake between the requesting master and the arbiter (CY82C599). Request and grant lines are point-to-point signals that are not universally shared on the bus. The CY82C599 will hold off granting the bus to a PCI agent if the CY82C599 is involved with a transaction. The PCI arbitration algorithm can be either a rotating or fixed priority (see control register 30h). When a fixed priority scheme is selected, $\overline{REQ0}$ /$\overline{GNT0}$ has the highest priority and $\overline{REQ3}$/$\overline{GNT3}$ the lowest priority. A rotating priority scheme starts out with same priority as the fixed algorithm ($\overline{REQ0}$/$\overline{GNT0}$ highest,...etc.). After each agent gains control of the bus it is delegated to the lowest priority. The highest priority is defaulted to the agent that has had the longest time since having control of the bus.

5.1.2 CPU Arbitration

When used in conjunction with the CY82C596/7, the CY82C599 conducts the first level arbitration on the CPU bus. If the 82C596/7 (or any device controlled by the CY82C596/7 on the ISA or VESA buses) requests control of the CPU bus, it must first assert a hold request (C597HOLD) to the CY82C599. The CY82C599 will asserts a hold request to the CPU (through the CPUHOLD signal). After completing the current transaction, the CPU acknowledges the hold by asserting the CPUHLDA signal back to the 82C599. Upon receiving this acknowledge, the CY82C599 grants the original bus request by asserting a hold acknowledge back to the CY82C596/7 by asserting C597HLDA. The CY82C599 gives the CY82C596/7 the highest priority and will interrupt PCI transactions when a request, such as a request to refresh, is received.

5.2 PCI Master Controlling PCI Bus (PP) State Machine

The PCI Master Controlling PCI Bus (PP) State Machine is responsible for executing all PCI bus transactions based on inputs from the PCI bus. This includes claiming and administering all PCI transactions where the target is on the CPU bus side of the 82C599 Interface. Such transactions are broken into two separate transfers; 1) PCI master device to the CY82C599 as the target, and 2) CY82C599 as the CPU bus master to CPU bus target. The first portion of the transaction is controlled by the PP state machine, while the second transaction is handled with the PC state machine. The PP state machine conducts all PCI related operations, provides control information to the PC state machine, and delivers the address and data to the internal FIFO.

5.3 PCI Master Controlling CPU Bus (PC) State Machine

The PCI Controlling CPU Bus (PC) state machine is responsible for all transactions on the CPU bus initiated by PCI bus inputs. These transactions include conducting a CPU bus cycle in order to deliver data from the internal FIFO to the CPU bus target. Although the PC state machine acts as the master on the CPU bus, it is not considered in control of the CY82C599 during any transaction. Instead, the PC state machine receives control signals from the PP state machine, who is in control of the CY82C599 PCI Interface.

5.4 CPU Master Controlling CPU Bus (CC) State Machine

The CPU Master Controlling CPU Bus (CC) State Machine is responsible for handling all CPU bus transactions initiated by CPU bus inputs. This includes claiming all transactions that are within the PCI or 'unknown' address spaces (memory or I/O). When a CPU bus cycle is claimed by the CY82C599, the CC state machine is in control of the CY82C599 Interface. CPU-to-PCI transfers are broken into two separate transactions; 1) CPU bus master device to the CY82C599 as the CPU bus target, and 2) CY82C599 as the PCI master to PCI bus target. The first portion of the transaction is controlled by the CC state machine, while the second transaction is handled by the CP state machine. The CC state machine conducts all CPU bus related operations, provides control information to the CP state machine, and delivers the address and data to the internal FIFO. When there are no pending bus requests, the CC state machine is the default owner of the CY82C599 Interface.

5.5 CPU Master Controlling PCI Bus (CP) State Machine

The CPU Master Controlling the PCI Bus (PC) State Machine is responsible for all transactions on the PCI bus initiated by CPU bus inputs. These transactions include conducting PCI bus cycle in order to deliver data from the internal FIFO to the PCI bus target. Although the CP state machine acts as the master on the PCI bus, it is not considered in control of the CY82C599 during any transaction. Instead, the CP state machine receives control signal from the CC state machine, who is in control of the CY82C599 Interface.

5.6 Post Write Operation

The CY82C599 allows Post-Writing for both CPU-to-PCI bus, and PCI-to-CPU bus transactions. The Post-Write FIFO is a four deep, 64-bit wide circular FIFO designed to allow a CPU or PCI bus agents to Post-Write four full words (32 bits of address and 32 bits of data) to the CY82C599. Once the information arrives in the FIFO, the CY82C599 requests control of the PCI or CPU bus in order to complete the write transaction. Once a line of data has been read from the FIFO, an additional line can be written in order to keep the FIFO full and increase throughput. Should a Post-Write to a PCI agent go unclaimed, the CY82C599 will retry a predetermined number of attempts (see register 33h). Should the transaction still go unclaimed, the data will be lost. By providing this Post-Write feature, the CY82C599 allows the CPU to Post-Write to the CY82C599, and then proceed with other transactions.

5.7 PCI Burst Pre-Read Operation

The CY82C599 supports CPU-to-PCI Burst Pre-Read operations. Pre-Reads are similar to Post-Writes, and are handled with the use of the same on-chip FIFO. The CY82C599 can pre-fetch read data, fill the internal FIFO, and then burst read to the requesting master on the PCI bus. During this pre-fetch, the CY82C599 holds the requesting bus by inserting wait states. The CY82C599 will burst the data to the requesting PCI agent in a linear sequence.

5.8 Synchronous/Asynchronous PCI Operation

The CY82C599 allows for both synchronous and asynchronous PCI bus operation. Synchronous PCI bus operation is defined as when the PCI and CPU buses are operating from the same clock. Asynchronous PCI operation is defined as when the PCI and CPU clocks are either out of phase or running at different frequencies. The CY82C599 is able to accommodate the two asynchronous buses through the use of advanced synchronization circuitry. The asynchronous operation can support a CPU clock up to 50MHz, and a PCI clock from 0 to 40MHz.

6.0 Address Space Priority

The CY82C599 employs a priority scheme for all memory and I/O transactions. The purpose for this priority system is to achieve predictable results should there be an overlap in the

memory or I/O address space, as well as accesses to 'unknown' address locations. The purpose of the following sections is to explain the priorities of each type of transaction from each side of the CY82C599 Interface.

6.1 CPU Bus Master Priority-Memory Accesses

The highest priority in a CPU bus master memory access is when the target resides in Local memory. During these cycles, the CY82C599 monitors, but does not participate in the transaction.

The second highest priority in a CPU bus master memory access is when the target is in PCI or VESA memory address space. For transactions to PCI memory space, the CY82C599 will claim the transaction by asserting $\overline{\text{LDEV}}$. The transaction is allowed to proceed normally, and is terminated on the CPU bus with $\overline{\text{CPURDY}}$ from the CY82C599. If the transaction is claimed by a VESA device, the VESA target will drive $\overline{\text{LDEV}}$ and terminates the transaction with $\overline{\text{CPURDY}}$.

The lowest priorities are CPU bus master memory accesses to VESA or ISA address space. The CY82C599 will monitor, but will not participate in the transaction.

The CY82C599 will claim all memory transactions to 'unknown' address space on the CPU bus by asserting $\overline{\text{LDEV}}$ and will immediately initiate a PCI cycle. If the target is a PCI device (in 'unknown' space), the transaction is claimed by the PCI device and proceeds normally, with the CY82C599 terminating the transaction by asserting $\overline{\text{CPURDY}}$ to the CPU. If the PCI transaction goes unclaimed, the CY82C599 de-asserts $\overline{\text{LDEV}}$. The CY82C599 will automatically de-assert $\overline{\text{LDEV}}$ if $\overline{\text{CPURDY}}$ goes active (the transaction was claimed and completed by a VESA device). If the target is a VESA device (in 'unknown' space), it asserts $\overline{\text{LDEV}}$ and claims the transaction. Since $\overline{\text{LDEV}}$ from the CY82C599 and the VESA devices are ANDed together, the CY82C596/7 will only pass the cycle to the ISA bus if neither VESA or PCI claims the transaction. Since VESA and PCI agents share the same priority, two memory devices (one on VESA and the other PCI) should never share the same address space. Doing so will cause a clash condition by having both devices claim the same transaction.

6.2 CPU Bus Master Priority-I/O Accesses

The highest priority CPU bus master I/O transaction is PCI/VESA space. These two types of devices I/O address spaces are considered to have the same priority. The CY82C599 will claim I/O transactions to PCI address space by asserting $\overline{\text{LDEV}}$. The transaction is allowed to proceed normally, and is terminated on the CPU bus with $\overline{\text{CPURDY}}$ from the CY82C599. If the transaction is to VESA I/O address space, the VESA target will claim the transaction by asserting $\overline{\text{LDEV}}$.

The second priority CPU bus master access to I/O space is when the target resides in ISA space. The CY82C599 will monitor, but not participated in CPU bus master transactions to ISA space.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. The CY82C599 will claim all I/O transactions to 'unknown' address space on the CPU bus by asserting $\overline{\text{LDEV}}$ and will immediately initiate a PCI cycle. If the target is a PCI device (in 'unknown' space), the transaction is claimed by the PCI device and proceeds normally, with the CY82C599 terminating the transaction by asserting $\overline{\text{CPURDY}}$ to the CPU. If the PCI transaction goes unclaimed, the CY82C599 de-asserts $\overline{\text{LDEV}}$. The CY82C599 will automatically de-assert $\overline{\text{LDEV}}$ if $\overline{\text{CPURDY}}$ goes active (the transaction was claimed and completed by a VESA device). If the target is a VESA device (in 'unknown' space), it asserts $\overline{\text{LDEV}}$ and claims the transaction. Since $\overline{\text{LDEV}}$ from the CY82C599 and the VESA devices are ANDed together, the CY82C596/7 will only pass the cycle to the ISA bus if neither VESA or PCI claims the transaction. Since VESA and PCI agents share the same priority, two I/O devices (one on VESA and the other PCI) should never share the same address space. Doing so will cause a clash condition by having both devices claim the same transaction.

6.3 PCI Master Priority-Memory Accesses

The highest priority PCI master memory transaction is an access to Local memory. During such transactions the CY82C599 will claim the CPU bus as quickly as possible by asserting a hold request to the CPU. PCI bus ownership is not be granted until a hold acknowledge is received back from the CPU. Once bus ownership has been established, the transaction proceeds normally with the CY82C599 as the CPU bus master.

The second priority PCI master memory transaction is to PCI memory located on another PCI card. During these transactions the CY82C599 monitors, but does not participate in the transaction. In addition, the CY82C599 will hold the CPU bus during the entire transaction.

The third priority PCI master memory transaction is to ISA/VESA address space. During these types of transfers, the CY82C599 will claim the ISA/VESA bus as soon as possible and initiate an ISA/VESA cycle.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. PCI agents are given the first opportunity to claim PCI master accesses to 'unknown' memory space. The CY82C599 will wait for a PCI agent to claim the transaction by monitoring $\overline{\text{DEVSEL}}$. If the transaction goes unclaimed on the PCI bus, the CY82C599 will automatically start a CPU bus cycle. If the transaction goes unclaimed on the CPU bus, the 82C596/7 will automatically pass the transaction to the ISA bus.

6.4 PCI Master Priority-I/O Accesses

The highest priority PCI master I/O access is to PCI address space. During these transactions the CY82C599 monitors, but does not participate in the transaction. In addition, the CPU bus is held during the entire transaction.

The second priority PCI master I/O transaction is to the ISA bus. During such transactions, the CY82C599 will claim the transaction by asserting $\overline{\text{DEVSEL}}$ and behave as the PCI target. The CY82C599 will also start a CPU bus as soon as possible and initiate an ISA/VESA cycle.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. PCI agents are given the first opportunity to claim PCI master accesses to 'unknown' I/O space. The CY82C599 will wait for a PCI agent to claim the transaction by monitoring the $\overline{\text{DEVSEL}}$. If the transaction goes unclaimed on the PCI bus, the CY82C599 will automatically start a CPU bus cycle. If the transaction goes unclaimed on the CPU bus, the 82C596/7 will automatically pass the transaction to the ISA bus.

7.0 Level 1 Write-Back Cache Support

The CY82C599 also provides for chipsets that support Level 1 write-back cache. The CY82C599 adheres to the $\overline{\text{HITM}}$ protocol required to maintain cache coherency. When $\overline{\text{HITM}}$ is asserted, the CPU has detected a hit to a modified line in the Level 1 cache. In order to allow the CPU to write-back the modified line, the CY82C599 de-asserts the HOLD request to the CPU. The CPU then proceeds to write the modified line to DRAM and L2 cache (if a L2 cache hit is detected). The CY82C599 immediately requests another HOLD to the CPU so the initial transaction can continue.

8.0 Stand-Alone Mode

The CY82C599 can work in conjunction with the 82C596/7 to provide a high performance VESA/ISA/PCI PC/AT system. The CY82C599 also has the built-in flexibility to work with other chipsets to provide a CPU-to-PCI bus bridge. This is referred to as Stand Alone Mode. In Stand-Alone mode, the CY82C599 has enough flexibility to accommodate other chipset's logic and is able to pass transactions to 'unknown' space from one bus to another. In order to operate properly in Stand-Alone mode, the register set of the accompanying chipset must be compatible with the CY82C599 (contact the factory for details).

9.0 Power Management Mode

The CY82C599 implements flexible power management logic. When used with the CY82C597 (for a full VESA/ISA/PCI system), most of the power management functions are performed by the CY82C599. The CY82C597 will only perform the SMM memory mapping. All other power management functions in the CY82C597 are disabled. For VESA/ISA-only systems, the CY82C597 provides all of the chipset power management.

There are eleven event detectors and five user-programmable timers in the CY82C599 allowing it to support full hardware power management (for CPUs that do not support SMM, System Management Mode) and software power management (through SMM).

9.1 Events that can be Monitored

The CY82C599 allows the following events to be monitored:

1) VESA master request
2) Keyboard command
3) Serial Port command
4) Parallel Port command
5) Hard Disk command
6) DMA/MASTER request from the ISA bus
7) Non-motherboard memory access
8) Video memory access
9) A specific I/O address
10) A specific memory range
11) A specific I/O range

When events are detected, the CY82C599 will transition to different power-down states.

9.2 Hardware Power Management

For hardware power management, the CY82C599 supports Full-speed/Stand-by/Suspend/Off states. In Stand-by state, the CY82C599 will assert the $\overline{\text{SLOWCLK}}$ signal that can be used by the system to slow down the CPU's clock frequency. In the Suspend state, the CY82C599 will assert the $\overline{\text{STOPCLK}}$ signal. $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or turn off the monitor and other supported peripherals.

In the Full-speed state, the CY82C599 will monitor all stand-by events. Any monitored event will reset the stand-by timer. If no events occur within the period specified by the stand-by timer, the CY82C599 will enter the Stand-by state and assert the $\overline{\text{SLOWCLK}}$ signal. Once Stand-by state has been entered, the CY82C599 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C599 will assert $\overline{\text{STOPCLK}}$ and enter the Suspend state. In the Suspend state, the assertion of $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or power-down any supported peripherals. If any monitored event is detected, the CY82C599 will return to the Full-speed state and $\overline{\text{STOPCLK}}$/$\overline{\text{SLOWCLK}}$ will be deasserted.

Any interrupt will temporarily cause the $\overline{\text{STOPCLK}}$ signal (and optionally the $\overline{\text{SLOWCLK}}$ signal) to be deasserted (allowing the CPU to service the interrupt). If the interrupt timer expires before a monitored event occurs, the CY82C599 will automatically return to the power-down state it was in prior to the interrupt (with the appropriate signal asserted).

9.3 Software Power Management

For software power management, the CY82C599 can fully utilize Intel's, AMD's, and Cyrix's power management modes to reduce system power requirements.

In the Full-speed state, the CY82C599 will monitor all stand-by events. If no events occur within the period specified by the stand-by timer, the CY82C599 will enter the Stand-by state and assert the $\overline{\text{SMI}}$ signal. In Stand-by state, the system clock can be slowed down by the assertion of the $\overline{\text{SLOWCLK}}$ signal. $\overline{\text{SLOWCLK}}$ is controlled through software (See Register 64). Once Stand-by state has been entered, the CY82C599 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C599 will assert $\overline{\text{SMI}}$ and enter the Suspend state. In the Suspend state, software assertion of $\overline{\text{STOPCLK}}$ (See register 64) can be used to stop the CPU's clock, the monitor can be turned off using a software driver, or the hard disk can be spun down. Please note that the assertion/deassertion of $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ is fully software controlled and can be implemented in any power-down state (Stand-by and Suspend are customary).

The Suspend timer is fully reprogrammable. In the Suspend state, the Suspend timer can be disabled, the timer value changed, and the timer re-enabled. After the new timer value has expired, $\overline{\text{SMI}}$ will once again be activated to allow for a user-defined power management mode.

The CY82C599 also contains three independent timers that can be used during the power-down control period. Different events and different time periods can be specified for each timer. Each timer will cause $\overline{\text{SMI}}$ to be asserted after the specified time period has expired. The three timers allow for more user-defined, power-down system states.

In order to identify the source of the $\overline{\text{SMI}}$ (System Management Interrupt), the CY82C599 maintains a status register (register 58) that keeps track of which event caused $\overline{\text{SMI}}$ to be asserted. Power-management software should read the status register before determining a course of action. The CPU and peripherals can be individually powered-down based on the source of the System Management Interrupt.

If any specified event is detected during Stand-by, Suspend, or any other power-down state, the CY82C599 will automatically return to the Full-speed state (with the stand-by timer reset). If the system is using software power management, the CY82C599 will assert $\overline{\text{SMI}}$ and within the $\overline{\text{SMI}}$ handler, software should bring all of the system clocks to their full-speed, full-power states through the de-assertion of $\overline{\text{STOPCLK}}$/$\overline{\text{SLOWCLK}}$.

10.0 Control Registers

This section summarizes the registers in the CY82C599.

The on-chip registers are accessed via I/O sequence 22H and 23H. Each register is selected by writing a byte containing the register address index to I/O address 22H. A subsequent byte read/write to I/O address 23H will modify/read-out the contents of the selected register.

The CY82C599 provides five groups of registers :

Memory address space configuration registers (except PC/AT high memory)

I/O address space configuration registers

Power down configuration registers

State machine configuration registers

PC/AT high memory address space configuration registers

The Local DRAM Address Configuration Registers are used to establish the boundary of the Local DRAM in the system. Index 20H and 21H are used to specify the ending address of on-board DRAMs. Index 22H to 27H are the configuration registers for Memory Blocks 0 and 1. They contain the base address of each memory block, the block sizes, and the mapping selection for each block : Local DRAM region, PCI region or ISA region. It is best to specify all Non-Local DRAM memory areas below 16Mbytes as ISA region and remap all other Non-Local DRAM memory areas above 2 Gbytes as the PCI region.

I/O Block Configuration Registers are used to specify the base address, block size, and function select for the user selectable I/O blocks. The pre-defined I/O blocks are simply enabled or disabled.

Power Down Configuration Registers allow various hardware events to be monitored in order to invoke or come out of power down mode.

State Machine configuration registers control features of the PCI and CPU bus State Machines. These features include the number of wait states, and arbitration priority of both State Machines.

PC/AT High Memory Address Space Configuration Registers are used to specify the memory regions from 000A0000H to 000FFFFFH (blocks A, B, C, D, E, and F). These bits are used with CY82C59/67 to provide shadowing in a PC/AT system.

Index 20H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3:0	Local DRAM Ending Address: $\overline{A27}$: $\overline{A24}$	0000	User selectable

Index 21H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Local DRAM Ending Address: $\overline{A23}$: $\overline{A16}$	00000000	User selectable

Index 22H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 0 Base Address: A31 : A24	00000000	User selectable

Index 23H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 0 Base Address: A23 : A16	0000000	User selectable

Index 24H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:6	Memory Block 0 Base Address: A15 : A14	00	User selectable
5:4	Memory Block 0 Function Select: 00: Disable (Default) 01: Local DRAM Region 10: PCI Region 11: ISA /VESA Region	00	User selectable
3:0	Memory Block 0 Size Select: 0000: 16KByte (Default) 0001: 32KByte 0010: 64KByte 0011: 128KByte 0100:: 256KByte 0101: 512KByte 0110: 1MByte 0111: 2MByte 1000: 4MByte 1001: 8MByte 1010: 16MByte 1011: 32MByte 1100: 64MByte 1110: 256MByte 1111: 512MByte	0000	User selectable

Index 25H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 1 Base Address: A31 : A24	00000000	User selectable

Index 26H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 1 Base Address: A23 : A16	00000000	User selectable

Index 27H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:6	Memory Block 1 Base Address: A15 : A14	00	User selectable
5:4	Memory Block 1 Function Select: 00: Disable (Default) 01: Local DRAM Region 10: PCI Region 11: ISA/VESA Region	00	User selectable
3:0	Memory Block 1 Size Select: 0000: 16KByte (Default) 0001: 32KByte 0010: 64KByte 0011: 128KByte 0100: 256KByte 0101: 512KByte 0110: 1MByte 0111: 2MByte 1000: 4MByte 1001: 8MByte 1010: 16MByte 1011: 32MByte 1100: 64MByte 1110: 256MByte 1111: 512MByte	0000	User selectable

Index 28H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Block 0 Base Address: A15 : A8	00000000	User selectable

Index 29H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	I/O Block 0 Base Address: A7 : A4	0000	User selectable
3:2	I/O Block 0 Function Select: 0X: Disable (Default) 10: PCI Region 11: ISA/VESA Region	00	User selectable
1:0	I/O Block 0 Size Select: 00: 16 Byte (Default) 01: 64 Byte 10: 256 Byte 11: 1024Byte	00	User selectable

Index 2AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Block 1 Base Address: A15 : A8	00000000	User selectable

Index 2BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	I/O Block 1 Base Address: A7 : A4	0000	User selectable
3:2	I/O Block 1 Function Select: 0X: Disable (Default) 10: PCI Region 11: ISA/VESA Region	00	User selectable
1:0	I/O Block 1 Size Select: 00: 16 Byte (Default) 01: 64 Byte 10: 256 Byte 11: 1024Byte	00	User selectable

Index 2CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Keyboard Detection Enable: 0: Disable 1: Enable	0	User selectable
6	Serial Port Detection Enable: 0: Disable 1: Enable	0	User selectable
5	Parallel Port Detection Enable: 0: Disable 1: Enable	0	User selectable
4	Hard Disk Detection Enable: 0: Disable 1: Enable	0	User selectable
3	CY82C599 Hold Detection Enable: 0: Disable 1: Enable	0	User selectable
2	Non Motherboard Memory Detection Enable: 0: Disable 1: Enable	0	User selectable
1	Non Motherboard I/O Detection Enable: 0: Disable 1: Enable	0	User selectable
0	Video RAM Detection Enable: 0: Disable 1: Enable	0	User selectable

Index 2DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved	0	0
6	Green Feature Timer Select (see Register 2DH, Bits 3:0).	0	User selectable
5	PCI Master Detection Enable: 0: Disable 1: Enable	0	User selectable
4	Floppy Disk Detection Enable: 0: Disable 1: Enable	0	User selectable
3:1	Green Feature Timer Delay Select: Bit 6=0 / Bit 6=1 000: 30 Second / 000: 0.2 Seconds 001: 4 Minute / 001: 0.4 Seconds 010: 8 Minute / 010: 1.0 Seconds 011: 16 Minute / 011: 1.8 Seconds 100: 32 Minute / 100: 3.5 Seconds 101: 65 Minute / 101: 7.0 Seconds 110: 130 Minute / 110: 14.0 Seconds 111: 260 Minute / 111: 30.0 Seconds	000	User selectable
0	Green Feature Enable 0: Disable 1: Enable	0	User selectable

Index 2EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Trap Address: IOA7 : IOA0	00000000	User selectable

Index 2FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3	I/O Trap Detection Enable: 0: Disable 1: Enable	0	User selectable
2	Reserved	0	0
1:0	I/O Trap Address: IOA9 : IOA8	00	User selectable

Index 30H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Function Enable: 0: Disable 1: Enable	0	1
6	Reserved	0	0
5	$\overline{\text{LRDY}}$ Delay Enable: 0: Disable 1: Enable	0	1
4	Reserved	0	0
3	Arbitration Fast Interface Enable: 0: Disable 1: Enable	0	0
2	PCI Hidden Arbitration Mode Enable: 0: Disable 1: Enable	0	0
1	Reserved	0	1
0	PCI Arbitration Rotate Priority Enable: 0: Disable (Fixed) 1: Enable (Rotating)	0	0

Index 31H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Reserved	00000000	00001000

Index 32H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Disable $\overline{\text{BOFF}}$ to CPU Control: 0: Disable 1: Enable	0	1
6:5	Reserved	00	01
4	CPU Master Post Write Buffer Enable: 0: Disable 1: Enable	0	1
3	CPU Master State Machine Fast Interface Enable: 0: Disable 1: Enable	0	0
2	CPU Master CPU State Machine Address 0WS Enable: 0: Disable (1 WS) 1: Enable (0 WS)	0	0
1	CPU Master CPU State Machine Data Write 0WS Enable: 0: Disable (1 WS) 1: Enable (0 WS)	0	0
0	CPU Master CPU State Machine Data Read 0WS Enable: 0: Disable (1 WS) 1: Enable (0 WS)	0	0

Index 33H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	CPU Master CPU State Machine I/O Post Write Cycle Enable: 0: Disable 1: Enable	0	0
6	Reserved	0	1
5:4	CPU Master PCI Retry: 00: Disable (Default) 01: 1 10: 3 11: Infinite	00	11
3	CPU Master Write Burst Mode Enable: 0: Disable 1: Enable	0	0
2	CPU Master PCI State Machine Fast Back-to-Back Enable: 0: Disable 1: Enable	0	0
1	CPU Master PCI State Machine Address OWS Enable: 0: Disable 1: Enable	0	0
0	CPU Master PCI State Machine Data Write OWS Enable: 0: Disable 1: Enable	0	0

Index 34H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved	0	0
6	PCI Master Post Write Buffer Enable: 0: Disable 1: Enable Note: Register 34 Bit 6 and Register 35, Bit4 together control the Post write funcitonality. See below for desired register settings. Reg. 34 Bit6 / Reg. Bit 4 / Function 0 / X / Non Burst, No Post-Write 1 / 0 / Non Burst, Post-Write 1 / 1 / Burst, Post-Write	0	0
5	Burst Pre-Read Enable: 0: Disable 1: Enable Note: Register 34 Bit 5 and Register 34, Bit4 together control the Burst Pre-Read funcitonality. See below for desired register settings. Reg. 34 Bit6 / Reg. Bit 4 / Function 0 / X / Burst Pre-Read Off 1 / 0 / Burst Pre-Read to Local Memory only. 1 / 1 / Burst Pre-Read to ISA, VESA, and Local memory	0	0
4	PCI Master Pre-read Buffer Enable: 0: Disable 1: Enable	0	0
3	PCI Master PCI State Machine VESA+ISA Post Write Enable: 0: Disable 1: Enable	0	0
2	PCI Master PCI State Machine Address 0WS Enable: 0: Disable (1 WS) 1: Enable (0 WS)	0	0
1	PCI Master CPU State Machine Address 0WS Enable: 0: Disable (1 WS) 1: Enable (0 WS)	0	0
0	PCI Master PCI State Machine Data Read 0WS Enable: 0: Disable (1 WS) 1: Enable (0 WS)	0	0

Index 35H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Master PCI State Machine Data Write 0WS Enable: 0: Disable 1: Enable	0	0
6	PCI Master PCI State Machine Burst Mode Enable: 0: Disable 1: Enable	0	0
5	PCI Master State Machine Fast Interface Enable: 0: Disable 1: Enable	0	0
4	PCI Master State Machine Generate Fast $\overline{ADS}$ Cycle Enable: 0: Disable 1: Enable Note: See register 34, Bit6.	0	0
3:2	CPU Master PCI $\overline{DEVSEL}$ Time Out Period: 00: 6 PCICLK (Default) 01: 5 PCICLK 10: 4 PCICLK 11: 3 PCICLK	00	00
1:0	PCI Master PCI Subtractive Decode $\overline{DEVSEL}$ Time Out Period: 00: 6 PCICLK (Default) 01: 5 PCICLK 10: 4 PCICLK 11: 3 PCICLK	00	10

Note: PCI Master PCI Subtractive Decode $\overline{DEVSEL}$ Time Out Period must be equal or less than CPU Master PCI $\overline{DEVSEL}$ Time Out Period

Index 36H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Configuration Address Cycle Enable: 0: Disable 1: Enable	0	1
6	Configuration Data Cycle Enable: 0: Disable 1: Enable	0	1
5	Configuration Data Special Cycle Enable: 0: Disable 1: Enable	0	1
4	PCI Master Configuration Address Cycle Enable: 0: Disable 1: Enable	0	0
3	Reserved	0	0
2	Reserved	0	0
1	First Level Arbitration Rotate Enable: 0: Disable 1: Enable	0	0
0	Reserved	0	1

Index 37H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:3	Reserved	00000	11111
2	Configuration Register TARGET ABORT Status Bit Enable: 0: Disable 1: Enable	0	0
1	$\overline{\text{PERR}}$ External Support Enable: 0: Disable 1: Enable	0	0
0	$\overline{\text{SERR}}$ External Support Enable: 0: Disable 1: Enable	0	0

Index 38H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block A0000h : A7FFFh Bits 7:6 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	0000
3:0	Shadow Block A8000h : AFFFFh Bits 3:2 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	1010

Index 39H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block B0000h : B7FFFh Bits 7:6 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	User selectable
3:0	Shadow Block B8000h : BFFFFh Bits 3:2 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	User selectable

Index 3AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block C0000h : C3FFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block C4000h : C7FFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block C8000h : CBFFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block CC000h : CFFFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D0000h : D3FFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block D4000h : D7FFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D8000h : DBFFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block DC000h : DFFFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D8000h : EFFFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block F0000h : FFFFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3:2	Pin 16,17 Function Select: Bits 3:2 Function: 00: Disabled 01: A30, A29 enabled 10: $\overline{\text{INTLI}}/\overline{\text{INTEO}}$ enable 11: Invalid condition, do not use.	00	User selectable
1:0	Pin 18 function Select: Bits 1:0 Function: 00: Disabled 01: A28 enabled 10: SLOWCLK enable 11: Invalid cond:ition, do not use.	00	User selectable

Index 40H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved. Must be set to 1 after power-on.	0	1
6	Reserved.	0	1
5	Reserved, Must be set to 1 after power-on.	0	1
4	I/O write 22H, 23H, & 61H $\overline{\text{LDEV}}$ mask enable.	0	0
3	Reserved, must be set to 1 after power-on.	0	1
2	Configuration register Read Enable: 0: Write only. 1: Read/Write.	0	1
1	Monitor VESA VL Bus $\overline{\text{LDEV}}$ enable.	0	0
0	VESA to PCI Stand Alone enable.	0	0

Index 41H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	VESA VL Bus $\overline{\text{BS16}}$ support enable.	0	0
6:0	Reserved	0000000	0010111

Index 42H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved.	0000	0001
3	Write back mode with no PCI Master HOLD support enable.	0	0
2:1	Reserved, set to 0 after power-on.	00	00
0	Level 1 Write back mode enable.	0	0

Index 43H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	$\overline{\text{LRDY}}$ delay 1 CPUCLK enable.	0	0
6:0	Reserved	0000000	0000000

Index 44H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Not used, available for BIOS storage.	00000000	00000000

Index 45H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Not used, available for BIOS storage.	00000000	00000000

Index 46H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Memory Block 2 Enable (A31=1, A27=0, A26=1J): Bits 0: Disable 1: Enable	0	1
6:4	PCI Memory Block 2 Address Select A30, A29, A28	000	000
3	PCI Memory Block 3 Enable (A31=1, A27=1, A26=0): Bits 0: Disable 1: Enable	0	1
2:0	PCI Memory Block 2 Address Select A30, A29, A28	000	000

Index 47H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	PCI I/O Block 2 base address A15–A12. Note: A15–A12=0H disable PCI I/O block 2.	0000	0000
3	Reserved. Set to 0.	0	0
2:1	PCI I/O block 2 size select S1-S0.: S1 S0 Size. 0 0 1KB 0 1 2KB 1 0 4KB 1 1 8KB	00	00
0	PCI I/O block 2 enable.	0	0

Index 48H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0100H to 010FH select enable.	0	User selectable
6	ISA/VESA I/O space 0110H to 011FH select enable.	0	User selectable
5	ISA/VESA I/O space 0120H to 012FH select enable.	0	User selectable
4	ISA/VESA I/O space 0130H to 013FH select enable.	0	User selectable
3	ISA/VESA I/O space 0140H to 014FH select enable.	0	User selectable
2	ISA/VESA I/O space 0150H to 015FH select enable.	0	User selectable
1	ISA/VESA I/O space 0160H to 016FH select enable.	0	User selectable
0	ISA/VESA I/O space 0170H to 017FH select enable.	0	User selectable

Index 49H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0180H to 018FH select enable.	0	User selectable
6	ISA/VESA I/O space 0190H to 019FH select enable.	0	User selectable
5	ISA/VESA I/O space 01A0H to 01AFH select enable.	0	User selectable
4	ISA/VESA I/O space 01B0H to 01BFH select enable.	0	User selectable
3	ISA/VESA I/O space 01C0H to 01CFH select enable.	0	User selectable
2	ISA/VESA I/O space 01D0H to 01DFH select enable.	0	User selectable
1	ISA/VESA I/O space 01E0H to 01EFH select enable.	0	User selectable
0	ISA/VESA I/O space 01F0H to 01FFH select enable.	0	User selectable

Index 4AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0200H to 020FH select enable.	0	User selectable
6	ISA/VESA I/O space 0210H to 021FH select enable.	0	User selectable
5	ISA/VESA I/O space 0220H to 022FH select enable.	0	User selectable
4	ISA/VESA I/O space 0230H to 023FH select enable.	0	User selectable
3	ISA/VESA I/O space 0240H to 024FH select enable.	0	User selectable
2	ISA/VESA I/O space 0250H to 025FH select enable.	0	User selectable
1	ISA/VESA I/O space 0260H to 026FH select enable.	0	User selectable
0	ISA/VESA I/O space 0270H to 027FH select enable.	0	User selectable

Index 4BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0280H to 028FH select enable.	0	User selectable
6	ISA/VESA I/O space 0290H to 029FH select enable.	0	User selectable
5	ISA/VESA I/O space 02A0H to 02AFH select enable.	0	User selectable
4	ISA/VESA I/O space 02B0H to 02BFH select enable.	0	User selectable
3	ISA/VESA I/O space 02C0H to 02CFH select enable.	0	User selectable
2	ISA/VESA I/O space 02D0H to 02DFH select enable.	0	User selectable
1	ISA/VESA I/O space 02E0H to 02EFH select enable.	0	User selectable
0	ISA/VESA I/O space 02F0H to 02FFH select enable.	0	User selectable

Index 4CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0300H to 030FH select enable.	0	User selectable
6	ISA/VESA I/O space 0310H to 031FH select enable.	0	User selectable
5	ISA/VESA I/O space 0320H to 032FH select enable.	0	User selectable
4	ISA/VESA I/O space 0330H to 033FH select enable.	0	User selectable
3	ISA/VESA I/O space 0340H to 034FH select enable.	0	User selectable
2	ISA/VESA I/O space 0350H to 035FH select enable.	0	User selectable
1	ISA/VESA I/O space 0360H to 036FH select enable.	0	User selectable
0	ISA/VESA I/O space 0370H to 037FH select enable.	0	User selectable

Index 4DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0378H to 037FH select enable.	0	User selectable
6	ISA/VESA I/O space 0380H to 038FH select enable.	0	User selectable
5	ISA/VESA I/O space 0390H to 039FH select enable.	0	User selectable
4	ISA/VESA I/O space 03A0H to 03AFH select enable.	0	User selectable
3	ISA/VESA I/O space 03B0H to 03BBH select enable.	0	User selectable
2	ISA/VESA I/O space 03BCH to 03BFH select enable.	0	User selectable
1	ISA/VESA I/O space 03C0H to 03CFH select enable.	0	User selectable
0	ISA/VESA I/O space 03D0H to 03DFH select enable.	0	User selectable

Index 4EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 03E0H to 03E7H select enable.	0	User selectable
6	ISA/VESA I/O space 03E8H to 03EFH select enable.	0	User selectable
5	ISA/VESA I/O space 03F0H to 03F5H select enable.	0	User selectable
4	ISA/VESA I/O space 03F6H to 03F7H select enable.	0	User selectable
3	ISA/VESA I/O space 03F8H to 03FFH select enable.	0	User selectable
2	ISA/VESA I/O space 0000H to 00FFH select enable.	0	User selectable
1	ISA/VESA I/O space ignore A15:10 decode enable.	0	User selectable
0	ISA/VESA I/O space C.R. 48H-4EH overall enable.	0	User selectable

Index 4FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI I/O space 01F0H to 01FFH select enable.	0	User selectable
6	PCI I/O space 03F6H to 03F7H select enable.	0	User selectable
5	PCI I/O space 0170H to 017FH select enable.	0	User selectable
4	PCI I/O space 0370H to 0377H select enable.	0	User selectable
3	PCI I/O space 03B0H to 03BBH select enable.	0	User selectable
2	PCI I/O space 03C0H to 03CFH select enable.	0	User selectable
1	PCI I/O space 03D0H to 03DFH select enable.	0	User selectable
0	PCI I/O space 03F0H to 03F5H select enable.	0	User selectable

Register 50: Suspend Timer and Interrupt Timer Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits (Suspend Timer Period) 0000: 3.8 min. 0001: 7.5 min. 0010: 15 min. 0011: 30 mins. 0100: 60 mins. 0101: 120 mins. 0110: 240 mins. 0111: 480 mins. 0000: 1 sec. 1001: 1.8 sec. 1010: 3.5 sec. 1011: 7 sec. 1100: 14 sec. 1101: 28 sec. 1110: 56 sec. 1111: 2 min.	0000	User selectable
3:0	Bits (Interrupt Timer Period) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 54 µsec. 0110: 107 µsec. 0111: 215 µsec. 0000: 430 µsec. 1001: 860 µsec. 1010: 1.7 msec. 1011: 3.4 msec. 1100: 7 msec. 1101: 14 msec. 1110: 28 msec. 1111: 55 msec.	0000	User selectable

The suspend timer is enabled when register 52 bit 1=0. When enabled, the suspend timer always follows the stand-by timer (i.e., it will not start counting until the stand-by timer has reached its terminal count. For hardware Power-down mode, the 82C599 will assert $\overline{\text{STOPCLK}}$ after the suspend timer has reached its terminal count. For software Power-down mode, the 82C599 will generate an $\overline{\text{SMI}}$ after its terminal count $\overline{\text{STOPCLK}}$ and other power-down features can be implemented in an $\overline{\text{SMI}}$ subroutines.

When the INTR input becomes active, the 82C599 will deassert $\overline{\text{STOPCLK}}$ and start the interrupt timer. After the interrupt timer reaches its terminal count, the 82C599 will assert $\overline{\text{STOPCLK}}$ again (if no event occurs during the interrupt period). This timer is used for both hardware and software Power-down modes and is enabled by register 51, Bit 2.

Hardware Power-down mode allows $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ to be controlled by the 82C599 hardware. Software Power-down mode will use System Management Mode ($\overline{\text{SMM}}$) subroutines to implement power-down control.

Register 51: Power-down Mode

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable hardware Power-down mode 1: Enable hardware Power-down mode	0	User selectable
6	Bits 0: Disable software Power-down mode 1: Enable software Power-down mode	0	User selectable
5	Bits 0: Disable interrupt input (INTR) 1: Enable interrupt input (INTR) Should be 1 when Power-down mode	0	User selectable
4	Should be 0	0	0
3	Bits 0: $\overline{\text{SLOWCLK}}$ does not change when input INTR active 1: $\overline{\text{SLOWCLK}}$ will be inactive when input INTR active	0	User selectable
2	Bits 0: Enable interrupt timer (default) 1: Disable interrupt timer	0	User selectable
1	Reserved.	0	0
0	Must have the same value as bit 6.	0	See bit 6.

Register 52: Power-Down Mode Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits Software initial $\overline{SMI}$ 0: Normal 1: Writing an 1 to this bit will generate an $\overline{SMI}$ to the CPU. After a 1 is written, software should write a 0 to this bit.	0	User selectable
6	Bits $\overline{SMI}$ inactive control 0: Normal 1: Writing a 1 to this bit will deassert the $\overline{SMI}$ signal. This is the only way to cause the 82C599 to deassert $\overline{SMI}$. After a 1 is written, 0 should be written to this bit to allow $\overline{SMI}$ to be deasserted.	0	User selectable
5	Bits $\overline{STOPCLK}$ Active Control 0: Normal 1: Writing a 1 to this bit will assert the $\overline{STOPCLK}$ signal. Software should subsequently write a 0 to this bit to allow $\overline{STOPCLK}$ to be deasserted.	0	User selectable
4	Bits Software $\overline{STOPCLK}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{STOPCLK}$. Software should subsequently write a 0 to this bit to allow $\overline{STOPCLK}$ to be asserted.	0	User selectable
3	Bits Software $\overline{SLOWCLK}$ Active Control 0: Normal 1: Writing a 1 will assert $\overline{SLOWCLK}$. Software should subsequently write a 0 to this bit to allow $\overline{SLOWCLK}$ to be deasserted.	0	User selectable
2	Bits Software $\overline{SLOWCLK}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{SLOWCLK}$. Software should subsequently write a 0 to this bit to allow $\overline{SLOWCLK}$ to be asserted.	0	User selectable
1	Bits Suspender Time Control 0: Enable suspend timer (default) 1: Disable suspend timer The 82C599 allows a second Suspend mode to be started after the current suspend timer has reached its terminal count (i.e. When the current suspend timer expires, it will assert $\overline{SMI}$.) Within the $\overline{SMI}$ subroutine, the suspend timer can be disabled and the suspend timer reenabled. After the new terminal count has been reached, the 82C599 will initiate another $\overline{SMI}$.	0	User selectable
0	Bits Disable Software Reset Mask 0: Normal 1: Force CY82C599 to inactivate pin 112. This bit should be set to "1", then set to "0" before leaving SMI subroutine.	0	0

Register 53: Power Management Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved.	0000	0000
3	Bits 0: Normal 1: Enable power down LED to flush when 82C599 is in power down mode. CY82C599 uses pin 60 to control LED.	0	User selectable
2	Bits 0: LED is active HIGH 1: LED is active LOW.	0	User selectable
1	Bits 0: INTEL SMM mode 1: CYRIX/AMD SMM mode.	0	User selectable
0	Reserved	0000	0000

Register 54: Special Memory and I/O Event Detection

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory cycle: memory address A31, A26, A25, A24, A23, A22, A21, A20 detection. I/O cycle: I/O address A7, A6, A5, A4, A3, A2, A1, A0 detection.	0	User selectable

Register 55: Special Memory and I/O Event Detection

Bit	Memory Cycle	I/O Cycle	Hardware Default	Recommended BIOS power-on setting
7	Mask A31	A15	0	User selectable
6	Mask A26	A14	0	User selectable
5	Mask A25	A13	0	User selectable
4	Mask A24	A12	0	User selectable
3	Mask A23	A11	0	User selectable
2	Mask A22	A10	0	User selectable
1	Mask A21	A9	0	User selectable
0	Mask A20	A8	0	User selectable

Register 56: Special Memory and I/O Event Detection

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable special memory I/O detection 1: Enable special memory I/O detection	0	User selectable
6	Bits 0: Detect I/O cycle 1: Detect memory cycle	0	User selectable
5	Bits 0: No write cycle detection 1: Detect write cycle	0	User selectable
4	Bits 0: No read cycle detection 1: Detect ready cycle	0	User selectable
3	I/O address A19.	0	User selectable
2	I/O address A18.	0	User selectable
1	I/O address A17.	0	User selectable
0	I/O address A16.	0	User selectable

Registers 54, 55, and 56 allow for special memory or I/O event detection. For memory detection, address A31, A26, A25, A24, A23, A22, A21, and A20 are monitored. Memory detection can also be limited to read cycles or write cycles. Certain memory addresses can also be masked. (Register 55) If the corresponding mask bit (e.g. mask A20) is set, then address (A20) will not be decoded. For I/O detection, addresses A19–A0 can be monitored. I/O detection can also be limited to read-only or write-only. I/O detection does not allow for address masking.

Register 57: Power Down Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved.	0	0
6:5	Bits (LED frequency control) 00: 0.4 sec. 01: 1.0 sec. 10: 1.8 sec. 11: 3.5 sec.	0	User selectable
4	Bits Quick Power Down control 0: Disable Quick Power Down mode. 1: Enable Quick Power Down mode.	0	User selectable
3:0	Reserved.	0	0

The 82C599 supports Quick Power Down through pin 18. When pin 18 is selected, the CY82C599 will bring itself into Power Down Mode in 3 seconds if no event is detected, and Register 57, Bit 4=1.

Register 58: 82C599 Status Register

Read Cycle:	Set A	Set B
7=1	SMI caused by start of stand-by mode.	Reserved.
6=1	SMI caused by end of stand-by mode.	Reserved.
5=1	SMI caused by suspend timer reaching its terminal count.	82C599 is in power-down mode (stand-by or suspend mode)
4=1	SMI caused by register 52, bit 7.	82C599 is in suspend mode. Once in suspend mode, this bit will stay 1 unless any suspend event becomes active, or power-down mode is disabled.
3=1	SMI caused by timer 3 reaching its terminal count.	$\overline{\text{STOPCLK}}$ pin is active
2=1	SMI caused by timer 3 reset by an event.	$\overline{\text{SLOWCLK}}$ pin is active
1=1	SMI caused by timer 4 reaching its terminal count.	Suspend timer has reached its terminal count. It will be 0 if register 52, bit 1 is set to 1 later.
0=1	SMI caused by timer 4 reset by an event.	$\overline{\text{SMI}}$ pin is active

The CY82C599 has two status registers (16 bits total) that can be read through register 58. Writing a 0 into bit 7 will cause A status set to be read on a read cycle. Writing a 1 into bit 7 will cause B status set to be read on a read cycle.

Register 58 contains the source of an $\overline{\text{SMI}}$ and some internal status. The status can be used to power-down/power-up individual system devices (monitor, CPU, hard disk, etc.).

Register 59: Power-Down Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved.	0	0
6	Bits Timer 4 event control 0: Norml 1: Timer 4 will ignore all events (once enabled, timer 4 will start counting until it reaches the specified terminal count).	0	User selectable
5	Bits SMI retry timer 0: Disable SMI retry timer 1: Enable SMI retry timer	0	User selectable
4:3	Bits SMI retry timer terminal count 00: 55 msec. 01: 0.2 msec 10: 1 sec. 11: 3.5 sec Once the SMI retry timer is enabled and any system manage ment interrupt ($\overline{\text{SMI}}$) is active longer than the value specified by $\overline{\text{SMI}}$ retry timer, the 82C599 will generate a new $\overline{\text{SMI}}$.	0	User selectable
2	Bits $\overline{\text{STOPCLK}}$ timer control 0: Disable $\overline{\text{STOPCLK}}$ timer 1: Enable $\overline{\text{STOPCLK}}$ timer	0	User selectable
1:0	Bits $\overline{\text{STOPCLK}}$ timer 00: 430 µsec. 01: 860 µsec. 10: 1.7 msec. 11: 7 msec. In software power-down mode, the assertion of $\overline{\text{STOPCLK}}$ can be delayed. The delay time is determined by $\overline{\text{STOPCLK}}$ timer.	0	User selectable

Register 5A: Timer 3 Event Detection Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0	User selectable
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0	User selectable
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0	User selectable
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0	User selectable
3	DMA/ISA master / AT refresh detection: 0: Disable DMA/ISA master / AT refresh detection 1: Enable DMA/ISA master / AT refresh detection	0	User selectable
2	Bits 0: Disable non-motherboard memory detection 1: Enable non-motherboard memory detection	0	User selectable
1	Bits 0: Disable access floppy detection 1: Enable access floppy detection	0	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0	User selectable

Index 5B: Timer 3 Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0	User selectable
3	Bits 0: Disable timer 3 1: Enable timer 3	0	User selectable
2	Bits 0: Disable special memroy I/O event detection (please see register 54, 55, and 56) 1: Enable special memory I/O event detection	0	User selectable
1	Bits 0: Disable I/O event detection 1: Enable I/O event detection (see Register 2EH and 2FH)	0	User selectable
0	Bits 0: Disable PCI/VESA master event detection 1: Enable PCI/VESA master event detection	0	User selectable

Index 5C: Timer 4 Event Detection Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0	User selectable
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0	User selectable
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0	User selectable
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0	User selectable
3	Bits 0: Disable DMA/ISA master / AT refresh event detection 1: Enable DMA/ISA master / AT refresh event detection	0	User selectable
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0	User selectable
1	Floppy Access Detection: 0: Disable Floppy Disk Detection 1: Enable Floppy Disk Detection	0	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0	User selectable

Index 5D: Timer 4 Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0	User selectable
3	Bits 0: Disable timer 4 1: Enable timer 4	0	User selectable
2	Bits 0: Disable special memroy I/O event detection (please see register 54, 55, and 56) 1: Enable special memory I/O event detection	0	User selectable
1	Bits 0: Disable I/O event detection (Please see register 2E, 2F) 1: Enable I/O event detection	0	User selectable
0	Bits 0: Disable PCI/VESA master event detection 1: Enable PCI/VESA master event detection	0	User selectable

Index 5E

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Reserved	00000000	00000000

Index 5F: Timer 5 Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Reserved	00000000	00000000

CY82C599 Pin Descriptions

PCI Interface

Name	I/O	Pin Number	Description
AD[31:0]	I/O	120, 122-128, 131-138, 152-160, 3-9	PCI Address and Data bus. During the address phase, AD[31:0] contain a physical address. During data phase, it contains 32-bit data.
$\overline{\text{CBE}}$[3:0]	I/O	129, 139, 151, 2	Bus Command and Byte Enables are multiplexed.
PAR	I/O	147	Parity is even parity across AD[31:0].
$\overline{\text{FRAME}}$	I/O	140	Cycle Frame is driven by the current master to indicate the beginning and duration of an access.
$\overline{\text{IRDY}}$	I/O	141	Initiator Ready indicates the master's ability to complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	I/O	142	Target Ready indicates the target agent's ability to complete the current data phase of the transaction.
$\overline{\text{STOP}}$	I/O	148	Stop indicates the current target is requesting the master to stop the current transaction.
$\overline{\text{REQ}}$[3:0]	I	11, 117, 118, 119	Request indicate to the arbiter that this agent desires of the bus.
$\overline{\text{GNT}}$[3:0]	O	10, 114, 115, 116	Grant indicate to the agent that access to the bus has been granted.
$\overline{\text{RST}}$	I	113	Reset.
PCICLK	I	12	Clock to every PCI device.
$\overline{\text{PCILOCK}}$	I/O	149	Lock indicates an atomic operation that may require multiple transactions to complete.
$\overline{\text{DEVSEL}}$	I/O	143	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current address. As an input, it indicates whether any device on the bus has been selected.
$\overline{\text{SERR}}$	I	145	System Error.
$\overline{\text{PERR}}$	I	144	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle.

CPU Interface

Name	I/O	Pin Number	Description
A31	I/O	13	Address bit 31.
A[27:2]	I/O	15, 19, 21-25, 27-36, 38-40, 42-43, 45-47, 44	Address bit 27 to 2.
$\overline{\text{SLOWCLK}}$/A28 /$\overline{\text{QPD}}$	I/O	18	Slow down clock signal. As and output, it can be used to control clock generator to slow down 486 CPU clock if power saving feature is supported. As an input, performed the quick power-down function. Or Address pin 28.
$\overline{\text{INTEO}}$/A29	I/O	17	Edge-triggered Interrupt Output or Address pin 29.
$\overline{\text{INTLI}}$/A30	I/O	16	Level-sensitive Interrupt input from PCI bus, or Address pin 30.
$\overline{\text{BE}}$[3:0]	I/O	80, 82, 83, 84	CPU Byte Enable.
D[31:0]	I/O	72-79, 85-91, 93-99, 101, 103-111	Data bit 31 to 0.
CPUCLK	I	59	Clock for CPU.
$\overline{\text{ADS}}$	I/O	71	CPU Address Strobe.
$\overline{\text{MIO}}$	I/O	48	CPU Memory/IO cycle status.
$\overline{\text{WR}}$	I/O	49	CPU Read/Write status.
$\overline{\text{DC}}$	I/O	53	CPU Data/Code status.
$\overline{\text{CPURDY}}$	I/O	52	Ready output to terminate CPU master cycle. Ready input to terminate PCI master cycle.
$\overline{\text{BLAST}}$	I/O	55	Burst Last signal indicates the completion of the burst cycle when the next $\overline{\text{BRDY}}$ is returned.
$\overline{\text{BRDY}}$	I/O	54	Burst Ready, when actively driven, indicates the end of burst transfer to CPU. As an input, it terminates PCI master cycle.
$\overline{\text{EADS}}$	O	56	External Address Strobe output to CPU.
$\overline{\text{BOFF}}$/LED	O	60	Back Off output to back off CPU cycle, or Jumper. Resistor to ground places device in Stand-Alone mode, pull-up resistor places in normal mode.
$\overline{\text{LIMCS}}$/INTR/ $\overline{\text{LDEVI}}$	I/O	66	Multifunctional pin. As input, connect INTR signal from 82C206 or other VESA $\overline{\text{LDEV}}$ in stand-alone mode. As output, it drives $\overline{\text{LIMCS}}$ signal. $\overline{\text{LDEV}}$ input from other VESA devices in stand-alone mode.
NMI	O	26	Non-maskable interrupt output.
$\overline{\text{STPCLK}}$	O	62	Stop Clock signal. Connect to 486 CPU to turn off the CLK input.

Miscellaneous

Name	I/O	Pin Number	Description
OSC/$\overline{\text{HITM}}$	I/O	58	Multifunctional pin. As OSC, connect to 14.31818MHz clock for the internal timer. As $\overline{\text{HITM}}$, connect to the $\overline{\text{HITM}}$ pin of 486.
OSC119/$\overline{\text{SMI}}$	I/O	57	Multifunctional pin. As output, it drives 1.19MHz clock output. As $\overline{\text{SMI}}$, connect to System Management Interupt pin of the 486.
$\overline{\text{SMIMASK}}$/ STATUS	O	63	Connect to $\overline{\text{IOCHCK}}$ signal of CY82C597. Jumper selects Synchronous or Asynchronous mode. Resistor to ground places device in Synchronous mode, pull-up resistor places in Asynchronous mode.
$\overline{\text{LDEV}}$	O	51	Local Device signal output.
$\overline{\text{LRDY}}$/$\overline{\text{LBS16}}$	I	61	Connect to LRDY signal from VESA local bus or LBS16 signal from the VESA bus.

Arbitration

Name	I/O	Pin Number	Description
CPUHLDA	I	67	Input from CPU HLDA signal.
CPUHOLD	O	68	Output to CPU HOLD signal.
C597HOLD	I	69	Input from 82C597 HOLD signal.
C597HLDA	O	65	Output to 82C597 HLDA signal.

Ground and V_{CC}

Name	I/O	Pin Number	Description
V_{CC}	I	20, 41, 64, 100, 121, and 146	+5V power supply
GND	I	1, 14, 37, 50, 70, 81, 92, 102, 112, 130, and 150	Ground

CY82C599 DC Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... +7 V

Ambient Operating Temperature ..... −25°C to +70°C

Ambient Storage Temperature ..... −40°C to 125°C

DC Voltage Applied to Outputs ..... −0.5V to +5.5V

DC Input Voltage ..... −0.5V to +5.5V

Electrical Characteristics Over the Operating Range (0°C to 70°C, V_{CC} = +5V ± 5%)

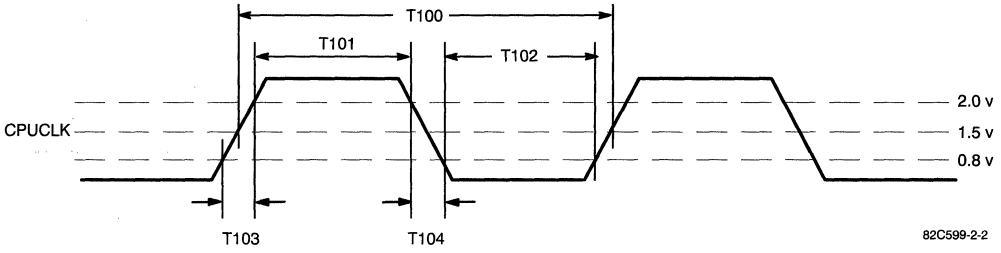
Parameter	Description		CY82C599 Min.	CY82C599 Max.	Unit
V_{IL}	Input LOW Voltage		−.05	0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}+0.5	V
V_{OL}	Output LOW Voltage			0.4	V
V_{OH}	Output HIGH Voltage		2.4		V
I_{IL}	Input Leakage Current			10	µA
I_{OL}	Output Leakage			10	µA
C_{IN}	Input Capacitance			10	pF
C_{OUT}	Output Capacitance			10	pF
I_{CC}	Power Supply Current	33 MHz		100	mA

Switching Characteristics

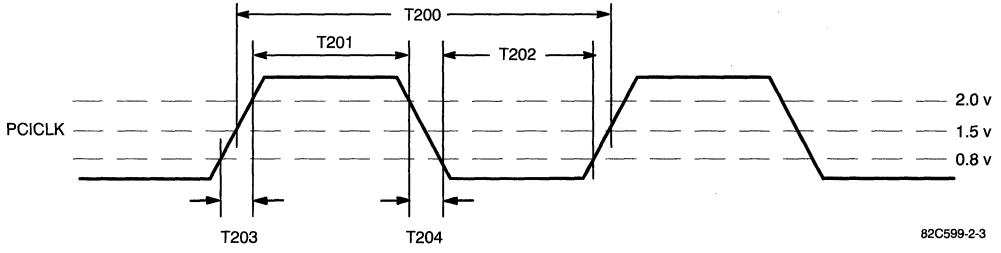
Parameter	Description	CY82C599 Min.	CY82C599 Max.	Unit
CPU CLOCK TIMING				
T_{100}	CPUCLK Period	20		ns
T_{101}	CPUCLK HIGH time at 2.0V	7		ns
T_{102}	CPUCLK LOW time at 0.8V	7		ns
T_{103}	CPUCLK rise time		2	ns
T_{104}	CPUCLK fall time		2	ns
PCI CLOCK TIMING				
T_{200}	PCICLK Period	25		ns
T_{201}	PCICLK HIGH time at 2.0V	10		ns
T_{202}	PCICLK LOW time at 0.8V	10		ns
T_{203}	PCICLK rise time		4	ns
T_{204}	PCICLK fall time		4	ns
CPU BUS INTERFACE TIMING				
T_{300}	CPUCLK Rise to data out VALID A[31:2], INTEQ, INTLI, BE[3:0], D[31:0], ADS, M/IO, W/R, D/C, CPURDY, BLAST, BRDY, EADS, BOFF, L1MCS, NMI, STOPCLK, SLOWCLK and control signals to the CY82C596/7.		15	ns
T_{301}	CPUCLK Rise to data out HOLD A[31:2], INTEQ, INTLI, BE[3:0], D[31:0], ADS, M/IO, W/R, D/C, CPURDY, BLAST, BRDY, EADS, BOFF, L1MCS, NMI, STOPCLK, SLOWCLK and control signals to the CY82C596/7.	2		ns
T_{302}	Input SET-UP to CPUCLK Rise A[31:2], INTEQ, INTLI, BE[3:0], D[31:0], ADS, M/IO, W/R, D/C, CPURDY, BLAST, BRDY, EADS, BOFF, L1MCS, NMI, STOPCLK and control signals to the CY82C596/7.	5		ns
T_{303}	Input HOLD to CPUCLK Rise A[31:2], INTEQ, INTLI, BE[3:0], D[31:0], ADS, M/IO, W/R, D/C, CPURDY, BLAST, BRDY, EADS, BOFF, L1MCS, NMI, STOPCLK and control signals to the CY82C596/7.	2		ns
PCI BUS INTERFACE TIMING				
T_{400}	PCICLK Rise to data out VALID AD[31:0], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, GNT, PCILOCK, DEVSEL.		18	ns
T_{401}	PCICLK Rise to data out HOLD AD[31:0], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, GNT, PCILOCK, DEVSEL.	2		ns
T_{402}	Input SET-UP to PCICLK Rise AD[31:0], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, GNT, PCILOCK, DEVSEL, REQ[3:0], RST, SERR, PERR.	5		ns
T_{403}	Input HOLD to PCICLK Rise AD[31:0], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, GNT, PCILOCK, DEVSEL, REQ[3:0], RST, SERR, PERR.	0		ns

Switching Waveforms

CPUCLK Timing

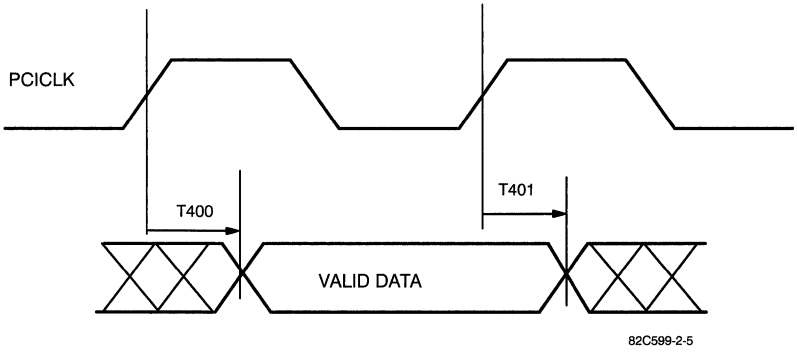


PCICLK Timing

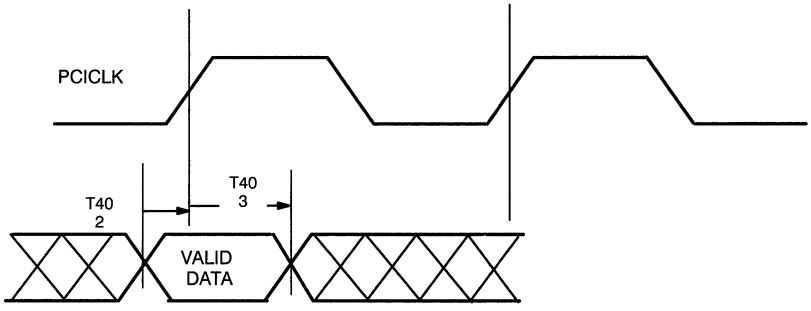


Switching Waveforms (continued)

PCI BUS INTERFACE TIMING



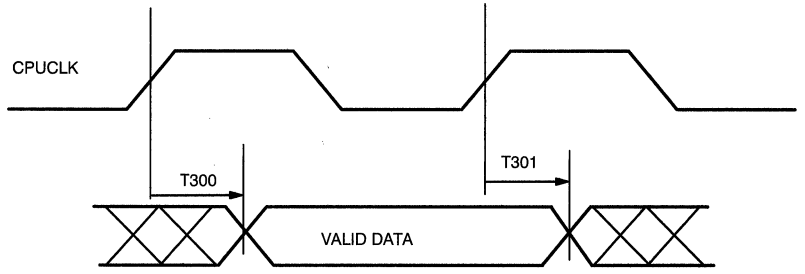
82C599-2-5



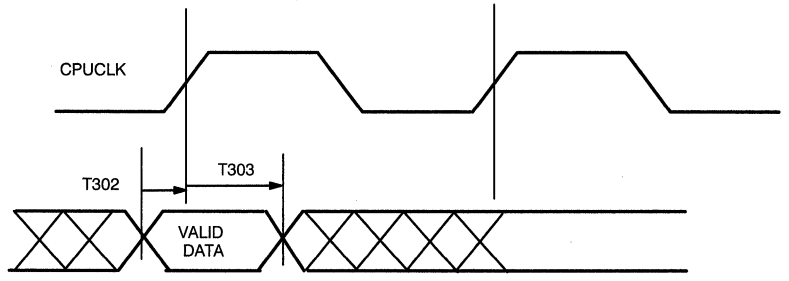
82C599-2-4

Switching Waveforms (continued)

CPU BUS INTERFACE TIMING



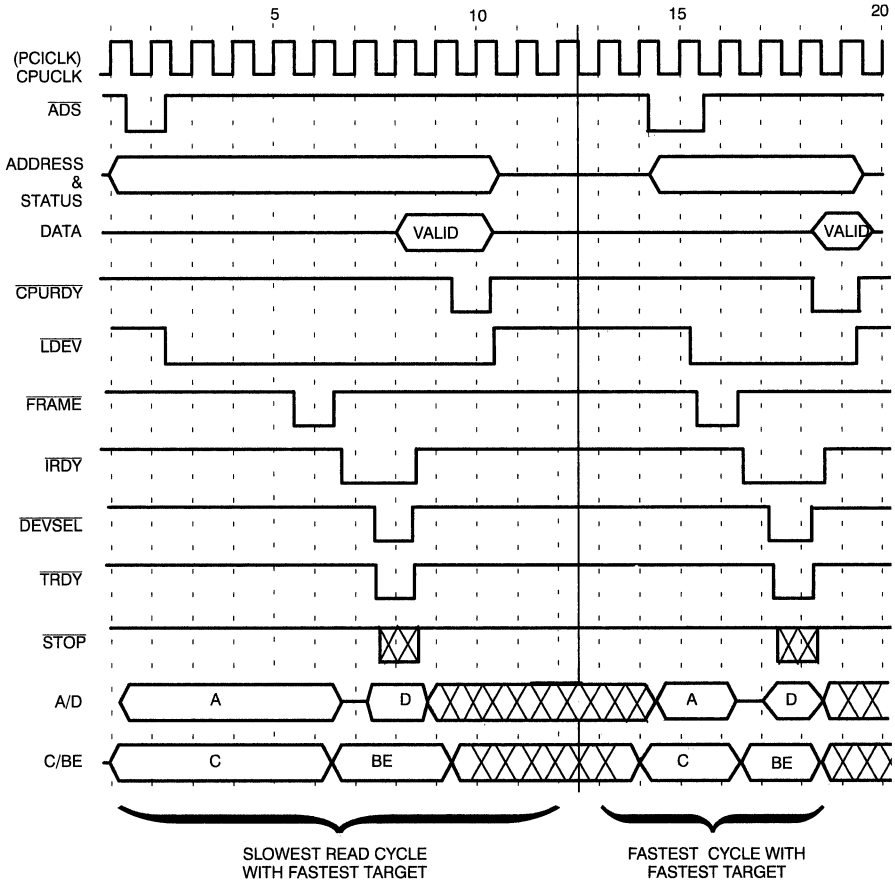
82C599-2-7



82C599-2-6

Switching Waveforms (continued)

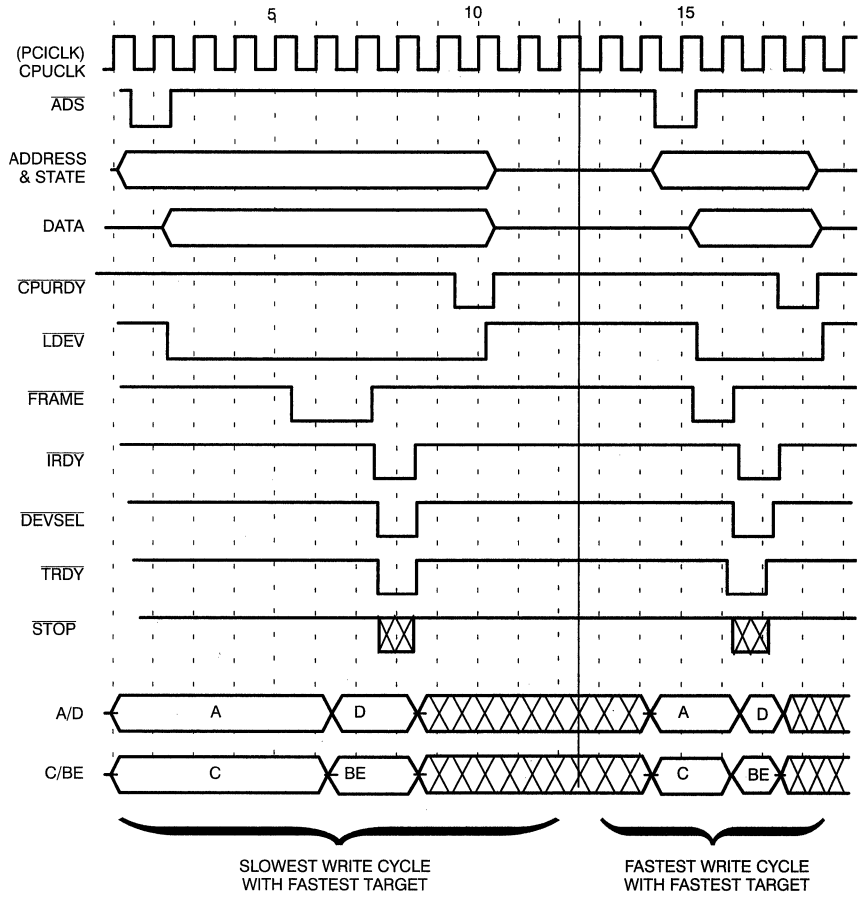
CPU Master Read PCI Target



82C599-2-8

Switching Waveforms (continued)

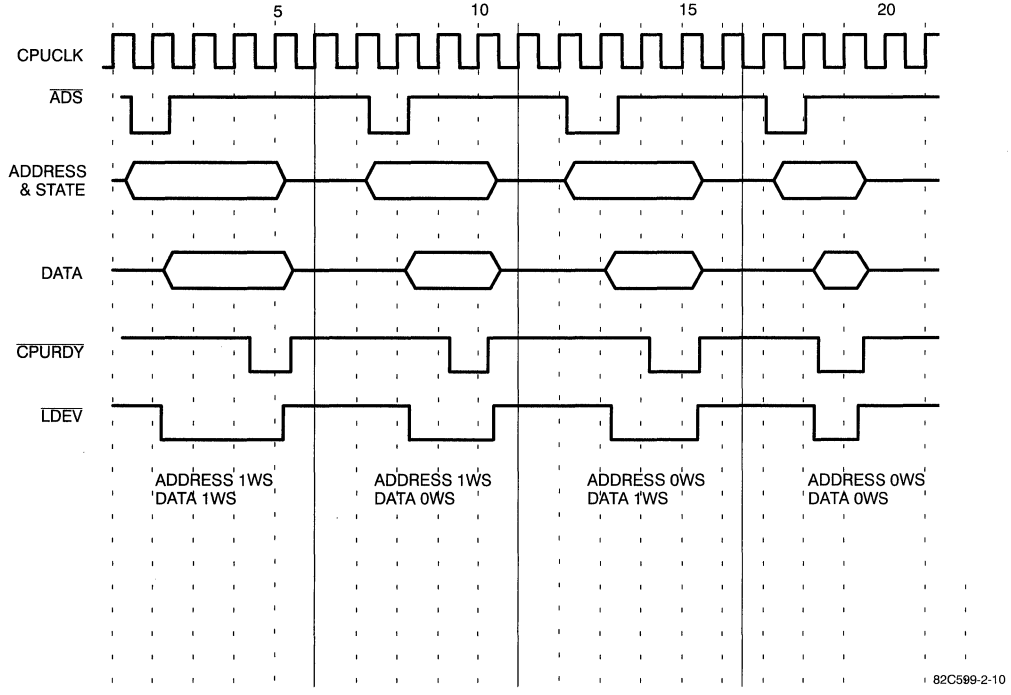
CPU Master Write PCI Target



82C599-2-9

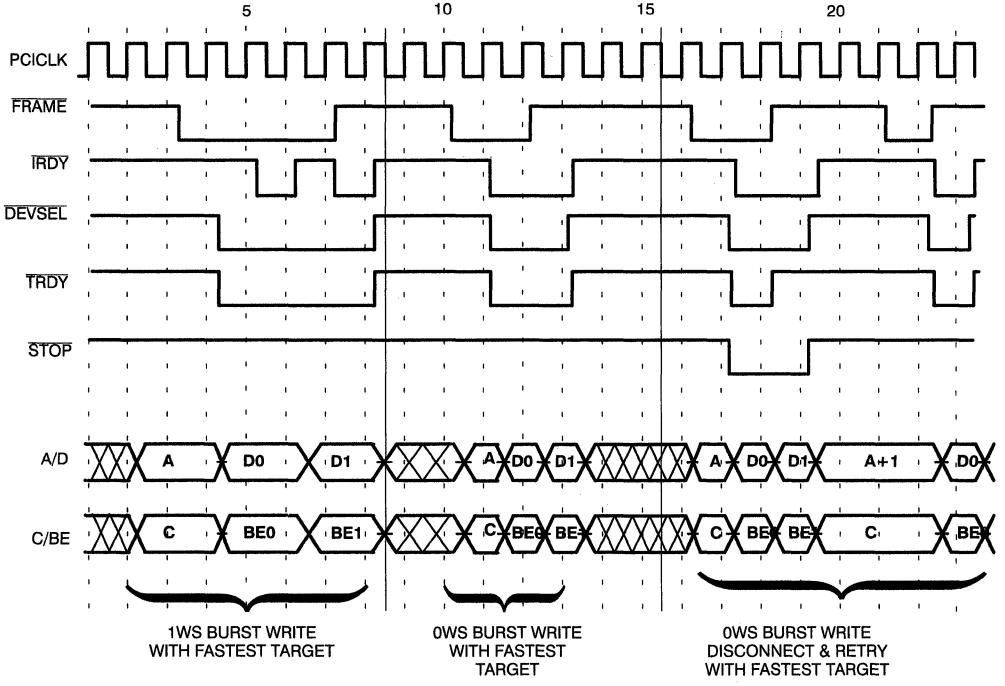
Switching Waveforms (continued)

CPU Master Post Write to PCI Target, CPU side, Buffer available.



Switching Waveforms (continued)

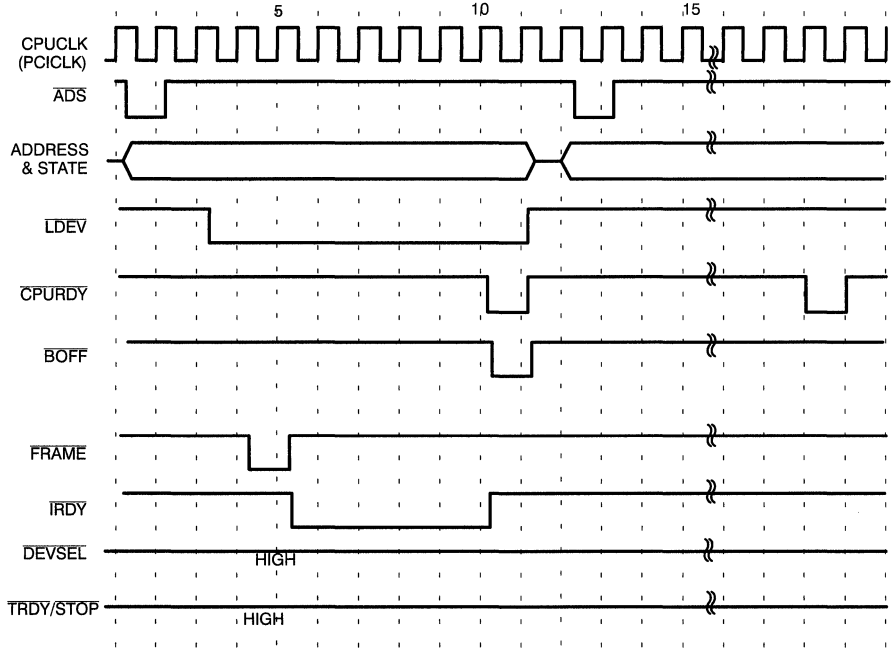
CPU Master Burst Post Write, to PCI Target (PCI side) Data Available in Buffer.



82C599-2-11

Switching Waveforms (continued)

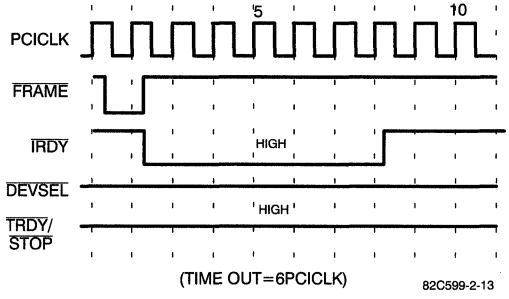
CPU Master Read/Write to PCI Bus "Miss" Cycle, Stand-Alone Mode (to CPU without claiming the same cycle)



82C599-2-12

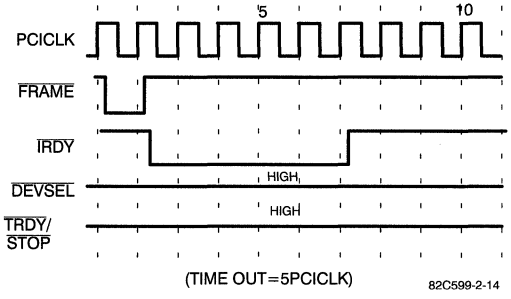
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



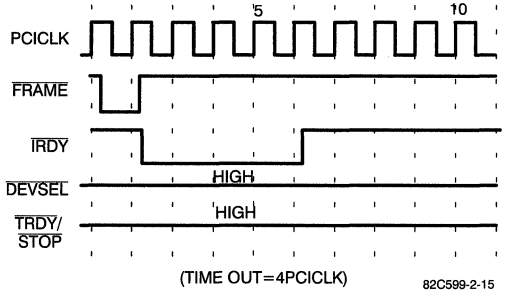
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



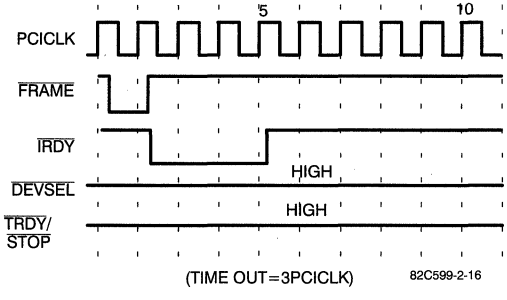
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



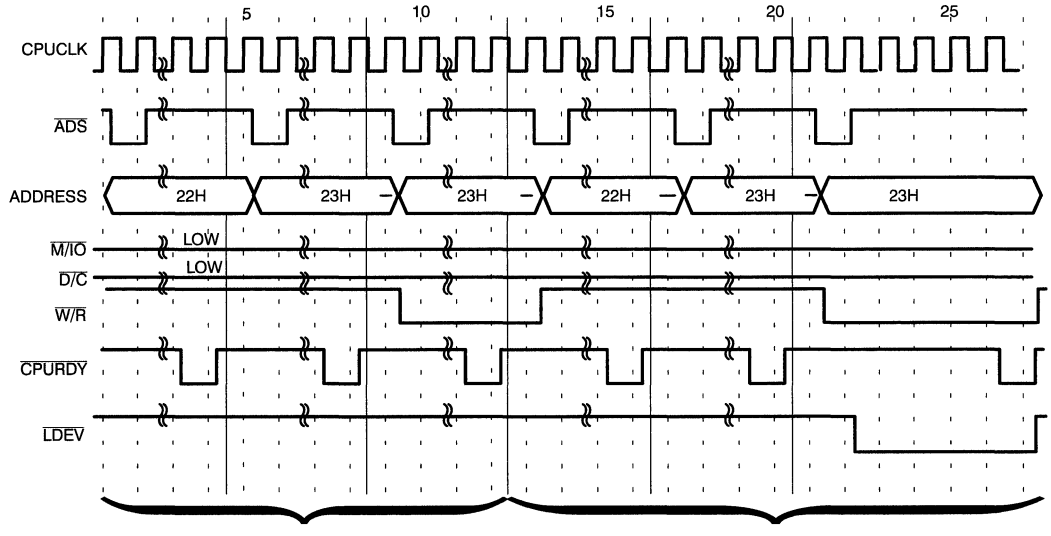
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



Switching Waveforms (continued)

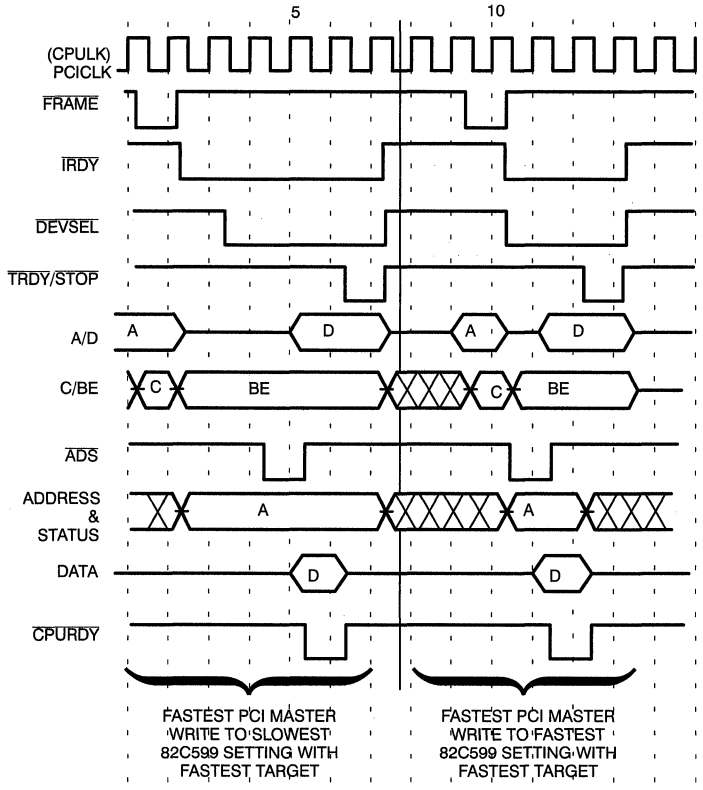
CPU Master I/O Read/Write to 22/23H location, Stand-Alone mode



82C599-2-17

Switching Waveforms (continued)

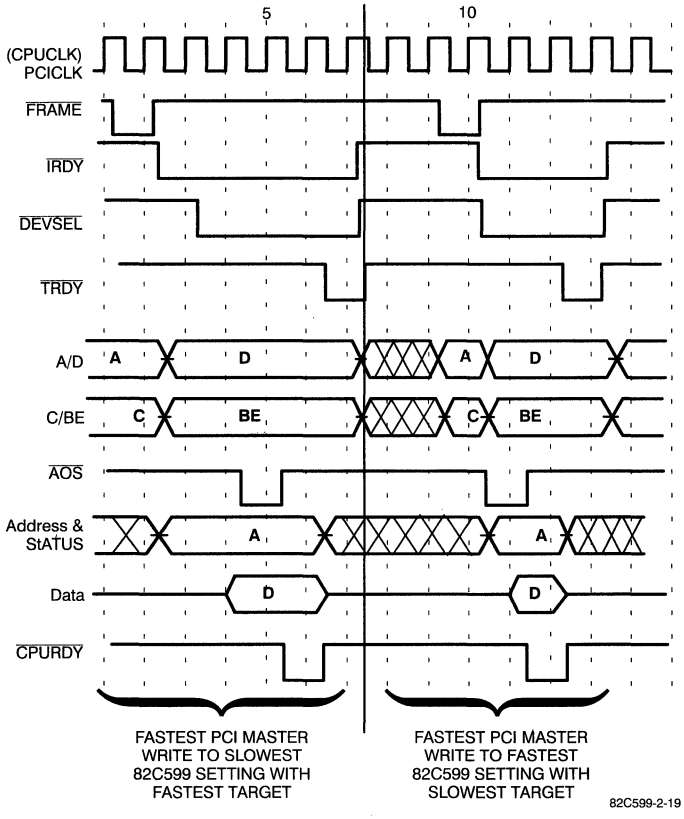
PCI Master Read From 82C599 Target



82C599-2-18

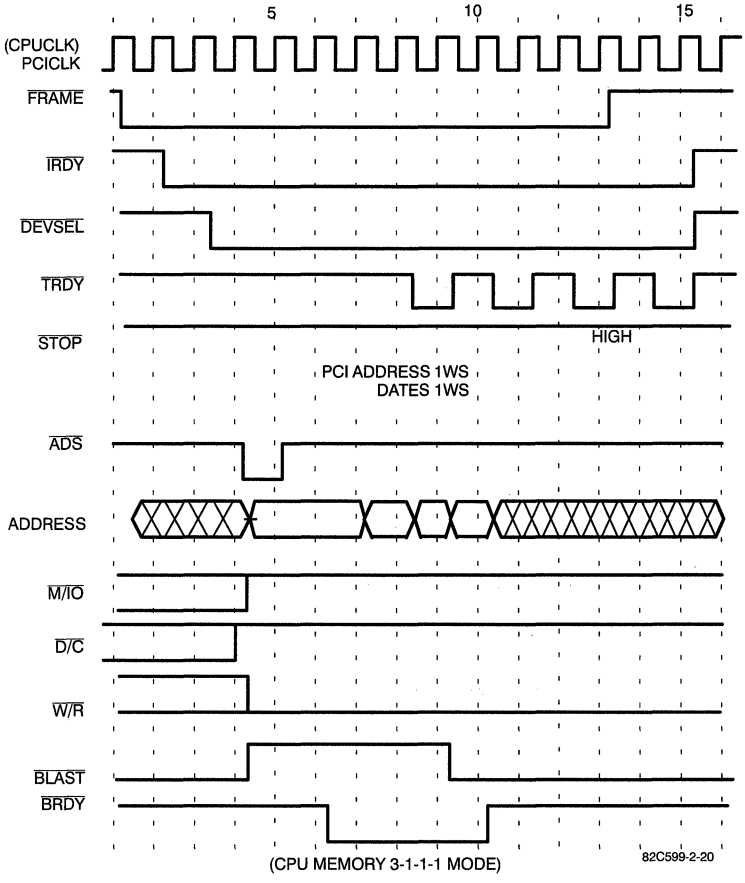
Switching Waveforms (continued)

PCI Master Write to 82C599 Target



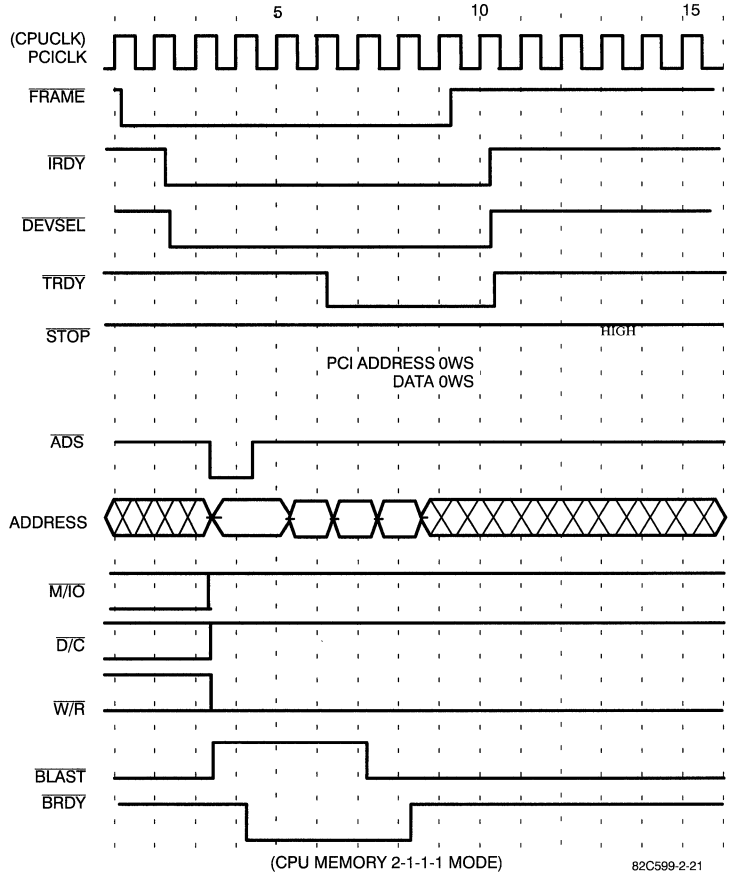
Switching Waveforms (continued)

PCI Master Burst Pre-Read to CPU



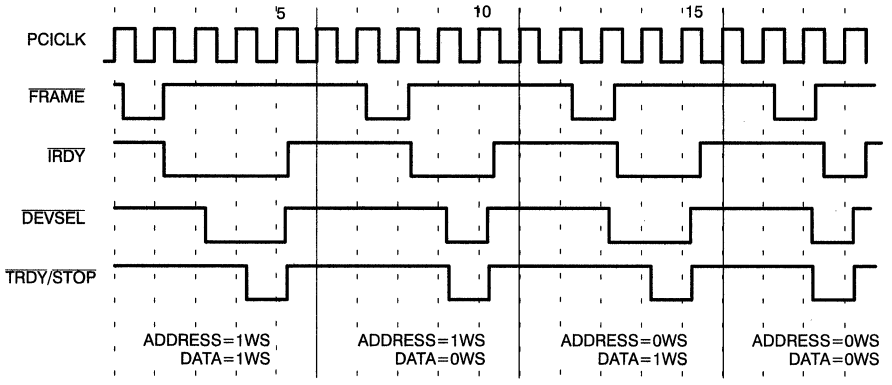
Switching Waveforms (continued)

PCI Master Burst Pre-Read to CPU



Switching Waveforms (continued)

PCI Master Post Write to CPU, PCI Side Buffer Available

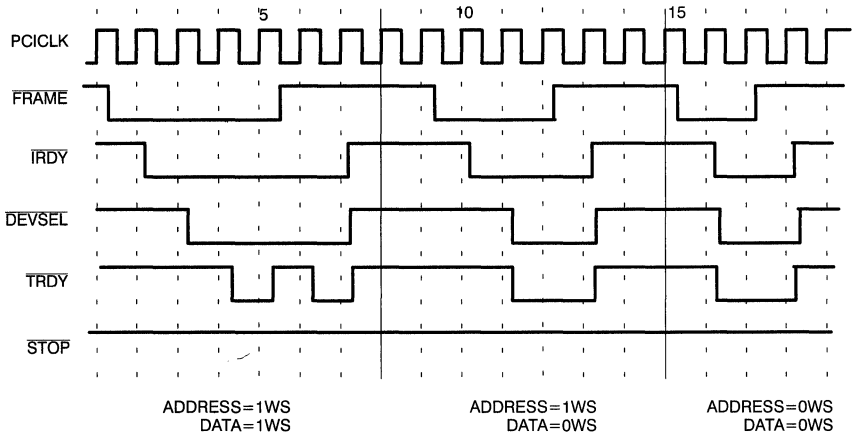


82C599-2-22

Note: CPU side same as 486 type CPU write cycle

Switching Waveforms (continued)

Master Burst Post Write to CPU, PCI Side Buffer Available

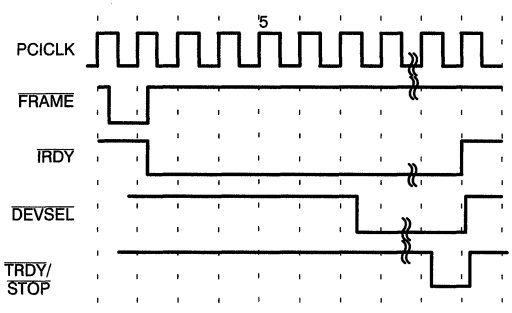


Note: CPU side same as 486 type CPU write cycle.

82C599-2-23

Switching Waveforms (continued)

PCI Master Subtractive Decode "DEVSEL" Timing

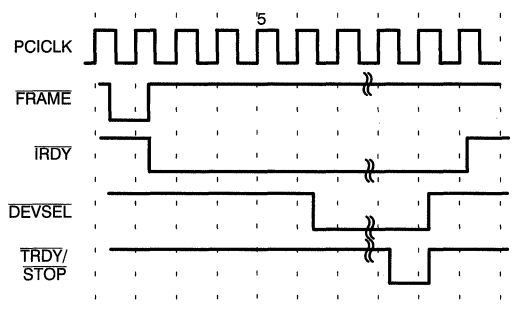


(SUB–DECODE=6PCICLK)

82C599-2-24

Switching Waveforms (continued)

PCI Master Subtractive Decode "DEVSEL" Timing

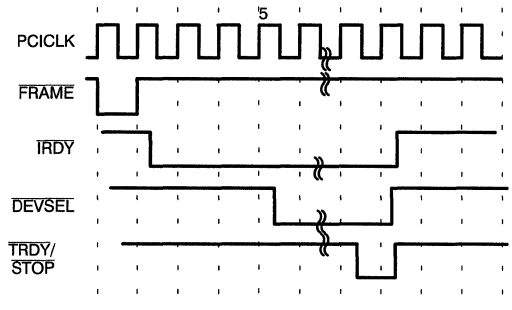


(SUB–DECODE=5PCICLK)

82C599-2-25

Switching Waveforms (continued)

PCI Master Subtractive Decode "DEVSEL" Timing

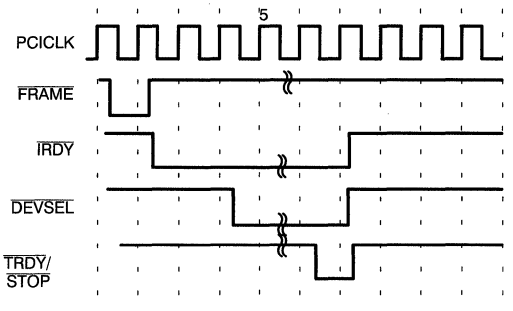


(SUB–DECODE=4PCICLK)

82C599-2-26

Switching Waveforms (continued)

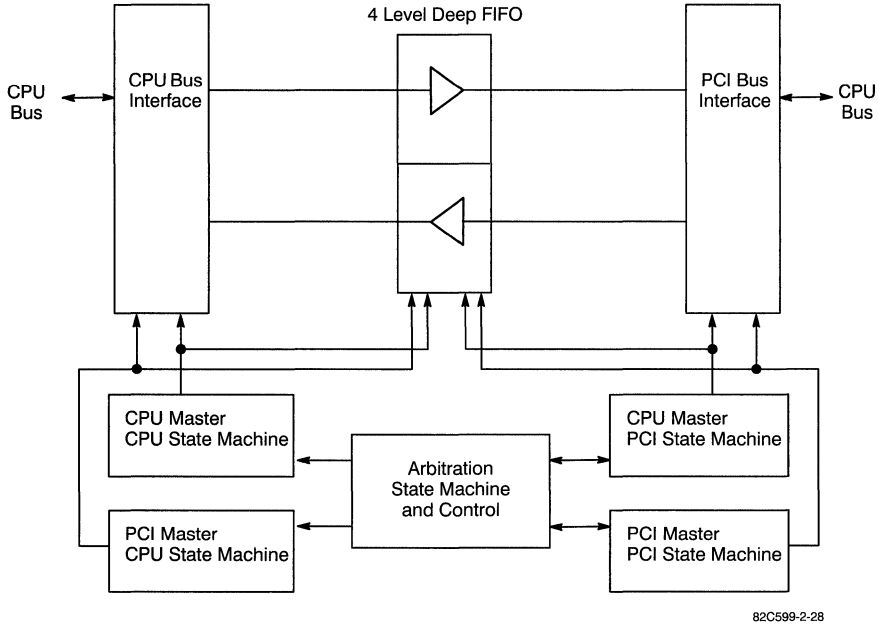
PCI Master Subtractive Decode "DEVSEL" Timing



(SUB–DECODE=3PCICLK)

82C599-2-27

82C599 Block Diagram



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY82C599-NC	N160	160-Lead Plastic Quad Flatpack	Commercial

Document #: 38−00413

Section Contents

Military Information **Page Number**

Military Overview

Features

Success in any endeavor requires a high level of dedication to the task. Cypress Semiconductor has demonstrated its dedication through its corporate commitment to support the military marketplace. This commitment starts with product design. All products are designed using our state-of-the-art CMOS and BiCMOS processes, and they must meet the full − 55 to +125 degrees Celsius operational criteria for military use. The commitment shows in our dedication to meet and exceed the stringent quality and reliability requirements of MIL-STD-883 and MIL-I-38535. It shows in Cypress's participation in each of the military processing programs: MIL-STD-883 compliant, SMD (Standardized Military Drawing), and QML. Finally, our commitment shows in our leadership position in special packages for military use.

Product Design

Every Cypress product is designed to meet or exceed the full temperature and functional requirements of military product. This means that Cypress builds military product as a matter of course, rather than as an accidental benefit of favorable test yield. Designs are being carried out in our industry-leading 0.65-micron CMOS and BiCMOS processes. Cypress is able to offer a family of products that are industry leaders in density, low operating and standby current, and high speed. In addition, our technology results in products with very small manufacturable die sizes that will fit into the LCCs and flatpacks so often used in military programs.

DESC-Certified Facility

On May 8, 1986, the Cypress facility at 3901 North First Street in San Jose, California was certified by DESC for the production of JAN Class B CMOS Microcircuits. And, most recently, on February 16, 1994, Cypress received QML (Qualified Manufacturers List) transitional certification from DESC to the requirements of MIL−I−38535. This certification allows Cypress to continue to produce JAN products as well as manufacture devices listed on the QML. QML certification attests to Cypress' commitment to quality and reliability through the use of statistical process control and total quality management. Our wafer fabrication facilities are Class 10 (San Jose) and Class 1 (Round Rock, TX and Bloomington, MN) manufacturing environments and our assembly facility is also a clean room.

Datasheet Documentation

Every Cypress final data sheet is a corporate document with a revision history. The document number and revision appears on each final data sheet. Cypress maintains a listing of all data sheet documentation and a copy is available to customers upon request. This gives a customer the ability to verify the current status of any data sheet and it also gives that customer the ability to obtain updated specifications as required.

Every final data sheet also contains detailed Group A subgroup testing information. All of the specified parameters that are tested at Group A are listed in a table at the end of each final data sheet, with a notation as to which specific Group A test subgroups apply.

Assembly Traceability Code™

Cypress Semiconductor places an assembly traceability code on every military package that is large enough to contain the code. The ATC automatically provides traceability for that product to the individual wafer lot. This unique code provides Cypress with the ability to determine which operators and equipment were used in the manufacture of that product from start to finish.

Quality and Reliability

MIL-STD-883 and MIL-I-38535 spell out the toughest of quality and reliability standards for military products. Cypress products meet all of these requirements and more. Our in-house quality and reliability programs are being updated regularly with tighter and tighter objectives. Please refer to the chapter on Quality, Reliability, and Process Flows for further details.

Military Product Offerings

Cypress offers three levels of processing for military product.

First, all Cypress products are available with processing in full compliance with MIL-STD-883.

Second, selected products are available to the SMD (Standardized Military Drawing) program administered by DESC. These products are not only fully MIL-STD-883 compliant, but are also screened to the electrical requirements of the applicable military drawing.

Third, selected products are available as QML/JAN devices. These products are processed in full accordance with MIL-I-38535 and they are screened to the electrical requirements of the applicable slash sheet.

Product Packaging

All packages for military product are hermetic. A look at the package appendix in the back of this data book will give the reader an appreciation of the variety of packages offered. Included are cerDIPs, windowed CerDIPs, leadless chip carriers (LCCs), windowed leadless chip carriers, cerpaks, windowed cerpaks, quad cerpaks, windowed quad cerpaks, bottom-brazed flatpacks, and pin grid arrays.

Summary

Cypress Semiconductor is committed to the support of the military marketplace. Our commitment is demonstrated by our product designs, our DESC-certified facility, our documentation and traceability, our quality and reliability programs, our support of all levels of military processing, and by our leadership in special packaging.

Static RAMs

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	883 Availability
64	16x4—Inverting	16	CY7C189		t_{AA} = 25	70 @ 25	Now
64	16x4—Non-Inverting	16	CY7C190	5962-89694	t_{AA} = 25	70 @ 25	Now
64	16x4—Inverting	16	CY27S03/A		t_{AA} = 25,35	100 @ 35	Now
64	16x4—Non-Inverting	16	CY27S07/A		t_{AA} = 25,35	100 @ 25	Now
1K	256x4—10K/10KH ECL	24	CY10E422L		t_{AA} = 5, 7	150 @ 5/7	Now
1K	256x4	22	CY7C122	5962-88594	t_{AA} = 25,35	90 @ 25	Now
1K	256x4	24S	CY7C123	5962-90696	t_{AA} = 10, 12, 15	150 @ 15	Now
1K	256x4	22	CY9122/91L22	5962-88594	t_{AA} = 35,45	90 @ 45	Now
1K	256x4	22	CY93422A/93L422A	5962-88594	t_{AA} = 45, 55, 60, 75	90 @ 55	Now
4K	4Kx1—CS Power-Down	18	CY7C147	M38510/289	t_{AA} = 35,45	110/10 @ 35	Now
4K	4Kx1—CS Power-Down	18	CY2147	M38510/289	t_{AA} = 45,55	140/25 @ 45	Now
4K	4Kx1—CS Power-Down	18	CY7C147	5962-88587	t_{AA} = 35,45	110/10 @ 35	Now
4K	4Kx1—CS Power-Down	18	CY2147	5962-88587	t_{AA} = 45,55	140/25 @ 45	Now
4K	1Kx4—10K/10KH ECL	24	CY10E474L	5962-91518	t_{AA} = 5, 7	190 @ 5/7	Now
4K	1Kx4—CS Power-Down	18	CY7C148	M38510/289	t_{AA} = 35,45	110/10 @ 35	Now
4K	1Kx4—CS Power-Down	18	CY2148	M38510/289	t_{AA} = 45,55	140/25 @ 45	Now
4K	1Kx4	18	CY7C149		t_{AA} = 35,45	110 @ 35	Now
4K	1Kx4	18	CY2149		t_{AA} = 45,55	140 @ 45	Now
4K	1Kx4—Separate I/O	24S	CY7C150	5962-88588	t_{AA} = 12, 15, 25, 35	100 @ 15	Now
8K	1Kx8—Dual Port	48	CY7C130/31	5962-86875	t_{AA} = 35, 45, 55	120/40 @ 45	Now
8K	1Kx8—Dual-Port Slave	48	CY7C140/41	5962-86875	t_{AA} = 35, 45, 55	120/40 @ 45	Now
16K	4Kx4—CS ECL	28	CY10E484L		t_{AA} = 7, 10	200 @ 10	Now
16K	2Kx8—CS Power-Down	24S	CY7C128A	5962-89690	t_{AA} = 20, 25	125 @ 20	Now
16K	2Kx8—CS Power-Down	24	CY6116A/7A	5962-89690	t_{AA} = 20, 25	125 @ 20	Now
16K	2Kx8—CS Power-Down	24S	CY7C128A	84036	t_{AA} = 35, 45, 55	125/40 @ 25	Now
16K	16Kx1—CS Power-Down	20	CY7C167A	84132	t_{AA} = 20, 25, 35, 45	70/20 @ 25	Now
16K	4Kx4—CS Power-Down	20	CY7C168A	5962-86705	t_{AA} = 20, 25, 35, 45	100/20 @ 25	Now
16K	4Kx4	20	CY7C169A		t_{AA} = 20, 25, 35, 40	100/20 @ 35	Now
16K	4Kx4—Output Enable	22S	CY7C170A		t_{AA} = 20, 25, 35, 45	120 @ 25	Now
16K	4Kx4—Separate I/O	24S	CY7C171A		t_{AA} = 20, 25, 35, 45	100/20 @ 25	Now
16K	4Kx4—Separate I/O, Power-Down	24S	CY7C172A	5962-89790	t_{AA} = 20, 25, 35, 45	90 @ 20	Now
16K	2Kx8—Dual-Port	48	CY7C132/36	5962-90620	t_{AA} = 35, 45, 55	170/65 @ 35	Now
16K	2Kx8—Dual-Port Slave	48	CY7C142/46	5962-90620	t_{AA} = 35, 45, 55	120/40 @ 45	Now
32K	4Kx8—Dual-Port	48	CY7B134	5962-93001	t_{AA} = 25, 35	280 @ 25	Now
32K	4Kx8—Dual-Port	52	CY7B135	5962-93001	t_{AA} = 25, 35	280 @ 25	Now
32K	4Kx8—Dual-Port Semaphores	52	CY7B1342		t_{AA} = 25, 35	280 @ 25	Now
32K	4Kx8—Dual-Port Semaphores Int, Busy	68	CY7B138		t_{AA} = 25, 35	280 @ 25	Now
32K	4Kx9—Dual-Port Semaphores Int, Busy	68	CY7B139		t_{AA} = 25, 35	280 @ 25	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-38294	t_{AA} = 20, 25, 35, 45	125 @ 20	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-89691	t_{AA} = 20, 25	125 @ 20	Now
64K	8Kx8—CS Power-Down	28S	CY7C185A	5962-85525	t_{AA} = 35, 45	100/20/1 @ 45	Now
64K	8Kx8—CS Power-Down	28S	CY7B185	5962-91594	t_{AA} = 10, 12, 15	145/50 @ 15	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-38294	t_{AA} = 20, 25, 35, 45	125 @ 20	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-89691	t_{AA} = 20, 25	125 @ 20	Now
64K	8Kx8—CS Power-Down	28	CY7C186A	5962-85525	t_{AA} = 35, 45, 55	100/20/1 @ 45	Now
64K	16Kx4—CS Power-Down	22S	CY7C164A	5962-89692	t_{AA} = 20, 25	90 @ 20	Now
64K	16Kx4—CS Power-Down	22S	CY7C164A	5962-86859	t_{AA} = 35	70/20/1 @ 35	Now
64K	16Kx4—CS Power-Down	22S	CY7B164	5962-91593	t_{AA} = 10, 12, 15	135/50 @ 15	Now
64K	16Kx4—CS Power-Down	24S	CY7C166A	5962-89892	t_{AA} = 20, 25	90 @ 20	Now
64K	16Kx4—Output Enable	24S	CY7C166A	5962-86859	t_{AA} = 35	70/20/1 @ 35	Now
64K	16Kx4—Output Enable	24S	CY7B166	5962-91593	t_{AA} = 10, 12, 15	135/50 @ 15	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7C161A	5962-90594	t_{AA} = 20, 25, 35	70/20/1 @ 35	Now
64K	16Kx4—Separate I/O	28S	CY7C162A	5962-89712	t_{AA} = 20, 25, 35	70/20/1 @ 35	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7B161		t_{AA} = 12, 15	135/50 @ 15	Now
64K	16Kx4—Separate I/O	28S	CY7B162	5962-92172	t_{AA} = 12, 15	135/50 @ 15	Now
64K	64Kx1—CS Power-Down	22S	CY7C187A	5962-86015	t_{AA} = 20, 25, 35	70/20/1 @ 35	Now
64K	8Kx8—Dual-Port Semaphores Int, Busy	68	CY7B144		t_{AA} = 25, 35	280 @ 25	Now
64K	8Kx9—Dual-Port Semaphores Int, Busy	68	CY7B145		t_{AA} = 25,35	280 @ 25	Now

Static RAMs (continued)

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	883 Availability
64K	4K x 18—Cache Tag	68	CY7B180		t_{AA} = 15.20	250@15	Now
64K	4K x 18—Cache Tag	68	CY7B181		t_{AA} = 15,20	250@15	Now
256K	32K x 8—CS Power-Down	28	CY7C198	5962-88662	t_{AA} = 15,20,25,35,45	180/40@20	Now
256K	32K x 8—CS Power-Down	28S	CY7C199	5962-88662	t_{AA} = 15,20,25,35,45	180/40@20	Now
256K	64K x 4—CS Power-Down	24S	CY7C194	5962-88681	t_{AA} = 15,20,25,35,45	150/40@20	Now
256K	64K x 4—CS, OE	28S	CY7C195	5962-89524	t_{AA} = 15,20,25,35,45	120/25@25	Now
256K	64K x 4—CS PD + OE/CE2	28S	CY7C196	5962-93225	t_{AA} = 15,20,25,35,45	150/40@20	Now
256K	64K x 4—Separate I/O, T-write	28S	CY7C191	5962-90664	t_{AA} = 15,20,25,35,45	150/40@20	Now
256K	64K x 4—Separate I/O	28S	CY7C192	5962-89935	t_{AA} = 15,20,25,35,45	150/40@20	Now
256K	256K x 1—CS Power-Down	24S	CY7C197	5962-88725	t_{AA} = 15,20,25,35,45	150/40@20	Now
1M	128K x 8—CS Power-Down	32	CY7C109A	5962-89598	t_{AA} = 15,20,25,35	140/30@25	4Q95
1M	128K x 8—CS Power-Down	32S	CY7C1009		t_{AA} = 15,20,25	180/40@15	4Q95
1M	256K x 4—CS Power-Down/OE	28S	CY7C1006	5962-91612	t_{AA} = 15,20,25	165/40@15	4Q95
1M	256K x 4—Separate I/O, T-Write	32S	CY7C1001		t_{AA} = 15,20,25	165/40@15	4Q95
1M	256K x 4—Separate I/O	32S	CY7C1002		t_{AA} = 15,20,25	165/40@15	4Q95
1M	1M x 1—CS Power-Down	28S	CY7C1007	5962-92316	t_{AA} = 15,20,25	145/40@15	4Q95

PROMs

Size	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns)	I_{CC}/I_{SB} (mA@ns)	883 Availability
4K	512x8—Registered	24S	CY7C225A	5962-88518(O)	$t_{SA/CO}$= 25/12,30/15,35/20	120	Now
8K	1Kx8—Registered	24S	CY7C235A	5962-88636(O)	$t_{SA/CO}$= 25/12,30/15,40/20	120	Now
8K	1Kx8	24S	CY7C281A	5962-87651(O)	t_{AA}=30,45	120	Now
8K	1Kx8	24	CY7C282A	5962-87651(O)	t_{AA}=30,45	120	Now
16K	2K x 8—Registered	24S	CY7C245	5962-87529(W)	$t_{SA/CO}$ = 35/15,45/25	120@35/15	Now
16K	2K x 8—Registered	24S	CY7C245A	5962-89815(W)	$t_{SA/CO}$ = 18/12,25/12,35/15	120@18/12	Now
16K	2K x 8—Registered	24S	CY7C245A	5962−88735(O)	$t_{SA/CO}$ = 18/12,25/12,35/15	120@18/12	Now
16K	2K x 8	24S	CY7C291	5962-87650(W)	t_{AA} = 25,35,50	120@35	Now
16K	2K x 8	24S	CY7C291A	5962-88734(O)	t_{AA} = 25,30,35,50	120@25	Now
16K	2K x 8—CS Power-Down	24S	CY7C293A	5962-88680(W)	t_{AA} = 25,30,35,50	120/30@25	Now
16K	2K x 8—CS Power-Down	24S	CY7C293A	5962-92341(O)	t_{AA} = 25,30,35,50	120/30@35	Now
16K	2K x 8	24	CY7C292		t_{AA} = 35,50	120@35	Now
16K	2K x 8	24	CY7C292A	5962-88734(O)	t_{AA} = 25,30,35,45,50	120@30	Now
32K	4K x 8	24	CY7C243/4		t_{AA} = 25,35,45,55,70	140	Now
64K	8K x 8—CS Power-Down	24S	CY7C261	5962-87515(W)	t_{AA} = 25,35,45,55	140/50@25	Now
64K	8K x 8—CS Power-Down	24S	CY7C261	5962-90803(O)	t_{AA} = 25,35,45,55	120/30@35	Now
64K	8K x 8	24S	CY7C263/4	5962-87515(W)	t_{AA} = 25,35,45,55	140@25	Now
64K	8K x 8	24	CY7C263/4	5962-90803(O)	t_{AA} = 25,35,45,55	120@35	Now
64K	8K x 8—Registered	28S	CY7C265	5962-89967(O)	$t_{SA/CO}$ = 15/12,25/20,50/25	140@18/15	Now
64K	8K x 8—Registered	28S	CY7C265	5962-89484(W)	$t_{SA/CO}$ = 15/12,25/20,50/25	120@50/25	Now
64K	8K x 8—Registered/Diagnostic	28S	CY7C269	5962-90831(O)	$t_{SA/CO}$ = 15/12,25/20,50/25	140@15/12	Now
64K	8K x 8—Registered/Diagnostic	28S	CY7C269	5962-90930(W)	$t_{SA/CO}$ = 15/12,25/20,50/25	140@15/12	Now
128K	16K x 8—CS Power-Down	28S	CY7C251	5962-89537(W)	t_{AA} = 45,55,65	120/35@45	Now
128K	16K x 8	28	CY7C254	5962-89538(W)	t_{AA} = 45,55,65	120@45	Now
128K	16K x 8—EPROM Pinout	28	CY27C128		t_{AA} = 45,55,70,90,120,150,200	55/20	Now

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PROMs (continued)

Size	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	883 Availability
256K	16Kx16	44	CY7C276		t_{AA}=25, 30, 35	250@30	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	5962-89817(W)	t_{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—CS Power-Down	28S	CY7C271	5962-93166(O)	t_{AA}=35, 45, 55	130/40@55	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	5962-89817(W)	t_{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—EPROM Pinout	28	CY7C274	5962-93166(O)	t_{AA} = 35, 45, 55	130/40 @ 35	Now
256K	32Kx8—EPROM PInout	28	CY27C256		t_{AA} = 45, 55, 70, 90, 120, 150, 200	55/20	Now
256K	32Kx8—Registered	28S	CY7C277	5962-91744(W)	$t_{SA/CO}$ = 40/20, 50/25	130 @ 40	Now
256K	32Kx8—Registered	28S	CY7C277	5962-92155(O)	$t_{SA/CO}$ = 40/20, 50/25	130 @ 40	Now
512K	64Kx8—EPROM Pinout	28	CY7C286	5962-91637(O)	t_{AA} = 60, 70	150 @ 60	Now
512K	64Kx8—EPROM Pin	28	CY7C286	5962-92071(W)	t_{AA} = 60, 70	150 @ 60	Now
512K	64Kx8—Registered	28S	CY7C287	5962-90913(W)	$t_{SA/CO}$ = 55/20, 65/25	150 @ 65	Now
512K	64Kx8—Registered	28S	CY7C287	5962-92065(O)	$t_{SA/CO}$ = 55/20, 65/25	150 @ 65	Now
1M	128Kx8	32	CY27H010		t_{AA} = 35, 45, 55, 70	85@35	Now

PLDs

	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns/MHz)	I_{CC} (mA @ ns/MHz)	883 Availability
PAL20	16L8, 16R8, 16R6, 16R4	20	PAL16XX	5962-92338(O)	t_{PD} = 7, 10	180 @ 7	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88678(W)	t_{PD} = 20, 30, 40	70 @ 20	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88713(O)	t_{PD} = 20, 30, 40	70 @ 20	Now
PALCE20	16V8—Macrocell	20S	PALCE16V8	5962-89839	$t_{PD/S/CO}$ = 10/10/7	130 @ 10	Now
PLD24	22V10C—Macrocell	24S	PAL22V10C	5962-91760(O)	$t_{PD/S/CO}$ = 10/3.6/7.5	190 @ 10	Now
PLD24	22V10C—Macrocell	24S	PAL22VP10C	5962-91760(O)	$t_{PD/S/CO}$ = 10/3.6/7.5	190 @ 10	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-87539(W)	$t_{PD/S/CO}$ = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-87539(W)	$t_{PD/S/CO}$ = 20/17/15	100 @ 20	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-88670(O)	$t_{PD/S/CO}$ = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-88670(O)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/507(W)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/508(O)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10D—Macrocell	24S	PALC22V10D	5962-89841(O)	$t_{PD/S/CO}$=10/6/7	130@10	Now
PLDC24	20G10—Generic	24S	PLDC20G10	5962-88637(O)	$t_{PD/S/CO}$ = 20/17/15	80 @ 30	Now
PLDC24	20RA10—Asynchronous	24S	PLD20RA10	5962-90555(O)	$t_{PD/SU/CO}$ = 20/10/20	100 @ 25	Now
PLDC24	20RA10—Asynchronous	24S	PLD20RA10	5962-90989(W)	$t_{PD/SU/CO}$=20/10/20	100@25	Now
PLDC28	7C330—State Machine	28S	CY7C330	5962-89546(W)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C330—State Machine	28S	CY7C330	5926-90802(O)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-90754(W)	t_{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-89855(O)	t_{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C332—Combinatorial	28S	CY7C332	5962-91584(W)	t_{PD} = 20, 25, 30	200 @ 24 MHz	Now
PLD28	7C335—Synchronous	28S	CY7C335	5862-94510(W)	f_{MAX5} = 66.6, 50, 83	160 @ 66.6 MHz	Now
MAX28	7C344—32 Macrocell	28S	CY7C344/B	5962-90611(W)	t_{PD} = 12, 20, 25, 35	220@25	Now
MAX40	7C343—64 Macrocell	40/44	CY7C343/B	5962-92158(W)	t_{PD} = 15, 20, 25, 30, 35	225@25	Now
MAX68	7C342—128 Macrocell	68	CY7C342/B	5962-89468(W)	t_{PD} = 15, 20, 25, 30, 35	320@30	Now
MAX84	7C341—192 Macrocell	84	CY7C341/B	5962-92062(W)	t_{PD} = 20, 25, 30, 35, 40	480@30	Now
MAX100	7C346—128 Macrocell	84/100	CY7C346/B	5962-91344(W)	t_{PD} = 20, 25, 30, 35	320@35	Now
PLDC28	7C361—State Machine	28S	CY7C361		100, 83, 66 MHz	150 @ 100 MHz	Now
37X–44	7C371—32 Macrocell	44	CY7C371	5962-94684(O)	$f_{MAX}/t_S/t_{CO}$=83MHz/ 10/10	260@83	Now
37X–44	7C372—64 Macrocell	44	CY7C372	5962-94688(O)	$f_{MAX}/t_S/t_{CO}$=83MHz/8/8	300@83	Now
37X–84	7C373—64 Macrocell	84	CY7C373	5962-94689(O)	$f_{MAX}/t_S/t_{CO}$=83MHz/8/8	300@83	Now
37X–84	7C374—128 Macrocell	84	CY7C374	5962-94713(O)	$f_{MAX}/t_S/t_{CO}$=83MHz/8/8	370@83	Now
37X–160	7C375—128 Macrocell	160	CY7C375		$f_{MAX}/t_S/t_{CO}$=83MHz/8/8	370@83	Now
FLASH370–160	7C376—192 Macrocell	160	CY7C376		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	4Q95
FLASH370–240	7C377—192 Macrocell	240	CY7C377		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	4Q95
FLASH370–160	7C378—256 Macrocell	160	CY7C378		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	2Q95

PLDs (continued)

	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns/MHz)	I_{CC} (mA @ ns/MHz)	883 Availability
FLASH370–240	7C379—256 Macrocell	240	CY7C379		$f_{MAX}/t_S/t_{CO}$=83MHz/12/12	300/TBD	2Q95
1KFPGA	CMOS 8x12	68	CY7C382A		–0, –1	20	Now
2KFPGA	CMOS 12x16	84	CY7C384A		–0, –1	20	Now
4KFPGA	CMOS 16x24	145	CY7C385A		–0, –1	20	Now
4KFPGA	CMOS 16x24	160	CY7C386A	5962-95599	–0, –1	20	Now
8KFPGA	CMOS 24x32	145/160/208	CY7C387A/8A		–0, –1	20	4Q95

FIFOs

Organization	Pins	Part Number	JAN/SMD Number	Speed	I_{CC}/I_{SB} (mA @ ns/MHz)	883 Availability
64x4—Cascadable	16	CY3341		1.2, 2 MHz	60 @ 2.0 MHz	Now
64x4—Cascadable	16	CY7C401		10, 15, 25 MHz	90 @ 15 MHz	Now
64x4—Cascadable/OE	16	CY7C403	5962-89523	10, 15, 25 MHz	90 @ 25 MHz	Now
64x5—Cascadable	18	CY7C402		10, 15, 25 MHz	90 @ 15 MHz	Now
64x5—Cascadable/OE	18	CY7C404	5962-86846	10, 15, 25 MHz	90 @ 25 MHz	Now
64x8—Cascadable/OE	28S	CY7C408A	5962-89664	15, 25 MHz	120 @ 25 MHz	Now
64x9—Cascadable	28S	CY7C409A	5962-89661	15, 25 MHz	120 @ 25 MHz	Now
512x9—Cascadable	28	CY7C420	5962-89863	t_A = 15, 20, 25, 30, 40, 65 ns	140/30 @ 30	Now
512x9—Cascadable	28S	CY7C421	5962-89863	t_A = 15, 20, 25, 30, 40, 65 ns	147/30 @ 25	Now
1Kx9—Cascadable	28	CY7C424	5962-91585	t_A = 15, 20, 25, 30, 40, 65 ns	140/30 @ 30	Now
1Kx9—Cascadable	28S	CY7C425	5962-91585	t_A = 15, 20, 25, 30, 40, 65 ns	147/30 @ 25	Now
2Kx9—Cascadable	28	CY7C428	5962-88669	t_A = 15, 20, 25, 30, 40, 65 ns	140/30 @ 30	Now
2Kx9—Cascadable	28S	CY7C429	5962-88669	t_A = 15, 20, 25, 30, 40, 65 ns	147/30 @ 25	Now
2Kx9—Bidirectional	28S	CY7C439	5962-92321	t_A = 15, 20, 25, 30, 40, 65 ns	170/45 @ 30	Now
4Kx9—Cascadable	28	CY7C432	5962-90715	t_A = 15, 20, 25, 30, 40, 65 ns	160/30 @ 30	Now
4Kx9—Cascadable	28S	CY7C433	5962-90715	t_A = 15, 20, 25, 30, 40, 65 ns	160/30 @ 30	Now
512x9—Clocked	28S	CY7C441		t_C = 14, 20, 30 ns	160 @ 14	Now
2Kx9—Clocked	28S	CY7C443		t_C = 14, 20, 30 ns	160 @ 14	Now
512x9—Clocked/Cascadable	32	CY7C451	5962-93173	t_C = 14, 20, 30 ns	160 @ 14	Now
2Kx9—Clocked/Cascadable	32	CY7C453	5962-93124	t_C = 14, 20, 30 ns	160 @ 14	Now
8Kx9—Half Full Flag	28	CY7C460		t_A = 20, 25, 40 ns	110 @ 20	Now
8Kx9—Prog. Flags	28	CY7C470		t_A = 20, 25, 40 ns	110 @ 20	Now
16Kx9—Half Full Flag	28	CY7C462	5962-93008	t_A = 20, 25, 40 ns	110 @ 20	Now
16Kx9—Prog. Flags	28	CY7C472		t_A = 20, 25, 40 ns	110 @ 20	Now
32Kx9—Half Full Flag	28	CY7C464	5962-93152	t_A = 20, 25, 40 ns	110 @ 20	Now
32Kx9—Prog. Flags	28	CY7C474	5962-94588	t_A = 20, 25, 40 ns	110 @ 20	Now

Logic

Organization	Pins	Part Number	JAN/SMD Number	Speed (ns)	I_{CC} (mA @ ns)	883 Availability
Programmable Skew Clock Buffer (TTL Outputs)	32	CY7B991	5962-94522	f_{REF} = 15 – 80 MHz	75	Now
Programmable Skew Clock Buffer (CMOS Outputs)	32	CY7B992	5962-93112	f_{REF} = 15 – 80 MHz	75	Now
2901—4-Bit Slice	40	CY7C901	5962-88535	t_{CLK} = 27, 32	90 @ 27	Now
2901—4-Bit Slice	40	CY2901C	5962-88535	C	180 @ 32	Now
4x2901—16-Bit Slice	64	CY7C9101	5962-89517	t_{CLK} = 35, 45	85 @ 35	Now
2909—Sequencer	28	CY7C909		t_{CLK} = 30, 40	55 @ 30	Now
2911—Sequencer	20	CY7C911	5962-90609	t_{CLK} = 30, 40	55 @ 30	Now
2909—Sequencer	28	CY2909A		A	90 @ 40	Now
2911—Sequencer	20	CY2911A	5962-90609	A	90 @ 40	Now
2910—Controller (17-Word Stack)	40	CY7C910	5962-87708	t_{CLK} = 46, 51, 99	90 @ 46	Now
2910—Controller (9-Word Stack)	40	CY2910A	5962-87708	A	170 @ 51	Now

VMEbus Interface Products

Organization	Pins	Part Number	JAN/SMD Number	Speed (MHz)	I_{CC} (mA)	883 Availability
VME Interface Controller	144/160	VIC068A	5962-92010	64	250	Now
VME Address Controller	144/160	VAC068A	5962-92009	50	150	Now
64-Bit VIC	144/160	VIC64		64	300	Now
Slave VME Interface Controller	64	CY7C960				Now
Bus Interface Logic Circuit	64	CY7C964	5962-95511			Now

Communication Products

Organization	Pins	Part Number	Speed (Mbps)	I_{CC} (mA)	Packages	883 Availability
HOTLink Transmitter	28	CY7B923	160 – 330	95	L	Now
HOTLink Receiver	28	CY7B933	160 – 330	165	L	Now

Modules

Size	Organization	Pins	Part Number	Packages	Speed (ns)	I_{CC} (mA @ ns)	883 Availability
1M	32K x 32 SRAM	66	CYM1828	HG01	t_{AA} = 35, 45, 55, 70	200@35	Now
2M	64K x 32 SRAM	60	CYM1830	HD06	t_{AA} = 35, 45, 55	880 @ 35	Now
4M	128K x 32 SRAM	66	CYM1838	HG01	t_{AA} = 25, 30, 35	720 @ 25	Now
4M	512K x 8 SRAM	32	CYM1466	HD12	t_{AA} = 35, 45, 55, 70, 85, 100, 120	350 @ 35	Now

Notes:

The following Cypress facilites have been granted Level Q (QML) certification by DESC:

Operation	Facility	Location
Fab	Fab2	Round Rock, TX
	Fab3	Bloomington, MN
Assy/Test	Bangkok	Bangkok, Thailand
Test	San Jose	San Jose, CA

All of the above products are available with processing to MIL-STD-883D at a minimum. Many of these products are also available either to SMDs (Standardized Military Drawings) or to JAN slash sheets.

The speed and power specifications listed above cover the full military temperature range.

Modules are available with MIL-STD-883D components. These modules are assembled and screened to the proposed JEDEC military processing standard for modules.

W = Windowed Package
O = Opaque Package
HD = Hermetic DIP Module

100K ECL devices are available only to extended temperature range.

22S stands for 22-pin 300-mil DIP.
24S stands for 24-pin 300-mil DIP.
28S stands for 28-pin 300-mil DIP.
32S stands for 32-pin 300-mil DIP.

HOTLink is a trademark of Cypress Semiconductor.

Cypress Semiconductor fully supports the DESC standardized Military Drawing Program for devices that are compliant to the Class B requirements of MIL-STD-883D.

Listed below are the SMDs for which Cypress is an approved source of supply. Please contact your local Cypress representative for the latest SMD update.

DESC SMD (Standardized Military Drawing) Approvals[1]

SMD Number		Cypress[2] Part Number	Package[3]		Product Description
			Description	Type	
84036	09JX	CY6116A–45DMB	24.6 DIP	D12	2K x 8 SRAM
84036	09KX	CY7C128A–45KMB	24 CP	K73	2K x 8 SRAM
84036	09LX	CY7C128A–45DMB	24.3 DIP	D14	2K x 8 SRAM
84036	09XX	CY6117A–45LMB	32 R LCC	L55	2K x 8 SRAM
84036	09YX	CY7C128A–45LMB	24 R LCC	L53	2K x 8 SRAM
84036	093X	CY6116A–45LMB	28 S LCC	L64	2K x 8 SRAM
84036	11JX	CY6116A–55DMB	24.6 DIP	D12	2K x 8 SRAM
84036	11KX	CY7C128A–55KMB	24 CP	K73	2K x 8 SRAM
84036	11LX	CY7C128A–55DMB	24.3 DIP	D14	2K x 8 SRAM
84036	11XX	CY6117A–55LMB	32 R LCC	L55	2K x 8 SRAM
84036	11YX	CY7C128A–55LMB	24 R LCC	D14	2K x 8 SRAM
84036	113X	CY6116A–55LMB	28 S LCC	L64	2K x 8 SRAM
84036	14JX	CY6116A–35DMB	24.6 DIP	D12	2K x 8 SRAM
84036	14KX	CY7C128A–35KMB	24 CP	K73	2K x 8 SRAM
84036	14LX	CY7C128A–35DMB	24.3 DIP	D14	2K x 8 SRAM
84036	14XX	CY6117A–35LMB	32 R LCC	L55	2K x 8 SRAM
84036	14YX	CY7C128A–35LMB	24 R LCC	L53	2K x 8 SRAM
84036	143X	CY6116A–35LMB	28 S LCC	L64	2K x 8 SRAM
84132	02RA	CY7C167A–45DMB	20.3 DIP	D6	16K x 1 SRAM
84132	05RA	CY7C167A–35DMB	20.3 DIP	D6	16K x 1 SRAM
5962–38294	11MTX	CY7C185A–45KMB	28 CP	K74	8K x 8 SRAM
5962–38294	25MUX	CY7C185A–45LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	11MXX	CY7C186A–45DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	11MYX	CY7C186A–45LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	11MZX	CY7C185A–45DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	13MTX	CY7C185A–35KMB	28 CP	K74	8K x 8 SRAM
5962–38294	27MUX	CY7C185A–35LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	13MXX	CY7C186A–35DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	13MYX	CY7C186A–35LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	13MZX	CY7C185A–35DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	15MTX	CY7C185A–25KMB	28 CP	K74	8K x 8 SRAM
5962–38294	29MUX	CY7C185A–25LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	15MXX	CY7C186A–25DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	15MYX	CY7C186A–25LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	15MZX	CY7C185A–25DMB	28.3 DIP	D22	8K x 8 SRAM
5962–38294	17MTX	CY7C185A–20KMB	28 CP	K74	8K x 8 SRAM
5962–38294	30MUX	CY7C185A–20LMB	28 R TLCC	L54	8K x 8 SRAM
5962–38294	17MXX	CY7C186A–20DMB	28.6 DIP	D16	8K x 8 SRAM
5962–38294	17MYX	CY7C186A–20LMB	32 R LCC	L55	8K x 8 SRAM
5962–38294	17MZX	CY7C185A–20DMB	28.3 DIP	D22	8K x 8 SRAM
5962–85525	06TX	CY7C185A–45KMB	28 CP	K74	8K x 8 SRAM
5962–85525	06UX	CY7C185A–45LMB	28 R TLCC	L54	8K x 8 SRAM
5962–85525	06XX	CY7C186A–45DMB	28.6 DIP	D16	8K x 8 SRAM
5962–85525	06ZX	CY7C185A–45DMB	28.3 DIP	D22	8K x 8 SRAM
5962–85525	07TX	CY7C185A–35KMB	28 CP	K74	8K x 8 SRAM
5962–85525	07UX	CY7C185A–35LMB	28 R TLCC	L54	8K x 8 SRAM
5962–85525	07XX	CY7C186A–35DMB	28.6 DIP	D16	8K x 8 SRAM
5962–85525	07ZX	CY7C185A–35DMB	28.3 DIP	D22	8K x 8 SRAM
5962–86015	01YX	CY7C187A–35DMB	22.3 DIP	D10	64K x 1 SRAM
5962–86015	01ZX	CY7C187A–35LMB	22 R LCC	L52	64K x 1 SRAM
5962–86015	02YX	CY7C187AL–35DMB	22.3 DIP	D10	64K x 1 SRAM
5962–86015	02ZX	CY7C187AL–35LMB	22 R LCC	L52	64K x 1 SRAM
5962–86705	12RA	CY7C168A–35DMB	20.3 DIP	D6	4K x 4 SRAM
5962–86705	12XA	CY7C168A–35LMB	20 R LCC	L51	4K x 4 SRAM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–86846 01VX	CY7C404–10DMB	18.3 DIP	D4	64 x 5 FIFO
5962–86846 012X	CY7C404–10LMB	20 S LCC	L61	64 x 5 FIFO
5962–86846 02VX	CY7C404–15DMB	18.3 DIP	D4	64 x 5 FIFO
5962–86846 022X	CY7C404–15LMB	20 S LCC	L61	64 x 5 FIFO
5962–86846 03VX	CY7C404–25DMB	18.3 DIP	D4	64 x 5 FIFO
5962–86846 032X	CY7C404–25LMB	20 S LCC	L61	64 x 5 FIFO
5962–86859 17LX	CY7C166AL–35DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–86859 17XX	CY7C166AL–35LMB	28 R TLCC	L54	16K x 4 SRAM w/OE
5962–86859 18LX	CY7C166A–35DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–86859 24YX	CY7C164A–35DMB	22.3 DIP	D10	16K x 4 SRAM
5962–86875 03XX	CY7C130–55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 03ZX	CY7C131–55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 04XX	CY7C130–45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 04ZX	CY7C131–45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 11XX	CY7C140–55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 11ZX	CY7C141–55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 12XX	CY7C140–45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 12ZX	CY7C141–45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 19XX	CY7C130–35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 19ZX	CY7C131–35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–86875 20XX	CY7C140–35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962–86875 20ZX	CY7C141–35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962–87515 05KX	CY7C261–45TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 05LX	CY7C261–45WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 053X	CY7C261–45QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 06KX	CY7C261–55TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 06LX	CY7C261–55WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 063X	CY7C261–55QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 07KX	CY7C261–35TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 07LX	CY7C261–35WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 073X	CY7C261–35QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 08JX	CY7C264–35WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962–87515 08KX	CY7C263–35TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 08LX	CY7C263–35WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 083X	CY7C263–35QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 09JX	CY7C264–45WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962–87515 09KX	CY7C263–45TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 09LX	CY7C263–45WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 093X	CY7C263–45QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 10JX	CY7C264–55WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962–87515 10KX	CY7C263–55TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 10LX	CY7C263–55WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 103X	CY7C263–55QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 11JX	CY7C264–25WMB	24.6 DIP	W12	8K x 8 UV EPROM
5962–87515 11KX	CY7C263–25TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 11LX	CY7C263–25WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 113X	CY7C263–25QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87515 12KX	CY7C261–25TMB	24 CP	T73	8K x 8 UV EPROM
5962–87515 12LX	CY7C261–25WMB	24.3 DIP	W14	8K x 8 UV EPROM
5962–87515 123X	CY7C261–25QMB	28 S LCC	Q64	8K x 8 UV EPROM
5962–87529 01LX	CY7C245–45WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962–87529 013X	CY7C245–45QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962–87529 02LX	CY7C245–35WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962–87529 023X	CY7C245–35QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962–87539 01LX	PALC22V10–25WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 013X	PALC22V10–25QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962–87539 02LX	PALC22V10–30WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 023X	PALC22V10–30QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962–87539 03LX	PALC22V10–40WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 04LX	PALC22V10B–20WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962–87539 043X	PALC22V10B–20QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–87650 01LX	CY7C291–50WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–87650 03KX	CY7C291–35TMB	24 CP	T73	2K x 8 UV EPROM
5962–87650 03LX	CY7C291–35WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–87650 033X	CY7C291–35QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962–87650 05KX	CY7C291A–25TMB	24 CP	T73	2K x 8 UV EPROM
5962–87650 05LX	CY7C291A–25WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–87650 053X	CY7C291A–25QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962–87651 02JX	CY7C281A–45DMB	24.6 DIP	D12	1K x 8 PROM
5962–87651 02KX	CY7C281A–45KMB	24 CP	K73	1K x 8 PROM
5962–87651 02LX	CY7C281A–45DMB	24.3 DIP	D14	1K x 8 PROM
5962–87651 023X	CY7C281A–45LMB	28 S LCC	L64	1K x 8 PROM
5962–87651 03JX	CY7C281A–30DMB	24.6 DIP	D12	1K x 8 PROM
5962–87651 03KX	CY7C281A–30KMB	24 CP	K73	1K x 8 PROM
5962–87651 03LX	CY7C281A–30DMB	24.3 DIP	D14	1K x 8 PROM
5962–87651 033X	CY7C281A–30LMB	28 S LCC	L64	1K x 8 PROM
5962–87708 04QX	CY7C910–51DMB	40.6 DIP	D18	Microprogram Controller
5962–87708 04UX	CY7C910–51LMB	44 LCC	L67	Microprogram Controller
5962–87708 05QX	CY7C910–46DMB	40.6 DIP	D18	Microprogram Controller
5962–87708 05UX	CY7C910–46LMB	44 LCC	L67	Microprogram Controller
5962–88518 04LX	CY7C225A–30DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962–88518 043X	CY7C225A–30LMB	28 S LCC	L64	512 x 8 Registered PROM
5962–88518 05LX	CY7C225A–35DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962–88518 053X	CY7C225A–35LMB	28 S LCC	L64	512 x 8 Registered PROM
5962–88518 06LX	CY7C225A–40DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962–88518 063X	CY7C225A–40LMB	28 S LCC	L64	512 x 8 Registered PROM
5962–88518 07LX	CY7C225A–25DMB	24.3DIP	D14	512 x 8 Registered PROM
5962–88518 073X	CY7C225A–25LMB	28S	L64	512 x 8 Registered PROM
5962–88535 01QX	CY7C901–32DMB	40.6 DIP	D18	4-Bit Slice
5962–88535 01XX	CY7C901–32LMB	44 LCC	L67	4-Bit Slice
5962–88535 02QX	CY7C901–27DMB	40.6 DIP	D18	4-Bit Slice
5962–88535 02XX	CY7C901–27LMB	44 LCC	L67	4-Bit Slice
5962–88588 01LX	CY7C150–35DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962–88588 02LX	CY7C150–25DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962–88588 03LX	CY7C150–15DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962–88594 02WX	CY7C122–35DMB	22.4 DIP	D8	256 x 4 SRAM
5962–88594 03WX	CY7C122–25DMB	22.4 DIP	D8	256 x 4 SRAM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–88636 03KX	CY7C235A–40KMB	24 CP	K73	1K x 8 Registered PROM
5962–88636 03LX	CY7C235A–40DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962–88636 033X	CY7C235A–40LMB	28 S LCC	L64	1K x 8 Registered PROM
5962–88636 04KX	CY7C235A–30KMB	24 CP	K73	1K x 8 Registered PROM
5962–88636 04LX	CY7C235A–30DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962–88636 043X	CY7C235A–30LMB	28 S LCC	L64	1K x 8 Registered PROM
5962–88636 05KX	CY7C235A–25KMB	24 CP	K73	1K x 8 Registered PROM
5962–88636 05LX	CY7C235A–25DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962–88636 053X	CY7C235A–25LMB	28 S LCC	L64	1K x 8 Registered PROM
5962–88637 01KX	PLDC20G10–40KMB	24 CP	K73	Generic CMOS PLD
5962–88637 01LX	PLDC20G10–40DMB	24.3 DIP	D14	Generic CMOS PLD
5962–88637 02KX	PLDC20G10–30KMB	24 CP	K73	Generic CMOS PLD
5962–88637 02LX	PLDC20G10–30DMB	24.3 DIP	D14	Generic CMOS PLD
5962–88637 023X	PLDC20G10–30LMB	28 S LCC	L64	Generic CMOS PLD
5962–88662 03MX	CY7C199–55KMB	28 CP	K74	32K x 8 SRAM
5962–88662 03NX	CY7C199–55DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 03UX	CY7C199–55LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 03XX	CY7C198–55DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 03YX	CY7C198–55LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 04MX	CY7C199–45KMB	28 CP	K74	32K x 8 SRAM
5962–88662 04NX	CY7C199–45DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 04UX	CY7C199–45LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 04XX	CY7C198–45DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 04YX	CY7C198–45LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 05MX	CY7C199–35KMB	28 CP	K74	32K x 8 SRAM
5962–88662 05NX	CY7C199–35DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 05UX	CY7C199–35LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 05XX	CY7C198–35DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 05YX	CY7C198–35LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 06MX	CY7C199–25KMB	28 CP	K74	32K x 8 SRAM
5962–88662 06NX	CY7C199–25DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 06UX	CY7C199–25LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 06XX	CY7C198–25DMB	28.6 DIP	D16	32K x 8 SRAM
5962–88662 06YX	CY7C198–25LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 07NX	CY7C199–20DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 07MX	CY7C199–20KMB	28 CP	K74	32K x 8 SRAM
5962–88662 07UX	CY7C199–20LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 07YX	CY7C198–20LMB	32 R LCC	L55	32K x 8 SRAM
5962–88662 08NX	CY7C199–15DMB	28.3 DIP	D22	32K x 8 SRAM
5962–88662 08MX	CY7C199–15KMB	28 CP	K74	32K x 8 SRAM
5962–88662 08UX	CY7C199–15LMB	28 R LCC	L54	32K x 8 SRAM
5962–88662 08YX	CY7C198–15LMB	32 R LCC	L55	32K x 8 SRAM
5962–88669 02XX	CY7C428–65DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 02YX	CY7C429–65DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 02ZX	CY7C429–65LMB	32 R LCC	L55	2K x 9 FIFO
5962–88669 03XX	CY7C428–50DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 03YX	CY7C429–50DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 03ZX	CY7C429–50LMB	32 R LCC	L55	2K x 9 FIFO
5962–88669 04XX	CY7C428–40DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 04YX	CY7C429–40DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 04ZX	CY7C429–40LMB	32 R LCC	L55	2K x 9 FIFO
5962–88669 05XX	CY7C428–30DMB	28.6 DIP	D16	2K x 9 FIFO
5962–88669 05YX	CY7C429–30DMB	28.3 DIP	D22	2K x 9 FIFO
5962–88669 05ZX	CY7C429–30LMB	32 R LCC	L55	2K x 9 FIFO
5962–88670 01KX	PALC22V10–25KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 01LX	PALC22V10–25DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 013X	PALC22V10–25LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88670 02KX	PALC22V10–30KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 02LX	PALC22V10–30DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 023X	PALC22V10–30LMB	28 S LCC	L64	24-Pin CMOS PLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–88670 03KX	PALC22V10–40KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 03LX	PALC22V10–40DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 04KX	PALC22V10B–20KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 04LX	PALC22V10B–20DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 043X	PALC22V10B–20LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88670 05KX	PALC22V10B–15KMB	24 CP	K73	24-Pin CMOS PLD
5962–88670 05LX	PALC22V10B–15DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962–88670 053X	PALC22V10B–15LMB	28 S LCC	L64	24-Pin CMOS PLD
5962–88678 01XX	PALC16L8–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 02XX	PALC16R8–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 03RX	PALC16R6–40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 03XX	PALC16R6–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 04RX	PALC16R4–40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 04XX	PALC16R4–40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 07XX	PALC16R6–30QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 09RX	PALC16L8–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 09XX	PALC16L8–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 10RX	PALC16R8–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 10XX	PALC16R8–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 11RX	PALC16R6–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 11XX	PALC16R6–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88678 12RX	PALC16R4–20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962–88678 12XX	PALC16R4–20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962–88680 01LX	CY7C293A–50WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–88680 02LX	CY7C293A–35WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–88680 03LX	CY7C293A–30WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–88680 04LX	CY7C293A–25WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962–88681 01LX	CY7C194–35DMB	24.3 DIP	D14	64K x 4 SRAM
5962–88681 01XX	CY7C194–35LMB	28 R LCC	L54	64K x 4 SRAM
5962–88681 02LX	CY7C194–45DMB	24.3 DIP	D14	64K x 4 SRAM
5962–88681 02XX	CY7C194–45LMB	28 R LCC	L54	64K x 4 SRAM
5962–88713 01RX	PALC16L8–40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 05RX	PALC16L8–30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 05XX	PALC16L8–30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962–88713 06RX	PALC16R8–30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 07RX	PALC16R6–30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 07XX	PALC16R6–30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962–88713 08RX	PALC16R4–30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 09RX	PALC16L8–20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 09XX	PALC16L8–20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962–88713 10RX	PALC16R8–20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 10XX	PALC16R8–20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962–88713 11RX	PALC16R6–20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 11XX	PALC16R6–20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962–88713 12RX	PALC16R4–20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962–88713 12XX	PALC16R4–20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962–88725 01LX	CY7C197–35DMB	24.3 DIP	D14	256K x 1 SRAM
5962–88725 01XX	CY7C197–35LMB	28 R LCC	L54	256K x 1 SRAM
5962–88725 02LX	CY7C197–45DMB	24.3 DIP	D14	256K x 1 SRAM
5962–88725 02XX	CY7C197–45LMB	28 R LCC	L54	256K x 1 SRAM
5962–88725 05LX	CY7C197–25DMB	24.3 DIP	D14	256K x 1 SRAM
5962–88725 05XX	CY7C197–25LMB	28 R LCC	L54	256K x 1 SRAM
5962–88734 02KX	CY7C291A–45KMB	24 CP	K73	2K x 8 EPROM
5962–88734 02LX	CY7C291A–45DMB	24.3 DIP	D14	2K x 8 EPROM
5962–88734 023X	CY7C291A–45LMB	28 S LCC	L64	2K x 8 EPROM
5962–88734 03KX	CY7C291A–35KMB	24 CP	K73	2K x 8 EPROM
5962–88734 03LX	CY7C291A–35DMB	24.3 DIP	D14	2K x 8 EPROM
5962–88734 033X	CY7C291A–35LMB	28 S LCC	L64	2K x 8 EPROM
5962–88734 04KX	CY7C291A–25KMB	24 CP	K73	2K x 8 EPROM
5962–88734 04LX	CY7C291A–25DMB	24.3 DIP	D14	2K x 8 EPROM
5962–88734 043X	CY7C291A–25LMB	28 S LCC	L64	2K x 8 EPROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–88735 01KX	CY7C245–45KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 01LX	CY7C245–45DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 013X	CY7C245–45LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–88735 02KX	CY7C245–35KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 02LX	CY7C245–35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 023X	CY7C245–35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–88735 03KX	CY7C245A–35KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 03LX	CY7C245A–35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 033X	CY7C245A–35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–88735 04KX	CY7C245A–25KMB	24 CP	K73	2K x 8 Registered PROM
5962–88735 04LX	CY7C245A–25DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962–88735 043X	CY7C245A–25LMB	28 S LCC	L64	2K x 8 Registered PROM
5962–89468 01XX	CY7C342–35RMB	68 PGA	R68	128-Macrocell UV EPLD
5962–89468 01YX	CY7C342–35HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962–89468 01ZX	CY7C342–35TMB	68 QFP	T91	128-Macrocell UV EPLD
5962–89468 02XX	CY7C342–30RMB	68 PGA	R68	128-Macrocell UV EPLD
5962–89468 02YX	CY7C342–30HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962–89468 02ZX	CY7C342–30TMB	68 QFP	T91	128-Macrocell UV EPLD
5962–89468 03XX	CY7C342B–25RMB	68 PGA	R68	128-Macrocell UV EPLD
5962–89468 03YX	CY7C342B–25HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962–89468 03ZX	CY7C342B–25TMB	68 QFP	T91	128-Macrocell UV EPLD
5962–89468 04XX	CY7C342B–20RMB	68 PGA	R68	128-Macrocell UV EPLD
5962–89468 04YX	CY7C342B–20HMB	68 SOJ	H81	128-Macrocell UV EPLD
5962–89468 04ZX	CY7C342B–20TMB	68 QFP	T91	128-Macrocell UV EPLD
5962–89484 01MXX	CY7C265–50WMB	28 CP	W22	8K x 8 Registered UV PROM
5962–89484 01M3X	CY7C265–50QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962–89484 02MXX	CY7C265–25WMB	28 CP	W22	8K x 8 Registered UV PROM
5962–89484 02M3X	CY7C265–25QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962–89484 03MXX	CY7C265–15WMB	28 CP	W22	8K x 8 Registered UV PROM
5962–89484 03M3X	CY7C265–15QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962–89517 01YX	CY7C9101–45LMB	68 S LCC	L81	16-Bit Slice
5962–89517 02YX	CY7C9101–35LMB	68 S LCC	L81	16-Bit Slice
5962–89523 01EX	CY7C403–10DMB	16.3 DIP	D2	64 x 4 FIFO
5962–89523 012X	CY7C403–10LMB	20 S LCC	L61	64 x 4 FIFO
5962–89523 02EX	CY7C403–15DMB	16.3 DIP	D2	64 x 4 FIFO
5962–89523 022X	CY7C403–15LMB	20 S LCC	L61	64 x 4 FIFO
5926–89523 05EX	CY7C401–10DMB	16.3 DIP	D2	64 x 4 FIFO
5926–89523 052X	CY7C401–10LMB	20 S LCC	L61	64 x 4 FIFO
5926–89523 06EX	CY7C401–15DMB	16.3 DIP	D2	64 x 4 FIFO
5926–89523 062X	CY7C401–15LMB	20 S LCC	L61	64 x 4 FIFO
5962–89524 03XX	CY7C195L–45DMB	28.3 DIP	D22	64K x 4 SRAM
5962–89524 04XX	CY7C195L–35DMB	28.3 DIP	D22	64K x 4 SRAM
5962–89524 05XX	CY7C195L–25DMB	28.3 DIP	D22	64K x 4 SRAM
5962–89537 01UX	CY7C251–65QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89537 01YX	CY7C251–65WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962–89537 01ZX	CY7C251–65TMB	28 CP	T74	16K x 8 UV EPROM
5962–89537 02UX	CY7C251–55QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89537 02YX	CY7C251–55WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962–89537 02ZX	CY7C251–55TMB	28 CP	T74	16K x 8 UV EPROM
5962–89537 03UX	CY7C251–45QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89537 03YX	CY7C251–45WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962–89537 03ZX	CY7C251–45TMB	28 CP	T74	16K x 8 UV EPROM
5962–89538 01XX	CY7C254–65WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962–89538 02XX	CY7C254–55WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962–89538 03UX	CY7C254–45QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962–89538 03XX	CY7C254–45WMB	28.3 DIP	W16	16K x 8 UV EPROM
5962–89538 03ZX	CY7C254–45TMB	28 CP	T74	16K x 8 UV EPROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–89546 01XX	CY7C330–28WMB	28.3 DIP	W22	PLD State Machine
5962–89546 02XX	CY7C330–40WMB	28.3 DIP	W22	PLD State Machine
5962–89546 02YX	CY7C330–40TMB	28 CP	T74	PLD State Machine
5962–89546 023X	CY7C330–40QMB	28 S LCC	Q64	PLD State Machine
5962–89546 03XX	CY7C330–50WMB	28.3 DIP	W22	PLD State Machine
5962–89546 03YX	CY7C330–50TMB	28 CP	T74	PLD State Machine
5962–89546 033X	CY7C330–50QMB	28 S LCC	Q64	PLD State Machine
5962–89598 35MMX	CY7C1009–45LMB	32 R LCC	L55	128K x 8 SRAM
5962–89598 35MTX	CY7C109A–45FMB	32 FP	F75	128K x 8 SRAM
5962–89598 35MUX	CY7C109A–45LMB	32 LCC	L55	128K x 8 SRAM
5962–89598 35MZX	CY7C109A–45DMB	32.4 DIP	D44	128K x 8 SRAM
5962–89598 36MMX	CY7C1009–35LMB	32 R LCC	L55	128K x 8 SRAM
5962–89598 36MTX	CY7C109A–35FMB	32 FP	F75	128K x 8 SRAM
5962–89598 36MUX	CY7C109A–35LMB	32 LCC	L55	128K x 8 SRAM
5962–89598 36MZX	CY7C109A–35DMB	32.4 DIP	D44	128K x 8 SRAM
5962–89598 37MMX	CY7C1009–25LMB	32 R LCC	L55	128K x 8 SRAM
5962–89598 37MTX	CY7C109A–25FMB	32 FP	F75	128K x 8 SRAM
5962–89598 37MUX	CY7C109A–25LMB	32 LCC	L55	128K x 8 SRAM
5962–89598 37MZX	CY7C109A–25DMB	32.4 DIP	D44	128K x 8 SRAM
5962–89598 38MMX	CY7C1009–20LMB	32 R LCC	L55	128K x 8 SRAM
5962–89661 01XX	CY7C409A–15DMB	28.3 DIP	D22	64 x 9 FIFO
5962–89661 01YX	CY7C409A–15KMB	28 CP	K74	64 x 9 FIFO
5962–89661 02XX	CY7C409A–25DMB	28.3 DIP	D22	64 x 9 FIFO
5962–89661 02YX	CY7C409A–25KMB	28 CP	K74	64 x 9 FIFO
5962–89664 01XX	CY7C408A–15DMB	28.3 DIP	D22	64 x 8 FIFO
5962–89664 02XX	CY7C408A–25DMB	28.3 DIP	D22	64 x 8 FIFO
5962–89690 01JX	CY6116A–25DMB	24.6 DIP	D12	2K x 8 SRAM
5962–89690 01KX	CY7C128A–25KMB	24 CP	K73	2K x 8 SRAM
5962–89690 01LX	CY7C128A–25DMB	24.3 DIP	D14	2K x 8 SRAM
5962–89690 01XX	CY6117A–25LMB	32 R LCC	L55	2K x 8 SRAM
5962–89690 01YX	CY7C128A–25LMB	24 R LCC	L53	2K x 8 SRAM
5962–89690 013X	CY6116A–25LMB	28 S LCC	L64	2K x 8 SRAM
5962–89690 02JX	CY6116A–20DMB	24.6 DIP	D12	2K x 8 SRAM
5962–89690 02KX	CY7C128A–20KMB	24 CP	K73	2K x 8 SRAM
5962–89690 02LX	CY7C128A–20DMB	24.3 DIP	D14	2K x 8 SRAM
5962–89690 02XX	CY6117A–20LMB	32 R LCC	L55	2K x 8 SRAM
5962–89690 02YX	CY7C128A–20LMB	24 R LCC	L53	2K x 8 SRAM
5962–89690 023X	CY6116A–20LMB	28 S LCC	L64	2K x 8 SRAM
5962–89691 02TX	CY7C185A–25KMB	28 CP	K74	8K x 8 SRAM
5962–89691 02UX	CY7C185A–25LMB	28 R TLCC	L54	8K x 8 SRAM
5962–89691 02XX	CY7C186A–25DMB	28.6 DIP	D16	8K x 8 SRAM
5962–89691 02ZX	CY7C185A–25DMB	28.3 DIP	D22	8K x 8 SRAM
5962–89691 04TX	CY7C185A–20KMB	28 CP	K74	8K x 8 SRAM
5962–89691 04UX	CY7C185A–20LMB	28 R TLCC	L54	8K x 8 SRAM
5962–89691 04XX	CY7C186A–20DMB	28.6 DIP	D16	8K x 8 SRAM
5962–89691 04ZX	CY7C185A–20DMB	28.3 DIP	D22	8K x 8 SRAM
5962–89692 02KX	CY7C164A–25KMB	24 CP	K73	16K x 4 SRAM
5962–89692 02YX	CY7C164A–25DMB	22.3 DIP	D10	16K x 4 SRAM
5962–89692 04KX	CY7C164A–20KMB	24 CP	K73	16K x 4 SRAM
5962–89692 04YX	CY7C164A–20DMB	22.3 DIP	D10	16K x 4 SRAM
5962–89694 01EX	CY7C190–25DMB	16.3 DIP	D2	16 x 4 SRAM
5962–89790 02KX	CY7C172A–20KMB	24 CP	K73	4K x 4 SRAM with Separate I/O
5962–89790 02LX	CY7C172A–20DMB	24.3 DIP	D14	4K x 4 SRAM with Separate I/O
5962–89790 023X	CY7C172A–20LMB	28 S LCC	L64	4K x 4 SRAM with Separate I/O
5962–89815 01LX	CY7C245A–35WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962–89815 01KX	CY7C245A–35TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962–89815 013X	CY7C245A–35QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM
5962–89815 02LX	CY7C245A–25WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962–89815 02KX	CY7C245A–25TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962–89815 023X	CY7C245A–25QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–89815 03LX	CY7C245A–18WMB	24.3 DIP	W14	2K x 8 Registered UV EPROM
5962–89815 03KX	CY7C245A–18TMB	24 CP	T73	2K x 8 Registered UV EPROM
5962–89815 033X	CY7C245A–18QMB	28 S LCC	Q64	2K x 8 Registered UV EPROM
5962–89817 01XX	CY7C271–55WMB	28.3 DIP	W16	32K x 8 UV EPROM
5962–89817 01YX	CY7C271–55TMB	28 CP	T74	32K x 8 UV EPROM
5962–89817 01ZX	CY7C271–55QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962–89817 02XX	CY7C271–45WMB	28.3 DIP	W16	32K x 8 UV EPROM
5962–89817 02YX	CY7C271–45TMB	28 CP	T74	32K x 8 UV EPROM
5962–89817 02ZX	CY7C271–45QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962–89817 03XX	CY7C271–35WMB	28.3 DIP	W22	32K x 8 UV EPROM
5962–89817 03YX	CY7C271–35TMB	28 CP	T74	32K x 8 UV EPROM
5962–89817 03ZX	CY7C271–35QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962–89817 04UX	CY7C274–55WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962–89817 04ZX	CY7C274–55QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962–89817 05UX	CY7C274–45WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962–89817 05ZX	CY7C274–45QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962–89817 06UX	CY7C274–35WMB	28.6 DIP	W16	32K x 8 UV EPROM
5962–89817 06ZX	CY7C274–35QMB	32 R LCC	Q55	32K x 8 UV EPROM
5962–89841 01KX	PALC22V10D–30KMB	24 CP	K73	CMOS EE PLD
5962–89841 01LX	PALC22V10D–30DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 013X	PALC22V10D–30LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 02KX	PALC22V10D–20KMB	24 CP	K73	CMOS EE PLD
5962–89841 02LX	PALC22V10D–20DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 023X	PALC22V10D–20LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 03KX	PALC22V10D–15KMB	24 CP	K73	CMOS EE PLD
5962–89841 03LX	PALC22V10D–15DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 033X	PALC22V10D–15LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 04KX	PALC22V10D–25KMB	24 CP	K73	CMOS EE PLD
5962–89841 04LX	PALC22V10D–25DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 043X	PALC22V10D–25LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 05KX	PALC22V10D–15KMB	24 CP	K73	CMOS EE PLD
5962–89841 05LX	PALC22V10D–15DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 053X	PALC22V10D–15LMB	28 S LCC	L64	CMOS EE PLD
5962–89841 06KX	PALC22V10D–10KMB	24 CP	K73	CMOS EE PLD
5962–89841 06LX	PALC22V10D–10DMB	24.3 DIP	D14	CMOS EE PLD
5962–89841 063X	PALC22V10D–10LMB	28 S LCC	L64	CMOS EE PLD
5962–89855 01MYX	CY7C331–40KMB	28 CP	K74	Asynchronous PLD
5962–89855 01MZX	CY7C331–40YMB	28 S JCQ	Y64	Asynchronous PLD
5962–89855 01M3X	CY7C331–40LMB	28 S LCC	L64	Asynchronous PLD
5962–89855 02MXX	CY7C331–30DMB	28.3 DIP	D22	Asynchronous PLD
5962–89855 02MYX	CY7C331–30KMB	28 CP	K74	Asynchronous PLD
5962–89855 02MZX	CY7C331–30YMB	28 S JCQ	Y64	Asynchronous PLD
5962–89855 03MXX	CY7C331–25DMB	28.3 DIP	D22	Asynchronous PLD
5962–89855 03MYX	CY7C331–25KMB	28 CP	K74	Asynchronous PLD
5962–89855 03MZX	CY7C331–25YMB	28 S JCQ	Y64	Asynchronous PLD
5962–89855 03M3X	CY7C331–25LMB	28 S LCC	L64	Asynchronous PLD
5962–89863 02XX	CY7C420–65DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 02YX	CY7C421–65DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 02ZX	CY7C421–65LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 03XX	CY7C420–50DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 03YX	CY7C421–50DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 03ZX	CY7C421–50LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 04XX	CY7C420–40DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 04YX	CY7C421–40DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 04ZX	CY7C421–40LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 05XX	CY7C420–30DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 05YX	CY7C421–30DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 05ZX	CY7C421–30LMB	32 R LCC	L55	512 x 9 FIFO
5962–89863 06XX	CY7C420–25DMB	28.6 DIP	D16	512 x 9 FIFO
5962–89863 06YX	CY7C421–25DMB	28.3 DIP	D22	512 x 9 FIFO
5962–89863 06ZX	CY7C421–25LMB	32 R LCC	L55	512 x 9 FIFO

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962–89892 02LX	CY7C166A–25DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–89892 04LX	CY7C166A–20DMB	24.3 DIP	D14	16K x 4 SRAM w/OE
5962–89935 01XX	CY7C192–45DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O
5962–89935 01ZX	CY7C192–45LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O
5962–89935 02XX	CY7C192–35DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O
5962–89935 02ZX	CY7C192–35LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O
5962–89935 03XX	CY7C192–25DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O
5962–89935 03ZX	CY7C192–25LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O
5962–89967 01MXX	CY7C265–60DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962–89967 01MYX	CY7C265–60KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962–89967 02MXX	CY7C265–50DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962–89967 02MYX	CY7C265–50KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962–89967 03MXX	CY7C265–25DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962–89967 03MYX	CY7C265–25KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962–89967 04MXX	CY7C265–18DMB	28.3 DIP	D22	8K x 8 Registered OTP PROM
5962–89967 04MYX	CY7C265–18KMB	28 CP	K74	8K x 8 Registered OTP PROM
5962–90555 01LX	PLDC20RA10–35DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962–90555 02KX	PLDC20RA10–25KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962–90555 02LX	PLDC20RA10–25DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962–90555 03KX	PLDC20RA10–20KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962–90555 03LX	PLDC20RA10–20DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962–90555 033X	PLDC20RA10–20LMB	28 S LCC	L64	Asynchronous CMOS OTP PLD
5962–90594 03XX	CY7C161A–25DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O, TW
5962–90594 04XX	CY7C161A–20DMB	28.3 DIP	D22	16K x 4 SRAM with Separate I/O, TW
5962–90611 02XX	CY7C344–25WMB	28.3 DIP	W22	32-Macrocell UV EPLD
5962–90611 02YX	CY7C344–25HMB	28 S JCQ	H64	32-Macrocell UV EPLD
5962–90620 01MYX	CY7C132–55DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962–90620 02MYX	CY7C132–45DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962–90620 03MYX	CY7C132–35DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962–90620 04MYX	CY7C142–55DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962–90620 05MYX	CY7C142–45DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962–90620 06MYX	CY7C142–35DMB	48.6 DIP	D26	2K x 8 Dual-Port SRAM
5962–90620 07MXX	CY7C136–55LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962–90620 08MXX	CY7C136–45LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962–90620 09MXX	CY7C136–35LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962–90620 10MXX	CY7C146–55LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962–90620 11MXX	CY7C146–45LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962–90620 12MXX	CY7C146–35LMB	52 LCC	L69	2K x 8 Dual-Port SRAM
5962–90644 01XX	CY7C191–45DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O, TW
5962–90644 01YX	CY7C191–45KMB	28 CP	K74	64K x 4 SRAM with Separate I/O, TW
5962–90644 01ZX	CY7C191–45LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O, TW
5962–90644 02XX	CY7C191–35DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O, TW
5962–90644 02YX	CY7C191–35KMB	28 CP	K74	64K x 4 SRAM with Separate I/O, TW
5962–90644 02ZX	CY7C191–35LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O, TW
5962–90644 03XX	CY7C191–25DMB	28.3 DIP	D22	64K x 4 SRAM with Separate I/O, TW
5962–90644 03YX	CY7C191–25KMB	28 CP	K74	64K x 4 SRAM with Separate I/O, TW
5962–90644 03ZX	CY7C191–25LMB	28 R LCC	L54	64K x 4 SRAM with Separate I/O, TW
5962–90696 01MLX	CY7C123–15DMB	24.3 DIP	D14	256 x 4 SRAM with Separate I/O
5962–90696 02MLX	CY7C123–12DMB	24.3 DIP	D14	256 x 4 SRAM with Separate I/O
5962–90696 03MLX	CY7C123–10DMB	24.3 DIP	D14	256 x 4 SRAM with Separate I/O
5962–90715 03MUX	CY7C433–65DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 03MXX	CY7C432–65DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 03MZX	CY7C433–65LMB	32 R LCC	L55	4K x 9 FIFO
5962–90715 04MUX	CY7C433–50DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 04MXX	CY7C432–50DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 04MZX	CY7C433–50LMB	32 R LCC	L55	4K x 9 FIFO
5962–90715 05MUX	CY7C433–40DMB	28.3 DIP	D22	4K x 9 FIFO
5962–90715 05MXX	CY7C432–40DMB	28.6 DIP	D16	4K x 9 FIFO
5962–90715 05MZX	CY7C433–40LMB	32 R LCC	L55	4K x 9 FIFO

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-90715 06MUX	CY7C433-30DMB	28.3 DIP	D22	4K x 9 FIFO
5962-90715 06MXX	CY7C432-30DMB	28.6 DIP	D16	4K x 9 FIFO
5962-90715 06MZX	CY7C433-30LMB	32 R LCC	L55	4K x 9 FIFO
5962-90754 01MYX	CY7C331-40TMB	28 CP	T74	Asynchronous UV PLD
5962-90754 01MZX	CY7C331-40HMB	28 S JCQ	H64	Asynchronous UV PLD
5962-90754 02MYX	CY7C331-30TMB	28 CP	T74	Asynchronous UV PLD
5962-90754 02MZX	CY7C331-30HMB	28 S JCQ	H64	Asynchronous UV PLD
5962-90754 02M3X	CY7C331-30QMB	28 S LCC	Q64	Asynchronous UV PLD
5962-90754 03MXX	CY7C331-25WMB	28.3 DIP	W22	Asynchronous UV PLD
5962-90754 03MYX	CY7C331-25TMB	28 CP	T74	Asynchronous UV PLD
5962-90754 03MZX	CY7C331-25HMB	28 S JCQ	H64	Asynchronous UV PLD
5962-90754 03M3X	CY7C331-25QMB	28 S LCC	Q64	Asynchronous UV PLD
5962-90803 01MLX	CY7C261-55DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 01M3X	CY7C261-55LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 02MLX	CY7C261-45DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 02M3X	CY7C261-45LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 03MLX	CY7C261-35DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 03M3X	CY7C261-35LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 04MLX	CY7C261-25DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 04M3X	CY7C261-25LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 05MJX	CY7C264-55DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803 05MLX	CY7C263-55DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 05M3X	CY7C263-55LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 06MJX	CY7C264-45DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803 06MLX	CY7C263-45DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 06M3X	CY7C263-45LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 07MJX	CY7C264-35DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803 07MLX	CY7C263-35DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 07M3X	CY7C263-35LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90803 08MJX	CY7C264-25DMB	24.6 DIP	D12	8K x 8 OTP PROM
5962-90803 08MLX	CY7C263-25DMB	24.3 DIP	D14	8K x 8 OTP PROM
5962-90803 08M3X	CY7C263-25LMB	28 S LCC	L64	8K x 8 OTP PROM
5962-90831 01MXX	CY7C269-60DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90831 02MXX	CY7C269-50DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90831 03MXX	CY7C269-25DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90831 04MXX	CY7C269-18DMB	28.3 DIP	D22	8K x 8 REG OTP PROM
5962-90913 01MXX	CY7C287-65WMB	28.3 DIP	W22	64K x 8 Registered UV PROM
5962-90913 01MYX	CY7C287-65QMB	32 R LCC	Q55	64K x 8 Registered UV PROM
5962-90913 02MXX	CY7C287-55WMB	28.3 DIP	W22	64K x 8 Registered UV PROM
5962-90913 02MYX	CY7C287-55QMB	32 R LCC	Q55	64K x 8 Registered UV PROM
5962-90930 01MXX	CY7C269-50WMB	28.3 DIP	W22	8K x 8 Registered UV PROM
5962-90930 01MYX	CY7C269-50TMB	28 CP	T74	8K x 8 Registered UV PROM
5962-90930 01M3X	CY7C269-50QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-90930 02MXX	CY7C269-25WMB	28.3 DIP	W22	8K x 8 Registered UV PROM
5962-90930 02MYX	CY7C269-25TMB	28 CP	T74	8K x 8 Registered UV PROM
5962-90930 02M3X	CY7C269-25QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-90930 03MXX	CY7C269-15WMB	28.3 DIP	W22	8K x 8 Registered UV PROM
5962-90930 03MYX	CY7C269-15TMB	28 CP	T74	8K x 8 Registered UV PROM
5962-90930 03M3X	CY7C269-15QMB	28 S LCC	Q64	8K x 8 Registered UV PROM
5962-90989 01MLX	PLDC20RA10-35WMB	24.3 DIP	W14	Asynchronous CMOS UV EPLD
5962-90989 02MLX	PLDC20RA10-25WMB	24.3 DIP	W14	Asynchronous CMOS UV EPLD
5962-90989 02M3X	PLDC20RA10-25QMB	28 S LCC	Q64	Asynchronous CMOS UV EPLD
5962-90989 03MLX	PLDC20RA10-20WMB	24.3 DIP	W14	Asynchronous CMOS UV EPLD
5962-90989 03M3X	PLDC20RA10-20QMB	28 S LCC	Q64	Asynchronous CMOS UV EPLD
5962-91518 01MZX	CY10E474L-7KMB	24 CP	K63	1K x 4 ECL SRAM
5962-91518 02MZX	CY10E474L-5KMB	24 CP	K63	1K x 4 ECL SRAM
5962-91584 01MYX	CY7C332-25TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962-91584 01MZX	CY7C332-25HMB	28 S JCQ	H64	Registered Combinatorial UV EPLD
5962-91584 02MYX	CY7C332-20TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962-91584 02MZX	CY7C332-20HMB	28 S JCQ	H64	Registered Combinatorial UV EPLD
5962-91584 02M3X	CY7C332-20QMB	28 S LCC	Q64	Registered Combinatorial UV EPLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-91585 03MXX	CY7C425-65DMB	28.3 DIP	D22	1K x 9 FIFO
5962-91585 03MYX	CY7C424-65DMB	28.6 DIP	D16	1K x 9 FIFO
5962-91585 03MUX	CY7C425-65LMB	32 R LCC	L55	1K x 9 FIFO
5962-91585 04MXX	CY7C425-50DMB	28.3 DIP	D22	1K x 9 FIFO
5962-91585 04MYX	CY7C424-50DMB	28.6 DIP	D16	1K x 9 FIFO
5962-91585 04MUX	CY7C425-50LMB	32 R LCC	L55	1K x 9 FIFO
5962-91585 05MXX	CY7C425-40DMB	28.3 DIP	D22	1K x 9 FIFO
5962-91585 05MYX	CY7C424-40DMB	28.6 DIP	D16	1K x 9 FIFO
5962-91585 05MUX	CY7C425-40LMB	32 R LCC	L55	1K x 9 FIFO
5962-91585 06MXX	CY7C425-30DMB	28.3 DIP	D22	1K x 9 FIFO
5962-91585 06MYX	CY7C424-30DMB	28.6 DIP	D16	1K x 9 FIFO
5962-91585 06MUX	CY7C425-30LMB	32 R LCC	L55	1K x 9 FIFO
5962-91594 01MYX	CY7B185-15LMB	28 R LCC	L54	8K x 8 BiCMOS SRAM
5962-91594 01MZX	CY7B185-15DMB	28.3 DIP	D22	8K x 8 BiCMOS SRAM
5962-91594 01MTX	CY7B185-15KMB	28 CP	K74	8K x 8 BiCMOS SRAM
5962-91594 02MYX	CY7B185-12LMB	28 R LCC	L54	8K x 8 BiCMOS SRAM
5962-91594 02MZX	CY7B185-12DMB	28.3 DIP	D22	8K x 8 BiCMOS SRAM
5962-91594 03MYX	CY7B185-10LMB	28 R LCC	L54	8K x 8 BiCMOS SRAM
5962-91594 03MZX	CY7B185-10DMB	28.3 DIP	D22	8K x 8 BiCMOS SRAM
5962-91744 01MXX	CY7C277-50WMB	28.3 DIP	W22	32K X 8 Registered UV PROM
5962-91744 01MYX	CY7C277-50QMB	32 R LCC	Q55	32K X 8 Registered UV PROM
5962-91744 01MZX	CY7C277-50TMB	28 CP	T74	32K X 8 Registered UV PROM
5962-91744 02MXX	CY7C277-40WMB	28.3 DIP	W22	32K X 8 Registered UV PROM
5962-91744 02MYX	CY7C277-40QMB	32 R LCC	Q55	32K X 8 Registered UV PROM
5962-91744 02MZX	CY7C277-40TMB	28 CP	T74	32K X 8 Registered UV PROM
5962-91760 01M3X	PAL22V10G-15LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 02M3X	PAL22V10G-12LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 03M3X	PAL22V10G-10LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 04M3X	PAL22VP10G-15LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 05M3X	PAL22VP10G-12LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 06M3X	PAL22VP10G-10LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 09M3X	PAL22V10G-7LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 10M3X	PAL22VP10G-7LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-92009 01MXC	VAC068A-GMB	145 PGA	G145	VME Address Controller
5962-92009 01MYC	VAC068A-UMB	160 FP	U162	VME Address Controller
5962-92010 01MXC	VIC068A-GMB	145 PGA	G145	VME Interface Controller
5962-92010 01MYC	VIC068A-UMB	160 FP	U162	VME Interface Controller
5962-92062 01MYX	CY7C341-40RMB	84 PGA	R84	192-Macrocell UV EPLD
5962-92062 02MXX	CY7C341-30HMB	84 S JCQ	H84	192-Macrocell UV EPLD
5962-92062 02MYX	CY7C341-30RMB	84 PGA	R84	192-Macrocell UV EPLD
5962-92062 03MXX	CY7C341-35HMB	84 S JCQ	H84	192-Macrocell UV EPLD
5962-92062 03MYX	CY7C341-35RMB	84 PGA	R84	192-Macrocell UV EPLD
5962-92065 01MYX	CY7C287-65RMB	32 R LCC	L55	64K X 8 REG OTP PROM
5962-92065 02MYX	CY7C287-55RMB	32 R LCC	L55	64K X 8 REG OTP PROM
5962-92071 01MXX	CY7C286-70WMB	28.3 DIP	W16	64K X 8 REG UV EPROM
5962-92071 02MXX	CY7C286-60WMB	28.3 DIP	W16	64K X 8 REG UV EPROM
5962-92155 01MXX	CY7C277-50DMB	28.3 DIP	D22	32K X 8 Registered OTP PROM
5962-92155 01MYX	CY7C277-50LMB	32 R LCC	L55	32K X 8 Registered OTP PROM
5962-92155 02MXX	CY7C277-40DMB	28.3 DIP	D22	32K X 8 Registered OTP PROM
5962-92155 02MYX	CY7C277-40LMB	32 R LCC	L55	32K X 8 Registered OTP PROM
5962-92158 02MXX	CY7C343-30HMB	44 S JCQ	H67	64-Macrocell UV EPLD
5962-92203 01MRX	CY54FCT244TDMB	20.3 DIP	D6	Octal Buffer/Driver NI
5962-92203 01M2X	CY54FCT244TLMB	20 S LCC	L61	Octal Buffer/Driver NI
5962-92203 02MRX	CY54FCT244ATDMB	20.3 DIP	D6	Octal Buffer/Driver NI
5962-92203 02M2X	CY54FCT244ATLMB	20 S LCC	L61	Octal Buffer/Driver NI
5962-92203 03MRX	CY54FCT244CTDMB	20.3 DIP	D6	Octal Buffer/Driver NI
5962-92203 03M2X	CY54FCT244CTLMB	20 S LCC	L61	Octal Buffer/Driver NI
5962-92213 01MRX	CY54FCT240TDMB	20.3 DIP	D6	Octal Buffer/Driver I
5962-92213 01M2X	CY54FCT240TLMB	20 S LCC	L61	Octal Buffer/Driver I

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-92213 03MRX	CY54FCT240ATDMB	20.3 DIP	D6	Octal Buffer/Driver I
5962-92213 03M2X	CY54FCT240ATLMB	20 S LCC	L61	Octal Buffer/Driver I
5962-92213 05MRX	CY54FCT240CTDMB	20.3 DIP	D6	Octal Buffer/Driver I
5962-92213 05M2X	CY54FCT240CTLMB	20 S LCC	L61	Octal Buffer/Driver I
5962-92214 01MRX	CY54FCT245TDMB	20.3 DIP	D6	Octal Tranceiver
5962-92214 01M2X	CY54FCT245TLMB	20 S LCC	L61	Octal Tranceiver
5962-92214 03MRX	CY54FCT245ATDMB	20.3 DIP	D6	Octal Tranceiver
5962-92214 03M2X	CY54FCT245ATLMB	20 S LCC	L61	Octal Tranceiver
5962-92214 05MRX	CY54FCT245CTDMB	20.3 DIP	D6	Octal Tranceiver
5962-92214 05M2X	CY54FCT245CTLMB	20 S LCC	L61	Octal Tranceiver
5962-92215 01MRX	CY54FCT273TDMB	20.3 DIP	D6	Octal D Flip-Flops
5962-92215 01M2X	CY54FCT273TLMB	20 S LCC	L61	Octal D Flip-Flops
5962-92215 03MRX	CY54FCT273ATDMB	20.3 DIP	D6	Octal D Flip-Flops
5962-92215 03M2X	CY54FCT273ATLMB	20 S LCC	L61	Octal D Flip-Flops
5962-92215 05MRX	CY54FCT273CTDMB	20.3 DIP	D6	Octal D Flip-Flops
5962-92215 05M2X	CY54FCT273CTLMB	20 S LCC	L61	Octal D Flip-Flops
5962-92217 01MRX	CY54FCT373TDMB	20.3 DIP	D6	Octal Transparent Latch
5962-92217 01M2X	CY54FCT373TLMB	20 S LCC	L61	Octal Transparent Latch
5962-92217 02MRX	CY54FCT373ATDMB	20.3 DIP	D6	Octal Transparent Latch
5962-92217 02M2X	CY54FCT373ATLMB	20 S LCC	L61	Octal Transparent Latch
5962-92217 03MRX	CY54FCT373CTDMB	20.3 DIP	D6	Octal Transparent Latch
5962-92217 03M2X	CY54FCT373CTLMB	20 S LCC	L61	Octal Transparent Latch
5962-92218 02MRX	CY54FCT374TDMB	20.3 DIP	D6	Octal D Flip-Flop W/OE
5962-92218 02M2X	CY54FCT374TLMB	20 S LCC	L61	Octal D Flip-Flop W/OE
5962-92218 04MRX	CY54FCT374ATDMB	20.3 DIP	D6	Octal D Flip-Flop W/OE
5962-92218 04M2X	CY54FCT374ATLMB	20 S LCC	L61	Octal D Flip-Flop W/OE
5962-92218 06MRX	CY54FCT374CTDMB	20.3 DIP	D6	Octal D Flip-Flop W/OE
5962-92218 06M2X	CY54FCT374CTLMB	20 S LCC	L61	Octal D Flip-Flop W/OE
5962-92219 01MRX	CY54FCT377TDMB	20.3 DIP	D6	Octal D Flip-Flop W/CE
5962-92219 01M2X	CY54FCT377TLMB	20 S LCC	L61	Octal D Flip-Flop W/CE
5962-92219 02MRX	CY54FCT377ATDMB	20.3 DIP	D6	Octal D Flip-Flop W/CE
5962-92219 02M2X	CY54FCT377ATLMB	20 S LCC	L61	Octal D Flip-Flop W/CE
5962-92219 03MRX	CY54FCT377CTDMB	20.3 DIP	D6	Octal D Flip-Flop W/CE
5962-92219 03M2X	CY54FCT377CTLMB	20 S LCC	L61	Octal D Flip-Flop W/CE
5962-92221 01MLX	CY54FCT543TDMB	24.3 DIP	D14	Octal Tranceiver/Reg
5962-92221 01M3X	CY54FCT543TLMB	28 S LCC	L64	Octal Tranceiver/Reg
5962-92221 02MLX	CY54FCT543ATDMB	24.3 DIP	D14	Octal Tranceiver/Reg
5962-92221 02M3X	CY54FCT543ATLMB	28 S LCC	L41	Octal Tranceiver/Reg
5962-92221 03MLX	CY54FCT543CTDMB	24.3 DIP	D14	Octal Tranceiver/Reg
5969-92221 03M3X	CY54FCT543CTLMB	28 S LCC	L64	Octal Tranceiver/Reg
5962-92222 01MRX	CY54FCT574TDMB	20.3 DIP	D6	Octal D Register
5962-92222 01M2X	CY54FCT574TLMB	20 S LCC	L61	Octal D Register
5962-92222 03MRX	CY54FCT574ATDMB	20.3 DIP	D6	Octal D Register
5962-92222 03M2X	CY54FCT574ATLMB	20 S LCC	L61	Octal D Register
5962-92222 05MRX	CY54FCT574CTDMB	20.3 DIP	D6	Octal D Register
5962-92222 05M2X	CY54FCT574CTLMB	20 S LCC	L61	Octal D Register
5962-92223 01MLX	CY54FCT646TDMB	24.3 DIP	D14	Octal Reg Tranceiver
5962-92223 01M3X	CY54FCT646TLMB	28 S LCC	L64	Octal Reg Tranceiver
5962-92223 03MLX	CY54FCT646ATDMB	24.3 DIP	D14	Octal Reg Tranceiver
5962-92223 03M3X	CY54FCT646ATLMB	28 S LCC	L41	Octal Reg Tranceiver
5962-92223 05MLX	CY54FCT646CTDMB	24.3 DIP	D14	Octal Reg Tranceiver
5969-92223 05M3X	CY54FCT646CTLMB	28 S LCC	L64	Octal Reg Tranceiver
5962-92230 01MLX	CY54FCT825ATDMB	24.3 DIP	D14	Octal Register W/OE
5962-92230 01M3X	CY54FCT825ATLMB	28 S LCC	L64	Octal Register W/OE
5962-92230 03MLX	CY54FCT825BTDMB	24.3 DIP	D14	Octal Register W/OE
5962-92230 03M3X	CY54FCT825BTLMB	28 S LCC	L41	Octal Register W/OE
5962-92230 05MLX	CY54FCT825CTDMB	24.3 DIP	D14	Octal Register W/OE
5969-92230 05M3X	CY54FCT825CTLMB	28 S LCC	L64	Octal Register W/OE
5962-92233 02MEX	CY54FCT138TDMB	16.3 DIP	D2	1-of-8 Decoder
5962-92233 02M2X	CY54FCT138TLMB	20 S LCC	L61	1-of-8 Decoder

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962–92233 04MEX	CY54FCT138ATDMB	16.3 DIP	D2	1-of-8 Decoder
5962–92233 04M2X	CY54FCT138ATLMB	20 S LCC	L61	1-of-8 Decoder
5962–92233 06MEX	CY54FCT138CTDMB	16.3 DIP	D2	1-of-8 Decoder
5962–92233 06M2X	CY54FCT138CTLMB	20 S LCC	L61	1-of-8 Decoder
5962–92237 01MRX	CY54FCT541TDMB	20.3 DIP	D6	Octal Buffer/Driver
5962–92237 01M2X	CY54FCT541TLMB	20 S LCC	L61	Octal Buffer/Driver
5962–92237 03MRX	CY54FCT541ATDMB	20.3 DIP	D6	Octal Buffer/Driver
5962–92237 03M2X	CY54FCT541ATLMB	20 S LCC	L61	Octal Buffer/Driver
5962–92237 05MRX	CY54FCT541CTDMB	20.3 DIP	D6	Octal Buffer/Driver
5962–92237 05M2X	CY54FCT541CTLMB	20 S LCC	L61	Octal Buffer/Driver
5962–92238 01MRX	CY54FCT573TDMB	20.3 DIP	D6	Octal Transparent Latch
5962–92238 01M2X	CY54FCT573TLMB	20 S LCC	L61	Octal Transparent Latch
5962–92238 02MRX	CY54FCT573ATDMB	20.3 DIP	D6	Octal Transparent Latch
5962–92238 02M2X	CY54FCT573ATLMB	20 S LCC	L61	Octal Transparent Latch
5962–92238 03MRX	CY54FCT573CTDMB	20.3 DIP	D6	Octal Transparent Latch
5962–92238 03M2X	CY54FCT573CTLMB	20 S LCC	L61	Octal Transparent Latch
5962–92247 01MLX	CY54FCT827ATDMB	24.3 DIP	D14	10-Bit Buffer
5962–92247 01M3X	CY54FCT827ATLMB	28 S LCC	L64	10-Bit Buffer
5962–92247 03MLX	CY54FCT827BTDMB	24.3 DIP	D14	10-Bit Buffer
5962–92247 03M3X	CY54FCT827BTLMB	28 S LCC	L41	10-Bit Buffer
5962–92247 05MLX	CY54FCT827CTDMB	24.3 DIP	D14	10-Bit Buffer
5962–92247 05M3X	CY54FCT827CTLMB	28 S LCC	L64	10-Bit Buffer
5962–92321 01MXX	CY7C439–65DMB	28.3 DIP	D22	2K x 9 BiFIFO
5962–92321 01MYX	CY7C439–65KMB	28 CP	K74	2K x 9 BiFIFO
5962–92321 01MZX	CY7C439–65LMB	32 R LCC	L55	2K x 9 BiFIFO
5962–92321 02MXX	CY7C439–40DMB	28.3 DIP	D22	2K x 9 BiFIFO
5962–92321 02MYX	CY7C439–40KMB	28 CP	K74	2K x 9 BiFIFO
5962–92321 02MZX	CY7C439–40LMB	32 R LCC	L55	2K x 9 BiFIFO
5962–92321 03MXX	CY7C439–30DMB	28.3 DIP	D22	2K x 9 BiFIFO
5962–92321 03MYX	CY7C439–30KMB	28 CP	K74	2K x 9 BiFIFO
5962–92321 03MZX	CY7C439–30LMB	32 R LCC	L55	2K x 9 BiFIFO
5962–92338 01MRX	PAL16L8–10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 01MSX	PAL16L8–10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 01MXX	PAL16L8–10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 02MRX	PAL16R8–10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 02MSX	PAL16R8–10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 02MXX	PAL16R8–10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 03MRX	PAL16R6–10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 03MSX	PAL16R6–10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 03MXX	PAL16R6–10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 04MRX	PAL16R4–10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 04MSX	PAL16R4–10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 04MXX	PAL16R4–10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 05MRX	PAL16L8–7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 05MSX	PAL16L8–7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 05MXX	PAL16L8–7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 06MRX	PAL16R8–7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 06MSX	PAL16R8–7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 06MXX	PAL16R8–7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 07MRX	PAL16R6–7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 07MSX	PAL16R6–7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 07MXX	PAL16R6–7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–92338 08MRX	PAL16R4–7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962–92338 08MSX	PAL16R4–7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962–92338 08MXX	PAL16R4–7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962–93008 01MXX	CY7C462-40DMB	28.6 DIP	TBD	16K X 9 FIFO
5962–93008 01MYX	CY7C462-40LMB	32 R LCC	L55	16K X 9 FIFO
5962–93008 02MXX	CY7C462-25DMB	28.6 DIP	TBD	16K X 9 FIFO
5962–93008 02MYX	CY7C462-25LMB	32 R LCC	L55	16K X 9 FIFO
5962–93008 03MXX	CY7C462-20DMB	28.6 DIP	TBD	16K X 9 FIFO
5962–93008 03MYX	CY7C462-20LMB	32 R LCC	L55	16K X 9 FIFO

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-93112 01MXX	CY7B992-7LMB	32 R LCC	D2	Prog Skew Clock Buffer
5962-93124 01MXX	CY7C453-30DMB	32.3 DIP	D32	2K x 9 Clocked FIFO
5962-93124 01MYX	CY7C453-30LMB	32 R LCC	L55	2K x 9 Clocked FIFO
5962-93124 02MXX	CY7C453-20DMB	32.3 DIP	D32	2K x 9 Clocked FIFO
5962-93124 02MYX	CY7C453-20LMB	32 R LCC	L55	2K x 9 Clocked FIFO
5962-93124 03MXX	CY7C453-14DMB	32.3 DIP	D32	2K x 9 Clocked FIFO
5962-93124 03MYX	CY7C453-14LMB	32 R LCC	L55	2K x 9 Clocked FIFO
5962-93144 01MZX	CY7C346-35RMB	100 PGA	R100	128-Macrocell UV EPLD
5962-93144 01MUX	CY7C346-35HMB	84 S JCQ	H84	128-Macrocell UV EPLD
5962-93144 02MZX	CY7C346-30RMB	100 PGA	R100	128-Macrocell UV EPLD
5962-93144 02MUX	CY7C346-30HMB	84 S JCQ	H84	128-Macrocell UV EPLD
5962-93152 01MXX	CY7C464-40DMB	28.6 DIP	TBD	32K X 9 FIFO
5962-93152 01MYX	CY7C464-40LMB	32 R LCC	L55	32K X 9 FIFO
5962-93152 02MXX	CY7C464-25DMB	28.6 DIP	TBD	32K X 9 FIFO
5962-93152 02MYX	CY7C464-25LMB	32 R LCC	L55	32K X 9 FIFO
5962-93152 03MXX	CY7C464-20DMB	28.6 DIP	TBD	32K X 9 FIFO
5962-93152 03MYX	CY7C464-20LMB	32 R LCC	L55	32K X 9 FIFO
5962-93166 01MXX	CY7C271-55DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 02MXX	CY7C271-45DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93166 03MXX	CY7C271-35DMB	28.3 DIP	D22	32K x 8 OTP PROM
5962-93173 01MXX	CY7C451-30DMB	32.3 DIP	D32	512 x 9 Clocked FIFO
5962-93173 01MYX	CY7C451-30LMB	32 R LCC	L55	512 x 9 Clocked FIFO
5962-93173 02MXX	CY7C451-20DMB	32.3 DIP	D32	512 x 9 Clocked FIFO
5962-93173 02MYX	CY7C451-20LMB	32 R LCC	L55	512 x 9 Clocked FIFO
5962-93173 03MXX	CY7C451-14DMB	32.3 DIP	D32	512 x 9 Clocked FIFO
5962-93173 03MYX	CY7C451-14LMB	32 R LCC	L55	512 x 9 Clocked FIFO
5962-93225 01MXX	CY7C196-45DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 01MYX	CY7C196-45LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-93225 02MXX	CY7C196-35DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 02MYX	CY7C196-35LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-93225 03MXX	CY7C196-25DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 03MYX	CY7C196-25LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-93225 04MXX	CY7C196-20DMB	28.3 DIP	D22	64K x 4 SRAM w/OE
5962-93225 04MYX	CY7C196-20LMB	28 R LCC	L54	64K x 4 SRAM w/OE
5962-94510 01MXX	CY7C335-50WMB	28.3 DIP	W22	Synchronous UV EPLD
5962-94510 01MYX	CY7C335-50HMB	28 S JCQ	H64	Synchronous UV EPLD
5962-94510 01MZX	CY7C335-50QMB	28 S LCC	Q64	Synchronous UV EPLD
5962-94510 02MXX	CY7C335-66WMB	28.3 DIP	W22	Synchronous UV EPLD
5962-94510 02MYX	CY7C335-66HMB	28 S JCQ	H64	Synchronous UV EPLD
5962-94510 02MZX	CY7C335-66QMB	28 S LCC	Q64	Synchronous UV EPLD
5962-94510 03MXX	CY7C335-83WMB	28.3 DIP	W22	Synchronous UV EPLD
5962-94510 03MYX	CY7C335-83HMB	28 S JCQ	H64	Synchronous UV EPLD
5962-94510 03MZX	CY7C335-83QMB	28 S LCC	Q64	Synchronous UV EPLD
5962-94522 01MXX	CY7B991-7LMB	32 R LCC	L55	Prog Skew Clock Buffer

Notes:

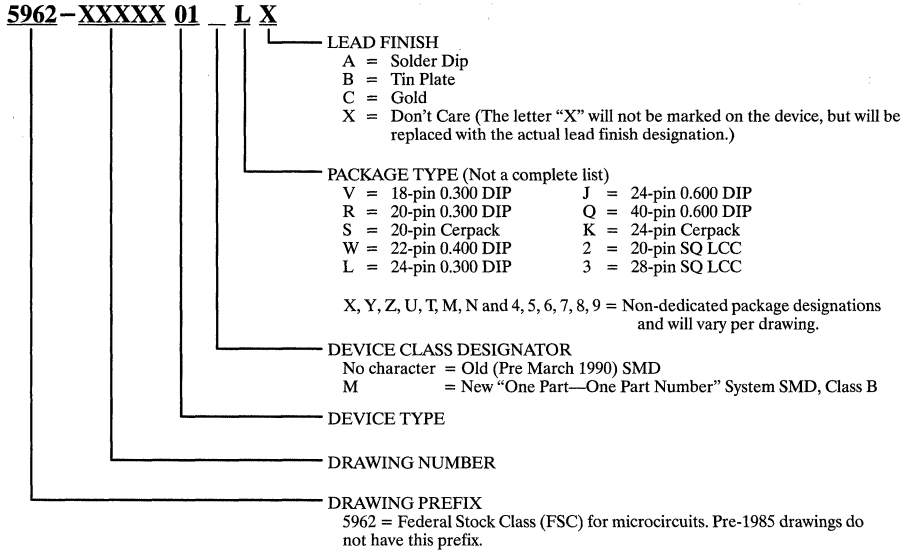
1. Devices listed have been approved by DESC for the SMD indicated as of the date of publication. Contact your local Cypress representative, or the Cypress SMD Hotline at 408/943-2716, for the latest update.
2. Use the SMD part number as the ordering code.
3. Package: 24.3 DIP = 24-pin 0.300″ DIP;
   24.6 DIP = 24-pin 0.600″ DIP;
   28 R LCC = 28 terminal rectangular LCC,
   S = Square LCC, TLCC = Thin LCC
   24 CP = 24-pin ceramic flatpack (Configuration 1);
   FP = brazed flatpack;
   PGA = Pin Grid Array.

SMD Hotline: 408/943-2716

JAN Qualifications to MIL-I-38535

JAN Number	Cypress[2] Part Number	Package[3]		Product Description	Qualification Status
		Description	Type		
JM 38510/50701B3A	PALC22V10B–30QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50703B3A	PALC22V10B–20QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50704B3A	PALC22V10B–15QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50801BLA	PALC22V10B–30DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50801BKA	PALC22V10B–30KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50801B3A	PALC22V10B–30LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50802BKA	PALC22V10B–25KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50803BKA	PALC22V10B–20KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50803B3A	PALC22V10B–20LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50804BLA	PALC22V10B–15DMB	24.3 DIP	D14	CMOS PLD	Qualified

SMD Ordering Information



Cypress Military Marking Information

Manufacturer's identification:

Cypress Logo, CYPRESS, CYP, and CY are trademarks of Cypress Semiconductor Corporation.

Manufacturer's designating symbol or CAGE CODE:

Designating symbol = CETK or ETK

CAGE CODE/FSCM Number = 65786

Country of origin:

USA = United States of America

THA = Thailand

In general, the codes for all products (except modules) follow the format below.

PAL & PLD

PREFIX	DEVICE	SUFFIX	FAMILY
PAL C	16R8	−20 DMB	PAL 20
PAL C	22V10	−15 WMB	PAL 24 VARIABLE PRODUCT TERMS
PLD C	20G10	−20 WMB	GENERIC PLD 24
CY	7C330	−50 DMB	PLD SYNCHRONOUS STATE MACHINE
CY	10E302	−4 DMB	10K ECL PLD

RAM, PROM, FIFO, µP, ECL

PREFIX	DEVICE	SUFFIX	FAMILY
CY	7C128A	−35 D M B	CMOS SRAM
CY	7B185	−10 D M B	BiCMOS SRAM
CY	7C245A	−18 W M B	PROM
CY	7C404	−10 D M B	FIFO
CY	7C901	−27 D M B	µP
CY	10E422L	−5 D M B	10K ECL SRAM

B = BiCMOS
C = CMOS

PROCESSING
B = HI REL MIL STD 883D FOR MILITARY PRODUCT
= LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT

TEMPERATURE RANGE
M = MILITARY (−55°C TO +125°C)

PACKAGE
D = CERDIP
F = FLATPAK
G = PIN GRID ARRAY (PGA)
H = WINDOWED LEADED CHIP CARRIER
K = CERPAK (GLASS-SEALED FLAT PACKAGE)
L = LEADLESS CHIP CARRIER
Q = WINDOWED LEADLESS CHIP CARRIER
R = WINDOWED PGA
T = WINDOWED CERPAK
U = CERAMIC QUAD FLATPACK
W = WINDOWED CERDIP
X = DICE (WAFFLE PACK)
Y = CERAMIC LEADED CHIP CARRIER

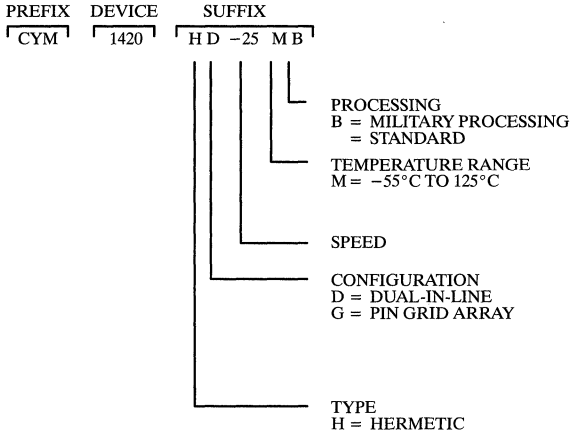
SPEED (ns or MHz)

L = LOW-POWER OPTION
A, B, C = REVISION LEVEL

e.g., CY7C128A−35DMB, PALC16R8−20DMB

Cypress FSCM #65786

The codes for module products follow the the format below.



Cypress FSCM #65786

Section Contents

Quality and Reliability **Page Number**

Quality, Reliability, and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability is built into every product design, starting from the initial design conception.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Assurance Documents

Cypress Semiconductor uses MIL-STD-883 and MIL-I-38535 as baseline documents to determine our Test Methods, Procedures and General Specifications for Semiconductors.

Customers using our commercial and industrial grade product receive the benefit of a military patterned process flow at no additional charge.

Product Testing Categories

Five different testing categories are offered by Cypress:

1. Commercial operating range product: 0°C to +70°C.
2. Industrial operating range product: − 40°C to +85°C.
3. Military Grade product processed to MIL-STD-883; Military operating range: − 55°C to +125°C.
4. QML (Qualified Manufacturers Line), JAN (Joint Army Navy), and SMD (Standardized Military Drawing) approved product: Military operating range: − 55°C to +125°C, electrically tested per the applicable Military Drawing.

Categories 1, 2, and 3 are available on all products offered by Cypress Semiconductor. Category 4 is offered on a more limited basis, dependent upon the specific part type in question.

Commercial Product Assurance Categories

Commercial grade devices are offered with two different classes of product assurance. Every device shipped, as a minimum, meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be reasonably accomplished.

Level 2: For enhanced reliability applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and a burn-in of 12 hours at 150°C.

Tables 1 and *2* list the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet requirements of these programs.

Military Product Assurance Categories

Cypress's Military Grade components and SMD products are processed per MIL-STD-883 using methods 5004 and 5005 to define our screening and quality conformance procedures. The processing performed by Cypress results in a product that meets the class B screening requirements as called out by these methods. Every device shipped, as a minimum, meets these requirements.

QML, JAN, SMD, and Military Grade devices supplied by Cypress are processed for applications where maintenance is difficult or expensive and reliability is paramount. *Tables 3* through *7* list the screening and quality conformance testing that is performed in order to meet the processing requirements required by MIL-STD-883 and MIL-I-38535.

Table 1. Cypress Commercial and Industrial Product Screening Flows—Components

Screen	MIL-STD-883 Method	Product Temperature Ranges			
		Commercial 0°C to +70°C; Industrial −40°C to +85°C			
		Level 1		Level 2	
		Plastic	Hermetic	Plastic	Hermetic
Visual/Mechanical					
• Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%
• Hermeticity					
– Fine Leak	1014, Cond A or B (sample)	Does Not Apply	LTPD = 5	Does Not Apply	LTPD = 5
– Gross Leak	1014, Cond C	Does Not Apply	100%	Does Not Apply	100%
Burn-in					
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Burn-in	Per Cypress Specification	Does Not Apply	Does Not Apply	100%[1]	100%[1]
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Percent Defective Allowable (PDA)		Does Not Apply	Does Not Apply	5% (max)[2]	5% (max)[2]
Final Electrical	Per Device Specification				
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supplies Extremes	Not Performed	Not Performed	100%[1]	100%[1]
	2. At Hot Temperature and Power Supply Extremes	100%	100%	100%	100%
Cypress Quality Lot Acceptance					
• External Visual	2009	Note 3	Note 3	Note 3	Note 3
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3	Note 3	Note 3

Table 2. Cypress Commercial and Industrial Product Screening Flows—Modules

Screen	MIL-STD-883 Method	Product Temperature Ranges	
		Commercial 0°C to +70°C; Industrial −40°C to +85°C	
		Level 1	Level 2
Burn-in			
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Burn-in	1015	Does Not Apply	100%
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Percent Defective Allowable (PDA)		Does Not Apply	15%
Final Electrical	Per Device Specification		
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supply Extremes	Not Performed	100%
	2. At Hot Temperature and Power Supply Extremes	100%	100%
Cypress Quality Lot Acceptance			
• External Visual	2009	Per Cypress Module Specification	Per Cypress Module Specification
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3

Notes:
1. Burn-in is performed as a standard for 12 hours at 150°C.
2. Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
3. Lot acceptance testing is performed on every lot. AOQL (the Average Outgoing Quality Level) for 1994 was <100 PPM.

Table 3. Cypress QML/JAN/SMD/Military Grade Product Screening Flows for Class B

Screen	Screening Per Method 5004 of MIL-STD-883	Product Temperature Ranges −55°C to +125°C	
		QML/JAN/SMD/Military Grade Product[4]	Military Grade Module
Visual/Mechanical			
• Internal Visual	Method 2010, Cond B	100%	N/A
• Temperature Cycling	Method 1010, Cond C, (10 cycles)	100%	Optional
• Constant Acceleration	Method 2001, Cond E (Min.), Y1 Orientation Only	100%	N/A
• Hermeticity:			
— Fine Leak	Method 1014, Cond A or B	100%	N/A
— Gross Leak	Method 1014, Cond C	100%	N/A
Burn-in			
• Pre-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%
• Burn-in Test	Method 1015, Cond D, 160 Hrs at 125°C Min. or 80 Hrs at 150°C	100%	100% (48 Hours at 125°C)
• Post-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA, for All Lots	5%	10%
Final Electrical Tests			
• Static Tests	Method 5005 Subgroups 1, 2, and 3	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Functional Tests	Method 5005 Subgroups 7, 8A, and 8B	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Switching	Method 5005 Subgroups 9, 10, and 11	100% Test to Applicable Device Specification	100% Test to Applicable Specification
Quality Conformance Tests			
• Group A[5]	Method 5005, see Tables 4 − 7 for details	Sample	Sample
• Group B		Sample	Sample
• Group C[6]		Sample	Sample
• Group D[6]		Sample	Sample
External Visual	Method 2009	100%	100%

Notes:

4. QML product is allowed a reduction in screening requirements with DESC approval per MIL-I-38535.
5. Group A subgroups tested for QML/SMD/Military Grade products are 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.
6. Group C and D end-point electrical tests for QML/SMD/Military Grade products are performed to Group A subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.

Table 4. Group A Test Descriptions

Sub-group	Description	Sample Size/Accept No.	
		Components	Modules[7]
1	Static Tests at 25°C	116/0	116/0
2	Static Tests at Maximum Rated Operating Temperature	116/0	116/0
3	Static Tests at Minimum Rated Operating Temperature	116/0	116/0
4	Dynamic Tests at 25°C	116/0	116/0
5	Dynamic Tests at Maximum Rated Operating Temperature	116/0	116/0
6	Dynamic Tests at Minimum Rated Operating Temperature	116/0	116/0
7	Functional Tests at 25°C	116/0	116/0
8A	Functional Tests at Maximum Temperature	116/0	116/0
8B	Functional Tests at Minimum Temperature	116/0	116/0
9	Switching Tests at 25°C	116/0	116/0
10	Switching Tests at Maximum Temperature	116/0	116/0
11	Switching Tests at Minimum Temperature	116/0	116/0

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military Grade component products have a Group A sample test performed on each inspection lot per MIL-I-38535/MIL-STD-883 and the applicable device specification.

Table 5. Group B Quality Tests

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
2	Resistance to Solvents, Method 2015	3/0	3/0
3	Solderability, Method 2003[8]	22/0	10
5	Bond Strength, Method 2011[9]	15/0	NA

Notes:
7. Military Grade Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules.
8. Sample size is based upon leads taken from a minimum of 3 devices.
9. Sample size is based upon leads taken from a minimum of 4 devices.

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Table 6. Group C Quality Tests

Sub-group	Description	LTPD	
		Components	Modules[7]
1	Steady State Life Test, End-Point Electricals, Method 1005, Cond D	45/0	15/0

Group C tests for all Military Grade products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-I-38535/MIL-STD-883 from each four calendar quarters production of devices, which is based upon the die fabrication date code.

End-point electrical tests and parameters are performed per the applicable device specification.

Table 7. Group D Quality Tests (Package Related)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
1	Physical Dimensions, Method 2016	15/0	15/0
2	Lead Integrity, Seal: Fine and Gross Leak, Method 2004 and 1014	45/0[8]	15/0
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine and Gross Leak, Visual Examination, End-Point, Electricals, Methods 1011, 1010, 1004 and 1014	15/0	15/0
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine and Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 and 1014	15/0	15/0

Table 7. Group D Quality Tests (Package Related) (continued)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[10]
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15/0	15/0
6	Internal Water-Vapor Content; 5000 ppm maximum @ 100°C. Method 1018	3(0) or 5(1)	N/A
7	Adhesion of Lead Finish,[11] Method 2025	15/0	15/0
8	Lid Torque, Method 2024[12]	5(0)	N/A

Notes:
10. Does not apply to leadless chip carriers.
11. Based on the number of leads.
12. Applies only to packages with glass seals.

Group D tests for all Military Grade products are performed per MIL-I-38535/MIL-STD-883 on each package type from each six months of production, based on the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per the applicable device specification.

Product Screening Summary

Commercial and Industrial Product

- Screened to either Level 1 or Level 2 product assurance flows
- Hermetic and molded packages available
- Incoming mechanical and electrical performance guaranteed:
  - 0.02% AQL Electrical Sample test performed on every lot prior to shipment
  - 0.01% AQL External Visual Sample inspection
- Electrically tested to Cypress data sheet

Ordering Information

Product Assurance Grade: Level 1

- Order Standard Cypress part number
- Parts marked the same as ordered part number
  Ex: CY7C122-15PC, PALC22V10-25PI

Product Assurance Grade: Level 2

- Burn-in performed on all devices to Cypress detailed circuit specification
- Add 'B' Suffix to Cypress standard part number when ordering to designate burn-in option
- Parts marked the same as ordered part number
  Ex: CY7C122-15PCB, PALC22V10-25PIB

Military Grade Product

- SMD and Military Grade components are manufactured in compliance with paragraph 1.2.1 of MIL-STD-883. Compliant products are identified by an 'MB' suffix on the part number (CY7C122-25DMB) and the letter "C"
- QML/JAN devices are manufactured in accordance with MIL-I-38535. Compliant products are identified with the letter "Q."
- Military grade devices electrically tested to:
  - Cypress data sheet specifications

    OR
  - SMD devices electrically tested to military drawing specifications

    OR
  - JAN devices electrically tested to slash sheet specifications
- All devices supplied in hermetic packages
- Quality conformance inspection: Method 5005, Groups A, B, C, and D performed as part of the standard process flow
- Burn-in performed on all devices
  - Cypress detailed circuit specification for non-Jan devices

    OR
  - Slash sheet requirements for JAN products
- Static functional and switching tests performed at 25°C as well as temperature and power supply extremes on 100% of the product in every lot
- JAN product manufactured in a DESC certified facility

Ordering Information

JAN/QML Product:

- Order per military document
- Marked per military document
  Ex: JM38510/28901BVA

SMD Product:

- Order per military document
- Marked per military document
  Ex: 5962-8867001LA

Military Grade Product:

- Order per Cypress standard military part number
- Marked the same as ordered part number
  Ex: CY7C122-25DMB

Military Modules

- Military Temperature Grade Modules are designated with an 'M' suffix only. These modules are screened to standard combined flows and tested at both military temperature extremes.
- MIL-STD-883 Equivalent Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules. All MIL-STD-883 equivalent modules are assembled with fully compliant MIL-STD-883 components.

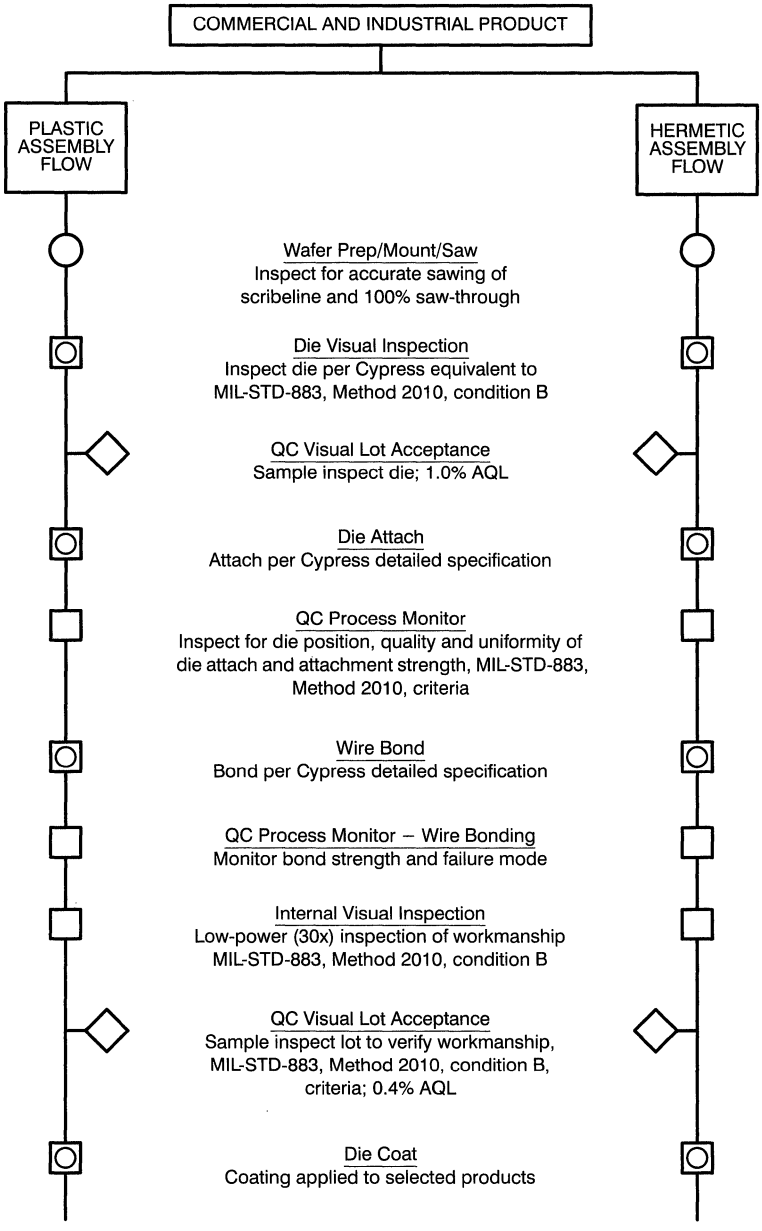
Product Quality Assurance Flow—Components

Area	PROCESS	Process Details
QC	INCOMING MATERIALS INSPECTION	All incoming materials are inspected to documented procedures covering the handling, inspection, storage, and release of raw materials used in the manufacture of Cypress products. Materials inspected are: wafers, masks, leadframes, ceramic packages and/or piece parts, molding compounds, gases, chemicals, etc.
FAB	DIFFUSION/ION IMPLANTATION	Sheet resistance, implant dose, species and CV characteristics are measured for all critical implants on every product run. Test wafers may be used to collect this data instead of actual production wafers. If this is done, they are processed with the standard product prior to collecting specific data. This insures accurate correlation between the actual product and the wafers used to monitor implantation.
FAB	OXIDATION	Sample wafers and sample sites are inspected on each run from various positions of the furnace load to inspect for oxide thickness. Automated equipment is used to monitor pinhole counts for various oxidations in the process. In addition, an appearance inspection is performed by the opeartor to further monitor the oxidation process.
FAB	PHOTOLITHOGRAPHY /ETCHING	Appearance of resist is checked by the operator after the spin operation. Also, after the film is developed, both dimensions and appearance are checked by the operator on a sample of wafers and locations upon each wafer. Final CDs and alignment are also sample inspected on several wafers and sites on each wafer on every product run.
FAB	METALIZATION	Film thickness is monitored on every run. Step coverage cross-sections are performed on a periodic basis to insure coverage.
FAB	PASSIVATION	An outgoing visual inspection is performed on 100% of the wafers in a lot to inspect for scratches, particles, bubbles, etc. Film thickness is verified on a sample of wafers and locations within each given wafer on each run. Pinholes are monitored on a sample basis weekly.
FAB	QC VISUAL OF WAFERS	
FAB	E-TEST	Electrical test is performed for final process electrical characteristics on every wafer.
FAB	QC MONITOR OF E-TEST DATA	Weekly review of all data trends; running averages, minimums, maximums, etc. are reviewed with the process control manager.
TEST	WAFER PROBE/SORT	Verify functionality, electrical characteristics, stress test devices.
TEST	QC CHECK PROBING AND ELECTRICAL TEST RESULTS	Pass/fail lot based on yield and correct probe placement.

TO ASSEMBLY AND TEST

(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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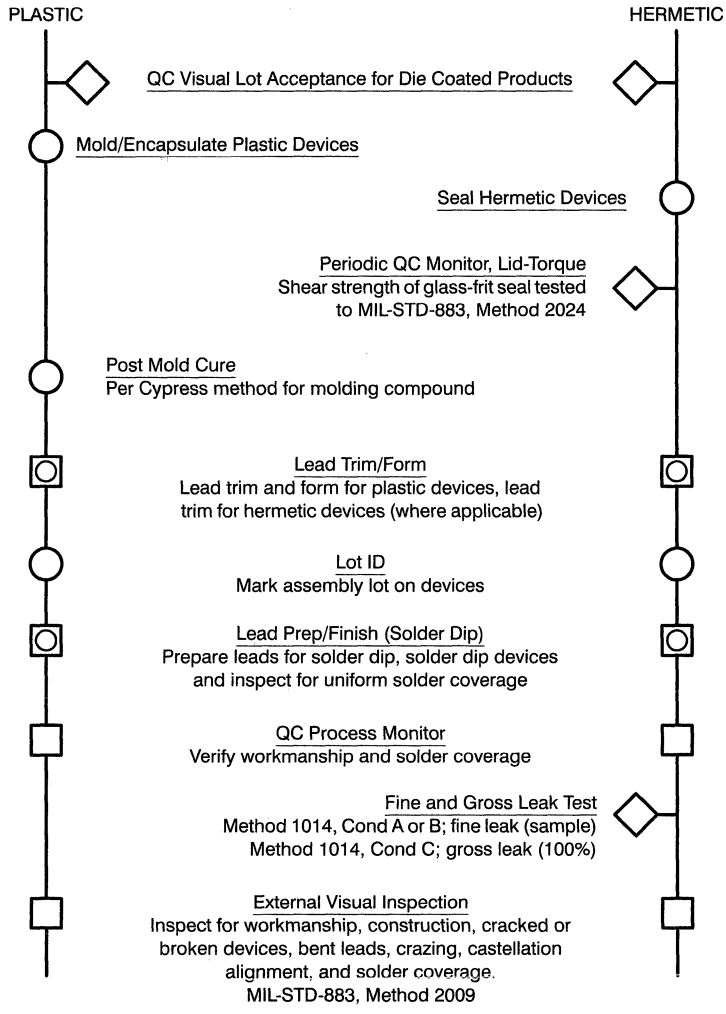
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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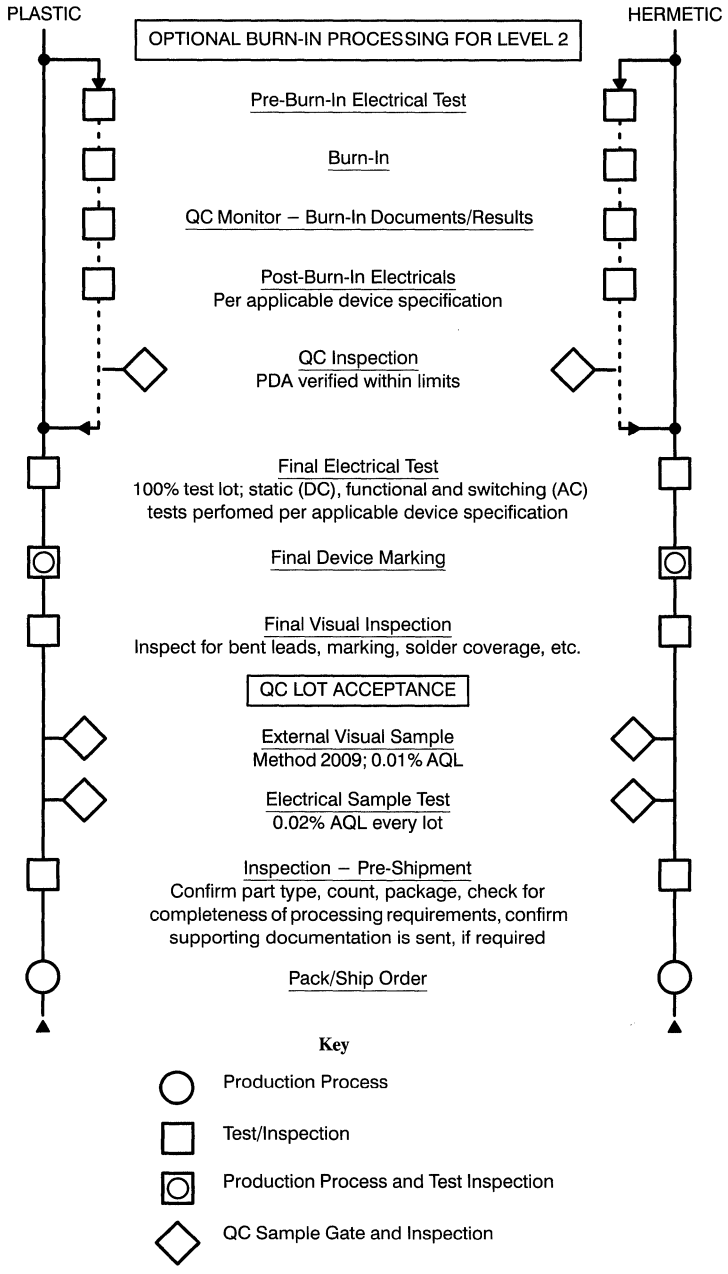
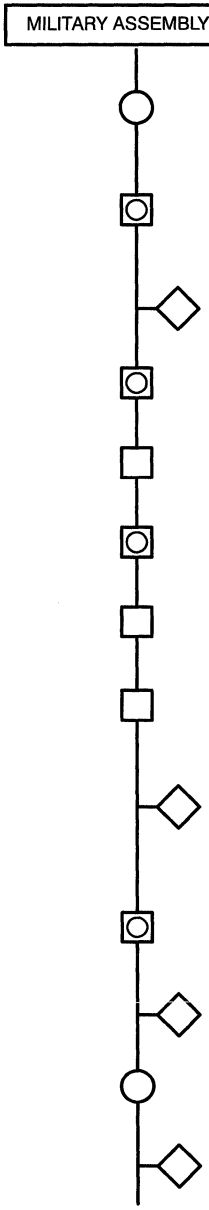
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

Product Quality Assurance Flow—Components
Military Components



Wafer Prep/Mount/Saw
Inspect for accurate sawing of scribeline and 100% saw-through

Die Visual Inspection
Inspect die per MIL-STD-883, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect die; 1.0% AQL

Die Attach
Attach per Cypress detailed specification

Die Adherence Monitor
MIL-STD-883, Method 2019 or Method 2027

Wire Bond
Bond per Cypress detailed specification

Bond Pull Monitor
MIL-STD-883, Method 2011

Internal Visual Inspection
Low-power and high-power inspection per
MIL-STD-883, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect lot per MIL-STD-883,
Method 2010, condition B, 0.4% AQL

Die Coat
Coating applied to selected products

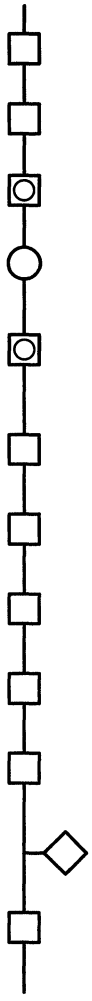
QC Visual Lot Acceptance for Die Coated Products

Seal

Periodic QC Monitor, Lid-Torque
Shear strength of glass

(continued)

Product Quality Assurance Flow—Components (continued)
Military Components



Temperature Cycle
Method 1010, Cond C, 10 cycles

Constant Acceleration
Method 2001, Cond E, Y1 Orientation

Lead Trim
Lead trim when applicable

Lot ID
Mark assembly lot on devices

Lead Finish
Solder dip or matte tin plate applicable devices and inspect

QC Process Monitor
Verify workmanship and lead finish coverage

External Visual Inspection
Method 2009

Pre-Burn-In Electrical Test
Method 5004, per applicable device specification

Burn-In
Method 1015, condition D

Post-Burn-In Electricals
Method 5004, per applicable device specification

PDA Calculation
Method 5004, 5%

Final Electrical Test
Method 5004; Static, functional and switching tests per applicable device specification

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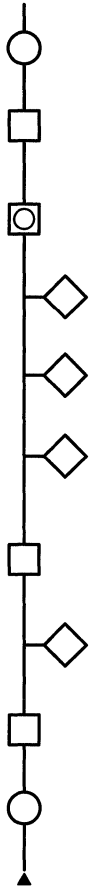
Product Quality Assurance Flow—Components (continued)
Military Components



Lead Finish – Solder Dip
Solder dip applicable devices

Fine and Gross Leak Test
Method 1014, condition A or B, fine leak; condition C, gross leak

Final Device Marking
MIL-STD-883 or applicable device specification

Group B
Method 5005

Group A
Method 5005, per applicable device specification

Group C and D
Method 5005, in accordance with
1.2.1 of MIL-STD-883; JAN devices
in accordance with MIL-I-38535

External Visual
Method 2009, 100% inspection

External Visual Sample
Method 2009, 0.01% AQL

Plant Clearance

Pack/Ship Order

Key

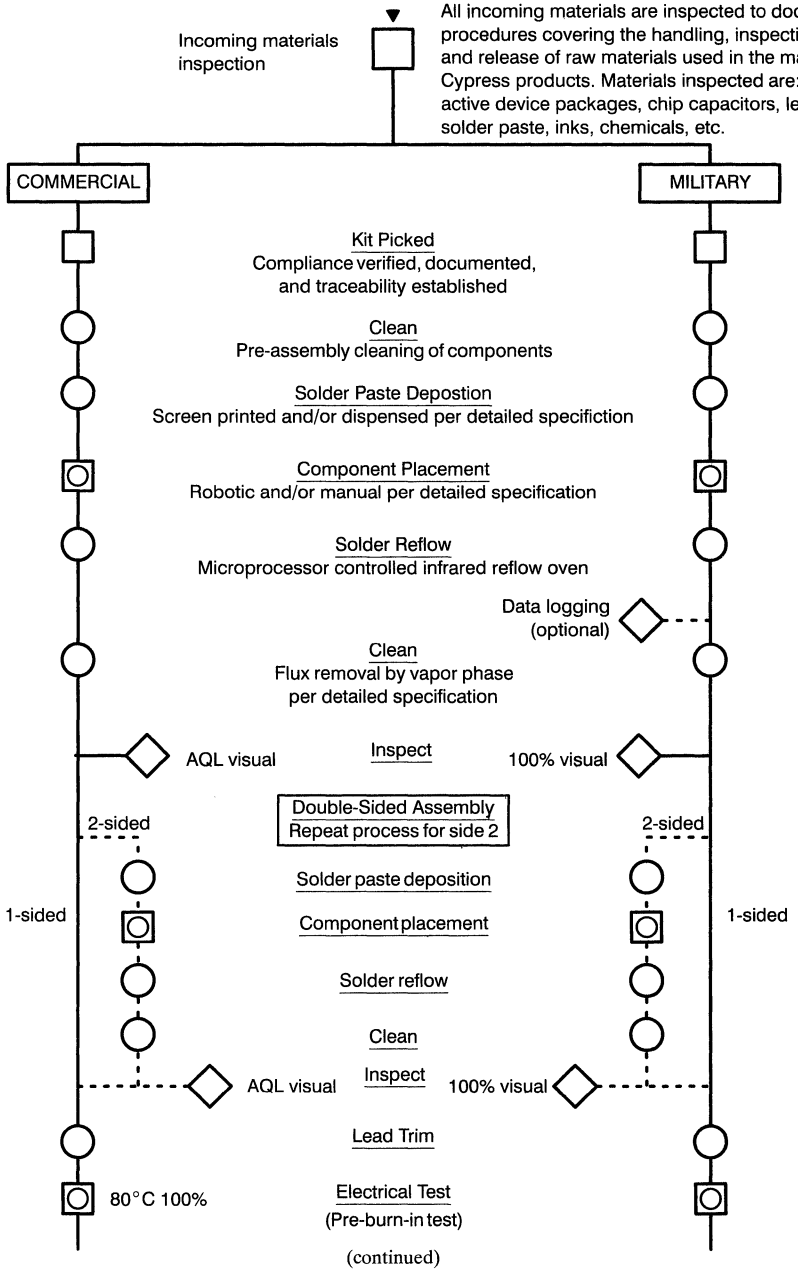
Production Process

Test/Inspection

Production Process and Test Inspection

QC Sample Gate and Inspection

Product Quality Assurance Flow—Modules



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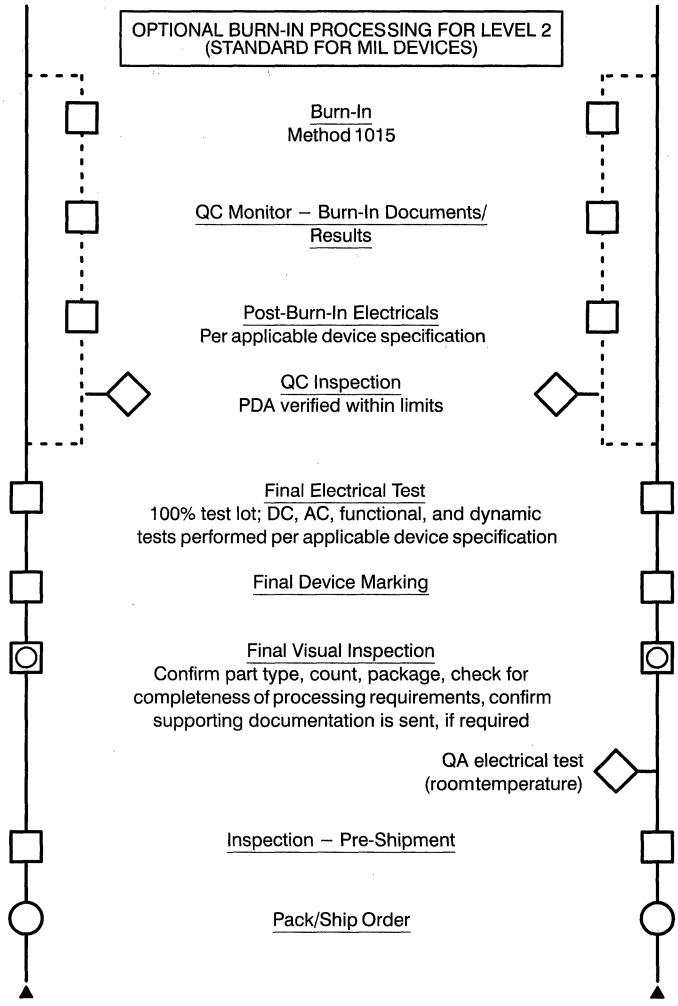
Product Quality Assurance Flow—Modules (continued)



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample gate and inspection

Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008, which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for Cypress customers. The Reliability Monitor Program monitors our most advanced technologies and packages. Every technology produced at a given fabrication site (Tech. – Fab.) and all assembly houses are monitored at least quarterly. If failures occur, detailed failure analyses are performed and corrective actions are implemented. A summary of the Reliability Monitor Program test and sampling plan is shown below.

Quarterly Reliability Monitor Test Matrix

Stress	Devices Tested	# per Quarter
HTOL	Tech. – Fab.	6
	All High Volume	2
HAST	Tech. – Fab.	6
	All High Volume	2
PCT	Plastic Packages	4
TC	Tech. – Fab.	6
	Plastic Packages	3
	Ceramic Packages	5
	All High Volume	2
DRET	FAMOS – San Jose and Texas	2
HTSSL	All Technologies	4
TEV	All Technologies	4
Total		46

Reliability Monitor Test Conditions

Test	Abbrev.	Temp. (°C)	R.H. (%)	Bias	Sample Size	LTPD	Read Points (hrs.)
High-Temperature Operating Life	HTOL	+150	N/A	5.75V Dynamic	116	2	48, 168, 500, 1000
High-Temperature Steady-State Life	HTSSL	+150	N/A	5.75V Static	116	2	48, 168, 500, 1000
Data Retention for Plastic Packages	DRET	+165	N/A	N/A	76	3	168, 1000
Data Retention for Ceramic Packages	DRET2	+250	N/A	N/A	76	3	168, 1000
Pressure Cooker	PCT	+121	100	N/A	76	3	96, 168
Highly Accelerated Stress Test	HAST	+140	85	5.5V Static	76	3	128
Temperature Cycling 1	TC	−40 to +125°C	N/A	N/A	76	3	500, 1000 Cycles
Temperature Cycling 2	TC2	−65 to +150°C	N/A	N/A	45	5	300, 1000 Cycles
Temperature Extreme Verification	TEV	Commercial Hot & Cold 0 to +70°C	N/A	N/A	116	2	N/A

Tape and Reel Specifications

Description

Surface-mounted devices are packaged in embossed tape and wound onto reels for shipment in compliance with Electronics Industries Association Standard EIA–481 Rev. A.

Specifications

Cover Tape

- The cover tape may not extend past the edge of the carrier tapes
- The cover tape shall not cover any part of any sprocket hole.
- The seal of the cover tape to the carrier tape is uniform, with the seal extending over 100% of the length of each pocket, on each side.
- The force to peel back the cover tape from the carrier tape shall be: 20 gms minimal, 70 gms nominal, 100 gms maximal, at a pull-back speed of 300 ± 10 mm/min.

Loading the Reel

Empty pockets between the first and last filled pockets on the tape are permitted within the following requirements:

- No two consecutive pockets may be left empty
- No more than a total of ten (10) empty pockets may be on a reel

The surface-mount devices are placed in the carrier tape with the leads down, as shown in *Figure 1*.

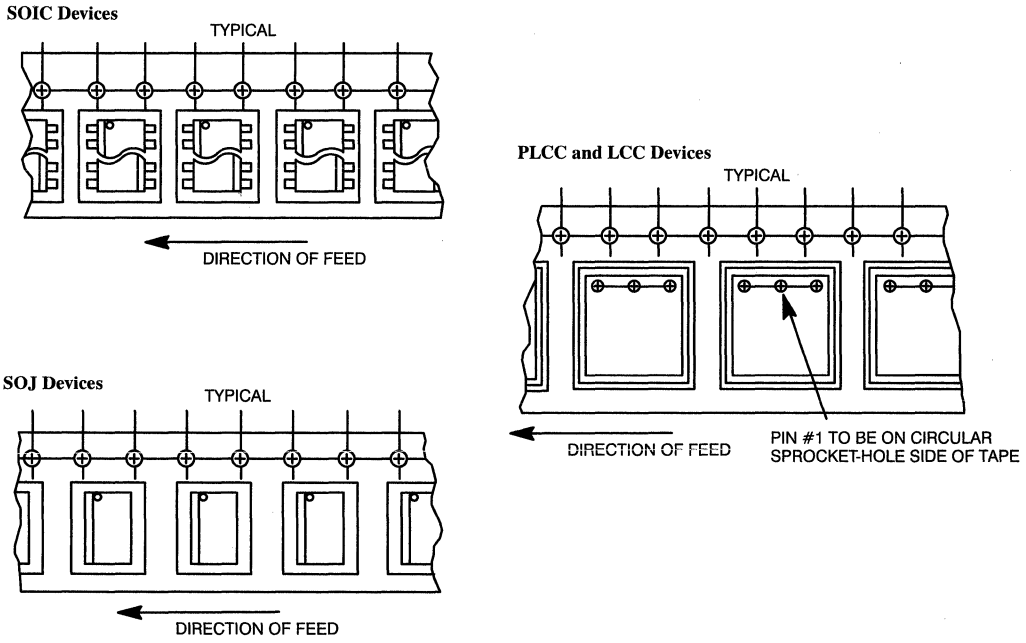


Figure 1. Part Orientation in Carrier Tape

Leaders and Trailers

The carrier tape and the cover tape may not be spliced. Both tapes must be one single uninterrupted piece from end to end.

Both ends of the tape must have empty pockets meeting the following minimum requirements:

- Trailer end (inside hub of reel) is 300 mm minimum
- Leader end (outside of reel) is 500 mm min., 560 mm max.
- Unfilled leader and trailer pockets are sealed
- Leaders and trailers are taped to tape and hub respectively using masking tape

Packaging

- Full reels contain a standard number of units (refer to *Table 1*)
- Reels may contain up to 3 inspection lots.
- Each reel is packed in an anti-static bag and then in its own individual box.
- Labels are placed on each reel as shown in *Figure 2*. The information on the label consists of a minimum of the following information, which complies with EIA 556, "Shipping and Receiving Transaction Bar Code Label Standard":
  - Barcoded Information:
    Customer PO number
    Quantity
    Date code
  - Human Readable Only:
    Package count (number of reels per order)
    Description
    "Cypress–San Jose"
    Cypress p/n
    Cypress CS number (if applicable)
    Customer p/n
- Each box will contain an identical label plus an ESD warning label.

Ordering Information

CY7Cxxx–yyzzz

xxx = part type

yy = speed

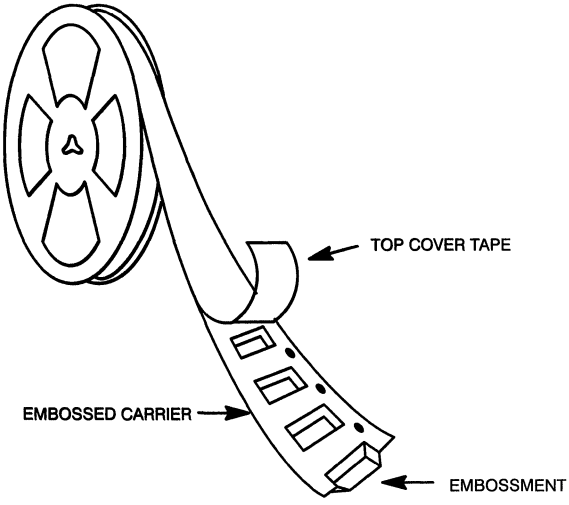
zzz = package, temperature, and options

SCT = soic, commercial temperature range
SIT = soic, inductrial temperature range
SCR = soic, commercial temperature plus burn-in
SIR = soic, industrial temperature plus burn-in
VCT = soj, commercial temperature range
VIT = soj, industrial temperature range
VCR = soj, commercial temperature plus burn-in
VIR = soj, industrial temperature plus burn-in
JCT = plcc, commercial temperature range
JIT = plcc, industrial temperature range
JCR = plcc, commercial temperature range plus burn-in
JIR = plcc, industrial temperature range plus burn-in

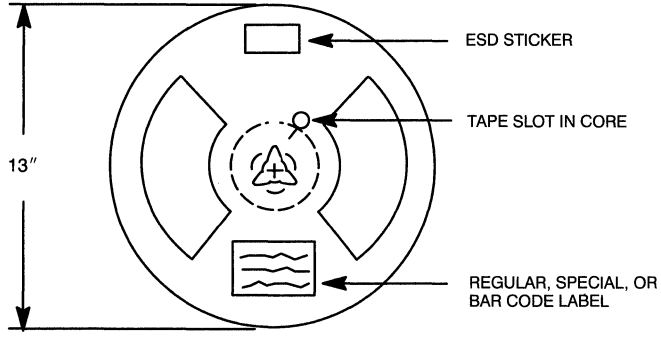
Notes:
1. The T or R suffix will not be marked on the device. Units will be marked the same as parts in a tube.
2. Order releases must be in full-reel multiples as listed in *Table 1*.

Table 1. Parts Per Reel and Tape Specifications

Package Type	Terminals	Carrier Width (mm)	Part Pitch (mm)	Parts Per Full Reel
PLCC	20	16	12	750
	28	24	16	500
	32R	24	16	500
	44	32	24	400
	52	32	24	400
	68	44	32	250
	84	44	32	250
SOIC	20	24	12	1,000
	24	24	12	1,000
	28	24	12	1,000
SOJ	20	24	3	1,000
	24	24	3	1,000
	28	24	3	1,000
	32 (400 mil)	32	3	1,000
TSOP	32	32	3	1,750
SSOP	20 (150 mil)	16	8	2,000
	24 (150 mil)	16	8	2,000
	48 (300 mil)	32	16	1,000
	56 (300 mil)	32	16	1,000
TSSOP	48	24	12	2,000
	56	24	12	2,000



Tape and Reel Shipping Medium



Label Placement

Figure 2. Shipping Medium and Label Placement

Section Contents

Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chemical reactions. The slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device (see *Figure 1*).

Typical activation energies for commonly observed failure mechanisms in CMOS devices are shown in *Table 1*.

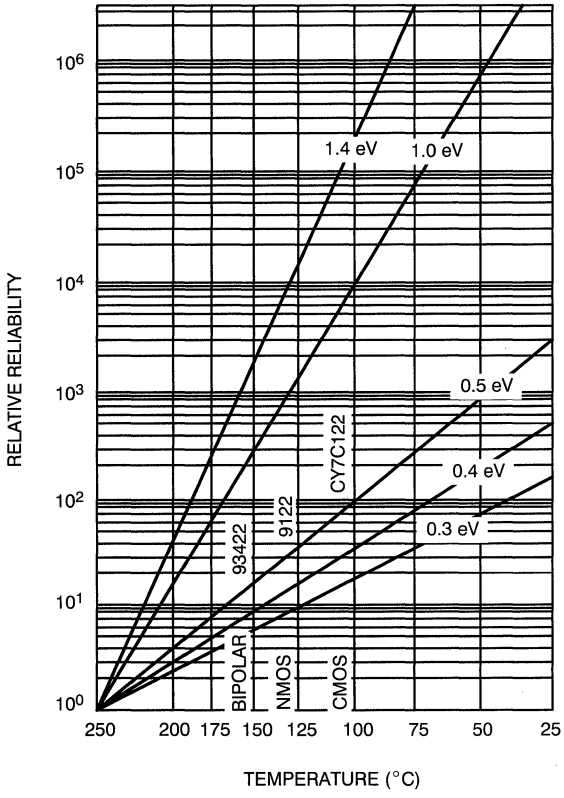


Figure 1. Arrhenius plot, which assumes a failure rate proportional to EXP ($-E_A/kT$) where E_A is the activation energy for the particular failure mechanism

Table 1. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (Eq)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5–1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally activated reliability failures, Cypress Semiconductor has optimized both their low-power-generating CMOS device fabrication process and their high-heat-dissipation packaging capabilities. *Table 2* demonstrates this optimized thermal performance by comparing bipolar, NMOS, and Cypress high-speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

Table 2. Thermal Performance of Fast 1K SRAMs in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I_{CC} (mA)	150	110	60
V_{CC} (V)	5.0	5.0	5.0
P_{MAX} (mW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Datasheet P_{MAX}[1]	160	136	91

During its normal operation, the Cypress 7C122 device experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0-eV activation energy failure mechanism, this translates into an improvement in excess of two orders of magnitude (100x) over the bipolar 93422 device, and more than one order of magnitude (30x) over the NMOS 9122 device.

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Thermal Resistance (θ_{JA}, θ_{JC})

Thermal resistance is a measure of the ability of a package to transfer the heat generated by the device inside it to the ambient.

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation is room temperature to 70°C.

T_J = Junction temperature of the IC chip.

T_C = Temperature of the case (package).

P = Power at which the device operates.

θ_{JC} = Junction-to-case thermal resistance. This is mainly a function of the thermal properties of the materials constituting the package.

θ_{JA} = Junction-to-ambient thermal resistance. The junction-to-ambient environment is a still-air environment.

θ_{CA} = Case-to-ambient thermal resistance. This is mainly dependent on the surface area available for convection and radiation and the ambient conditions among other factors. This can be controlled at the user end by using heat sinks providing greater surface area and better conduction path or by air or liquid cooling.

Thermal Resistance: Finite Element Model

θ_{JC} and θ_{JA} values given in the following figures and listed in the following tables have been obtained by simulation using the Finite element software ANSYS[2]. SDRC-IDEAS Pre and Post processor software[3] was used to create the finite element model of the packages and the ANSYS input data required for analysis.

SEMI Standard (Semiconductor Equipment and Materials International) method SEMI G30-88[4] states "heat sink" mounting technique to be the "reference" method for θ_{JC} estimation of ceramic packages. Accordingly, θ_{JC} of packages has been obtained by applying the boundary conditions that correspond to the heat sink mounted on the packages in the simulation.

For θ_{JA} evaluation, SEMI standard specification SEMI G38-87 suggests using a package-mounting arrangement that approximates the application environment. So, in evaluating the θ_{JA}, package on-board configuration is assumed.

Notes:
1. $T_{ambient}$ = 70°C
2. *ANSYS Finite Element Software User Guides*
3. *SDRC-IDEAS Pre and Post Processor User Guide*
4. *SEMI International Standards*, Vol. 4, Packaging Handbook, 1989.

Model Description

- One quarter of the package is mounted on a FR-4 PC board.
- Leads have been modeled as a continuous metallic plane, and equivalent thermal properties have been used to account for the plastic (or the glass in the case of ceramic packages) that fills the space between the leads.
- 1W power dissipation over the entire chip is assumed.
- 70°C ambient condition is considered.

Comparison of Simulation Data with Measured Data

In the case of ceramic packages, it is not unusual to see significant differences in θ_{JC} values when a heat sink is used in the place of fluid bath.[5] However, SEMI G30-88 test method recommends the heat sink configuration for θ_{JC} evaluation.

θ_{JA} values from simulation compare within 12 percent of the measured values. θ_{JA} values obtained from simulation seem to be *conservative* with an accuracy of about +12 percent.

Measured values given in *Table 3* used the Temperature Sensitive Parameter method described in MIL STD 883C, method 1012.1. The junction-to-ambient measurement was made in a still-air environment where the device was inserted into a low-cost standard-device socket and mounted on a standard 0.062" G10 PC board.

Table 3. 24-Lead Ceramic and Plastic DIPs

Package	Cavity/PAD Size (mils)	θ_{JA} (°C/W)		
		Measured	Simulation	% Diff.
24LCDIP[6]	170 x 270	64	67	5
24LPDIP[7]	160 x 210	72	82	12

Thermal Resistance of Packages with Forced Convection Air Flow

One of the methods adopted to cool the packages on PC boards at the system level is to used forced air (fans) specified in linear feet per minute or LFM. This helps reduce the device operating temperature by lowering the case to ambient thermal resistance. Available surface area of the package and the orientation of the package with respect to the air flow affect the reduction of thermal resistance that can be achieved. A general rule of thumb is:

- For plastic packages:
  - 200 LFM air flow can reduce θ_{JA} by 20 to 25%
  - 500 LFM air flow can reduce θ_{JA} by 30 to 40%
- For ceramic packages:
  - 200 LFM air flow can reduce θ_{JA} by 25 to 30%
  - 500 LFM air flow can reduce θ_{JA} by 35 to 45%

If θ_{JA} for a package in still air (no air flow) is known, approximate values of thermal resistance at 200 LFM and 500 LFM can be estimated. For estimation, the factors given in *Table 4* can be used as a guideline.

Table 4. Factors for Estimating Thermal Resistance

Package Type	Air Flow Rate (LFM)	Multiplication Factor
Plastic	200	0.77
Plastic	500	0.66
Ceramic	200	0.72
Ceramic	500	0.60

Example:

θ_{JA} for a plastic package in still air is given to be 80°C/W. Using the multiplication factor from *Table 4*:

- θ_{JA} at 200 LFM is (80 x 0.77) = 61.6°C/W
- θ_{JA} at 500 LFM is (80 x 0.66) = 52.8°C/W

θ_{JA} for a ceramic package in still air is given to be 70°C/W. Using *Table 4*:

- θ_{JA} at 200 LFM is (70 x 0.72) = 50.4°C/W
- θ_{JA} at 500 LFM is (70x0.60) = 42.0°C/W

Presentation of Data

The following figures and tables present the data taken using the aforementioned procedures. The thermal resistance values of Cypress standard packages are graphically illustrated in *Figures 2* through *6*. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary=5000 mils^2, lower boundary = 100,000 mils^2) in their thermally optimized packaging environments. These graphs should be used in conjunction with *Table 10*, which lists the die sizes of Cypress devices.

Tables 5 through *9* give the thermal resistance values for other package types not included in the graphs. The letter in the header (*D, P, J*, etc.) of these tables refer to the package designators as detailed in the Package Diagrams section of this catalog. The numeric values given in the table (e.g., 20.3) refer to the lead count (20) and package width in inches (.3). If no decimal appears, the reader must refer to the package diagrams.

Packaging Materials

Cypress plastic packages incorporate

- High thermal conductivity copper lead frame
- Molding compound with high thermal conductivity
- Gold bond wires

Cypress cerDIP packages incorporate

- High conductivity alumina substrates
- Silver-filled glass as die attach material
- Alloy 42–lead frame
- Aluminum bond wires
- Silver-filled conductive epoxy as die attach material

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Notes:
5. "Thermal resistance measurements and finite calculations for ceramic hermetic packages." James N. Sweet et. al., *SEMI-Therm*, 1990.
6. 24LCDIP = 24-lead cerDIP
7. 24LPDIP = 24-lead plastic DIP

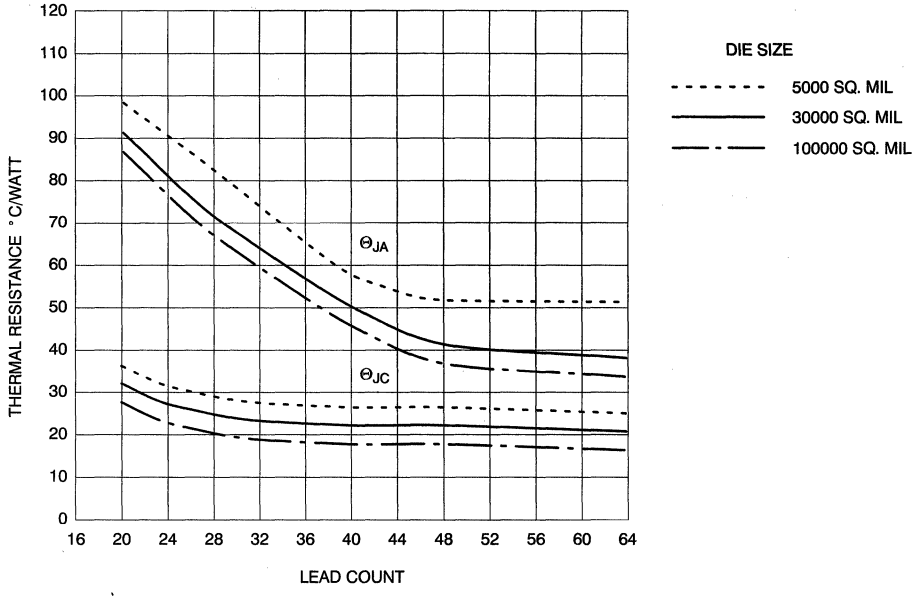

Figure 2. Thermal Resistance of Cypress Plastic DIPs (Package type "P")

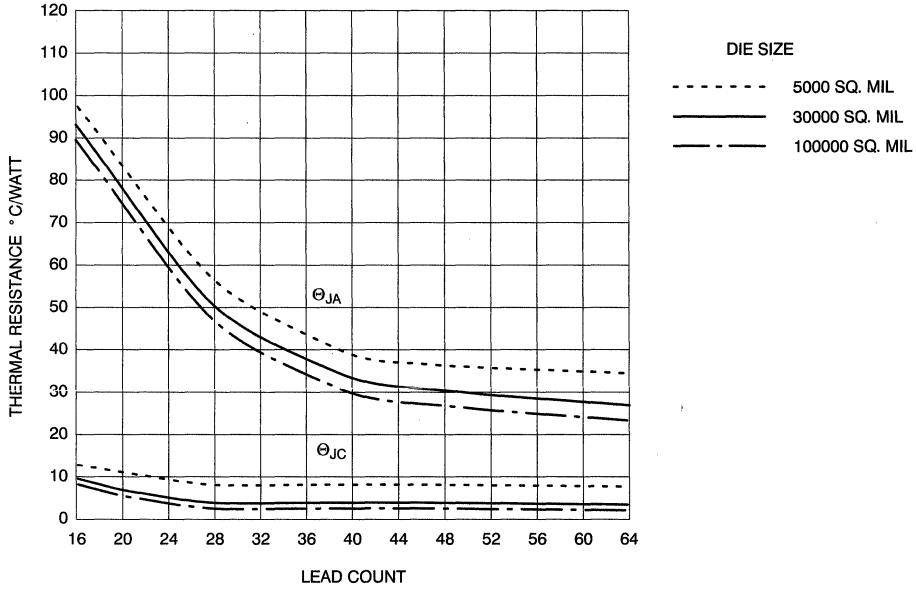

Figure 3. Thermal Resistance of Cypress Ceramic DIPs (Package type "D" and "W")

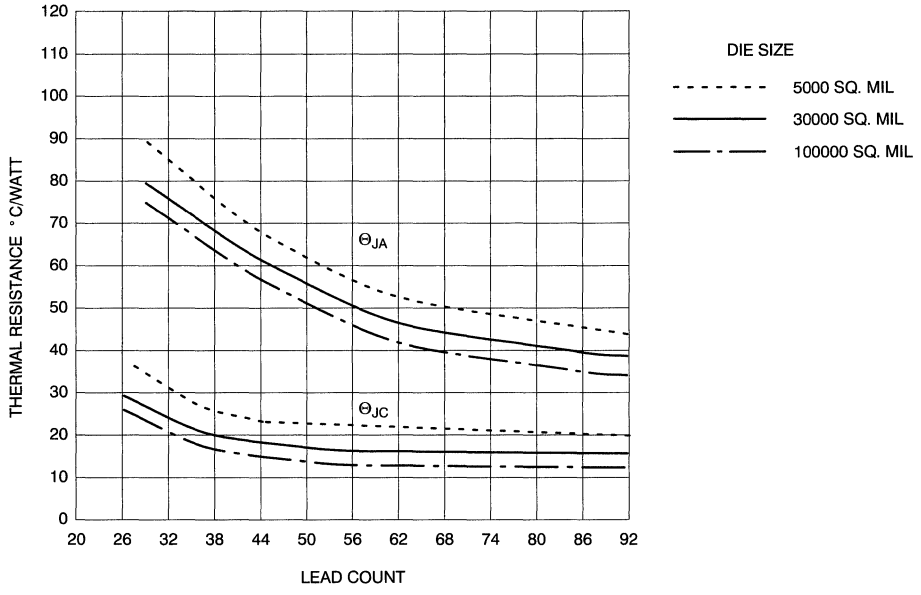

Figure 4. Thermal Resistance of Cypress PLCCs (Package type "J")

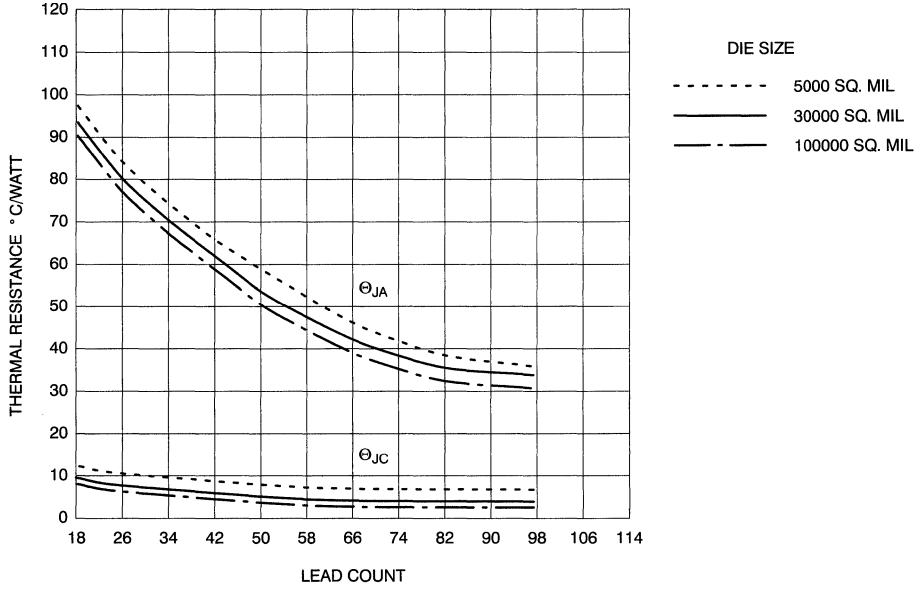

Figure 5. Thermal Resistance of Cypress LCCs (Package type "L" and "Q")

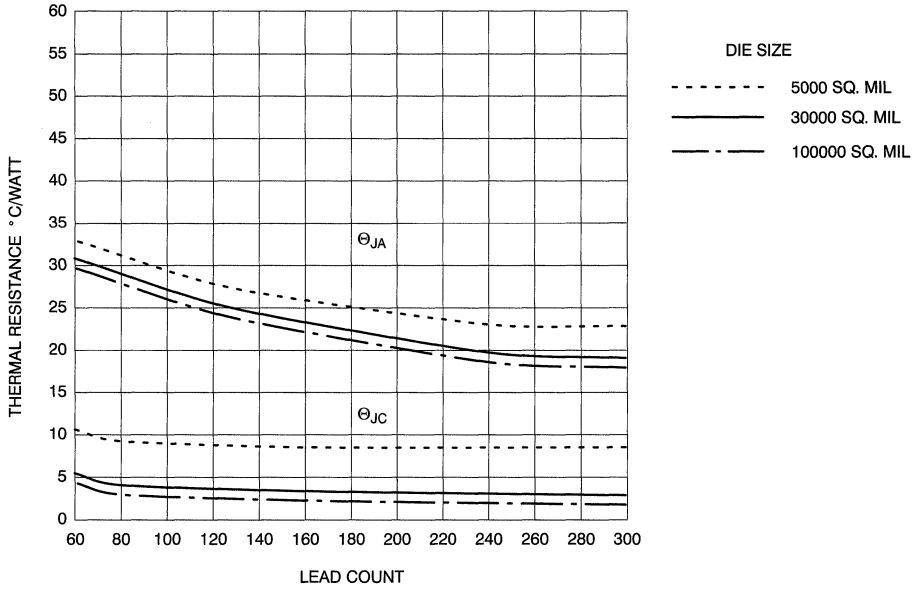

Figure 6. Thermal Resistance of Cypress Ceramic PGAs

Table 5. Plastic Surface Mount SOIC, SOJ[8,9]

Package Type "S" and "V"	Paddle Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 170	Copper	98 x 84	8,232	19.0	120
18	140 x 170	Copper	98 x 84	8,232	18.0	116
20	180 x 250	Copper	145 x 213	30,885	17.0	105
24	180 x 250	Copper	145 x 213	30,885	15.4	88
24	170 x 500	Copper	141 x 459	64,719	14.9	85
28	170 x 500	Copper	145 x 213	30,885	16.7	84
28	170 x 500	Copper	141 x 459	64,719	14.4	80

Table 6. Plastic Quad Flatpacks

Package Type "N"	LF Material	Paddle Size (mil)	Die Size (mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
100	Copper	310 x 310	235 x 235	17	51
144	Copper	310 x 310	235 x 235	18	41
160	Copper	310 x 310	230 x 230	18	40
184	Copper	460 x 460	322 x 311	15	38.5
208	Copper	400 x 400	290 x 320	16	39

Notes:
8. The data in *Table 6* was simulated for SOIC packaging.
9. SOICs and SOJs have very similar thermal resistance characteristics. The thermal resistance values given above apply to SOJ packages also.

Table 7. Ceramic Quad Flatpacks

Package Type "H" and "Y"	Cavity Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
28	250 x 250	Alloy 42	123 x 162	19,926	9.2	96
28	250 x 250	Alloy 42	150 x 180	27,000	8.9	93
32	316 x 317	Alloy 42	198 x 240	47,520	7.5	72
44	400 x 400	Alloy 42	310 x 250	77,500	5.9	55
52	400 x 400	Alloy 42	250 x 310	77,500	5.9	55
68	400 x 400	Alloy 42	310 x 250	77,500	5.4	33
84	450 x 450	Alloy 42	310 x 250	77,500	5.4	29

Table 8. Cerpacks

Package Type "K" and "T"	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 200	Alloy 42	100 x 118	11,800	10	107
18	140 x 200	Alloy 42	100 x 118	11,800	10	104
20	180 x 265	Alloy 42	128 x 170	21,760	9	102
24	170 x 270	Alloy 42	128 x 170	21,760	10	102
28	210 x 210	Alloy 42	150 x 180	27,000	9	98
32	210 x 550	Alloy 42	141 x 459	64,719	7	81

Table 9. Miscellaneous Packaging

Package Type	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
24 VDIP[10]	500 x 275	Alloy 42	145 x 213	30,885	6	57
68 CPGA[11]	350 x 350	Kovar Pins	323 x 273	88,179	3	28

Notes:
10. VDIP = "PV" package.
11. CPGA = "G" package.

Table 10. Die Sizes of Cypress Devices

Part Number	Size (mil^2)
SRAMs	
CY2147	10132
CY2148	9983
CY2149	9983
CY27LS03	4130
CY27S03A	4130
CY27S07A	4130
CY6116	20007
CY6116A	20007
CY6117	20007
CY6117A	20007
CY74S189	4130

Part Number	Size (mil^2)
CY7B134	76152
CY7B1342	76152
CY7B135	76152
CY7B138	76152
CY7B139	76152
CY7B144	76152
CY7B145	76152
CY7B160	27244
CY7B161	27244
CY7B162	27244
CY7B164	27244
CY7B166	27244

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil^2)
CY7B173	102200
CY7B174	102200
CY7B180	54600
CY7B181	54600
CY7B185	27244
CY7B186	27244
CY7B191	73152
CY7B192	73152
CY7B194	73152
CY7C122	6300
CY7C123	6300
CY7C128	20007
CY7C128A	17400
CY7C130	36636
CY7C131	36636
CY7C132	36636
CY7C136	36636
CY7C140	36636
CY7C141	36636
CY7C142	36636
CY7C146	36636
CY7C147	10132
CY7C148	9983
CY7C149	9983
CY7C150	6634
CY7C157	86460
CY7C161A	30885
CY7C162A	30885
CY7C164A	30885
CY7C166A	30885
CY7C167	21228
CY7C167A	21228
CY7C168	21228
CY7C168A	21228
CY7C169	21228
CY7C169A	21228
CY7C170	21228
CY7C170A	21228
CY7C171	21228

Part Number	Size (mil^2)
CY7C171A	21228
CY7C172	21228
CY7C172A	21228
CY7C183	65636
CY7C184	65636
CY7C185	30885
CY7C186	30885
CY7C187	30885
CY7C189	4130
CY7C190	4130
CY7C191	68150
CY7C192	68150
CY7C194	68150
CY7C196	68150
CY7C197	68150
CY7C198	68150
CY7C199	68150
CY7C191 (RAM2.5)	51590
CY7C192 (RAM2.5)	51590
CY7C194 (RAM2.5)	51590
CY7C196 (RAM2.5)	51590
CY7C197 (RAM2.5)	51590
CY7C198 (RAM2.5)	51590
CY7C199 (RAM2.5)	51590
CY7C9122	6300
CY93422A	6300
PROMs	
CY7C225	11815
CY7C235	13900
CY7C245	19321
CY7C245A	9394
CY7C251	49536
CY7C254	49536
CY7C261	28290
CY7C263	28290
CY7C264	28290
CY7C265	28290
CY7C266	28290
CY7C268	29400

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil^2)
CY7C269	29400
CY7C271	38750
CY7C274	38750
CY7C277	38750
CY7C279	38750
CY7C281	13900
CY7C282	13900
CY7C285	43875
CY7C286	43875
CY7C287	43875
CY7C289	43875
CY7C291	19182
CY7C291A	9394
CY7C292	19321
CY7C292A	9394
CY7C293A	9394
PLDs	
CY7C330	20088
CY7C331	16536
CY7C332	19116
CY7C335	23111
CY7C341	136320
CY7C342	83475
CY7C342B	49104
CY7C343	43953
CY7C344	21977
CY7C361	25872
PAL16L8	13552
PAL16R4	13552
PAL16R6	13552
PAL16R8	13552
PAL22V10C	18834
PAL22VP10C	18834
PALC16L8	9700
PALC16R4	9700
PALC16R6	9700

Part Number	Size (mil^2)
PALC16R8	9700
PALC22V10	19926
PALC22V10B	13284
PALC22V10D	12954
PLD20G10C	18834
PLDC18G8	7744
PLDC20G10	19926
PLDC20G10B	13284
PLDC20RA10	13284
FIFOs	
CY3341	8064
CY7C401	8064
CY7C402	8064
CY7C403	8064
CY7C404	8064
CY7C408A	16268
CY7C409A	16268
CY7C420	41019
CY7C421	41019
CY7C424	41019
CY7C425	41019
CY7C428	41019
CY7C429	41019
CY7C432	50040
CY7C433	50040
CY7C439	47160
CY7C441	44756
CY7C443	44756
CY7C451	44756
CY7C453	44756
CY7C460	89445
CY7C462	89445
CY7C464	89445
CY7C470	89445
CY7C472	89445
CY7C474	89445

Table 10. Die Sizes of Cypress Devices (continued)

Part Number	Size (mil^2)
Logic	
CY2909A	7968
CY2910A	21750
CY2911A	7968
CY7C2901	11800
CY7C510	30704
CY7C516	29000
CY7C517	29000
CY7C901	11800
CY7C909	7968
CY7C910	21750
CY7C9101	36108
CY7C911	7968

Part Number	Size (mil^2)
ECL	
CY100E301L	14875
CY100E302L	14875
CY100E422	6960
CY100E474	10830
CY100E494	29575
CY10E301L	14875
CY10E302L	14875
CY10E422	6960
CY10E474	10830
CY10E494	29575
Bus Interface	
CY7C964	21460
VAC068	101060
VIC068A	103620
VIC64	103620

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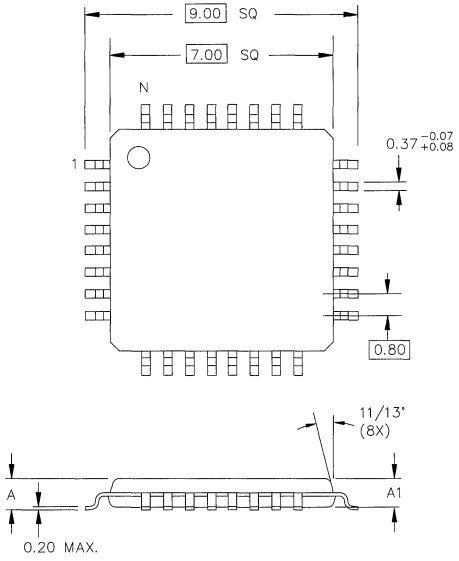
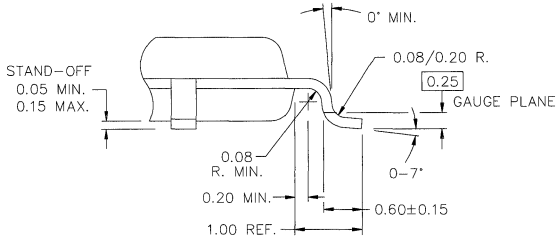
Package Diagrams

Thin Quad Flat Packs

32-Lead Thin Plastic Quad Flat Pack A32



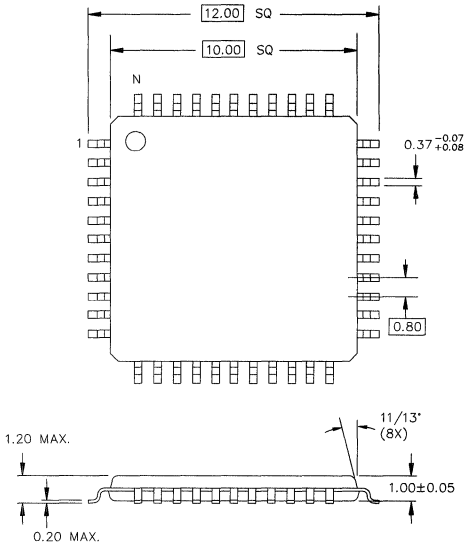
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



DIM. A	DIM. A1
1.60 MAX.	1.40±0.05 PKG. THICK
1.20 MAX.	1.00±0.05 PKG. THICK

Thin Quad Flat Packs (continued)

44-Lead Thin Plastic Quad Flat Pack A44



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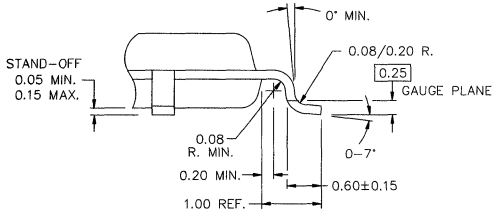
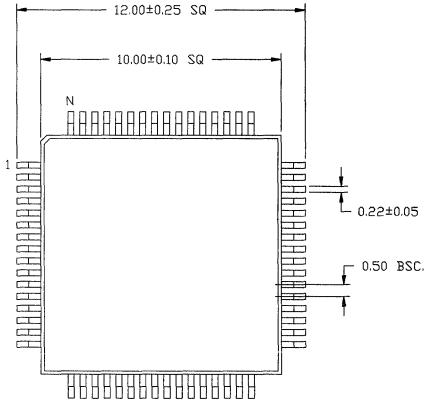
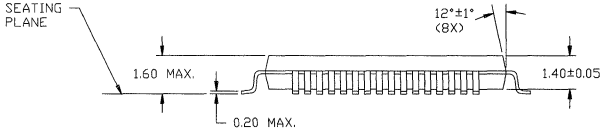
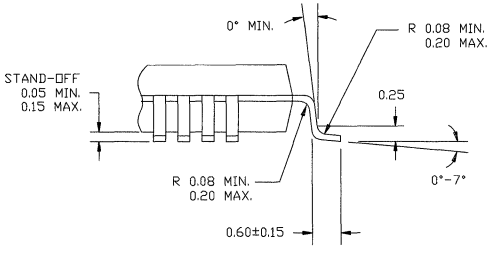


64-Pin Thin Quad Flat Pack A64



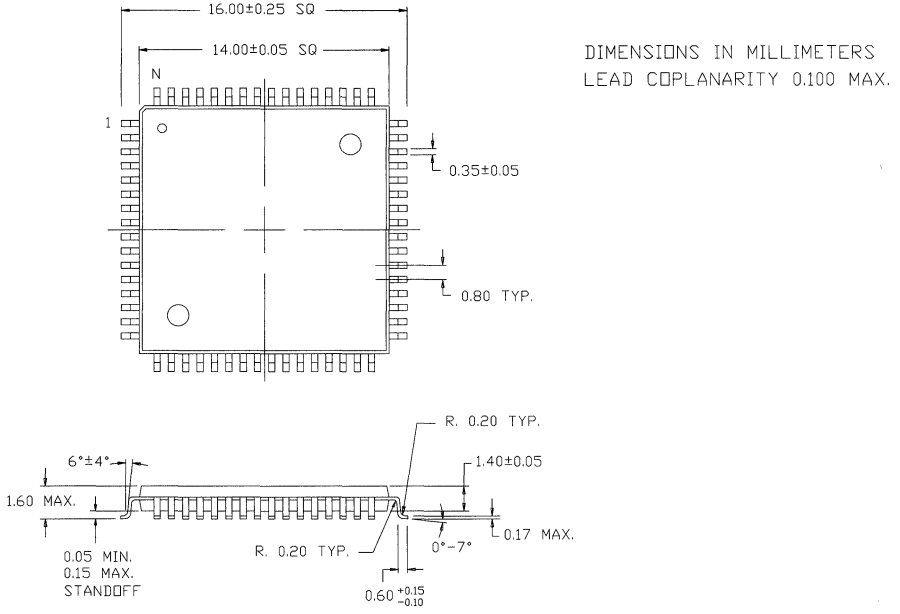
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



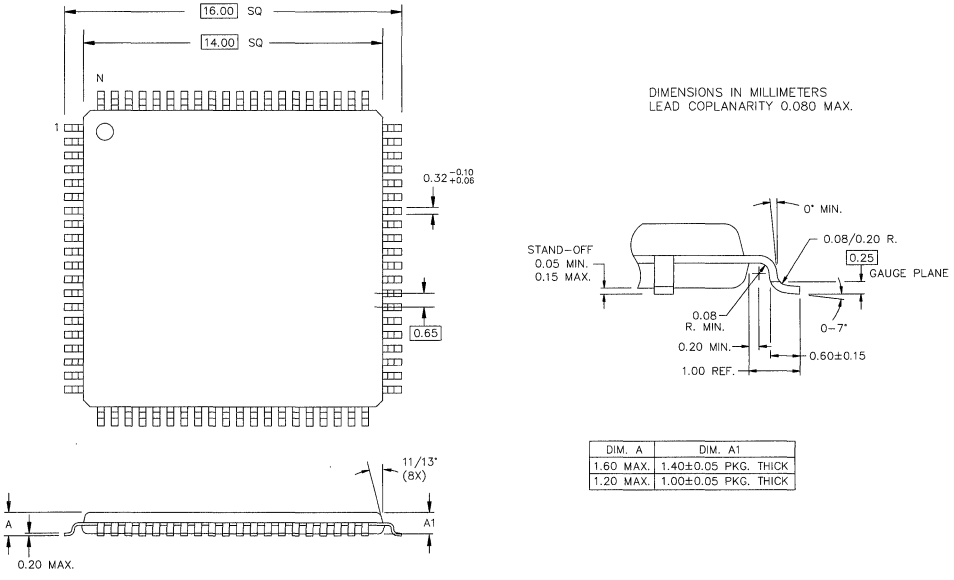


Thin Quad Flat Packs (continued)

64-Lead Thin Plastic Quad Flat Pack A65



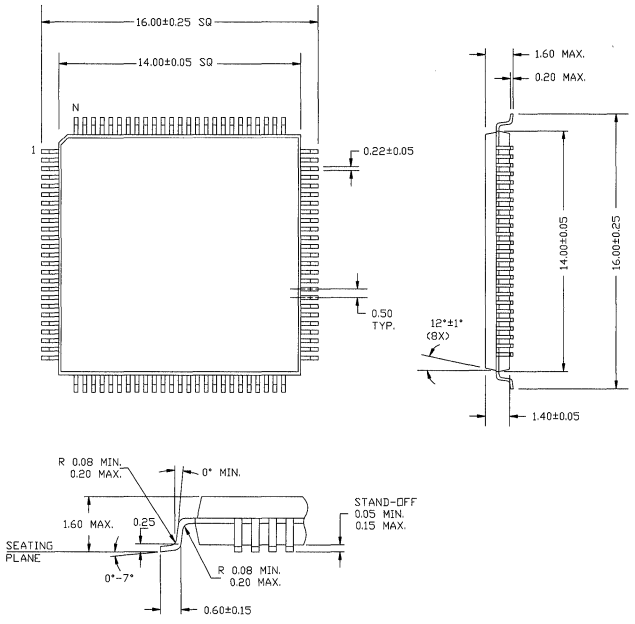
80-Pin Thin Plastic Quad Flat Pack A80



DIM. A	DIM. A1
1.60 MAX.	1.40±0.05 PKG. THICK
1.20 MAX.	1.00±0.05 PKG. THICK

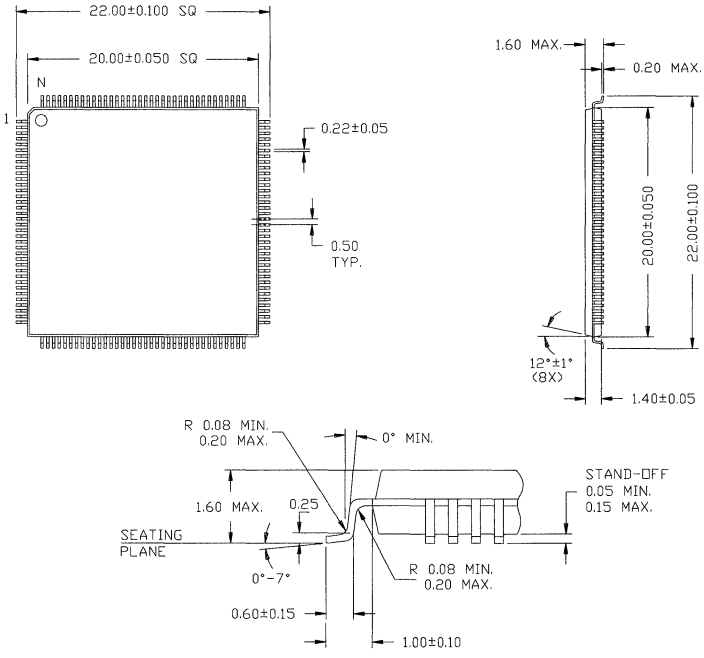
Thin Quad Flat Packs (continued)

100-Pin Thin Quad Flat Pack A100



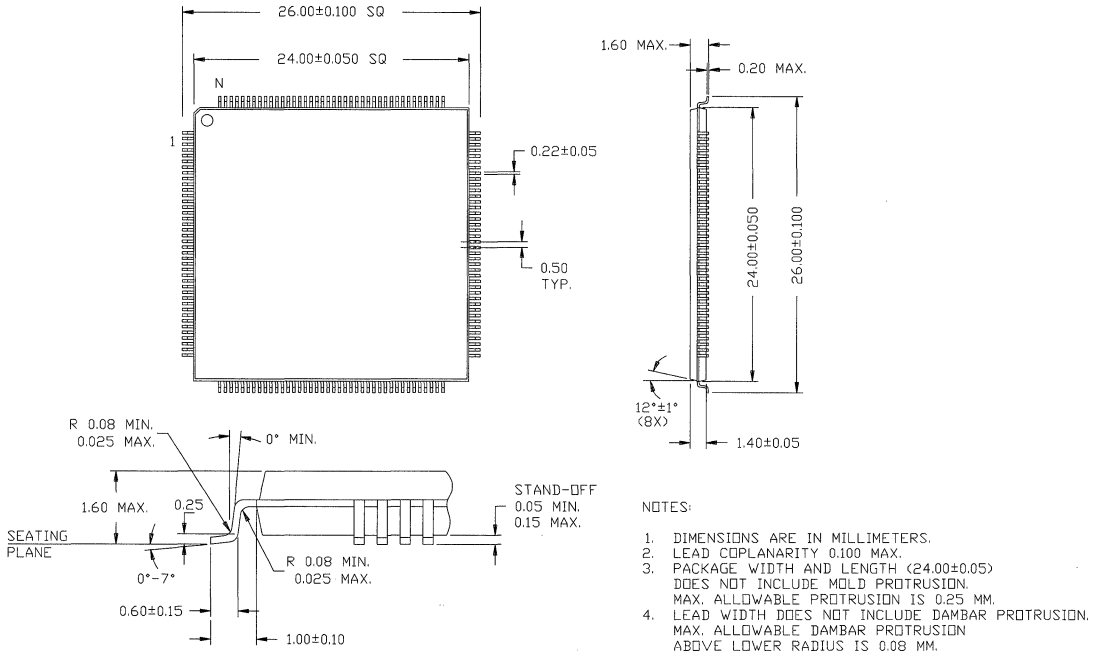
Thin Quad Flat Packs (continued)

144-Pin Thin Quad Flat Pack A144



Thin Quad Flat Packs (continued)

160-Lead Thin Quad Flat Pack (TQFP) A160

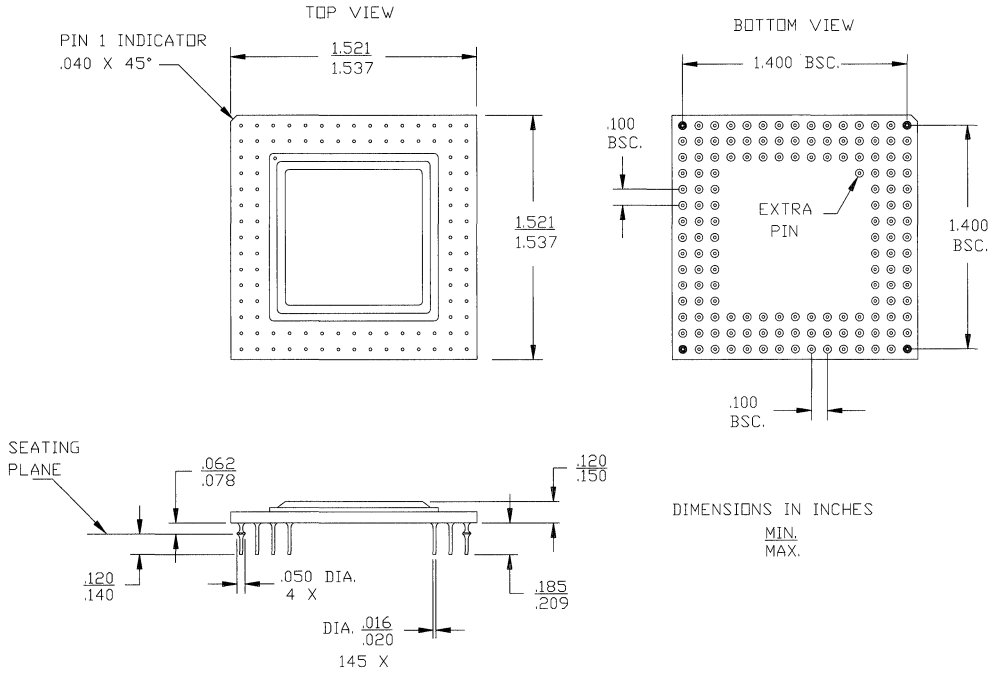


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00±0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

Plastic Pin Grid Arrays

145-Pin Plastic Grid Array (Cavity Up) B144



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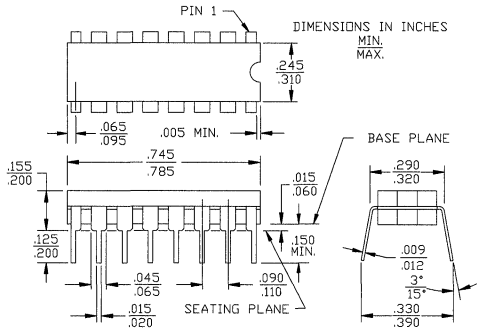
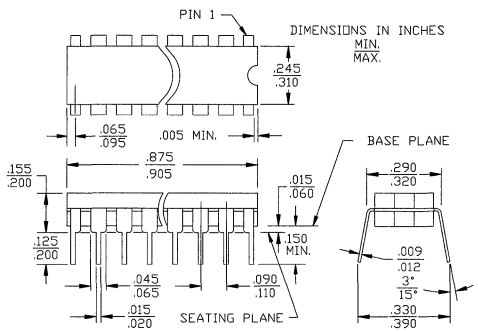
Ceramic Dual-In-Line Packages

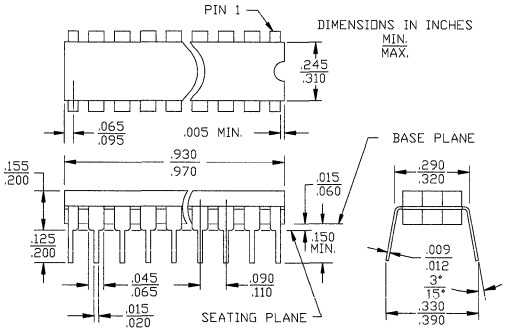
16-Lead (300-Mil) CerDIP D2
MIL–STD–1835 D–2 Config. A



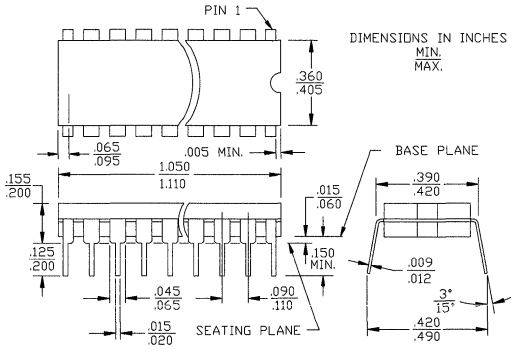
18-Lead (300-Mil) CerDIP D4
MIL–STD–1835 D–8 Config. A



20-Lead (300-Mil) CerDIP D6
MIL–STD–1835 D–8 Config. A

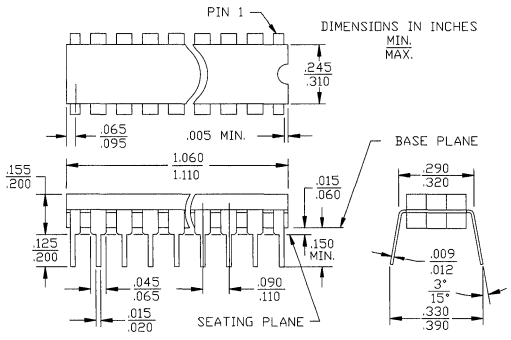


22-Lead (400-Mil) CerDIP D8
MIL–STD–1835 D–7 Config. A

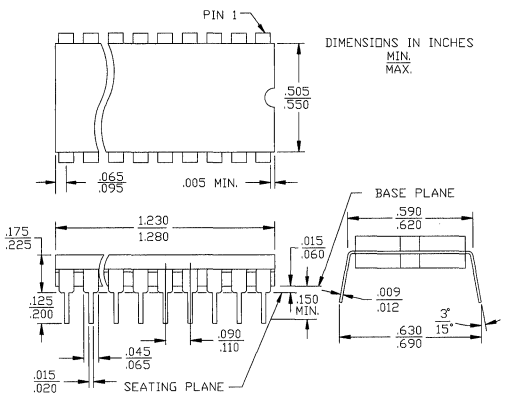


Ceramic Dual-In-Line Packages (continued)

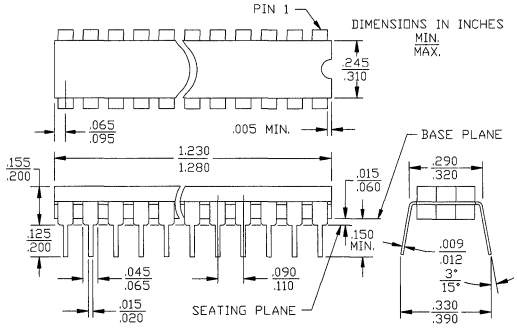
22-Lead (300-Mil) CerDIP D10



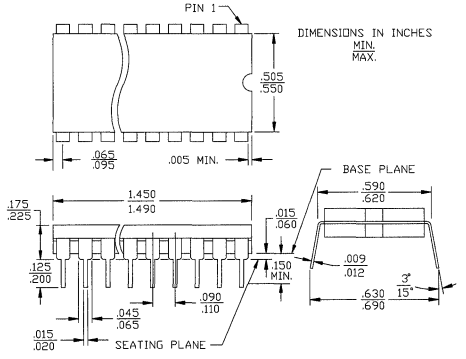
24-Lead (600-Mil) CerDIP D12
MIL–STD–1835 D–3 Config. A



24-Lead (300-Mil) CerDIP D14
MIL–STD–1835 D–9 Config. A



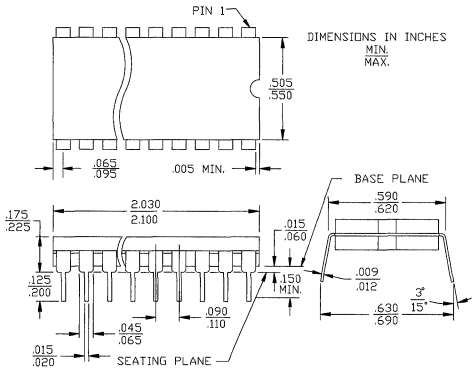
28-Lead (600-Mil) CerDIP D16
MIL–STD–1835 D–10 Config. A



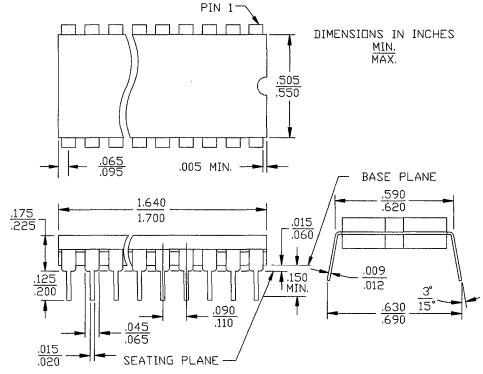
14

Ceramic Dual-In-Line Packages (continued)

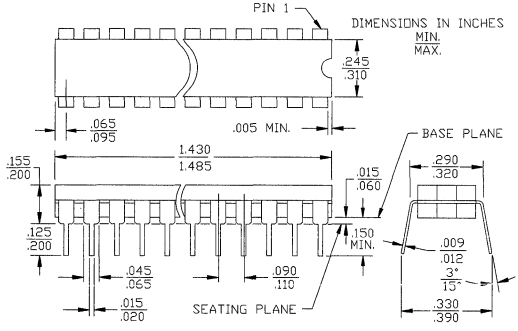
40-Lead (600-Mil) CerDIP D18
MIL–STD–1835 D–5 Config. A



32-Lead (600-Mil) CerDIP D20

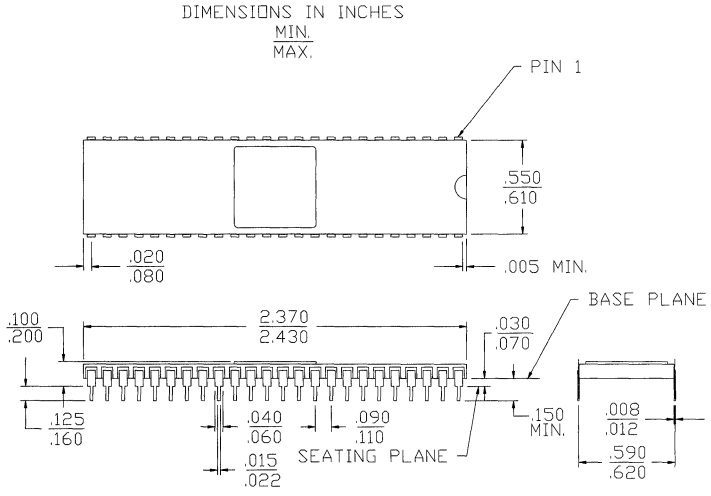


28-Lead (300-Mil) CerDIP D22
MIL–STD–1835 D–15 Config. A

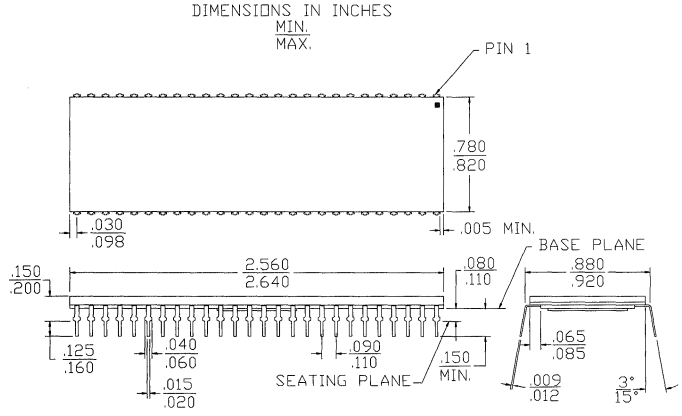


Ceramic Dual-In-Line Packages (continued)

48-Lead (600-Mil) Sidebraze DIP D26
MIL–STD–1835 D–14 Config. C



52-Lead (900-Mil) Bottombraze DIP D28



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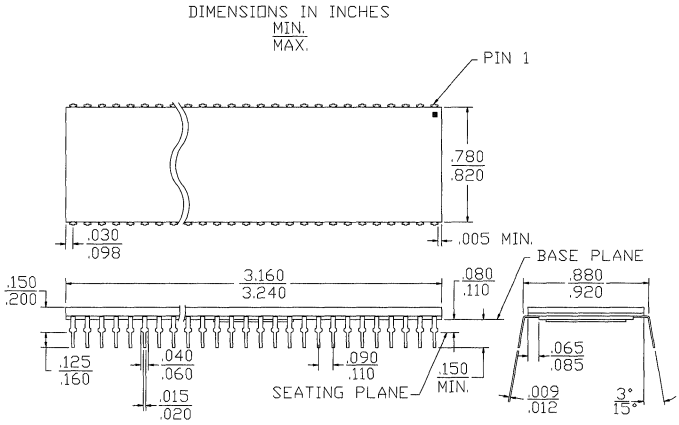
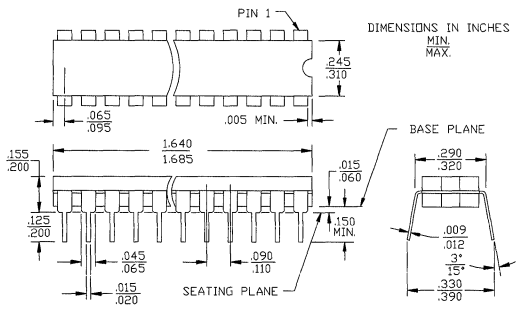
Ceramic Dual-In-Line Packages (continued)

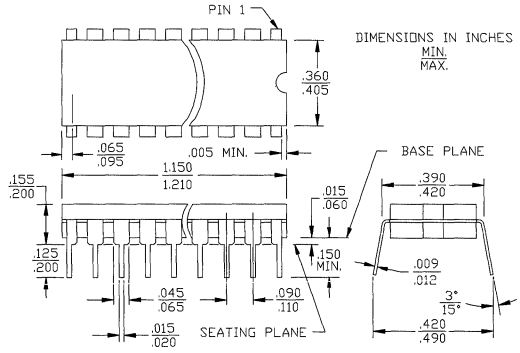
64-Lead (900-Mil) Bottombraze DIP D30



32-Lead (300-Mil) CerDIP D32

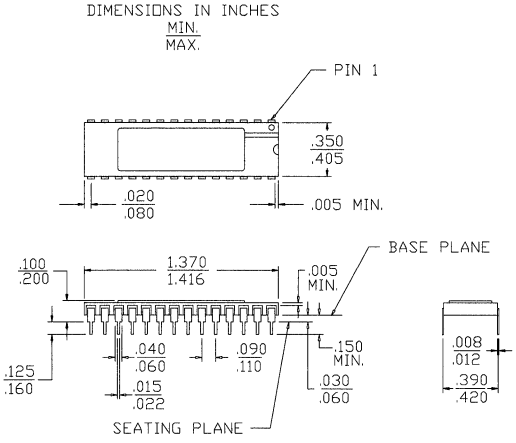


24-Lead (400-Mil) Sidebraze DIP D40
MIL−STD−1835 D−11 Config. A

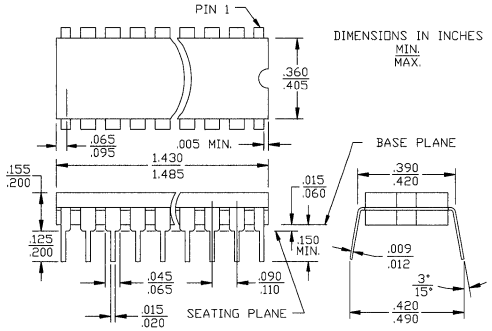


Ceramic Dual-In-Line Packages (continued)

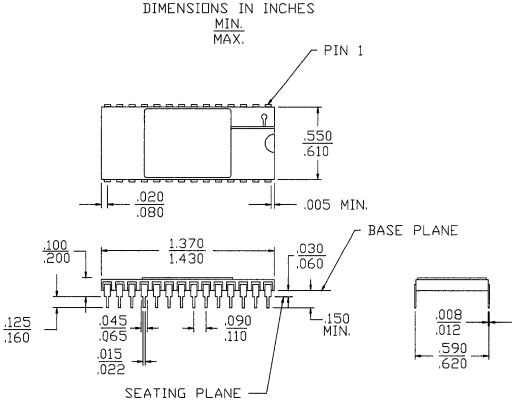
28-Lead (400-Mil) Sidebraze DIP D41



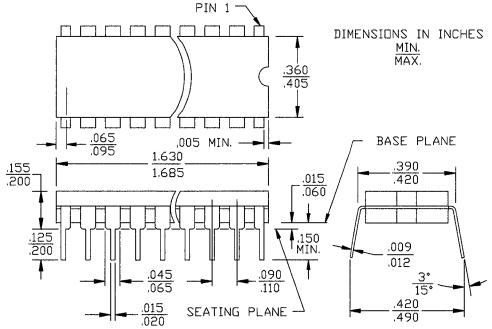
28-Lead (400-Mil) CerDIP D42



28-Lead (600-Mil) Sidebraze DIP D43



32-Lead (400-Mil) CerDIP D44



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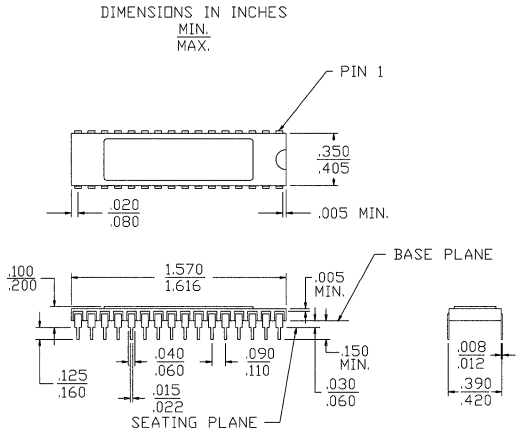
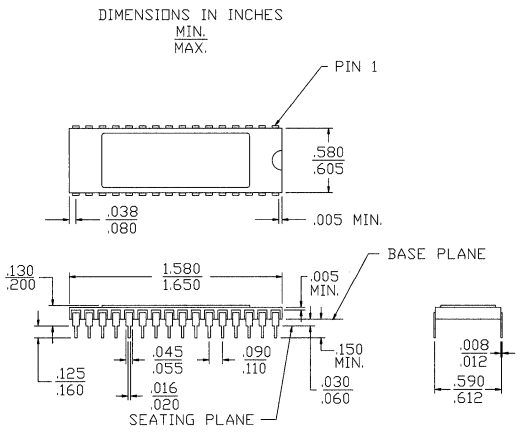
Ceramic Dual-In-Line Packages (continued)

32-Lead (400-Mil) Sidebraze DIP D46

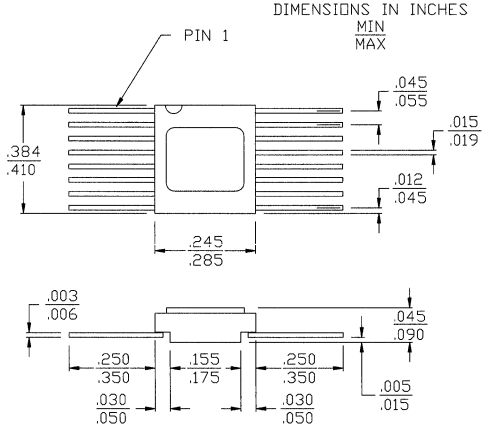


32-Lead (600-Mil) Sidebraze DIP D50

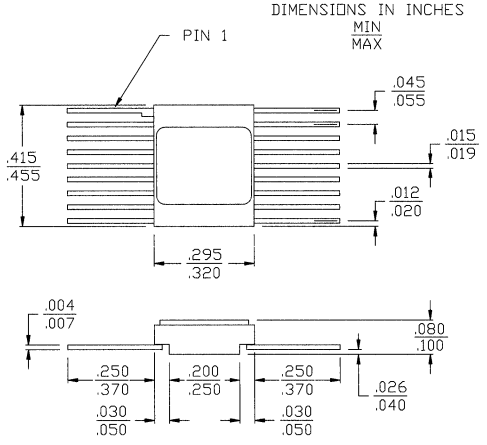


Ceramic Flatpacks

16-Lead Rectangular Flatpack F69
MIL–STD–1835 F–5 Config. B

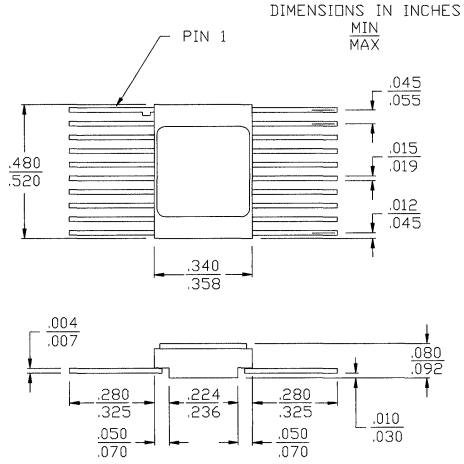


18-Lead Rectangular Flatpack F70

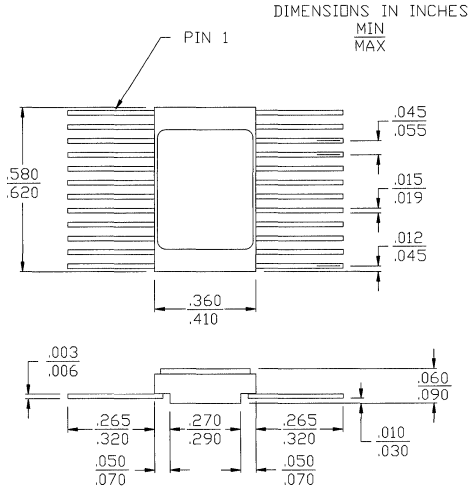


Ceramic Flatpacks (continued)

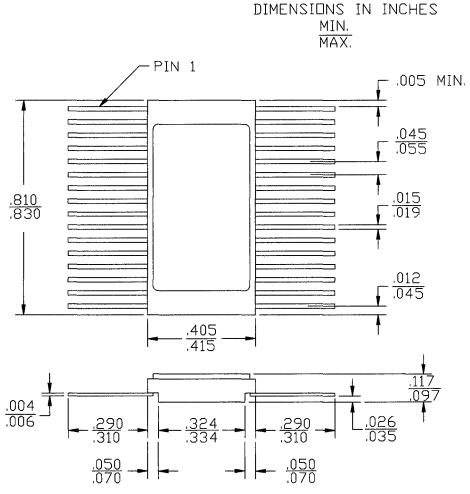
20-Lead Rectangular Flatpack F71



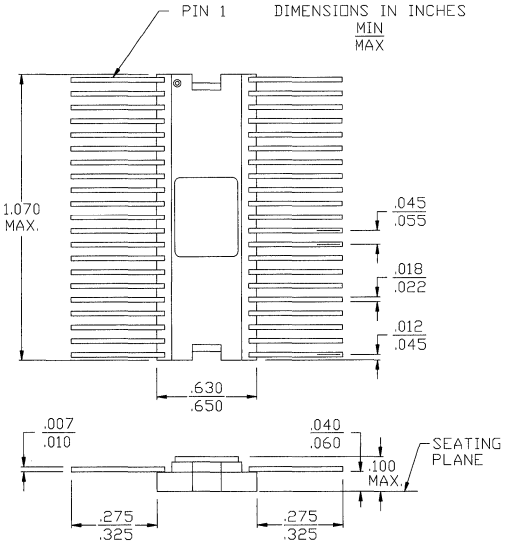
24-Lead Rectangular Flatpack F73
MIL–STD–1835 F–6 Config. B



32-Lead Rectangular Flatpack F75

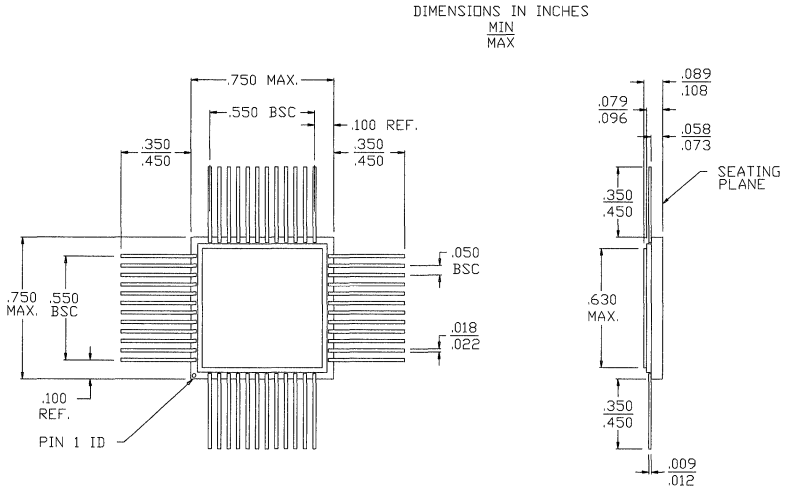


42-Lead Rectangular Flatpack F76

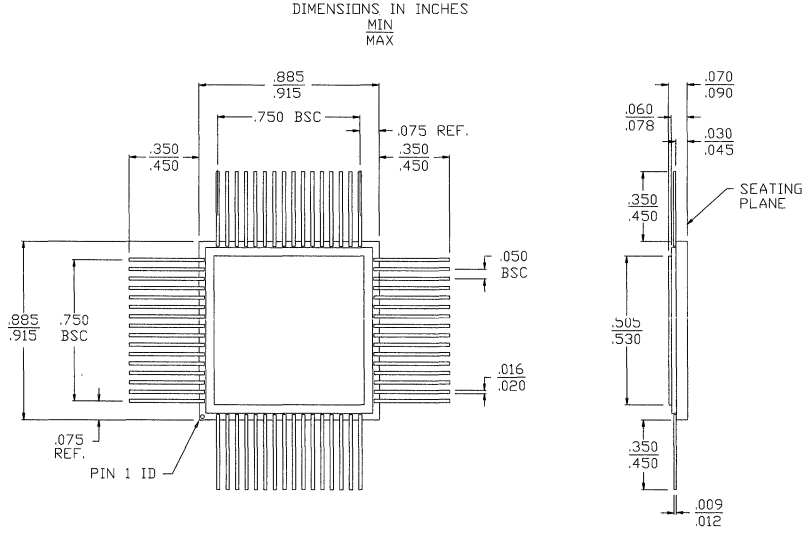


Ceramic Flatpacks (continued)

48-Lead Quad Flatpack F78

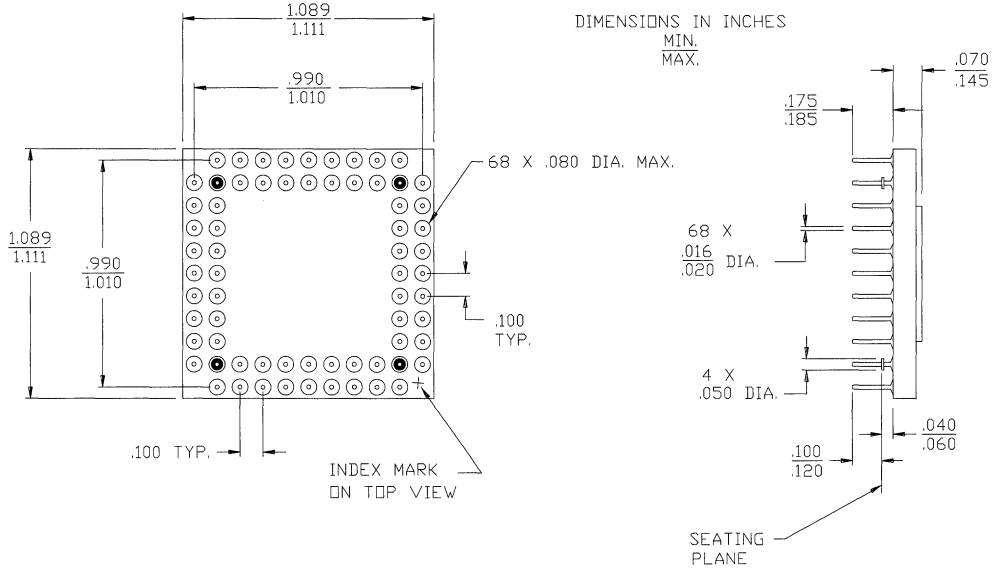


64-Lead Quad Flatpack F90

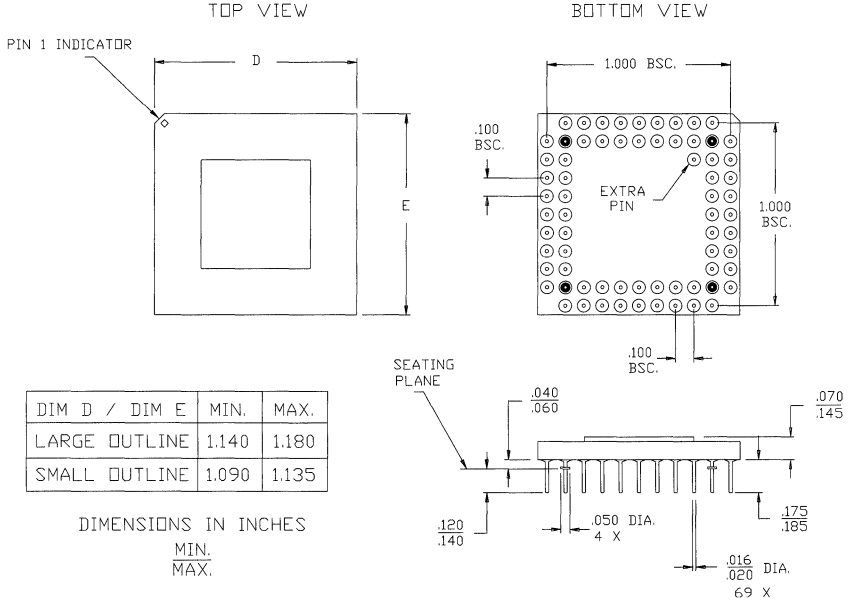


Ceramic Pin Grid Arrays

68-Pin Grid Array (Cavity Up) G68



69-Pin Grid Array (Cavity Up) G69

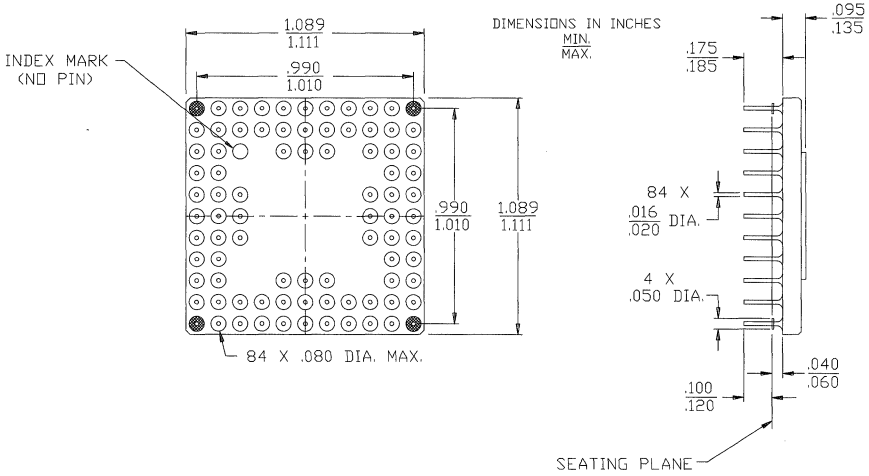


DIM D / DIM E	MIN.	MAX.
LARGE OUTLINE	1.140	1.180
SMALL OUTLINE	1.090	1.135

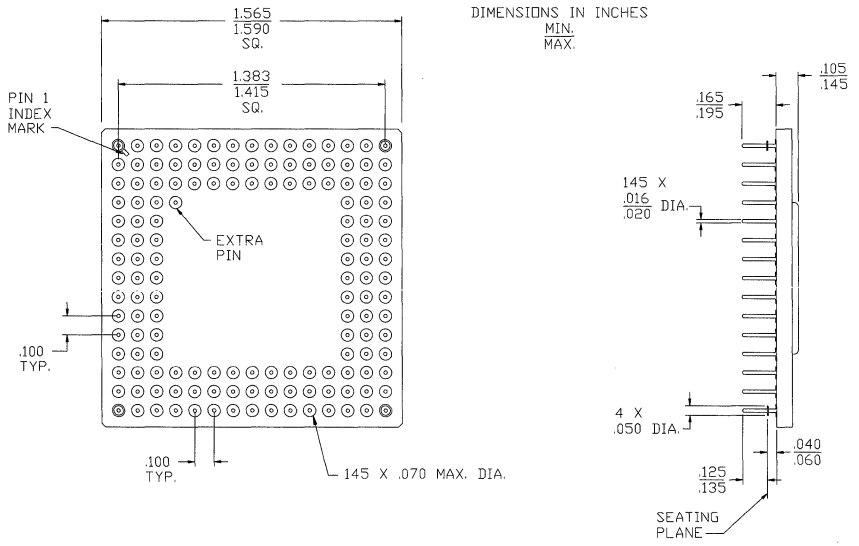
DIMENSIONS IN INCHES
MIN.
MAX.

Ceramic Pin Grid Arrays (continued)

84-Pin Grid Array (Cavity Up) G84

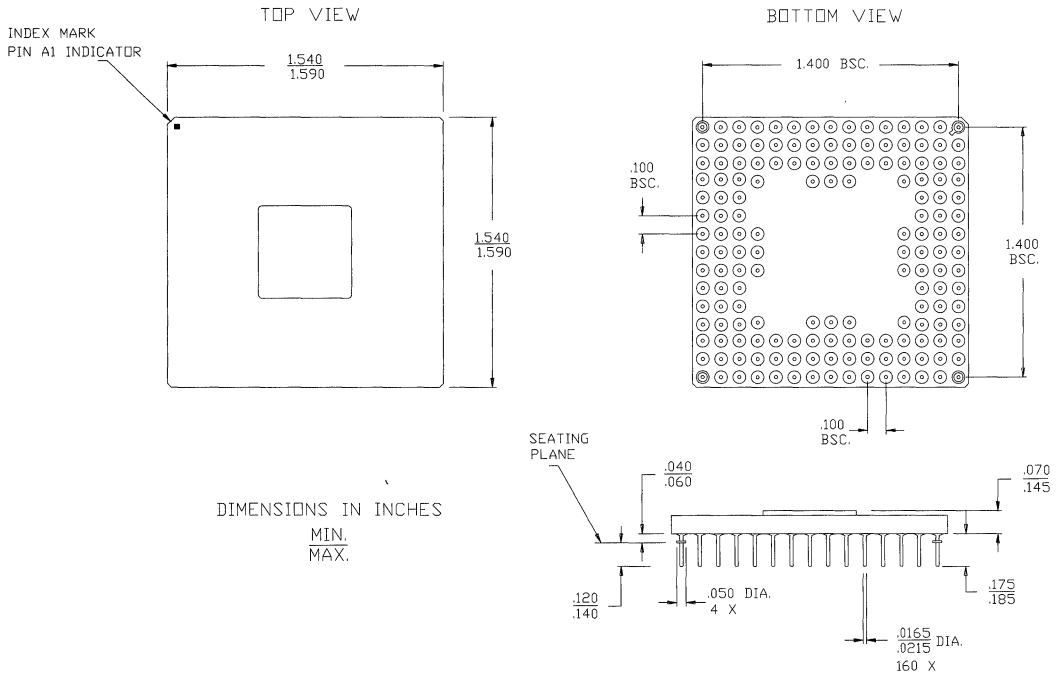


145-Pin Grid Array (Cavity Up) G145



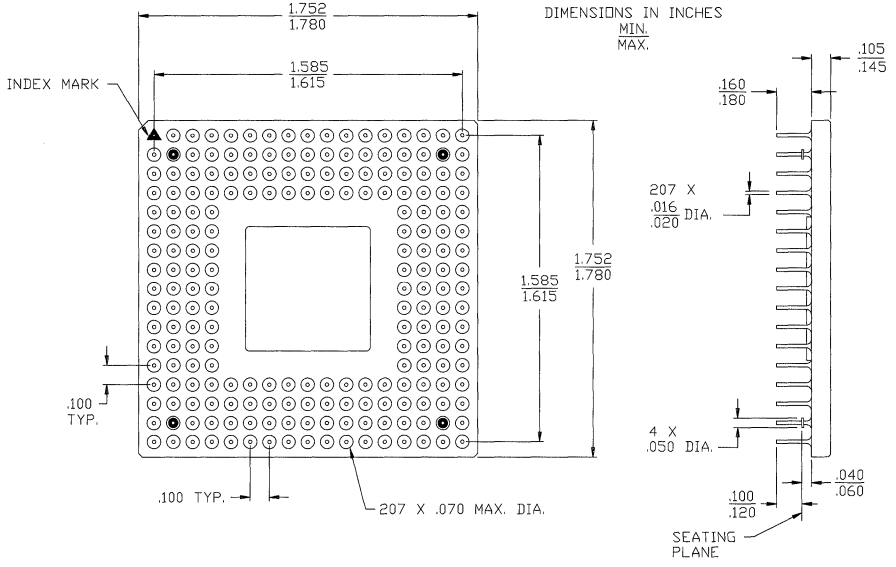
Ceramic Pin Grid Arrays (continued)

160-Pin PGA G160



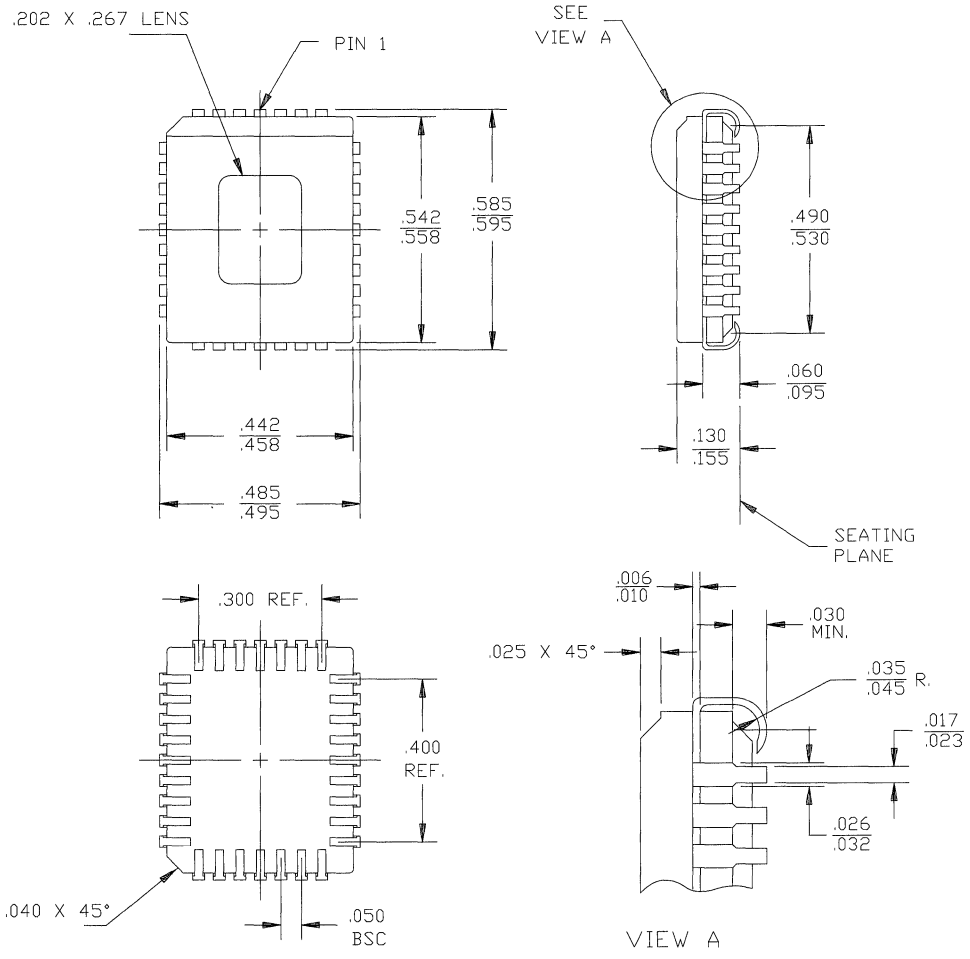
Ceramic Pin Grid Arrays (continued)

207-Pin Grid Array (Cavity Down) G207



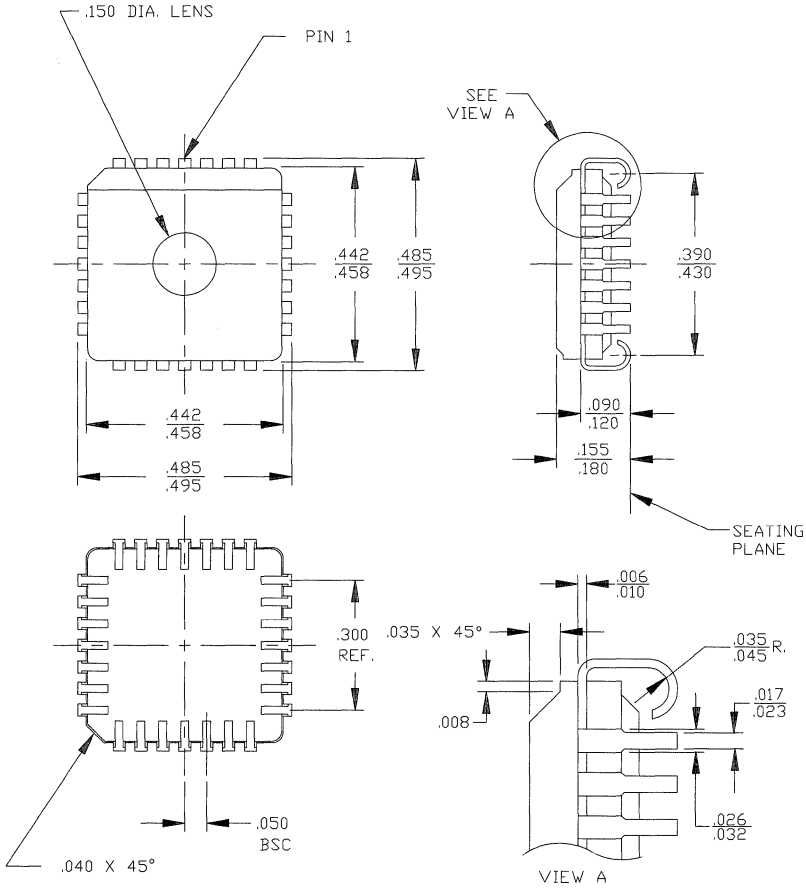
Ceramic Windowed J-Leaded Chip Carriers

32-Pin Windowed Leaded Chip Carrier H32



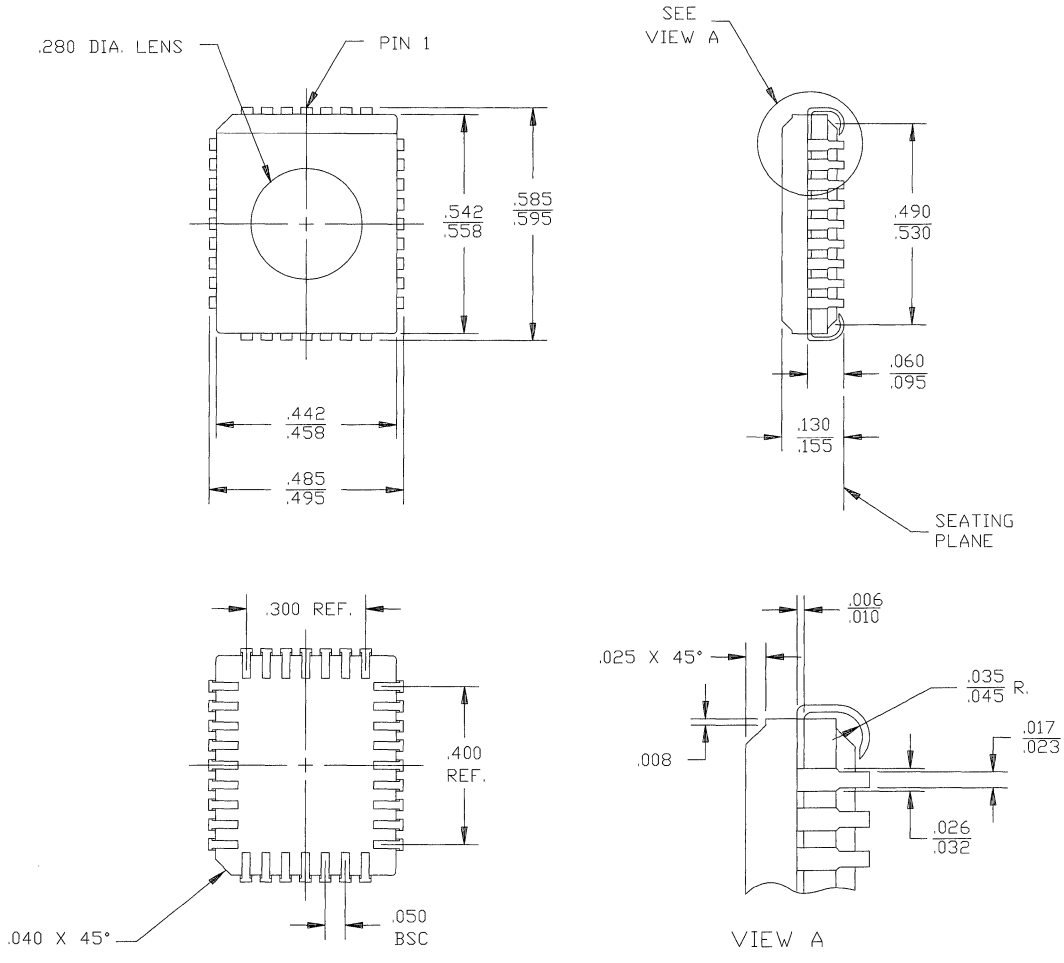
Ceramic Windowed J-Leaded Chip Carriers (continued)

28-Pin Windowed Leaded Chip Carrier H64



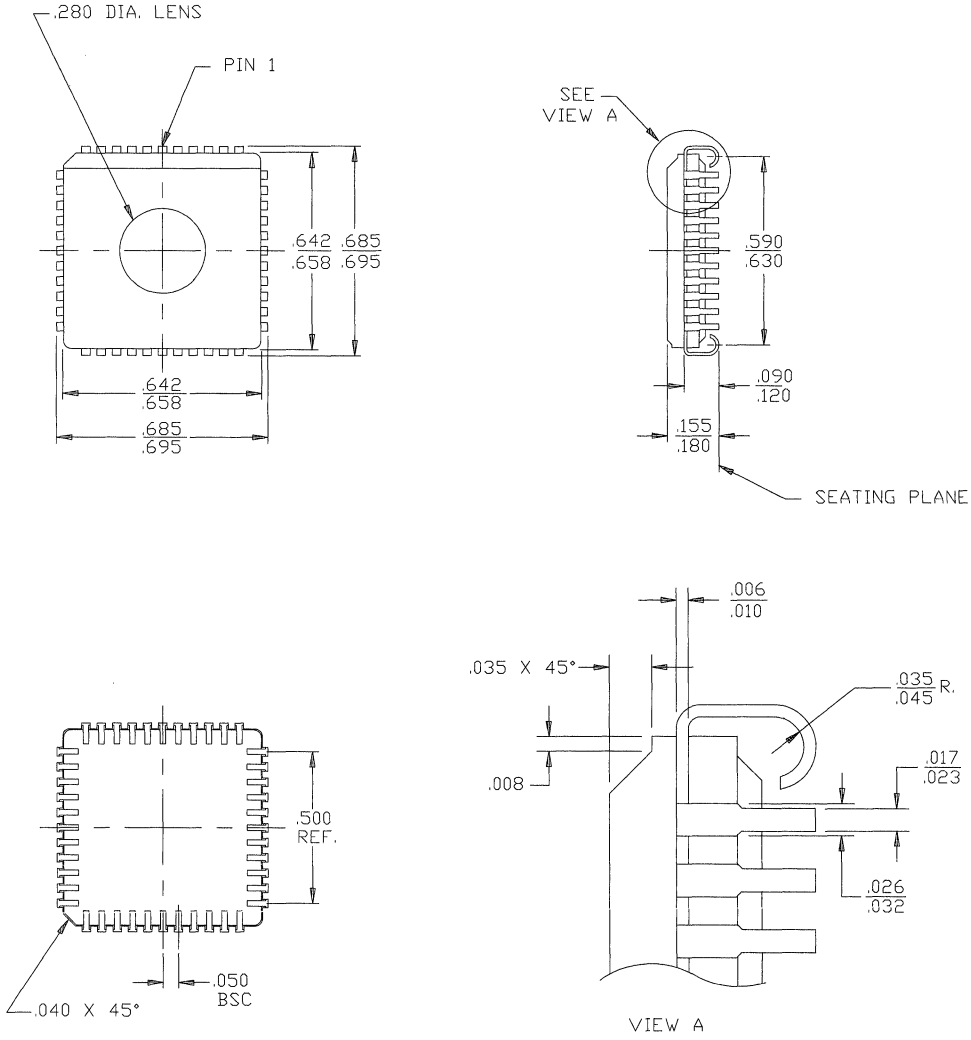
Ceramic Windowed J-Leaded Chip Carriers (continued)

32-Pin Windowed Leaded Chip Carrier H65



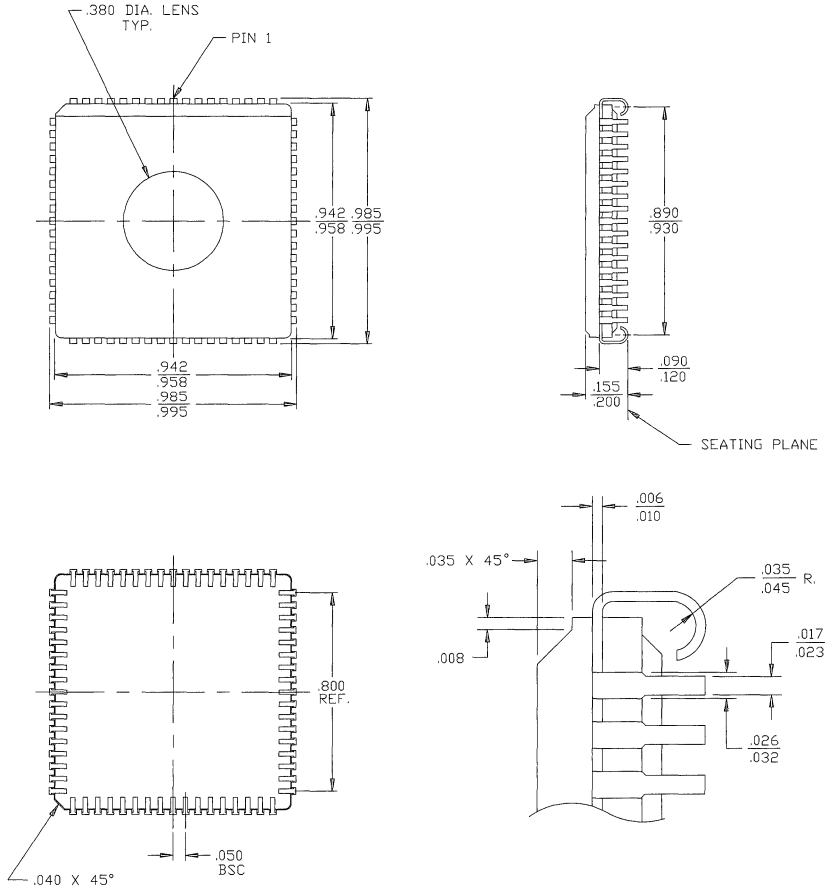
Ceramic Windowed J-Leaded Chip Carriers (continued)

44-Pin Windowed Leaded Chip Carrier H67



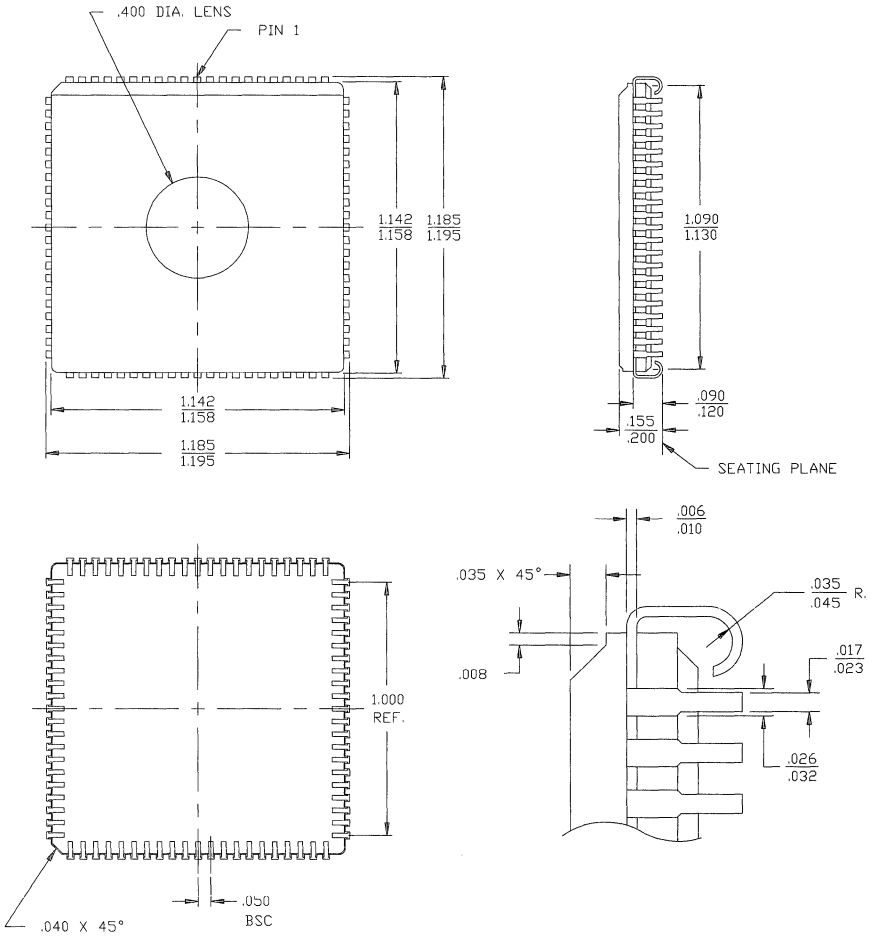
Ceramic Windowed J-Leaded Chip Carriers (continued)

68-Pin Windowed Leaded Chip Carrier H81



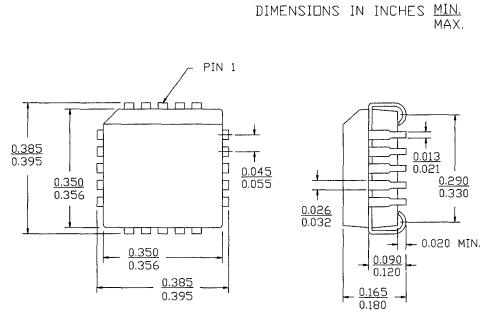
Ceramic Windowed J-Leaded Chip Carriers (continued)

84-Lead Windowed Leaded Chip Carrier H84

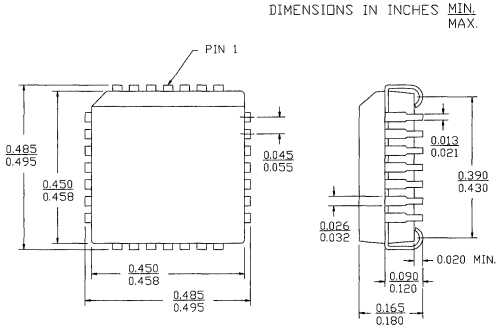


Plastic Leaded Chip Carriers

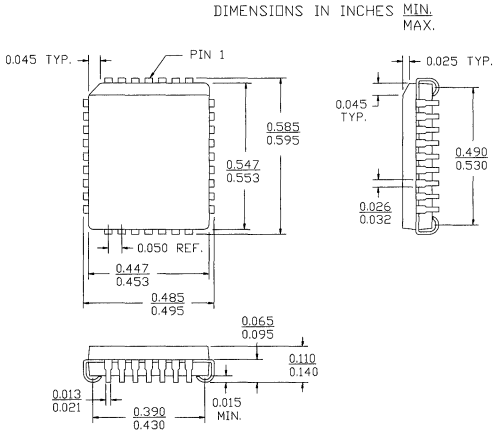
20-Lead Plastic Leaded Chip Carrier J61



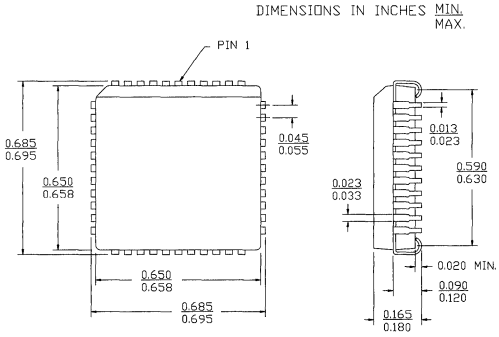
28-Lead Plastic Leaded Chip Carrier J64



32-Lead Plastic Leaded Chip Carrier J65

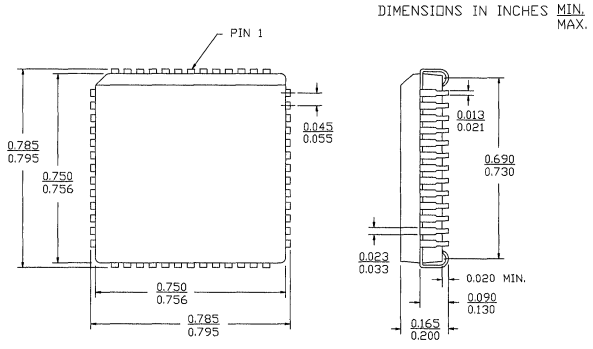


44-Lead Plastic Leaded Chip Carrier J67

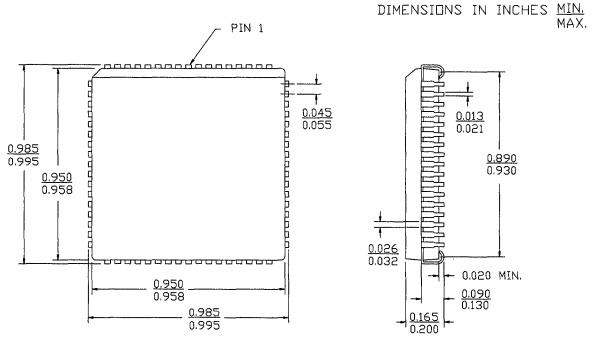


Plastic Leaded Chip Carriers (continued)

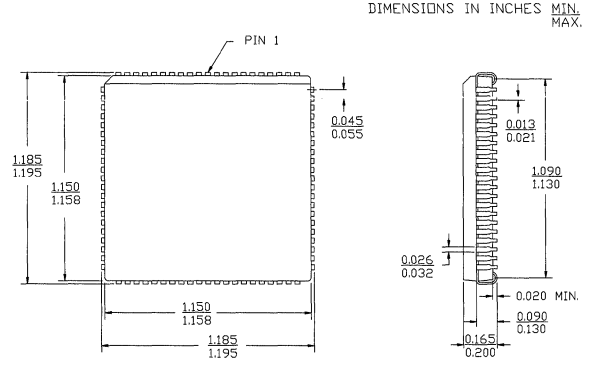
52-Lead Plastic Leaded Chip Carrier J69



68-Lead Plastic Leaded Chip Carrier J81

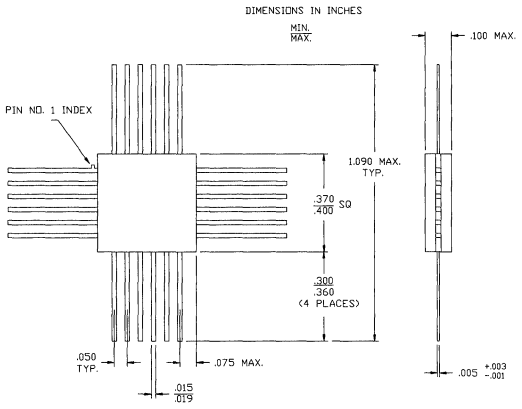


84-Lead Plastic Leaded Chip Carrier J83



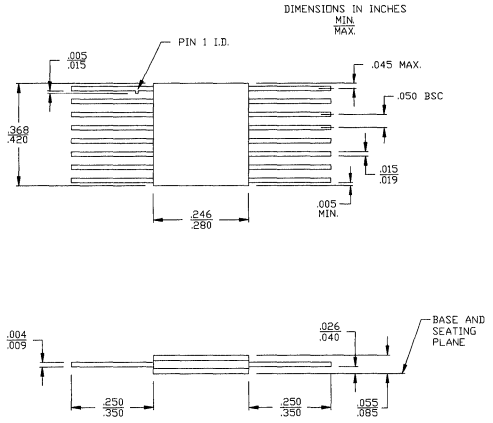
Cerpacks

24-Lead Square Cerpack K63



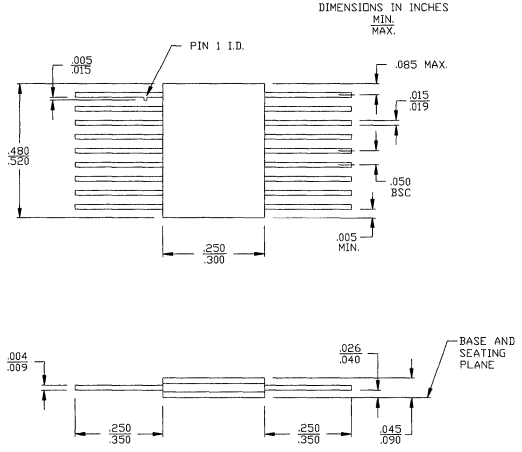
16-Lead Rectangular Cerpack K69

MIL–STD–1835 F–5 Config. A



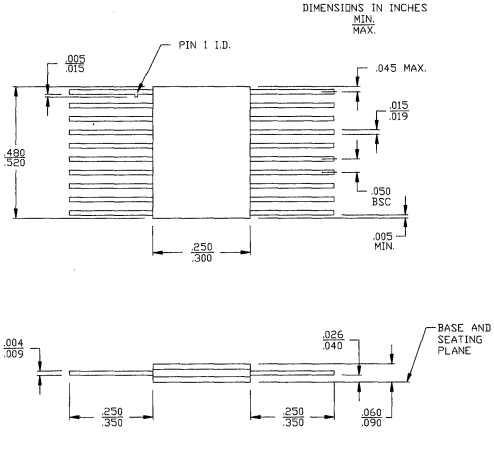
18-Lead Rectangular Cerpack K70

MIL–STD–1835 F–10 Config. A



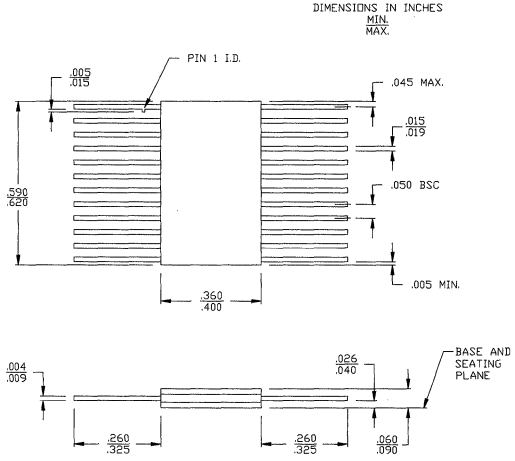
20-Lead Rectangular Cerpack K71

MIL–STD–1835 F–9 Config. A

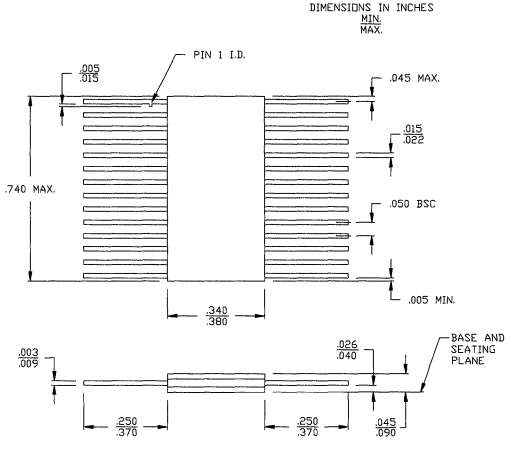


Cerpacks (continued)

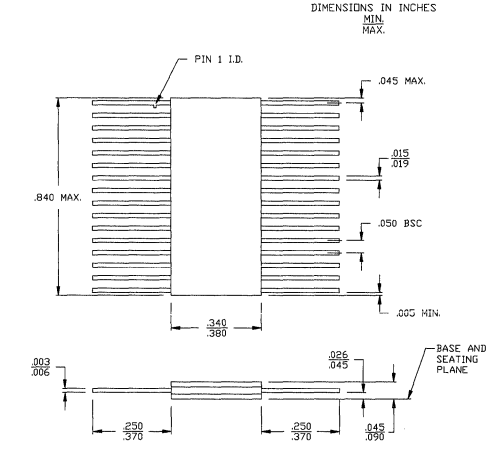
24-Lead Rectangular Cerpack K73
MIL–STD–1835 F–6 Config. A



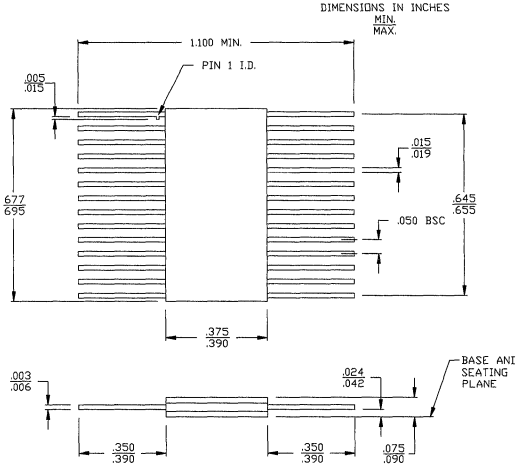
28-Lead Rectangular Cerpack K74
MIL–STD–1835 F–11 Config. A



32-Lead Rectangular Cerpack K75

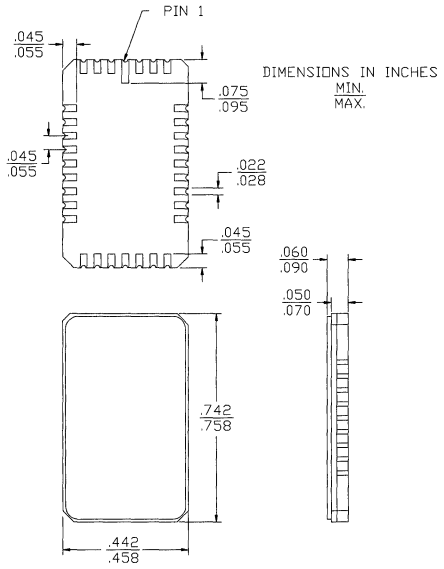


28-Lead Rectangular Cerpack K80

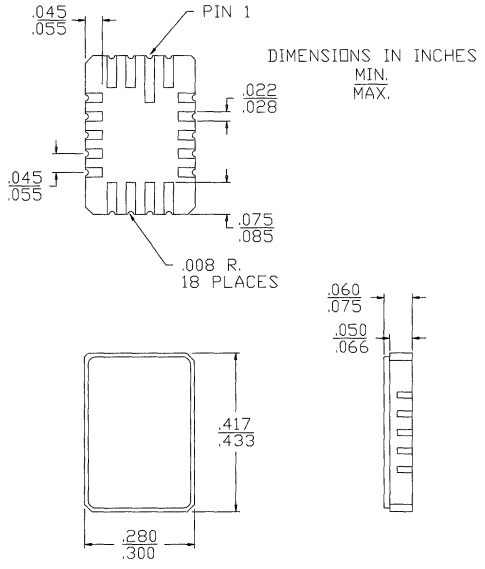


Ceramic Leadless Chip Carriers

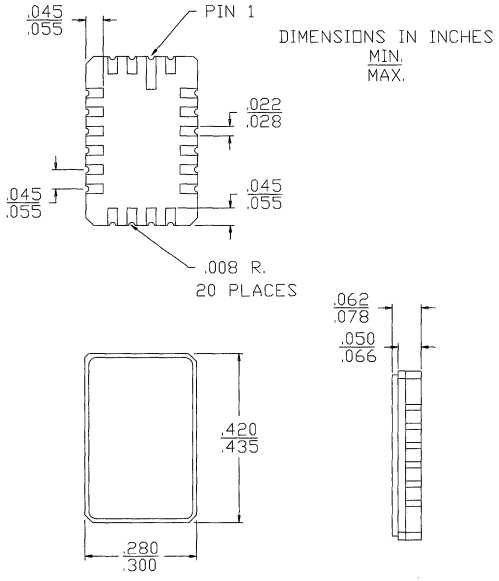
32-Lead Leadless Chip Carrier L45



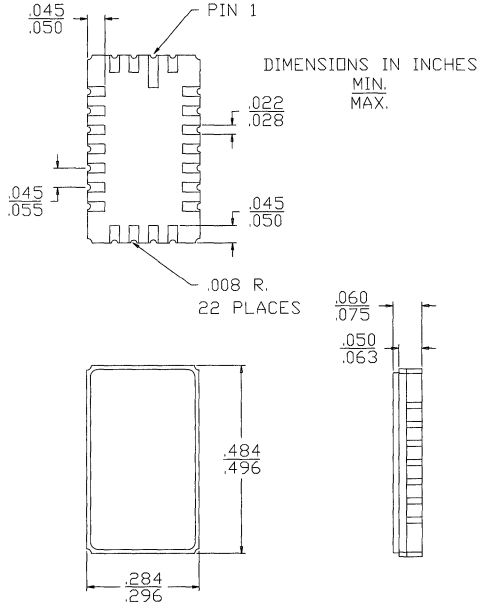
18-Pin Rectangular Leadless Chip Carrier L50
MIL–STD–1835 C–10A



20-Pin Rectangular Leadless Chip Carrier L51
MIL–STD–1835 C–13

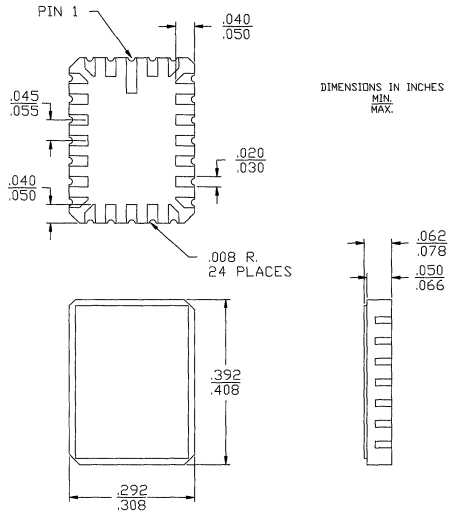


22-Pin Rectangular Leadless Chip Carrier L52

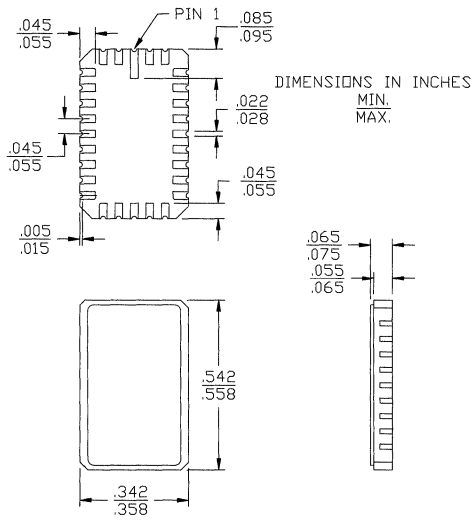


Ceramic Leadless Chip Carriers (continued)

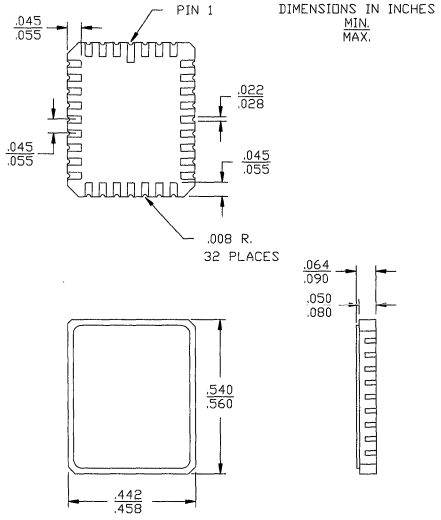
24-Pin Rectangular Leadless Chip Carrier L53



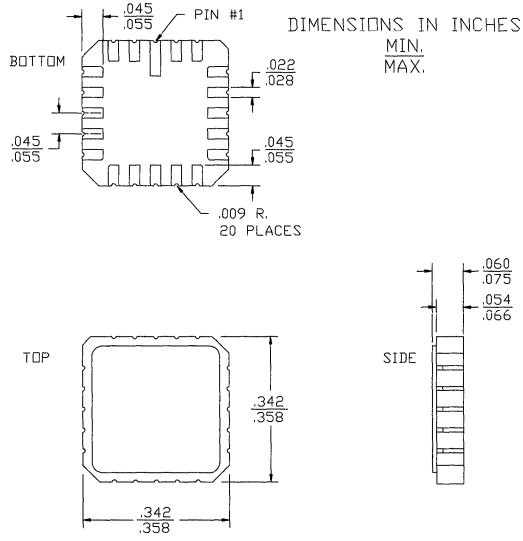
28-Pin Rectangular Leadless Chip Carrier L54
MIL-STD-1835 C-11A



32-Pin Rectangular Leadless Chip Carrier L55
MIL-STD-1835 C-12

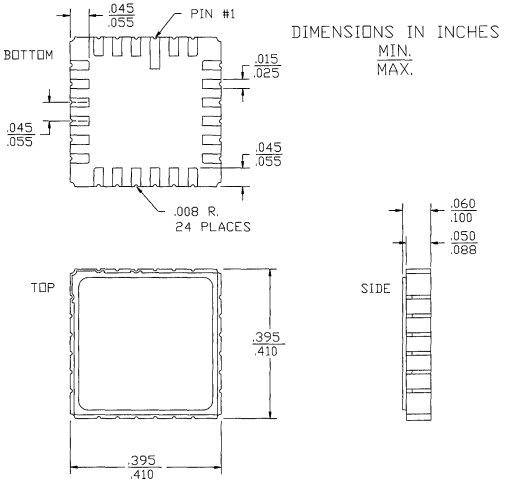


20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A

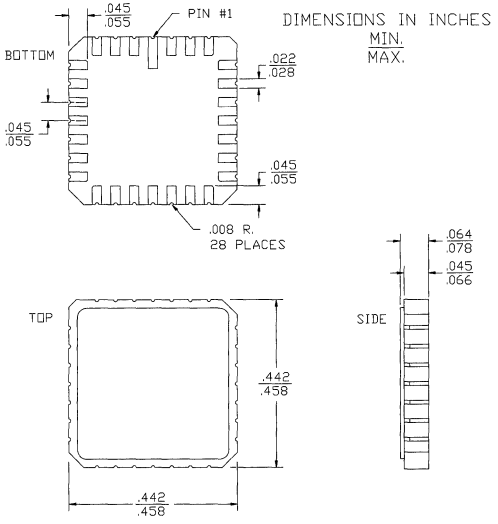


Ceramic Leadless Chip Carriers (continued)

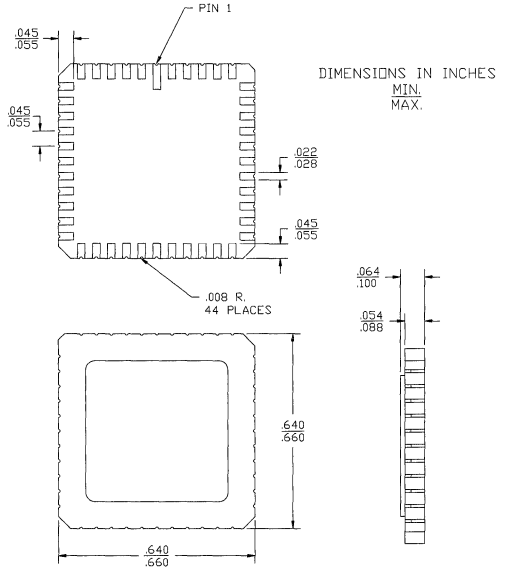
24-Square Leadless Chip Carrier L63



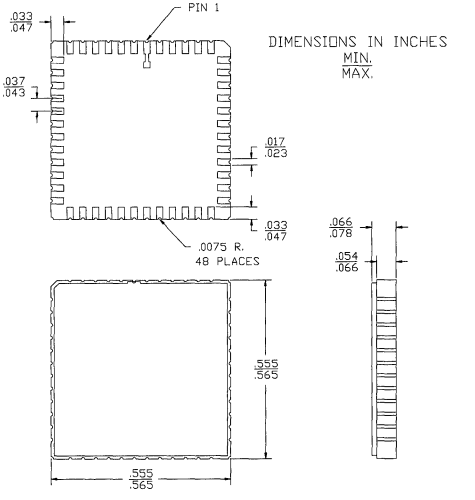
28-Square Leadless Chip Carrier L64
MIL–STD–1835 C–4



44-Square Leadless Chip Carrier L67
MIL–STD–1835 C–5

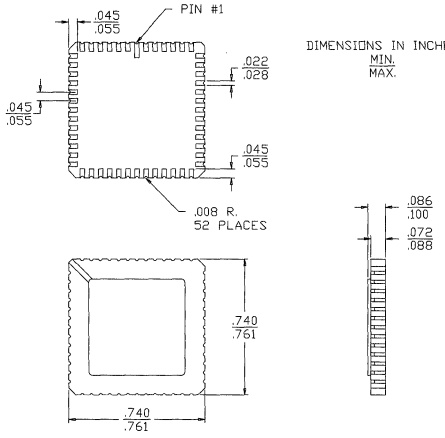


48-Square Leadless Chip Carrier L68

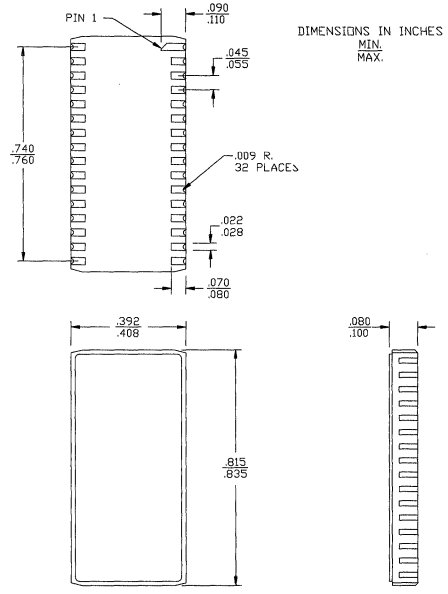


Ceramic Leadless Chip Carriers (continued)

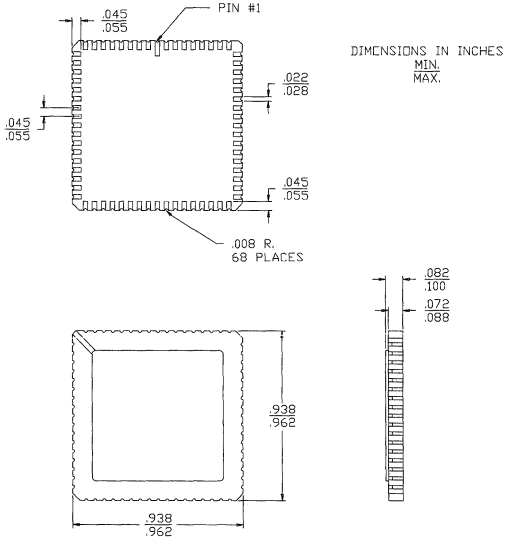
52-Square Leadless Chip Carrier L69



32-Pin Leadless Chip Carrier L75

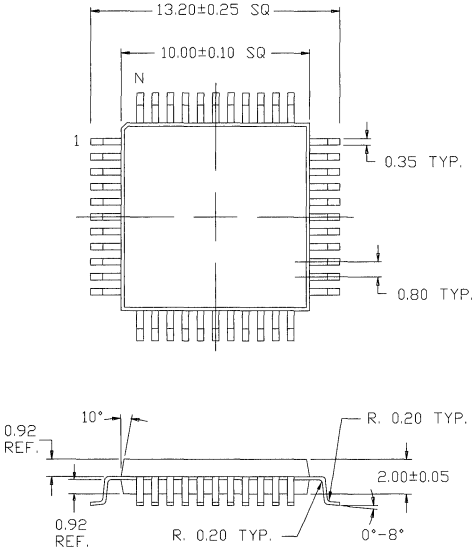


68-Square Leadless Chip Carrier L81
MIL–STD–1835 C–7

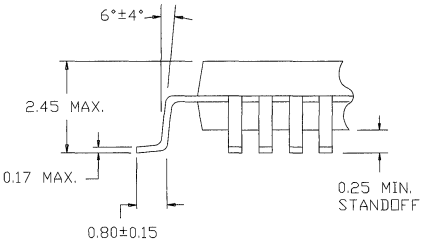


Plastic Quad Flatpacks

44-Lead Plastic Quad Flatpack N44

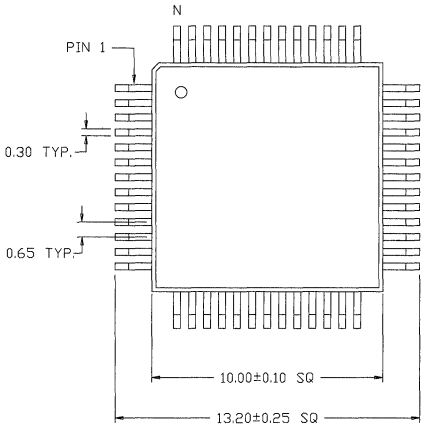


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

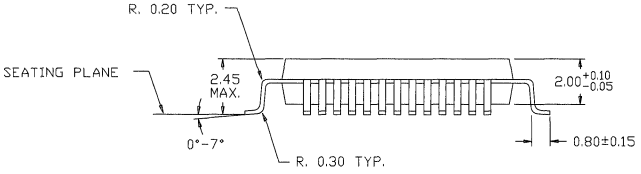


Plastic Quad Flatpacks (continued)

52-Lead Plastic Quad Flatpack N52

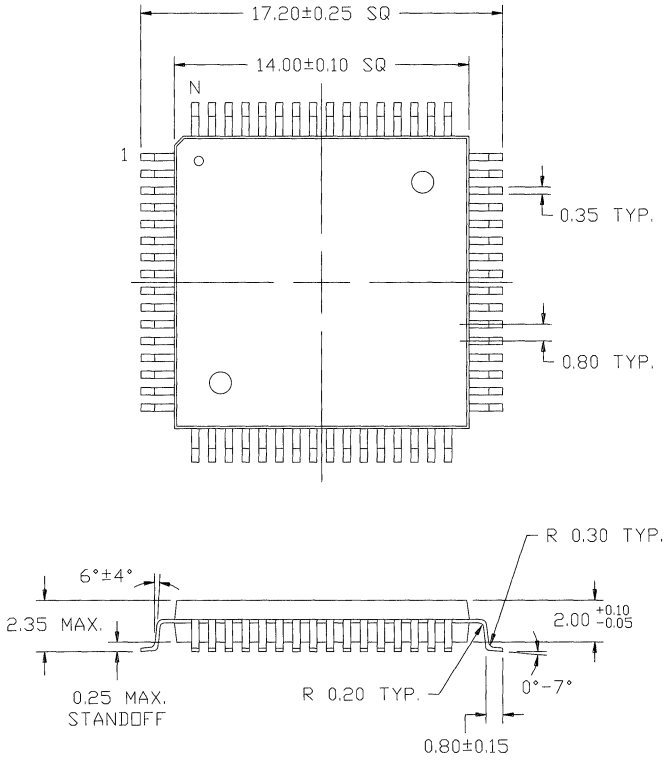


DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



Plastic Quad Flatpacks (continued)

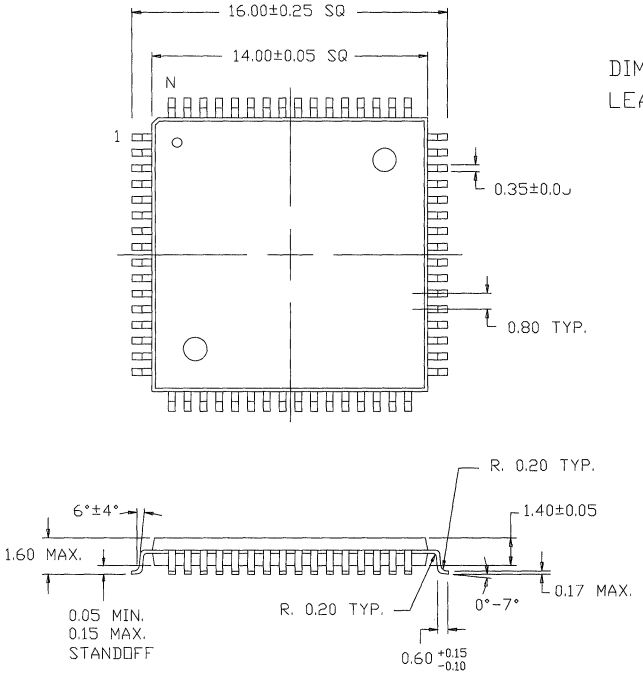
64-Lead Plastic Quad Flatpack N64



DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

Plastic Quad Flatpacks (continued)

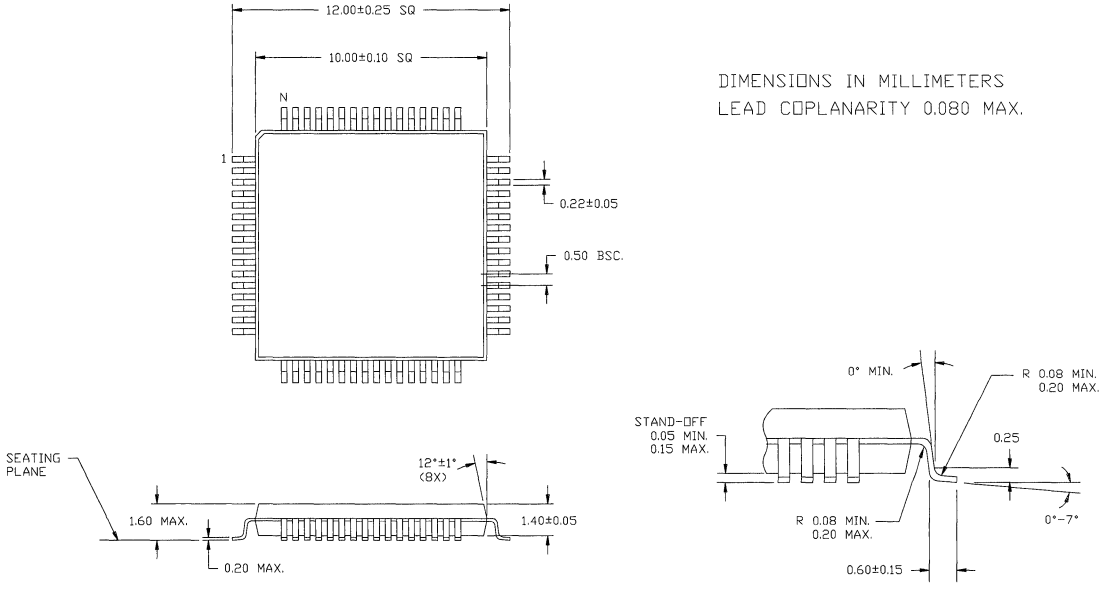
64-Lead Plastic Thin Quad Flatpack N65



DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.100 MAX.

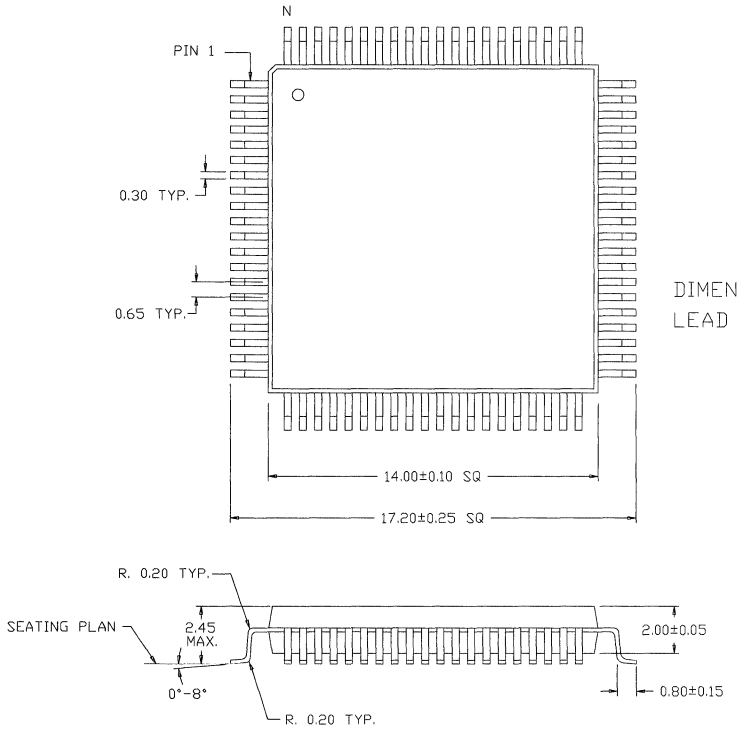
Plastic Quad Flatpacks (continued)

66-Lead Plastic Thin Quad Flatpack N66



Plastic Quad Flatpacks (continued)

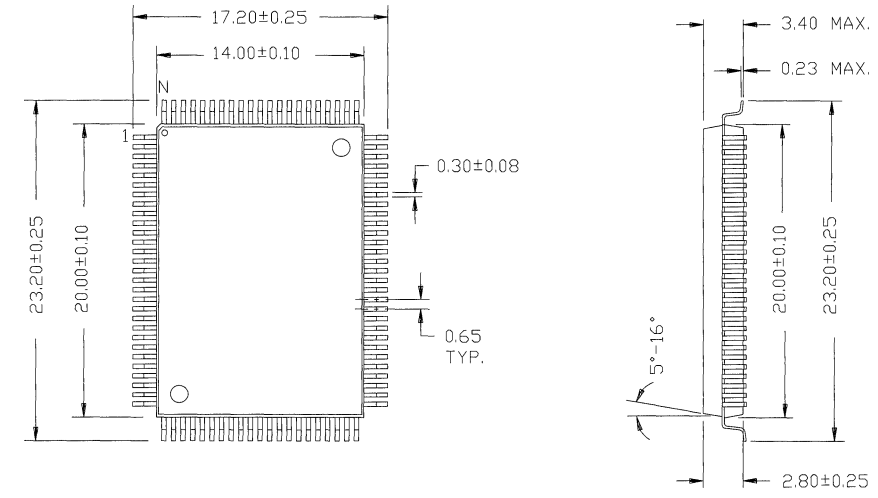
80-Lead Plastic Quad Flatpack N80

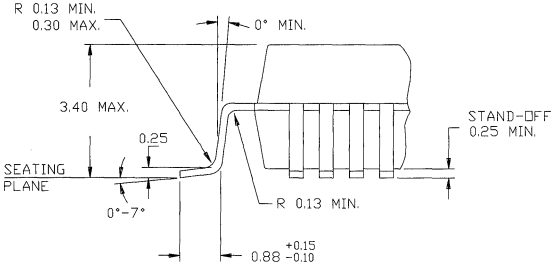


DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

Plastic Quad Flatpacks (continued)

100-Lead Plastic Quad Flatpack N100



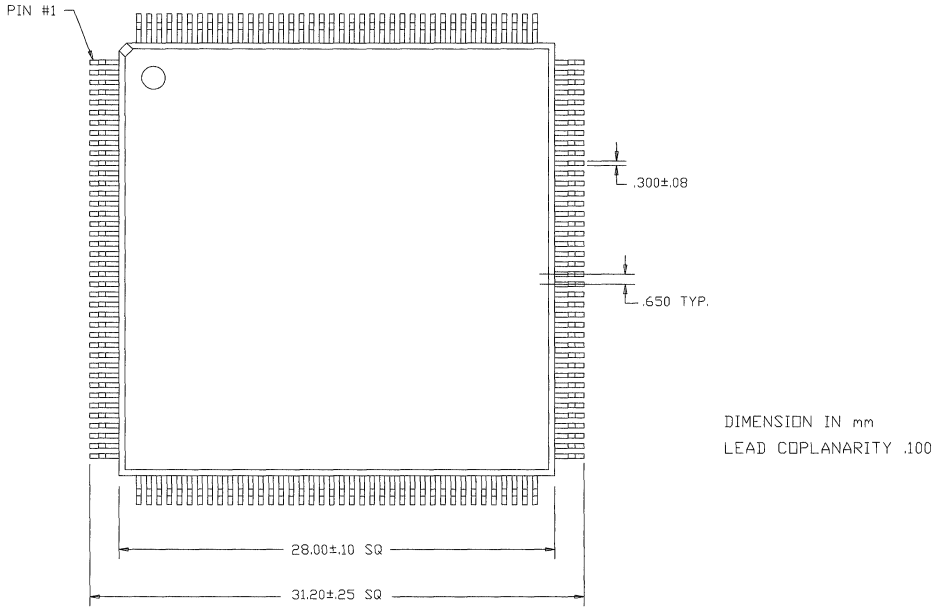


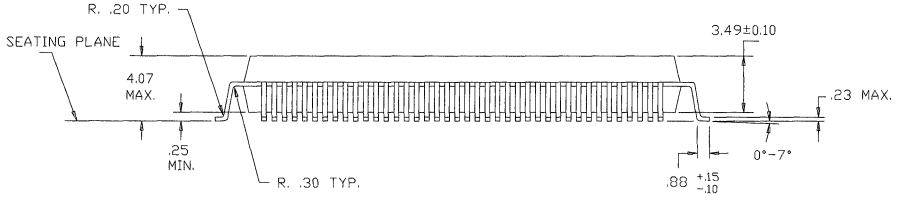
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH (14.00±0.10) AND LENGTH (20.00±0.10) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

Plastic Quad Flatpacks (continued)

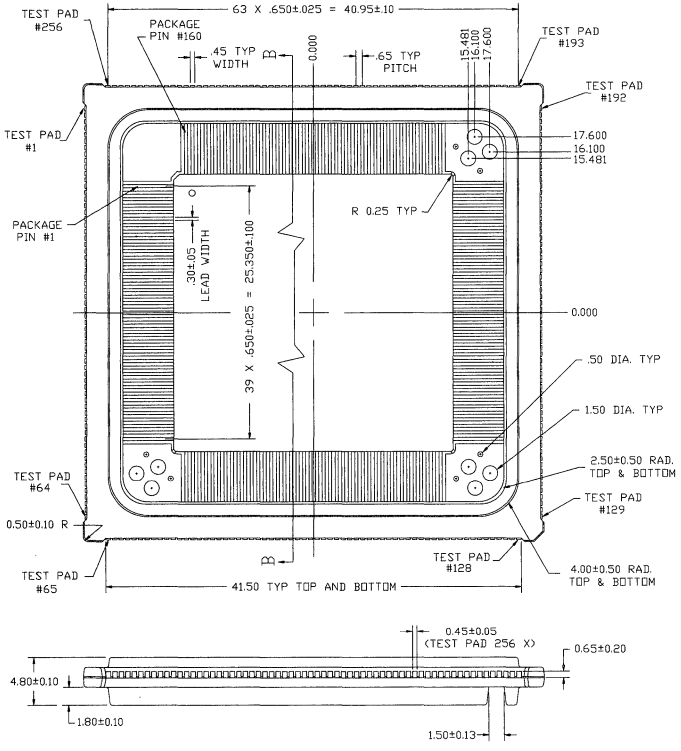
160-Lead Plastic Quad Flatpack N160

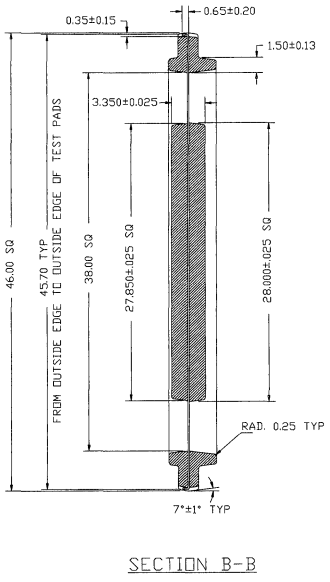




Plastic Quad Flatpacks (continued)

160-Lead Plastic Quad Flatpack with Molded Carrier Ring N161

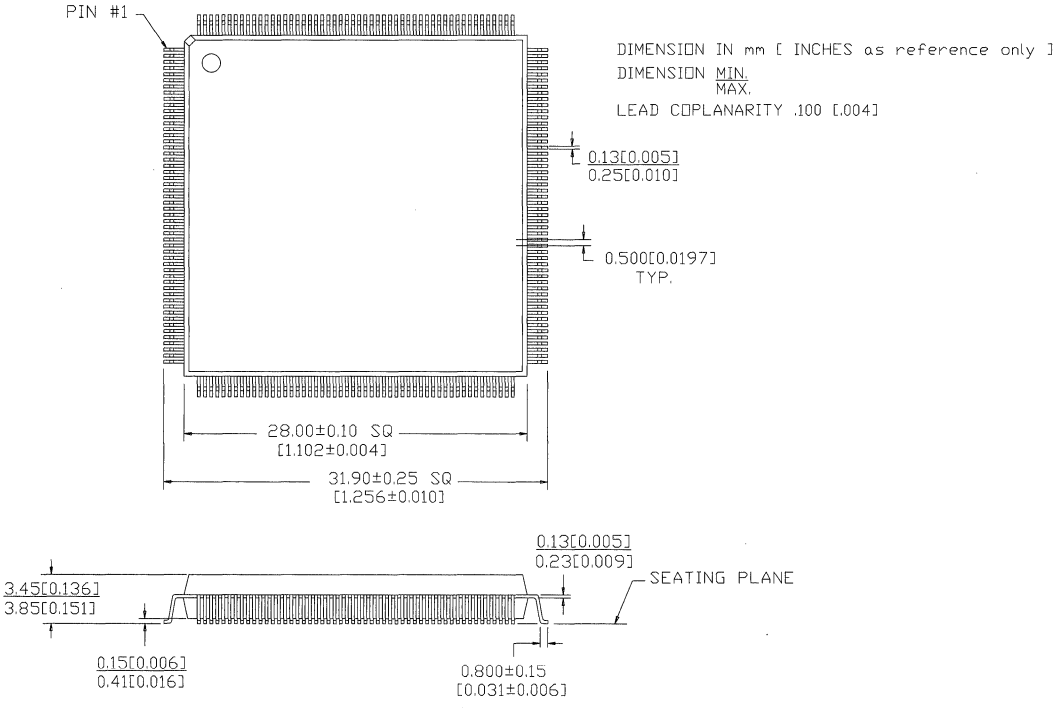




SECTION B-B

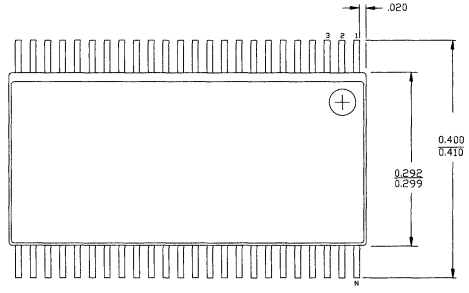
Plastic Quad Flatpacks (continued)

208-Lead Plastic Quad Flatpack N208

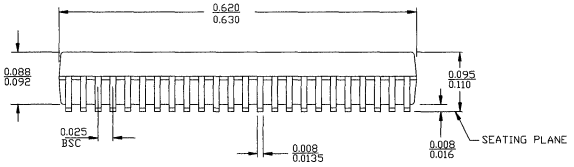


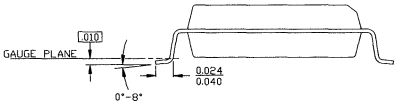
Shrunk Small Outline Packages

48-Lead Shrunk Small Outline Package O48

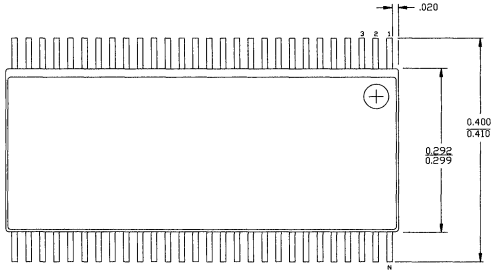


DIMENSIONS IN INCHES MIN.
MAX.

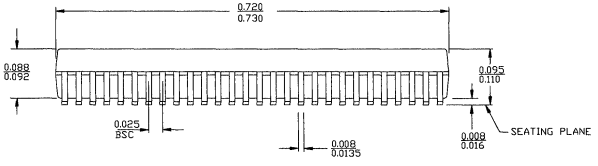


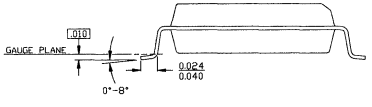


56-Lead Shrunk Small Outline Package O56



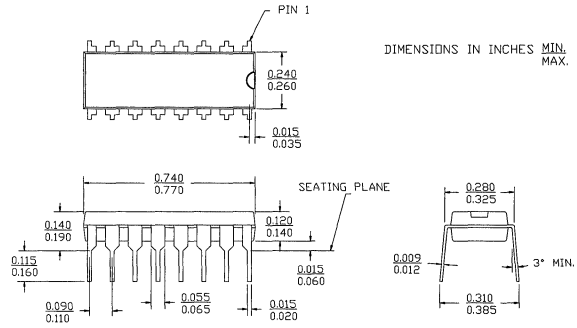
DIMENSIONS IN INCHES MIN.
MAX.



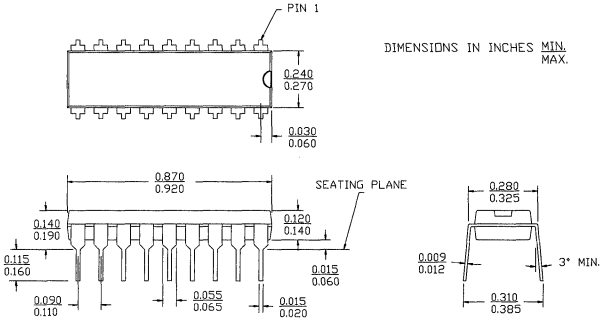


Plastic Dual-In-Line Packages

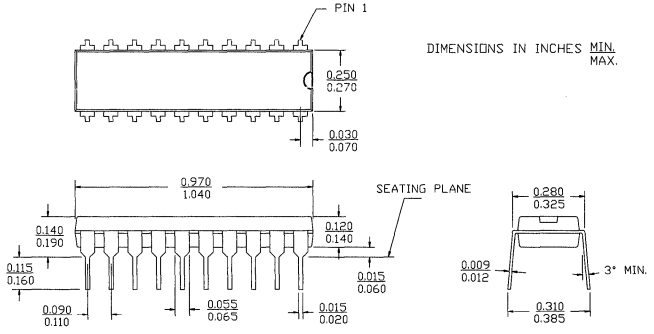
16-Lead (300-Mil) Molded DIP P1



18-Lead (300-Mil) Molded DIP P3

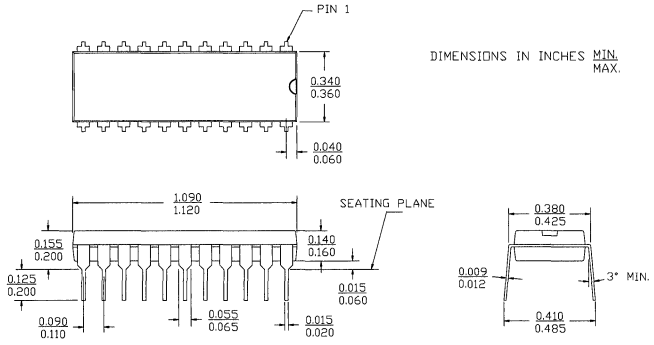


20-Lead (300-Mil) Molded DIP P5

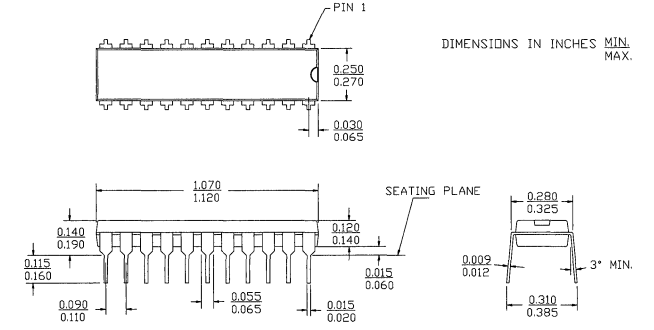


Plastic Dual-In-Line Packages (continued)

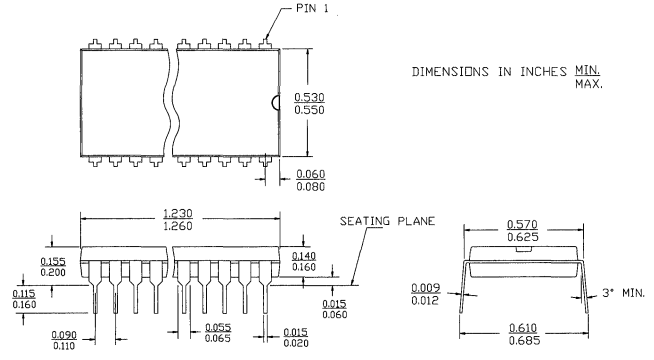
22-Lead (400-Mil) Molded DIP P7



22-Lead (300-Mil) Molded DIP P9

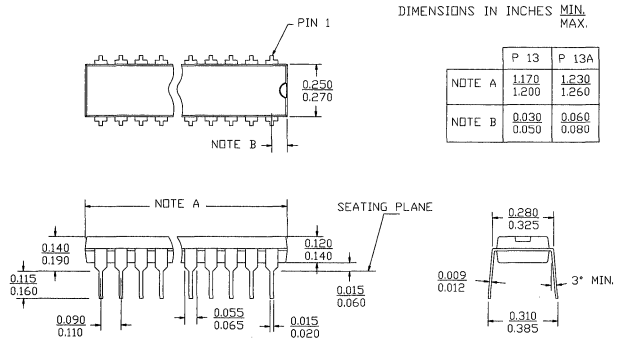


24-Lead (600-Mil) Molded DIP P11



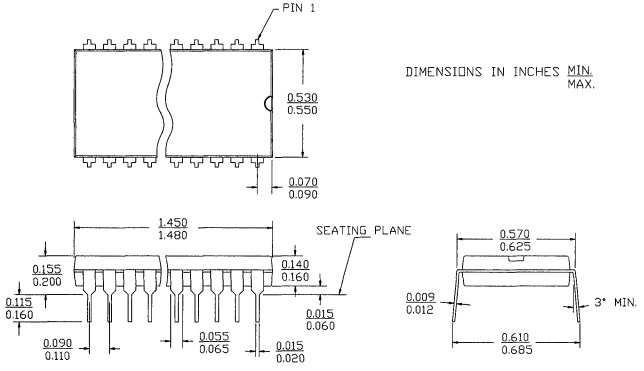
Plastic Dual-In-Line Packages (continued)

24-Lead (300-Mil) Molded DIP P13/P13A

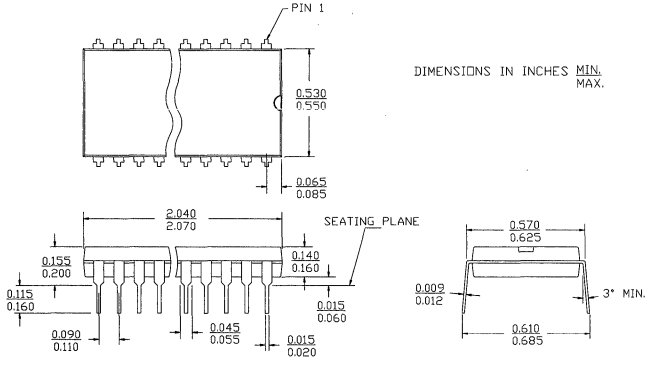


	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

28-Lead (600-Mil) Molded DIP P15

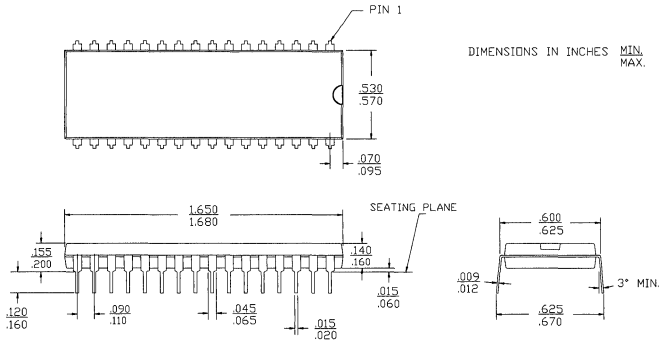


40-Lead (600-Mil) Molded DIP P17

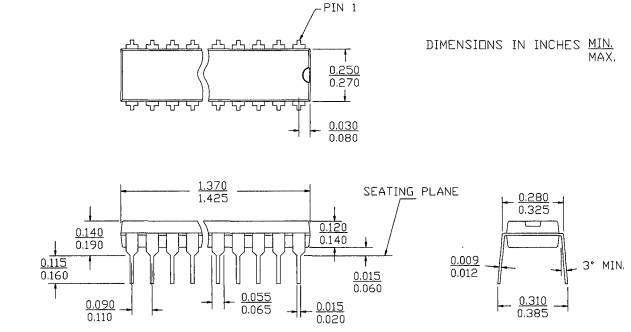


Plastic Dual-In-Line Packages (continued)

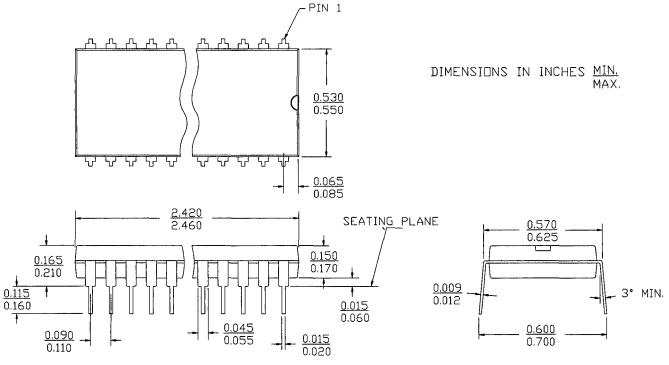
32-Lead (600-Mil) Molded DIP P19



28-Lead (300-Mil) Molded DIP P21

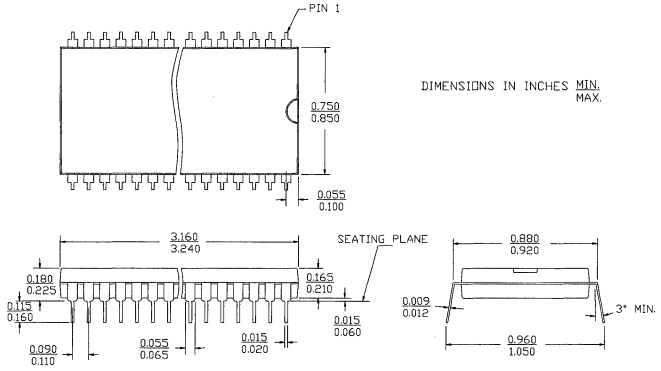


48-Lead (600-Mil) Molded DIP P25

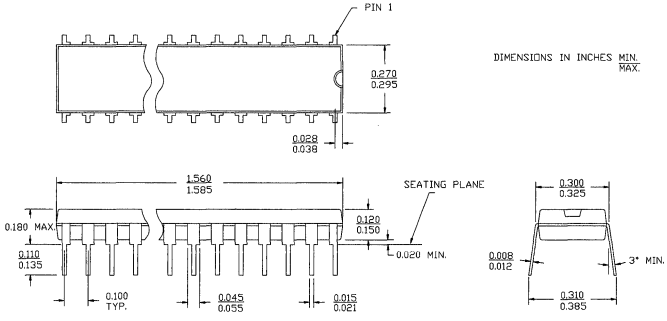


Plastic Dual-In-Line Packages (continued)

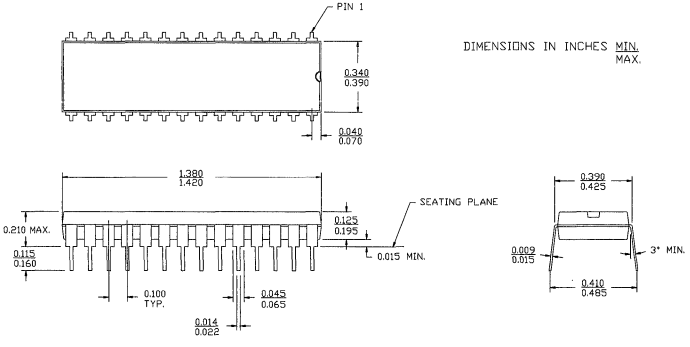
64-Lead (900-Mil) Molded DIP P29



32-Lead (300-Mil) Molded DIP P31

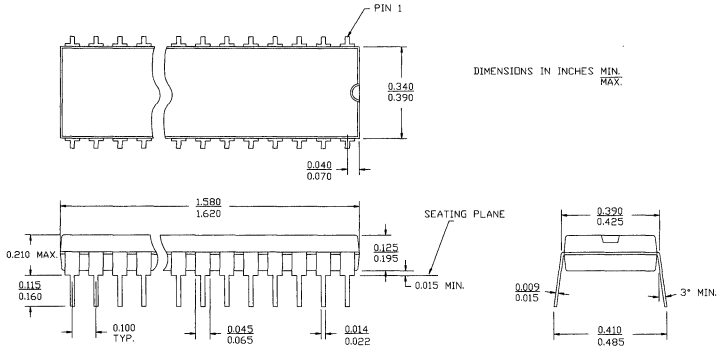


28-Lead (400-Mil) Molded DIP P41



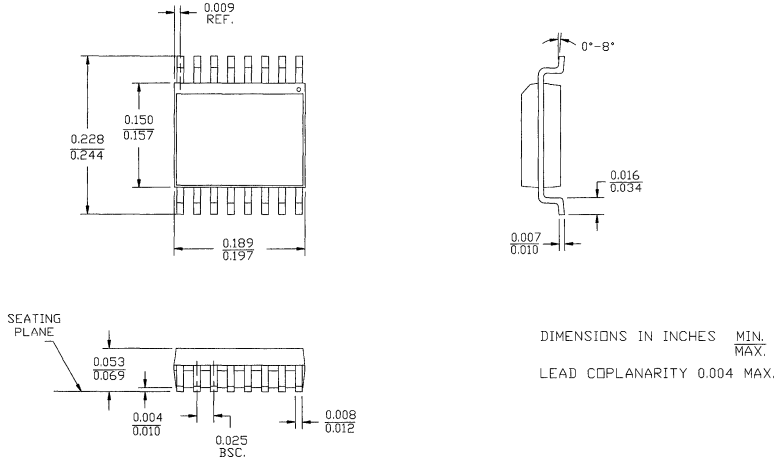
Plastic Dual-In-Line Packages (continued)

32-Lead (400-Mil) Molded DIP P43



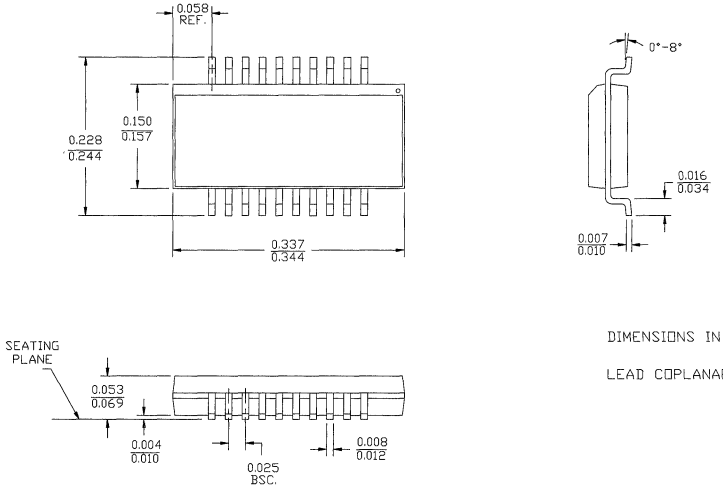
Quarter Size Outline Packages

16-Lead Quarter Size Outline Q1



Quarter Size Outline Packages

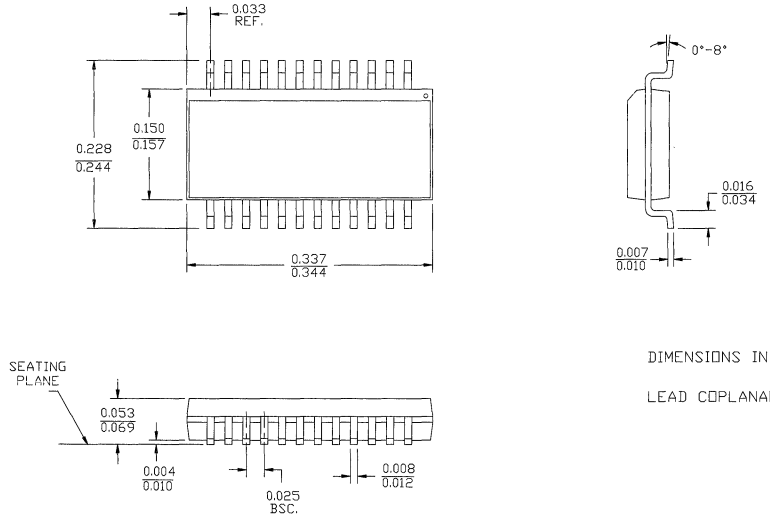
20-Lead Quarter Size Outline Q5



DIMENSIONS IN INCHES MIN. / MAX.

LEAD COPLANARITY 0.004 MAX.

24-Lead Quarter Size Outline Q13

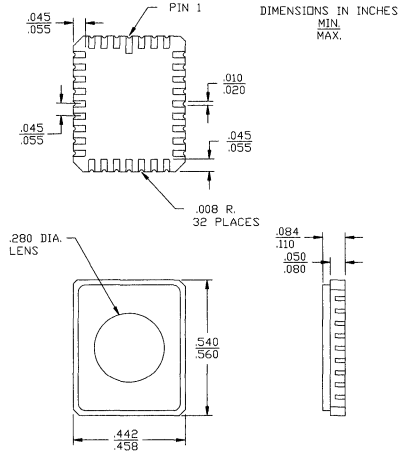


DIMENSIONS IN INCHES MIN. / MAX.

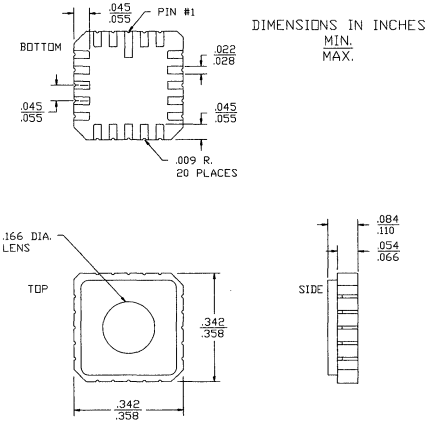
LEAD COPLANARITY 0.004 MAX.

Ceramic Windowed Leadless Chip Carriers

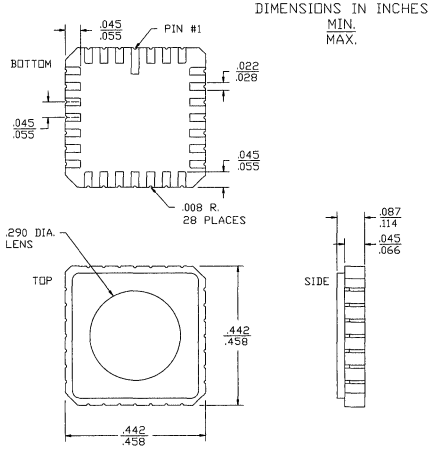
32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL–STD–1835 C–12



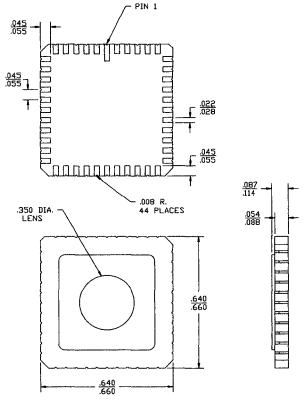
20-Pin Windowed Square Leadless Chip Carrier Q61
MIL–STD–1835 C–2A



28-Pin Windowed Leadless Chip Carrier Q64
MIL–STD–1835 C–4

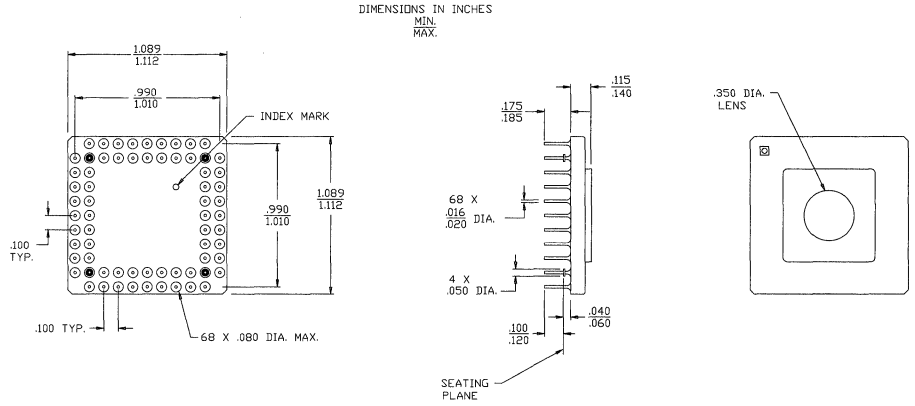


44-Pin Windowed Leadless Chip Carrier Q67
MIL–STD–1835 C–5

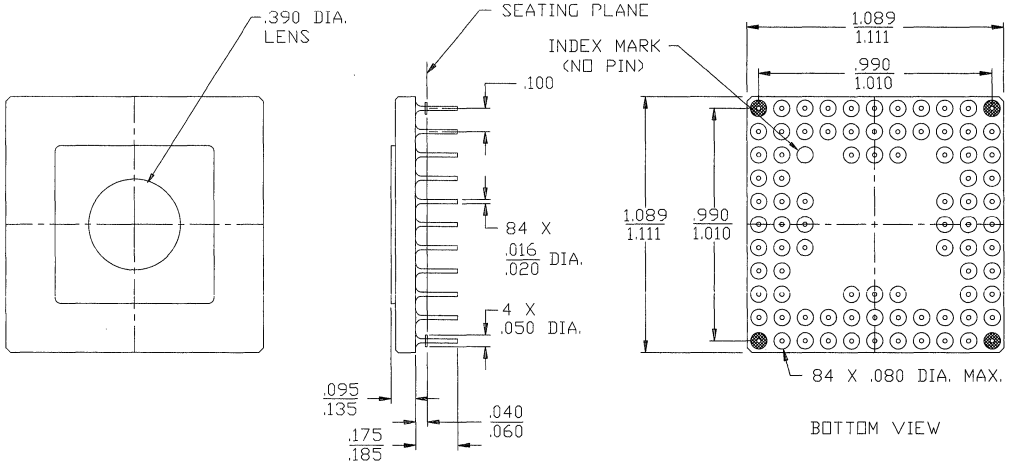


Ceramic Windowed Pin Grid Arrays

68-Pin Windowed PGA Ceramic R68

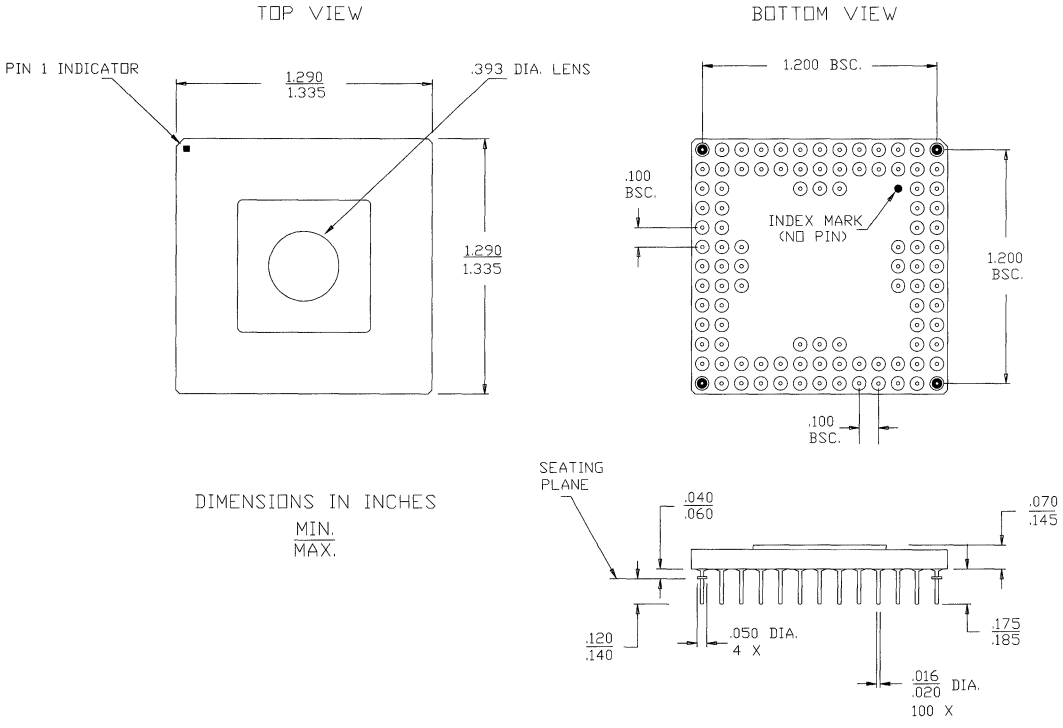


84-Lead Windowed Pin Grid Array R84



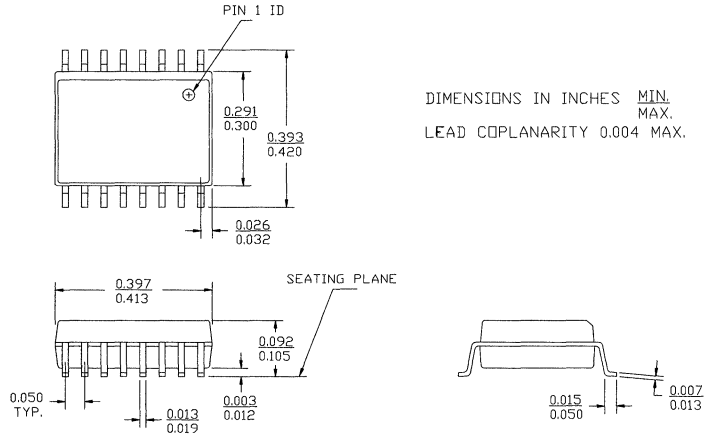
Ceramic Windowed Pin Grid Arrays (continued)

100-Pin Windowed Ceramic Pin Grid Array R100

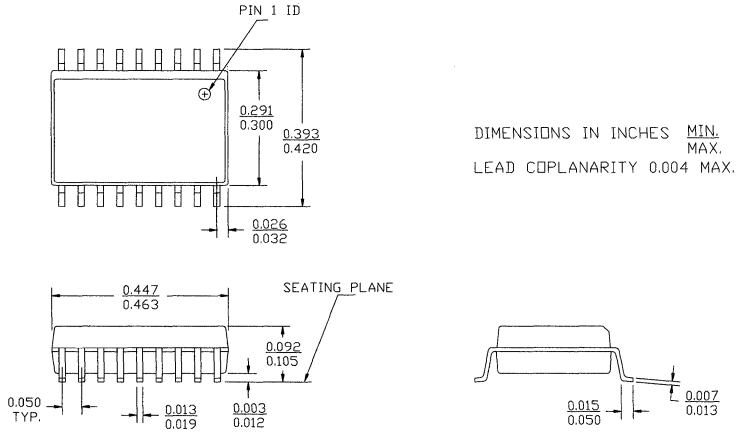


Plastic Small Outline ICs

16-Lead Molded SOIC S1

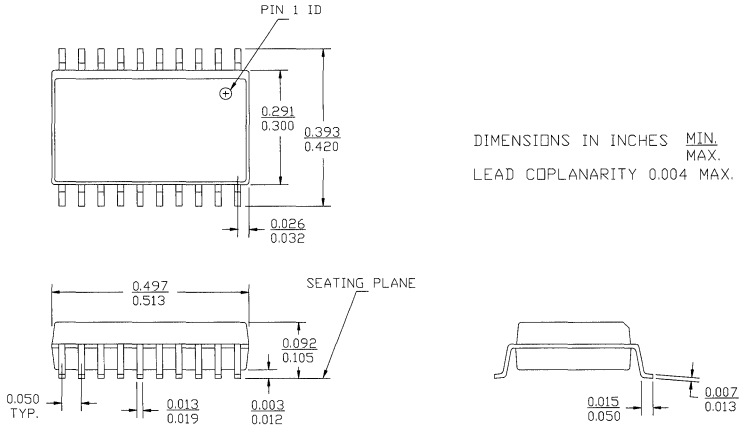


18-Lead (300-Mil) Molded SOIC S3



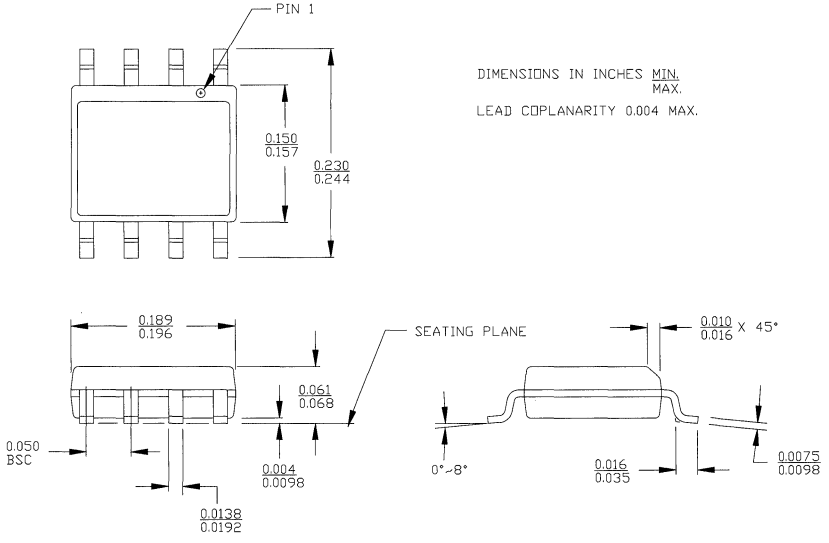
Plastic Small Outline ICs (continued)

20-Lead (300-Mil) Molded SOIC S5



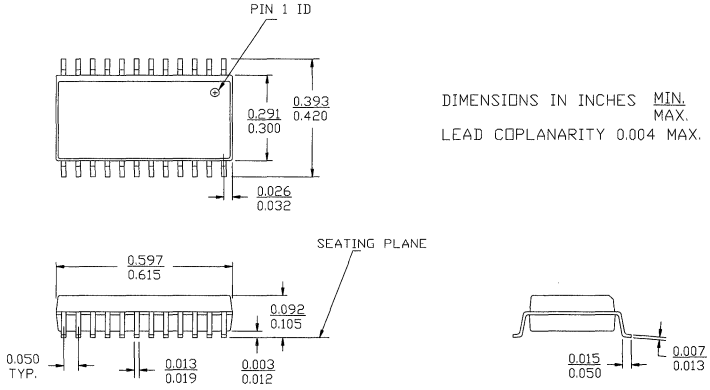
8-Lead (150-Mil) SOIC S8

PIN 1 ID IS OPTIONAL,
ROUND ON SINGLE LEADFRAME
RECTANGULAR ON MATRIX LEADFRAME

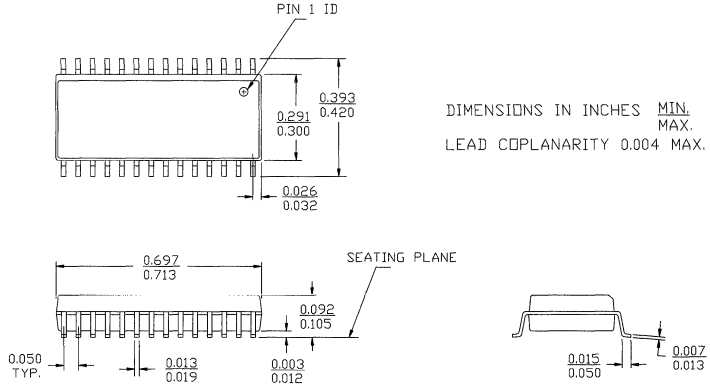


Plastic Small Outline ICs (continued)

24-Lead (300-Mil) Molded SOIC S13

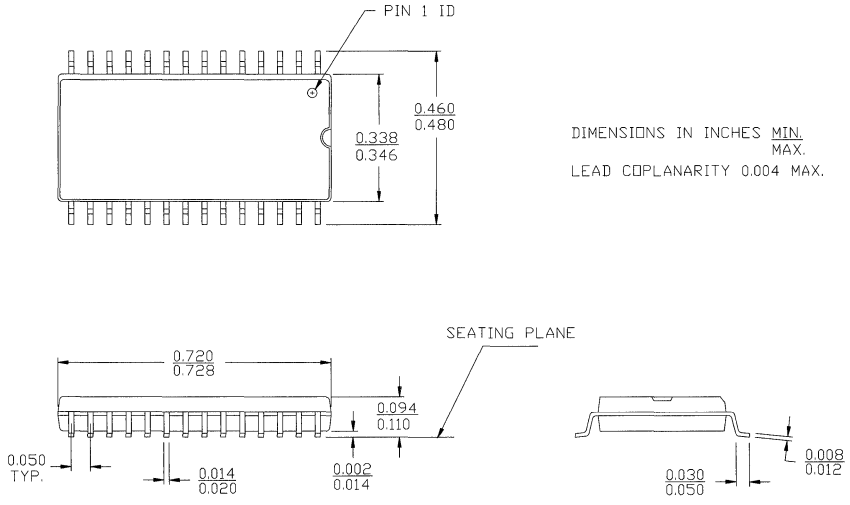


28-Lead (300-Mil) Molded SOIC S21

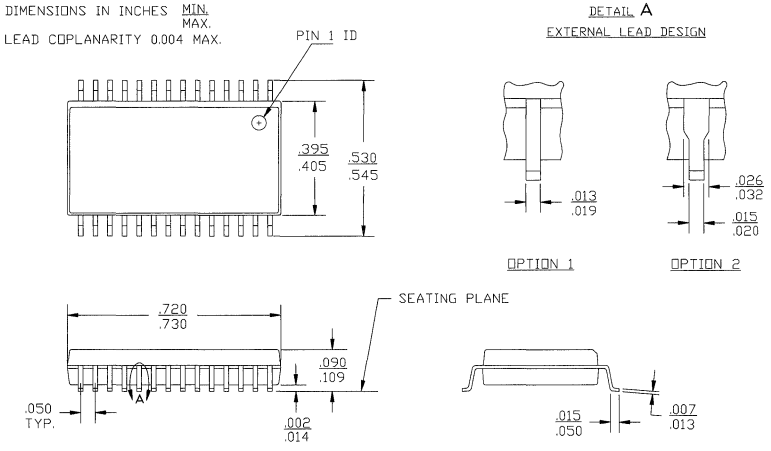


Plastic Small Outline ICs (continued)

28-Lead (330-Mil) SOIC S23

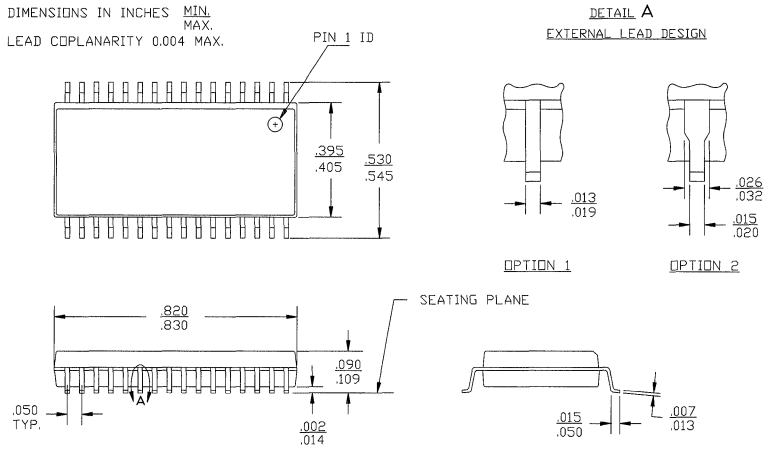


28-Lead (400-Mil) Molded SOIC S28



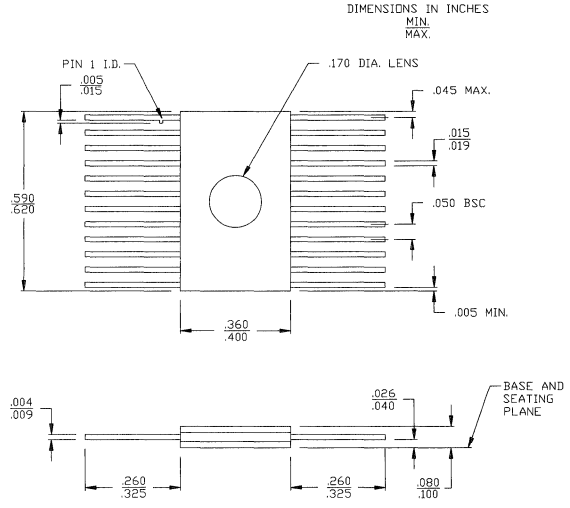
Plastic Small Outline ICs (continued)

32-Lead (400-Mil) Molded SOIC S33

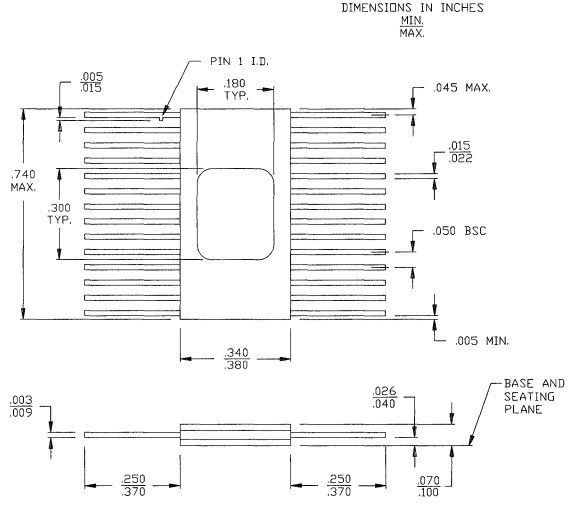


Windowed Cerpacks

24-Lead Windowed Cerpack T73

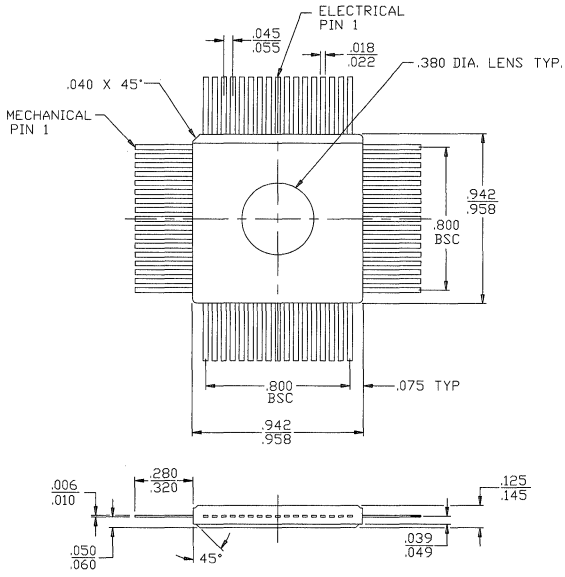


28-Lead Windowed Cerpack T74



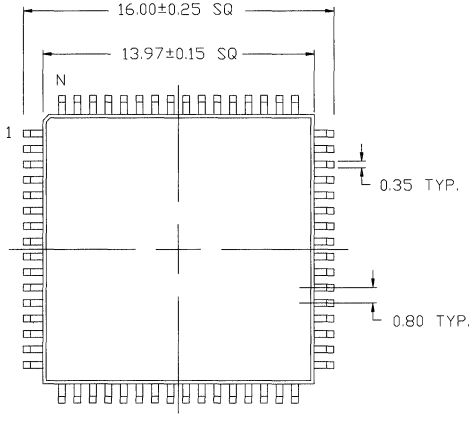
Windowed Cerpacks (continued)

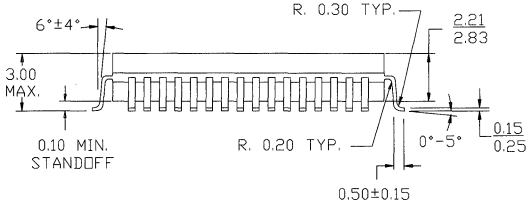
68-Lead Windowed Cerquad Flatpack T91



Ceramic Quad Flatpacks

64-Lead Ceramic Quad Flatpack (Cavity Up) U65





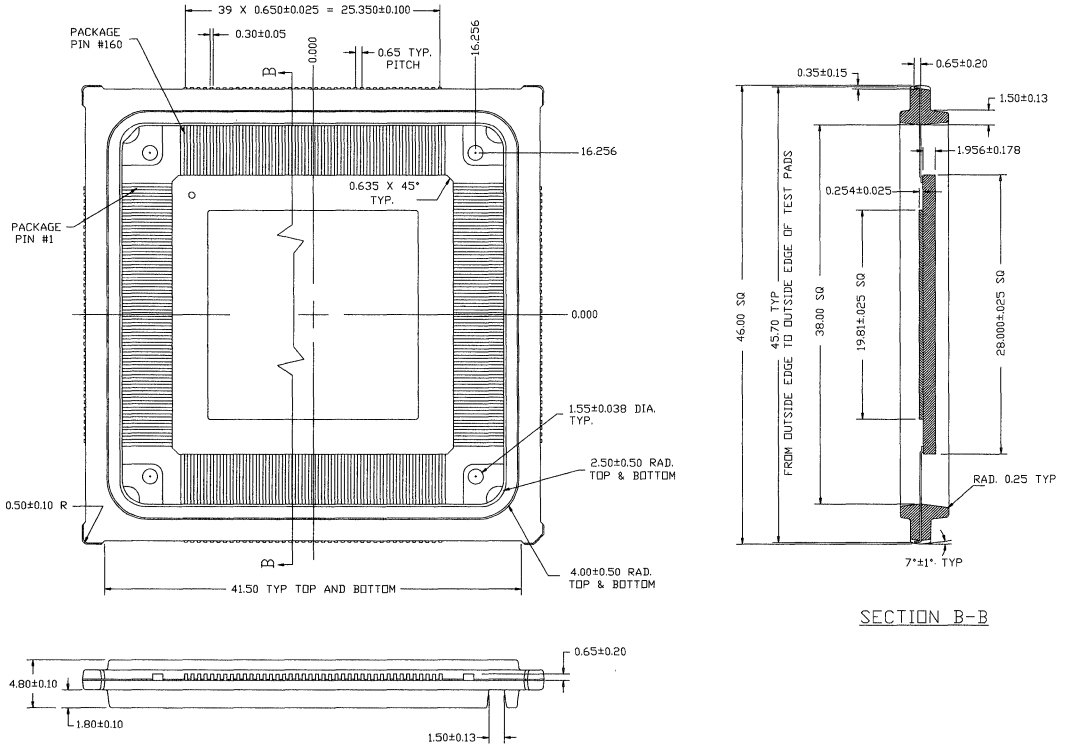
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

DIMENSION	MIN. / MAX.

14

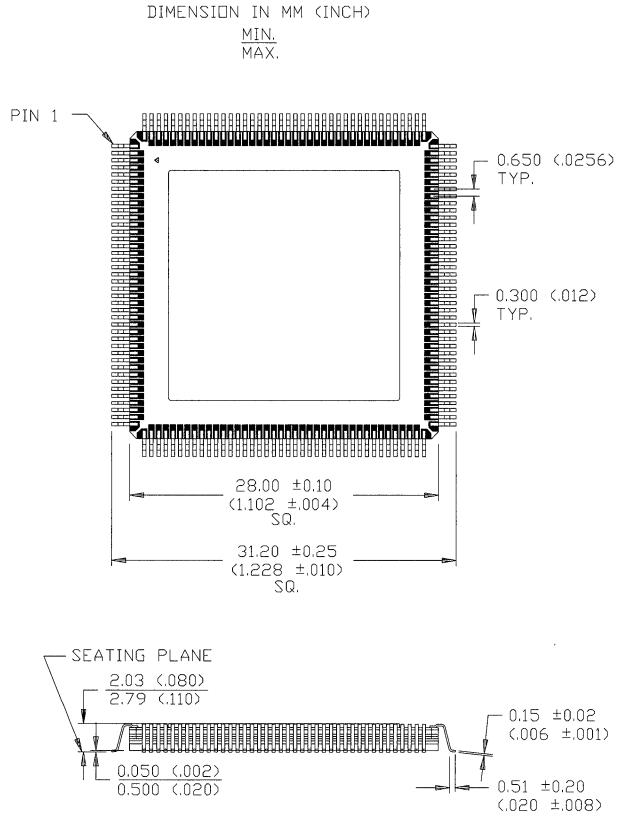
Ceramic Quad Flatpacks (continued)

160-Lead Ceramic Quad Flatpack In Ring U160



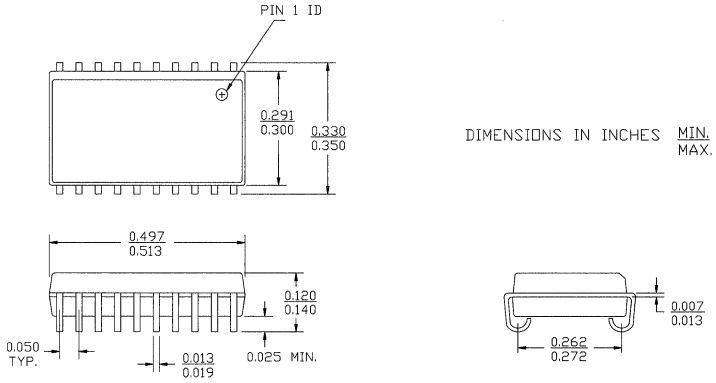
Ceramic Quad Flatpacks (continued)

160-Lead Ceramic Quad Flatpack (Cavity Up) U162

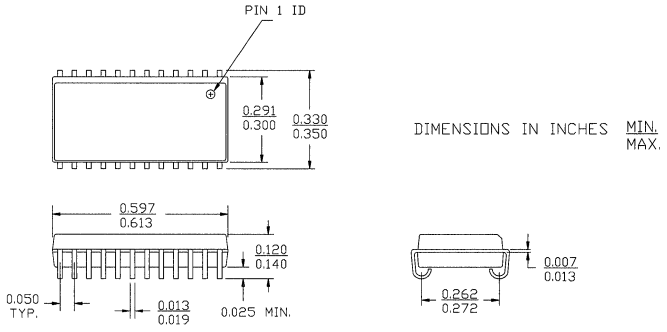


Plastic Small Outline J−Bend

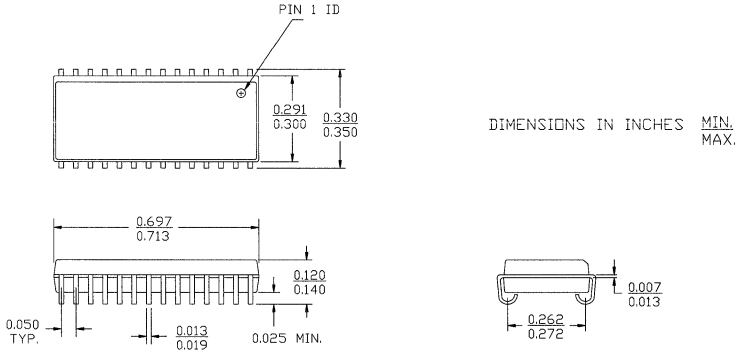
20-Lead (300-Mil) Molded SOJ V5



24-Lead (300-Mil) Molded SOJ V13

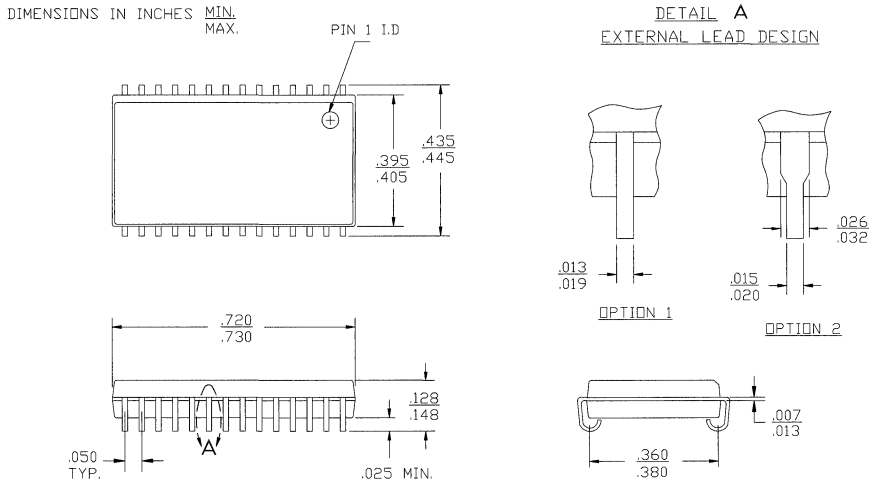


28-Lead (300-Mil) Molded SOJ V21

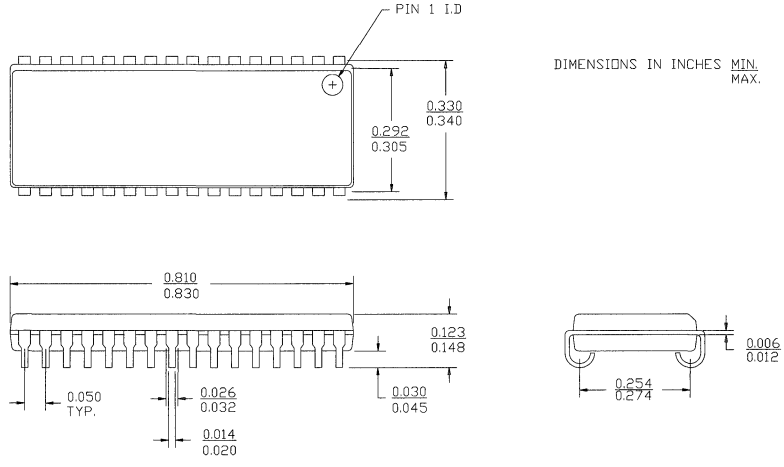


Plastic Small Outline J−Bend (continued)

28-Lead (400-Mil) Molded SOJ V28

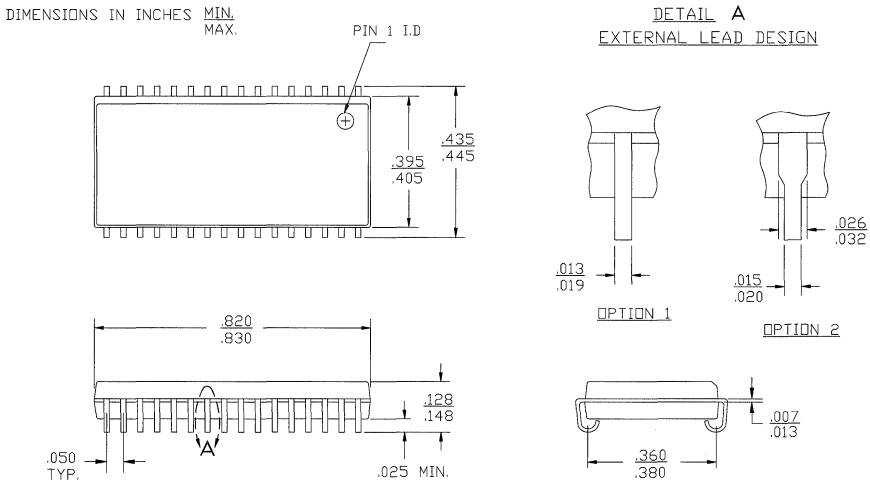


32-Lead (300-Mil) Molded SOJ V32



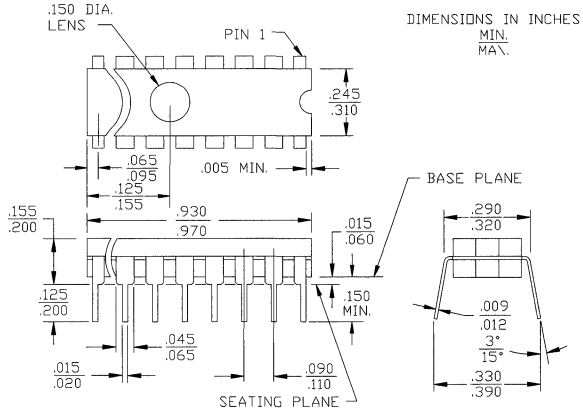
Plastic Small Outline J−Bend (continued)

32-Lead (400-Mil) Molded SOJ V33

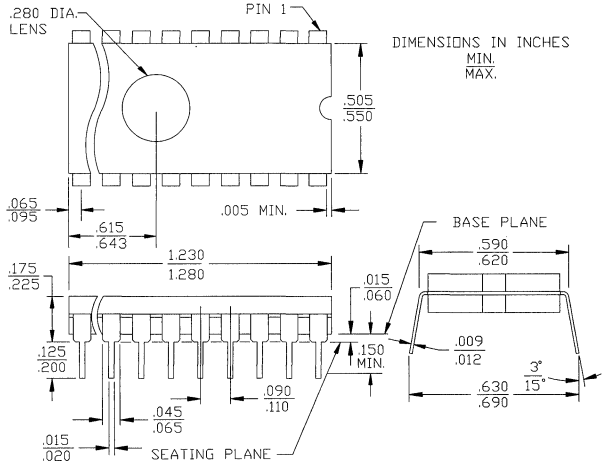


Ceramic Windowed Dual-In-Line Packages

20-Lead (300-Mil) Windowed CerDIP W6
MIL–STD–1835 D–8 Config. A



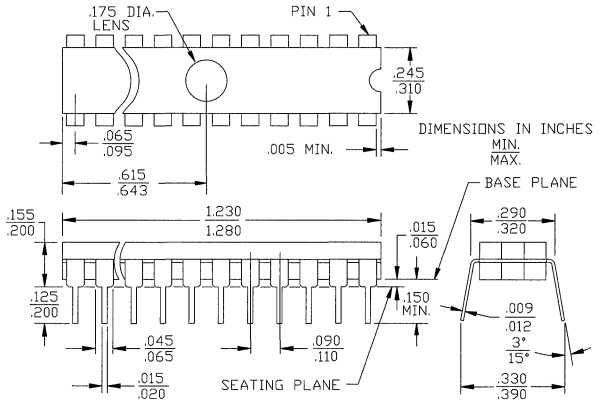
24-Lead (600-Mil) Windowed CerDIP W12
MIL–STD–1835 D–3 Config. A



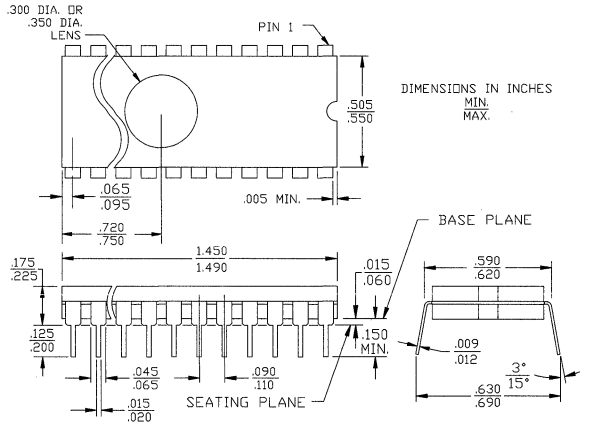
14

Ceramic Windowed Dual-In-Line Packages (continued)

24-Lead (300-Mil) Windowed CerDIP W14
MIL–STD–1835 D–9 Config. A

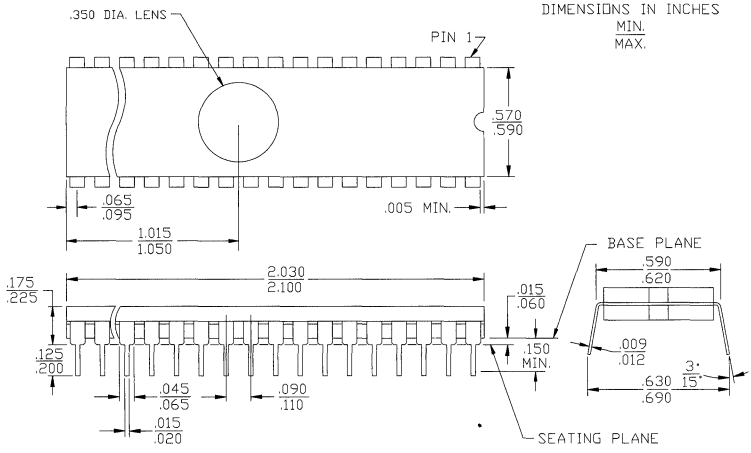


28-Lead (600-Mil) Windowed CerDIP W16
MIL–STD–1835 D–10 Config. A

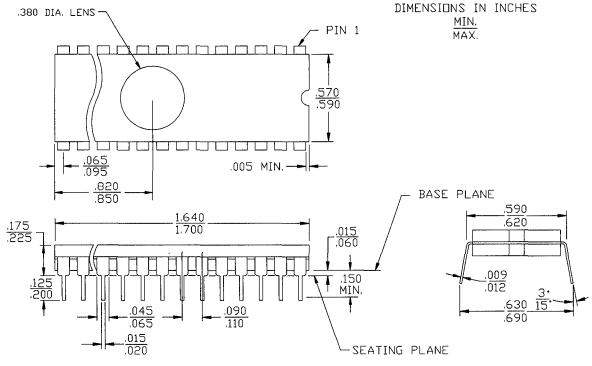


Ceramic Windowed Dual-In-Line Packages (continued)

40-Lead (600-Mil) Windowed CerDIP W18



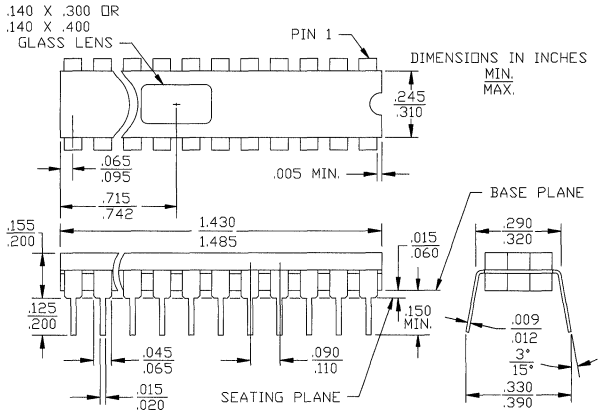
32-Lead (600-Mil) Windowed CerDIP W20



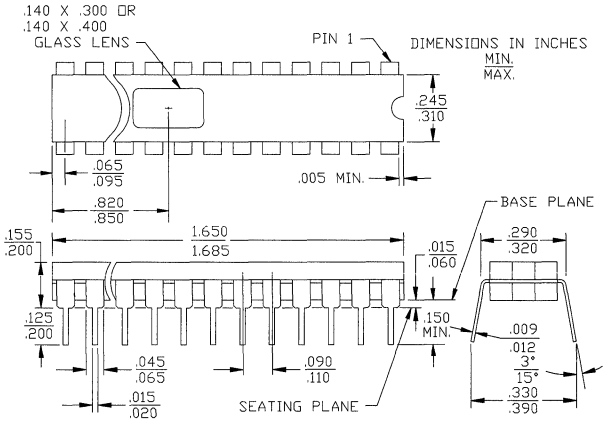
14

Ceramic Windowed Dual-In-Line Packages (continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL–STD–1835 D–15 Config. A

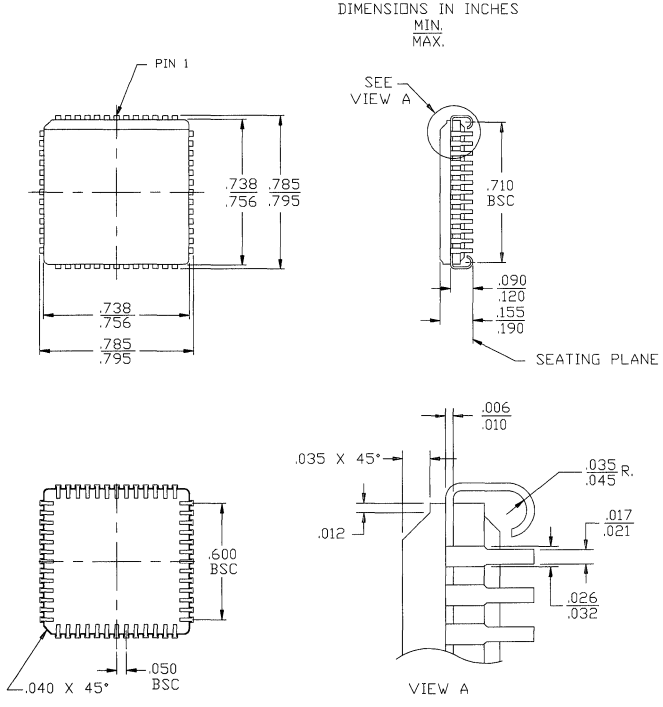


32-Lead (300-Mil) Windowed CerDIP W32



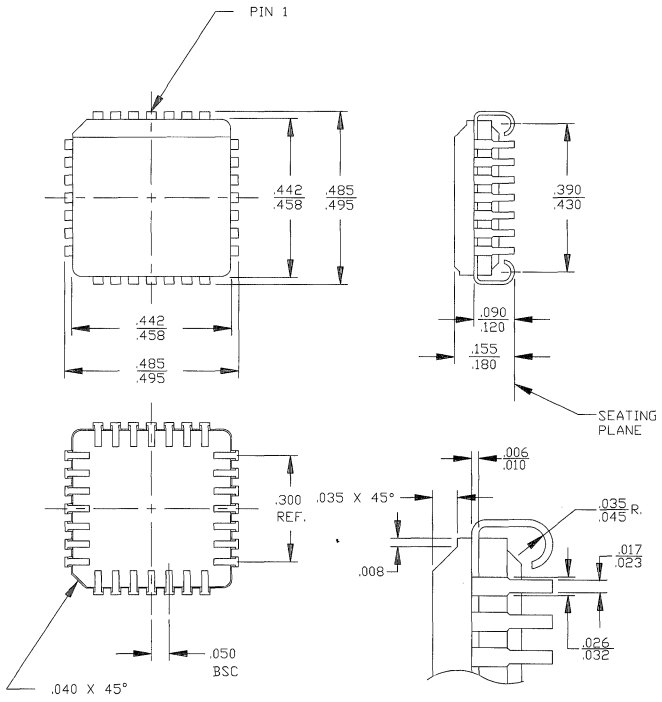
Ceramic J-Leaded Chip Carriers

52-Pin Ceramic Leaded Chip Carrier Y59



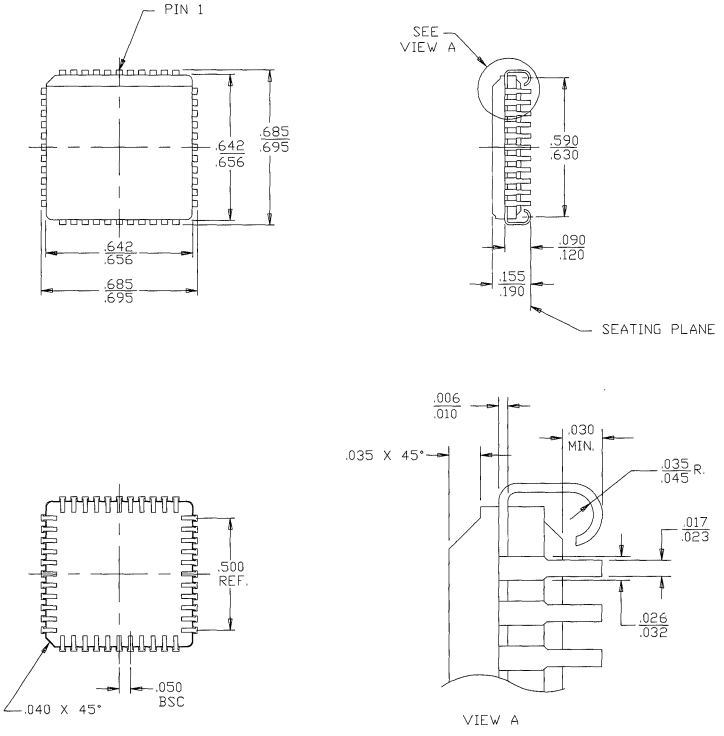
Ceramic J-Leaded Chip Carriers (continued)

28-Pin Ceramic Leaded Chip Carrier Y64



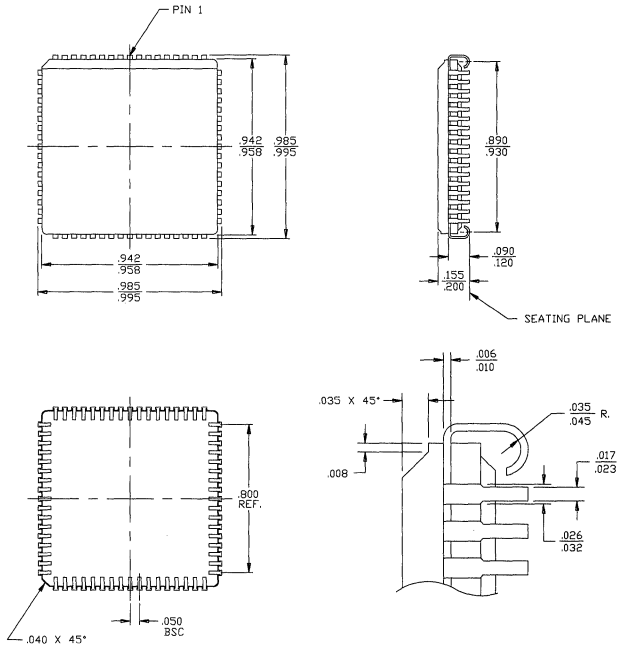
Ceramic J-Leaded Chip Carriers (continued)

44-Pin Ceramic Leaded Chip Carrier Y67



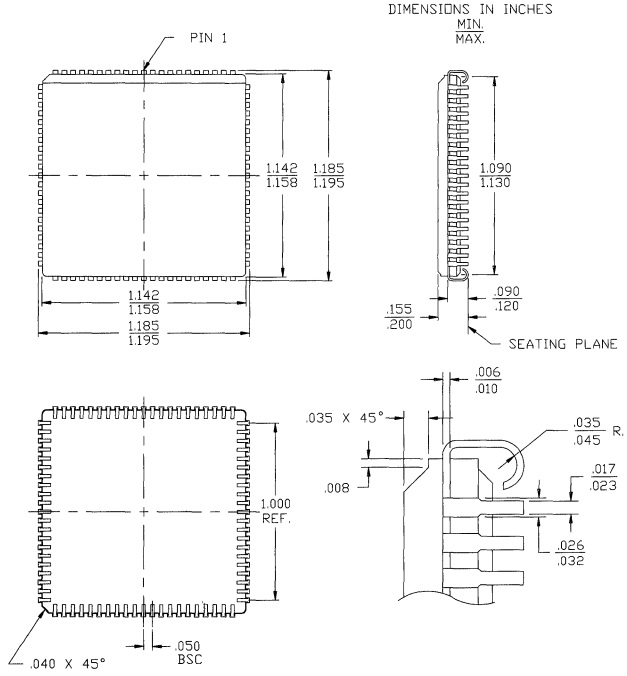
Ceramic J-Leaded Chip Carriers (continued)

68-Pin Ceramic Leaded Chip Carrier Y68



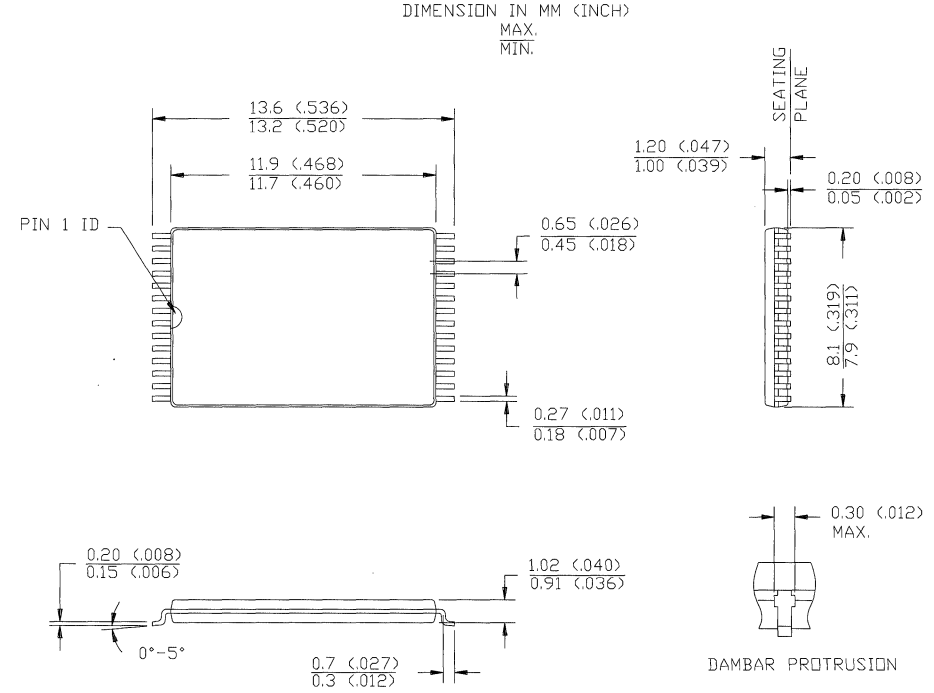
Ceramic J-Leaded Chip Carriers (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



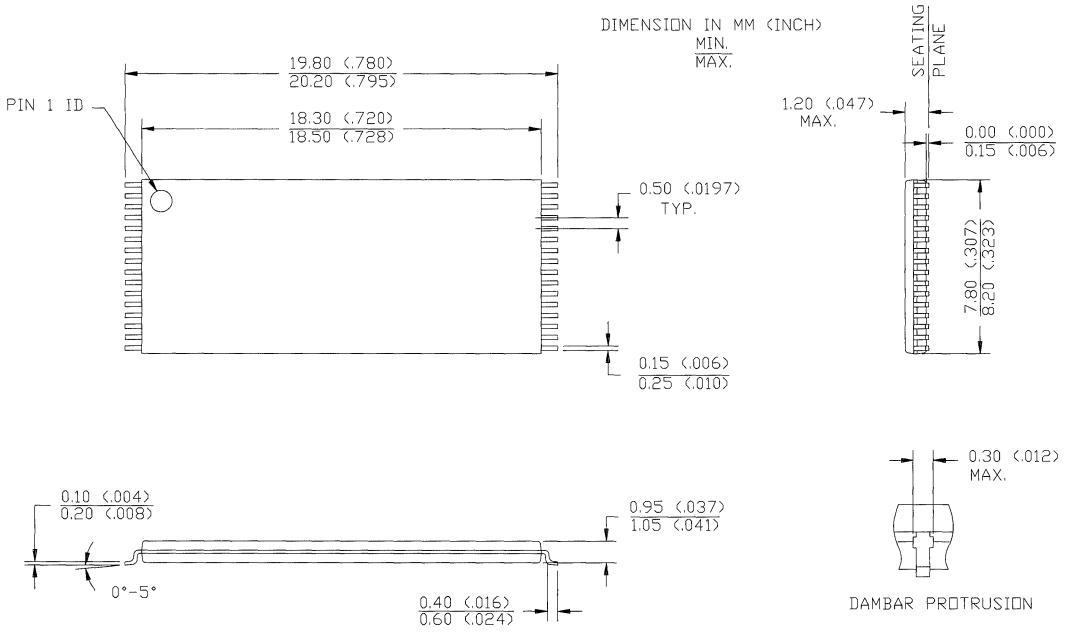
Thin Small Outline Packages

28-Lead Thin Small Outline Package Z28



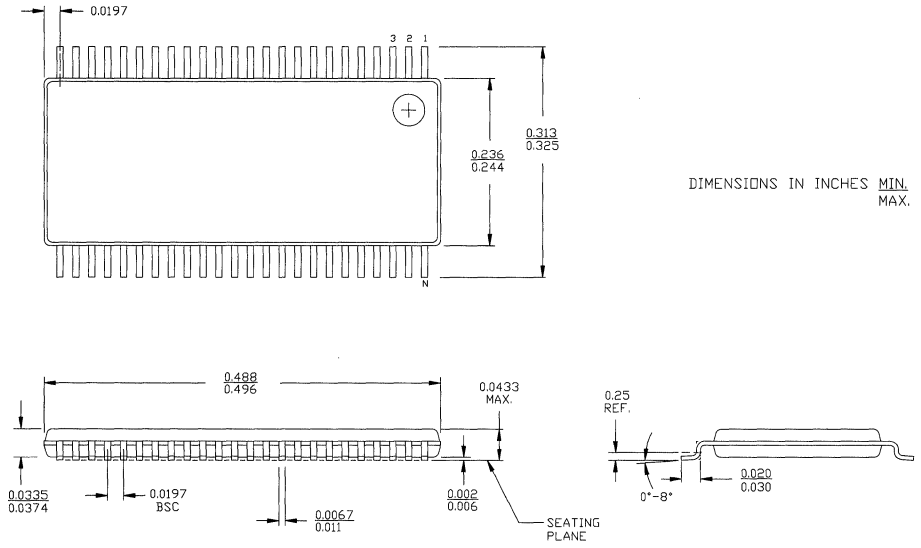
Thin Small Outline Packages (continued)

32-Lead Thin Small Outline Package Z32

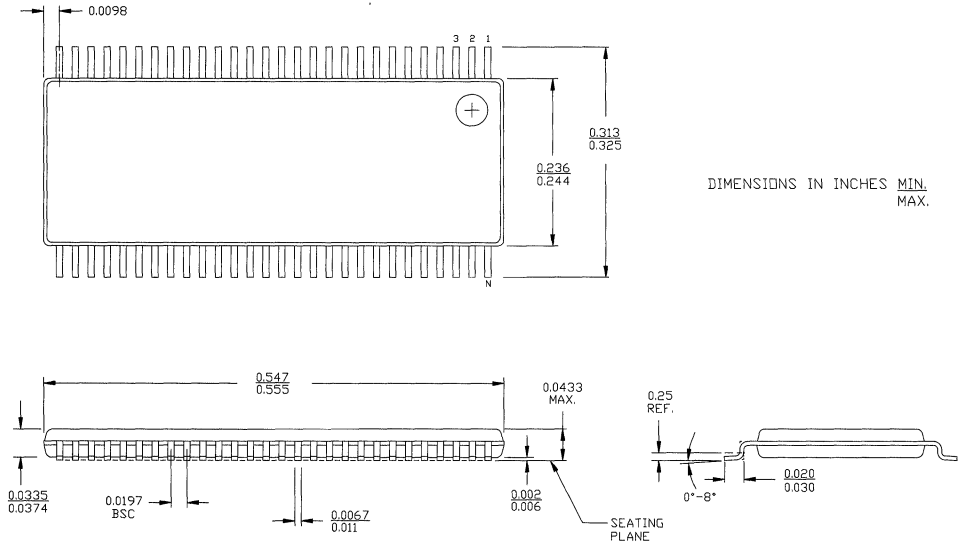


Thin Small Outline Packages (continued)

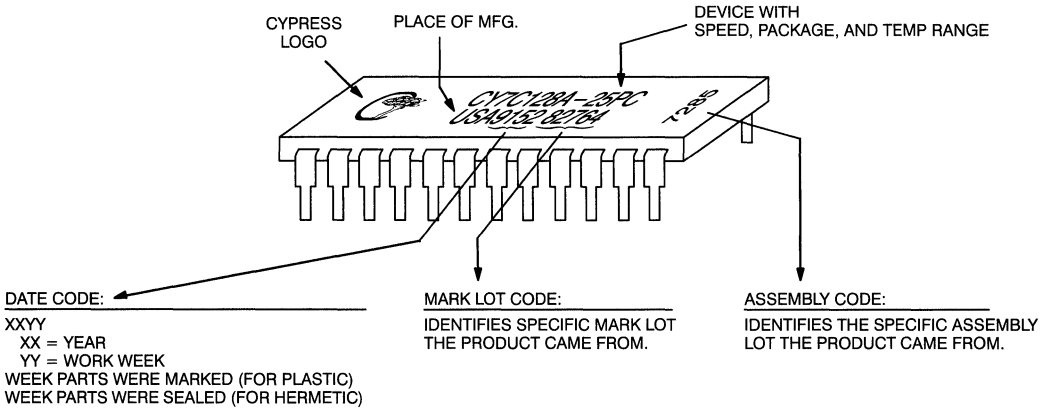
48-Lead Thin Shrunk Small Outline Package Z48



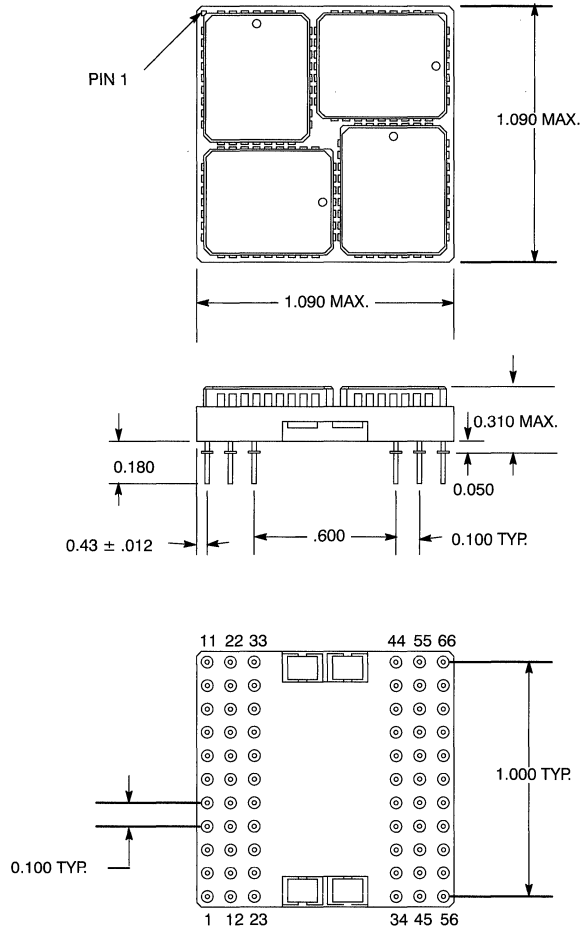
56-Lead Thin Shrunk Small Outline Package Z56



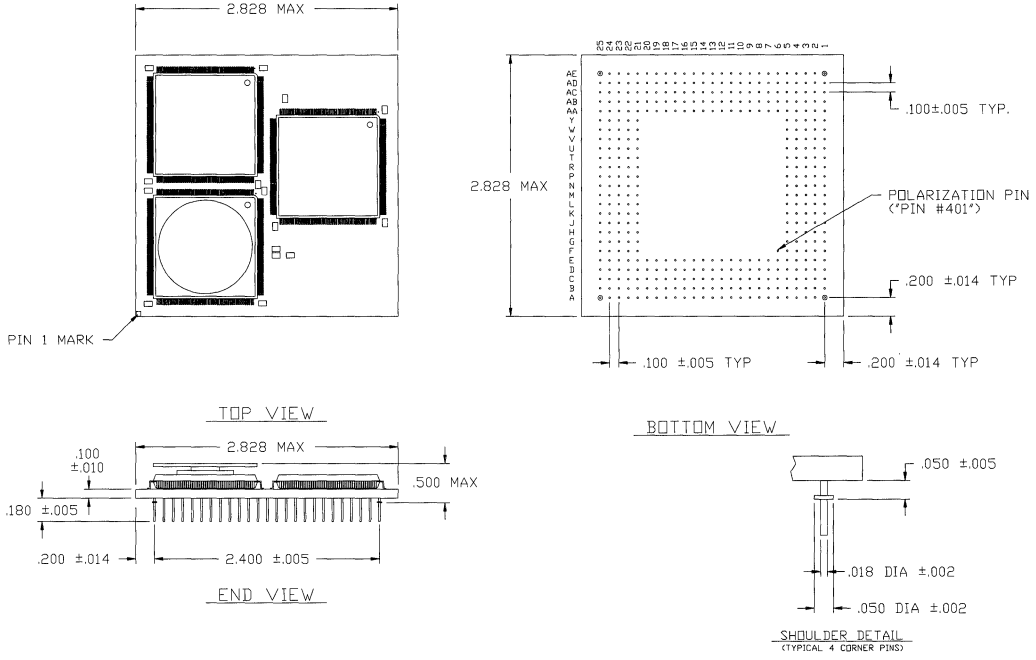
Typical Marking for DIP Packages (P and D Type)



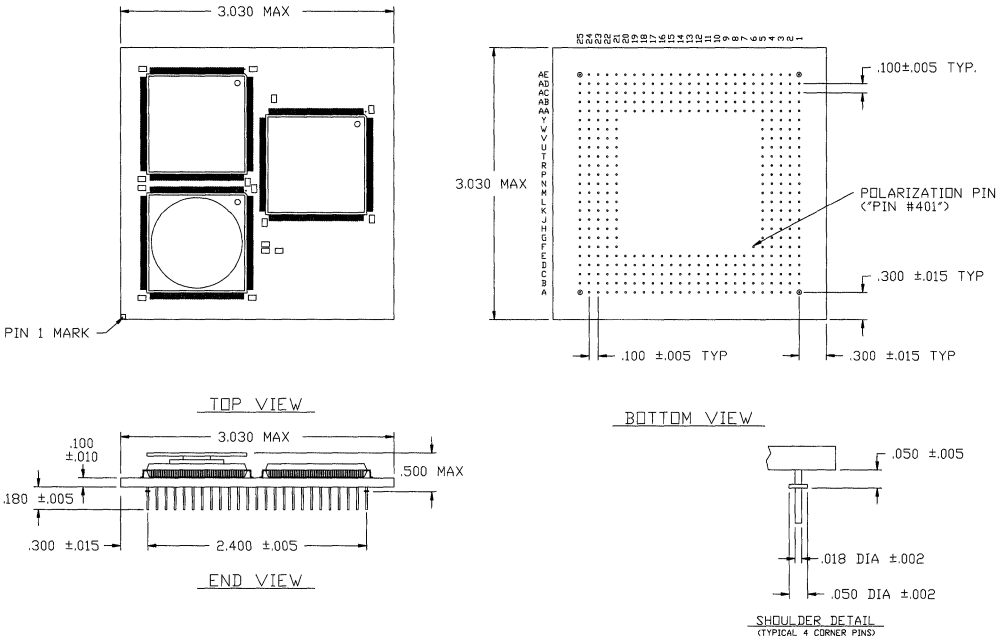
66-Pin PGA Module HG01



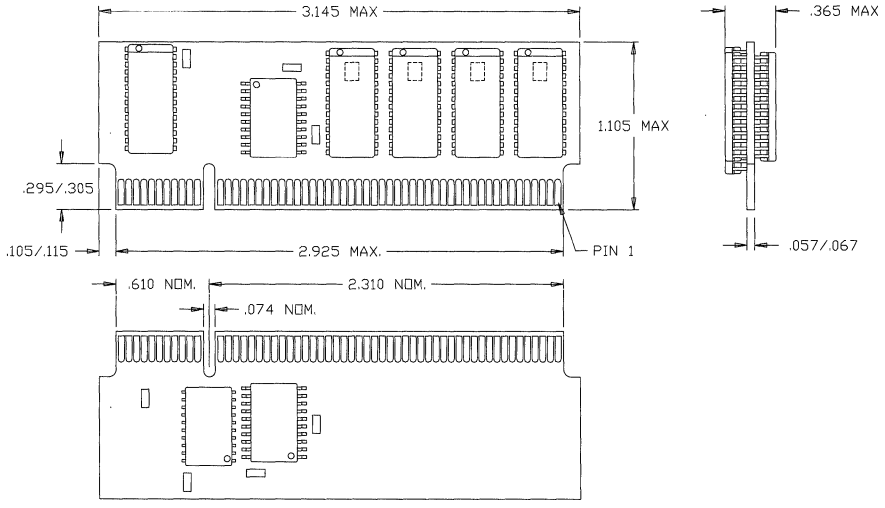
401-Pin PGA Module HG02



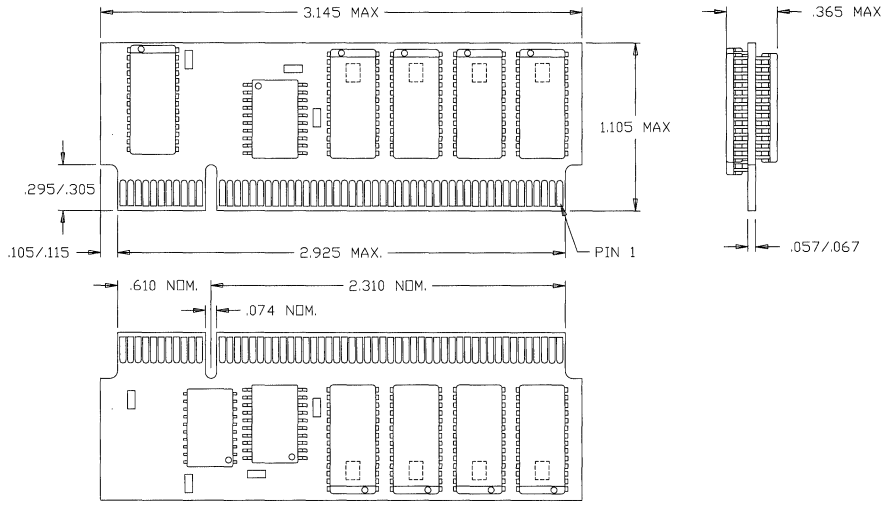
401-Pin PGA Module HG03



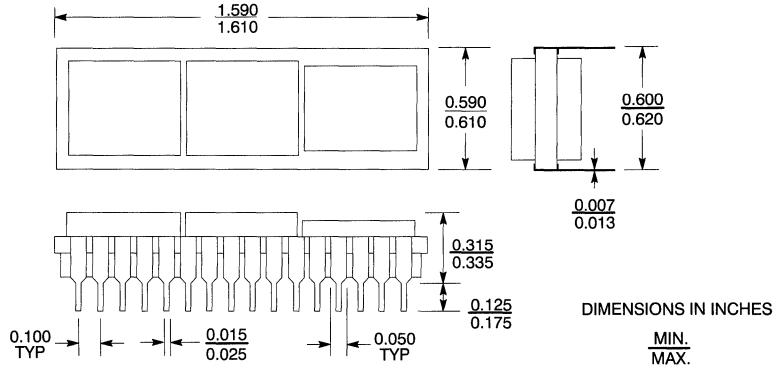
112-Pin Dual-Readout SIMM PB17



112-Pin Dual-Readout SIMM PB18



32-Pin DIP Module PD02



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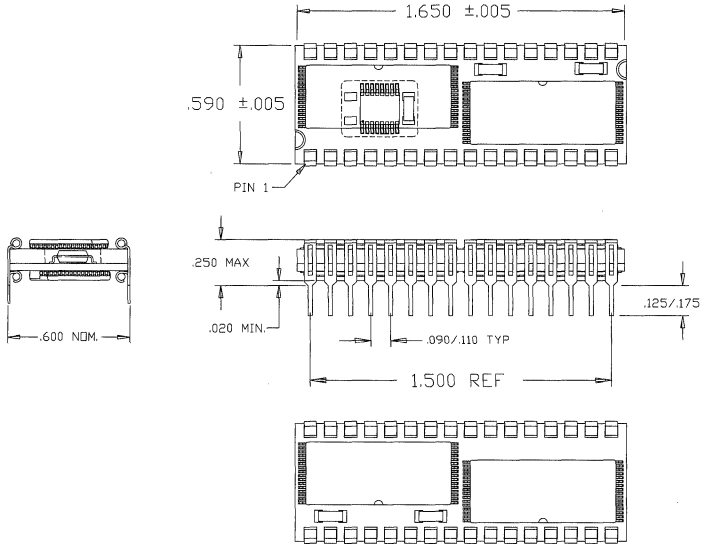
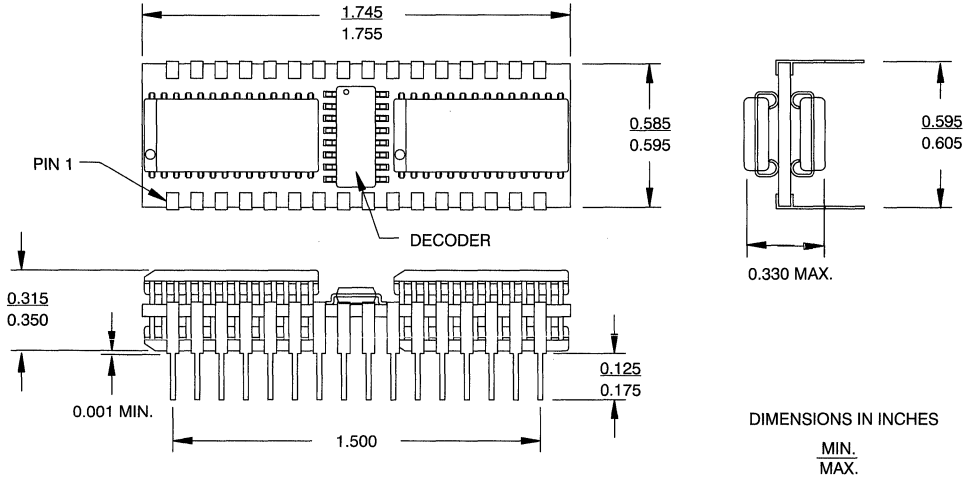
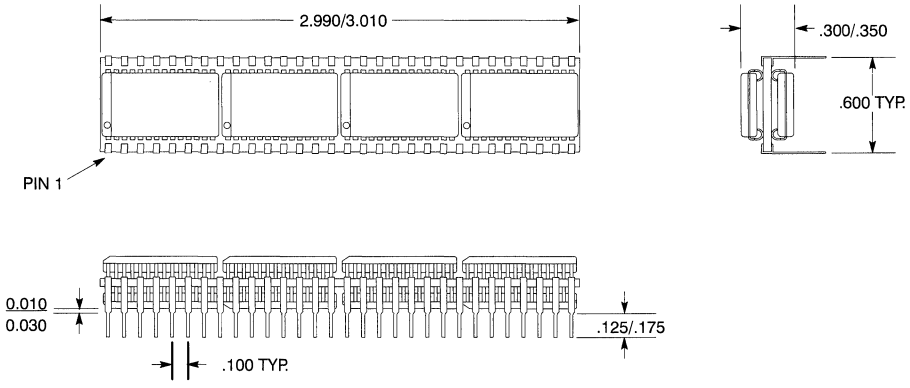
32-Pin DIP Module PD03



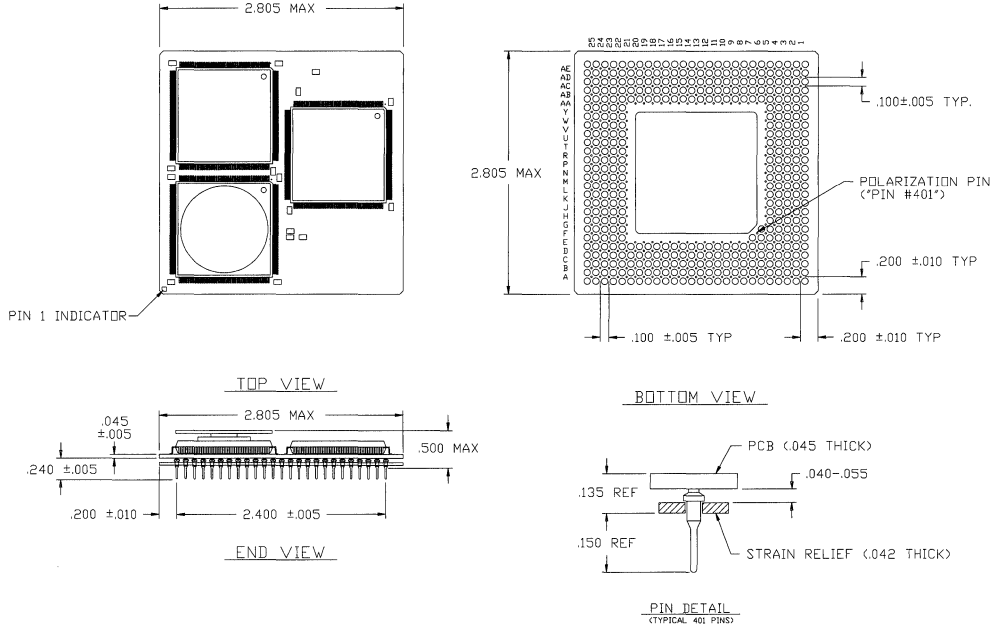
32-Pin DIP Module PD05



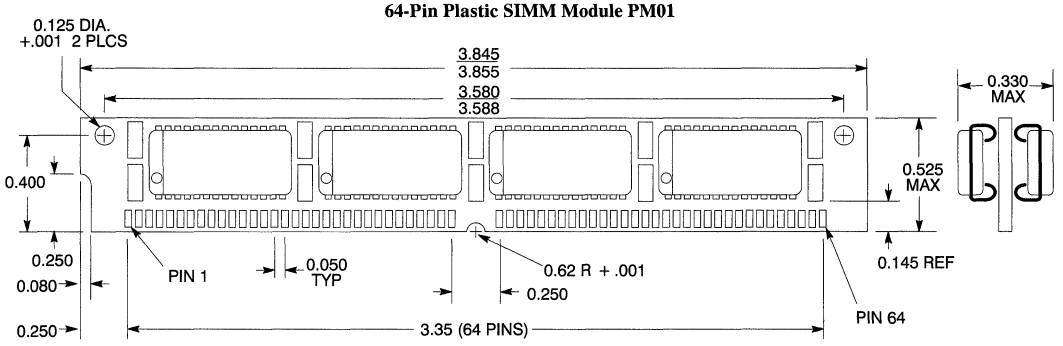
60-Pin DIP Module PD06



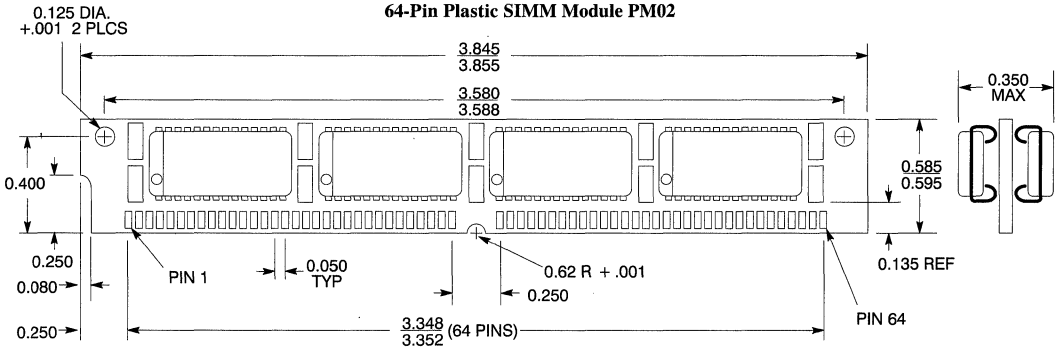
401-Pin PGA Module PG02



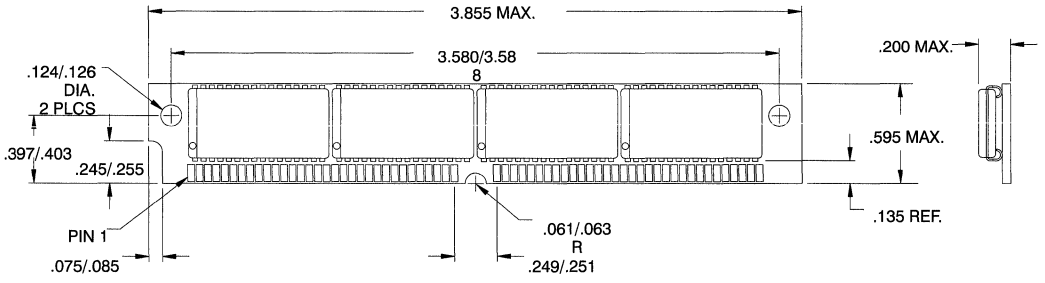
64-Pin Plastic SIMM Module PM01



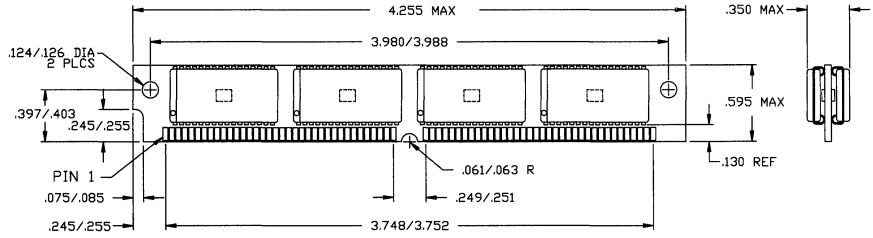
64-Pin Plastic SIMM Module PM02



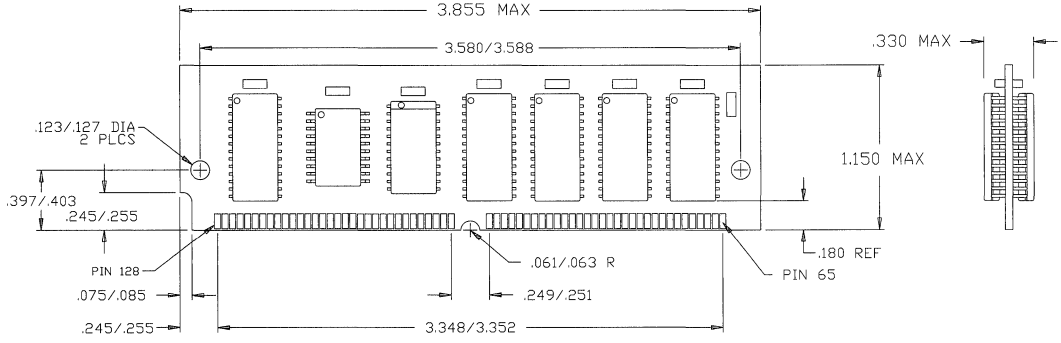
64-Pin SIMM Module PM03



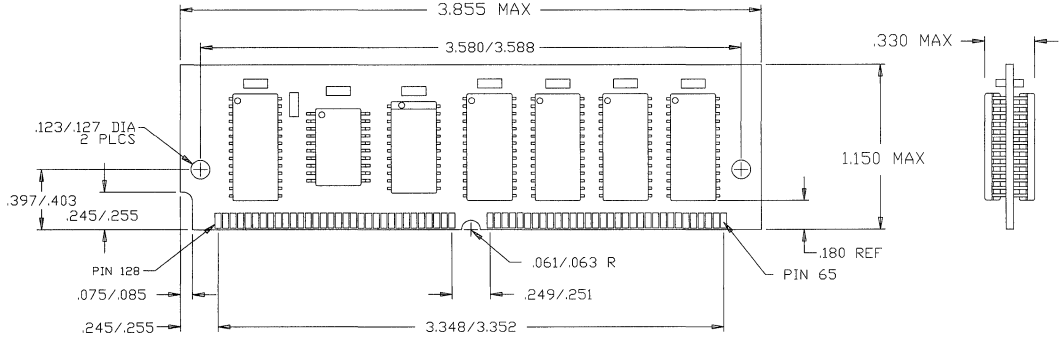
72-Pin Plastic SIMM Module PM04



128-Pin Dual-Readout SIMM Module PM05



128-Pin Dual-Readout SIMM Module PM06



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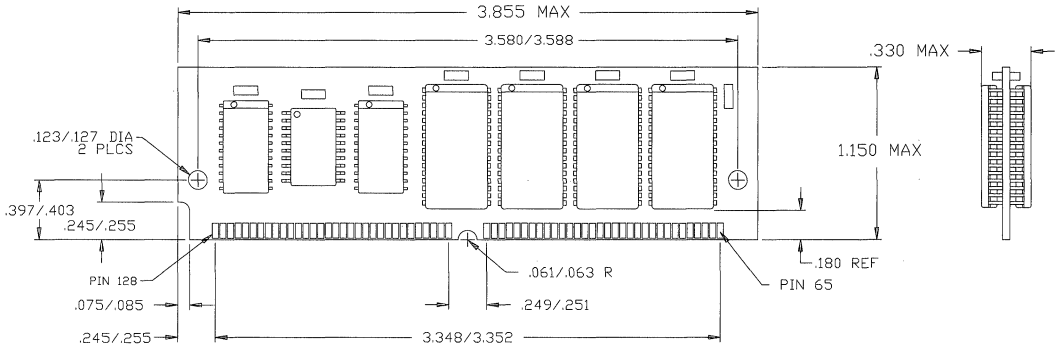
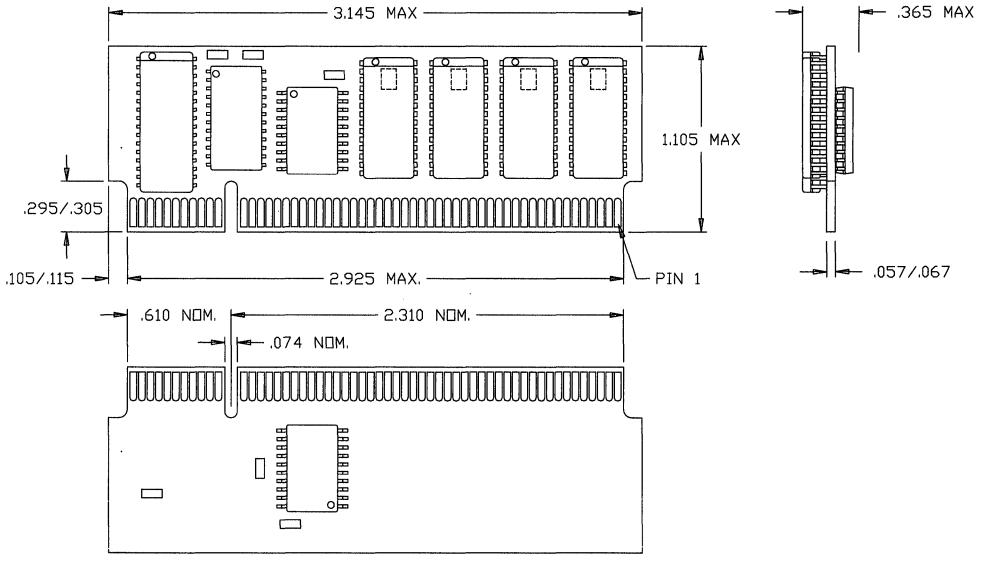
128-Pin Dual-Readout SIMM Module PM07



112-Pin Dual-Readout SIMM PM09



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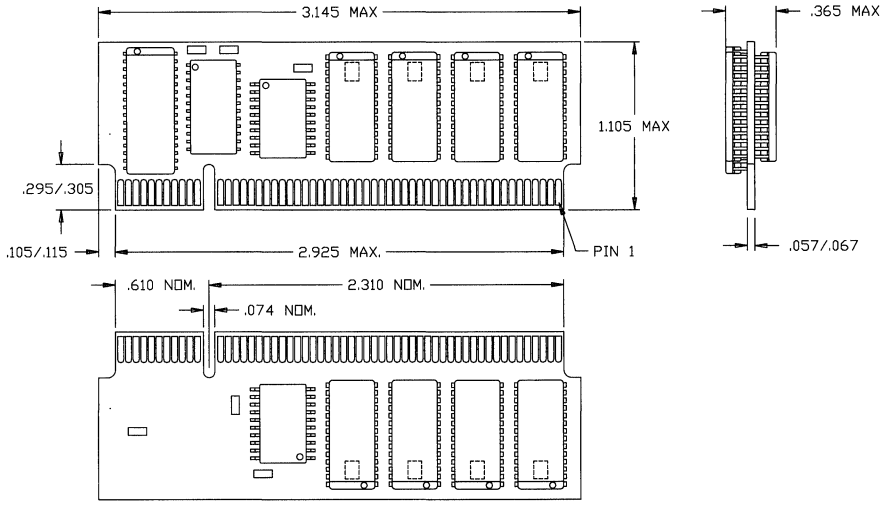

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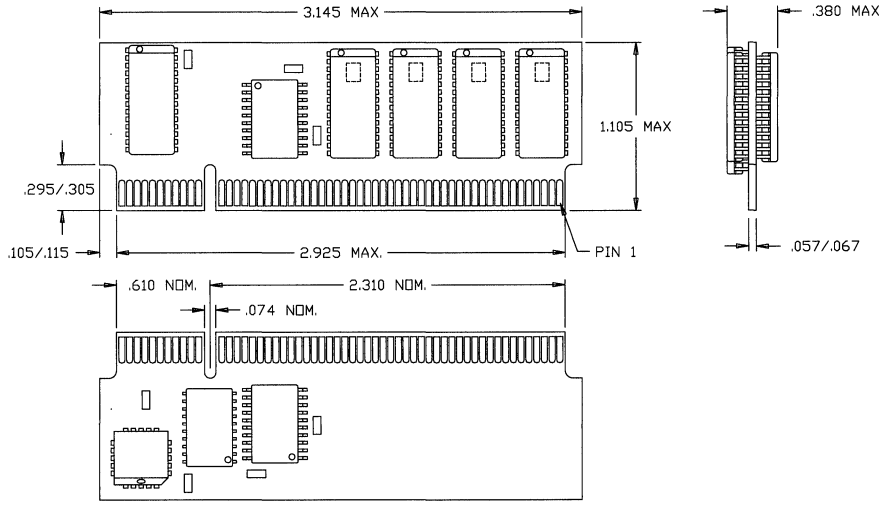

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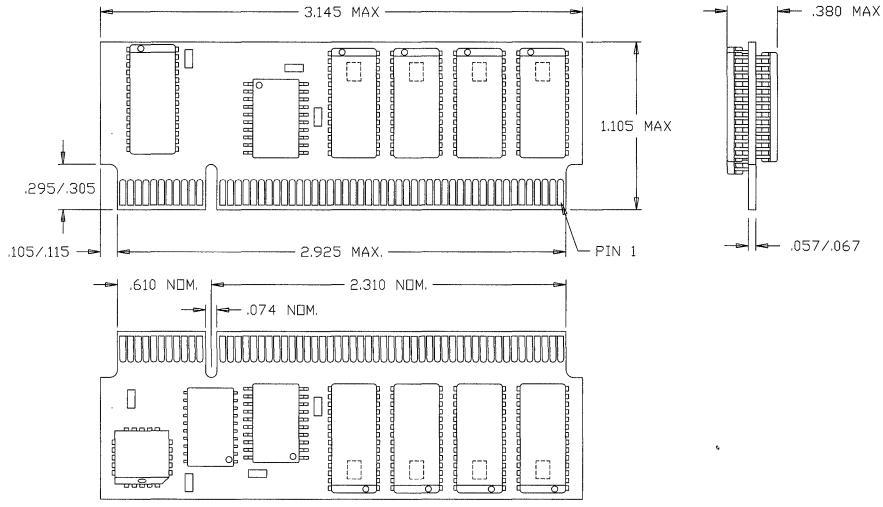
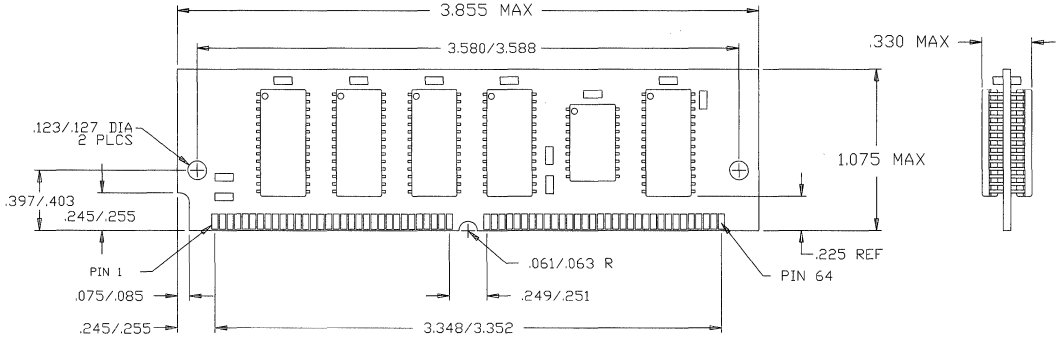
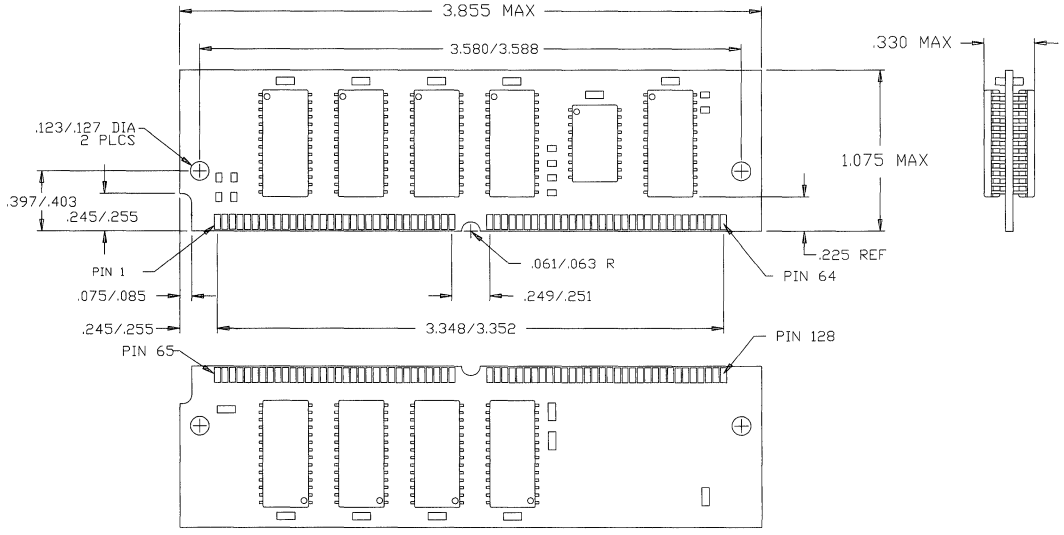
112-Pin Dual-Readout SIMM PM12



128-Pin Dual-Readout SIMM PM13



128-Pin Dual-Readout SIMM PM14



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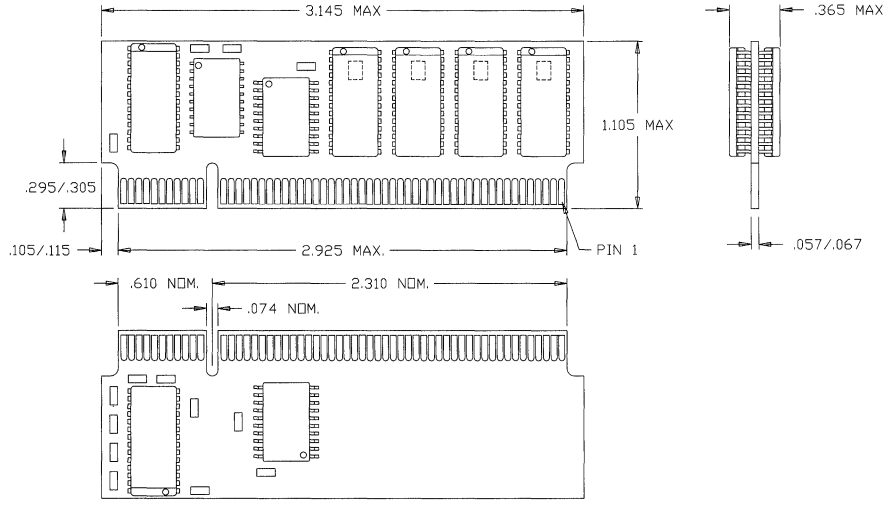

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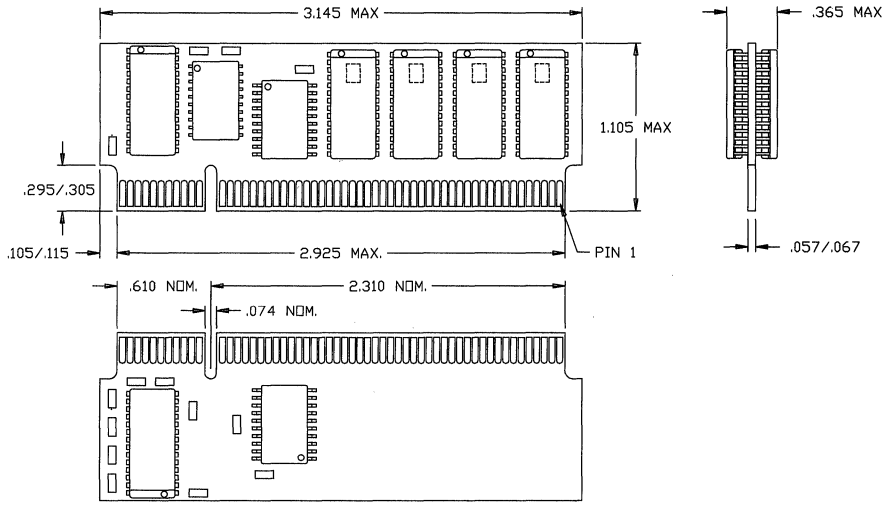

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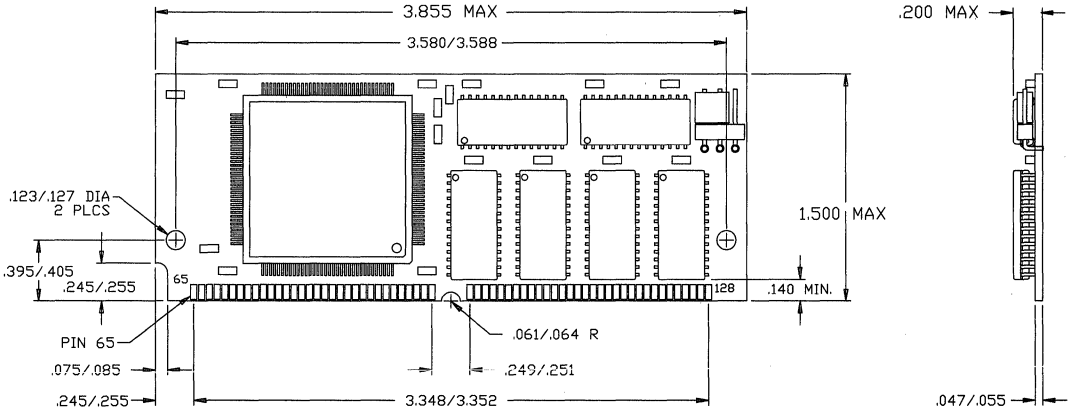
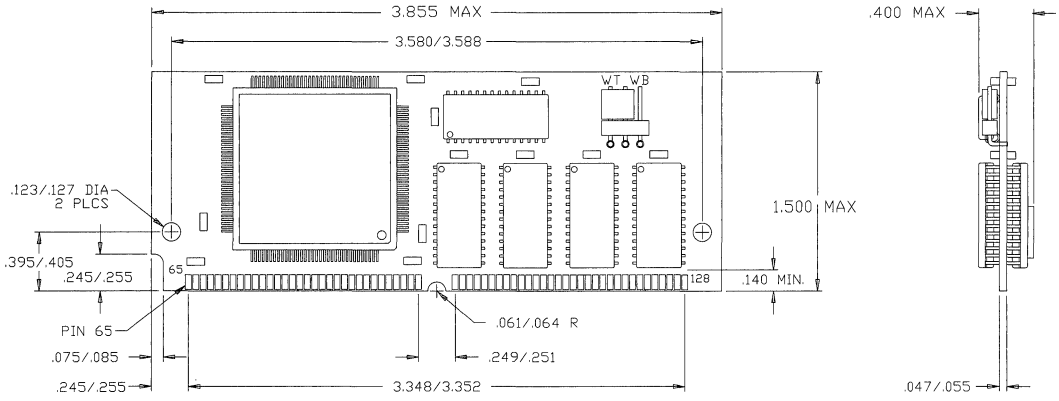
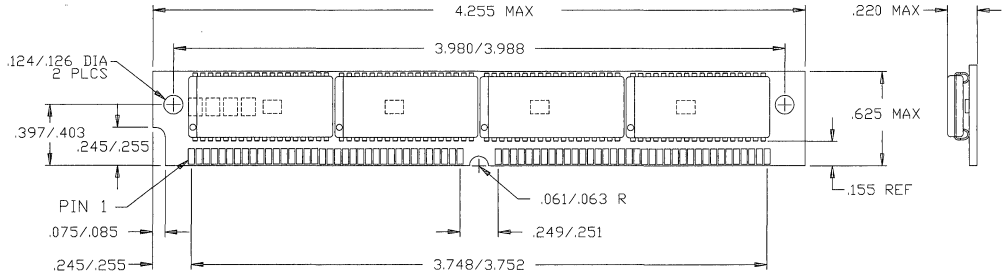
128-pin Dual-Readout SIMM PM19



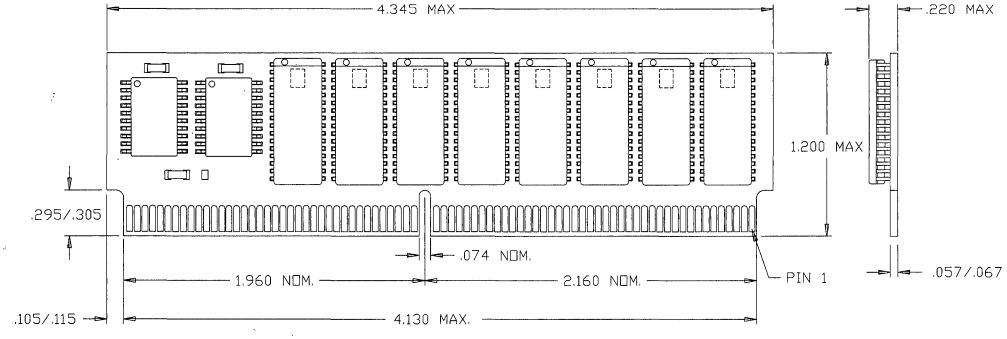
128-pin Dual-Readout SIMM PM20



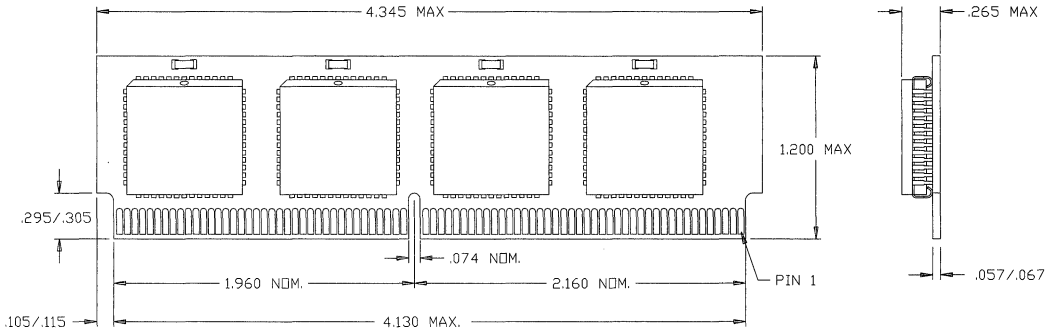
72-Pin Plastic SIMM Module PM21



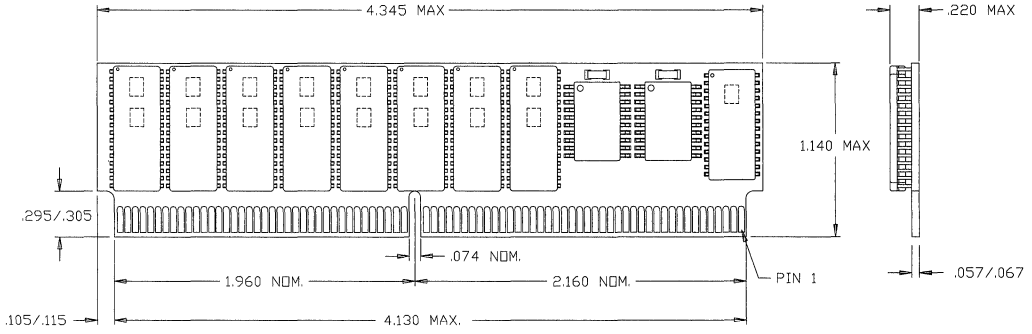
160-Pin Dual-Readout SIMM PM25



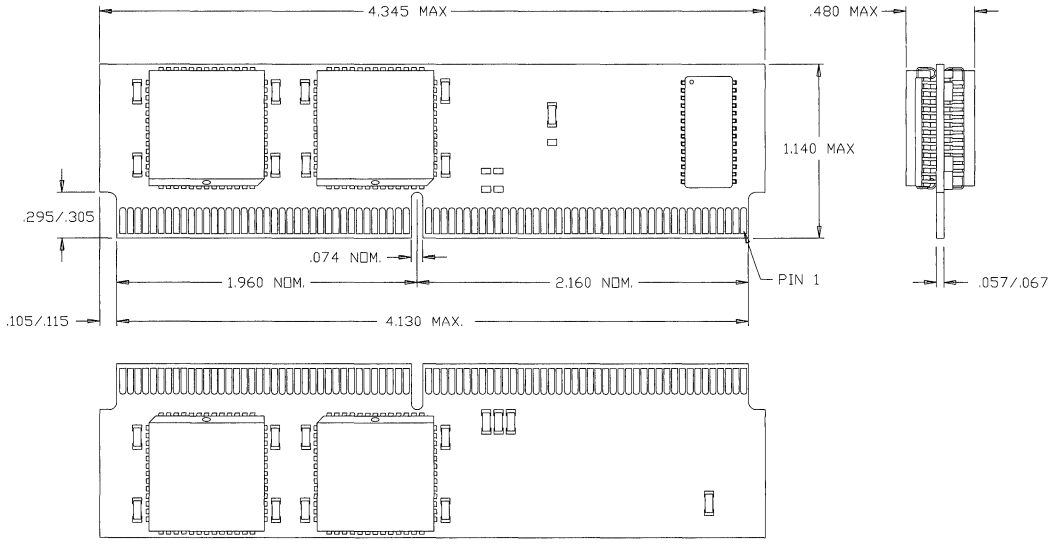
160-Pin Dual-Readout SIMM PM26



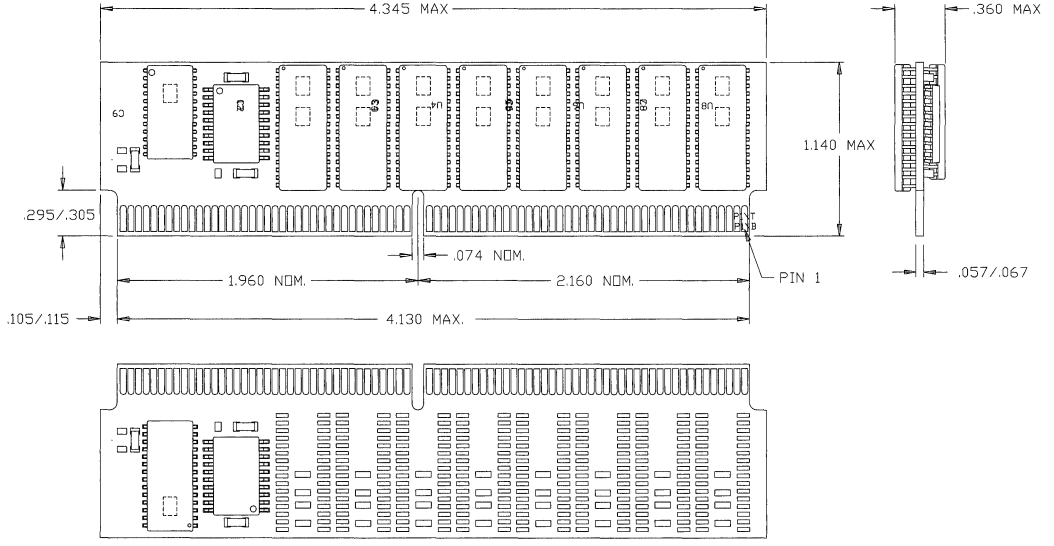
160-Pin Dual-Readout SIMM PM27



160-Pin Dual-Readout SIMM PM28



160-Pin Dual-Readout SIMM PM31



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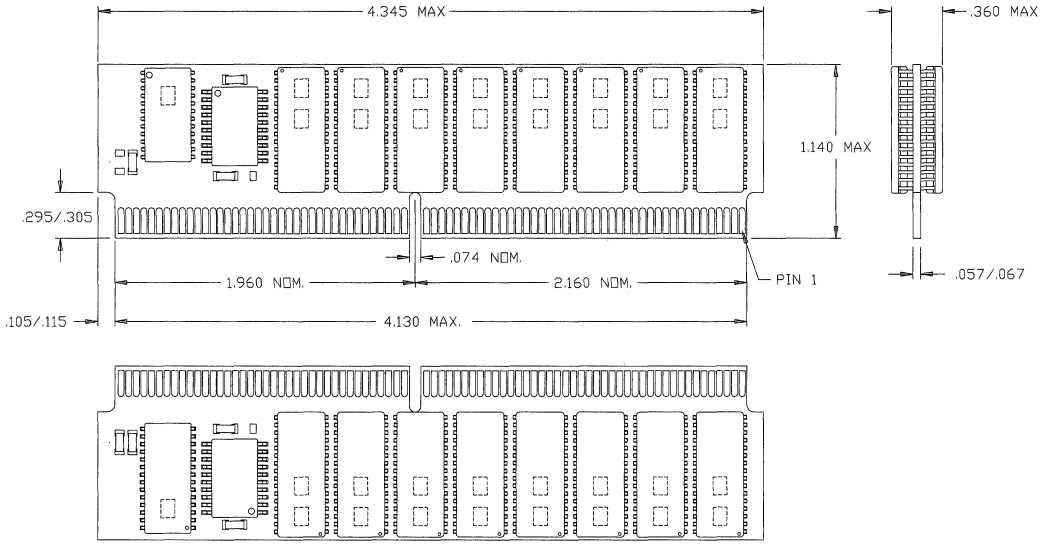
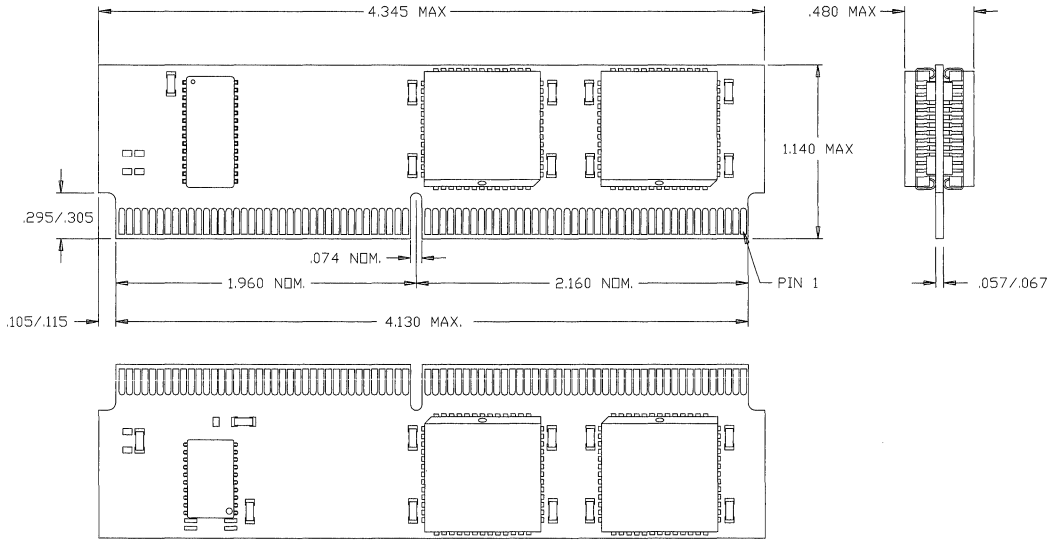
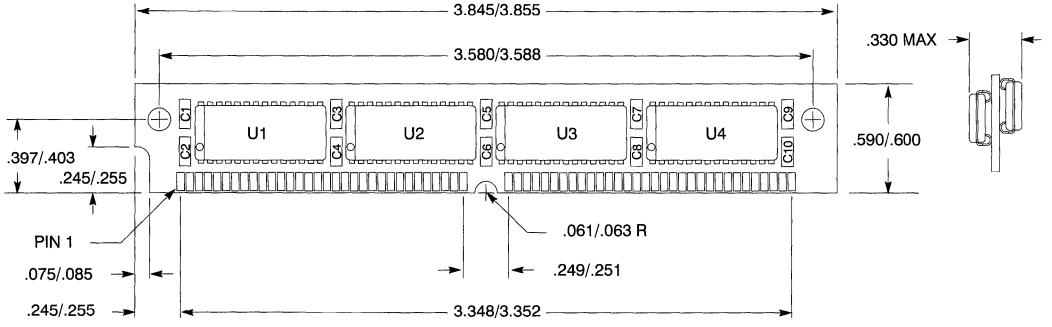
160-Pin Dual-Readout SIMM PM32



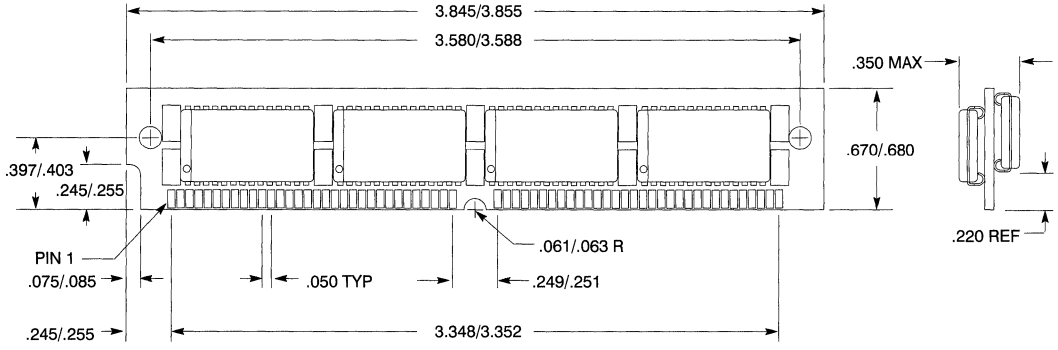
160-Pin Dual-Readout SIMM PM33



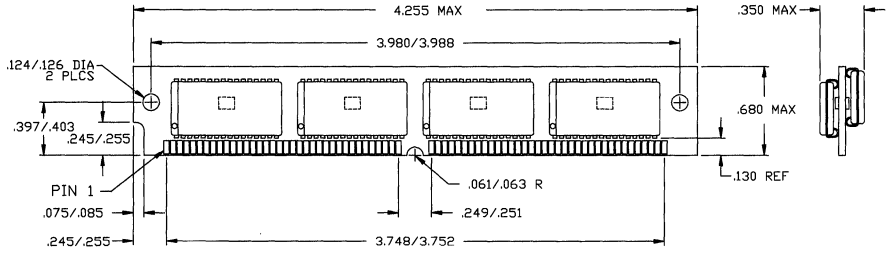
64-Pin Plastic Angled SIMM Module PN01



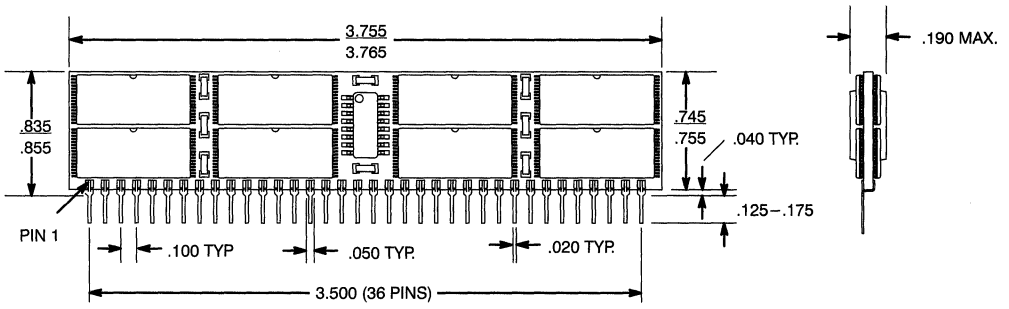
64-Pin Plastic Angled SIMM Module PN02



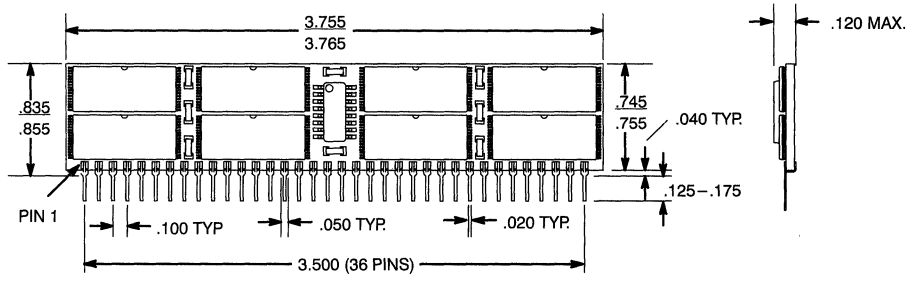
72-Pin Plastic Angled SIMM Module PN04



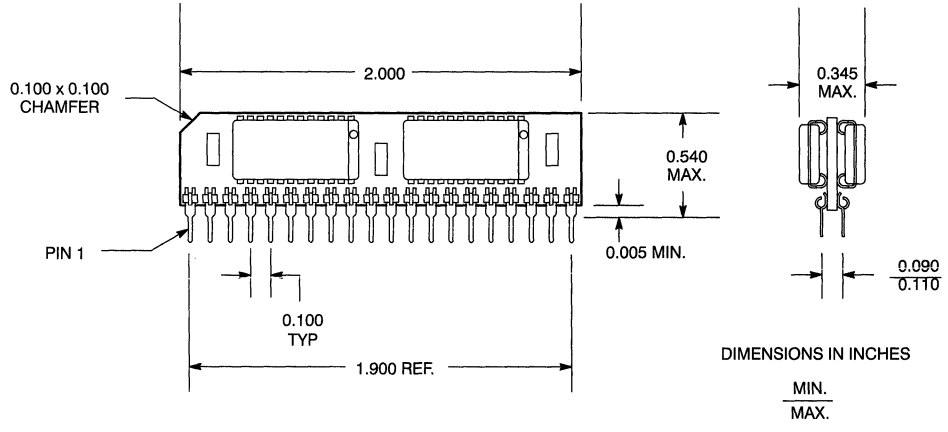
36-Pin SIP Module PS06



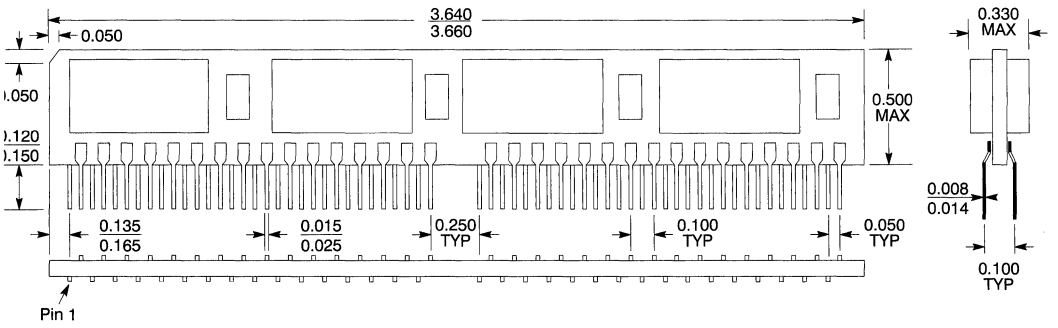
36-Pin SIP Module PS08



40-Pin Plastic VDIP Module PV04



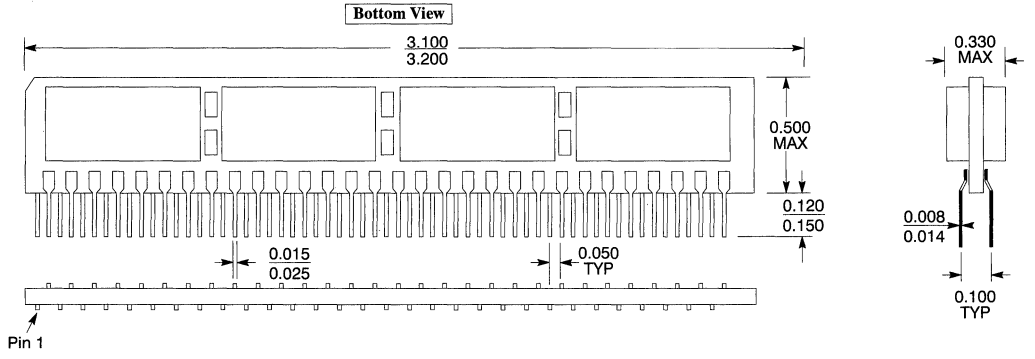
64-Pin Plastic ZIP Module PZ01



DIMENSIONS IN INCHES

MIN.
MAX.

60-Pin Plastic ZIP Module PZ02

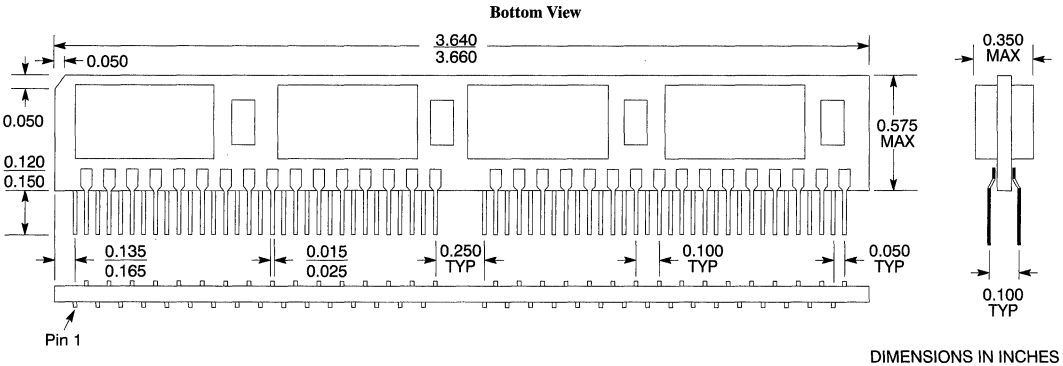


DIMENSIONS IN INCHES

MIN.
MAX.

14

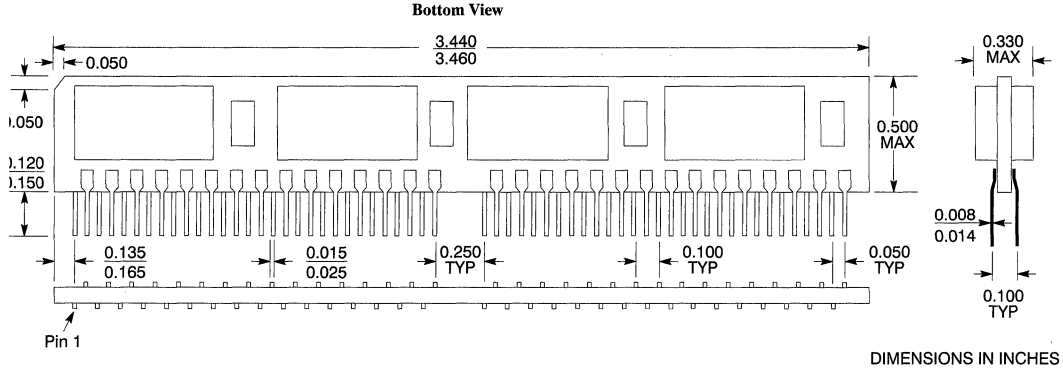
64-Pin Plastic ZIP Module PZ03



DIMENSIONS IN INCHES

MIN.
MAX.

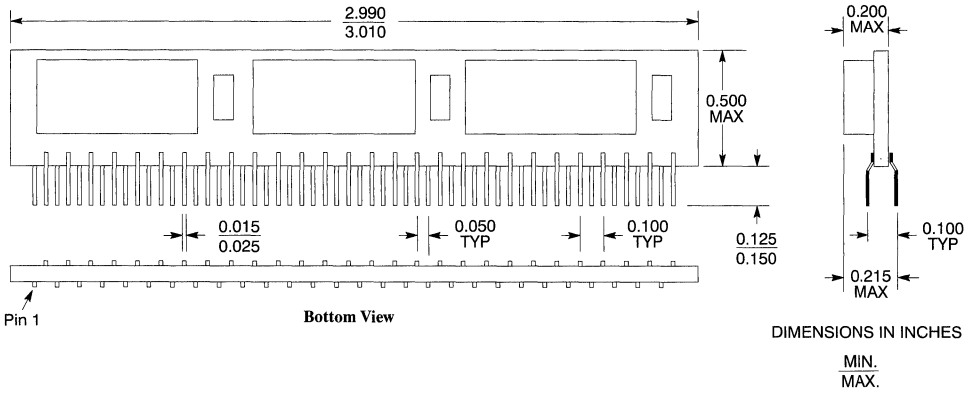
60-Pin Plastic ZIP Module PZ04



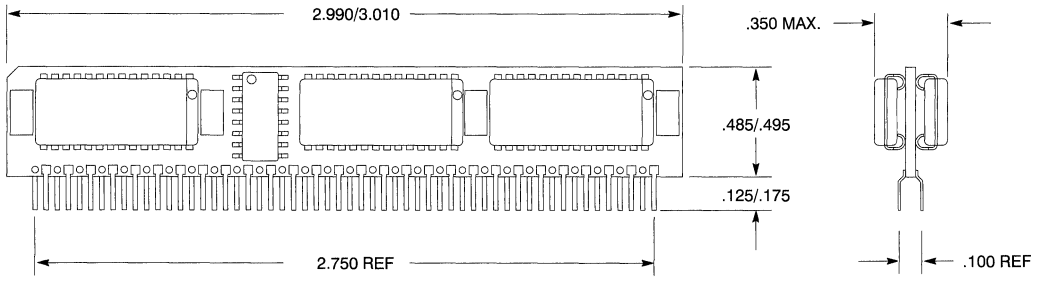
DIMENSIONS IN INCHES

MIN.
MAX.

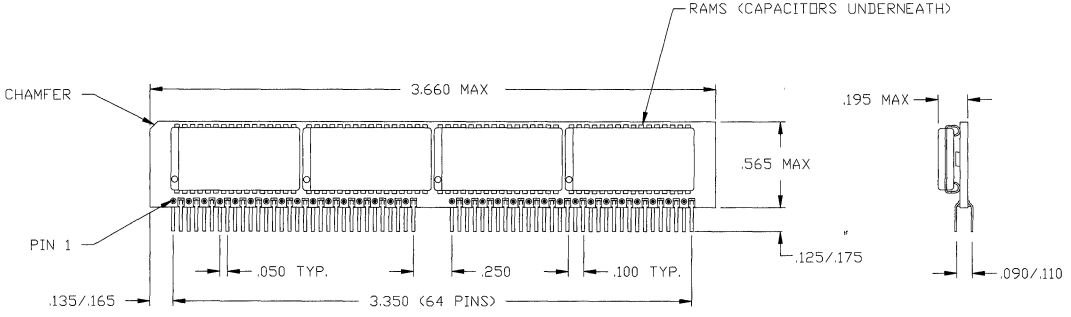
56-Pin Plastic ZIP Module PZ05



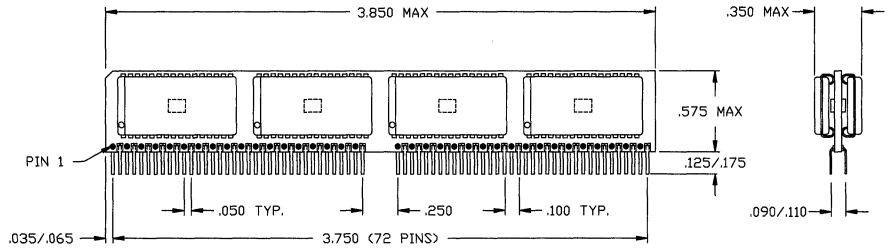
56-Pin Plastic ZIP Module PZ07



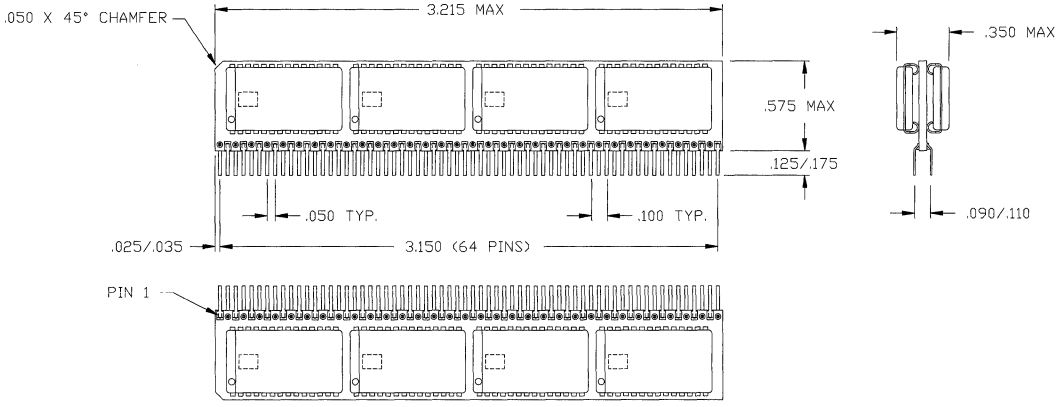
64-Pin Plastic ZIP Module PZ08



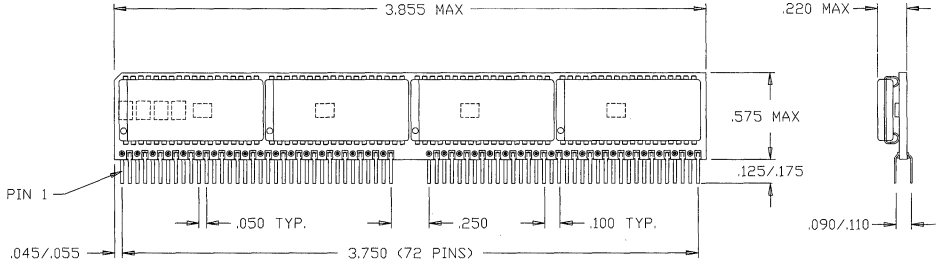
72-Pin Plastic ZIP Module PZ09



64-Pin Plastic ZIP Module PZ10



72-Pin Plastic ZIP Module PZ11



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