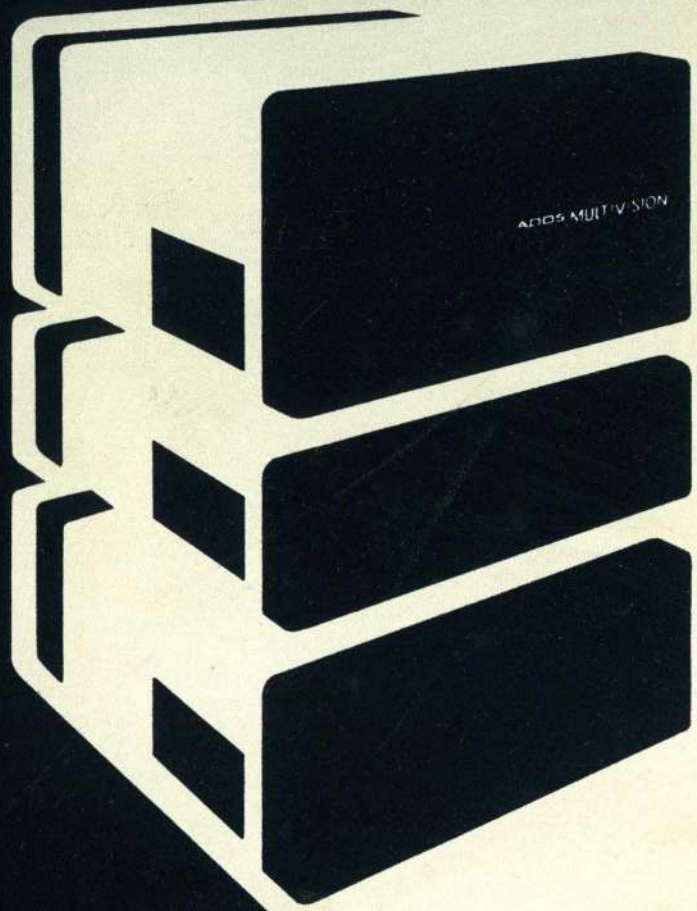

ADDS
Applied Digital Data Systems Inc.

MULTIVISION

MULTIVISION™

THEORY OF OPERATIONS

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Applied Digital Data Systems Inc

9/81

This is the first release of the Multivision™ Theory of Operation Manual.

Future revisions will have a list of changed pages in this position, with a margin bar on affected text pages.

Users are urged to use the Comment Sheet at the back of the book to communicate their comments to the ADDS' Technical Publications Department, Systems Division.

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Multivision is comprised of a family of three desk-top computers referred to as Multivision 1, Multivision 2, and Multivision 3.

Multivision 1 is a single user mini disk system that can be expanded, by the addition of easily connected modules, to a single user hard disk system, Multivision 2; and a multi-user hard disk system, Multivision 3.

This manual provides the user with a description of the hardware for Multivision 1, 2, and 3 along with the software designed for each device.

Functional descriptions of the hardware are provided along with block diagrams and schematics for each of the three modules which make up the Multivision family. Schematics are also provided for all major subassemblies, peripherals, and internal connections within the modules.

All PC boards are represented by block diagrams as well. Major logic sections are described along with the major busses and connections. I/O control lines with their corresponding I/O addresses are shown, where applicable.

The software information provided explains how the hardware is directly controlled, without the use of any of ADDS' operating system software. The information is sufficient for the Multivision user to adapt his own operating system, if desired.

Multivision 1 is comprised of six major subassemblies consisting of two mini disks, a power supply, and three PC boards (printed circuit boards), mounted in a card cage assembly.

System Bus

Each PC board in a Multivision 1 plugs directly into the system bus. The bus is comprised of 100 common pins including power. Physically, the bus is made from a multi-layer PC board with an integral ground plane. Data and address lines are physically isolated and spare ground lines surround all critical strobes. At the system level, all signals on or off the bus are unit loads. Drivers and receivers on the individual PC boards are highly noise immune components placed within close proximity to the actual PC board connectors. Signal termination is provided on the CPU board.

CPU PC Board (129-25300)

The CPU contains a 5MHz 8085A-2 microprocessor, a four channel DMA controller (with memory to memory transfer capability at four times the speed of an equivalent programming loop), an interrupt controller with 8 individual interrupt vectors, a three channel timer, 256 bytes of non-volatile memory, a 4K diagnostic and program load "shadow" EPROM, and two serial communication ports.

The first serial port is used for serial asynchronous communication to the console device (up to 9600 baud). The second can be configured for either asynchronous or synchronous communication, (up to 9600 baud), including serial printer applications. Timing for these ports is provided independently by two channels of the three channel timer. The third channel is used for general operating system timing functions. A separate 50/60Hz timing circuit is provided for custom timing applications (i.e., time-of-day).

The non-volatile memory is used primarily to replace mechanical switches in the storing of communication parameters for the serial ports and to store system diagnostic information. Spare portions of this memory are available to the user for other applications such as soft serial numbers.

64K RAM PC Board (129-23300)

The RAM PC board contains 64K bytes of dynamic memory with parity. The memory is organized into four banks, each of which contain 16K bytes. Parity is detected at the bank level. Each bank may be selected or deselected in any one of the four 16K banks the CPU can address. These addressing features are primarily designed for multi-user and sparing operations.

Mini Disk/Printer Interface PC Board (129-23100)

The PC board contains the two-drive mini disk controller and two independent parallel printer ports. The first port is an 8-bit parallel Centronics-compatible interface and the second is a 13-bit Qume-compatible letter quality interface (some popular printers which use the letter quality interface are QUME, NEC, and DIABLO models).

The Mini Disk/Printer Interface is designed around a Western Digital FD1793 disk controller. This circuit, in conjunction with phase lock loop and write precompensation logic, provides the ability to position, format, read, and write both mini disk drives in a double-sided, double-density configuration.

Mini Disk Drives

Each drive uses double-sided double-density 5 1/4" disks capable of storing 358K bytes of data for each formatted disk or 716K bytes per system (both disks). Stepping is performed by a band actuator which provides a track-to-track positioning rate of 6mS.

Access is enhanced by treating the top and bottom tracks as cylinders. The disk format is made up of 35 cylinders with 2 tracks per cylinder, 10 sectors per track, and 512 bytes per sector. Under control of MUON (the CP/M compatible operating system designed for Multivision), typical throughput is 25K bytes/second on a track basis and 10K bytes/second averaged over several consecutive cylinders.

Multivision 2 consists of the Multivision 1 Module plus the Hard Disk Module. The addition of a third drive, the hard disk, provides vastly greater storage capacity and access time, complementing Multivision 1's hardware and software features.

Hard Disk Module

The Hard Disk Module contains a 10M byte 8" hard disk drive and power supply. The hard disk employs state-of-the-art 8" Winchester technology incorporating such concepts as enclosed head units and lubricated magnetic media surfaces to assure reliability. Unformatted capacity for the disk is 10.67M bytes. The formatted capacity is 8.39M bytes arranged on 256 cylinders each of which contain four tracks with 32 sectors per track and 256 bytes per sector. The instantaneous data transfer rate to system memory is 580K bytes/second. The average rate, on a cylinder basis, is 100K bytes/second which is reduced to 80K bytes/second when averaged over several cylinders. These rates are based on ADDS' MUON Operating System calls.

Hard Disk Controller PC Board (129-25400 or 129-28700)

The Hard Disk Controller PC board is inserted into the bottom slot of the Multivision 1 backplane. Flat ribbon cables connect the PC board to the actual drive. The controller has a low cost, low parts count, and high reliability design. This is accomplished by a unique dual processor design along with a high system bus bandwidth. The first processor is an 8035 microcomputer which controls all of the slow speed functions of the drive such as head selection, stepping, and interface with the CPU. The second processor is a bipolar ROM-based 32 state sequencer which is driven by the 8035 and provides the required high speed data manipulations. CRC generation, checking, and sector header verification are performed by discrete components. Data is transferred directly to system memory via DMA control from an onboard 16-character FIFO. Since the system bus bandwidth is 1.2M bytes/second and the hard disk's transfer rate is 580K bytes/second, there is ample bandwidth remaining for other concurrent system operations to be performed.

Hard Disk Backup

Backup of hard disk files is made possible through the versatility of the mini disks. There are three techniques available:

1. Transaction backup. Applications must be structured to create transaction files which are used to update hard disk master files and are then saved as a backup library on the mini disks.

2. File backup. Entire files are selectively backed up on one or more mini disks, as necessary. Using MUON, an entire mini disk can be filled in 70 seconds.

3. Incremental change backup. MUON will copy to mini disk only those records from a given file that have been modified. Since the image on the mini disk is an exact replica of the data on the hard disk, full file dumps are not required. The amount of mini disk storage will always be equivalent to the size of the file. This technique substantially reduces the amount of time required to maintain a backup copy of a hard disk file.

Multivision 3 consists of a Multivision 2 plus the Expansion Module. The Expansion Module is situated between the Multivision 1 Module (top module) and the Hard Disk Module (bottom module). The Expansion Module contains an extension of the system bus which is attached to the Multivision 1 by two connectors. Power is supplied to the expansion bus from the power supply in the Hard Disk Module. The card cage, which is the only subassembly in the Expansion Module, contains slots for four PC boards: a 4 Port I/O PC board, and up to three additional 64K RAM PC boards.

4 Port I/O PC Board (129-24700)

The 4 Port I/O PC board contains four fully independent asynchronous serial communication ports. Baud rates are independently selectable (up to 9600 baud). Communication parameters are all software selectable and stored where they are user-modifiable in the CPU PC board's non-volatile memory. The circuitry which controls the ports is designed around the operating system I/O drivers so that maximum system throughput may be obtained in a multi-user environment. For example, access to the four ports is controlled by a steering register located on the PC board; this allows the use of a common software driver. The concurrent operation of the four terminals at 9600 baud is guaranteed by a 16-character FIFO associated with the receive input of each port.

Memory Organization

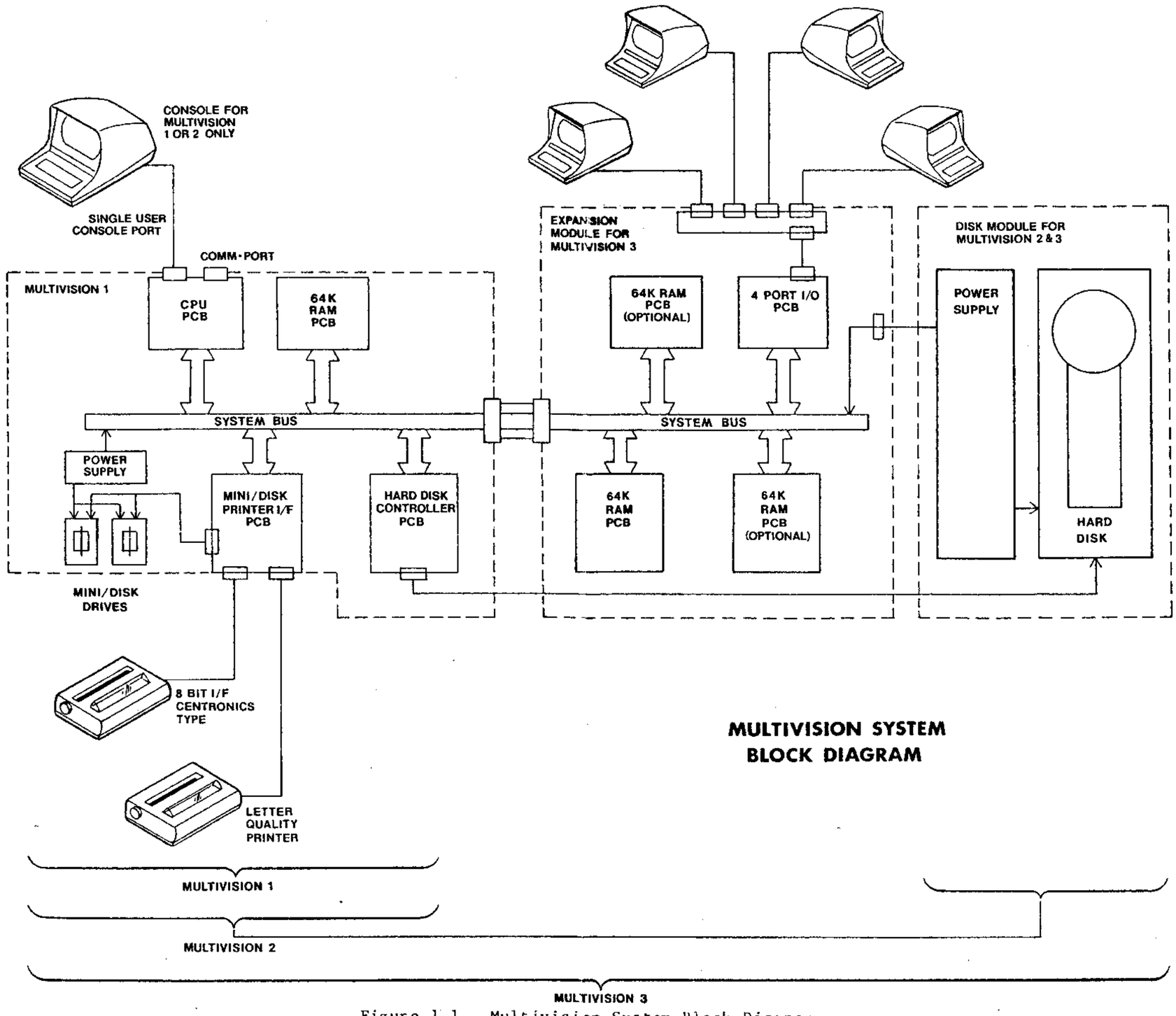
Each 64K RAM PC board in the Expansion Module is identical to the RAM PC board in the Multivision 1 Module. The cards are differentiated by jumper selections.

MUON uses the 64K RAM PC board's bank selection logic to implement multi-user operation. Each user has 48K bytes of real memory, while 16K bytes are always used by the operating system. At task or user switch time, the three banks allocated to the present user are deselected and the next user's three banks are selected. Task switch time is greatly reduced by using real memory to store each user's program instead of the classical disk paging and virtual memory schemes. Because the real memory is stored for each user, a 64K RAM PC board is needed for each user.

Since each user requires only 48K bytes (or three banks) of memory, and only one operating system is needed regardless of the number of users, each time another PCB is installed, another spare memory bank becomes available.

The extra banks may be used if parity errors are detected in other banks. The information regarding the use of a spare bank is stored in the non-volatile memory until the failed PC board is retested. Failed banks are automatically bypassed by the operating system when assigning user memory banks. This is possible due to bank address relocation.

Spare banks may also be used for background tasks. MUON (which is a true multi-tasking operating system) provides features to easily implement these tasks. One such background task, a print queue manager, is provided with the operating system.



MULTIVISION SYSTEM BLOCK DIAGRAM

Figure 1-1. Multivision System Block Diagram

OVERVIEW

The Multivision Central Processing Unit is logically divided into the 12 sections listed in Table 2.1 below and described on the following pages. The CPU Block Diagram, Figure 2-1, shows the major components located on the CPU PC Board. It can be used as a reference to depict interrelationships between the various components.

Table 2.1. CPU Logic Sections

Logic Section	Description
Processor	8085A-2 5MHz operating frequency.
DMA Controller	An 8237-2 5MHz 4 channel controller.
CMOS Memory	The 256 x 8 memory element, used for system parameters, is accessed via I/O ports. Back-up battery power is used to retain these parameters for use by the diagnostic EPROM and operating system.
EPROM	The 4K x 8 2732 EPROM, used for system power-up diagnostics and coldboot procedure, is disabled after the coldboot operation to free the 4K address space for operation of the system.
Serial I/O	Two 8251A USARTs. The first port is used as a console device in a single user system; the second port is used in user-defined serial communications or serial peripheral device operation.
Timer	The 8253-5 Programmable Interval Timer has 3 channels. Channel 0 is used as an interval timer by the operating system for internal timing considerations. Channels 1 and 2 are used as baud rate generators for serial ports.
Interrupts	The 8085A has 5 interrupt lines and the 8259A Programmable Interrupt Controller allows direct vectoring for up to 8 additional interrupts.

Table 2.1. CPU Control Sections (continued)

Logic Section	Description
Reset	Power on reset is a one-shot reset which uses the Reset button on the front panel of Multivision 1. It provides a .5 second reset pulse to all system peripherals.
Refresh	This circuit provides the basic refresh timing for dynamic memory within the system. For detailed information on refresh circuitry, see Section 3, RAM PC Board.
RTC	Real Time Clock circuitry monitors the AC line frequency and provides a 10Hz clock which is used by the interrupt input of the 8259A for real time measurements. RTC is not supported by ADDS' software.
Oscillator	A 20MHz crystal oscillator provides a 10MHz fundamental frequency for the 8085A-2 processor, and provides a 2MHz comm clock used for internal timing in most peripheral devices.
Decode	Address I/O decode circuitry, handling all onboard chip select signals, generates an onboard signal for selecting an onboard data bus which allows processor access to onboard devices.

Functional Description

The 8085A-2 Microprocessor is the heart of the Multivision system. It is a complete 5MHz 8-bit parallel central processor with 16 address lines which can access 64K memory locations and 256 I/O port addresses.

The 8085A-2 has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A-2 register set is shown in Figure 2-1 below.

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC,DE,HL	General Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

Figure 2-1. 8085A-2 Register Set

The 8085A-2 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8 bits are latched externally by the Address Latch Enable (ALE) signal. During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The 8085A-2 provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge (INTA) signal is also provided. HOLD, READY, and all interrupts are synchronized with the processor's internal clock. The 8085A-2 also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

Interrupt Structure

The 8085A-2 has 5 interrupt inputs: TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending. The order is as follows: highest priority -- TRAP, then RST 7.5, RST 6.5, RST 5.5 and, INTR -- the lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The three maskable interrupts, RST 5.5, 6.5 and 7.5, initiate the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. TRAP, the non-maskable interrupt, causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks.

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive as INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

Interrupts 5.5 and 6.5 are connected to the USARTs which control the two serial ports on the CPU PC board. Interrupt 5.5 generates an interrupt whenever the console port USART has a character ready to be input to the CPU. The communications port USART receiver ready is connected to Interrupt 6.5.

Interrupt 7.5 is connected to Counter 0 of the 8253 timer chip. This interrupt is used by MUON to control task scheduling and for the system timer services.

The RST 7.5 requires only a pulse to set an integral flip-flop which generates the internal interrupt request. This flip-flop remains set until the request is serviced. Then it is reset automatically. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085A-2.

The status of the three RST interrupts can only be affected by the SIM instruction and RESET IN.

Interrupt INTR is connected to an 8259A Programmable Interrupt Controller, providing an additional 8 interrupt lines to the 8085A-2.

See the Intel Component Data Catalog for the hardware specifications for this chip, and also the Intel 8080/8085 Assembly Language Programming Manual for information on programming this part.

Functional Description

The Multivision CPU makes use of the 8237-2 DMA Controller to reduce the burden placed on the system's software and hardware for data transfers between memory and peripherals such as the mini disk and the hard disk. The device is also capable of performing transfers of data blocks from one memory block to another, reducing the time required for these operations.

DMA (Direct Memory Access) is an operation whereby control of the system bus is taken away from the processor (the 8085) and given to the DMA Controller. Once the Controller is programmed, it remains in an idle state until there is a need for data transfer. The Controller receives an active signal on one of its DREQ (DMA request) lines and, if the device has been programmed to respond to that DREQ, it will issue a HOLD signal to the processor. When the processor receives this hold signal, it completes the operational cycle it is currently in, places program and status information on its stack, and goes into an idle state, freeing the bus for DMA operation. When the processor goes into this idle state, it issues a hold acknowledge (HLDA) signal to the DMA device. Upon receiving HLDA, the Controller initiates a data transfer by placing the address information stored in that channel's address register. The Controller then issues the signal DACK (DMA acknowledge) for the channel it is responding to. While DACK is active, the Controller issues the appropriate read/write signals. The DACK signal is used by the requesting device as a device select, allowing the read/write signals to affect the device, completing the data transfer. Upon completion of the transfer, the Controller goes inactive, placing HOLD and DACK in the idle state. This allows the processor to regain control of the system.

For peripheral to system operations (mini disk, hard disk), the Controller is used in the demand mode of operation, which initiates single byte transfers, until the channel count register reaches completion count. This is done to minimize the time taken from the processor since the mini disk and hard disk interfaces require a relatively large amount of time to make a character available to the Controller.

For memory-to-memory operations, the Controller is used in a block transfer format, as the data is immediately available for the Controller. Memory-to-memory transfers make use of an internal data storage register within the Controller. The Controller first reads the data from the source address, stores the data in this register, then writes the data to the destination address.

Source and destination addresses are stored internally, utilizing channels 0 and 1 of the Controller. For a complete description of the 8237-2, refer to the appropriate Intel documentation.

Software Operations

Table 2.2. Multivision Port Assignments for DMA

Port Number	Register
0A0H	channel 0 address
0A1H	channel 0 count
0A2H	channel 1 address
0A3H	channel 1 count
0A4H	channel 2 address
0A5H	channel 2 count
0A6H	channel 3 address
0A7H	channel 3 count
0A8H	status
0A8H	command
0A9H	request
0AAH	mask
0ABH	mode
0ACH	clear flip-flop
0ADH	reset
0AFH	mask write

The following examples illustrate the use of the 8237 for data transfer under MUON.

1. Memory-to-Memory DMA Transfer

For memory-to-memory data transfer, channel 0 is programmed as the source and channel 1 as the destination. The 8237 may be programmed as follows:

a.	Clear flip-flop	OUT 0ACH
b.	Set source address register (channel 0)	A<--Source address (low byte) OUT 0A0H A<--Source address (high byte) OUT 0A0H
c.	Set source count register (channel 0)	A<--Transfer count -1 (low byte) OUT 0A1H A<--Transfer count -1 (high byte) OUT 0A1H
d.	Set destination address register (channel 1)	A<--Destination address (low byte) OUT 0A2H A<--Destination address (high byte) OUT 0A2H
e.	Set destination count register (channel 1)	A<--Transfer count -1 (low byte) OUT 0A3H A<--Transfer count -1 (high byte) OUT 0A3H
f.	Set mode register for channel 0 block read and channel 1 block write (address increment is selected and auto initialize is deselected)	MVI A,88H OUT 0ABH MVI A,85H OUT 0ABH
g.	Set command register for memory-to-memory transfer	MVI A,41H OUT 0A8H
h.	Set request register to begin transfer (no instructions will be executed until the transfer is completed)	MVI A,04H OUT 0A9H

2. Memory <=> Mini Disk DMA Transfer

Channel 2 is used for data transfer between the Mini Disk Controller and memory. The following steps show how to set up the 8237 for demand mode DMA which is initiated by requests from the disk controller for disk data transfer.

a.	Clear flip-flop	OUT 0ACH
b.	Set address register for channel 2	A<--Memory address (low byte) OUT 0A4H A<--Memory address (high byte) OUT 0A4H
c.	Set count register for channel 2 (the count should be the same as the number of requests that the disk controller will issue)	A<--Transfer count -1 (low byte) OUT 0A5H A<--Transfer count -1 (high byte) OUT 0A5H
d.	Set mode register for demand mode read or write on channel 2 (auto initialization is disabled, address increment is selected)	MVI A,0AH (memory-to-mini disk) or MVI A,06H (mini disk-to-memory) OUT 0ABH
e.	Set command register non-memory-to-memory DMA	MVI A,40H OUT 0A8H
f.	Set mask register to set channel 2 mask	MVI A,02H OUT 0AAH

3. Memory <=> Hard Disk DMA Transfer

Channel 3 is used for data transfer between the Hard Disk Controller and memory. Below is an example of the programming steps required to set up this channel for a read or write data transfer.

a.	Clear flip-flop	OUT 0ACH
b.	Set address register for channel 3	A<--Memory address (low byte) OUT 0A6H A<--Memory address (high byte) OUT 0A6H
c.	Set count register for channel 3	A<--Transfer count -1 (low byte) OUT 0A7H A<--Transfer count -1 (high byte) OUT 0A7H
d.	Set mode register for demand read or write, address increment selected and auto initialize disabled	MVI A,0BH (write) or MVI A,07H (read)
e.	Set command register for non-memory-to-memory DMA	MVI A,40H OUT 0A8H
f.	Set mask register to set channel 3 mask	MVI A,3 OUT 0AAH

Functional Description

The CMOS memory circuit utilizes two 5101L-1 256 x 4 bit memory chips. These ICs are capable of storing information while in a "power down" state by drawing current from a backup power source. The power source used on the CPU is a 3 volt lithium battery with a design life of five years in the circuit used by the CPU. This battery supplies a 2 volt Vcc for the memory chips while the systemm is powered down, allowing the ICs to retain data. When the system is powered up, the 5 volt system supply provides Vcc for the ICs. The drain on the battery is shut down by the use of a diode which overrides the current flow from the battery to the memory chips.

The CMOS memory is accessed through the use of I/O ports, so the memory elements do not use memory space allocated for system use. I/O port 98H activates CMOS by raising the level of the chip disable (standby mode) pin in the memory chip. It is necessary to activate the circuit prior to any read or write to CMOS. After access is complete, the circuit must be disabled to prevent possible data loss during system power down. Writing an '04' to I/O port 98H activates the circuit, while writing a '00' to port 98H disables the circuit. Accessing port 98H toggles a flip-flop circuit providing a chip enable/disable signal for the memory chip.

In order to read or write data to memory after it has been enabled, you must first load in the memory address you wish to access (00H-FFH) by writing the address into port 92H. This activates an 8-bit latch which holds the address information stable on the memory chip address line. To read or write to this memory location, simply read or write to port 93H, as this port activates the read/write pins of the memory chip. In order to access another memory location in CMOS, it is necessary to again set up the proper address by writing to port 92H, then reading or writing to port 93H to manipulate the data at that location in memory. After all memory accesses are finished, write a '00H' to port 98H to disable the memory circuit.

CMOS memory is used by the "shadow" EPROM during diagnostic self-testing of the system, and by the operating system for initialization of system parameters for proper system operation. Any errors found by the diagnostic programs are stored in a table located in CMOS, and the diagnostic program refers to this table whenever self-testing is active. Any errors flagged in CMOS will be displayed on the console screen and, if required, the operator must take appropriate action to correct these errors. The shadow EPROM also uses CMOS to set up the system parameters of the particular system in use (e.g., memory allocation, terminal configuration, disk configuration, etc.). During loading of the operating system (bootstrap operation), CMOS is accessed so the operating system can check and set system parameters and check memory allocation tables as required.

In order to insure that the data stored in CMOS is correct, the system makes use of a check-sum operation within CMOS. This entails making a count of the number of bits high within the CMOS memory and calculating a check-sum to determine if the bit total has changed. If no change has occured, it is assumed that the data stored in the memory is valid. If the check-sum is incorrect, the shadow EPROM will use a set of default parameters stored within the EPROM for system initialization. It will then store these parameters within CMOS and calculate a new check-sum, placing the check-sum in CMOS memory.

A further step to insure data integrity is the use of a "triple redundancy" scheme, where the data is stored in three identical blocks, each with a checksum. The PROM or operating system reads block one and its checksum is verified. If the checksum is correct, the data is used to update the other two blocks. If the checksum is incorrect, it goes to block two. Block two is then read and, if the checksum is correct, the data stored in this block is used to update blocks one and three, etc. The good "third" will always update the other two blocks.

Programming CMOS

Information is passed from the Diagnostic/Bootstrap program to the operating system through 256 bytes of non-volatile CMOS RAM. Recorded here are the results of the diagnostic portion of the program, the bank number containing the booted operating system, and certain other system parameters such as console baud rate and parity settings. CMOS is accessed as an I/O peripheral through the following ports:

PORT	USAGE
92H	Write only: CMOS Address Register
93H	Read/Write: CMOS Data Register

CMOS must be "turned on" before reading or writing any data. This is done by outputting a '4' to port 98H, then waiting at least 10 milliseconds. CMOS should be "turned off" after all CMOS operations are complete by outputting a '0' to port 98H.

Refer to the topic entitled Diagnostic/Bootstrap and System Load for details on the layout of information in CMOS.

Programming examples for manipulating CMOS are shown below:

1. To determine the diagnostic for the console port on the CPU, the result is returned in register A:

```
GETDIA:
     MVI     A,05H          ;Select the CMOS address
     OUT     92H
     IN      93H            ;Read the data at that address
     RET
```

2. To update the contents of a given address of CMOS while correctly maintaining the checksum byte, the update address is passed in register D, and the new data value is passed in register E. This routine only updates the first CMOS block:

```
WRCMOS:
     MOV     A,D            ;Select address to be updated.
     OUT     92H
     IN      93H            ;Read current data value there.
     MOV     B,A            ;Save current value in B
     MOV     A,E            ;and write new value there.
     OUT     93H
     MOV     A,053H         ;Select address of checksum byte.
     OUT     92H
     IN      93H            ;Read current checksum.
     SUB     B              ;Subtract old data value
     ADD     E              ;and add in new data value.
     OUT     93H            ;Write out new checksum value.
     RET                    ;The end.
```

Functional Description

The shadow EPROM 2732 resides on the CPU PC board. It contains a set of diagnostic programs which test all elements within the system. The EPROM has a set of messages stored which provide the operator with error information, system status information, and operator prompts which are used when the system requires outside input. Included in the program set are:

1. Memory Diagnostics -- This program places an alternating pattern of "ones" and "zeros" within system memory and then checks the pattern for any changes. If any changes occur, the memory bank being tested is flagged as bad and an error message is displayed on the system console, indicating which bank and memory board are affected. This program will test all memory within the system, up to the 256K used in a multi-user system.

2. Serial I/O -- All serial I/O ports within the system are tested utilizing the loop test feature of the serial ports. This program initializes the USARTs, places the channel in loopback, and outputs a character through the port. It then reads the character received by the channel and compares this character to the character sent out. If the characters do not match, the EPROM will issue an error message to the screen indicating which PCB contains the defective serial port. This program tests not only the serial device, but also the associated timer, which supplies the port baud rate, and tests much of the gating logic associated with these ports.

3. CMOS -- This program reads CMOS, calculates a check sum and then compares the check sum calculated with the check sum already stored in CMOS. If there is an error, a message is sent to the console device and the CMOS is cleared. New system parameters are then stored in CMOS using a table stored in the EPROM, and a new check sum is then calculated and stored in CMOS.

4. Mini Disk -- This program tests the Mini Disk Controller (an FDI793) by outputting information to the controller device. The program writes to the registers within the 1793, and then reads back from those registers to insure the device can be written to and read from. The program also issues a restore command to the 1793 in order for it to be in a known state for the boot operation which takes place upon completion of diagnostic testing.

5. Interrupt Controller -- This program tests the Interrupt Controller by programming the device to respond to an interrupt and then issuing the correct vector address for the 8085. The program places a jump instruction at this address which will return the system to the diagnostic program's control. If the Interrupt Controller does not respond properly, the program issues an error message to the console device and flags the error in CMOS.

6. Interval Timer -- This program sets up the interval timer's channel 0 to issue a pulse in a specific amount of time. The output of channel 0 triggers RST 7.5 in the 8085. If the timer does not respond within the correct time, the program issues an error message and flags CMOS. Channels 1 and 2 of the timer are tested during the serial port test.

7. DMA Controller -- This program tests the DMA Controller by writing to the internal registers of the device and reading back the data to be sure it is correct. It then programs the DMA Controller for a memory-to-memory transfer operation, placing a known data pattern in the source memory block, and issuing the command to execute the transfer operation. The program then compares the data in the source memory block with the data in the destination memory block to determine whether the data was transferred properly. If the data is not correct, an error message is issued and the error is flagged in CMOS.

8. Real Time Clock -- This program determines whether the circuit is issuing a 10Hz signal by programming the Interrupt Controller to respond to the real time clock interrupt (INT 6). If an interrupt does not occur, an error message is generated and the error is flagged in CMOS.

Diagnostics/Bootstrap and System Load

The Multivision Diagnostic/Bootstrap program is contained in the 2732 EPROM. I/O port 9CH controls this EPROM which, when enabled, occupies memory address space 0000H to 0FFFH. Upon power-up or system reset, the EPROM is enabled, control is passed to location 0000H, and program execution begins. Upon successful completion of the diagnostic and bootstrap procedure, the operating system will have been read into a memory bank occupying the address space 0C000H to 0FFFFH, the EPROM is disabled, and control is transferred to address 0C000H.

The EPROM is activated by outputting a "one" to port 9CH; it is deactivated when a "zero" is written to 9CH.

Information is passed from the Diagnostic/Bootstrap program to the operating system through 256 bytes of non-volatile CMOS RAM. Recorded here are the results of the diagnostic portion of the program, the bank number containing the booted operating system, and certain other system parameters such as console baud rate and parity settings. Refer to Section 3, RAM PC board, for details accessing the information stored there.

Table 2.3 contains the layout of the information which is passed to CMOS from the Diagnostic/Bootstrap Program.

Table 2.3. CMOS RAM Layout

Byte(s)	Bit(s)	Usage
00H	7 (MSB)	Diagnostic on Memory Bank 0
	6	Diagnostic on Memory Bank 1
	5	Diagnostic on Memory Bank 2
	4	Diagnostic on Memory Bank 3
	3	Diagnostic on Memory Bank 4
	2	Diagnostic on Memory Bank 5
	1	Diagnostic on Memory Bank 6
	0 (LSB)	Diagnostic on Memory Bank 7
01H	7 (MSB)	Diagnostic on Memory Bank 8
	6	Diagnostic on Memory Bank 9
	5	Diagnostic on Memory Bank A
	4	Diagnostic on Memory Bank B
	3	Diagnostic on Memory Bank C
	2	Diagnostic on Memory Bank D
	1	Diagnostic on Memory Bank E
	0 (LSB)	Diagnostic on Memory Bank F
02H		Bank Number Occupied by System
03H		Mini Disk Booted from 0 - Drive A 1 - Drive B
04H		Hard Disk Diagnostic
05H		CPU Board Port Diagnostic bit 0 - Console fail bit 7 - EIA fail
06H		Serial Port 0 Diagnostic
07H		Serial Port 1 Diagnostic
08H		Serial Port 2 Diagnostic
09H		Serial Port 3 Diagnostic
0AH		Console/Serial Port 0 Baud Rate
0BH		Console/Serial Port 0 Parity
0CH		Serial Port 1 Baud Rate
0DH		Serial Port 1 Parity
0EH		Serial Port 2 Baud Rate
0FH		Serial Port 2 Parity
10H		Serial Port 3 Baud Rate
11H		Serial Port 3 Parity
12H	7 (MSB)	Memory Card 0 Present/Absent
	6	Memory Card 1 Present/Absent
	5	Memory Card 2 Present/Absent
	4	Memory Card 3 Present/Absent
	3	Serial Port Card Present/Absent
	2	Hard Disk Controller Present/Absent
	1,0	--Reserved--
13H-52H		--Reserved--

*See notes regarding this layout on following page

NOTES

1. Memory banks 0-3 reside on RAM PC board 0, banks 4-7 on PC board 1, banks 8-B on PC board 2, and banks C-F on PC board 3. Memory card 0 is in the Multivision 1 Module. Cards 1,2 and 3 are present in the Expansion Module.

2. Bits 7-2 of byte 12H indicate the presence of a PC board if set, or its absence if reset.

3. The memory bank diagnostics in bytes 00H and 01H indicate that a given bank failed the test if it was reset. A set bit indicates either that the bank passed or the bank is not physically present. A memory bank is available for system use if the PC board on which it resides is present in the system, and if it passed the diagnostic test.

4. The disk and port diagnostics (bytes 03H to 09H) are reported as a zero value for pass, nonzero for fail.

5. In a Multivision 1 or 2, the console port is on the CPU PC board, and its baud rate and parity settings are indicated in bytes 0AH and 0BH respectively. In a Multivision 3, the console ports are on the 4 Port I/O Interface PC board in the Expansion Module, and the baud rate and parity settings are given in bytes 0AH to 11H.

6. The correspondence between baud rate settings and baud rates is shown below:

SETTING	BAUD RATE
30H	110
31H	150
32H	300
33H	1200
34H	1800
35H	2400
36H	4800
37H	9600
38H	75
39H	600
3AH	2000
3BH	7200

7. The correspondence between parity settings and parity usage is shown below:

SETTING	USAGE
45H	7 Data Bits, Even Parity
4EH	7 Data Bits, No Parity
4FH	7 Data Bits, Odd Parity

8. Byte 053H is used to maintain an arithmetic checksum on bytes 00H - 052H, and is checked by the Diagnostic Program.

9. Bytes 54H through 0A7H and 0A8H through 0FBH are identical to bytes 00H through 53H. All three blocks should be updated when CMOS data is changed. If the checksum at byte 53H is wrong, then the boot EPROM will use the data in block two. If that too, is wrong, then the data in block three is used. Each block is read in turn until a proper checksum is found. The data in this block is used to update the other two blocks. If all three checksums are incorrect, then all three blocks of CMOS are reinitialized to default values. If no fatal errors are detected by the Diagnostic Program, a system bootstrap is attempted.

   It is assumed that the operator has inserted a disk containing a copy of MUON into drive A. The bootstrap program selects a "good" memory bank, activates it in address space 0C000H through 0FFFH, and reads 16K of data into it starting from track 0, sector 1, side 0 of drive A and proceeds sequentially. The number of the bank selected for bootstrap is recorded in byte 02H of CMOS. Assuming a successful read, the EPROM is disabled and control is passed to address 0C000H.

   This is the means by which the operating system is bootstrapped. MUON then initializes various software structures, programs hardware components such as the PIC, PITs, USARTs and Disk Controllers, and creates a foreground task for each system console. This last part includes acquiring sufficient memory for each task, and reading in the Command Line Interpreter (CLI) from the system disk in drive A. The system scheduler is then set into motion, and task execution begins. Much of the information recorded in CMOS is used during this initialization process.

   Programming examples for the EPROM are shown below:

   1. To deactivate the EPROM:

```
XRA     A           ;Output a zero through the
OUT     9CH         ;EPROM control port.
```

   2. To force a "cold" boot of the operating system, essentially imitating the actions of system power-up or reset in software:

```
DI                  ;Interrupts off.
MVI     A,1         ;Enable the EPROM.
OUT     9CH
JMP     0           ;and begin execution of the
                    ;Diagnostic/Bootstrap program.
```

Functional Description

Two serial I/O ports are provided on the CPU for interface to the system console device (CRT) and a user-definable serial peripheral (printer, modem, etc.). Both ports utilize an 8251A USART to interface from the system to the serial devices. The USART is used to transfer parallel data from the system bus to a serial output line which is RS232C compatible. The primary port is the system console port, which is used to interface the user's device to the system. This port is usable only in an asynchronous mode of operation, with standard baud rates available from 110 to 9600. These baud rates are supplied using channel 2 of the 8253-5 Timer on the CPU PC board. In the standard mode of operation, this port is configured for 9600 baud, odd parity and 2 stop bits. These parameters are redefinable by the user using the SYSMOD Utility of MUON. This port is configured as a Data Set to interface directly to a terminal, eliminating the need for special cables or reversal plugs.

The secondary serial port can be configured in either the asynchronous mode or synchronous mode, depending on the needs of the user. Of the six serial ports on a Multivision 3, only this port is capable of synchronous communications; the other five are asynchronous only. This port, which is configured as a Data Terminal or other Data Set device, may be used to interface to a serial peripheral such as a printer or modem, with the user supplying the necessary software.

Each of the ports is attached to one channel of a 8253 Timer chip which provides the baud rate clock for both transmission and reception through that port. This enables the individual ports to be run at different baud rates and with different frame characteristics.

The two ports on the CPU PC Board make use of interrupts to reduce the burden placed on the system software for interfacing these I/O ports. Two interrupts can be generated by each device. The highest priority interrupt is the receiver ready interrupt, which is used to signal the system that the USART has a character to be read from its internal receive data buffer. The second interrupt generated is used to signal the system that the transmit buffer is empty and the USART is ready to transmit another character from the system to the serial device.

Port Assignments

The I/O port assignments for the console and communications ports on the Multivision 1 Module are shown in Table 2.4 below:

Table 2.4. I/O Port Assignments for Multivision 1

Port	Usage
88H	Read: Data received, console port Write: Data to transmit, console port
89H	Read: Port status, console port Write: Command register, console port
8CH	Read: Data received, communications port Write: Data to transmit, communications port
8DH	Read: Port status, communications port Write: Command register, communications port
90H	Write only: Bit 0: 1 = Loop test on Bit 1: 1 = Synchronous mode enabled on communications port
91H	Read only: Bit 0: Communications clear to send complement Bit 1: Communications carrier detect complement Bit 2: Communications reverse channel complement Bit 3: Console clear to send complement Bit 4: Console carrier detect complement Bit 5: Console reverse channel complement

The baud rate clocks for the communications and console ports respectively, are counters 1 and 2 of the 8253 Timer in the Multivision 1 Module. They are programmed by ports 81H through 83H as follows:

Port	Usage
81H	Counter 1: Communications port counter
82H	Counter 2: Console port counter
83H	Timer command register

For a description of how to program this chip, see the topic entitled Programmable Internal Timer (PIT) 8253-5.

The 8251A chips in the Multivision 1 Module are directly tied to several interrupt lines. Console data received activates RST 5.5 and communications data received activates RST 6.5. The console transmitter ready will raise interrupt line 7 and the communication transmitter ready will raise interrupt line 5 on the 8259 Interrupt Controller. Each of these signals is individually maskable.

For RS232 serial interfaces, there are two important configurations of the control lines. One is referred to as Data Terminal, the other is referred to as Data Set. The two configurations are functionally complementary. A Data Terminal device is intended to be plugged into a Data Set device, and vice-versa. In specific terms, a Data Terminal controls the signals Data Terminal Ready (DTR) and Request To Send (RTS) while reading the state of the signals Clear to Send (CB), Data Set Ready (DSR), and Carrier Detect (CF). For a Data Set, the exact opposite is true.

The console port on the Multivision 1 Module and the four serial ports of the Expansion Module are configured as Data Sets so that terminals, which are the Data Terminal configurations, may be plugged directly into them. Raising the RTS signal on one of these ports will raise the CB signal. This will become noticeable to the terminal plugged into that port and also to the CF signal. Raising the port's DTR signal will cause the attached terminal to perceive the rise of DSR. The Multivision 1 communications port is, however, a Data Terminal intended to be connected to a Data Set.

Programming The 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This format defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be inserted.

Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components sharing the same package: one Asynchronous and the other Synchronous. The format definition can be changed only after a master chip Reset.

When parity is enabled, it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data Line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

1. Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU, the 8251A automatically adds a start bit (low level) followed by the data bits (least significant bit first), and the programmed number of stop bits to each character. Also, an even or odd parity bit is inserted prior to the stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{\text{TxC}}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{\text{TxC}}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A, the TxD output remains "high" (marking) unless a BREAK (continuously low) has been programmed.

2. Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists), and the stop bits. If a parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of RxC. If a low level is detected as the STOP bit, the FRAMING Error flag will be set. The STOP bit signals the end of a character. The receiver requires only one STOP bit, regardless of the number of STOP bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

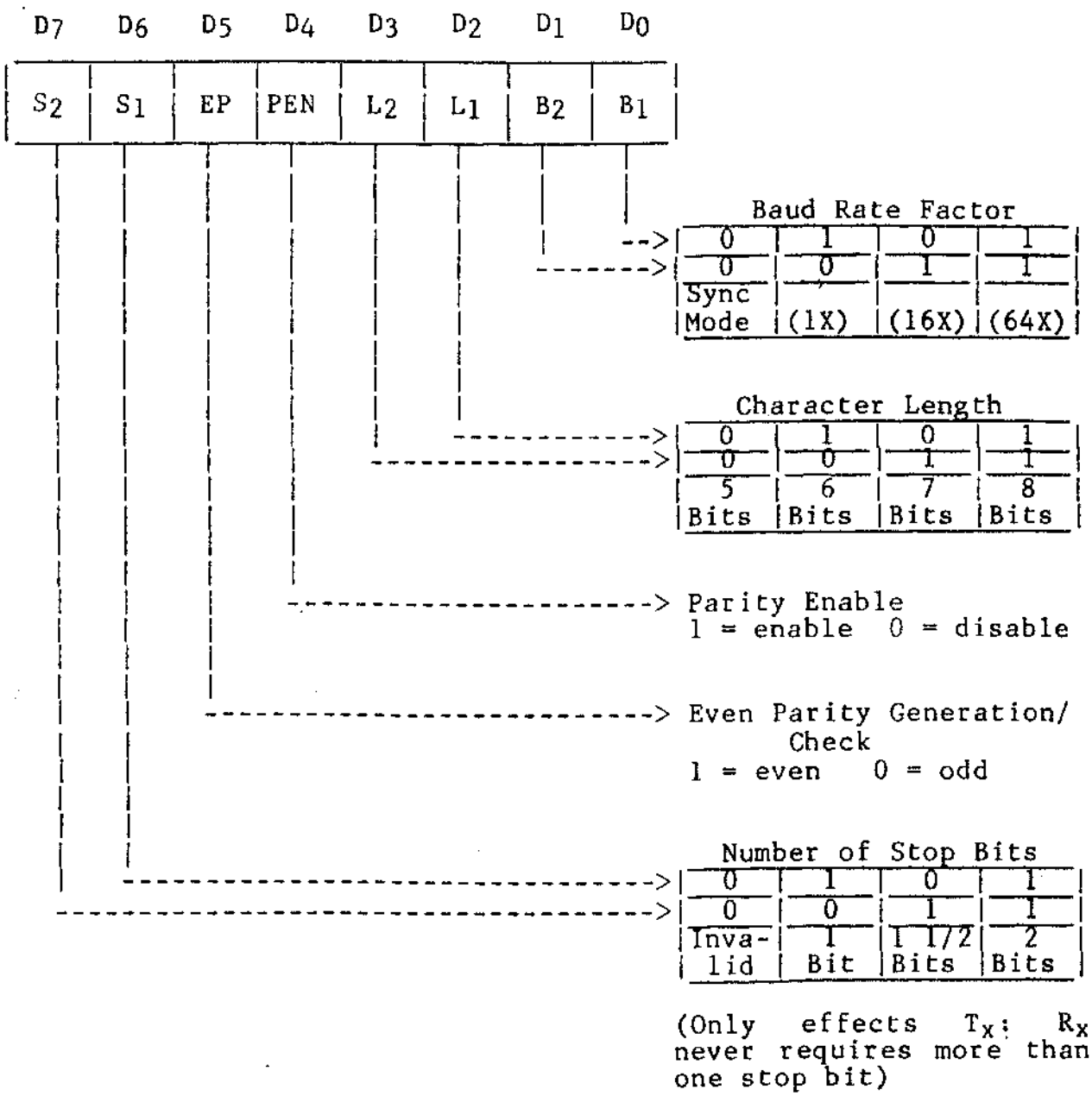
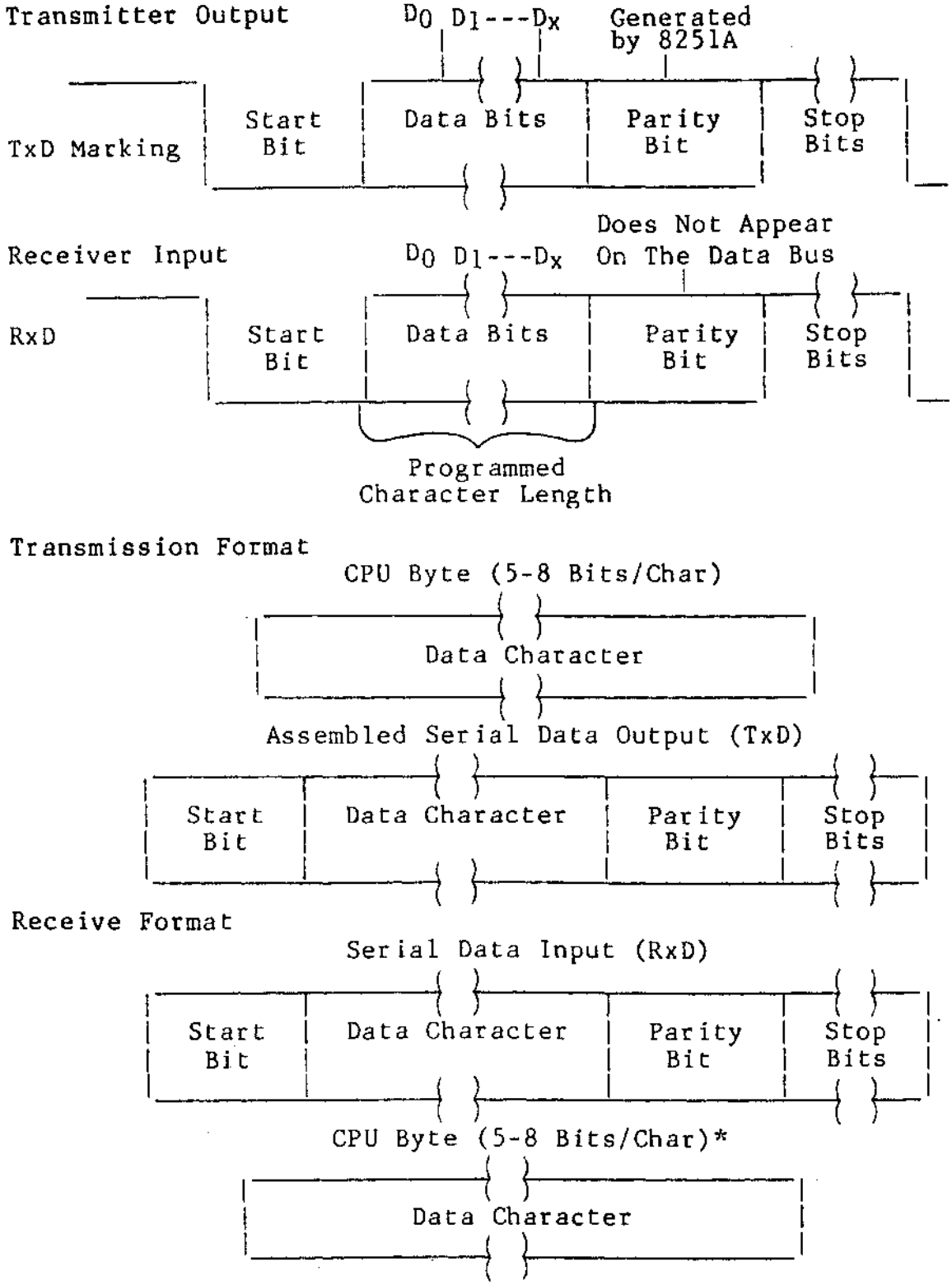


Figure 2-2. Mode Instruction Format - Asynchonous



*If character length is defined as 5, 6 or 7 bits, the unused bits are set to zero.

Figure 2-3. Asynchronous Mode

3. Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A, which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see Figure 2-4 below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.

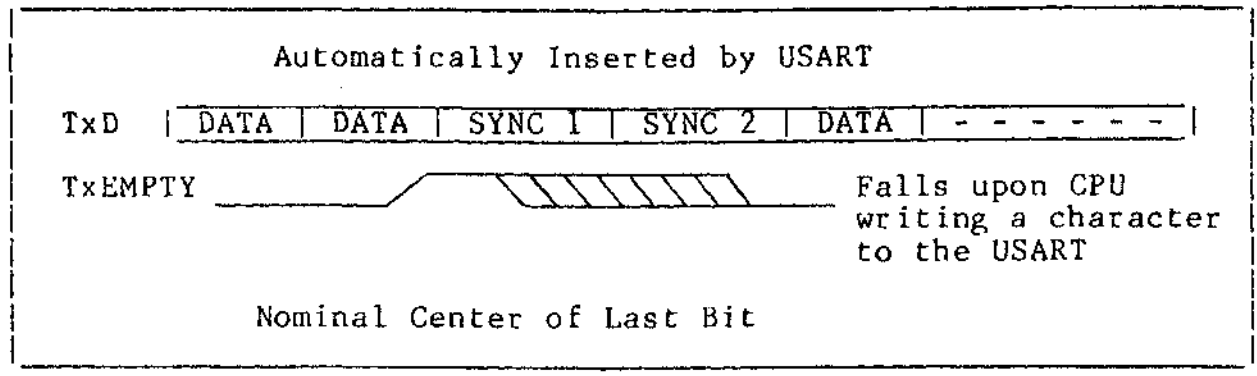


Figure 2-4. TxEMPTY Pin

4. Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, an ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity errors and overrun errors are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in HUNT, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. The SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, Sync Detection is still functional, but it only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character SYNC has been programmed, then both SYNC characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

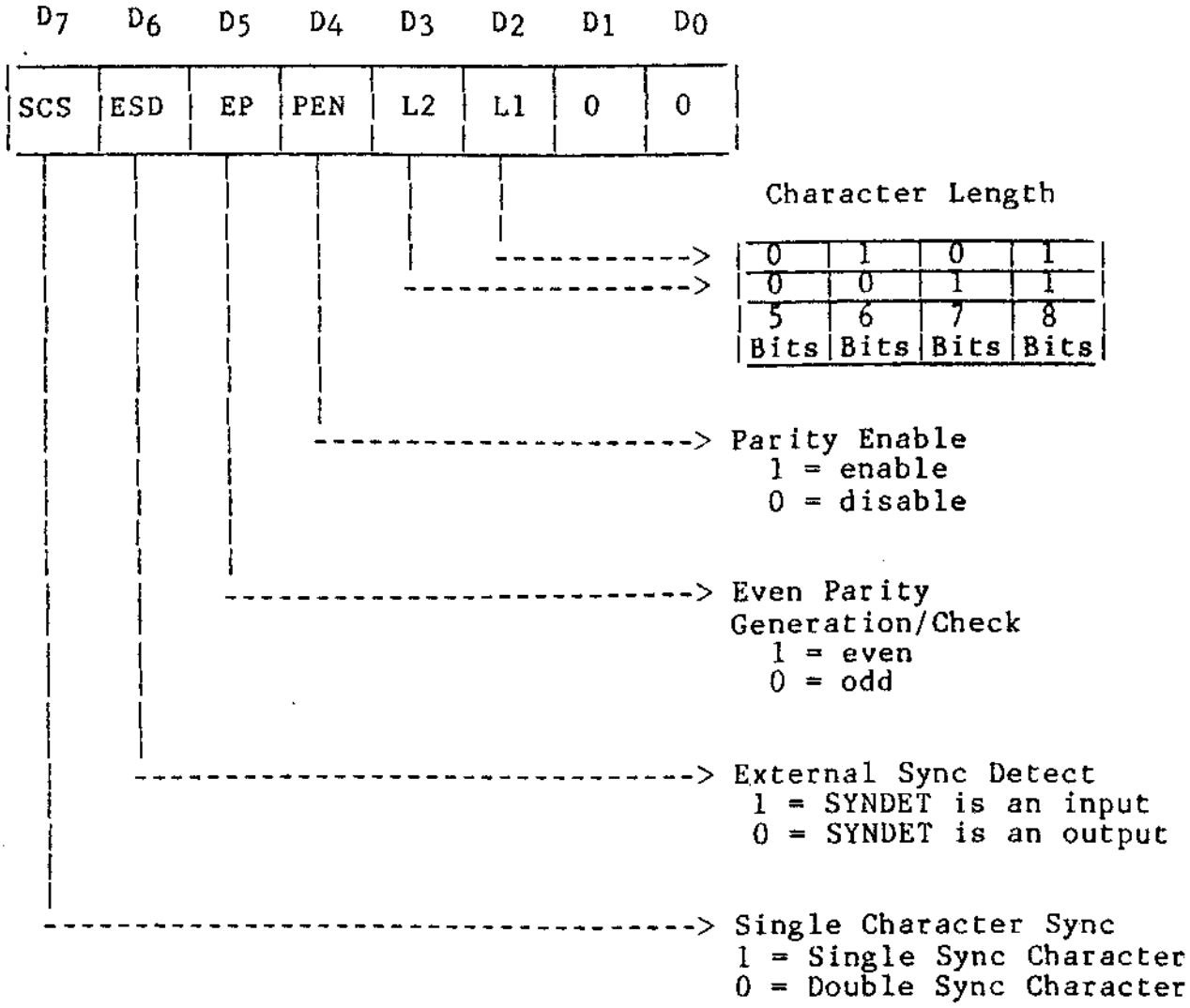
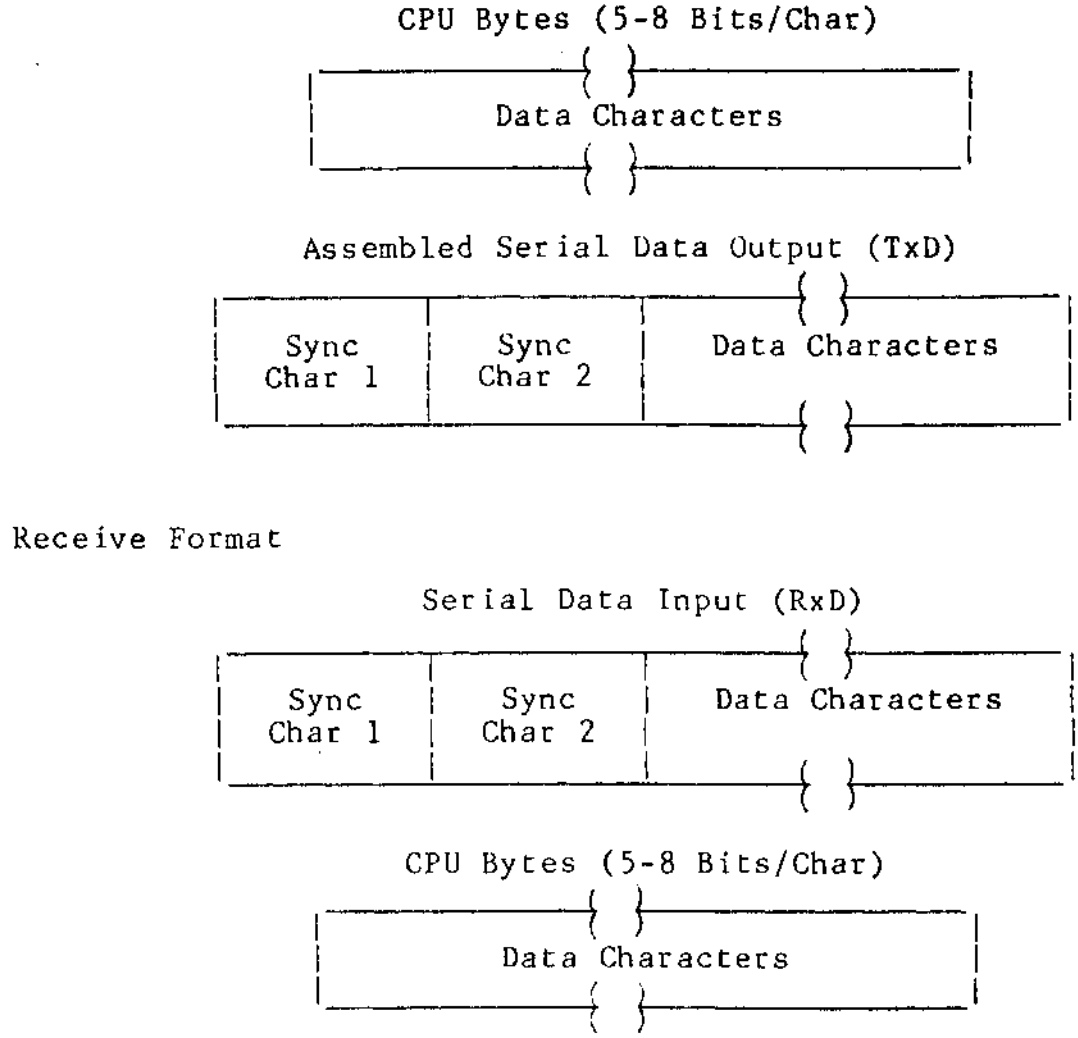


Figure 2-5. Mode Instruction Format



Receive Format

Figure 2-6. Data Format - Synchronous Mode

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time during its operation. To return to the Mode Instruction format, set the Reset bit in the Command Instruction word. The internal Reset operation will automatically place the 8251A into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

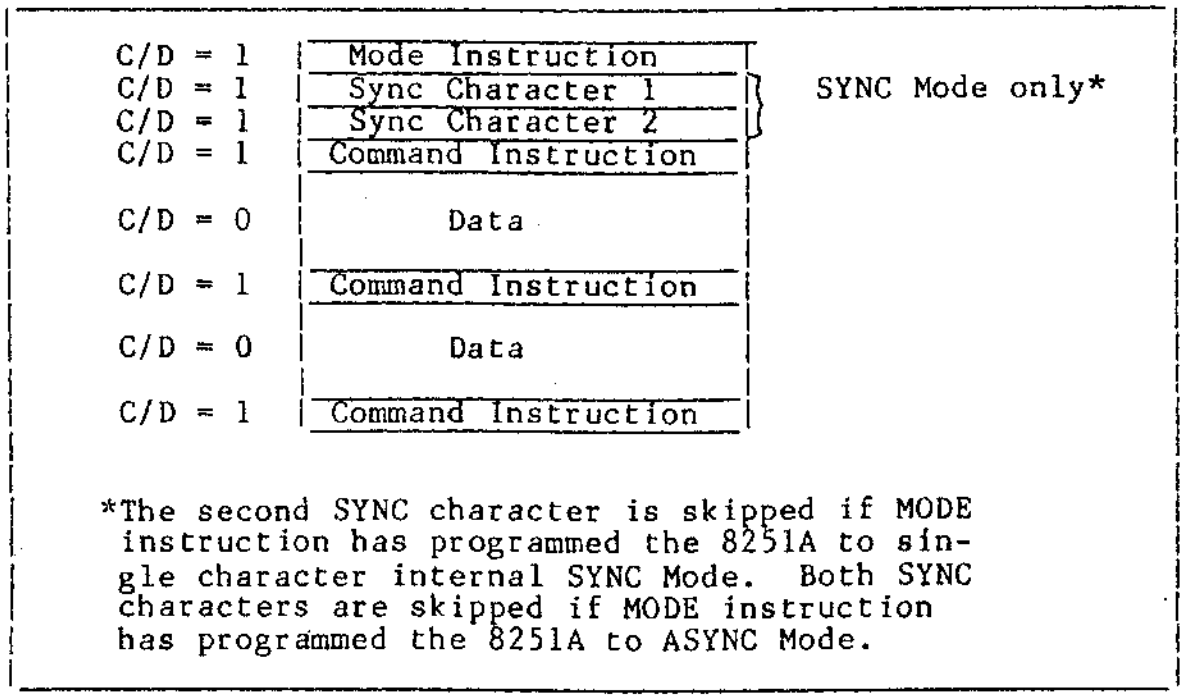
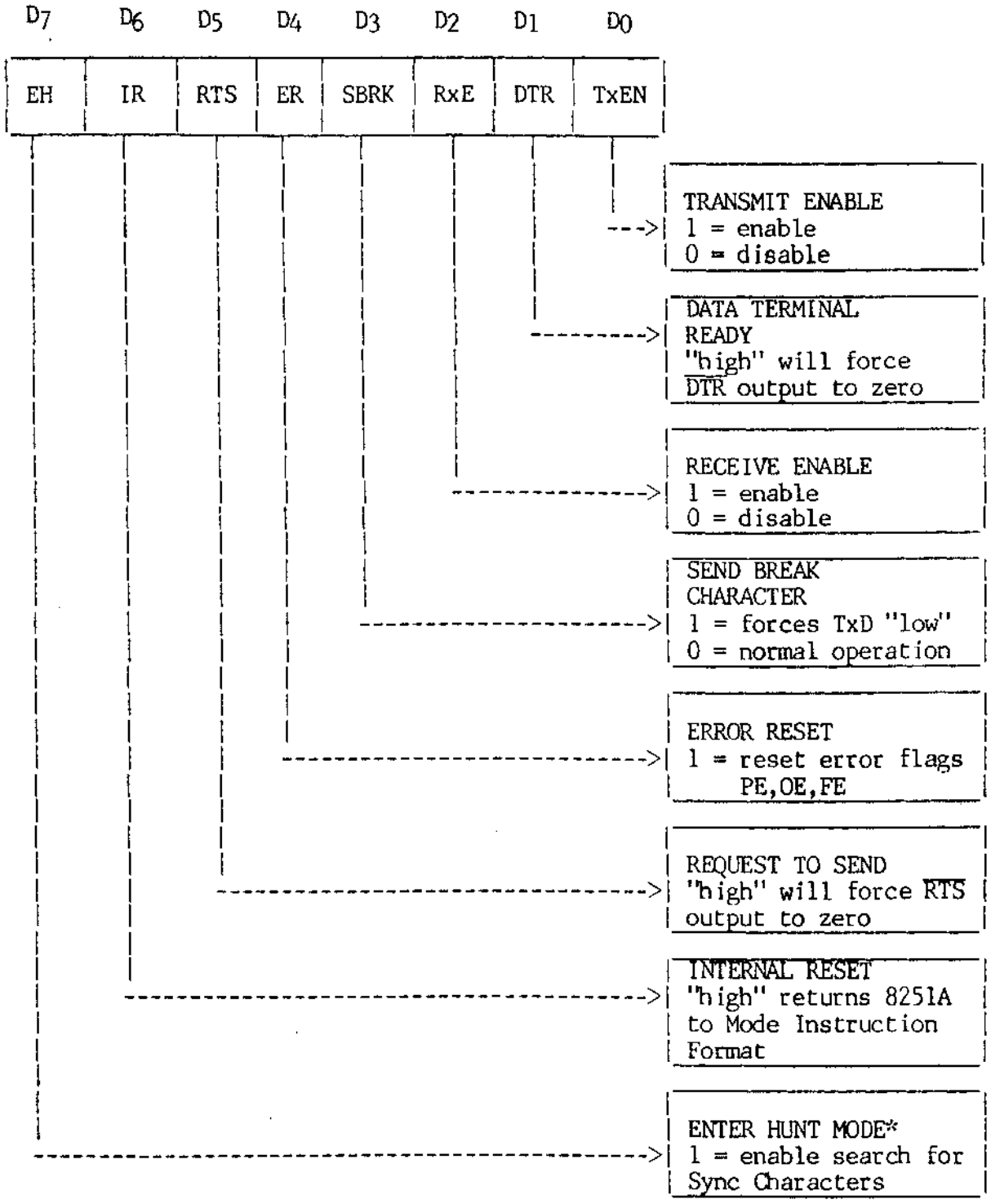


Figure 2-7. Typical Data Block



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 2-8. Command Instruction Format

Command Instruction Definition

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode), then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as Enable Transmit/Receive, Error Reset, and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.

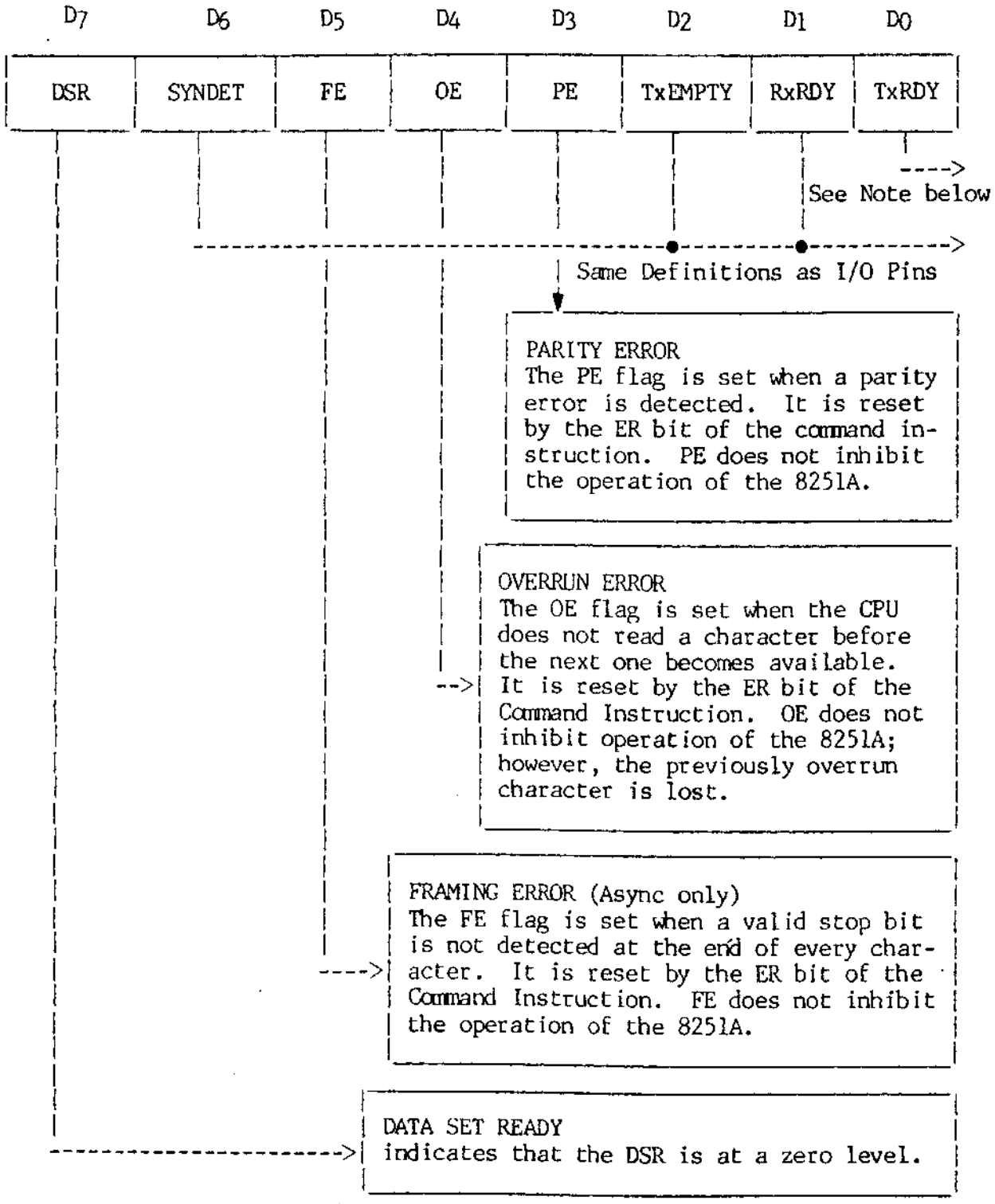
Status Read Definition

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (The status update is inhibited during status read.)

A normal "read" command is issued by the CPU with $C/\overline{D}$=1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely Polled environment or in an interrupt driven environment. TxRDY is an exception.

Status updates can have a maximum delay of 28 clock periods from the actual event affecting the status.



Note: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.
i.e., TxRDY status bit = DB Buffer Empty
TxRDY pin out = DB Buffer Empty (CTS = 0)(TxEN = 1)

Figure 2-9. Status Read Format

Functional Description

The CPU uses an 8253-5 Programmable Interval Timer for baud rate generation for the two serial ports, and to provide a timing reference for the operating system. Channel 0 of this port is used as the timing reference for the operating system, and to trigger an interrupt to the 8085A (RST 7.5). This interrupt is used for task switching operations and other operating system-oriented timing requirements. Channels 1 and 2 are used to provide the baud rates for the two serial ports on the CPU.

Two additional PITs are on the 4 Port I/O Interface PCB; they provide baud rate timing for the serial ports on the board. All timing done by the Timer is with reference to the 2MHz comm clock signal generated in the oscillator section of the CPU. By counting the specified number of cycles, the timer is able to provide the proper outputs for this function.

For programming information concerning use of this component, refer to the appropriate Intel manuals.

Programming PITs

The PITs are programmed as I/O peripherals using the following port assignments:

Port	Usage
58H	Counter 0: Serial Port 2
59H	Counter 1: Serial Port 3
5AH	Counter 2: -- Reserved --
5BH	Timer Command Register
5CH	Counter 0: Serial Port 0
5DH	Counter 1: Serial Port 1
5EH	Counter 2: -- Reserved --
5FH	Timer Command Register
80H	Counter 0: RST 7.5
81H	Counter 1: Communications Port
82H	Counter 2: Console Port
83H	Timer Command Register

Each counter of an 8253 may be programmed by issuing a series of control words specifying its operational characteristics. The hardware specifications for the PIT along with a full description of the modes of operation are given in the Intel Component Data Catalog. The options used by MUON in programming the PITs are:

1. Mode 3 - A square wave rate generator is used;

2. 16-bit binary countdown value, the value of which depends upon the actual use of the counter.

Examples of PIT programming are shown below:

1. The MUON Task Scheduler expects a timing interrupt every five milliseconds on the RST 7.5 line. This is provided by programming Counter 0 of the PIT residing on the CPU PC board.

SETPIT:

```
DI                  ;Interrupts off.
MVI     A,36H       ;Select Counter 0, Mode 3, binary
OUT     83H         ;countdown value.
LXI     B,10000D    ;10,000 cycles of a 2MHz clock yields
MOV     A,C         ;a 5mS interval - output low order
OUT     80H         ;byte first, to Counter 0
MOV     A,B         ;then high order byte.
OUT     80H
EI                  ;Interrupts back on.
RET                 ;Exit.
```

2. Several of the PIT counters are used to time the rate at which characters are output through various USARTs. The table below lists the character baud rates supported by MUON along with the required timing values (in decimal), based on a 2MHz clock:

Baud Rate	Countdown Value
75	1666
110	1136
150	833
300	416
600	208
1200	104
1800	69
2000	65
2400	52
4800	26
7200	17
9600	13

The following routine programs console port 1 on the 4 Port I/O Interface PCB for 9600 baud operation:

BAUD 01:

```
DI                  ;Interrupts off.
MVI     A,76H       ;Select Counter 1, Mode 3, binary
OUT     5FH         ;countdown value.
LXI     B,13D       ;13 cycles on a 2MHz clock ensures
MOV     A,C         ;9600 baud operation - low order
OUT     5DH         ;byte first, then
MOV     A,B         ;high order byte
OUT     5DH         ;to Counter 1.
EI                  ;Interrupts on.
RET                 ;Exit.
```

The CPU uses an 8259A Programmable Interrupt Controller to increase the number of interrupts available within the system from 5 (using only the 8085 supported lines) to 12 using the 8085 INTR line as an interface to the Controller. Each of the 8 channels of the Controller can be individually programmed to recognize the interrupt and issue the vector address for the interrupt service routine. (One interrupt, TRAP, is used only for Multivision development and is not available to user.) This is accomplished using the signal INTR to the 8085A. On receipt of this signal, the 8085A issues the signal INTA. When the Controller receives this signal it places a jump instruction onto the data bus, which notifies the 8085A that the Controller has an address vector to issue. The 8085A issues two INTA pulses which are used by the Controller to place the address information onto the data bus. This information is captured by the 8085A and the processor then jumps to that address, which contains the interrupt service routine for the channel triggering the interrupt.

Information regarding the 8085 interrupts serviced, their vector addresses, and programming information for the controller are contained in Intel's Component Data Catalog and MCS-85 User's Manual.

The vector associated with the PIC is a table of addresses which is used to "point" the program counter to the appropriate service routine when a PIC-controlled interrupt is generated. The PIC itself is programmed by the system software as an I/O peripheral by a sequence of initialization and command words. The I/O ports assigned to the PIC are as follows:

Port	Usage
84H	Command/Status
85H	Command/Status

The eight interrupt lines into the PIC are assigned in Multivision as shown in Figure 2-10 below.

Line	Usage
0	Memory Parity
1	Serial Port Receiver (SIO PCB)
2	Serial Port Transmitter (SIO PCB)
3	Mini Disk Controller
4	Hard Disk Controller
5	Communications Port Transmitter (CPU)
6	60 cycles/second Clock
7	Console Port Transmitter (CPU)

Figure 2-10. PIC Interrupt Lines

MUON uses the following options in programming the PIC:

1. Level Interrupt Mode -- The edge detect logic on the interrupt inputs is disabled,

2. Call Address Interval = 4 -- A compact vector of service addresses is used, with four (rather than eight) bytes per entry,

3. Auto End-of-Interrupt Mode -- The in-service bit for a given interrupt is automatically reset at the end of the interrupt acknowledge pulse,

4. Vector Address = 0C020H -- This is the memory address used by the operating system for the table of actions to be performed for a given interrrupt.

Depending upon whether the system is configured as a Multivision 1, 2 or 3, only certain interrupt lines are actually serviced by MUON:

1. Line 0 (Memory Parity) is enabled in all Multivision systems,

2. Lines 1 and 2 (Serial Port Receiver and Transmitter) are enabled only in Multivision 3,

3. Line 3 (Mini Disk Controller) is always enabled,

4. Line 4 (Hard Disk Controller) is enabled only in Multivision 2 and 3,

5. Line 5 (Communications Port Transmitter) is enabled by MUON's SYSGENable serial printer driver or communications services,

6. Line 6 (10 Cycles/Second Clock) is not used by MUON; it is a customer programmable option,

7. Line 7 (Console Transmitter) is enabled only in Multivision 1,

8. TRAP is used only for Multivision development,

9. RST 7.5 (Timer) is always enabled,

10. RST 6.5 (Comm Port Receiver) is always enabled,

11. RST 5.5 (Console Receiver on CPU board) is enabled only for Multivision 1.

Sample code segments of PIC programming are shown below:

1. To program the PIC for a Multivision 1 system:

```
SETPIC:

        DI                      ;Interrupts off for PIC manipulation.
        LXI     H,0C020H        ;PIC vector is at this address.
        MVI     A,1FH           ;Single PIC, level interrupt mode
        ORA     L               ;combined with low order byte of PIC
        OUT     84H             ;address makes up initialization word 1.
        MOV     A,H             ;Initialization word 2 is high order
        OUT     85H             ;byte of PIC address.
                                ;Initialization word 3 not necessary
                                ;for single PIC.
        MVI     A,02H           ;Auto end of interrupt mode specified
        OUT     85H             ;in initialization word 4.
        MVI     A,76H           ;Enable transmitter, mini disk, parity
        OUT     85H             ;interrupts in operation command word 1.
        EI                      ;Interrupts on.
        RET                     ;Exit
```

2. To determine by reading the PIC status, which interrupt lines are presently enabled (the interrupt mask is returned in the A register):

```
RDPIC:

        IN      85H             ;Read status.
        RET
```

Functional Description

The Real Time Clock circuit is designed to produce a 10Hz signal by monitoring the AC line frequency. This is accomplished using a 4-bit binary counter, preset to either 10 or 11. As the counter is incremented past this preset it will trigger an output after every 6 or 5 line cycles. This produces the required 10Hz output from the circuit. The output is then used to trigger a flip-flop, the output of which is used to trigger the interrupt input of the 8259A. This circuit can be used as a real time counter to produce time-of-day measurements or computer time used in a time-sharing operation. This circuit is not used or supported by the system for any purpose, and it is necessary for the user to provide any software drivers for its use. After each interrupt, the circuit must be reset in order to trigger on the next output of the 10Hz counter. Issuing an I/O write to port 94H accomplishes the reset. Interrupt line 6 is used by the 8259A to monitor this circuit. In order to preset the circuit for 50HZ or 60Hz operation, a wire jumper must be installed at location JP1 or JP2 on the CPU PC board, JP2 for 50Hz, JP1 for 60Hz.

Real Time Clock Interrupt Routine

To make use of this interrupt for a Real Time Clock, an interrupt handling routine must be written and the interupt enabled.

An example of a Real Time Clock Interrupt Routine is shown below:

```
        Real Time Clock Interrupt Service Routine
        Note:  Hrs, Mins, Sec & 10th Sec are kept in ASCII
Calling Parameters
        None
Registers Modified
        None
Global Variables Modified
        None
Routines Called
        IRTIME
```

```
RTCINT: PUSH    H               ;Save all registers.
        PUSH    D
        PUSH    B
        PUSH    PSW

        OUT     94H             ;Clear the Real Time Clock Interrupt.
        EI                      ;Enable interrupts.

        LXI     H,TENRTC        ;Increment 10 sec. counter.
        INR     M
        MVI     A,'9'
        CMP     M               ;Is it > 9?
        JNC     RTCI01          ;Jump if no to exit.

        MVI     M,'0'           ;Clear 10th sec. counter.

        DCX     H               ;Point to least significant byte -
        DCX     H               ;of seconds.

        CALL    IRTIME          ;Increment seconds.
        JNC     RTCI01          ;Overflow? - jump if no to exit.
        DCX     H               ;Point to least significant byte -
        DCX     H               ;of minutes.

        CALL    IRTIME          ;Increment minutes.
        JNC     RTCI01          ;Overflow? - jump if no to exit.

        DCX     H               ;Point to least significant byte -
        DCX     H               ;of hours.

        CALL    IRTIME          ;Increment hours.

        ;IS HOUR > 24 ?

        MVI     A,'2'           ;Most significant byte > 2?
        CMP     M
        JNZ     RTCI01          ;Jump if no to exit.

        INX     H               ;Most significant byte = 2.
        MVI     A,'4'           ;Check least significant byte.
        CMP     M               ;Is it = 4?
        JNZ     RTCI01          ;Jump if no to exit.

        ;Reset Hours to Zero

        MVI     A,'0'           ;Zero most significant byte,
        MOV     M,A
        DCX     H               ;then least significant byte.
        MOV     M,A
```

```
RTCI01: POP     PSW             ;Restore all registers.
        POP     B
        POP     D
        POP     H

        RET                     ;Return.
```

```
IRTIME
        Increment Time, If Time> 59 Set It To Zero
Calling Parameters
        HL = Pointer To LSB Of Hours, Minutes or Seconds
Returning Parameters
        HL = Points To MSB
        CY = 1 If Reset To Zero Occurred
Registers Modified
        PSW, HL
Global Variables Modified
        None
Routines Called
        None
```

```
IRTIME: INR     M               ;Increment least significant byte.
        MVI     A,'9'
        CMP     M               ;Is it > 9?
        JNC     IRTI01          ;Jump if no to exit.
        MVI     M,'0'           ;Zero it.

        DCX     H               ;Point to MSB.
        INR     M               ;Increment it.
        MVI     A,'5'
        CMP     M               ;Is most significant byte > 5?
        JNC     IRTI02          ;Jump if no to exit.

        MVI     M,'0'           ;Zero it.
        JMP     IRTI02          :Exit.

IRTI01: DCX     H               ;Point HL to most significant byte.

IRTI02: RET


:       RAM AREA FOR REAL TIME CLOCK

HRSRTC: DB      '00:'           ;Hours - initialized to zero
MINRTC: DB      '00:'           ;Minutes
SECRTC: DB      '00:'           ;Seconds
TENRTC: DB      '0'             ;Tenth Second Counter

END
```

20MHz OSCILLATOR

The oscillator circuit is a simple crystal-controlled 20MHz oscillator. The output of this circuit is used to provide the 10MHz fundamental frequency for the 5MHz 8085A and also generates the 2MHz Comm Clock used by most system peripherals as the internal timing reference in these peripherals.

ADDRESS DECODING

The address decoding circuit provides the address select signal for all on-board devices, combining the proper address select with the signal IO/M* to gate the devices when the correct I/O port is selected by the processor. The circuit also provides the signal ON BD*, which is used by the CPU to gate the data busses for proper data flow, and the Shadow ROM enable signal PROMSEL*, which when active selects the shadow ROM and triggers ON BD to assure proper data bus selection. The CPU I/O port addresses are from I/O port 0-F and 80-BF. Any access to these I/O ports will trigger the proper device and the ON BD* signal.

The following table lists the I/O port assignments for the CPU:

Table 2.5 I/O Port Assignments for the CPU

Port Number	Assignment
I/O PORT 0-F	Reserved for future use
I/O PORT 80-83	Timer ports 80- Channel 0 81- Channel 1 82- Channel 2 83- Command/status port
I/O PORT 84-85	Interrupt Controller Command Ports
I/O PORT 86-89	Console Serial Port 88- data 89- command
I/O PORT 8C-8D	Secondary Serial Port 8C- data 8D- command
I/O PORT 90	Serial Port Control bit 0 -Looptest Looptest for system b0 high=on diagnostic test b0 low=off Sync/async for bit 1-sync/async user supplied b1 high=sync communications b1 low =async
I/O PORT 91	Serial I/O port communication status read only port b0=CTS* b1=ACF* b2=ASCF* b3=BCTS* b4=BCF* b5=BSCF*
I/O PORT 92	CMOS Memory Address Latch
I/O PORT 93	CMOS Memory Data Access
I/O PORT 94	Real Time Clock Reset - I/O write clears this signal
I/O PORT 98	CMOS Memory Enable Circuit b2 high=on b2 low =off
I/O PORT 9C	Shadow ROM Enable Circuit b0 high=on b0 low =off
I/O PORT A0-AF	DMA Controller Select - see topic on DMAC in this section for individual port assignments.

The CPU controls all system bus operations, either through the 8085A-2 or the DMA Controller 8237-2. All signals transmitted to and from the system bus are buffered to reduce bus noise and to minimize signal loading. Use of Schmidtt triggered devices wherever possible provides additional noise reduction to and from the bus. Most bus signals are active-low to again reduce noise sensitivity within the system.

The CPU bus structure is comprised of both an on-board bus and interface circuitry to the system bus. To eliminate bus contention problems, the CPU uses the signal ON BD* which allows the CPU access to only one bus at a time. When an onboard device is selected, the address decoding circuitry generates the ON BD* signal which switches bus access from the system bus to the onboard bus. Because data busses are the only busses which are bidirectional, they are the only busses affected by the ON BD* signal.

The 8085 and the 8237 share a common address/data bus (AD0-AD7) which is used to multiplex 8 address lines and 8 data lines. The 8085 makes use of the signal ALE to separate the address information from the bus during the first clock cycle of an instruction cycle. This is accomplished by latching the address information in an 8-bit latch at the trailing edge of the ALE signal. The 8 address bits are then placed on the address bus by the output of the 8-bit latch. The DMA controller uses this combined bus in much the same fashion. During DMA sequences, the controller places 8 address bits on the bus and latches them to a separate 8-bit latch using the signal ADSTB. This is accomplished during the first clock cycle which frees the bus for data transfer at the end of the clock cycle. The 8085 uses the lower 8 address bits (A0-A7) in this combined bus, while the DMA controller uses the upper 8 address bits (A8-AF).

The 8085 and 8237 both use bidirectional data transceivers, which are two 8304 8-bit data buffers. One buffer is used between the AD0-AD7 bus and the system data bus (DAT0-DAT7)and the other buffer is used between the AD0-AD7 bus and the onboard data bus (DB0-DB7). When the signal ON BD* is active (low), the system bus is deselected and the onboard data bus is activated. The 8304's can operate either in transmit (from 8085, 8237) or receive (to 8085, 8237) mode. The direction of data transfer is determined by the status signal BS1. This signal is generated by the 8085 during a read operation, or by a memory read during DMA memory to memory transfers. The devices are enabled during the actual read or write operation, providing a "window" for data transfer. During non-data transfers, the devices are in a tri-state mode, allowing the bus to remain inactive.

The system address bus (ADR0-ADRF) originates from the CPU PC board. This 16-bit bus can address 64K of memory space, and also access the 256 I/O ports available for the 8085. The CPU contains peripheral devices using the I/O port numbers 0-F and 80-BF. Memory space from 0-0FFF is used for the shadow EPROM; this memory space is activated through an I/O port and may be switched off to free the memory space for system use whenever the shadow EPROM is not in use. While the shadow EPROM is switched on, any access to this memory space blocks out system memory in order for the EPROM to be accessed without bus contention, due to multiple memory access.

All system control signals (RD, WR, etc.) are generated on the CPU. Bus access for all other elements within the system has been simplified by using a single source for all system control. System elements are accessed by using their proper address decodes. Bus access for these elements is controlled by the CPU.

The Multivision backplanes utilize a 100 pin common bus orientation, enabling the use of any Multivision PC boards in any slot of the card cage. The backplanes have an internal ground plane (multilayered PCB) to reduce noise transmission from signal to signal and to provide reduced noise levels on all signals.

The Multivision 1 backplane includes an opto isolator circuit to provide a TTL level 10Hz signal to the CPU for the real time clock circuit, eliminating the danger of shorting the PCB to the AC line. The backplanes are connected directly to the power supplies of each module to provide DC power to the system.

The two backplanes are connected with forty and fifty pin flat ribbon cables to ensure that the backplanes cannot be connected improperly. All signals are carried through these cables, including several ground pins to prevent potential differences between the two supplies. The CPU, being the originating PCB for most signals, is placed in the top slot of the system backplane to produce the least possible noise on the backplanes.

Table 2.6. Pinouts For 100 Pin Bus

Pin #	Signal	Meaning
1	RSW*	Reset switch input to CPU Board
2	RTC	Real Time Clock AC Frequency input to CPU
3	GND	
4	GND	
5	DAT 0	8 Bit bi-directional Data Bus
6	1	
7	2	
8	3	
9	4	
10	5	
11	6	
12	7	
13	GND	
14	GND	
15	CAS 0	Cascade input for use with interrupt controller on CPU in event of interrupt structure expansion
16	WAIT*	CPU or DMA not ready signal
17	INT 0*	Parity interrupt
18	1*	Serial I/O board receiver interrupt
19	2*	Serial I/O board transmitter interrupt
20	3*	Mini Disk Controller interrupt
21	4*	Hard Disk Controller interrupt
22	Not Used	
23	GND	
24	GND	

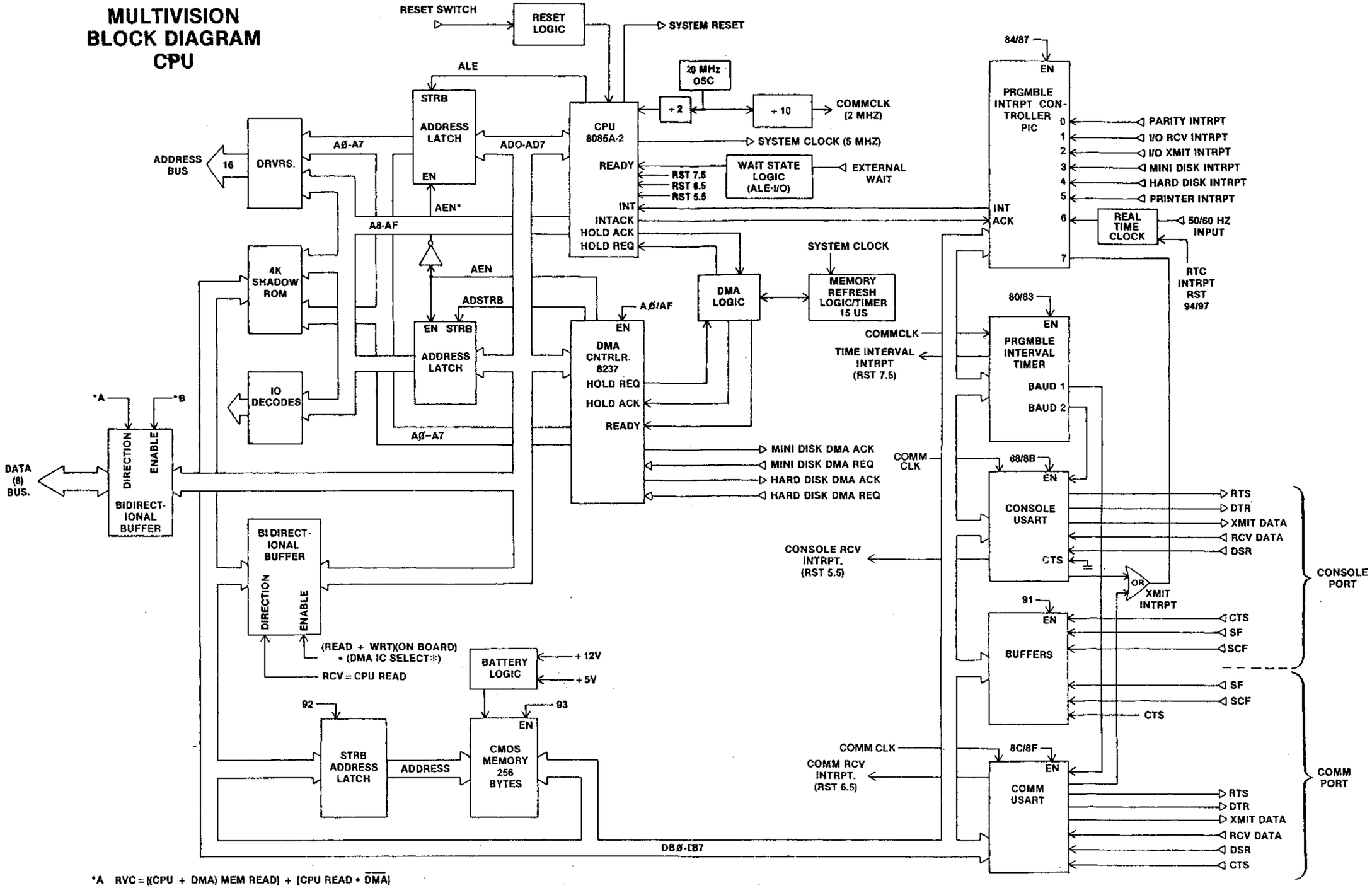
Table 2.6. Pinouts For 100 Pin Bus (continued)

Pin #	Signal	Meaning
25	MRD*	Memory Read signal issued by CPU
26	IORD*	I/O Read signal issued by CPU
27	GND	
28	GND	
29	MWR*	Memory Write signal issued by CPU
30	IOWR*	I/O Write signal issued by CPU
31	GND	
32	GND	
33	IO/M*	I/O Memory Status signal
34	ALE*	Address latch enable signal issued by CPU
35	S 0	Status signals providing operational status
36	S 1	of 8085 (see INTEL manual)
37	GND	
38	GND	
39	-12 V	
40	-12 V	
41	GND	
42	GND	
43	+5 V	
44	+5 V	
45	+5 V	
46	+5 V	
47	GND	
48	GND	
49	+12 V	
50	+12 V	
51	GND	
52	GND	
53	DREQ 0	DMA Request channel 0 (reserved)
54	DREQ 1	DMA Request channel 1 (reserved)
55	DACK 0	DMA Acknowledge channel 0 (reserved)
56	DACK 1	DMA Acknowledge channel 1 (reserved)
57	DREQ 2	DMA Request 2 (Mini Disk Controller)
58	DREQ 3	DMA Request 3 (Hard Disk Controller)
59	DACK 2	DMA Acknowledge 2 (Mini Disk)
60	DACK 3	DMA Acknowledge 3 (Hard Disk)
61	BGRT*	Bus Grant (reserved for expansion of system control capability)
62	BREQ*	Bus Request
63	TRAP*	Trap interrupt of 8085 used by system monitor card (MV CE PCB 129-26900)
64	INH 2*	Bus inhibit signal issued by system monitor card
65	EXWT*	Sent by serial I/O controller to inhibit CPU operation during data capture from serial ports by FIFO circuit on serial I/O board
66	INTA*	Interrupt acknowledge issued by CPU
67	Spare	
68	SRESET*	System reset signal
69	GND	

Table 2.6. Pinouts For 100 Pin Bus (continued)

Pin #	Signal	Meaning
70	GND	
71	ADR 0*	16 bit address bus controlled by CPU
72	1*	
73	2*	
74	3*	
75	4*	
76	5*	
77	6*	
78	7*	
79	8*	
80	9*	
81	A*	
82	B*	
83	C*	
84	D*	
85	E*	
86	F*	
87	GND	
88	GND	
89	Spare	
90	Spare	
91	Spare	
92	Spare	
93	GND	
94	GND	
95	REFCNT*	Refresh Count Timing Signals issued by CPU to
96	REFR*	Refresh dynamic memory refresh operation
97	GND	
98	GND	
99	COMCLK*	2 MHz system clock
100	SCLK*	5 MHz system clock

MULTIVISION BLOCK DIAGRAM CPU



*A RVC = [(CPU + DMA) MEM READ] + [CPU READ • $\overline{DMA}$]

*B EN = [(CPU + DMA) (READ + WRITE)] • $\overline{DMA}$ • $\overline{ON\ BOARD}$

Figure 2-11. CPU PC Board Block Diagram

OVERVIEW

The Multivision Dynamic RAM PCB (129-23300) is a 64K byte RAM designed to operate with a 5MHz 8085A in a Multivision system. The basic memory element is the industry standard 16K x 1 Dynamic RAM. Features on the RAM board include refresh address generation, parity error detection, programmable bank selection and addressing, and DMA capability.

REFRESH AND HOLD LOGIC

The Dynamic RAM I.C.'s used on this board require that each memory cell be refreshed at least once every 2mS. A refresh operation is defined as setting up an address and applying a RAS pulse. This causes the 128-bit cells in the chip with that address to be refreshed. Thus, a memory read or a memory write cycle are both refresh operations. Since there is no guarantee during the course of normal CPU program execution that all RAM locations will be accessed every 2mS, it is necessary to insert special 'refresh only' cycles. The Multivision system supports a distributed refresh mechanism, through circuitry on the CPU and RAM boards, which insures that the maximum time between refreshes of a particular cell is 1.995mS.

During normal operation (no DMA), refreshing takes place as follows (refer to CPU schematic for circuitry). Every 13.6uS, a hardware timer sets an S-R flip-flop, which issues a hold request to the microprocessor. When the uP returns hold acknowledge, two signals are sent to the memory board(s) via the backplane. The two signals are:

1. 'Refresh Count' (REFCNT) - causes a refresh address to be supplied to the RAM chips.

2. 'Refresh' (REFR) - serves two functions:

    a. It is logically ANDed with REFCNT to produce a RAS pulse, and

    b. REFR is applied to the RAS demultiplexing circuitry to distribute the RAS pulse to all RAM chips on the board.

Whenever hold acknowledge from the uP goes active, REFR will also go active. This insures that all chips not being accessed will receive RAS pulses.

The entire refresh cycle places the CPU board in a hold state for 400nS; thus, insuring proper refreshing uses about 2.9% of the processor's time. During normal operation, each bit cell is refreshed once each 1.74mS.

Situations exist during normal operation when the refresh circuitry is suspended for a while. The most critical situation is when the DMA Controller on the CPU board is performing a memory-to-memory transfer. When the DMAC is operating, the CPU is in a hold state. If any device other than the refreshing circuit or CPU (in this case, the DMAC) is in control of the bus, then the refresh circuitry is locked out. When this is the case, either (1) the bus must be relinquished in time for the refresh circuitry to resume normal operation (within 12uS) or (2), the device controlling the bus will access each of 128 consecutive locations within 2ms.

A DMA device must transfer a single byte of data and then release the bus within 12uS. If it is transferring a block of data, it must do so at a rate of at least 2uS/byte, and must transfer at least 128 bytes.

The RAM board may be divided functionally into the following five areas. A detailed explanation of each area is provided below:

1. The RAM ARRAY,
2. Address Multiplexing and Refresh Address Generation,
3. RAS and CAS Generation,
4. RAS and CAS Demultiplexing,
5. Parity Generation and Checking.

RAM ARRAY

Basic Element

The basic element used in the RAM array is the 4416 Dynamic RAM chip with an access timer of 150ns.

The active signals perform the following functions:

A0-A6 (Address Input Lines) -- In order to address 16K locations, 14 address lines are required. To keep package size small, these 14 lines are multiplexed into the chip through the seven address inputs: the lower seven address bits first, followed by the high order address bits.

DIN (Data Bit Input) -- This is the data that is written to the chip when a memory write operation occurs.

DOUT (Data Bit Output) -- Normally tristate, this output displays data when a read operation occurs.

WRITE -- When this input is low, a write may be done; when high, a read operation occurs.

RAS (Row Address Strobe) -- This signal, upon transition from a high to a low, latches the lower seven address bits from the address lines into the chip. It also causes a refresh operation to occur at 128 memory locations.

CAS (Column Address Strobe) -- Upon transition from high to low, this signal latches the high order address. During a read operation, this signal also causes the data output to leave the high impedance state.

Organization

Thirty six 4116's are used in the RAM array, organized as nine rows by four columns. Each column is one 16K bank, consisting of eight data bits, and one parity bit. All chips in the array share the same address lines. The WRITE pin is also common to all chips. In each row (4 chips) all of the DOUT pins are connected, and all of the DIN pins are connected. In each column (9 chips) all the RAS inputs are connected together, as are all CAS inputs. It is the RAS and CAS signals that select which bank is accessed during a memory operation (READ, WRITE or REFRESH).

ADDRESS MULTIPLEXING AND REFRESH ADDRESS GENERATION

The sixteen address lines from the system bus are buffered onto the board through Schmitt trigger devices to help provide a greater measure of noise immunity. From the inverters, the lower fourteen address lines are connected to a 3242 I.C. This 28-Pin I.C. has two functions:

1. It serves as an address multiplexer which outputs to the memory array either the lower seven or the upper seven address bits, depending on whether an input call row enable is high or low, respectively.

2. The 3242 contains a seven-bit counter whose output can be gated to the memory array with the application of a signal called REFRESH ENABLE. This count determines which row of 128 bits inside the 4116's is refreshed during a refresh operation.

RAS AND CAS GENERATION

The three basic operations performed on the RAM are WRITE, READ, and REFRESH. Each of these require a RAS signal. In addition, the read and write operations also require CAS. These signals are generated by the two blocks labeled Early Read Detect and Memory Timing on the RAM Block Diagram.

During a read operation by an 8085A running at 5MHz, data must be present at the uP 150nS after the start of the read signal. The access time of the 4116-2 is 150nS; however, because the data bus drivers and receivers add a delay, it is necessary to start a read cycle before the read signal occurs. The early read detection circuitry examines the state of processor signals S1 and IO/Memory at the trailing edge of ALE, and starts the read cycle at least 60nS before the read pulse is issued by the 8085A.

The major component of the memory timing block is a delay line. Signals from the memory timing block are RAS, CAS, and ROW ENABLE. At the beginning of a memory cycle, the signal MCYCLE is input to the delay line. MCYCLE is also distributed to the RAS demultiplexing circuitry. RAS is derived from MCYCLE. 20nS after MCYCLE is input to the delay line, ROW ENABLE (an output from the delay line) is inverted, causing the address multiplexer to switch from outputting the row address to outputting the column address. 20nS after the address switch, the signal CAS emerges from the delay line. If the cycle is a refresh only type cycle, CAS is blocked from entering the array so as not to activate the output buffers of the 4116's. If the cycle is a read or write, both RAS and CAS are fed into demultiplexer circuitry for routing to the appropriate memory bank.

RAS AND CAS DEMULTIPLEXING

Associated with each 16K bank on the memory board, is a 3-bit bank control register which holds information relevant to its respective bank. One bit tells whether the bank is engaged or not, the other two bits describe which address range the bank is located in.

If a particular bank is enabled, and a memory access is made to a location in that bank's specified address range, then the RAS and CAS demux circuitry will steer the RAS and CAS signals from the memory timing block to that bank.

A bank control register may be written to at I/O address 41H. To determine which register to write to, write to I/O address 40H.

PARITY GENERATION AND CHECKING

When a byte is written to memory, it is also fed into a 74S280. This chip is a parity generator/checker with an output that describes the parity of its 9 input lines. During a memory write, the ninth input is held at zero, and the output will be one if the parity of the byte being written is even, zero if the byte has odd parity. This output is written into the ninth 4116 in each bank.

During a memory read, this ninth bit is fed into the 74S280 along with the eight data bits being read. If there is no error, the resulting parity for the nine bits should be odd. If the parity is even, this indicates that 1, 3, 5, 7 or 9 bits have gone bad at that memory location. This information is clocked into a flip-flop, and a parity interrupt is generated for the CPU.

In the event of a parity interrupt, the CPU can read which bank the failure occured in at I/O port 41H. The interrupt is cleared by reading I/O port 40H.

PROGRAMMING RAM

Multivision's memory is programmable in the following ways:

1. The ability to read and write to it,

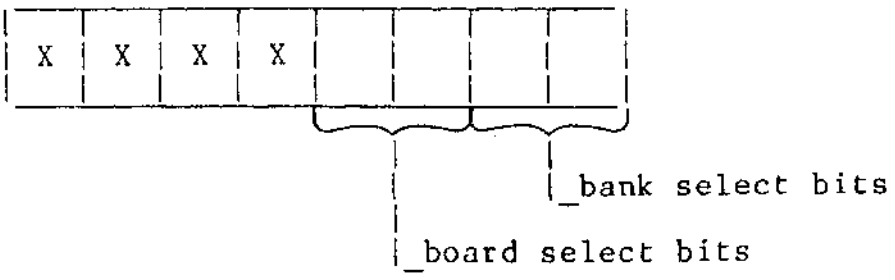
2. The programmability of the address base for each 16K bank, independent of all others,

3. The ability to enable or disable each 16K bank independently,

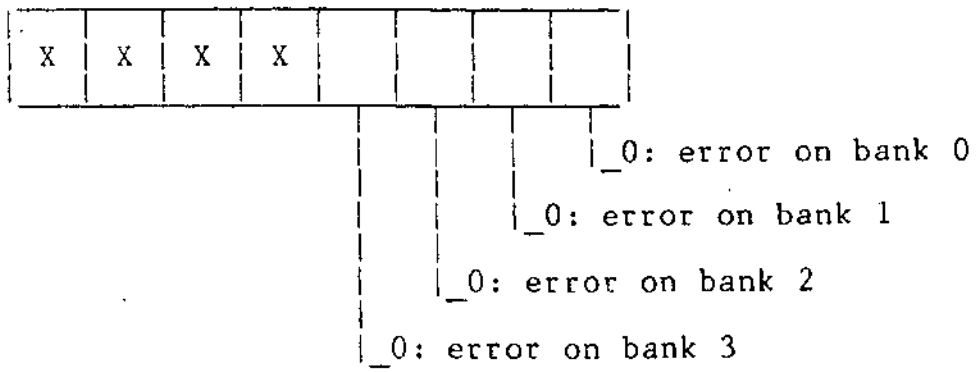
4. The parity error detection scheme.

There are two control ports for Multivision memory:

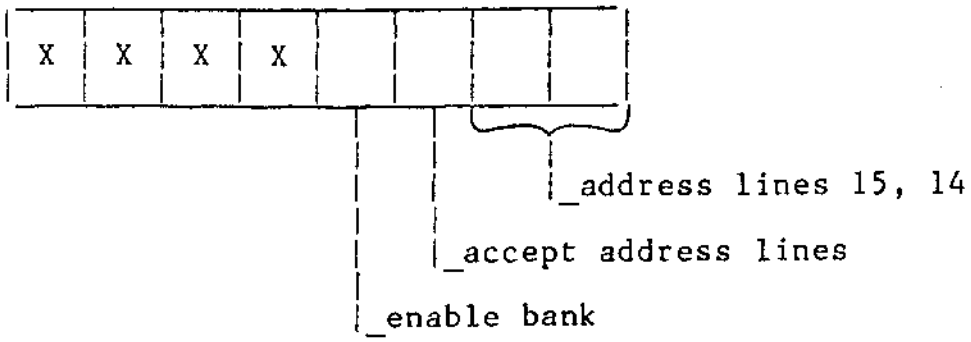
	Port	Usage
1.	40H	Read: Clears parity interrupt on currently selected memory board.
		Write: Selects board and bank for action from register 41H, as follows:



2.	41H	Read: Returns parity error status on banks of currently selected memory board, as follows:



Write: Programs selected board/bank as follows:



Examples of memory control are shown below:

```
        MVI     A,08H       ; Clear any parity interrupt
        OUT     40H         ; which might be pending
        IN      40H         ; on board 2.
;
        MVI     A,0EH       ; Enable
        OUT     40H         ; bank 2 of board 3
        MVI     A,8         ; at its previously established
        OUT     41H         ; address base.
;
        MVI     A,0CH       ; Reset the address base
        OUT     40H         ; for board 3 bank 0
        MVI     A,7         ; to 0C000 hex,
        OUT     41H         ; whatever it may have been.
;
        MVI     A,4         ; Read the parity error status
        OUT     40H         ; for all banks
        IN      41H         ; on board 1.
```

NOTES

1. The top two address lines of all 16-bit address patterns for a given 16K bank are programmed into the bank and not resolved externally.

2. Parity errors are reported on a board-by-board basis, and are cleared in the same way.

3. The enabling or disabling of a bank is independent of the programming of its address base, though both operations can be performed with one command.

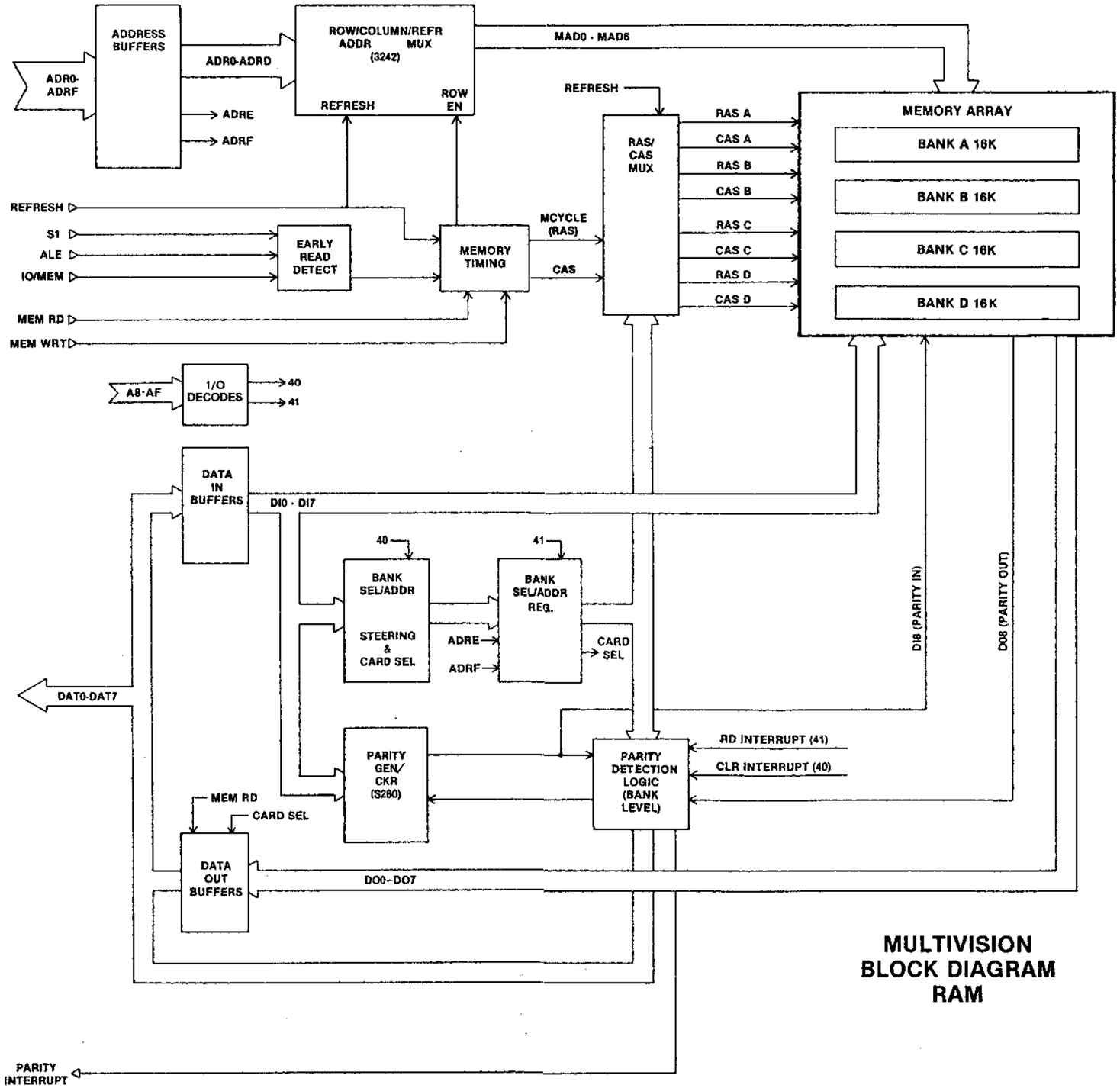


Figure 3-1. RAM PC Board Block Diagram

FUNCTIONAL DESCRIPTION

The Mini Disk/Printer Interface PC board (129-23100) controls the mini disk drives as well as the 13-bit and 8-bit parallel printers. This board generates all mini disk drive control signals, printer control lines, data lines, and strobes.

There is a 20MHz oscillator which is divided down to 1MHz for use in the disk controller circuitry. All ADDRESS, DATA and CPU Control signals are buffered coming on and going off of the board onto the bus.

The heart of the mini disk circuitry is an FD1793 disk controller. This device is the direct interface for the mini disk drives and performs all the functions necessary to read or write data to the disk. The FD1793 does not select the drive.

The 1793 contains five internal registers that can be read or written to. These registers are used to write commands, read status, and read and write data to and from the mini disk. They are selected by a proper binary code on the A0, A1 lines when the device is selected. The registers and their addresses are shown in Figure 4-1 below:

CS	A.	A.	RE = 0	WE = 0
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg
1	*	*	Deselected	Deselected

* = Don't care

Figure 4-1. FD1793 Internal Registers

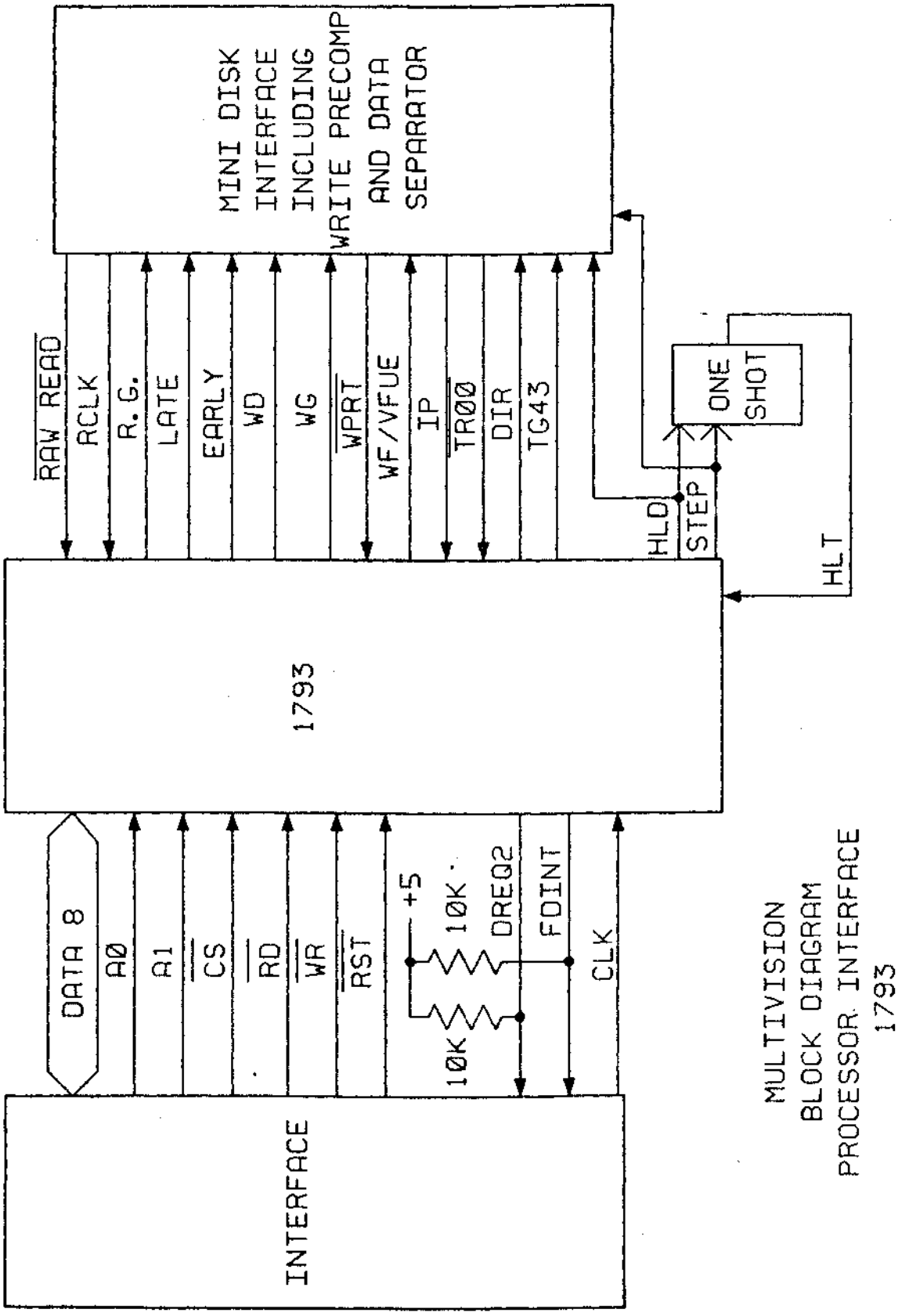


Figure 4-2. Processor Interface 1793 Block Diagram

Data Request

The data request line (pin 38) and the data request bit of the status register indicate valid data transfers. When performing any read command, it indicates that valid data is contained in the data register and the processor may read this byte. In any write command, it indicates the data register is empty and may be loaded by the processor with a new data byte.

Head Load Timing

The Head Load Output (HLD) controls the movement of the R/W head against the media. When HLD=1, the head is loaded against the disk. An internal 15mS delay along with an external one-shot set up, for approximately 500mS delay, allows the head to settle and fully engage. There is also an external one-shot set up which creates a 50mS delay everytime the drive steps to another track. This is used to give the head time to settle.

Read Gate

The read gate output from the 1793 is used to inform the external data separator circuitry (WD1691.745124) that a field of one's or zero's has been read off the disk. In a Modified Frequency Modulation (MFM) mode the Read Gate (RG) has specific characteristics. Assume the 1793 is searching for an ID field; when 4 consecutive bytes of zeros are detected, RG is made active. RG will reset if any one of the following conditions exist:

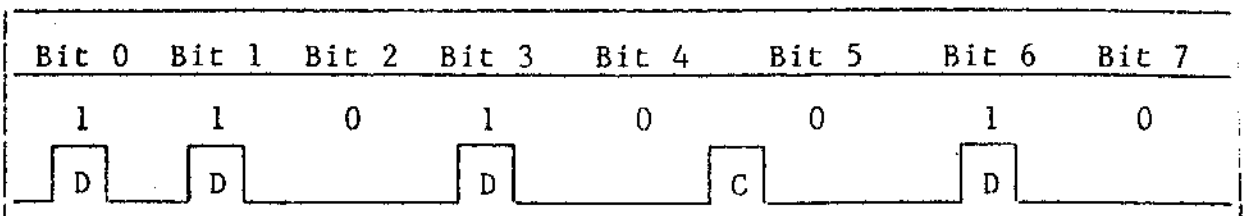
1. 3 Al's with missing clocks not found within 16 bytes,
2. Hex "FE" not found within the next byte,
3. One byte after CRC, and
4. Invalid track/sector address (only during a READ/WRITE sector command).

If the ID search is unsuccessful, the 1793 will continue to search for the specified ID field. When the correct ID field is encountered and, if the current command is a write sector, RG will remain at a logic "0". If the current command is a read sector, the 1793 will look for 4 consecutive bytes of zeros. If 4 bytes are found within the next 33 bytes, RG will be set to a logic "1".

RG is now deactivated (RG=0) upon one of the following conditions:

1. Al's with missing clocks found within 16 bytes,
2. Hex "FB" or "F8" not found within the next byte, and
3. After CRC is read (successfully completed).

Below is a diagram of an M.F.M. recording.



Notes

1. Write data bits at center of bit cell if a "1".

2. Write clock bits at leading edge of bit cell if;
   a. no data bit has been written last, and
   b. no data bit will be written next.

Figure 4-3. Diagram of an M.F.M. Recording

Write Precomp

Write Precompensation is a technique where the write data (both clock and data) is written in the opposite direction of the anticipated bit shift. Write Precompensation is achieved by the use of an external 5-bit shift register in conjunction with WD, early and late. Data is shifted through the shift register either late or early, so data may be recorded evenly on the disk.

Data Separator

The Data Separator takes raw data from a drive and sets up a window for the 1793 so it can interpret the data from the disk. This window is used to "frame" each raw read transition. The 1793 will determine whether the raw read pulse is a clock or data. This window is called read clock.

The read clock signal is supplied from the Data Separator and is used to "frame" each raw read transition. The Data Separator used is a WD1691 along with a voltage controlled oscillator (74S124). Raw data from the drive is fed into a monostable multivibrator (74121) with a Schmitt trigger input to clean up the signal. From there it is fed into the Data Separator. If the RDD line (pin 11 RDD) has made its transition in the beginning of its window, PUSH UP (PU) will go from hi-Z STATE to a logical "1", requesting an increase in frequency from the V.C.O. (74S124). If the RDD line has made its transition at the end of its window, PUSH DOWN (PD) will go to a logical "0" while PU will stay in a hi-Z STATE requesting a decrease in frequency.

When the leading edge of the RDD occurs in the center of the RCLK window, both PU and PD will remain tristate, indicating that no adjustment of the V.C.O. frequency is needed. The V.C.O. rides on a nominal 2MHz clock and responds from the PU or PD by either raising or lowering the 2MHz frequency to align the data in the center of the clock pulse.

Power Supply and V.C.O. Set Up

The power supply and V.C.O. must be set to certain specifications. The procedures for adjusting the 5-volt output on the Multivision 1 power supply is as follows:

1. The Multivision must be set up as a full system with the following installed:

   a. CPU Board -- 129-25300
   b. Dynamic RAM Board -- 129-23300
   c. Mini Disk/Printer S/F -- 129-23100
   d. Two mini disk drives -- 405-07100

2. The voltage at the 5-volt test point on the back of the CPU Board must be measured and adjusted for 5.1 volts ±1%. The adjustment is made by adjusting R8 on the Multivision 1 power supply PCB.

The procedure for adjusting the V.C.O. input and output are as follows:

1. Set up the 5 volts on the power supply as described. Then adjust the input of the V.C.O, Pin 2 of F4, for 1.4V ±1% by adjusting R15.

2. Adjust the output of the V.C.O., Pin 7 of F4, for 2MHz ±1% by adjusting R16.

PROGRAMMING THE MINI DISK CONTROLLER FD1793

The Mini Disk Controller has the capability to force interrupts, read/write sectors or tracks, and to command the head to step in or out, seek a specified track, and restore (seek track 0). MUON assumes that the mini disks are double-sided, double-density with 512 bytes per sector, 10 sectors per side, two sides per cylinder and 35 cylinders per disk. MUON transfers data between mini disk and memory by setting up DMA Channel 2 (see 8237 DMA Controller) for a read or write, then commands the 1793 to seek the desired cylinder and to read or write the desired sector. The 1793 will issue DMA requests until all the data is transferred.

The following examples are based on MUON's use of the 1793 in conjunction with the 8237 DMA Controller. (Refer to Western Digital's documentation on the 1793 for completion statuses and alternate programming modes.)

1. Forced Interrupt
   Force Immediate Interrupt

```
MVI A,0D8H
OUT 34H
```

2. Side, Drive, Density Selection

```
MVI A, command
OUT 38H
```

   The command byte is defined as follows:

bit 0	0:	deselect drive A	1:	select drive A
bit 1	0:	deselect drive B	1:	select drive B
bit 2	0:	select side 0	1:	select side 1
bit 3	0:	single density	1:	double density
bit 4-7	not used			

3. Seek a Track

   a. Set track register to current cylinder.

```
A <-- current cylinder
OUT 35H
```

   b. Set data register to desired cylinder.

```
A <-- desired cylinder
OUT 37H
```

   c. Output seek command (with head load and no verify).

```
MVI A,18H
OUT 34H
```

   d. An interrupt will be generated upon completion or error detection.

4. Read a Sector

a.	Set up DMA for 512-byte mini-to-memory transfer.	(Refer to Section 2)
b.	Set sector register to desired sector.	A <-- desired sector OUT 36H
c.	Output read single sector command.	MVI A, 80H OUT 34H
d.	An interrupt will be generated upon completion or when an error is detected. If the status indicates no errors, then make sure that the DMA has completed.	IN 0A8H ;Input DMA status ANI 04H ;Completed? JZ ERROR ;Jump if no to ;error routine

5. Write a Sector

a.	Set up DMA for 512 byte memory-to-mini transfer.	(Refer to Section 2)
b.	Set sector register to desired sector.	A <-- desired sector OUT 36H
c.	Output write single sector command.	MVI A, 0A0H OUT 34H
d.	An interrupt will be generated upon completion or when an error is detected. If the status indicates no error, then make sure that the DMA has completed.	IN 0A8H ;Input DMA status ANI 04H ;Completed? JZ ERROR ;Jump if no to ;error routine

6. Restore--Seek Track 0

a.	Output restore with head load and verify command.	MVI A,0CH OUT 34H
b.	An interrupt will be generated when track 0 is reached or if an error is detected.	

7. Clearing the Interrupt

An interrupt is cleared by issuing a termination command. The status can then be input.

```
MVI A,0D0H ;Clear the
OUT 34H    ;interrupt
IN  34H    ;input status
```

Port #	Register
34H	Command
35H	Track
36H	Sector
37H	Data
38H	Select

Figure 4-4. Multivision Port Assignments

FD1793 Commands

The FD1793 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. Commands are divided into four types. Commands and types are summarized in Tables 4.1 through 4.5. Tables 4.6 through 4.8 summarize the status register.

Table 4.1. FD1793 Command Summary

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 4.2. Flag Summary for Type I Commands

Flag	Value
h = Head Load Flag (Bit 3)	
	h = 1, Load head at beginning h = 0, Unload head at beginning
V = Verify Flag (Bit 2)	
	V = 1, Verify on destination track V = 0, No verify
r_1r_0 = Stepping Motor Rate (Bits 1-0)	
	Refer to Table 4.5 for rate summary
u = Update Flag (Bit 4)	
	u = 1, Update track register u = 0, No update

Table 4.3. Flag Summary for Type II and III Commands

Flag	Value
m = Multiple Record Flag (Bit 4)	
	m = 0, Single Record m = 1, Multiple Records
a_0 = Data Address Mark (Bit 0)	
	a_0 = 0, FB (Data Mark) a0 = 1, F8 (Deleted Data Mark)
E = 15mS Delay (2MHz)	
	E = 1, 15mS delay
	E = 0, no 15mS delay
(F_2) S = Side Select Flag	
	S = 0, Compare for Side 0 S = 1, Compare for Side 1
(F_1) C = Side Compare Flag	
	C = 0, disable side select compare C = 1, enable side select compare

Table 4.4. Flag Summary for Type IV Command

Flag	Value
I_i = Interrupt Condition Flags (Bits 3-0)	
	I_0 = 1, Not-Ready to Ready Transition I_1 = 1, Ready to Not-Ready Transition I_2 = 1, Index Pulse I_3 = 1, Immediate Interrupt
	I_3 - I_0, Terminate With No Interrupt

Table 4.5. Stepping Rates

CLK	2MHz	2MHx	1MHz	1MHz	2MHz	1MHz
$\overline{DDEV}$	0	1	0	1	X	X
R1R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3mS	3mS	6mS	6mS	184uS	368uS
0 1	6mS	6mS	12mS	12mS	190uS	380uS
1 0	10mS	10mS	20mS	20mS	198uS	396uS
1 1	15mS	15mS	30mS	30mS	208uS	416uS

Table 4.6. Status Register Summary

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready
S6	Write Protect	0	0	0	Write Protect	Write Protect
S5	Head Loaded	0	Record Type	0	Write Fault	Write Fault
S4	Seek Error	RNF	0	0	RNF	0
S3	CRC Error	CRC Error	CRC Error	0	CRC Error	0
S2	Track 0	Lost Data	Lost Data	Lost Data	Lost Data	Lost Data
S1	Index	DRQ	DRQ	DRQ	DRQ	DRQ
S0	Busy	Busy	Busy	Busy	Busy	Busy

Table 4.7. Status For Type I Commands

Bit Name	Meaning
S7 Not Ready	When set, it indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ORed' with MR.
S6 Protected	When set, it indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 Head Loaded	When set, it indicates that the head is loaded and engaged. This bit is a logical "AND" of HLD and HLT signals.
S4 Seek Error	When set, the desired track was not verified. This bit is reset 0 when updated.
S3 CRC Error	CRC encountered in ID field.
S2 Track 00	When set, it indicates that Read/Write head is positioned to track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1 Index	When set, it indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 Busy	When set, command is in progress. When reset, no command is in progress.

Table 4.8. Status For Type II and III Commands

Bit Name	Meaning
S7 Not Ready	When set, it indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ORed' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 Write Protect	On Read Record or Read Track it is not used. On any Write, it indicates a Write Protect. This bit is reset when updated.
S5 Record Type/ Write Fault	On Read Record, it indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write, it indicates a Write Fault. This bit is reset when updated.
S4 Record Not Found (RNF)	When set, it indicates that the desired track, sector, or side was not found. This bit is reset when updated.
S3 CRC Error	If S4 is set, an error has been found in one or more ID fields; otherwise, it indicates an error in the data field. The bit is reset to zero when updated.
S2 Lost Data	When set, it indicates that the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 Data Request	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write Operation. This bit is reset to zero when updated.
S0 Busy	When set, command is under execution. When reset, no command is under execution.

MULTIVISION
BLOCK DIAGRAM
MINI DISK/PRINTER I/F

(SHEET 1)

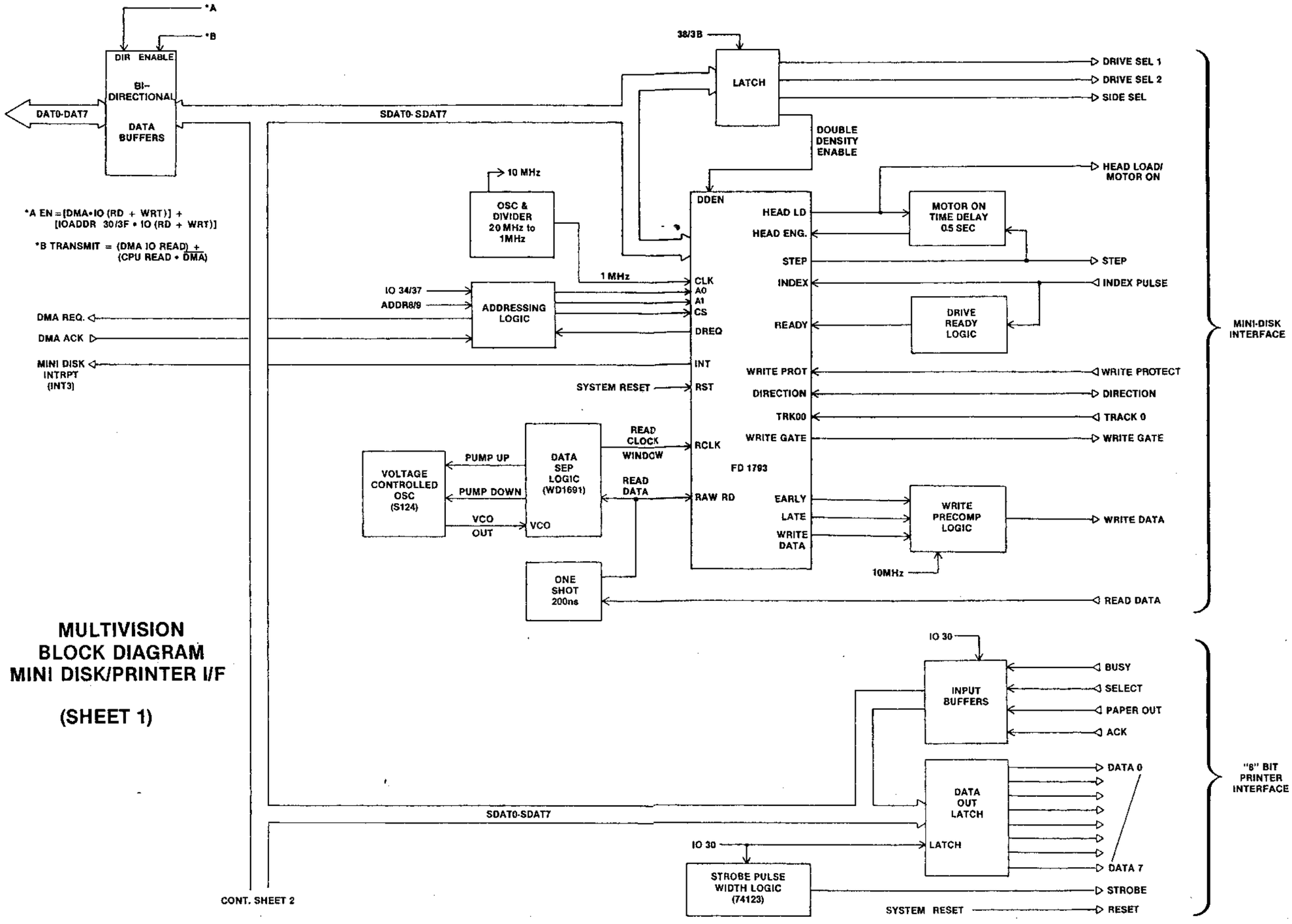
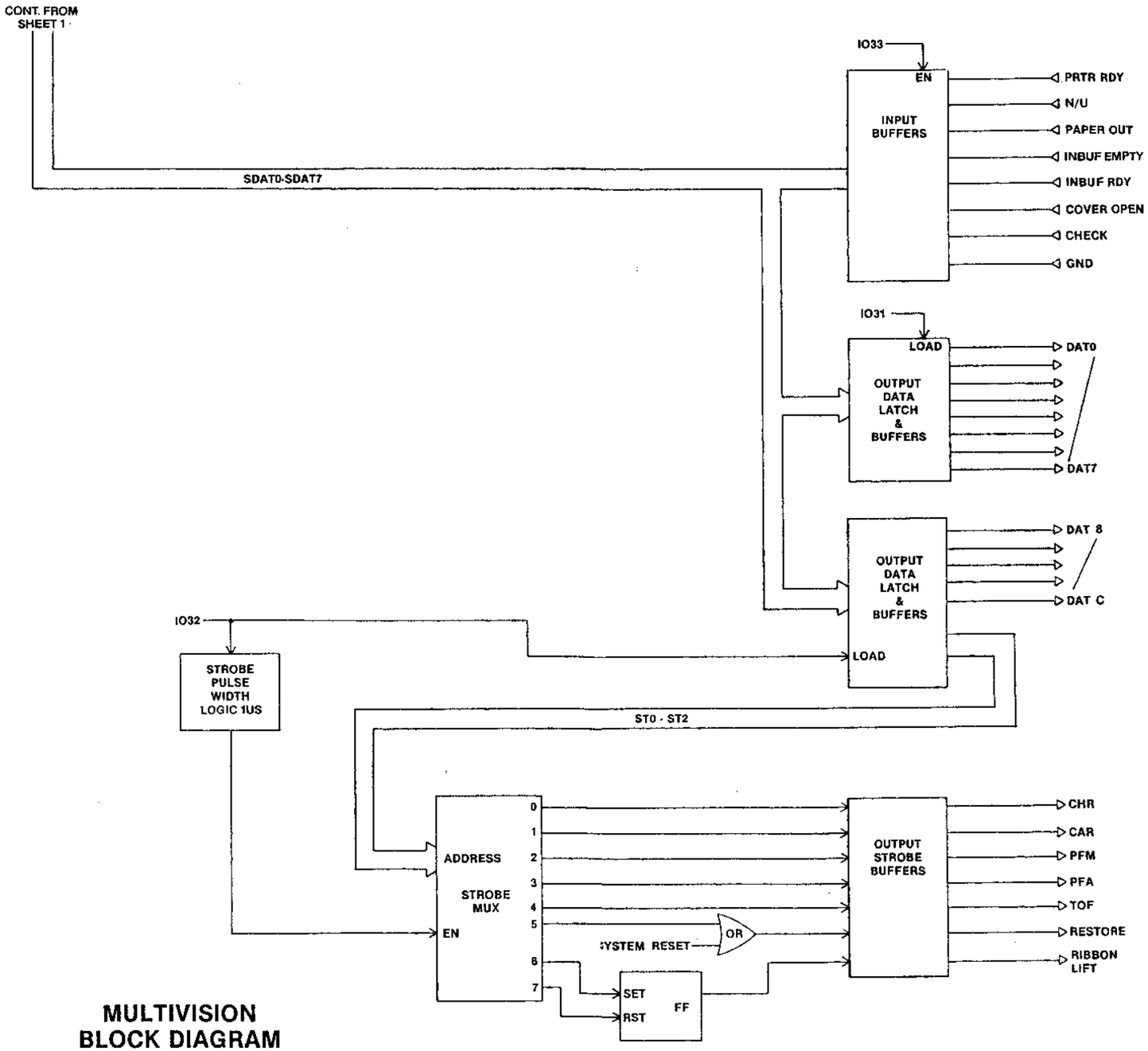


Figure 4-5. Mini Disk/Printer Interface Block Diagram
(Sheet 1)



MULTIVISION
BLOCK DIAGRAM
MINI DISK/PRINTER I/F
(SHEET 2)

Figure 4-5. Mini Disk/Printer Interface Block Diagram (Sheet 2)

PRINTER INTERFACE

There are two parallel interfaces on the PC board for printers. One is a 13-bit letter quality compatible interface and the other is an 8-bit Centronics-compatible interface. Both printer interfaces use a strobe pulse which is generated from onboard addressing gated with I/O write and fed into a pair of one-shots for correct strobe pulse widths.

The 13-bit interface has an 8-bit input buffer which handles the printer signals PRTR RDY, N/U, PAPER OUT, INBUF EMPTY, INBUF RDY, COVER OPEN, and CHECK. This interface also has two output data latches and buffers which handle the 13 data bits and control signals. Each latch is 8 bits wide. Three signals ST0, ST1, and ST2 are demultiplexed by 74CS138 to generate control signals CHR, CAR, PFM, PFA, TOF, RESET and RIBBON LIFT.

NOTE

> This procedure is done at the factory and is not required to be readjusted for the life of the unit.

The 8-bit printer interface (Centronics-compatible) has one input buffer which handles BUSY, SLCT, PAPER OUT and ACK. There is also an 8-bit data latch which handles your 8 data bits.

A list of Printer I/O Ports is shown in Figure 5-1 below.

I/O Port	Type	I/O Read	I/O Write
		READ STATUS	
30	8-Bit Centronics Compatible Interface	Bit0 - BUSY Bit1 - SLCY Bit2 - PE Bit3 - ACK	Bit 0-7 ASCII OUT
31	13-Bit Letter Quality Compatible Interface		Bit 0-7 ASCII OUT
32	13-Bit Letter Quality Compatible Interface		Bit 8-12 Bit 5 - ST0 Bit 6 - ST1 Bit 7 - ST2 ST0 ST1 ST2 Func 0 0 0 CHAR 1 0 0 CAR 0 1 0 PFM 1 1 0 PFA 0 0 1 TOF 1 0 1 RESET 0 1 1 RB LIFT SET 1 1 1 RB LIFT RESET
33	13-Bit Letter Quality Compatible Interface	Letter Quality Status Bit0-PRTR RDY Bit1-N/U Bit2-Paper Out Bit3-Inbuf Empty Bit4-Inbuf RDY Bit5-Cover Open Bit6-Check Bit7-Ground	

Figure 5-1. Printer I/O Ports

8-BIT PARALLEL PRINTER PORT

The 8-bit parallel port is intended to support a Centronics-compatible parallel printer, and provide the voltage levels necessary for that function. It is a latch device, which holds the last pattern written into it until that pattern is over-written. Its control is as follows:

Port	Usage
30H	Read: Returns three status signals: Bit 0: 1 = Busy Bit 1: 1 = Printer Deselected Bit 2: 1 = Printer Out of Paper Write: Outputs a complemented character to the Centronics-compatible device. That is, the character "A" (41H) would be output by putting 0BEH to port 30H.

Figure 5-2. Port Assignment for 8-Bit Parallel Printer Port

Table 5.1 lists the pin assignments for the 8-bit printer port.

Table 5.1. 8-Bit Printer Port Pin Assignments

Signal Name	Printer Connector ADDS	Printer Connector CENTRONICS	Signal Name	Printer Connector ADDS	Printer Connector CENTRONICS
B1	11	2, 20	INPUT PRIME*	23	30, 31
B2	2	3, 21	DATA STROBE*	24	1, 19
B3	3	4, 22	GND	1, 7	14
B4	8	5, 23	ACK*	13	10, 28
B5	18	6, 24	SELECT*	9	13
B6	12	7, 25	BUSY	20	11, 29
B7	14	8, 26	PAPER OUT	22	12
B8	4	9, 27			

*Active Low Signal

13-BIT PARALLEL PRINTER PORT

A 13-bit Qume-compatible printer port is available for controlling letter quality printers. Any printer that is Qume-compatible such as the NEC Spinwriter, Diablo Hitype or any of the Qume Sprint series may be connected to this port. The port assignments for the 13-bit parallel printer port are as follows:

Port Number	Function
31H	Bits 0-7 - ASCII Character
32H	Bits 0-4 - Carriage Movement* Bits 5-7 - Strobe Command Bits Bits 765 000 - Character 001 - Horizontal Carriage Movement 010 - Vertical Carriage Movement 101 - Reset Printer 110 - Lift Ribbon
33H	Status: - Active High Bit 0 - Printer Ready (Floats High) Bit 1 - Always 0 Bit 2 - Out of Paper Bit 3 - Input Buffer Empty Bit 4 - Input Buffer Ready Bit 5 - Cover Closed Switch Bit 6 - Error Check** Bit 7 - Printer Connected

*See the Manual for the Printer being used for specific instructions on how to control carriage movement.

**Error check can occur for a number of failures. To clear this bit, a reset command must be issued to the printer.

Figure 5-3. Port Assignments for 13-Bit Parallel Printer Port

If the printer is ready for a character, the status read will be a B9H.

Typical Command Sequence;

1. Check status and wait for PRINTER READY,
2. Send character, and
3. Send strobe command.

Commands 2 and 3 are required for any output to the printer, and must be issued in that order.

To insure that the printer is ready to accept commands, it is good practice to issue a reset command before each printing session. Also, as part of the initialization procedure, the ribbon must be lifted.

Programming Example:

```
                ;Message to be printed

MSG:    DB      '13-bit printer output'

START:  IN      33              ;Check status.
        CPI     0B9H            ;Ok?
        JNZ     ERROR           ;Jump if no to error handler.

;RESET PRINTER

        XRA     A               ;Send null character required to
        OUT     31H             ;maintain proper command sequence.
        MVI     A,0A0H          ;Send reset command.
        OUT     32H

        XRA     A               ;Send null character.
        OUT     31H
        MVI     A,0C0H          ;Lift ribbon.
        OUT     32H

        LXI     H,MSG           ;Pointer to start of message.
CONT:   MOV     A,M             ;Get next message character.
        INX     H               ;Bump message pointer.
        CPI     '$'             ;Message terminator?
        JZ      EXIT            ;Jump if done.
        RLC                     ;Position character for output.
        MOV     B,A             ;Save character.

;POSITION CARRIAGE FOR PRINTING NEXT CHARACTER

        XRA     A               ;Send null character.
        OUT     31H
        MVI     A,20H           ;Horizontal position command
        ORI     0BH             ;added to displacement.
        OUT     32H             ;Output command.
        IN      33H             ;Check status.
        CPI     0B9H            ;Ok?
        JNZ     ERROR           ;Jump on error.
        MOV     A,B             ;Get character back.
        OUT     31H             ;Output it.
        XRA     A               ;Output character strobe.
        OUT     32H
        JMP     CONT            ;Continue.
```

Table 5.2 lists the pin assignments for the 13-bit printer port.

Table 5.2. 13-Bit Printer Port Pin Assignments

Pin #	Signal Name	Pin #	Signal Name
1	GND	26	$\overline{\text{TOP OF FORM STROBE}}$ (OPT)
2	$\overline{\text{DATA 1/2}}$	27	GND
3	$\overline{\text{DATA 1}}$	28	$\overline{\text{RIBBON LIFT COMMAND}}$
4	$\overline{\text{DATA 2}}$	29	GND
5	$\overline{\text{DATA 4}}$	30	$\overline{\text{RIBBON OUT}}$ (OPT)
6	$\overline{\text{DATA 8}}$	31	GND
7	$\overline{\text{DATA 16}}$	32	$\overline{\text{PRINTER SELECT}}$ (GND)
8	$\overline{\text{DATA 32}}$	33	GND
9	$\overline{\text{DATA 64}}$	34	$\overline{\text{COVER INTERLOCK}}$ (OPT)
10	$\overline{\text{DATA 128}}$	35	GND
11	$\overline{\text{DATA 256}}$	36	GND
12	$\overline{\text{DATA 512}}$	37	$\overline{\text{CHECK}}$
13	$\overline{\text{DATA 1024}}$	38	GND
14	$\overline{\text{DATA 2048}}$	39	$\overline{\text{INPUT BUFFER (CHAR) RDY}}$
15	GND	40	GND
16	$\overline{\text{RESTORE}}$	41	$\overline{\text{INPUT BUFFER (CARRIAGE) RDY}}$
17	GND	42	GND
18	$\overline{\text{CHARACTER STROBE}}$	43	$\overline{\text{INPUT BUFFER (PAPER FEED) RDY}}$
19	GND	44	GND
20	$\overline{\text{CARRIAGE STROBE}}$	45	$\overline{\text{INPUT BUFFER EMPTY}}$
21	GND	46	GND
22	$\overline{\text{PAPER FEED MAIN STROBE}}$	47	$\overline{\text{PRINTER RDY}}$
23	GND	48	GND
24	$\overline{\text{PAPER FEED AUXILIARY STROBE}}$ (OPTIONAL)	49	$\overline{\text{PAPER OUT}}$ (OPT)
25	GND	50	GND

OVERVIEW

The Hard Disk Controller consists of a single PC board designed to interface an SA 1002/4 or Memorex 101, or an equivalent 8" fixed disk drive to the Multivision system bus. The controller's functions include: command and status control, data formatting, encoding, decoding and DMA operations. The circuitry used to implement these functions is:

1. a MOS microprocessor,
2. a high speed microcontroller, and
3. random logic.

The four major subsystems which make up the Hard Disk Controller are the System Bus, Microprocessor, Microcontroller, and Serial Disk Data Encoding/Decoding. Each of these subsystems are described below.

SYSTEM BUS I/O

The system bus I/O logic utilizes an address decoder, host interrupt logic, status latch, data latch, 8-bit by 16 word FIFO buffer and FIFO control circuit. Status is obtained by a host read where the appropriate I/O address is decoded and status presented. Commands and data are transferred by the 16 word FIFO. Commands are loaded into the FIFO with host writes which fall through and are acted upon by the 8035 Microprocessor. Detection of a disk read or write command causes the MPU to initiate DMA transfers via the FIFO. During disk write operations data is transferred from the host through the FIFO, which serializes the data. Disk read functions use derived clock and regenerated serial data to load data into the FIFO for output to the host bus via DMA.

MICROPROCESSOR

The 8035 Microprocessor interprets host commands, controls the FIFO and monitors serial data shifting. A 2716 EPROM contains the 8035 firmware. The low order addresses for this memory are latched on the Port 0 bus by the ALE pulse. Port 0 is also used for outputting status bytes to the status latch.

An expander port is used to sense CRC errors and overrun conditions, control head selection, position, and microcontroller steering. The expander uses four bits in Port 2. The remaining bits are decoded to produce pulses which read and clear the FIFO buffer, write header bytes from Port 1, acknowledge interrupts, and read a switch register into Port 1. Commands from the FIFO are used to switch register bits and output header bytes to the header registers. This is accomplished by using Port 1.

The 8035 TO/TI test inputs are used to sense microcontroller state and data shifting. The interrupt is used to synchronize MPU operation with microcontroller state.

MICROCONTROLLER

The microcontroller is made up of a counter, PROM and decoder (which is responsible for sector synchronization), data formatting, disk data shift controls, CRC controls, and read/write gate controls. Inputs to the microcontroller consist of a format and byte counter used for sector timing and formatting. Index, header, and CRC are used to control the sequence of the counter. Logic to generate interrupts to the 8035 synchronize the microcontroller to the microprocessor. Records are written by first serially comparing for SYNC and the appropriate header, and then overwriting them with SYNC and CRC. Data is read in a similar manner until after the correct header is detected. Data is outputted by the FIFO.

The resulting sector format is shown in Figure 6-1 below.

314 Byte Sector

	Header Field								Write Update Area					
Function -	FG	IG*	CSG	SYN	AM	CYL	HD	SEC	CRC	BWG	CSG	SYN	DF	CRC	SG
# of Bytes-	62+	6	14	1	1	1	1	1	2	2	14	1	256	2	18

FG	Format Gap '4E' 62-450 Bytes
IG	Index Gap 0's
CSG	Clock Search Gap 0's before ID field
SYN	Sync Byte 'A1' before ID field
AM	Address Marker 'FE'
CYL	Cylinder (1 of 256)
HD	Head (1 of 4)
SEC	Sectors (1 of 32)
CRC	Cyclic Redundancy Check (2 bytes) of ID field
BWG	Before Write Gap 0's
CSG	Clock Search Gap 0's before data field
SYN	Sync Byte 'A1' before data field
DF	Data Field 256 bytes
CRC	Cyclic Redundancy Check (2 bytes) of data field
SG	Splice Gap '4E'

*Index

Figure 6-1. Microcontroller Sector Format

SERIAL DISK DATA ENCODING/DECODING

Serial write data is MFM encoded and pulse position precompensated. The MFM data is formed by using a shift register and decoder. By utilizing previous and current list information, they produce:

1. Flux transitions for ones,

2. No flux transitions for zeroes, and

3. Flux transitions if no transition was written in the last cell and no transition in the next cell.

Precompensation is accomplished via a delay line, shift register, and encoding logic which position the resulting flux transitions in the opposite direction of the expected bit shift.

Serial read data from the disk is decoded by a phase locked oscillator and transition time-out detector. Multiples of the read data transitions make up a constant bit cell time which is derived from the phase locked oscillator. NRZ data is obtained by timing the position of the read data transition relative to the bit cell time.

The Hard Disk Controller used in Multivision 2 and 3 is an intelligent controller that provides the user with a simple interface to the hard disk. The controller transfers data to and from the disk via channel 3 of the DMA controller.

Commands

Table 6.1 contains commands that are used with the Disk Controller. Commands are issued to I/O port 10H. Those commands that cause an action (e.g., READ, WRITE, SEEK) will return an interrupt upon completion. When the controller issues interrupt 4, the status of the completed command may be read at I/O port 10H, clearing the interrupt. In the table below, those commands that return an interrupt are listed on the left; commands on the right do not return an interrupt.

Table 6.1 Disk Controller Commands

Hex	Command	Hex	Command
00	- ECHO LAST COMMAND	40+$S_5S_4S_3S_2S_1S_0$	- SET SECTOR
01	- ECHO SECTOR	80+$T_5T_4T_3T_2T_1T_0$	- SET TRACK LSB
02	- ECHO TRACK LSB	C0 + $H_1H_0T_7T_6$	- SET TRACK MSB and HEAD
03	- ECHO TRACK MSB		
04	- ECHO SWITCH		
20	- RESTORE		
21	- SEEK		
22	- WRITE		
23	- READ		
24	- FORMAT		

Echo Commands

The first five commands in Table 6.1 are Echo Commands which cause the controller to return with the requested information. They are used primarily for debugging. The ECHO SWITCH Command returns the setting of a switch on the controller board that is used to configure the board for different drives. In response to the ECHO SWITCH, a C0H at port 10H signifies a Shugart Drive with 256 cylinders and 32 sectors per track, while a D0H implies that the controller is connected to a Memorex Drive with 244 cylinders and 36 sectors per track.

Setup Commands

The commands on the right side of the table are used to set the cylinder, head, and sector prior to reading from or writing to the disk. Since the disk may contain up to 256 cylinders, the SET TRACK Command is broken into two commands: one to set the lower 6 bits of the cylinder number, the other to set the upper two bits of the cylinder number and the head select bits.

Action Commands

These commands cause the controller to actually do something with the drive. The RESTORE Command causes the read/write head of the drive to step to track zero and resets the controller to sector 1, track 0, head 0. The SEEK Command causes the head to move to the track selected by the SET TRACK Command. READ and WRITE cause a read or write of the specified sector. The FORMAT Command is used for laying down sector headers on the track.

Each of these commands returns an interrupt and status upon completion. Status bytes are tabulated below.

Table 6.2. Interrupt Status Bytes for Action Commands

Status	Meaning
00H	Successful Operation
02H	CRC Error in Data Field
04H	DMA Overrun Error
13H	CRC Error in Header
11H	Record Not Found
1FH	Write Fault in Drive
FFH	Time Out Error

Formatting the Hard Disk

To format the hard disk, follow the steps listed below:

1. Seek the desired track to be formatted by selecting a cylinder and head, then issuing a SEEK Command.

2. Set up the DMA Controller for a transfer of 1600 bytes of '4E' Hex.

3. Issue the FORMAT Command.

4. Write 'E5' Hex to all sectors on the track using the WRITE Command.

5. Read back all sectors to verify the format.

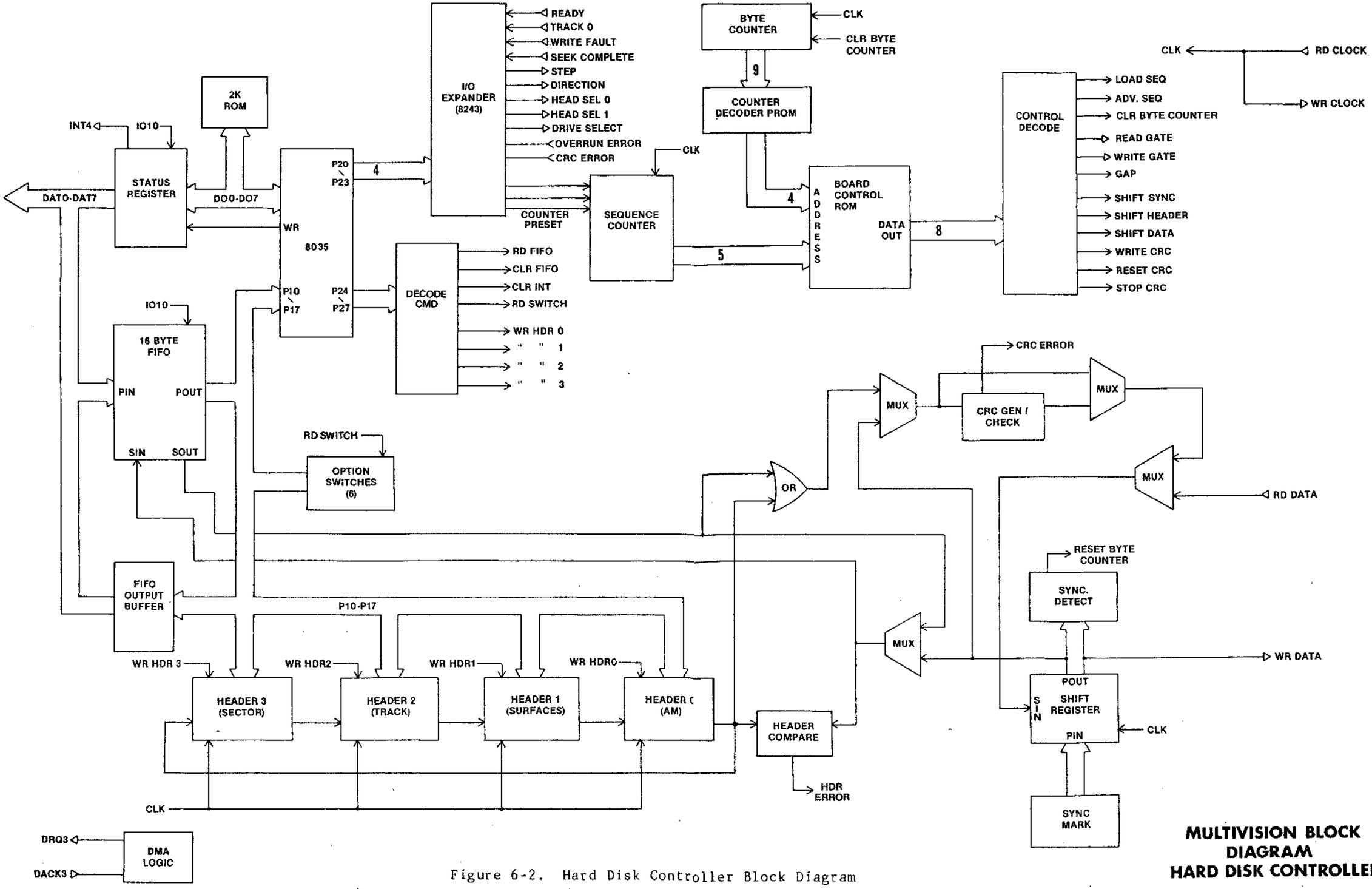
6. After all tracks have been formatted, read the first sector of each track to verify head positioning and selection.

A Sample Write Routine

An example of a write routine for the hard disk follows:

```
Write: ;set up DMA controller for a write

       OUT     0ACH             ;Clear DMA Controller.

       LXI     H,BUFFER         ;Get buffer address.
       MOV     A,L              ;Output address to DMA,
       OUT     0A6H             ;low byte then
       MOV     A,H
       OUT     0A6H             ;high byte.

       LXI     H,256-1          ;Terminal count is sector size-1.
       MOV     A,L              ;Output count to DMA,
       OUT     0A7H             ;low byte
       MOV     A,H              ;then
       OUT     0A7H             ;high byte.

       MVI     A,0BH
       OUT     0ABH             ;Set DMA mode.

       MVI     A,40H
       OUT     0A8H             ;Set DMA command.

       MVI     A,3              ;Output mask to DMA.
       OUT     0AAH

       ;set up Hard Disk Controller

       MVI     A,CYLNDR         ;Desired cylinder.
       ANI     3FH              ;Mask for least significant 6 bits.
       ORI     80H              ;OR in command.
       OUT     10H              ;Output command.

       MVI     A,CYLNDR         ;Desired cylinder.
       RLC                      ;Position 2 most significant bits.
       RLC
       ANI     3H               ;Mask for them only.
       MOV     B,A              ;Save in B.
       MVI     A,HEAD           ;Desired head select.
       RAL                      ;Position bits.
       RAL
       ORA     B                ;OR in cylinder.
       ORI     0C0H             ;OR in command.
       OUT     10H              ;Output command.

       MVI     A,SECTOR         ;Desired sector.
       ORI     40H              ;OR in command.
       OUT     10H              ;Output command.
```

```
        MVI     A.23H           ;Output read command to
        OUT     10H             ;Hard Disk Controller.

        EI                      ;Enable interrupts.
        HLT                     ;Wait for completion interrupt.

        IN      10H             ;Get status.
        ORA     A               ;Error?
        JNZ     ERROR           ;Jump to error handler.

... CONTINUE

        ; I/O BUFFER

BUFFER:         DS      256
```



MULTIVISION BLOCK DIAGRAM
HARD DISK CONTROLLER

Figure 6-2. Hard Disk Controller Block Diagram

FUNCTIONAL DESCRIPTION

The I/O Controller is responsible for communication on the Multivision 3. The PC board will handle up to four RS232C compatible serial ports. All address, data, and control lines are buffered coming on and going off of the board onto the bus.

The heart of the I/O Controller is an 8251A USART (Universal Synchronous/Asynchronous Receiver Transmitter). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Conversely, it can receive serial data streams and convert them into parallel data characters for the CPU. There are four of these USARTs on the I/O Controller to handle a total of four ports. The USARTs are set up in the same mode of operation as the console port on the CPU board.

There are two 8253 Programmable Interval Timers used with the USARTs. These two Timers are used to set up the four independent baud rates for the USARTs. Default baud rates for these timers are 9600 baud.

The I/O Controller uses FIFO memory for temporary storage of data being received. The reason for this is to prevent the loss of data when receiving to the system. When data is received and assembled in the USART data buffer, it is loaded into a FIFO and then read by the CPU from the FIFO. The FIFO used is a 74S225. Each one of these parts is organized as 16 words of 5 bits. Since we have an 8-bit data bus, we use two 74S225's per USART to give us storage capability of 16 words by 8 bits. Up to 16 words of 8 bits can be received by the USART and stored in the FIFO without the CPU reading the information until it is ready.

There is a priority scheme designed on the board to avoid the possibility of two USARTs trying to load the FIFOs at the same time. There are two different logic signals which perform this function. One signal is the (A+C) group logic signals and the other is the LOCK signal. The (A+C) group is used when two USARTs receive a character at the same time. When this happens the priority is Port 0, Port 1, Port 2 and Port 3. The LOCK signal is used when one USART has already received a character and another USART follows behind. LOCK always gives priority to the USART that receives the character first.

The I/O Controller uses interrupts to notify the CPU that there is either a character to be read from the FIFO or a character to be transmitted. There are two interrupt lines which run to the CPU, notifying it that it either has a XMIT or RCV INT pending. Once this is triggered, the CPU reads an I/O port (port 52) to tell it which of the four USARTs is interrupting it. Figure 7-1 below, shows a chart for the XMIT and RCV interrupt bits.

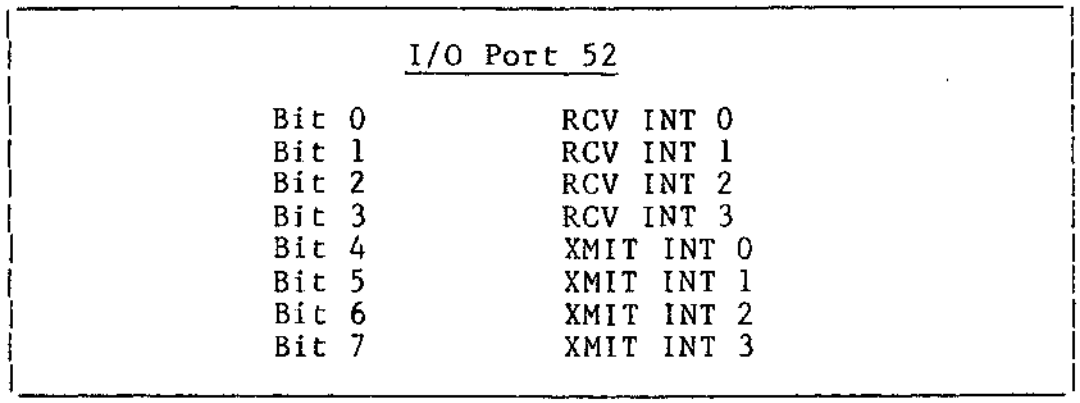


Figure 7-1. XMIT and RCV Interrupt Bits

Control of the serial ports in the Expansion Module is different from those in the Multivision 1 Module. These ports are also 8251A elements, but are all controlled by the same set of I/O ports, as shown in Table 7.1 below.

Table 7.1. I/O Port Assignments for Expansion Module

Port	Usage
52H	Read: Interrupt identification register Bit 0: Received data, port 0 Bit 1: Received data, port 1 Bit 2: Received data, port 2 Bit 3: Received data, port 3 Bit 4: Transmitter ready, port 0 Bit 5: Transmitter ready, port 1 Bit 6: Transmitter ready, port 2 Bit 7: Transmitter ready, port 3 Write: Port select register Bit 0: Select port 0 Bit 1: Select port 1 Bit 2: Select port 2 Bit 3: Select port 3 Bit 4: Loop test
51H	Read: Selected port status Write: Command register for selected port
50H	Write only: Transmit data for selected port
54H	Read only: Received data for selected port

In order to control serial port n, it must be selected first. Interrupt data from port 52H will usually be the steering information. Receive interrupts raise line one on the 8259 Interrupt Controller, and transmit interrupts raise line two.

There are two 8253 timers on the 4 Port I/O PC board to provide baud rate clocks. They are set up as follows:

Port	Usage
58H	Counter 0: for port 2
59H	Counter 1: for port 3
5AH	Reserved
5BH	Timer command register
5CH	Counter 0: for port 0
5DH	Counter 1: for port 1
5EH	Reserved
5FH	Timer command register

For a description of how to program these chips, please refer to the topic entitled Programmable Interval Timer (PIT), 8253-5 in Section 2.

To program the initialization of the Multivision I console port:

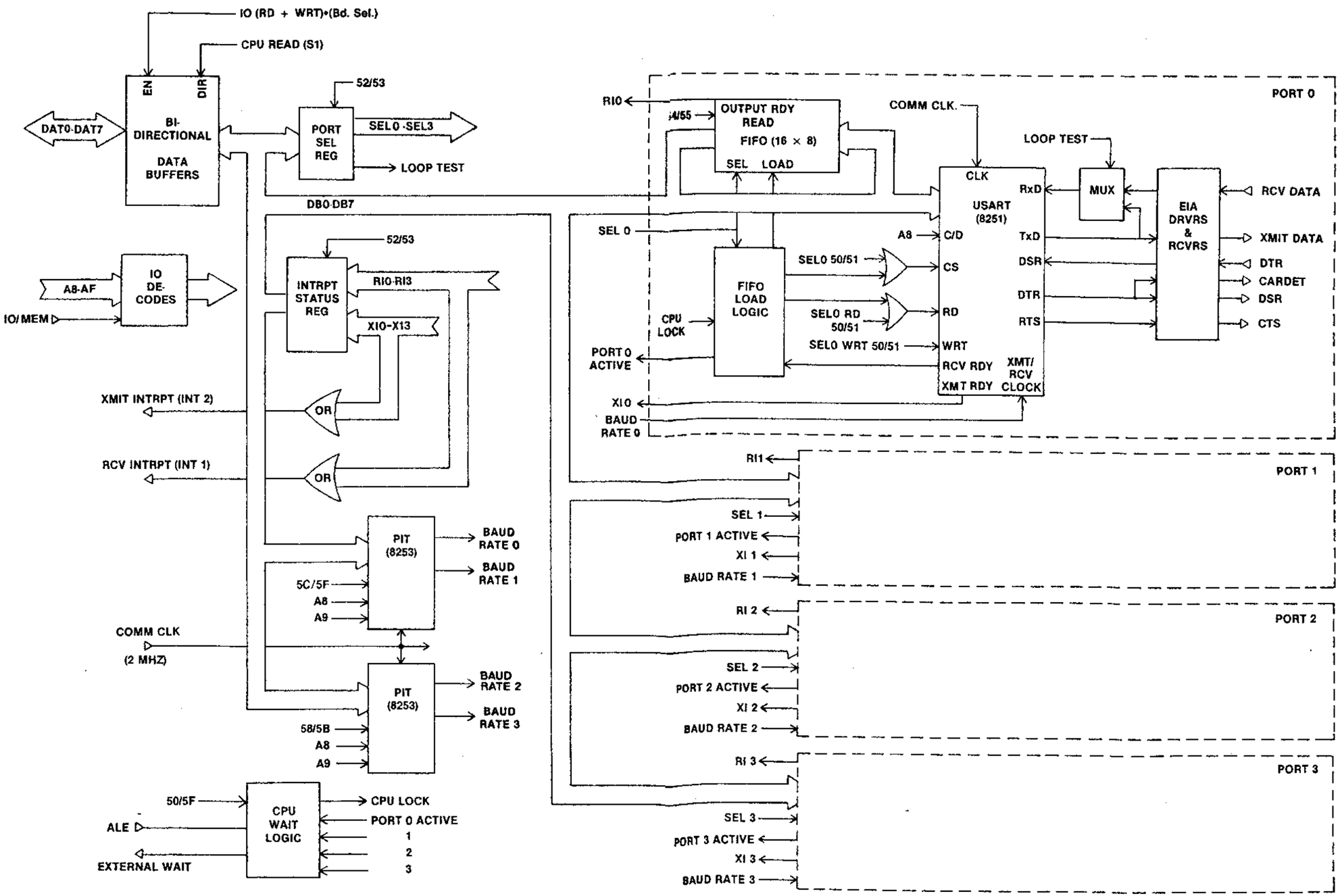
```
CINIT:  DI              ;Safest
        XRA     A
        OUT     89H     ;Six zeros
        OUT     89H     ;to the
        OUT     89H     ;command port
        OUT     89H     ;to guarantee that the 8251A
        OUT     89H     ;has recycled internally
        OUT     89H     ;and is idle.
        MVI     A,40H
        OUT     89H     ;Enter "set USART mode" state.
        CALL    WASTIM  ;Delay at least 4uS
                        ;between commands.
        MVI     A,0DAH  ;Set USART for 7 data bits,
                        ;odd parity,
        OUT     89H     ;baud divider =16, 1 stop bit,
                        ;ASYNC mode.
        CALL    WASTIM  ;Delay another 4uS.
        MVI     A,36H   ;Command to raise RTS, DTR,
                        ;reset error and
        OUT     89H     ;Receiver Enable on USART.
        RET             ;Now ready at selected baud rate.
WASTIM: NOP             ;Delay about 5uS.
        NOP
        NOP
        NOP
        RET
```

The 8251A USART is used by each of the console ports on the 4 Port I/O Interface PC board. However, data is not read directly from this component. Rather, received data is buffered in a 16-character hardware FIFO associated with the USART. This buffer helps to prevent data loss at high transmission speeds.

To fetch a character from the FIFO, a receive interrupt must first be generated. The character is then sent to register A and the port number is sent to register B. The controlling program then returns with a zero flag clear indicating the fetch procedure has been completed.

Following is a sample of the programming used in fetching a character:

```
GETCHR:
        DI              ;Interrupts off.
        IN      52H     ;Read the interrupts status
                        ;register;
        ANI     OFH     ;only interested in receive
                        ;interrupts.
        MOV     C,A     ;Copy receive line status into C.
        MVI     B,3     ;Determine interrupting port.
        MVI     A,BIT3  ;Is it port 3?
        ANA     C
        JNZ     GETCO1  ;(yes)
        DCR     B
        MVI     A,BIT2  ;Port 2?
        ANA     C
        JNZ     GETCO1  ;(yes)
        DCR     B
        MVI     A,BIT1  ;Port 1?
        ANA     C
        JNZ     GETCO1  ;(yes)
        DCR     B
        MVI     A,BIT0  ;Port 0?
        ANA     C
        RZ              ;(no)
GETCO1:
        OUT     52H     ;Yes.  Select port using mask in A
        IN      54H     ;and read character.
        EI              ;Interrupts back on
        RET             ;and return with char in A,
                        ;port # in B.
```



MULTIVISION BLOCK DIAGRAM 4 PORT I/O

Figure 7-2. 4 Port I/O Block Diagram

OVERVIEW

The Multivision mini disk drives (405-07100) are compact disk memory devices designed for random access data storage, data entry, and data output applications. Multivision has two sources for mini disk drives. The first of those is the M.P.I. Model 52 and the second is the Tandon Model T100. The mechanical components consist of an aluminum chassis on which is mounted a spindle (belt driven by a DC motor), a stepper motor/band combination for positioning the magnetic head assembly and a cone/clutch assembly for centering and holding the recording media under operation. Power and interface signals plug directly into this board. The following basic circuits are included:

1. Stepper Motor Control Logic
2. Read Circuit
3. Write/Erase Circuit
4. Spindle Motor Speed Control
5. Index - Track 00 and Write Protect Sensing

FUNCTIONAL DESCRIPTION

The mini disk drives are self contained and require no operator intervention during operation other than opening and closing the doors. The drives consist of a media rotating system, a head load and positioning system, and a write/erase and read system. When the front door is opened, access for inserting the disk is provided. When inserting the disk, all positions except in/out are controlled by physical guides internally. Closing the front door activates the cone/clutch system which serves two purposes:

1. To correct centering of the media, and
2. To clamp the media to the spindle HUB.

The spindle HUB rotates at a constant speed of 300 R.P.M. by means of a D.C. motor/tachometer and a reference in a closed loop system. The receiving head is positioned over the correct track by means of a four-phase stepper motor/band direct-drive mechanism, and its associated electronics. A one-stop movement causes a one-track movement. When a write protect disk is inserted, the write protect sensor normally disables the write/erase circuits in the drive. Data recovery electronics include a low frequency amplifier, a differentiator, a cross-over detector, a digital filter, and a final pulse generator.

GENERAL

Parameter	Characteristics
Media	ANSI standard 5 1/4-inch diskette
Number of Tracks	70/52
Track Density	48 TPI
Start/Stop Time	.5 sec
Rotational Speed	300 rpm ± 1 1/2%
Average Latency	100mS
Head Loading Time	35mS
Access Time	6mS, track-to-track
Head Setting Time	15mS
Head Life	20,000 hours
Media Life	3 x 10^6 passes on single track
Recording Method	MFM
Recording Density (FM)	2810/5620 bpi
Flux Density	5620 fci max.
Data-Transfer Rate	250K bits/sec.
Power-up Delay	1 sec

PHYSICAL

Height	3.25 inches (8.255 cm)
Width	5.75 inches (14.605 cm)
Length	7.5 inches (19.05 cm)
Weight	3.0 pounds (1.36 kg)

POWER REQUIREMENTS

Power	+12 VDC±5%, 1.5A +5 VDC±5%, 0.7A
Typical Power Dissipation	15W Operation 6W Standby

ENVIRONMENT

Parameter	Characteristics
Operating Temperature	40° to 115°F (4.4°C to 46.1°C)
Relative Humidity	20 to 80% (noncondensing)

Figure 8-1. Specifications for M.P.I. Model 52 Mini Disk Drives

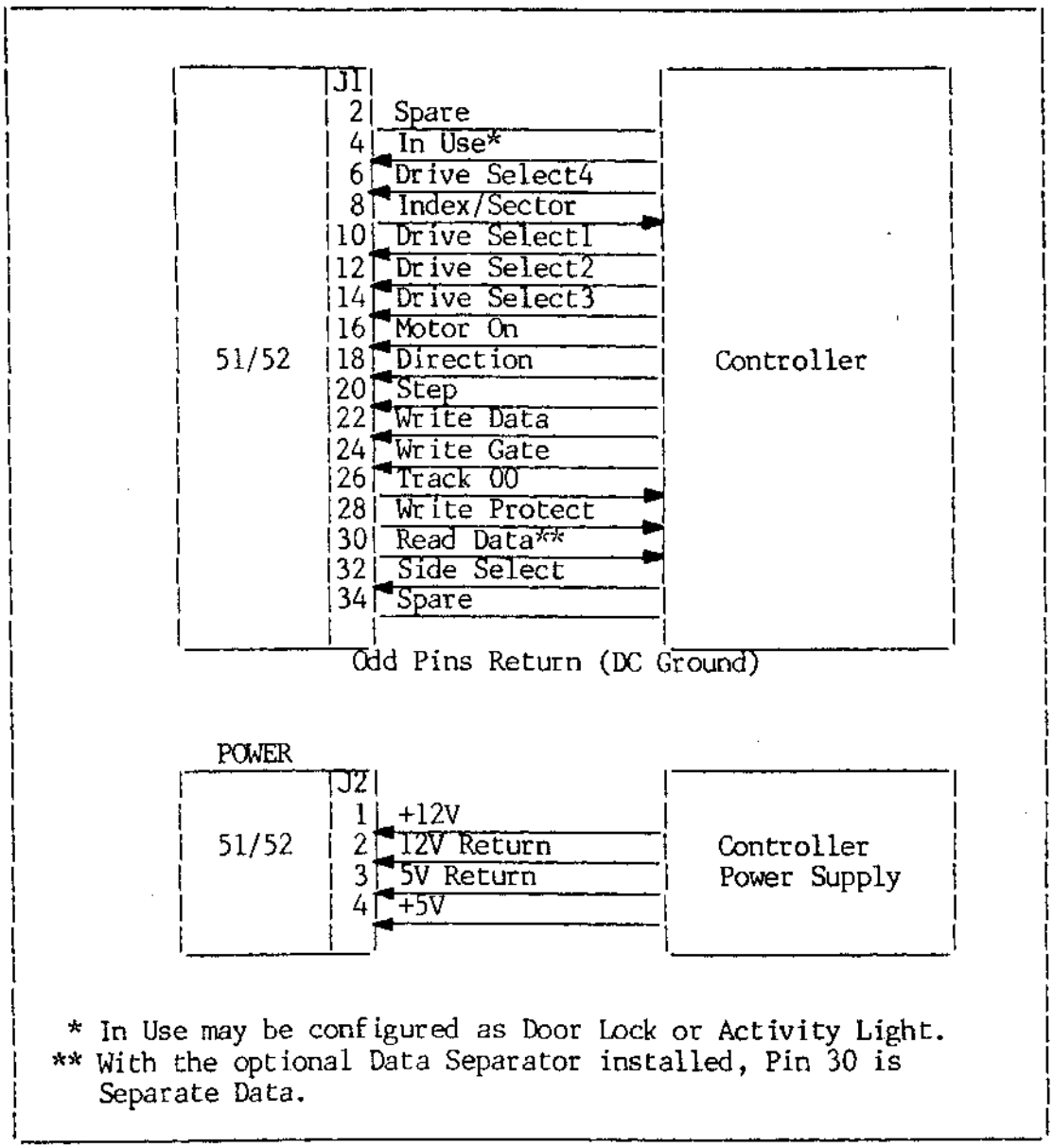


Figure 8-2. Mini Disk Interface Signals

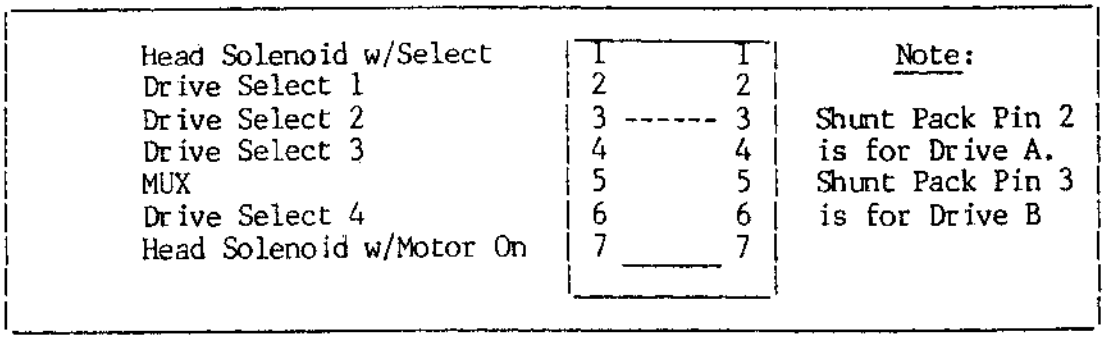


Figure 8-3. M.P.I. Shunt Configuration

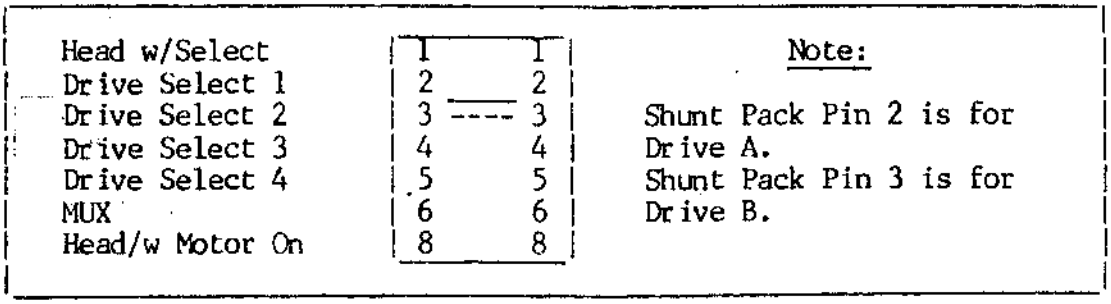


Figure 8-4. Tandon T100 Shunt Configuration

OVERVIEW

Multivision 2 and 3 use an SA1004 Disk Drive. This drive is a random access storage device with two non-removable eight inch disks as storage media. Each disk surface employs one moveable head to service 256 data tracks. This disk provides 10 megabytes of storage accessed by four moveable heads. Low cost and unit reliability are achieved through the use of a unique band actuator design. The inherent simplicity of mechanical construction and electrical controls allows scheduled maintenance-free operation throughout the life of the drive. Mechanical and contamination protection for the head actuator and disk are provided by an impact resistant plastic and aluminum enclosure. A self-contained recirculating system supplies clean air through a .3 Micron Filter.

Features

- Unformatted storage Capacity of 10.67 megabytes.
- Double density recording with encoding and write precomp.
- Proprietary fast flex 111 band actuator
- 4.34M Bits/second transfer rate

The Hard Disk Drive consists of: read/write and control electronics, read/write heads, track positioning mechanism, media, and air filtration system. These components interpret and generate control signals, position the heads over the selected track, and read and write data.

Read/Write Electronics

The standard electronics are packaged on a single printed circuit board containing the following:

- Index Detector Circuit
- Head Positioning Actuator Driver
- Read/Write Amps
- Drive Ready Timers
- Drive Select Circuit
- Write Fault Detection Circuit
- Read/Write Head Select Circuit
- Step Buffers with Ramp Stepper Circuit
- Track 000 Indicator

Read/Write Heads and Disks

The recording media consists of a lubricated thin magnetic oxide coating on a 200 mm DIA aluminum substrate. This coating formulation, together with the low load force/low mass Winchester type flying heads, permit reliable contact start/stop operation. Data on each disk surface is read by one read/write head, each of which accesses 256 tracks. The ten megabyte drive configuration has two disks with four read/write heads.

Using our format, the disk is broken down as follows:

Four sides/drive
256 cylinders/drive
32 sectors/side
256 bytes/sector

SPECIFICATIONS

Physical Specifications

Environmental Limits

Ambient Temperature	=	50° to 115°F (10° to 46°C)
Relative Humidity	=	8% to 80%
Maximum Wet Bulb	=	78° non-condensing

AC Power Requirements

50/60Hz + 0.5Hz
100/115 VAC Installations = 90-127V at 1.1A typical
200/230 VAC Installations = 180-253V at 0.6A typical

DC Voltage Requirements

+24VDC ± 10% 2.8A typical during stepping
(0.2A typical steady state, non stepping)
+5VDC ± 5% 3.6A typical
-5VDC ± (-7 to -16VDC optional) .2A typical

Mechanical Dimensions

	Rack Mount	Standard Mount
Height =	4.62 in. (117.3mm)	4.62 in. (117.3mm)
Width =	8.55 in. (217.2mm)	9.50 in. (241.3mm)
Depth =	14.25 in. (362.0mm)	14.25 in. (362.0mm)
Weight =	17 lbs.(7.7Kg)	17 lbs.(7.7Kg)

Heat Dissipation = 511 BTU/Hr. typical (150 Watts)

Reliability Specifications

MTBF: 8,000 POH typical usage
PM: None required
MTTR: 30 minutes
Component Life: 5 years

Error Rates:

Soft Read Errors:	1 per 10^{10} bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^{6} seeks

Performance Specifications

Capacity	SA1004
Unformatted	
Per Drive	10.67 M bytes
Per Surface	2.67 M bytes
Per Track	10.4 K bytes
Formatted	
Per Drive	8.4 M bytes
Per Surface	2.1 M bytes
Per Track	8.2 K bytes
Per Sector	256 bytes
Sectors/Track	32
Transfer Rate	4.34 Mbits/sec
Access Time	
Track to Track	19 msec
Average	70 msec
Maximum	150 msec
Average Latency	9.6 msec

Functional Specifications

Rotational Speed	3125 rpm
Recording Density	6270 bpi
Flux Density	6270 fci
Track Density	172 tpi
Cylinders	256
Tracks	1024
R/W Heads	4
Disks	2

OVERVIEW

The power supplies used in Multivision are of standard linear design. They provide stable, reliable DC output power at low cost.

Schematics and specifications for 285-02600 (MVI) and 285-02700 (MV2) are contained in this section.

MULTIVISION 1 POWER SUPPLY SPECIFICATIONS

Output Voltage	5.2 V	+12 V	-12 V
Current	7.0 A	4.0 A	0.5 A
Setting @ 115/230 VAC	5.2 V		
No Load	4.9-5.5 V Adjustable range	11.6 - 12.24 Fixed	11.76 - 12.24 Fixed
Line Regulation	.1%	.1%	.25%
Typical	2 MV	6 MV	10 MV
Load Regulation (See Note)	.2%	.2%	.5%
Typical	6 MV	10 MV	10 MV
Ripple (P-P)	10 MV	10 MV	25 MV
Typical	5 MV	6 MV	10 MV

Overload Protection — All outputs must be protected against continuous overload and short circuit. Recovery shall be automatic upon removal of overload condition.

+5 V and +12 V outputs are protected by a current foldback circuit.

Foldback of +5 V output shall be between 8 and 10 amps.

Foldback of +12 V output shall be between 4.6 and 5.5 amps.

The -12 V circuit IC regulator has internal current limit protection and thermal shutdown.

Short circuit for the +5 V output shall be less than 3.5 A and for +12 V output, less than 1.2 A.

Overvoltage Protection — +5 V circuit shall be protected by O.V. crowbar circuit. Trip point shall be between 6.5 and 7.5 V. The +12 VDC output have a combined crowbar preset between 13.5 and 15 V for each output. Reset requires interruption of line voltage.

Temperature Coefficient — .025%/°C

Stability — 0.1% for any 8 hour period after 30 min. stabilization

Operating Temperature — 0° to 50°C

Storage Temperature — -55° to +85°C

Cooling — The power supply is designed for operation with forced air over power supply heatsink area utilizing a 70 CPM fan.

Fusing — To protect the power supply from internal faults, an input fuse should be used.

For 115 V input use 3 A Slo-Blo
For 230 V input use 1.5 A Slo-Blo

Thermostat protection shall be provided to turn off AC input in the event that heatsink temperature exceeds 100°C (permissible range 100°-108°C).

NOTE

Connections to load and test instruments for the purpose of specifying and measuring load regulation are listed below. This is done to minimize the voltage drop in the test connector.

Output	+5 V	+12 V	-12 V
Load Connection (J2) Pin 1 and 3 Common return	2	6	7
Test pins (J2) Pin 5 in common	4	8	7

MULTIVISION 2 POWER SUPPLY SPECIFICATIONS

Output Ratings

Output #	1	2	3	4	5
Voltage	+24V	+5V	-5V	+12A	-12V
Current	3A (see note A)	11A	1A	2A	.5A
Adjustment Range	±1V	±.25V	Fixed 4.75-5.25V	±.6V	Fixed 11.4-12.6V
Line regulation	.02%	.1%	.1%	0.5%	.16%
Typical	<3 mV	<2 mV	<3 mV	<3 mV	<5 mV
Load regulation (see Note 2)	.1%	.3%	1.2%	.2%	.5%
Ripple mV (P.P.)	10 mV	10 mV	10 mV	10 mV	12 mV
Typical	<5 mV	<5 mV	<5 mV	<5 mV	<5 mV

Temperature Coefficient	.025%/°C
Stability	.1% for any 8 hour period after 30 minutes stabilization.
Operating Temperature	0° to 50°C
Storage Temperature	-55° to 85°C
Cooling	The power supply shall be operated with forced air over power supply heatsink area utilizing at CFM fan. A thermostat shall interrupt input power in case of an excessive heatsink temperature.

To protect the power supply from internal faults, an input fuse shall be used.

For 115V input use 6.2A
For 230V input use 3.2A

NOTES

1. 24V output shall have a peak current capability of 5A.

2. Load regulation to be measured directly at output connector.

3. Output 3 and 5 are protected by current limiting 2.2A max and the I.C.'s have internal thermal shutdown.

4. Output 1, 2 and 4 shall be potentiometer adjustable.
   Output 3 and 5 shall be fixed.
   Specified setting to be measured at no load.

5. Overvoltage protection reset requires interruption of input voltage.

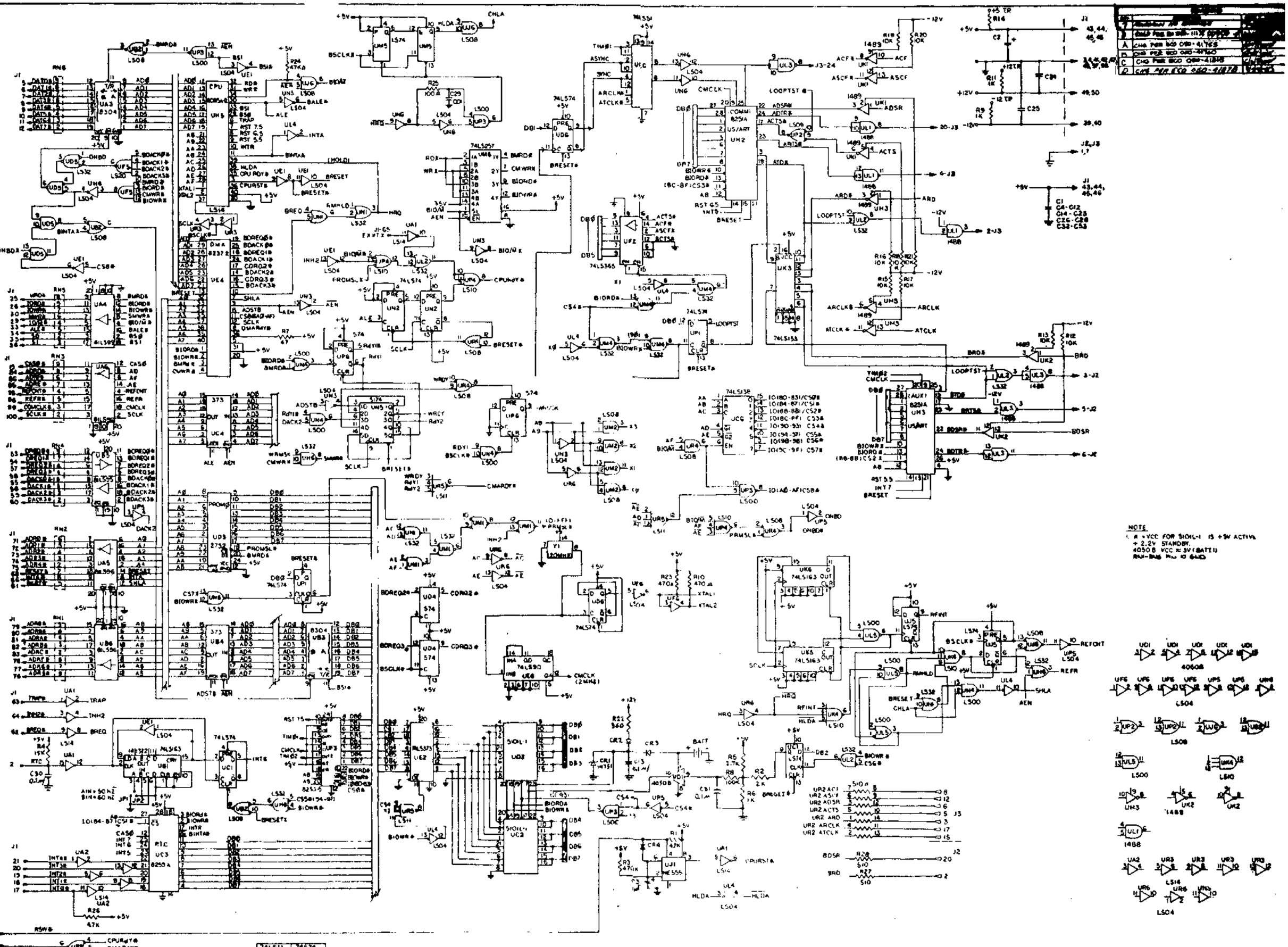
Overload protection — All outputs, except output #1 (+24V), must be protected against continuous overload and short circuit (see Note 5).

Output #	1	2	3	4	5
Overvoltage Protection Limit	N.A.	6-7V	6-7.5V	13.8-15.6V	13.8-15.6V
Current Limit	5.75-6.5A	12.65-14.3A	(see Note) 3	2.4-2.8A	(see Note) 3
Short Circuit Current	1.8-2.5A	6-8A	(see Note) 4	.9-1.3A	(see Note) 4

SECTION 11:

SCHEMATICS

This section contains a complete set of schematics for the Multivision Computer System.



REF. DESIG.	74LS00	74LS04	74LS08	74LS10	74LS14	74LS20	74LS32	74LS51	74LS74	81LS95	81LS96	74LS138	74LS153	74LS163	74LS174	74LS257	74LS365	74LS373	2732	4050B	8085A-2	8251A	8253	1488	1489A	MK5565	8253-5	8255A	8304
	UE6	UR4 UL3 UP3	UR3 UR5 UP1 UH6	UB2 UH2 UR4 UJ6 UP2	UP4	UR4	UA2 UR3	UA1	UF5	UH1 UH6 UB4 UL2	UB5 UB6 UH1	UA4 UA5 UA6	UR5 UR6 UB1	UK5 UK6 UB1	UH5	UH6	UF2	UB4 UC4 UE2	UD3	UD1 SEE NOTE 1	UD2 UC2 SEE NOTE 1	UH5	UH2 UH3	UE4	UL1 UL3	UK1 UH3 UR2	UD1	UF3	UC3	UA3 UB3
	8	14	14	14	14	14	14	14	14	20	20	16	16	16	16	16	20	20	24	n.c.	n.c.	40	26	31		14	8	24	28	20
	10	7	7	7	7	7	7	7	7	10	10	8	8	8	8	8	10	10	12	8	22	20	4	20	7	7	1	12	14	10
																									14					
																									7					

A	CHG PER ECO 080-41365
B	CHG PER ECO 080-41548
C	CHG PER ECO 080-41818
D	CHG PER ECO 080-41878

ADDS
SCHMATIC DIAGRAM
CPU BOARD

NOTES: 1- ALL RESISTORS ARE IN OHMS, 1/4 W 5% UNLESS OTHER WISE SPECIFIED.
2- ALL CAPACITORS IN UFD UNLESS OTHER WISE SPECIFIED.

REV	DESCRIPTION
C	REVISED
B	REV PWR, GRND - ///REVISED
-	REL PRE PRODUCTION

ADDS

SCHEMATIC DIAGRAM
DYNAMIC RAM BOARD

135-23300

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
1	EN 051-11175 CCCCCC	2-26-81	
-	EN 051-11402 REL. FOR PROD	7/28/81	

IOWR-IORD

IOW-

RST-

+5V

INT-
IOWR-
IORD-
IO/M-
ADRC
ADRF
ADRD
ADRB
ADRA
ADRD
ADRB
ADRE
SRESET-

DAT 0
DAT 1
DAT 2
DAT 3
DAT 4
DAT 5
DAT 6
DAT 7

+5V

+ C5 22uf + C31 22uf

UA2 UB7 UB2 UB3 UB7 UB2 UA7 UB7 UC2

C33 22 PF C32 22 PF Y2 4.00

UD6 8035

UA4 374 UE3 374 UD3 2716

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

UB7 +5V R20 10K INT-

A B C

HD0 EPC OVRE

UE4 PROG P25 P22 P21 P20 P40 P41 P42 P43 P62 P61 P73 P72 P71 P70 P53 P52 SEL-

CRCE STEP DIR HD2 HD1 M3 M2 M1

UB7 SEL1

UJ4 SEL 0

FLT C

P10 P11 P12 P13 P14 P15 P16 P17

UF5 42

RCD- BR- INTA- IWR- WRH- WRH1- WRH2- WRH3-

-2V

SIO

UA6 374 UB4 UB6

A-

UA2 UA2 UA1

UB3 UD1 SND- RCLK

IOW-

UA1

IOWR-

MWR

UB7 UD1 UC1 UB3 UD2 OVRE

UB1 UA2 UA3 UA3

J1 60 DACK3-

RCO-

IORD-

P13 P12 P11 P10 P17 P16 P15 P14

UB1 UB2 UB1 J1 60 DRQ3

CWR-

TOLERANCES: 1/64 .005 1° FRAC DEC ANG DO NOT SCALE DWG		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN MAI 2/24/81		SCHEMATIC DIAGRAM CONTROLLER
CHECKED		
ENGR	3/12/81	
APPROVED		SIZE C SCALE - SHEET 1 OF 6 DWG NO 135-28700 REV -

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
7	REDRAWN		
8	EN 051-11175 PRR#		
-	REL FOR PRODUCTION		

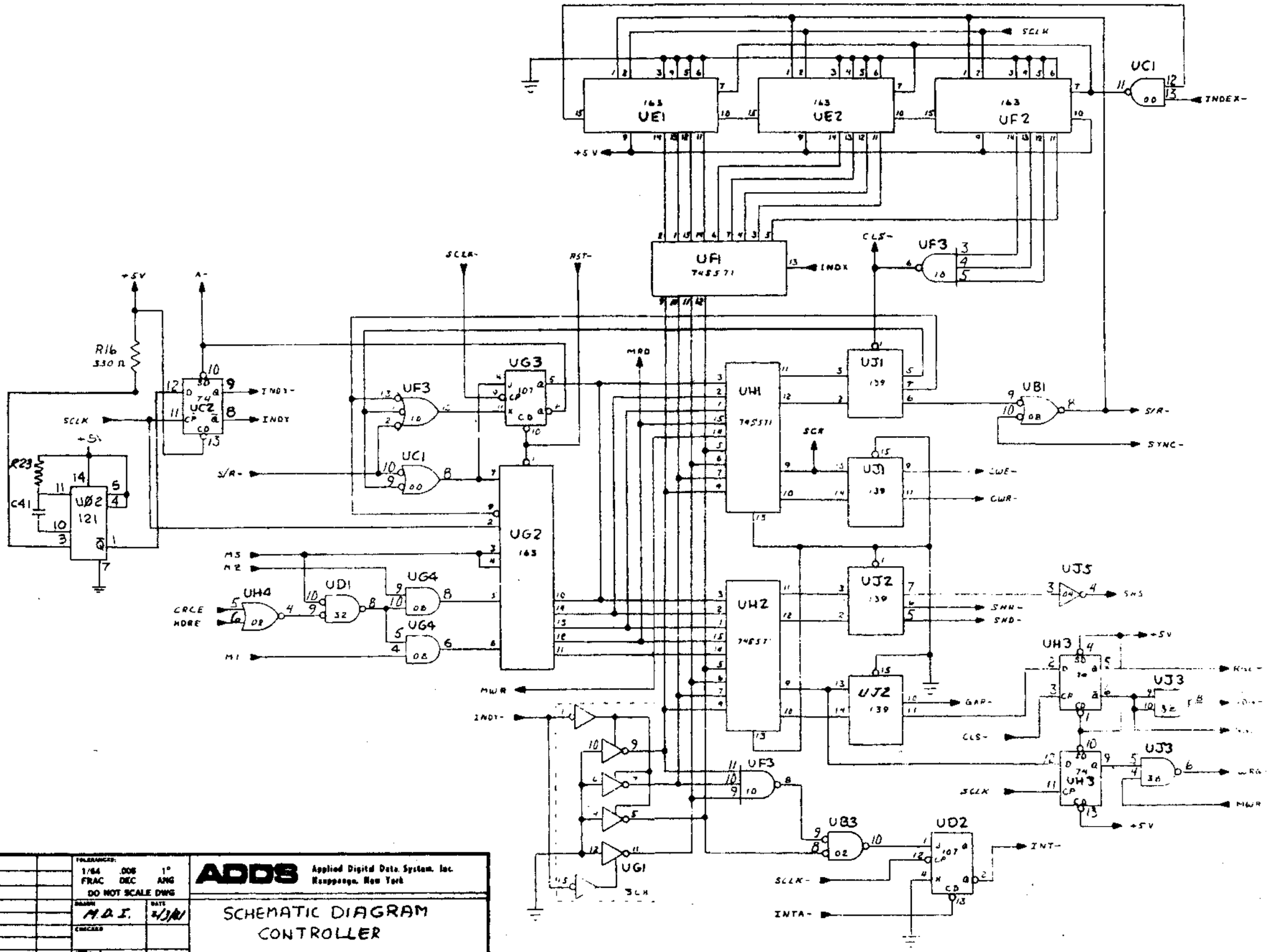
NOTES
1. ALL RESISTORS IN OHMS 1/4W 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS IN UFD UNLESS OTHERWISE SPECIFIED.

ADDS Applied Digital Data Systems, Inc. Hauppauge, New York

SCHEMATIC
I/O CONTROLLER

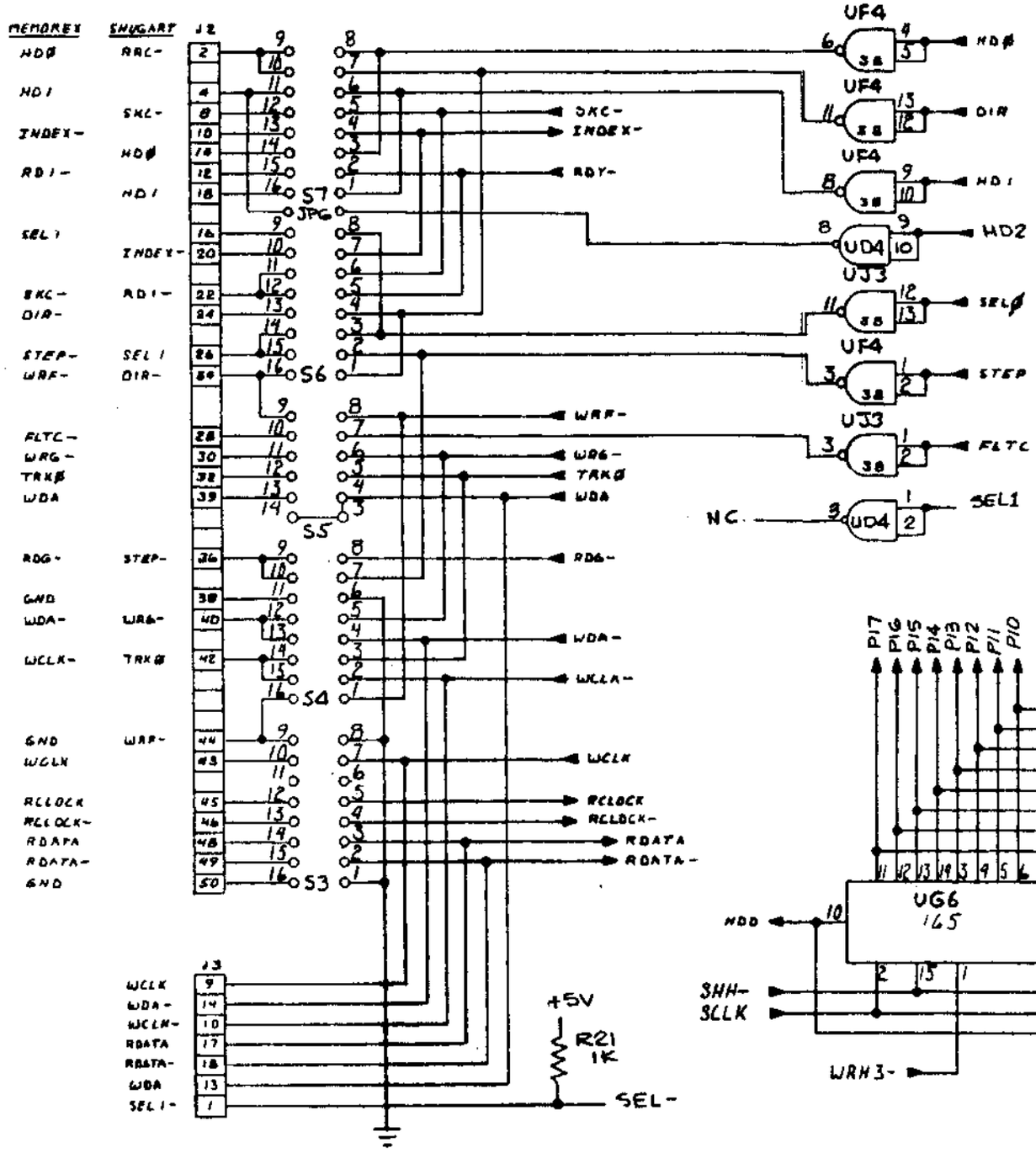
135-24700 D

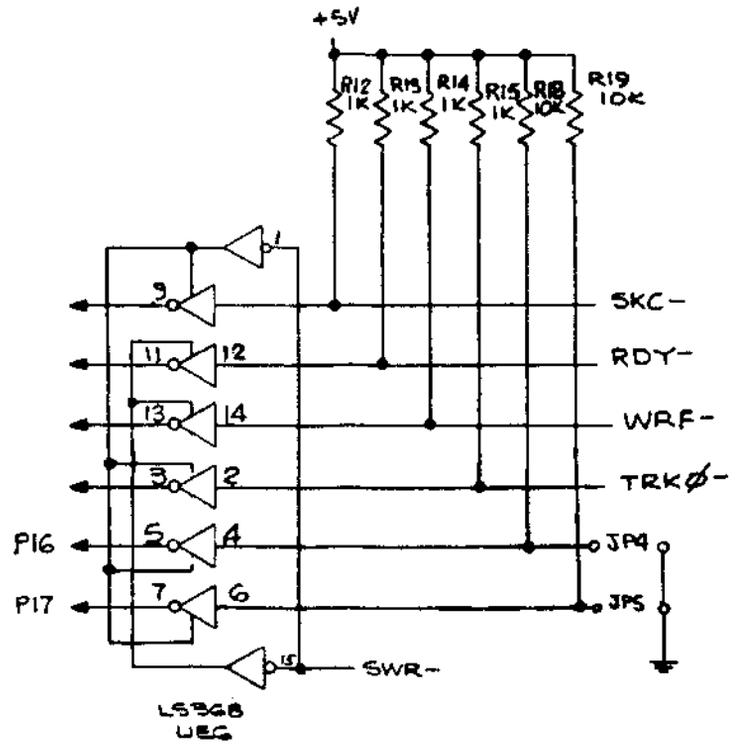
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1 FOR REV LEVEL		JXL

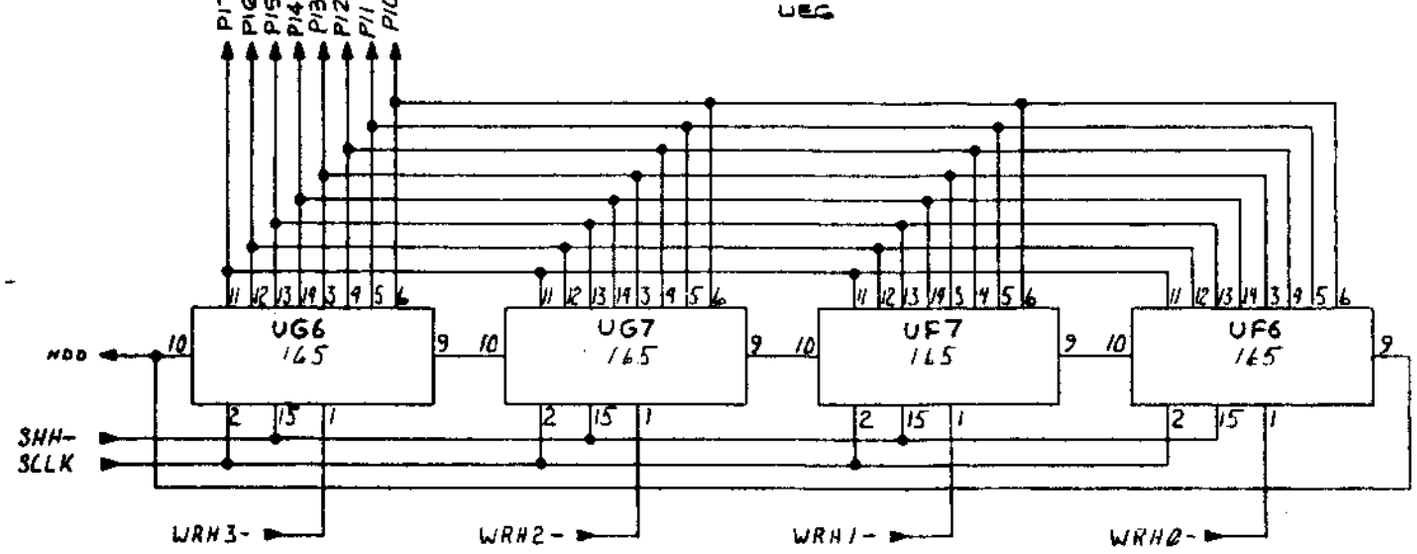


		TOLERANCES: 1/64 .005 1° FRAC DEC ANG DO NOT SCALE DWG	ADDS Applied Digital Data Systems, Inc. Hauppauge, New York		
		DRAWN M.D.I.	DATE 2/3/81	SCHEMATIC DIAGRAM CONTROLLER	
		CHECKED			
		ENGR	2/11/81		
		APPROVED		SIZE C	SCALE 2/3 SHEET 2 OF 6
				DWG NO 135-28700	REV —
USED ON	QTY				

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1 FOR REV. LEVEL	2-26-81	







NOTES: UNLESS OTHERWISE SPECIFIED

1. ODD NUMBERED PINS 1 THRU 37, 41 AND 47 OF J1 ARE CONNECTED TO GROUND.
2. PINS 2,4,6,8,11,12,15,16,19 AND 20 OF J3 ARE CONNECTED TO GROUND
3. WHEN JP1 IS INSTALLED, UL2 IS NOT INSTALLED, Y1 IS INSTALLED.
4. J4 NOT SHOWN IS A 34 PIN CONNECTOR WITH THE SAME PINOUTS AS J1, EXCEPT FOR THE FOLLOWING CONNECTIONS

J4	TO J1
6	40
10	42
12	44
24	36

TOLERANCES: 1/64 FRAC, .005 DEC, 1° ANG. DO NOT SCALE DWG

DRAWN: M.O.I. 2/[illegible]

CHECKED:

APPROVED: [illegible] 3/11

USED ON | QTY

ADDS Applied Digital Data Systems, Inc. Hauppauge, New York

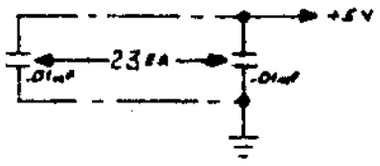
SCHEMATIC DIAGRAM
CONTROLLER

SIZE C | SCALE [illegible] | SHEET 3016 | DWG NO 135-28700 | REV —

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1 FOR REV LEVEL	2-26-81	

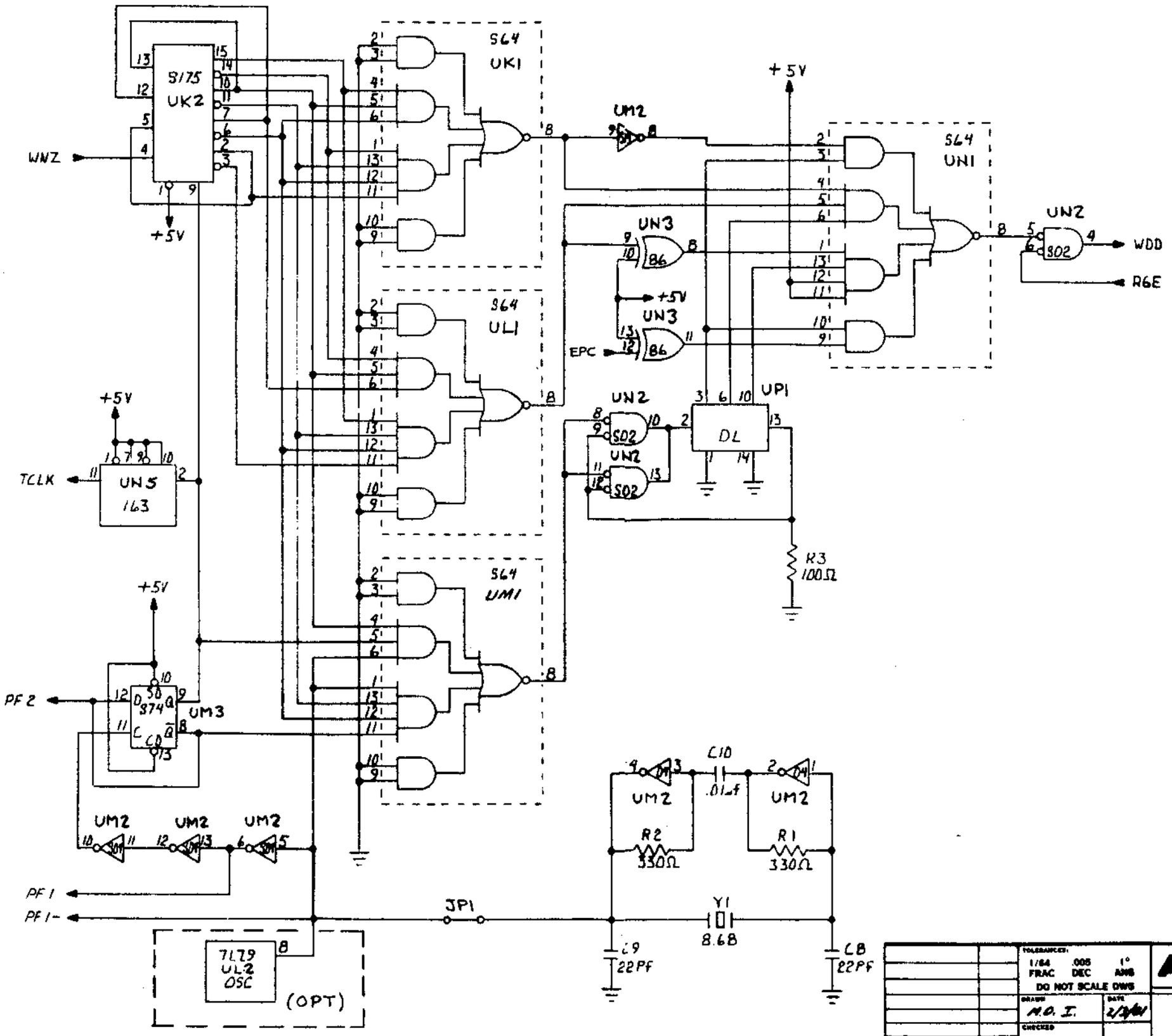
RDATA
RDATA-
+5V
UP7
75107B
RDI
SID
S2
RDD
UK5
MWR-
MWR
UJ5
UH4
CWR-
GAP-
UH6
UG4
UG3
HDD
SHH-
SOD
UH5
HORG
INT-
CWE-
UJ7
95
UK7
UK6
UJ6
SCLK-
SCLK
RCLK
UJ4
UG5
ZNBY-
CALE
RCLOCK
RCLOCK-
RDCL
-12V
220Ω
R11
C37
.01MF
IN751
CR3
Z2
51Ω
260
MRD
UH7
75113
WCLK
WCLK-
TCLK
WDA
WDA-
+5V
UN7
UN2
UN3
UM5
86
00
GAP-
WDD
SYNC-

C1-4, C6-C9, C11-C18, C22-C30, C34, C35

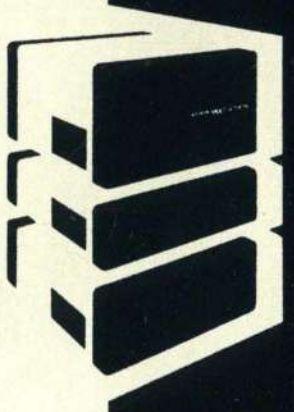


USED ON	QTY	TOLERANCES: 1/64 FRAC, .005 DEC, 1° ANG. DO NOT SCALE DWG.	ADDS Applied Digital Data Systems Inc. Hauppauge, New York		
		DRAWN M.O.S. 2/13/81	SCHEMATIC DIAGRAM CONTROLLER		
		CHECKED			
		ENGR Q.L. 3/11/81			
		APPROVED	SIZE C	SCALE NONE SHEET 4 OF 6	DWG NO 135-28700 REV —

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1 FOR REV. LEVEL		922



USED ON	QTY	TOLERANCES: 1/64 FRAC, .005 DEC, 1° ANG. DO NOT SCALE DWG	ADDS Applied Digital Data System, Inc. Hauppauge, New York		
		DRAWN M.O.I. 2/7/84	SCHEMATIC DIAGRAM CONTROLLER		
		CHECKED			
		ENGR			
		APPROVED	SIZE C	SCALE SHEET 5 OF 6	DWG NO 135-28700 REV —



ADDS

Applied Digital Data Systems Inc.

SOMETHING EXTRA IN EVERYTHING WE DO

516 - 30600