SA800 Series Diskette Storage Drive

Double Density Design Guide

Application Bulletin

Shugart Associates

SA800 Series Diskette Storage Drive

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Table of Contents

List of Illustrations

1.0 Introduction

This Application Bulletin provides the reader with a basic understanding of double density encoding which can be employed in the Shugart Associates SA800 Series Diskette Storage Drive.

1.1 General

Single density drives use the double frequency (2F) non return to zero (NRZI) method of recording. Double frequency is the method of inserting a clock bit at the beginning of each bit cell, thereby doubling the frequency of the recorded bits.

In double density a clock bit is not written at the beginning of a bit cell if a data bit is present. This reduces the size of the bit cell by one-half and, thus, doubles the space available for data. Table 1 is a comparison of single density and double density capacities.

This decreased size of the bit cell makes encoding prior to writing on the disk and decoding when reading from the disk more difficult which results in more complex circuitry. Another factor is, with a smaller bit cell tolerance to bit shift is less and additional circuitry must be designed for this smaller tolerance. Figure 1 provides a simple overview of single and double density systems.

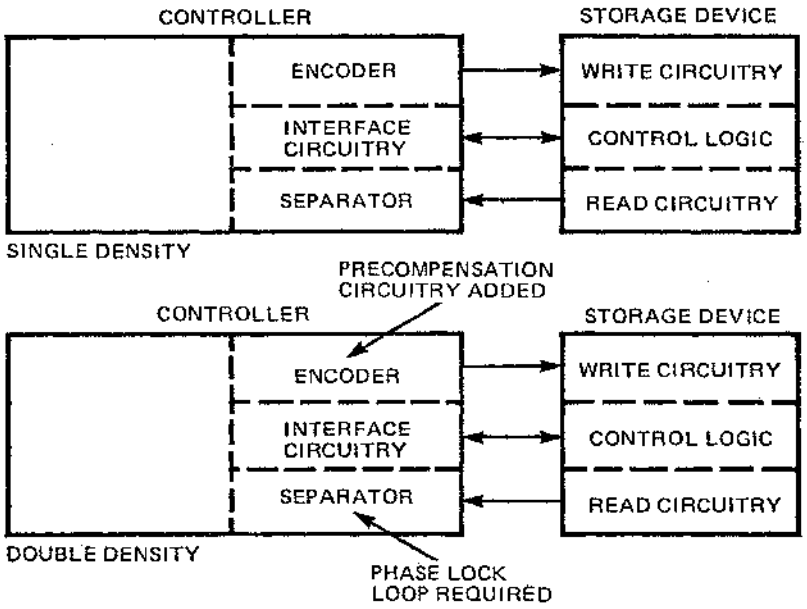


FIGURE 1 SYSTEM OVERVIEW

Comparison

	FM Single Density	MFM/M^{2}FM Double Density
■ Unformatted Capacity		
bits/diskette	3,208,128	6,416,256
bits/track	41,664	83,328
■ Formatted Capacity		
8 records – bits/diskette	2,523,136	5,046,272
" bits/track	32,768	65,536
15 records – bits/diskette	2,365,440	4,730,880
" – bits/track	30,720	61,440
26 records – bits/diskette	2,050,048	4,100,096
" – bits/track	26,624	53,248
32 records – bits/diskette	N/A	5,046,272
" – bits/track	N/A	65,536
■ Format Efficiency		
8 records (IBM)	78.6%	78.6%
15 records (IBM)	73.7%	73.7%
26 records (IBM)	63.9%	63.9%
32 records (Shugart)	N/A	78.6%
■ Transfer Rate		
kilobits/second	250	500
kilobytes/second	31.25	62.5
■ Density at Track 76		
bits/inch (BPI)	3268	6536
flux changes/inch (FCI)	6536	6536

TABLE 1. COMPARISON (SINGLE AND DOUBLE DENSITY)

Table 2 illustrates the degree of difficulty in implementing a double density system assuming the current level of read/write head/media resolutions and electronic technology.

	FM	MFM	M^2FM	GCR
Established in hard disk drives	Yes	Yes	No	No
Encoder complexity	Simple	Moderate	Moderate	Complex
Precompensation required	No	Yes	Yes	Probably
R/W head switching problem	No	No	No	Probably
High resolution head required	No	Yes	No	Yes
High resolution media required	No	Yes	No	Yes
Low head/media resolution problem	No	Bit Shift	No	Bit Shift
High head/media resolution problem	No	No	Droop	Droop
Droop circuitry required	No	No	Yes	Yes
Media certification problem	No	No	No	Probably
Read channel gain affected	–	No	No	Yes
Read channel bandwidth affected	–	No	Low End	Both Ends
Separator complexity	Simple	Moderate	Moderate	Complex

TABLE 2. IMPLEMENTATION COMPARISON

2.0 DISKETTE FORMATS

2.1 General

This section discusses the various track formats that may be utilized with double density encoding.

2.2 Storage Device Parameters Affecting Format

The following parameters should be considered when selecting a format:

- minimum length of inside track
- rotational tolerance
- instantaneous revolution tolerance
- physical index variation
- write oscillator tolerance
- read preamplifier recovery time
- maximum bytes between the end of erase core and R/W gap.
- nominal byte time
- nominal rotational time
- nominal bytes per track

2.3 Soft Sector

Soft sector is the physical allocation of space on the storage media. Each track, one revolution of the media, is divided into a number of records. For the purpose of discussion, let us define the areas of the single density 26 records per track format as introduced by IBM (Figure 2). See Figure 3 for comparison to MFM and M^2FM format areas.

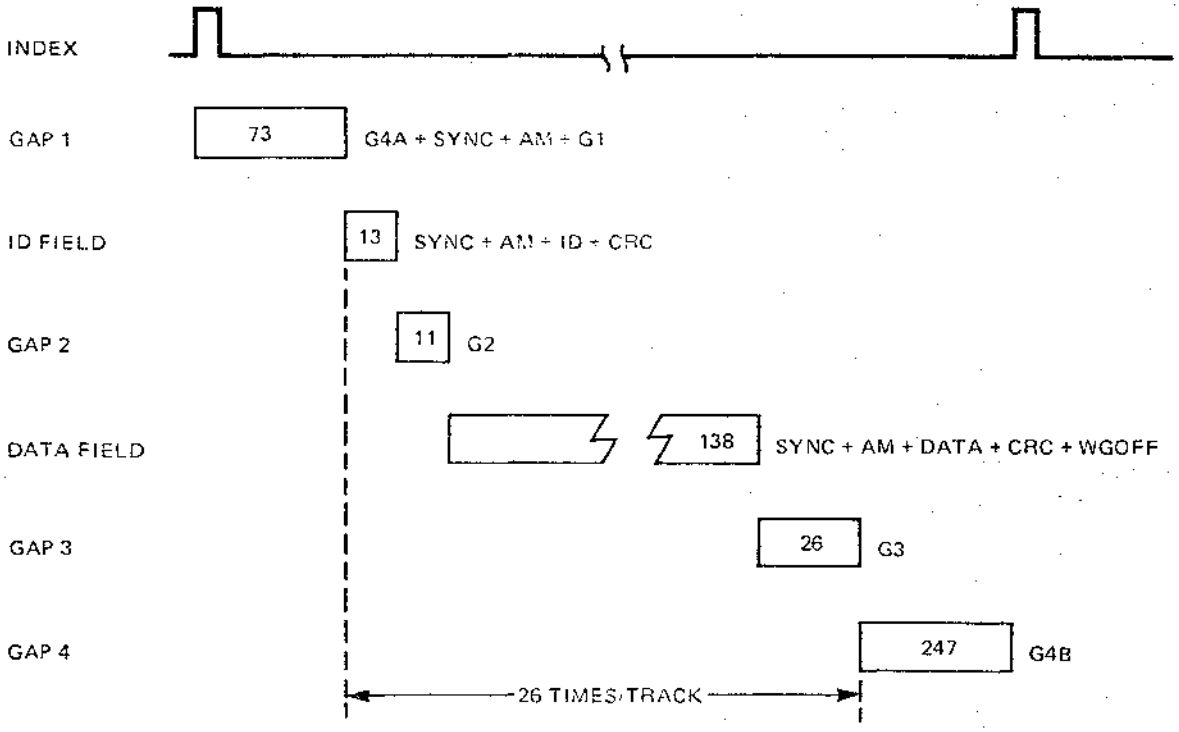


FIGURE 2 TRACK FORMAT

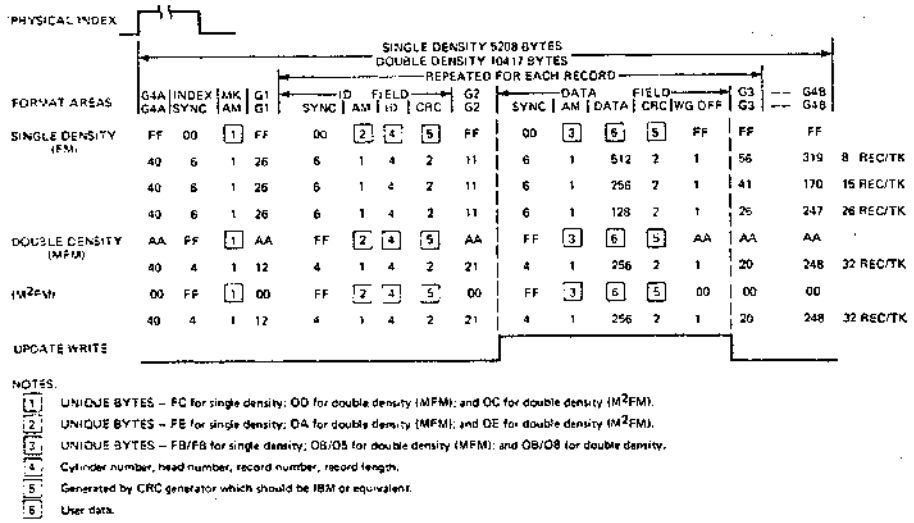


FIGURE 3 SOFT SECTOR COMPARISON

Index is the physical detector indicating one revolution of the media and is used to initiate format operations, generate the Ready signal in the storage device, insure one complete revolution of the media has been searched, and for a deselect storage device signal after a certain number of revolutions.

Gap 1 – **G4A** is from the physical index to index address mark sync and allows for physical index variation, speed variation and interchange between Storage Devices.

Sync is a fixed number of bytes for Separator synchronization prior to the address mark. It includes a minimum of two bytes plus worst case Separator sync up requirements.

Address Mark is a unique byte to identify the Index Field and is not written per the encode rules. (Refer to Figure 4).

G1 is from index address mark to ID field address mark sync.

ID Field – **Sync** is a fixed number of bytes for Separator synchronization prior to the AM. Includes a minimum of two bytes plus worst case Separator sync up requirements.

AM is a unique byte to identify the ID Field and not written per the encode rules (refer to Figure 5).

ID is a four byte address containing cylinder number, head number, record number, and record length.

CRC is two bytes for cyclic redundancy check.

Gap 2 – Gap from ID CRC to data AM sync and allows for speed variation, oscillator variation, and erase core clearance of ID CRC bytes prior to write gate turn on for an a update write.

Data Field – **Sync** is a fixed number of bytes for Separator synchronization prior to an AM. Includes a minimum of two bytes plus worst case Separator sync up requirements.

AM is a unique byte to identify the Data Field and is not written per the encode rules. (Refer to Figures 6 & 7).

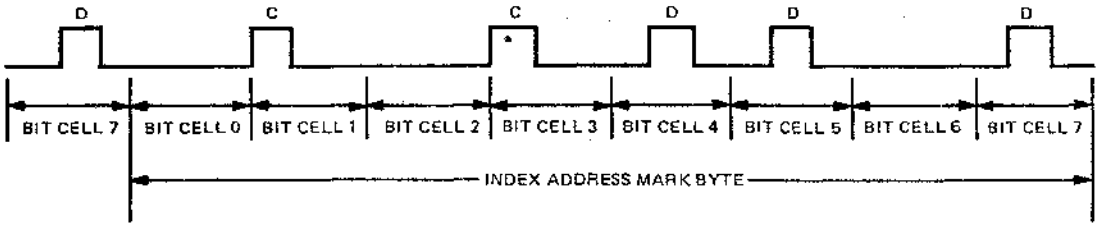
Data is the area for user storage.

CRC is two bytes for cyclic redundancy check.

WG OFF (Write Gate Off) is one byte to allow for Write Gate turn off after an update write.

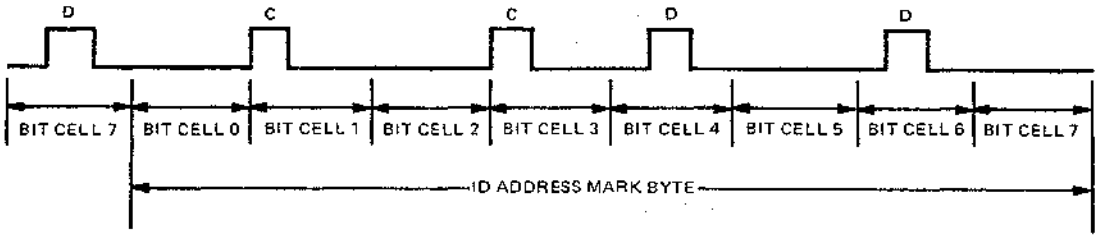
Gap 3 – Gap from WG OFF to next ID AM sync and allows for the erase core to clear the Data Field CRC bytes, speed and write oscillator variation, read preamplifier recovery time and system turn around time to read the following ID Field.

Gap 4 – G4B is the last gap prior to physical index and allows for speed and write oscillator variation during a format write and physical index variation.



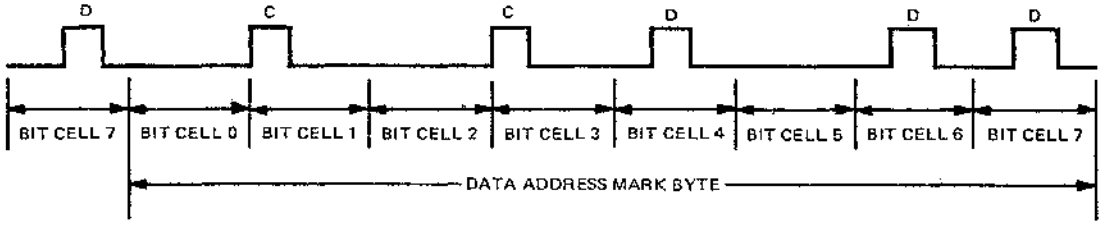
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	0	0	0	0	1	1	0	1	DATA BITS 0D
CLOCK BITS	0	1	0	1	0	0	0	0	CLOCK BITS 50

FIGURE 4 INDEX ADDRESS MARK (MFM)



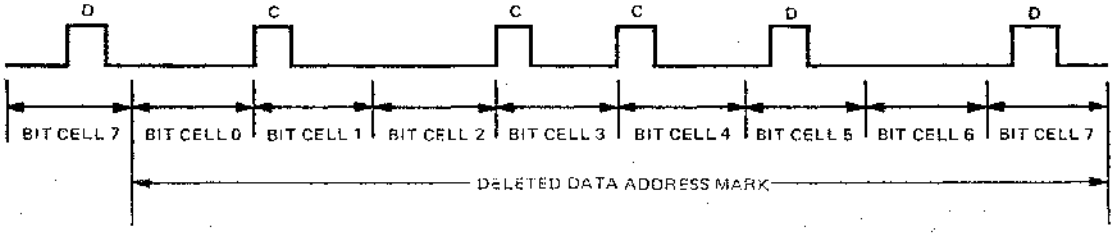
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	0	0	0	0	1	0	1	0	DATA BITS 0A
CLOCK BITS	0	1	0	1	0	0	0	0	CLOCK BITS 50

FIGURE 5 ID ADDRESS MARK (MFM)



BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	0	0	0	0	1	0	1	1	DATA BITS 0B
CLOCK BITS	0	1	0	1	0	0	0	0	CLOCK BITS 50

FIGURE 6 DATA ADDRESS MARK (MFM)



BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	0	0	0	0	0	1	0	1	DATA BITS 05
CLOCK BITS	0	1	0	1	1	0	0	0	CLOCK BITS 58

FIGURE 7 DELETED DATA ADDRESS MARK (MFM)

MAXIMUM FORMATS

FORMAT	G4A	INDEX MK		G1	REPEATED FOR EACH RECORD												G4B
					ID FIELD				G2	DATA FIELD					G3		
5208 BYTES	G4A	SYNC	AM	G1	SYNC	AM	ID	CRC	G2	SYNC	AM	DATA	CRC	WG	OFF	G3	G4B
	40	6	1	26	6	1	4	2	8	6	1		2		1		
RECORDS																	
1												4994			0		110
2												2429			105		5
3												1597			70		41
4												1185			53		59
5												940			43		65
6												776			36		77
7												660			31		81
8												573			27		87
9												505			25		86
10												451			22		95
11												407			21		86
12												370			19		95
13												339			18		91
14												313			17		81
15												289			16		95
16												269			15		95
17												251			14		103
18												236			13		95
19												221			13		100
20												209			12		95
21												197			12		95
22												187			11		97
23												177			11		98
24												168			10		119
25												160			10		110
26												153			10		91
27												146			10		86
28												140			9		95
29												134			9		89
30												128			9		95
31												123			9		82
32												118			8		111

TABLE 3. FM OPTIMIZED FORMATS (MAXIMUM BYTES/RECORD)

MAXIMUM FORMATS

FORMAT	G4A	INDEX MK		G1	REPEATED FOR EACH RECORD											G4B
					ID FIELD				G2	DATA FIELD					G3	
10417	G4A	SYNC	AM	G1	SYNC	AM	ID	CRC	G2	SYNC	AM	DATA	CRC	WG OFF	G3	G4B
BYTES																
	40	4	1	12	4	1	4	2	14	4	1		2	1		
RECORDS																
1												10107		0		220
2												4931		211		10
3												3253		141		79
4												2423		106		112
5												1927		85		135
6												1598		71		148
7												1363		62		154
8												1187		54		168
9												1051		48		172
10												942		44		170
11												852		40		185
12												778		37		184
13												715		34		194
14												661		32		196
15												615		30		190
16												574		28		200
17												538		27		194
18												506		26		190
19												478		24		195
20												452		23		200
21												429		22		196
22												407		21		218
23												388		21		194
24												370		20		208
25												354		19		210
26												339		19		194
27												325		18		208
28												312		17		224
29												300		17		210
30												289		16		220
31												279		16		192
32												269		16		184

TABLE 4. MFM/M^{2}FM OPTIMIZED FORMATS (MAXIMUM BYTES/RECORD

2.4 Soft Sector Optimized Formats

Tables 3 and 4 show the maximum storage available from 1 through 32 records per track for single and double density formats respectively.

The higher data capacity is possible because of the smaller distances from the R/W gap to the rear of the erase core as shown in Figure 8. This allows higher format efficiency with respect to user storage area.

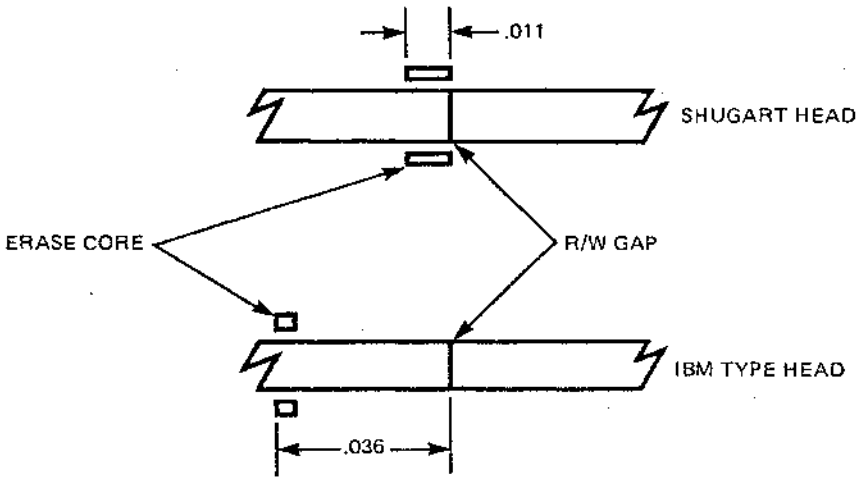
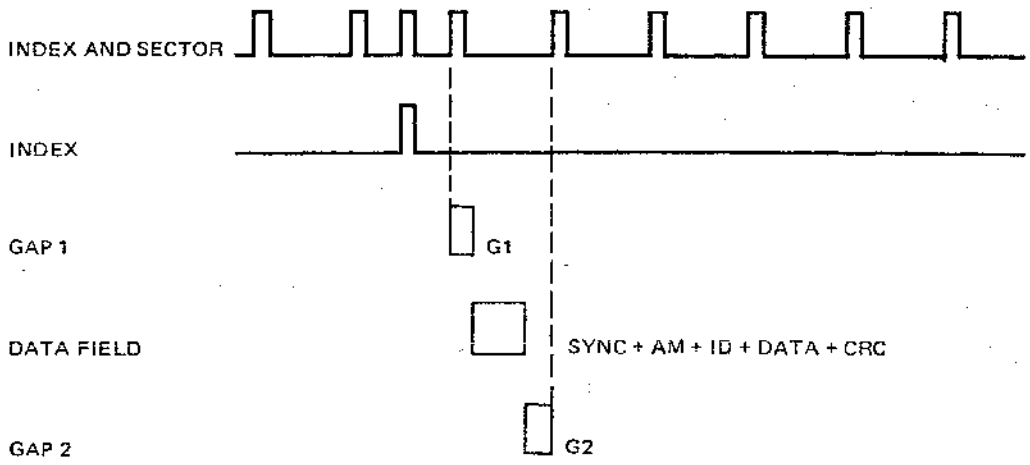


FIGURE 8 HEAD COMPARISON

2.5 Hard Sector

Hard Sector is also the physical allocation of area on the storage media. Each track is subdivided into the number of records (sectors) required. These sectors are prepunched holes on the media with the same radius as the index hole. Once the index is separated from the sector holes, the sectors are sequentially counted from index. This essentially replaces the record number address of the ID field in soft sectored formats. The cylinder and head number should still be included but it is not shown in our recommended formats. The separator sync area is also not shown, but it is a better approach to hard sector formats. With the advent of the single chip IBM type format controller, this hard sector format will undoubtedly disappear.

Figures 9 and 10 illustrate the hard sector format.



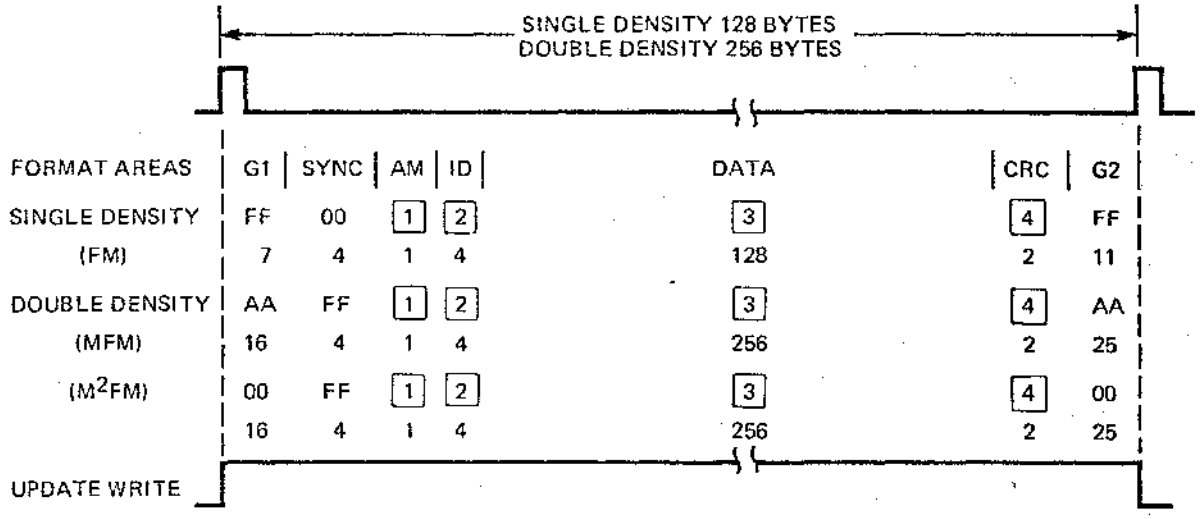
INDEX & SECTOR — Index has the same use as in soft sector once separated from the Sector pulses. The Sector pulses are counted from Index to determine the proper sector.

GAP 1 — This gap is to allow for physical Sector variation, speed variation inclusive of interchange between Storage Devices, and erase core clearance of previous sector.

DATA FIELD — The Sync, AM, DATA, and CRC are identical to the data field in Soft Sector. The new addition is an ID the same as in soft sector.

GAP 2 — This gap is to allow for speed and oscillator variation, physical sector variation, and erase core clearance for a following sector update prior to the next sector pulse.

FIGURE 9 HARD SECTOR FORMAT



NOTES:

1. UNIQUE BYTES – F8 for single density; 0B for double density (MFM or M^2FM).
2. Cylinder number, head number, record number, record length.
3. User data.
4. Generated by CRC generator which should be IBM or equivalent.

FIGURE 10 HARD SECTOR COMPARISON

3.0 ENCODER

The encoder translates serialized data from the controller into a digital code for recording within the Storage Device. This digital code may also include the addition of parity, precompensation, etc., which is dependent on overall system requirements. There are four codes used today, namely FM for single density and MFM, M^2FM, or GCR for double density. GCR is included in this section only for comparison.

See Figure 11 data stream comparison.

3.1 Encoder Rules

FM encode:

1. Write data bits at the center of the bit cell, and
2. Write clock bits at the beginning of the bit cell.

MFM encode:

1. Write data bits at the center of the bit cell, and
2. Write clock bits at the beginning of the bit cell if:
   A. no data has been written in the previous bit cell, and
   B. no data bit will be written in the present bit cell.

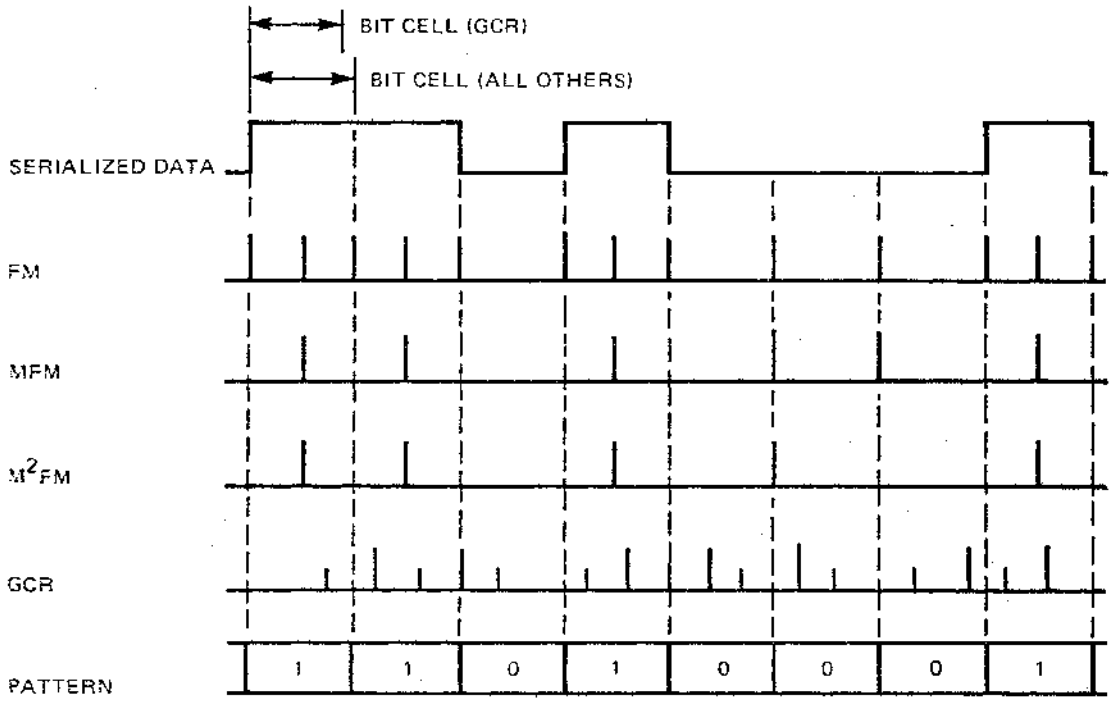
M^2FM encode:

1. Write data bits at the center of the bit cell, and
2. Write clock bits at the beginning of the bit cell if:
   A. no data or *clock* bit has been written in the previous bit cell, and
   B. no data bit will be written in the present bit cell.

GCR encode:

This code translates 4 bits into 5 bits of binary data for storing information and then re-translates the 5 bits into 4 bits during a read operation.

4 Bit Data	5 Bit Recorded Data
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111



Comparison

	FM	MFM	M^2FM	GCR
Bit Cell	4μs	2μs	2μs	1.6μs
Flux changes/cell	2	1	1	1
Flux changes/inch (FCI)	6536	6536	6536	8170
Kilo bits/second (KBS)				
Storage Device	250	500	500	625
System	250	500	500	500
Frequency ratios	2/1	2/1	2.5/1	3/1
Bit to bit spacings	2μs	2μs	2μs	1.6μs
	4μs	3μs	3μs	3.2μs
		4μs	4μs	4.8μs
			5μs	

FIGURE 11. ENCODED DATA STREAM COMPARISON

4.0 MAGNETIC RECORDING

The write element is essentially a ferrite loop with a gap and coil. When current flows through the coil it creates a magnetic flux field across the gap. Around the gap is a fringe field which magnetizes the oxide on the media in one of two directions. As the direction of current is reversed, so is the direction of flux in the gap as well as the magnetization of the oxide. It is this change of direction (transition) that relates to the bit being written (Figure 12).

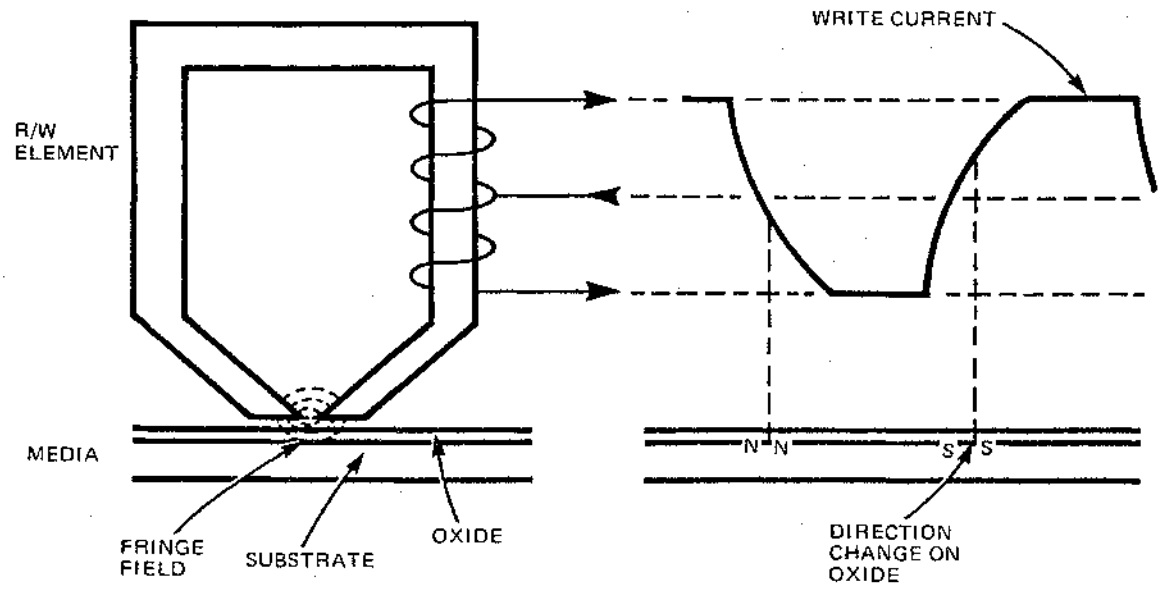


FIGURE 12 RECORDING CURRENT AND FLUX

The read element may be the same as the recording element or physically different, in either case the principle is the same. The coil and gap act as a monitor to detect flux direction changes on the oxide. If there is no direction change directly under the gap, then there is a constant flux from the oxide surface and a voltage is not created from the coil. When a flux direction change is detected the coil generates a voltage pulse (Figures 13, 14 and 15).

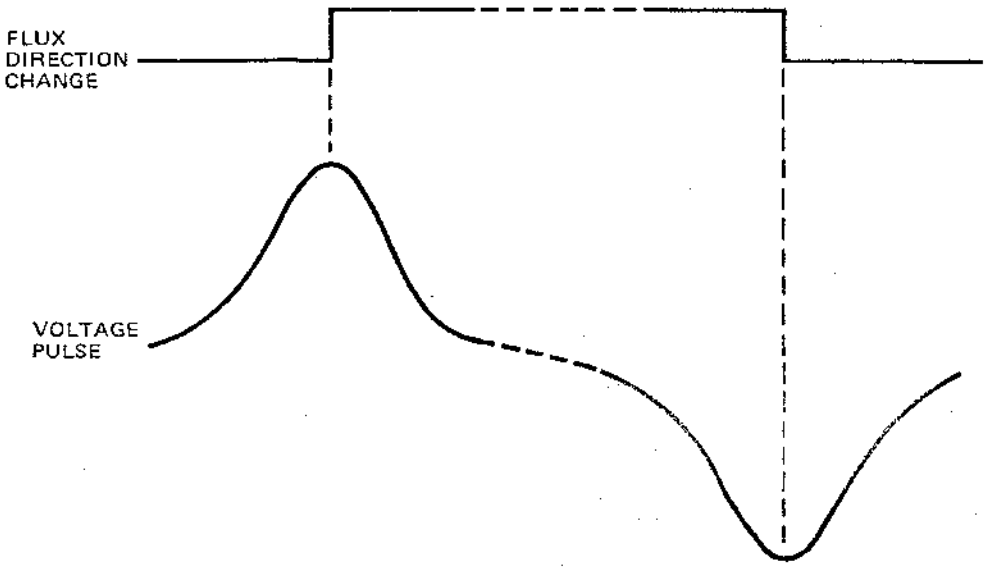


FIGURE 13 READBACK FLUX/VOLTAGE CHANGES

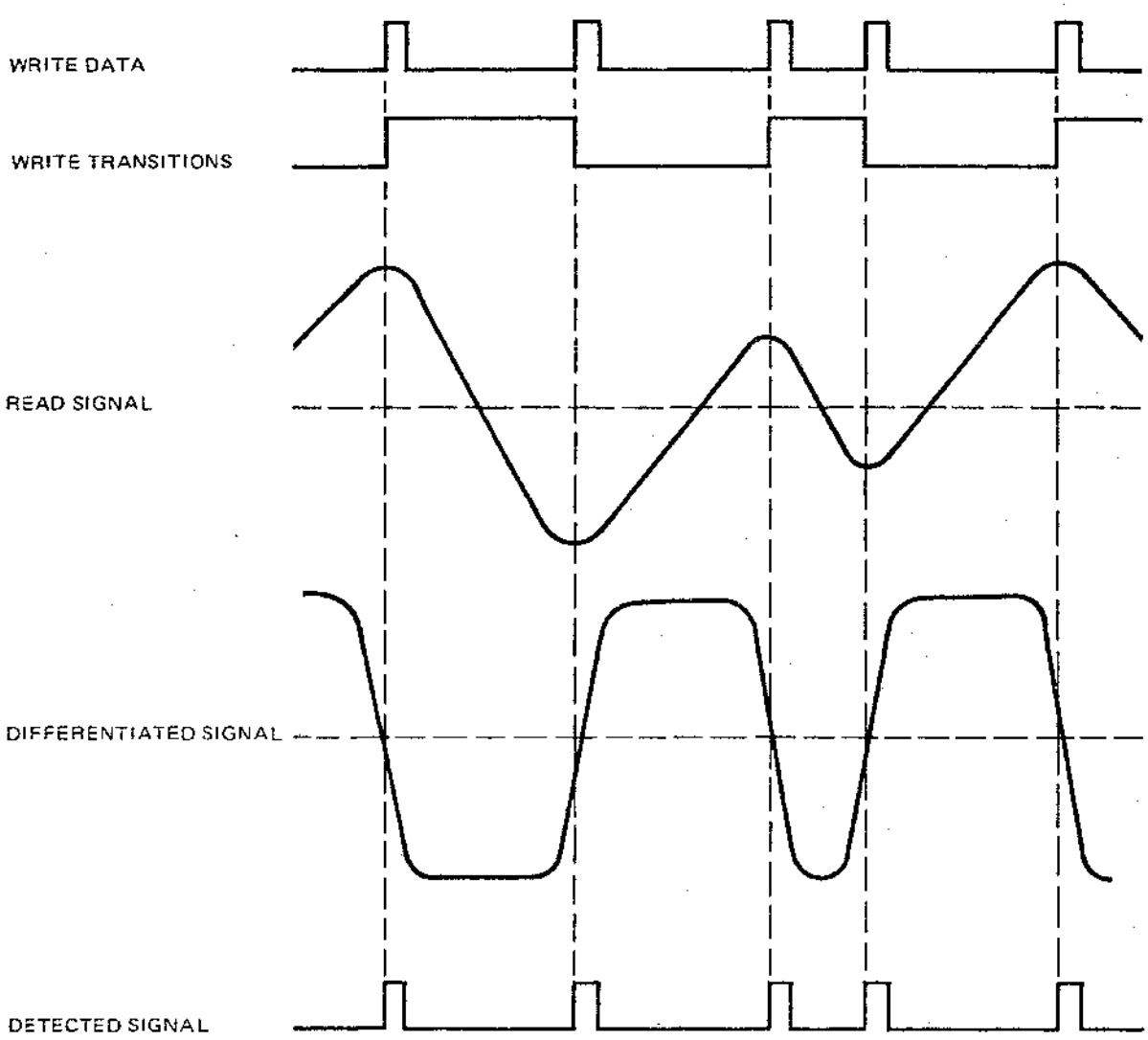


FIGURE 14 STORAGE DEVICE FUNCTION

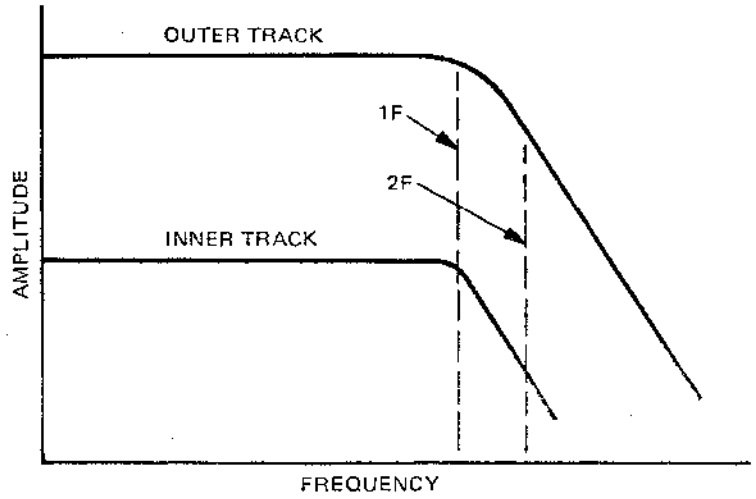


FIGURE 15 STORAGE DEVICE OPERATING RANGE

5.0 MEDIA

5.1 General

The parameters described in this section must be considered when selecting/using media.

5.2 Mechanical Considerations

- substrate material and thickness
- coefficient of expansion
- hygroscopic expansion
- oxide material and thickness
- oxide adhesion to substrate
- oxide wear, abrasion, and durability
- torque within the jacket
- humidity range
- temperature range

5.3 Electrical Considerations

- amplitude limits
- resolution limits
- modulation – period $\geqslant$ 10ms
- drop out – period $\leqslant$ 10ms
- extra bit – 30% of average signal
- write over limit

5.4 Certification/Formatting

- The entire surface area contained within the usable tracks limit is evaluated for extra bits, missing bits, modulation, and minimum amplitude requirements. The write frequency is 6536 FCI which is identical to actual usage.
- The diskette speed is controlled to ±1% and the write oscillator to ±.01% in order to insure that the diskette is formatted as close to nominal as practical.

5.5 Environment

- storage – 50° to 125°F and 8 to 80% relative humidity
- operating – same as storage but as measured near the R/W head/media interface
- change of – should allow 1 hr. for diskette to stabilize to the new environment prior to using.

5.6 Handling

Extreme care must be exercised in handling diskettes to minimize contamination. This includes foreign matter as well as oil from fingerprints which come in contact with the media surface. The foreign matter is mostly taken care of by the diskette wiper but the "oil" is not. Thus the R/W head and load pad may collect this "oil" and excessive foreign matter and in a short time the diskette drive system will require maintenance.

6.0 WRITE PRECOMPENSATION

The purpose of write precompensation is to improve the data handling margin in the overall system. Figure 16 shows two pulses superimposed with their peaks at the nominal write spacing and their summation relating to the peak spread.

Figure 16 also shows the effective bit spread (shift) from the nominal position by 800 ns. The separator circuit see this as one pulse early by 400 ns and the other one late by 400 ns. If the separator window is 50% of these bits, then 100 ns is allowed for media, interchange, off track, speed variation, and jitter. This does not allow enough overall system margin. If the separator window is 60%, then there is 200 ns for system margin which should be the low limit.

Precompensation is accomplished by writing a bit in the opposite direction to its known shift from nominal. Previously, the bit spreading phenomenon was 800 ns. If we write the two transitions closer to one another by 200 ns each (precomp the bits by 200 ns each) there is an effective bit shift from the nominal position by 500 ns (Figure 17). The separator circuit will see this as one pulse early by 250 ns and the other late by 250 ns. If the separator window is 50% for these bits then 250 ns is allowed for system margin.

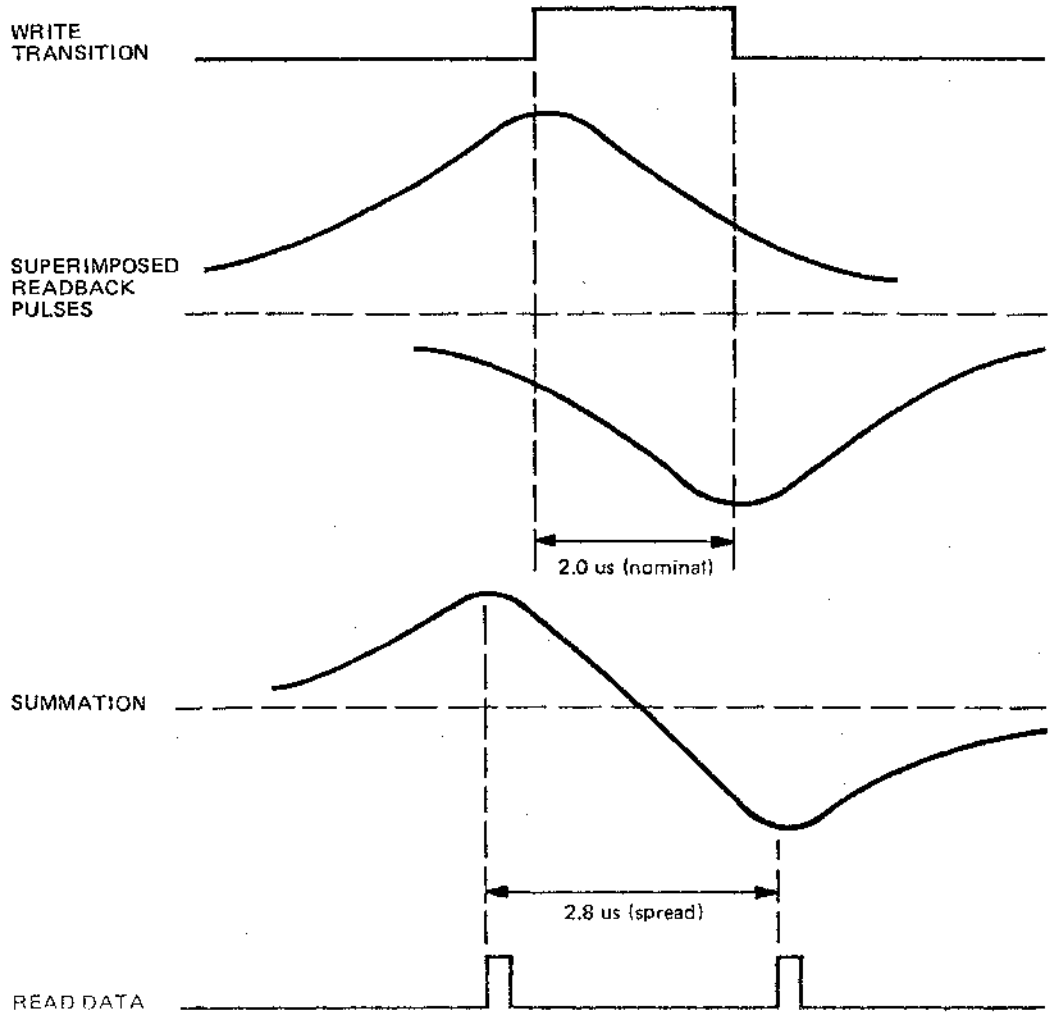


FIGURE 16 SUPERPOSITION

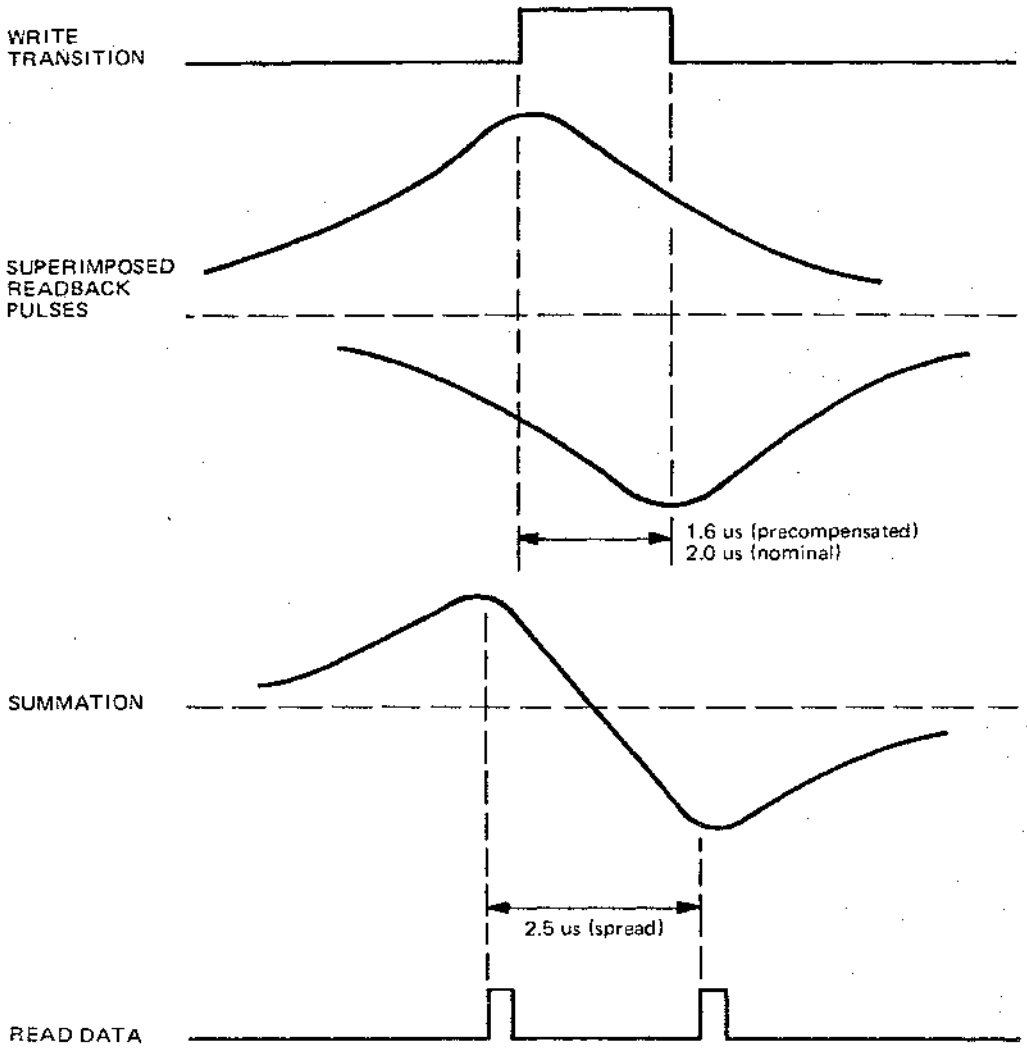


FIGURE 17 200 NS BIT PRECOMPENSATION

Table 5 is a list of data bit patterns (excluding clock bits) which shift in a similar manner. The center bit cell is the one from which write data is derived (the bit to be written) while the outer positions are used to determine the amount of bit shift to expect. This table also lists information as to what has been written.

Write Data	Degree of Shift At Inner Track	Precomp Required	Pattern
0 0 | 0 | 0 0			
0 0 | 0 | 0 1			
0 0 | 0 | 1 0			
0 0 | 0 | 1 1			
0 0 | 1 | 0 0	C	None	
0 0 | 1 | 0 1	C	None	
0 0 | 1 | 1 0	A	Maximum Late	0 1 1 0
0 0 | 1 | 1 1	B	Minimum Late	0 1 1 1
0 1 | 0 | 0 0			
0 1 | 0 | 0 1			
0 1 | 0 | 1 0			
0 1 | 0 | 1 1			
0 1 | 1 | 0 0	A	Maximum Early	0 1 1 0
0 1 | 1 | 0 1	A	Maximum Early	0 1 1 0
0 1 | 1 | 1 0	C	None	
0 1 | 1 | 1 1	C	None	
1 1 | 1 | 0 X	B	Minimum Early	1 1 1 0

A = maximum shift expected
B = approximately 1/2 of maximum shift expected
C = less than 1/4 of maximum shift expected

TABLE 5. PRECOMPENSATION PATTERNS

Table 5 indicates that there are three patterns to be precompensated. It also indicates a multilevel two level precompensation where there are two early and two late amounts of precompensation.

If Table 5 were carried out with a 1 in the first column another pattern would be picked up, 1110X, which requires minimum early precompensation. Obviously more patterns could be precompensated with a still lesser value but is impractical at this point in time.

Multilevel	Pattern	MFM	M^2FM
	0 1 1 0	max E	max E
	1 1 1 0	min E	min E
	0 1 1 0	max L	max L
	0 1 1 1	min L	min L
	1 0 0 0 1	max E	NA
	0 0 0 0 1	min E	min E (AM only)
	1 0 0 0 1	max L	NA
	1 0 0 0 0	min L	min L (AM only)
	0 0 0 0 1	none	NA
	0 0 0 1	none	min E (data field)

Single level	Pattern	MFM	M^2FM
	1 1 0	max E	max E
	0 1 1	max L	max L
	0 0 0 1	max E	NA/none
	1 0 0 0	max L	none
	0 0 0 1	none	max E

TABLE 6. SINGLE AND MULTILEVEL PRECOMPENSATION PATTERNS

All patterns not listed are written without precompensation. NA is not applicable. The address marks break the encode rules like MFM uses a M^2FM pattern and M^2FM uses a MFM pattern in the clock area. M^2FM address marks should be precompensated in multilevel.

In summary, precompensation is dependent on the encode used and whether multilevel or single level is selected. Multilevel gives better bit positioning but is more costly. Single level is a trade off on the amount of precompensation used for both the minimum and maximum patterns and is less costly. Multilevel will give better system margin when head/media resolution is poor or densities are higher.

It is obvious that the optimum and most costly would be to precompensate every track. However, to be practical the outside 40 tracks do not require precompensation while the remaining inner tracks do, unless the head/media resolution approaches 1:1. If precompensation is optimized on the inner track and then move outward until zero bit spread is reached, precompensation can then be removed for the remainder of the tracks.

With present head/media resolutions precompensation should begin at track 40. A subset of this (Figure 18) is four regions with three values of precompensation as shown by the dotted line.

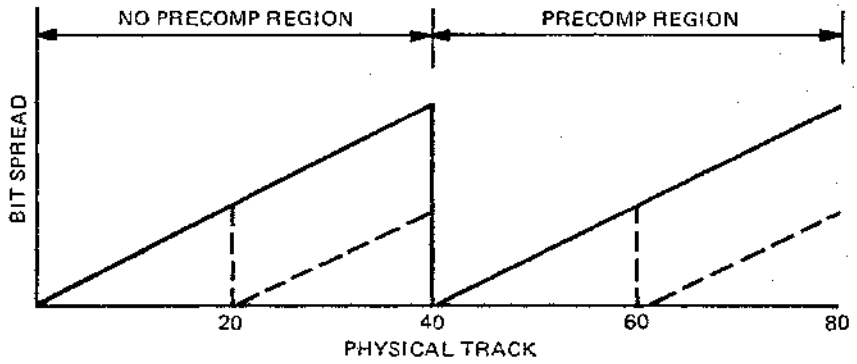


FIGURE 18 WRITE PRECOMPENSATION

Recommendations

1 – Start precompensation between track 36 and 44 depending on easiest method to obtain the decode.

2 – Use single level decode as multilevel does not enhance system margin significantly at this time.

3 – Use the following values of precompensation as applicable for MFM or M^2FM. GCR is not supported.

200-225ns for max E and max L (multi level)
100-125ns for min E and min L (multi level)
150-175ns for max E and max L (single level)

Precompensation above 225-250ns does not ensure the current in the Read/Write head has reached a static state prior to switching again. This creates further problems in that the lower frequencies have more current than the higher precompensated frequencies for media saturation and write over. This results in skew in the data separator and a lower system signal to noise ratio. Another problem is the loss of signal amplitude in the read channel which exhibits itself in the form of jitter and in turn bit shift.

7.0 Separator

The separator is generally described as circuitry that separates clock and data bits from the data stream as received from the storage device. However, the separator is actually performing three functions; namely start/stop control, separation, and interface logic to the controller (Figure 19).

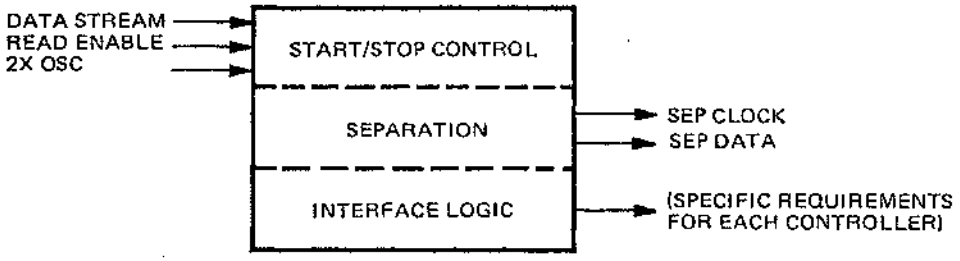


FIGURE 19 SEPARATOR FUNCTIONAL BLOCK DIAGRAM

The start/stop control logic recognizes areas within the data stream such as sync areas prior to an address mark. If the sync area were four bytes long, then the logic could count two of these bytes in sequence and them allow the separator to start. A twice the frequency (2F) area prior to the address mark gives twice the bits per byte to permit the separator to synchronize more rapidly with the data stream. Once count two is reached, an address mark is expected within the next three bytes. If it is not detected within four bytes a reset pulse should occur from the controller to reset the logic and start again (Read Enable can perform this from the controller. (Figure 20.)

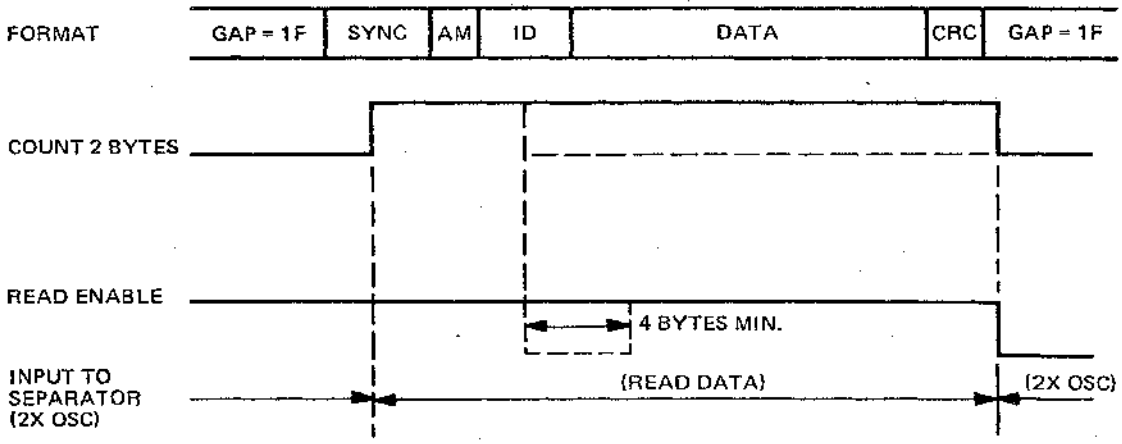


FIGURE 20 ADDRESS MARK DETECTION TIMING DIAGRAM

Separation includes the phase locked loop, window generator, window extender, data stream adjust, and the clock/data separation logic.

The phase locked loop performs the initial start synchronization as well as averaging the effects of speed variation and bit shift.

The window generator divides the bit cell into a clock and a data window.

This division of the bit cell may be 50% for clock and 50% for data or any other division like 60% for data and 40% for clock. The actual division is dependent on the encode, write channel symmetry, read/write head, media, read channel symmetry and separator response.

The window extender insures that the leading edge of any clock or data bit once detected, cannot fall into another window. The data bit width also becomes independent of system margin as only the leading edge is significant (Figure 21).

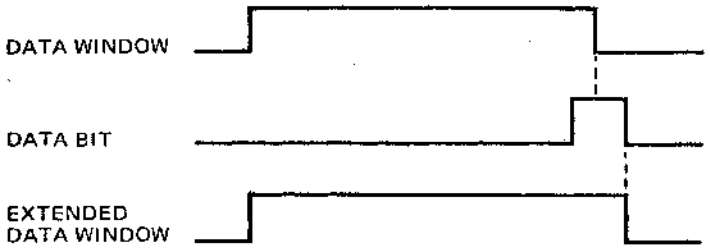


FIGURE 21 WINDOW EXTENDER

Data stream adjust allows adjustment of the leading edge of the data stream bits to the center of the window. This is generally required because of the inherent circuit delays between the data stream and the window generator (Figure 22).

FIGURE 22 DATA STREAM ADJUST

Clock/Data separation logic provides two single lines, sep clock and sep data, to the controller.

The controller, whether it is a discreet type or microprocessor, must be fully understood with respect to its gating and clocking limits. It does absolutely no good to have a reliable Separator and then not be able to get a bit into the controller.

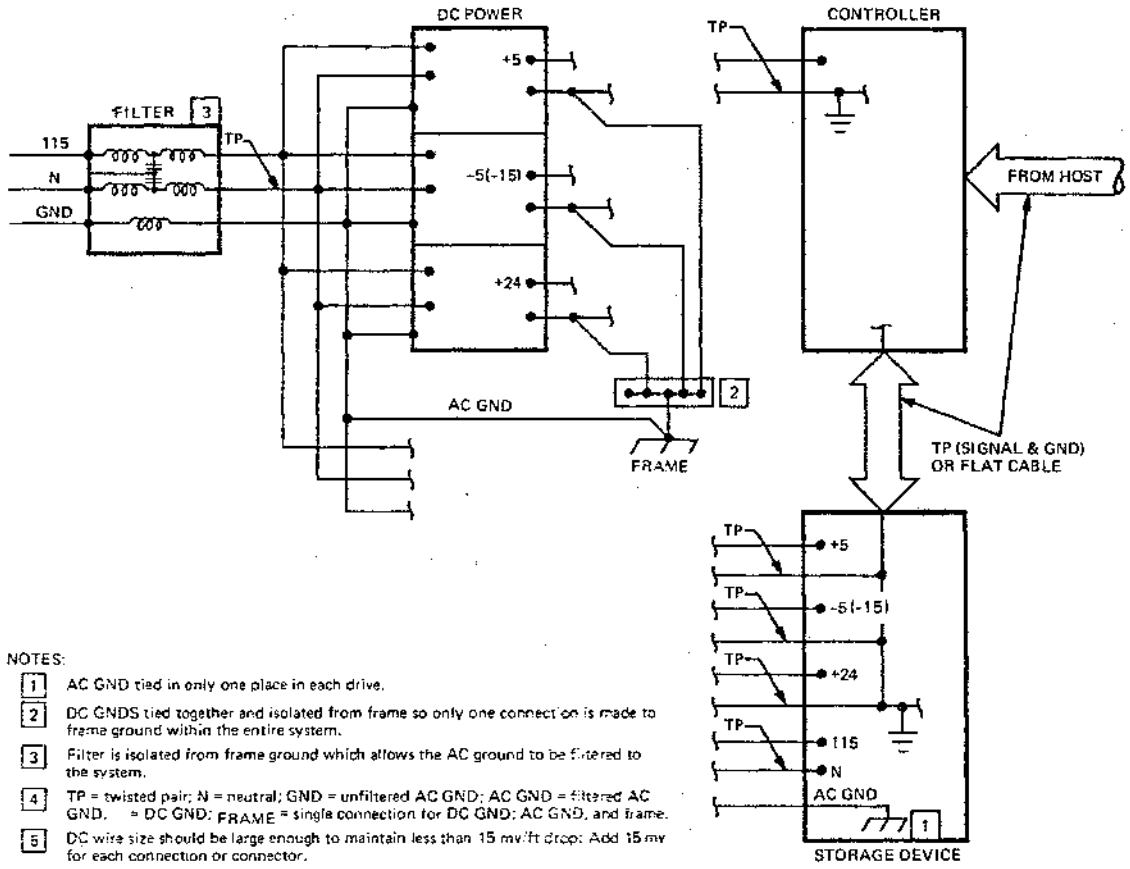
With respect to the various discreet controllers, it becomes the designer's responsibility to insure that the separated bits near either edge of the Separator window are always clocked into the controller. The inherent problem is the failure to clock into the controller a bit late in the Separator window.

	FM	MFM	M^2FM	GCR
60% clock window	±1200ns	NA	NA	NA
40% clock window	NA	NA	±400	NA
50% clock & data window	±1000ns	±500ns	±500	NA
60% data window	NA	NA	±600ns	NA
100% data window	NA	NA	NA	±800

TABLE 7. SEPARATOR TOLERANCES

8.0 POWER AND GROUND DISTRIBUTION

Power requirements are critical in overall system margin and therefore special consideration should be given by the system designer in selection of adequate power supplies. Figure 23 is provided to insure proper power and ground distribution.



NOTES:

1. AC GND tied in only one place in each drive.
2. DC GNDS tied together and isolated from frame so only one connection is made to frame ground within the entire system.
3. Filter is isolated from frame ground which allows the AC ground to be filtered to the system.
4. TP = twisted pair; N = neutral; GND = unfiltered AC GND; AC GND = filtered AC GND. = DC GND; FRAME = single connection for DC GND; AC GND, and frame.
5. DC wire size should be large enough to maintain less than 15 mv/ft drop; Add 15 mv for each connection or connector.

FIGURE 23 POWER AND GROUND DISTRIBUTION

9.0 SYSTEM EVALUATION

9.1 General

This section provides the system designer with a check list to evaluate overall system performance.

9.2 Voltage Margins

Insure DC voltage drop in cabling and connectors do not exceed 10-15 mv/ft. Vary each DC supply independently to its limits and then all supplies high with one at a time to the low limit to insure system operation.

9.3 Seek Operation

Verify seek interface timing.

9.4 Write Operation

Verify Encoder and Precompensation timing including Address Marks.

9.5 Read Margins

Use any of the following methods to determine system margin with a worst case bit shifted data pattern on the inner track:

- reduce Separator window size to failure point. These limits also provide the optimum window size.
- move data in Separator window to failure point.
- remove or reduce precompensation to failure point.
- without the window extender, widen the data pulse to failure point. Note that the center of the pulse must be centered in the window.

When the failure point is reached it must be determined if it occurred in the Separator or the "clocking" into the Controller. The "clocking" into the Controller is oftentimes where most system margin is lost.

9.6 Interchange

Use three drives (A, B and C) aligned to two opposite limits and one at nominal. Select three diskettes as recommended by the manufacturer and perform the following matrix:

	A	B	C
format and verify	1	2	3
read"n"passes	3	1	2
read"n"passes	2	3	1

Repeat for update write and read operation.