

SA4000 Fixed Disk Drive

OEM Manual

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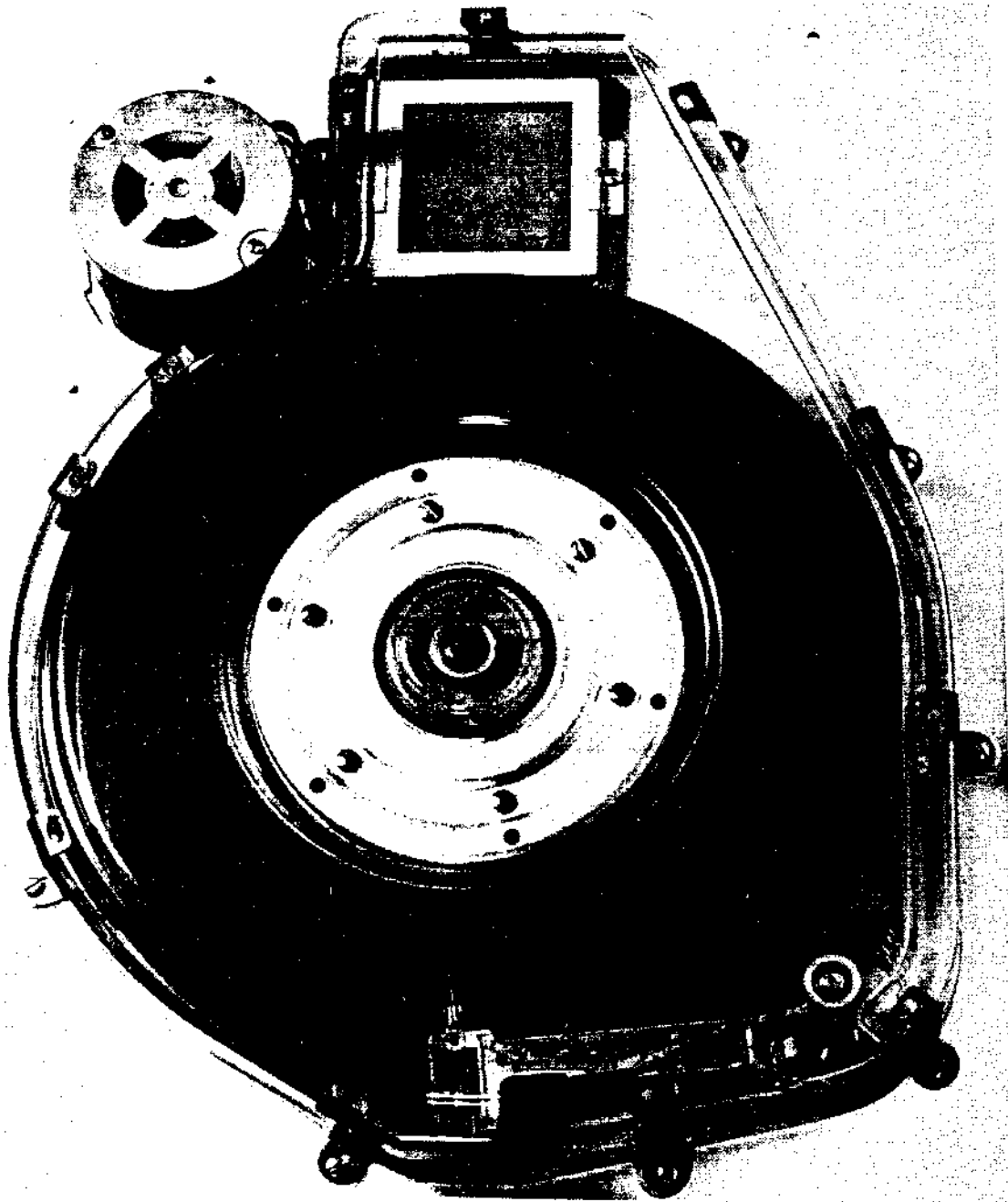


Figure 1. SA4000

1.0 INTRODUCTION

1.1 General Description

The Shugart Series SA 4000 Disk Drive is a random access storage device with one or two fixed (non-removable) fourteen inch disk(s) as the storage media. A positioning mechanism positions the Read/Write heads onto 202 discrete positions (cylinders). The SA 4004 version contains a single disk with four Read/Write heads (two per surface). In this configuration each cylinder then contains four data tracks.

The SA 4008 version contains two disks with eight Read/Write heads (two per surface). In this configuration each cylinder then contains eight data tracks. An option is available which provides eight fixed heads (one per track) to be selected, providing 144 Kbytes of fast access storage (18 Kbytes per track). Up to four SA 4000 drives may be daisy chain connected in one system.

Low cost and reliability of the unit is achieved with a unique actuator design. The inherent simplicity of mechanical construction and electronic controls of the assembly allows maintenance free operation for the life of the drive.

Mechanical and contamination protection for the head, actuator, and disk is provided by an impact-resistant plastic enclosure. A self-contained recirculating system supplies clean air through an absolute filter. The filters are designed to last through the life of the drive.

A single track of clock information is written on the disk and read by a single fixed head. These clock pulses are used to synchronize the Phase Locked Oscillator (PLO) in the data separation circuitry and provide Index, Sector and Write Clocking information from the disk. A jumper programmable counter is provided that converts the clock pulse into virtually any number of sectors per track.

A data separator PCB is mounted in the drive enclosure. In addition to VFO separation of MFM Read Data, this PCB MFM encodes and write pre-compensates standardized Write Data.

The drive can be mounted in any 19 inch rack. It occupies 5.25 inches of vertical space and is 22 inches long.

1.2 Specifications Summary

1.2.1 Performance and Functional Specifications

MODEL	4004	4008
No. of Disk Surfaces	2	4
No. of Heads	4	8
No. of Cylinders	202	202
No. of Tracks	808	1616
Gross Capacity (M bytes)	14.54	29.08
Access Time including seek settle of 20 ms (Milliseconds)		
One Track	20	20
Average (67 Track Seek)	65	65
Maximum (201 Track Seek)	140	140
Disk Speed	2964 RPM	
Recording Mode	MFM	
Recording Density	5534 BPI	
Flux Density	5534 FCI	
Track Capacity	18000 Bytes	
Track Density	172 TPI	
Transfer Rate	7.11 x 10 ⁶ bits/sec. 889 x 10 ³ bytes/sec.	
Sectors	Programmable	
Start Time	1.5 minutes (See section 3.1)	

1.2.2 Physical Specifications

Environmental Requirements

	Operating	Shipping	Storage
Temperature (host ambient) – F	50 to 105	-40 to 144	-8 to 117
Relative humidity – %	(10 to 41°C) 8 to 80	(-40 to 62°C) 1 to 95	(-22 to 47°C) 1 to 95
Maximum wet bulb	78°F non-condensing		

Maximum Operating Altitude 6000 Ft. (1830 meters) ASL

Maximum Non Operating Altitude 12000 Ft. (3660 meters) ASL.

AC Power Requirements

50/60 Hz ± 0.5 Hz

100/115 VAC Installations = 90 to 127 V @ 3.0A maximum

200/230 VAC Installations = 180 to 253 V @ 1.5A maximum

DC Voltage Requirements

+24 V ± 10% @ 3A maximum

+5V ± 5% @ 3A maximum

-7 to -16 V @ 0.15A maximum (option -5 V ± 5% @ 0.10A maximum)

Physical Dimensions

Height 5.22 inches maximum (132.6 mm)

Width 16.60 inches maximum (421.6 mm)

Depth 21.9 inches maximum (556.3 mm)

Weight 35 pounds (15.9 kg)

Heat dissipation 682 BTU/Hr. typical (200 Watts)

1.2.3 Reliability Specifications

MTBF: 8000 power on hours

MTTR: 30 minutes

Component life: 5 years normal usage

Acoustic noise level: less than NR 55

Error Rates:

Soft read errors: 1 per 10¹⁰ bits read

Hard read errors: 1 per 10¹² bits read

Seek errors: 1 per 10⁶ seeks

Preventive Maintenance: none required

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA4000 Fixed Disk Drive consists of read/write and control electronics, VFO data separator, MFM encode/decode electronics, read/write heads, track positioning mechanism, drive mechanism, disk(s), and air filtrations system. These components perform the following functions:

- Interpret and generate control signals
- Move read/write head to the selected track
- Read and write data

2.2 Read/Write and Control Electronics

The electronics are packaged on four printed circuit boards:

Read/Write PCB

1. Read Amplifier and Transition Detector
2. Read/Write Head Selection Circuit
3. Write Driver
4. Clock Track Amplifier

Actuator Drive PCB

1. Step Buffer
2. Head Position Actuator Driver
3. Track 00 Detector Amplifier
4. Voltage Regulation

Control PCB

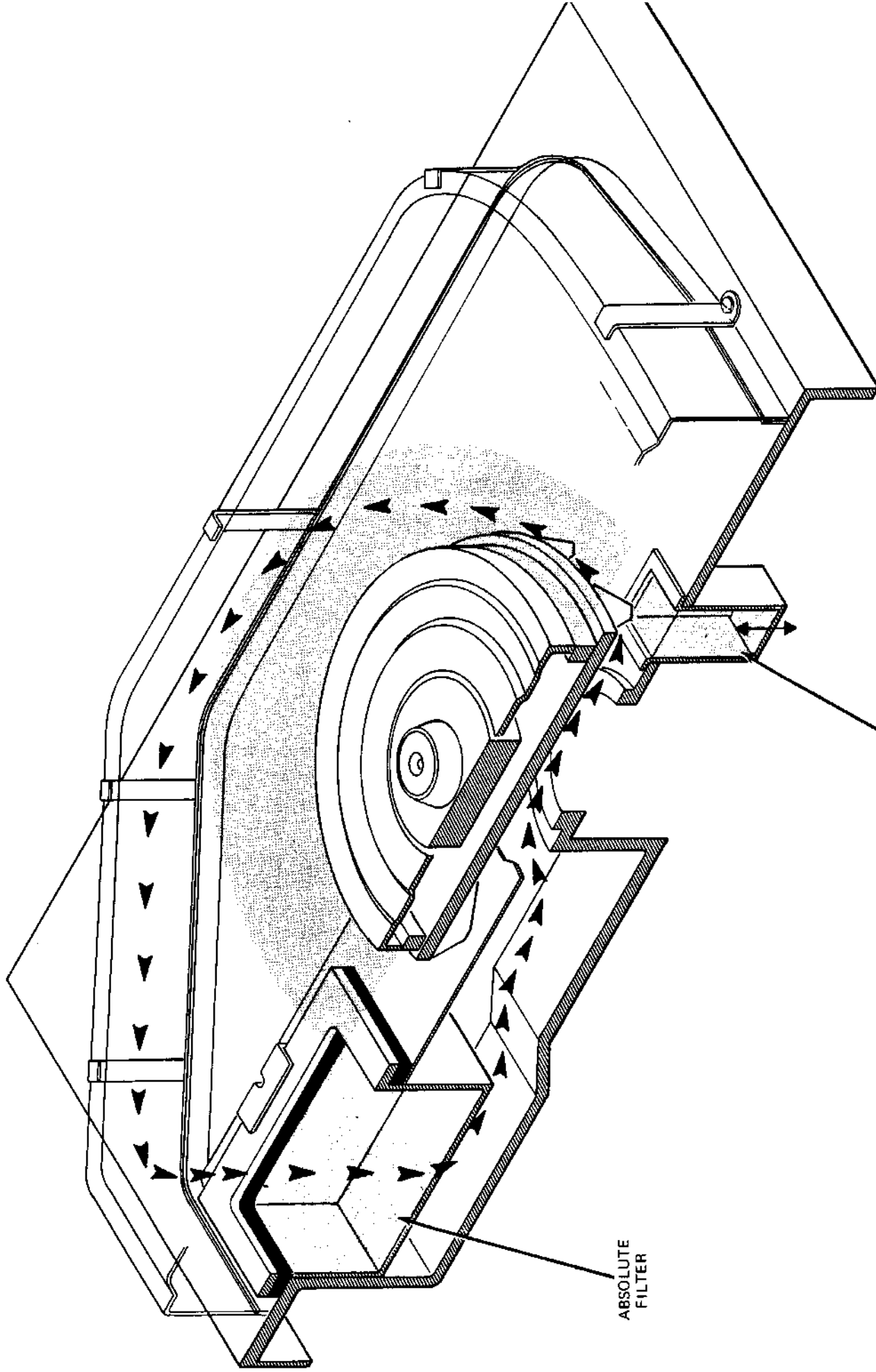
1. Interface Drivers/Receivers
2. Drive Select Circuits
3. Write Fault Detection Circuits
4. Byte (sector optional) Clock Generation Circuit
5. Drive Ready Timer Circuit
6. PLO Clock Generator Circuit

Data Separator PCB

1. Data Separator
2. MFM Encode/Decode Circuit

2.3 Air Filtration System (Figure 2)

The disk(s) and read/write heads are fully enclosed in a module using an integral recirculation air system with an absolute filter which maintains a clean environment. A separate absolute breather filter permits pressure equalization with the ambient air without contamination.



ABSOLUTE
FILTER

ABSOLUTE FILTER FOR
PRESSURE COMPENSATION

Figure 2. Air Filtration System

2.4 Positioning Mechanism (Figure 3)

The read/write heads are mounted on an arm which is positioned by the Fasflex II™ actuator. A stepping motor is used to precisely position the head/arm assembly through the use of a unique metal band/capstan concept.

2.5 Read/Write Heads and Disk (Figure 4)

The recording media consists of a lubricated magnetic oxide coating on an aluminum substrate. This coating formulation, together with the low load force/low mass Winchester type flying heads, permits reliable contact start/stop operation.

Data on each disk surface is read by two read/write heads, each of which accesses 202 tracks. The drive is available in two basic configurations: one disk with four read/write heads, or two disks with eight read/write heads.

A separate read head mounted to the base casting reads a prerecorded track which provides the master clock for the drive as well as the clock for write clock generation.

The optional fixed heads are mounted on an assembly which is mounted directly on the base casting.

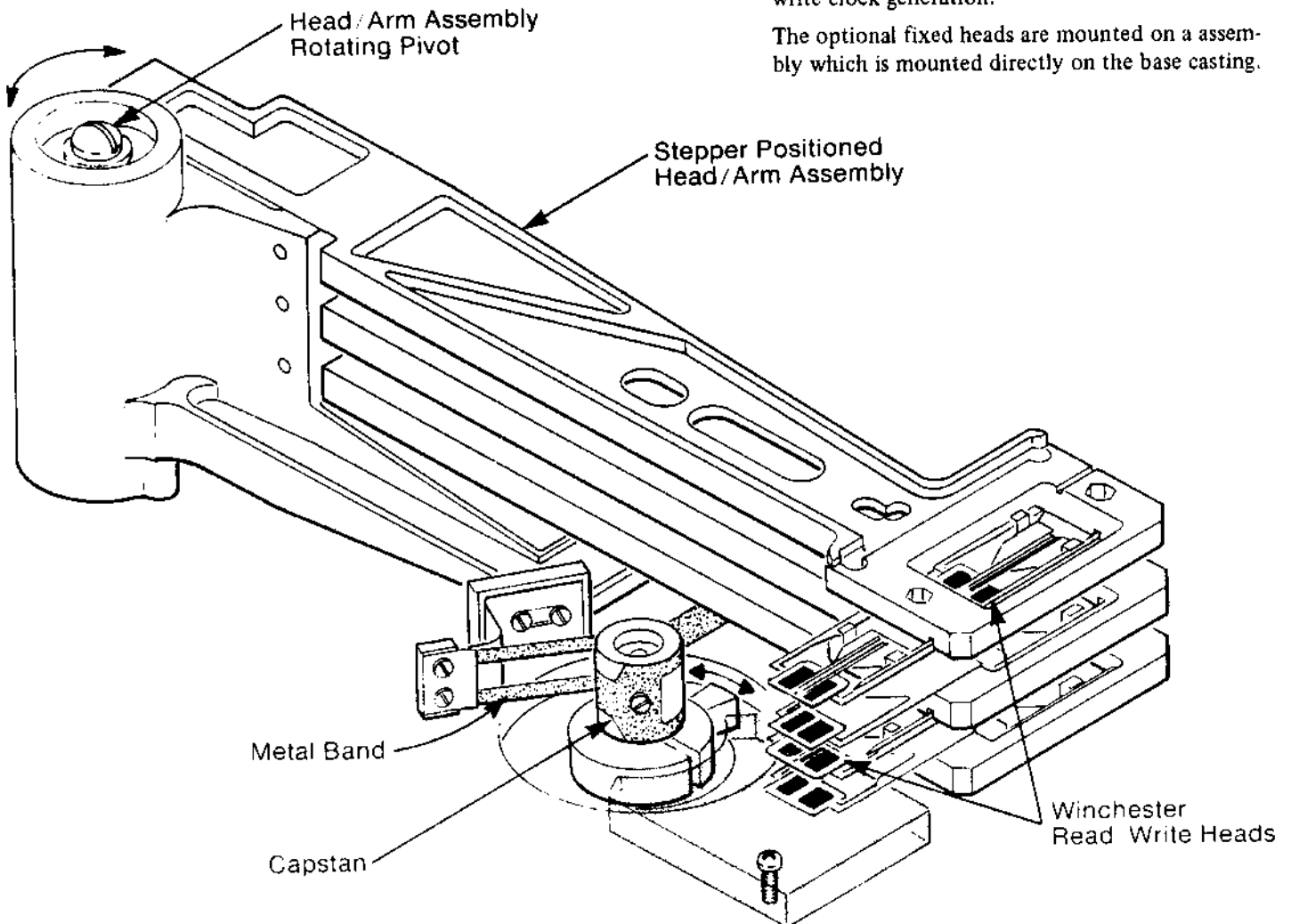


Figure 3. Read/Write Heads

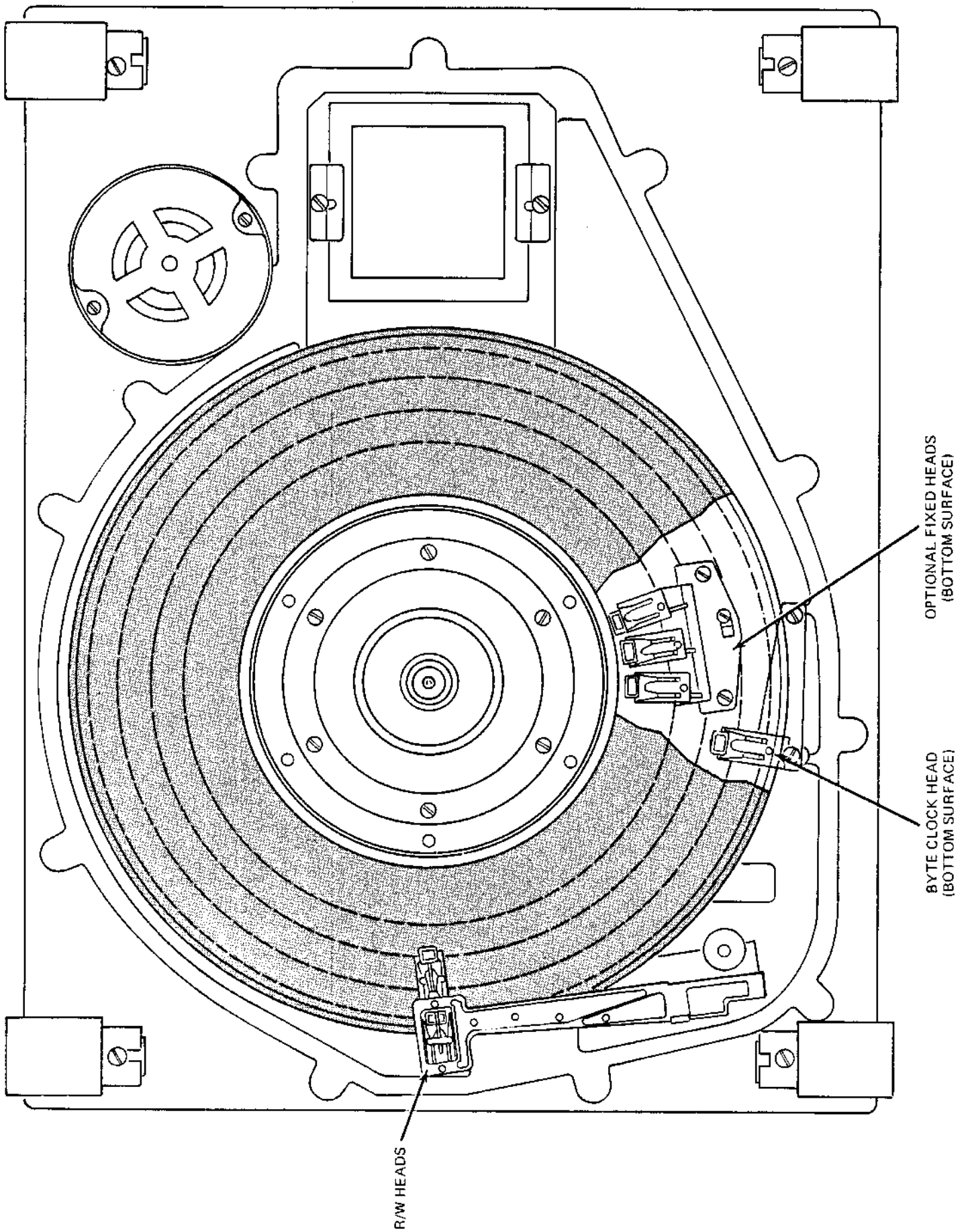


Figure 4. SA4000 Head Locations

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

Applying AC and DC power to the SA4000 can be done in any sequence, however, once power has been applied, the ready line must be active prior to any read, write, or seek operation. After application of DC power, a 1.25 minute internally generated delay to ready is introduced. If AC and DC power are applied simultaneously, the delay to ready will be approximately 1.5 minutes. The delay is necessary to allow thermal warmup and disk rotational stability. After power on, the initial position of the read/write heads is indeterminate. In order to assure proper positioning of the read/write heads after power on, a step out operation should be performed until the track 00 line becomes active (see section 4.1.1.2).

CAUTION: If the "T" jumper is removed (see Section 7.4), AC power must be applied 2 seconds (min) prior to applying DC power. This is done to insure that if the read/write heads move as a result of applying DC power, the disk(s) will be rotating above the minimum velocity to avoid possible disk/head damage.

3.2 Drive Selection

Drive selection occurs when a drive's Drive Select line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the Drive Select line will apply power to the stepper motor, enable the input lines and activate the output lines.

3.3 Track Accessing

Seeking from one track to another is accomplished by:

- a. Activating Drive Select line.
- b. Selecting desired direction utilizing Direction Select line.
- c. Write Gate being inactive.
- d. Pulsing the Step line.

Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached or by using the buffered step modes. Each pulse on the Step line will cause the R/W heads to move one track either in or out depending on the Direction Select line. Head movement is initiated on the trailing edge of the Step Pulse. See Section 4.1.1.3 for detailed description.

3.4 Read Operation

Reading data from the SA4000 Disk Storage drive is accomplished by:

- a. Activating Drive Select line.
- b. Selecting head.
- c. Write Gate being inactive.
- d. Read Gate being active.

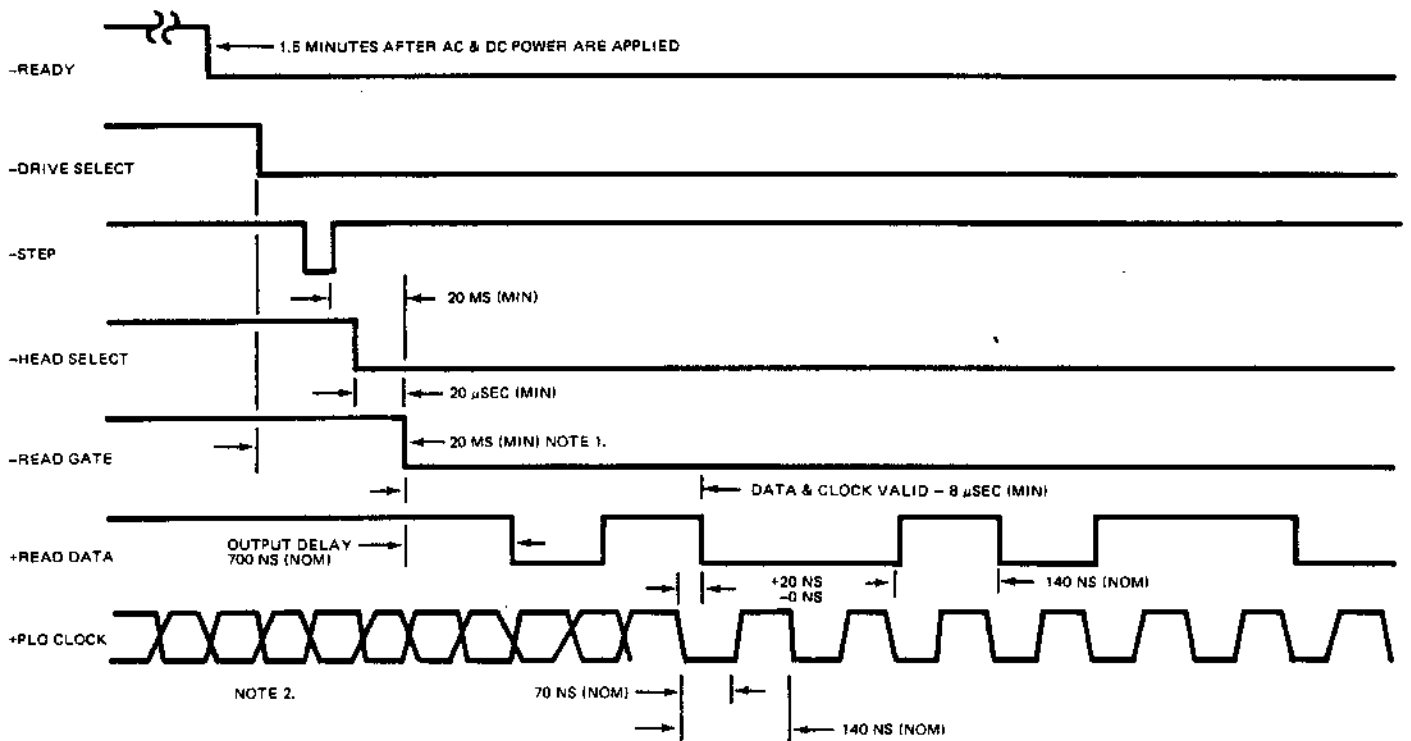
The timing relationships required to initiate a read sequence are shown in Figure 5. These timing specifications are required in order to guarantee that the R/W heads position has stabilized prior to reading.

3.5 Write Operation

Writing data to the SA4000 is accomplished by:

- a. Activating the Drive Select line.
- b. Selecting head.
- c. Activating the Write Gate line.
- d. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W heads position has stabilized prior to writing.



NOTES:

1. IF STEPPER POWER IS ENABLED CONTINUOUSLY (D JUMPER OPEN), THIS TIME = 500 NS (MIN).
2. WHEN THE READ GATE IS INACTIVE - PLO CLOCK IS LOCKED TO CLOCK TRACK (USED BY CONTROLLER TO GENERATE WRITE CLOCK).

Figure 5. Read Initiate Timing.

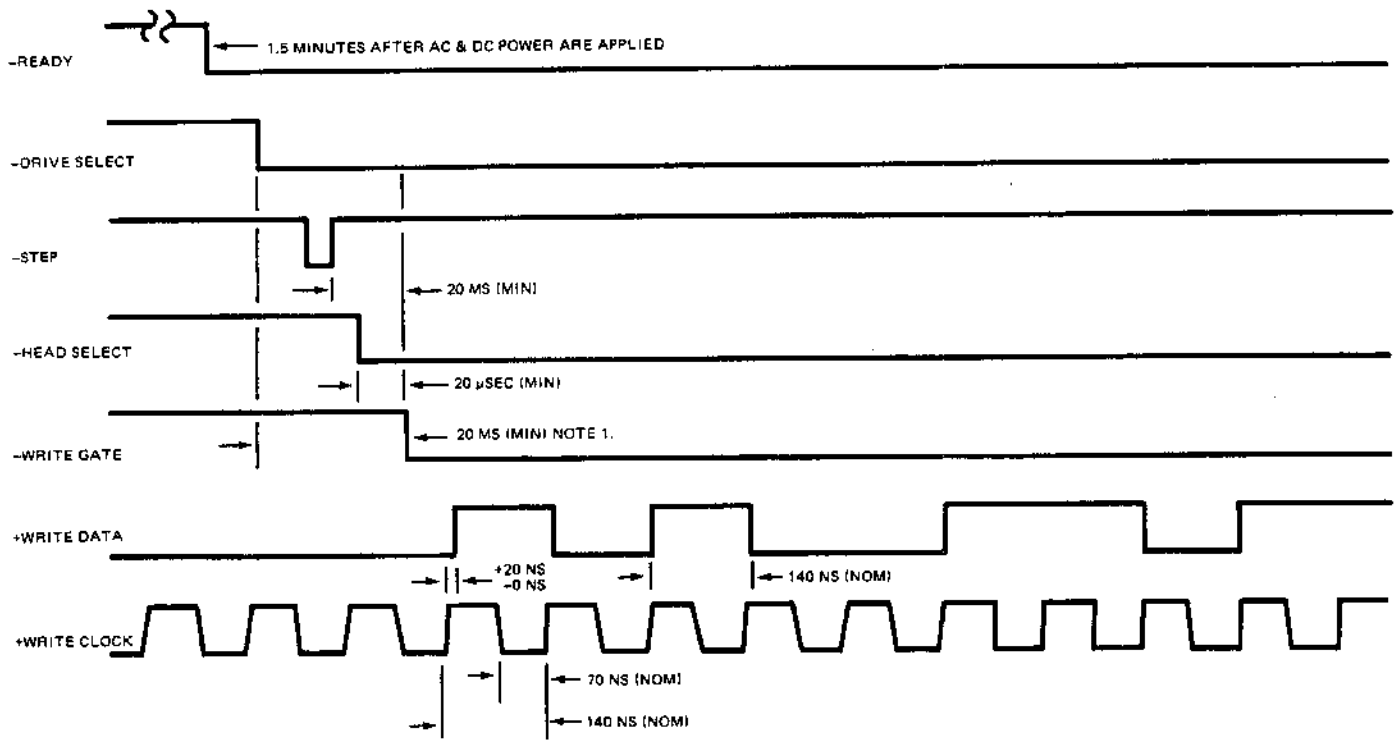


Figure 6. Write Initiate Timing

4.0 ELECTRICAL INTERFACE

The interface of the SA4000 drive can be divided into three categories:

1. Signal
2. DC Power
3. AC Power

The following sections provide the electrical definition for each line.

4.1 Signal Interface

The signal interface consists of three categories:

1. Control Input Lines
2. Control Output Lines
3. Data Transfer Lines

All control lines are digital in nature and either provide signals to the drive (input) or provide signals to the host (output) via the interface connector J1/P1. The data transfer signals are differential in nature; they provide data and clocking, either to or from the drive, via J1/P1 or J2/P2 when the optional daisy chain interface is used.

4.1.1 Control Input Lines

The control input signals are of two types: Those intended to be multiplexed in a multiple drive system and those intended to control the multiplexing. The control input signals to be multiplexed are STEP, DIRECTION, HEAD SELECT 1, 2, 4, & 8, FAULT CLEAR, WRITE GATE and READ GATE. The signals which are intended to do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to Figure 11 for the recommended circuit.

True = 0.0 V DC to 0.4 V DC @ $I_{in} = 40 \text{ MA}$ (Max)
False = 2.5 V DC to 5.25 V DC @ $I_{in} = 0 \text{ MA}$ (Open)

4.1.1.1 Drive Select 1-4

DRIVE SELECT when true, logically connects the drive to the control lines. Only one DRIVE SELECT line may be active at a time and will allow the drive to respond to input signals and gate outputs.

Trace options DS1, DS2, DS3, & DS4 are used to select which drive select input line will activate the interface for a unique drive. Drive select 4 can be configured as SEEK COMPLETE on a single drive system.

Interface signals are valid 500 nanoseconds (max) after drive select.

4.1.1.2 Direction Select

This signal defines direction of motion of the read/write head when the STEP line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the STEP line, the read/write head will move away from the center of the disk.

Conversely, if this input has a logical zero level applied, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the read/write head moves toward the center of the disk. A 220/330Ω resistor network provides line termination.

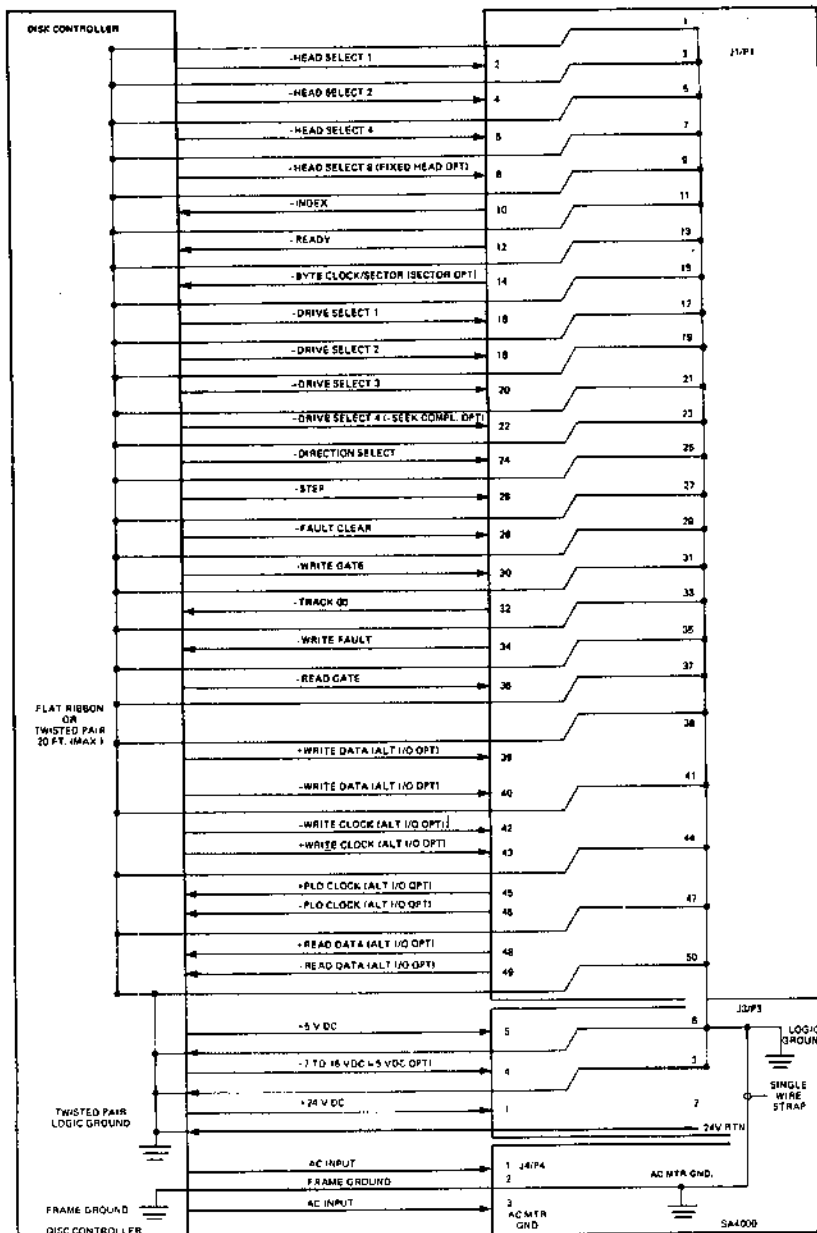


Figure 7. Interface Connection (J1 Connector)

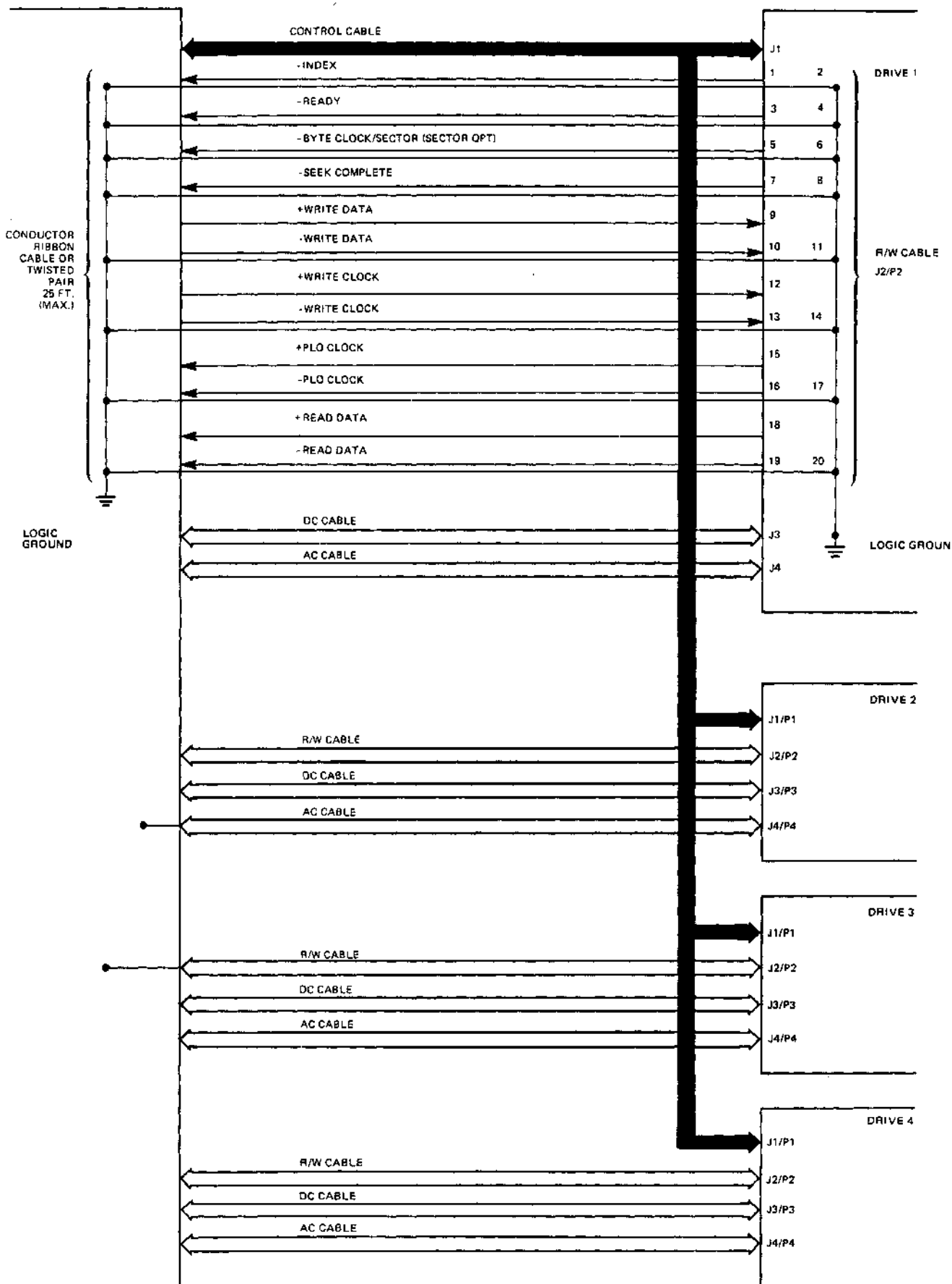


Figure 8. Interface Connection Multiple Drive System (J2 Connector)

4.1.1.3 Step

This line causes the read/write head to move with the direction of motion defined by the Direction Select Line.

The access motion is initiated at each logical zero to logical one transition or the trailing edge of this signal pulse. Any change in the Direction Select Line must be made at least 200 ns before the trailing edge of the step pulse.

There are two modes of operation for stepping the read/write head, the normal mode and the buffered mode.

When the seek complete line becomes active after a step, a 20 millisecond delay must be initiated to allow the positioning mechanism to settle prior to any Read/Write operation.

A 200/330 Ω resistor pack allows line termination.

4.1.1.3.1 Normal Step Mode

In this mode of operation the read/write head will move at the rate of the incoming step pulses. The minimum time between successive steps is 1 ms. The maximum pulse width is 10 μ s and the minimum is 1 μ s. See Figure 9 for normal step mode timing.

4.1.1.3.2 Buffered Step Mode

In this mode of operation the step pulses are received at a high rate and buffered into a counter. After the last pulse the read/write head will then begin stepping the appropriate number of cylinders and Seek Complete will go true after the read/write head arrives at the cylinder.

Once the step pulses have been sent to the drive, the Drive Select Line may be dropped and a different drive selected. See Figure 10 for buffered step mode timing.

4.1.1.3.3 Calculating Access Times

Access times in the buffered seek mode can be calculated by realizing that the head positioning mechanism is accelerated to a nominal step rate during the first 16 steps of a seek. The positioning mechanism is then decelerated at the same rate during the last 16 steps. If a seek involves less than 32 cylinders, only the appropriate portion of the acceleration/deceleration curve is utilized. The drive is initially stepped at a 1.05 millisecond rate and accelerated to 0.552 milliseconds per step. The following table shows the step values used during acceleration/deceleration.

Table 1. Acceleration/De-Acceleration Curve

<u>Step #</u>	<u>Step Time (μsec)</u>
1	984
2	1050
3	884
4	812
5	755
6	708
7	671
8	641
9	617
10	598
11	583
12	572
13	564
14	558
15	554
16	552

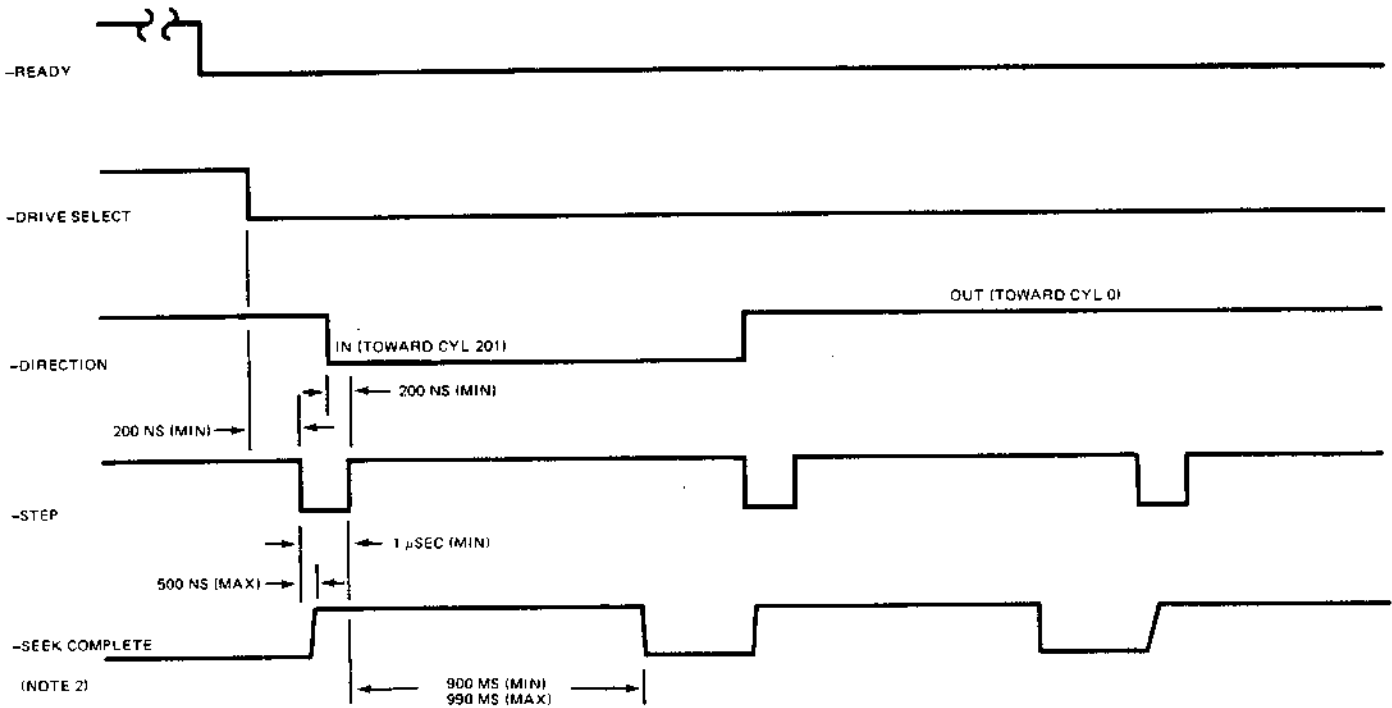


Figure 9. Normal Step Mode Timing

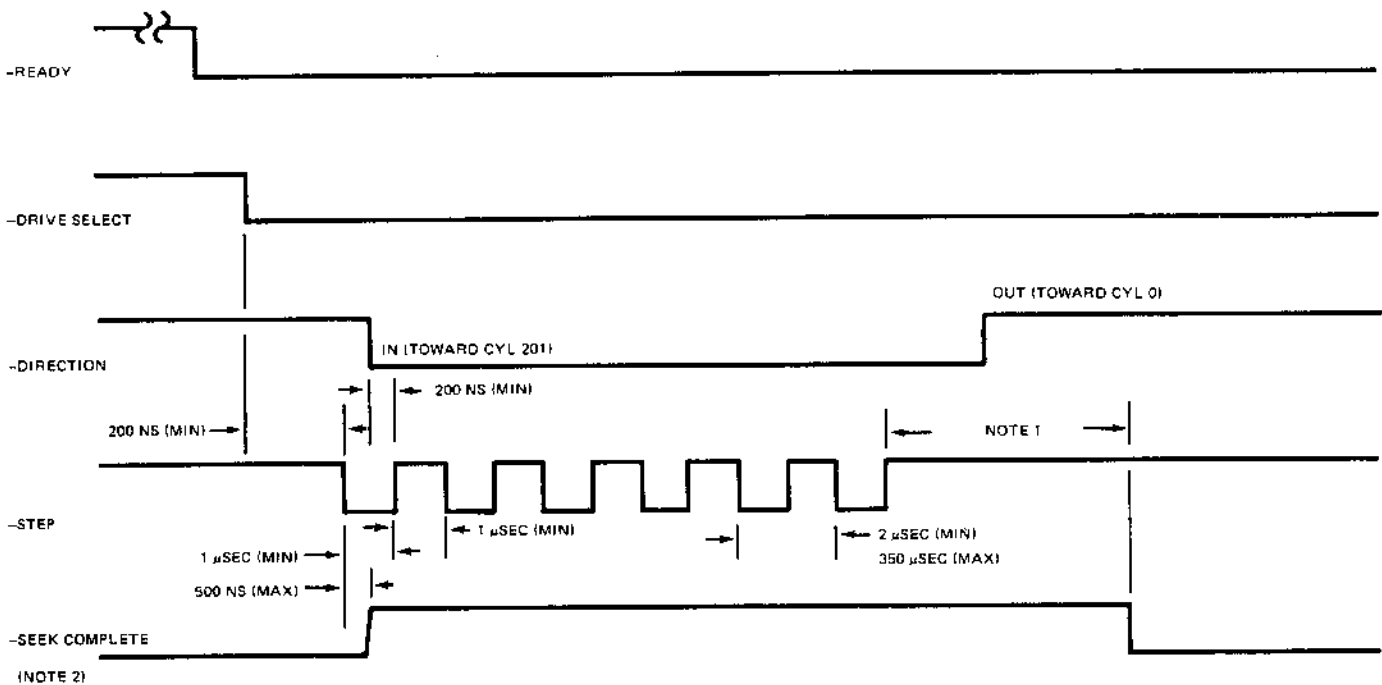


Figure 10. Buffered Step Mode Timing

NOTES:

- SEEK COMPLETE WILL OCCUR 1 MILLISECOND AFTER LAST STEP HAS OCCURRED.
- A 20 MILLISECOND DELAY SHOULD BE INITIATED FOLLOWING SEEK COMPLETE BEFORE ANY READ/WRITE OPERATIONS MAY BE PERFORMED.

4.1.1.4 Head Select 1, 2, 4, & 8

These four lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 1 is the least significant line. Heads are numbered 0 through 15 with the last 8 heads being the optional fixed heads. When all HEAD SELECT lines are false, head 0 will be selected. Table 2 shows the HEAD SELECT sequence and model variations for the HEAD SELECT LINES.

A 200/330 Ω resistor pack allows for termination on each line.

Table 2. Head Select

HEAD SELECT LINES				HEAD # SELECTED	HEAD # SELECTED
8	4	2	1	SA4004	SA4008
H	H	H	H	0	0
H	H	H	L	1	1
H	H	L	H	2	2
H	H	L	L	3	3
H	L	H	H	—	4
H	L	H	L	—	5
H	L	L	H	—	6
H	L	L	L	—	7
L	H	H	H	8	8
L	H	H	L	9	9
L	H	L	H	10	10
L	H	L	L	11	11
L	L	H	H	12	12
L	L	H	L	13	13
L	L	L	H	14	14
L	L	L	L	15	15

Heads 8 through 15 are the optional fixed heads

4.1.1.5 Fault Clear

FAULT CLEAR is used to reset the WRITE FAULT condition if it occurs at the drive. This line disables writing at the drive while it is active and therefore may be used in a write protect function. WRITE FAULT is reset on the leading edge of the FAULT CLEAR pulse. A minimum 100 ns pulse is required on this line to reset a fault.

4.1.1.6 Write Gate

The active state of this signal, or logical zero level, enables write data to be written on the disk. The inactive state of this signal, or logical one level, enables data to be transferred from the drive. Also, the inactive state of this signal enables the STEP pulses to step the read/write actuator. Refer to Figure 6 for timing considerations.

A 220/330 Ω resistor pack allows for line termination.

4.1.1.7 Read Gate

This line is used to control the data separator in the drive. This line must go active in a known area of all zeroes or all ones 8 μ s or more before the sync byte. After the first 8 μ s that READ GATE is active, the PLO CLOCK and the READ DATA (NRZ) will be synchronized such that the positive transition of PLO CLOCK may be used to clock the read data line into the host controller. When READ GATE is inactive, the READ DATA will be inactive. However, the PLO CLOCK will continue to run at the nominal bit rate. Refer to Figure 5 for the timing considerations.

A 220/330 Ω resistor pack allows for line termination.

4.1.2 Control Output Lines

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at logical zero or true state with maximum voltage of 0.4 V measured at the driver. When the line driver is in logical one or false state, the driver transistor is off and the collector cutoff current is a maximum of 250 microamperes.

All J1 output lines are enabled by the DRIVE SELECT line.

Figure 11 shows the recommended control signal driver/receiver combination.

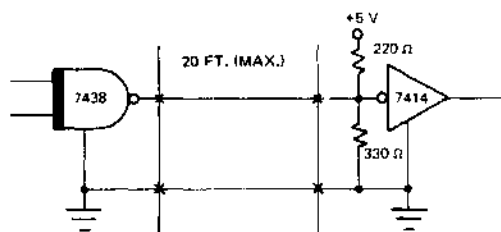


Figure 11. Control Signal Driver/Receiver Combination

4.1.2.1 Track 00

This interface signal indicates a true state only when the drive's read/write arm is positioned at TRACK ZERO (the outermost data track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at logical one level, or false state, when the selected drive's read/write arm is not at TRACK ZERO.

4.1.2.2 Index

This interface signal is provided by the drive once each revolution (20.24 ms) to indicate the beginning of the track. Normally, this signal is a logical one level and makes the transition to the logical zero level for a period of approximately 1.1 μ s once each revolution. The timing of this signal is shown in Figure 12.

4.1.2.3 Ready

This interface signal indicates that the drive is ready to read, write, or seek and that the BYTE CLOCK (sector, when option jumpered), INDEX and PLO CLOCK signals are valid. When this line is false, all writing on the disk and seeking is inhibited at the drive.

READY will be true after the drive is up to speed, the temperature has stabilized, and the PLO is "locked" to the speed of the disk.

The nominal time for READY to become true after power on is 1.5 minutes.

4.1.2.4 Write Fault

This signal is provided by the drive and is used to indicate that a condition existed at the drive that caused improper writing on the disk. When this line goes true, further writing is inhibited at the drive until the condition is reset by FAULT CLEAR. If a FAULT CLEAR signal goes true without a fault condition, WRITE FAULT will go true, thus inhibiting a write operation until FAULT CLEAR becomes false.

The following are the WRITE FAULT conditions:

1. WRITE GATE true without WRITE CURRENT in the selected head or WRITE CURRENT in the selected head without WRITE GATE active.
2. Multiple HEADS selected (Drive Defect).
3. WRITE GATE active when READY is false.
4. WRITE GATE and READ GATE active simultaneously.

4.1.2.5 Seek Complete

This line will go true immediately after the read/write head arrives on track but before the head has settled. Therefore the user should wait 20 ms before attempting to read or write. See Figure 9. Seek Complete is enabled by Ready, internal to the drive, and is available on the J2 interface connector, and on the J1 connector as a jumper option. See Section 7.4.

4.1.2.6 Byte Clock

This signal is a nominal square wave with a period equal to 1.1 μs. There are exactly 18,000 cycles per revolution on this line. This condition only holds true when READY, internal to the drive, is true. See Figure 13 for timing tolerances.

4.1.2.7 Sector Synthesizer (Jumper Option)

When the optional SECTOR SYNTHESIZER (Jumper SC) is jumpered the byte clock line will transmit sector marks to the host system. The sector marks are 1.1 μs in duration. The number of sector marks per revolution is programmable via jumpers in the drive. Figure 14 shows a method for computing sector length. Index will fall coincident with sector. The sector pulse at index time may be removed via a jumper option. (See Section 7.4).

4.1.3 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. For single drive systems J1/P1 is used to carry data. J2/P2 connector provides for radial attachment of up to four drives.

Four signals are used for data transfer in a standard drive, WRITE DATA, READ DATA, PLO CLOCK, and WRITE CLOCK. The WRITE DATA/READ DATA lines are non-return to zero (NRZ) format. Figure 15 illustrates the driver/receiver combination used in the SA4000 drive for DATA TRANSFER signals.

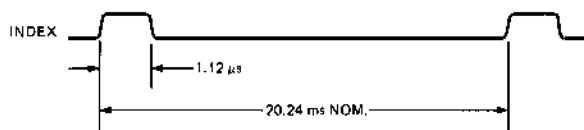


Figure 12. Index Timing

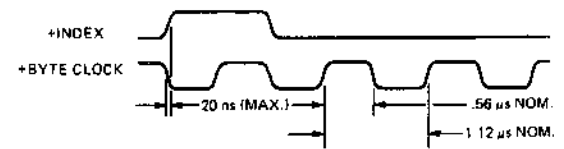
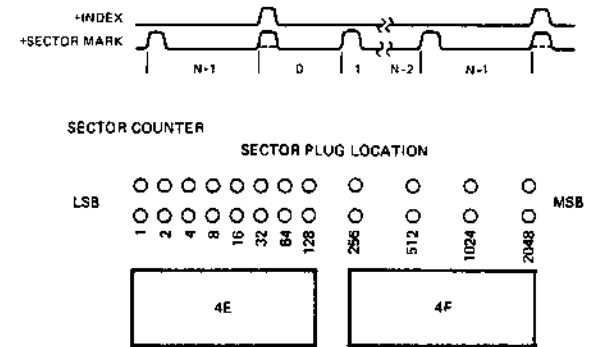


Figure 13. Byte Clock Timing



Formula for computing sector length versus the number of sectors: $X = \left(\frac{18000}{N} \right) - 2$ where $x =$ number of bytes per sector, $N =$ number of sectors. Fractional remainders may be ignored.

Example: 32 sectors

$$\text{No. of Sectors} = 32 / \frac{562.5}{18000}$$

Number of bytes per sector = 562 (subtract remainder of .5)

Two bytes must be subtracted $\underline{-2}$

560 = Actual synthesizer count

To program synthesizer:

1. Begin with all 12 locations plugged.
2. Subtract largest synthesizer number that is less than sector length number and repeat until result is zero:

$$\begin{array}{r} 560 \\ -512 \quad \text{Remove 512 jumper} \\ \hline 48 \\ -32 \quad \text{Remove 32 jumper} \\ \hline 16 \\ -16 \quad \text{Remove 16 jumper} \\ \hline 0 \end{array}$$

Figure 14. Sector Synthesizer

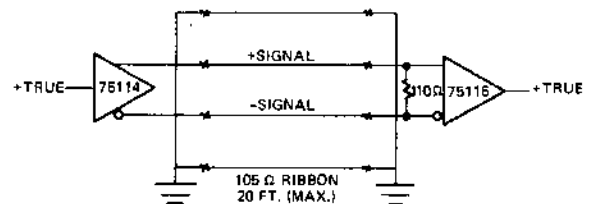


Figure 15. Data Line Driver Receiver

4.1.3.1 Write Data

Provides the drive with the data to be written on the track in standardized NRZ (non return to zero) format. When the +WRITE DATA line is more positive than the -WRITE DATA line a logical "one" is present on the line; the inverse is a logical "zero." This signal is sampled at the drive on the trailing edge of each WRITE CLOCK PULSE. WRITE DATA is gated at the drive by WRITE GATE, READY, and WRITE FAULT.

4.1.3.2 Write Clock

Is used by the drive to sample the standardized WRITE DATA. The control unit should ensure the WRITE DATA line is stable at the negative transition of WRITE CLOCK. This clocking scheme will ensure data integrity if the WRITE DATA and CLOCK lines are equal in length. See Figure 6 for timing.

4.1.3.3 PLO Clock

When the control unit has activated DRIVE SELECT this interface line will send to the controller a nominal square wave that is derived from the clock track written on the disk. There are 144,000 pulses per revolution of the disk on this line. When WRITE GATE is active, PLO clock may be used by the control unit to clock write data into the drive (PLO clock becomes write clock).

When read gate is active, PLO clock is locked to read data (See Figure 5).

4.1.3.4 Read Data

This carries the READ DATA in standardized NRZ format to the control unit. This line will not contain valid data until 8.0 μ s after the READ GATE signal is activated. READ DATA is enabled by DRIVE SELECT and READ GATE and is clocked by the positive transition of PLO clock (See Figure 5).

4.1.4 Alternate Output Signals

Three alternate output signals, READY, INDEX, and BYTE CLOCK, are offered when the J2/P2 radial connection is chosen. These signals are not enabled with DRIVE SELECT but are continuously available.

The corresponding signals in the J1 connector are deleted from that connector by removal of jumper plugs RY, IX, ST respectively.

4.2 Power Interface

The drive requires both AC and DC power for operation. The AC power is used for the drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC Power

The AC power to the drive is via the connector J4 located on the PCB side of the drive near the AC motor capacitor. Table 3 shows a listing of the AC power requirements.

4.2.2 DC Power

DC power to the drive is via connector J3/P3 located on the component side of the Actuator Driver PCB. The three DC voltages and their specifications along with their J3/P3 pin designations, are outlined in Table 4.

Table 3. AC Power Requirements

Conn P4	60 HZ		50 HZ	
	110V (Standard)	208/230 V	110 V	220 V
1	90 – 127 V	180 – 253 V	90 – 127 V	180 – 253 V
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	90 – 127 V Return	180 – 253 V	90 – 127 V Return	180 – 253 V
MAX RUN CURRENT	2.2 A	1.4 A	2.9 A	1.9 A
FREQ TOL	±0.5 HZ		±0.5 HZ	
TYPICAL RUN CURRENT	1.9 A	1.2 A	2.4 A	1.5 A
MAXIMUM SURGE (DUR = 30 SEC)	9.72 A	5.60 A	9.72 A	5.60 A

Table 4. DC Power Requirements

P3	DC VOLTAGE	TOLERANCE	CURRENT	MAX. RIPPLE (P-P)
1	+24 VDC	±2.4 VDC	3.0 A (Max.) 2.5 A (Typ.)	1 V
2	+24 Return			
3	-5 V Return	±0.25 VDC	0.10 A Typical 0.15 A Max.	N/A
4	-7 to -16 VDC Optional -5 VDC			
5	+5 VDC	±0.25 VDC	3.0 A Max. 2.5 A Typical	50 MV
6	+5 V Return			

NOTE: The frame and DC ground must be connected together at either the host system or at the drive through a single wire.

5.0 PHYSICAL INTERFACE

The electrical interface between the SA4000 and the host system is via four connectors. The first connector, J1, provides control signals for the drive; the second connector, J2, provides for the radial connection of the read/write signals for multiple drive systems; the third connector, J3, provides DC power; and the fourth connector, J4, provides AC power and frame ground. Refer to Figure 20 for the connector locations.

5.1 J1/P1 Connector

Connection to J1 is through a 50 pin PCB edge connector. The dimensions for this connector are shown in Figure 16. The pins are numbered 1 through 50 with the even numbered pins located on the component side of the PCB and odd pins located on the non-component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the AC connector and is labeled. A Key Slot is provided between pins 6 and 8. The *recommended mating connector* for P1 is a Scotchflex ribbon connector P/N 3415-0001 or AMP Thinleaf printed circuit connector P/N 1-583717-1 utilizing AMP contacts P/N 1-583616-1.

5.2 J2/P2

Connection to J2 is through a 20 pin PCB edge connector. The pins are numbered 1 through 20 with the even numbered pins located on the component side of the PCB. The *recommended mating connector* for P2 is a Scotchflex ribbon connector P/N 3461-0001 or AMP P/N 583717-1 with AMP contacts P/N 1-583616-1. Figure 17 shows the dimensions for the connector.

5.3 J3/P3

The DC power connector, J3, is a 6 pin AMP Mate-N-Lock connector P/N 1-380999-0, Figure 18, mounted on the component side of the Driver/Actuator PCB. The *recommended mating connector*, P3, is an AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. The J3 pins are labeled on the connector.

5.4 J4/P4

AC power and frame ground is interfaced through a 3 pin connector, J4, located on the PCB side of the drive near the AC motor capacitor. The AMP part number for J4 is 1-480701-0 with pins AMP P/N 35087-1 and 350654-1 (ground pin), refer to Figure 19. The *recommended mating connector*, P4, is AMP socket P/N 1-480700-0 with AMP pins P/N 350536-1.

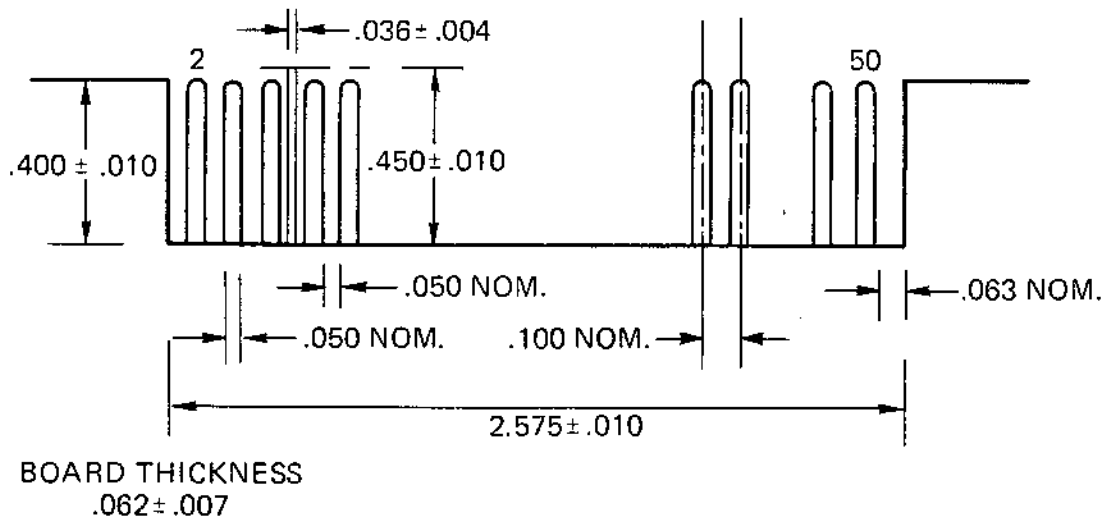


Figure 16. J1 Connector Dimensions

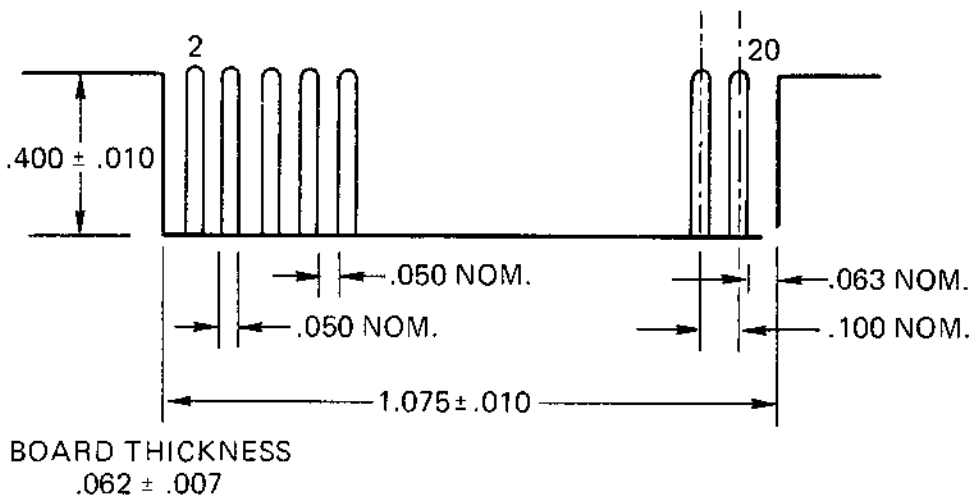


Figure 17. J2 Connector Dimensions

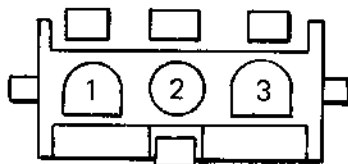


Figure 18. J4 Connector

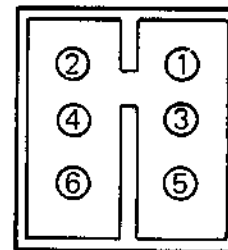


Figure 19. J3 Connector

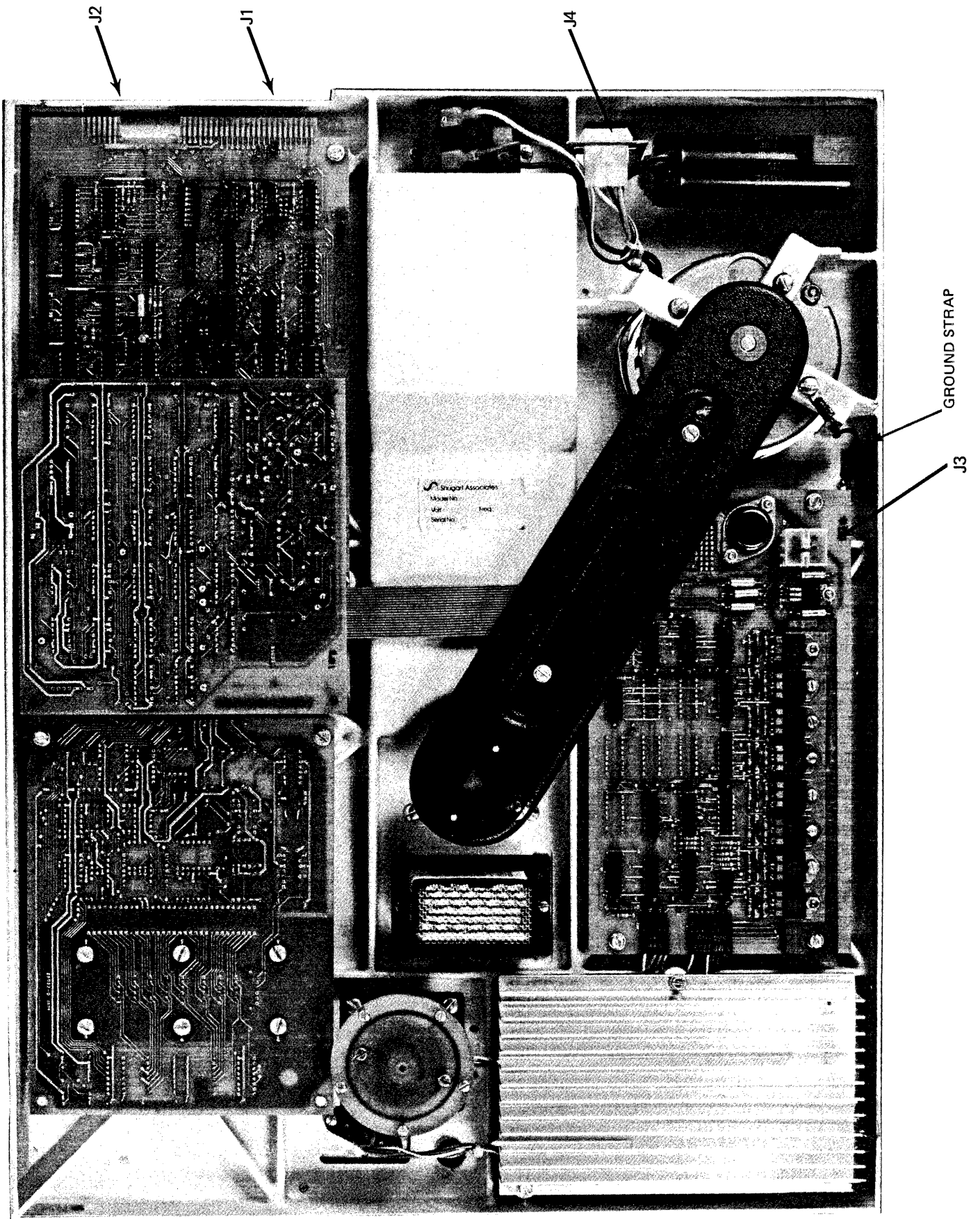


Figure 20. Interface Connectors

5.5 Drive Ground

The drive is shipped with DC ground (base casting) and AC ground (drive motor) connected together with a ground strap located on the drive motor, Figure 20. If system configuration requires the separation of these grounds, remove the ground strap.

6.0 DRIVE PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for this SA4000.

6.1

Reference Figure 21 for dimensions of the SA4000.

6.2

The SA4000 is capable of being mounted in either one of the following positions.

1. Vertical – Spindle drive motor up.
2. Horizontal – PCB's facing up.

Note: No other method of mounting is recommended as this may cause unsatisfactory dissipation of heat.

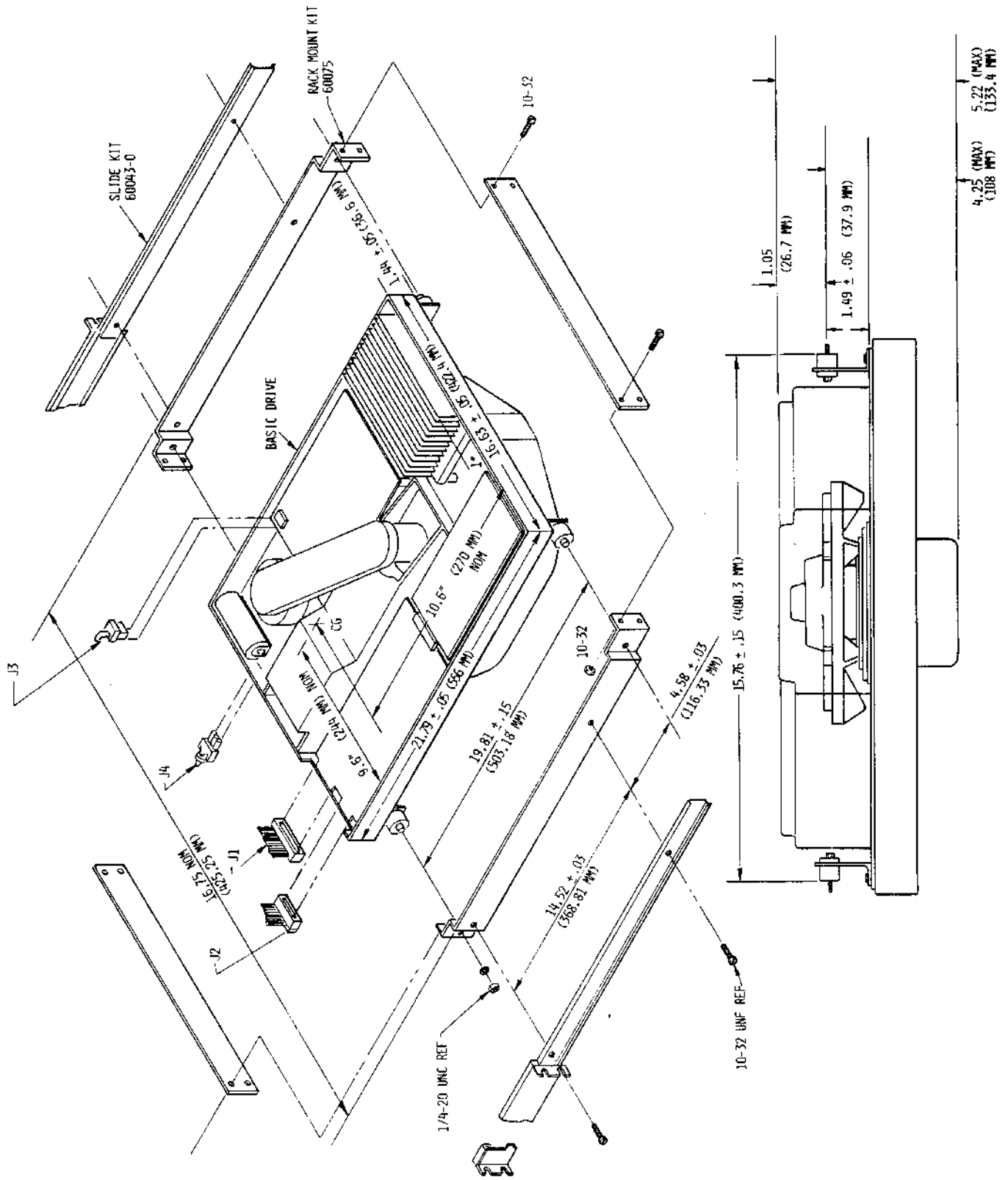


Figure 21. SA4000 Physical Dimensions

7.0 INSTALLATION INSTRUCTIONS

7.1 Mounting

The SA4000 is equipped with four shipping brackets, which should be removed when installing the unit in your system. However, during receiving inspection, the drive may be tested while resting on these brackets. It is recommended that the drive be mounted by the rubber shock mounts provided. These mounts can be expected to sag a maximum of 0.100 inches (.25 cm) when mounted (static measurement). See figure 21 for mounting dimensions.

7.2 CAUTIONS

Remove the locking screw on the spindle pulley.

Caution: Avoid rotating the spindle pulley. Head/Media damage could result if rotated backwards.

7.3 JUMPER OPTIONS (Actuator PCB) (Fig. 22)

Designator	Description
-5/-15	Drive requires -5V input (-5 position) but will regulate higher negative voltages from -7 to -16 (-15 position). Normally shipped with jumper in -15 position.

7.4 JUMPER OPTIONS (Control PCB) (Fig. 23)

Designator	Description
X	Drive always selected – normally shipped in this position.
DS1, 2, 3, 4	Four drive select jumpers allow logical drive assignment.
ST	Allows byte clock/sector signal to be active on J1 cable. Shipped jumpered.
RY	Allows ready signal to be active on J1 cable. Shipped jumpered.
IX	Allows Index pulse signal to be active on J1 cable. Shipped jumpered.
T	If jumpered, allows internal delay from power on to ready active. Shipped jumpered.
C	If jumpered, allows seek complete signal to connect to D54. Line (single drive system). Shipped open.
SC	If jumpered, enables sector marks to be active on byte clock line. Shipped jumpered.
BC	If jumpered, enables byte clock signal on byte clock line. Shipped open.

Designator	Description
LSB, MSB	Sector Synthesizer option (see Section 4.1.2.7 for description). Shipped with all locations jumpered.
D	If jumpered, enables stepper motor power (+24 V) with drive select (reduces power requirements in multiple drive system). Shipped jumpered.
E	If jumpered, enables sector pulse at index pulse time (see Figure 14). Shipped Open.
SI	If jumpered, enables sector pulse at index pulse time (see Figure 14). Shipped Open.
S2	If jumpered, masks sector pulse at index pulse time (see Figure 14). Shipped jumpered.
4H	16 pin jumper shunt allows – write clock, write data, read data, and PLO clock to be active on the J1 cable (single drive system). Shipped with shunt.
E1, E2, E3	Pins for connecting led option which allows visual confirmation of the following signals: ready, drive select, and write fault.
R	If jumpered, connects ready line to LED. Shipped jumpered.
S	If jumpered, connects drive select to LED. Shipped open.
F	If jumpered, connects write fault to LED. Shipped open.
SL	If jumpered, enables the following I/O signals when drive select is active: index, ready, and byte clock. If jumper is removed, these signals are continuously active. Shipped jumpered.

7.5 JUMPER OPTIONS (Data Separator PCB) (Fig. 24)

Designator	Description
C	If jumpered, data separator will synchronize on field of zero's. Shipped jumpered.
D	If jumpered, data separator will synchronize on field of one's. Shipped open.

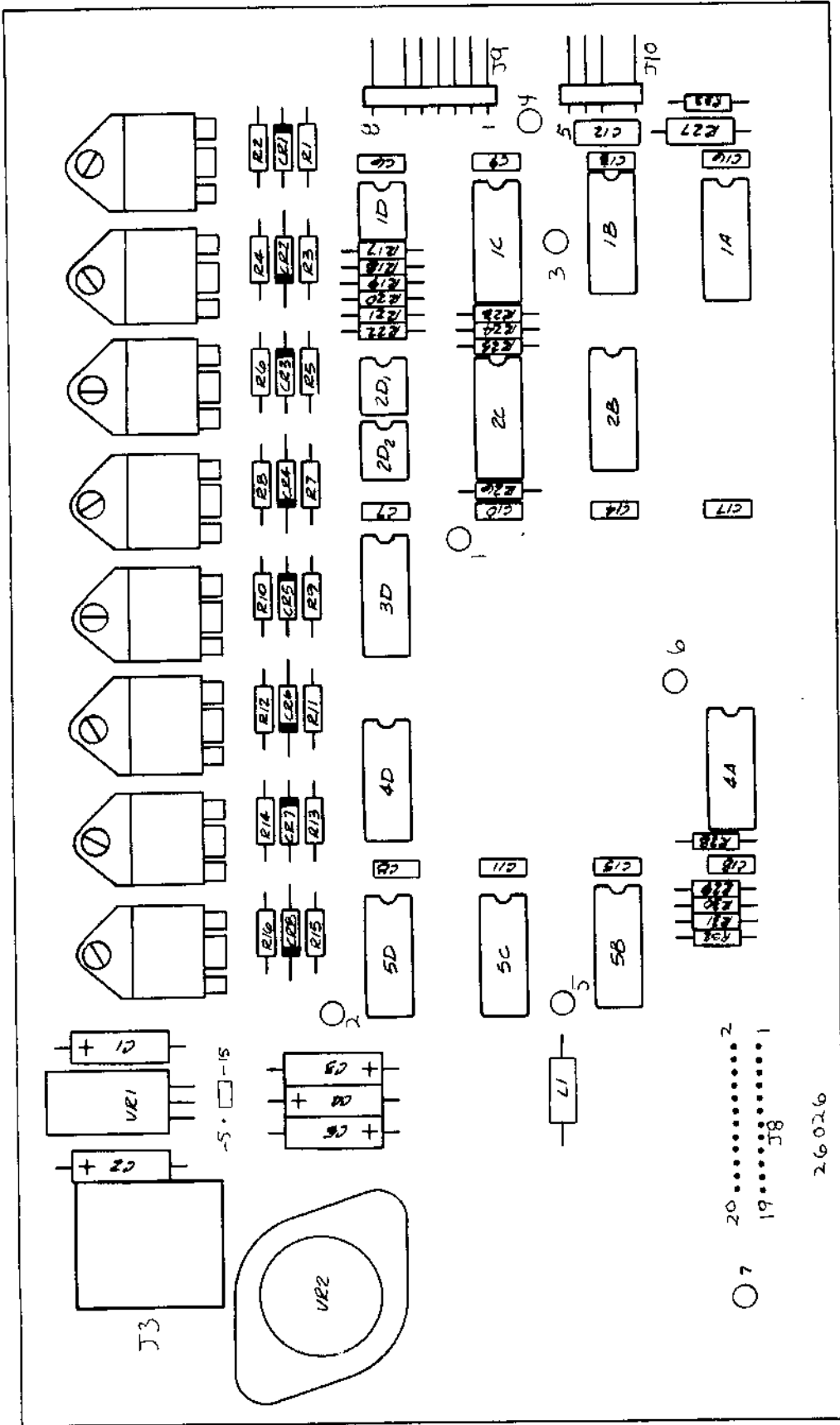


Figure 22. Stepper PCB

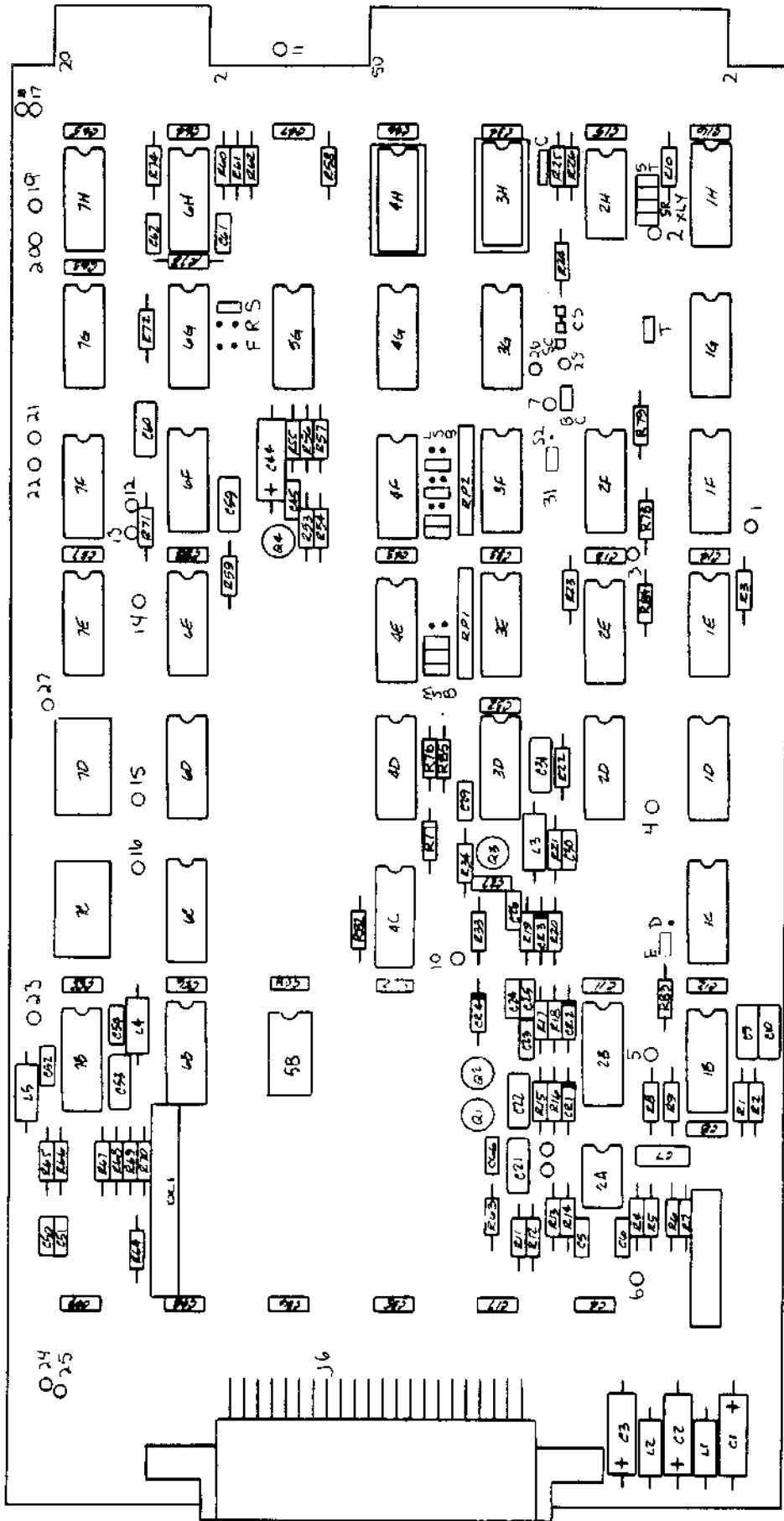


Figure 23. Control PCB

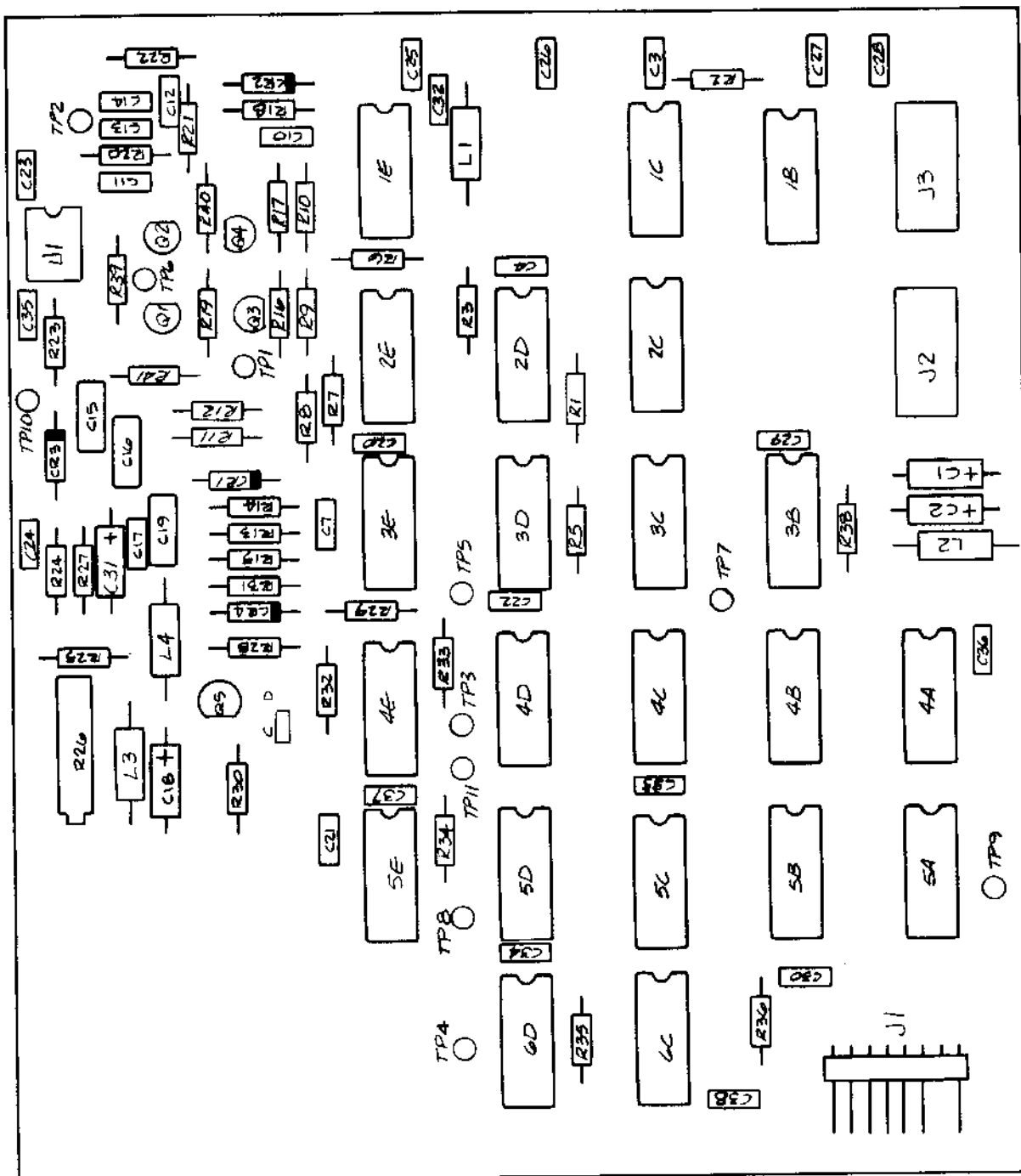


Figure 24. VFO PCB

8.0 SA4000 TRACK FORMAT

To establish a track format, review the following discussion and refer to figure 25.

8.1 INDEX/SECTOR TIMING CONSIDERATIONS

The SA4000 contains a clock track that is used to generate index and sector marks. There are exactly 9000 transitions per revolution of this clock track. A special pattern which is written on the clock track is decoded to provide an index pulse.

Internal to the drive, the clock track is multiplied, using a phase lock oscillator (PLO). The PLO clock output (7.1 MHz) is then divided to provide a byte clock output (18000 pulses per revolution). This byte clock is further divided by the sector synthesizer to provide sector mark pulses (see Section 4.1.2.7).

Detection of the index or sector marks will occur within $A \pm 8$ bit (\pm one byte) tolerance.

8.2 READ/WRITE TIMING CONSIDERATIONS

Any time the write gate signal is activated, write current is allowed to pass through the read/write head. This causes an undefined flux transition to occur on the media which is approximately one bit cell in length. If the data separator reads through this area, it is possible for the separator to decode data improperly. Therefore the read gate should always be activated beyond the known write turn on area.

Whenever the read gate is activated, it should be done in a sync up area prior to the sync character.

The data separator requires 8 microseconds maximum to lock to the data. Therefore, read gate should be activated at least 8 μ sec prior to any sync character. This timing restraint determines the minimum lengths of gaps 1, 2, and 3 (see Figure 25).

Another consideration for gap length is the write to read recovery time (20 μ sec). If, for example, a data field were being written and the next sequential sector was to be read/written, the length of gap 3 would have to take into account the 20 μ sec recovery time (about 17 bytes).

8.3 GAP LENGTH CALCULATION

Gap 1 may be calculated by adding the worst case index/sector jitter (2 bytes) plus the data separator sync up time (8 μ sec or \approx 7 bytes) plus approximately 3 bytes for the read gate turn on delay which gives us about 12 bytes.

Gap 2 is calculated the same as gap 1 except that an additional byte delay for read gate turn on is introduced. This gives us 13 bytes.

Gap 3, as mentioned previously, is only required to take into account the write/read recovery time of 20 μ sec, which gives us 17 bytes.

These calculations are minimums. No constraints are placed on longer gap lengths.

8.4 THE IDENTIFICATION (ID) FIELD

Figure 25 shows an ID field which precedes each data field. The ID field contains cylinder, head, and sector information. The first byte of the ID field is a sync character. This special sync character defines the beginning position of the ID field and also defines the byte boundaries.

Appended to the end of the ID field are two bytes (16 bits) of a polynomial known as cyclic redundancy check characters (CRC). This polynomial is absolutely unique for the contents of the ID field and is used to verify that the contents of the ID field are correct.

8.5 THE DATA FIELD

Figure 25 shows the data field which is the actual storage area of the system data. Data fields may be virtually any length, but most common lengths vary from 128 bytes to 512 bytes.

The first byte of the data field is a sync character which is different in pattern from that used in the ID field.

Appended to the end of the data field are two bytes of crc which is absolutely unique for the contents of the data field.

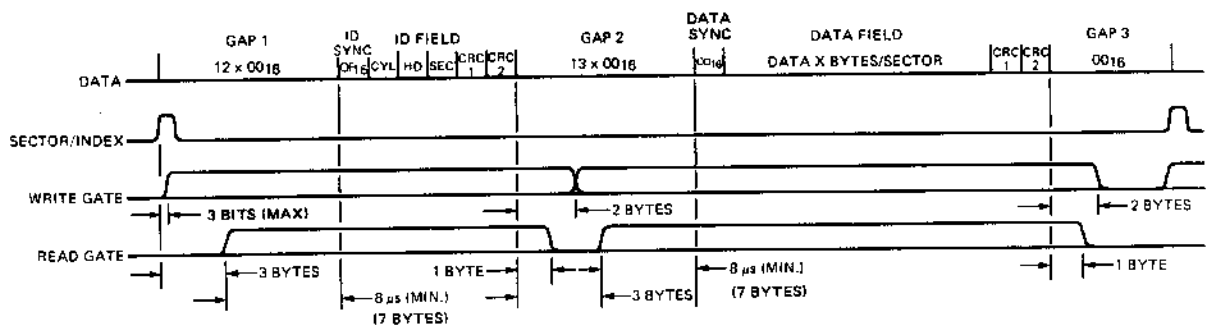


Figure 25. SA4000 Suggested Track Format

APPENDIX A

The SA4000 can be incorporated into a system utilizing many different interconnect approaches. The following diagrams are presented as an aid to the system designer.

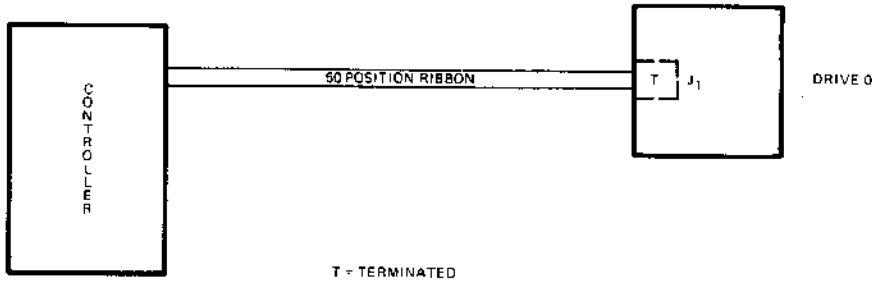


Figure A1. Single Drive System

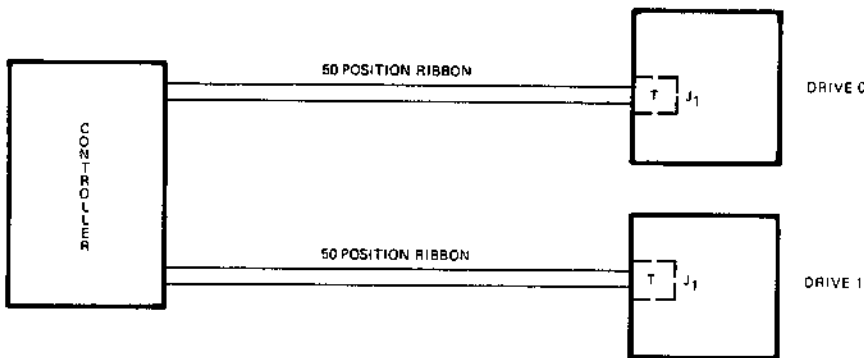


Figure A2. Multiple Drive System Radial Connection

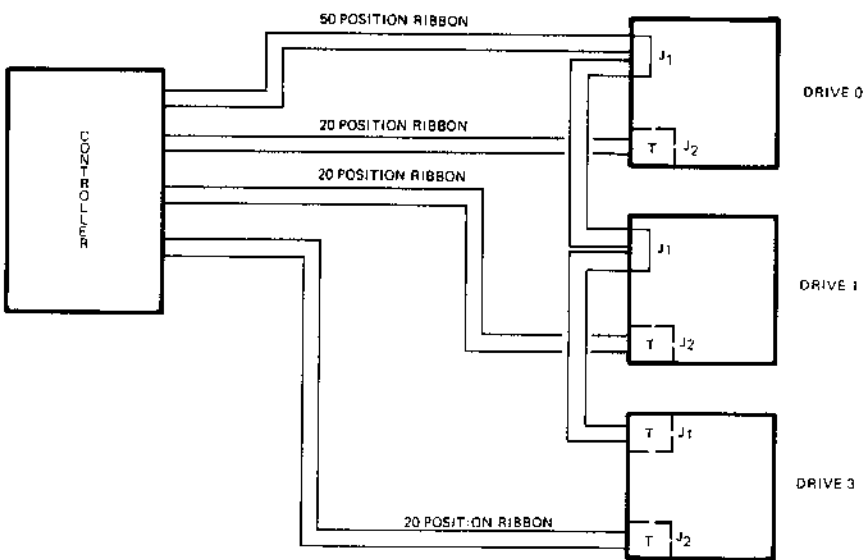


Figure A3. Multiple Drive System, Daisy Chain Connection

APPENDIX B

MEDIA DEFECT & ERRORS

Introduction

In high density digital recording storage systems it is necessary to increase the reliability or improve the operational performance by providing an error detection and correction scheme. For disk storage systems, the predominant error pattern is a burst of errors occurring in one or more tracks which are drop outs (absent bits) or shifted bits from their nominal position more than the data separator can tolerate them to shift. These errors are due to defects in the media as well as signal to noise ratio contributing to probability of error occurrence. The error rate is dependent upon noise and phase characteristics of media, Read/Write circuits, head and mispositioning of actuator.

Why Have Errors?

The errors are due to defects or minute imperfections in the disk media. As the storage size and density of information increases, these defects become more apparent to the system. Winchester technology utilizes a higher bit packing ratio, 5000 to 6000 BPI, than older types of drives and generally provides greater capacity per disk.

What Is The Definition Of An Error?

An error is a discrepancy between a recovered data and a true correct recorded data. There can be an extra bit or a missing bit, i.e., a "zero" can be transformed into "one" or a "one" can be changed to zero. Errors can be classified into soft or hard errors. Soft errors are generally related to signal to noise ratio of the system and represent marginal conditions of head, media, Read/Write circuits.

If an error is repeatable with a high probability, it is due to a media defect and is termed a hard error. Some hard errors may be ignored if they reside in an unused area of the format.

For those areas that contain media defects, alternate track/sector areas must be allocated or the area is simply avoided. Media defects are addressed per level of controller and software sophistication, i.e., skip and/or reassignment of bad sector(s), or skip and/or reassignment of bad track(s).

How Will Shugart Find The Errors?

The errors will be identified prior to shipment and information incorporated in a usable format to enable the user to skip those defective locations per his system capability. Shugart will have a unique

media test system which will exercise the drive in extreme marginal conditions and measure the amplitude and phase distortion of each bit recorded on the disk storage. Thus, drives shipped will be tested for media defects. These defects will be reported in a map shipped with the drive.

Error Reporting

A map will be provided with each drive showing defective bytes as a location from index identified by cylinder and head address. Additionally, an error free track at track 0 for each head and for the optional fixed heads will be guaranteed.

Error Acceptance Criteria

There will be no more than 12 tracks with defects per head of which no more than 4 tracks will contain multiple defects.

APPENDIX C

Ordering Information

1. Product Selection Index

Table C1 provides the information for constructing a unique P/N for an SA4000.

2. Accessories

- A. Rack Mounting Kit P/N 60075
- B. Slide Kit P/N 60043
- C. Evaluation Kit P/N 60066 contains:
 - 1. Signal Cable Connector Kit P/N 50604
 - 2. DC Connector Kit P/N 50605
 - 3. AC Connector Kit P/N 50879

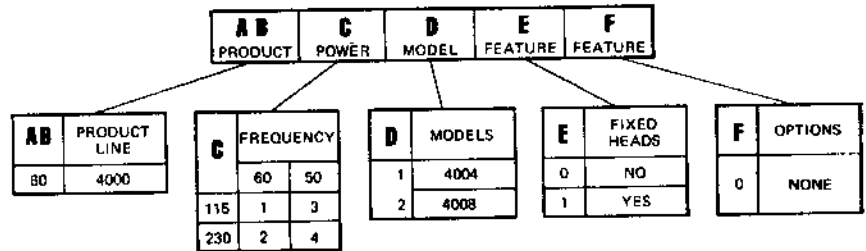


Table C1. Product Selection Index

3. AC Voltage and/or Frequency Conversion

If it is required that the AC voltage or frequency be changed on an SA4000, the following ordering information is offered.

PRIMARY VOLTAGE & FREQUENCY	PART NUMBERS		
	MOTOR ASM.	MOTOR PULLEY	BELT
115 VAC, 60 Hz	60082	60024	10902
110/115 VAC, 50 Hz	60082	60056	10903
230 VAC, 60 Hz	60081	60024	10902
230 VAC, 50 Hz	60081	60056	10903



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