SA1403 Controller

OEM Manual

Shugart

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1.0 INTRODUCTION

The SA1403 Controller consists of a microprocessor-based controller with on-board data separator logic, and is able to control a maximum of four drives. The drives can be any combination of Shugart SA1000 fixed disk drives, SA800 floppy disk drives, or SA850 floppy disk drives. The SA1403 can be mounted on the SA1000 drive.

Commands are issued to the controller over a bidirectional bus connected to the host computer. The data separator/"serdes" logic serializes bytes and converts to MFM data, and deserializes MFM data into 8-bit bytes.

Due to the microprogrammed approach utilized in the controller, limited diagnostic capabilities are implemented. This methodology increases fault isolation efficiency and reduces system down time. Error detection and correction will tolerate media imperfections up to one 4-bit burst error per sector on the SA1000.

1.1 SA1403 CONTROLLER FEATURES

OVERLAPPED SEEK	In multiple drive configurations, the host can issue seeks to different drives without waiting for the first drive to complete its seek.
AUTOMATIC SEEK AND VERIFY	A seek command is implied in every data transfer command (READ, WRITE, CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.
FAULT DETECTION	Two classes of faults are flagged to improve error handling: * Controller faults * Disk faults
AUTOMATIC HEAD AND CYLINDER SWITCHING	If, during a mutli-block data transfer, the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.
DATA ERROR SENSING AND CORRECTION	If a data error is detected during a disk data transfer, the controller indicates whether or not it is correctable. If correctable, it can be automatically corrected.
LOGICAL TO PHYSICAL DRIVE CORRELATION	Logical unit numbers (LUN's) are independent of physical port numbers. All accesses specify LUN's.
ON BOARD SECTOR BUFFER	A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.
EFFICIENT HOST INTERFACE PROTOCOL	A bidirectional bus between the controller and host provides a simple yet efficient communication path. In addition, a high level command set permits effective command initiation.
SECTOR INTERLEAVE	Sector interleaving is programmable with up to a 16 way interleave.
ODD PARITY	The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.
FIXED SECTOR SIZE	The sector size is fixed at 256 bytes of data.
NUMBER OF DRIVES	The controller will connect to a maximum of four (4) drives. The drives can be any combination of SA1000's and/or SA850's and/or SA800's.

1.1.1 OPTIONAL MICRO DIAGNOSTICS

A set of diagnostic PROM's are available to allow stand alone diagnostic testing of both drives and controller. Reference Appendix A.

1.2 SYSTEM CONFIGURATION

The controller and data separator comprise a single PCB that can be mounted onto the SA1000 drive. A maximum of four (4) drives may be connected as shown in Figure 2.

2.0 SPECIFICATION SUMMARY

2.1 ENVIRONMENTAL LIMITS:

	Operating	Storage
Temperature F/C	32°/0° to 131°/55°	-40°/-40° to 167°/75°
Relative Humidity	10% to 95%	10% to 95%
Max Wet Bulb	80°F	non-condensing
Altitude	Sea level to 10,000 ft	Sea level to 15,000 ft

2.2 POWER REQUIREMENTS

Three power supply voltages are required for the SA1400 series controllers. The maximum current requirements are as follows:

+5VDC ± 5% at 4.6 Amps

-5VDC ± 5% at 0.5 Amps

+24VDC ± 10% at 0.1 Amps

Power is applied to the SA1400 series controller via J10 which is a 6 pin AMP Mate-N-Lok connector P/N 1-38099-0, mounted on the component side of the PCB. The recommended mating connector is an AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. The J10 pins are labeled on the connector. Figure 1 shows the pin assignments.

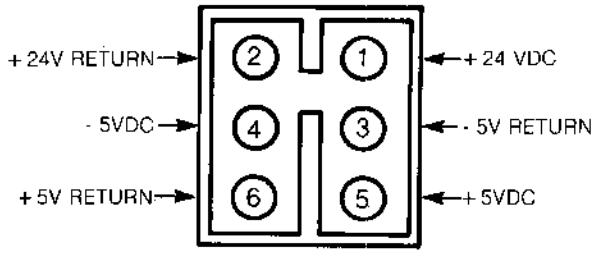


FIGURE 1. J10 PIN ASSIGNMENTS

2.3 PHYSICAL PARAMETERS

Refer to figure Figure 10 for dimensional layout. This physical parameters are as follows:

Length:	13.7 inches (34.8cm)	± .030" (.076cm)
Width:	8.25 inches (21cm)	± .010" (.025cm)
Height:	0.5 inches (1.3cm)	± .030" (.076cm)
Weight:	1.12 lbs (0.5Kg)	± .010 lbs (0.25g)

3.0 SA1403 DISK DRIVE INTERFACE

Shugart SA1000 and SA800/850 disk drives are interfaced to the controller via J1, J2, J3, J4, and J5. Refer to Figure 2 for connection block diagram.

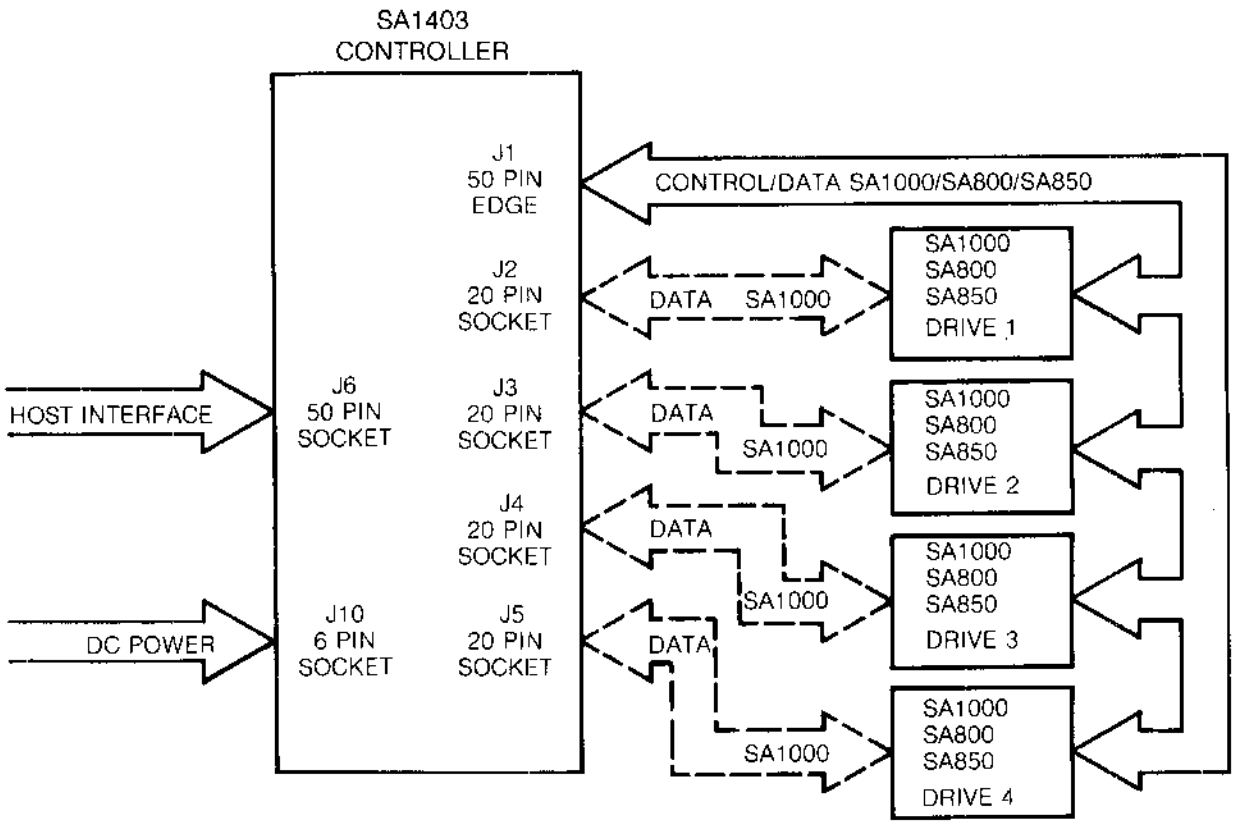


FIGURE 2. SA1403 INTERCONNECT DIAGRAM

NOTE: The last physical device on the control cable (drive to be terminated) must be an SA1000.

J1 is a 50 pin edge type connector which connects all drives in a daisy chain configuration. This connector carries control and data information for the floppy disk drives and control information only for the SA1000 disk drive. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J1 is a 3M Scotchflex P/N 3415-0001.

J2 through J5 are 20 pin socket type connectors used to radially connect the SA1000 data lines to the controller. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J2 through J5 is a 3M Scotchflex ribbon connector P/N 3421-3000. Figure 3 shows the pinouts for J1 and J2 through J5.

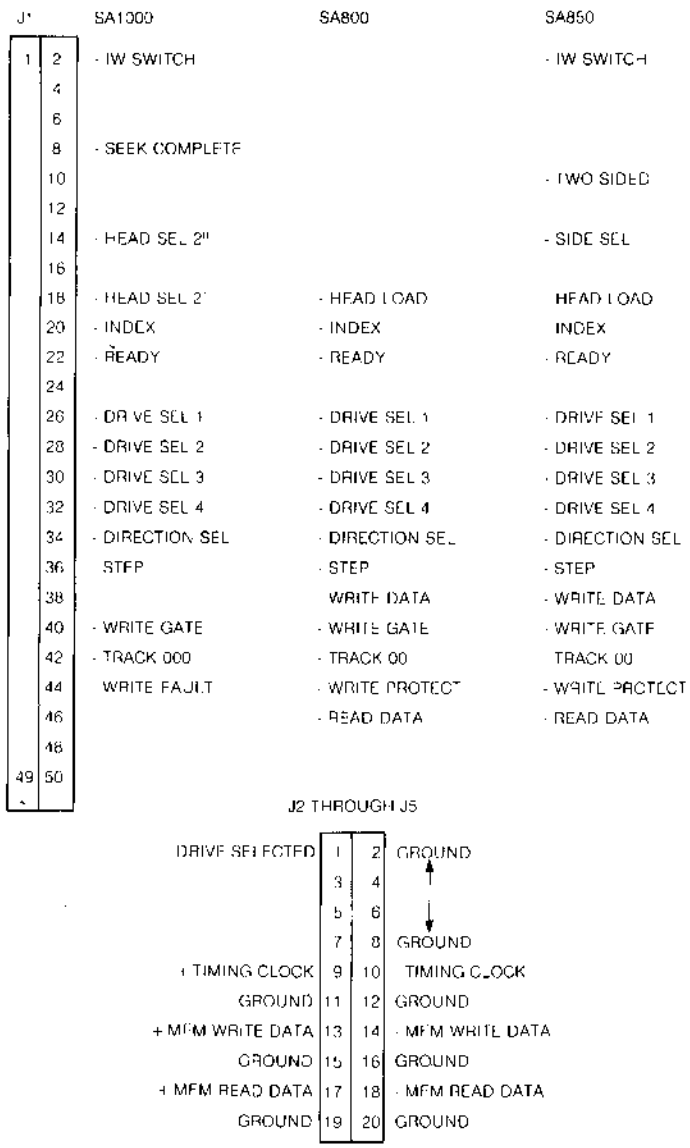


FIGURE 3. DRIVE CONNECTOR PINOUTS

3.1 CABLE TERMINATION

The last physical drive at the end of the J1 (50 pin) cable must be properly terminated. Termination networks are provided on the drives (refer to SA1000, SA800, or SA850 OEM manuals for location of termination networks). Termination networks must be removed from all drives except the last drive on the cable to avoid multiple termination.

NOTE: If a combination of fixed and floppy drives are used, the last drive terminated must be an SA1000.

4.0 HOST CPU INTERFACE

The SA1403 controller interface is a general purpose 8 bit parallel bus.

The Host CPU is interfaced to the controller via connector J6. J6 is a 50 pin socket type connector. The recommended mating connector for J6 is a 3M Scotchflex ribbon connector P/N 3425-3000. The J6 interface cable should not exceed 20 feet (6 meters).

4.1 HOST CPU ELECTRICAL INTERFACE

All Host CPU interface signals are negative true. The signals are "Asserted" or active at 0 VDC to 0.4 VDC. The signals are "Deasserted" or inactive at 2.5 VDC to 5.25 VDC.

4.1.1 HOST CPU INTERFACE TERMINATION

All Host CPU interface timings are terminated with a 220/330 ohm network. The Host CPU adaptor should be terminated in a similar fashion (see Figure 4).

The devices driving the controller inputs should be open collector devices capable of sinking at least 48 milliamps to voltage level of less than 0.5 VDC (7438 or equivalent).

The devices receiving the controller outputs should be of the SCHMITT trigger type to improve the noise margin (74LS240, 74LS14, or equivalent). The Host adaptor should not load the bus with more than 1 standard TTL input load per line.

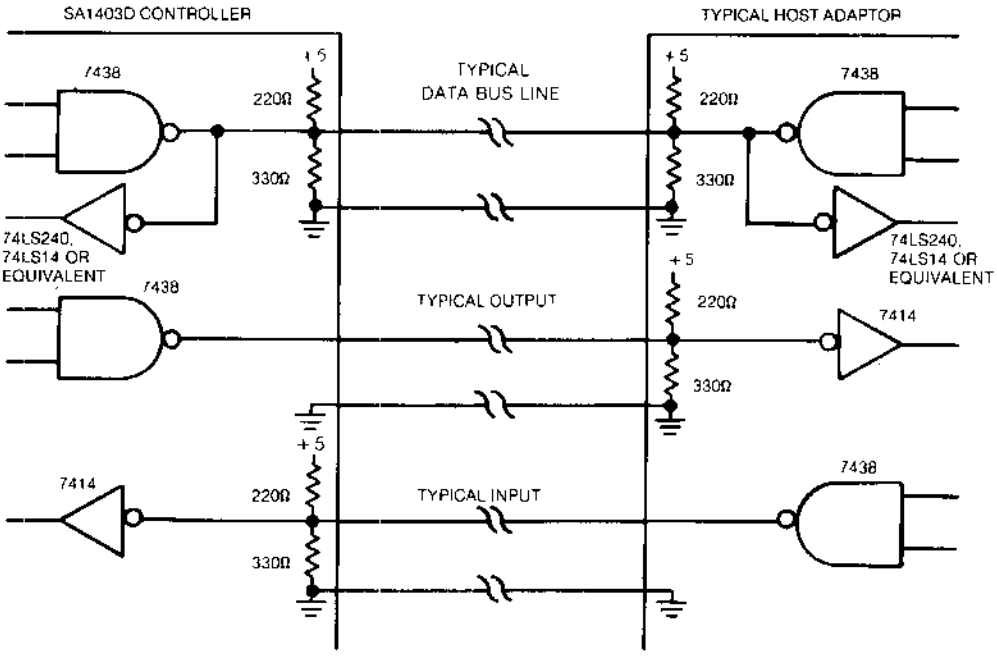
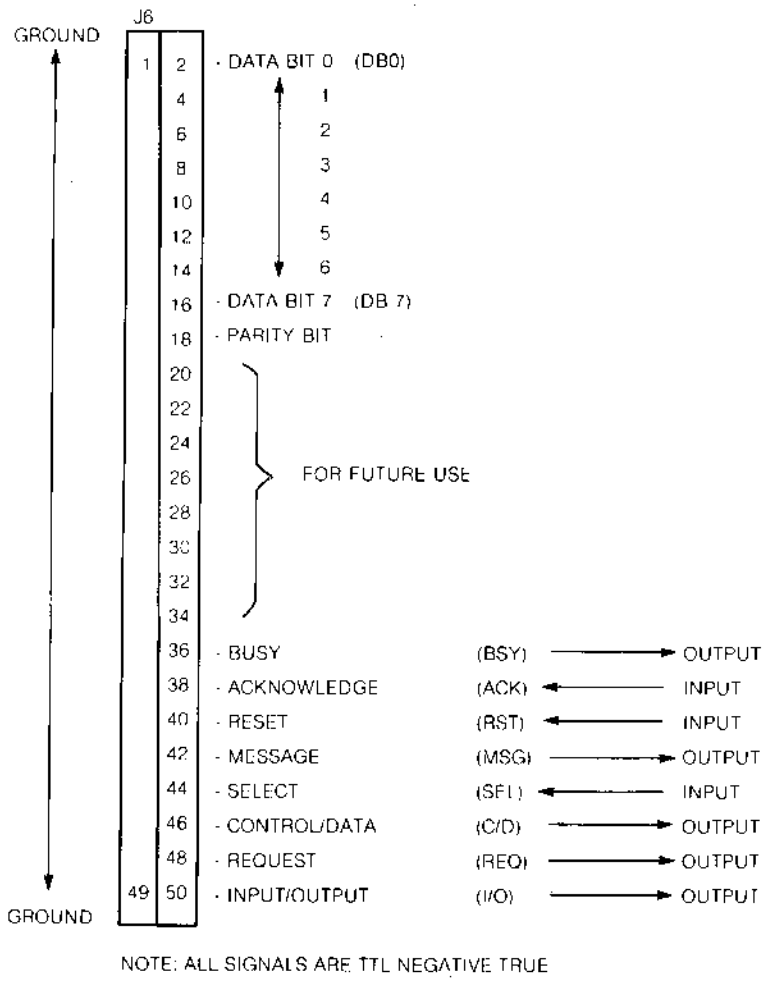


FIGURE 4. HOST ADAPTOR BUS TERMINATION

4.1.2 HOST CPU SIGNAL INTERFACE

The Host CPU signals are interfaced via J6. See Figure 5 for J6 pinouts.



NOTE: ALL SIGNALS ARE TTL NEGATIVE TRUE

FIGURE 5. J6 HOST INTERFACE CONNECTOR PINOUT

4.2 SA1403 HOST BUS

4.2.1 THEORY OF OPERATION

Disk commands are issued to the SA1403 via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution. (Command structure is described in Section 5.0). Depending on the type of command, the controller will request up to 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will send completion status to the host. (Further delineation of the completion status may be requested by issuing the appropriate sense commands).

Odd parity is generated by the SA1403 for all information that it puts on the I/O bus. If enabled, the SA1403 flags all information that it receives with bad parity.

4.3 SIGNAL DEFINITION

4.3.1 UNIDIRECTIONAL SIGNALS DRIVEN BY CONTROLLER

I/O — **Input/Output.** When asserted, the data on the bus is driven by the controller. When deasserted, the data on the bus is driven by the host adaptor. The host adaptor will use this line to enable its drivers onto the data bus.

C/D — **Control/Data.** When asserted, the data transmitted across the bus will be the command or status bytes. When deasserted, the data will be the disk data or request sense bytes.

BUSY — **Busy** is asserted as a response to the SEL line from the host adapter and to indicate that the host bus is currently in use.

MSG — **Message,** when asserted, indicates that the command is completed. This bit is always followed with the assertion of I/O, and the assertion of REQ.

REQ — **Request.** This bit operates in conjunction with I/O, C/D, & MSG. When asserted and I/O is asserted, REQ will mean that the data on the host bus is driven by the controller. When asserted and I/O is deasserted, REQ will mean that the data is driven by the host adaptor (H/A).

BUSY	I/O	C/D	MSG	MEANING
A	D	D	D	WRITE DATA BYTE TO CONTROLLER
A	A	D	D	READ DATA BYTE FROM CONTROLLER
A	D	A	D	WRITE COMMAND BYTE TO CONTROLLER
A	A	A	D	READ STATUS BYTE FROM CONTROLLER
A	A	A	A	READ MESSAGE BYTE FROM CONTROLLER
D	X	X	X	CONTROLLER IDLE

A = ASSERTED (0 VDC) D = DEASSERTED (>2.4 VDC) X = DO NOT CARE

TABLE 1. 1403 CONTROLLER STATE DECODE CHART

4.3.2 UNIDIRECTIONAL SIGNALS DRIVEN BY HOST ADAPTOR

ACK — **Acknowledge.** This bit is asserted as a response to REQ from the controller. The timing requirements on this signal with respect to the data are described in the REQuest section. ACK must be returned for each REQ assertion. Once REQ has been asserted, the controller waits 256μs for ACK return before timing out.

RST — **Reset.** When asserted, this bit forces the controller to the beginning of its microcode. Any error status request will result in invalid information after RST has been asserted. All signals to the drives are deasserted. RST must be asserted for a minimum of 250ns and a maximum of 10μs.

SEL — **Select.** When asserted, indicates the beginning of the command transaction. The H/A asserts SEL to gain the attention of the controller. A data bit on the host bus must also be asserted during SEL time to determine which controller is selected. SEL must not be asserted on the host bus before the data bit. The controller will return BUSY within 1μs.

4.4 DATA BUS BITS 0-7 (DB)

These bidirectional data lines are used to transfer 8 bit parallel data to/from the host adaptor. Bit 7 is most significant bit.

4.4.1 PARITY BIT

This bit is asserted to maintain odd parity on all data and status information transferred to the Host. If enabled, the controller will test for odd parity on all command and data information transferred to the controller (see section 11).

4.5 HOST INTERFACE PROTOCOL

There are 4 sequences required to initiate and complete a command to the SA1403 controller.

1) Controller Selection Sequence
2) Command Transfer Sequence
3) Data Transfer Sequence
4) Status and Message Transfer Sequence

4.5.1 CONTROLLER SELECTION SEQUENCE

In order to gain the attention of the controller it is necessary to perform a selection sequence. Refer to Figure 6.

The Host must first test BSY to determine if the controller is available. If BSY is deasserted, the Host will assert data bit 0 (controller ID) and then assert SEL. The controller will then respond by asserting BSY. At this point the Host must deassert SEL and data bit 0. I/O will remain deasserted throughout the selection sequence.

4.5.2 COMMAND TRANSFER SEQUENCE

Following the selection sequence the controller will assert REQ (see Figure 6). The Host will then place the first byte of the command descriptor block (see section 5.0) on the data bus. The Host will then assert ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, the controller will abort the command transfer sequence and attempt to transfer a status byte - see section 4.5.4). The controller will respond by reading the byte on the data bus and then deasserting REQ. The Host then must deassert ACK to begin the next transfer REQ/ACK handshake. This handshake continues until all bytes of the command descriptor block have been transferred.

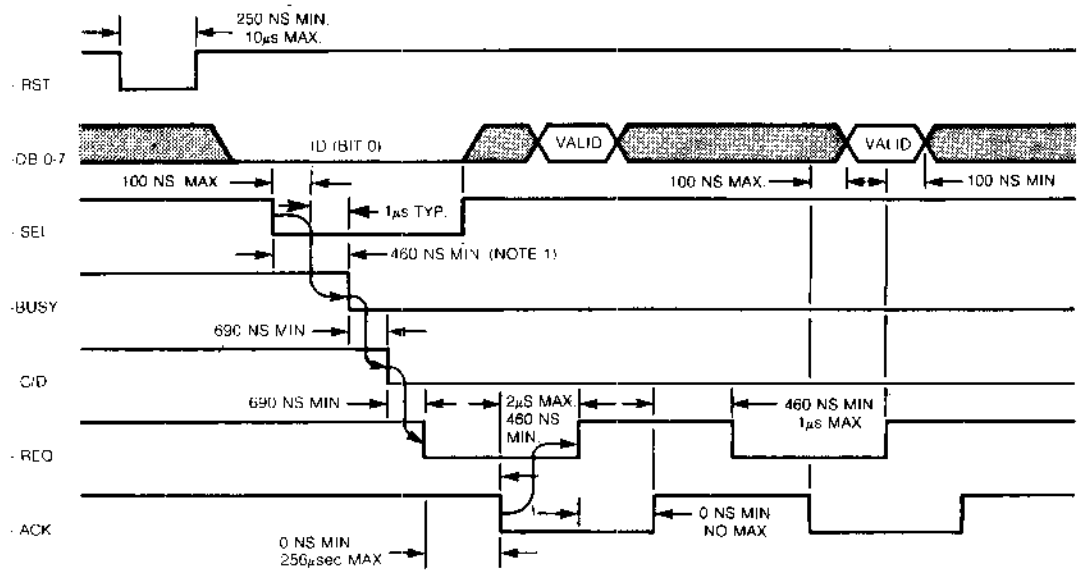


FIGURE 6. SELECT SEQUENCE TIMING

4.5.3 DATA TRANSFER SEQUENCE

Following the command transfer sequence, the controller will respond in one of four ways:

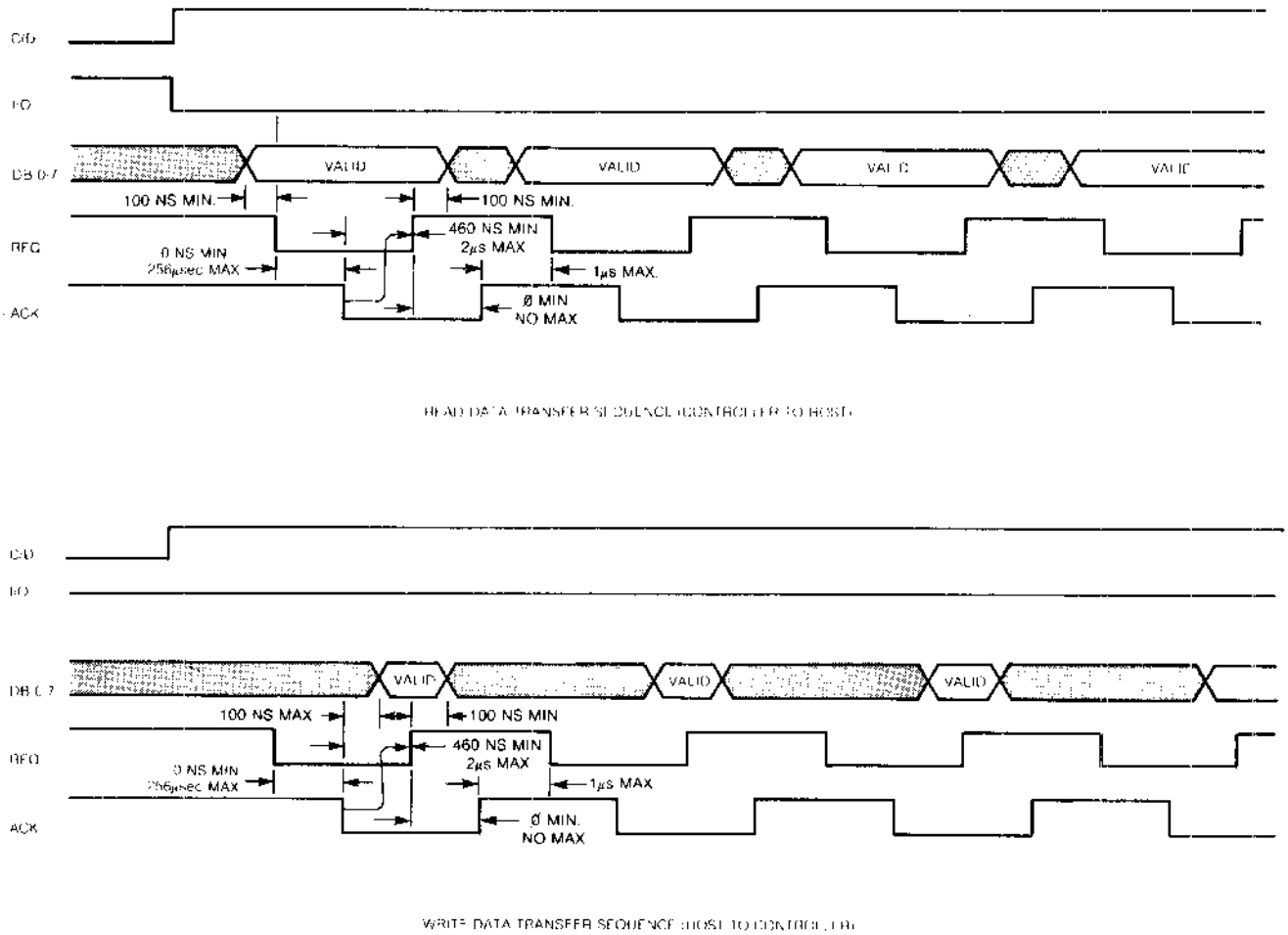
1) Begin seeking the drive.

2) Begin accepting write data from the Host.

3) Begin transferring read data to the Host.

4) Return status to the Host.

If the command sent to the controller involves a data transfer (see Figure 7), the controller will deassert the C/D line to indicate a data transfer. If the data transfer is from the Host to the controller (write data) the I/O line will be deasserted. If the data transfer is from the controller to the Host (read data) the I/O line will be asserted. The controller will then set the REQ line to request a byte transfer. The Host will respond by transferring a byte across the data bus and then asserting ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, the controller will abort the data transfer sequence and attempt to transfer a status byte - see section 4.5.4). The Host will then deassert ACK and wait for the next assertion of REQ. This handshake continues until 256 bytes of data have been transferred. For all data transfers, all 256 bytes will first be transferred to the sector buffer. The data will then be transferred to its destination, one byte at a time.



READ DATA TRANSFER SEQUENCE (CONTROLLER TO HOST)

WRITE DATA TRANSFER SEQUENCE (HOST TO CONTROLLER)

FIGURE 7. DATA TRANSFER SEQUENCE TIMING

4.5.4 STATUS AND MESSAGE TRANSFER SEQUENCE

Following a command transfer or data transfer, the controller will initiate a status byte and completion message transfer.

When a status byte transfer is required, the controller will assert C/D and I/O (see Figure 8). The controller will then assert REQ. The Host must then read the status byte on the data bus and then assert ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, REQ will be deasserted. REQ will then be asserted again transferring a status byte indicating that a time-out error has occurred.) The controller will then deassert REQ. The Host will then deassert ACK.

Following the status byte transfer, a completion message byte of all zero's will be transferred to indicate operation complete. The controller will assert the MSG line (along with I/O and C/D) and then assert REQ. The Host may read the completion message byte on the data bus and assert ACK (if ACK is not asserted within 256 microseconds, the controller will deassert the MSG line and attempt to transfer a status byte). The controller will respond by deasserting REQ. The Host will then deassert ACK. At this point BSY and all other controller I/O lines will be deasserted and the controller will return to an idle loop awaiting the next selection sequence.

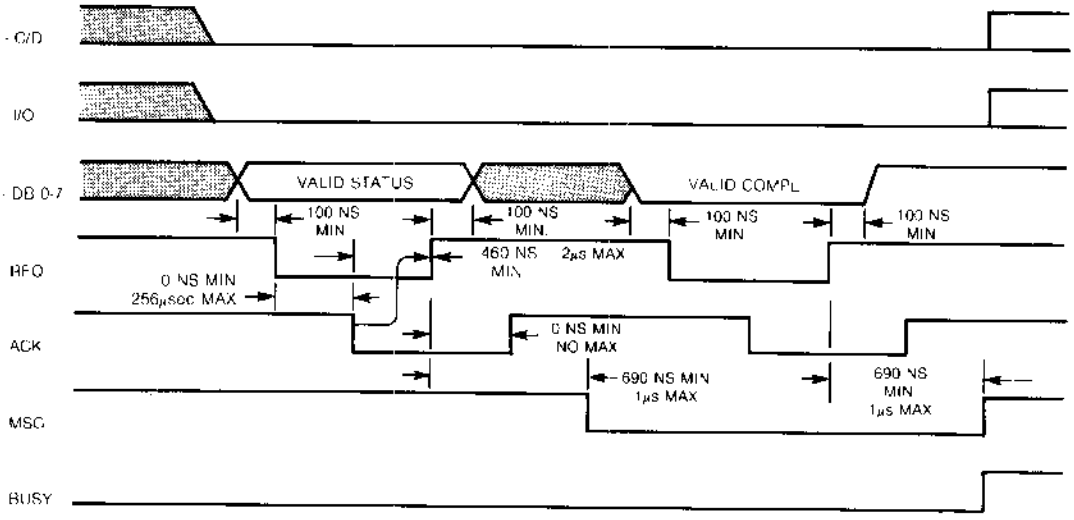


FIGURE 8. STATUS AND COMPLETION SEQUENCE TIMING

5.0 CONTROLLER COMMAND DESCRIPTOR BLOCK

Following the controller selection sequence the controller will request a command descriptor block (CDB) which, depending on the class of command, may be either 6 or 10 bytes in length. The first byte of CDB contains the command class and the command operation code. The remaining bytes specify the drive logical unit number (LUN), logical sector address, number of sectors to be transferred to a destination device (Copy Command), and a control field byte. If an error occurs in the CDB, the transfer is aborted upon detection of the error. The controller will then attempt to transfer a status byte to the host.

Commands are categorized into four classes:

Class 0 - Non-data Transfer, Data Transfer and Status Commands

Class 1 - Disk Copy Commands

Class 2-6 - Reserved

Class 7 - Diagnostic Commands

The command descriptor blocks in Command Class 0 and 7 are 6 bytes long. Those in Class 1 are 10 bytes long.

The controller will check all incoming command descriptor blocks for validity and will also check (if enabled) all CDB's and data for odd parity (see section 9.1). A parity error will cause an immediate halt of the command or data transfer. This will not cause incorrect data to be written because the write does not occur until the sector buffer has been filled. An error in the command structure will cause a status byte transfer to occur upon completion of the CDB transfer.

5.1 COMMAND DESCRIPTION (CLASS 0)

WARNING!
Commands READ and WRITE require that the floppy disk used be formatted. If unformatted, the controller will appear to 'hang' - i.e., continue waiting for an I.D. address mark. (Reset to clear this condition if it should occur).

Opcode (Hex)	**Description**
00	Test drive ready. Selects the drive and verifies drive ready. (No Op)
01	Recalibrate. Positions the R/W arm to Track 00, clears error status in the drive.
02	Request Syndrome - returns two bytes of error offset and syndrome to the Host System for Host error correction capability (see Table 2). The first byte is offset in the data field of the error location. The most significant 3 bits of the second byte point to the beginning bit of the error location. The least significant 4 bits of the second byte are the syndrome which is a data correction mark to be exclusive or'ed with the faulty data. This command is only valid if the automatic data correction has been disabled.

	MSB							LSB
	7	6	5	4	3	2	1	0
BYTE 1	BYTE OFFSET							
BYTE 2	BIT OFFSET			0	SYNDROME			

TABLE 2.

03 Request Sense. This command must be issued immediately after an error. It returns 4 bytes of drive and controller sense for the specified LUN (see copy block for exception). Reference section 5.3.2 for a description of the Sense Block.

04 Format Drive. Formats all blocks with ID field according to interleave factor and data fields. The data field contains 6C Hex.

05 Check Track Format.* Checks format on the specified track for correct ID and interleave. Does not read the data field.

06 Format Track.* Formats the specified track with bad block flag cleared in all blocks of that track. Writes 6C Hex in the data fields.

07 Format Bad Track* (bad block flag). Formats the specified track with bad block flag set in the ID fields. Writes 6C Hex in the data fields.

08 Read. Reads the specified number of blocks starting from initial block address given in the CDB.

0A Write. Wrties the specified number of blocks starting from initial block address given in the CDB.

0B Seek. Initiates seek to specified block and immediately returns completion status before the seek is complete for those drives capable of overlap seek.

* The track is addressed via the logical sector address, which may be any address within the desired track.

5.1.2 COMMAND DESCRIPTION (CLASS 1)

00 Copy Blocks. Copies the specified number of blocks from source LUN starting at the specified logical address to destination LUN starting at the specified logical address. The number of sectors transferred may be from 1 to 256. The completion status byte will indicate the source LUN. If an error occurs, the Request Sense command is issued to the source LUN. The sense will indicate type of error for the appropriate LUN. Note that the data in the blocks will be truncated or appended with undefined data if the source and destination block sizes are not the same (e.g. Source block size - 128 bytes/sector, and Destination block size - 256 bytes/sector).

5.1.3 COMMAND DESCRIPTION (CLASS 7)

00 RAM Diagnostic. Performs a data pattern test on the RAM buffer.

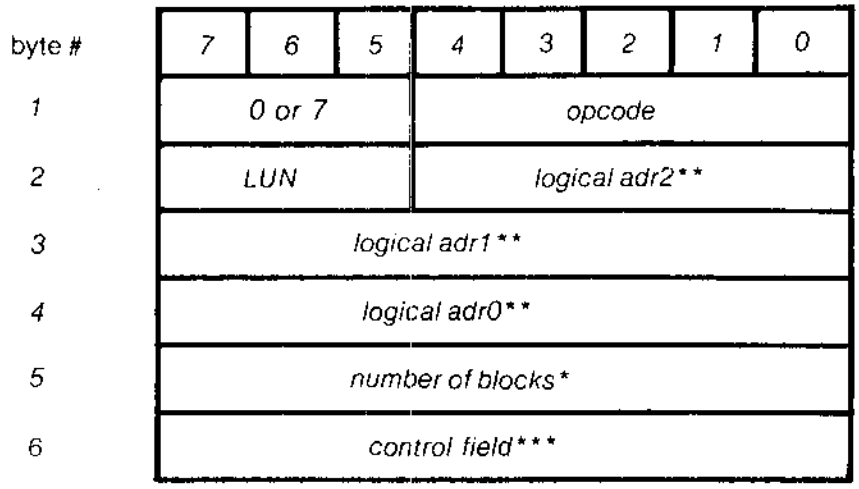
01 Write ECC. Displaces data on the disk by three bytes so that the ECC bytes can be written from the data specified. Used to verify the ECC logic.

02 Read ID. Transfers the cylinder, head, sector and 3 ECC bytes for the specified block ID field.

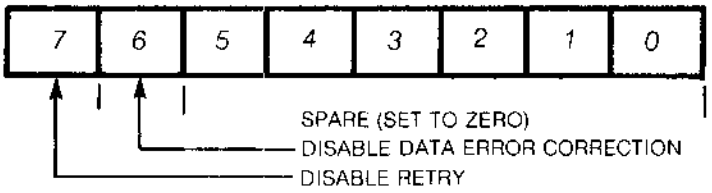
03 Drive Diagnostic 0. Performs a drive diagnostic. Reads sector 0 on all cylinders sequentially. Reads sector 0 on 256 random cylinders.

5.2 COMMAND FORMAT

5.2.1 CLASS 0 & 7 COMMANDS



*Interleave factor for Format, Check Track, and Read ID commands.
**Refer to section 5.5 Logical Address.
***The control field is defined as follows:



Commands in this group

a) NOP (Test drive ready)
b) Format Drive
c) Check Format
d) Request Sense
e) Request Syndrome
f) Recalibrate
g) Read Block(s)
h) Read ID
i) Write Block(s)
j) Format Track
k) Format Track (bad track flag)
l) Seek
m) Ram Diagnostic
n) Drive Diagnostic
o) Write ECC

5.2.2 CLASS 1 COMMANDS

byte	7	6	5	4	3	2	1	0
1	0	0	1	opcode				
2	LUN/s			logical adr2/s* (MS)				
3	logical adr1/s*							
4	logical adr0/s* (LS)							
5	number of blocks							
6	LUN/d			logical adr2/d* MS				
7	logical adr 1/d*							
8	logical adr0/d* (LS)							
9	spare							
10	control**							

where 's' indicates the source device and 'd' indicates the destination device.
*Refer to Section 5.5 Logical Address.
**Refer to Section 5.2.1 for Control Field definition.

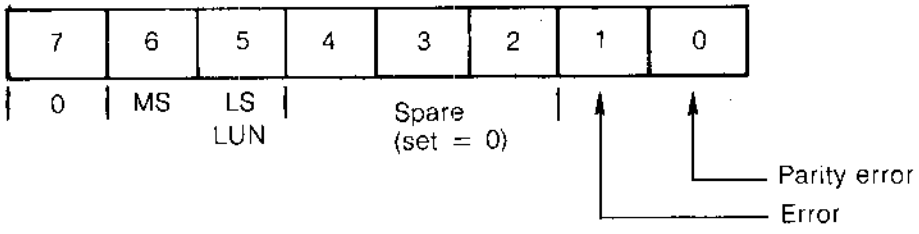
5.3 STATUS FORMAT

5.3.1 COMPLETION STATUS BYTE FORMAT

At the normal termination of a command, or following error detection, the controller will cause a status byte to be transferred from the controller to the Host. Bit 0, the least significant bit of the status byte, will be set equal to 1 if the controller detects a parity error during a command or data transfer to the controller (if enabled - see section 11). Bit 1 will be set = 1 if the controller detects an error condition. Bits 5 and 6 represent the LUN of the device where the error occured. If no error occurs, bit 0 - 4 will be set equal to 0.

Following the transfer of the status byte, the MSG line will be asserted to indicate a completion message. At this time the message consists of a single byte transfer will all bits set = 0.

Prior to an error condition the controller, unless disabled (see section 5.2.1 Control Field), will retry 3 times before posting the error.

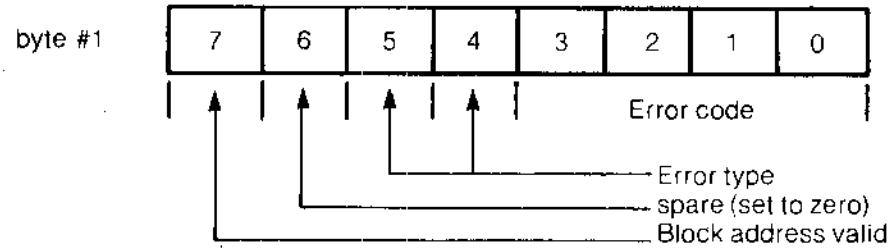


Bit 0 Parity error during transfer from host to controller.
Bit 1 Error occured during command execution.
Bit 2-4 Spare (set to zero).
Bit 5-7 Logical unit number of the drive.

5.3.2 DRIVE AND CONTROLLER SENSE

Following an error indication from the status byte, the Host may perform a REQUEST SENSE command to obtain more detailed information about the error.

The REQUEST SENSE command will transfer a block of 4 bytes to the Host system.



byte #	7	6	5	4	3	2	1	0
2	LUN			logical adr2*				
3	logical adr1*							
4	logical adr0*							

*Refer to Section 5.5 Logical Address.

5.4 ERROR CODES

5.4.1 TYPE 0 (DRIVE) ERROR CODES

0	No status
1	No index signal
2	No seek complete
3	Write fault (SA1000 only)
4	Drive not ready
5	Drive not selected (SA1000 only)
6	No track 00

5.4.2 TYPE 1 (CONTROLLER) ERROR CODES

0	ID read error.
1	Uncorrectable data error during a read.
2	ID Address Mark not found.
3	Data Address Mark not found
4	Record not found. Found correct cylinder and head but not sector.
5	Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
6	DMA Data time out error. No acknowledge within 256μs.
7	Write protected (SA800/850 only).
8	Correctable data field error.
9	Bad block found.
A	Format Error. The controller detected that during the Check Track command, the format on the drive was not expected.

5.4.3 TYPE 2 (COMMAND) ERROR CODES

0 Invalid Command received from the Host.
1 Illegal disk address. Address is beyond the maximum address.

5.4.4 TYPE 3 (MISC) ERROR CODES

0 RAM error. Data error detected during Sector buffer RAM diagnostic.

5.5 LOGICAL ADDRESS

The logical address is computed as follows:

Logical adr = (CYADR * HDCYL + HDADR) * SETRK + SEADR

Where: CYADR = cylinder address
HDADR = head address
SEADR = sector address
HDCYL = number of heads per cylinder
SETRK = number of sectors per track

Bit 0 of Logical adr0 = the least significant bit.
Bit 4 of Logical adr2 = the most significant bit.

NOTE: All logical addresses begin at 00.

6.0 SECTOR INTERLEAVE CODES

In order to tailor host system data transfer speed to the disk rotational speed, sector interleaving is offered. Sixteen interleave codes are offered numbered 1 to 16. Not all interleave codes will result in optimum sector interleave, therefore the interleave should be chosen carefully. In order to maintain IBM floppy disk compatibility an interleave code of 1 should be used. This will result in a non-interleave condition.

NOTE: Due to timing limitations on data transfers, an interleave code of 16 may not result in increased speed.

The interleave code given during the format command is used to calculate the logical sector number as follows: Logical Sector = (Physical Sector × Interleave code) (mod 32). Note: when the logical sector number exceeds 31 the next logical sector is the lowest available physical sector. This does not always create a true modulo function.

The interleave algorithm is: Sector + Interleave.

Two exampes of interleave codes are shown:

Interleave code of 2:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
Physical:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31

Interleave code of 11:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	11	22	1	12	23	2	13	24	3	14	25	4	15	26	5
Physical:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	16	27	6	17	28	7	18	29	8	19	30	9	20	31	10	21

Code	Number of Disk Revolutions Required to Read One Track	Time available to Transfer one Byte of Data (including controller time)	Minimum Number of Idle Sectors Between Reads
11	3	4.7μs	2
8	4	7.0μs	3
6	6	9.4μs	4
5	7	11.7μs	5
4	8	16.4μs	7
3	11	23.4μs	10
2	16	35.1μs	15
1	32	72.5μs	31

* (for SA1400 series controllers operating with SA1000 series drives - double density, 32 sectors, 256 bytes/sector.)
Note: Other codes will work, but require more revolutions of the disk to read all sectors of one track.

TABLE 3. INTERLEAVE CODE SELECTION CHART*

7.0 DIAGNOSTIC PHILOSOPHY

7.1 OPTIONAL MICRODIAGNOSTIC PROMS

Fault Isolation Microdiagnostic (Optional)
The controller can be further checked out off-line by initiating explicit microdiagnostic routines via optional firmware diagnostic sets. The routines are initiated by a set of control switches. Errors will be displayed on a set of LED's. See Appendix A for a detailed description of this option.

8.0 STATUS LED ERROR INTERPRETATION

Drive/controller error conditions are displayed on the 8 LED display lights provided near the J10 DC power connector (see Figure 10). The following list of hexadecimal numbered error codes describe error meanings. Note that these error codes do not necessarily match the request sense block error codes. LED number 7 is the MSB.

00	No Error
01	No Index Detected
02	No Track Zero Detected
03	Illegal Logical Sector Address - beyond maximum sectors available for type of drive
04	Drive Not Selected (SA1000 only)
05	No Seek Complete Detected
06	ID Address Mark Not found (unformatted)
07	Data Address Mark Not found
08	Seek Error. R/Whead not positioned on correct track
09	Record Not found - found correct cylinder and head but not sector
0A	ID ECC or CRC error (uncorrectable)
0B	DMA Timeout Error - no Host acknowledge within 256 μsec after request
0C	Invalid Command Received from Host
0D	Incorrect Data Address Mark
0E	Incorrect ID Address Mark
0F	Incorrect Cylinder Address
10	Incorrect Sector Address
11	Incorrect Head Address
12	Uncorrectable Data Field ECC or CRC error
13	Correctable Data Field ECC error
14	Drive Not Ready
15	Write Fault (SA1000 only)
16	Spare
17	Write Protected (SA800/850 only)
18	RAM Diagnostic Error
19, -1F	Spare
20	Parity Error
21	Bad Sector found - a sector within a track that has been flagged bad has been found
22	Invalid function for this drive type.
81	Multiple Hard Disks Selected. Reset to clear condition.

9.0 CONTROLLER OPTION SELECTION

9.1 PARITY SELECT JUMPERS

Odd parity may be used by the Host system for data integrity verification. The controller will always output odd parity to the Host system.

Odd parity checking by the controller may be allowed or inhibited by moving a 3 position jumper located near the J6 Host connector (see Figure 10). With jumper at position A + B the controller will test for odd parity on all data input to the controller (normally shipped in this position). With jumper at position B + C the controller will not check for parity.

9.2 DRIVE TYPE SELECTION DIPSWITCH

The dipswitch settings for various types of drives for the SA1403 are shown below:

LOCATION: 3D

SWITCH BITS FIELD DEFINITION	8 7	6 5	4 3	2 1	
	LUN 0 DRIVE TYPE	LUN 1 DRIVE TYPE	LUN 2 DRIVE TYPE	LUN 3 DRIVE TYPE	OFF ON

SWITCH SETTINGS		DRIVE DESCRIPTION	TRACK FORMAT
EVEN	ODD		
on	on	SA1002	2 HEADS, 256 CYLINDERS
on	off	SA1004	4 HEADS, 256 CYLINDERS
off	on	SA850	2 HEADS, 77 CYLINDERS
off	off	SA800	1 HEAD, 77 CYLINDERS

All drives are 32 sector/track, 256 bytes/sector, MFM

EXAMPLE LOCATION: 3D

8 7	6 5	4 3	2 1	
LUN 0 DRIVE TYPE	LUN 1 DRIVE TYPE	LUN 2 DRIVE TYPE	LUN 3 DRIVE TYPE	OFF ON
ON ON	OFF ON	ON OFF	OFF OFF	

DRIVE 0 IS SET UP FOR SA1002
DRIVE 1 IS SET UP FOR SA850
DRIVE 2 IS SET UP FOR SA1004
DRIVE IS SET UP FOR SA800

10.0 TRACK FORMAT DESCRIPTION

10.1 SECTOR FORMAT

The 32 sector format employs MFM encoding on all tracks of the SA1000. The SA1403 controller also uses this format for the floppy disk drives. This format yields 32 sectors of 256 bytes per sector. Figure 9 shows the 32 sector format.

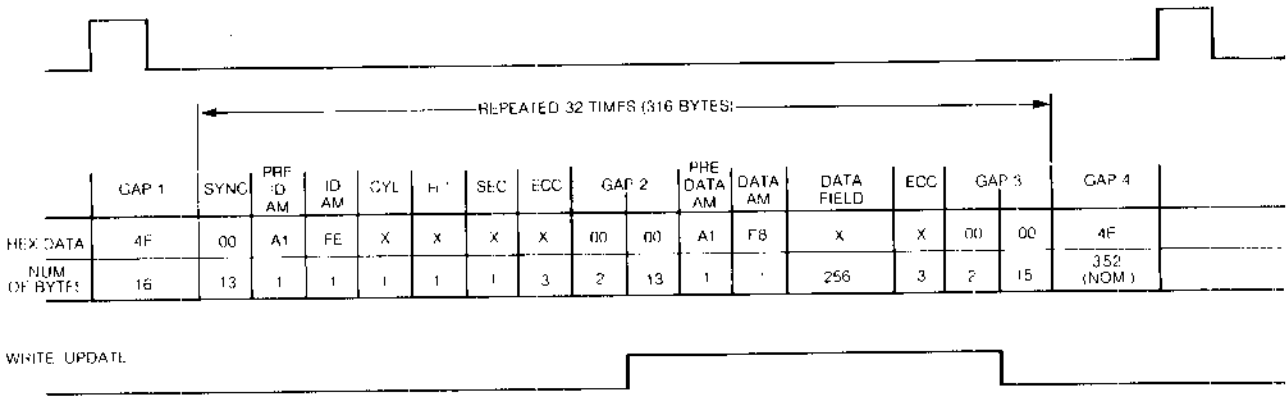


FIGURE 9. 32 SECTOR FORMAT

11.0 DRIVE JUMPER SETTINGS

11.1 JUMPER SETTINGS FOR SA800/801 FLOPPY

The following information is contained in the SA800/801 Diskette Storage Drive OEM Manual, Shugart Associates.

Jumper Name	Function (Enabled if Jumper Installed)
A	Install enable DRSEL to drive selection
B	Install, Head Load on Drive Select
C	Remove, Drive Select loads heads
D	Remove, In Use to LED is disabled
DC	Remove, Disable Disk Change to return to controller
DS	Install enable stepper on Drive Select
DS1-4	Install one only, DS1 = LUN 0 (Drive Select)
HL	Remove, Head Load on Drive Select
L	Jumper for -5V (remove for -15V), controller requires -5V only
T1	Remove, Head Load terminator
T2	Install, Pullup for Drive Select lines
T3	Install, Direction terminator
T4	Install, Step terminator
T5	Install, Write Data terminator
T6	Install, Write Gate terminator
X	Install, Head Load Enable
Y	Remove, Disable Hdld from driving LED
Z	Install drive select drives in use LED
800	Install, enables 800 index only operation
801	Remove, disables 801 mode operation

11.2 JUMPER SETTINGS FOR SA850/851 FLOPPY

Jumper Name	Function (Enabled if Jumper Installed)

Controller is compatible with the factory jumper configuration. (See SA850/851 OEM Manual).

Note: 850/851 select must be on 850.

11.3 JUMPER SETTINGS FOR SA1000 WINCHESTER

Jumper Name	Function (Enabled if Jumper Installed)

Controller is compatible with the factory jumper configuration. (See SA1000 OEM Manual).

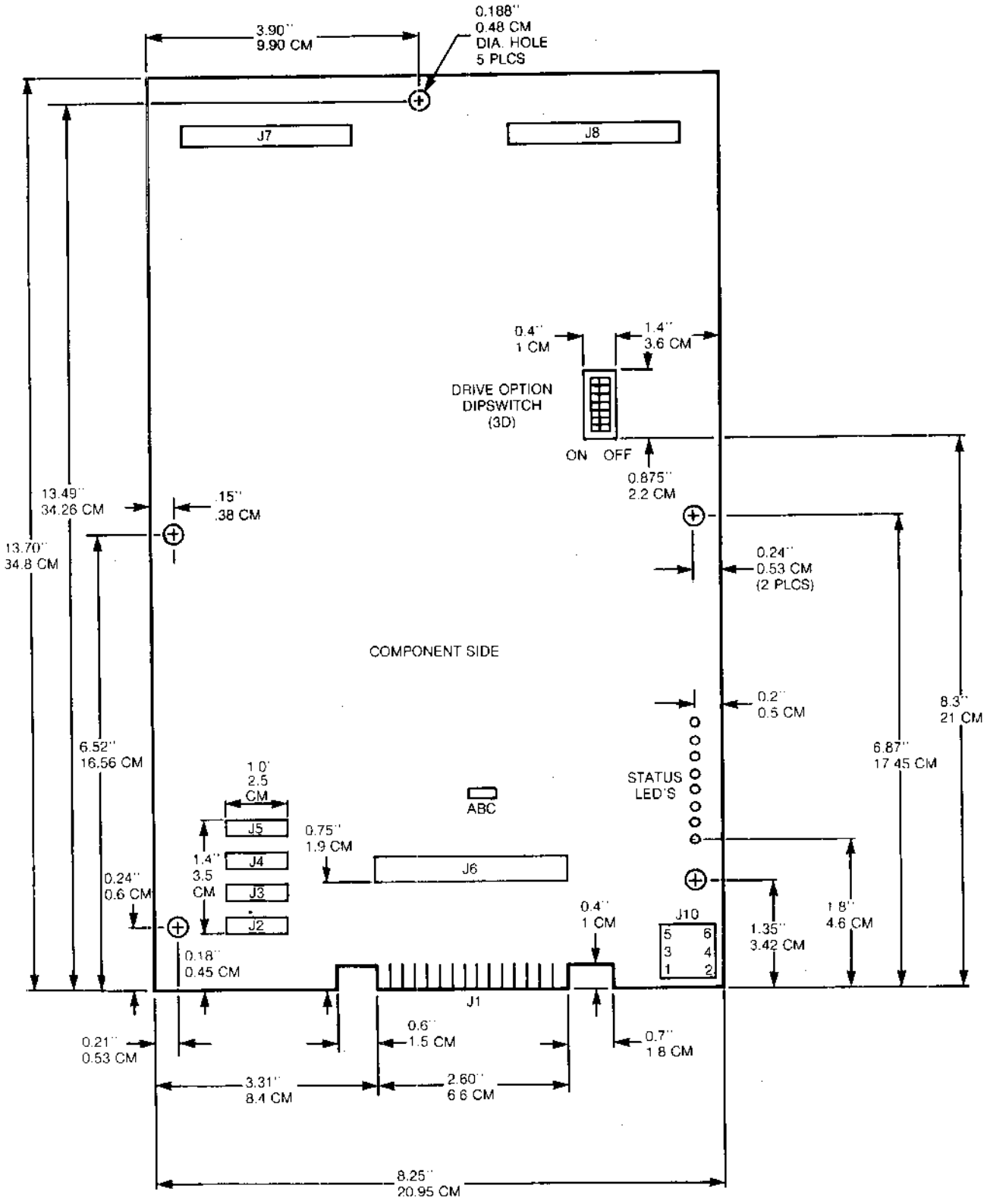


FIGURE 10. SA1403 DIMENSIONAL DIAGRAM

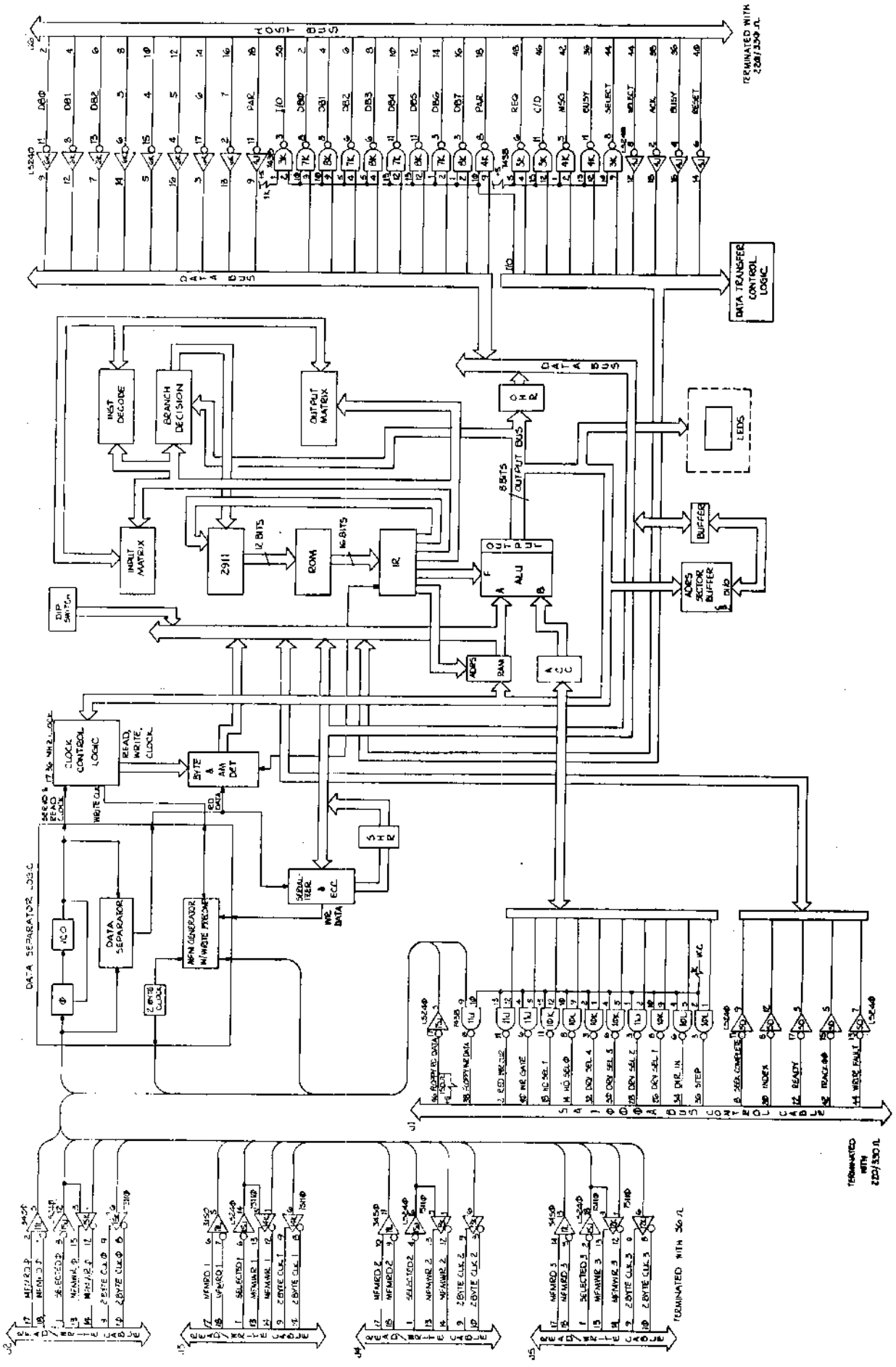


FIGURE 11. SA1403 FUNCTIONAL BLOCK DIAGRAM

APPENDIX A

OPTIONAL DIAGNOSTIC FIRMWARE
SA1403 DISK CONTROLLER

Optional diagnostic PROM's are available for the SA1403 disk controller to enable testing of the controller or the attached disk drives. When using the diagnostics, the controller/host interface cable is disconnected. The four PROM's are then plugged into IC positions 1A, 2A, 3A and 4A on the controller board.

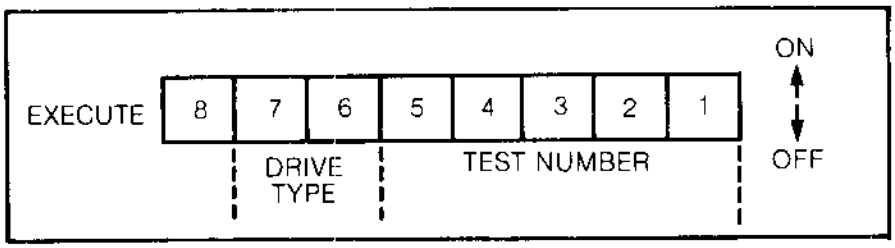
They are installed in the same manner as the customer PROM set in the order I, II, III, and IV.

The Part Number for the Prom set is 12652 and its identifying Prom number, I - IV, is 1K13 or U14.

DRIVE DIAGNOSTICS

In order to execute the drive diagnostics, the dipswitch on the controller board is used. The following table shows the diagnostic switch functions:

Dipswitch Location: 3D



EXECUTE SWITCH — SWITCH 8:

1. Before starting the diagnostics, be sure switch 8 is in the ON position before applying DC power to the controller board. Test selection and drive type selection can be performed only when switch 8 is ON.

2. To execute the diagnostic tests, turn switch 8 OFF.

3. To terminate the test execution, set switch 8 in the ON position. Test 02 (Format Entire Disk), once initiated, will format the entire disk and ignore switch 8 before accessing the switches again. The other tests will stop execution immediately when switch 8 is turned ON.

DRIVE TYPE AND LOGICAL UNIT NUMBER SET-UP — SWITCHES 7 & 6:

Switches 7 and 6 are used to define the disk drive type. A logical unit number (LUN) is assigned according to the drive type as indicated below:

	DRIVE TYPE	SWITCH SETTING SWITCH 7	SWITCH 6	LUN
SA1403 CONTROLLER	SA800/850	OFF	ON	0
	SA1002	ON	ON	1
	SA1004	ON	OFF	1

TEST NUMBER SWITCHES — SWITCHES 5 THROUGH 1

Switch 5 is the most significant switch.
Switch 1 is the least significant switch.
ON = 0 OFF = 1

Associated hexadecimal-numbered tests are described below. Because each test is a singular unit, the diagnostics may continue running even if an error is encountered. Errors will be given in the diagnostic status LED's (see ERROR DISPLAY section).

TEST OPTIONS

00 Check ECC Logic for Correctable Error - a pattern with a changed bit is written on sector 0, head 0, cylinder 0 and then read back. The controller should correct the error and enable the status LED's to show a correctable data error.

01 Check ECC Logic for Uncorrectable Error - a pattern is written on sector 0, head 0, cylinder 0 and then read back with multiple errors (more than 4 in burst or 2 or more bits spaced greater than 4 bits apart). The controller should display an uncorrectable data error to the status LED's.

Tests 00 and 01 verify the ability of the ECC logic to detect and correct data errors.

Note: Test 0A (Write Sequential) *must* be executed after executing tests 00 and 01 to avoid getting a data error during tests 07 (Sequential Read) and 08 (Random Read).

02 Format Entire Disk - formats all cylinders with hex 6C data pattern in the data fields.

03 Format Innermost Track - same as test 02, except only the innermost track will be formatted.

04 Format Outermost Track - same as test 02, except only track 0 will be formatted.

Tests 02 - 04 are write only, without verify. The controller will keep the write gate asserted for the entire track. Format begins upon the detection of Index. The interleave factor is set at 1. Since these tests begin at a known point, Index, they are recommended for debugging write problems.

05 Seek Incremental Cylinder Command - sequentially seeks one cylinder at a time from 0 to innermost track; does a seek to cylinder 0 and repeats the test.

Test 05 performs an unverified seek, no read or write. The seek is performed in buffered step mode.

06 Read Command (innermost track) - reads all sectors on innermost track and checks for correct ECC in ID and data fields.

07 Read Command (sequential cylinders) - same as test 06, except all sectors of the entire disk are read sequentially.

08 Read Command (random cylinder) - same as test 06, except all cylinders are read randomly.

09 Write Command (innermost track) - writes all sectors of innermost track filling data fields with hex 6C data pattern.

0A Write Command (sequential) - same as test 09, except all cylinders are written sequentially.

0B Write Command (random) - same as test 09, except all cylinders are written randomly.

0C Write/Read Command (innermost track) - writes all sectors of innermost track filling data fields with incrementing data patterns and then reading back the information, checking for ECC errors and comparing the data.

0D Write/Read Command (sequential cylinder) - same as test 0C, except all cylinders are tested sequentially.

0E Write/Read Command (random cyliner) - same as test 0C, except all cylinders are tested randomly.

0F Recal Command - recalibrates the heads to cylinder 0.

Test 0F issues one step pulse at a time outward until track 0 is encountered.

10 Check Innermost Track Format - checks ID fields for the innermost track.

11 Check Outermost Track Format - checks ID fields for cylinder 0.

Tests 10 and 11 are read only. The check tests are best suited to diagnose readback problems. The controller seeks to the specified track and verifies the format for the entire track. The sequence of the test is as follows: First, the controller seeks to the specified track and waits for the Index pulse. The read gate is then turned on to verify the ID field for correct cylinder, head, and sector address and to check the ID ECC for the first sector of the track (tracks must be formatted with interleave factor 1). The other sectors are then verified after each sector pulse detected. Upon detection of an error, the controller will display the error in the LED's and restart the test.

12 - 18 Not Applicable.

19 Random Seek (not read/write) - same as test 05.

1A Read Outermost Track - same as test 06.

1B Write Outermost Track - same as test 09.

1C Write/Read Outermost Track - same as test 0C.

NOTES:

1. Floppy drive can only be used with tests 02 - 0F, 19 - 1C.
2. The step rate is approximately 100μs.
3. When a test is started, the controller issues a recalibrate command before initiating the particular test. This insures that the read/write heads are over track 0.

ERROR DISPLAY

Any errors uncovered by the controller during the performance of selected tests will be reported via the LED's according to the error codes listed below. Once the controller detects an error, the error display will maintain the error indication even if subsequent tests are performed correctly. In this way, the controller can be left running for long periods of time. However, only the last error will be displayed on the LED's. To reset the error display, stop the test and start again.

Error Code (HEX, DSO is LSB)	Interpretation
01	No index
02	No track 00
03	Illegal disk address
04	Drive not selected
05	No seek complete
06	No ID address mark (possible unformatted tracks)
07	No data address mark
08	Seek error
09	Sector not found
0A	ID ECC error
0B	No host acknowledge
0C	Invalid command
0D	Incorrect data mark
0E	Incorrect ID mark (format error)
0F	Incorrect cylinder (format error)
10	Incorrect sector address
11	Incorrect head address
12	Uncorrectable data error
13	Correctable data error
14	Drive not ready
15	Write fault (write protected on floppies)
16	Bad track flag set
17	Write protected
18	RAM diagnostic error
19 - 1F	Not used
20	Parity error from host adaptor. If this error occurs, the host adaptor has a fault in the parity generation circuitry.
21	Bad block detected from drive
22	Invalid function for this drive type

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