SA1400 Controller OEM Manual

Shugart

TABLE OF CONTENTS

1.1.3 SA1404 D

4.2.9 DATA BUS BITS 0-7 (DB)

LIST OF ILLUSTRATIONS

SA1400 SERIES DISK CONTROLLER

OEM MANUAL

1.0 INTRODUCTION

The SA1400 series disk controller is a microprocessor based controller which is capable of controlling Shugart SA4000/4100 series 14 inch Winchester disk drives, SA1000 series 8 inch Winchester disk drives, and SA800 or SA850 8 inch floppy disk drives.

Three models of the SA1400 disk controller will be discussed in this manual. Refer to table 1 for an overview of the features of each model.

1.1 CONTROLLER MODEL FEATURES

1.1.1 SA1403

The SA1403 controller will control up to 4 disk drives. The drives can be any combination of SA1000 series 8 inch Winchester disk drives or SA800 or SA850 8 inch floppy disk drives. A 32 sector format is utilized for both SA1000 and SA800 or SA850 disk drives (see section 12.2).

1.1.2 SA1403 D

The SA1403 D controller is the same as the SA1403 except that only one model of 8 inch floppy disk drive may be combined with the SA1000 disk drive. SA800 and SA850 floppy disk drives may not be combined on the same controller.

The SA1403 D controller employs a 32 sector format for the SA1000 (see section 12.2) and a 26 sector IBM compatable format for the floppy disk drives (see section 12.1).

1.1.4 SA1404 D

The SA1404 D controller will control up to 4 disk drives. The drives can be any combination of SA4000/SA4100 series 14 inch Winchester disk drives or SA800 or SA850 8 inch floppy disk drives. However, only one model of 8 inch floppy disk may be combined with the SA4000 disk drives. SA800 and SA850 disk drives may not be combined on the same controller. The floppy disk format employed is a 26 sector IBM compatible format (see section 12.1).

FEATURES	MODEL DESIGNATION 1403	1403D	1404D
CONTROLS SA1000 SERIES 8'' WINCHESTER DRIVES	X	X	
CONTROLS SA4000 SERIES 14'' WINCHESTER DRIVES			X
CONTROLS SA800/SA850 SERIES 8'' FLOPPY DISK DRIVES	X	X	X
AUTOMATIC SEEK AND VERIFY	X	X	X
ERROR SENSING AND CORRECTION (ECC)	X	WINCHESTER ONLY	WINCHESTER ONLY
CYCLIC REDUNDANCY CHECK (CRC) - FLOPPY DISK ONLY		X	X
32 SECTORS × 256 BYTE FORMAT	X	WINCHESTER ONLY	
60 SECTORS × 256 BYTE FORMAT			WINCHESTER ONLY
26 SECTORS × 256 BYTE FORMAT (FLOPPY IBM SYSTEM 34)		FLOPPY ONLY	FLOPPY ONLY
CONTROL OF UP TO 4 DRIVES (ANY COMBINATION)	X	X	X
FULL SECTOR BUFFER	X	X	X
SECTOR INTERLEAVE CAPABILITY	X	X	X
OVERLAPPED SEEK CAPABILITY	X	X	X
ODD PARITY CHECKING	X	X	X
MULTIPLE HOST I/O CAPABILITY (PRIMITIVE)	X	X	X
LOGICAL SECTOR ADDRESSING	X	X	X

TABLE 1. SA1400 SERIES CONTROLLER FEATURE TABLE

1.2 ADDITIONAL FEATURES

A) All models utilize error correction code (ECC) which will handle burst errors up to 4 bits in length. The SA1403 D and SA1404 D controller utilize cyclic redundancy check (CRC) for the floppy disk to maintain IBM compatability.

B) A full sector buffer is used to allow asynchronous DMA data transfers.

C) Sector interleave capability with 16 possible interleave codes.

D) Overlapped seek is possible on up to 4 drives.

E) All controller models will output odd parity. If enabled, the controller will test input data for odd parity.

F) Multiple Host Interface capability.

G) Logical sector addressing. Sectors are addressed sequentially beginning at cylinder 0, head 0, sector 0 (or sector 1 for IBM floppy). All heads are read sequentially up to the maximum number. Then the next sequential cylinder is accessed beginning with head 0. All head switching and seeks are transparent to the host system.

1.3 TRACK FORMATS AND CAPACITY

Four track formats are utilized by the SA1400 series controllers:

A) 32 sectors of 256 bytes per sector (SA1000 and SA800/SA850 only).

B) 60 sectors of 256 bytes per sector (SA4000/4100 only).

C) 26 sectors of 256 bytes per sector (SA850 only).

D) 26 sectors of 128 bytes per sector (SA800 and track 0 of SA850 only).

Refer to table 2 for the format/capacity relationships. See section 12 for format description.

	32 SECTOR	60 SECTOR	26 SECTOR
SA800	2463		2001
SA850	4927		4003
SA1002	16383		
SA1004	32767		
SA4004		48479	
SA4008		96959	
SA4100		193919	

TABLE 2. FORMAT/CAPACITY RELATIONSHIP
MAXIMUM LOGICAL SECTOR ADDRESS SHOWN

***NOTE:** Fixed Head Option (if applicable) will be addressed directly above the maximum movable head address. Fixed heads will add 480 available sectors to the maximum logical address.

EXAMPLE:
SA4004 Logical Address = 0 to 48479
Fixed Head Address = 48480 to 48959

1.4 FAULT DETECTION

Three classes of fault detection are provided for fault diagnosis:

1) Disk related faults.

2) Controller related faults.

3) Host command or I/O timing faults.

Fault detection is available from the interface as a status message and is also visibly displayed on a row of status LED's on the controller P.C.B.

1.5 OPTIONAL DIAGNOSTIC FIRMWARE

A set of diagnostic PROM's are available to allow stand alone diagnostic testing of both drive and controller. Contact Shugart Technical Support Department for futher information.

2.0 SPECIFICATION SUMMARY

2.1 ENVIRONMENTAL LIMITS:

	Operating	Storage
Temperature F/C	32°/0° to 131°/55°	-40°/-40° to 167°/75°
Relative Humidity @ 40°F Wet Bulb non-condensing	10% to 95%	10% to 95%
Altitude	Sea level to 10,000ft	Sea level to 15,000ft

2.2 POWER REQUIREMENTS

Three power supply voltages are required for the SA1400 series controllers. The maximum current requirements are as follows:

+5VDC ± 5% at 4.6 Amps

-5VDC ± 5% at 0.5 Amps

+24VDC ± 10% at 0.1 Amps

Power is appled to the SA1400 series controller via J10 which is a 6 pin AMP connector. The recommended mating connector is an AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. The J10 pins are labeled on the connector. Figure 1 shows the pin assignments.

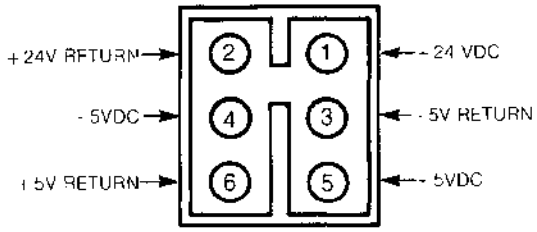


FIGURE 1. J10 DC POWER CONNECTOR

2.3 PHYSICAL PARAMETERS

Refer to figures 15 thru 17 for dimensional layout. The physical parameters are as follows:

Length:	13.7 inches (34.8cm)
Width:	8.25 inches (21cm)
Height:	0.5 inches (1.3cm)
Weight:	1.12 lbs (0.5Kg)

3.0 CONTROLLER TO DISK DRIVE INTERFACE

3.1 SA1403 AND SA1403 D DISK DRIVE INTERFACE

Shugart SA1000 and SA800/SA850 disk drives are interfaced to the controller via J1, J2, J3, J4, and J5. Refer to Figure 2 for connection block diagram.

J1 is a 50 pin edge type connector which connects all drives in a daisy chain configuration. This connector carries control and data information for the floppy disk drives and control information only for the SA1000 disk drive. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J1 is a 3M Scotchflex P/N 3415-0001.

J2 through J5 are 20 pin socket type connectors used to radially connect the SA1000 data lines to the controller. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J2 through J5 is a 3M Scotchflex P/N 3421-3000. Figure 3 shows the pinouts for J1 and J2 through J5.

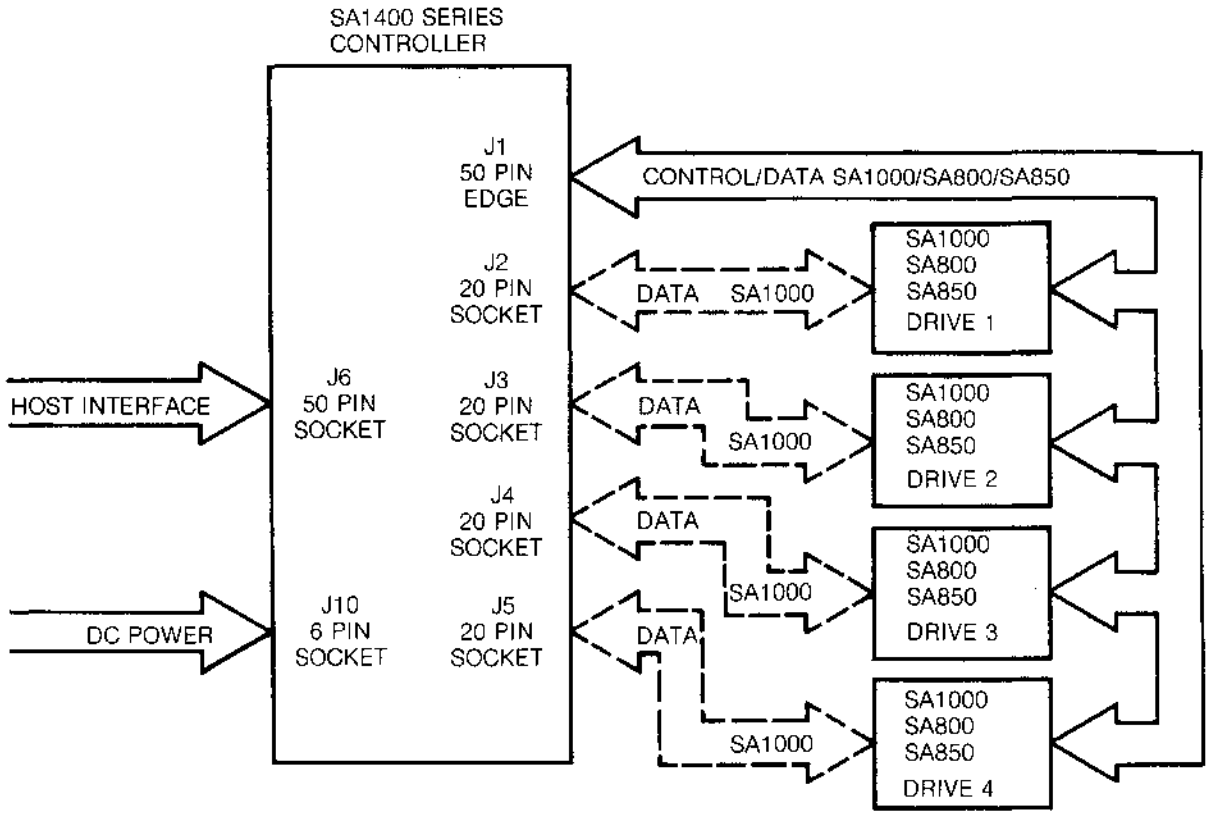


FIGURE 2. SA1403, SA1403D INTERCONNECT DIAGRAM

J1		SA1000	SA800	SA850
1	2	- IW SWITCH		- IW SWITCH
	4			
	6			
	8	- SEEK COMPLETE		
	10			- TWO SIDED
	12			
	14	- HEAD SEL 2^0		- SIDE SEL
	16			
	18	- HEAD SEL 2^1	- HEAD LOAD	- HEAD LOAD
	20	- INDEX	- INDEX	- INDEX
	22	- READY	- READY	- READY
	24			
	26	- DRIVE SEL 1	- DRIVE SEL 1	- DRIVE SEL 1
	28	- DRIVE SEL 2	- DRIVE SEL 2	- DRIVE SEL 2
	30	- DRIVE SEL 3	- DRIVE SEL 3	- DRIVE SEL 3
	32	- DRIVE SEL 4	- DRIVE SEL 4	- DRIVE SEL 4
	34	- DIRECTION SEL	- DIRECTION SEL	- DIRECTION SEL
	36	- STEP	- STEP	- STEP
	38		- WRITE DATA	- WRITE DATA
	40	- WRITE GATE	- WRITE GATE	- WRITE GATE
	42	- TRACK 000	- TRACK 00	- TRACK 00
	44	- WRITE FAULT	- WRITE PROTECT	- WRITE PROTECT
	46		- READ DATA	- READ DATA
	48			
49	50			

J2 THROUGH J5

- DRIVE SELECTED	1	2	GROUND
	3	4	
	5	6	
	7	8	GROUND
+ TIMING CLOCK	9	10	- TIMING CLOCK
GROUND	11	12	GROUND
+ MFM WRITE DATA	13	14	- MFM WRITE DATA
GROUND	15	16	GROUND
+ MFM READ DATA	17	18	- MFM READ DATA
GROUND	19	20	GROUND

FIGURE 3. SA1403, SA1403D DRIVE CONNECTOR PINOUTS

3.1.1 CABLE TERMINATION

The last physical drive at the end of the J1 (50 pin) cable must be properly terminated. Termination networks are provided on the drives (refer to SA1000, SA800, or SA850 OEM manuals for location of termination networks). Termination networks must be removed from all drives except the last drive on the cable to avoid multiple termination.

3.2 SA1404 D DISK DRIVE INTERFACE

Shugart SA4000/4100 and SA800/SA850 disk drives are interfaced to the controller via J1, J2, J3, J4, J5 and J9. Refer to figure 4 for interconnection block diagram.

J1 is a 50 pin edge type connector which connects the floppy disk drives in a daisy chain configuration. This connector carries control and data information for the SA800 or SA850 floppy disk drives. Maximum cable length should not exceed 20 feet (6 meters). The recommended mating connector for J1 is a 3M Scotchflex P/N 3415-0001.

J2 through J5 are 20 pin socket type connectors used to radially connect the SA4000/4100 data lines to the controller. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J2 through J5 is a 3M Scotchflex P/N 3421-3000.

J9 is a 50 pin edge type connector which connects the SA4000/4100 disk drives in a daisy chain configuration. This connector carries control information for the SA4000/4100 disk drives. Maximum cable length should not exceed 20 feet (6 meters). The recommended mating connector for J9 is a 3M Scotchflex P/N 3415-0001. Figure 5 shows the pinouts for J1, J2 through J5, and J9.

3.2.1 CABLE TERMINATION

The last physical drive at the end of the J1 cable and the J9 cable must be properly terminated. Termination networks are provided on the drives (refer to SA4000, SA4100, SA800 or SA850 OEM manuals for location of termination networks). Termination networks must be removed from all drives except the last drive on the cable(s) to avoid multiple termination.

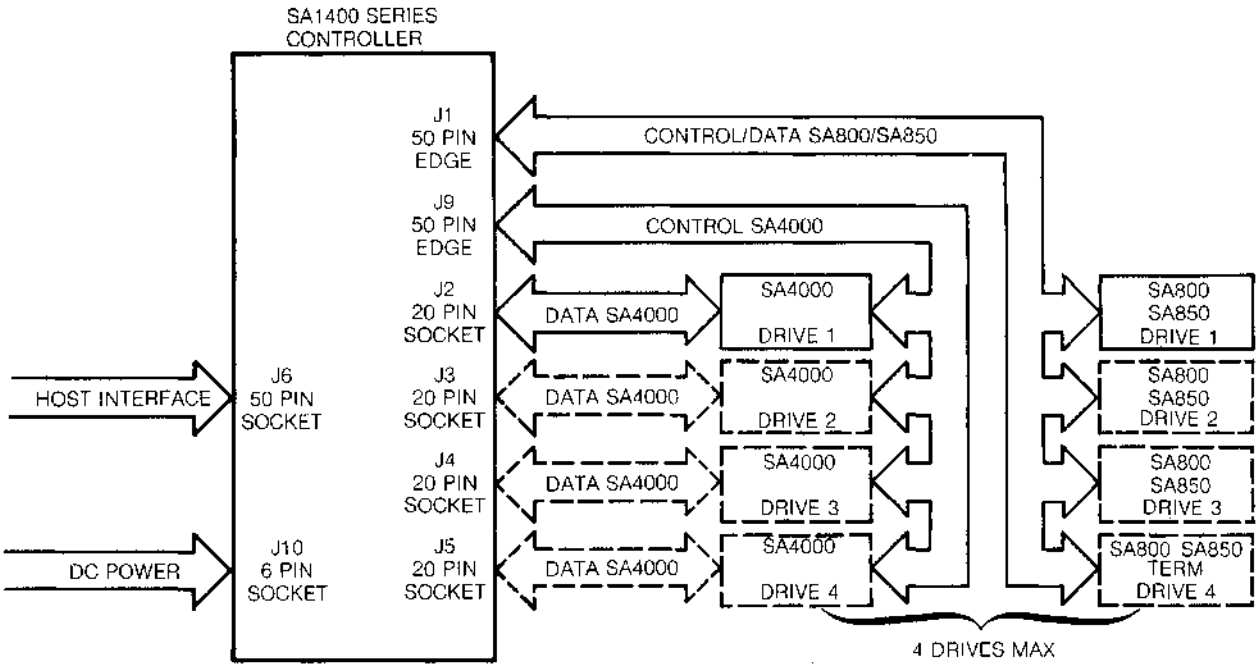


FIGURE 4. SA1404D INTERCONNECT DIAGRAM

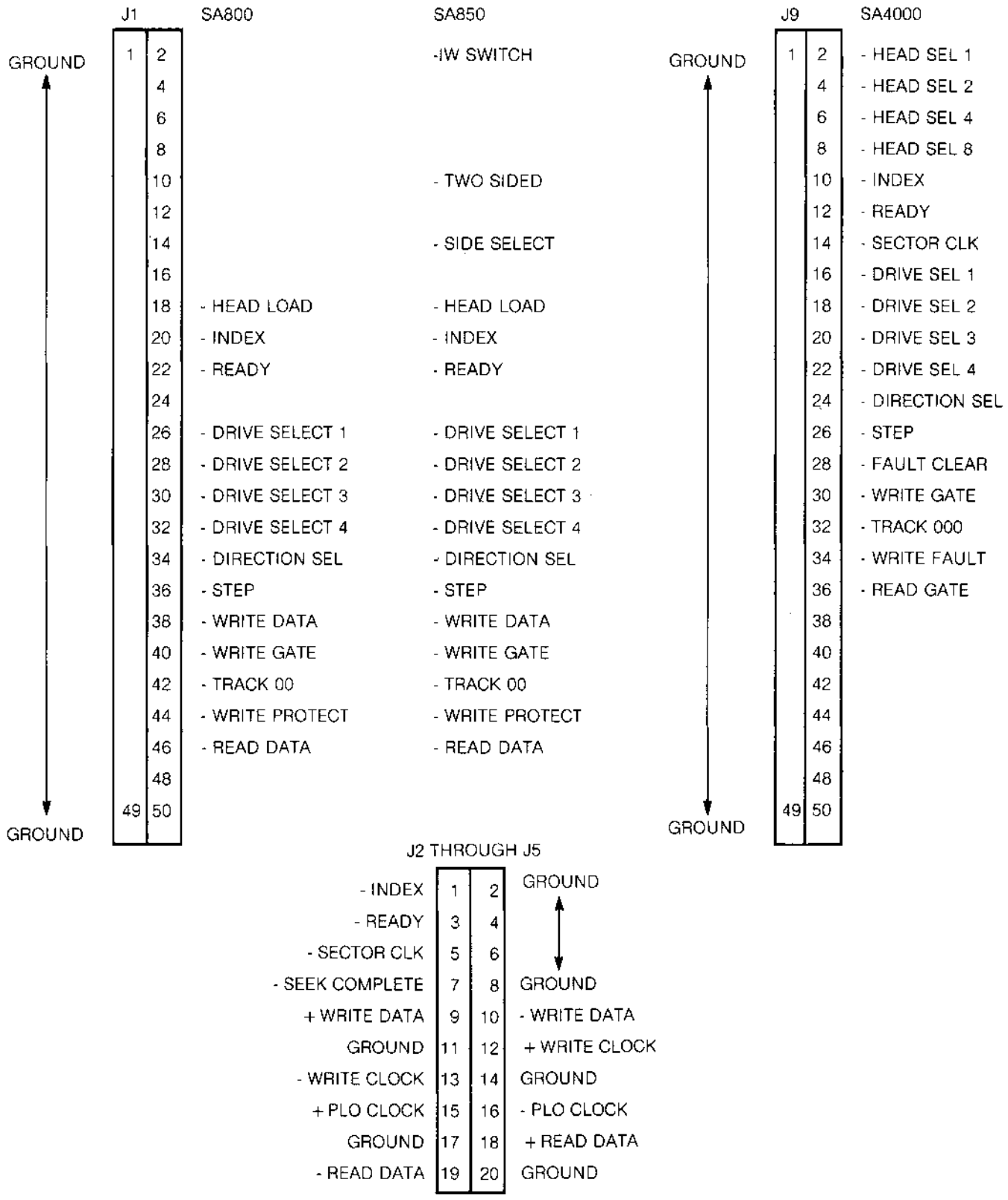


FIGURE 5. SA1404D DRIVE CONNECTOR PINOUTS

4.0 HOST CPU INTERFACE

The SA1400 series controller interface is a general purpose 8 bit parallel DMA type which is capable of interfacing with up to 7 Host CPU "Adapters".

The Host CPU is interfaced to the controller via connector J6. J6 is a 50 pin socket type connector. The recommended mating connector for J6 is a 3M Scotchflex P/N 3425-3000. The J6 interface cable should not exceed 20 feet (6 meters).

4.1 HOST CPU ELECTRICAL INTERFACE

All Host CPU interface signals are negative true. The signals are "Asserted" at 0 VDC to 0.4 VDC. The signals are "Deasserted" or inactive at 2.5 VDC to 5.25 VDC.

4.1.1 HOST CPU INTERFACE TERMINATION

All Host CPU interface timings are terminated with a 220/330 ohm network. The Host CPU adaptor should be terminated in a similar fashion (see Figure 6). In a multiple Host "adapter" system the adapter which is physically farthest from the controller should contain the termination network.

The devices driving the controller inputs should be open collector devices capable of sinking at least 48 milliamps to a voltage level of less than 0.5 VDC (7438 or equivalent).

The devices receiving the controller outputs should be of the SCHMITT trigger type to improve the noise margin (74LS240, 74LS14, or equivalent). The Host adaptor should not load the bus with more than 1 standard TTL input load per line.

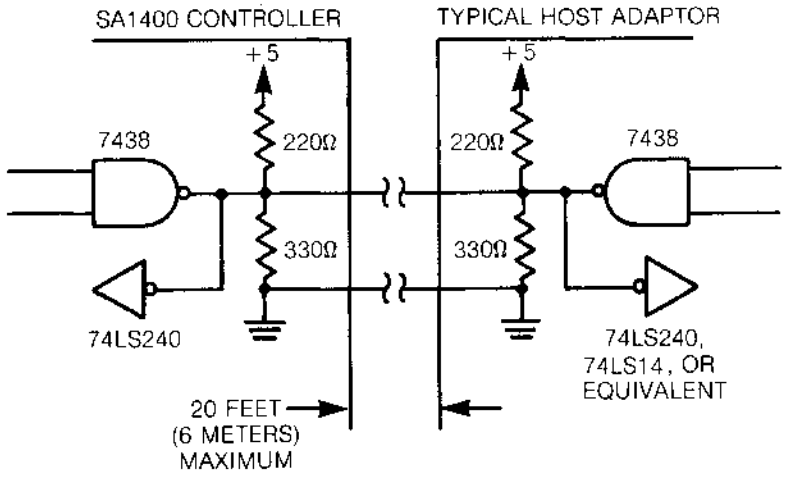
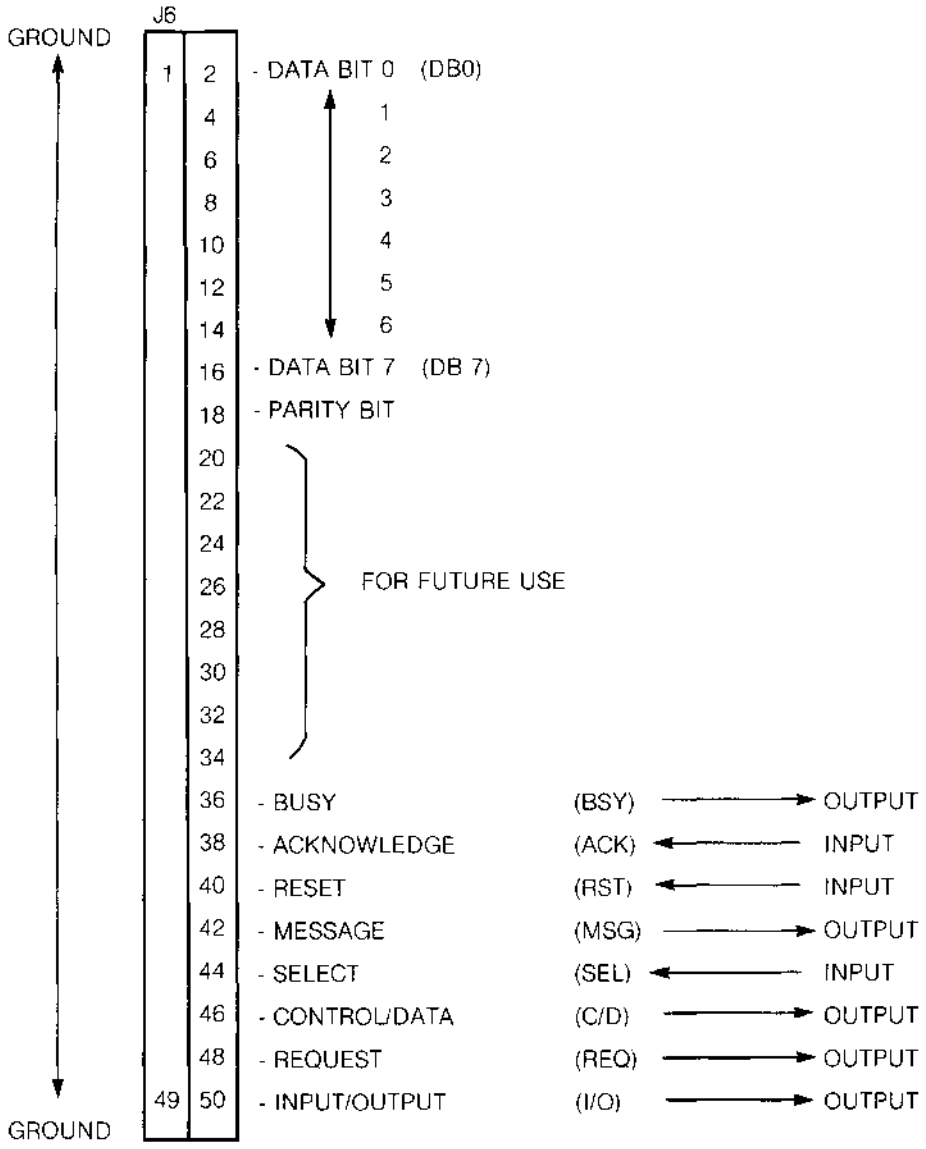


FIGURE 6. HOST ADAPTOR BUS TERMINATION



NOTE: ALL SIGNALS ARE TTL NEGATIVE TRUE

FIGURE 7. J6 HOST INTERFACE CONNECTOR PINOUT

4.2 HOST CPU SIGNAL INTERFACE

The Host CPU signals are interfaced via J6. See Figure 7 for J6 pinouts.

4.2.1 RESET (RST)

Assertion by the Host causes the controller to cease all operations and return to an idle condition. This signal is normally used during a power up sequence. A reset during a write operation would cause incorrect data to be written on the selected disk. The reset pulse should be at least 25 microseconds wide. The controller may take a maximum of 2 seconds to respond to the select sequence following deassertion of the RESET line.

4.2.2 SELECT (SEL)

Assertion by the Host along with the controllers address bit (data bit 0) causes the controller to be selected. The SELECT line must be deasserted when the controller asserts the BUSY line.

4.2.3 BUSY (BSY)

Assertion by the controller indicates that the controller has control of the interface bus and cannot be interupted.

4.2.4 CONTROL/DATA (C/D)

Assertion by the controller indicates that command or status information is to be transferred on the data bus while deassertion of this line indicates that data information is to be transferred on the data bus.

4.2.5 INPUT/OUTPUT (I/O)

Assertion by the controller indicates that information will be transferred to the Host from the controller. Deassertion indicates that information will be transferred to the controller from the Host.

4.2.6 REQUEST (REQ)

Assertion by the controller indicates that an 8 bit byte is to be transferred on the data bus. REQUEST is deasserted following the assertion of the Acknowledge line. If ACK is not asserted within 256 microseconds, the controller will terminate the operation and transfer a status message.

4.2.7 ACKNOWLEDGE (ACK)

Assertion by the Host indicates that data has been accepted by the Host or that data is ready to be transferred from the Host to the controller.

4.2.8 MESSAGE (MSG)

Assertion by the controller indicates that a status byte transfer has been accomplished. When MSG is asserted, REQ will be asserted in order to transfer an 8 bit byte of all zero's to indicate end of operation. When the REQ/ACK handshake is complete the controller will deassert all interface signal lines and return to an IDLE state.

DATA BUS BITS 0-7 (DB)

These bidirectional data lines are used to transfer 8 bit parallel data to/from the Host adaptor. Bit 7 is most significant bit.

4.2.10 PARITY BIT

This bit is asserted to maintain odd parity on all data and status information transfered to the Host. If enabled, the controller will test for odd parity on all command and data information transfered to the controller (see section 11).

5.0 HOST INTERFACE PROTOCOL

There are 4 sequences required to initiate and complete a command to the SA1400 series controller:

1) Controller Selection Sequence

2) Command Transfer Sequence

3) Data Transfer Sequence

4) Status and Message Transfer Sequence

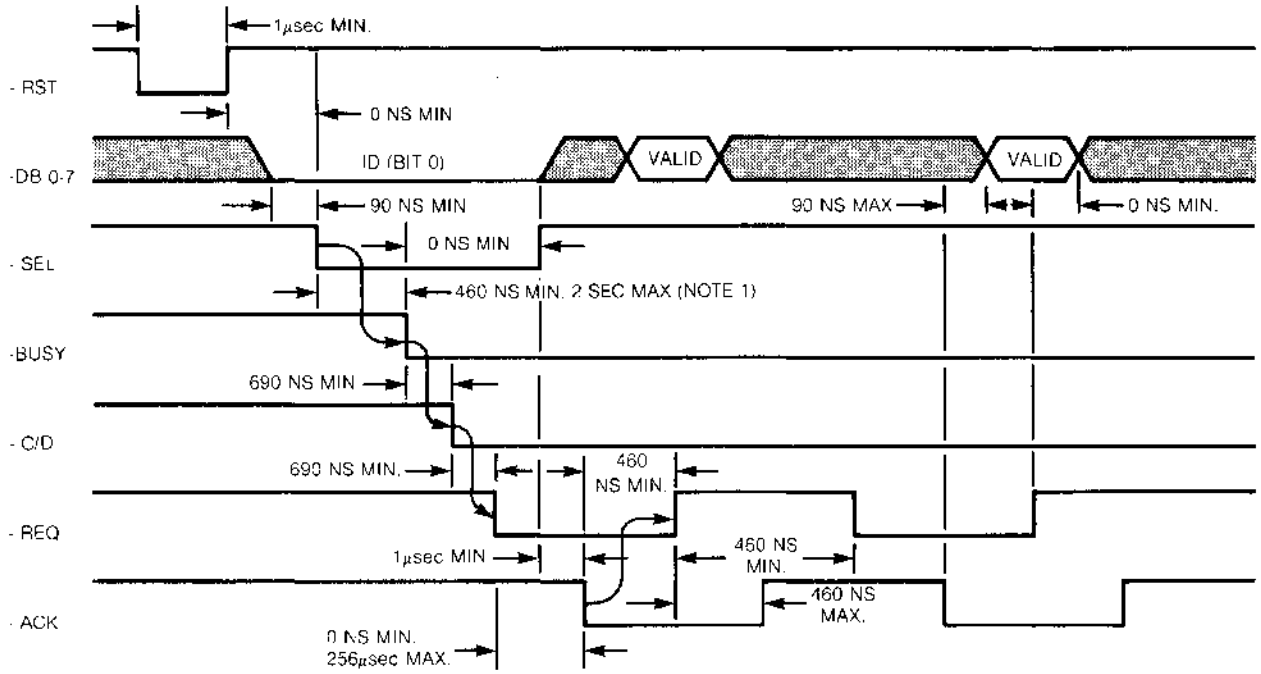
5.1 CONTROLLER SELECTION SEQUENCE

In order to gain the attention of the controller it is necessary to perform a selection sequence. Refer also to Figure 8.

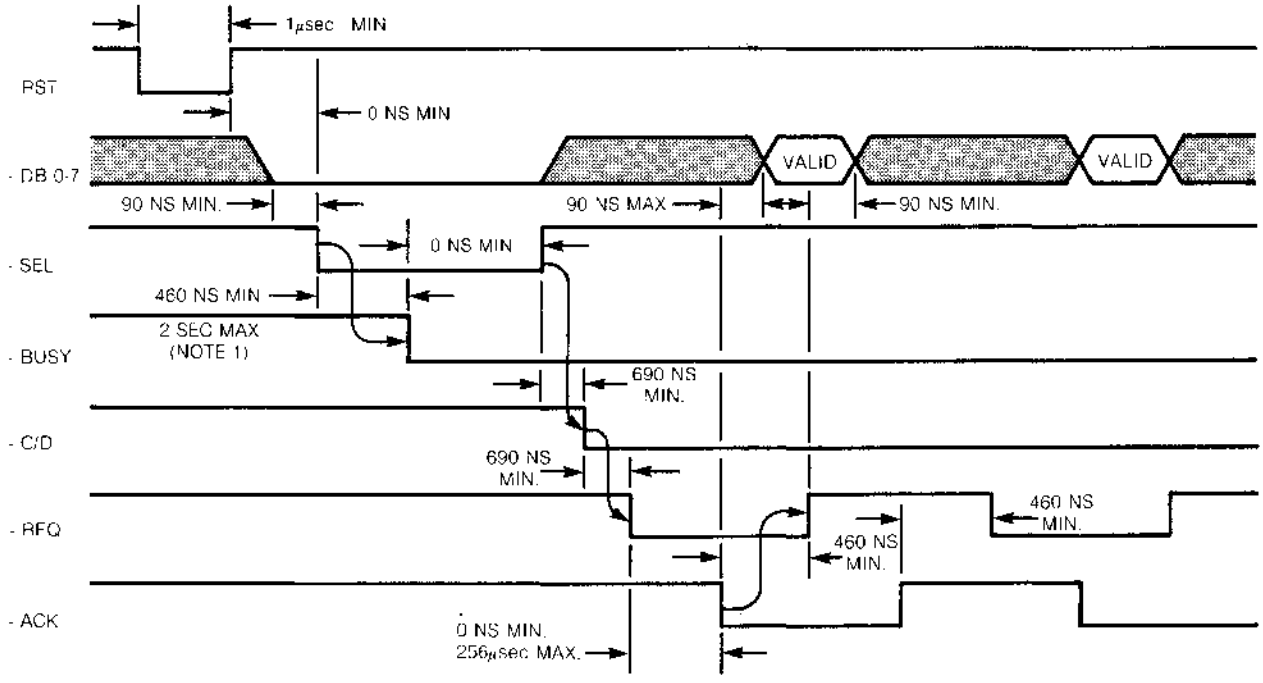
The Host must first test BSY to determine if the controller is available. If BSY and all other I/O lines are deasserted, the Host will assert data bit 0 (controller ID) and then assert SEL. The controller will then respond by asserting BSY. At this point the Host must deassert SEL and data bit 0. I/O will remain deasserted throughout the selection sequence.

5.2 COMMAND TRANSFER SEQUENCE

Following the selection sequence the controller will assert REQ (see Figure 8). The Host will then place the first byte of the command descriptor block (see section 6.0) on the data bus. The Host will then assert ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, the controller will abort the command transfer sequence and attempt to transfer a status byte - see section 5.4). The controller will respond by reading the byte on the data bus and then deasserting REQ. The Host then must deassert ACK to begin the next transfer REQ/ACK handshake. This handshake continues until all bytes of the command descriptor block have been transferred.



SELECT TIMING FOR SA1403
NOTE 1 - 2 SEC MAXIMUM AFTER RESET.



SELECT TIMING FOR SA1403D, SA1404D

FIGURE 8. SELECT SEQUENCE TIMING

5.3 DATA TRANSFER SEQUENCE

Following the command transfer sequence, the controller will respond in one of four ways:

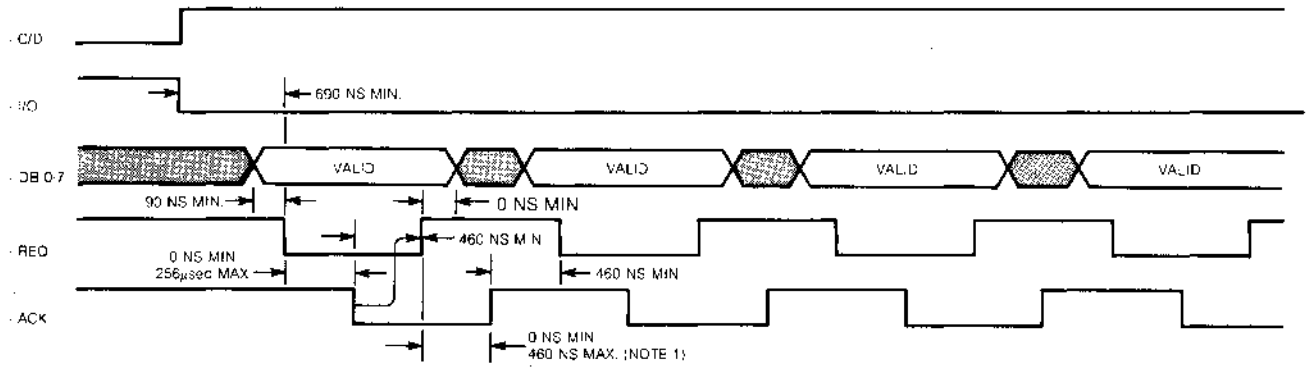
1) Begin seeking the drive.

2) Begin accepting write data from the Host.

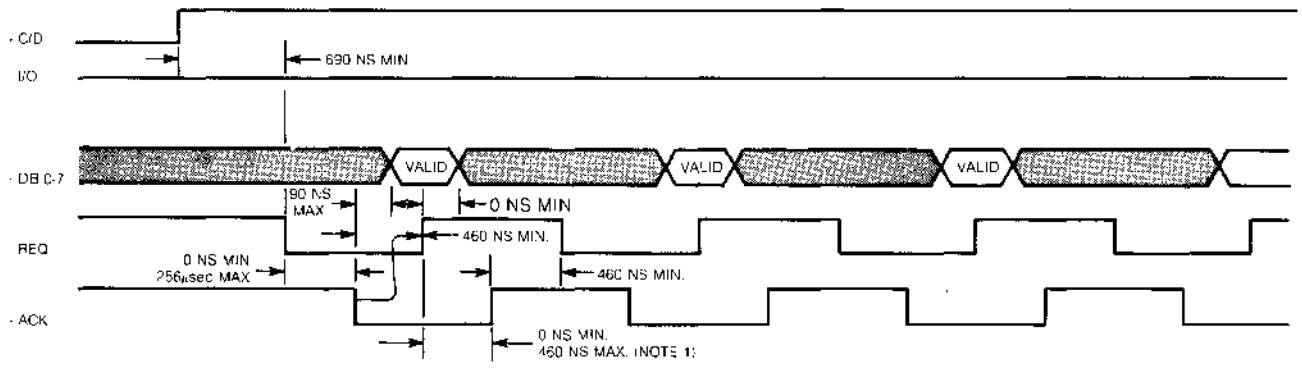
3) Begin transferring read data to the Host.

4) Return status to the Host.

If the command sent to the controller involves a data transfer (see Figure 9), the controller will deassert the C/D line to indicate a data transfer. If the data transfer is from the Host to the controller (write data) the I/O line will be deasserted. If the data transfer is from the controller to the Host (read data) the I/O line will be asserted. The controller will then set the REQ line to request a byte transfer. The Host will respond by transferring a byte across the data bus and then asserting ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, the controller will abort the data transfer sequence and attempt to transfer a status byte - see section 5.4). The Host will then deassert ACK and wait for the next assertion of REQ. This handshake continues until 256 bytes of data have been transferred.



READ DATA TRANSFER SEQUENCE (CONTROLLER TO HOST)



WRITE DATA TRANSFER SEQUENCE (HOST TO CONTROLLER)

NOTES:
1. 460 NS MAX. FOR SA1403. NO MAXIMUM FOR OTHER MODELS.

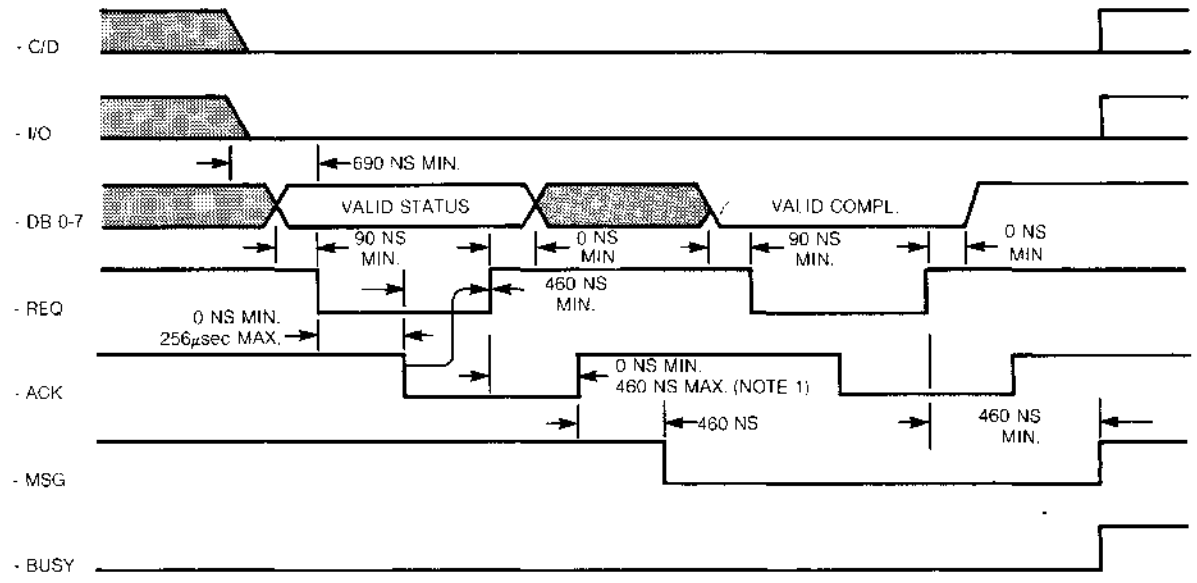
FIGURE 9. DATA TRANSFER SEQUENCE TIMING

5.4 STATUS AND MESSAGE TRANSFER SEQUENCE

Following a command transfer or data transfer, the controller will initiate a status byte and completion message transfer.

When a status byte transfer is required, the controller will assert C/D and I/O (see Figure 10). The controller will then assert REQ. The Host adaptor must then transfer the status byte on the data bus to the Host CPU and then assert ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, REQ will be deasserted. REQ will then be asserted again. This sequence will continue until ACK is asserted. The controller will then deassert REQ. The Host will then deassert ACK.

Following the status byte transfer, a completion message byte of all zero's will be transferred to indicate operation complete. The controller will assert the MSG line (along with I/O and C/D) and then assert REQ. The Host adaptor then may transfer the completion message byte on the data bus to the Host and assert ACK (if ACK is not asserted within 256 microseconds, the controller will deassert the MSG line and attempt to transfer a status byte). The controller will respond by deasserting REQ. The Host will then deassert ACK. At this point BSY and all other controller I/O lines will be deasserted and the controller will return to an IDLE condition awaiting the next selection sequence.



NOTES:
1. 460 NS MAXIMUM FOR SA1403. NO MAXIMUM FOR OTHER MODELS.

FIGURE 10. STATUS AND COMPLETION SEQUENCE TIMING

6.0 CONTROLLER COMMAND DESCRIPTOR BLOCK

Following the controller selection sequence the controller will request a command descriptor block (CDB) which, depending on the class of command, may be either 6 or 10 bytes in length. The first byte of the CDB contains the command class and the command operation code. The remaining bytes specify the drive logical unit number (LUN), logical sector address, number of sectors to be transferred or a destination device (Copy Command), and a control field byte.

Commands are categorized into four classes:

1) Class 0 - Utility, data transfer, and status commands.

2) Class 1 - Disk copy commands.

3) Class 2 thru 6 - Unused at this time.

4) Class 7 - Diagnostic commands.

Command Descriptor blocks for class 0 and class 7 commands are 6 bytes in length, and those for class 1 commands are 10 bytes in length (see Figure 11).

The controller will check all incoming command descriptor blocks for validity and will also check (if enabled) all CDB's and data for odd parity (see section 11). A parity error will cause an immedaite halt of the command or data transfer, terminating with a status byte transfer. This will not cause incorrect data to be written because the write does not occur until the sector buffer has been filled.

An error in the command structure will cause a status byte transfer to occur upon completion of the CDB transfer.

6.1 COMMAND DESCRIPTION (CLASS 0)

The following commands are listed by their respective hexadecimal operation codes:

Opcode	Command Description
00	Test Drive Ready - selects a particular drive and verifies that it is "ready". The ready conditon is indicated by the status byte. A not ready drive will cause bit 1 of the status byte to be set.
01	Recalibrate - positions the head(s) of the selected drive over track 00 and clears any fault conditions.

CLASS 0 AND 7 COMMAND DESCRIPTOR BLOCK

	MSB 7	6	5	4	3	2	1	LSB 0
BYTE #1	CLASS - NOTE 1			OPERATION CODE				
2	0	LUN		LOGICAL SECTOR ADRS 2 (MS)				
3	LOGICAL SECTOR ADRS 1							
4	LOGICAL SECTOR ADRS 0 (LS)							
5	NUMBER OF SECTORS/INTERLEAVE CODE							
6	CONTROL FIELD - NOTE 2							

CLASS 1 COMMAND DESCRIPTOR BLOCK

	MSB 7	6	5	4	3	2	1	LSB 0
BYTE #1	0	0	1	OPERATION CODE				
2	0	LUN (S)		LOGICAL SECTOR ADRS 2 (S)				
3	LOGICAL SECTOR ADRS 1 (S)							
4	LOGICAL SECTOR ADRS 0 (S) (LS)							
5	NUMBER OF SECTORS							
6	0	LUN (D)		LOGICAL SECTOR ADRS 2 (D)				
7	LOGICAL SECTOR ADRS 1 (D)							
8	LOGICAL SECTOR ADRS 0 (D)							
9	SPARE (SHOULD = 0)							
10	CONTROL FIELD - NOTE 2							

(S) = SOURCE DEVICE (D) = DESTINATION DEVICE

NOTES:

1. CLASS 0 = 000. CLASS 7 = 111.
2. THE CONTROL FIELD IS DEFINED AS FOLLOWS:

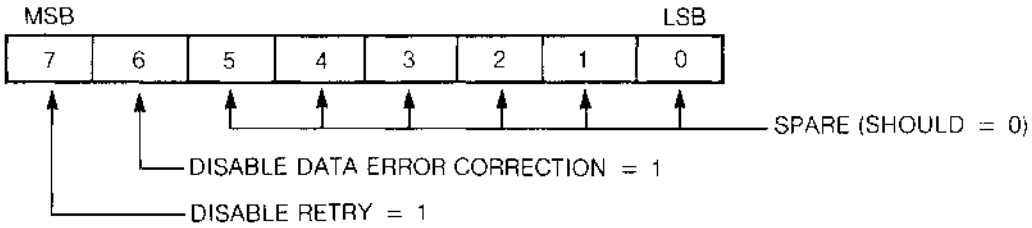


FIGURE 11. COMMAND DESCRIPTOR BLOCK MAP

02 Request Syndrome - returns two bytes to the Host system of error offset and syndrome for Host error correction capability (see Table 3). The first byte is the byte offset in the data field of the error location. The most significant 3 bits of the second byte point to the beginning of the error location. The least significant 4 bits of the second byte are the syndrome which is a data correction mark which is to be exclusive or'ed with the faulty data. This command is only valid if the automatic data correction has been disabled (see Figure 11).

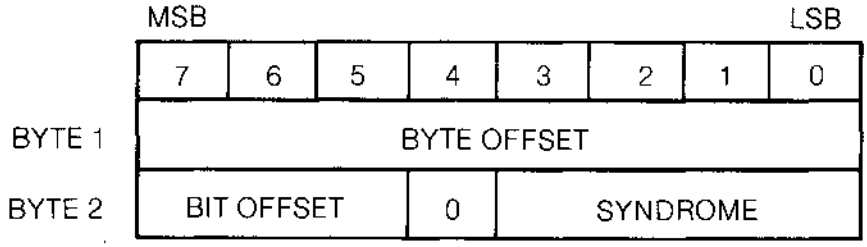


TABLE 3. REQUEST SYNDROME BLOCK

03 Request Sense - following an error, the Host may perform a request sense command for a more detailed error analysis. See section 8.0 for detailed description.

04 Format Drive - formats all cylinders with the ID fields set according to the specified interleave code (see section 10.) Data fields will contain a hexadecimal 6C data pattern.

05 Check Track Format - verifies correct ID fields and data sync marks for all sectors on a single data track. The data track is addressed via the logical sector address which may be any address within the desired track. SA4000/4100 fixed heads - see section 6.4.

06 Format Track - same as the Format Drive Command except that only one data track is formatted. The data track is addressed via the logical sector address which may be any address within the desired track. SA4000/4100 fixed heads - see section 6.4.

07 Format Bad Track - formats the specified track (or sector on SA4000/4100) with the bad track flag set in the ID field(s) (bit 7 of the Head Address Byte set). The track is addressed via the logical sector address which may be any address within the desired track (SA1000 or SA800/SA850).

08 Read - reads the designated number of sectors from the disk beginning with the logical sector address given in the command descriptor block. SA4000/4100 fixed heads - see section 6.4.

0A Write - writes the designated number of sectors to the disk beginning with the logical sector address given in the command descriptor block. SA4000/4100 fixed heads - see section 6.4.

0B Seek - a seek is performed to the logical sector address specified in the command descriptor block.

6.2 COMMAND DESCRIPTION (CLASS 1)

00 Copy Sector - copies the specified number of sectors from a source LUN to a destination LUN. Number of sectors transferred may be from 1 to 256. The completion status byte will indicate the source LUN. If an error occurs, a REQUEST SENSE command is issued to the source LUN. The sense bytes will indicate type of error for the appropriate LUN. SA4000/4100 fixed heads - see section 6.4.

6.3 COMMAND DESCRIPTION (CLASS 7)

00 Ram Diagnostic - performs a data pattern test on the controller internal buffer.

01 Write ECC - allows the Host system to write ECC bytes for verification of ECC logic. The controller will request 256 bytes of data from the Host. The Host will then write 253 bytes of data followed by 3 bytes of ECC. The controller will write 3 bytes of zero's at the beginning of the data field. The ECC should be computed assuming 3 bytes of zero's plus the remaining 253 bytes of user data. ECC logic is verified if no error occurs with a correct ECC and an error occurs with an incorrect ECC.

02 Read ID - this command will cause the ID field of the specified sector to be transfered to the Host. Six bytes are transfered: cylinder, head, sector, and three ECC bytes.

03 Drive Diagnostic - sector 0 of all tracks on the selected LUN are read. Then sector 0 of 256 randomly selected tracks are read.

6.4 SA4000/4100 FIXED HEAD ADDRESSING

The SA4000/4100 fixed head logical address is located at the next higher logical address beyond the maximum logical address of the movable heads (see Table 2).

A format drive command with a logical address set an any valid fixed head address will format all fixed heads.

The fixed heads will add an additional 480 (decimal) sectors to the maximum logical address.

Bit 7 of the first byte is a valid logical sector address bit (MSB) which indicates if the logical sector address bytes are valid for the type of error. If this bit = 0, the logical sector address may be ignored. Bit 6 is not used and will always = 0. Bits 4 and 5 denote the type of error encountered. Bits 0 through 3 denote the error code.

Bits 5 and 6 of the second byte are the LUN of the device where the error occured. Bit 7 will always = 0. Bits 0 through 4 are the high order 5 bits of the 21 bit logical sector address. Bit 4 is the most significant bit.

Bytes 3 and 4 are the low order 16 bits of the logical sector address. Bit 0 of byte 4 is the least significant bit.

	MSB							LSB
	7	6	5	4	3	2	1	0
BYTE 1	*	**	ERROR TYPE		ERROR CODE			
BYTE 2	**	LUN		LOGICAL SECTOR ADRS 2				
BYTE 3	LOGICAL SECTOR ADRS 1							
BYTE 4	LOGICAL SECTOR ADRS 0							

* VALID SECTOR ADDRESS = 1
**SPARE (SET = 0)

TABLE 5. DRIVE AND CONTROLLER SENSE BLOCK

7.0 STATUS AND COMPLETION BYTE FORMAT

At the normal termination of a command or following a fatal error, the controller will cause a status byte to be transferred from the controller to the Host (see Table 4). Bit 0, the least significant bit of the status byte, will be set = 1 if the controller detects a parity error during a command or data transfer to the controller (If enabled - see section 11). Bit 1 will be set = 1 if the controller detects an error condition. Bits 5 and 6 represent the LUN of the device where the error occured. If no error occurs, bits 0-4 will be set = 0.

Following the transfer of the status byte, the MSG line will be asserted to indicate a completion message. At this time the message consists of a single byte transfer with all bits set = 0.

Prior to an error condition the controller, unless disabled (see Figure 11), will retry 3 times before posting the error.

7	6 5	4 3 2	1	0
0	MS LS LUN	SPARE (SET = 0)	ERROR	PARITY ERROR

TABLE 4. STATUS BYTE FORMAT

8.0 DRIVE AND CONTROLLER SENSE BLOCK

Following an error indication from the status byte the Host may perform a REQUEST SENSE command to obtain more detailed information about the error.

The REQUEST SENSE command will transfer a block of 4 bytes to the Host system (see Table 5).

8.1 ERROR CODE DESCRIPTION

The following hexadecimal numbered error codes reflect the codes present in bits 0 through 5 of byte 1 of the request sense block.

8.1.1 TYPE 0 (DRIVE ERROR CODES)

00	No Error
01	No Index Signal Detected
02	No Seek Complete Detected
03	Write Fault (SA1000 and SA4000/4100 only)
04	Drive Not Ready
05	Drive Not Selected (1000 only)
06	No Track 000 Detected

8.1.2 TYPE 1 (DATA ERROR CODES)

10	ID Field ECC or CRC error (uncorrectable)
11	Data Field ECC or CRC error (uncorrectable)
12	ID Address Mark Not Found (unformatted disk)
13	Data Address Mark Not Found
14	Record Not Found - found correct cylinder and head but not sector
15	Seek Error - R/W head not positioned on correct track
16	DMA Timeout Error - no Host acknowledge within 256 usec after request
17	Write Protected (SA800/850 only)
18	Correctable Data Field ECC error - correction is automatic if not disabled
19	Bad Sector Found - sector within a track that has been flagged bad has been found
1A	Format Error - illegal interleave code received from the Host.

8.1.3 TYPE 2 (COMMAND ERROR CODE)

20	Invalid Command received from Host
21	Illegal logical Sector Address - beyond maximum sectors available for type of drive.

8.1.4 TYPE 3 (DIAGNOSTIC ERROR CODES)

30	Ram Diagnostic Error - detected during buffer RAM diagnostic test (see section 6.3). SA1403, and SA1403D only.

9.0 STATUS LED ERROR INTERPRETATION

Drive/controller error conditions are displayed on the 8 LED display lights provided near the J10 DC power connector (see Figures 15 - 17). The following list of hexadecimal numbered error codes describe error meanings. Note that these error codes do not necessarily match the request sense block error codes. LED number 7 is the MSB.

01	No Index Detected
02	No Track Zero Detected
03	Illegal Logical Sector Address - beyond maximum sectors available for type of drive
04	Drive Not Selected (SA1000 only)
05	No Seek Complete Detected
06	ID Address Mark Not found (unformatted)
07	Data Address Mark Not found
08	Seek Error - R/W head not positioned on correct track
09	Record Not found - found correct cylinder and head but not sector
0A	ID ECC or CRC error (uncorrectable)
0B	DMA Timeout Error - no Host acknowledge within 256 usec after request
0C	Invalid Command Received from Host
0D	Incorrect Data Address Mark
0E	Incorrect ID Address Mark
0F	Incorrect Cylinder Address
10	Incorrect Sector Address
11	Incorrect Head Address
12	Uncorrectable Data Field ECC or CRC error
13	Correctable Data Field ECC error
14	Drive Not Ready
15	Write Fault (SA1000 and SA4000/4100 only)
16	Spare
17	Write Protected (SA800/850 only)
18	RAM Diagnostic Error
19	Spare
20	Spare
21	Bad Sector found - a sector within a track that has been flagged bad has been found.

10.0 SECTOR INTERLEAVE CODES

In order to tailor host system data transfer speed to the disk rotational speed, sector interleaving is offered. Sixteen interleave codes are offered numbered 1 to 16. Not all interleave codes will result in optimum sector interleave, therefore the interleave should be chosen carefully. In order to maintain IBM floppy disk compatability an interleave code of 1 should be used. This will result in a non-interleave condition.

The interleave code given during the format command is calculated as follows:

- The interleave algorithm is: Sector + interleave.

Two examples of interleave codes are shown:

Interleave code of 2:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
Physical:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31

Interleave code of 16:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	16	1	17	2	18	3	19	4	20	5	21	6	22	7	23
Physical:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	8	24	9	25	10	26	11	27	12	28	13	29	14	30	15	31

11.0 CONTROLLER OPTION SELECTION

11.1 PARITY SELECT JUMPERS

Odd parity may be used by the Host system for data integrity verification. The controller will always output odd parity to the Host system.

Odd parity checking by the controller may be allowed or inhibited by moving a 3 position jumper plug at W2 located near the J6 Host connector (see Figures 15 thru 17). With jumper at position A + B the controller will test for odd parity on all data input to the controller. With jumper at position B + C the controller will not check for parity (normally shipped in this position).

11.2 DRIVE TYPE SELECTION DIPSWITCH

Table 6 shows the dipswitch settings for various types of drives for the SA1403.

Table 7 shows the dipswitch settings for various types of drives for the SA1403D model.

Table 8 shows the dipswitch settings for the SA1404D model.

The settings shown are only examples and may be set in any order of LUN.

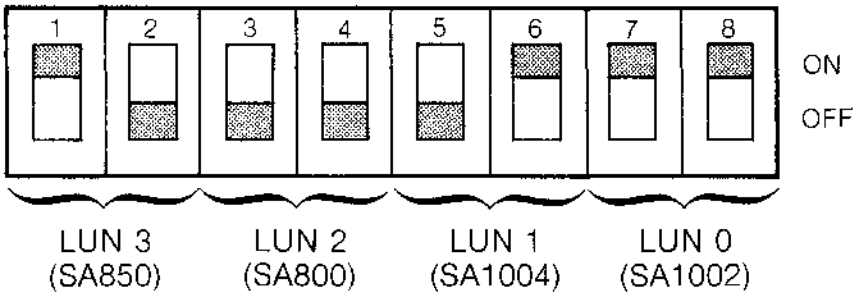


TABLE 6. SA1403 DIPSWITCH SETTING EXAMPLE

THIS INFORMATION NOT AVAILABLE AT THIS TIME

TABLE 7. SA1403D DIPSWITCH SETTING EXAMPLE

PRELIMINARY SETUP
LOCATION: 2J

SWITCH BITS	1 2	3 4 5	6 7 8	
FIELD DEFINITION	NOT USED	LUN 3 DRIVE TYPE	LUN 0-2 DRIVE TYPE	ON
				OFF

DRIVE TYPE	SWITCH SETTING	DESCRIPTION	
0	ON-ON-ON	SA4004	4 MOVABLE HEADS, 201 CYLINDERS
1	ON-ON-OFF	SA4008	8 MOVABLE HEADS, 201 CYLINDERS
2	ON-OFF-ON	SA850	2 HEADS, 77 CYLINDERS (MFM)
3	ON-OFF-OFF	SA800	1 HEAD, 77 CYLINDERS (FM)
4	OFF-ON-ON	SA4100	16 MOVABLE HEADS, 201 CYLINDERS

ALL SA4000 DRIVES ARE 60 SECTORS/TRACK, 256 BYTES/SECTOR.
ALL SA800 DRIVES ARE 26 SECTORS/TRACK, 128 BYTES/SECTOR.
ALL SA850 DRIVES ARE 26 SECOTRS/TRACK, 256 BYTES/SECTOR (MFM).

** EXAMPLE: LOCATION: 2J

1 2	3 4 5	6 7 8	
NOT USED	LUN 3 DRIVE TYPE	LUN 0-2 DRIVE TYPE	ON
	ON-OFF-ON	ON-ON-ON	OFF

UNIT 0 - 2 ARE SETUP FOR SA4004

UNIT 3 IS SET UP FOR SA850 (MFM MODE ONLY)

TABLE 8. SA1404D DIPSWITCH SETTING EXAMPLE

12.0 TRACK FORMAT DESCRIPTION

12.1 26 SECTOR FORMAT

The 26 sector format is an IBM compatable format which employs FM single density encoding on all tracks of the SA800 (IBM 3740 compatable) and on track 0, side 0, of the SA850. This format yields 26 sectors of 128 bytes per sector.

The remainder of the tracks on the SA850 are encoded with MFM double density which yields 26 sectors of 256 bytes per sector (IBM system 34 compatable). Figure 12 shows the two types of encoding utilized.

This format is used on the SA1403D and SA1404D disk controllers.

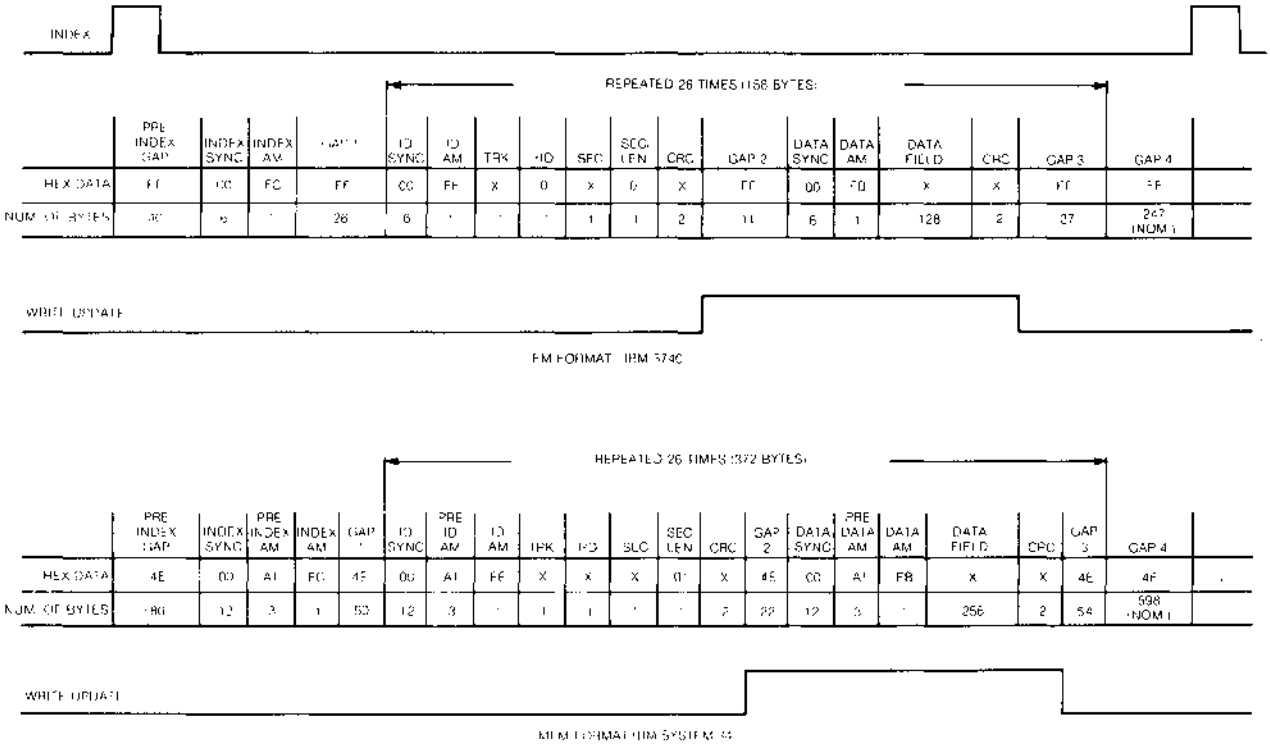


FIGURE 12. 26 SECTOR FORMAT - SA800/850

12.2 32 SECTOR FORMAT

The 32 sector format employs MFM encoding on all tracks of the SA1000. The SA1403 controller also uses this format for the floppy disk drives. This format yields 32 sectors of 256 bytes per sector. Figure 13 shows the 32 sector format.

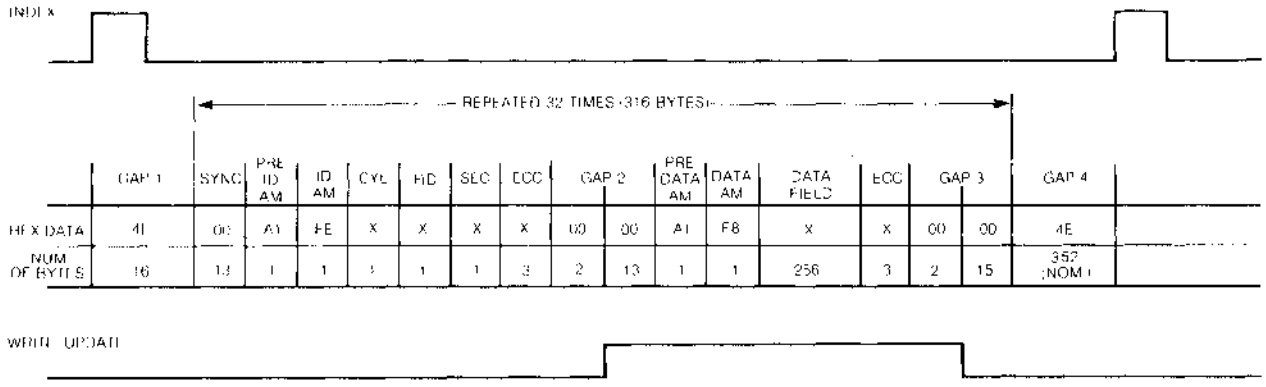


FIGURE 13. 32 SECTOR FORMAT - SA800/850, SA1000

12.3 60 SECTOR FORMAT

The 60 sector format shown in Figure 14 is used with the SA4000/4100 disk drives. This format yields 60 sectors of 256 bytes per sector.

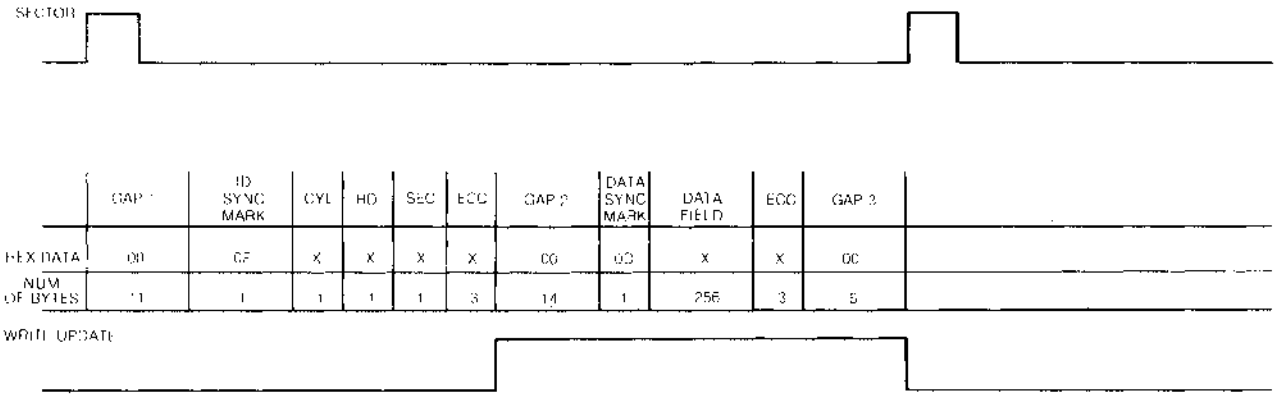


FIGURE 14. 60 SECTOR FORMAT - SA4000/4100

13.0 DRIVE JUMPER SETTINGS

13.1 JUMPER SETTINGS FOR SA800/SA801 FLOPPY

The following information is contained in the SA800/801 Diskette Storage Drive OEM Manual, Shugart Associates, 1977.

Jumper Name	Function (Enabled if Jumper Installed)
A	Install enable DRSEL to drive selection
B	Install, Head Load on Unit Select
C	Remove, Unit Select loads heads
D	Remove, In Use to LED is disabled
DC	Remove, Disable Disk Change to return to controller
DS	Install enable stepper on USel
DS1-4	Install one only, DS1 = LUN 0
HL	Remove, Head load on Unit Select
L	Jumper for -5V (remove for -15V), controller requires -5V only
T1	Remove, Head Load terminator
T2	Install, Pullup for DSx
T3	Install, Direction terminator
T4	Install, Step terminator
T5	Install, Wr Data terminator
T6	Install, Wr Gate terminator
X	Install, Head Load Enable
Y	Remove, Disable Hdld from driving LED
Z	Install drive select drives in use LED
800	Install, enables 800 index only operation
801	Remove, disables 801 mode operation

13.2 JUMPER SETTINGS FOR SA850/851 FLOPPY

Jumper Name	Function (Enabled if Jumper installed)

Controller is compatible with the factory jumper configuration.

13.3 SETTINGS FOR SA4000/4100 WINCHESTER

The following information is contained in the SA4000 Fixed Disk Drive OEM Manual, Shugart Associates 1978.

Control PCB

X - open	Drive selected only be SELECT line
DS - 1,2,3,4 user selectable	Set to determine LUN (DS1 = LUN 0)
ST - jumpered	Sector to J1 connector
RY - open	Ready to radial connector only (J2 connector)
IX - jumpered	Index to J1 connector
T - jumpered	Drive Ready enabled after time delay
C - open	Seek Complete to J2 connector only
SC - jumpered	Sector to J1 connector
BC - open	No Byte Clock on J1
LSB - jumper 1,4,16,64,128	60 Sectors/track
MSB - jumper 512,1024,2048	60 Sectors/track
D - open	Stepper motor always enabled
E - jumpered	Stepper Motor always enabled
S1 - open	Sector/Index generated simultaneously
S2 - jumpered	Sector/Index generated simultaneously
4H - shunt removed	R/W on radial cable only. Seek Complete on radial cable only.
E1,E2,E3 - don't care	
R - jumpered	
S - open	
F - open	
SL - jumpered	Status signals only when drive is selected

Data Separator PCB

C - jumpered	sync on zero's field
D - open	sync on zero's field

13.4 JUMPER SETTINGS FOR SA1000 WINCHESTER

Jumper Name	**Function (enabled if jumper installed)**

Controller is compatable with the factory jumper configuration.

14.0 SA1400 CONTROLLER DIMENSIONAL DRAWINGS

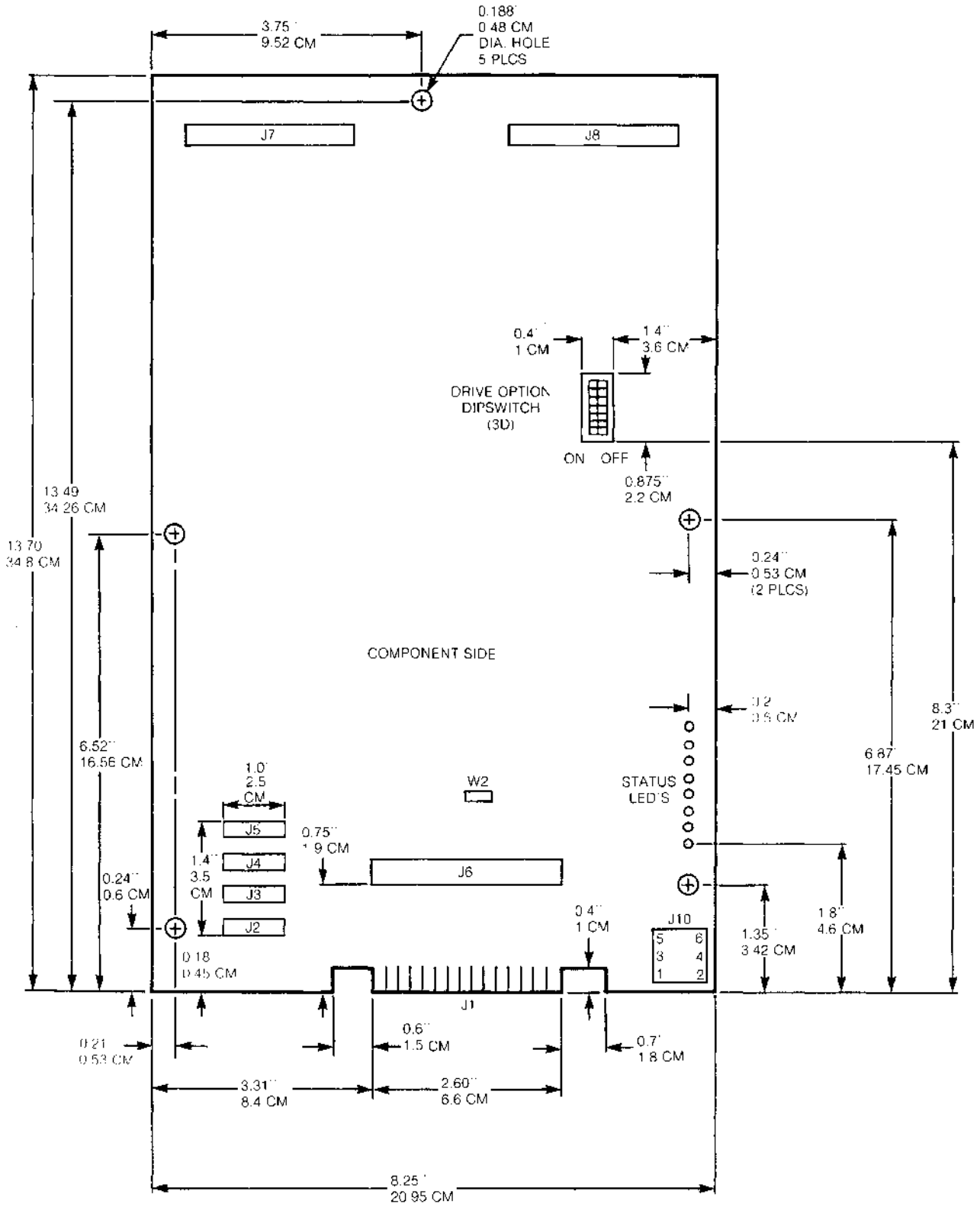


FIGURE 15. SA1403 DIMENSIONAL DRAWING

THIS INFORMATION NOT AVAILABLE AT THIS TIME

FIGURE 16. SA1403D DIMENSIONAL DRAWING

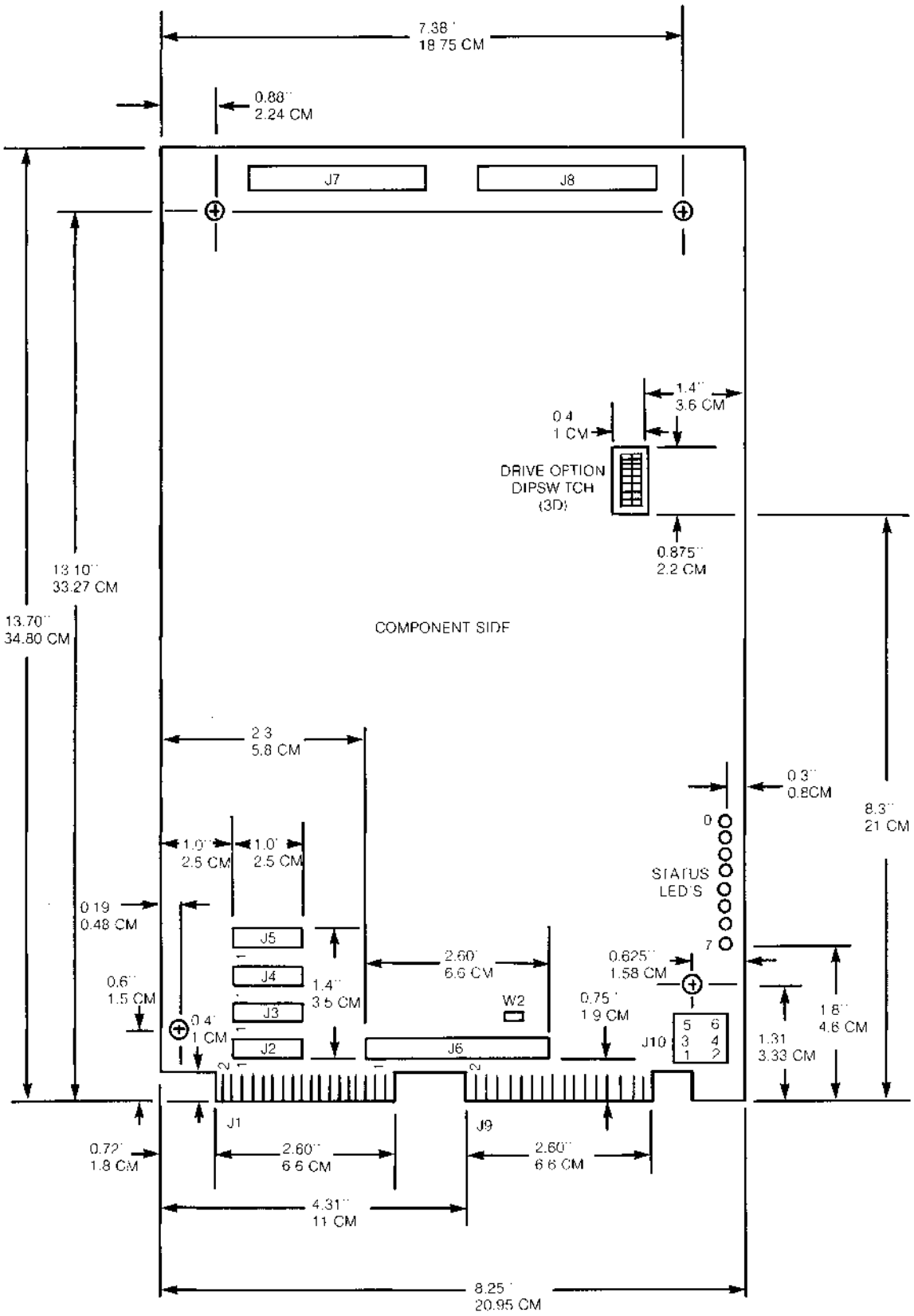


FIGURE 17. SA1404D DIMENSIONAL DRAWING

Shugart

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SERVICE MEMO

Product: SA1403D Controllers **Date:** April 7, 1981 **Memo #:** 2

Subject: Obsolete SA1400 Series Controller Publications

It has come to the attention of Technical Support, that obsolete documents are being used in conjunction with SA1400 series controllers. These documents, the SA1400 Controller OEM Manual (P/N 39016-0) and Engineering Specification no. 30127, do not accurately reflect the product and should **not** be used.

The correct documentation may be obtained from the Shugart Spares Department by requesting the following part numbers:

SA 1403D OEM — P/N 39022
SA 1403 OEM — P/N 39021
SA 1404D OEM — P/N 39023

For information regarding controllers in the SA1400 series, other than those listed above, please contact Technical Support, in Sunnyvale.

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