ST506 MicroWinchester

OEM MANUAL

PRELIMINARY

APRIL 1, 1981

Seagate Technology

Figures:

Figures (Continued)

Tables

1.0 Introduction

1.1 General Description:

The ST506 disc drive is a random access storage device with two non-removable 5¼ inch discs as storage media. Each disc surface employs one movable head to service 153 data tracks. The total formatted capacity of the four heads and surfaces is 5 megabytes. (32 sectors per track, 256 bytes per sector, 612 tracks).

Low cost and unit reliability are achieved through the use of a band actuator and open loop stepper head positioning mechanism. The inherent simplicity of mechanical construction and electronic controls allows maintenance free operation throughout the life of the drive. Both Electronic PCB's are mounted outside HDA for field serviceability.

Mechanical and contamination protection for the heads, actuator and discs are provided by an impact resistant aluminum enclosure. A self contained recirculating system supplies clean air through a 0.3 micron filter. A second port in the filter assembly allows pressure equalization with ambient air without chance of contamination. A patented spindle pump assures adequate air flow and uniform temperature distribution throughout the head and disc area. Thermal isolation of the stepper and spindle motor assemblies from the disc enclosure yields a very low temperature rise within the enclosure, providing significantly greater off track margin and the ability to immediately perform read and write operations after power up with no thermal stabilization delay.

The ST506 electrical interface is similar to the Shugart Associates SA1000 family of 8 inch fixed disc drives. The ST506 size and mounting is identical to the industry standard minifloppy disc drives and uses the same DC voltage and connector. No AC power is required.

Key Features:

- Storage Capacity of 6.38 megabytes unformatted, 5.0 megabytes formatted as shipped.
- Winchester design reliability, 9.5 gram head load force, 19 micro-inch flying height.
- Same physical size and mounting as the minifloppy.
- Same DC voltages as the minifloppy.
- Band actuator and stepper motor head positioning.
- 5.0 megabit/second transfer rate.
- Simple floppy like interface.
- Same track capacity as a double density 8 inch floppy.

- 170 millisecond random average access time, reducible to 95 ms via a simple software algorithm (See Section 4.5.3)

1.2 Specification Summary:

1.2.1 Physical Specifications:

Environmental Limits:

Ambient Temperature = 40° to 122°F (4° to 50°C)
Relative Humidity = 8 to 80%
Maximum Wet Bulb = 78° non-condensing
Maximum Altitude = 10,000 feet

DC Power Requirements

+12V ± 5%, 1.8A typical, 4.5A at power on

+5V ± 5%, 0.7A typical, 1.0A maximum

+12V/+5V Maximum Ripple = 50mV P-P

Mechanical Dimensions:

Height = 3.25 inches
Width = 5.75 inches
Depth = 8.00 inches
Weight = 4.2 lbs. (1.9 kg)

Heat Dissipation - 25 watts typical
- 29 watts maximum

1.2.2 Reliability Specifications:

MTBF = 11,000 POH, typical usage
PM = Not required
MTTR = 30 minutes
Component Design Life = 5 years

Error Rates:

Soft read errors = 1 per 10^{10} bits read
*Hard read errors = 1 per 10^{12} bits read
Seek errors = 1 per 10^{6} seek

*Not recoverable within 16 re-tries.

1.2.3 Performance Specifications:

Capacity		
Unformatted		
	Per Drive	6.38 Megabytes
	Per Surface	1.59 Megabytes
	Per Track.	10416 Bytes
Formatted		
	Per Drive	5.0 Megabytes
	Per Surface	1.25 Megabytes
	Per Track	8192 Bytes
	Per Sector	256 Bytes
	Sectors per Track	32
Transfer Rate		5.0 Megabits per second
Access Time		
	Track to Track	3 ms
	Average (Inc. Settle)	170 ms, reducible to 95 ms. (See Section 4.5.3)
	Maximum (Inc. Settle)	500 ms, reducible to 245 ms. "
	Settling Time	15 ms
Average Latency		8.33ms

1.2.4 Functional Specifications

Rotational speed	3600 rpm ± 1%
Recording density	7690 bpi max
Flux density	7690 fci
Track density	255 tpi
Cylinders	153
Tracks	612
R/W Heads	4
Disks	2

2.0 Functional Characteristics

2.1 General Operation

The ST506 disc drive consists of Read/Write and control electronics, read/write heads, track positioning actuator, media, and air filtration system. The components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the desired track.
3. Read and write data.
4. Provide a contamination free environment.

2.2 Read/Write and Control Electronics

Electronics are packaged on two printed circuit boards. The primary board to which power, control and data signals are connected includes:

1. Index detection circuit.
2. Head position/actuator circuit.
3. Read/write circuits.
4. Drive up to speed circuit.
5. Head select circuit.
6. Write fault detection circuit.
7. Step motor drive circuit.
8. Drive select circuit.
9. Track zero detector circuit.

The second PCB, mounted to the baseplate under the primary board derives its power from the primary board and provides power and speed control to the spindle drive motor.

2.3 Drive Mechanism

A Brushless DC drive motor rotates the spindle at 3600 rpm. The spindle is driven directly with no belt or pulley being used. The motor is thermally isolated from the baseplate to minimize temperature rise in the sealed chamber containing the heads and discs. The motor and spindle are dynamically balanced to insure a low vibration level. A brake is used to provide a fast stop to the spindle motor when power is removed. The baseplate is shock mounted to minimize transmissibility of vibration to the chassis or frame.

2.4 Air Filtration System (Figure 1)

The discs and read/write heads are fully enclosed in a module using a integral recirculation air system with an absolute filter which maintains a clean environment. Integral to the filter is a port which also permits pressure equalization with the ambient air without contaminate entry.

2.5 Positioning Mechanism (Figure 2)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by a band actuator connected to the stepper motor shaft. The stepper motor is thermally isolated from the baseplate to minimize temperature rise in the sealed chamber containing the heads and discs.

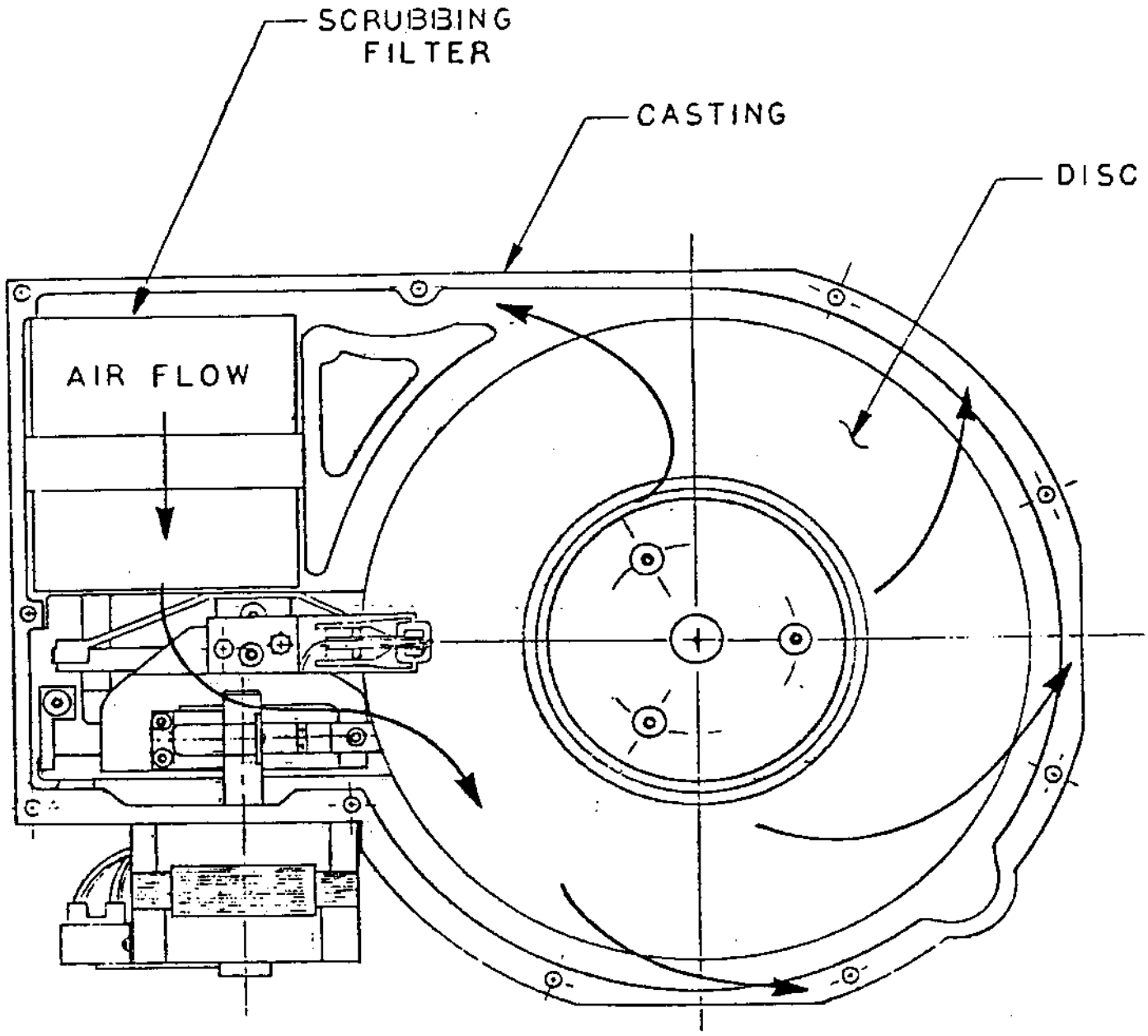


FIG 1A

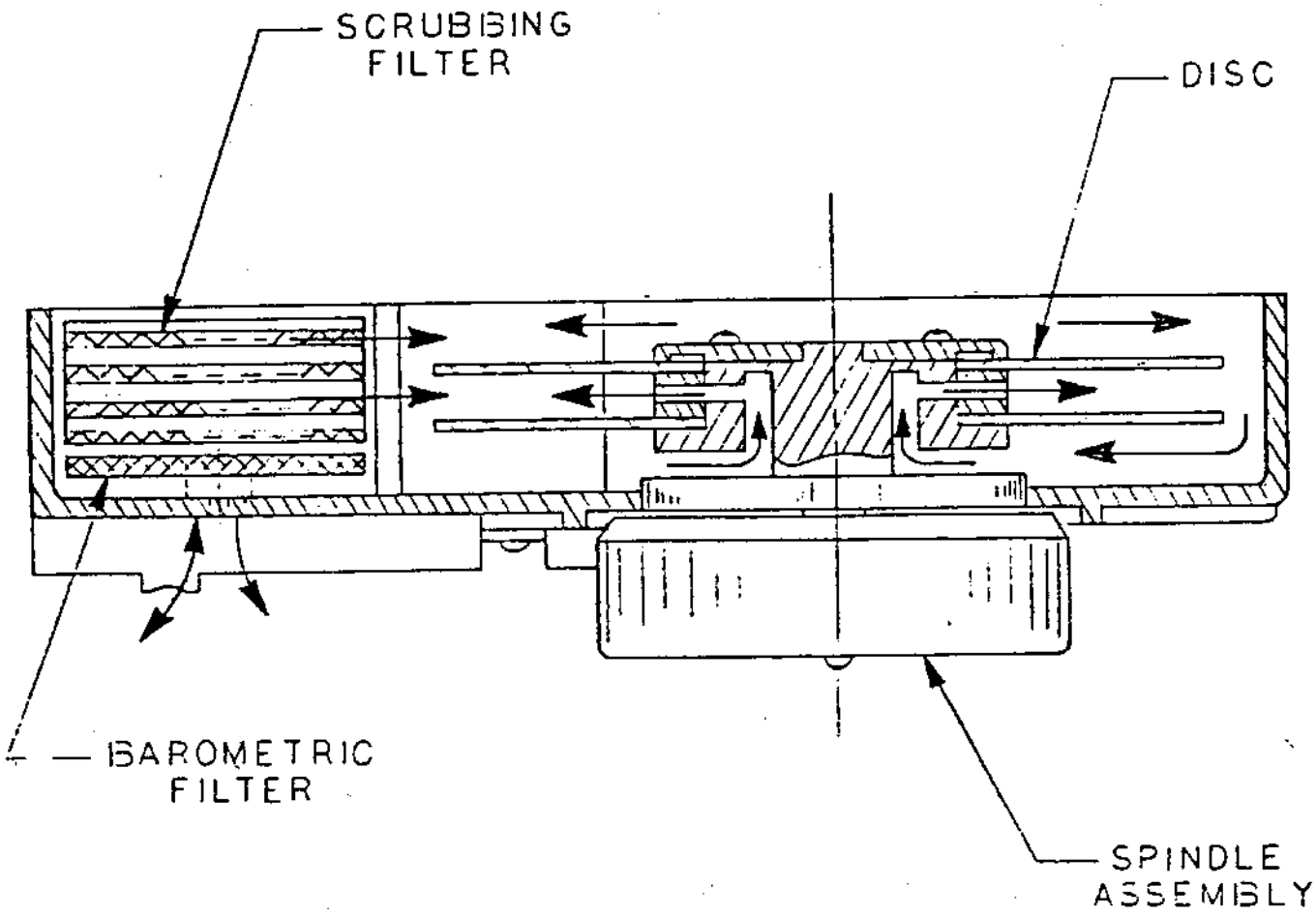

SCRUBBING FILTER
DISC
BAROMETRIC FILTER
SPINDLE ASSEMBLY

FIG 1B

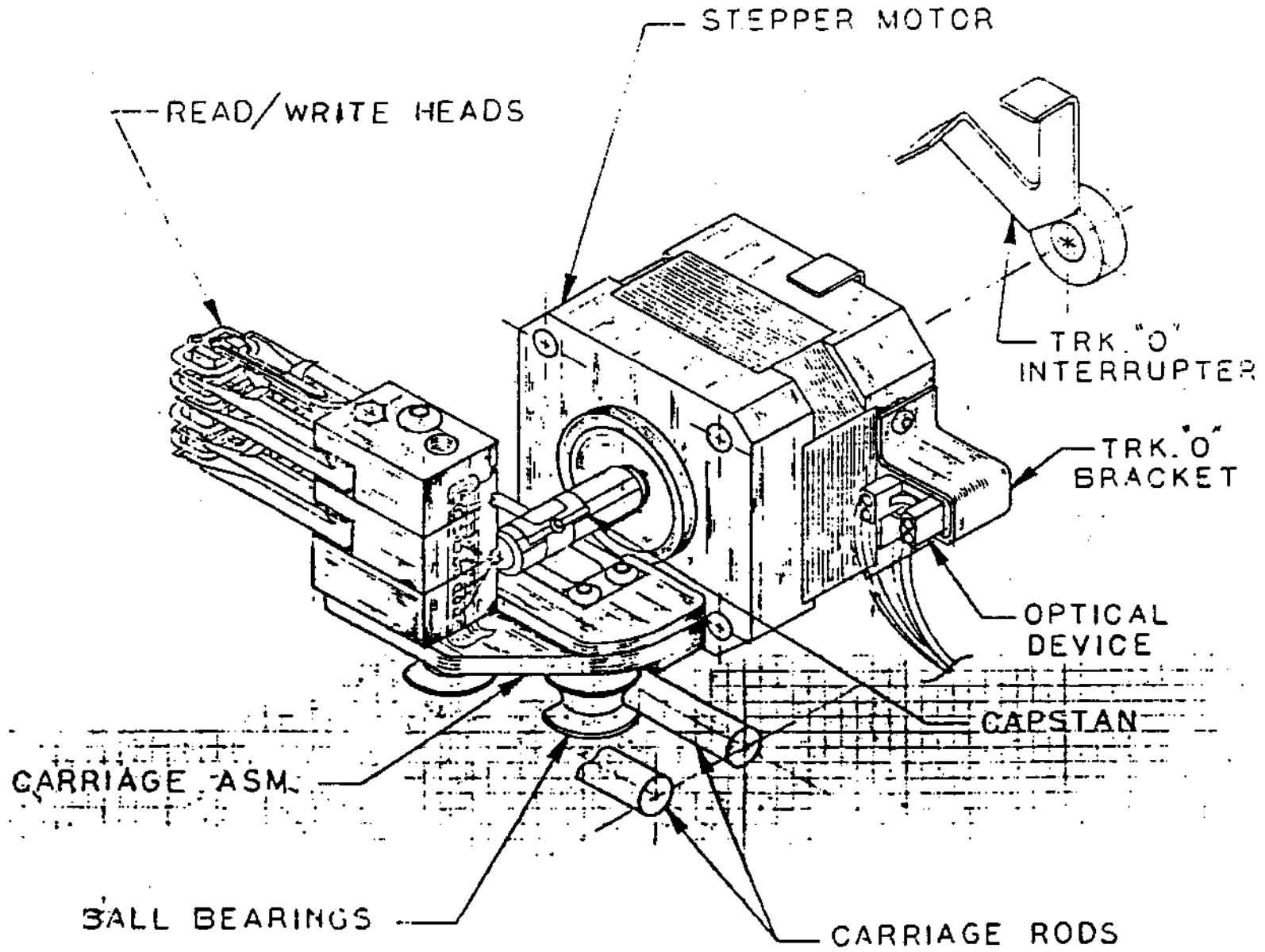

STEPPER MOTOR
READ/WRITE HEADS
TRK. "0" INTERRUPTER
TRK. "0" BRACKET
OPTICAL DEVICE
CAPSTAN
CARRIAGE ASM.
BALL BEARINGS
CARRIAGE RODS

FIG 2

2.6 Read/Write Heads and Discs

The recording media consists of a lubricated thin magnetic oxide coating on a 130 mm diameter aluminum substrate. This coating formulation, together with the low load force/ low mass Winchester type flying heads, permit reliable contact start/stop operation.

Data on each of the four disc surfaces is read by one read/write head, each of which accesses 153 tracks.

3.0 Functional Operations

3.1 Power Sequencing (Figure 3).

+5 and +12 volts may be applied in any order. +12 volts must be applied to start the spindle drive motor. A speed sense circuit counts 512 disc revolutions. After 512 revolutions, the heads will automatically recalibrate to track Ø. (See Section 4.5.2 for exception). For this recalibration to occur, the step input signal must be inactive. Track Ø, seek COMPLETE and READY signals on the interface will become true sequentially. The drive will not perform read & write or seek functions until READY becomes true.

3.2 Drive Selection

Drive selection occurs when one of the drive select lines are activated. Only the drive selected will respond to the input signals, and only that drive's output signals are then gated to the controller interface. (See Section 4.5.1 for exception).

3.3 Track Accessing

Read/write head positioning is accomplished by:

a) Deactivating write gate.

b) Activating the appropriate Drive Select Line.

c) Being in the READY condition with SEEK COMPLETE true.

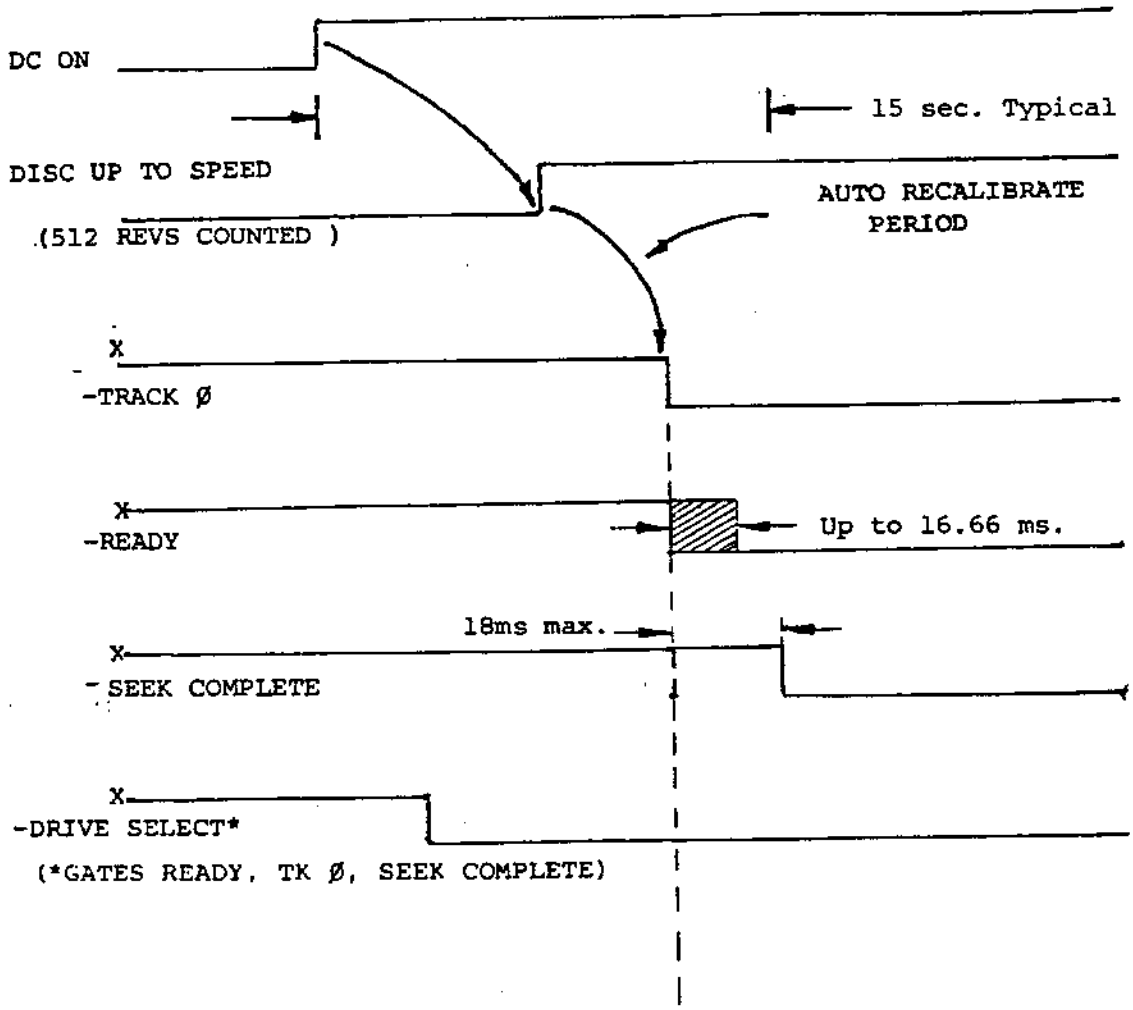
d) Selecting the appropriate direction.

e) Pulsing the step line.

Each step pulse will cause the heads to move either 1 track in or 1 track out depending on the level of the

FIGURE 3

POWER UP SEQUENCE



Direction Line. A true on the Direction Line will cause a seek inward toward the spindle; a false outward toward track Ø.

3.4 Head Selection.

Any of the 4 heads can be selected by placing the head's binary address on the two Head Select Lines.

3.5 Read Operation

Reading data from the disk is accomplished by:

a) Deactivating the Write Gate Line.

b) Activating the appropriate Drive Select Line.

c) Assuring the drive is Ready.

d) Selecting the appropriate head.

3.6 Write Operation

Writing data onto the disk is accomplished by:

a) Activating the appropriate Drive Select line.

b) Assuring that the drive is Ready.

c) Selecting the proper head.

d) Insuring no write fault conditions exist.

e) Activating Write Gate and placing data on the Write Data line.

4.0 Electrical Interface

The interface to the ST506 can be divided into three categories, each of which are physically separated.

1. Control signals.

2. Data signals.

3. DC power.

All control lines are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the host (output) via interface connection J1/P1. The data transfer signals are differential in nature and provide data either to (write) or from (read) the drive via J2/P2. (Defined by EIA RS-422-A)

Tables I through III and Figures 4 through 6 show connector pin assignments and interconnection of cabling between the host controller and drives.

ST506 DRIVE INTERFACE

TABLE I J1/P1 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	- REDUCED WRITE CURRENT
3	4	RESERVED (Head 2^2 in future products)
5	6	- WRITE GATE
7	8	- SEEK COMPLETE
9	10	- TRACK Ø
11	12	- WRITE FAULT
13	14	- HEAD SELECT 2^0
15	16	RESERVED (TO J2 PIN 7)
17	18	- HEAD SELECT 2^1
19	20	- INDEX
21	22	- READY
23	24	- STEP
25	26	- DRIVE SELECT 1
27	28	- DRIVE SELECT 2
29	30	- DRIVE SELECT 3
31	32	- DRIVE SELECT 4
33	34	- DIRECTION IN

TABLE II J2/P2 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	- DRIVE SELECTED
4	3	RESERVED
6	5	SPARE
8	7	RESERVED (TO J1 PIN 16)
	9,10	SPARE
12	11	GND
	13	+ MFM WRITE DATA
	14	- MFM WRITE DATA
16	15	GND
	17	+ MFM READ DATA
	18	- MFM READ DATA
20	19	GND

VOLTAGE		GROUND	
PIN 1	+12V VOLTS DC	PIN 2	+12V VOLT RETURN
PIN 4	+5V VOLTS DC	PIN 3	+5V VOLT RETURN

TABLE III

P3 - DC CONNECTOR PIN ASSIGNMENTS

ST506 DRIVE INTERFACE

FIGURE 4: CONTROL SIGNALS
J2/P2 NOT SHOWN

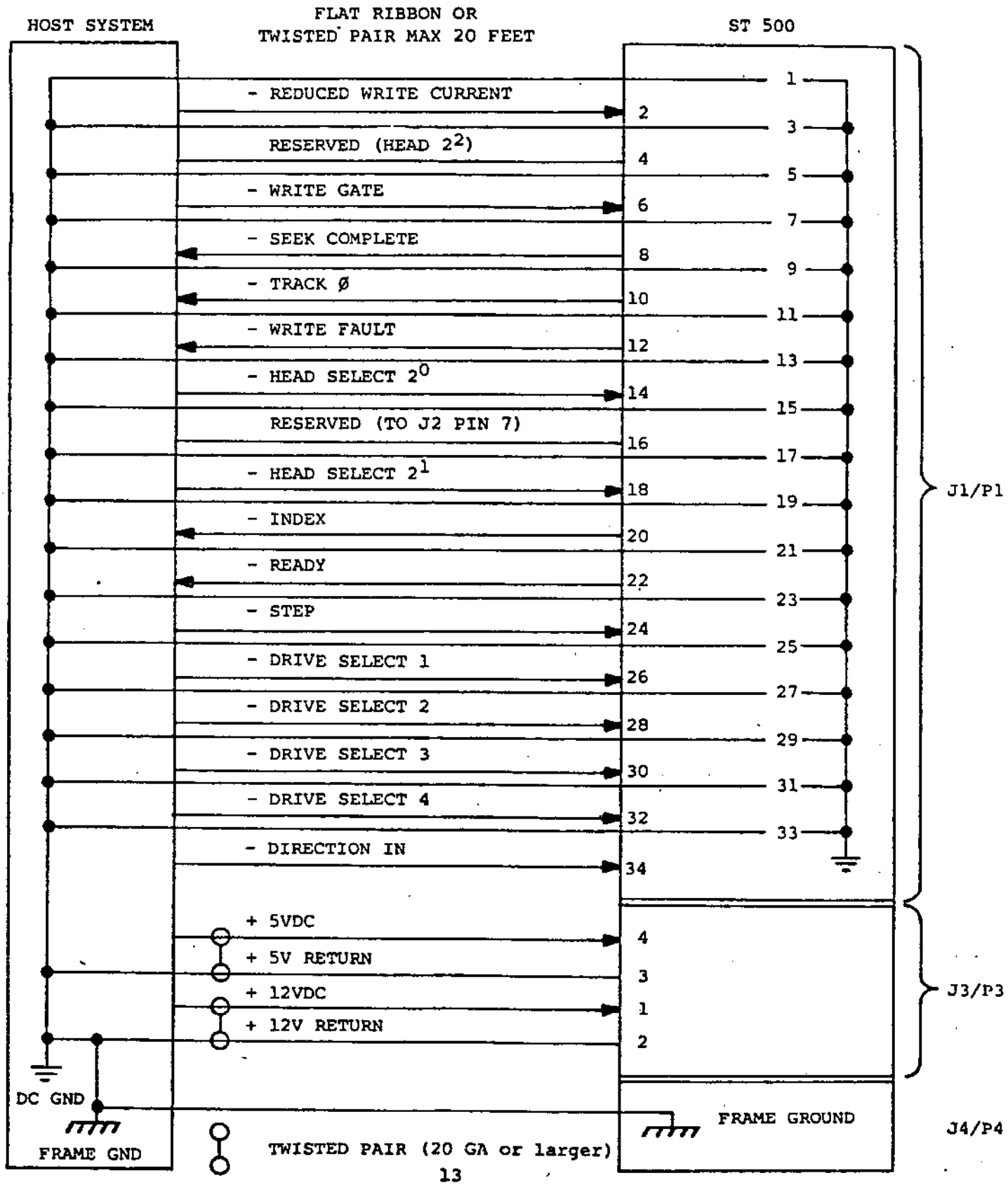


FIGURE 5: DATA SIGNALS

FLAT CABLE OR TWISTED PAIR
20 FEET MAXIMUM

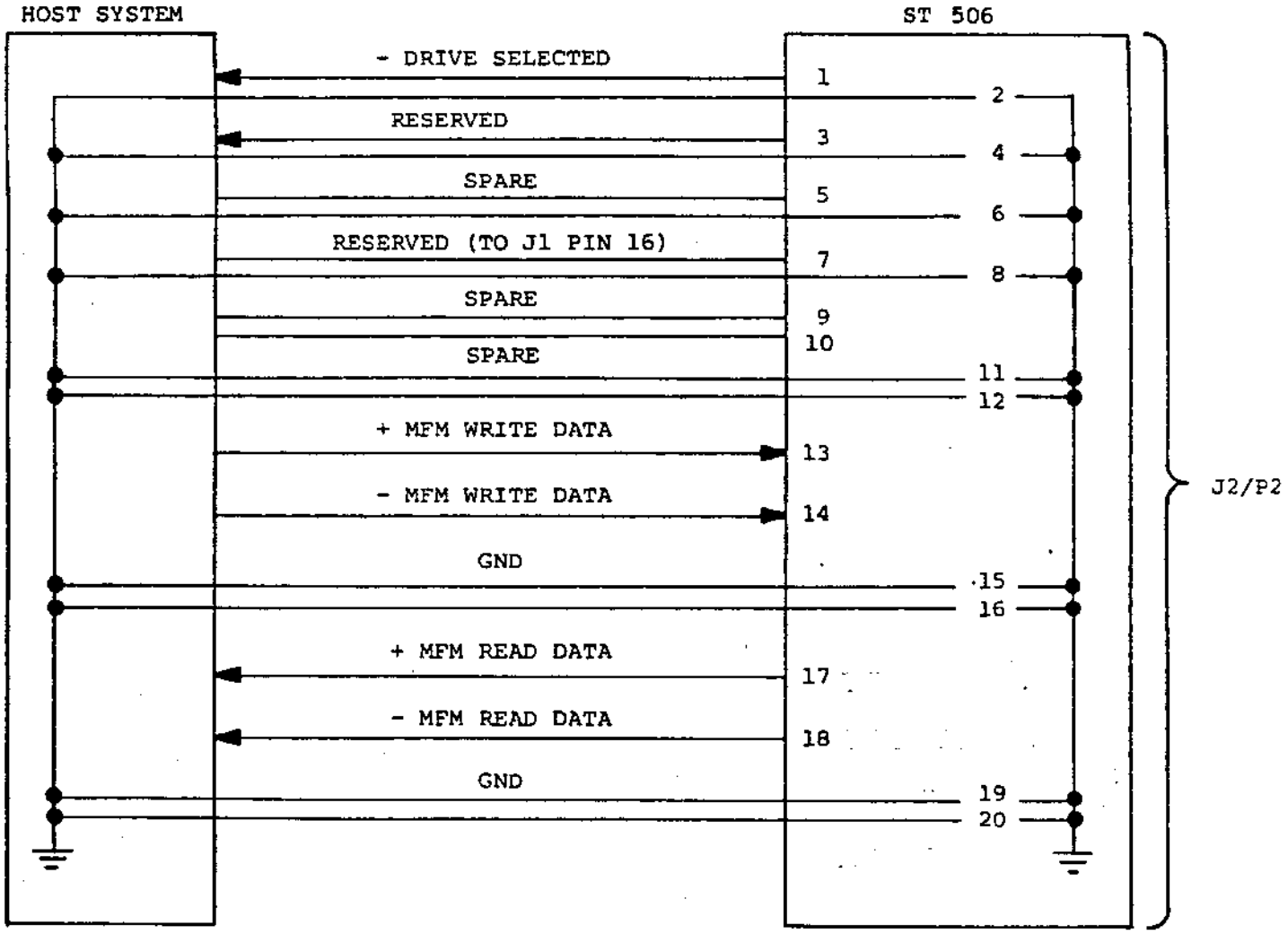
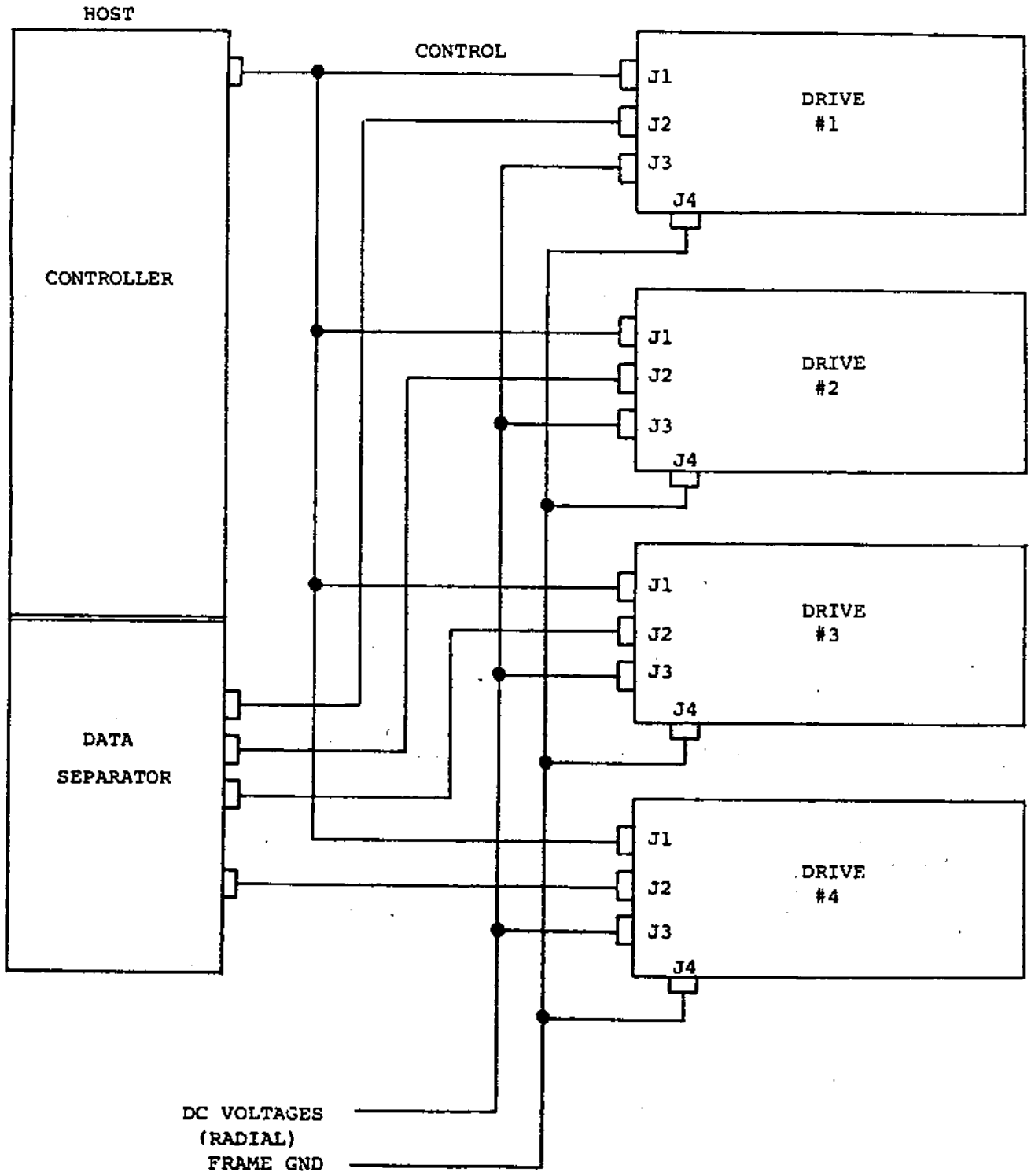


FIGURE 6: TYPICAL CONNECTION, 4 DRIVE SYSTEM



4.1 Control Input Lines

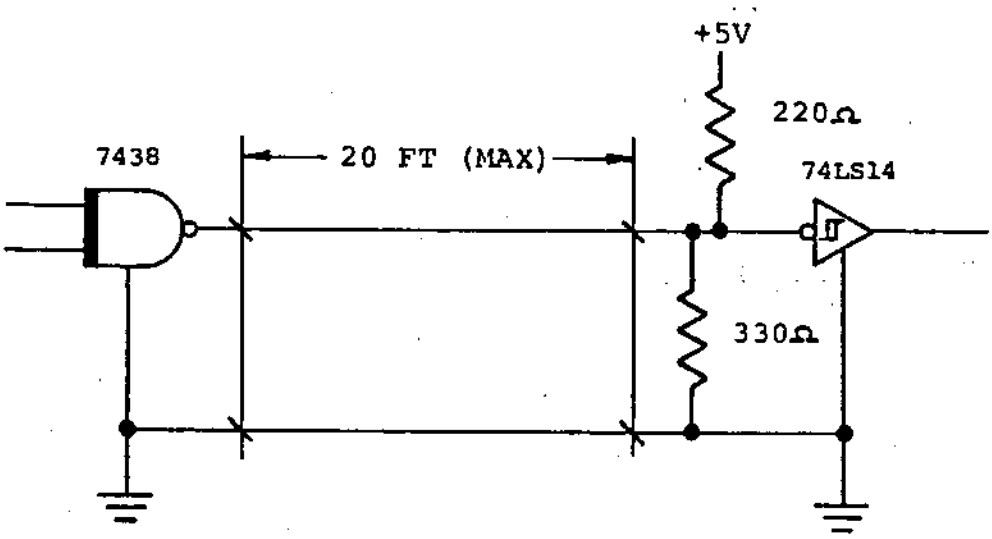
The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are REDUCED WRITE CURRENT, WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1; STEP and DIRECTION IN. The signal to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to Figure for the recommended circuit.

TRUE: 0.0VDC to 0.4VDC @ I = -40 mA (max)

FALSE: 2.5VDC to 5.25VDC @ I = +250 μA (open)

FIGURE 7: CONTROL SIGNALS DRIVER/RECEIVER COMBINATION



4.1.1 Reduced Write Current

This line, when active together with WRITE GATE, causes the write circuitry to write on the disk with a lower write current. It is required that this line be set true when writing is to be performed on cylinders 128 through 152, and set false when writing is to be performed on cylinders 0 through 127.

A 220/330 resistor pack allows for line termination.

4.1.2 Write Gate

The active state of this signal, or logical zero level, enables write data to be written on the disk. The inactive state of this signal, or logical one level, enables data to be transferred from the drive. Also, the inactive state of this signal enables the step pulses to step the R/W head positioner.

A 220/330 resistor pack allows for line termination.

4.1.3 Head Select 2^0 And 2^1

These two lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered Ø through 3. When both HEAD SELECT lines are false head Ø will be selected.

A 220/330 resistor pack allows for line termination.

4.1.4 Direction In

This signal defines direction of motion of the R/W head when the STEP line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the STEP line the R/W heads will move away from the center of the disk. If this line is a logical zero the direction of motion is defined as "in" and the R/W heads will move toward the center of the disk. Change in direction must meet the requirement shown in Figure 8.
A 220/330 resistor pack allows for line termination.
Note: Direction must not change during step time.

4.1.5 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion defined by the DIRECTION IN line.

The access motion is initiated at the logical zero to logical one transition or the trailing edge of this signal pulse. Any change in the DIRECTION IN line must be made at least 100ns before the leading edge of the step pulse.

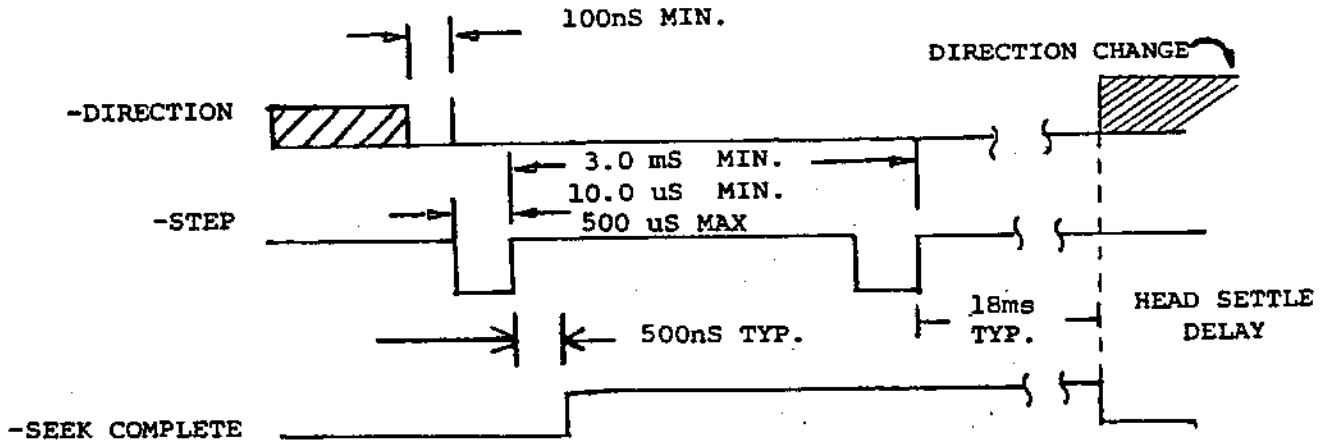
The R/W head will move at the rate of the incoming step pulses. The minimum time between successive steps is 3.0mS. The minimum pulse width is 10.0 μsec. See Figure 8 for step timing.

Step pulses issued at 3.0mS intervals results in a random average access time of 170mS. An option available on the printed circuit board allows a decrease in this time. See Section 4.5.3.

A 220/330 resistor pack allows for line termination.

FIGURE 8

STEP MODE TIMING



* Change in direction can not be made prior to seek complete.

4.1.6 DRIVE SELECT 1 - 4

DRIVE SELECT, when logically true, connects the drive interface to the control lines. Cutting the appropriate shunts at IC position 6C will determine which select line on the interface will activate that drive. The following table indicates which DRIVE SELECT shunts must be cut at IC position 6C.

DRIVE SELECT	CUT SHUNTS
DS 1	10-7, 11-6, and 12-5
DS 2	9-8, 11-6, and 12-5
DS 3	9-8, 10-7, and 12-5
DS 4	9-8, 10-7, and 11-6

4.2 CONTROL OUTPUT LINES

The output control signals are driven with an open collector output stage capable of sinking a maximum of 40mA at logical zero or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the logical one or false state, the driver transistor is off and the collector cutoff current is a maximum of 250µA.

All J1 output lines are enabled by the respective DRIVE SELECT line.

Figure 7 shows the recommended circuit.

4.2.1 SEEK COMPLETE

This line will go true when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when SEEK COMPLETE is false.

SEEK COMPLETE will go false in three cases:

1) A recalibration sequence is initiated (by drive logic) at power on because R/W heads are not over track zero.

2) 500nS (typical) after the leading edge of a step pulse or series of step pulses.

3) If +5 volts or +12 volts are lost momentarily but restored.

4.2.2 TRACK Ø

This interface signal indicates a true state or locical zero only when the drive's R/W heads are positioned at track zero (the outermost data track).

4.2.3 WRITE FAULT

This signal is used to indicate a condition exists at the drive that causes improper writing on the disk. When this line is true, further writing and stepping is inhibited at the drive until the condition is corrected. It cannot be reset via the interface.

There are three conditions detected:

a) Write current in a head without WRITE GATE active or no write current in the head with WRITE GATE active and DRIVE SELECTED.

b) Multiple heads selected, no head selected, or improperly selected.

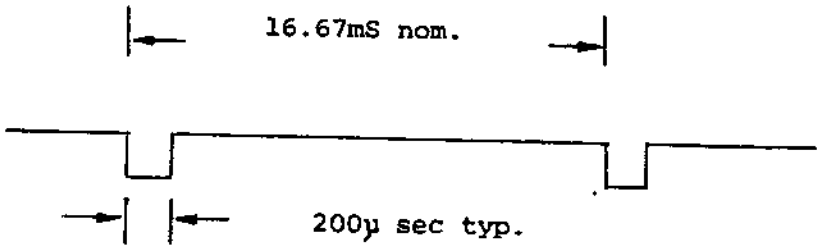
c) DC voltages are grossly out of tolerance.

4.2.4 INDEX

This interface signal is provided by the drive once each revolution (16.67mS nom.) to indicate the beginning of the track. Normally, this signal is a logical one level and makes the transition to the logical zero level to indicate INDEX. Only the transition from one to zero is valid. See Figure 9.

FIGURE 9

INDEX TIMING



4.2.5 READY

This interface signal when true together with SEEK COMPLETE, indicates that the drive is ready to read, write or seek, and that the I/O signals are valid. When this line is false, all writing and seeking are inhibited.

The typical time after power on for READY to be true is 15 seconds.

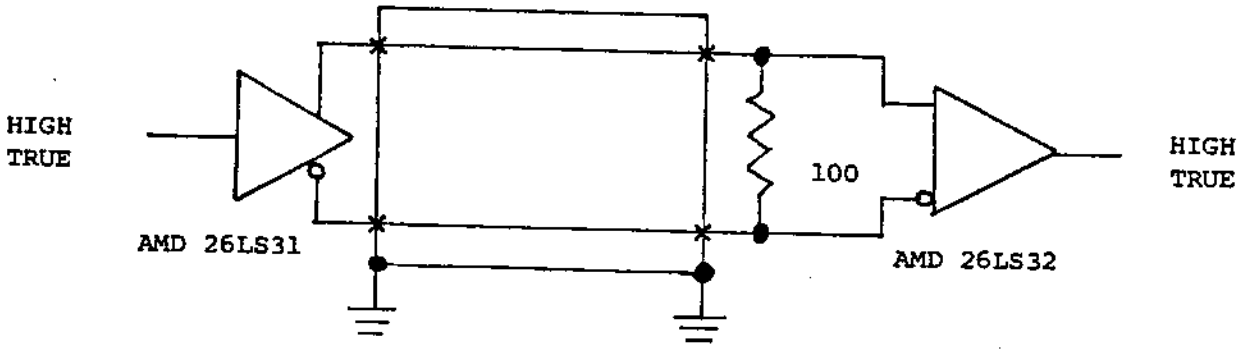
4.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Two pairs of balanced signals are used for the transfer of data: WRITE DATA and READ DATA. Figure 10 illustrates the driver/receiver combination used in the ST506 drive for DATA TRANSFER signals.

FIGURE 10

DATA LINE DRIVER/RECEIVER COMBINATION



Z = 105Ω
FLAT RIBBON OR TWISTED PAIR MAX 20 FT.

NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE.

4.3.1 MFM WRITE DATA

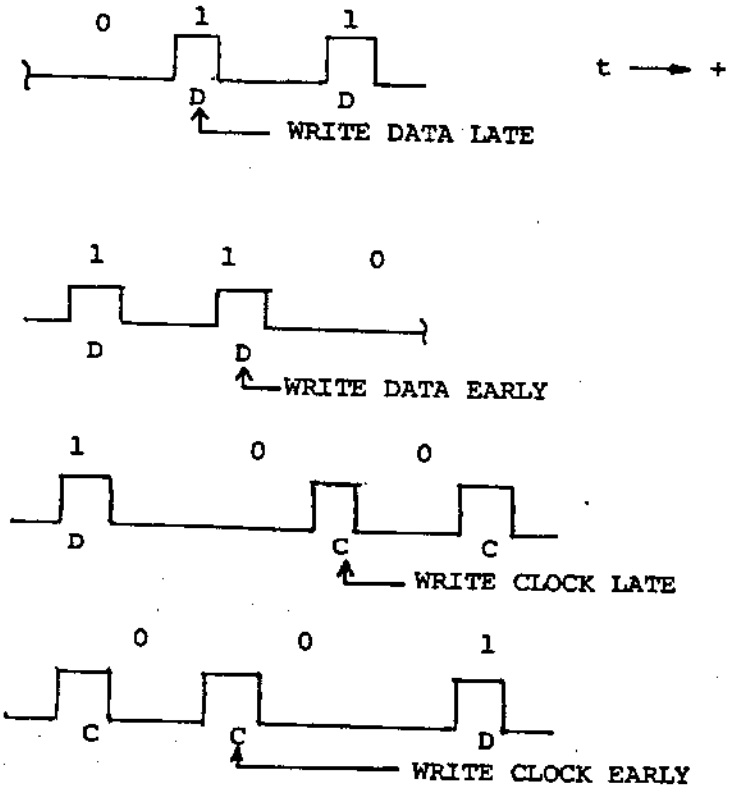
This is a differential pair that defines the transitions to be written on the track. The transition of +MFM WRITE DATA line going more positive than the -MFM WRITE DATA will cause flux reversal on the track provided WRITE GATE in active. This signal must be driven to an inactive state (+MFM WRITE DATA more negative than -MFM WRITE DATA) by the host system when in a read mode.

To insure data integrity at the error rate specified, the write data presented by the host must be pre-compensated on tracks 64 through 152.

The optimum amount of pre-compensation is 12nS for both early and late written bits. Figure 11 shows the bit patterns to be compensated. All other patterns are written "on time."

FIGURE 11

WRITE PRE-COMPENSATION PATTERNS



Writing should occur out of a shift register which is used to observe the pattern. "On time" represents a nominal delay. Early and late represent less or more delay respectively.

4.3.2 MFM READ DATA

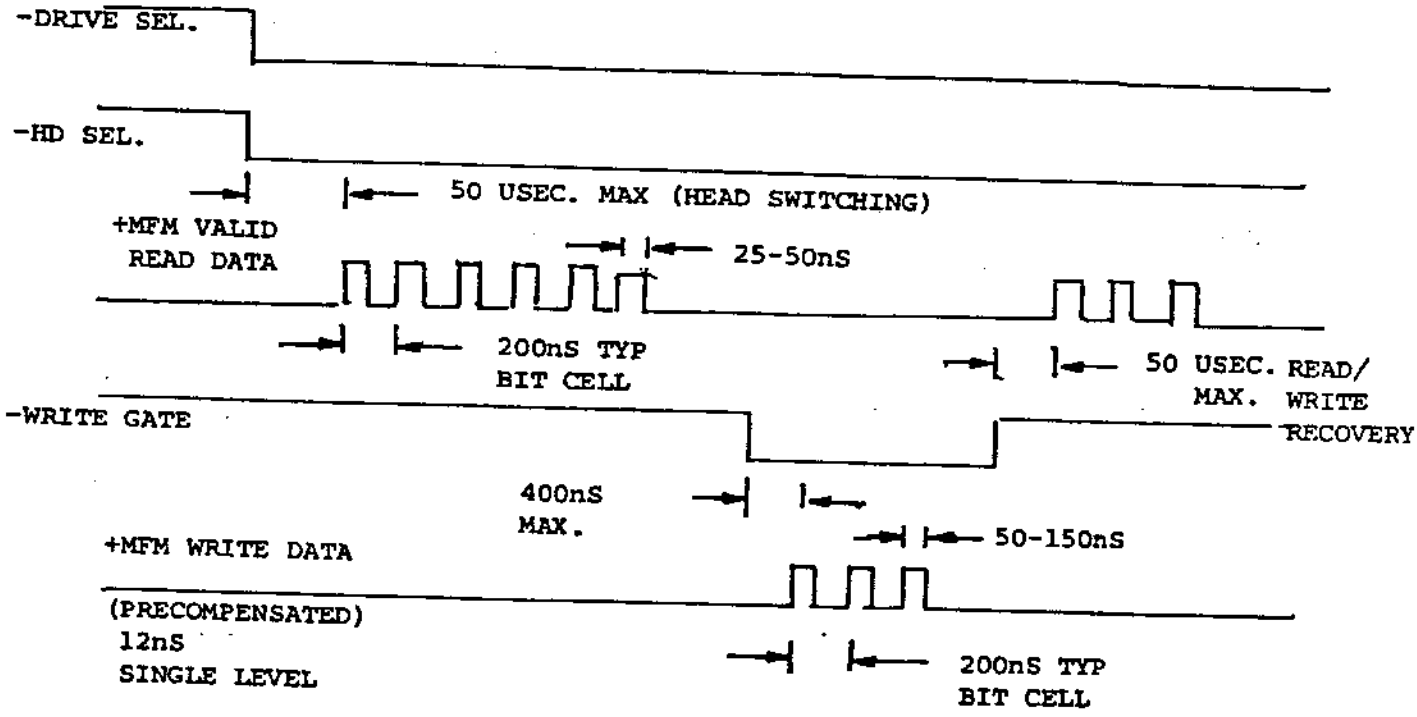
The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

4.3.3 READ/WRITE TIMING

The timing diagram as shown in Figure 12 shows the necessary sequence of events (with associated timing restrictions) for proper Read/Write operation of the drive.

FIGURE 12

READ/WRITE DATA TIMINGS



4.4 DRIVE SELECTED

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 7. This signal will go active only when the drive is programmed as drive X (X=1,2,3, or 4) by programming the shunt on the drive and that the DRIVE SELECT X line at J1/P1 is activated by the host system.

4.5 CUSTOMER OPTIONS

Three optional features which are implemented via a shunt block at IC position 6C on the main printed circuit board are available for customer reconfiguration of the drive functions.

4.5.1 "R" (Radial) Option

As shipped, the 14 pin shunt block installed in IC 6C position (16 pin socket) is plugged in pins 2-8, leaving pins 1 and 16 open. This results in a daisy chain operation. Outputs are not active until the drive is selected. Moving the shunt block one position to use pins 1 and 16 result in radial operation. In this case, all output signals are active, even if the drive is not selected. However, in this case, the front panel LED will not be on. Drive Select must be active to light the LED.

4.5.2 "D" (Defeat Recal) Option

As shipped, the "D" shunt, pins 2-15, is shorted. In this case, whenever a power up sequence is performed, or DC is bad, the heads will automatically be repositioned to track ØØ. Cutting shunt D will defeat the automatic recal operation, allowing the drive to become "ready" earlier. However, during power up, the stepper circuitry will always put phase "A" active. Thus, there is no guarantee that the drive heads will be positioned at the same cylinder as existed when the drive was powered down. It would start at the same track only if the track corresponded to one which utilizes phase A. When using this option

Issuing a Read ID command would allow determination of the active track address, and could be used to initialize a present track address register.

4.5.3 "H" (Half step) Option

As shipped, the "H" shunt, pins 4-13, is shorted. In this case, step pulses are applied to the interface at an interval of 3 milliseconds as shown in Figure 8. Cutting shunt "H" allows a significant decrease in access time when used in conjunction with a simple software algorithm supplied by the user. For detailed implementation information, contact the factory for a copy of Application Note ST001.

5.0 Physical Interface:

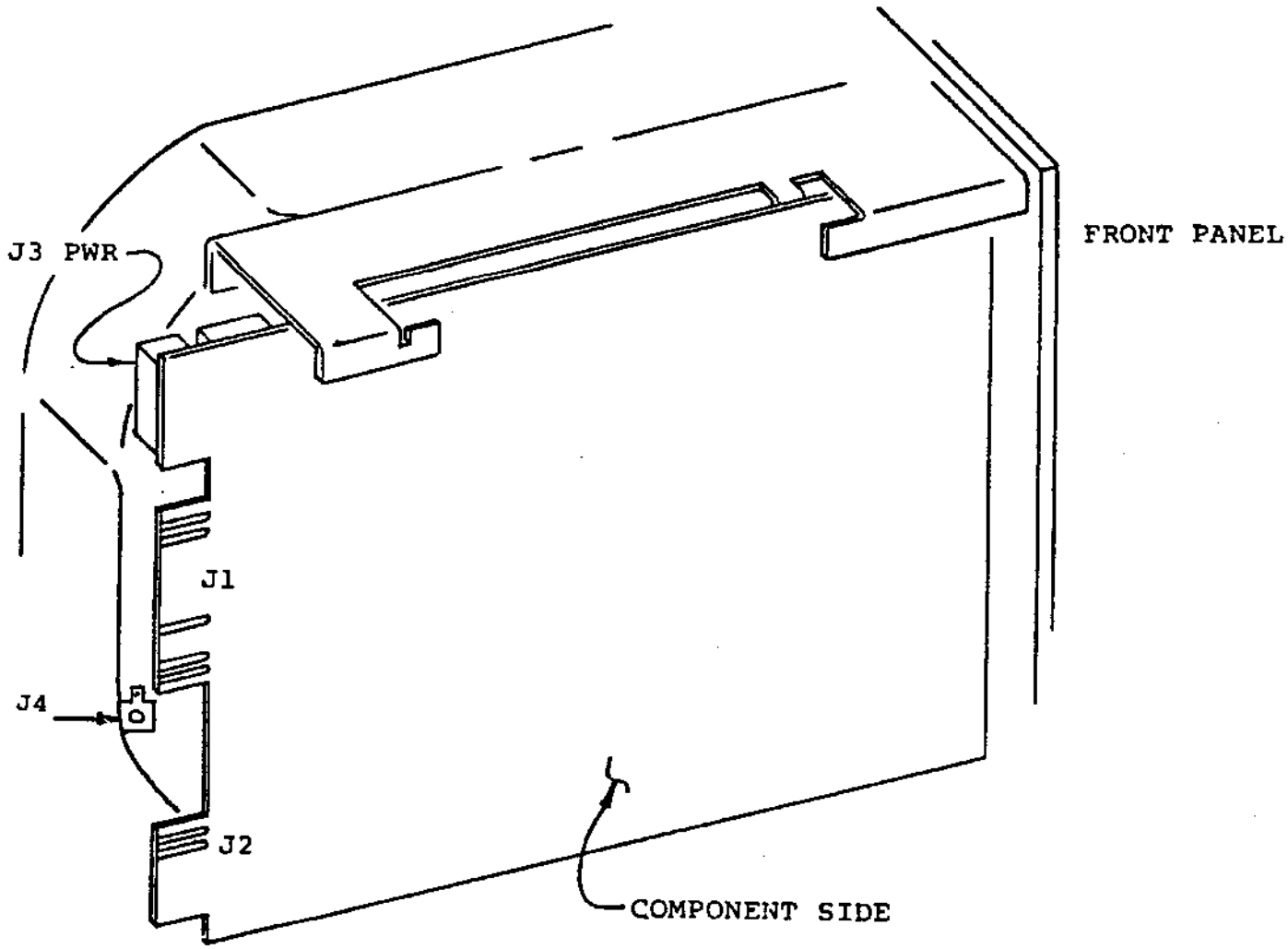
The electrical interface between the ST506 and the host controller is via four connectors:

1. J1 - Control signals, multiplexed
2. J2 - Read/write signals, radial
3. J3 - DC power input
4. J4 - Frame ground

Refer to Figure 13 for connector locations.

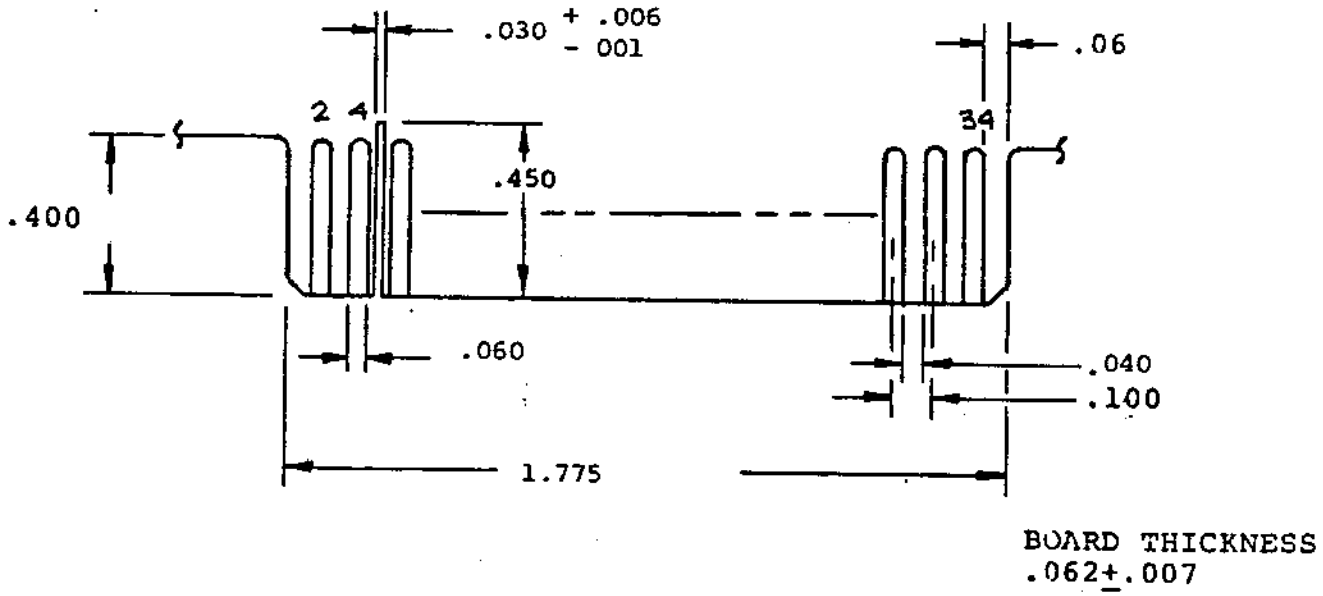
FIGURE 13

INTERFACE CONNECTOR PHYSICAL LOCATIONS



5.1 J1/P1 Connector - Control Signals

Connection to J1 is through a 34 pin PCB edge connector. The dimensions for this connector are shown in Figure 14. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the DC Power connector J3/P3 and is labeled. A KEY SLOT is provided between pins 4 and 6. The recommended mating connector for P1 is AMP ribbon connector P/N 88373-3. All odd pins are ground.



Unless noted, .XX = ± .030, .XXX = ± .010

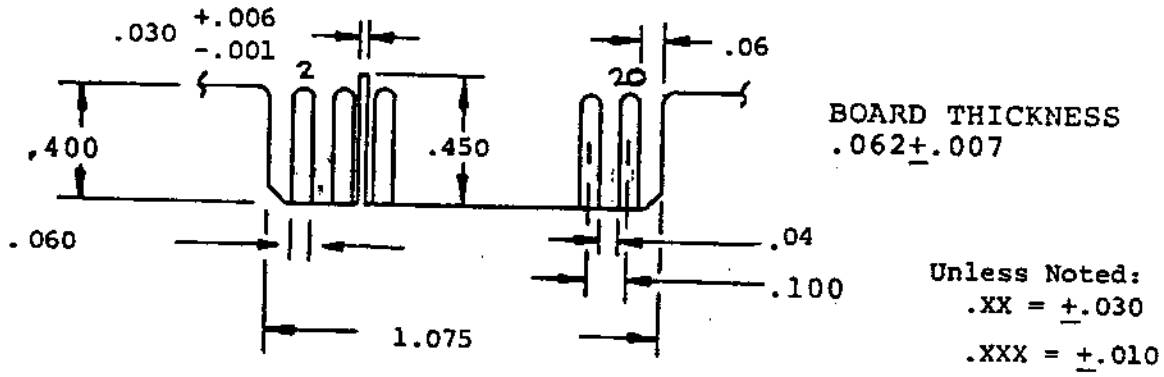
Figure 14 J1 Connector dimensions

5.2 J2/P2 Connector - Data Signals

Connection to J2 is through a 20 pin edge connector. The dimensions for the connector are shown in Figure 15. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6.

A key slot is provided between pins 4 and 6.

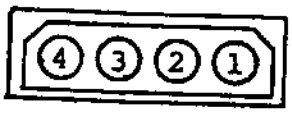
Figure 15: J2 Connector Dimensions



5.3 J3/P3 Connector - DC Power

DC power connector (J3) is a 4 pin AMP Mate-N-Lok connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4. J3 pins are numbered as shown in Figure 16.

Figure 16: J3 Connector - Drive PCB Solder Side

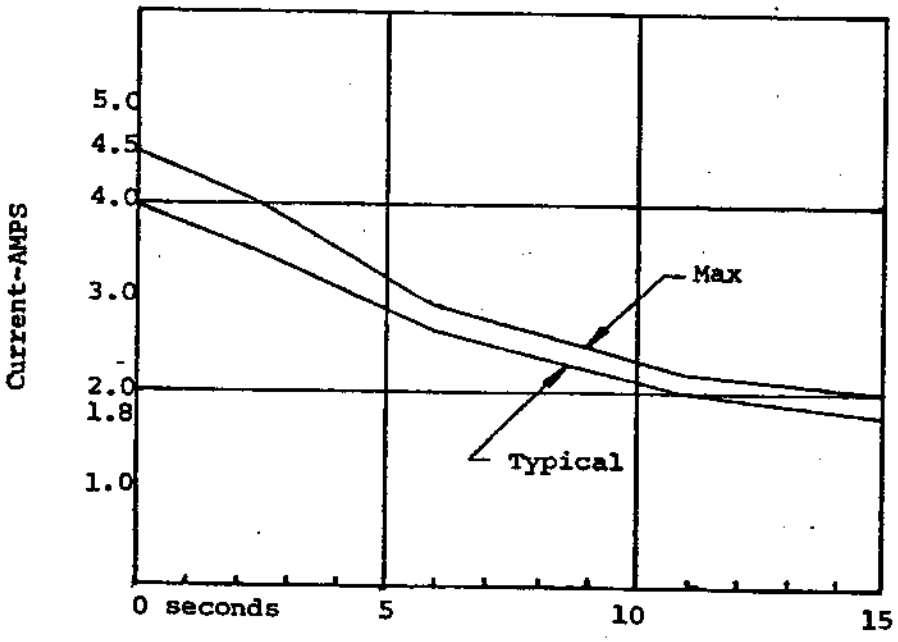


Current requirements and connector pin numbers are shown in Table IV.

J3 Connector	Current AMPS	
	Max	Typ
Pin 4 +5 Volts DC ± 5% Pin 3 +5 Volt Return	1.0	0.7
Pin 1 +12 Volts DC ± 1 5%* Pin 2 +12 Volt Return	4.5**	1.8

* ±10% on power unit or seeking, ±5% for READ or WRITE.
** Occurs only during power up, per curve below.

Table IV: DC Power Requirements



+12V current power up cycle

5.4 J4/P4 Frame Ground Connector

Faston AMP P/N 61761-2

Recommended mating connector AMP 62187-1

Note that DC logic ground in the Printed Circuit Board is not connected to frame ground. Use of the frame ground connection is very important to reduce ground loops and noise problems which may cause excess errors.

If used, the hole in J4 will accomodate wire size of 18 AWG max.

6.0 Physical Specifications

This section describes the mechanical dimensions and mounting recommendations for the ST506.

6.1 Mounting Orientation

Recommended orientation is either vertical on either side or horizontal with PCB down. The only prohibited orientation is horizontal with PCB up (disk surface down, parallel and next to mounting surface). In the final mounting configuration, insure that operation of the four shock mounts which isolate the aluminum base casting from the frame is not restricted.

6.2 Mounting Holes

Eight mounting holes, four on bottom and two on each side are provided for mounting the drive into an enclosure. The size and location of these holes, shown in Figure 17, are identical to the industry standard minifloppy drive.

6.3 Physical Dimensions

Overall height/width/depth and other key dimensions are shown in Figures 17 and 18. As in the case of the mounting holes, the dimensions are identical to the minifloppy, allowing a direct physical replacement.

6.4 Shipping Requirement

During shipping the heads shall be positioned on track 152 to eliminate the possibility of damage. This shall be done while the discs are spinning.

FIGURE 17

MOUNTING PHYSICAL DIMENSIONS

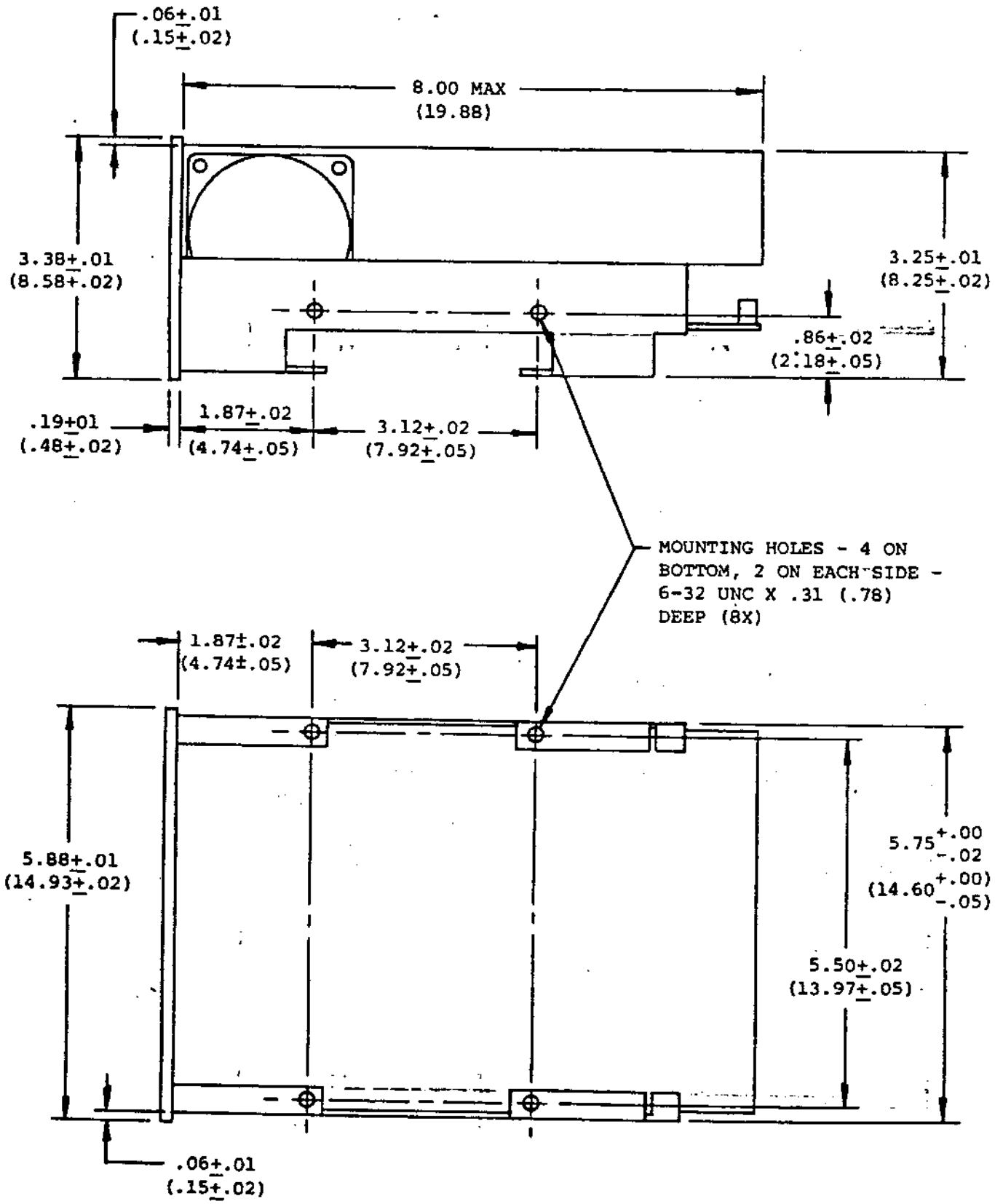
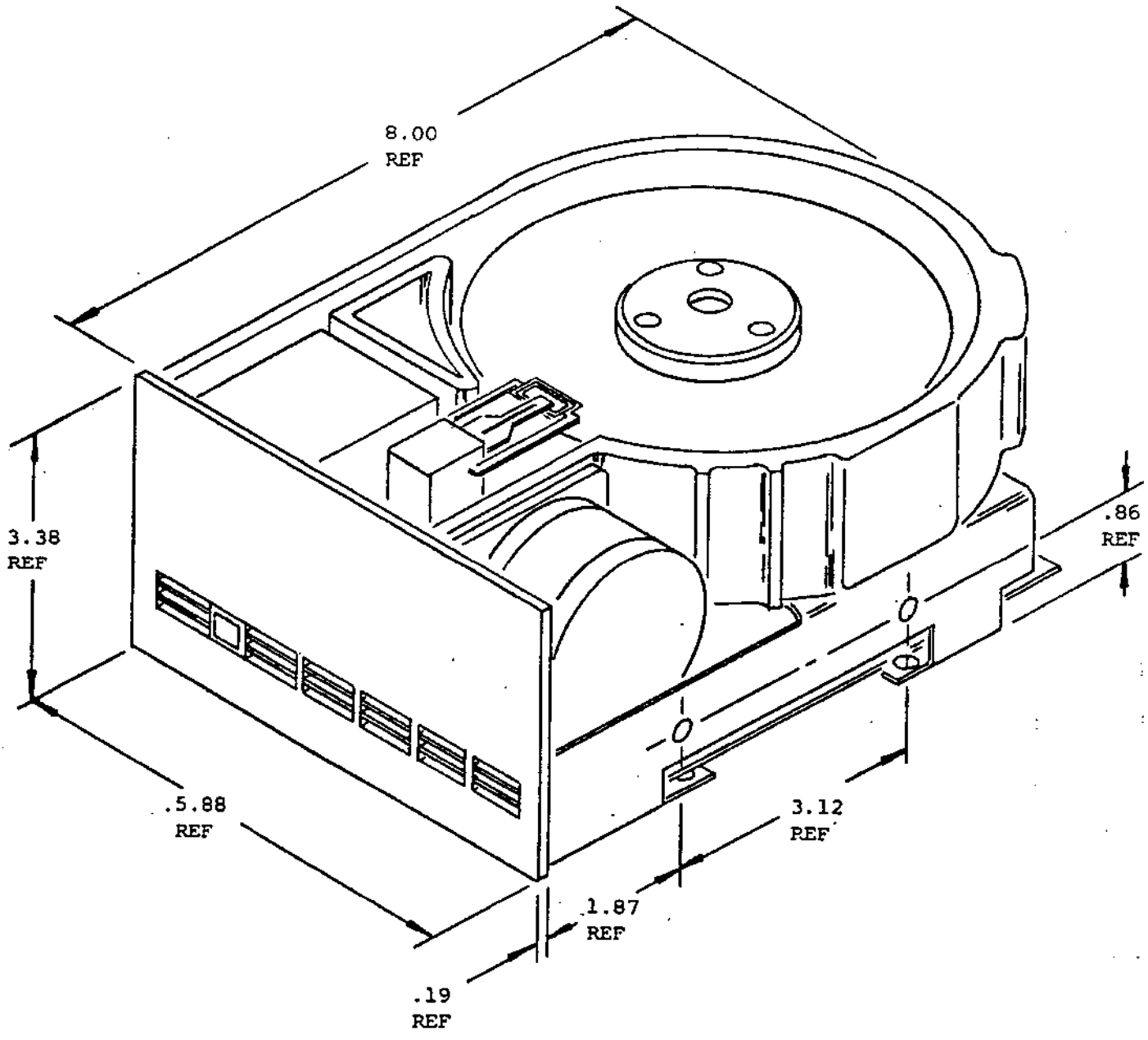


FIGURE 18

OVERALL PHYSICAL DIMENSIONS



7.0 ST506 Track Format

The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors. The ST506 format is a soft sectored type which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field.

The format is a slightly modified version of the IBM System 34 double denisty format which is commonly used on floppy disk drives. The encoding method is Modified Frequency Modulation (MFM).

Figure 19 shows the track format as shipped. 8192 bytes are available on each track, based on 32 sectors, each having 256 bytes of user data.

The beginnings of both the ID field and the data field are flagged by unique characters called address marks. An address mark is two bytes in length. The first byte is an "A1" data pattern. This is followed by either an "FE" pattern for an ID address mark, or an F8 pattern for the data address mark.

The "A1" pattern is made unique by violating the encode rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination that could occur on the track. See Figure 20 for make up of the "A1" byte. Each ID and data field are followed by a 16 bit cyclic redundancy check (CRC) character used for data verification. Each CRC character is unique for a particular data pattern.

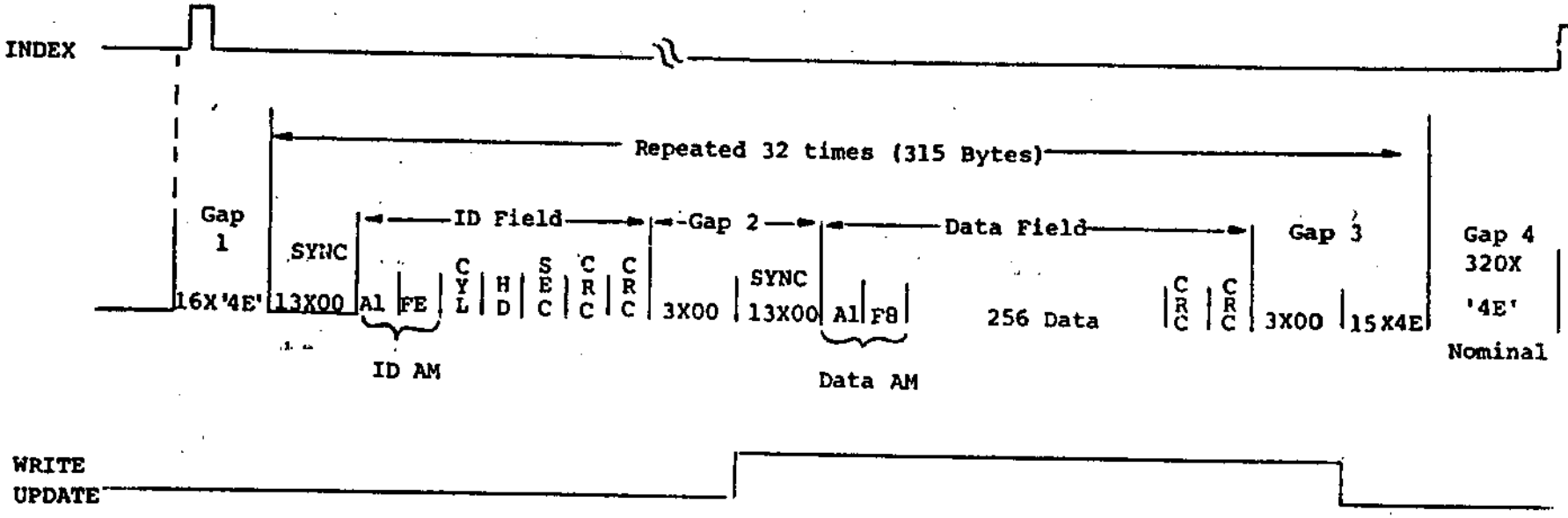
Surrounding the ID and data fields are gaps used to establish physical and timing relationships between these fields.

7.1 Gap 1

Gap 1 is to provide a head switching recovery period so that when switching from one head to another, sequential sectors may be read without loosing a disk revolution. Additionally, gap 1 provides for variations in Index. As shipped, gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field prior to the ID field of the first sectors.

7.2 Gap 2

Gap 2 follows the CRC bytes of the ID field, and continues up to the data field address mark. It provides a known area for the data field write update splice to occur. The latter portion of this gap serves as the sync up area for the data field AM. As shipped, gap 2 is 16 bytes. Minimum length required is determined by the "lock up" performance of the phase-lock-loop in the data separator, which is part of the host control unit.



NOTES:

1. Nominal Track Capacity = 10416 Bytes
2. CRC Fire Code = $X^{16} + X^{12} + X^5 + X^0$
3. Bit 7 of Head Byte ID Field equals 1 in a defective sector (Cylinder Ø is error free)
4. Total Data Bytes/Track = 256 X 32 = 8,192
5. Sector interleave factor is 4. Sequential ID Fields are sector numbered 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26, . . . etc.
6. Data Fields contain the bit pattern 0000 as shipped
7. Bit patterns shown are hexidecimal

Figure 19 Track Format As Shipped

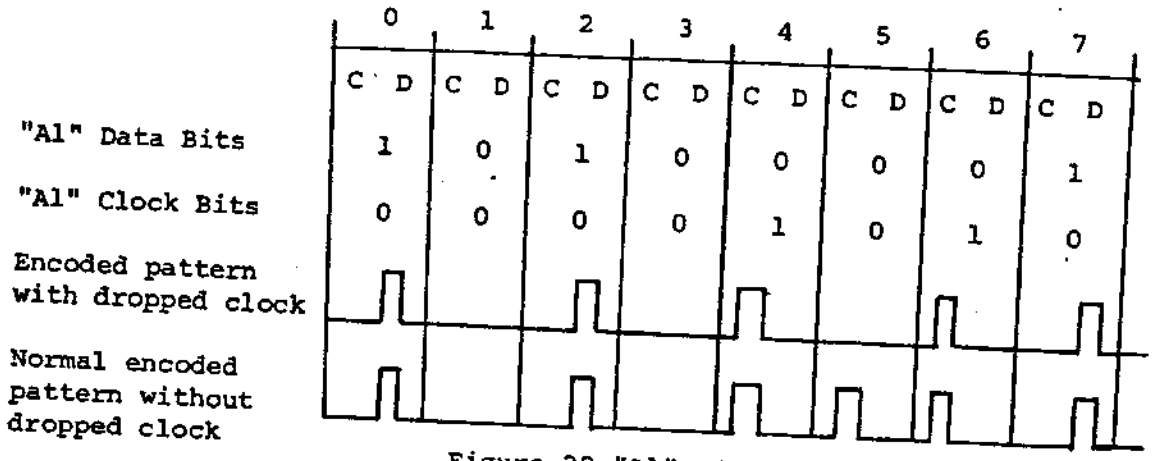


Figure 20 "A1" Address Mark Byte

7.3 Gap 3

Gap 3 following each data field allows for spindle speed variations. This allows a situation where a track has been formatted while the disk is running slower than nominal, then write updated with the disk running faster than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field could be over written. As shipped, the gap allows a ± 3% speed variation. (Actual drive spec is ± 1%) Minimum gap is 8 bytes for a 256 byte record size.

7.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes the ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depends on the exact rotating speed during the format operation.

7.5 Sector Interleaving

As shipped, the track format uses an interleave factor of 4. That is, sequential sector ID numbers are 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26, etc. This allows sufficient system turnaround time to process multiple sectors during a single revolution, thus enhancing through-put of typical file write/read operations.

7.6 Defective Sector Flags

As shipped, any sector which is considered marginal for data recording or which has permanent defect, will be indicated by the presence of a 1 bit in bit position 7 of the head byte in the ID field.

In addition, a printout will be provided with each drive which lists the location of these same defects in terms of head number, cylinder number, and bytes from index.

Testing for defects involves an analysis of the total media surface under marginalized test conditions.