SERVICE LETTER

DATE: September 23, 1974

NUMBER: DK3024

SUBJECT:

D3000 INTERMITTENT DATA ERRORS

SYMPTONS:

Intermittent data errors on all surfaces. Over several months of service activity at this account, heads and read/write PCBA's were replaced which at the time seemingly corrects this marginal problem. On a few occasions, the problem appeared to follow the head when connectors were swapped adding more credence to a possible head failure.

CAUSE:

(Prime, Eastern Region) designed their interface in such a manner that the write clock was on, all the time. The result was 2.5 MHz RF noise on the interface.

Close examination of the data error problem by our Q.A. Engineering staff revealed that the 2.5 MHz noise was primarily responsible for the high error rate. The noise was not gated and approximately 25 MV of 2.5 MHz signal could be measured at the emitter of transistor Q28.

Grounding the write clock driver significantly reduced the presence of noise at the read amp, as did tying signal ground to chassis ground. An all night test was run first with the write clock driver grounded and then later with the write clock driver grounded and the R/W PCBA signal ground tied to chassis ground. Under the former conditions, there were two errors (probably when the building lights were turned off). Under the latter conditions, there was one error (probably when the lights were turned on in the morning).

The customer has added a change to their controller, gating the write clock. The following data determines the degree of noise reduction with both of the remediable approaches (Q28 emitter):



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- No signal ground, continuous write clock, noise = 25MV.
- 2. No signal ground, gated write clock, noise = 12.5MV.
- 3. Signal ground, gated write clock, noise = 5MV.
- 4. Computer and controller power off, no signal ground, noise = 10MV.

GATING of the write clock reduced the data error rate to an acceptable level. However, it was decided to leave the braided signal to chassis ground, since the ground showed a significant reduction in noise not necessarily associated with the 2.5 MHz write clock.

CURE:

A braided ground strap is jumpered between the Read/Write PCBA Power Supply ground installed at hole adjacent to CR 34 and to the positioner current insulating strip mounting screw.

It was Pertec's decision to ECN the topbill on D3000's for Prime Computer. In this way, all future drives of their configuration would ship with the ground strap installed as a result of this unique account problem.

Today's position is one of which the jumper strap has been evaluated by Engineering and disapproved at this time for the entire product line.

If in certain conditions observation is made of intermittent data errors which are caused, REPEAT, caused by RF noise from the customers interface being coupled into the drive, a very remote solution could be a jumper

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strap. We must caution each of you, however, in that such an action may result in potential liability to Pertec: i.e. the inclusion of this change on all of the customers products. This is not to say that Pertec would not install a strap should it become necessary. It is simply that we must be absolutely convinced from a Q.A., Engineering, and Marketing standpoint that the source of these intermittent data errors is RF noise and ground strap is in fact a reasonable solution. If it becomes necessary to try the ground strap technique, notify Product Support immediately.

In summary, your need for such an approach to intermittent data errors would be extremely remote. We are confident that our service organization can execute the proper judgement so as not to expose Pertec to any unneccessary liability.