DYNAMIC RAM CARD

Model WH-8-64

595-2768-01

HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

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INTRODUCTION

The WH-8-64 Dynamic RAM Card supplies the H-8 Computer with a maximum of 64k of memory on one card.

The Dynamic RAM Card comes supplied with 32k of RAM, and has room for an additional 32k. Because all 64k of memory can now be placed on only one card, you can use the extra space in your H-8 Computer for other cards, such as a color generator, disk controllers, and other I/O devices.

You can also configure the RAM in many ways with the switches located in the center of the RAM Card. These switches allow you to choose which banks of memory will respond to which range of addresses. This capability is useful in troubleshooting or in configuring your additional memory around existing memory.

Power requirements for the RAM Card are vastly reduced from the requirements of earlier H-8 RAM cards. While the older 8k cards needed up to 1.5 amperes for 16k of memory or less, this card needs only 750 ma with all 64k of memory installed.

All of the information you need to use the features of the RAM Card is contained within this Manual. Please read it carefully before attempting to use your WH-8-64 Dynamic RAM Card.

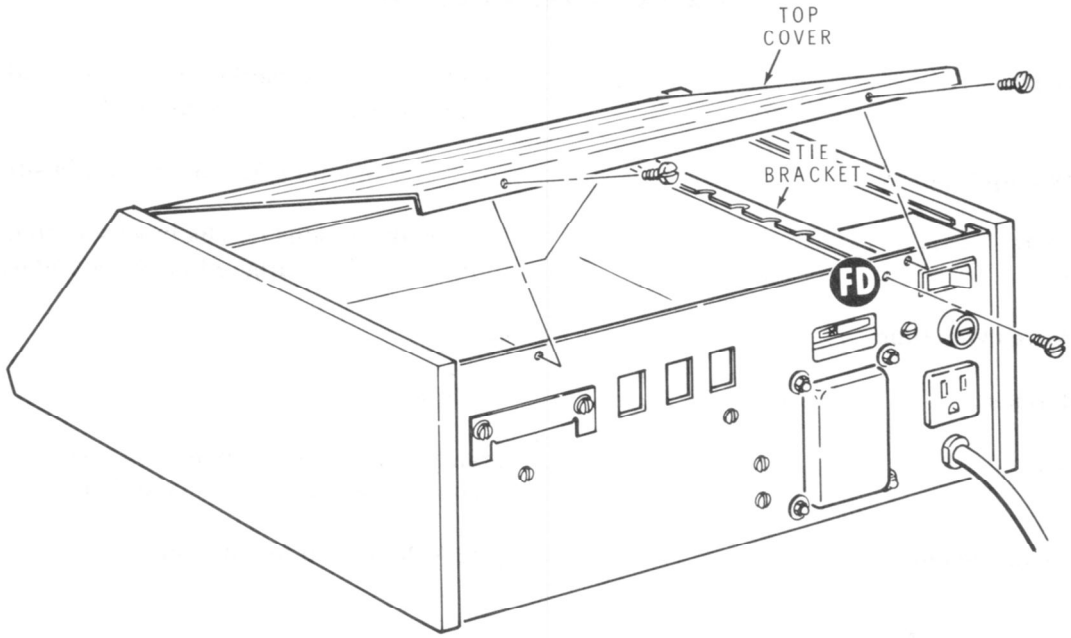
SPECIFICATIONS

Memory size	65,536 × 8 in 4 banks of 16,384. Banks 0 and 1 supplied. Banks 2 and 3 optional.
Memory chip type	16k × 1 dynamic RAM. 5-volt single supply.
Addressing	Each bank contains two 8k blocks, each of which are independently addressed on 8k boundaries.
Read/Write cycle time	450 ns.
Bus interface	Heath H-8.
Refresh	Transparent, synchronized with signal M1. Asynchronous refresh in absence of M1.
Power requirements	7-12 VDC @ 750 ma maximum.

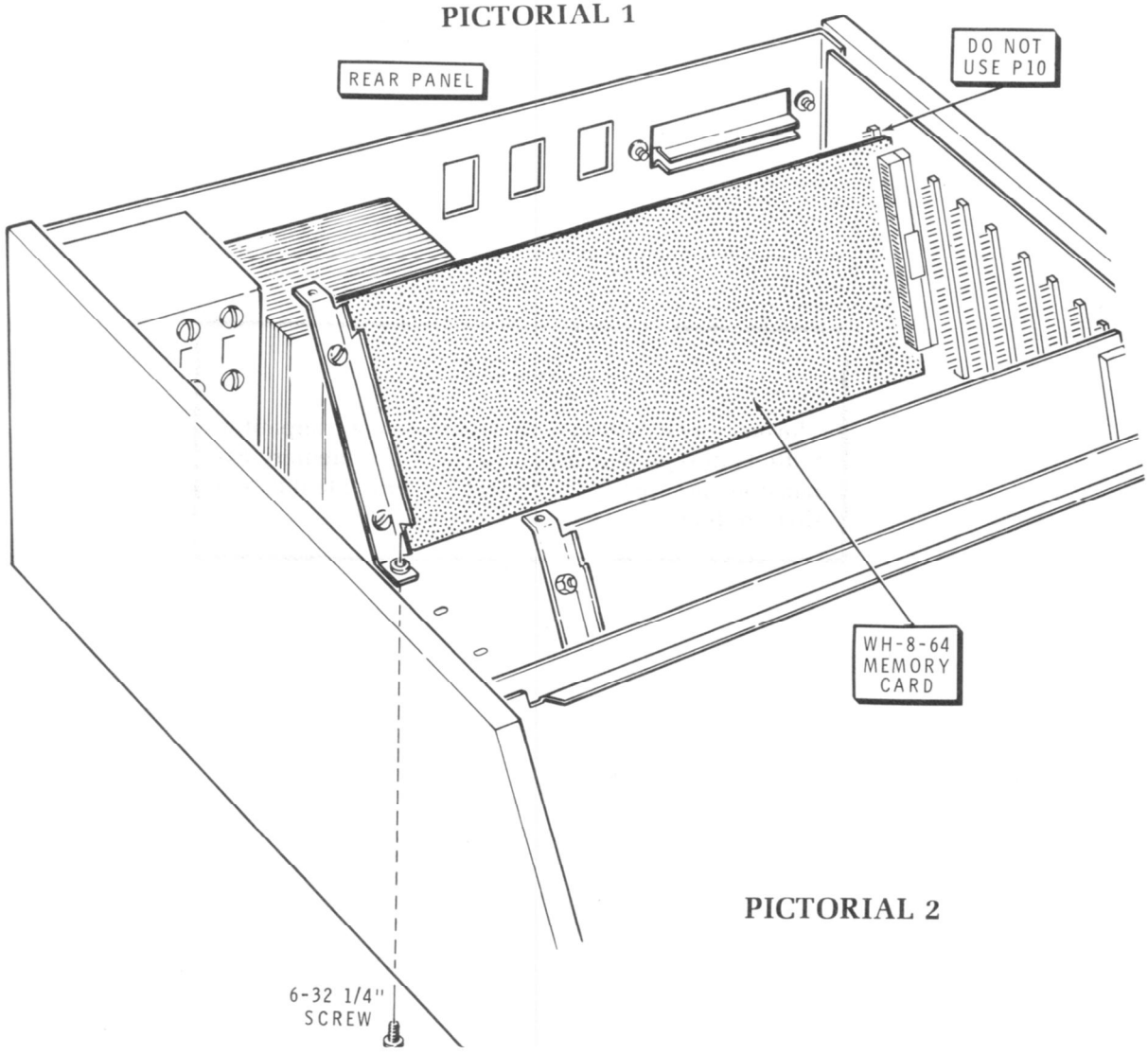
CAUTION

The memory IC's used in this Card are not compatible with 4116-type IC's commonly sold for memory expansion. Be sure to use only 4517 or equivalent IC's in this product.

INSTALLATION



PICTORIAL 1



PICTORIAL 2

Refer to Pictorial 1 for the following steps.

( ) Be sure your Computer is turned off.

( ) Remove the two rear panel screws holding the top cover and set the top cover aside if this has not already been done.

( ) Remove rear panel screw FD. Then loosen the other screws in the tie bracket, remove the bracket, and set it aside.

Each 16k bank of memory on your RAM Card must be assigned addresses. This is accomplished by setting switches SW1 through SW4. Each switch corresponds to a memory bank as follows:

SW	BANK
1	3
2	2
3	1
4	0

Your RAM card normally comes equipped with 32K of memory. These 32K of memory are located in banks 1 and 0, which are addressed by switches SW3 and SW4.

SW3 and SW4 are factory-set as follows:

SW3		SW4	
slide	1-2 — Off	slide	1-2 — On
slide	3-4 — On	slide	3-8 — Off
slide	5-8 — Off		

This arrangement places bank 1 in the 16-32K address block, and bank 0 in the 0-16K address block.

SLIDE NO.	ADDRESS BLOCK	OCTAL ADDRESSES	HEX ADDRESSES
1	0- 8K	000.000-037.377	0-1FFF
2	8-16K	040.000-077.377	2000-3FFF
3	16-24K	100.000-137.377	4000-5FFF
4	24-32K	140.000-177.377	6000-7FFF
5	32-40K	200.000-237.377	8000-9FFF
6	40-48K	240.000-277.377	A000-BFFF
7	48-56K	300.000-337.377	C000-DFFF
8	56-64K	340.000-377.377	E000-FFFF

Table 1
Memory Bank Addressing.

You may change these settings if you wish. The definition of each switch slide is given in Table 1. Set only two switch slides per switch.

As an example of how to assign addresses, assume that your system has no other memory installed and that you are using Heath software. You may then set the switches as follows:

SW4		SW3	
slide	1 — Off	slide	1 — Off
slide	2-3 — On	slide	2-3 — Off
slide	4-8 — Off	slide	4-5 — On
		slide	6-8 — Off

SW1 and SW2 should be off.

The above setting will assign the addresses 040.000 to 137.377 (8k to 24k) to bank 0, and addresses 140.000 to 237.377 (24k to 40k) to bank 1. Addresses 000.000 to 037.377 (0 to 8k) are reserved for the system and disk memory, and should not be assigned to a RAM board unless the Extended Configuration Option or the Z-80 CPU board is in use.

The switch settings you use depend on the amount of memory your system has and on your own personal preference. Please read the portion of the Circuit Description concerning address assignments for a clearer understanding of how to set these switches.

( ) Set addressing switches SW3 and SW4.

( ) Be sure a jumper is positioned between E8 and E9 if you have an 8080 CPU, or between E6 and E7 if you have a Z-80 CPU.

( ) Refer to Pictorial 2 and plug your WH-8-64 RAM Card into any unused slot from P3 to P9 in the H-8 Computer.

( ) Install a 6-32 × 1/4" screw through the bottom of the computer chassis to hold the card in place.

( ) Replace the tie bracket and top cover as shown in Pictorial 1.

CIRCUIT DESCRIPTION

Refer to the block diagram of the WH-8-64 RAM Card shown in Pictorial 3 as you read the following description.

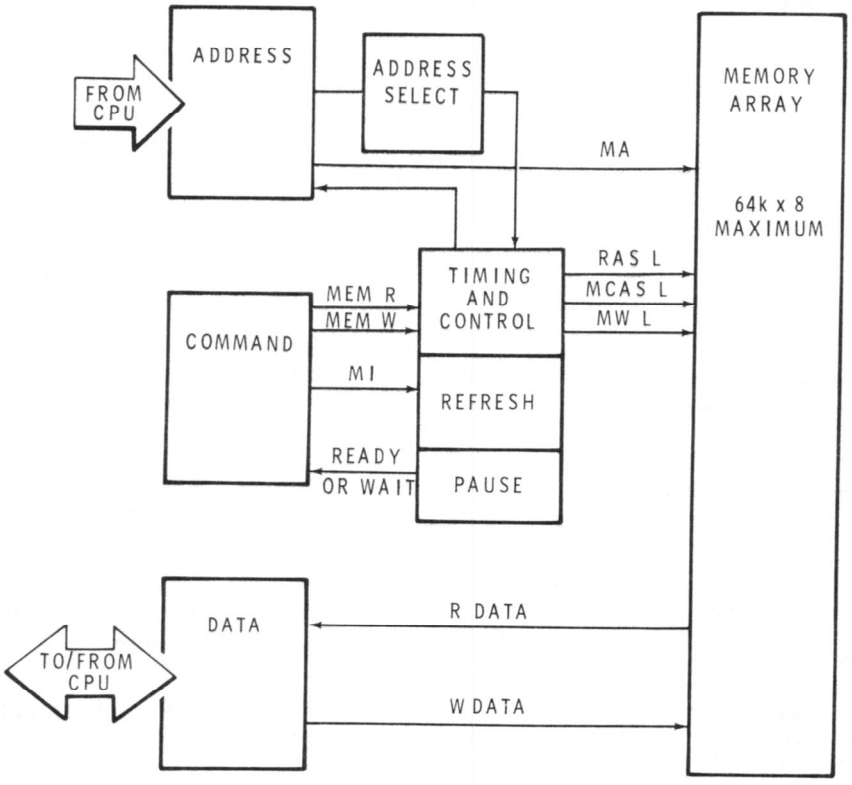
The RAM Card receives address information from the CPU on a 16-bit bus. The information is buffered and latched by the "address receive" portion of the card, then sent on directly to the memory array in two "pieces". The first 7-bit piece tells the array which row is being sought, while the second 7-bit piece tells the array which column is wanted. The two remaining bits, as well as the most significant row bit, tell the array which block of 16k memory is to receive the row and column information. The array receives the block-select bits through the "address select" and "timing and control logic" portions of the card, where the signals are decoded for the array.

Read and write commands are buffered by the "command" portion of the card, where they are sent to be decoded by the "timing and control logic." "Timing and control logic" then sends the information to the array.

The "command" portion also receives the wait signal from the "pause logic." The wait signal tells the CPU that the memory is busy performing a refresh cycle.

The "refresh logic" portion of the card refreshes memory automatically either during a memory read cycle or on its own without a memory access from the CPU.

Finally, the "data" portion of the card buffers and latches the data as it is read or written.



PICTORIAL 3

Please refer to the schematic when reading the following.

ADDRESS LOGIC

The address lines 0 to 15 are buffered by the U62 and U63 receivers. The address signals are latched by U54, U55, and U65. Signal ADD LATCH L, the result of READ ORed to EARLY WRITE, keeps the address signals latched until the end of the read or write operation. If a refresh cycle is in process at the time a read or write signal is issued, the latches keep the address information stored so that the memory can respond to the read/write signals at the end of the refresh cycle.

The outputs of U54 and U55 are common to allow address multiplexing. U54's MA output signals are enabled during the address row search by MSXH not asserted. When MSXH becomes asserted, U54's outputs are disabled and U55's outputs are enabled so that the address column search can begin.

During a refresh cycle, both U54's and U55's outputs are disabled, and the refresh address is placed on the MA bus via U53.

Address lines 13 to 15 are latched by U65. They are used for module select via decoder U48 and switches SW1 through SW4.

The memory array is organized into four banks of 16k each. Each 16k bank is divided into two 8k parts. Switches SW1 through SW4 assign addresses to each 8k block of memory. For example, SW1 slide 1 assigns the address block 000.000 to 037.377 (octal) to bank 3, part 1. Table 1 shows other switch settings.

CAUTION

You should not assign more than one memory bank to the same address. For example, both SW3 and SW4 could be set identically; both banks would then respond to a memory operation simultaneously. This is not recommended because of uncertain loading and timing effects.

Unless you are using the HA-8-8 Extended Configuration Option or the HA-8-6 Z-80 CPU board, do not assign addresses 0 to 8k to RAM.

The bank select SEL B*L outputs (from 0 to 3) enable the row address select signals (that is, the RAS signals) via U35. The signals are then ORed through U41 to form MEMSLH. Provisions for using up to 16 WH-8-64's in a 1-megabyte address space are provided via J1, SW5, and U60. However, Heath does not support extended addressing at this time, and this part of the Board is supplied unpopulated. Table 2 shows the SW5 switch settings for this expanded memory case. Note that J1 is used for the external address or module select lines. These lines do not originate on the bus.

SW5 POSITION	64K CARD NUMBER (PAGE)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	X	O	X	O	X	O	X	O	X	O	X	O	X	O	X	O
2	X	X	O	O	X	X	O	O	X	X	O	O	X	X	O	O
3	X	X	X	X	O	O	O	O	X	X	X	X	O	O	O	O
4	X	X	X	X	X	X	X	X	O	O	O	O	O	O	O	O

X = ON
O = OFF

Table 2
Memory Expansion Option.

MEMORY COMMANDS

Input signals MEMR, MEMW, ϕ2, RESET, and M1A are buffered by U64. The MEMW line is clocked by ϕ2 on the memory board. However, because of the close proximity of ϕ2 to MEMW, the MEMW signals may cause glitches on ϕ2 during the MEMW transitions. RC combination R28 and C53 minimize the effects of this coupling.

The MEMR signal starts a read cycle in memory when high and clears latch U49 when low. When used with the Z-80 processor, access time is not critical; therefore, jumper E6 to E7 should be installed. This allows the MEMR signal to be clocked by the leading edge of ϕ2 for use within the memory module. Clocking the MEMR signal minimizes the likelihood of false reads occurring because of noise on the MEMR signal.

With the 8080 processor, access time is critical. The added delay caused by using the latch U49 is too great; therefore, jumper E8 to E9 should be installed and jumper E6 to E7 removed.

MEMRH is ORed with SMEMWH at U42 pins 9 and 8. It is then ANDed with MEMSEL L to initiate the memory cycle. MEMRH is also gated with MEMSRL H at U41 to enable the output data buffer U43. U41, pin 8, forms SELECTED MEMR, which is subsequently gated with the early write signal to latch the incoming address.

The MEMW signal requires special conditioning in both 8080 and Z-80 applications. The 8080 MEMW signal occurs well before data is valid; therefore, the memory must wait until data becomes valid before initiating the write cycle. The Z-80 MEMW signal is much narrower than that of the 8080, so that if a refresh is starting just before a MEMW signal occurs, the MEMW pulse width will not allow the memory to complete its cycle before the MEMW becomes not asserted. In the case of the Z-80, the input data must be latched and the internal write pulse must be lengthened. This guarantees that data and address will remain latched until the memory cycle is completed.

MEMW is passed through a short RC filter to minimize edge coupling into ϕ2. It is buffered by U64 and then gated with memory select at U40. U56 pin 6 forms the E WRITE L (early write) signal that latches the address. It also prevents new refresh cycles from beginning once a selected MEMW occurs.

Selected MEMW is clocked into U66 pin 12 by the next rising edge of ϕ2. The Q output of U66 starts the memory write cycle via U56, pin 12. This edge also latches DATA IN from the bus at U38, pins 1 and 11. If the memory is doing a refresh cycle when SMEMWH occurs, the write command is stretched by clocking into U66, pin 2, at the next rising edge of ϕ2. U66 is always cleared via U50, pin 3, by CYLKH, or by the trailing edge of MEMW from the bus. CYLKH, generated by the trailing edge of CAS, indicates the completion of a memory cycle.

MEMORY CYCLE CONTROL LOGIC

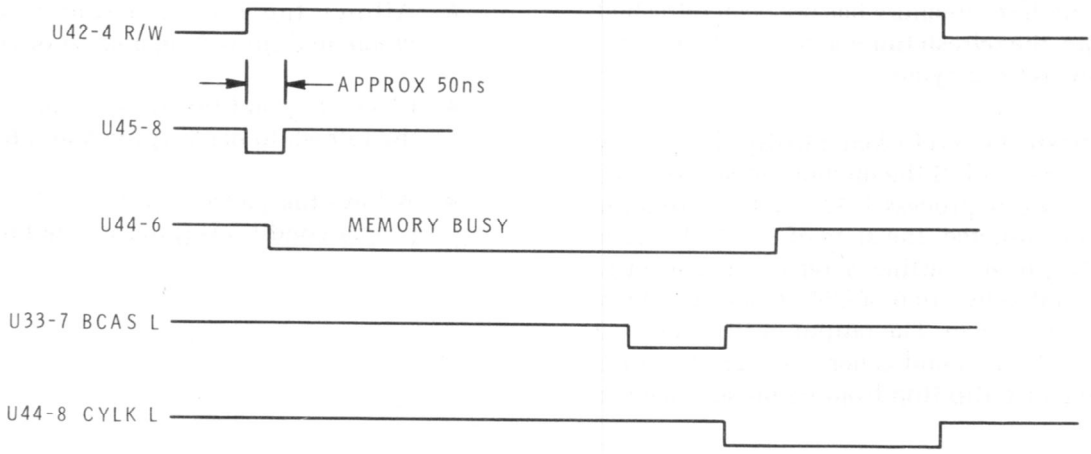
The memory module determines whether to perform a normal memory cycle or a refresh cycle when there is contention between the two operations. U45 is the control element. Its pin 12 receives read/write cycle inputs while its pins 2 and 3 receive refresh cycle inputs. In general, if a refresh cycle request occurs simultaneously with a memory cycle request, the memory performs the refresh first. Once a cycle is in process, no other cycle requests are honored until completion of the current cycle.

Read/Write Cycle

The request to perform a read/write cycle (via U42, pin 4) is executed if the memory is not busy, that is, if U45, pin 13, is high. When pin 12 of U45 is asserted (high), pin 8 is asserted (low). This sets U44, pin 5, causing a pulse to propagate down delay line DL1. U44, pin 6, is set low, causing a low on pins 1 and 13 of U45. This locks out further requests while the memory is busy.

Near the end of the memory cycle, BCASL is generated on U33, pin 7. The trailing edge of BCASL sets the flip-flop at pins 8 and 9 of U44. This prevents pins 10 and 11 of U45 from accepting further read/write requests from U42. Therefore, memory can not perform multiple read/write cycles because of a wide read/write pulse.

At the end of the read/write signal from pin 4 of U42, the flip-flop at pin 8 of U44 is reset, enabling U45. Refer to Pictorial 4.


U42-4 R/W
APPROX 50ns
U45-8
U44-6
MEMORY BUSY
U33-7 BCAS L
U44-8 CYLK L

PICTORIAL 4

Refresh Cycle

The memory normally operates under two refresh modes, mode 1 and mode 2.

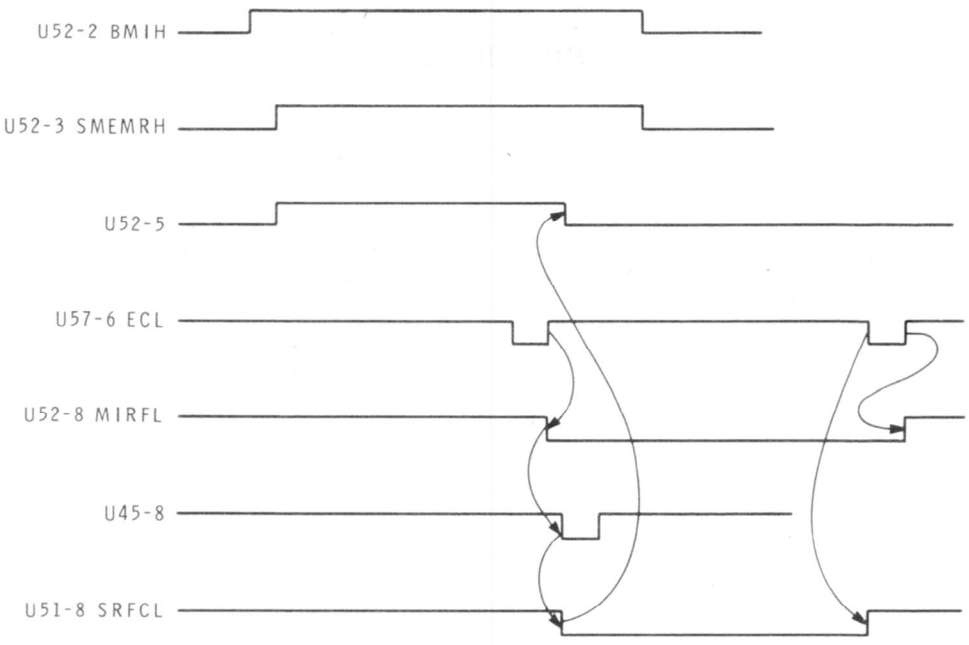
A mode 1 refresh causes memory to be refreshed each time the memory is selected during an M1 MEMR cycle. The refresh occurs after the memory read is completed. The memory refresh timer is reset whenever a mode 1 refresh occurs.

A mode 2 refresh occurs when the memory refresh timer times out. If the memory has not been refreshed for 12 to 16 μs, the refresh timer asserts pin 1 of U57, starting a new refresh cycle.

In mode 1 refresh, BMI is clocked into flip-flop U52 by selected memory read. If the memory is not selected or if no M1 cycle is in process, U52 is not set. After the read cycle is completed, the state of pin 5 of U52 is transferred to pin 8, starting a refresh cycle. ECL, which is generated by pin 6 of U57, clocks pin 11 of U52 during every cycle. The output of flip-flop U52 resets the refresh timer and generates M1RFL, which prevents the pause flip-flop from being set. Refer to Pictorial 5.

The refresh flip-flop performs a number of functions when set:

- Blocks CAS to the memory array (pins 4, 5, and 6 of U40).
- Disables address from the MA bus (pins 11, 12, and 13 of U57).
- Enables refresh address to the array (pins 8, 9, and 10 of U58).
- Allows the refresh counter to be incremented (pins 8, 9, and 10 of U58).
- Clears the conditional flip-flops that caused the refresh to occur (pins 5 and 6 of U51).
- Allows the pause flip-flop to be set under proper conditions (pins 4, 5 and 6 of U58).



PICTORIAL 5

Refresh Timer

The refresh timer consists of U67, a dual monostable. The timer is self-starting and is enabled when pin 9 of U52 is low (the reset condition). Pin 5 of U67 is normally high until it times out. The descending edge of the signal at pin 5 of U67 triggers pin 4, which in turn triggers pin 5. R24 and C56 set the length of the signal at pin 5 to about 12 μs.

Refresh Counter

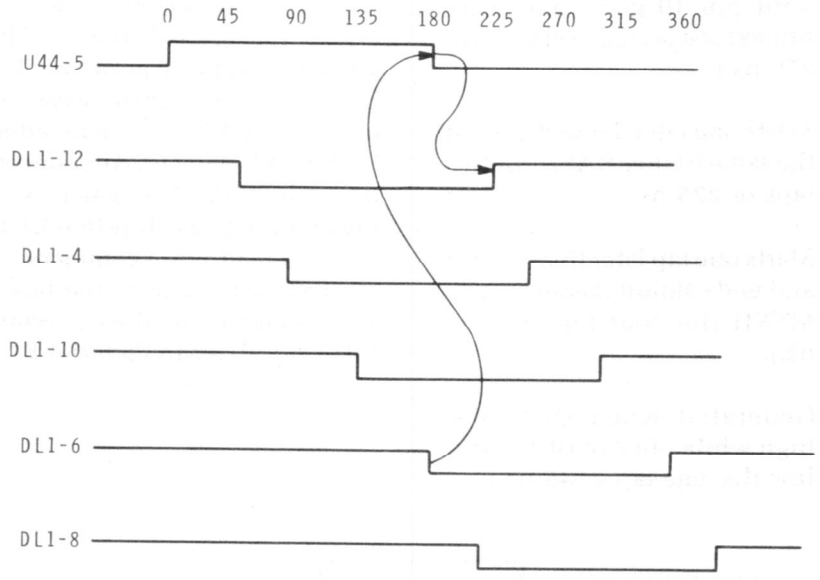
The refresh counter, U61, is incremented after each refresh cycle to refresh each of 128 row addresses.

Memory Cycle Timing

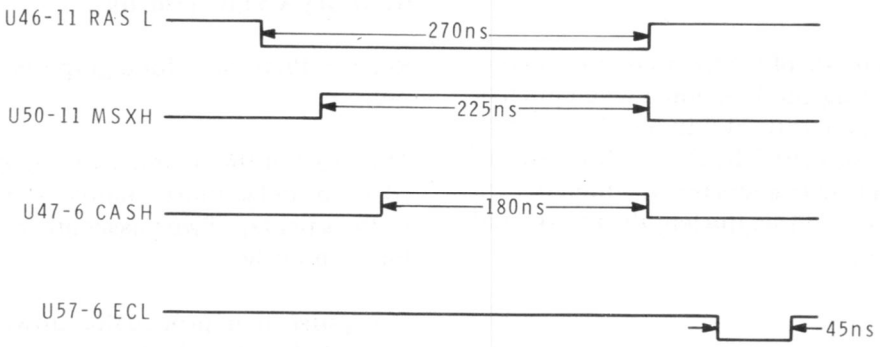
Refer to Pictorial 6 for a graph of memory cycle timing.

The heart of the memory timing circuit is delay line DL1. The delay line contains five taps; there is a delay of 45 ns per tap. Two passes are made through the line for each cycle.

The pulse that propagates down the delay line is generated by U44 being set. Tap 4 of the delay line (pin 6) is fed back to the clear input of U44, causing a positive edge to propagate down the line.



PICTORIAL 6



PICTORIAL 7

Timing Terms

Refer to Pictorial 7 for an illustration of the following timing signals.

RASL (pin 11, U46) Generated when DL1, pin 12, becomes low and continues until pin 10 goes high (continues for a period of six taps or 270 ns.).

MSXH (pin 11, U50) Starts one tap later and ends at the same time as RASL (for five taps or 225 ns.).

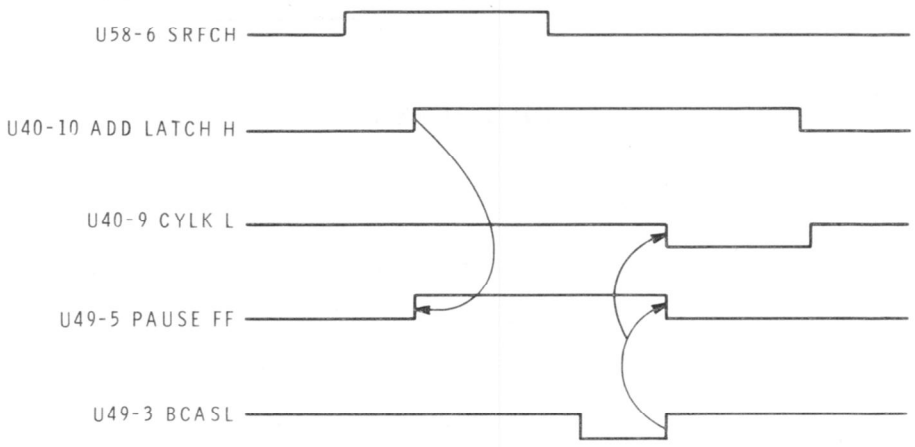
CASH (pin 6, U47) Starts one tap later than MSXH and ends simultaneously with MSXH (for four taps or 180 ns.).

ECL (pin 6, U57) Generated when DL1 goes high while pin 8 of DL1 is still low (for one tap or 45 ns.).

PAUSE FLIP-FLOP

The memory pause circuit consists of flip-flop U49, pins 4, 5, and 6 of U50, pins 4, 5, and 6 of U58, pins 8, 9, and 10 of U49, and pins 8, 9, and 10 of U50.

The pause flip-flop is set whenever a memory read or write request occurs while a refresh is in process, except during an M1 refresh. The pause flip-flop is set when pin 6 of U50 goes low. This occurs if SRFCH is high and M1RFL is not asserted (not an M1 refresh), and ADD LATCH H is asserted (ADD LATCH H = MEMR or E WRITE). After the memory has completed its cycle, CYCKL is gated with ADD LATCH H to prevent the pause flip-flop from being set during the end of a read/write command. The pause flip-flop is cleared by reset from the bus upon power up; it is always cleared by the occurance of a memory cycle. (BCASL). Refer to Pictorial 8.



PICTORIAL 8

GLOSSARY OF TERMS

$\overline{A}$	Address at the bus.
ADD LATCH H(L)	Signal used to latch address. Term consists of Early Write or Selected Memory Read.
B CASL	Buffered Column Address Select signal. Used to clear pause FF, set cycle lockout FF.
B MEMRH	Buffered Memory Read. Used to initiate Memory Read cycle. Gated with Memory Select to form Selected Memory Read.
B M1 H	Buffered M1. Used to initiate refresh after Read when memory is selected.
CASH	Column Address Select. Formed by memory timing. using to form all CAS related terms. Gated with refresh to indicate whether current cycle is memory or refresh cycle.
B	Data at the bus.
ECL	End Cycle. Generated by timing and used to clear refresh FF and M1 FF.
E WRITE H(L)	Early Write. Used to latch address and to lock out new refresh cycles from starting after leading edge.
M CAS L	Column Address Select to memory array.
MEMSEL H(L)	Memory Select. Consists of the OR of the 4-bank select terms. Used to enable the memory cycle.
MSXH	Address Multiplexer signal. Used to disable Row address and enable Column address.
MWL	Memory Write to memory array. Formed by selected Write and gated with refresh.
MA	Memory Address bus to memory array. Contains Row address, Column address or refresh address.
RAS L	Row Address Select to memory array. RAS0L corresponds to bank 0, etc.
RST L	Reset from Bus. Used to clear Pause FF and M1 FF.
RD	Data from memory array. Latched by back edge of CAS H.
SELB L	Memory Bank Select terms. Each bank can be selected to start on any 8K boundary via switches S3-S6. Used to select RAS terms.
SMEMRH	Selected Memory Read. Used to clock M1 to set up M1 refresh. Enables DATA OUT and latches address.
SMEMWH	Selected Memory Write (latched Write). Used to initiate memory cycle, to form MWL and to latch DATA IN from the bus.
SRFCH (L)	Start Refresh Cycle. Used to determine that current cycle is refresh cycle. Enables Pause FF, Refresh Counter Refresh Address; blocks MWL, CAS; diables Address Latches; clears M1 refresh latches, jam sets, all RAS signals simultaneously.
WD	Write Data to memory array.

IN CASE OF DIFFICULTY

If you installed your WH-8-64 RAM Card on an H-8 Computer that previously worked, check the jumper positions on the card. Then, check switches SW1 through SW4. Make sure the jumpers and switches are set as specified in the Installation section.

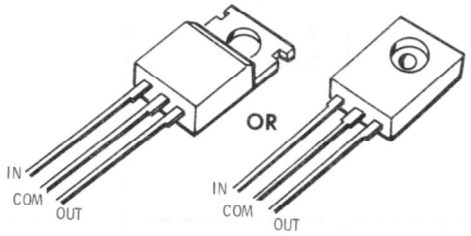
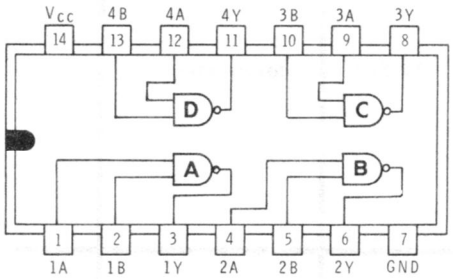
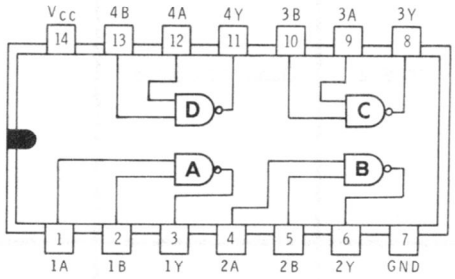
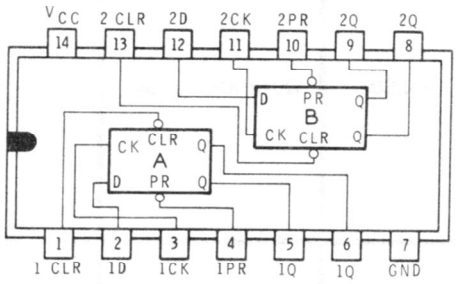
If you purchased the WH-8-64 RAM Card at the same time as the H-8 Computer, and the system has not yet functioned properly, refer to the H-8 Operation Manual for troubleshooting information.

If your RAM Card does not pass the dynamic RAM test listed in the H-8 Operation Manual, read the warranty supplied with your card. Then, either return the card to Heath, or, replace the RAM or RAMs that were assigned the addresses that were failing. You may wish to swap addresses between banks of memory to confirm that the suspected RAMs have failed. If you need to replace them, refer to the "Circuit Board X-Ray View" for the physical location of the RAMs on the card.

If all addresses fail, check to see if the card has been installed correctly. The card should be installed firmly on the plug. Make sure no pins on the plug are accidentally bent.

You may wish to see if the bus itself is intact. To do that, either inspect the bus card on the H-8 Computer, or perform a resistance check on the bus lines. Before you perform a resistance check, remove all circuit cards in the computer. Then, check for zero resistance between the pins of the plug to which you connected the RAM Card and the pins of the CPU card.

SEMICONDUCTOR IDENTIFICATION CHART

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
442-54	UA7805	5 V voltage regulator	
443-77	SN7438	Quad NAND gates	
443-728	74LS00	Quad NAND gates	
443-730	74LS74	Dual flip-flop	

Semiconductor Identification Chart (Cont'd.)

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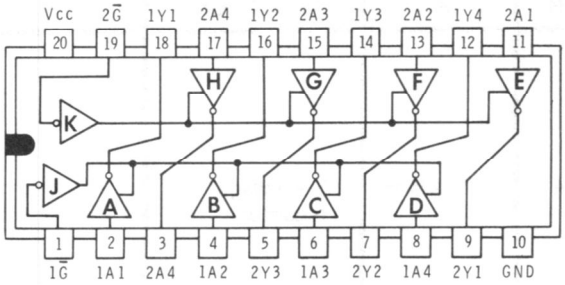
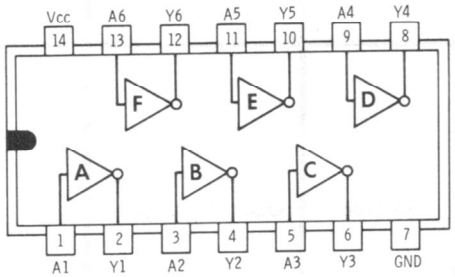
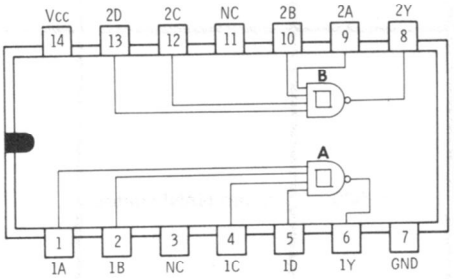
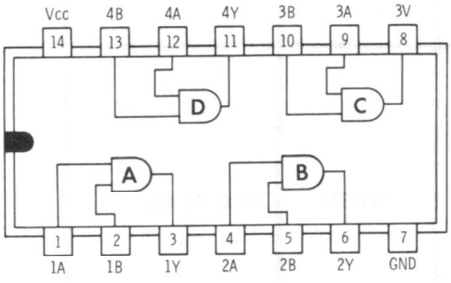
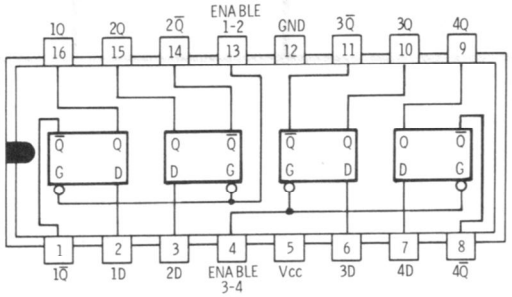
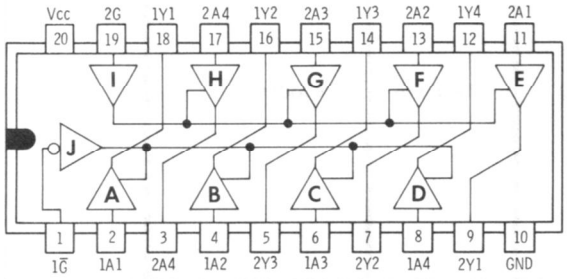
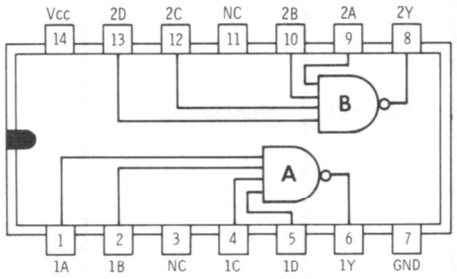
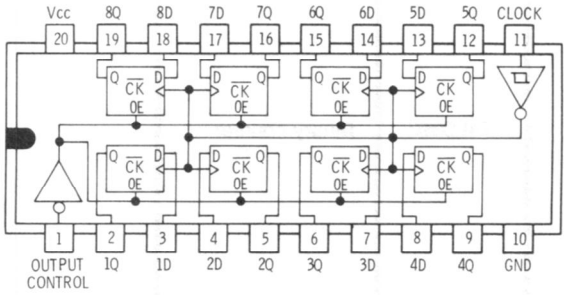
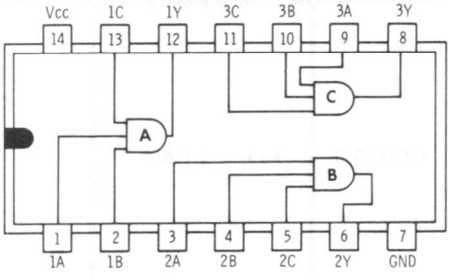
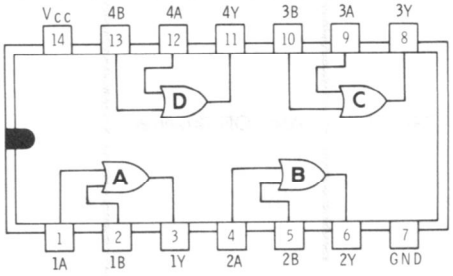
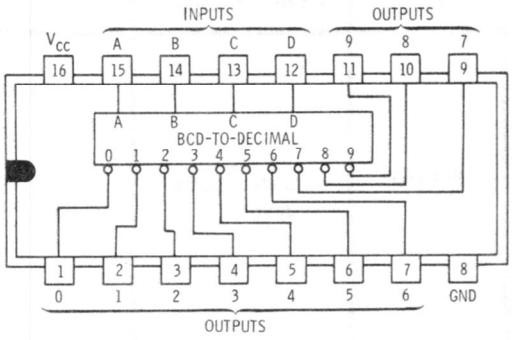
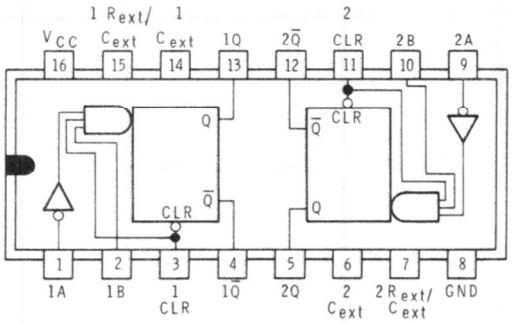
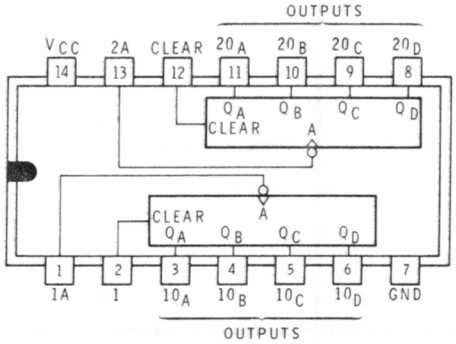
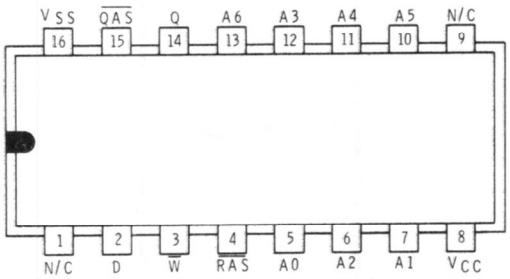
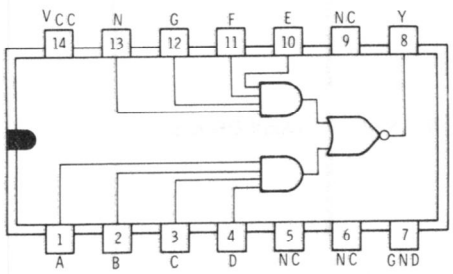
443-754	74LS240	3-state octal buffer	
443-755	74LS04	Hex inverter	
443-779	74LS02	Quad NOR gates	
443-780	74LS08	Quad AND gates	
443-781	74LS75	Latch	

Semiconductor Identification Chart (Cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-791	74LS244	3-state buffer driver	
443-798	74LS20	Dual NAND gates	
443-837	74LS373	3-state 8-bit latch	
443-864	74LS11	Triple AND gates	
443-875	74LS32	Quad OR gates	

Semiconductor Identification Chart (Cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-889	74LS145	Decoder	
443-942	74LS123	Multivibrator	
443-973	74LS393	Binary counter	
443-1005	MCM4517	16 k × 1 RAM	
443-1006	74LS55	AND/OR /Inverter	

REPLACEMENT PARTS LIST

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
RESISTORS		
All resistors are 1/4 watt, 5%.		
R1		
R2	6-330-12	33 Ω
R3-R7	6-102-12	1000 Ω
R8-R14	6-390-12	39 Ω
R15-R16	6-102-12	1000 Ω
R17		Not used
R18	6-102-12	1000 Ω
R19	6-221-12	220 Ω
R20-R22		Not used
R23	6-472-12	4700 Ω
R24	6-333-12	3300 Ω
R25		Not used
R26	6-330-12	33 Ω
R27	6-102-12	1000 Ω
R28	6-151-12	150 Ω
R29	9-125	47 Ω resistor pack
R30-R31	9-126	33 Ω resistor pack
CAPACITORS		
C1, C3	25-195	22 μF electrolytic
C2, C4	25-866	22 μF electrolytic
C5-C36	21-769	.01 μF ceramic
C37-C52	21-769	.01 μF ceramic
C53	20-102	100 pF mica
C54	20-130	12 pF mica
C55	21-769	.01 μF ceramic
C56	20-171	820 pF mica
C57	20-96	36 pF mica
INTEGRATED CIRCUITS		
See "Semiconductor Identification Chart" and Schematic for part numbers.		