HEATH ZENITH

H47 INTERFACE AND SERIAL I/O CARD

Model WH8-47

OPERATION 595-2469

HEATH COMPANY
Benton Harbor, Michigan 49022

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INTRODUCTION

The Heath H47 Interface and Serial I/O Card Model WH8-47 allows you to add the H47 Floppy Disk System to your H8 Computer. This system greatly expands the mass storage capability of your H8 Computer.

In addition to the disk interface circuitry, this Card contains two channels of RS232C asynchronous serial interface for interfacing to such devices as the Heath H19 Terminal, H14 Printer, or a modem. Each serial channel is fully programmable (including baud rate) and can be independently addressed to any port location.

When this Card is used alone, the H47 Disk System must be booted from 5-1/4" disk SYØ:. However, if you install the accessory HA8-8 Extended Configuration Board in your H8 Computer, then you can boot from any drive that you select.

See Page 7 for a list of software that will operate the system. Cassette operation is not supported while the H47 Disk System is installed.

NOTE: Your Interface and Serial Card was assembled from high quality parts and was tested at the factory to make sure that it operates properly. You will probably never experience difficulty with this Card; but if you do, a red light-emitting diode (LED) and bare wire have been supplied as test instruments as described in the "In Case of Difficulty" section of this Manual.

Insert the LED into the envelope supplied and tape the envelope to the inside front cover of the Manual. Use the piece of supplied tape. It is sticky on both sides when the protective coverings are removed.

SPECIFICATIONS

DISK INTERFACE

Type	8-bit bidirectional parallel interface with an additional 8 dedicated handshaking lines.
Interrupts	3 through 7, selectable.

SERIAL INTERFACE

Channels	Two, EIA, RS232C. Each channel provides serial data and primary RS232C handshake.
Output Levels	RS232C.
Input Levels	RS232C compatible.
User-Programmable Functions	
Character Length	5, 6, 7, or 8 bits.
Parity	Even, odd, stick, or disabled.
Stop Bits	1, 1-1/2, or 2.
Baud Rates	Continuous, including all standard rates to 19,200 baud.

GENERAL

Computer Interface	For use with Heath H50 bus.
Operating Temperature	0 degrees to 40 degrees Celsius.
Power Requirements	+8 volts DC at 1.1 ampere. +18 volts DC at 50 milliamperes. −18 volts DC at 50 milliamperes.

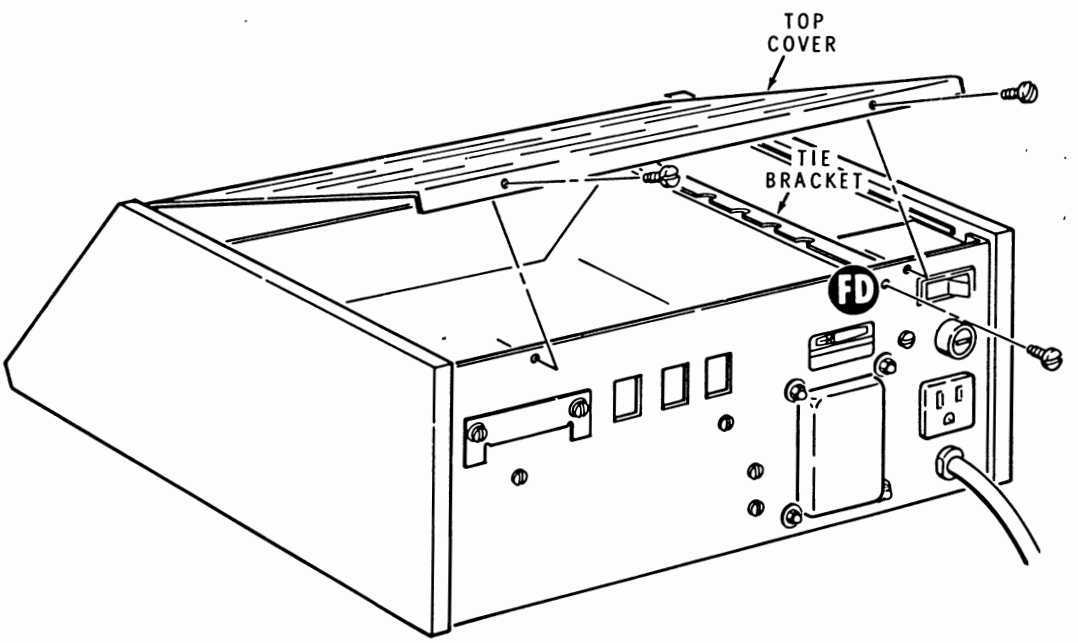
INSTALLATION

Refer to Pictorial 1 for the following steps.

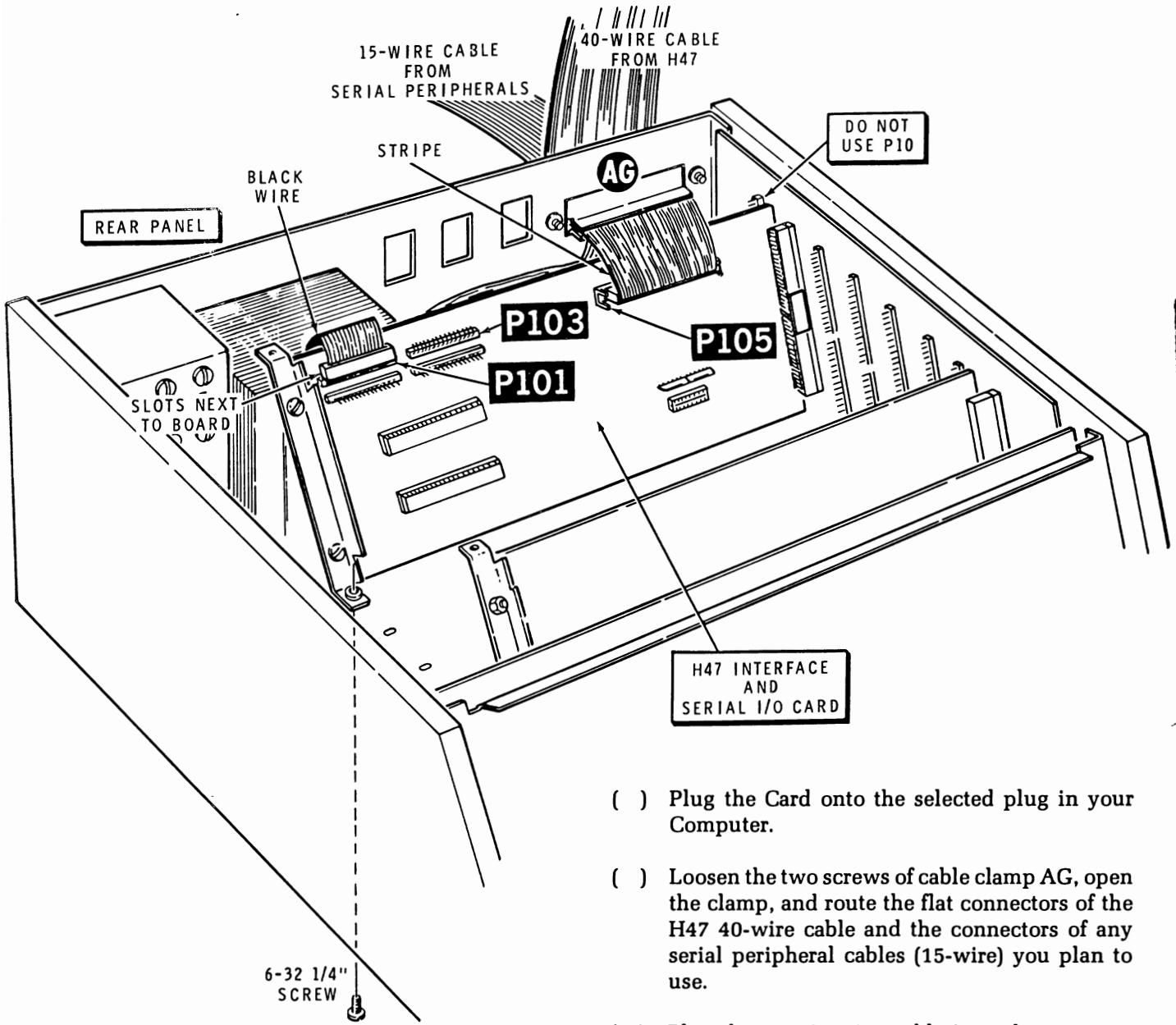
( ) Be sure your Computer is turned off.

( ) Remove the two rear panel screws holding the top cover and set the top cover aside if this has not already been done.

( ) Remove rear panel screw FD. Then loosen the other screws in the tie bracket, remove the bracket, and set it aside.



PICTORIAL 1



PICTORIAL 2

Refer to Pictorial 2 for the following steps.

( ) Set the Card programming jumpers to their proper positions. If necessary, refer to the "Heath System Configuration" section on Page 7 of this Manual.

NOTE: In the next step, you will install the Card into the Computer. Install the Card in one of the unused plugs near the rear of the Computer, but do not try to install it at P10. It will not fit.

( ) Plug the Card onto the selected plug in your Computer.

( ) Loosen the two screws of cable clamp AG, open the clamp, and route the flat connectors of the H47 40-wire cable and the connectors of any serial peripheral cables (15-wire) you plan to use.

( ) Plug the 40-wire H47 cable into plug P105 as shown in Pictorial 2. Be sure to position the striped edge of the cable as shown.

( ) Plug any serial peripheral cables (H9, H19, H14, etc.) into either plug P101 or plug P103 of the Card.

( ) Close clamp AG until it is snug and retighten the screws.

( ) Install a 6-32 × 1/4" screw through the bottom of the computer chassis to hold the Card in place.

( ) Replace the tie bracket as shown in Pictorial 1.

HEATH SYSTEM CONFIGURATION

To operate your H47 Interface and Serial I/O Card, you must use the proper software, correctly position the card programming jumpers, and correctly connect the H47 Disk System, or peripheral devices (terminal, printer, etc.), or both, to your H8 Computer.

If you have not installed the HA8-8 Extended Configuration Board, then you can only boot your system from 5-1/4" drive SYØ:. If you have installed the Extended Configuration Board, then refer to your software documentation manual for instructions on how to boot from the desired drive.

SOFTWARE REQUIREMENTS

Heath system — Use HOS 817-1 or HOS 847-1.
CP/M — Use HOS 817-2 or HOS 847-2.

DISK PROGRAMMING

Refer to Pictorial 3 (Illustration Booklet, Page 1) and push the programming jumper at DISK ENABLE down over the pins at ON. Then set the other disk programming jumpers as follows. These jumpers select ports 170 through 173 for the H47 disk system.

J102	100
J103	70
J104	0-3

Set DISK INTERRUPT jumper J114 to 5.

J105 AND J106 SET THE INTERRUPTS FOR THE SERIAL PORTS

SERIAL I/O PROGRAMMING

The H8 system can address (communicate with) 256_{10} input/output devices by applying a unique binary code on 8 address lines ($2^8 = 256_{10}$). These codes, expressed in octal, represent the range 000 through 377.

Each serial channel requires seven consecutive addresses. Thus, for example, if you choose a starting address of 350_8, the channel would require addresses 350 through 357. Therefore, it is only necessary to designate the highest and middle digits when you program a serial channel address. When you use Heath software, the software documentation will specify the correct address.

Refer to the following I/O address assignments and find the correct address for the type of peripheral that you want to connect. For example, the Heath software requires that a console terminal be assigned the address 350. Install programming jumpers on the address connectors to program the desired address. Pictorial 3 shows channel 0 configured for address 350. Therefore, program jumpers are installed at 300 and at 50, and the terminal cable is connected to P101.

TABLE OF I/O ADDRESS ASSIGNMENTS

DESCRIPTION	ADDRESS (OCTAL)
Console terminal	350 (350-357)
Line printer	340 (340-347)
Alternate terminal 0	300 (300-307)
Alternate terminal 1	310 (310-317)
Alternate terminal 2	320 (320-327)
Alternate terminal 3	330 (330-337)

NOTE: Any address may be assigned to any channel, but two channels must not be assigned the same address.

Set the CHANNEL ENABLE jumper to the "ON" position if that channel is used.

Some peripheral devices require that you use interrupts. The software documentation will tell you which (if any) interrupts you need for each type of peripheral device. (When an interrupt is not needed, install the programming jumper at position 3 of that channel.)

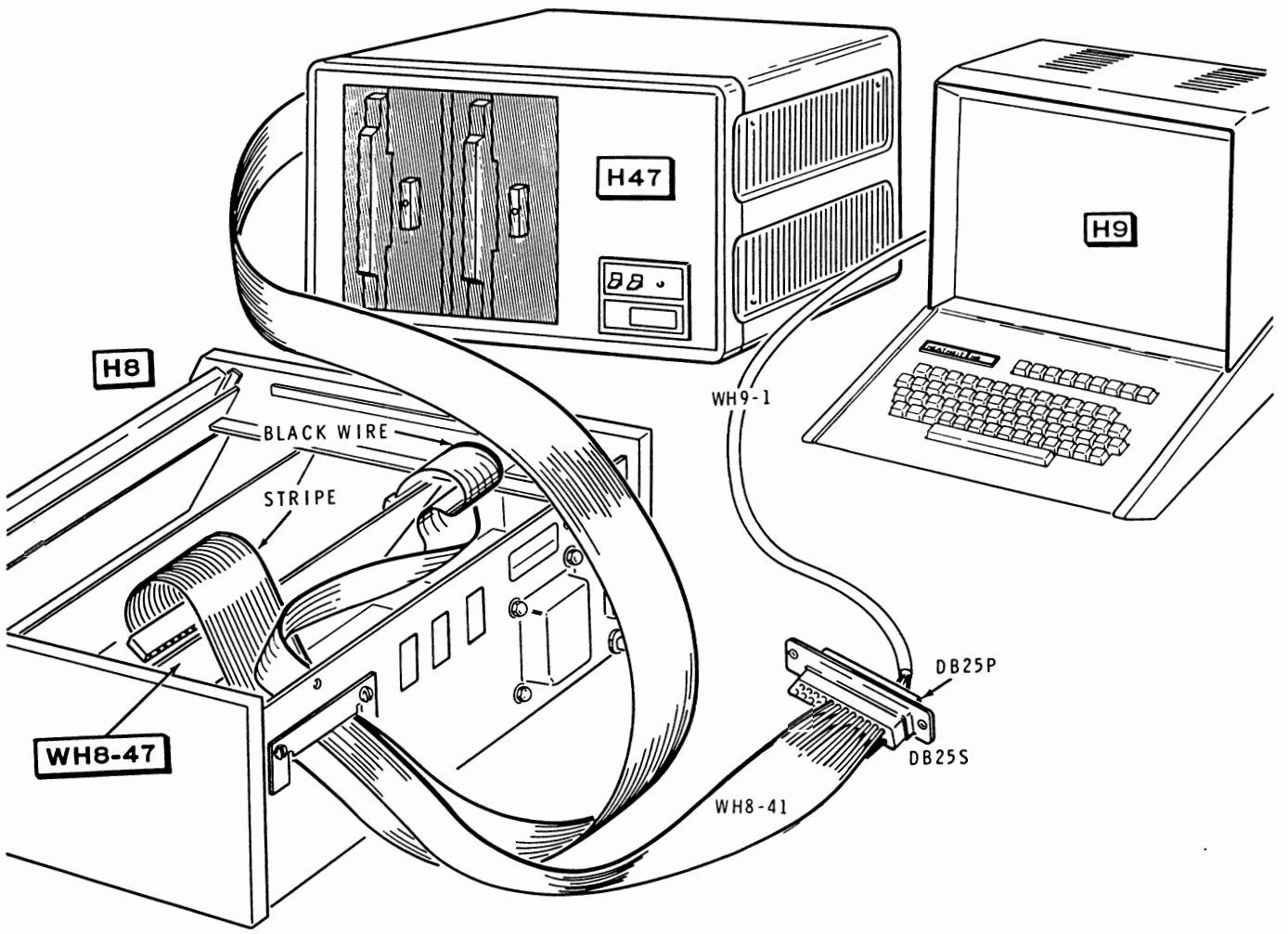
PERIPHERAL INTERFACE

Peripheral devices connect to the serial I/O connectors of the Card with a 15-conductor flat cable that terminates in an EIA standard connector for RS-232C interface. One such cable is supplied; additional cables (WH8-41) are available from Heath Company. This cable mates with equipment using the standard RS-232C interface. To connect to an H9 Terminal, a WH9-1 cable will be needed as shown in Pictorial 4.

There are two I/O connectors for each channel; the upper ones are marked "DCE" (Data Communications Equipment) and should be connected to terminals and printers (H9, H19, H14, etc.). The lower ones are marked "DTE" (Data Terminal Equipment) and should be connected to modems, etc.

LA36 DEC Writer

The LA36 must be equipped with the EIA option. Then connect the D connector (DB25P) of the LA36 to the D connector (DB25S) of the WH8-41 cable.



PICTORIAL 4

RS-232C INTERFACING

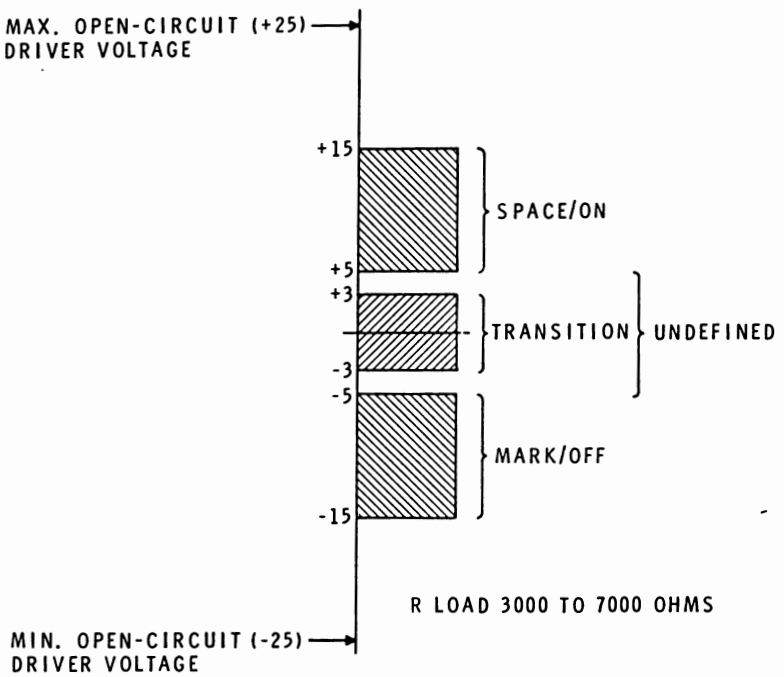
This Card was designed to interface with peripherals using the RS-232C standards of the Electronic Industires Association. This standard defines an asynchronous serial interface, its voltages (see Pictorial 5), its impedances, and its physical connectors.

RS-232C places all equipment into one of two general categories:

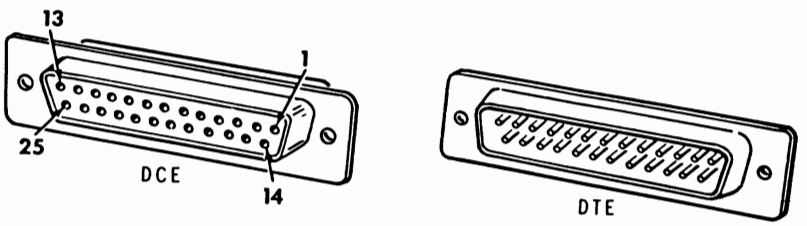
DTE — Data Terminal Equipment.

DCE — Data Communication Equipment.

Computers and modems are two types of DCE; while terminals, printers, and most peripherals are DTE. Always connect a DTE to a DCE. Never connect two like types together.



PICTORIAL 5



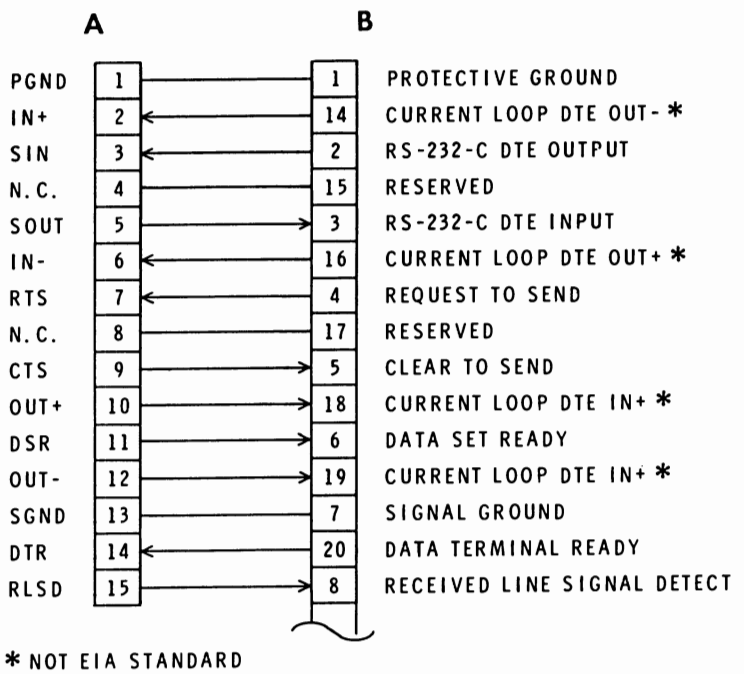
PICTORIAL 6

Connectors (see Pictorial 6) are:

DCE — DB-25S (female pins)

DTE — DB-25P (male pins)

Pictorial 7 shows a DCE cable that will interface the Card with a DTE unit. End A is a 15-pin in-line connector that mates with a DCE plug on the card. End B is a 25-pin female "D" connector that mates with peripheral equipment.



PICTORIAL 7

SERIAL I/O FUNCTIONAL TESTS

These tests will thoroughly check the operation of the serial portion of your H47 Interface Serial I/O Card. Perform the tests if you think there is a problem on the serial portion of the Card or if you just want to be sure it is working properly before you start using it.

Refer to Pictorial 3 (Illustration Booklet, Page 1) and set the programming jumpers as follows:

Channel ø to øøø (øøø and øø).

Channel 1 to 11ø (1øø and 1ø).

Both CHANNEL ENABLES to ON.

Both CHANNEL INTERRUPTS to 5.

NOTES:

1. When RESET is called for in the ACTION column, simultaneously press the RST/ø and ø keys on the H8 front panel.

2. When ENTER is called for, first press the MEM key. (The H8 readout decimal points will light.) Then press the six keys in the order listed in the DIGITS ENTERED/EXPECTED DISPLAY column for the channel under test. After you enter the numbers, the decimal points will turn off.

3. The ACTION column will also call for the IN, OUT, +, and − keys to be pushed.

4. If the EXPECTED DISPLAY is correct, check YES and then proceed to the next test. If the display is not correct, check NO but continue on through the test. (This may help you in troubleshooting.) Then proceed to the "In Case of Difficulty" section on Page 24 of your Manual.

5. The Data Readouts (three right-hand digits) are disregarded in these tests.

6. An X in a digit position denotes a "don't care" for that particular display.

7. Unless you have a difficulty, DO NOT turn off the H8 Power switch during the test.

There are three "Functional Tests." Perform all the steps for a channel before you proceed to the other channel, as shown by the arrows at the bottoms and tops of the columns.

If you make a keystroke error during a test sequence for a channel, you should reset and start the test over. It is not necessary to restart and go through all the tests.

Proceed to the Functional Tests.

TEST #1 — ACE STATUS AFTER RESET

The various registers in the 8250 ACE are placed in a known condition after a general reset. This test will verify each channel for proper status after reset.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0	(Y) (N)	CH1	(Y) (N)
RESET	RESET		RESET	
ENTER	0.0.0. 0.0.0.		0.0.0. 1.1.0.	
IN	X X X 0 0 0		X X X 1 1 0	
+	X X X 0 0 1		X X X 1 1 1	
IN	0 0 0 0 0 1	( ) ( )	0 0 0 1 1 1	( ) ( )
+	0 0 0 0 0 2		0 0 0 1 1 2	
IN	0 0 1 0 0 2	( ) ( )	0 0 1 1 1 2	( ) ( )
+	0 0 1 0 0 3		0 0 1 1 1 3	
IN	0 0 0 0 0 3	( ) ( )	0 0 0 1 1 3	( ) ( )
+	0 0 0 0 0 4		0 0 0 1 1 4	
IN	0 0 0 0 0 4	( ) ( )	0 0 0 1 1 4	( ) ( )
+	0 0 0 0 0 5		0 0 0 1 1 5	
IN	1 4 0 0 0 5	( ) ( )	1 4 0 1 1 5	( ) ( )
+	1 4 0 0 0 6		1 4 0 1 1 6	
IN	0 0 0 0 0 6	( ) ( )	0 0 0 1 1 6	( ) ( )
+	0 0 0 0 0 7		0 0 0 1 1 7	
IN	3 7 7 0 0 7	( ) ( )	3 7 7 1 1 7	( ) ( )

If all results were YES, go on to TEST #2. Otherwise, see the "In Case of Difficulty" section.

TEST #2 — HARDWARE INTERRUPT FUNCTION

The 8250 ACE generates an interrupt for any of several operations. This test checks the logic that places the interrupt on the H8 bus.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 (Y) (N)	CH1 (Y) (N)
RESET	RESET	RESET
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4
IN	0 2 0 0 0 4 ( )( )	0 2 0 1 1 4 ( )( )
ENTER	0.1.7. 0.0.1.	0.1.7. 1.1.1.
OUT	BLANK with Tone sounding. ( )( )	BLANK with Tone sounding. ( )( )
RESET	RESET	RESET
REMOVE	CH0 INT jumper	CH1 INT jumper

If there are any "NO" answers, refer to the "In Case of Difficulty" section.

TEST #3 — INTERNAL CONTROL AND COMMUNICATION

The internal loop back capability of the 8250 ACE will be used here to test the Control/Sense and Data paths inside the ACE.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 (Y) (N)	CH1 (Y) (N)
RESET	RESET	RESET
ENTER	2.0.0. 0.0.3.	2.0.0. 1.1.3.
OUT	2 0 0 0 0 3	2 0 0 1 1 3
IN	2 0 0 0 0 3 ( )( )	2 0 0 1 1 3 ( )( )
ENTER	0.0.0. 0.0.1.	0.0.0. 1.1.1.
OUT	0 0 0 0 0 1	0 0 0 1 1 1
IN	0 0 0 0 0 1 ( )( )	0 0 0 1 1 1 ( )( )
ENTER	3.0.0. 0.0.0.	3.0.0. 1.1.0.
OUT	3 0 0 0 0 0	3 0 0 1 1 0
IN	3 0 0 0 0 0 ( )( )	3 0 0 1 1 0 ( )( )
ENTER	0.0.3. 0.0.3.	0.0.3. 1.1.3.
OUT	0 0 3 0 0 3	0 0 3 1 1 3
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4
ENTER	0.1.7. 0.0.1.	0.1.7. 1.1.1.
OUT	0 1 7 0 0 1	0 1 7 1 1 1
ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.
IN	X X X 0 0 6	X X X 1 1 6
IN	0 0 0 0 0 6 ( )( )	0 0 0 1 1 6 ( )( )
ENTER	0.3.7. 0.0.4.	0.3.7. 1.1.4.
OUT	0 3 7 0 0 4	0 3 7 1 1 4

*

*

*Proceed to the top of this same column on Page 16.

TEST #3 (cont'd.)

ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.
IN	X X X 0 0 6	X X X 1 1 6
IN	3 6 0 0 0 6 ( )( )	3 6 0 1 1 6 ( )( )
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4
ENTER	1.7.7. 0.0.3.	1.7.7. 1.1.3.
OUT	1 7 7 0 0 3	1 7 7 1 1 3
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.
IN	0 0 6 0 0 2 ( )( )	0 0 6 1 1 2 ( )( )
ENTER	0.0.0. 0.0.5.	0.0.0. 1.1.5.
IN	1 7 1 0 0 5 ( )( )	1 7 1 1 1 5 ( )( )
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.
IN	0 0 4 0 0 2 ( )( )	0 0 4 1 1 2 ( )( )
ENTER	3.7.7. 0.0.0.	3.7.7. 1.1.0.
IN	0 0 0 0 0 0 ( )( )	0 0 0 1 1 0 ( )( )
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.
IN	0 0 2 0 0 2 ( )( )	0 0 2 1 1 2 ( )( )
IN	0 0 0 0 0 2 ( )( )	0 0 0 1 1 2 ( )( )
ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.
IN	0 1 7 0 0 6 ( )( )	0 1 7 1 1 6 ( )( )
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.
IN	0 0 1 0 0 2 ( )( )	0 0 1 1 1 2 ( )( )
	↓ *	↓ *

*Proceed to the top of this same column on Page 17.

TEST #3 (cont'd.)

RESET	RESET	RESET
ENTER	2.0.0. 0.0.3.	2.0.0. 1.1.3.
OUT	2 0 0 0 0 3	2 0 0 1 1 3
ENTER	0.0.0. 0.0.1.	0.0.0. 1.1.1.
OUT	0 0 0 0 0 1	0 0 0 1 1 1
ENTER	3.0.0. 0.0.0.	3.0.0. 1.1.0.
OUT	3 0 0 0 0 0	3 0 0 1 1 0
ENTER	0.0.3. 0.0.3.	0.0.3. 1.1.3.
OUT	0 0 3 0 0 3	0 0 3 1 1 3
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4
ENTER	1.2.5. 0.0.0.	1.2.5. 1.1.0.
OUT	1 2 5 0 0 0	1 2 5 1 1 0
+	1 2 5 0 0 1	1 2 5 1 1 1
IN	0 0 0 0 0 1 ( ) ( )	0 0 0 1 1 1 ( ) ( )
-	0 0 0 0 0 0	0 0 0 1 1 0
IN	1 2 5 0 0 0 ( ) ( )	1 2 5 1 1 0 ( ) ( )
ENTER	2.5.2. 0.0.0.	2.5.2. 1.1.0.
OUT	2 5 2 0 0 0	2 5 2 1 1 0
+	2 5 2 0 0 1	2 5 2 1 1 1
IN	0 0 0 0 0 1 ( ) ( )	0 0 0 1 1 1 ( ) ( )
-	0 0 0 0 0 0	0 0 0 1 1 0
IN	2 5 2 0 0 0 ( ) ( )	2 5 2 1 1 0 ( ) ( )

*

*Return to the top of the **next** column on Page 15.

If there are any "NO" answers, refer to the "In Case of Difficulty" section.

CIRCUIT DESCRIPTION

Refer to the Block Diagram (Illustration Booklet, Page 2; and the Schematic Diagram, fold-in) as you read the following information.

The circuitry is in three main sections. The first section is the H8 bus interface circuits, the second section is the two RS-232C serial I/O channels, and the third section is the disk I/O control logic. Each section is discussed in detail.

H8 BUS INTERFACE CIRCUITS

Data Buffers

Bidirectional buffers U109 and U111 invert the inverted bus data lines (pins 10-17, D0-D7) and isolate the on-board data lines from the bus. These buffered data bits are connected directly to the eight data lines of the two ACE's (U114, U118). When the read buffer enable ($\overline{RBEN}$) line is high, the data buffers feed data from the Card to the data bus. When the write buffer enable ($\overline{WBEN}$) is low, signals from the data bus are coupled through the buffers and applied to the two ACE's.

Control Buffers

Four control signals from the H8 bus (pins 21, 22, 26, and 29) are used throughout the Card. IOR (input/output read) and IOW (input/output write) control signals from the H8 bus are applied to low pass RC filter networks R101/C101 and R102/C102 to reduce bus noise before being buffered by the tri-state inverting buffers of U112. Control signals $\overline{RESET}$ and $\overline{\phi 2}$ are also buffered by inverting buffers of U112.

Address Buffers and Decoders

Address signals $\overline{A\phi}$ through $\overline{A7}$ (pins 30-37) from the H8 bus are inverted and buffered by U101. These buffered address lines are then decoded by U102 and U107. A3 through A5 are decoded by U102 into eight possible states. A6 through A7 and A1 through A2 are each decoded into four possible states. These 12 outputs of the address decoders are routed to the disk address selector connectors (J102, J103, and J104) and both of the serial I/O channel connectors (J107, J108 and J111, J112). The inverted and non-inverted form of A2 is also routed to the disk I/O address selection connectors. The three lowest-order bits (Aϕ-A2) are also connected to the address lines of both ACE's. Decoding inside the ACE's provide one-of-seven address decoding (only six are used).

H8 Monitor Disable Circuit

Logic on this Card provides the ability to disable (by software) the H8 Monitor ROM on the H8 CPU Card. This is done by setting D5 to a logic 1 and outputting

it to I/O port 362. The Monitor ROM is reenabled by either outputting a D5 logic 0 to I/O port 362 or by a system RESET. This disabling of the H8 Monitor ROM is first done by decoding I/O port address 362 by U104, which latches the D5 bit into flip-flop U105B. This latched D5 bit is inverted by an open collector gate (U106B) and applied to pin 46 of the H8 bus.

Interrupt Drivers

Five lines of the H8 bus (35-39) are CPU interrupts. By asserting one of these lines, a peripheral device (such as the disk I/O or either serial I/O channel on this Card) can request service from the CPU. These interrupt signals (IDSK, ICH0, ICH1) from the disk I/O and ACE's are connected to three open-collector NAND gates (U106A, U106D, and U142B) where they are inverted and connected to the interrupt patch area (J105, J106, and J114). Here, the interrupt signal from the disk I/O or either serial I/O channel can be connected to any H8 bus interrupt line (INT3, 4, 5, 6, or 7) by jumper plugs. During system reset, the outputs of the interrupt drives are held high, which disables all interrupt requests.

Voltage Regulator Circuits

All the circuits on the Card, except the RS-233C drivers (U115 and U119), are powered by +5 volts DC. The unregulated +8 volts from the H8 bus is regulated to 5 volts by regulators U147 and U148.

The plus and minus 18-volt unregulated voltages from the H8 bus are regulated by U145 and U146 to provide the ±12 volts needed by RS-232C drivers U115 and U119. Filter capacitors insure that the regulators remain stable.

RS-232C SERIAL I/O CHANNELS

The two serial channels are electrically identical with data buffer control circuitry shared by both channels. Therefore, only channel 0 and the data buffer control circuitry will be described.

Channel Address Selection

The state of the eight address lines selects one of the 256 discrete I/O addresses. $2^8 = 256_{10}$ or 000_8 - 377_8; where the left or highest digit is represented by A7 and A6; the middle digit by A5, A4, and A3; and the least or right digit by A2, A1, and A0.

Since each channel requires seven continuous addresses, only the first (highest) and middle digits need to be jumper selected. Placing a programming jumper in the 000, 100, 200, or 300 position selects the decoded high digit from U102A. Similarly, placing a jumper at one of the locations 00-70 of the second digit selects one of the eight outputs from U107. Placing a jumper at the CHAN ENABLE ON or OFF position enables or disables the serial channel.

Asynchronous Communications Element (ACE)

The ACE has three address inputs that are connected directly to the buffered address lines; A0, A1, and A2. This permits the selection of the internal status and control registers when the unit has been address enabled by $\overline{CS2}$ and CHAN ENABLE by CS0. The $\overline{CS2}$ enabling signal is generated by taking pins 12 and 13 of U103D low simultaneously through jumper plugs at the channel address select connectors, J107 and J108. The $\overline{CH0HD}$ (Channel 0 high digit) signal may be connected to 000, 100, 200, or 300 for the first digit of the 3-digit octal port address. The CH0MD (middle digit) signal may be connected to 00 through 70 for the middle digit of the port address. When the H8 address bus carries the binary code that corresponds to these two selected digits, the $\overline{CS2}$ input of the ACE will become low, enabling the ACE.

When the ACE is enabled, the CS Out (chip select out) will go high and indicate that U114 has been selected. This signal is inverted by U112. The $\overline{CH0SEL}$ signal,

along with the $\overline{IOR}$ signal from the control buffer, are NOR'd together by U113C. The high output of U113C is applied to DISTR (Data Input Strobe) input, indicating that the ACE is in the read mode. Now data from the internal register that has been selected by the address code on pins 26, 27, and 28 will be present on pins 1 through 8. At the same time, the data buffer control logic enables this data by RBEN to be applied to the H8 bus through the data buffers.

When the $\overline{IOW}$ signal is present with $\overline{CH0W}$ from the data buffer control logic, the DOSTR line is set high and the ACE (U114) is in the write mode. The data on pins 1 through 8 from the data buffers will be stored in the internal register selected by address pins 26, 27, and 28. The $\overline{WBEN}$ signal from the data buffer control logic allowed data from the H8 bus to be applied to the ACE by way of the data buffers.

1.843 MHz Oscillator

The 1.843 MHz crystal oscillator serves as the clock for the baud rate generators of the ACE's. The oscillator uses CMOS inverters to prevent crystal loading. Separate output CMOS inverters provide buffering for each ACE.

RS-232C Receivers/Drivers

Four outputs form U114, S out (pin 11), $\overline{RTS}$ (pin 32), $\overline{DTR}$ (pin 33) and $\overline{OUT2}$ (pin 31) are buffered by U115. Here, they are converted from TTL levels to RS-232 (approximately ± 10 volts) and routed to the two I/O connectors DTE0 (data terminal equipment, channel 0) and DCE0 (data communications equipment, channel 0).

Four inputs to U114, S in (pin 10), $\overline{CTS}$ (pin 36), $\overline{DSR}$ (pin 37), and $\overline{RLSD}$ (pin 38) came from U104 where the RS-232C input levels are converted to TTL for U114.

The only signals on the Card that are not TTL logic levels are those between the RS-232C transmitter and receiver chips (U115, U119 and U116, U121) and the DTE/DCE connectors.

Data Buffer Control Logic

This group of control logic receives signals from both ACE's ($\overline{CH0SEL}$, $\overline{CH1SEL}$) and the control buffers ($\overline{IOR}$, $\overline{IOW}$, and 02), and then combine them and retime them with flip-flops and gating. Two of the signals that are produced are RBEN (read buffer enable) and $\overline{WBEN}$ (write buffer enable). These signals are used to control the direction of data flow to and from the H8 bus. When either ACE is enabled, producing a CSOUT (pin 24 of ACE) and at the same time an $\overline{IOR}$ (I/O Read) signal is received by the control buffers, U122 produces an RBEN signal. Similarly, a $\overline{WBEN}$ signal is formed with an $\overline{IOW}$ signal instead of $\overline{IOR}$.

As described earlier, $\overline{CH0W}$ is needed for the production of an ACE $\overline{DOSTR}$ signal. $\overline{CH0W}$ is formed by ANDing together $\overline{CH0SEL}$ and $\overline{IOW}$, and the result retimed using $\overline{\emptyset 2}$ by flip-flop U126B. $\overline{CH1W}$ is produced in a similar manner by flip-flop U126A.

DISK I/O INTERFACE

The disk I/O interface is a parallel interface with status and control handshaking signals designed for interfacing intelligent disk drives to the H8 system. A single 8-bit bidirectional bus is used to transfer all commands, data and status, to and from the H8. The bus transfer direction is indicated by a single line ($\overline{DDOUT}$). The $\overline{DTR}$ and the $\overline{DTAK}$ lines are used as handshaking signals between the H8 and the disk system. Two additional lines are used to transmit $\overline{BUSY}$ and $\overline{ERROR}$ status to the H8 system.

The control lines are defined as follows:

$\overline{D0}$-$\overline{D7}$ — Bidirectional data bus $\overline{D0}$ through $\overline{D7}$ transmits data, status, and commands between the H8 and the disk system. To provide an input to the disk system ($\overline{DDOUT}$ high), the data bus is asserted prior to $\overline{DTAK}$ going low in response to a $\overline{DTR}$ low and is held valid until $\overline{DTR}$ goes high. To provide output to the H8 ($\overline{DDOUT}$ low), the data bus is valid prior to $\overline{DTR}$ going low and remains valid for 80 nS after receipt of a low $\overline{DTAK}$. $\overline{DTR}$ will become high after the data bus is invalid.

BUSY — Busy output. A low state indicates that the disk system has received a command and is in the process of executing that command (including illegal commands). A high state indicates that the disk system is idle and will accept a command.

DTR — Data Transfer Request output. A low signal indicates that the disk system requires data on the data bus for an input (DDOUT high) or has placed data on the bus for an output (DDOUT low). DTR will become high after the data bus is invalid.

DMA GRT — Not used.

DMA RQ — Not used.

MRST — Master ReSeT input. A low signal will cause the system to stop any operation in process, clear all error conditions, raise all master and slave heads, and reset the disk system to an idle state.

DDOUT — Data Direction OUT to H8. The data direction signal line is controlled by the disk system to indicate the direction that data is being transmitted on the bidirectional data bus D0 through D7. A high signal indicates a data transfer into the disk system. A low signal indicates a data transfer to the H8.

DTAK — Data Transfer AcKnowledge. A low signal from the H8 acknowledges that data has been placed on or taken from the data bus, depending on the level of DDOUT in response to a DTR.

ERROR — ERROR output. A low signal indicates that one of the following error conditions has occurred: (1) Record not found, (2) CRC error, (3) Lost data, (4) Illegal command, (5) Excess bad tracks, (6) Drive not ready when accessed, (7) Attempting to write on a write protected diskette, or (8) Sector with deleted data mark encountered. The specific error condition(s) can be found by a read status command.

I/O Transaction Sequence

All I/O transactions between the H8 and the disk system operate as follows:

a. The first byte transferred to the subsystem while it is in a system ready state (that is, BUSY high and DTR low) is interpreted as a command. The disk system will set BUSY low and DTR high upon receipt of a command (including invalid commands).

b. The disk system will determine the direction of data transfer using the DDOUT line. DDOUT low indicates data flow to the H8; DDOUT high indicates data flow from the H8 system.

c. All data transfers are requested by the disk system by the assertion of DTR low.

d. All data transfers must be acknowledged by the H8 with a DTAK in response to a DTR from the disk system. NOTE: Data input or output, to or from the H8, precede a DTAK. Data output from the H8 must remain valid until DTR goes high.

e. The error flag is valid for the preceding operation (that is, when the disk system completes an operation and sets BUSY high and DTR low).

f. MRST (Master ReSeT) will unconditionally abort any operation and set the disk system to the system ready state. The error flag will not be valid.

g. When a command has been completed, the disk system will return to the system ready state.

Depending on the command presented by the H8, the disk system will request additional parameters (unit #, track #, sector #, etc.) in the sequence outlined in steps c and d above.

Disk Address Selection

As described in the serial "Channel Address Selection" description, 256 different I/O addresses (000_8 - 377_8) can be selected from eight address lines (A0 - A7) as shown.

A7 A6	A5 A4 A3	A2 A1 A0	Binary
3	7	7	Octal

Using programming jumpers, the first two octal digits can be fully programmed. Ranges of the least-significant digit can be programmed as follows.

XX0 to XX3 - - - - XX4 to XX7 - - - - : Two possible ranges used for disk I/O

XX0 XX1 to XX6 XX7 : Four possible ranges used for general purpose parallel I/O

When an I/O port address is received by the address decoders and its first two digits in octal match the disk jumper programmed address, and the third digit is within the programmed range of last digits, then a DISK ENABLE signal (logic 0) is produced.

Read/Write Port Decoder

U134 determines (decodes) when the disk interface is in one of the following modes:

a) Write Status
b) Write Data
c) Read Status
d) Read Data

The signals needed to determine the disk I/O mode are DISK ENABLE, write (BWR), read (BRD), A0 (BA0), and A1 (BA1). The relationship between these input signals and output signals are presented in the following truth table:

OUTPUTS (low)		INPUTS				
		$\overline{\text{DISK ENABLE}}$	$\overline{\text{BWR}}$	$\overline{\text{BRD}}$	BA0	BA1
WRITE STATUS	($\overline{\text{WSTAT}}$)	L	L	H	H	L
WRITE DATA	($\overline{\text{WDAT}}$)	L	L	H	L	H
READ STATUS	($\overline{\text{RSTAT}}$)	L	H	L	H	L
READ DATA	($\overline{\text{RDAT}}$)	L	H	L	L	H

Disk I/O Control Logic

This logic is the heart of the disk interface. It controls data to and from the disk. It also allows the H8 system to control and read the status of the disk system.

The disk can be reset by one of two ways, a hardware reset or a software reset. The H8 system can reset the disk I/O and disk by a hardware reset. This reset is from the H8 bus (pin 29). When reset, the interrupt flip-flop (U141A) and the disk transfer acknowledge flip-flop (U139B) are cleared. A software reset can also be performed by writing to the status port address with D1 high. This will reset the disk transfer acknowledge flip-flop and send a master reset ($\overline{\text{MRST}}$) to the disk system.

Disk I/O Modes

When the disk system address is jumper programmed, it will respond to at least two consecutive I/O addresses; that is, 170 and 171. The first address is considered the STATUS post address and the second is the DATA port address. Reading and writing can be performed on both addresses.

When the disk I/O is addressed ($\overline{\text{DISK ENABLE}}$), the $\overline{\text{BRD}}$ read signal is used to control the direction of data transfer through the disk data bus drivers (U127 and U128). When $\overline{\text{BRD}}$ is low, data or status is being read from the disk system. If $\overline{\text{BRD}}$ is high, data or status information is being written to the disk system.

1. Write status (WSTAT) — Certain disk I/O and disk system parameters can be set by writing to the status port with certain data bits set as shown below.

D6 — Interrupts Enabled
D1 — Master Reset
D0 — Flip-flop U137B set

2. Read Status (RSTAT) — Used to read the disk I/O status buffer (U143). The correlation between the status conditions and the status word is as follows:

D0	$\overline{\text{ERR}}$ —	Error condition from disk system
D1	SW101—A	Disk I/O status, switch SW101 (not presently used)
D2	SW101—B	
D3	SW101—C	
D4	SW101—D	
D5	$\overline{\text{DONE}}$ —	Disk system waiting for command
D6	$\overline{\text{INT ENABLE}}$ —	Disk interrupt has been enabled
D7	$\overline{\text{TR}}$ —	Disk system requesting information transfer

3. Write Data ($\overline{\text{WDAT}}$) — When $\overline{\text{DDOUT}}$ ($\overline{\text{OUT}}$) are low, $\overline{\text{WDAT}}$ strobes H8 bus data into data latches (U129). At the same time, ACK goes high and DTAK (Data Transfer Acknowledge) goes low and indicates that data is latched into the disk data latches and can be read by the disk data system. Also, any interrupt that has occurred is cleared.

4. Read Data ($\overline{\text{RDAT}}$) — Data from the disk system passes through U133 to the H8 bus because $\overline{\text{RDAT}}$ has enabled U133. U131 and U132 have been disabled by $\overline{\text{DDOUT}}$ ($\overline{\text{OUT}}$) being high. This put the disk data buffers in the read mode. Like the write data mode, ACK goes high and $\overline{\text{DTAK}}$ goes low indicating that the route is clear for a disk to H8 Bus transfer. If any interrupt has occurred, the $\overline{\text{RDAT}}$ signal will clear it.

IN CASE OF DIFFICULTY

This section of the Manual is divided into two parts. The first part, titled "Troubleshooting and Repair Precautions," points out the care that you should use when you service the unit to prevent damaging components.

The second part, titled "Troubleshooting Charts" gives a test program and troubleshooting charts to help you find the difficulty.

If the "Troubleshooting Charts" section does not help you locate the problem, read the "Circuit Description" and refer to the Schematic Diagram (fold-in) to help you determine where the trouble is.

Refer to the "Circuit Board X-Ray View" (Illustration Booklet, Page 6) for the physical location of parts on the circuit board.

NOTE: In an extreme case where you are unable to resolve a difficulty, refer to the "Customer Service" information inside the rear cover of the Manual. Your warranty is also located inside the rear cover.

TROUBLESHOOTING AND REPAIR PRECAUTIONS

1. Make sure you do not short any adjacent terminals or foils when you make test or voltage measurements. If a probe or test lead slips, for example, and shorts together two adjacent connections, it is very likely to damage one or more of the transistors, diodes, or IC's.

2. Be especially careful when you test any circuit that contains an IC or transistor. Although these components have an almost unlimited life when used properly, they are much more vulnerable to damage from excess voltage and current than many other parts.

3. Do not remove any components while the unit is turned on.

4. Use a voltmeter with a high input impedance when you measure voltages.

5. Never apply +5 volts or ground potentials to the output of any IC.

6. When you make repairs, make sure you eliminate the cause as well as the effect of the trouble. If, for example, you find a damaged resistor, be sure you find out what damaged the resistor. If the cause is not eliminated, the replacement resistor may also become damaged when you put the unit back into operation.

7. In several areas of the circuit board, the foil patterns are quite narrow. When you unsolder a part to check or replace it, avoid excessive heat while you remove the part. A suction-type desoldering tool makes part removal easier.

COMPONENTS

To remove faulty resistors or capacitors; first clip them from their leads, then heat the solder on the foil and allow each lead to fall out of its hole. Preshape the leads of the replacement part and insert them into the holes in the circuit board. Solder the leads to the foil and cut off the excess lead lengths.

You can remove transistors in the same manner as resistors and capacitors. Make sure you install the replacement transistor with its leads in the proper holes. Then solder the leads quickly to avoid heat damage. Cut off the excess lead lengths.

FOIL REPAIR

To repair a break in a circuit board foil, bridge solder across the break. Bridge large gaps in the foil with bare wire. Lay the wire across the gap and solder each end to the foil. Carefully trim off any excess bare wire.

TROUBLESHOOTING CHARTS

The Troubleshooting Charts are divided into two sections: "Disk Interface" and "Serial I/O." Proceed to the section that pertains to your Computer's problem.

Disk Interface

The following tests will help you locate the trouble by testing different sections of the disk interface circuits.

MRESET TEST

Refer to Pictorial 3 (Illustration Booklet, Page 1) and set the disk I/O address jumpers to 170 (100, 70, and 0-3).

Use the front panel keys to enter the following program in your H8.

ADDRESS		DATA (OCTAL)	
040	100	076	MVI A
040	101	002	data byte
040	102	323	OUT
040	103	170	port number
040	104	303	JMP
040	105	100	Memory address
040	106	040	040 100

Set PC to 040 100 and press GO. The program will output data 002 (D1 line high) to port 170 and then repeat. This will cause master reset (MRST) pulses at P105 pin 25 (or U142 pin 11).

DATA REGISTER AND CONTROL CIRCUIT TEST

This test will check each bit in the data register. It will:

- Move each of the numbers 0, 1, 2, 4, 8, 16, 32, 64, 128, and 256 to the data buffer.
- Check to be sure that the appropriate signal line is asserted at the disk interface connector after each move.
- Read the data buffer after each move. The data should be the same as that which was written.

1. Refer to Pictorial 3 and set the disk I/O address jumper to 170 (100, 70, and 0-3).
2. Reset the H8.
3. Press the MEM key.
4. Enter 000 (data) followed by I/O address 171 (data port).

5. The front panel ADDRESS displays should show 000 171.

6. Press the OUT key.

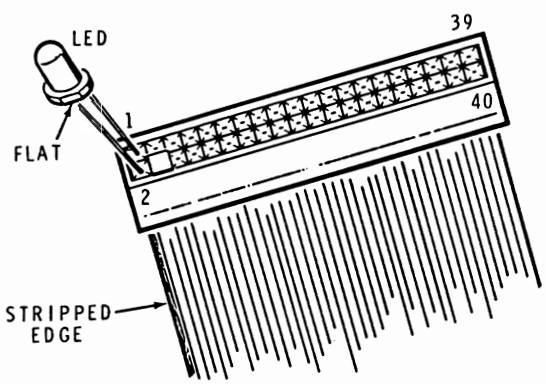
7. Insert the LED in the end of the 40-pin cable socket (at pins 1 & 2). Be sure to position the flat of the LED as shown in Pictorial 8. The LED should light (only the first time through these steps).

8. Remove the LED.

9. Press the IN key. The display should continue to read 000 171.

10. Repeat the above steps, but change the **data** you entered (at step 4) and the LED location (step 7) as shown in the following chart. Also, step 9 will display the new data; and in step 7, the LED should **not** light for the remainder of the test.

DATA (for step 4)	LED at pins:	BIT SET*
001	1&2	D0
002	3&2	D1
004	5&6	D2
010	7&8	D3
020	9&10	D4
040	11&12	D5
100	13&14	D6
200	15&16	D7



PICTORIAL 8

*Only this data bit is set to a logic 1 (indicated by the LED not lit), and all the rest are logic 0 (LED lit).

STATUS REGISTER TEST

This test will check the bits in the status register. It will:

— Set the INT ENB bit in the status register and then read the status register to see if it is set. Next the bit is cleared and again read to see if it was cleared.

— Short the ERROR input line to ground and read the status register. After the ERROR bit is detected, then the ERROR line is ungrounded.

— Short the DTR input line to ground and read the status register. The proper response is the DONE bit set low. Then leaving the DTR line shorted, also short the BUSY input line to ground. The status register should produce the TR bit set low.

INT ENable Bit

Reset the H8.

Press the MEM key.

Enter 100 170.

Press the OUT key. U143 pin 8 should be low.

ERROR Bit

Cut the supplied bare wire into three equal lengths and bend them into U's, like hair pins.

Refer to Pictorial 8 and install one of these shorting wires into socket pins 31 and 32 of the 40-pin cable socket.

Reset the H8.

Press the MEM key.

Enter 000 170.

Press the IN key. 001 170 should be displayed and U143 pin 2 should be low.

Remove the shorting wire.

DTR Bit

Refer to Pictorial 8 and install a shorting wire into socket pins 19 and 20.

Reset the H8.

Press the MEM key.

Enter 000 170.

Press the IN key. 040 170 should be displayed and U143 pin 13 should be low.

Install another shorting wire into socket pins 17 and 18.

Press the IN key. 200 170 should be displayed, U143 pin 11 should be low, and U143 pin 13 should be high.

Remove the shorting wires.

H8-TO-H47 HANDSHAKING TEST

Install shorting wires at socket pins 19 and 20 (DTR) and at pins 17 and 18 (BUSY).

Insert the LED into pins 29 and 30. (Be sure the lead near the flat of the LED is in hole 30.) The LED should light. (This indicates that $\overline{\text{DTAK}}$ is not set-logic 1.)

Press the MEM key.

Enter 000 171.

Press the OUT key. The LED should not light. (This indicates that the $\overline{\text{DTAK}}$ is set-logic 1.)

Remove the jumper from between pins 19 and 20 (DTR not set). The LED should light again.

Replace the jumper between pins 19 and 20 (DTR set). U143 pin 11 should now be low.

Install a shorting wire between pins 27 and 28 ($\overline{\text{DDOUT}}$ set).

Press the OUT key. The LED should remain lit.

Press the IN key. The LED should not be lit. (This indicates that $\overline{\text{DTAK}}$ is set.)

Remove the jumper from between pins 19 and 20 ($\overline{\text{DTR}}$ not set). The LED should again light to indicate that $\overline{\text{DTAK}}$ is set.

Remove the remaining jumper wires.

Serial I/O

If you have not already done so, refer to Page 12 and complete the "Functional Tests." Then continue with the following.

NOTE: Most IC's on the circuit board have duplicates. If you find an IC that you think is bad, substitute it with an IC of the same type from the other channel.

DIFFICULTY TEST PROGRAM

Use a logic probe or an oscilloscope to check U112 pin 9 for a logic low.

Press the reset buttons. The logic level should go high. If it does not, replace U112.

The following Test Program produces read and write pulses on the I/O lines of both channels 0 and 1. These pulses are the necessary test signals for the Serial I/O Troubleshooting Chart (Illustration Booklet, Page 3 and 4). As you work through the Serial I/O Troubleshooting Chart, follow the section (channel 0 or 1) that pertains to the channel that you are testing.

NOTE: Be sure the programming jumpers are still connected as described in the "Serial I/O Functional Tests" section on Page 12.

Load and run the following test program. Then proceed to the "Serial I/O Troubleshooting Chart."

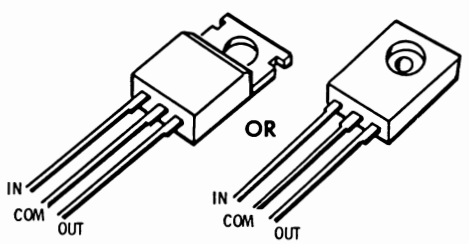
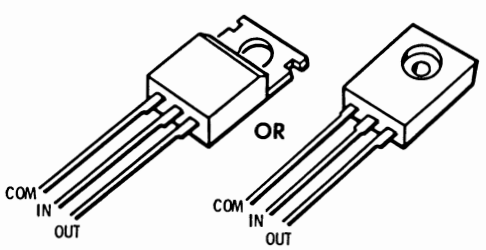
Test Program

ADDRESS		DATA		
040	100	363	START	DI
	101	041		LXI H, OPORT
	102	122		
	103	040		
	104	021		LXI D, IPORT
	105	124		
	106	040		
	107	006		MVI B, 125
040	110	125		
	111	066		MVI M, 357
	112	357		
	113	170	TEST	MOV A, B
	114	057		CMA
	115	107		MOV B, A
	116	064		INR M
	117	353		XCHG
040	120	064		INR M
	121	323		OUT OPORT
	122	000		
	123	333		IN IPORT
	124	000		
	125	303		JMP TEST
	126	113		
040	127	040		

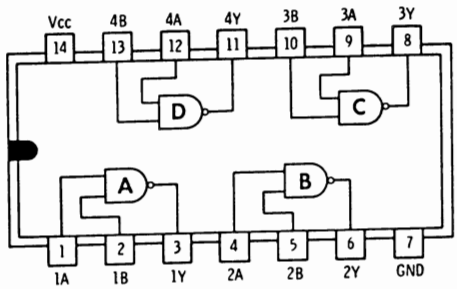
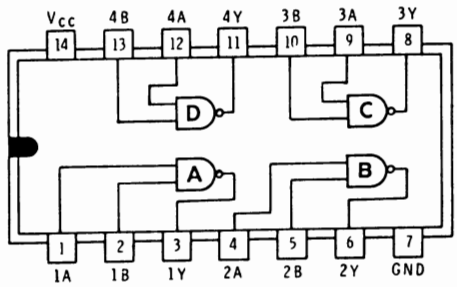
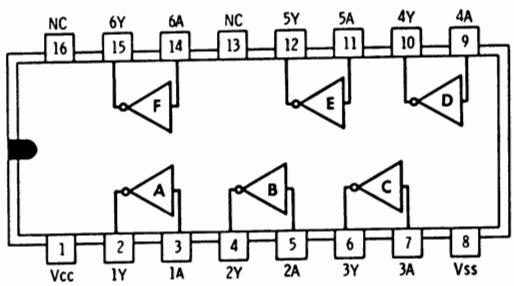
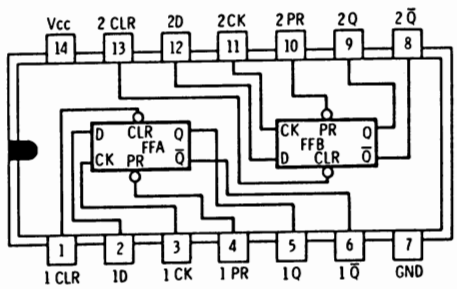
Set PC to 040 100 and press GO key.

SEMICONDUCTOR IDENTIFICATION CHARTS

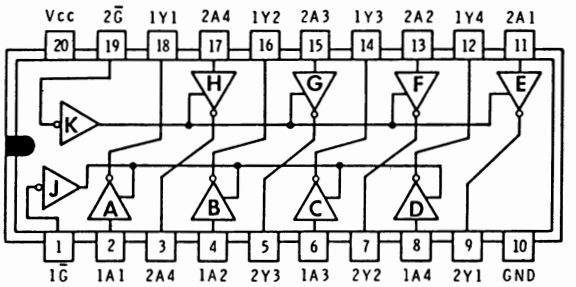
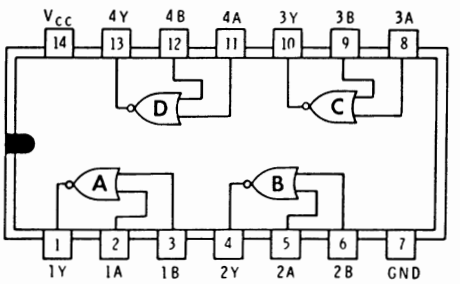
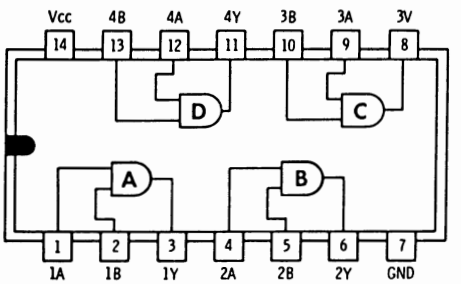
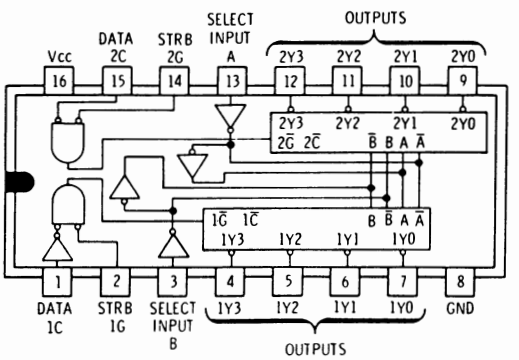
INTEGRATED CIRCUITS

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
442-54	UA7805	U147, U148	
442-674	UA7812	U145	
442-675	UA7912	U146	

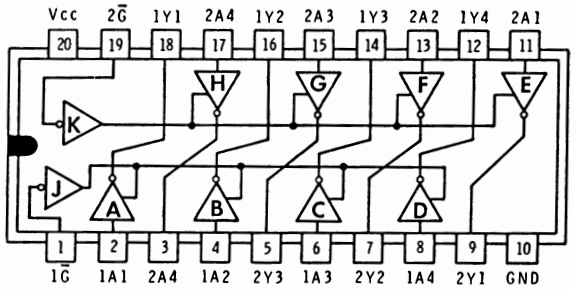
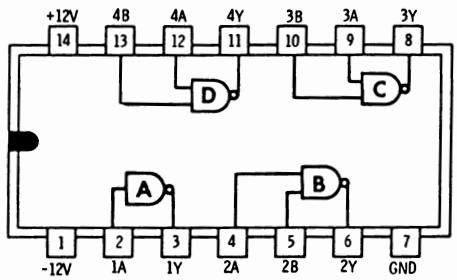
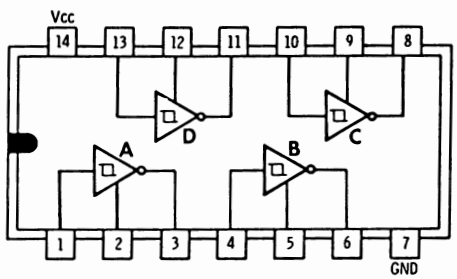
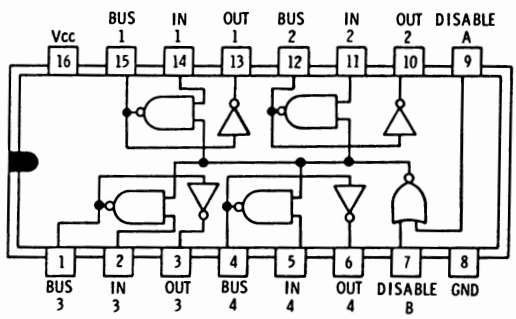
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
443-54	7403	U106	
443-77	7438	U142	
443-728	74LS00	U123, U124	
443-701	14049	U117	
443-730	74LS74	U105, U126, U137, U139, U141	

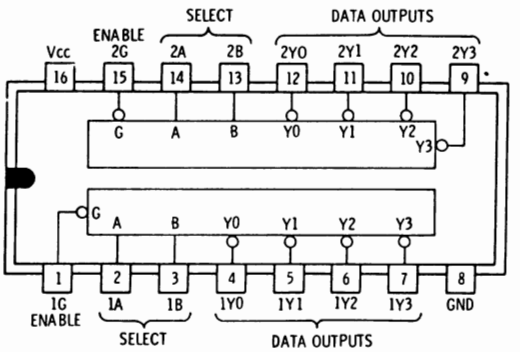
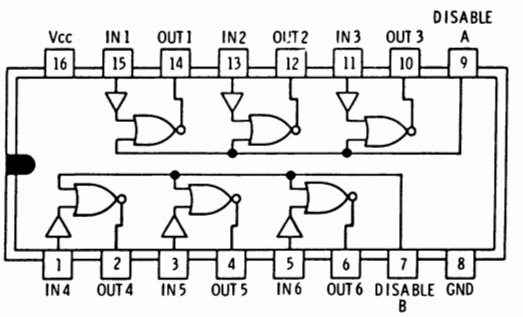
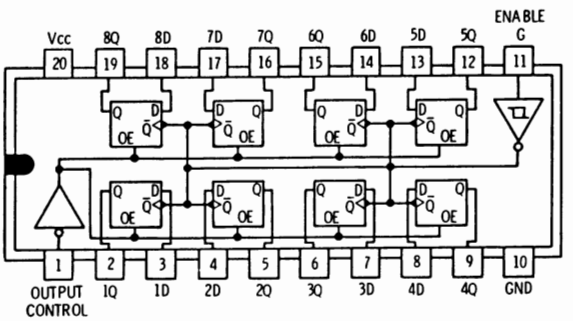
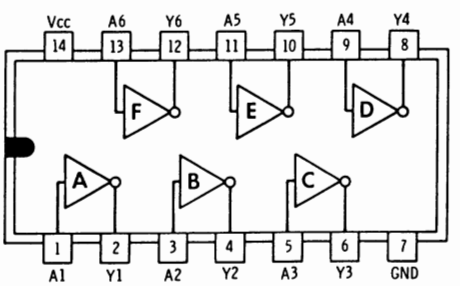
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
443-754	74LS240	U101, U112, U127, U128, U143	
443-779	74LS02	U113, U122, U135	
443-780	74LS08	U138	
443-782	74LS155	U134	

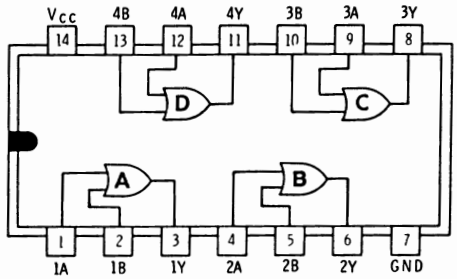
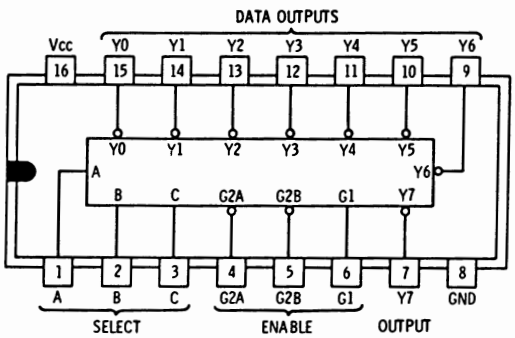
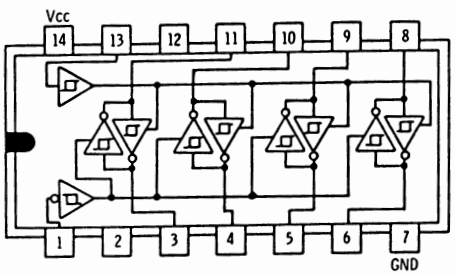
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
443-791	74LS244	U133	
443-794	75188 or 1488	U115, U119	
443-795	75189 or 1489	U116, U121	
443-819	DS8838	U131, U132	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
443-822	74LS139	U102	
443-860	8837	U144	
443-863	74LS374	U129	
443-872	74LS14	U136	

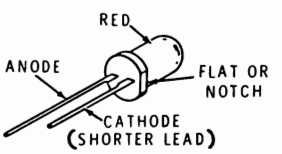
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
443-875	74LS32	U103, U104	
443-877	74LS138	U107	
443-884	74LS242	U109, U111	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION (TOP VIEW)
443-952	8250	U114, U118	
NOT USED		U149	

LED

HEATH PART NUMBER	MAY BE REPLACED WITH	CIRCUIT COMPONENT NUMBER	IDENTIFICATION
412-616		Test LED	

REPLACEMENT PARTS LIST

RESISTORS

All resistors are 1/4-watt, 5%.

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
R1	6-102-12	1000 Ω
R2	6-102-12	1000 Ω
R3	6-102-12	1000 Ω
R4	6-102-12	1000 Ω
R5	6-225-12	2.2 MΩ
R101	6-150-12	15 Ω
R102	6-150-12	15 Ω
R106	9-99	1 kΩ resistor pack
R107	9-99	1 kΩ resistor pack
R109	9-99	1 kΩ resistor pack
R112	9-107	180 Ω/390 Ω resistor pack
R113	9-107	180 Ω/390 Ω resistor pack
R114	9-107	180 Ω/390 Ω resistor pack
R202	6-471-12	470 Ω
R303	6-471-12	470 Ω

CAPACITORS

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
C3	21-147	47 pF ceramic
C4	21-147	47 pF ceramic
C101	20-102	100 pF mica
C102	20-102	100 pF mica
C103	25-917	10 μF electrolytic
C104	25-917	10 μF electrolytic
C105	25-917	10 μF electrolytic
C106	25-917	10 μF electrolytic
C107	25-917	10 μF electrolytic
C108	21-185	.01 μF ceramic
C109	25-917	10 μF electrolytic
C111	25-917	10 μF electrolytic
C112-C149	21-185	.01 μF glass ceramic
C303	21-164	.0015 μF (1500 pF) ceramic
C404	21-46	.005 μF ceramic

SEMICONDUCTORS

(See "Semiconductor Identification Chart")

APPENDIX A: 8250 PIN DESCRIPTION

NOTE: The following material is selected documentation from National Semiconductor and reprinted with their permission.

The function of all INS8250 input/output pins are described in the following paragraphs. (See the INS8250 Block Diagram, Illustration Booklet, Page 2). Some of these descriptions reference internal circuits. A low in these descriptions represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

Input Signals

Chip Select ($\overline{CS0}$, CS1, $\overline{CS2}$), Pins 12 - 14: When $\overline{CS0}$ and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{\text{DISTR}}$), Pins 22 and 21: When DISTR is high or $\overline{\text{DISTR}}$ is low while the chip is selected, this allows the CPU to read status information or data from a selected register of the INS8250.

NOTE: Only an active DISTR or $\overline{\text{DISTR}}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{\text{DISTR}}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{\text{DOSTR}}$), Pins 19 and 18: When DOSTR is high or $\overline{\text{DOSTR}}$ is low while the chip is selected, this allows the CPU to write data or control words into a selected register of the INS8250.

NOTE: Only an active DOSTR or $\overline{\text{DOSTR}}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{\text{DOSTR}}$ input permanently high, if not used.

Address Strobe ($\overline{\text{ADS}}$), Pin 25: When low, it provides latching for the Register Select (A0, A1, A2) and Chip Select (CSØ, CS1, $\overline{\text{CS2}}$) signals.

NOTE: An active $\overline{\text{ADS}}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{\text{ADS}}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 - 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain INS8250 registers. The DLAB is reset low when the Master Reset (MR) input is active (low); the DLAB must be set high by the system software to access the baud generator divisor latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, it clears all the registers (except the receiver buffer, transmitter holding, and divisor latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{\text{OUT 1}}$, $\overline{\text{OUT 2}}$, $\overline{\text{RTS}}$, $\overline{\text{DTR}}$) are affected by an active MR input. (Refer to Table 4.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{\text{CTS}}$), Pin 36: The $\overline{\text{CTS}}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM status register. Bit 0 (DCTS) of the MODEM status register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM status register.

NOTE: Whenever the CTS bit of the MODEM status register changes state, an interrupt is generated if enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, it indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM status register. Bit 1 (DDSR) of the MODEM status register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM status register.

NOTE: Whenever the DSR bit of the MODEM status register changes state, an interrupt is generated if enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, it indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM status register. Bit 3 (DRLSD) of the MODEM status register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM status register.

NOTE: Whenever the RLSD bit of the MODEM status register changes state, an interrupt is generated if enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, it indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM status register. Bit 2 (TERI) of the MODEM status register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM status register.

NOTE: Whenever the RI bit of the MODEM status register changes from a high to a low state, an interrupt is generated if enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, it informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM control register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, it informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM control register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: A user-designated output that can be set to an active low by programming bit 2 ($\overline{OUT\ 1}$) of the MODEM control register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: A user-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM control register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active CSØ, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D_7 - D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250 . The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud generator divisor latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by typing this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt sources has an active high condition: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the

Marking (logic 1) state upon a Master Reset operation.

Input/Output Signals

Data (D_7 - D_0) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D_7 - D_0 data bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1 - 7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 Are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low
	MODEM Signal Inputs	Bits 4 - 7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into Either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT} \cdot \text{RCLK} \cdot \text{DISTR}}$ (AT Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
D_7 - D_0 Data Bus Lines	In TRI-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	TRI-STATE DATA (ACE to CPU) DATA (CPU to ACE)

Table 4

Reset Control of Registers and Pinout Signals.

APPENDIX B: 8250 PROGRAMMING

When you use Heath software, you will not be concerned with programming the 8250 ACE (asynchonous communications element) in the WH8-47. However, this section will be indispensable if you intend to assemble your own program code. (It is selected material from National Semiconductor and reprinted with their permission.)

INS8250 ACCESSIBLE REGISTERS

You (the system programmer) may access or control any of the INS8250 registers summarized in Table 1 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 Line Control Register

Specify the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, you may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 1 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This is the Parity Enable bit. When Bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This is the Divisor Latch Access bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud rate generator during a Read or Write operation. It must be set low (logic 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Table 1
Summary of INS8250 Accessible Registers.

8250 PROGRAMMABLE BAUD RATE GENERATOR

The 8250 contains a programmable baud rate generator that takes the 1.8432 MHz clock and divides it by any divisor from 1 to 2^{16} - 1. The output frequency of the baud generator is 16 × the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

Table 2 illustrates the standard baud rates and the contents of the LS (least significant) and MS (most significant) latches expressed in byte octal.

BAUD RATE	DIVISOR LATCH (LS)	(MS)
75	000	006
110	027	004
134.5	131	003
150	000	003
300	200	001
600	300	000
1200	140	000
2400	060	000
4800	030	000
9600	014	000
19200	006	000

Table 2
Baud Rates.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the line status register are indicated in Table 1 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the receiver buffer register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the receiver buffer register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the line status register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the line status register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the transmitter shift register is idle. It is reset to logic 0 upon a data transfer from the transmitter holding register to the transmitter shift register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt are stored in the interrupt identification register (refer to table 3). The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 1 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 3.

Bits 3 through 7: These five bits of the IIR are always logic 0.

INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the INS8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and MODEM status registers. The contents of the interrupt enable register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1. Bit 1 is reset to logic 0 immediately upon reading the Interrupt Identification Register.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM control register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{\text{DTR}}$) output. When bit 0 is set to a logic 1, the $\overline{\text{DTR}}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{\text{DTR}}$ output is forced to a logic 1.

NOTE: The $\overline{\text{DTR}}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{\text{RTS}}$) output. Bit 1 affects the $\overline{\text{RTS}}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{\text{OUT 1}}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{\text{OUT 1}}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{\text{OUT 2}}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{\text{OUT 2}}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four MODEM control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM control Interrupts are also operational but the interrupts sources are now the lower four bits of the MODEM control register instead of the four MODEM control inputs. The interrupts are still controlled by the interrupt enable register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the line status register and the lower four bits of the MODEM status register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM status register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM status register.

The contents of the MODEM status register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector, Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 3

Interrupt Control Functions.