HEATH ZENITH

Z80 CPU CIRCUIT BOARD

Model HA-8-6

595-2652-01

HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

TABLE OF CONTENTS

NOTICE

If the container in which this unit was shipped shows any evidence of rough handling, inspect the circuit board very carefully. Any shipping damage must be reported to the carrier at once.

INTRODUCTION

This Model HA-8-6 Z80 CPU Circuit Board will replace the 8080 CPU board that was supplied with the Model H-8 Computer. When it is installed, your Computer will have the greater power of the Z80 microprocessor, including the use of zero-based software, double sided diskette drives, and 64 K of RAM.

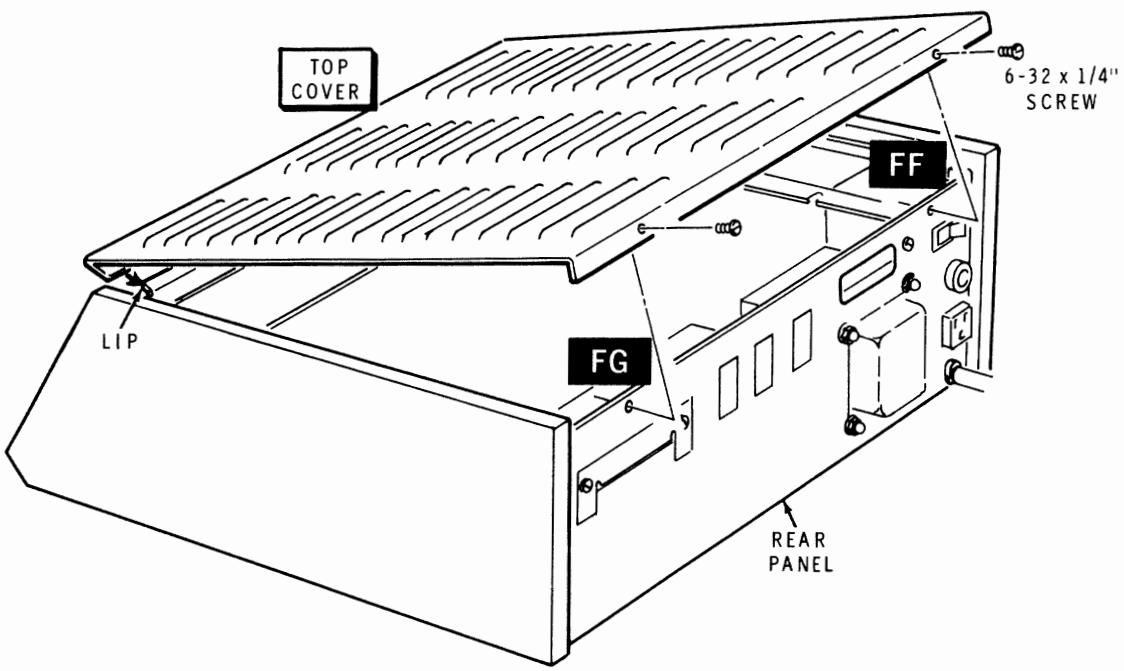
The Z80 CPU Board contains all the features of the HA-8-8 Extended Configuration accessory, including ROM Disable (ORG 0), in which the first RAM is addressed at 000 000 octal instead of 040 000 octal. However, unless your H-17 controller board is modified and your memory boards reconfigured, user RAM will originate at 8 K (200 H or 040 000 octal).

With the Z80 CPU Board, and the modification and reconfiguration, your H-8 Computer can use the CP/M operating system, Microsoft Basic, HDOS Version 2.0 or higher, and most other sophisticated programs, providing you have enough memory installed.

INSTALLATION

NOTE: Do not discard any screws or hardware that you remove from your Computer. You will need them when you install the circuit boards and replace the top cover.

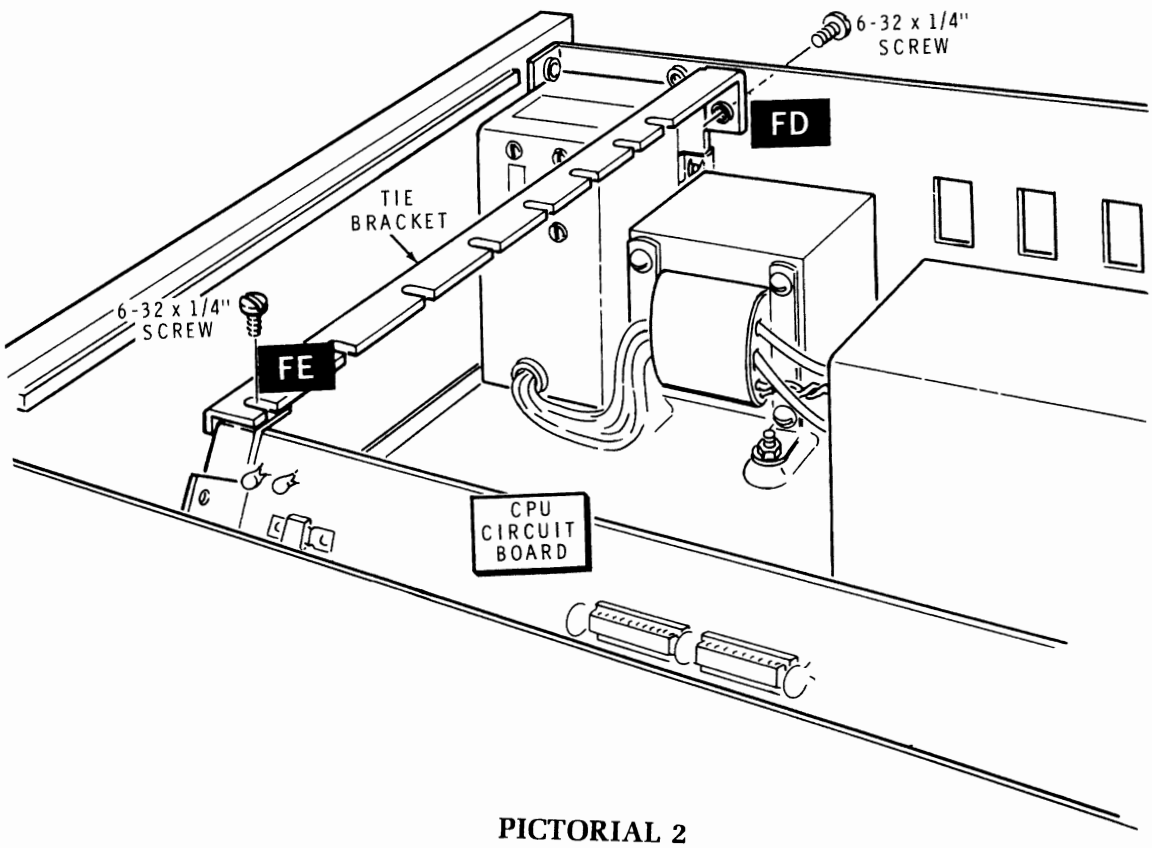
( ) Refer to Pictorial 1 and remove the two 6-32 × 1/4" screws that secure the top cover to the rear panel of the Computer. Then remove the top cover and set it aside.



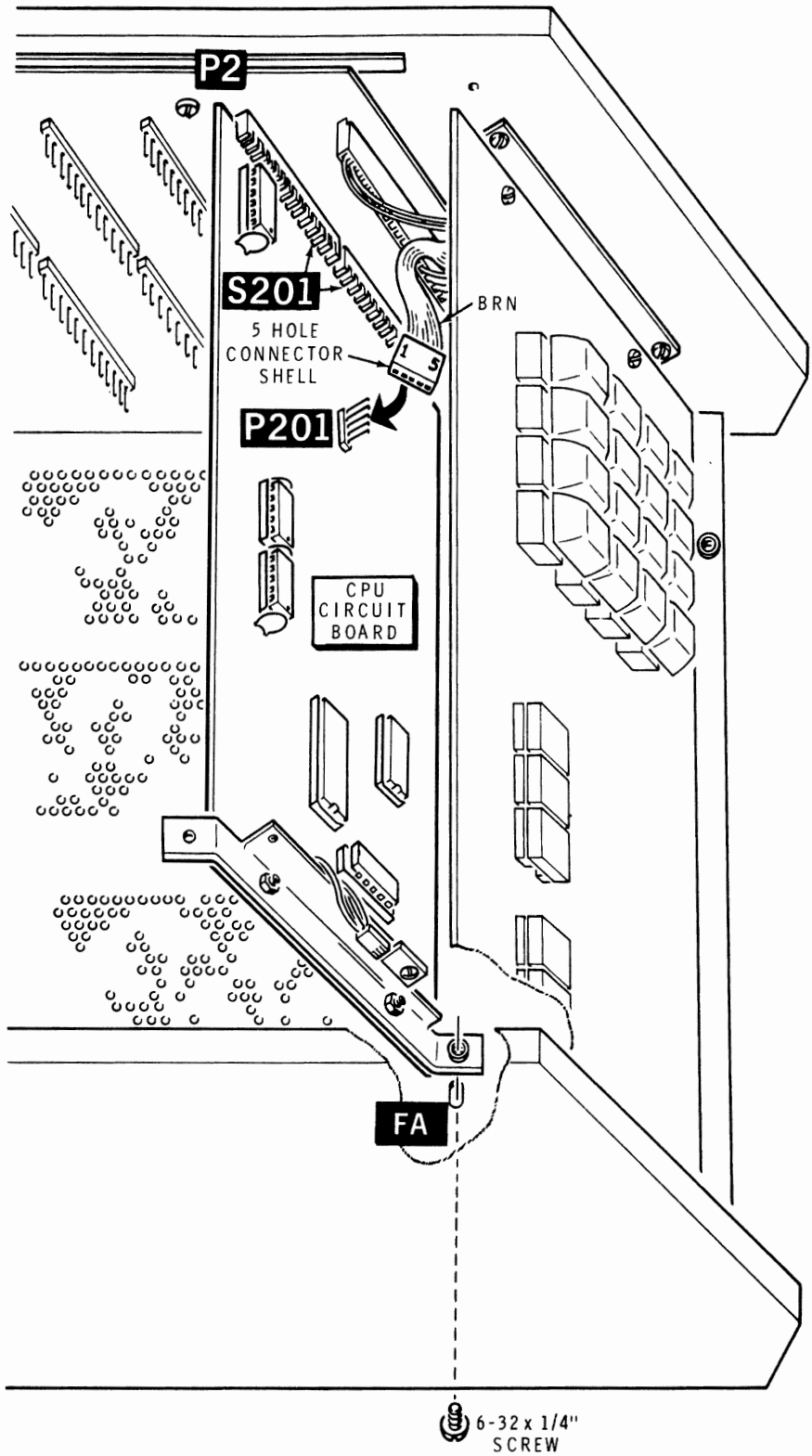
PICTORIAL 1

( ) Refer to Pictorial 2 and remove the screw that holds the CPU board to the tie bracket. Then loosen any screws that hold other circuit boards to the tie bracket.

( ) Remove the screw at FD on the rear panel. Then remove the tie bracket and set it aside.



PICTORIAL 2


P2
S201
5 HOLE
CONNECTOR
SHELL
1
5
BRN
P201
CPU
CIRCUIT
BOARD
FA
6-32 x 1/4"
SCREW

PICTORIAL 3

Refer to Pictorial 3 and perform the following steps.

( ) Remove the 6-32 × 1/4" screw at FA on the cabinet bottom.

( ) Carefully unplug the CPU board from the mother board.

( ) Remove the 5-hole connector shell from P201 on the CPU board. Then remove the CPU board and set it aside.

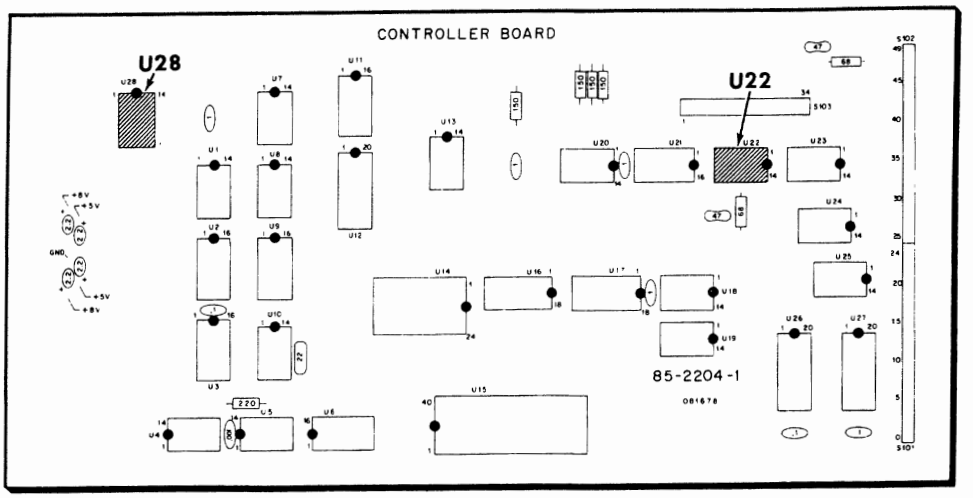
NOTE: If an HA-8-8 Extended Configuration option was previously installed in your Computer, remove it and proceed to "Configuration" on Page 10. If an HA-8-8 option was NOT installed and you DO NOT want to use ROM Disable (ORG 0), you can also bypass the following section.

ROM DISABLE (ORG 0)

The ROM Disable function is normally used with the CP/M operating system. Since the system RAM must be a continuous block originating at zero instead of 8 k, your first RAM circuit board will be addressed at 000 instead of 040 000 (2000 H).

You can also use this function with Microsoft Basic under HDOS, since the unused memory area between PAM-8 and the H-17 ROM/RAM is an excellent location for user functions. However, you must take care in this application that you do not overwrite the PAM-8 or H-17 ROM/RAM areas. This is because these areas now exist in read/write RAM rather than in ROM and write-protected RAM. You can also use up to 64 k of memory with this configuration. NOTE: If you have 64 k of memory, you must use HDOS Version 2.0 or higher. For less than 64 k of memory, you can use any version of HDOS.

This function allows an output to port 362 Q (F2H) to toggle the ROM disable line on the bus, based on the state of bit 5 (LSB = bit 0). ROM is disabled if bit 5 is a logic one. The CPU board itself also responds to this action by disabling the on-board ROM and accessing the system bus for memory references between 0 and 8 k.



PICTORIAL 4

To use the ROM Disable function, make the following modifications to the circuit boards in your H-8 Computer:

H-17 Controller Modification

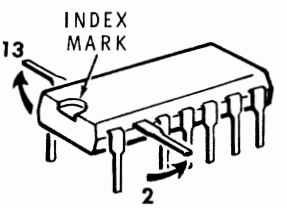
( ) Carefully unplug the H-17 controller board from your Computer.

NOTE: Earlier productions of the H-17 controller board did not have IC U28 installed in the upper left corner of the board (see Pictorial 4). If your board DOES have an IC U28, disregard the next four steps and proceed to "If an IC is installed at U28". If there is no IC at U28, perform the following four steps.

If there is no IC at U28 — Refer to Pictorial 4 and complete the following four steps. Then reinstall the controller circuit board in your computer.

1. ( ) Carefully remove IC U22 from its socket on the circuit board.

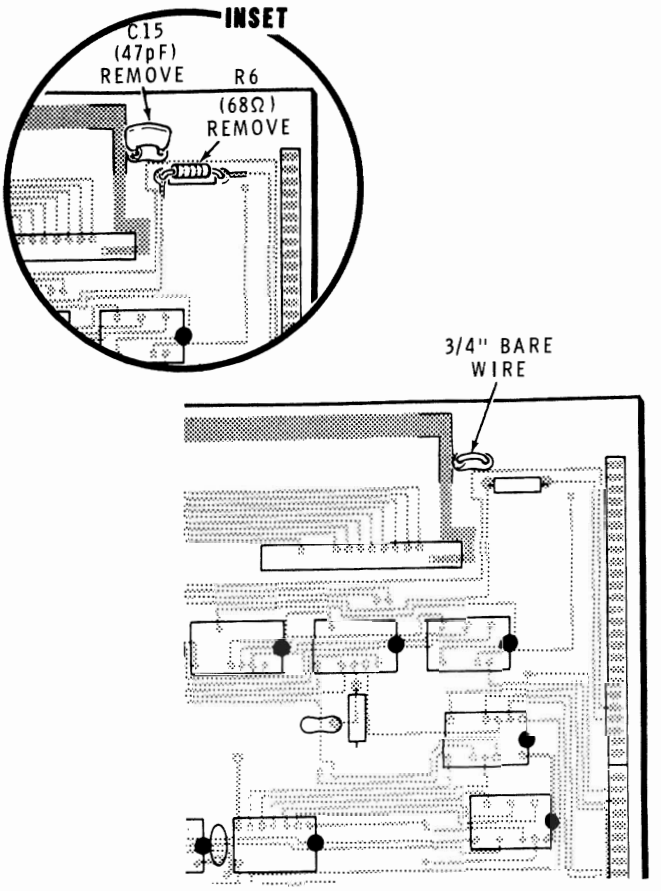
2. ( ) Refer to Detail 4A, position the IC as shown, and then bend pins 2 and 13 outward so they will not make contact when the IC is reinstalled.



Detail 4A

3. ( ) Reinstall the IC at U22. Make sure you position the pin 1 end toward the index mark on the circuit board.

4. ( ) Reinstall the controller board in the Computer and proceed to "Configuration".



PICTORIAL 5

If an IC is installed at U28 — Refer to Pictorial 5 and perform the following four steps.

1. ( ) Refer to the inset drawing and carefully clip both leads of resistor R6 (68 Ω, blu-gry-blk). Remove this resistor; it will no longer be used.

2. ( ) Refer again to the inset drawing and clip both leads of capacitor C15 (47pF mica). Remove this capacitor; it will no longer be used.

3. ( ) Cut a 3/4″ length of bare wire. Then solder this bare to the foils where the capacitor you removed was connected.

4. ( ) Reinstall the controller circuit board in your Computer and proceed to "Configuration".

CONFIGURATION

Your Computer memory boards and the status port on your Z80 CPU board must be configured to suit your total system.

Memory Board Configuration

Reconfigure the memory boards in your Computer so they are in sequence starting at 000.000 octal (0 k) instead of 040.000 octal (8 k). (To set the Model WH-8-16 16 k Memory Board to start at 0 k, push the four ORG ADDR switches to OFF, and the ENABLE switch to ON.) Refer to the separate manuals for each of your memory boards and make the necessary changes to each board. Then reinstall the boards in the Computer.

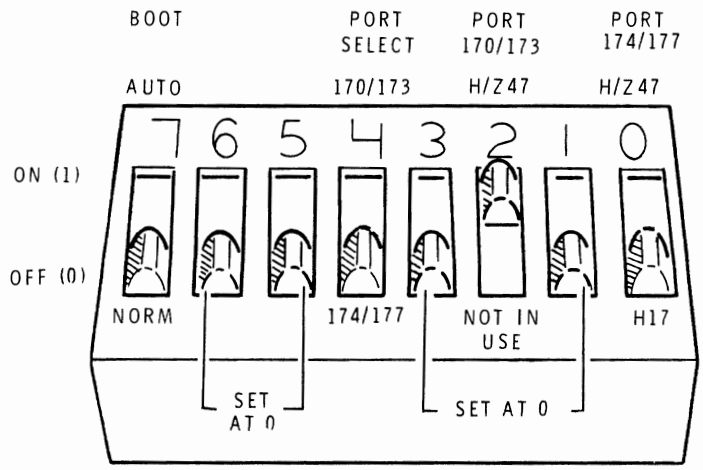


Figure 1
Status port switches

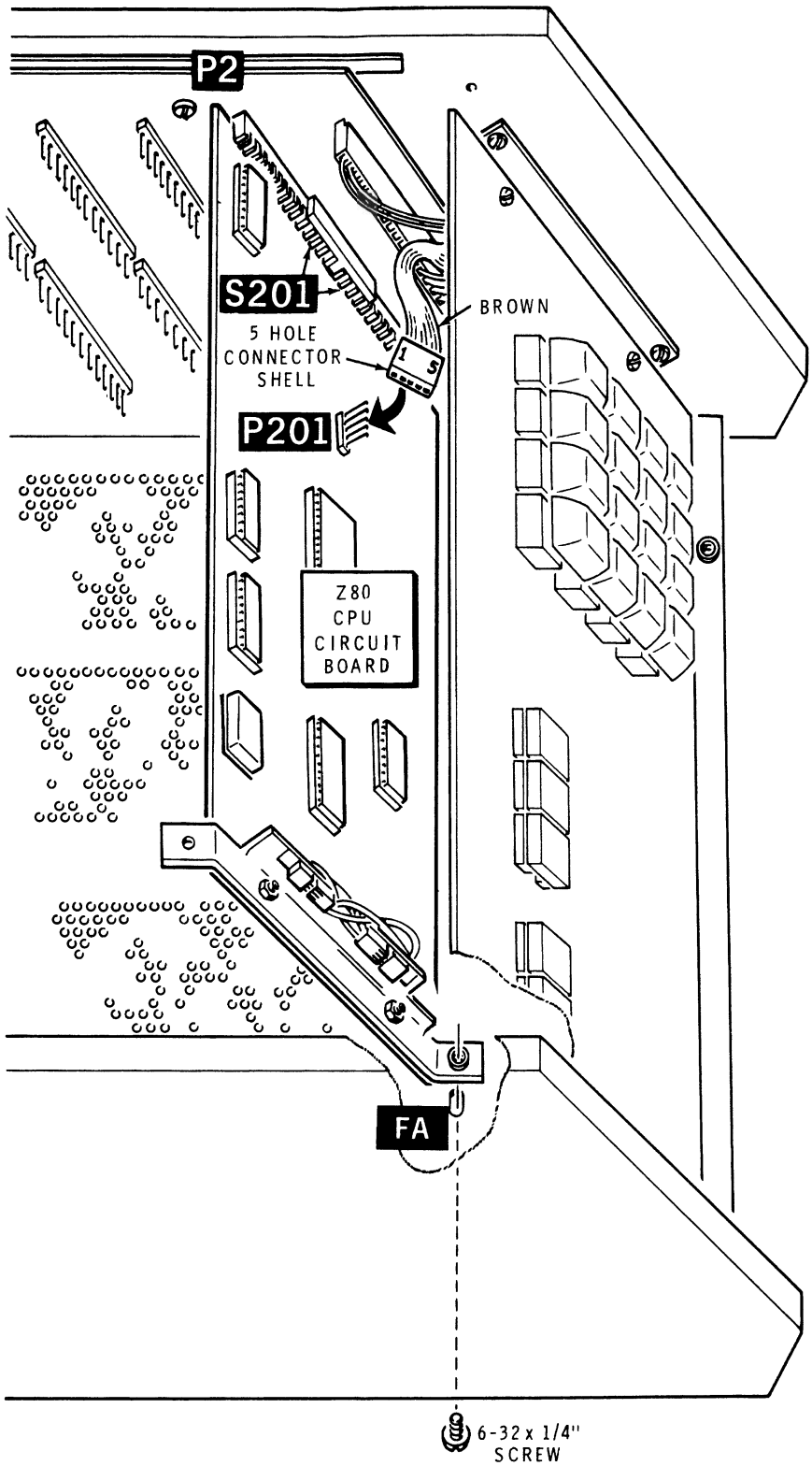
Status Port, Z80 CPU Board

Heath CP/M, HDOS version 2.0 or later, and some user programs will interrogate the status port to determine system configuration on boot-up.

Figure 1 shows the 8-section status switch and defines the function of each section. Set these switches according to your system configuration before you install the Z80 CPU board in your Computer.

SWITCH	SETTING	FUNCTION
7	0	Normal Boot
	1	Auto Boot
6	0	(SET AT ZERO)
5	0	(SET AT ZERO)
4	0	Boot from Port 174/177 (normal)
	1	Boot from Port 170/173
3	0	(SET AT ZERO)
2	0	Port 170/173 not in use
	1	Port 170/173 has H/Z47 (normal)
1	0	(SET AT ZERO)
0	0	Port 174/177 has H-17 Disk (normal)
	1	Port 174/177 has H/Z47 Disk

When you have set the status switches according to your system configuration, continue with the Installation instructions that follow.


P2
S201
5 HOLE
CONNECTOR
SHELL
BROWN
P201
Z80
CPU
CIRCUIT
BOARD
FA
6-32 x 1/4"
SCREW

PICTORIAL 6

INSTALLATION (Continued)

Refer to Pictorial 6 and perform the following steps.

( ) Carefully set the HA-8-6 Z80 CPU Board in the chassis and connect the 5-hole connector shell to P201. Make sure the brown lead is positioned as shown.

( ) Carefully plug S201 onto P2 of the mother board.

( ) Install a 6-32 × 1/4" screw at FA on the bottom of the Computer. Use one of the screws that were previously removed.

( ) Check all of the circuit boards to be sure they are mounted with screws to the bottom of the Computer.

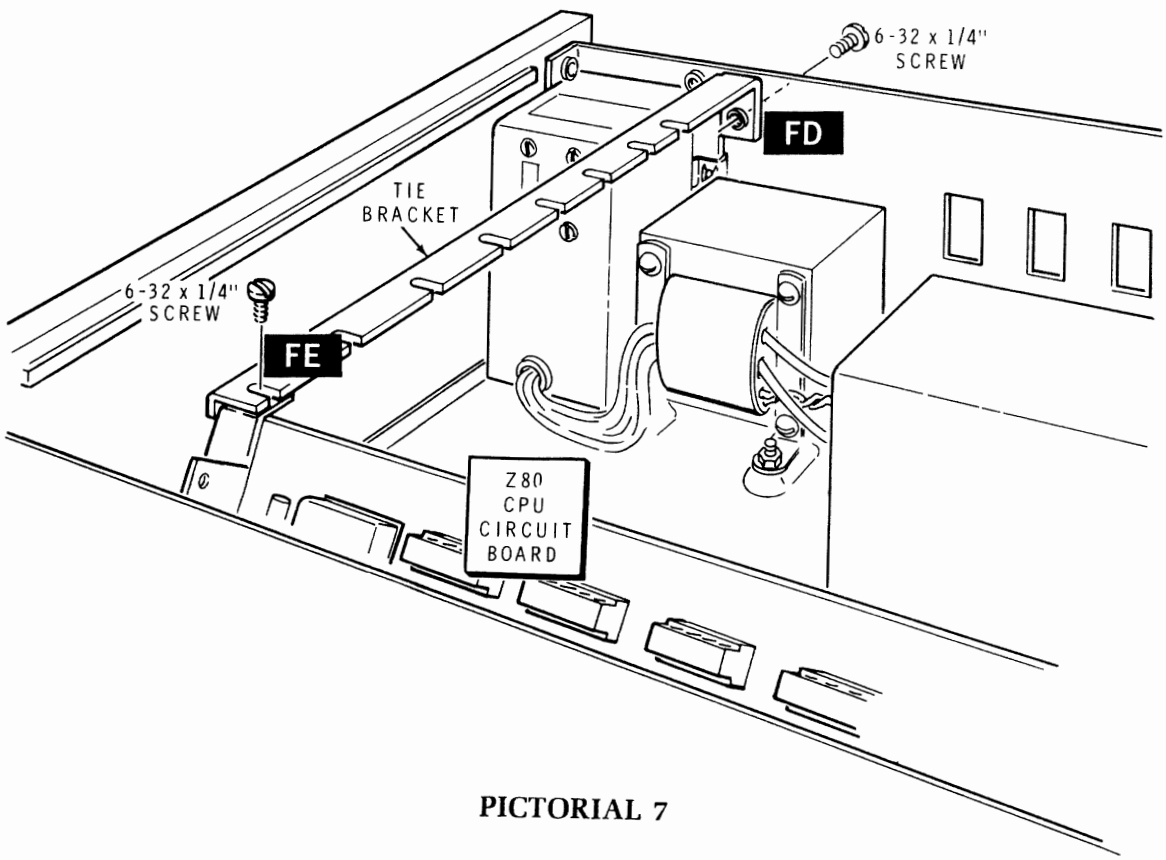
( ) Refer to Pictorial 7 and install the tie bracket. Be sure the screws on the top of the circuit boards are in the bracket slots.

( ) Start a 6-32 × 1/4" screw into the Z80 CPU board at FE, but do not tighten this screw.

( ) Secure the tie bracket to the rear panel with a 6-32 × 1/4" screw at FD. Tighten this screw.

( ) Now tighten each screw that holds a circuit board to the tie bracket.

This completes the installation of the CPU Board. Do not install the top cover on your Computer until you have completed the Checkout that follows.



PICTORIAL 7

CHECKOUT

( ) Make sure the POWER switch on the rear panel is in the OFF position.

( ) Connect the line cord to a proper AC outlet.

NOTE: Read the next step completely through so you will know what results to expect when you turn on the Computer. If you do not obtain the proper results, push the POWER switch to OFF and recheck your work in the modification and configuration of the circuit boards. Also be sure each circuit board is properly installed in the correct location and that connectors are also properly installed. If you still do not obtain the proper results, return the CPU board to Heath Company. See the Service Information on the inside rear cover of this Manual.

( ) Push the POWER switch to ON. The PWR, RUN, MON, and INT LED's should light and the Address and Data LED's should indicate the Stack Pointer address (upper memory limit).

( ) Push the POWER switch to OFF and unplug the line cord.

Proceed to the Final Assembly instructions that follow.

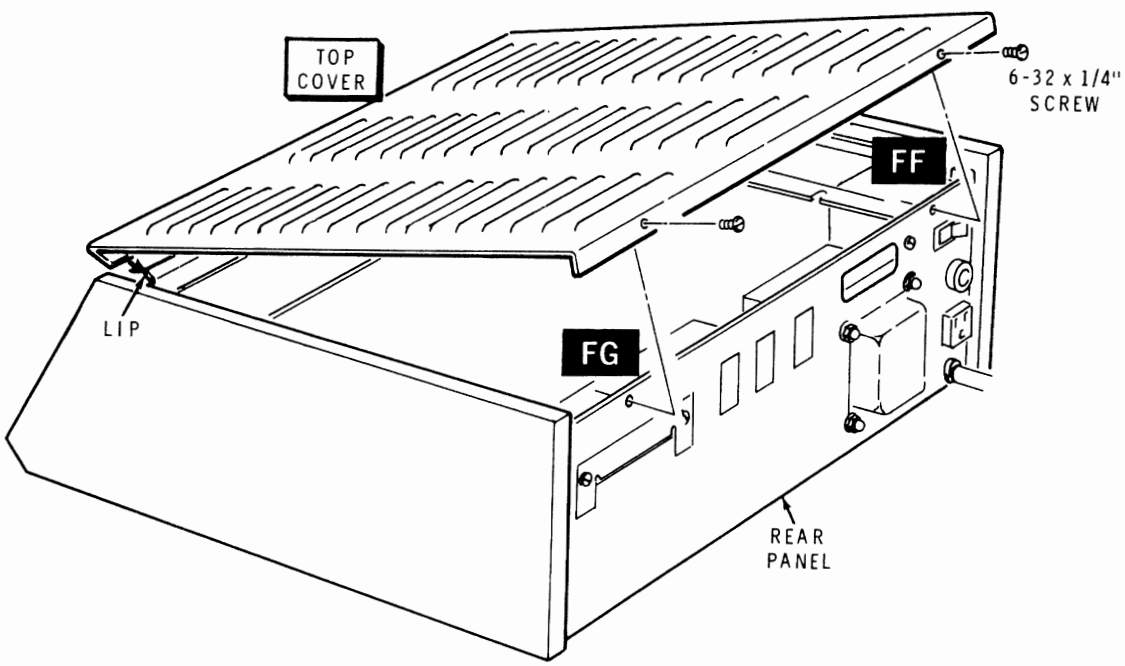
FINAL ASSEMBLY

Refer to Pictorial 8 and install the top cover on your Computer as follows:

( ) Hook the front of the top cover over the lip on the front panel. Then push the rear of the top cover down onto the edge of the rear panel.

( ) Secure the top cover to the rear panel with 6-32 × 1/4" screws at FF and FG.

This completes the Installation and Final Assembly.



PICTORIAL 8

OPERATION

With the Model HA-8-6 Z80 CPU Circuit Board installed in your H-8 Computer, you retain all the capabilities of the 8080 CPU described in your H-8 Operation Manual plus the advantages of the Z80 microprocessor. References to the 8080 also apply to the Z80 in the Operation Manual and in the XCON-8 Panel Monitor Manual, while the Z80 architecture and instruction set are described in the Z80 Programming Manual V2.0.

CIRCUIT DESCRIPTION

This Circuit Description is presented for those with a knowledge of computer logic and technology. It assumes that the Z80 CPU board is installed in an operating H-8 Computer for the Address, Data, Control, and other logic referenced in this description. Refer to the Schematic Diagram as you read this Circuit Description.

ADDRESS AND DATA BUS LOGIC

Address lines A0 through A15 from the Z80 microprocessor (U8) are buffered by U4 and U9. Lines A0 through A7 are then buffered and inverted by U16 and passed on to the bus. When BUSAK (Bus Acknowledge) is asserted, U16 will be turned off. This puts these bus address lines in a tri-state condition for DMA processing. Address lines A8 through A15 are buffered and inverted by U5 before being passed on to the bus. U5 will be turned off during DMA processing and I/O requests. More about that later.

IORQ (I/O Request) and $\overline{\text{BUSAK}}$ (inverted Bus Acknowledge) are NANDed together in U14A to produce $\overline{\text{IOADEN}}$ (I/O Address Enable), which will be asserted low during all I/O requests. This signal turns on U10 to put A0 through A7 on bus address lines A8 through A15 during I/O operations. $\overline{\text{BUSAK}}$ and $\overline{\text{IOADEN}}$ are NANDed in U14D to produce HBDSBL, which will be asserted high during DMA processing and I/O operations. This signal is used to turn U5 off at the proper times.

$\overline{\text{BUSAK}}$ and an optional interrupt acknowledge line are ORed in U25D to produce a $\overline{\text{DBDSBL}}$ (Data Bus Disable Line), which will be asserted low whenever $\overline{\text{BUSAK}}$ is asserted or the optional line is asserted low. The $\overline{\text{DBDSBL}}$ is NANDed with $\overline{\text{IOR}}$ (I/O Read) and $\overline{\text{BMEMR}}$ (Buffered Memory Read) in U35A to produce REN (Read Enable). REN will be asserted high during I/O reads, memory reads, or DMA processing. REN is then NANDed with $\overline{\text{ROMEN}}$ (ROM Enable) in U36B to produce $\overline{\text{REN}}$; which is asserted low during I/O reads, DMA processing, and memory reads to addresses other than the ROMs. Asserting $\overline{\text{REN}}$ turns on U28 to pass data from the data bus to U8. REN is also NANDed with $\overline{\text{DBDSBL}}$ to produce $\overline{\text{WEN}}$ (Write Enable), which remains asserted except during I/O reads, memory reads, or DMA processing. Asserting $\overline{\text{WEN}}$ turns on U27 to pass data from microprocessor U8 to the data bus.

ROM ADDRESSING AND CHIP SELECT LOGIC

Address lines A12, A13, A14 and A15 are NANDed together in U1 with the I/O Latch Enable Line and the ROM Disable line from the bus to produce ROMEN, which will be asserted low whenever the address on the bus is in the range of 0 through 017.377 octal and I/O Latch Enable and the ROM Disable line are not asserted. Jumper options E4 and E5 are used to enable the second ROM addresses. When this jumper is removed, ROMEN will go low whenever the address on the bus is in the range 0 through 037.377 octal. Both ROMs will be disabled if either I/O Latch Enable is asserted or the bus ROM Disable is brought low.

ROMEN is inverted by U20F to produce ROMEN, which is then NANDed with A12 and BMEMR (Buffered Memory Read) in U2B. The output of U2B is ROMSEL1 (ROM Select 1) and will be asserted low whenever a memory read operation is performed from memory addresses 0 through 017.377 octal. This drives the chip select input of ROM1. Jumper options E15, E16 and E17 allow for different types of ROMs installed in ROM1 socket.

ROMEN and BMEMR are also NANDed with A12 in U2C. The output of U2C is ROMSEL2 (ROM Select 2), and will be asserted low whenever a read operation is performed from memory addresses 020.000 octal through 037.377 octal (if the jumper between E4 and E5 has been removed). This drives the chip select input of ROM2. Jumper options E24, E25, and E26 allow for different types of ROMs at ROM2.

Addresses A0 through A11 are decoded inside of the ROMs. Data line D0 through D7 are connected directly to the data bus from U8.

MEMORY AND I/O READ-WRITE LOGIC

The IORQ (I/O Request), MREQ (Memory Request), WR (Write), and RD (Read) signals from microprocessor U8 are buffered and inverted U3 B,C,D, and E to produce IORQ, MREQ, WR, and RD. IORQ and RD are NANDed together in U21C to produce IOR. This signal will be asserted low whenever a read operation is performed to the port pointed to by the address bus. IORQ and WR are NANDed together in U21A to produce IOR (I/O Read). This signal will be asserted low whenever a write to port on the address bus is performed. MREQ and RD are ANDed together in U25C to produce BMEMRD (Buffered Memory Read). This signal will be asserted high whenever data is read from the memory location on the address bus. U11D inverts this signal to produce BMEMRD, which is NANDed with ROMEN in U21D to produce MEMR. This prevents MEMR (on the mother board) from being asserted when reading the ROMs. MREQ and WR are NANDed together in U21B to produce MEMW. This signal will be available on the mother board if a jumper is installed between E48 and E50.

An early memory write signal can be generated by sampling RFSH (Refresh), MREQ (Memory Request), and BMEMR (Buffered Memory Read). U12A and U25A do just that. RFSH and MREQ are ANDed by U25A, whose output will go high when MREQ is asserted and RFSH is not. This will enable U12A to latch the state of BMEMR with the next low-to-high transition of the CPU clock. If BMEMR is not asserted, pin 6 of U12 will go low for EMEMW (Enable Memory Write) to indicate a write operation. If BMEMR is asserted, pin 6 will remain high. When MREQ is negated, pin 1 of U12 will go low. This resets U12, causing pin 6 to go high, indicating the end of the write operation. This early write pulse will be put on the bus if a jumper is connected between E49 and E51.

The M1 (Machine 1) signal from U8 is inverted once by U3F to produce BM1 (Buffered M1). BM1 is inverted again by U3A so the M1 pulse on the bus is in proper phase.

MEMR, MEMW (or EMEMW), IOR, IOW, and BM1 are buffered and inverted by U22 before they are placed on the bus. When BUSAK is asserted, the outputs of U22 will go to a tri-state level to allow DMA processing.

STATUS AND COMMAND PORT

Address lines $\overline{A0}$, $\overline{A2}$, $\overline{A3}$, A1, A4, A5, A6, and A7 are NANDed together in U18 to decode the status and command port address (362Q). The output of U18 will go low when this address is on the address bus. This low is ANDed with $\overline{IOW}$ by U24C to produce W362L, which will be asserted low whenever a write to port 362Q is performed. The low from U18 is also ANDed with $\overline{IOR}$ by U24B to produce R362L, which will be asserted low whenever a read from port 362Q is performed.

Power Up switch SW1 is connected to buffer U31. When R362L is asserted, the information from SW1 will be inverted and passed on the the data bus by U31. Resistor pack R24 provides a pull-up resistor for each section of SW1.

When W362L is asserted, the state of Data Lines BD3, BD5, and BD6 are latched into U30. The latched output from BD6 is connected through R21 to the base of transistor Q1. When this latched output goes high, Q1 will turn on and sink current from the TTL device connected to P202. Jumper pad E46 allows you to connect this signal to any of the unused mother board connectors. The latched output from BD5 forms $\overline{I/O\ LATCH\ EN}$. The latched output from BD3 can be used as either $\overline{NMIMASK}$ or NMIMASK, depending on the option selected with jumper pads E30, E33, and E34. U30 will be cleared when $\overline{RESET}$ is asserted.

INTERUPT LOGIC

BM1 and IORQ are NANDed together to produce $\overline{BINTA}$ (Buffered Interrupt Acknowledge), which will be asserted low when the processor is ready to handle the interrupt request. The bus interupt lines ($\overline{INT10}$ through $\overline{INT70}$) and an optional level 0 interrupt line are connected to the 8 to 3 line priority encoder U38. The three output lines from U38 are used to form the proper RST instruction for the interrupt level in U26. When $\overline{BINTA}$ is asserted, the outputs of U26 are enabled to pass this RST instruction onto the data bus. Jumper option E43 allows you to connect the level 0 input to one of the unused bus lines. A jumper between E33 and E34 will put a NOP instruction, instead of a RST 0 instruction, on the data bus for a level 0 interrupt.

Data lines $\overline{D0}$, $\overline{D1}$, and $\overline{D4}$ through $\overline{D7}$ are inverted by U33. These data lines are NANDed with $\overline{D2}$ in U32 to produce $\overline{EIDI}$ (Enable Interrupt or Disable Interrupt), which will go low whenever a DI or EI instruction are on the data bus. $\overline{EIDI}$ and $\overline{D3}$ are ANDed together in U24D producing $\overline{373Q}$ which will be asserted low when an EI instruction is on the data bus. $\overline{D3}$ is also inverted by U11F and ANDed with EIDI to produce $\overline{363Q}$, which will go low when a DI instruction is on the data bus. $\overline{BINTA}$ and $\overline{RESET}$ are ORed in U25B. The output of U25B will go low when either $\overline{BINTA}$ or $\overline{RESET}$ is asserted. This clears U35A and B to turn the front panel interupt light off.

BM1 and BMEMR are NANDed together in U23C to procduce $\overline{OCF}$, which will be asserted low during the opcode fetch part of each machine cycle. $\overline{OCF}$ is inverted by U11E to produce OCF. The leading edge of OFC clocks the state of U35A into U35B. The Q output of U35B will then be high if the interupts are enabled. This high allows $\overline{363Q}$ to be gated through U36D. The low from U36D (when $\overline{363Q}$ is asserted) will be gated through U36C to the input of U35A. The trailing edge of $\overline{OCF}$ will latch the low from U36C into U35A, causing $\overline{Q}$ output to go high. This turns the front panel interupt light off. With the interrupts disabled, the leading edge of OCF will clock a low into U35B. This low keeps the output of U36D high allowing 373Q to be gated through and inverted by U36C. The high from U36C (when $\overline{373Q}$ is asserted) is clocked into U35A by the trailing edge of $\overline{OCF}$. This causes the $\overline{Q}$ output to go low and turn on the front panel interrupt light.

CLOCK LOGIC

An 18.432 mHz TTL oscillator is the source of the clock signal. This signal feeds a divide-by-9 circuit formed by U6 and U7. R4 and C9 form the power up reset circuit for this clock only. The time constant of this circuit keeps U6 and U7A in the reset state until the +5 volt supply is up. The CPU clock signal is inverted by U11A and passed on to the clock input of U8. When a jumper is installed between E1 and E2, the clock signal comes from the divide-by-9 clock circuit. When a jumper is installed between E2 and E3, and a jumper between E18 and E20, the CPU clock signal will come from the 02 clock line on the bus.

The 02 clock on the bus also comes from the divide-by-9 circuit. Jumper options E6, E7, E8, E9, E10 and E11 determine the phase of the 02 output with respect to the CPU clock output of the divide-by-9 circuit. With a jumper installed between E19 and E20, the 02 output of the divide-by-9 circuit is applied to the bus.

DMA LOGIC

The $\overline{\text{HOLD}}$ line from the bus is buffered by U15G and passed to pin 25 of U8 ($\overline{\text{BUSRQ}}$ input). When this line is asserted low, it tells the Z80 that another device requires use of the bus. At the end of the current machine cycle U8 will assert pin 23 low ($\overline{\text{BUSAK}}$ output). This output and an optional line from the bus are ORed in U14B to produce BUSAK, which is then inverted by U20C, producing $\overline{\text{BUSAK}}$. BUSAK and $\overline{\text{BUSAK}}$ are used to put the data, address and control buffers in a tri-state condition. $\overline{\text{BUSAK}}$ is also buffered by U15E and put on the bus $\overline{\text{HLDA}}$ line.

RESET LOGIC

$\overline{\text{RESIN}}$ (Reset In) is connected through R14 to pin 2 of timer U17. The trailing edge of the pulse will trigger the timer. The output pulse from U17 is inverted by U11B to produce $\overline{\text{BRESET}}$ (Buffered Reset) with a pulse width determined by R11 and C28. The time constant of R13 and C33 keep the trigger input (pin 2) of U17 at a low state until the +5 volt supply is up. Jumper options E12, E13, and E14, and E21, E22, and E23, determine the source of the reset pulse for the CPU logic. The reset pulse can come from either the reset logic or the $\overline{\text{RESET}}$ line on the bus.

POWER SUPPLY

+8 volts from the bus is applied to voltage regulators U40 and U41. These regulators provide the +5 volts to power the logic. C10, C15, C38, and C39 provide filtering for these regulators.

SPECIFICATIONS

CPU Type	Z80.
Clock	2.048 MHz.
ROM	4k Monitor. 000.000 to 017.377. Provisions for additional 4k 020.000 to 037.377.
Power Requirments	750 ma. Max @ 8 Vdc.

The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

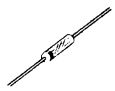
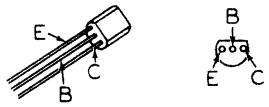
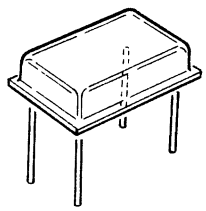
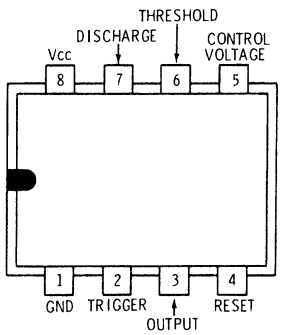
REPLACEMENT PARTS LIST

This list will show only those parts that may not be readily available. Resistors and capacitors are standard items that you may purchase through your local electronics parts distributor or store. Refer to the "Schematic Diagram" and "X-Ray Views" for the values of these parts. Diodes, transistors, and integrated circuits are listed in the "Semiconductor Identification Chart."

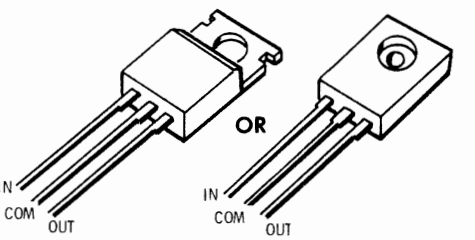
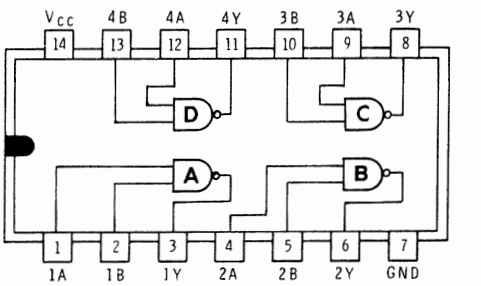
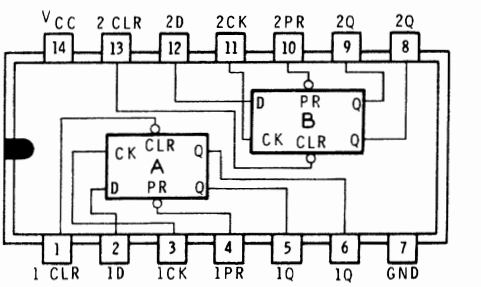
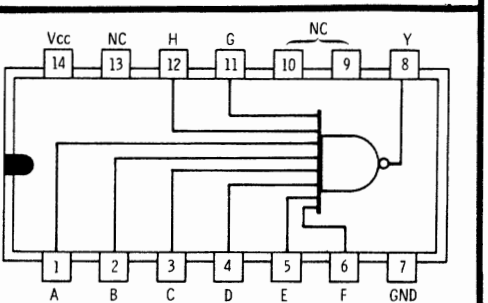
CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
R26, R27	9-118	Resistor Pack, 1000 Ω
R24	9-119	Resistor Pack, 10 kΩ
SW1	60-621	8-section, 2-position slide switch
P201	432-1082	5-pin Molex male connector
P202	432-986	3-pin Molex male connector
S201	432-1076	25-pin Molex female connector (2)

Heathkit®

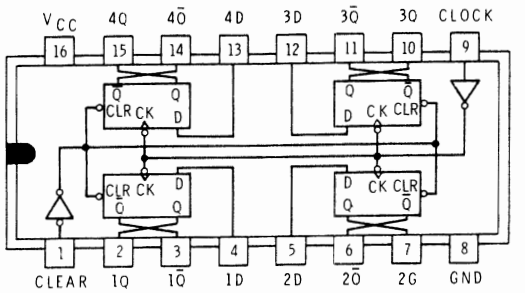
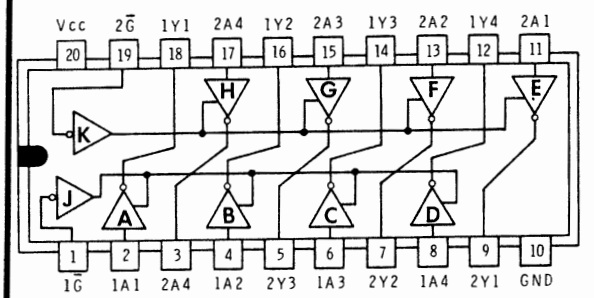
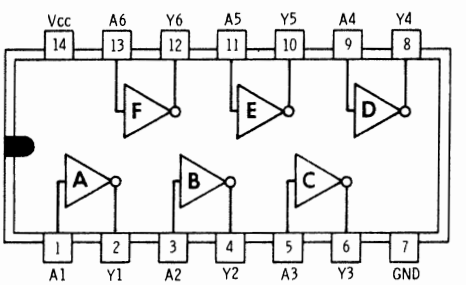
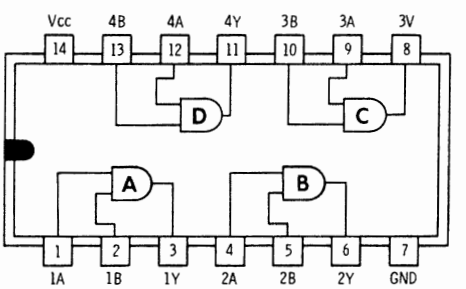
SEMICONDUCTOR IDENTIFICATION CHART

Heath Part No.	May Be Replaced With	Circuit Comp. No.	Description	Identification
56-56	1N4149	D1, D2, D3	Diode	
417-875	2N3904	Q1	NPN transistor	
150-117		Y1	18.432 MHz crystal oscillator	
442-53	NE555V	U17	Timer integrated circuit	

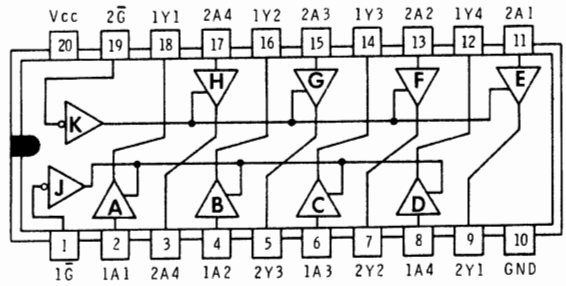
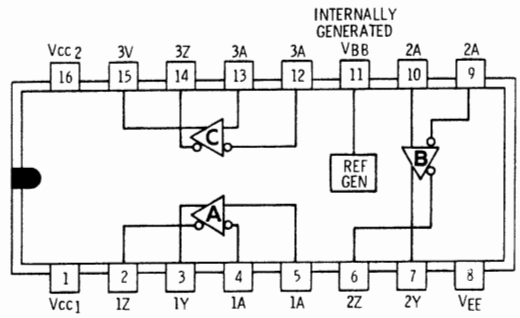
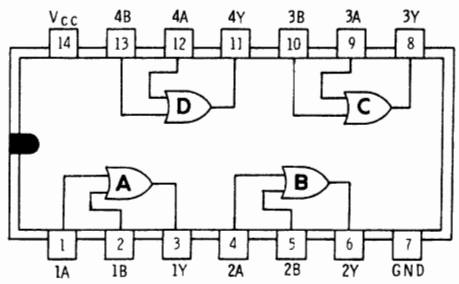
Semiconductor Identification Chart (Cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	Circuit Comp. No.	DESCRIPTION	Identification
442-54	UA7805	U40, U41	5-volt regulator IC	
443-728	74LS00	U14, U21, U23, U36	Quad 2-input NAND gate IC	
443-730	74LS74	U12, U35	Dual D flip-flop IC	
443-732	74LS30	U1, U18, U32	8-input NAND gate IC	

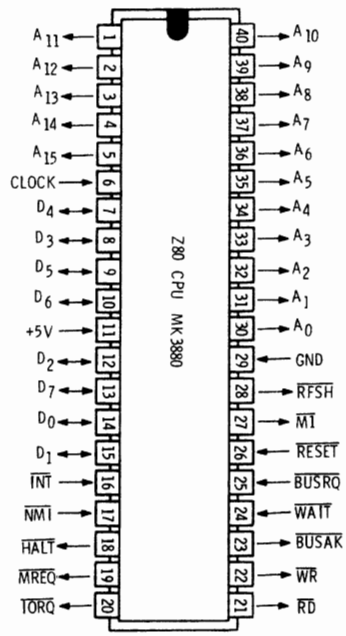
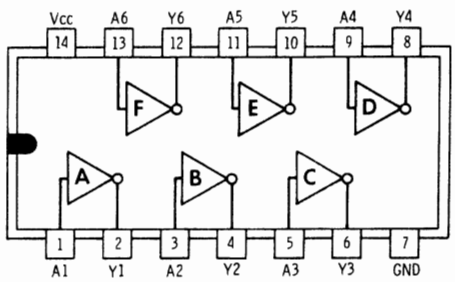
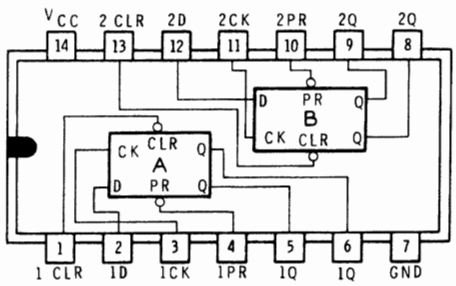
Semiconductor Identification Chart (Cont'd.)

Heath Part No.	May Be Replaced With	Circuit Comp. No.	Description	Identification
443-752	74LS175	U30	Quad Latch IC	
443-754	74LS240	U5, U10, U16, U22, U26, U27, U28, U31	3-state Octal buffer IC	
443-755	74LS04	U3, U20, U33	Hex Buffer IC	
443-780	74LS08	U25	Quad 2-input AND gate IC	

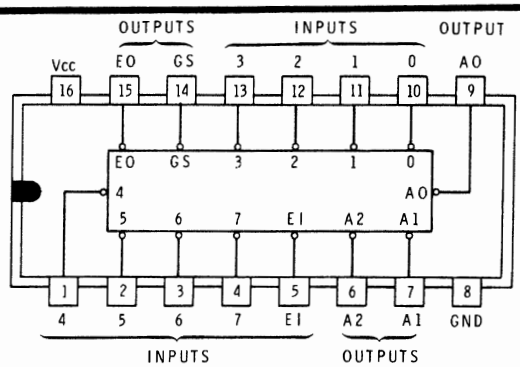
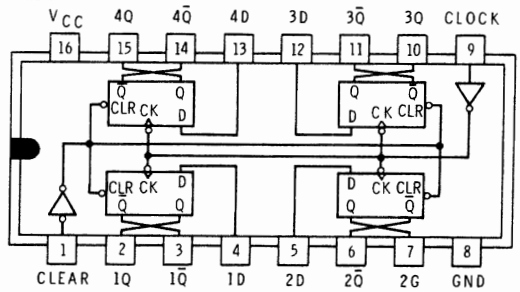
Semiconductor Identification Chart (Cont'd.)

Heath Part No.	May Be Replaced With	Circuit Comp. No.	Description	Identification
443-791	74LS244	U4, U9, U15	3-state non-inverting Octal buffer IC	
443-747	74LS10	U2	Triple 3-input NAND gate IC	
443-875	74LS32	U24	Quad 2-input OR gate IC	

Semiconductor Identification Chart (Cont'd.)

Heath Part No.	May Be Replaced With	Circuit Comp. No.	Description	Identification
443-881		U8	Z80 8-bit microprocessor IC	
443-897	74S04	U11	Hex inverter IC	
443-900	74S74	U7	Dual, D Flip-flop IC	

Semiconductor Identification Chart (Cont'd.)

Heath Part No.	May Be Replaced With	Circuit Comp. No.	Description	Identification
443-912	74LS148	U38	8 - 3 priority encoder IC	
443-983	74S175	U6	D flip-flop IC	
444-70		U13	4 k × 8 ROM IC