Heathkit® Manual

for the

PARALLEL I/O INTERFACE

Model H8-2

595-2033-02

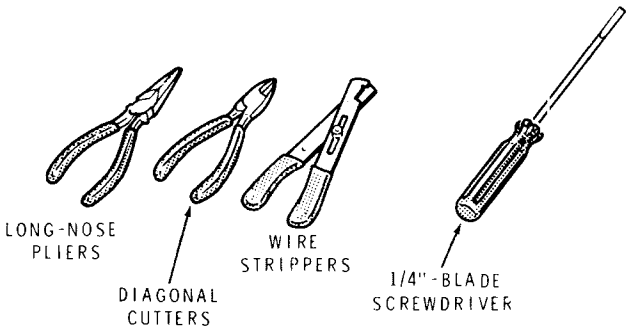
HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

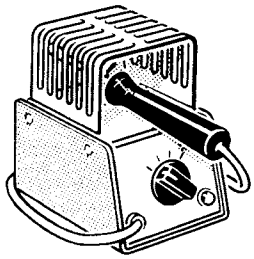
TABLE OF CONTENTS

ASSEMBLY NOTES

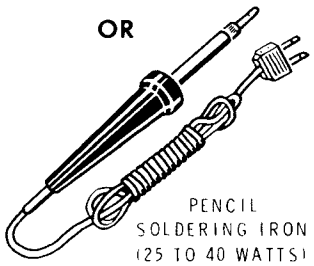
TOOLS

You will need these tools to assemble your kit.

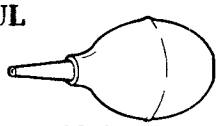


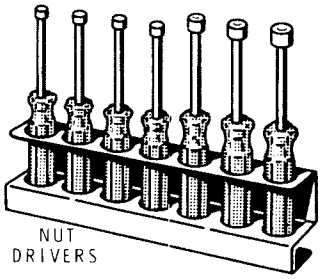


OR



OTHER HELPFUL TOOLS





*TO REMOVE SOLDER FROM CIRCUIT CONNECTIONS.

ASSEMBLY

1. Follow the instructions carefully. Read the entire step before you perform each operation.

2. The illustrations in the Manual are called Pictorials and Details. Pictorials show the overall operation for a group of assembly steps; Details generally illustrate a single step. When you are directed to refer to a certain Pictorial "for the following steps," continue using that Pictorial until you are referred to another Pictorial for another group of steps.

3. Most kits use a separate "Illustration Booklet" that contains illustrations (Pictorials, Details, etc.) that are too large for the Assembly Manual. Keep the "Illustration Booklet" with the Assembly Manual. The illustrations in it are arranged in Pictorial number sequence.

4. Position all parts as shown in the Pictorials.

5. Solder a part or a group of parts only when you are instructed to do so.

6. Each circuit part in an electronic kit has its own component number (R2, C4, etc.). Use these numbers when you want to identify the same part in the various sections of the Manual. These numbers, which are especially useful if a part has to be replaced, appear:

   — In the Parts List,

   — At the beginning of each step where a component is installed,

   — In some illustrations,

   — In the Schematic,

   — In the section at the rear of the Manual.

7. When you are instructed to cut something to a particular length, use the scales (rulers) provided at the bottom of the Manual pages.

SAFETY WARNING: Avoid eye injury when you cut off excess lead lengths. Hold the leads so they cannot fly toward your eyes.

SOLDERING

Soldering is one of the most important operations you will perform while assembling your kit. A good solder connection will form an electrical connection between two parts, such as a component lead and a circuit board foil. A bad solder connection could prevent an otherwise well-assembled kit from operating properly.

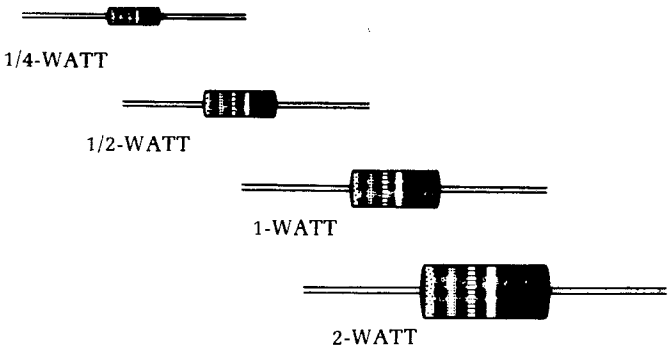
It is easy to make a good solder connection if you follow a few simple rules:

1. Use the right type of soldering iron. A 25 to 40-watt pencil soldering iron with a 1/8" or 3/16" chisel or pyramid tip works best.

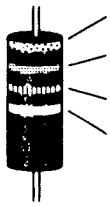
2. Keep the soldering iron tip clean. Wipe it often on a wet sponge or cloth; then apply solder to the tip to give the entire tip a wet look. This process is called tinning, and it will protect the tip and enable you to make good connections. When solder tends to "ball" or does not stick to the tip, the tip needs to be cleaned and retinned.

PARTS

Resistors will be called out by their resistance value in Ω (ohms), kΩ (kilohms), or MΩ (megohms). Certain types of resistors will have the value printed on the body, while others will be identified by a color code. The colors of the bands and the value will be given in the steps, therefore the following color code is given for information only.



EXAMPLES:



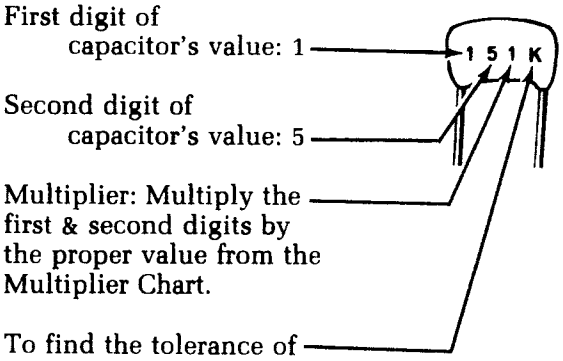
15 × 1,000 = 15,000 Ω (15,000 OHMS), or "15 kΩ"

30 × 100,000 = 3,000,000 Ω (or 3 MΩ)
3 MΩ = 3 MEGOHMS

RESISTOR COLOR CODE

COLOR	1st DIGIT	2nd DIGIT	MULTIPLY BY
BLACK	0	0	1
BROWN	1	1	10
RED	2	2	100
ORANGE	3	3	1,000
YELLOW	4	4	10,000
GREEN	5	5	100,000
BLUE	6	6	1,000,000
VIOLET	7	7	10,000,000
GRAY	8	8	100,000,000
WHITE	9	9	1,000,000,000
GOLD			.1
SILVER			.01

Capacitors will be called out by their capacitance value in μF (microfarads) or pF (picofarads) and type: ceramic, Mylar*, electrolytic, etc. Some capacitors may have their value printed in the following manner:



EXAMPLES:

151K = 15 × 10 = 150 pF
759 = 75 × 0.1 = 7.5 pF

NOTE: The letter "R" may be used at times to signify a decimal point; as in: 2R2 = 2.2 (pF or μF).

MULTIPLIER		TOLERANCE OF CAPACITOR		
FOR THE NUMBER.	MULTIPLY BY:	10pF OR LESS	LETTER	OVER 10pF
0	1	±0.1pF	B	
1	10	±0.25pF	C	
2	100	±0.5pF	D	
3	1000	±1.0pF	F	±1%
4	10,000	±2.0pF	G	±2%
5	100,000		H	±3%
			J	±5%
8	0.01		K	±10%
9	0.1		M	±20%

*DuPont Registered Trademark

PARTS LIST

Check each part against the following list and the Parts Pictorial (Illustration Booklet, Page 1). Any part that is packed in an individual envelope with a part number on it should be placed back in the envelope after you identify it until it is called for in a step. Do not throw away any packing material until all parts are accounted for.

To order a replacement part, always include the Part Number and use the Parts Order Form furnished with this kit. If a Parts Order Form is not available, use one of the Expedited Parts Order Forms at the rear of this Manual, or refer to "Replacement Parts" inside the rear cover. Your Warranty is inside the front cover. For pricing information, refer to the separate "Heath Parts Price List."

RESISTORS, 1/4-Watt

NOTE: The following resistors have a 5% tolerance (gold fourth band). The resistors may be packed in more than one envelope. Open all the resistor envelopes before you check the resistors against the Parts List.

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.
A1	1-62-12	1	220 Ω (red-red-brown)	R103
A1	1-92-12	1	330 Ω (orange-orange-brown)	R102
A1	1-65-12	1	470 Ω (yellow-violet-brown)	R104
A1	1-69-12	13	1000 Ω (brown-black-red)	R101, R105, R106, R107 R108, R115, R116, R117 R118, R125, R126, R127, R128

CAPACITORS

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.
B1	21-95	13	.1 μF ceramic	C103 thru C109, C113 thru C118
B2	25-221	4	2.2 μF tantalum	C101, C102, C111, C112

DIODES

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.
C1	56-56	24	1N4149	D100 thru D107, D110 thru D117 D120 thru D127

TRANSISTOR — INTEGRATED CIRCUITS

IMPORTANT: If any components are missing from the sealed IC package, return the unopened package for replacement. Claims for missing IC's will not be honored.

Transistors — Integrated Circuits (cont'd.)

If you locate damaged or defective IC's, order individual replacements. Be sure to follow the standard instructions on the "Parts Order Form" and on the inside rear cover of the manual. Save defective or damaged components for return instructions.

Transistors and integrated circuits (IC's) are marked for identification in one of the following four ways:

1. Part number.
2. Type number (This refers only to the numbers, disregard any letters before or after the number.)
3. Part number and type number.
4. Part number with a type number other than the one shown

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.
C2	417-875	1	2N3904 transistor	Q131
C3	442-54	2	7805 IC	IC144, IC145
C4	443-6	1	7474 IC	IC132
C4	443-12	1	7410 IC	IC142
C4	443-46	3	7402 IC	IC105, IC115, IC125
C4	443-731	1	74LS290 IC	IC131
C4	443-54	3	7403 IC	IC106, IC116, IC126
C4	443-698	6	7486 IC	IC101, IC102, IC111, IC112, IC121, IC122
C4	443-755	5	74LS04 IC	IC109, IC119, IC129, IC139, IC141
C5	443-53	3	7442 IC	IC134, IC135, IC138
C5	443-822	2	74LS139 IC	IC133, IC136
C5	443-841	6	74120 IC	IC107, IC108, IC117, IC118, IC127, IC128

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.

Transistor — Integrated Circuits (cont'd.)

C6	443-754	2	74LS240 IC	IC137, IC143

NOTE: The following IC's are packed in a protective foam material. DO NOT remove this foam material until you are instructed to do so or the IC can be damaged by static electricity.

C7	443-776	3	8251 IC	IC103, IC113, IC123
C8	443-761	3	6402 IC	IC104, IC114, IC124

CONNECTORS — SOCKETS

D1	432-704	1	24-hole connector plug
D2	432-865	2	3-hole connector shell
D3	432-946	3	25-pin circuit board plug
D4	432-947	2	25-hole circuit board socket
D5	432-948	4	25-hole connector socket
D6	434-298	20	14-pin IC socket
D7	434-299	11	16-pin IC socket
D8	434-311	2	20-pin IC socket
D9	434-312	3	28-pin IC socket
D10	434-253	3	40-pin IC socket
D11	432-855	25	Female connector pin
D12	432-866	85	Spring connector

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.

HARDWARE

E1	250-56	6	6-32 × 1/4" screw
E2	252-3	4	6-32 nut
E3	254-1	4	#6 lockwasher

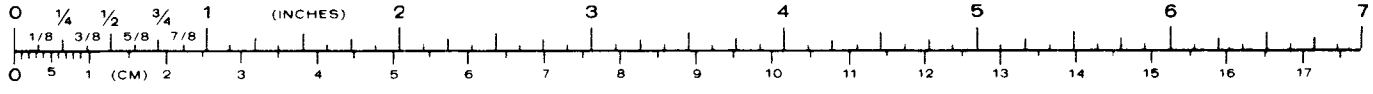
WIRE — CABLE

	134-1023	1	Interconnect cable
	344-55	5'	Green wire
	344-111	6"	Orange wire
	344-120	6"	Black wire
	344-121	6"	White wire

MISCELLANEOUS

	73-151	1	Double-stick tape
	85-2075-1	1	Parallel I/O circuit board
	204-2266	1	Bracket
F1	266-966	1	Connector key
F2	352-13	1	Silicone grease
	391-34	1	Blue and white label
	490-185	1	*Soder Wick
	597-260	1	Parts Order Form
		1	Assembly Manual (See Page 1 for the part number.)
			Solder

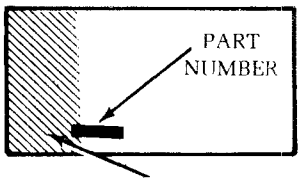
*Registered Trademark, Solder Removal Company



STEP-BY-STEP ASSEMBLY

CIRCUIT BOARD ASSEMBLY

IDENTIFICATION DRAWING



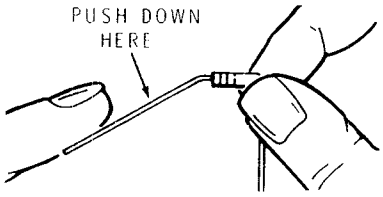
The steps performed in this Pictorial are in this area of the circuit board.

START

Position the circuit board as shown in the Identification Drawing at the top of the Page. The other side of the board is the foil side.

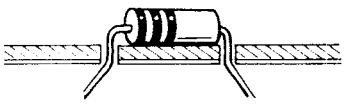
In the following steps, you will be given detailed instructions on how to install and solder the first part on the circuit board. Read and perform each step carefully. Then use the same procedure whenever you install parts on a circuit board.

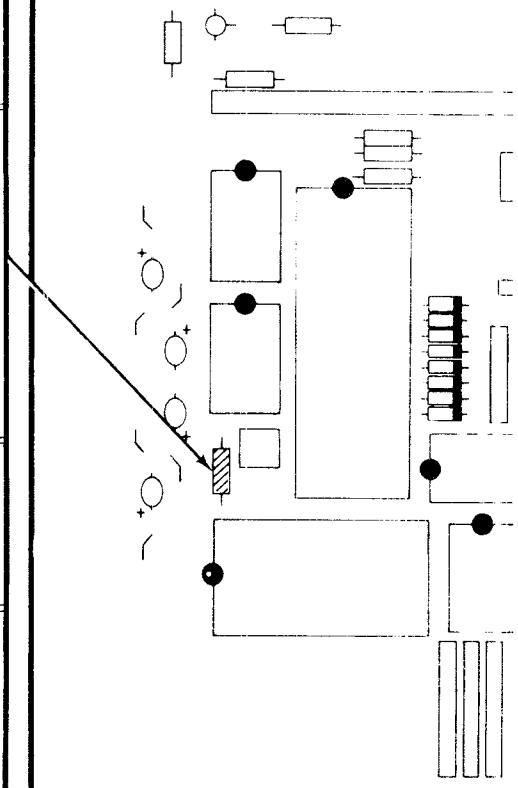
( ) R105: Locate a 1000 Ω (brown-black-red) resistor. Hold the resistor and bend the leads straight down as shown.



( ) Push the leads through the holes at the indicated location on the circuit board. The end with color bands may be positioned either way.

( ) Press the resistor against the circuit board. Then bend the leads outward slightly to hold the resistor in place.



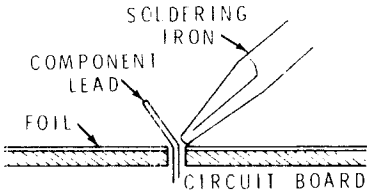


PICTORIAL 1-1

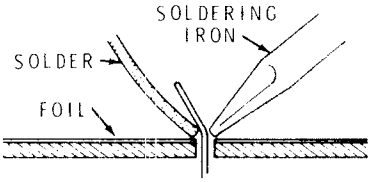
CONTINUE

( ) Solder the resistor leads to the circuit board as follows:

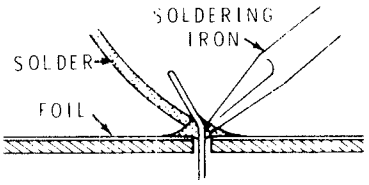
1. Push the soldering iron tip against both the lead and the circuit board foil. Heat **both** for two or three seconds.



2. Then apply solder to the other side of the connection. IMPORTANT: Let the heated lead and the circuit board foil melt the solder.



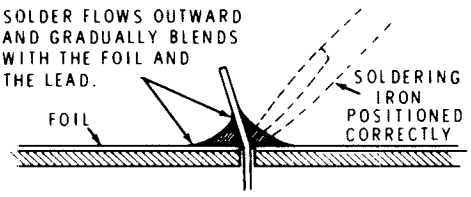
3. As the solder begins to melt, allow it to flow around the connection. Then remove the solder and the iron and let the connection cool.



( ) Cut off the excess lead lengths close to the connection. WARNING: Clip the leads so the ends will not fly toward your eyes.

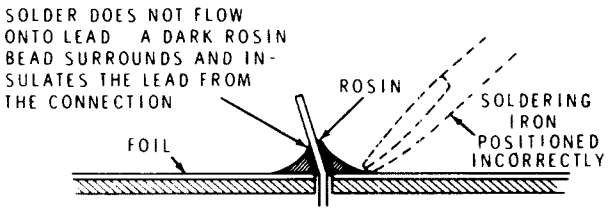
( ) Check each connection. Compare it to the illustrations on Page 9. After you have checked the solder connections, proceed with the assembly on Page 10. Use the same soldering procedure for each connection.

A GOOD SOLDER CONNECTION

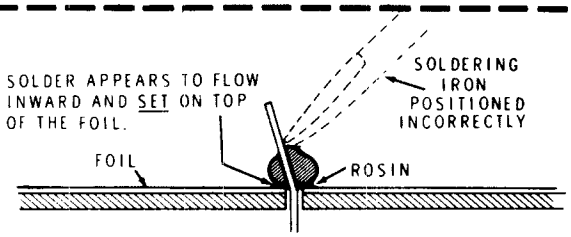


When you heat the lead and the circuit board foil at the same time, the solder will flow evenly onto the lead and the foil. The solder will make a good electrical connection between the lead and the foil.

POOR SOLDER CONNECTIONS



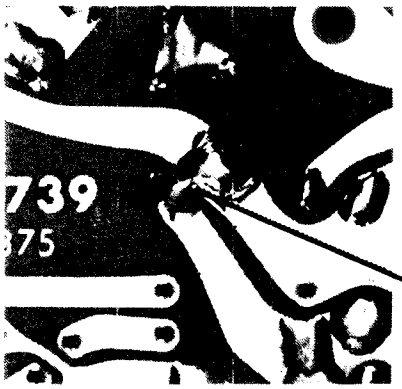
When the lead is not heated sufficiently, the solder will not flow onto the lead as shown above. To correct, reheat the connection and, if necessary, apply a small amount of additional solder to obtain a good connection.



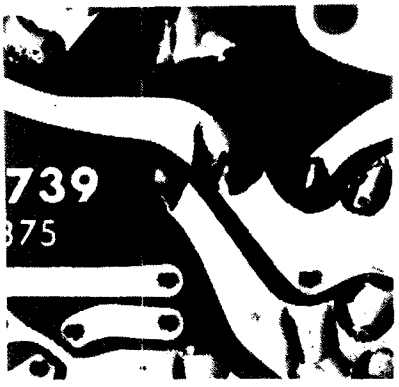
When the foil is not heated sufficiently the solder will blob on the circuit board as shown above. To correct, reheat the connection and, if necessary, apply a small amount of additional solder to obtain a good connection.

SOLDER BRIDGES

A solder bridge between two adjacent foils is shown in photograph **A**. Photograph **B** shows how the connection should appear. A solder bridge may occur if you accidentally touch an adjacent previously soldered connection, if you use too much solder, or if you "drag" the soldering iron across other foils as you remove it from the connection. A good rule to follow is: always take a good look at the foil area around each lead before you solder it. Then, when you solder the connection, make sure the solder remains in this area and does not bridge to another foil. This is especially important when the foils are small and close together. NOTE: It is alright for solder to bridge two connections on the same foil.



Use only enough solder to make a good connection, and lift the soldering iron straight up from the circuit board. If a solder bridge should develop, turn the circuit board foil-side-down and heat the solder between connections. The excess solder will run onto the tip of the soldering iron, and this will remove the solder bridge. NOTE: The foil side of most circuit boards has a coating on it called "solder resist." This is a protective insulation to help prevent solder bridges.



START

NOTE: Do not solder components to the printed side of the circuit board, only to the foil side.

IMPORTANT: Make sure you have installed the first resistor on Page 8.

( ) R103: 220 Ω (red-red-brown).

( ) R102: 330 Ω (orange-orange-brown)

( ) R104: 470 Ω (yellow-violet-brown).

Install 1000 Ω (brown-black-red) resistors at the following locations.

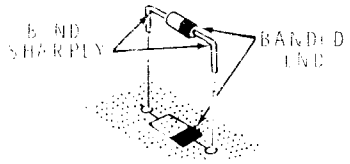
( ) R106

( ) R107

( ) R108

( ) Solder the leads to the foil and cut off the excess lead lengths.

Install 1N4149 diodes (#56-56) at the following locations. Be sure to position the banded end as shown on the circuit board. Bend both leads sharply to prevent shorting to top foil.



( ) D100

( ) D101

( ) D102.

( ) D103

( ) D104

( ) D105.

( ) D106

( ) D107.

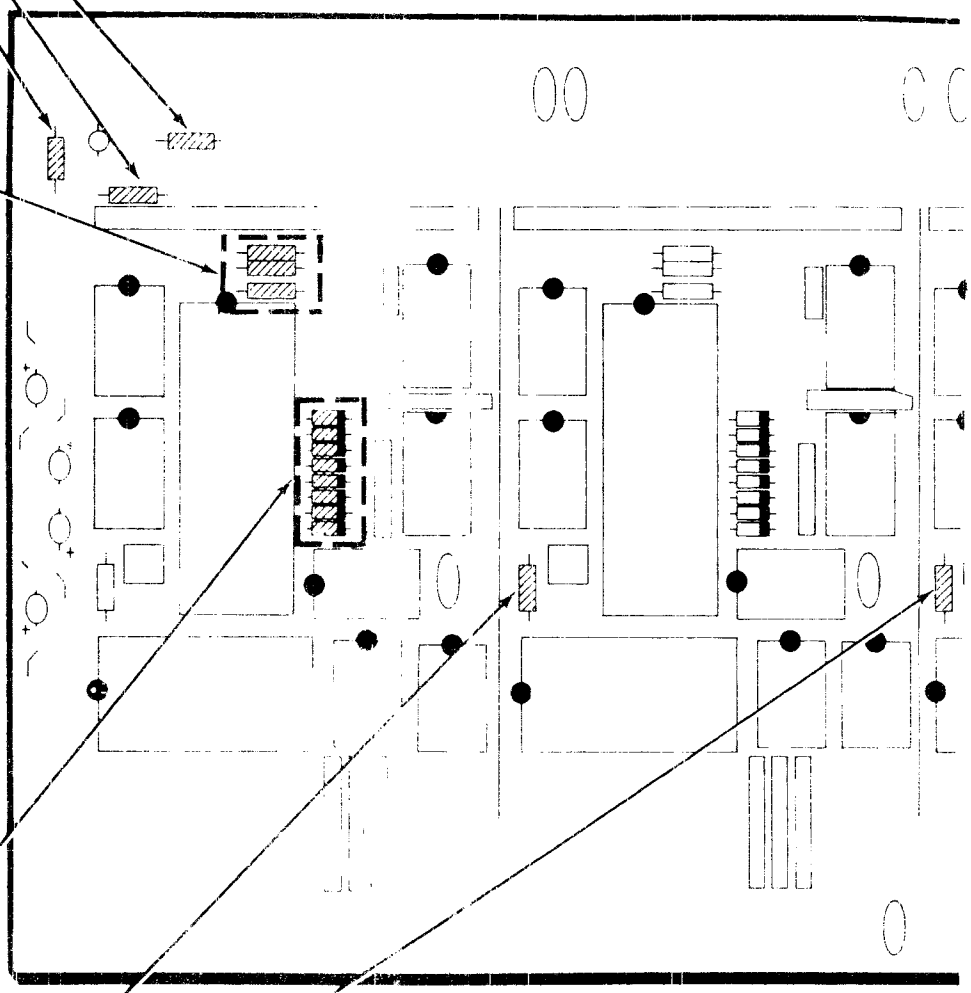
( ) R115: 1000 Ω (brown-black-red)

( ) R125: 1000 Ω (brown-black-red)

( ) Solder the leads to the foil and cut off the excess lead lengths

The steps performed in this Pictorial are in this area of the circuit board.

IDENTIFICATION DRAWING



PICTORIAL 1-2

START

Install 1000 Ω (brown-black-red) resistors at the following locations.

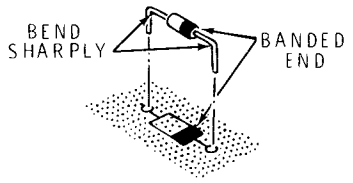
( ) R101

( ) R126.
( ) R127.
( ) R128.

( ) R116.
( ) R117.
( ) R118.

( ) Solder the leads to the foil and cut off the excess lead lengths.

Install 1N4149 diodes (#56-56) at the following locations. Be sure to position the banded end as shown on the circuit board. Bend both leads sharply to prevent shorting to top foil.



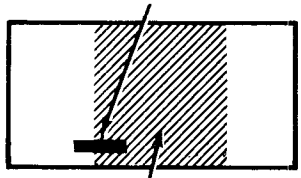
( ) D110.
( ) D111.
( ) D112.
( ) D113.
( ) D114.
( ) D115.
( ) D116.
( ) D117.

( ) Solder the leads to the foil and cut off the excess lead lengths.

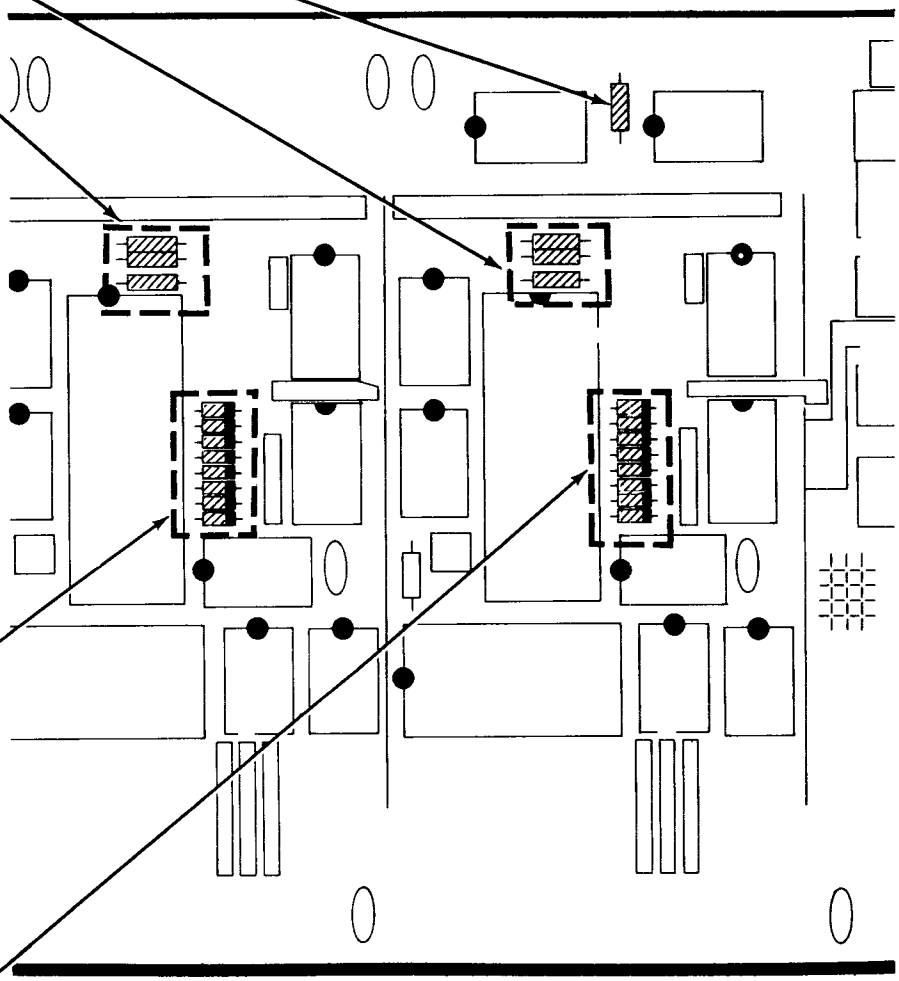
( ) D120.
( ) D121.
( ) D122.
( ) D123.
( ) D124.
( ) D125.
( ) D126.
( ) D127.

( ) Solder the leads to the foil and cut off the excess lead lengths.

IDENTIFICATION DRAWING

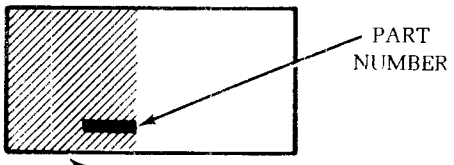


The steps performed in this Pictorial are in this area of the circuit board.



PICTORIAL 1-3

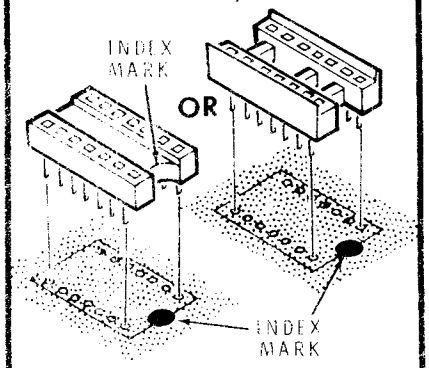
IDENTIFICATION DRAWING



The steps performed in this Pictorial are in this area of the circuit board.

START

NOTE: 14-pin, 16-pin, 20-pin, 28-pin, and 40-pin IC sockets are used in this kit. Be very careful when you install the sockets, as it is possible to place a 14-pin socket in a 16-pin socket location by mistake. Make sure all pins are straight and insert the socket pins into the circuit board holes. The index mark on the circuit board must still be visible after it is installed. Solder the pins to the foil.



( ) 16-pin IC socket at IC107.

( ) 14-pin IC socket at IC101.

( ) 14-pin IC socket at IC102.

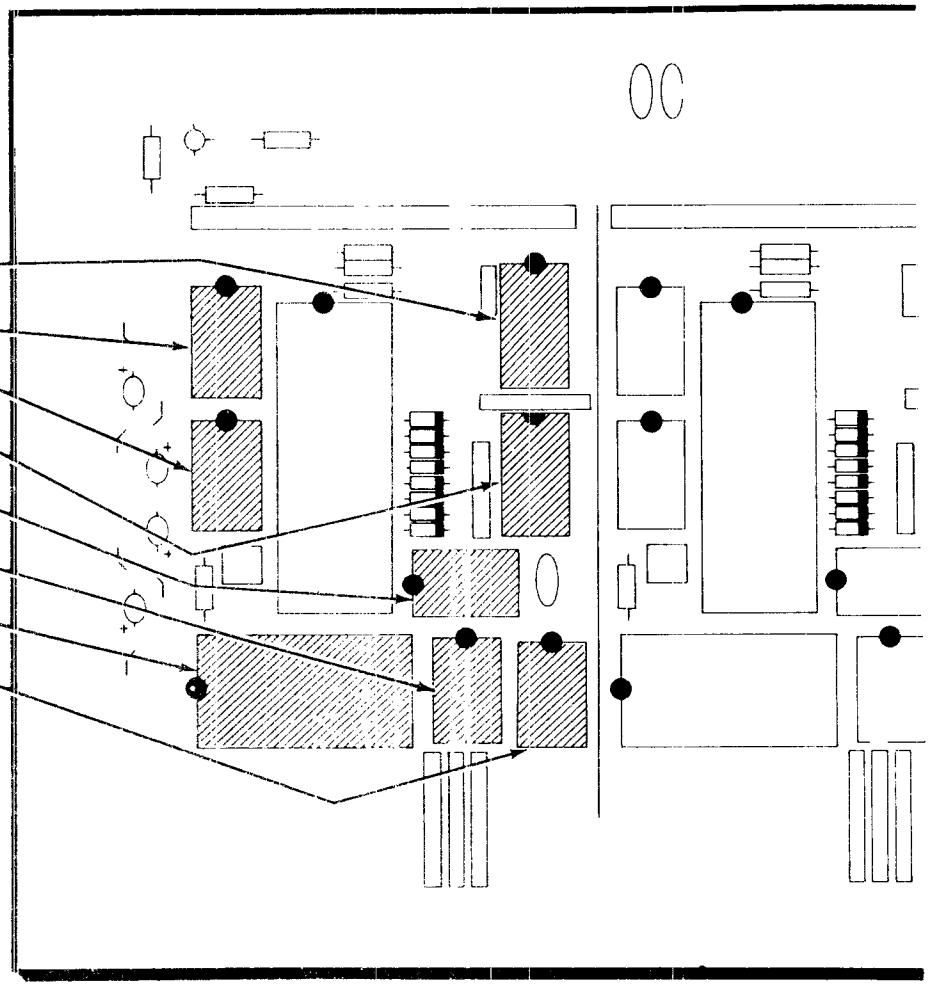
( ) 16-pin IC socket at IC108.

( ) 14-pin IC socket at IC105.

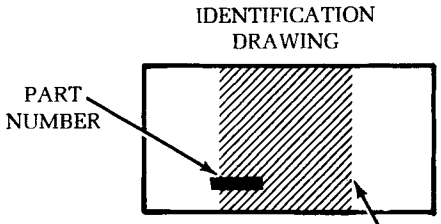
( ) 14-pin IC socket at IC106.

( ) 28-pin IC socket at IC103.

( ) 14-pin IC socket at IC109.



PICTORIAL 1-4



The steps performed in this Pictorial are in this area of the circuit board.

START

Install the following IC sockets in the same manner as before.

14-pin IC sockets at:

( ) IC131.
( ) IC132.

14-pin IC sockets at:

( ) IC121.
( ) IC122.

16-pin IC sockets at:

( ) IC117.
( ) IC118.

14-pin IC sockets at:

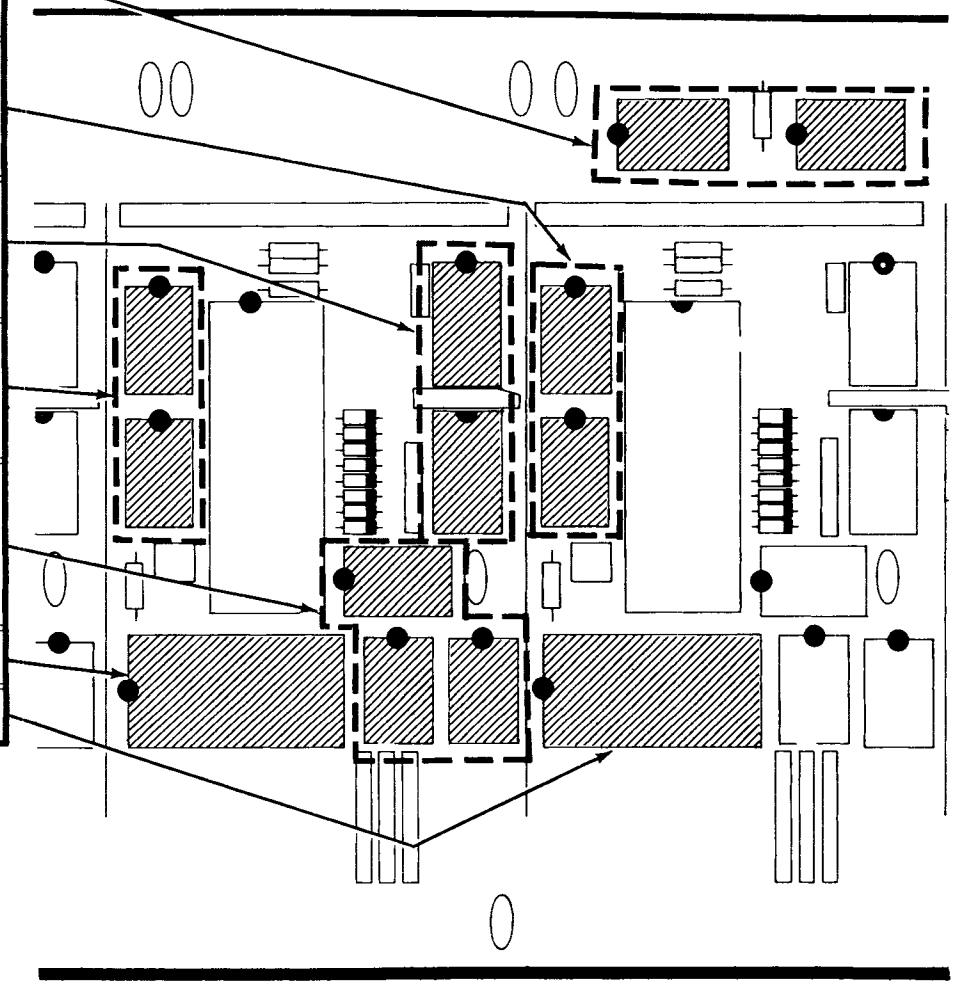
( ) IC111.
( ) IC112.

14-pin IC sockets at:

( ) IC115.
( ) IC116.
( ) IC119.

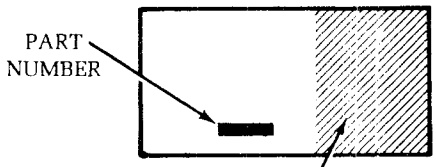
( ) 28-pin IC socket at IC113.

( ) 28-pin IC socket at IC123.



PICTORIAL 1-5

IDENTIFICATION
DRAWING



The steps performed in this Pictorial are in this area of the circuit board.

START

Install the following IC sockets in the same manner as before.

16-pin IC sockets at:

( ) IC133.
( ) IC138.

16-pin IC sockets at:

( ) IC134.
( ) IC135.

( ) IC136.

16-pin IC sockets at:

( ) IC127.
( ) IC128.

14-pin IC sockets at:

( ) IC125.
( ) IC126.
( ) IC129.

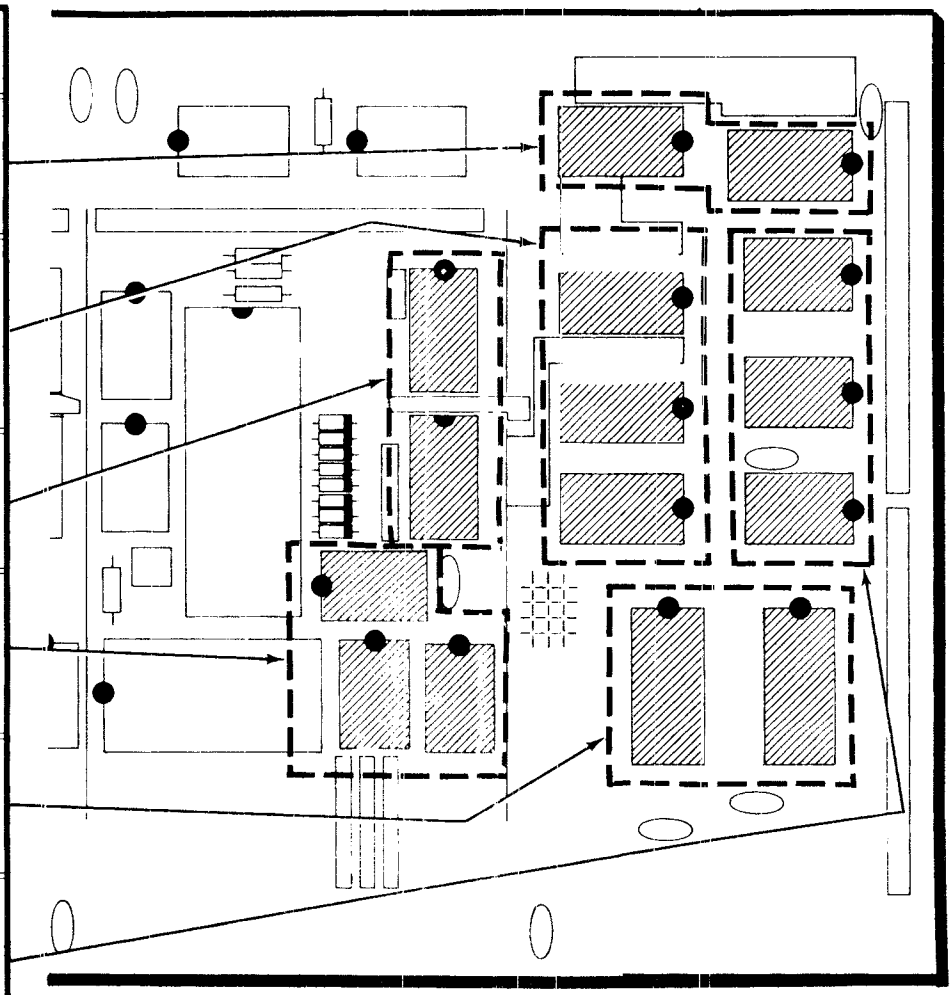
20-pin IC sockets at:

( ) IC137.
( ) IC143.

14-pin IC sockets at:

( ) IC139.
( ) IC141.

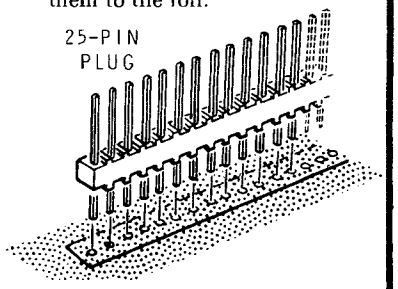
( ) IC142.



PICTORIAL 1-6

START

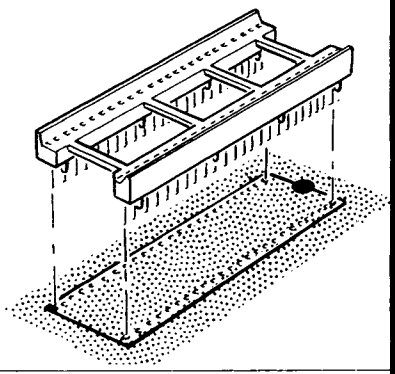
( ) P121: 25-pin circuit board plug. Install the short pins through the circuit board and solder them to the foil.



( ) P111: 25-pin circuit board plug.

( ) P101: 25-pin circuit board plug.

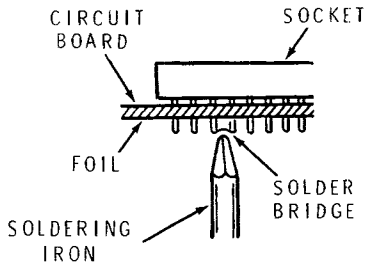
( ) Install a 40-pin IC socket at IC104 as shown. Push the socket firmly against the circuit board and solder the pins to the foil.

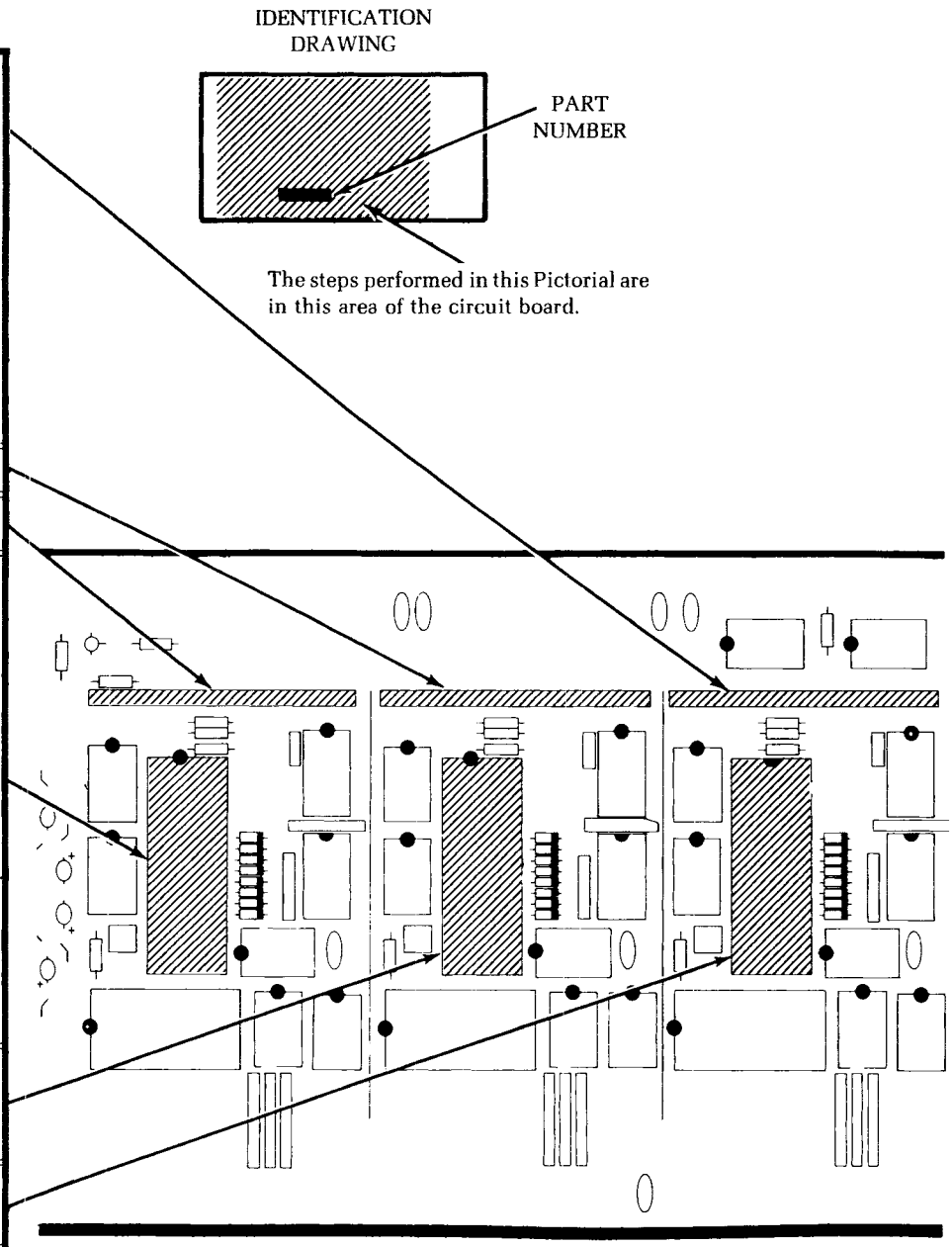


( ) Install a 40-pin IC socket at IC114. Solder the pins to the foil.

( ) 40-pin IC socket at IC124. Solder the pins to the foil.

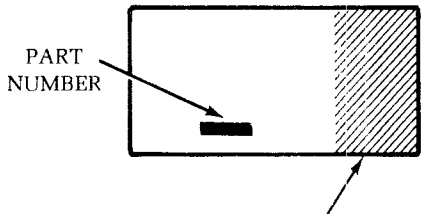
( ) Carefully check each socket for solder bridges between pins. If a solder bridge has occurred, hold the circuit board foil-side-down as shown, and hold the soldering iron tip between the two points that are bridged. The solder will flow down the soldering iron tip.





PICTORIAL 1-7

IDENTIFICATION DRAWING



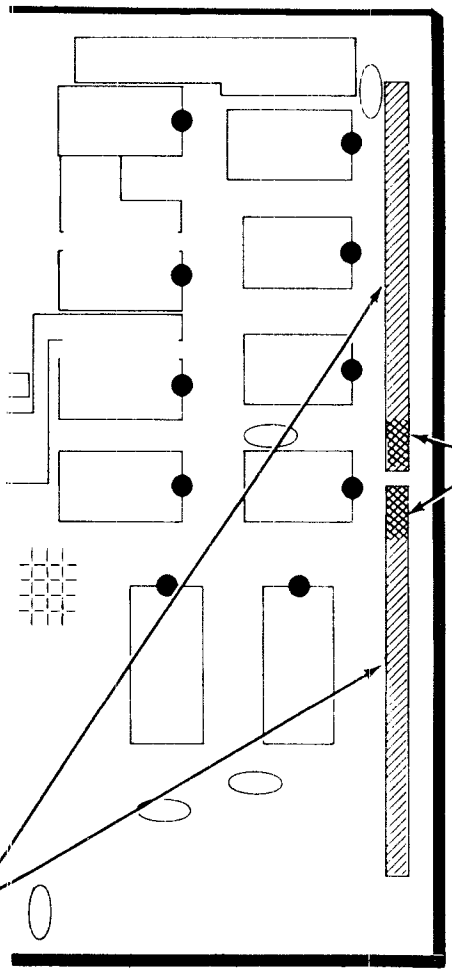
The steps performed in this Pictorial are in this area of the circuit board.

START

NOTE: When you install a 25-pin connector:

- Refer to Detail 1-8A, part A, and position the socket on a hard flat surface with the pins along the surface as shown.
- Refer to part B of the Detail and roll the socket forward and bend the pins up approximately 15°.
- Refer to part C of the Detail and position the connector with its notches against the edge of the circuit board and the pins over the circuit board holes.
- Refer to part D of the Detail and roll the connector forward and insert the pins into the circuit board holes. Make sure the connector is tight against the board and then solder two pins at each end of the connector to the foils. Check the alignment and then solder the remaining pins to the foils.

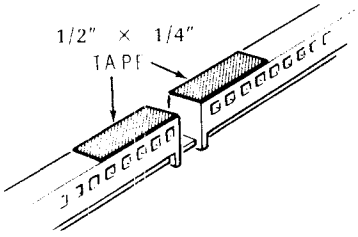
( ) S101: Install two 25-pin connectors.



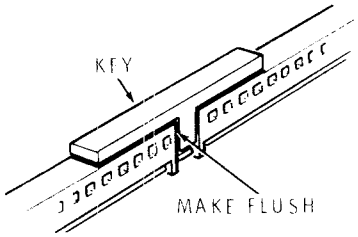
CONTINUE

( ) Install the connector key as follows:

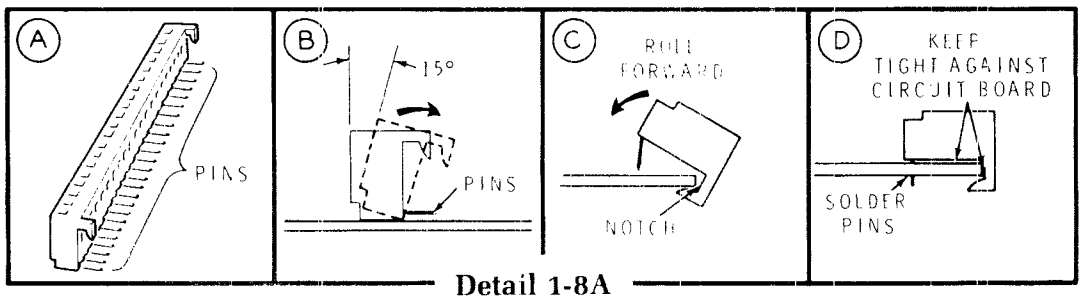
- Cut two 1/2" × 1/4" lengths of tape, remove the protective covering from one side of each length, and apply the tape to the connectors at the locations shown.



- Remove the other protective covering from the lengths of tape and press the connector key down onto the tape. Be sure the key is flush with the edge of the connector as shown.



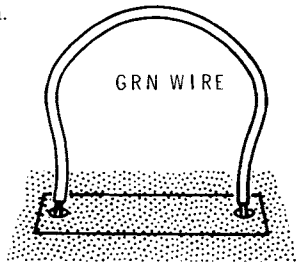
PICTORIAL 1-8



Detail 1-8A

START

NOTE: When you are instructed to prepare a jumper wire in the following steps, cut a green wire to the indicated length and remove 1/4" of insulation from each end. Form a loop in the wire and insert the wire ends through the indicated circuit board holes. **Do not bend the bare wire ends over since you will remove some of the jumpers later and the foil may be torn upon removal.** Solder the wire ends to the foil. The jumpers are made long for easy installation and removal. After you have installed all of the jumpers the circuit board will be in a "test" configuration.



( ) Prepare six 1" and two 1-1/2" jumper wires.

Connect the jumper wires to the circuit board as follows:

( ) 1" jumper wire between A1 and A2.

( ) 1" jumper wire between A1 and A2.

( ) 1-1/2" jumper wire between B1 and B2.

( ) 1" jumper wire between C1 and C2.

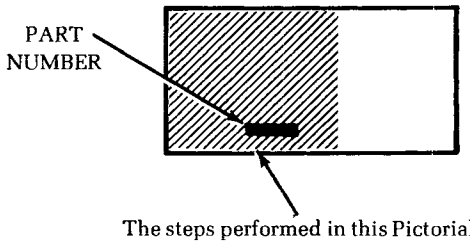
( ) 1" jumper wire between E1 and E2.

( ) 1-1/2" jumper wire between B1 and B2.

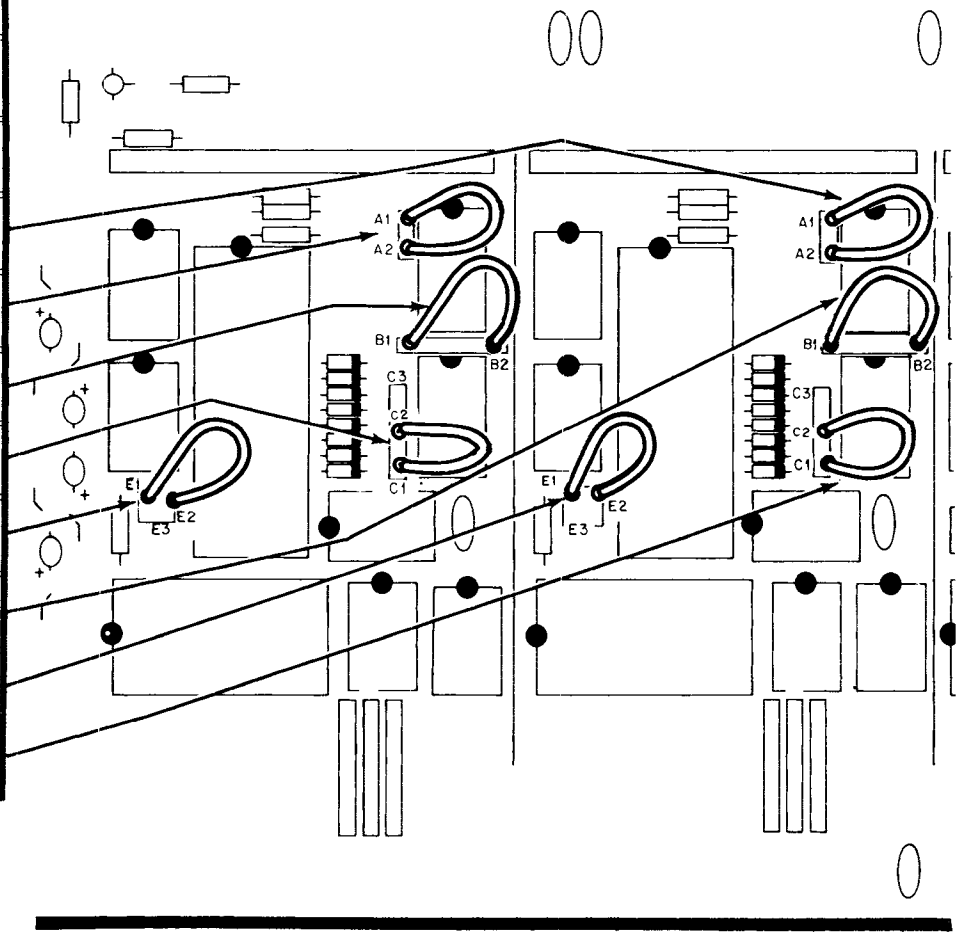
( ) 1" jumper wire between E1 and E2.

( ) 1" jumper wire between C1 and C2.

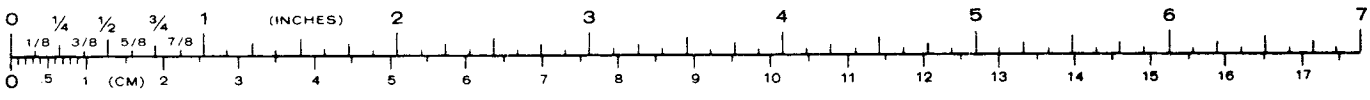
IDENTIFICATION DRAWING



The steps performed in this Pictorial are in this area of the circuit board.



PICTORIAL 1-9



START

( ) Prepare twelve 1" and one 2" jumper wire.

Install the following jumper wires in the same manner as before.

( ) 1" jumper wire between 70 and the hole directly across from 70.

( ) 1" jumper wire between 0 and the hole directly across from 0.

( ) 1" jumper wire between hole 4 and the hole directly across from 4.

( ) 1" jumper wire between hole 70 and the hole directly across from 70.

( ) 1" jumper wire between A1 and A2

( ) 1" jumper wire between hole 70 and the hole directly across from 70.

( ) 2" jumper wire between B1 and B2.

( ) 1" jumper wire between hole E1 and E2.

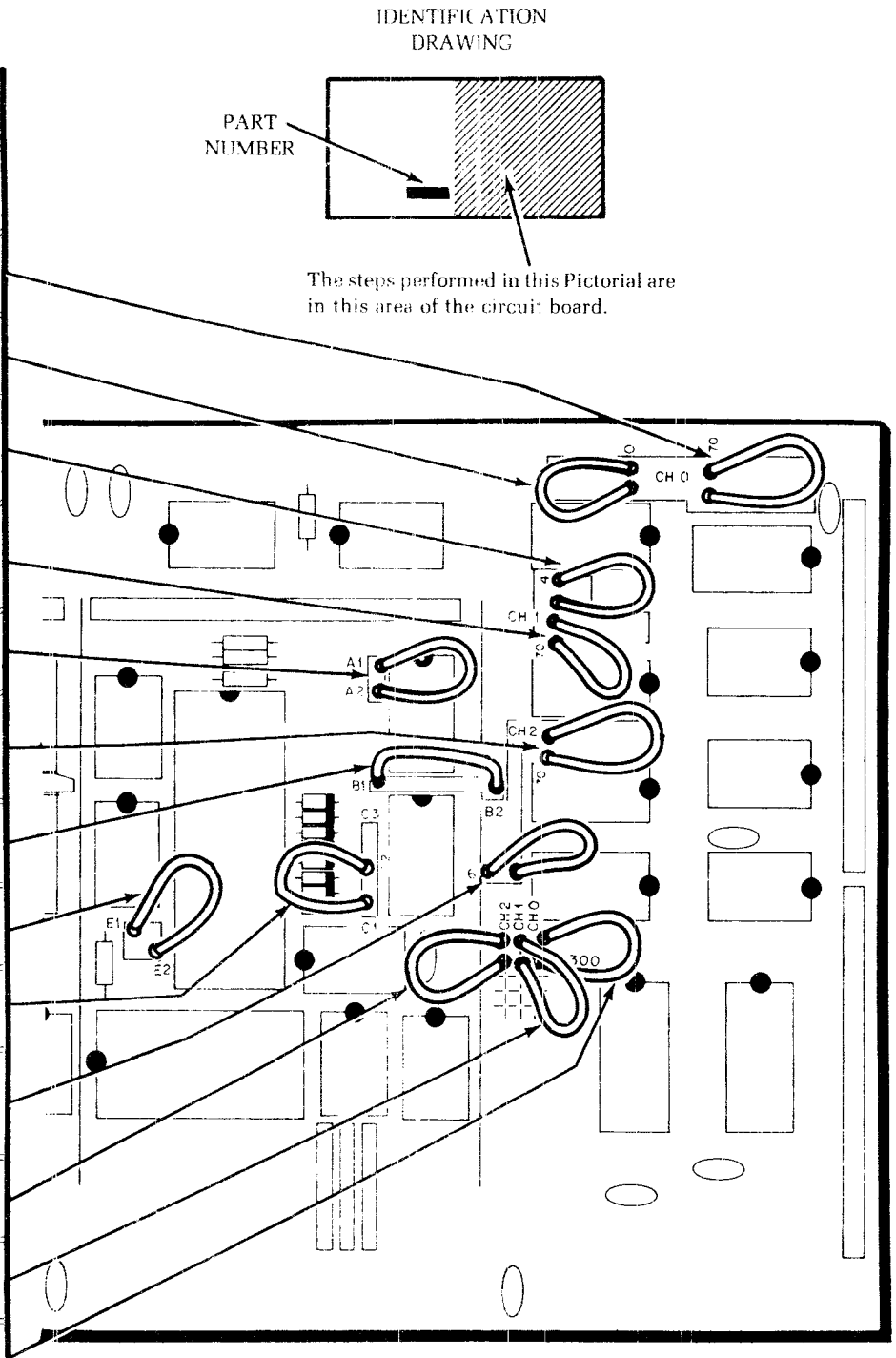
( ) 1" jumper wire between C1 and C2.

( ) 1" jumper wire between hole 6 and the hole directly across from 6.

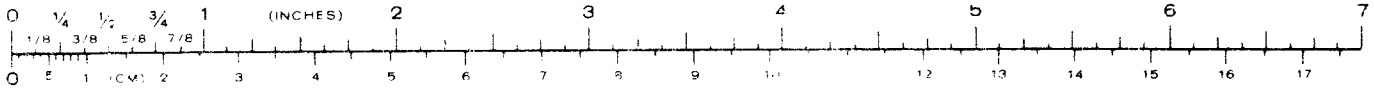
( ) 1" jumper wire between CH2 and 300.

( ) 1" jumper wire between CH1 and 300.

( ) 1" jumper wire between CH0 and 300.

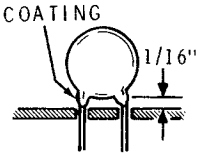


PICTORIAL 1-10



START

NOTE: A coating on ceramic capacitor leads can extend through the circuit board and make soldering difficult. Therefore, always space ceramic capacitors 1/16" off the circuit board.

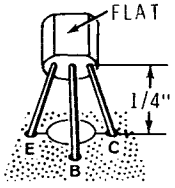


( ) C104: .1 μF ceramic.

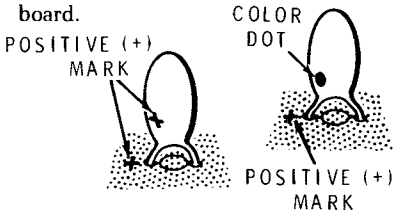
( ) C105: .1 μF ceramic.

( ) Solder the leads to the foil and cut off the excess lead lengths.

( ) Q131: 2N3904 transistor (#417-875). Position the transistor over the outline on the circuit board. Then insert the transistor leads into their correct E, B, and C holes. Solder the leads to the foil and cut off the excess lead lengths as you install each transistor.



NOTE: When you install tantalum capacitors, be sure to position the plus (+) or color dot marked lead in the plus marked hole in the circuit board.



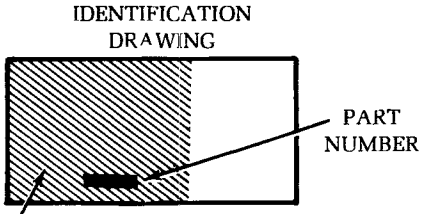
Install tantalum capacitors at the following locations:

( ) C101.
( ) C102.
( ) C111.
( ) C112.

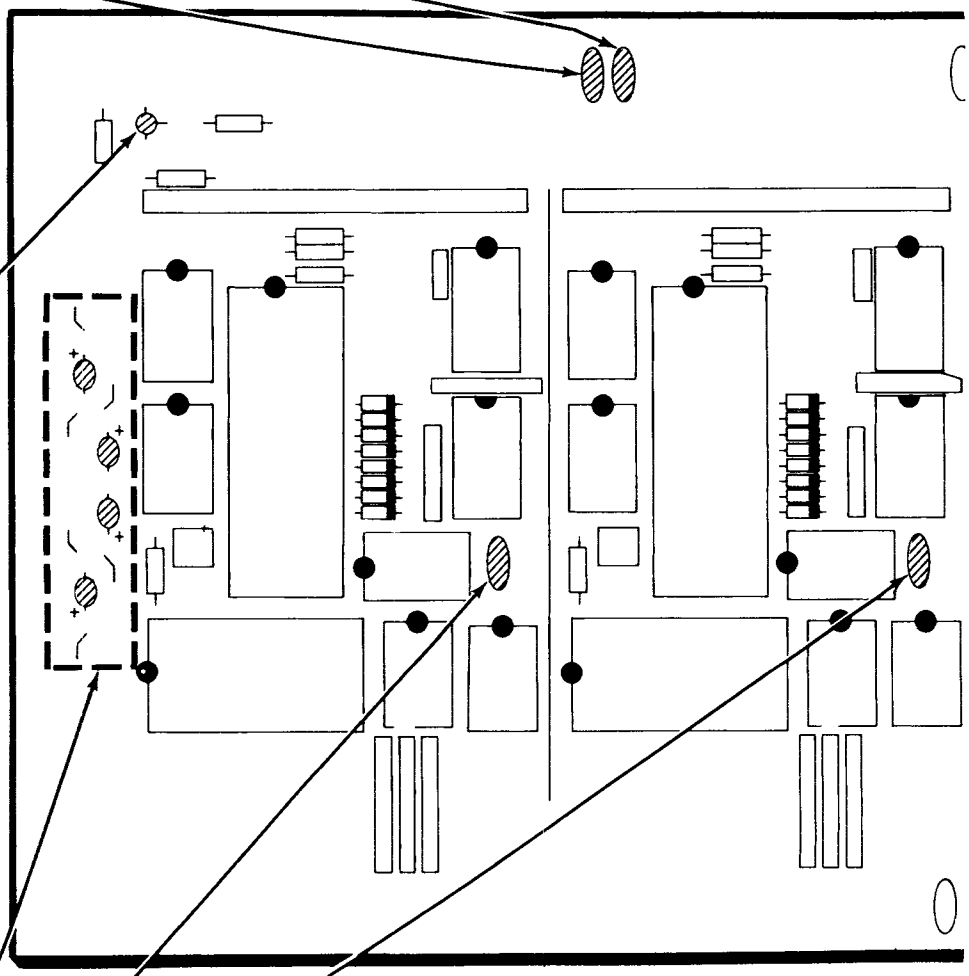
( ) C103: .1 μF ceramic.

( ) C106: .1 μF ceramic.

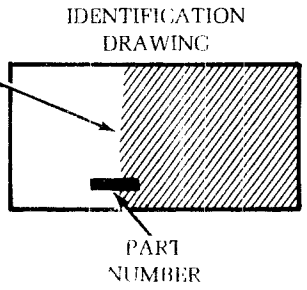
( ) Solder the leads to the foil and cut off the excess lead lengths.



The steps performed in this Pictorial are in this area of the circuit board.



PICTORIAL 1-11



START

( ) C106: .1 μF ceramic.

( ) C107: .1 μF ceramic.

( ) C109: .1 μF ceramic.

( ) C117: .1 μF ceramic.

( ) C114: .1 μF ceramic.

( ) C118: .1 μF ceramic.

( ) C116: .1 μF ceramic.

( ) C115: .1 μF ceramic.

( ) C113: .1 μF ceramic.

CIRCUIT BOARD CHECKOUT

Carefully inspect the circuit board for the following conditions.

( ) Unsoldered connections.

( ) Poor solder connections.

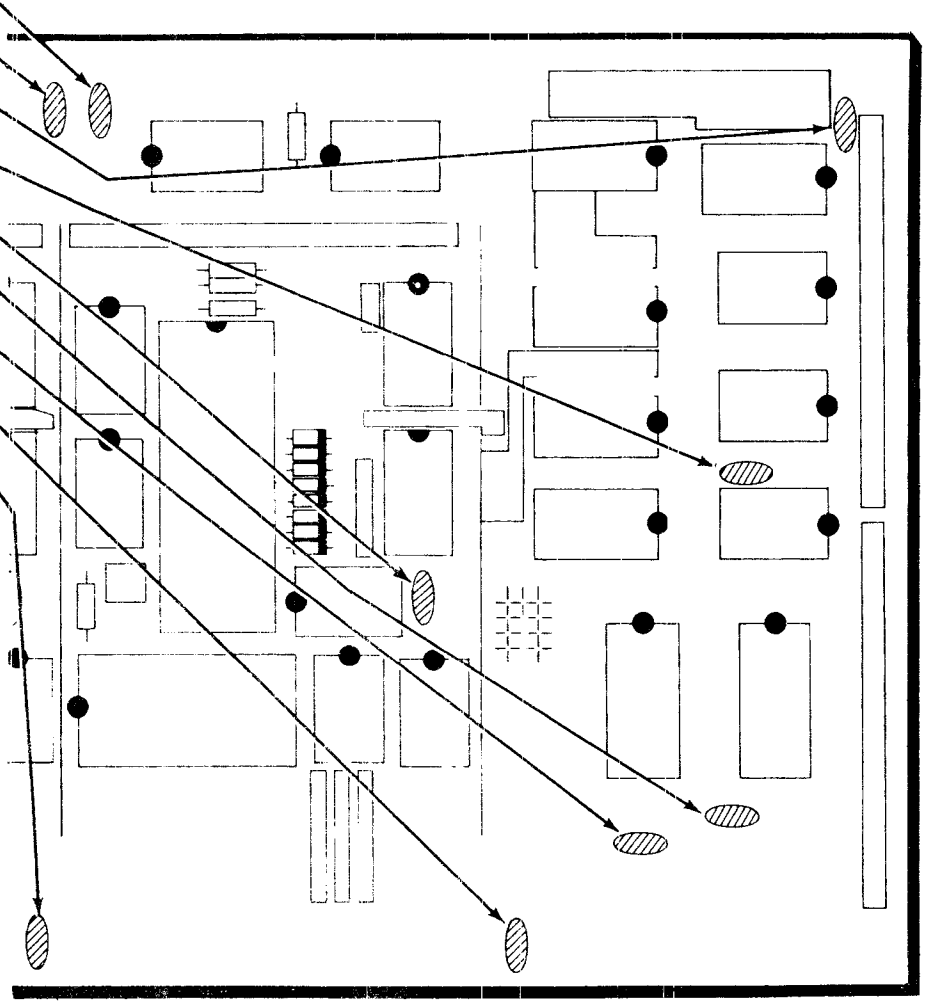
( ) Solder bridges between foil patterns.

( ) Protruding leads which could touch together.

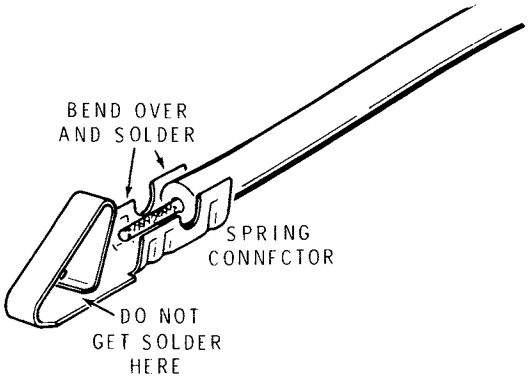
( ) Transistors and IC's for the proper **type** and **installation**.

( ) Tantalum capacitors for the correct position of the positive (+) end.

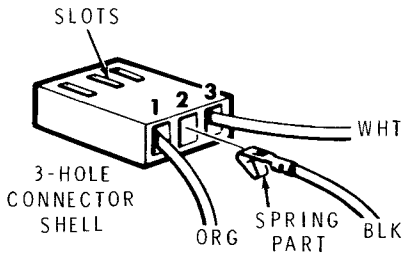
( ) Diodes for the correct position of the banded end.



PICTORIAL 1-12



Detail 1-13A



Detail 1-13B

Refer to Pictorial 1-13 (Illustration Booklet, Page 2) for the following steps.

( ) Prepare the following lengths of stranded wire. Remove 1/8" of insulation from one end of each wire and 1/4" from the other end.

(2) 3" orange
(2) 3" black
(2) 3" white

NOTE: If it is ever necessary to remove a spring connector from a connector shell, press a small screwdriver into the slot in the shell while you pull on the wire.

( ) Refer to Detail 1-13A and install a spring connector onto the 1/8" end of an orange wire.

( ) In the same manner, install spring connectors onto the 1/8" end of the other prepared wires.

( ) Refer to Detail 1-13B and position a 3-hole connector shell as shown with the slotted side up. Then insert the spring connector on one of the orange wires into hole 1. Be sure to position the spring part of the connector away from the slotted side of the connector shell.

( ) Insert the spring connector on one of the black wires into hole 2.

( ) Insert the spring connector on one of the white wires into hole 3.

( ) Gently pull on each wire to make sure it is locked into the connector shell. Then set this connector shell aside temporarily.

( ) Locate the other 3-hole connector shell and install the remaining three wires in the same manner.

( ) Solder the orange wire coming from 3-hole connector shell A to hole +8 V on the circuit board. NOTE: There are two sets of holes in the circuit board with identical markings. Use the hole that is near IC145.

( ) Solder the white wire coming from 3-hole connector shell A to hole +5 V. Use the hole that is near IC145.

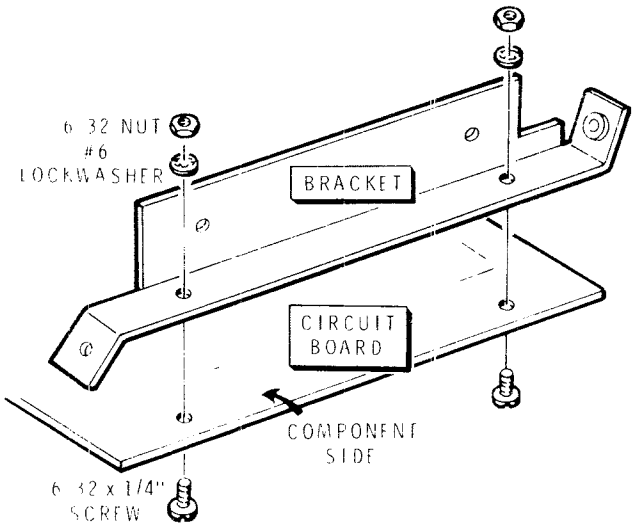
( ) Solder the black wire coming from 3-hole connector shell A to the indicated hole marked GND.

Solder the wires coming from 3-hole connector shell B to the circuit board holes near IC144 as follows:

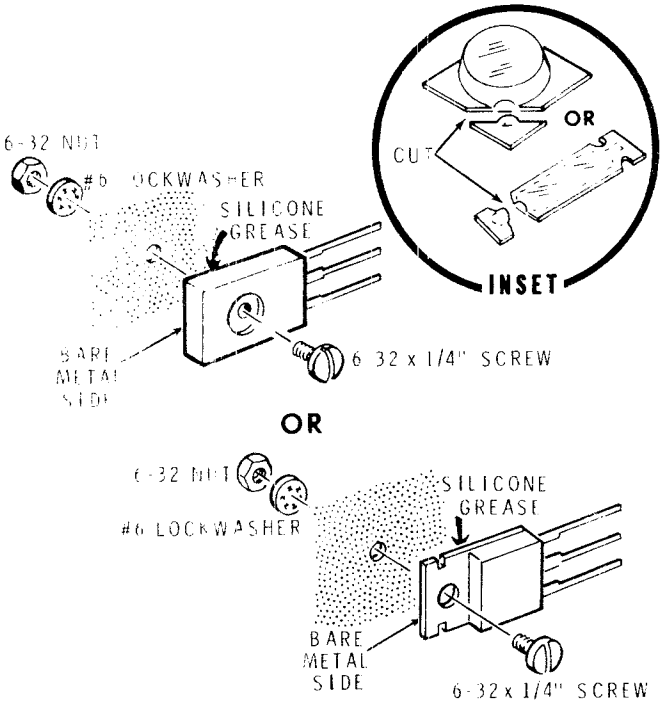
( ) Orange wire to +8 V.

( ) White wire to +5 V.

( ) Black wire to GND.



Detail 1-13C



Detail 1-13D

Refer to Pictorial 1-13 (Illustration Booklet, Page 2) for the following steps.

( ) Refer to Detail 1-13C and mount the bracket to the printed side of the circuit board with two 6-32 × 1/4" screws, two #6 lockwashers, and two 6-32 nuts.

( ) Refer to the inset drawing of Detail 1-13D and open the silicone grease pod. Apply a liberal amount of grease to the bare metal side of both UA7805 integrated circuits (#442-54).

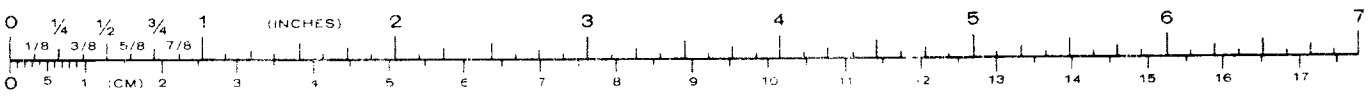
( ) IC144: Refer to Detail 1-13D and mount one of the UA7805 integrated circuits (#442-54) to the bracket at IC144. Use a 6-32 × 1/4" screw, a #6 lockwasher, and a 6-32 nut. Position the bare metal side of the IC toward the bracket.

( ) IC145: In the same manner, mount the other IC to the bracket at IC145.

( ) Push connector shell A onto the leads of IC144 as shown in the inset drawing. Dress the leads over the bracket as shown.

( ) Push connector shell B onto the leads of IC145. Dress the leads over the bracket as shown.

This completes the assembly of your Parallel I/O circuit board. Proceed to "Regulator Test."



REGULATOR TEST

Refer to Pictorial 1-14 (Illustration Booklet, Page 2) for the following steps.

( ) Make sure the POWER switch (on the rear of your Computer) is in the OFF position.

( ) Unplug the Computer's line cord.

( ) If not already done, remove the two screws that hold the top cover on the Computer. Then remove the cover.

( ) Remove the tie bracket from the Computer if not already done.

( ) Position the Parallel I/O circuit board inside the chassis as shown. Then carefully push the connectors on the edge of the circuit board onto an unused plug on the mother circuit board near the rear of the Computer. Do not use plug P-10. It is reserved for other applications.

( ) Plug the line cord into the proper AC outlet.

NOTE: If you do not obtain the proper results in the following steps, push the POWER switch to OFF and refer to the "Possible Cause" chart which follows each check.

( ) Push the POWER switch to ON. The PWR LED and RUN LED on the front panel should light.

PROBLEM	POSSIBLE CAUSE
PWR LED does not light. Fuse F1 is open.	A. Solder bridge on parallel circuit board.

NOTE: The following checks require a VTVM or VOM. If you do not have one available, remove the parallel I/O circuit board from the Computer and carefully inspect the circuit board for solder bridges. Then proceed to "Integrated Circuit Installation."

( ) Connect the common lead of your meter to the chassis.

( ) Set your meter to measure +15 volts DC.

( ) Touch the probe of your meter to the indicated foil at TP1 (+8V, orange wire). The meter should indicate between 7.5 and 11.5 volts.

( ) Touch the probe of your meter to the indicated foil at TP2 (+8V, other orange wire). The meter should indicate between 7.5 and 11.5 volts.

PROBLEM	POSSIBLE CAUSE
TP1 and TP2 do not indicate 8 volts.	A. Solder bridge on parallel circuit board. B. Wiring error on parallel circuit board at IC144 and IC145. C. IC's 144 and 145 are defective.

( ) Touch the meter probe to the indicated foil at TP3 (+5V, white wire). The meter should indicate 5 volts ±.25 volts).

PROBLEM	POSSIBLE CAUSE
TP3 measures below 2 volts.	A. Solder bridge on parallel circuit board. B. Wiring error on parallel circuit board at IC144.
TP3 measures 0 volts.	A. IC144 is defective. B. Capacitor C102 is defective.

( ) Touch the meter probe to the indicated foil at TP4 (+5V, other white wire). The meter should indicate 5 volts (±.25 volts).

PROBLEM	POSSIBLE CAUSE
TP4 measures below 2 volts.	A. Solder bridge on parallel circuit board. B. Wiring error on parallel circuit board at IC145.
TP4 measures 0 volts.	A. IC145 is defective. B. Capacitor C112 is defective.

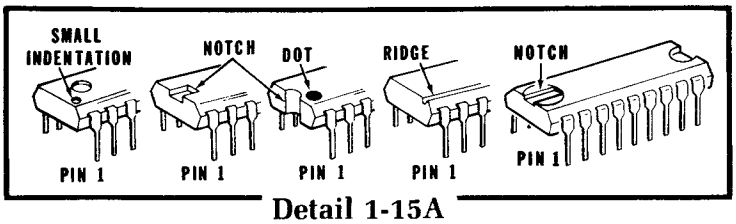
( ) Push the POWER switch to OFF and unplug the line cord.

( ) Disconnect the meter from the chassis and the parallel I/O circuit board.

( ) Remove the parallel I/O circuit board from the Computer.

This completes the "Regulator Test." Proceed to "Integrated Circuit Installation."

INTEGRATED CIRCUIT INSTALLATION

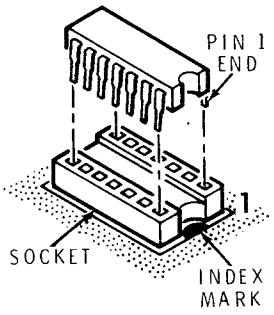


Detail 1-15A

START

In the following steps, install IC's (integrated circuits) in the designated sockets. Be careful to match the pin 1 end of each IC to the index mark on the circuit board. See Detail 1-15A on this page.

Before you apply downward pressure to an IC, make sure each IC pin is centered in its proper socket hole. Handle IC's with care, as their pins bend very easily.



( ) IC101: 7486 IC (#443-698).

( ) IC102: 7486 IC (#443-698).

( ) IC107: 74120 IC (#443-841).

( ) IC108: 74120 IC (#443-841).

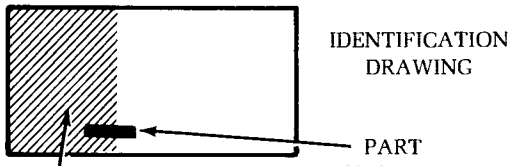
( ) IC105: 7402 IC (#443-46).

( ) IC106: 7403 IC (#443-54).

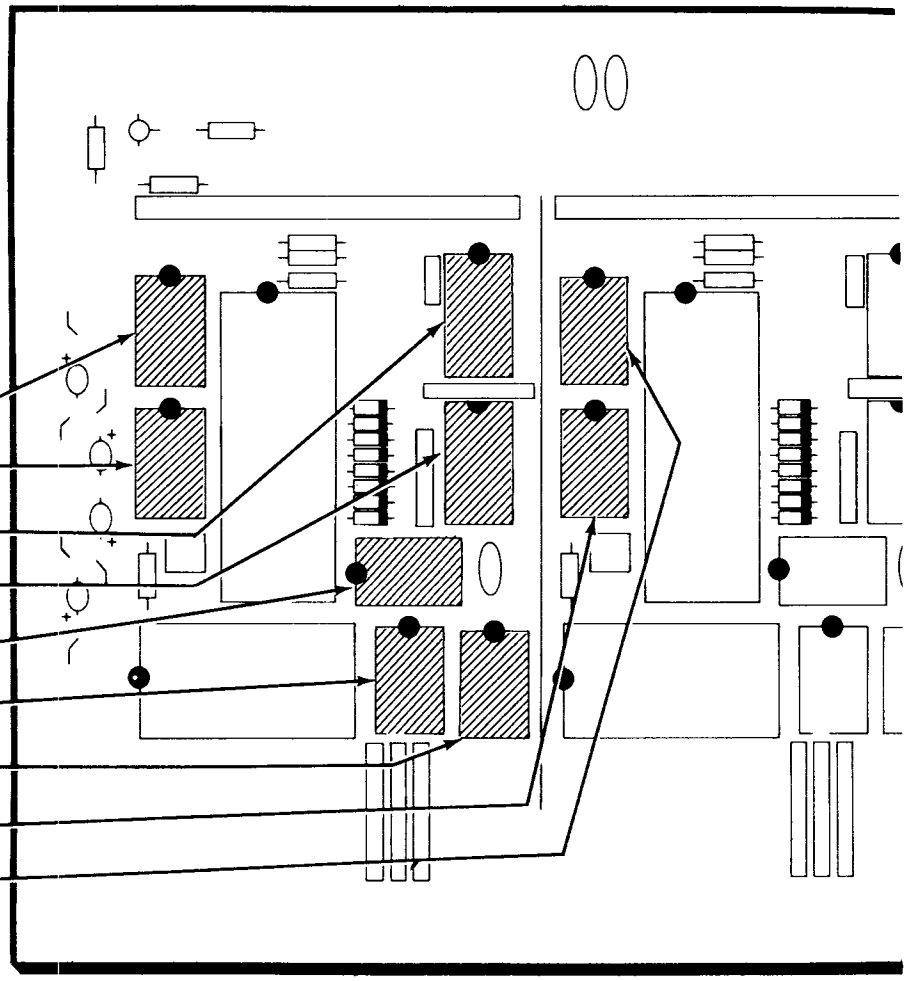
( ) IC109: 74LS04 IC (#443-755).

( ) IC112: 7486 IC (#443-698).

( ) IC111: 7486 IC (#443-698).

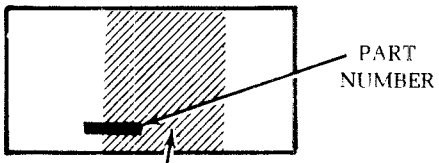


The steps performed in this Pictorial are in this area of the circuit board.



PICTORIAL 1-15

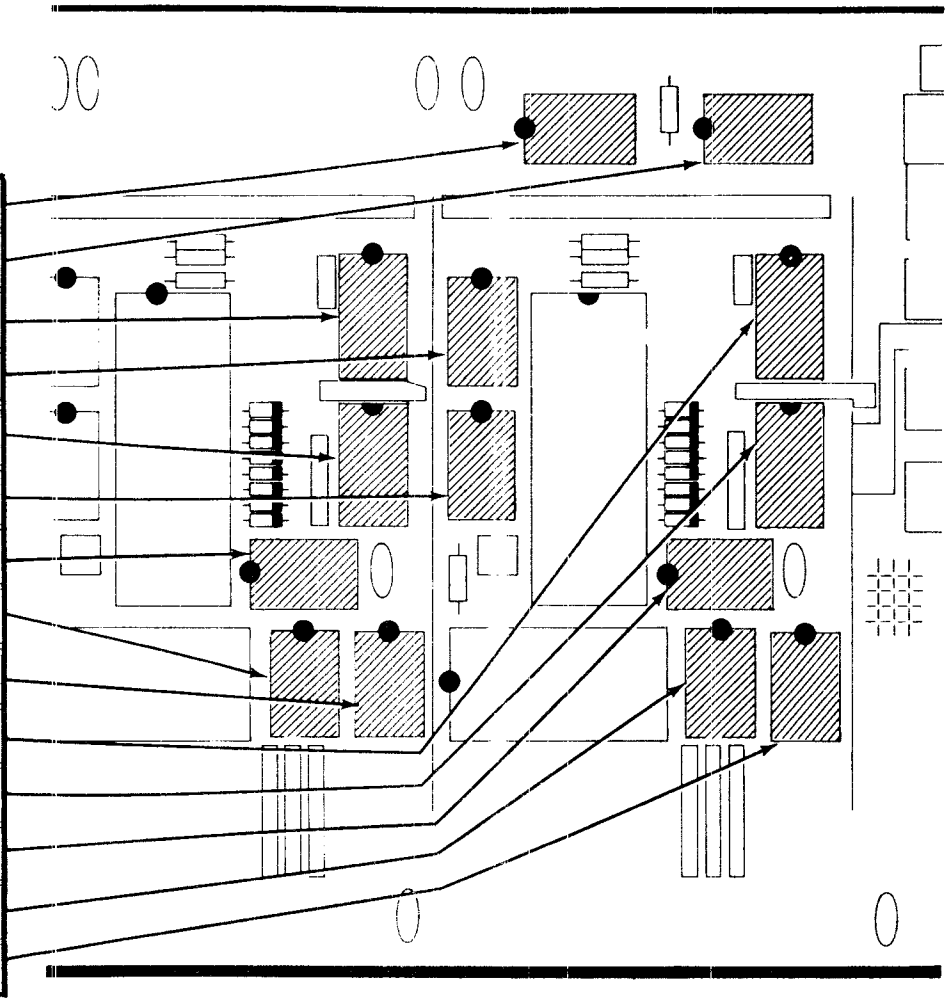
IDENTIFICATION
DRAWING



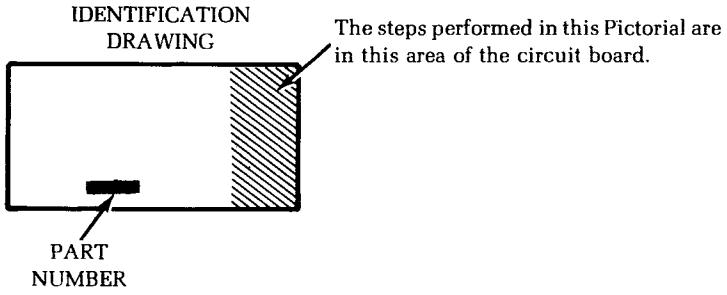
The steps performed in this Pictorial are in this area of the circuit board.

START

- ( ) IC131: 74LS290 (#443-731).
- ( ) IC132: 7474 IC (#443-6).
- ( ) IC117: 74120 IC (#443-841).
- ( ) IC121: 7486 IC (#443-698).
- ( ) IC118: 74120 IC (#443-841).
- ( ) IC122: 7486 IC (#443-698).
- ( ) IC115: 7402 IC (#443-46).
- ( ) IC116: 7403 IC (#443-54).
- ( ) IC119: 74LS04 IC (#443-755).
- ( ) IC127: 74120 IC (#443-841).
- ( ) IC128: 74120 IC (#443-841).
- ( ) IC125: 7402 IC (#443-46).
- ( ) IC126: 7403 IC (#443-54).
- ( ) IC129: 74LS04 IC (#443-755).



PICTORIAL 1-16



START

( ) IC133: 74LS139 IC (#443-822).

( ) IC134: 7442 IC (#433-53).

( ) IC135: 7442 IC (#443-53).

( ) IC136: 74LS139 IC (#443-822).

NOTE: Do not confuse the 74**LS**240 IC in the following step, with the 74**S**240 IC.

( ) IC137: 74LS240 IC (#443-754).

CONTINUE

( ) IC138: 7442 IC (#443-53).

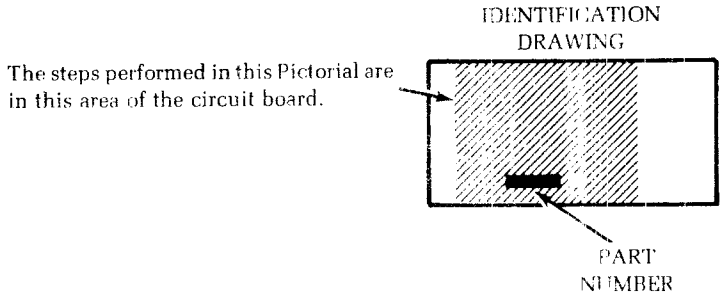
( ) IC139: 74LS04 IC (#443-755).

( ) IC141: 74LS04 IC (#443-755).

( ) IC142: 7410 IC (#443-12).

( ) IC143: 74LS240 IC (#443-754).

PICTORIAL 1-17



START

CAUTION: The following integrated circuits can be damaged by the static electricity in your body. It is VERY IMPORTANT that you handle these IC's carefully.

Once you remove an IC from its protective foam, do not set the IC down until it is installed in the circuit board. As long as you hold the IC, there is no danger of static electricity. If it becomes necessary to set the IC down, put it back in the protective foam.

( ) IC124: 6402 IC (#443-761).

( ) IC114: 6402 IC (#443-761).

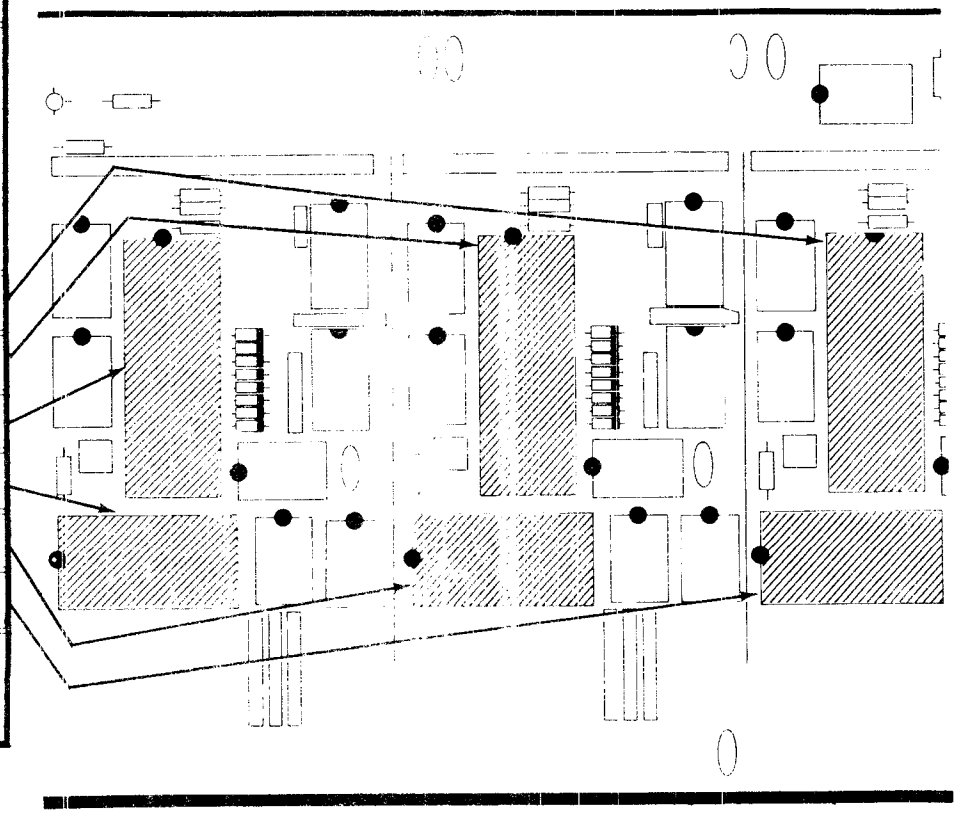
( ) IC104: 6402 IC (#443-761).

( ) IC103: 8251 IC (#443-776).

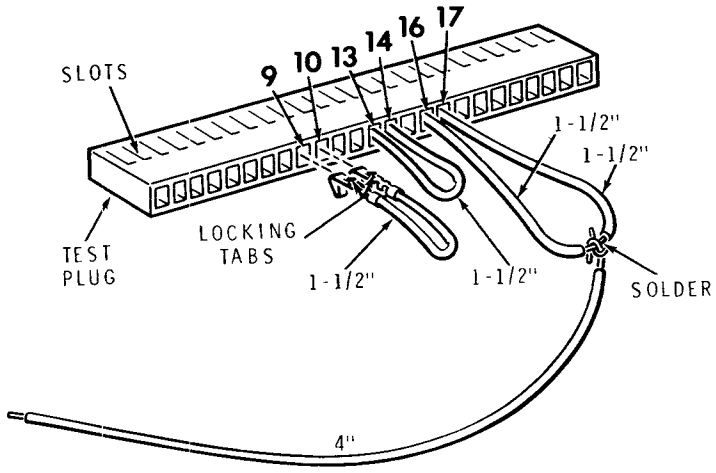
( ) IC113: 8251 IC (#443-776).

( ) IC123: 8251 IC (#443-776).

This completes the "Integrated Circuit Installation." Proceed to "Cable Preparation."



INSTALLATION AND TESTS



PICTORIAL 2-1

NOTE: After you install your Parallel I/O Card in the Computer, you will test one channel at a time in the Continuous Mode. In the following section, you will construct a special test plug from one of the unused I/O plugs and connect it to the channel under test. During construction, jumpers have been installed so that:

Channel ϕ will respond to I/O 370/371.

Channel 1 will respond to I/O 374/375.

Channel 2 will respond to I/O 376/377.

I/O cards or any other devices you may have in the system which respond to 370, 371, 374, 375, 376, and 377, must be disabled at this time. You will need only the CPU (Central Processing Unit) and 4k of memory to conduct these tests. After you complete the tests, you will have verified all bits of all data ports and partially tested the handshake lines.

TEST PLUG ASSEMBLY

Refer to Pictorial 2-1 for the following steps.

( ) Prepare the following green wires:

(4) 1-1/2"
(1) 4"

( ) Crimp and solder a spring connector on each end of two 1-1/2" green wires.

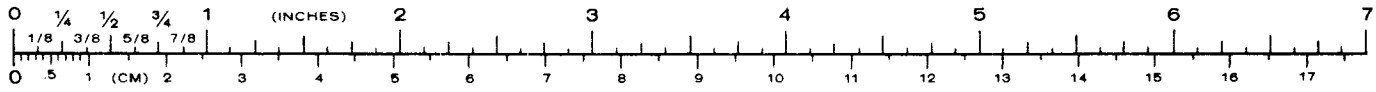
( ) Crimp and solder a spring connector on one end only of the two remaining 1-1/2" green wires.

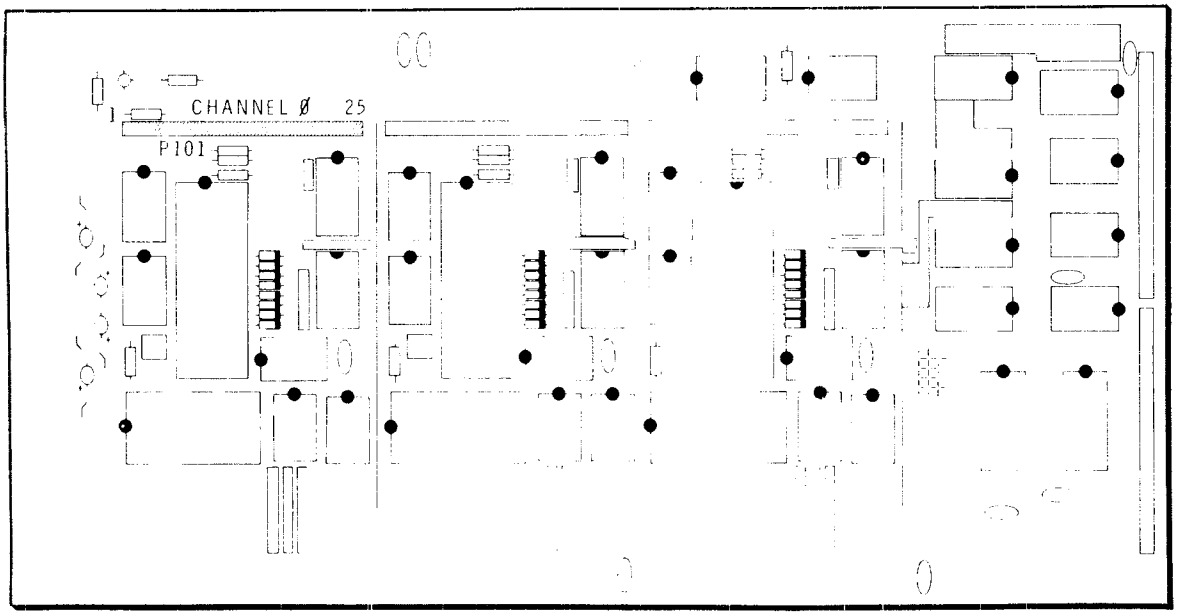
( ) Insert a 1-1/2" green wire with a spring connector on each end into connector plug holes 9 and 10. Make sure the locking tabs on each pin faces up as shown.

( ) Insert a spring connector on each end of the other green wire into test plug holes 13 and 14.

( ) Insert a spring connector on the end of the remaining two green wires into test plug holes 16 and 17.

( ) Form a hook in the free end of the wires coming from pins 16 and 17 of the test plug and at one end of the 4" green wire. Hook the three wires together and close the hooks. Then solder the connection.





PICTORIAL 2-2

CHANNEL ϕ TEST

Data Output

NOTE: For this test, the 8 output lines will be turned on and off. You will be able to observe these pulses with an oscilloscope or logic probe.

Equipment needed:

Logic probe
OR
10 MHz oscilloscope

Refer to Pictorial 2-2 for the following steps.

( ) Install the test plug at P-101 (Channel ϕ). Make sure you position the slots facing up.

( ) Turn on the Computer.

NOTE: Perform all of the following tests. If a problem occurs during a test, proceed with the next test until you complete all nine. Then refer to "Trouble shooting charts" to help you locate the cause of any problems which may have occurred. If a failure occurs, note the failure in the appropriate channel box in Chart 1.

( ) Press the RST/ϕ and ϕ keys simultaneously.

( ) Start at memory location 040 200 and enter the following program: (Refer to the Computer Operation Manual if you are not familiar with the use of the control panel.)

MEMORY ADDRESS		INSTRUCTION BYTE(S)
040	200	076
040	201	005
040	202	323
040	203	371
040	204	323
040	205	370
040	206	057
040	207	303
040	210	204
040	211	040

( ) Set the PC Register to 040 200.

( ) Press the GO key.

( ) Use the logic probe and observe the pulses on each pin 1 through 8 of test plug P-101. Touch the probe tip to the pins through the slots in the plug. Observe the presence of the pulses.

NOTE: Channel ϕ will be in the proper configuration to operate the H-10 Paper Tape System. The other ports may be left as they are until they are required. Refer to the "Operation" section in the Manual for their use.

( ) Set the PC Register to 040 200.

( ) Press the GO key.

( ) Use the logic probe and observe the pulses at each pin 1 through 8 of the test plug.

Data In

( ) Press the RST/ϕ and ϕ keys simultaneously.

( ) Start at memory location 040 100 and enter the following test program:

MEMORY ADDRESS		INSTRUCTION BYTES
040	100	076
040	101	116
040	102	323
040	103	375
040	104	076
040	105	047
040	106	323
040	107	375
040	110	333
040	111	374
040	112	303
040	113	110
040	114	040

( ) Set the PC Register to 040 100.

( ) Select the AF Register.

( ) Press the GO key.

( ) Use the long test wire coming from the test plug and touch it to input pins 25 through 18.

The following numbers should be displayed at Register A when you touch the indicated pins:

PIN#	NUMBER DISPLAYED
None	377
25	376
24	375
23	373
22	367
21	357
20	337
19	277
18	177

Device Control

( ) Press the RST/ϕ and ϕ keys simultaneously.

( ) Perform the following steps:

Press MEM
Enter 116 375
Press OUT
Press MEM
Enter 000 375
Press OUT
Press IN

( ) Read 205 375
Press MEM
Enter 040 375
Press OUT
Press IN

( ) Read 005 375

This completes "Channel 1 Test." Proceed to "Channel 2 Test."

CHANNEL 2 TEST

Data Output

Refer to Pictorial 2-4 for the following steps.

( ) Remove the test plug from P-111 and install it at P-121.

( ) Press RST/ϕ and ϕ keys simultaneously.

( ) Start at memory location 040 200 and enter the following test program:

MEMORY ADDRESS		INSTRUCTION BYTE(S)
040	200	076
040	201	116
040	202	323
040	203	377
040	204	076
040	205	005
040	206	323
040	207	377
040	210	323
040	211	376
040	212	057
040	213	303
040	214	210
040	215	040

( ) Set the PC Register to 040 200

( ) Press the GO key.

( ) Use the logic probe and observe the pulses at pins 1 through 8 on P-121.

Data Input

( ) Press the RST/ϕ and ϕ keys simultaneously.

( ) Start at memory location 040 100 and enter the following test program:

MEMORY ADDRESS		INSTRUCTION BYTES
040	100	076
040	101	116
040	102	323
040	103	377
040	104	076
040	105	047
040	106	323
040	107	377
040	110	333
040	111	376
040	112	303
040	113	110
040	114	040

( ) Set the PC Register to 040 100.

( ) Select the AF Register.

( ) Press the GO key.

( ) Use the long test wire coming from the test plug and touch it to input pins 25 through 18. The following numbers should be displayed at Register A when you touch the indicated pins:

PIN#	NUMBER DISPLAYED
None	377
25	376
24	375
23	373
22	367
21	357
20	337
19	277
18	177

Device Control

( ) Press the RST/ϕ and ϕ keys simultaneously.

( ) Perform the following steps:

Press MEM
Enter 116 377
Press OUT
Press MEM
Enter 000 377
Press OUT
Press IN
( ) Read 205 377
Press MEM
Enter 040 377
Press OUT
Press IN
( ) Read 005 377

( ) Remove the test plug from P-121.

NOTE: The A1-A2, B1-B2 jumpers must be removed from channel ϕ to operate the H10. Channel ϕ will then be in the proper configuration to operate the H10 Paper Tape System. The other ports may be left as they are until they are required. Refer to the "Operation" section in the Manual for their use.

You may want to save the plug to build another cable at a later time. Perform the following steps only if you intend to connect the H8 to the H10.

Refer to Pictorial 2-5 (Illustration Booklet, Page 3) for the following steps.

( ) Install the Parallel I/O Card into the unused plug near the rear of the Computer as before. DO NOT install the card at P-10. It is reserved for other applications.

( ) Loosen the two screws at clamp AG, open the clamp, and route the indicated end of the interconnect cable through the clamp as shown.

( ) Plug the end of the cable in the Computer into the Parallel I/O Card as shown. Route the cable as shown, close the clamp, and retighten the screws.

( ) Install a 6-32 × 1/4" screw through the bottom of the Computer chassis to hold the card in place.

This completes the "Installation and Tests."

OPERATION

NOTE: The following description applies to any of the three channels on the Parallel I/O Card.

The Parallel I/O Card provides 3 channels of INPUT/OUTPUT capability with complete Handshake facilities. The unique characteristic of this card is that it is program compatible with the Serial I/O and Cassette Interface Card. Therefore, you can use Parallel and Serial ports interchangeably without software modifications. This capability is achieved by connecting a programmable UART (Universal Asynchronous Receiver Transmitter) and a non-programmable UART back-to-back. The CPU (Central Processing Unit) bus then sees a programmable port that programs in the same manner as the Serial I/O and Cassette Interface Card and the peripheral device sees a latched 8-bit output port and a latched 8-bit input port. Pictorial 3-1 shows a Block Diagram for a Parallel-Serial-Parallel Input/Output Port.

ADDRESS SECTION

Each section is individually selected to any I/O address pair between 000/001 and 376/377. Three jumpers are required; one for each digit of the address. Refer to Pictorial 3-2 (Illustration Booklet, Page 4) for a description of these jumpers. Addresses 320-377 are reserved for Heath Systems.

DATA PORTS

A separate I/O plug is provided for each channel. The plug number for each channel is as follows:

Channel ϕ — P101
Channel 1 — P111
Channel 2 — P121

The output data associated with these plugs appears on pins 1 through 8 as follows:

PIN #	DATA BIT
1	D0 (LSB) (Least Significant Bit)
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	Ground

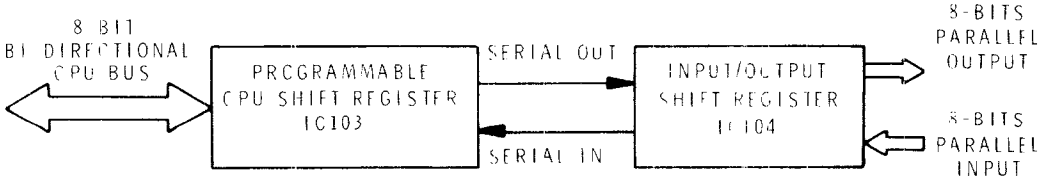
The output polarity is selectable with the E1, E2, and E3 jumper set. These jumpers can be connected as follows: See Pictorial 3-2.

E1-E2 Non-inverted
E2-E3 Inverted

DATA PORTS (INPUT)

The Data Input Ports are associated with pins 18 through 25 as follows:

PIN#	DATA BIT
17	Ground
18	D7
19	D6
20	D5
21	D4
22	D3
23	D2
24	D1
25	D0 (LSB)



CHANNEL Ø BLOCK DIAGRAM
PARALLEL - SERIAL - PARALLEL
INPUT/OUTPUT PORT

PICTORIAL 3-1

Portions of this Section are reprinted by permission from Intel Corporation.

PROGRAM CONSIDERATIONS

Each channel of the Parallel I/O Interface must be "Initialed On Program" before data can be transferred in or out. For most applications, the software supplied by Heath Company will automatically take care of this. For specialized applications, you will need to know how to program the I/O Interface. For a more detailed explanation, study the 8251 Basic Functional Description on Page 55 of this Manual.

Each channel occupies two consecutive I/O addresses. (100 and 101 for example.) The lower address is the data port.

1. Data in the CPU accumulator will be transferred to the output terminals when a 323 (output) instruction is executed.

2. Data present at the input terminals will be transferred to the CPU accumulator when a 333 (input) instruction is executed.

Before data can be transferred, the I/O channel must be initialized. This requires that two bytes, the Mode Word and the Command Word be sent (323) to the higher address.

1. The first, or Mode byte, will always be 116 for the H8-2. Once set, this byte cannot be changed unless cancelled by a system (hardware) or software (command word) reset.

2. The second byte, sent to this same address, is the command word. The command word may be reprogrammed at any time (provided that the mode word has not been reset).

   D_0 Data Out — 1=Enable, 0=Disable.

   D_1 Interrupt — 1=Enable, 0=Disable.

   D_2 Data In — 1=Enable, 0=Disable.

   D_3 0

   D_4 0

   D_5 Device Control — 1 = output pins 12 and 14 set to logic low.
   0 = Logic high.

   D_6 Internal Reset — 1 returns the channel to mode instruction.

See *Note 1 for three command examples.

3. The status of the channel may be tested by reading (I/O input) the high channel address. (101 for example).

The following three bits will be of interest.

D_0 — 1 indicates that the channel is ready to accept a data byte from the CPU.

D_1 — 1 indicates that the channel has data for the CPU.

D_7 — 1 indicates that pin 13 of the I/O plug (Device Ready) is at logic low.

The following sequence summarizes those operations necessary to program the I/O channels.

1. Reset
2. Send a Mode Instruction.
3. Send a Command Instruction.
4. Read STATUS.
5. Transfer data in or out.

* Note 1.

Command Word examples:

005 — (00 000 101) will Enable data in, Enable data out, Enable interrupts, and turn the Device Control off (Logic high).

047 — (00 100 111) will Enable data in, Enable data out, Enable interrupts, and turn the Device Control on (Logic low).

100 — (01 000 000) will reset the channel. Mode and Command must be programmed.

H8 to H10 INTERFACE TABLE

Refer to Pictorial 3-3 for the following table.

NOTE: The following table indicates the configuration for channel ϕ on the H10 Interface.

Address — 370
A1-A2 OPEN
B1-B2 OPEN
Jumpers C1-C2 INSTALLED
E1-E2 INSTALLED
F, G, and H — OPEN (unless called for in the software instruction).

This completes the "Operation."

The H8-2 to H10 Interconnect Cable is tabulated below.

H8-2 Interface				H10 Interface	
Function	Pin	Wire color	Signal Flow	Pin	Function
Data ϕ	1	Black	→	11	Data ϕ
Data 1	2	Brown	→	12	Data 1
Data 2	3	Red	→	13	Data 2
Data 3	4	Orange	→	14	Data 3
Data 4	5	Yellow	→	15	Data 4
Data 5	6	Green	→	16	Data 5
Data 6	7	Blue	→	17	Data 6
Data 7	8	Violet	→	18	Data 7
Ground	9	Gray		24	Ground
Data Taken	10	White	←	21	Punch Ready
Take Data	11	Black	→	20	Punch Command
Device Control	12	Brown	→	22	N/C
Device Ready	13	Red	←	19	Punch Ready
Device Control	14	Orange	→	23	N/C
Send Data	15	Yellow	→	10	Reader Start
Data Sent	16	Green	←	9	Reader Ready
Ground	17	Blue		24	Ground
Data 7	18	Violet	←	8	Data 7
Data 6	19	Gray	←	7	Data 6
Data 5	20	White	←	6	Data 5
Data 4	21	Black	←	5	Data 4
Data 3	22	Brown	←	4	Data 3
Data 2	23	Red	←	3	Data 2
Data 1	24	Orange	←	2	Data 1
Data ϕ	25	Yellow	←	1	Data ϕ

PICTORIAL 3-3

IN CASE OF DIFFICULTY

The Troubleshooting information on Page 38 for your Parallel I/O Card is presented in a series of test charts. If you know that a problem exists in a particular circuit, proceed to the test chart that covers that circuit. Read the following paragraphs carefully before you begin troubleshooting.

PRECAUTIONS FOR TROUBLESHOOTING

1. Be cautious when testing transistors and integrated circuits. Although they have almost unlimited life when used properly, they are much more vulnerable to damage from excessive voltage and current than other circuit components.

2. Do not remove any components from the circuit board while the Computer is turned on.

3. When you make repairs to the circuit board, make sure you eliminate the cause as well as the effect of the trouble. If, for example, you find a damaged resistor, make sure you find out what caused the resistor to become damaged (wiring error, etc.) If the cause is not eliminated, the replacement resistor may also become damaged when the Computer is put back into operation.

4. Refer to the "X-RAY Views" and "Schematic Diagram" to locate various components.

5. The following symbols and procedures are used in the troubleshooting charts:

   Follow the "YES" arrow when you obtain the proper result or condition.

   Follow the "NO" arrow when you do not obtain the proper result or condition.

   N/O means non-operative. If a component is N/O, be sure to check the associated circuitry for wiring errors, assembly errors, solder bridges, etc. Also, when wiring errors, solder bridges, etc. are listed as a possible cause of trouble, this does not apply to factory assembled units.

   Unless called for, pulse width and pulse shape are not measured. Only the excursion between TTL high and TTL low states is important for these tests. TTL high is +2V minimum and TTL low is +.8V maximum.

   A logic probe may be used instead of an oscilloscope for all measurements. Where noted, a logic probe is preferred instead of an oscilloscope.

   In an extreme case where you are unable to resolve a difficulty, refer to the "Customer Service" information inside the rear cover of the Assembly Manual.

6. If a problem occurs, check for the following conditions before you proceed to the "Troubleshooting Charts."

   a) Are all the required jumper wires installed on the circuit board?

   b) Is the test plug installed on the channel under test?

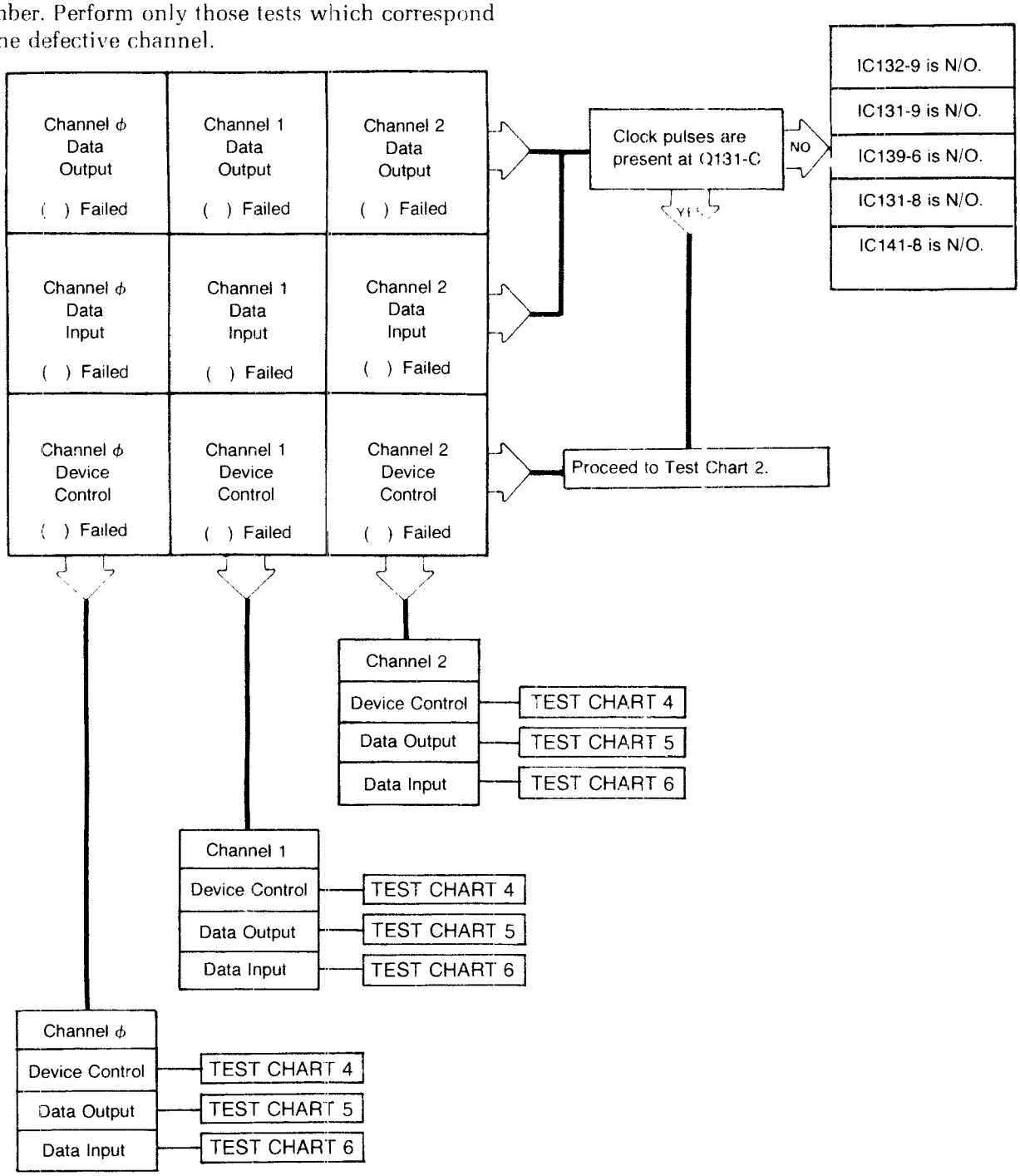
   c) Does the white wire near IC's 144 and 145 measure 5± .25 volts dc?

7. If you suspect a faulty IC in one channel, interchange the suspected IC with a known good one of the same type from one of the other channels. Be careful not to bend the pins when you remove or install an IC. Note: IC's 103, 104, 114, 123, and 124 are MOS devices and can be damaged by static electricity. Use care when you handle them.

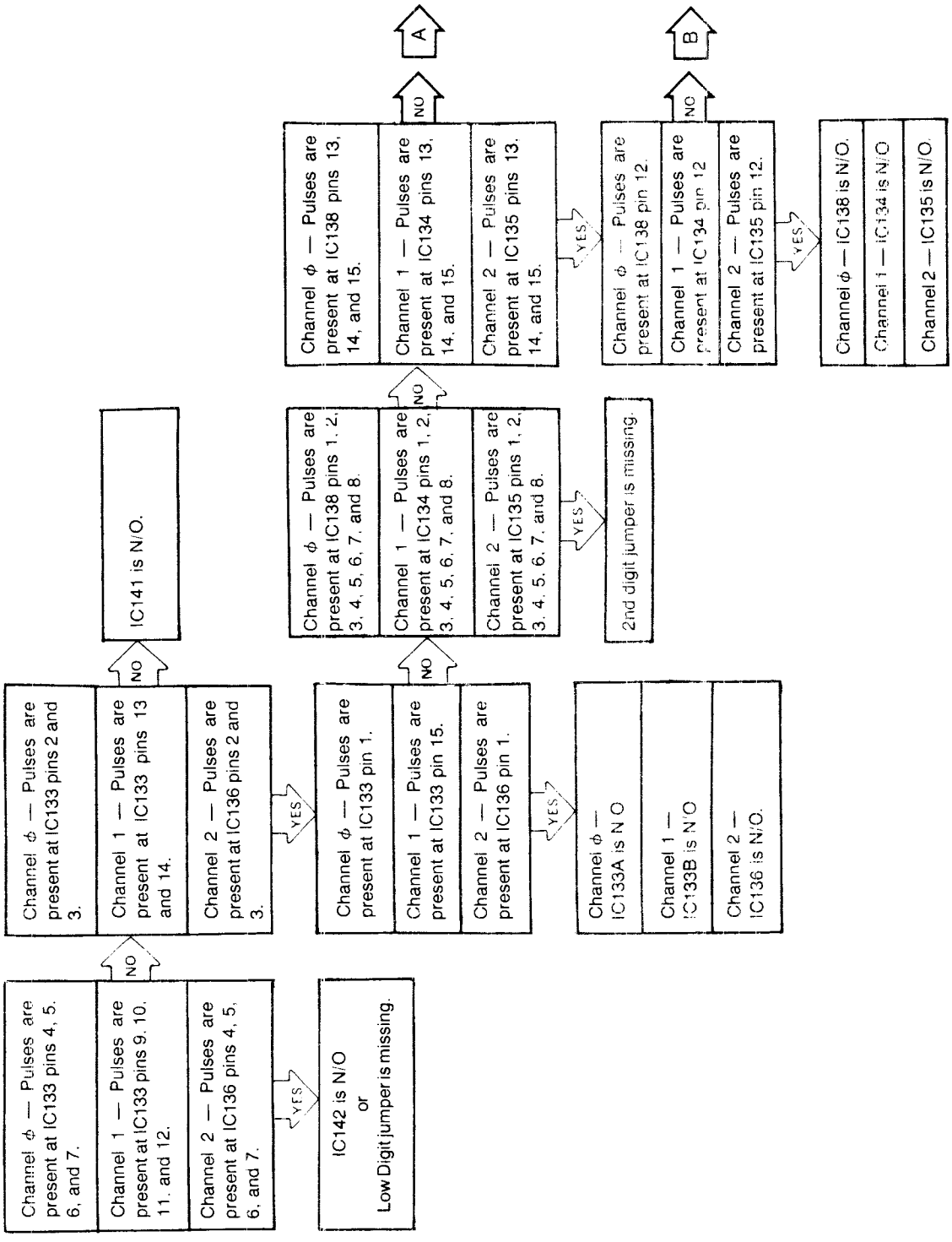
Troubleshooting Charts

TEST CHART 1

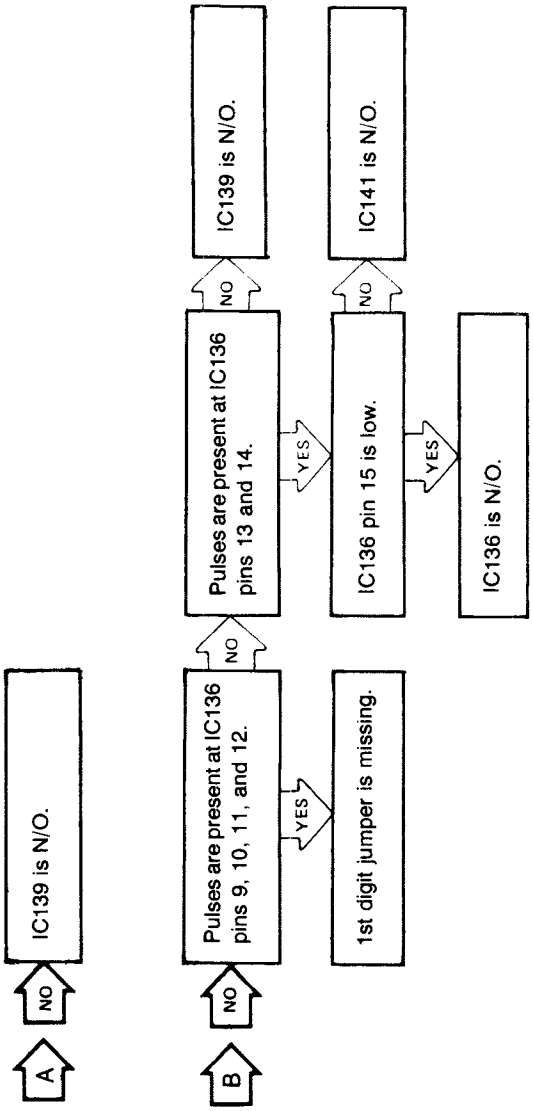
NOTE: If a failure occurs in any channel, check the failure in the appropriate "Failure" box. If three failures occur horizontally (across), the fault is common to all three channels. Continue with the tests to the right of the chart. Failures in a vertical row of boxes indicates a fault peculiar to a separate channel. Continue downward to locate the correct test chart number. Perform only those tests which correspond to the defective channel.



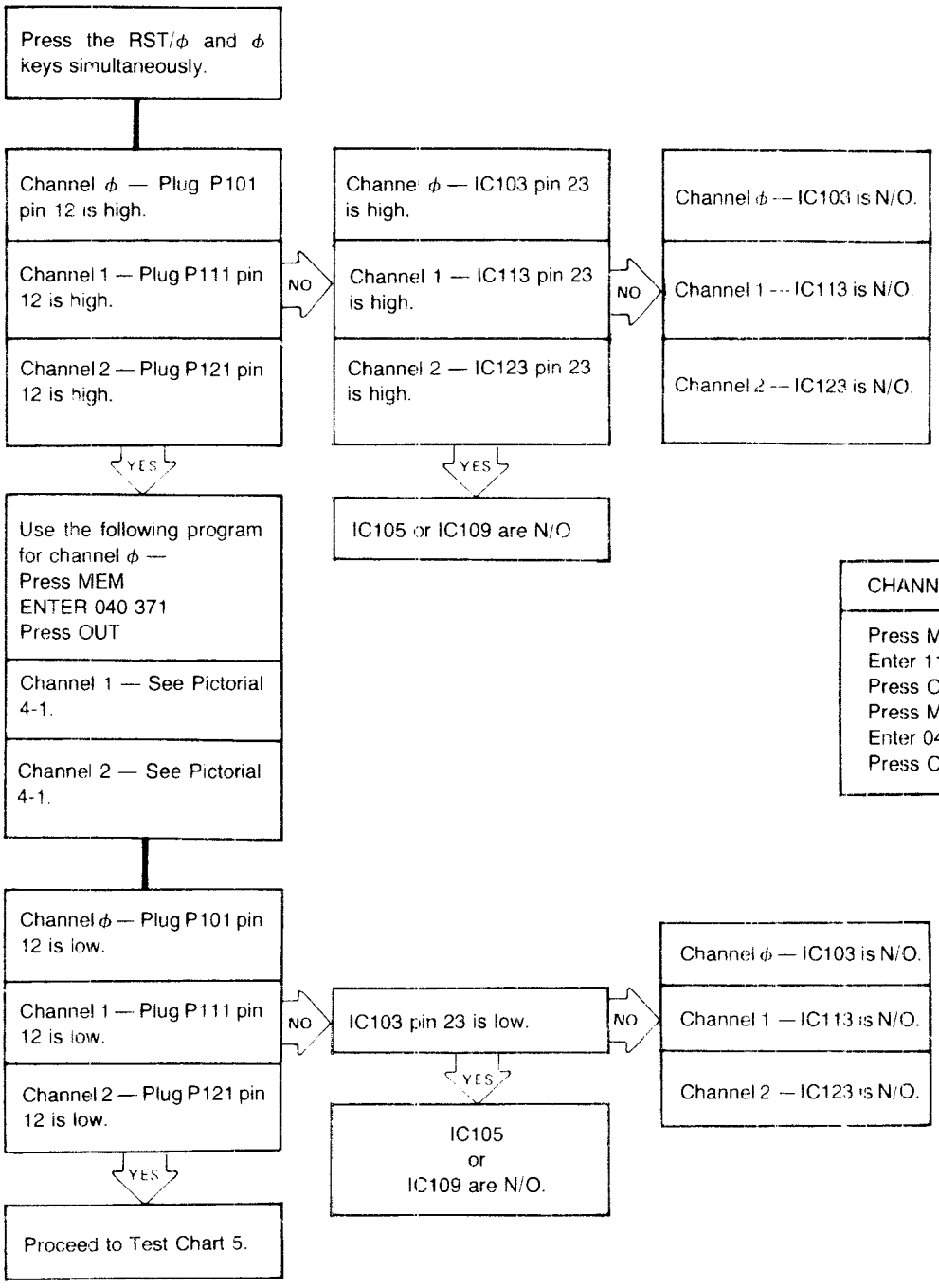
TEST CHART 3


Channel ϕ — Pulses are present at IC133 pins 4, 5, 6, and 7.
Channel 1 — Pulses are present at IC133 pins 9, 10, 11, and 12.
Channel 2 — Pulses are present at IC136 pins 4, 5, 6, and 7.
NO
YES
IC142 is N/O or Low Digit jumper is missing.
Channel ϕ — Pulses are present at IC133 pins 2 and 3.
Channel 1 — Pulses are present at IC133 pins 13 and 14.
Channel 2 — Pulses are present at IC136 pins 2 and 3.
NO
YES
IC141 is N/O.
Channel ϕ — Pulses are present at IC133 pin 1.
Channel 1 — Pulses are present at IC133 pin 15.
Channel 2 — Pulses are present at IC136 pin 1.
NO
YES
Channel ϕ — IC133A is N/O
Channel 1 — IC133B is N/O
Channel 2 — IC136 is N/O.
Channel ϕ — Pulses are present at IC138 pins 1, 2, 3, 4, 5, 6, 7, and 8.
Channel 1 — Pulses are present at IC134 pins 1, 2, 3, 4, 5, 6, 7, and 8.
Channel 2 — Pulses are present at IC135 pins 1, 2, 3, 4, 5, 6, 7, and 8.
NO
YES
2nd digit jumper is missing.
Channel ϕ — Pulses are present at IC138 pins 13, 14, and 15.
Channel 1 — Pulses are present at IC134 pins 13, 14, and 15.
Channel 2 — Pulses are present at IC135 pins 13, 14, and 15.
NO
YES
A
Channel ϕ — Pulses are present at IC138 pin 12.
Channel 1 — Pulses are present at IC134 pin 12
Channel 2 — Pulses are present at IC135 pin 12.
NO
YES
B
Channel ϕ — IC138 is N/O.
Channel 1 — IC134 is N/O
Channel 2 — IC135 is N/O.

Test Chart 3 (cont'd.)



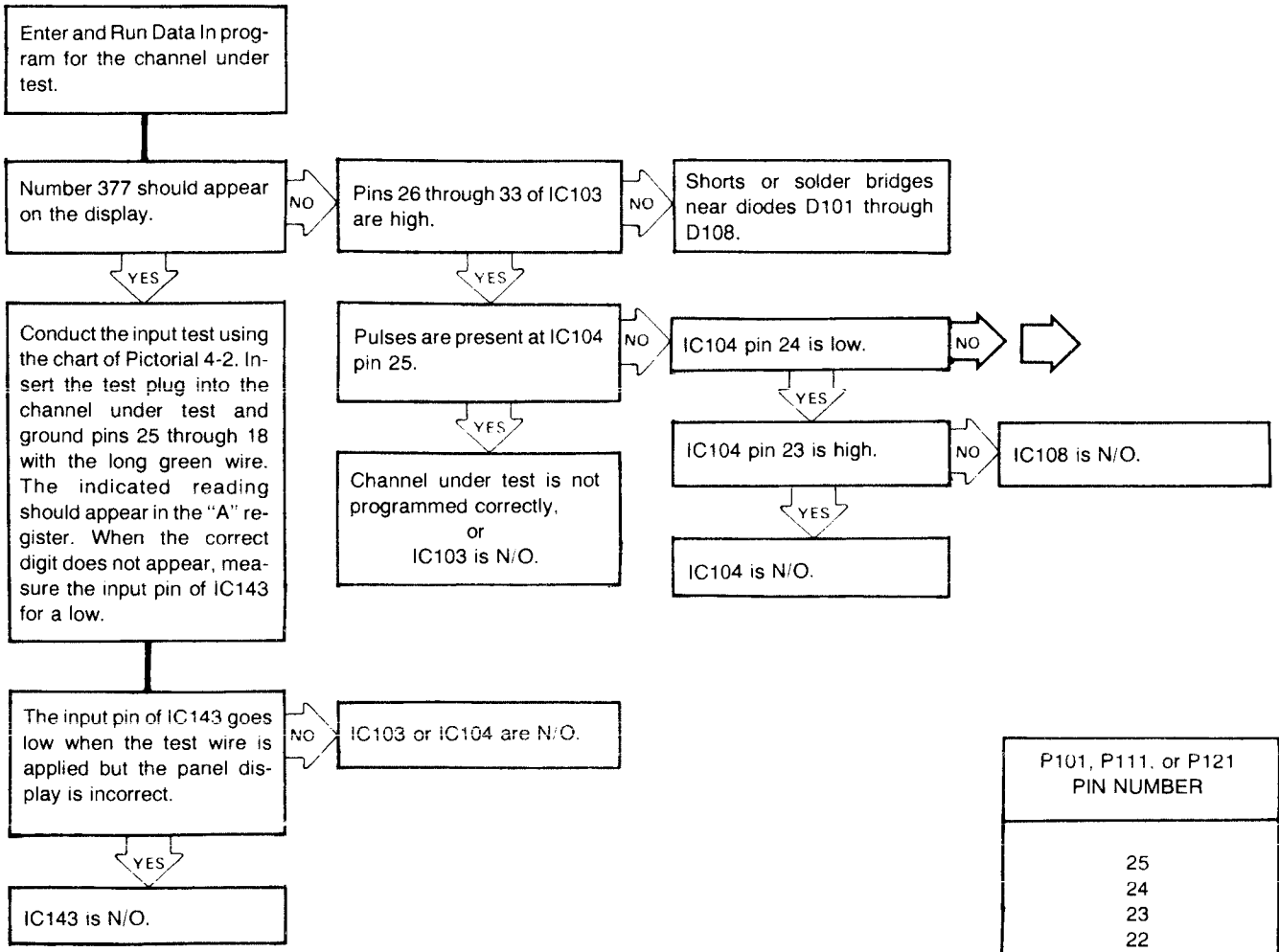
TEST CHART 4



CHANNEL 1	CHANNEL 2
Press MEM Enter 116 375 Press OUT Press MEM Enter 040 375 Press OUT	Press MEM Enter 116 377 Press OUT Press MEM Enter 040 377 Press OUT

PICTORIAL 4-1

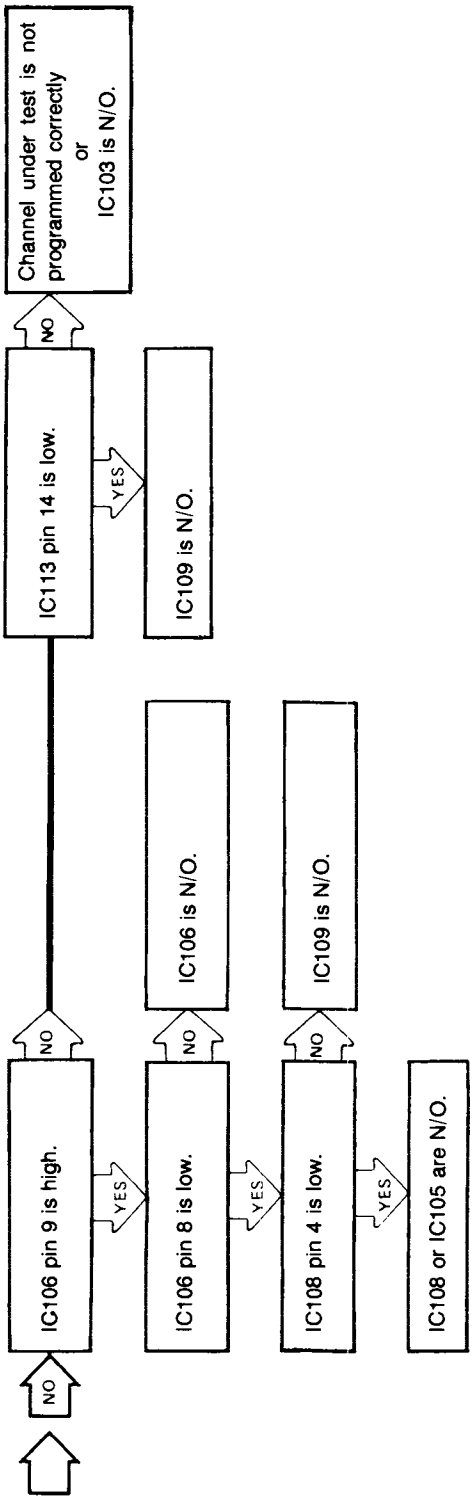
TEST CHART 6



P101, P111, or P121 PIN NUMBER	READING	IC143 INPUT PIN#
25	376	8
24	375	6
23	373	4
22	367	2
21	357	17
20	337	15
19	277	13
18	177	11

PICTORIAL 4-2

Test Chart 6 (cont'd.)



SPECIFICATIONS

Data	3 independent channels of input and output ports. Transfer rate-2500 bytes per second, maximum.
Control	Continuous transfer or Handshake mode. All Handshake functions occur on 1 to 0 transition. Reader Control Capability.
	All data and control outputs are TTL buffered with 10-Load drive capability.
	All data and control inputs, 1 TTL load, maximum.
Interrupt Capability	Separate input and output interrupt capability under CPU control.
Programming	Each port may be addressed by any I/O address pair from 000 to 377.
General	Operating temperature 0° to 40° C.
	Power Requirements-8 volts DC at 800ma (from H-8 bus).

CIRCUIT DESCRIPTION

Refer to the Schematic Diagram (Fold-in) and to Pictorial 4-3 (Illustration Booklet, Page 4) while you read this "Circuit Description.

NOTE: For the pin assignments and function, refer to "Operation" for IC103 and to the Glossary at the end of the "Circuit Description" for IC104.

The H-8-2 Parallel I/O Card provides three identical channels of parallel I/O ports. Since the three channels (Channel ϕ, Channel 1, and Channel 2,) are identical, only Channel ϕ will be discussed.

The three channels, along with their respective IC's are as follows:

Channel ϕ — IC's 101 through 109.

Channel 1 — IC's 111 through 119.

Channel 2 — IC's 121 through 129.

IC's 131 through 139, IC's 141, 142, 143, and transistor Q131, provide common functions to all of the channels.

ADDRESS DECODER

The channel decoder causes each I/O channel to respond only to its particular number. When the CPU addresses a channel, the number is put on the lower 8 bits of the address line. (Due to the structure of the Computer, the address data lines go to a low state when asserted.) These lines are fed to IC136B (common to all three channels), IC138, IC134, IC135, IC133A, IC133B, and IC136A. IC136B selects the most significant digit. With the correct jumpers in place, IC's 133A, B, and 136A will respond when specific addresses are present. Each channel has a separate 3-digit decoder, and each decoder has three sections. The channels and their associated decoder IC's are as follows:

Channel ϕ — IC's 136B, 138, and 133A.

Channel 1 — IC's 136B, 134, and 133B.

Channel 2 — IC's 136B, 135, and 136A.

As soon as the selected output of IC136B goes low, it enables the 2nd-digit decoder IC138, IC134, or IC135.

When the output of the second digit decoder goes low, it enables the least significant digit selector IC131A, IC133B, or IC136A. (Note that only even-numbered addresses are available from the third-digit decoders. This is because each channel requires a pair or addresses — one for the data and one to control the data.) The least significant bit of the address ($\overline{A_0}$) is used to select between control and data modes. The selected output of IC133A goes low when it is addressed. This output then goes to the $\overline{CS}$ input of IC103 (for channel ϕ) and enables it. The output of IC's 133B and 136A go to the enabled line of IC113 and IC123 respectively. The address decoders are active during the memory references also and the decoder chain may be enabled. This has no effect on the memory references since the I/O Read and Write pulses are not present.

DATA BUS BUFFERS

IC's 137 and 143 form a bi-directional, tri-state, data bus buffer. When any of the three data channels are being read, the bus driver, IC143, is turned on. When the CPU is writing to one of the channels, the bus Receiver, IC137, is enabled. This inverts the system data bus and puts it on the local data bus to IC's 103, 113, and 123.

CONTROL LOGIC

IC142B is a negative OR gate which responds to the three address decoders. When any of the three channels is addressed, the output of IC142B goes high. This output is tied to the inputs of IC's 142A and 142C where it is "And" ed with the I/O Read (IOR) and I/O Write (IOW) signals. When a channel has been addressed and IOR is high, IC142A goes low, turning on IC143 and asserting the $\overline{RD}$ line to IC's 103, 113, and 123. Since only one of these has the $\overline{CD}$ set low, only one is turned on in the Read mode. When the IOW pulse is present with the address enable signal, IC142C goes low in a similar manner and asserts the $\overline{WR}$ line to IC's 103, 113, and 123. The $\overline{WR}$ signal is also connected to the reset and "D" input of IC132A. A low on the Reset causes the output of IC132A to go low, enabling the bus receiver, IC137. When the signal from IC142C returns high, the bus receiver will remain on. The next low to high transition of the $\overline{\phi 2}$ clock will set the Q output high, turning off the bus receiver.

CLOCK SCALER

The $\overline{\phi 2}$ clock goes through an inverting buffer, IC141D. This drives the clock (pin 20) of IC's 103, 113, and 123. (Do not confuse this with the Receiver and Transmitter clock of the same IC's). IC141D also drives IC131B which is a ÷ 5 scaler. This is buffered by IC139B and is used for the Receiver and Transmitter clocks of IC's 103, 104, 113, 114, 123, and 124. IC141D also drives IC's 131A and 132B for an additional ÷4 scaler. This signal is buffered by Q131 and drives the clock input of IC's 107A, 107B, 108A, 108B, 117A, 117B, 118A, 118B, 127A, 127B, 128A, and 128B.

DATA TRANSFER OUT

With the data to be transferred present on the data bus (D0 through D8) of IC103 and with pin 11 ($\overline{CS}$) low and pin 10 ($\overline{WR}$) strobed, IC103 accepts the parallel data byte and generates a serial form of this byte. The serial word is transmitted at a rate equal to 1/16 of the clock signal at pin 9 (T_xC). The serial word is sent to pin 20 (RRI) of IC104. The shift register in IC104 is clocked at the same rate as the shift register in IC103 that is generating the data stream. Here it is converted back to a parallel byte. The parallel byte appears at RB1 through RB8 of IC104. The output of IC104 is buffered by IC's 102 and 101 to protect IC104 and to increase the output drive capability. When IC104 senses the end of a serial word, it sets DR high to indicate that the data register has been loaded. This signal is sent to ($\overline{CTS}$) pin 17 of IC103. Before the CPU transfers a new byte to the output port of a channel, it must inspect the $\overline{CTS}$ bit of the status word to determine if the output register is already occupied. The data ready signal is also inverted by IC109E and is applied to the $\overline{S_2}$ input of IC107B. Each time the $\overline{S_2}$ input receives a 1 to 0 transition, the output will transmit one pulse synchronously with the clock input (pin 11). This pulse is the "take data" handshake signal. The $\overline{DR}$ signal is also applied to the reset of IC107A. When the reset line is low, a 1 to 0 transition from the "data taken" handshake at the $\overline{S_2}$ input of IC107A permits the transmission of a single pulse to DRR (pin 18) of IC104. This pulse on the DRR resets the DR output which then clears the CTS status flag of IC103 and allows the next data transfer. In the Continuous mode (with the A1 to A2 jumper in place), the DR output may remain in the low state and the "Take Data" handshake will not be available. The "Take Data" input must be held low to assure pulses from IC107A to the DRR input of IC104. The "Data Taken" may not be used to control the channel in the Continuous mode.

DATA TRANSFER IN

With the data to be transferred present on the TBR1 through TBR8 (pins 26 through 33 of IC104), a 1 to 0 transition must take place at the "Data Sent" input. This allows IC108A to transmit one clock pulse to TBRL (pin 23). This pulse at the Transmitter Buffer Load Register Line caused IC104 to latch and then to transmit the serial data stream from TRO (pin 25) to RxD (pin 3) of IC103. When the serial transfer from IC104 is complete, TRE (pin 24) will be set. This sets $\overline{R}$ of IC108A low and allows the next "data sent" transition to clock TBRL (pin 23). The serial data transfer to IC103 are asserted, the data is present at D_0 through D_8 1/16 of the clock rate. When the complete serial word has been received by IC103, the RxRDY bit is set in the status register of IC103. This allows the CPU to test to see if a data byte is available. When $\overline{CS}$ and $\overline{RD}$ of IC103 is asserted, the data is present at D_0 through D_8 of IC103 and connected to the CPU data bus. When the CPU reads the data register of IC103, RxRDY (pin 14) goes low. (A high indicates the receiver contains a byte for the CPU.) This output is buffered by IC109B and the 1 to 0 transition allows IC108B to transmit one clock pulse from the "data sent" handshake.

For Continuous operation, the B1-B2 jumper is in place. When the inverted RxRDY is high, indicating that the buffer in IC103 is available, the output of IC106C will go low and IC108A will transmit pulses to TBRL of IC104.

DEVICE LINES

The $\overline{RTS}$ (pin 23) of IC103 is buffered by IC109D and IC105B to provide a "Device Control" output. The output goes low whenever the $\overline{RTS}$ bit D_5 of IC103 command word is set. This function is provided for the CPU control of external devices. With the C1-C2 jumper in place, it may be used for CPU control of the "data sent" handshake.

The "Device Ready" handshake input is buffered and inverted by IC105A and connected to (DSR) (pin 22) of IC103. This controls D_7 in the status word of IC103 and may be used to allow the CPU to monitor the status.

INTERRUPT

The complete CPU interrupt bus is available on the Parallel I/O Card. Lines I1 through I7 are asserted low and are held high with pull up resistors at the CPU. **Three outputs from IC103 suitable for interrupts (TxE, TxRDY, and RxRDY) are inverted by the open collector buffer IC106. Any combination of IC106A, B, or D may be connected to the channel interrupt bus at G2, F2, and H2. This bus can then be connected to any** CPU interrupt line from $\overline{I1}$ through $\overline{I7}$. Inputs 2, 5, and 13 of IC106 are tied together to provide a control for the interrupts. The outputs of IC106A, B, and D will be forced high as long as the control line is held high. The $\overline{DTR}$ is a general purpose output controlled by bit D_1 of IC103 command word. It must be set after each reset to enable the interrupts.

POWER SUPPLY

All components of the H8-2 Parallel I/O Card operate on +5 volts DC. This is provided by two 3-terminal 5-volt regulators, IC's 144 and 145, which are powered from the 8-volt H8 bus. These regulators provide 5 volts DC (± .25 volts) and are current-limited to protect against overload.

Glossary

PIN ASSIGNMENT AND FUNCTIONS (IC's 104, 114, 124)

PIN	SYMBOL	DESCRIPTION
1	VCC	+5 volts Supply
2	N/C	No connection
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5 thru 12	RBR8 thru RBR1	The contents of the RECE VER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified from RBR1-RBR8.
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is prohibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.

PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data, and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT
26 thru 33	TBR1-TBR8	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits, the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking, and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format, and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
38	CLS1	See Pin 37 - CLS2.
39	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

8251 Basic Functional Description

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility.

In a communication environment, an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

The following is a general set of requirements needed to properly operate the USARTs. This information is then followed by more technical and detailed information.

The following sequence of events must happen for a USART to work properly:

1. At power-up, or following a master reset, the USART is reset.

2. A MODE INSTRUCTION is sent to the USART defining the following characteristics of the I/O channel:

   - Clock rate.
   - Character length.
   - Parity.
   - Number of stop bits.

   The Mode Instruction is a word sent by the CPU to the USART register at the odd-numbered port of the two ports assigned to each USART. The normal mode instruction for the Heath system is 116, which programs the USART for standard asynchronous operation.

3. A COMMAND INSTRUCTION is sent to the same port as the mode instruction. This word controls the actual operation of the USART. It enables portions of the circuitry, sets various bits, and resets the error flags.

4. A STATUS WORD may be read from this same port. It allows the CPU to determine when data may be transferred, which bits are set, and which errors have occurred.

5. Data is transferred between the USART and the CPU through the even-numbered port of the two ports assigned to each USART. (This is the port number which is actually programmed at the port decoder.) The mode and command instructions use the next higher port number.

6. A new Command Instruction may be sent to the USART at any time. If, however, the USART had a character in its transmit buffer, that character would be lost.

RESET (Reset)

A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition.

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4.5 times for asynchronous mode).

$\overline{WR}$ (Write)

A "low" on this input informs the 8251 that the CPU is outputting data or control words, in essence, the CPU is writing out to the 8251. See Pictorial 5-1.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251 ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	X	X	1	DATA BUS ⇒ 3-STATE

PICTORIAL 5-1

$\overline{RD}$ (Read)

A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251 that the word on the Data Bus is either a data character, control word, or status information.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general-purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is general-purpose in nature, Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions, such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is general-purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control, such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is general-purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control, such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique), and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals, both externally and internally, to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for the Polled operation the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty)

When the 8251 has no characters to transmit, the TxE output will go "high." It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers."

$\overline{\text{TxC}}$ (Transmitter Clock)

The transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{\text{TxC}}$ is equal to the actual Band Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{\text{TxC}}$ is a multiple of the actual Band Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x, or 64x the Band Rate.

For example:

If Baud Rate equals 110 Baud,
$\overline{\text{TxC}}$ equals 110 Hz (1x)
$\overline{\text{TxC}}$ equals 1.76 kHz (16x)
$\overline{\text{TxC}}$ equals 7.04 kHz (64x).
If Baud Rate equals 9600 Baud,
$\overline{\text{TxC}}$ equals 614.4 kHz (64x).

The falling edge of $\overline{\text{TxC}}$ shifts the serial data out of the 8251.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique, and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for Polled operation, the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{\text{RxC}}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{\text{RxC}}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{\text{RxC}}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x, or 64x the Baud Rate.

For example:

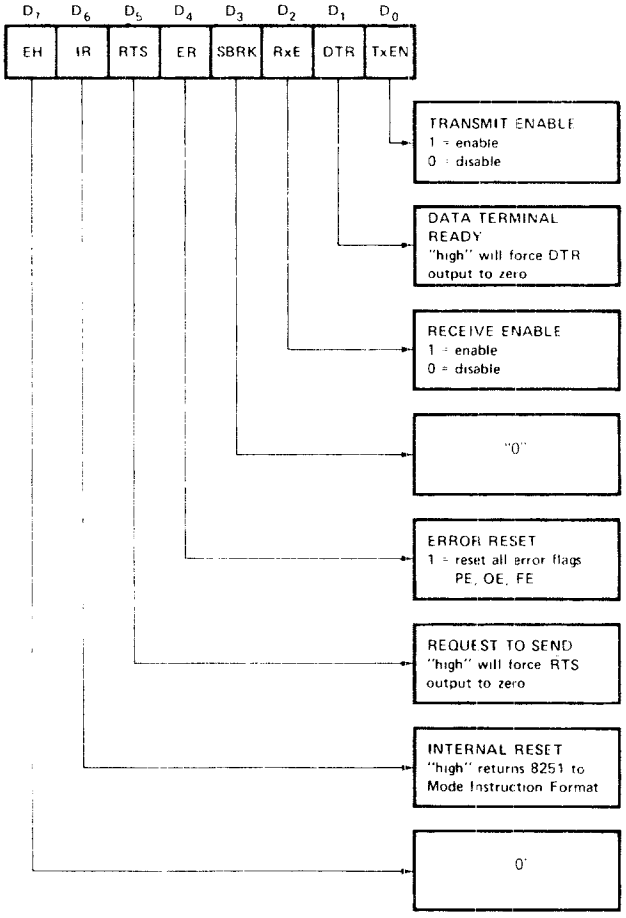
If Baud Rate equals 300 Baud,
$\overline{\text{RxC}}$ equals 300 Hz (1x)
$\overline{\text{RxC}}$ equals 4800 Hz (16x)
$\overline{\text{RxC}}$ equals 19.2 kHz (64x).
If Baud Rate equals 2400 Baud,
$\overline{\text{RxC}}$ equals 2400 Hz (1x)
$\overline{\text{RxC}}$ equals 38.4 kHz (16x)
$\overline{\text{RxC}}$ equals 153.6 kHz (64x).

Data is sampled into the 8251 on the rising edge of $\overline{\text{RxC}}$.

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Instruction, the device is ready to be used for data communication. (See Pictorial 5-2). The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset, and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251, then all further "control writes" (C/$\overline{D}$=1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.

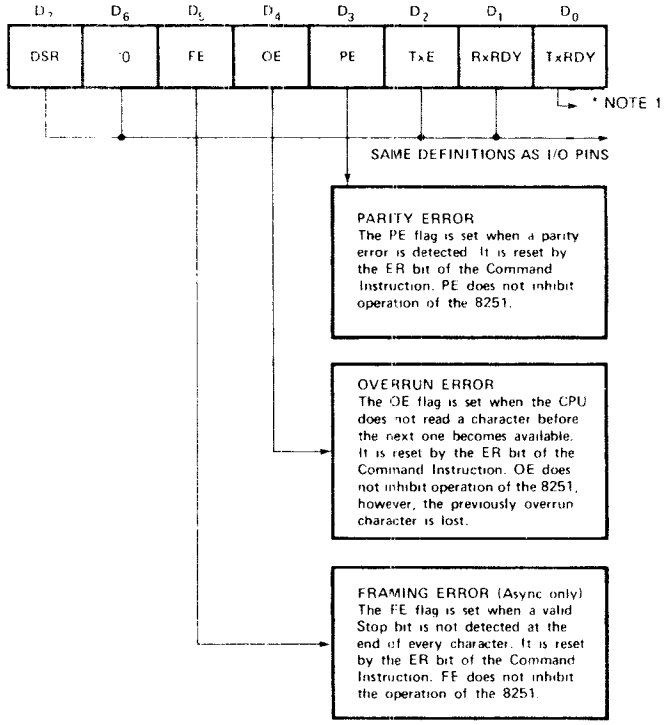


PICTORIAL 5-2

STATUS READ DEFINITION

In data communication systems, it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions have occurred that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. See Pictorial 5-3.

A normal "read" command is issued by the CPU with the C/$\overline{D}$ input at "one" to accomplish this function.



PICTORIAL 5-3

*Note 1 TxRDY status bit has similar meaning as the TxRDY output pin. The former is not conditioned by CTS and TxEN; the latter is conditioned by both CTS and TxEN.

e TxRDY status bit DB Buffer Empty
TxRDY pin out DB Buffer Empty•CTS•TxEN

Mode Instruction Definition

Asynchronous Mode (Transmission)

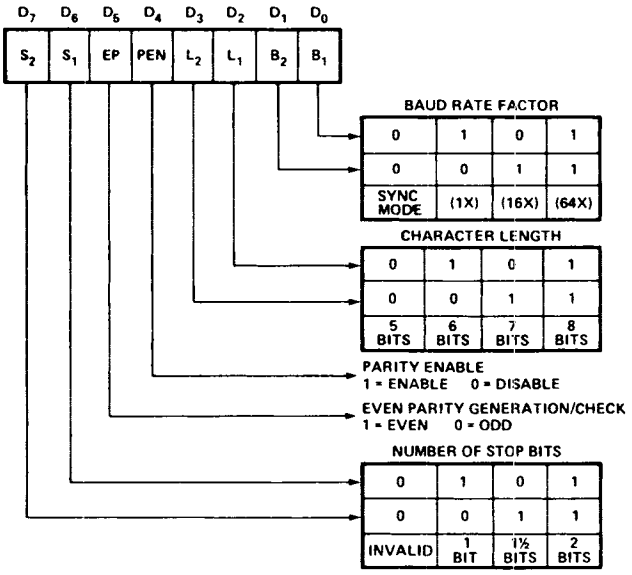
Whenever a data character is sent by the CPU, the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. (See Pictorial 5-4 and 5-5.) Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. Break characters can be continuously sent to the TxD if commanded to do so.

When no data characters have loaded into the 8251, the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

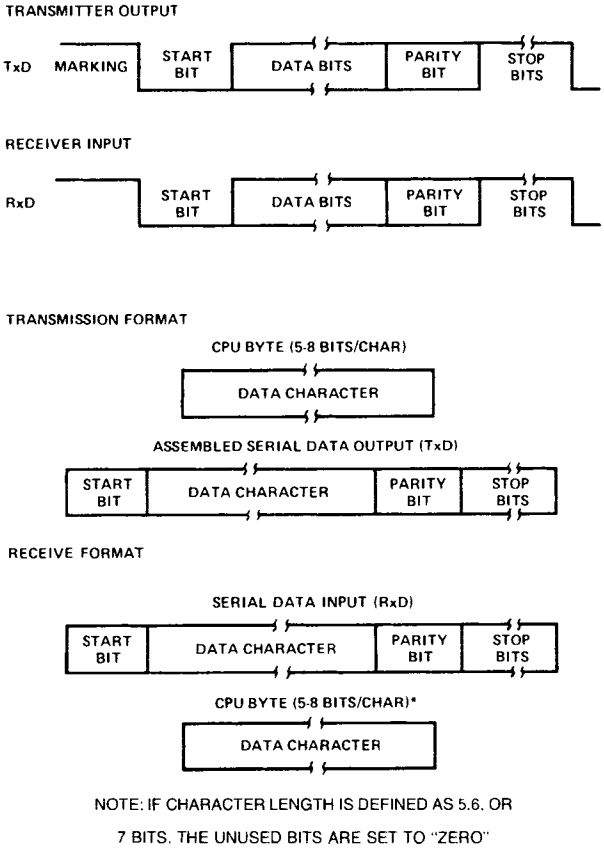
Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a Start bit. The validity of this Start bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid Start bit, and the bit counter will start counting.

The bit counter locates the center of the data bits, the parity bit (if it exists), and the Stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the Stop bit, the Framing Error flag will be set. The Stop bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the Overrun flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.



PICTORIAL 5-4



PICTORIAL 5-5

NOTE: In most communication systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and are tied together and connected to a single frequency source.

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, Even/Odd Parity, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

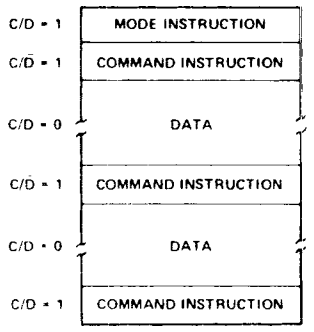
This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251.

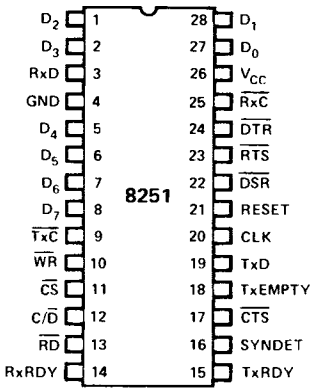
Both the Mode and Command instructions must conform to a specified sequence for proper device operation. (See Pictorial 5-6.) The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format, a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions.



PICTORIAL 5-6

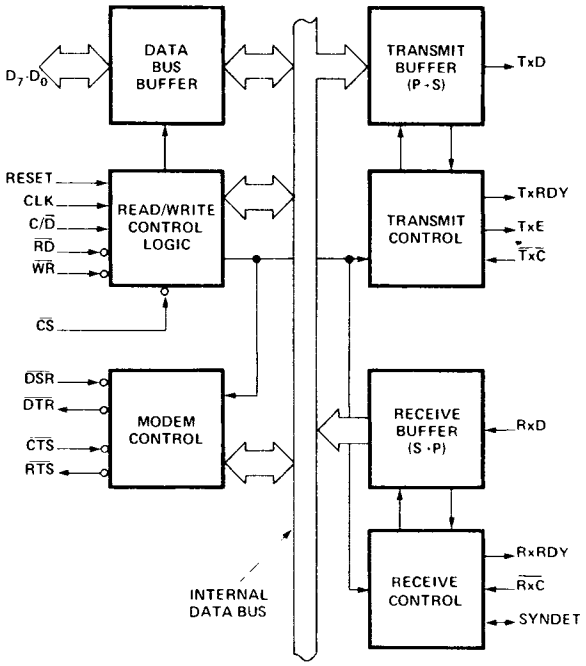
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



PICTORIAL 5-7

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SEMICONDUCTOR IDENTIFICATION

This section is divided into two parts; Component Number Index and Part Number Index. The Component Number Index provides a cross-reference between component numbers and their respective Part Numbers. The component numbers are listed in numerical order. The Part Number Index provides a lead configuration detail (basing diagram) for each semiconductor Part Number. The Part Numbers in this section are also listed in numerical order.

COMPONENT NUMBER INDEX

This index shows the Part Number of each semiconductor on the Parallel I/O Circuit Board.

Diodes

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D100 — D107	56 — 56
D110 — D117	56 — 56
D120 — D127	56 — 56

Transistor

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
Q101	417-875

Integrated Circuits

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
IC101	443-698
IC102	443-698
IC103	443-776
IC104	443-761
IC105	443-46
IC106	443-54
IC107	443-841
IC108	443-841
IC109	443-755

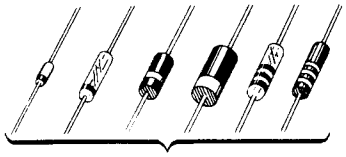
Integrated Circuits (cont'd.)

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
IC111	443-698
IC112	443-698
IC113	443-776
IC114	443-761
IC115	443-46
IC116	443-54
IC117	443-841
IC118	443-841
IC119	443-755
IC121	443-698
IC122	443-698
IC123	443-776
IC124	443-761
IC125	443-46
IC126	443-54
IC127	443-841
IC128	443-841
IC129	443-755
IC131	443-731
IC132	443-6
IC133	443-822
IC134	443-53
IC135	443-53
IC136	443-822
IC137	443-754
IC138	443-53
IC139	443-755
IC141	443-755
IC142	443-12
IC143	443-753
IC144	442-54
IC145	442-54

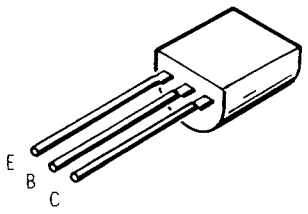
PART NUMBER INDEX

This index shows a lead configuration detail (basing diagram) of each semiconductor Part NUMBER.

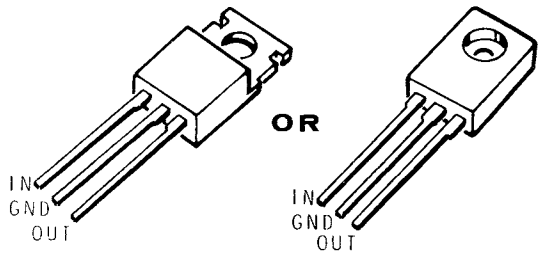
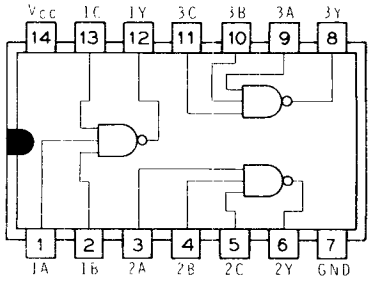
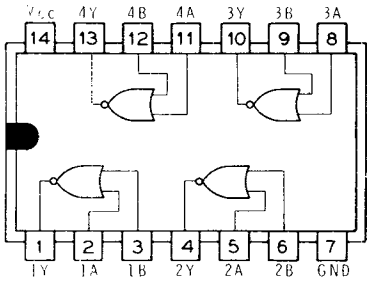
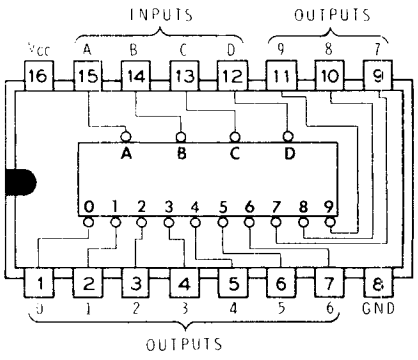
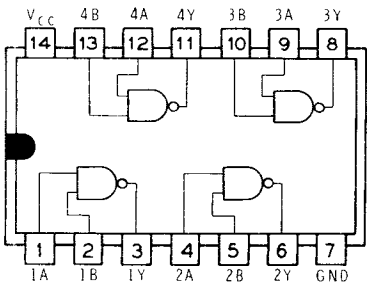
Diodes

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
56-56	1N4149	S1 DIODE 10mA, 75V	NOTE: DIODES MAY BE SUPPLIED IN ANY OF THE FOLLOWING SHAPES. ALWAYS POSITION THE BANDED END AS SHOWN ON THE CIRCUIT BOARD.  BANDED END

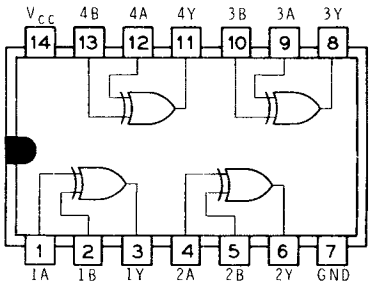
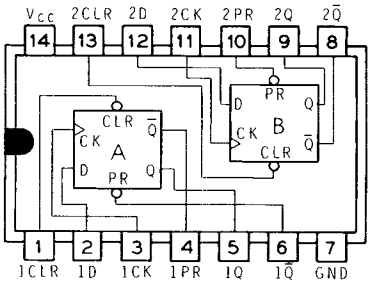
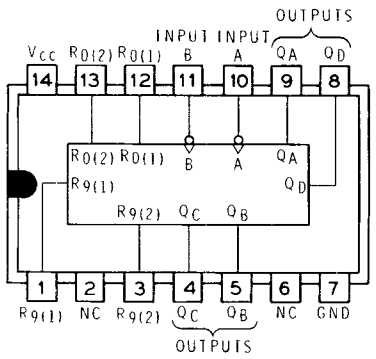
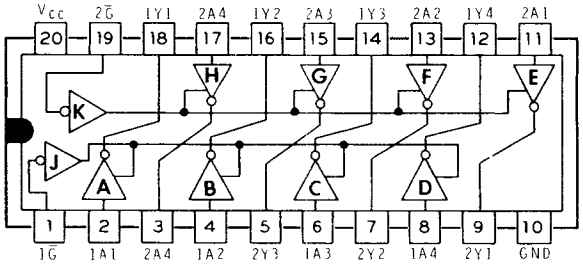
Transistor

HEATH PART NUMBER	MAY BE REPLACED WITH	IDENTIFICATION
417-875	2N3904	

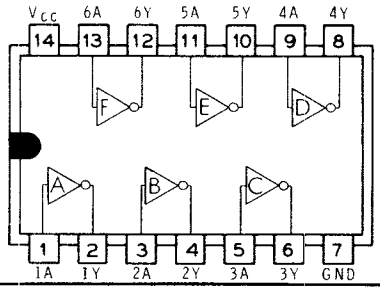
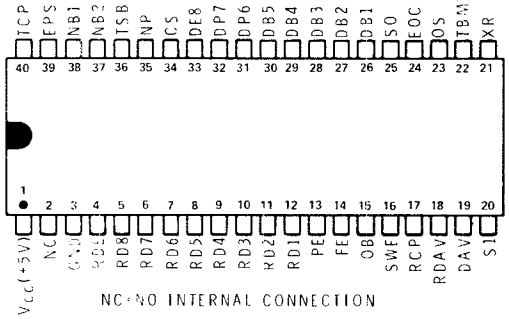
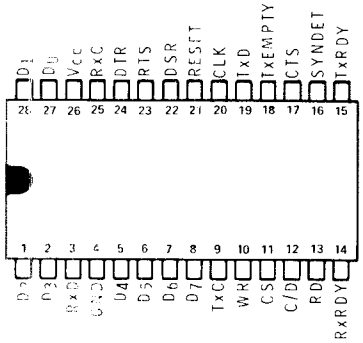
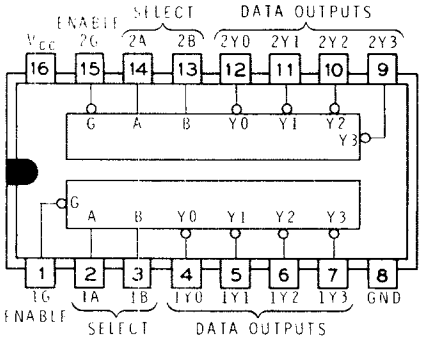
Integrated Circuits

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
442-54	7805	5-VOLT REGULATOR	
443-12	7410	TRIPLE 3 INPUT NAND GATE	
443-46	7402	QUAD 2-INPUT POSITIVE NOR GATE	
443-53	7442	4 TO 10 LINE DECODER	
443-54	7403	QUAD 2-INPUT NAND GATE	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-698	7486	QUAD EXCLUSIVE OR GATE	
443-6	7474	DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	
443-731	74LS290	BCD UP COUNTER	
443-754	74LS240	OCTAL BUFFERS/ LINE DRIVERS/ LINE RECEIVERS INVERTED 3-STAGE OUTPUTS	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-755	74LS04	HEX INVERTER	
443-761	6402	UART	
443-776	8251	USART	
443-822	74LS139	DUAL 2 TO 4 LINE DECODER	
443-841	74120	DUAL PULSE SYNCHRONIZER/ DRIVER