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GRAPHICS—256

298-138-B

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ADDENDUM TO GRAPHICS—256 DOCUMENTATION

1. Included with your Graphics Display Board kit are two 220 pfd capacitors. Attach one between IC33 pin 1 and ground and the other between IC39 pin 1 and ground.
2. In the Vertical Output Circuitry of the schematic, change the label U42 of the 7420 with pins 1,2,4,5 and 8 to U27.
3. In the Vertical Output Circuitry section of the schematic add a 2.2K pull-up resistor on the line labeled GRAPH. This line is connected to Z2 pin 7.

I. INTRODUCTION

The Digital Group High Resolution Graphics Display board is a high resolution graphics interface with 256 display points on each of 256 raster scan lines. Sufficient graphics power is available to plot detailed charts and graphs, draw pictures or sketches, create intricate game boards, or run space-war simulations. The possibilties are limited only by your imagination.

Utilizing a memory mapping technique, the High Resolution Graphics Display does not use up RAM already dedicated to the CPU since it contains its own 8K bytes of onboard memory. This on board memory is seen by the CPU as another 8K RAM board and can be used for additional program memory when graphics operation is not desired. A separate board enable/disable line is available to selectively enable the board under software control, allowing overlapping of other memory. Only CPU access is disabled, therefore display is continuous. This effectively gives you 72K of available memory.

The Light Pen functions with the High Resolution Graphics Display under software control to allow the user to precisely indicate points on the screen. Not only does the Light Pen allow you to indicate a character or line on the display, but it gives you the ability to draw detailed pictures by precisely knowing its position on the screen.

A video mixer circuit and external sync lines are provided in order to synchronize the display with your TV readout board. Either the TV readout or graphics may be selected manually or under software control, or they may be superimposed for writing captions on charts and graphs, messages on game displays, or monitoring the operation of your program. The video output is compatible with a TV monitor.

II. SET UP AND OPERATION

General

The Digital Group High Resolution Display has three basic modes of operation including Free Standing Display, Light Pen and Graphics Control, and External Sync and Video Mixing. Following is a discussion of each mode and a description of setting up the Graphics Display for each mode in a Digital Group System.

In addition to the set up of the Graphics Display, some modifications to the Z80 CPU board and motherboard must be made. First, install a germanium diode (1N60 or 1N48) between the 2.2k pull up resistor and ROM enable line to IC20 pin 14 on the Z80 CPU board. This requires cutting the trace between IC20 and the pull-up. This is diode A in Figure 1. Second, install a 1N4148 diode (diode B) and a 330 ohm, ¼watt resistor according to Figure 2. Cut the trace to IC28 pin 12 between the 470 ohm pull down resistor and pin 6 of IC 21. For some early disk installations, IC21 has been removed from the CPU. If IC21 has been removed, do not install the 330 ohm resistor. Third, connect a wire between pin 12 of IC28 and finger BC of the edge connector on the Z80 CPU board.

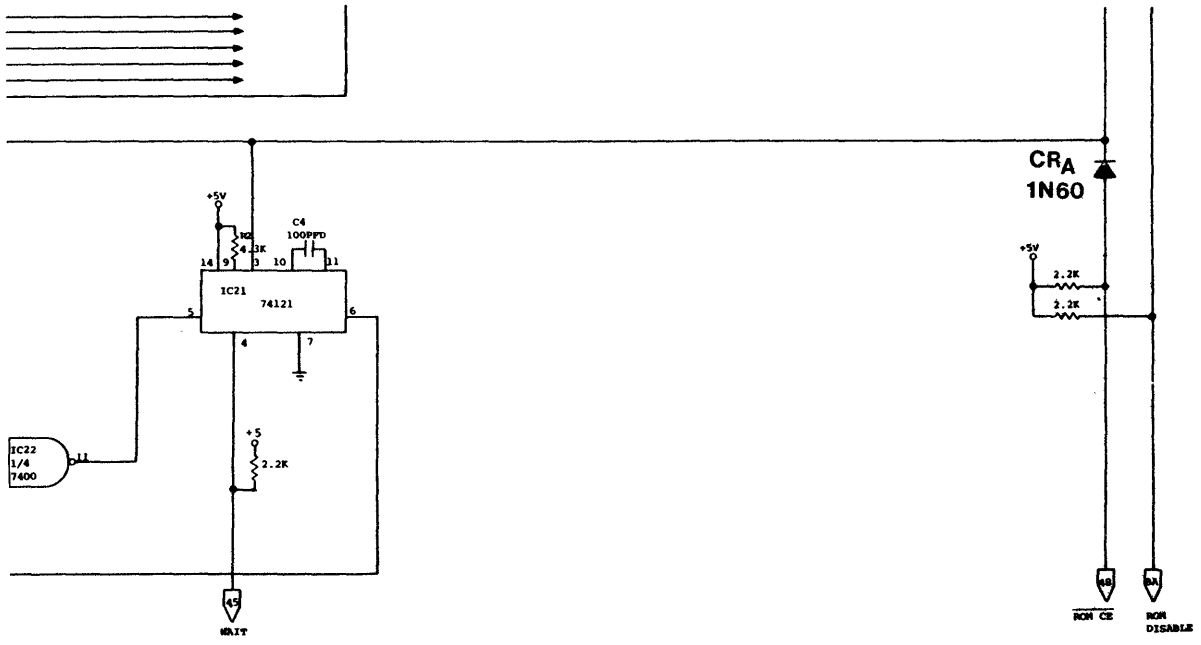


FIGURE 1. INSTALLATION OF CRA on Z80 CPU.

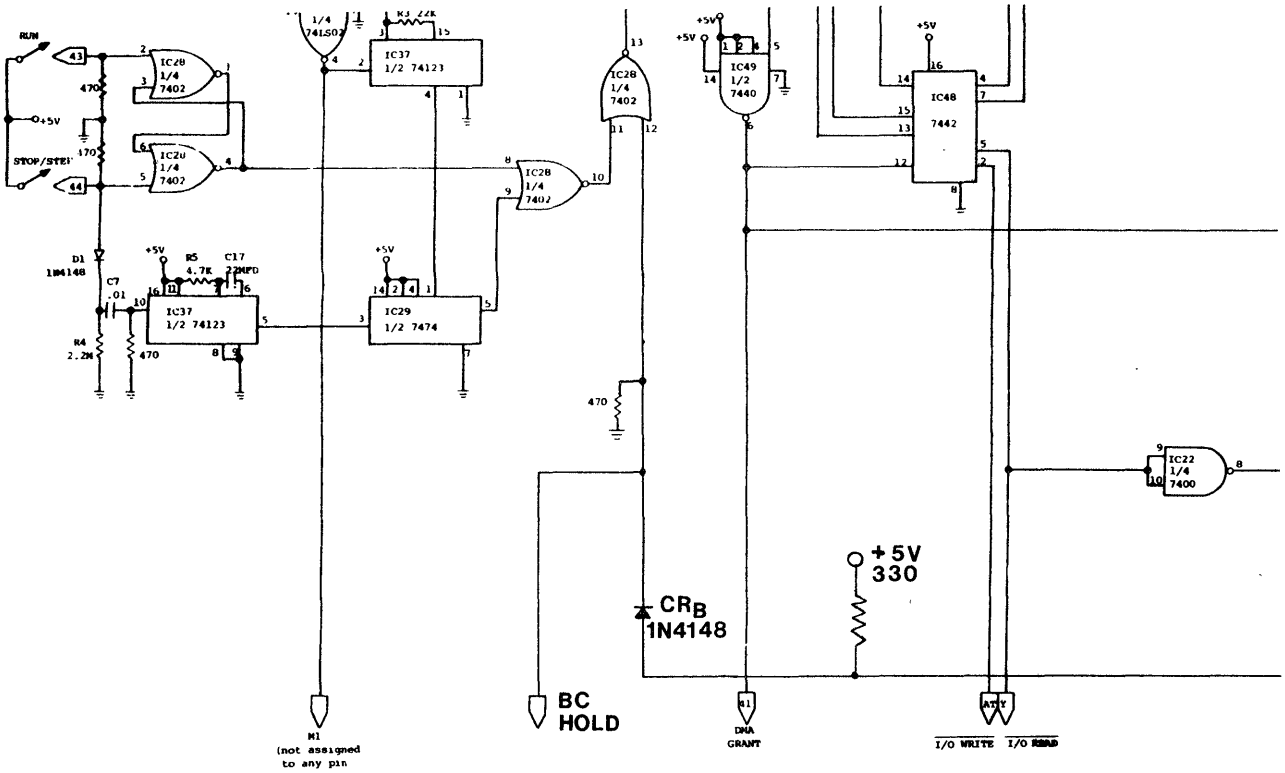


FIGURE 2. INSTALLATION OF CRB, 330 ohm resistor on Z80 CPU.

If your system has been configured for a Floppy Disk Controller, diode B may already be installed as well as a diode between BC on the edge connector and pin 12 of IC28. If so, remove the diode between BC and IC28 and install it on the disk controller board between pin 36 of the edge connector and pin 11 of IC34. Refer to Figure 3 for the proper orientation of the diode on the disk controller. The trace to pin 36 must be cut.

Fourth, connect a wire between pin 20 of the memory bus and pin BC of the Z80 CPU slot on the bottom of the motherboard.

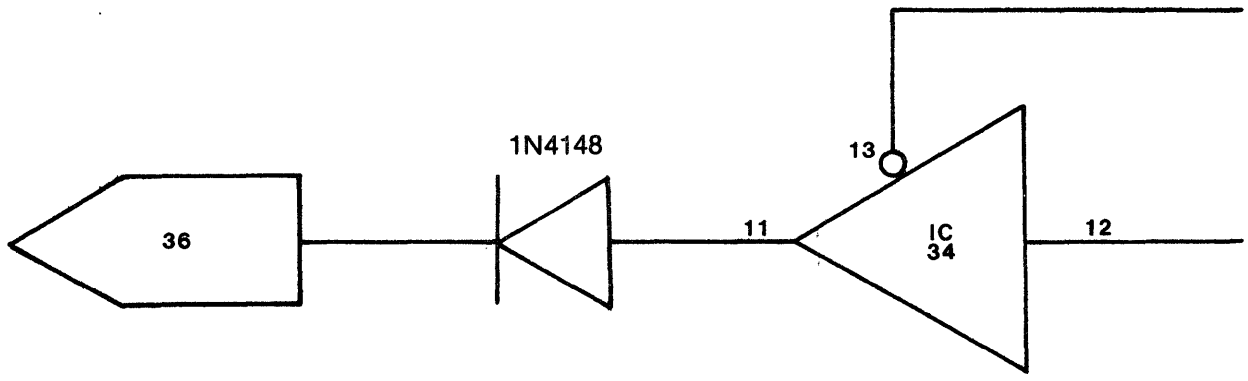


FIGURE 3. DIODE INSTALLATION ON DISK CONTROLLER

A. Free Standing Display

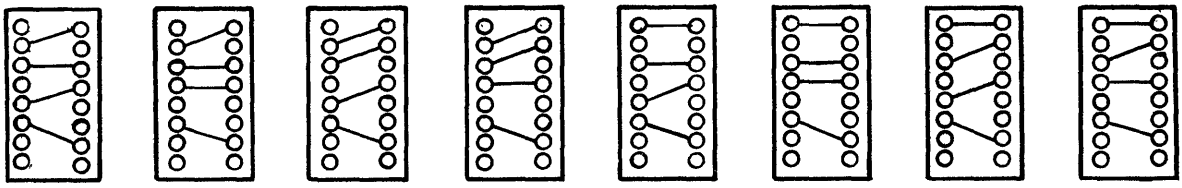
General

This mode of operation allows the user to perform all plotting and pictorial functions of the Graphics Display as well as use of the board as 8K of system memory. The board is inserted in a memory slot without connecting the associated cabling and Light Pen. Since the Graphics Control Cable, Graphics Input Cable and Light Pen are not connected, several functions are not available. Unavailable functions are: use of the Light Pen, superimposing an external video signal such as the TVC-64 output over the graphics display and software control of video and the ability to enable or disable the memory when overlapping another memory board in the system.

Set up for this mode requires installing several jumpers for addressing and memory accessing. Figure 4 shows the address jumper configurations for any 8k block of memory in a Digital Group Z80 based system. Refer to the Parts Layout in the Appendix to locate the jumper socket. Pins 7,8, and 9 of A2 are used for jumpering the ROM enable signal ($\overline{ROM}$), which also disables RAM boards in the Digital Group system. Figure 5 shows the proper jumper configuration for $\overline{ROM}$ when the Graphics Display overlaps either a RAM board or a ROM board. If the Graphics Display is not overlapping other memory, the $\overline{ROM}$ jumper may be omitted or jumpered as if it were overlapping a RAM board.

Jumper socket A1 and jumpers JPR1 through JPR5 set up the video section of the Graphics Display. The video output may be set up for either composite video (video with sync signals) or separate video and sync signals. Separate video and syncs would be used with the Digital Group Data Monitor without a sync separator (MON9D-COMP). Most monitors will require composite video. For the Free Standing Mode, the video output will be connected at Pin M of the memory bus and JPR2 must be installed.

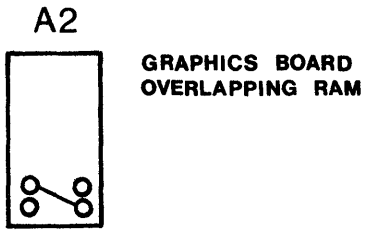
Two dot widths are available, half dot width and full dot width. Half dot width makes a more defined dot and is recommended for initial testing. Full dot width makes adjacent dots touch causing the display to appear brighter.

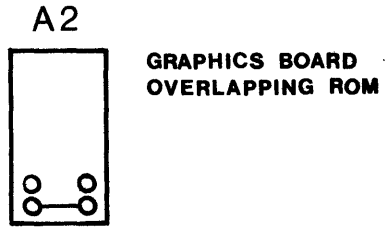


0-8K (00-1F)	8-16K (20-3F)	16-24K (40-5F)	24-32K (60-7F)	32-40K (80-9F)	40-48K (A0-BF)	48-56K (C0-DF)	56-64K (E0-FF)

JUMPERS DEFINE START OF 8K BOUNDARIES

FIGURE 4. ADDRESS JUMPERS - SOCKET A2





IF GRAPHICS BOARD IS NOT OVERLAPPING ANY OTHER MEMORY, NO JUMPER IS REQUIRED

FIGURE 5. ROM JUMPER - SOCKET A2

COMPOSITE VIDEO OUT

Install the jumpers as pictured in Figure 6 with the desired dot width. Connect the video from pin M of the memory bus to the video input of the monitor.

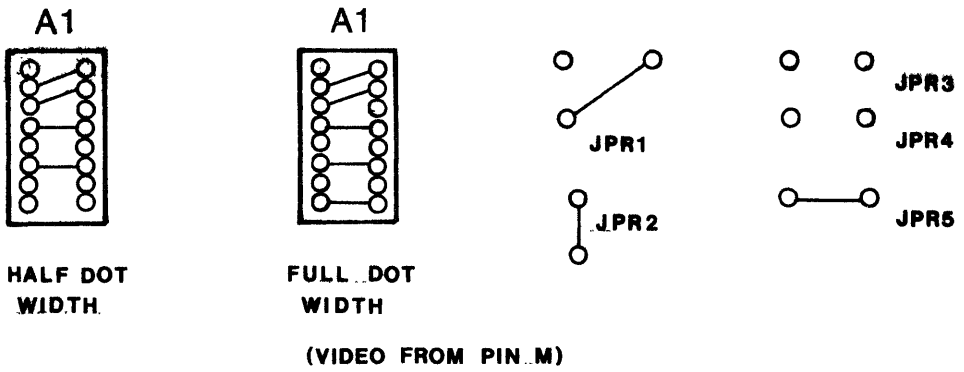


FIGURE 6. FREE STANDING MODE, COMPOSITE VIDEO OUT

SEPARATE VIDEO AND SYNC OUT

Install the jumpers as pictured in Figure 7 with the desired dot width. Remove R14 from the board. The horizontal sync (HORSYN) and vertical sync (VERSYN) are the bottom two pins of socket A3. Connect HORSYN to pin 6 of the edge connector of the Digital Group Data Monitor and VERSYN to pin 9. Connect the video out from pin M of the memory bus to pin 8 of the Data Monitor.

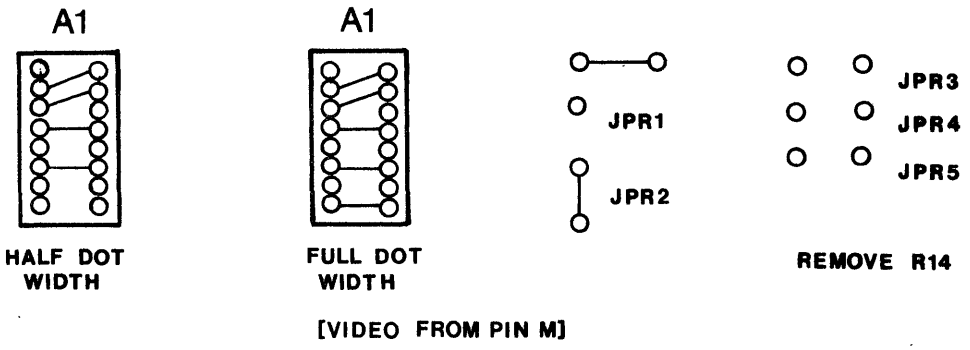


FIGURE 7. FREE STANDING MODE, SEPARATE SYNC OUT

B. Light Pen and Display Control

General

Operation of the Graphics Display with the Light Pen and Display Control requires installation of the Graphics Control Cable, Graphics Input Cable, Light Pen Cable with Paddlecard and the eight conductor double ended Molex cable. Refer to Appendix E for Digital Group bus pin assignments and Appendix F for cabling diagrams when installing the various cables.

Input Cable Installation

The Graphics Input Cable is connected between socket A3 and an unused Input Port by plugging the 16 pin dual in line connector into A3 and the 8 position Molex connector over the appropriate pins on the bottom of the I/O slot. Refer to Appendix E for the I/O pin assignments and Appendix F for the proper orientation of the cable and the pin out of A3.

Graphics Control Cable Installation

Insert the 16 pin dual in line connector into socket A4 and connect the two eight position Molex connectors to pins D through W of the back panel connector. Refer to Appendix F for the proper orientation of the cable and the back panel connector pin out.

Eight Conductor Cable Installation

Connect one end of the cable to pins 4 through 11 of the back panel connector and the other end to the Output Port you have assigned to the Graphics Display. Refer to Appendix E for the back panel connector pin out and the I/O bus pin out.

Light Pen and Paddle Card Installation

The Light Pen Cable includes the paddle card for connection to the back panel. Light pen operation is independent of the video output mode and external video mode. The paddle card is plugged into the back panel connector with the side with pins 1 and 22 marked oriented up. Connect the video cable for the monitor to VIDEO OUT and the shield to one of the GND holes.

Light Pen Operation and Control Signals

Control Signals

One eight bit output port is utilized for control signals to the Graphics Display. Seven of the bits control various functions of the display while one is used as feedback to the Light Pen to turn on the LED. Following is a brief description of each signal and its effect on the display.

$\overline{\text{LED}}$, MSB of output data, will turn on the LED in the Light Pen handle when at a logic Ø. The LED may be used to signal the user that the pushbutton on the Light Pen is closed (pushed), to tell the user that the computer is busy and unable to input Light Pen data, or any other function the user chooses.

A16, MSB-1 of output data, is used to enable or disable the memory of the Graphics Display. When A16 is at a logic 1, the memory is enabled. If the Graphics Display memory is overlapping a RAM board, that RAM will be disabled when A16 is high and the memory at that address is accessed. To access the RAM board instead of the Graphics Display, A16 must be at a logic Ø. The $\overline{\text{ROM}}$ jumper must be installed as in Figure 5 for overlapping RAM.

EXTVID, MSB-2, allows an external video signal to be superimposed over the Graphics Display video. When EXTVID is high, the external video is displayed. When low, only the Graphics video is displayed. The external sync will still effect the display however.

$\overline{\text{INV}}$, MSB-3, will invert the output video when at a logic Ø. When $\overline{\text{INV}}$ is a logic 1 the video will be white on black. Do not invert the video with external video superimposed on the Graphics Display.

GRAPH, LSB+3, is similar in function to EXTVID. A logic 1 on this bit enables the graphics data to be displayed in the output video. A logic Ø will display only the external video, provided EXTVID is high.

$\overline{\text{WHITE}}$, LSB+2, will fill the screen with dots when at a low level. In the normal white on black video display this will result in an all white screen. When $\overline{\text{WHITE}}$ is a Ø the CPU will see an FFH in all 8K memory locations of the Graphics Display. Data may be written into memory when $\overline{\text{WHITE}}$ is low but cannot be read. The data can be read when $\overline{\text{WHITE}}$ goes high. $\overline{\text{WHITE}}$ must be high at all times if the Graphics Display is being utilized as system memory. $\overline{\text{WHITE}}$ in conjuction with PSELØ will generate a signal labeled $\overline{\text{BLACK}}$ which blacks the screen when low. $\overline{\text{BLACK}}$ will be low when PSELØ is low and $\overline{\text{WHITE}}$ is high.

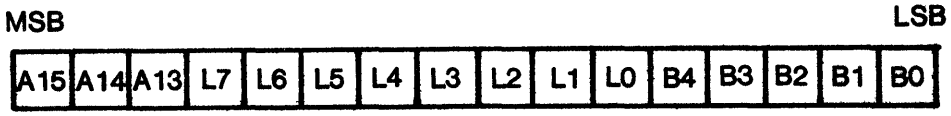
PSEL 1, LSB+1,and PSEL Ø, LSB enable the Light Pen data and board status. The Light Pen data will be either the line counter values (LØ-L7) or the bit counter values (BitØ-B4). The line count is enabled when PSEL Ø and PSEL 1 are both low. The bit count is enabled when PSEL Ø is high and PSEL 1 is low. The status is enabled when PSEL 1 is high. A logic Ø on PSEL Ø also clears the flip-flop that is triggered by light from the Light Pen and generates FOUND.

Light Pen Input Signals

The Graphics Input cable carries eight bits of data to an input port for locating the Light Pen on the monitor and four bits of data that relay the status of the location counters and Light Pen signals.

Data

The data that is enabled when PSEL0=0 and PSEL 1=0 is the line count at the time light is detected. The top line of the screen is line 0, or L0-L7 all zeros. Line 255 is the bottom line of the screen, or L0-L7 all ones.When PSEL0=1 and PSEL 1=0, the data is Bit 0-Bit2 and B0-B4. The leftmost dot of a line corresponds to Bit0-B4 all zeros while the right most dot is all ones. However, when the data is stored in memory, the leftmost bit of each memory location is bit 7. Therefore, in order to turn on a dot under the Light Pen in drawing routines, the value of Bit0-Bit2 must be complemented. The bit count indicates the horizontal or X distance from the left and line count is the vertical or Y distance from the top. The sixteen bit address of the memory location containing the dot is as pictured below.



The complement of Bit0, Bit 1, Bit 2 defines which bit (0-7) of the data is on or 1.

Status

When PSEL 1 is high, the data to the CPU is the status. POS4=$\overline{SW}$, POS5=B5, POS6=L8 and POS7=FOUND. The four least significant bits are not used when inputting status.

B5 is high during horizontal retrace, L8 is high during vertical retrace, FOUND is high each time light is detected by the Light Pen. Strobing in the line count (PSEL0=0) will clear FOUND. FOUND clocks the tri-state latches, therefore the values of L0-L7, B0-B4, and BIT0-BIT2 at the output of the latches are not valid until FOUND goes high.

$\overline{SW}$ is low when the push-button switch on the Light Pen is pushed.

Using the Light Pen

The operation of the Light Pen is dependent upon the brightness of the monitor. Too little brightness will not trigger the Light Pen while too much brightness may overdrive the pen. Before using the Light Pen, refer to the Light Pen Calibration program in the SAMPLE SOFTWARE ROUTINES in the Appendix and follow the directions for calibration. Anytime the brightness is changed, the calibration will also change.

Video Output

The video output is connected to the paddle card through the Graphics Control Cable. The set up for the video output modes is the same as for the Free Standing mode except that JPR2 which connects the video to pin M of the edge connector is not required.

External Sync and Video Mixing

General

This mode of operation enables the user to superimpose an external video signal such as the TVC-64 over the Graphics Display. Superimposing may be useful for labeling a display, however the primary purpose of including this capability is to allow using the same monitor for displaying the graphics and operating system messages.

The video section may be set up for either composite external video or separate external syncs and video. As discussed in the set up for the Free Standing Display mode, the output video may also be composite video or separate syncs and video. All cabling in the following descriptions pertains to Digital Group systems.

Composite External Video

The external video may be connected to the Graphics Display inside the cabinet by connecting a wire from pin 16 of the TVC-64 edge connector to pin 18 of the back panel connector (Refer to the Back Panel Connector Pin Out in the Appendix). The external video may also be connected outside the cabinet at the point labeled VIDEO IN on the paddle card. (Refer to the Parts Layout for the Paddle Card in the Appendix). For composite external video, install the two jumpers labeled VIDEO and SYNC on the paddle card. Refer to Figure 8 and install the jumpers in socket A1 for composite external video. The sync level is adjusted by R8 and the video level by R13.

Separate External Video and Syncs

Connect the external video to either pin 18 on the back panel connector or VIDEO IN on the paddle card. The video output of the Digital Group TVC is pin 16 of the edge connector in the motherboard. Install the VIDEO jumper on the paddle card if the video is connected to pin 18. Connect the horizontal sync to EXHSYN on the paddle card and the vertical sync to EXVSYN. The horizontal and vertical sync outputs of the TVC-64 are pins 12 and 13 respectively on the edge connector. Refer to the TVC pin out in the Appendix for the required signals. Install the jumpers as pictured in Figure 8 for separate external video and syncs. Omitting JPR3 and JPR4 will invert the EXHSYN and EXVSYN signals.This will result in syncing on the trailing edge instead of the leading edge of the sync and the external video will be shifted with respect to the Graphics Display video.

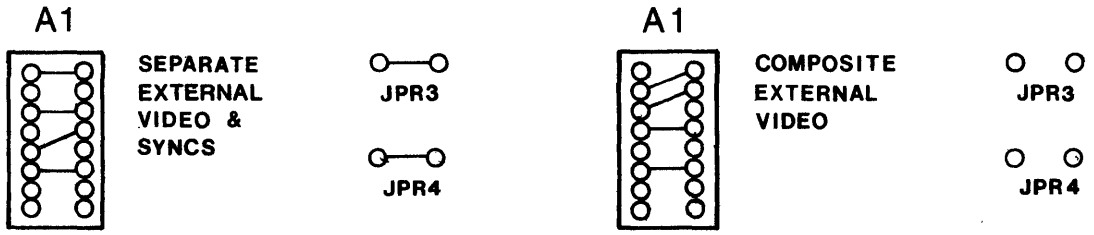


FIGURE 8. JUMPERS FOR EXTERNAL SYNC AND VIDEO MIXING

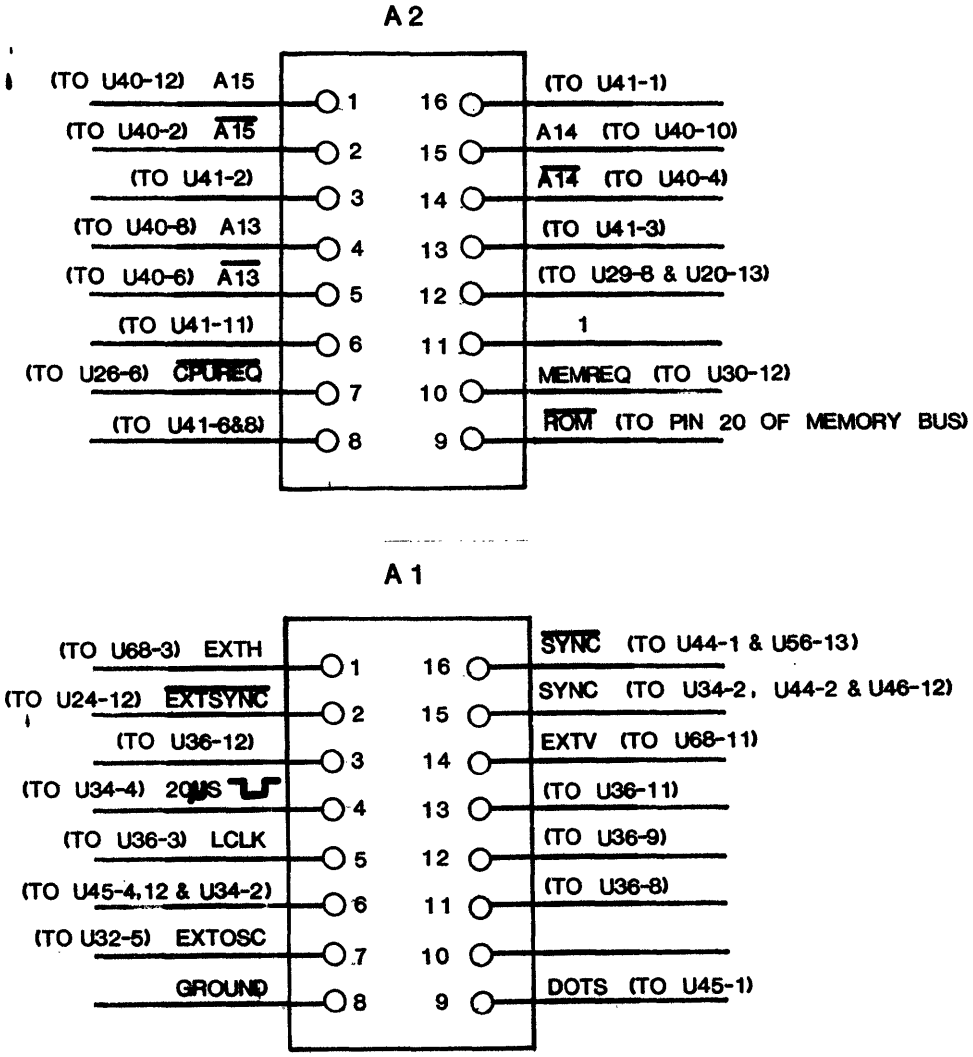


FIGURE 9. JUMPER SOCKET PIN ASSIGNMENTS

III. THEORY OF OPERATION

The general organization of the Graphics Interface is shown in the Block Diagram in Appendix A. The central section of the unit is a Random Access Memory which receives data from the Central Processing Unit (CPU) and outputs data to either the CPU or a TV Output Circuit. The TV Output Circuit converts the stored data into a video signal which can be displayed on a standard video monitor or TV modified for direct video input. Also contained in the TV Output Circuit are provisions for synchronizing the display with another video signal and superimposing the two on one screen. Control and multiplexing circuits allow the Memory to be accessed by both the CPU and TV display while preventing conflicts. Clock and timing circuits provide memory cycle timing, TV signal timing, and trigger an address counter which tracks the location of the next byte to be displayed.

MEMORY

The Memory section consists of 16 TMS-4050 4K Dynamic RAMS (U1 to 16) organized as an 8k block of 8-bit bytes. Refresh is accomplished by the continuous reading of data to be displayed. In order to expedite refresh, one bank of 8 RAMS (U1 to 8)contain all EVEN addresses and the other bank of 8 RAMS (U9 to 16) contains all ODD addresses. Using this scheme, the 128 memory accesses required to refresh all 64 rows of both banks represent 4 lines of displayed data. Since the duration of a display line is approximately 63.6 microseconds (a time fixed by the standard TV sweep frequencies), a complete refresh occurs in 0.254 milliseconds, considerably more often than the required 2 milliseconds. Data from the CPU is buffered by the 7401 data buffers (U37 &38) and applied to the memories. Since the TMS 4050 uses open-collector multiplexed I/O, a Data Enable (DE) is applied to the data input buffers to ensure they are enabled only when a memory write is to be performed. Both banks of the memory are fed in parallel by the data buffers but there is no conflict since both banks are never enabled simultaneously. Note that since the 7401 buffers invert the incoming data, all data is stored inverted and must be re-inverted after being read. Data read out from the memories is buffered by the 7400 data buffers (U25 & 47) and fed to the TV display 74165 shift registers (U48 & 49) and the 74173 CPU data output latches (U58 & 59). A signal ($\overline{\text{WHITE}}$) applied to the 7400 data buffers will force the output of the buffers to be all 1's if $\overline{\text{WHITE}}$=Ø. The purpose of this signal will be seen later. The memory address lines are driven by four 74367 tri-state buffers (U50, 51, 60, & 61). U51 & 61 are enabled when $\overline{\text{DISP}}$=Ø (i.e. DISP=1) allowing signals from the display address counter to be applied to the memory address lines. It will be seen later that the condition DISP=1 means that a memory cycle is to be performed to retrieve data for the DISPLAY. When DISP=Ø(and consequently DISPBUF=Ø) a CPU read or write cycle is to be performed; therefore, U50 & 60 are enabled, applying address signals from the CPU to the address lines of the memories. The derivation of the signals CEODD, CEEVEN, and R/W will be discussed in another section.

CLOCK, TIMING GENERATION, AND ADDRESS COUNTER

The clock frequency required is determined by the data rate which will produce the desired display on a TV monitor utilizing U.S. standard Vertical and Horizontal frequencies. Each data line is 46 Bytes long (3 bytes for a sync pulse, 5 bytes for a left margin, 32 bytes of data, and 6 bytes for a right margin). Therefore we have (based on 262 lines/frame):

Frame Time = (1/60) sec = 16.667msec (Vert Sweep = 60Hz)
Line Time = (1/60)(1/262) sec = 63.613usec (Horiz.Sweep = 15.72kHz)
Byte Time = (1/60)(1/262)(1/46) sec = 1.3829 usec
Bit Time = (1/60)(1/262)(1/46)(1/8) sec = 172.86nsec (5.784960 MHz)

The required data rate is 5.784960 MHz. A crystal twice this frquency is used to generate CK1=11.569920 MHz and then divided by two to achieve CK2 at the appropriate frequency. Signals CK1 and CK2 are used to clock and enable a counter chain (U33, 39, 52, 53, 62, & 63) which supplies the memory address used when a DISPLAY data fetch memory cycle is to be accomplished. U33, 52, and 62 may be thought of as the "Line Counter", keeping track of the number of the line currently being displayed. I.C.'s 39, 63, and the most significant bit of U53 may be thought of as the "Byte Counter", keeping track of the next data byte to be displayed. The Byte Counter is always one count ahead of the data byte currently being displayed because it is used to fetch the next data byte from memory before it is required. (Note that "Byte Ø" on any line is the first DATA byte, NOT the first byte of the line which would occur during the sync pulse, and NOT the first byte of the margin, either). The three least-significant bits of U53 are the "Bit Counter" and represent the data bit currently being displayed.

Memory cycle timing is accomplished by a 74195 shift register (U21) clocked by CK2. A memory cycle is begun by applying a Cycle Start (CS) signal to U21 pins 2, 3, and 9, and, depending upon conditions to be discussed later, may be either two or three cycles in length. The QA output of U21 is a TTL level signal labeled CE (Chip Enable) and is used directly to drive the 75451 which generates the 12 Volt Chip Enable signals (CEODD and CEEVEN) applied to the memory chips. The QB and QC outputs of U21 are labeled 2Q and 3Q respectively and are used elsewhere for timing purposes. Appendix B contains diagrams illustrating memory cycle timing.

Control Section

The control section determines when a memory cycle is required by the CPU or the display, sequences the requests to avoid conflicts, and issues appropriate control and timing signals. Control of the memory is allocated to either the Display or the CPU by a D-type 7474 flip flop (½U28) whose outputs are designated DISP and $\overline{DISP}$. The DISP signal is active when the Display is in control of the memory and, conversely, $\overline{DISP}$ is active when the CPU is in control of the memory.

A CPU memory cycle begins when the high order address lines (A15, A14, and A13) are addressed in the pattern selected by the address block select jumpers. These signals are applied thru the address select jumpers to a 7430 NAND gate (U41). Certain other signals are also fed to U41 and must be present to initiate a CPU cycle. $\overline{REFRESH}$ is gated in to assure that Z-80 refresh cycles do not trigger an unnecessary cycle. A16 is an extra "high order address line" and essentially serves as an externally driven "board select" line to allow the board to be enabled or disabled at will. Both $\overline{REFRESH}$ and A16 are tied to +5 thru pullup resistors so they are not affected when not in use. $\overline{MEMREQ}$ is inverted and gated to U41 in the case of Z-80 systems as is the composite of $\overline{MEMRD}$ and $\overline{MEMWR}$ for 8080 systems. Optionally, $\overline{ROM}$ can be gated in thru a jumper to allow a ROM to overlap the onboard memory without conflict. When the appropriate signals are present, $\overline{CPUREQ}$ is made low, indicating the CPU has requested a memory cycle. The falling edge of $\overline{CPUREQ}$ sets U31, ½ of a 7473 J-K flip flop, bringing COMPREQ high. COMPREQ is applied to the D input of a 7474 (U28) and, if $\overline{CE}$ is high (i.e. CE is low indicating that a memory cycle is not currently in progress) the next rising edge of $\overline{CK2}$ will set $\overline{DISP}$ high, giving memory control to the CPU. In the event $\overline{CE}$ is low, a memory cycle is in progress and control of the memory cannot be shifted to the CPU until the cycle is completed. Once $\overline{DISP}$ becomes high, a series of gates applies a HOLD signal to the CPU card thru pin 20. When 3Q becomes high, U31 is reset, driving COMPREQ low. After $\overline{CE}$ returns high (indicating completion of the CPU memory cycle) U28 will switch on the next rising edge of $\overline{CK2}$ and control of the memory will automatically revert to the Display.

A Display memory request is generated by making DISPREQ high on the next falling edge of $\overline{CK1}$ after BIT0, BIT1, and BIT2 become high simultaneously. DISPREQ is cleared by the occurrance of 2Q while DISP is high.

Once a CPU or Display memory cycle has been requested by making CPUREQ or DISPREQ high, a Cycle Start (CS) signal will be applied to the 74195 shift register (U21) and a memory cycle will begin. The gating (U20, and 27) will cause the memory cycle to be two CK2 cycles long for a Display Read and three CK2 cycles long for a CPU Read or Write.

DATA OUTPUT LATCHES

Output data to the CPU is latched in two 74173 tri-state D Registers. These registers are selected when DISP is low and data is clocked into them by 3Q. The tri-state outputs are enabled onto the data bus by $\overline{CPUREQ}$ being low.

TV OUTPUT CIRCUIT

Data to be displayed is loaded alternately into U48 and 49, the 74165 shift registers, depending on whether B0 is 1 or 0 (except that no data is loaded when $\overline{B5}$ is low indicating the margin of the picture. The data is then shifted out of the appropriate shift register by $\overline{CK2}$. The data from the shift registers (QHSR1 and QHSR2) is gated into the output circuit unless the terminal GRAPH is pulled low, disabling the display of graphics. If the terminal DOTS is not grounded, $\overline{CK2}$ is gated to the output breaking up horizontal lines into a series of dots to prevent horizontal lines from appearing brighter than vertical lines. Comparator U24 separates an external video signal into high and low levels which can be superimposed on the screen by bringing EXTVID high. The entire picture can be inverted by bringing $\overline{INV}$ low or can be blacked out by bringing $\overline{BLACK}$ low.

TV Synchronization

The Graphics Display provides all the signal processing necessary for TV synchronization for the various modes of operation including composite video output, separate video and sync output, composite external video, separate external video and sync, and no external video.

Horizontal sync pulses are provided by a one-shot with a 5us pulse width (U34) which is triggered by RSB, the reset to the bit counters (U53, U63). RSB is generated when the bit counters reach the end of a line or an external horizontal sync occurs. The horizontal sync is applied to the circuit consisting of U43 and U56 which produces a serrated sync to ensure that horizontal sync is maintained during vertical retrace. In the composite video output mode, the serrated sync is fed to an inverter (U23) through JPR1 to produce active low pulses and added to the video through JPR5. If separate output video and syncs are being employed to the Data Monitor, the noninverted serrated sync is connected to the horizontal sync input of the monitor. When an external video signal is input to the Graphics Display, an RSB is generated each time a horizontal sync pulse is detected by the sync separator circuit.

Vertical sync is provided by the line counter chain (U52,U62 and U33). Vertical sync occurs when L8 goes high as a result of the line count reaching 256 or an external vertical sync pulse is detected forcing L8 high. L8 is fed to U56 to provide serrated sync to be added to the video in the composite video output mode. For the separate video and syncs output mode, L8 is fed to an inverter (U23) through JPR1. The resulting L8 is connected to the vertical sync input of the Data Monitor. JPR5 is removed to omit sync pulses from the video output.

When composite external video is employed, the external video is fed to a comparator (U24) which removes the video and produces active low pulses corresponding to the external sync pulses. These pulses are inverted and fed to the D input of U46, the D input of U36 through the jumper between pins 3 and 15 of A1 and to the positive going trigger input of a one-shot with a 20us pulse width (U34). The horizontal and vertical sync pulses are separated by clocking the pulses through U46 and U57 to obtain an AUXRSB for each horizontal vertical sync pulse and clocking U36 with the rising edge of the active low 20us pulse. Since U36 is clocked 20us after the start of a sync pulse, only the vertical sync will be long enough to allow an AUXRSL to be generated. AUXRSL is fed to U67 to reset the line counters and to U33 to force L8 high and begin the vertical sync. The clears to U46 and U57 prevent generating more than one RSB for each external sync.

For the separate external video and sync mode the horizontal sync (EXHSYN) is fed to U68 and, for positive horizontal sync pulses, inverted by omitting JPR3. The horizontal sync generation is then the same as for composite external video. The external vertical sync (EXVSYN) is applied to another section of U68 and inverted for negative sync pulses by omitting JPR4. These pulses are then fed to the D input of U36 through the jumper between pins 3 and 14 of A1. U36 will now be clocked by LCLK through the jumper between pins 5 and 13 of A1. Now AUXRSL will be generated at the end of the line following the start of the external vertical sync pulse.

Light Pen Circuitry

Light is detected by the phototransistor (Q1) and converted to active low pulses which trigger a flip-flop (U57) to produce the signal FOUND. FOUND latches the present values of the line and bit counters into U54, U55, U64 and U65. U55 and U64 latch the line count and the tri-state outputs are enabled when PSEL Ø is high and PSEL 1 is low. U66 is a tri-state buffer that is enabled when PSEL 1 is high. Enabling U66 allows the status of FOUND, $\overline{SW}$, L8 and B5 to be input to the CPU. In addition to enabling the tri-state latches, PSEL Ø clears U57 when pulled low to ensure that FOUND is high only when light has been detected. PSEL Ø is also inverted and fed to U35 along with $\overline{WHITE}$ to generate $\overline{BLACK}$ which will black the screen.

IV. SPECIFICATIONS

Display Area	Square, 256 × 256 point display, 65,536 points total.
Memory	8K bytes on-board. This memory can be used for programs or data when not being used for graphics.
External Sync	Inputs for synchronizing to an external devise. Outputs for synchronizing an external device such as the TVC-64 or the Digital Group Data Monitor.
Graphics Boards per system	Unlimited.
Video Mixer	Selects TV readout, graphics, or superimposed.
Light Pen	Pen location to one dot resolution with software supplied.

Requirements:

Power	+5V at 1.5A +12V at .3A -5V at 5ma
	Video Monitor
	One Output Port to command board options
	One Input Port to accept Light Pen data and board status
	One memory slot in system

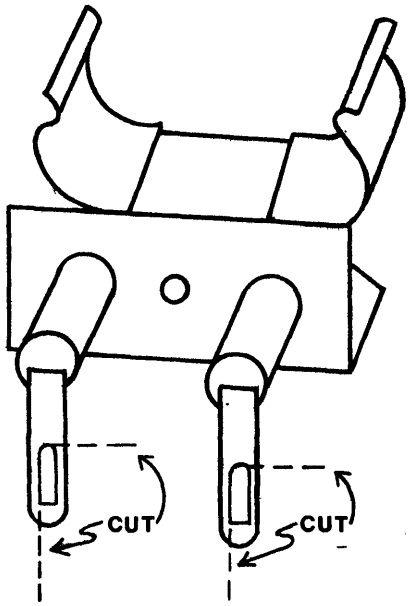
V.CONSTRUCTION

A. Graphics Display Board

1. Refer to the Parts List and Parts Layout in the Appendix when assembling the Graphics Display. Ensure all the components are present.

2. Insert the one 8-pin, thirty-three 14-pin, twenty-four 16-pin and sixteen 18-pin IC sockets. Place a book or other flat object over the sockets and invert the board. Carefully solder all pins, being alert not to cause "solder bridges" between pins or nearby traces.

3. Cut the tabs on the crystal holder as indicated in the Crystal Socket Preparation Detail below. Solder the crystal socket in place.



CRYSTAL SOCKET PREPARATION DETAIL

4. Solder the two 220 ohm, 1 watt resistors in place. Cut the leads close to the board.

5. Solder the sixteen .01 ufd disc bypass capacitors in place. Cut the leads close to the board.

6. Solder the eight .1 ufd disc bypass capacitors in place. Cut the leads close to the board.

7. Insert and solder the two .001 ufd disc, one 750 pfd, five 1 ufd and two 4.7 ufd capacitors. Note the polarity for the 1 ufd and 4.7 ufd capacitors marked on the board. The positive lead is marked by a + sign or a blue dot. Cut the leads close to the board.

8. Insert and solder the sixteen ¼W resistors. Cut the leads close to the board. R21 is not included as this is an optional part for use on systems without a -5V supply.

9. Insert and solder the two 5K ohm variable resistors. Be sure the slots for adjusting are toward the top edge of the board. Cut the leads close to the board.

10. Insert and solder CR1 (1N4148). Cut the leads close to the board.

11. Insert and solder the 75 ohm, ¼ watt resistor (Rt) in the paddle card. This resistor terminates the video. Cut the leads.

12. Measure the resistance between each power supply voltage pin and ground. Ground is pin 2 of the edge connector, +5V is pin 1, +12V is pin 36, -5V is pin B and -12V is pin R. +5V will read approximately 200 ohms on a DVM or a VOM on R×10 or greater. The others should read 400 ohms or greater.

13. Install the crystal and all IC's except the memory chips. Plug the board into your system and check the supply voltages on the board. Check that +12V at the memory chips is on pin 10 only, -5V on pin 1 and ground on pin 18. This step may prevent damaging the memory IC's.

14. Refer to the set up and operation section and install the address and video jumpers. For the initial chek out, jumper the address to an unused memory area.

15. Install the memory IC's and test the memory by running a memory test program or by using a memory editor. If the board fails the memory check, refer to the Troubleshooting Section.

16. Check that the video is synchronized and that the control bits (Graph, INV, etc.) operate properly. Refer to the Troubleshooting Section if any problems are encountered.

B. Light Pen

1. Refer to the Parts List and Parts Layout in the Appendix. Ensure that all parts are present.

2. Insert and solder the ten ¼watt resistors. Cut the leads close to the board.

3. Insert and solder the one 1 ufd tantalum capacitor. Note the polarity marked on the board. The positive lead of the capacitor is marked by either a + sign or a dot. Cut the leads close to the board.

4. Insert and solder the two .033 ufd disc capacitors. Cut the leads close to the board.

5. Insert and solder the one 2N5139 and two 2N5129 transistors. Cut the leads close to the board.

6. Insert and solder the LED. Orient the cathode toward the bottom of the board. (The cathode is marked by a notch in the body of the LED or by a longer lead). The anode is connected to +5V. Seat the body of the LED against the circuit board, otherwise it may contact the Light Pen case causing misalignment of the circuit board inside the tube. Cut the leads close to the board.

7. Refer to the Light Pen Construction diagram in Figure 10 before installing the phototransistor. If the phototransistor is installed too close to the circuit board, the operation of the Light Pen will be effected since detection of light as it passes over the hole in the end cap is diminished. The emitter lead (nearest the tab) is connected to hole number 2, the base to the center hole, and the collector to hole number 1.

8. Insert and solder the pushbutton switch. Seat the switch against the circuit board.

9. Solder one end of the cable to the holes (3 through 6) at the end of the board. Secure the cable to the board with a small cable tie.

10. Push the free end of the cable through the hole in the flat end cap so that the smaller diameter section is toward the circuit board. Refer to the Light Pen Construction in Figure 10.

11. Slide the Light Pen body over the circuit board. Align the small hole in the side of the body over the switch.

12. Insert the 3/16" roll pin in the pushbutton. Insert the other end of the roll pin into the hole in the top of the switch so that the pushbutton has freedom of movement in the hole of the Light Pen case.

13. Carefully place the rounded end cap over the phototransistor. Ensure that the transistor is parallel to the plane of the circuit board and centered within the opening in the end cap. The tab on the transistor may need to be cut for full penetration into the end cap. Align the slot in the end cap with the circuit board.

14. Push the flat end cap into the Light Pen body.

15. Refer to the Parts Layouts for the Paddle Card and Light Pen in the Appendix. Identify the wires in the cable by signal name as they were connected to the Light Pen. Solder each wire to the corresponding point on the Paddle Card.

16. Check the Light Pen operation using the Calibrate routine in the Appendix. If the operation is not correct, refer to the Troubleshooting section.

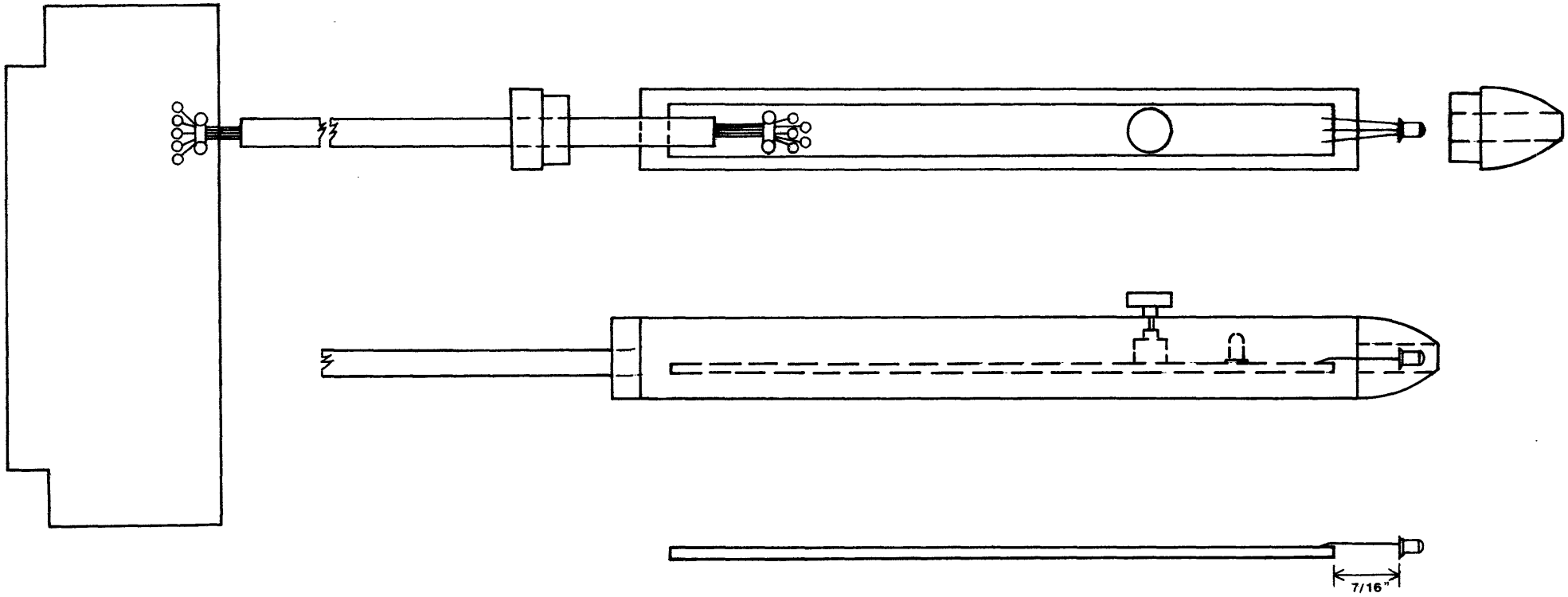


FIGURE 10. LIGHT PEN CONSTRUCTION

VI. TROUBLESHOOTING

A. General

Most problems with printed circuit boards are caused by construction errors. Therefore, the first step is to double-check all components for proper values, check for bent IC pins and solder bridges or splashes. Another problem source could be improper jumper configurations. Refer to the Set Up and Operation section and verify that all jumpers are proper for the mode of operation.

If no construcion errors are found, determine what area is malfunctioning and refer to the Block Diagram in the Appendix to determine associated areas that effect the problem area. The schematic is divided into areas corresponding to the functional blocks in the block diagram as an aid in troubleshooting. Reading the Theory of Operation and the Set Up and Operation sections and studying the Block Diagram and Timing Diagrams should enable you to find nearly any problem.

B. Memory Errors

1. Refer to the Block Diagram to determine the areas that effect the memory.
2. Check the clocks, CK1 and CK2. CK1 is 11.569 MHz and CK2 is 5.785 MHz.
3. Check for $\overline{\text{CPUREQ}}$ at U32. Ensure that the address jumpers are correct.
4. Check for chip enable (CE, CEEVEN. CEODD) and R/W.
5. Check the timing of B1—L7. These form the memory address during display and refresh.
6. Check DE to ensure the data to memory is being enabled.
7. Ensure that $\overline{\text{WHITE}}$ is high or the data from memory will always be FFH.

C. Video Output Problems

1. Refer to the Block Diagram to determine the areas that effect the video output.
2. Check that GRAPH is high or the display data will not be enabled to the video output.
3. Check the signals at U23, U27, U42, U43, and U68 in the video output circuit.
4. Check the inputs to and outputs from the shift registers.

D. Horizontal Sync Problems

1. Refer to the Block Diagram for areas that effect horizontal sync.
2. Check the sync generator circuitry for a 5us pulse at pin 12 of U34, RSB at pin 9 of U34 and B4, B5 and L8 at U56.
3. Ensure that the serrated sync is present at pin 8 of U56.

E. Vertical Sync Problems

1. Refer to the Block Diagram to determine which areas effect vertical sync.
2. Check for L8 at U56 in the composite video mode and L8 at pin 13 of U23 in the separate syncs mode.
3. Check the counter chain (LØ-L8).
4. Check that the vertical sync is present in the output video.

F. Sync Separator Problems (External video modes only)

1. Refer to the Block Diagram to determine the areas effecting the sync separator.
2. Ensure that the jumpers are correct for the mode of operation.
3. Verify that AUXRSB and AUXRSL are being generated.
4. Check that the 20us pulse is present at pin 4 of U34 and pin 11 of U36 in the composite video mode.
5. Check that LCLK is present at pin 11 of U36 in the separate syncs mode.
6. Check for SYNC at pin 12 of U46 and pin 12 of U36.

G. Light Pen Problems

1. Refer to the Block Diagram to determine which areas effect the Light Pen circuitry.
2. Verify that LIGHT is present at pin 5 of U57 and FOUND is generated.
3. Check that Bit Ø—L7 are present at U54, U55, U64, and U65.
4. Check that PSEL Ø and PSEL 1 are present and the 74173's are being enabled.
5. Check the status inputs and outputs at U66.
6. Ensure that the phototransistor is centered in the end of the Light Pen.

VII. APPENDIX

A. BLOCK DIAGRAM

B. TIMING DIAGRAMS

C. SAMPLE SOFTWARE ROUTINES

D. PARTS LIST

1. Graphics Display
2. Light Pen

E. DIGITAL GROUP BUS PIN ASSIGNMENTS

1. Memory Bus
2. I/O Bus
3. TVC Pin Out
4. Back Panel Connector Pin Out

F. CABLING DIAGRAMS

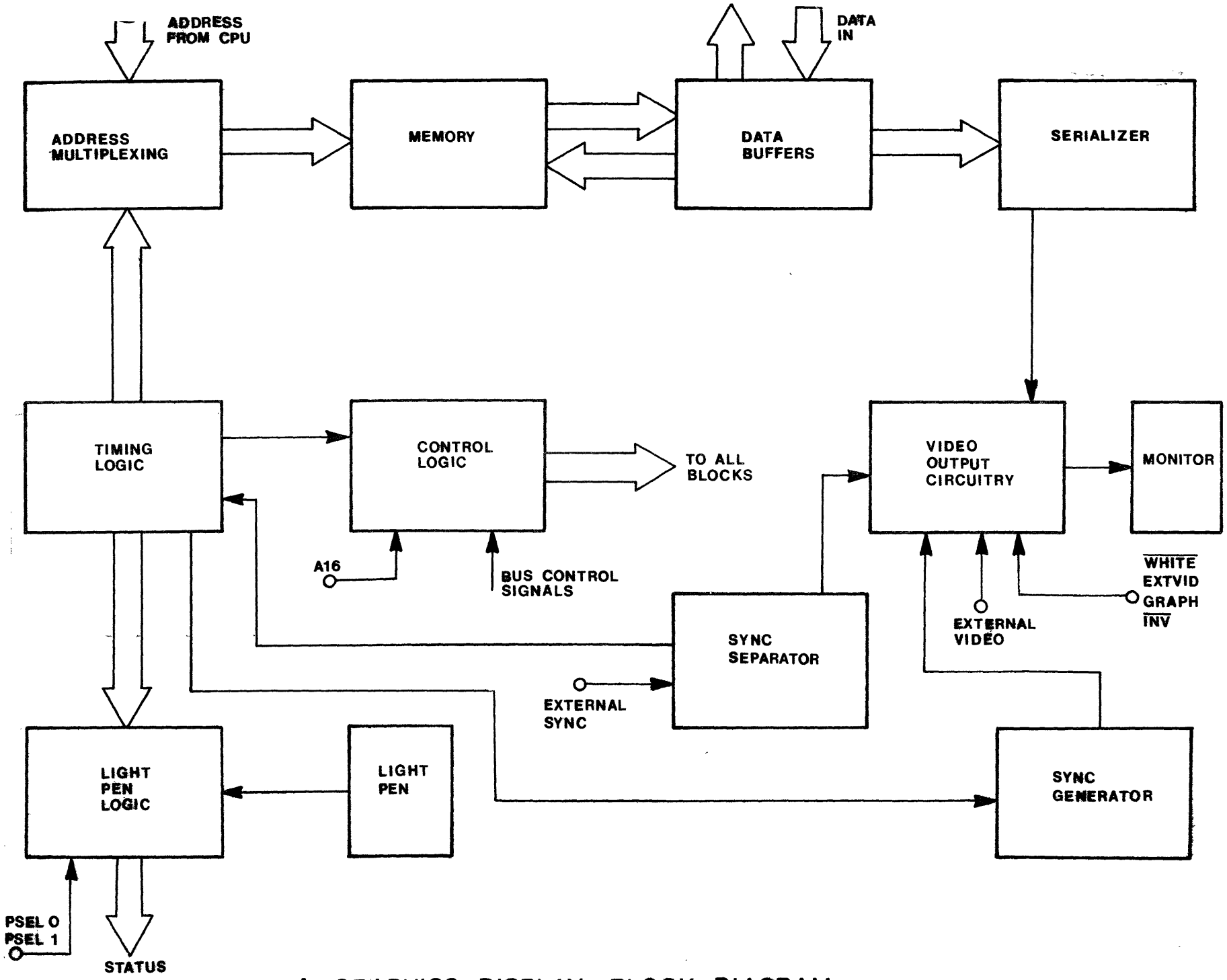
1. Graphics Control Cable Wire Diagram
2. Graph Input Cable Wire Diagram
3. Cable Orientation Diagrams

G. PARTS LAYOUT

1. Graphics Display Board
2. Light Pen

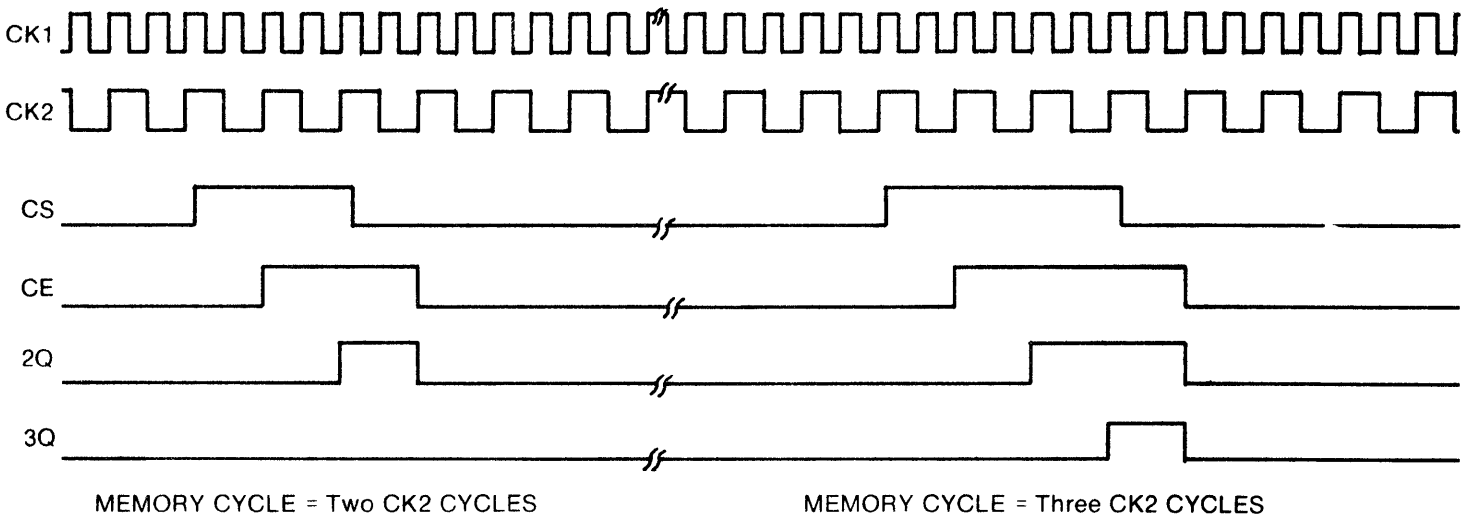
H. SCHEMATICS

1. Graphics Display Board
2. Light Pen

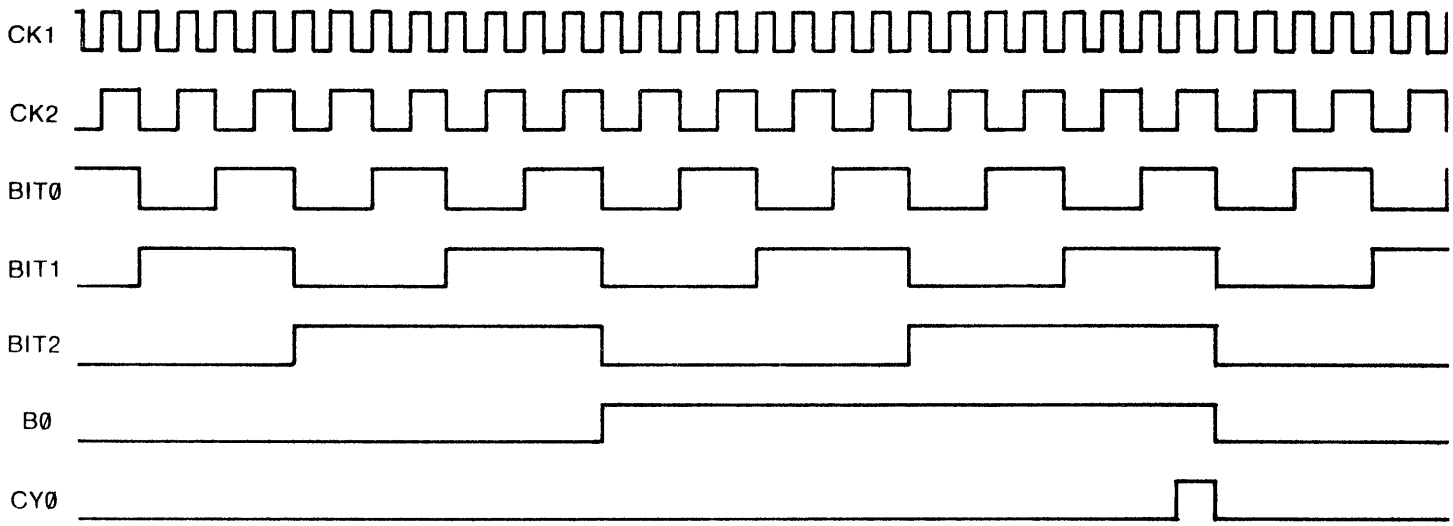


A. GRAPHICS DISPLAY, BLOCK DIAGRAM

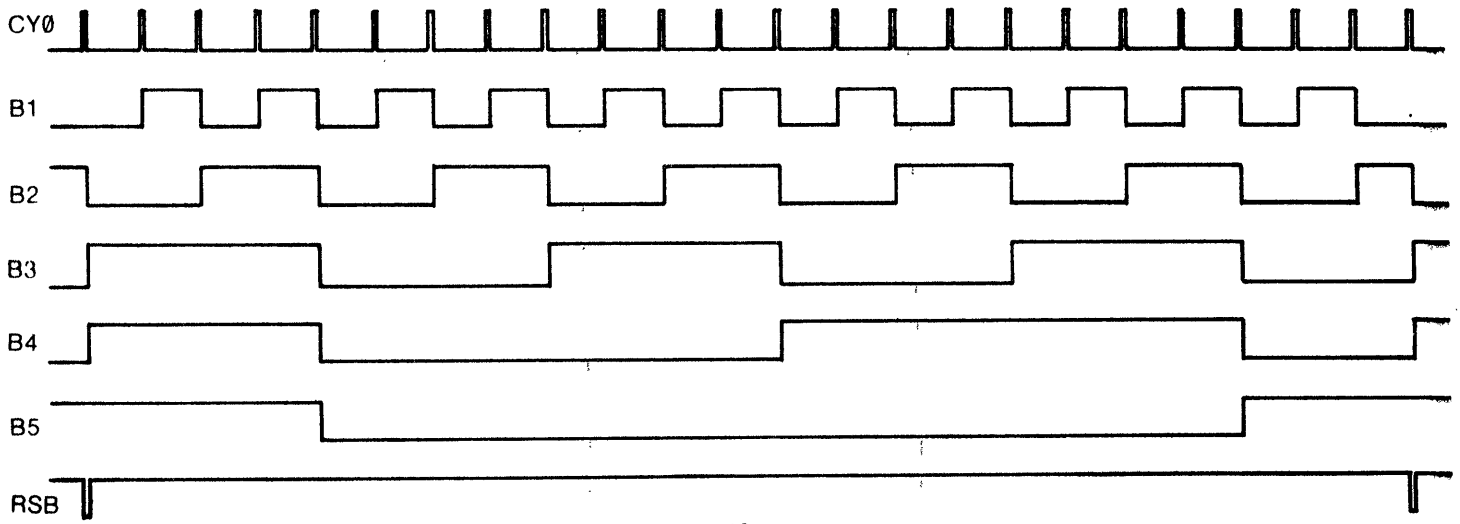
B.1 MEMORY CYCLE TIMING



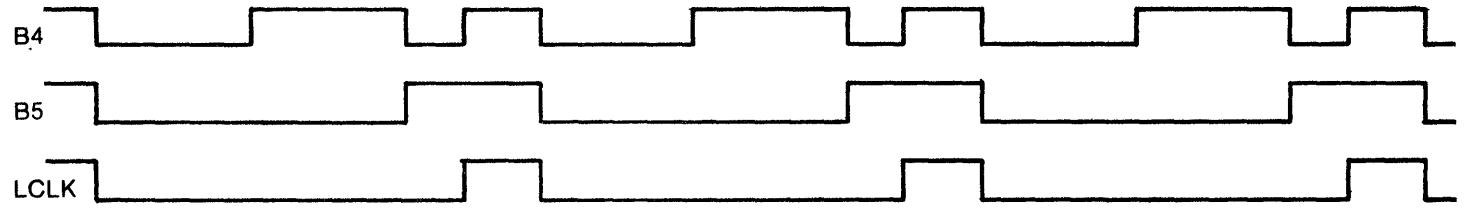
B.2 BIT COUNTER TIMING, BIT0-B0



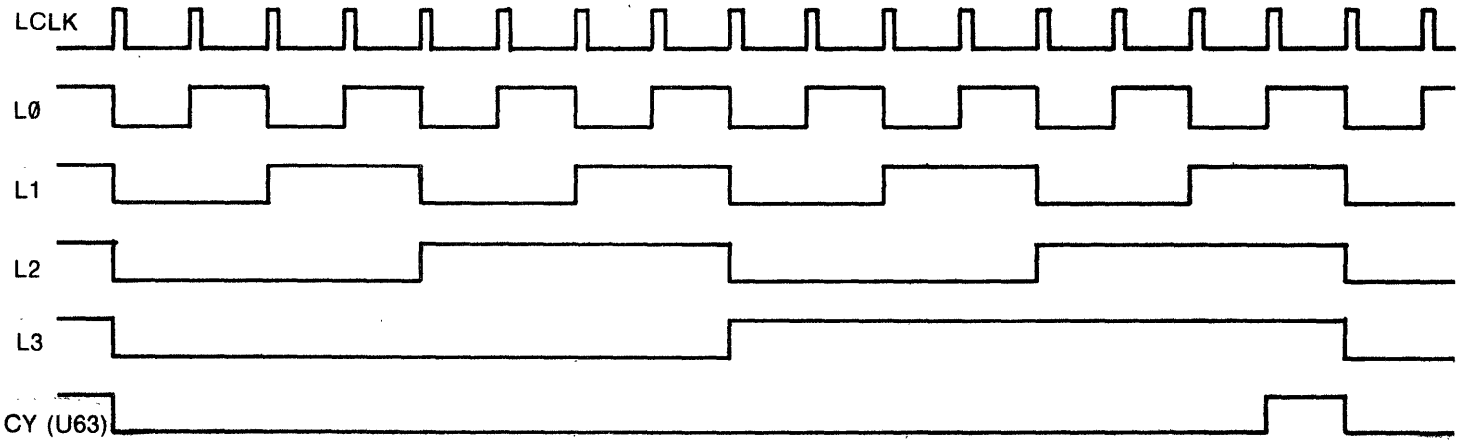
B.3 BIT COUNTER TIMING, B1-B5, RSB GENERATION



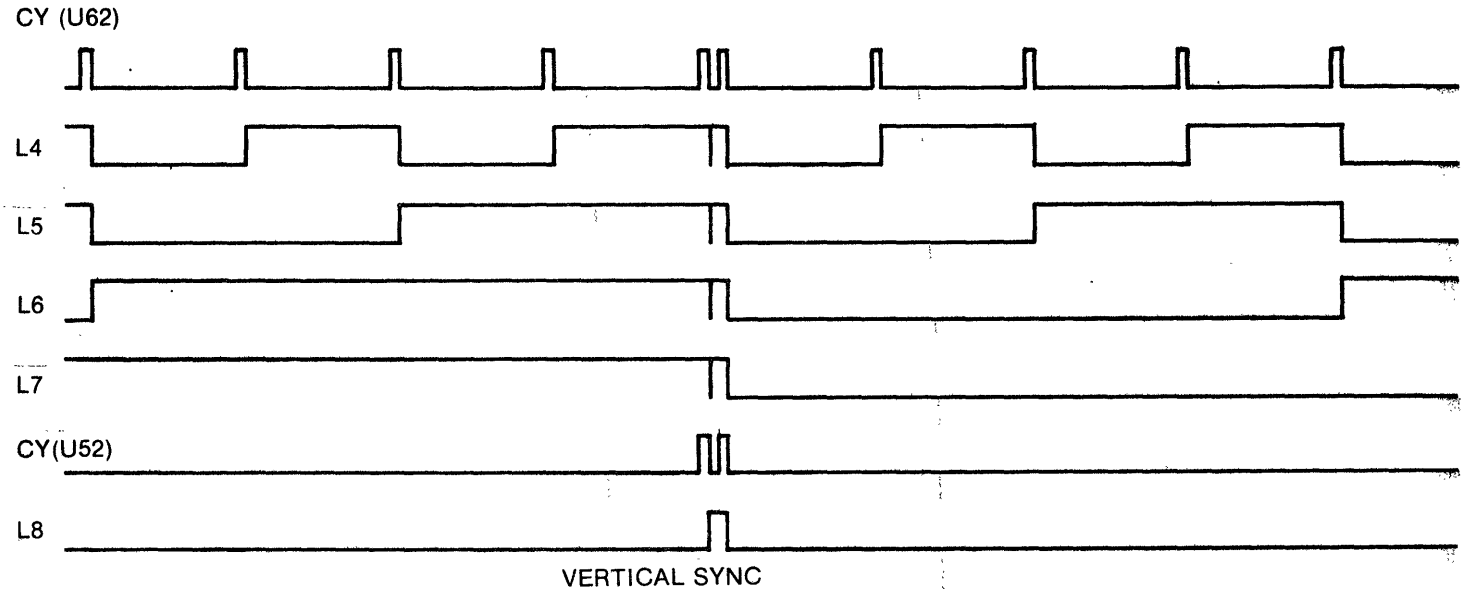
B.4 LCLK GENERATION



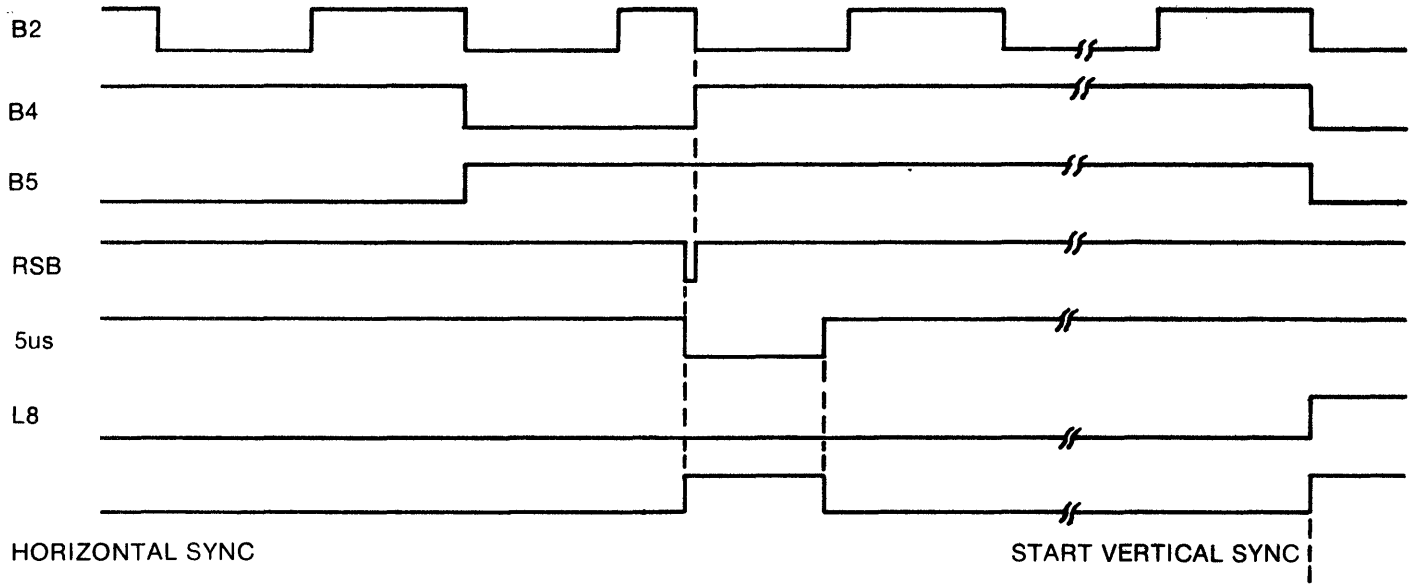
B.5 LINE COUNTER TIMING, LØ-L3



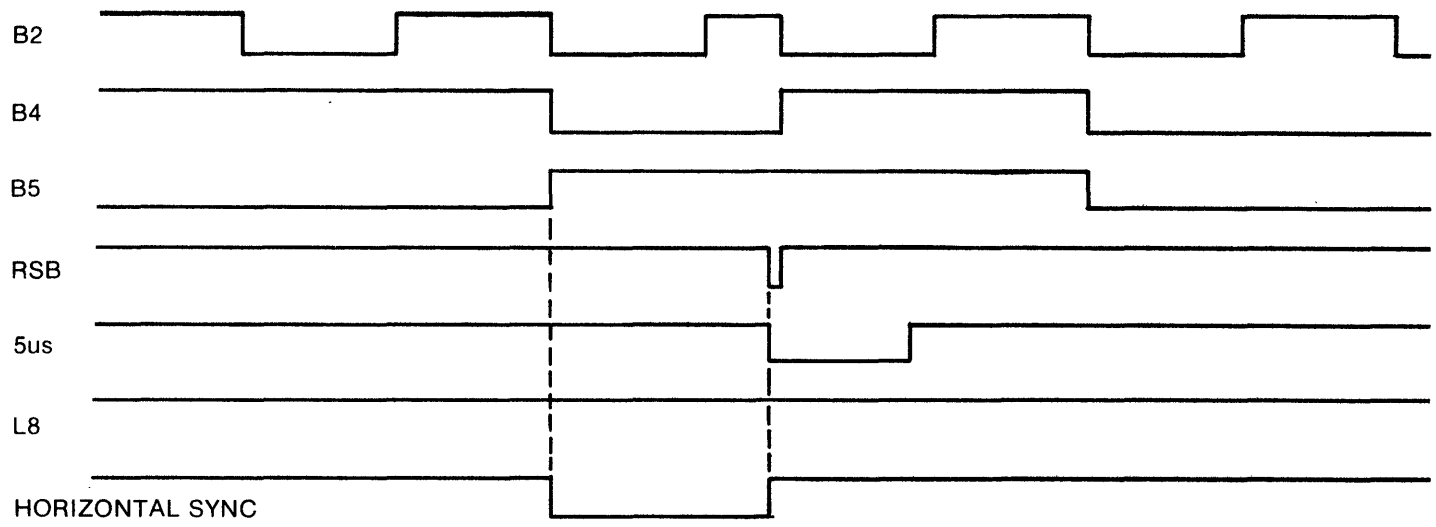
B.6 LINE COUNTER TIMING, L4-L8, VERTICAL SYNC GENERATION



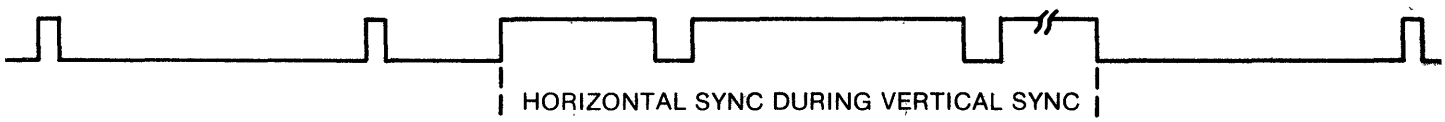
B.7 HORIZONTAL SYNC GENERATION—NO VERTICAL SYNC



B.8 HORIZONTAL SYNC GENERATION DURING VERTICAL SYNC



B.9 SERRATED SYNC



C. SAMPLE SOFTWARE ROUTINES

SOFTWARE INSTRUCTIONS

The Digital Group Graphics Board is supplied with the Basic software routines needed for plotting dots and lines. These routines will run with Basic or independently.

The Graphics Board is a bit mapped video device. Therefore each dot appearing on the screen is an address in memory serially fed to the video.

We have already written for you the algorithms necessary to convert these addresses into singly addressable coordinates. That is, to put a dot on the screen in the spot you want to, you do not have to find the sixteen bit address and enter a number with the appropriate bit on in it. Instead, you place two eight bit numbers in "X" and "Y" , a one in the "DE" and call "GETVAL" .

The following routines are on the tape you received with your board:

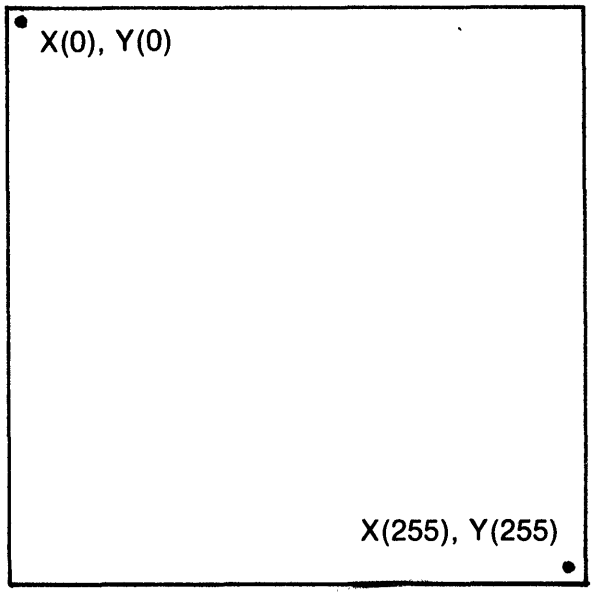
VALUE: Variable that points to the routine that you want to execute. All routines are called via the variable "VALUE", simply by placing the appropriate number into the "DE" register pair. Therefore these routines can be used with Basic or independently. These routines must be called via "GETVAL" or the stack will be destroyed.

THE VALUE	"0"	Turn off dot.
THE VALUE	"1"	Turn on dot.
THE VALUE	"2"	Compliment the dot (invert).
THE VALUE	"3"	Test the dot. Test returns a value in the HL register of Ø if dot was off,non Ø if dot was on.
THE VALUE	"4"	Plot a line with the dots off.
THE VALUE	"5"	Plot a line with the dots on.
THE VALUE	"6"	Calibrate the light pen.
THE VALUE	"7"	Continuously draw with the light pen.
THE VALUE	"8"	Locates the light pen and returns the two "X" and "Y" values.
THE VALUE	"9"	Clears the graphics buffer.
THE VALUE	"10"	Initializes the IO to the Graphics Board.

Description of each function

1. POINT: Allows you to plot single dots by an INVERTED CARTESIAN COORDINATE system, i.e. X=Ø to 255 and Y=Ø to 255. "X (0) " being the left hand side of the screen, "X (255) " being the right hand side of the screen and "Y (0) " being the top of the screen, "Y (255) " being the bottom of the screen.

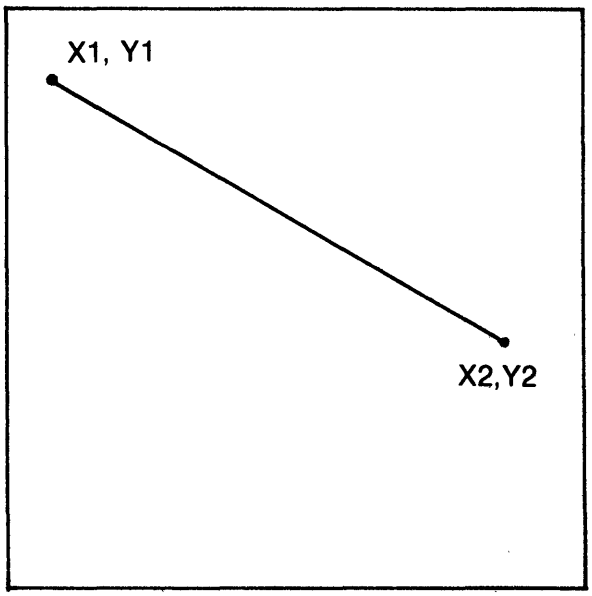
   EXAMPLE:



To place a dot at the coordinate you wish, you first have your program deposit the values for "X" and "Y" in the specified temporaries for point, place a one into the "DE" register, and call "GETVAL".

2. PLOT: Allows you to plot a line from one point on the graphics screen to another, E.G. X1, Y1 to X2, Y2. X1 being the starting value horizontally, Y1 being the starting value vertically. So therefore X2 is the ending value horizontally and Y2 the ending value vertically.

   EXAMPLE:



Place the starting and ending values for your line in the variables "X1", "X2", "Y1" and "Y2". Also be sure to place the appropriate number in "VALUE" to cause the line to be on or off.

3. CLEAR: Clears the screen.

4. CALIBRATE LIGHT PEN: This routine is set up to allow you to calibrate the light pen accurately to your own needs. More specifics on this routine are mentioned further on in the text.

5. LOCATE LIGHT PEN: Supplies the necessary software needed to interpret the location registers on the graphics board. This routine in turn can be used in conjunction with POINT or PLOT. The pen location is returned in "X" and "Y".

6. INITIALIZE: Sets up the Graphics Board IO. Documentation on the port assignments is in the hardware description. The board has an input socket that is plugged into a standard IO port. A hex FF will initialize the board so that you may see the graphics buffer.

Each of the routines listed here except "LOCATE", have their own set of variables that need to be set before calling.

POINT, PLOT and CLEAR all have to know where you have jumpered the graphics memory. **It is critical that you set "GRFST" (graphics start), before you execute any of these routines!!!**

For example, if you have jumpered the board for 8000 Hex, you will go into the monitor, go to the address that "GRFST" is and set it to "00 80". At that point all the routines know where your board is located. This can also be accomplished in Basic with the FILL command. The difference is Basic uses the decimal equivalent of the hexidecimal number mentioned previously.

USING THE CALIBRATE LIGHT PEN ROUTINE

Set "GRFST" to the location at which your board is jumpered. Least significant byte first, most significant byte last! Place a "6" into the "DE" register and call "GETVAL". A dot at the coordinates "80-80/HEX", the middle of the screen, will appear.

To calibrate the pen to place a dot under the pen, place the pen on your monitor screen over the dot, then press the button. The screen will then flash white, and adjust the brightness and contrast for the differences inherent in your monitor.

By adjusting the brightness and contrast on your monitor you can fine tune for best results.

The following is a list of all the variables and their functions:

GETVAL=(Ø6ØD)	Start of Graphics routines. You must always enter here by placing a value into the "DE" register and calling this address.
GRFST=(Ø8CB)	Page the graphics buffer starts on. All routines use this location.
X=(Ø8C5)	Horizontal parameter for point routine.
Y=(Ø8C7)	Vertical parameter for point routine.
X1=(Ø8C9)	First horizontal parameter of line for plot routine.
Y1=(Ø8CA)	First vertical parameter of line for plot routine.
X2=(Ø8F1)	Second horizontal parameter of line.
Y2=(Ø8F2)	Second vertical parameter of line.
VALUE=(Ø8C3)	Flag that vectors to the subroutines.
XOFF=(Ø8D2)	X offset for calibrate light pen routine.
YOFF=(Ø8D1)	Y offset for calibrate light pen routine.

The IO port assignments for this software are 7 for IN and 7 for OUT. These ports are used for the light pen registers and controlling the Graphics Board functions via software.

You do not need to hook up IO cables to your board if you don't want these functions. If you do and you don't have ports at the given locations you must change the port assignments in the software using the listing supplied.

Here are a few basic programs as examples:

HEX ROUTINES

Cassette Routine Parameters

READ 600-8F5

```
0600                    0100          ST    0600H
0600 C9                 0110          RET
0601 00                 0120          NOP
0602 00                 0130          NOP
0603 C9                 0140          RET
0604 00                 0150          NOP
0605 00                 0160          NOP
0606 C9                 0170          RET
0607 00                 0180          NOP
0608 00                 0190          NOP
0609 C9                 0200          RET
060A 00                 0210          NOP
060B 00                 0220          NOP
060C C9                 0230          RET
060D ED 53 C3 08        0240 GETVAL   LD    (VALUE),DE
0611 21 1F 06           0250          LD    HL,TAB
0614 3A C3 08           0260          LD    A,(VALUE)
0617 CB 17              0270          RL    A
0619 85                 0280          ADD   L
061A 6F                 0290          LD    L,A
061B 30 01              0300          JR    NC,MTAB
061D 24                 0310          INC   H
061E E9                 0320 MTAB     JP    (HL)
061F 18 14              0330 TAB      JR    OFF
0621 18 1E              0340          JR    ON
0623 18 25              0350          JR    CPL
0625 18 75              0360          JR    TEST
0627 18 6B              0370          JR    LOFF
0629 18 6D              0380          JR    LON
062B 18 2B              0390          JR    LCAL
062D 18 56              0400          JR    LDRAW
062F 18 58              0410          JR    LPEN
0631 18 5D              0420          JR    LCLEAR
0633 18 1E              0430          JR    LINIT
0635 CD 6C 08           0440 OFF      CALL  POINT
0638 3A CD 08           0450          LD    A,(HANDLE)
063B 4F                 0460          LD    C,A
063C 78                 0470          LD    A,B
063D 2F                 0480          CPL
063E A1                 0490          AND   C
063F 18 66              0500          JR    FINISH
0641 CD 6C 08           0510 ON       CALL  POINT
0644 3A CD 08           0520          LD    A,(HANDLE)
0647 B0                 0530          OR    B
0648 18 5D              0540          JR    FINISH
064A CD 6C 08           0550 CPL      CALL  POINT
064D 3A CD 08           0560          LD    A,(HANDLE)
0650 A8                 0570          XOR   B
0651 18 54              0580          JR    FINISH
0653 3E FF              0590 LINIT    LD    A,0FFH
0655 D3 07              0600          OUT   OPORT
0657 C9                 0610          RET
0658 97                 0620 LCAL     SUB   A
0659 32 D1 08           0630          LD    (YOFF),A
065C 32 D2 08           0640          LD    (XOFF),A
```

NOTE:

The tape supplied with the Graphics Board contains the code to be inserted from 0600H to 08FFH in MAXI BASIC. This can be done in the AUDIO version by changing the starting address located at 0118H to 00H, 0119H to 06H, and the ending address at 011AH to FFH and 011BH to 08H. After the code has been read into the correct locations, a new cassette can be written that will contain the new code as well as MAXI BASIC by option 2, WRITE CASSETTE.

```
065F 3E 80        0650          LD    A,80H
0661 32 C6 08     0660          LD    (X+1),A
0664 32 C8 08     0670          LD    (Y+1),A
0667 CD 41 06     0680          CALL  ON
066A CD AF 06     0690          CALL  STAT1
066D CD D1 06     0700          CALL  LOCATE
0670 3A C8 08     0710          LD    A,(Y+1)
0673 C6 80        0720          ADD   80H
0675 ED 44        0730          NEG
0677 32 D1 08     0740          LD    (YOFF),A
067A 3A C6 08     0750          LD    A,(X+1)
067D C6 80        0760          ADD   80H
067F ED 44        0770          NEG
0681 32 D2 08     0780          LD    (XOFF),A
0684 C9           0790          RET
0685 CD BE 06     0800 LDRAW    CALL  DRAW
0688 C9           0810          RET
0689 CD AF 06     0820 LPEN     CALL  STAT1
068C CD D1 06     0830          CALL  LOCATE
068F C9           0840          RET
0690 CD AC 08     0850 LCLEAR   CALL  CLRM
0693 C9           0860          RET
0694 CD 04 08     0870 LOFF     CALL  PLOT
0697 C9           0880          RET
0698 CD 04 08     0890 LON      CALL  PLOT
069B C9           0900          RET
069C 3A CD 08     0910 TEST     LD    A,(HANDLE)
069F B0           0920          OR    B
06A0 62           0930          LD    H,D
06A1 6F           0940          LD    L,A
06A2 28 0A        0950          JR    Z,FINYT
06A4 2C           0960          INC   L
06A5 18 07        0970          JR    FINYT
06A7 2A CF 08     0980 FINISH   LD    HL,(NHAN)
06AA 77           0990          LD    (HL),A
06AB 2A C3 08     1000 FINNT    LD    HL,(VALUE)
06AE C9           1010 FINYT    RET
06AF DB 00        1020 STAT1    IN    KEY
06B1 FE 91        1030          CP    91H
06B3 C8           1040          RET   Z
06B4 FE 83        1050          CP    83H
06B6 C8           1060          RET   Z
06B7 DB 07        1070          IN    IPORT
06B9 CB 67        1080          BIT   4,A
06BB 20 F2        1090          JR    NZ,STAT1
06BD C9           1100          RET
06BE DB 07        1110 DRAW     IN    IPORT
06C0 CB 67        1120          BIT   4,A
06C2 20 06        1130          JR    NZ,DRAW1
06C4 CD D1 06     1140          CALL  LOCATE
06C7 CD 41 06     1150          CALL  ON
06CA DB 00        1160 DRAW1    IN    KEY
06CC FE 91        1170          CP    91H
06CE C8           1180          RET   Z
06CF 18 ED        1190          JR    DRAW
06D1              1200 LOCATE   EQU   $
06D1 3E FE        1210 CSTART   LD    A,0FEH      CLR FOUND,STROBE STATUS,WHITE
06D3              1220 *                          OFF,LED OFF,BLACK ON
06D3 D3 07        1230          OUT   OPORT
06D5 3C           1240 BLKOFF   INC   A           BLACK OFF
```

```
06D6 D3 07        1250         OUT   OPORT
06D8 DB 07        1260 L8      IN    IPORT
06DA CB 77        1270         BIT   6,A          L8=1?
06DC 28 FA        1280         JR    Z,L8
06DE 3E 7B        1290 L8CON   LD    A,7BH
06E0 D3 07        1300         OUT   OPORT
06E2 5F           1310         LD    E,A
06E3 06 00        1320         LD    B,0          INITIALIZE COUNT
06E5 0E 07        1330         LD    C,IPORT
06E7 16 40        1340         LD    D,40H        L8 MASK
06E9 21 F2 08     1350         LD    HL,USTACK-1
06EC              1360 *
06EC              1370 *
06EC              1380 ******** LOOK FOR RETRACE TIME *********
06EC DB 07        1390 L8NOT   IN    IPORT
06EE A2           1400         AND   D
06EF 20 FB        1410         JR    NZ,L8NOT
06F1 18 11        1420         JR    STAT2
06F3              1430 ****** GET LIGHT PEN LOCATIONS ********
06F3 3E 78        1440 INPOS   LD    A,78H
06F5 D3 07        1450         OUT   OPORT
06F7 ED AA        1460         IND
06F9 3C           1470         INC   A            STROBE 01
06FA D3 07        1480         OUT   OPORT
06FC ED AA        1490         IND
06FE 3E E0        1500         LD    A,0E0H
0700 90           1510         SUB   B
0701 CA D1 06     1520         JP    Z,CSTART
0704 7B           1530 STAT2   LD    A,E          STATUS STROBE
0705 D3 07        1540         OUT   OPORT
0707 ED 78        1550 STAT2X  IN    A,(C)
0709 FA F3 06     1560         JP    M,INPOS       FOUND=1?
070C A2           1570         AND   D             NO,L8=1?
070D CA 07 07     1580         JP    Z,STAT2X     NO
0710 3E 7F        1590 STXCON  LD    A,7FH
0712 D3 07        1600         OUT   OPORT
0714 3E F9        1610         LD    A,0F9H
0716 B8           1620         CP    B
0717 FA D1 06     1630         JP    M,CSTART
071A              1640 ****** INITIALIZE TO COMPUTE DOT LOCATIONS ******
071A 78           1650 COMP    LD    A,B           CALCULATE NUMBER OF POINTS
071B CB 2F        1660         SRA   A
071D 2F           1670         CPL
071E 32 F3 08     1680         LD    (NPTS),A
0721              1690 * MOST X CORD 00---, OR 11---
0721 21 EF 08     1700 CK      LD    HL,USTACK-4
0724 3A F3 08     1710         LD    A,(NPTS)
0727 47           1720         LD    B,A
0728 0E 00        1730         LD    C,0
072A 7E           1740 CK1     LD    A,(HL)
072B E6 C0        1750         AND   0C0H
072D 28 05        1760         JR    Z,CK2
072F EE C0        1770         XOR   0C0H
0731 28 01        1780         JR    Z,CK2
0733 0C           1790         INC   C
0734 2B           1800 CK2     DEC   HL          MORE TO NEXT X
0735 2B           1810         DEC   HL
0736 10 F2        1820         DJNZ  CK1         NOT DONE
0738 3A F3 08     1830         LD    A,(NPTS)
073B CB 3F        1840         SRL   A
```

```
073D 91           1850         SUB  C        POS IF MOSTLY 00XXXX,11XXXXX
073E 97           1860         SUB  A
073F FA 53 07     1870         JP   M,CK3    MOSTLY 01XXXXX,10XXXXX (HAD JR M)
0742              1880 *   XOR ALL X WITH 1000-0000
0742 21 EF 08     1890         LD   HL,USTACK-4
0745 3A F3 08     1900         LD   A,(NPTS)
0748 47           1910         LD   B,A
0749 7E           1920 CK4     LD   A,(HL)
074A EE 80        1930         XOR  80H
074C 77           1940         LD   (HL),A
074D 2B           1950         DEC  HL
074E 2B           1960         DEC  HL
074F 10 F8        1970         DJNZ CK4
0751 3E 01        1980         LD   A,1
0753 32 F4 08     1990 CK3     LD   (FLAG),A
0756 3E 80        2000         LD   A,128D      INIT AVERAGES
0758 32 C6 08     2010         LD   (XAVG),A
075B 32 C8 08     2020         LD   (YAVG),A
075E 32 F5 08     2030         LD   (DIST),A
0761 CD 93 07     2040         CALL AVRG
0764 3E 20        2050         LD   A,32D        TOSS IF >32
0766 32 F5 08     2060         LD   (DIST),A
0769              2070 *
0769 CD 93 07     2080         CALL AVRG
076C 3E 05        2090         LD   A,5
076E              2100 *
076E 7B           2110         LD   A,E          > THAN 4 SAMPLES ?
076F D6 05        2120         SUB  5
0771 FA D1 06     2130         JP   M,CSTART
0774 3A C8 08     2140         LD   A,(YAVG)     ADD OFFSET
0777 47           2150         LD   B,A
0778 3A D1 08     2160         LD   A,(YOFF)
077B 80           2170         ADD  B
077C 32 C8 08     2180         LD   (YAVG),A
077F 3A F4 08     2190         LD   A,(FLAG)      INVERT BIT 7
0782 B7           2200         OR   A
0783 3A C6 08     2210         LD   A,(XAVG)      ADD X OFFSET
0786 28 02        2220         JR   Z,OFF1        NO
0788 EE 80        2230         XOR  80H
078A 47           2240 OFF1    LD   B,A
078B 3A D2 08     2250         LD   A,(XOFF)
078E 80           2260         ADD  B
078F 32 C6 08     2270         LD   (XAVG),A
0792 C9           2280         RET
0793              2290 *
0793              2300 *
0793              2310 *
0793 16 00        2320 AVRG    LD   D,0          INIT
0795 4A           2330         LD   C,D
0796 0D           2340         DEC  C
0797 DD 21 00 00  2350         LD   IX,0
079B FD 21 00 00  2360         LD   IY,0
079F 21 F0 08     2370         LD   HL,USTACK-3
07A2 3A F3 08     2380         LD   A,(NPTS)
07A5 47           2390         LD   B,A
07A6 5E           2400 AVRG2   LD   E,(HL)
07A7 2B           2410         DEC  HL
07A8 3A C8 08     2420         LD   A,(YAVG)
07AB 93           2430         SUB  E
07AC 30 02        2440         JR   NC,AVRG1       ABSOLUTE VALUE
```

```
07AE ED 44        2450         NEG
07B0 5F           2460 AVRG1   LD   E,A
07B1 3A F5 08     2470         LD   A,(DIST)
07B4 93           2480         SUB  E                 OUT OF RANGE ?
07B5 38 1B        2490         JR   C,AVRG3           YES
07B7 5E           2500         LD   E,(HL)            CHECK X VALUE
07B8 3A C6 08     2510         LD   A,(XAVG)
07BB 93           2520         SUB  E
07BC 30 02        2530         JR   NC,AVRG4           ABSOLUTE VALUE
07BE ED 44        2540         NEG
07C0 5F           2550 AVRG4   LD   E,A
07C1 3A F5 08     2560         LD   A,(DIST)
07C4 93           2570         SUB  E                  OUT RANGE ?
07C5 38 0B        2580         JR   C,AVRG3            YES
07C7 0C           2590         INC  C                    INCREMENT N
07C8 28 08        2600         JR   Z,AVRG3              TOSS FIRST DOT
07CA 23           2610         INC  HL
07CB 5E           2620         LD   E,(HL)             SUM Y
07CC FD 19        2630         ADD  IY,DE
07CE 2B           2640         DEC  HL
07CF 5E           2650         LD   E,(HL)             SUM X
07D0 DD 19        2660         ADD  IX,DE
07D2              2670 *
07D2 2B           2680 AVRG3   DEC  HL
07D3 10 D1        2690         DJNZ AVRG2              NOT DONE
07D5 59           2700         LD   E,C                YAVG = IY/N
07D6 FD E5        2710         PUSH IY
07D8 E1           2720         POP  HL
07D9 CD EB 07     2730         CALL DIV
07DC 78           2740         LD   A,B
07DD 32 C8 08     2750         LD   (YAVG),A
07E0 DD E5        2760         PUSH IX                 XAVG = IX/N
07E2 E1           2770         POP  HL                 VERY SHARP ALLAN
07E3 CD EB 07     2780         CALL DIV
07E6 78           2790         LD   A,B
07E7 32 C6 08     2800         LD   (XAVG),A
07EA C9           2810         RET
07EB              2820 * B=HL/E
07EB 53           2830 DIV     LD   D,E
07EC AF           2840         XOR  A          CLEAN A
07ED 06 08        2850         LD   B,8D       DO 8 TIMES
07EF 4F           2860         LD   C,A
07F0 5F           2870         LD   E,A
07F1 CB 21        2880 DIV3    SLA  C          SHIFT C, CLEAN CARRY
07F3 CB 3A        2890         SRL  D
07F5 CB 1B        2900         RR   E
07F7 ED 52        2910         SBC  HL,DE
07F9 F2 FF 07     2920         JP   P,DIV1
07FC 19           2930         ADD  HL,DE
07FD 18 01        2940         JR   DIV2
07FF 0C           2950 DIV1    INC  C
0800 10 EF        2960 DIV2    DJNZ DIV3
0802 41           2970         LD   B,C
0803 C9           2980         RET
0804              2990 *PLOT & POINT*
0804 3A F2 08     3000 PLOT    LD   A,(Y2TEMP)         GET SECOND Y VECTOR
0807 67           3010         LD   H,A                PUT IT IN H REG
0808 3A CA 08     3020         LD   A,(Y1TEMP)         GET FIRST Y VECTER
080B 94           3030         SUB  H                  SUBTRACT Y2 FROM Y1
080C 47           3040         LD   B,A                PUT Y DIS/256 IN DELTA Y
```

```
080D 3E 00        3050          LD   A,0            CLEAR ACCUMULATOR
080F 30 01        3060          JR   NC,L2          JUMP IF THERE WAS NO BORROW
0811 2F           3070          CPL                 CORRECT SIGN OF HB IF IT WAS NE
0812 4F           3080 L2       LD   C,A            FIXED DELTA Y+1
0813 3A F1 08     3090          LD   A,(X2TEMP)     GET SECOND X VECTOR
0816 67           3100          LD   H,A            PUT IT IN H REG
0817 3A C9 08     3110          LD   A,(X1TEMP)     GET FIRST X VECTER
081A 94           3120          SUB  H              SUBTRACT X2 FROM X1
081B 57           3130          LD   D,A            PUT X DIS/256 IN DELTA X
081C 3E 00        3140          LD   A,0            CLEAR ACCUMULATOR
081E 30 01        3150          JR   NC,L3          JUMP IF THERE WAS NO BORROW
0820 2F           3160          CPL                 CORRECT SIGN OF HB IF IT WAS NE
0821 5F           3170 L3       LD   E,A            FIXED DELTA X+1
0822 21 00 00     3180          LD   HL,0           START COUNTER ANEW
0825 22 C5 08     3190          LD   (X),HL         THIS IS TO CLEAR THE LOW BYTE
0828 22 C7 08     3200          LD   (Y),HL         ONLY,BUT TO SAVE BYTES CLEAR BO
082B 3A F2 08     3210          LD   A,(Y2TEMP)     PRESET X+1 & Y+1
082E 32 C8 08     3220          LD   (Y+1),A        TO THE FIRST POINT WE WILL PLOT
0831 3A F1 08     3230          LD   A,(X2TEMP)
0834 32 C6 08     3240          LD   (X+1),A        SAME HERE
0837 C5           3250 JPOINT   PUSH BC             SAVE DELTA Y
0838 D5           3260          PUSH DE             SAVE DELTA X
0839 E5           3270          PUSH HL             SAVE THE COUNTER
083A 3A C3 08     3280          LD   A,(VALUE)
083D FE 04        3290          CP   4
083F 28 05        3300          JR   Z,PL2
0841 CD 41 06     3310          CALL ON
0844 18 03        3320          JR   PPOINT
0846 CD 35 06     3330 PL2      CALL OFF
0849 E1           3340 PPOINT   POP  HL
084A D1           3350          POP  DE             RESTORE DELTA X
084B C1           3360          POP  BC             RESTORE DELTA Y
084C 3A C7 08     3370 FADD     LD   A,(Y)          GET Y
084F 80           3380          ADD  B              MOVE Y ONE POINT BY ADDING 1/25
0850 32 C7 08     3390          LD   (Y),A          PUT IT BACK IN Y
0853 3A C8 08     3400          LD   A,(Y+1)        GET Y+1
0856 89           3410          ADC  C              ADC DELTA Y+1
0857 32 C8 08     3420          LD   (Y+1),A        PUT RESULT BACK IN Y+1
085A 3A C5 08     3430 SEADD    LD   A,(X)          GET X
085D 82           3440          ADD  D              MOVE X 1 POINT BY +1/256 OF DIS
085E 32 C5 08     3450          LD   (X),A          PUT RESULT BACK IN X
0861 3A C6 08     3460          LD   A,(X+1)        GET X+1
0864 8B           3470          ADC  E              ADC DELTA X+1
0865 32 C6 08     3480          LD   (X+1),A        PUT RESULT BACK IN X+1
0868 2D           3490          DEC  L              START THE COUNT
0869 20 CC        3500          JR   NZ,JPOINT      PLOT ALL 256 TO SAVE TIME
086B C9           3510 RETURN   RET
086C 2A CB 08     3520 POINT    LD   HL,(GRFST)     BEGINING OF POINT ROUTINE
086F ED 5B C8 08  3530 YCOUNT   LD   DE,(Y+1)       FIRST GET GRAFICS BUFFER
0873 16 00        3540          LD   D,0            THEN Y+1.NOW CLEAR D REG.
0875 B7           3550          OR   A              CLEAR CARRY FLAG
0876 CB 13        3560          RL   E              MULTIPLY THE DE REG.
0878 CB 12        3570          RL   D              BY 32 TO GIVE US OUR
087A CB 13        3580          RL   E              LINE COUNT.THIS SUBR.
087C CB 12        3590          RL   D              MOVES THE COUNT BY 32
087E CB 13        3600          RL   E              WHICH IS THE NUMBER OF
0880 CB 12        3610          RL   D              BYTES IN A LINE
0882 CB 13        3620          RL   E
0884 CB 12        3630          RL   D
0886 CB 13        3640          RL   E
```

```
0888 CB 12        3650         RL   D            NOW ADD GRFST TO NUMBER
088A 19           3660         ADD  HL,DE        LINES TO GET Y
088B E5           3670 XCOUNT  PUSH HL           BEGIN X COUNT ROUTINE
088C 3A C6 08     3680         LD   A,(X+1)      GET X
088F 4F           3690         LD   C,A          STORE IT IN C REG.
0890 E6 07        3700         AND  07H          GET LAST 3 BITS
0892 21 BB 08     3710         LD   HL,TABLE     GET ADDR. OF TABLE
0895 85           3720 XLOOP   ADD  L            ADD L TO A TO GET OFFSET
0896 6F           3730         LD   L,A          PUT OFFSET IN L REG.
0897 30 01        3740         JR   NC,MORE      IF CARRY WE KNOW THE BIT
0899 24           3750         INC  H
089A 46           3760 MORE    LD   B,(HL)       LOAD B REG. BYTE
089B 79           3770         LD   A,C          GET OLD X
089C 0F           3780         RRCA              DIVIDE IT BY 8
089D 0F           3790         RRCA
089E 0F           3800         RRCA
089F E6 1F        3810         AND  1FH          GET LAST 5 BITS
08A1 E1           3820         POP  HL           GET LINE COUNT
08A2 85           3830         ADD  L            ADD LOW LINE COUNT TO A
08A3 6F           3840         LD   L,A          PUT ADDR. IN L REG.
08A4 7E           3850         LD   A,(HL)       PUT ADDR. IN A
08A5 32 CD 08     3860         LD   (HANDLE),A PUT IT IN A TEMP
08A8 22 CF 08     3870         LD   (NHAN),HL
08AB C9           3880         RET
08AC              3890 *ROUTINE TO CLEAR THE SCREEN*
08AC ED 5B CB 08  3900 CLRM    LD   DE,(GRFST)     GET ADDR. OF GRAPHICS BUFF.
08B0 62           3910         LD   H,D
08B1 6B           3920         LD   L,E
08B2 01 FF 1F     3930         LD   BC,8191D
08B5 97           3940         SUB  A
08B6 12           3950         LD   (DE),A
08B7 13           3960         INC  DE
08B8 ED B0        3970         LDIR
08BA C9           3980         RET
08BB              3990 TABLE   DB   80H            TABLE FOR BIT MASKS FOR POINT
  80
08BC              4000         DB   40H            ROUTINE
  40
08BD              4010         DB   20H
  20
08BE              4020         DB   10H
  10
08BF              4030         DB   08H
  08
08C0              4040         DB   04H
  04
08C1              4050         DB   02H
  02
08C2              4060         DB   01H
  01
08C3              4070 VALUE   DS   2
08C5              4080 X       DS   2
08C7              4090 Y       DS   2
08C9              4100 X1TEMP  DS   1
08CA              4110 Y1TEMP  DS   1
08CB              4120 GRFST   DS   2
08CD              4130 HANDLE  DS   2
08CF              4140 NHAN    DS   2
08D1              4150 YOFF    DS   1
08D2              4160 XOFF    DS   1
```

```
08D3                4170 OPORT   EQU  7
08D3                4180 IPORT   EQU  7
08D3                4190 KEY     EQU  0
08D3                4200 STACK   DS   32D
08F3                4210 USTACK  EQU  $
08F3                4220 NPTS    DS   1
08F4                4230 FLAG    DS   1
08F5                4240 XAVG    EQU  X+1
08F5                4250 YAVG    EQU  Y+1
08F5                4260 X2TEMP  EQU  USTACK-2
08F5                4270 Y2TEMP  EQU  USTACK-1
08F5                4280 DIST    DS   1
```

LTABLE

AVRG	0793	AVRG1	07B0	AVRG2	07A6	AVRG3	07D2
AVRG4	07C0	BLKOFF	06D5	CK	0721	CK1	072A
CK2	0734	CK3	0753	CK4	0749	CLRM	08AC
COMP	071A	CPL	064A	CSTART	06D1	DIST	08F5
DIV	07EB	DIV1	07FF	DIV2	0800	DIV3	07F1
DRAW	06BE	DRAW1	06CA	FADD	084C	FINISH	06A7
FINNT	06AB	FINYT	06AE	FLAG	08F4	GETVAL	060D
GRFST	08CB	HANDLE	08CD	INPOS	06F3	IPORT	0007
JPOINT	0837	KEY	0000	L2	0812	L3	0821
L8	06D8	L8CON	06DE	L8NOT	06EC	LCAL	0658
LCLEAR	0690	LDRAW	0685	LINIT	0653	LOCATE	06D1
LOFF	0694	LON	0698	LPEN	0689	MORE	089A
MTAB	061E	NHAN	08CF	NPTS	08F3	OFF	0635
OFF1	078A	ON	0641	OPORT	0007	PL2	0846
PLOT	0804	POINT	086C	PPOINT	0849	RETURN	086B
SEADD	085A	STACK	08D3	STAT1	06AF	STAT2	0704
STAT2X	0707	STXCON	0710	TAB	061F	TABLE	08BB
TEST	069C	USTACK	08F3	VALUE	08C3	X	08C5
X1TEMP	08C9	X2TEMP	08F1	XAVG	08C6	XCOUNT	088B
XLOOP	0895	XOFF	08D2	Y	08C7	Y1TEMP	08CA
Y2TEMP	08F2	YAVG	08C8	YCOUNT	086F	YOFF	08D1

OCTAL ROUTINES

Cassette Routine Parameters
READ 6000-10365

```
006000                          0100          ST    0600H
006000 311                      0110          RET
006001 000                      0120          NOP
006002 000                      0130          NOP
006003 311                      0140          RET
006004 000                      0150          NOP
006005 000                      0160          NOP
006006 311                      0170          RET
006007 000                      0180          NOP
006010 000                      0190          NOP
006011 311                      0200          RET
006012 000                      0210          NOP
006013 000                      0220          NOP
006014 311                      0230          RET
006015 355 123 303 010          0240 GETVAL   LD    (VALUE),DE
006021 041 037 006              0250          LD    HL,TAB
006024 072 303 010              0260          LD    A,(VALUE)
006027 313 027                  0270          RL    A
006031 205                      0280          ADD   L
006032 157                      0290          LD    L,A
006033 060 001                  0300          JR    NC,MTAB
006035 044                      0310          INC   H
006036 351                      0320 MTAB     JP    (HL)
006037 030 024                  0330 TAB      JR    OFF
006041 030 036                  0340          JR    ON
006043 030 045                  0350          JR    CPL
006045 030 165                  0360          JR    TEST
006047 030 153                  0370          JR    LOFF
006051 030 155                  0380          JR    LON
006053 030 053                  0390          JR    LCAL
006055 030 126                  0400          JR    LDRAW
006057 030 130                  0410          JR    LPEN
006061 030 135                  0420          JR    LCLEAR
006063 030 036                  0430          JR    LINIT
006065 315 154 010              0440 OFF      CALL  POINT
006070 072 315 010              0450          LD    A,(HANDLE)
006073 117                      0460          LD    C,A
006074 170                      0470          LD    A,B
006075 057                      0480          CPL
006076 241                      0490          AND   C
006077 030 146                  0500          JR    FINISH
006101 315 154 010              0510 ON       CALL  POINT
006104 072 315 010              0520          LD    A,(HANDLE)
006107 260                      0530          OR    B
006110 030 135                  0540          JR    FINISH
006112 315 154 010              0550 CPL      CALL  POINT
006115 072 315 010              0560          LD    A,(HANDLE)
006120 250                      0570          XOR   B
006121 030 124                  0580          JR    FINISH
006123 076 377                  0590 LINIT    LD    A,0FFH
006125 323 007                  0600          OUT   OPORT
006127 311                      0610          RET
006130 227                      0620 LCAL     SUB   A
006131 062 321 010              0630          LD    (YOFF),A
006134 062 322 010              0640          LD    (XOFF),A
```

```
006137 076 200          0650          LD    A,80H
006141 062 306 010      0660          LD    (X+1),A
006144 062 310 010      0670          LD    (Y+1),A
006147 315 101 006      0680          CALL  ON
006152 315 257 006      0690          CALL  STAT1
006155 315 321 006      0700          CALL  LOCATE
006160 072 310 010      0710          LD    A,(Y+1)
006163 306 200          0720          ADD   80H
006165 355 104          0730          NEG
006167 062 321 010      0740          LD    (YOFF),A
006172 072 306 010      0750          LD    A,(X+1)
006175 306 200          0760          ADD   80H
006177 355 104          0770          NEG
006201 062 322 010      0780          LD    (XOFF),A
006204 311              0790          RET
006205 315 276 006      0800 LDRAW    CALL  DRAW
006210 311              0810          RET
006211 315 257 006      0820 LPEN     CALL  STAT1
006214 315 321 006      0830          CALL  LOCATE
006217 311              0840          RET
006220 315 254 010      0850 LCLEAR   CALL  CLRM
006223 311              0860          RET
006224 315 004 010      0870 LOFF     CALL  PLOT
006227 311              0880          RET
006230 315 004 010      0890 LON      CALL  PLOT
006233 311              0900          RET
006234 072 315 010      0910 TEST     LD    A,(HANDLE)
006237 260              0920          OR    B
006240 142              0930          LD    H,D
006241 157              0940          LD    L,A
006242 050 012          0950          JR    Z,FINYT
006244 054              0960          INC   L
006245 030 007          0970          JR    FINYT
006247 052 317 010      0980 FINISH   LD    HL,(NHAN)
006252 167              0990          LD    (HL),A
006253 052 303 010      1000 FINNT    LD    HL,(VALUE)
006256 311              1010 FINYT    RET
006257 333 000          1020 STAT1    IN    KEY
006261 376 221          1030          CP    91H
006263 310              1040          RET   Z
006264 376 203          1050          CP    83H
006266 310              1060          RET   Z
006267 333 007          1070          IN    IPORT
006271 313 147          1080          BIT   4,A
006273 040 362          1090          JR    NZ,STAT1
006275 311              1100          RET
006276 333 007          1110 DRAW     IN    IPORT
006300 313 147          1120          BIT   4,A
006302 040 006          1130          JR    NZ,DRAW1
006304 315 321 006      1140          CALL  LOCATE
006307 315 101 006      1150          CALL  ON
006312 333 000          1160 DRAW1    IN    KEY
006314 376 221          1170          CP    91H
006316 310              1180          RET   Z
006317 030 355          1190          JR    DRAW
006321                  1200 LOCATE   EQU   $
006321 076 376          1210 CSTART   LD    A,0FEH      CLR FOUND,STROBE STATUS,WHITE
006323                  1220 *                          OFF,LED OFF,BLACK ON
006323 323 007          1230          OUT   OPORT
006325 074              1240 BLKOFF   INC   A           BLACK OFF
```

```
006326 323 007          1250         OUT  OPORT
006330 333 007          1260 L8      IN   IPORT
006332 313 167          1270         BIT  6,A          L8=1?
006334 050 372          1280         JR   Z,L8
006336 076 173          1290 L8CON   LD   A,7BH
006340 323 007          1300         OUT  OPORT
006342 137              1310         LD   E,A
006343 006 000          1320         LD   B,0          INITIALIZE COUNT
006345 016 007          1330         LD   C,IPORT
006347 026 100          1340         LD   D,40H        L8 MASK
006351 041 362 010      1350         LD   HL,USTACK-1
006354                  1360 *
006354                  1370 *
006354                  1380 ******** LOOK FOR RETRACE TIME *********
006354 333 007          1390 L8NOT   IN   IPORT
006356 242              1400         AND  D
006357 040 373          1410         JR   NZ,L8NOT
006361 030 021          1420         JR   STAT2
006363                  1430 ****** GET LIGHT PEN LOCATIONS ********
006363 076 170          1440 INPOS   LD   A,78H
006365 323 007          1450         OUT  OPORT
006367 355 252          1460         IND
006371 074              1470         INC  A            STROBE 01
006372 323 007          1480         OUT  OPORT
006374 355 252          1490         IND
006376 076 340          1500         LD   A,0E0H
007000 220              1510         SUB  B
007001 312 321 006      1520         JP   Z,CSTART
007004 173              1530 STAT2   LD   A,E          STATUS STROBE
007005 323 007          1540         OUT  OPORT
007007 355 170          1550 STAT2X  IN   A,(C)
007011 372 363 006      1560         JP   M,INPOS       FOUND=1?
007014 242              1570         AND  D             NO,L8=1?
007015 312 007 007      1580         JP   Z,STAT2X     NO
007020 076 177          1590 STXCON  LD   A,7FH
007022 323 007          1600         OUT  OPORT
007024 076 371          1610         LD   A,0F9H
007026 270              1620         CP   B
007027 372 321 006      1630         JP   M,CSTART
007032                  1640 ****** INITIALIZE TO COMPUTE DOT LOCATIONS ******
007032 170              1650 COMP    LD   A,B           CALCULATE NUMBER OF POINTS
007033 313 057          1660         SRA  A
007035 057              1670         CPL
007036 062 363 010      1680         LD   (NPTS),A
007041                  1690 * MOST X CORD 00---, OR 11---
007041 041 357 010      1700 CK      LD   HL,USTACK-4
007044 072 363 010      1710         LD   A,(NPTS)
007047 107              1720         LD   B,A
007050 016 000          1730         LD   C,0
007052 176              1740 CK1     LD   A,(HL)
007053 346 300          1750         AND  0C0H
007055 050 005          1760         JR   Z,CK2
007057 356 300          1770         XOR  0C0H
007061 050 001          1780         JR   Z,CK2
007063 014              1790         INC  C
007064 053              1800 CK2     DEC  HL         MORE TO NEXT X
007065 053              1810         DEC  HL
007066 020 362          1820         DJNZ CK1        NOT DONE
007070 072 363 010      1830         LD   A,(NPTS)
007073 313 077          1840         SRL  A
```

```
007075 221                1850          SUB  C        POS IF MOSTLY 00XXXX,11XXXXX
007076 227                1860          SUB  A
007077 372 123 007        1870          JP   M,CK3    MOSTLY 01XXXXX,10XXXXX (HAD JR M)
007102                    1880 *   XOR ALL X WITH 1000-0000
007102 041 357 010        1890          LD   HL,USTACK-4
007105 072 363 010        1900          LD   A,(NPTS)
007110 107                1910          LD   B,A
007111 176                1920 CK4      LD   A,(HL)
007112 356 200            1930          XOR  80H
007114 167                1940          LD   (HL),A
007115 053                1950          DEC  HL
007116 053                1960          DEC  HL
007117 020 370            1970          DJNZ CK4
007121 076 001            1980          LD   A,1
007123 062 364 010        1990 CK3      LD   (FLAG),A
007126 076 200            2000          LD   A,128D       INIT AVERAGES
007130 062 306 010        2010          LD   (XAVG),A
007133 062 310 010        2020          LD   (YAVG),A
007136 062 365 010        2030          LD   (DIST),A
007141 315 223 007        2040          CALL AVRG
007144 076 040            2050          LD   A,32D         TOSS IF >32
007146 062 365 010        2060          LD   (DIST),A
007151                    2070 *
007151 315 223 007        2080          CALL AVRG
007154 076 005            2090          LD   A,5
007156                    2100 *
007156 173                2110          LD   A,E           > THAN 4 SAMPLES ?
007157 326 005            2120          SUB  5
007161 372 321 006        2130          JP   M,CSTART
007164 072 310 010        2140          LD   A,(YAVG)      ADD OFFSET
007167 107                2150          LD   B,A
007170 072 321 010        2160          LD   A,(YOFF)
007173 200                2170          ADD  B
007174 062 310 010        2180          LD   (YAVG),A
007177 072 364 010        2190          LD   A,(FLAG)       INVERT BIT 7
007202 267                2200          OR   A
007203 072 306 010        2210          LD   A,(XAVG)       ADD X OFFSET
007206 050 002            2220          JR   Z,OFF1         NO
007210 356 200            2230          XOR  80H
007212 107                2240 OFF1     LD   B,A
007213 072 322 010        2250          LD   A,(XOFF)
007216 200                2260          ADD  B
007217 062 306 010        2270          LD   (XAVG),A
007222 311                2280          RET
007223                    2290 *
007223                    2300 *
007223                    2310 *
007223 026 000            2320 AVRG     LD   D,0           INIT
007225 112                2330          LD   C,D
007226 015                2340          DEC  C
007227 335 041 000 000    2350          LD   IX,0
007233 375 041 000 000    2360          LD   IY,0
007237 041 360 010        2370          LD   HL,USTACK-3
007242 072 363 010        2380          LD   A,(NPTS)
007245 107                2390          LD   B,A
007246 136                2400 AVRG2    LD   E,(HL)
007247 053                2410          DEC  HL
007250 072 310 010        2420          LD   A,(YAVG)
007253 223                2430          SUB  E
007254 060 002            2440          JR   NC,AVRG1        ABSOLUTE VALUE
```

```
007256 355 104          2450          NEG
007260 137              2460 AVRG1    LD    E,A
007261 072 365 010      2470          LD    A,(DIST)
007264 223              2480          SUB   E                  OUT OF RANGE ?
007265 070 033          2490          JR    C,AVRG3            YES
007267 136              2500          LD    E,(HL)             CHECK X VALUE
007270 072 306 010      2510          LD    A,(XAVG)
007273 223              2520          SUB   E
007274 060 002          2530          JR    NC,AVRG4            ABSOLUTE VALUE
007276 355 104          2540          NEG
007300 137              2550 AVRG4    LD    E,A
007301 072 365 010      2560          LD    A,(DIST)
007304 223              2570          SUB   E                   OUT RANGE ?
007305 070 013          2580          JR    C,AVRG3             YES
007307 014              2590          INC   C                     INCREMENT N
007310 050 010          2600          JR    Z,AVRG3               TOSS FIRST DOT
007312 043              2610          INC   HL
007313 136              2620          LD    E,(HL)               SUM Y
007314 375 031          2630          ADD   IY,DE
007316 053              2640          DEC   HL
007317 136              2650          LD    E,(HL)               SUM X
007320 335 031          2660          ADD   IX,DE
007322                  2670 *
007322 053              2680 AVRG3    DEC   HL
007323 020 321          2690          DJNZ  AVRG2                NOT DONE
007325 131              2700          LD    E,C                  YAVG = IY/N
007326 375 345          2710          PUSH  IY
007330 341              2720          POP   HL
007331 315 353 007      2730          CALL  DIV
007334 170              2740          LD    A,B
007335 062 310 010      2750          LD    (YAVG),A
007340 335 345          2760          PUSH  IX                 XAVG = IX/N
007342 341              2770          POP   HL                 VERY SHARP ALLAN
007343 315 353 007      2780          CALL  DIV
007346 170              2790          LD    A,B
007347 062 306 010      2800          LD    (XAVG),A
007352 311              2810          RET
007353                  2820 * B=HL/E
007353 123              2830 DIV      LD    D,E
007354 257              2840          XOR   A          CLEAN A
007355 006 010          2850          LD    B,8D       DO 8 TIMES
007357 117              2860          LD    C,A
007360 137              2870          LD    E,A
007361 313 041          2880 DIV3     SLA   C          SHIFT C, CLEAN CARRY
007363 313 072          2890          SRL   D
007365 313 033          2900          RR    E
007367 355 122          2910          SBC   HL,DE
007371 362 377 007      2920          JP    P,DIV1
007374 031              2930          ADD   HL,DE
007375 030 001          2940          JR    DIV2
007377 014              2950 DIV1     INC   C
010000 020 357          2960 DIV2     DJNZ  DIV3
010002 101              2970          LD    B,C
010003 311              2980          RET
010004                  2990 *PLOT & POINT*
010004 072 362 010      3000 PLOT     LD    A,(Y2TEMP)         GET SECOND Y VECTOR
010007 147              3010          LD    H,A                PUT IT IN H REG
010010 072 312 010      3020          LD    A,(Y1TEMP)        GET FIRST Y VECTER
010013 224              3030          SUB   H                 SUBTRACT Y2 FROM Y1
010014 107              3040          LD    B,A               PUT Y DIS/256 IN DELTA Y
```

```
010015 076 000          3050         LD   A,0            CLEAR ACCUMULATOR
010017 060 001          3060         JR   NC,L2          JUMP IF THERE WAS NO BORROW
010021 057              3070         CPL                 CORRECT SIGN OF HB IF IT WA
010022 117              3080 L2      LD   C,A            FIXED DELTA Y+1
010023 072 361 010      3090         LD   A,(X2TEMP)     GET SECOND X VECTOR
010026 147              3100         LD   H,A            PUT IT IN H REG
010027 072 311 010      3110         LD   A,(X1TEMP)     GET FIRST X VECTER
010032 224              3120         SUB  H              SUBTRACT X2 FROM X1
010033 127              3130         LD   D,A            PUT X DIS/256 IN DELTA X
010034 076 000          3140         LD   A,0            CLEAR ACCUMULATOR
010036 060 001          3150         JR   NC,L3          JUMP IF THERE WAS NO BORROW
010040 057              3160         CPL                 CORRECT SIGN OF HB IF IT WA
010041 137              3170 L3      LD   E,A            FIXED DELTA X+1
010042 041 000 000      3180         LD   HL,0           START COUNTER ANEW
010045 042 305 010      3190         LD   (X),HL         THIS IS TO CLEAR THE LOW BY
010050 042 307 010      3200         LD   (Y),HL         ONLY,BUT TO SAVE BYTES CLEA
010053 072 362 010      3210         LD   A,(Y2TEMP)     PRESET X+1 & Y+1
010056 062 310 010      3220         LD   (Y+1),A        TO THE FIRST POINT WE WILL
010061 072 361 010      3230         LD   A,(X2TEMP)
010064 062 306 010      3240         LD   (X+1),A        SAME HERE
010067 305              3250 JPOINT  PUSH BC             SAVE DELTA Y
010070 325              3260         PUSH DE             SAVE DELTA X
010071 345              3270         PUSH HL             SAVE THE COUNTER
010072 072 303 010      3280         LD   A,(VALUE)
010075 376 004          3290         CP   4
010077 050 005          3300         JR   Z,PL2
010101 315 101 006      3310         CALL ON
010104 030 003          3320         JR   PPOINT
010106 315 065 006      3330 PL2     CALL OFF
010111 341              3340 PPOINT  POP  HL
010112 321              3350         POP  DE             RESTORE DELTA X
010113 301              3360         POP  BC             RESTORE DELTA Y
010114 072 307 010      3370 FADD    LD   A,(Y)          GET Y
010117 200              3380         ADD  B              MOVE Y ONE POINT BY ADDING
010120 062 307 010      3390         LD   (Y),A          PUT IT BACK IN Y
010123 072 310 010      3400         LD   A,(Y+1)        GET Y+1
010126 211              3410         ADC  C              ADC DELTA Y+1
010127 062 310 010      3420         LD   (Y+1),A        PUT RESULT BACK IN Y+1
010132 072 305 010      3430 SEADD   LD   A,(X)          GET X
010135 202              3440         ADD  D              MOVE X 1 POINT BY +1/256 OR
010136 062 305 010      3450         LD   (X),A          PUT RESULT BACK IN X
010141 072 306 010      3460         LD   A,(X+1)        GET X+1
010144 213              3470         ADC  E              ADC DELTA X+1
010145 062 306 010      3480         LD   (X+1),A        PUT RESULT BACK IN X+1
010150 055              3490         DEC  L              START THE COUNT
010151 040 314          3500         JR   NZ,JPOINT      PLOT ALL 256 TO SAVE TIME
010153 311              3510 RETURN  RET
010154 052 313 010      3520 POINT   LD   HL,(GRFST)     BEGINING OF POINT ROUTINE
010157 355 133 310 010  3530 YCOUNT  LD   DE,(Y+1)       FIRST GET GRAFICS BUFFER
010163 026 000          3540         LD   D,0            THEN Y+1.NOW CLEAR D REG.
010165 267              3550         OR   A              CLEAR CARRY FLAG
010166 313 023          3560         RL   E              MULTIPLY THE DE REG.
010170 313 022          3570         RL   D              BY 32 TO GIVE US OUR
010172 313 023          3580         RL   E              LINE COUNT.THIS SUBR.
010174 313 022          3590         RL   D              MOVES THE COUNT BY 32
010176 313 023          3600         RL   E              WHICH IS THE NUMBER OF
010200 313 022          3610         RL   D              BYTES IN A LINE
010202 313 023          3620         RL   E
010204 313 022          3630         RL   D
010206 313 023          3640         RL   E
```

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010210 313 022          3650         RL   D            NOW ADD GRFST TO NUMBER
010212 031              3660         ADD  HL,DE        LINES TO GET Y
010213 345              3670 XCOUNT  PUSH HL           BEGIN X COUNT ROUTINE
010214 072 306 010      3680         LD   A,(X+1)      GET X
010217 117              3690         LD   C,A          STORE IT IN C REG.
010220 346 007          3700         AND  07H          GET LAST 3 BITS
010222 041 273 010      3710         LD   HL,TABLE     GET ADDR. OF TABLE
010225 205              3720 XLOOP   ADD  L           ADD L TO A TO GET OFFSET
010226 157              3730         LD   L,A          PUT OFFSET IN L REG.
010227 060 001          3740         JR   NC,MORE      IF CARRY WE KNOW THE BIT
010231 044              3750         INC  H
010232 106              3760 MORE    LD   B,(HL)       LOAD B REG. BYTE
010233 171              3770         LD   A,C          GET OLD X
010234 017              3780         RRCA              DIVIDE IT BY 8
010235 017              3790         RRCA
010236 017              3800         RRCA
010237 346 037          3810         AND  1FH          GET LAST 5 BITS
010241 341              3820         POP  HL           GET LINE COUNT
010242 205              3830         ADD  L            ADD LOW LINE COUNT TO A
010243 157              3840         LD   L,A          PUT ADDR. IN L REG.
010244 176              3850         LD   A,(HL)       PUT ADDR. IN A
010245 062 315 010      3860         LD   (HANDLE),A PUT IT IN A TEMP
010250 042 317 010      3870         LD   (NHAN),HL
010253 311              3880         RET
010254                  3890 *ROUTINE TO CLEAR THE SCREEN*
010254 355 133 313 010  3900 CLRM    LD   DE,(GRFST)     GET ADDR. OF GRAPHICS BUFF.
010260 142              3910         LD   H,D
010261 153              3920         LD   L,E
010262 001 377 037      3930         LD   BC,8191D
010265 227              3940         SUB  A
010266 022              3950         LD   (DE),A
010267 023              3960         INC  DE
010270 355 260          3970         LDIR
010272 311              3980         RET
010273                  3990 TABLE   DB   80H            TABLE FOR BIT MASKS FOR POINT
  200
010274                  4000         DB   40H            ROUTINE
  100
010275                  4010         DB   20H
  040
010276                  4020         DB   10H
  020
010277                  4030         DB   08H
  010
010300                  4040         DB   04H
  004
010301                  4050         DB   02H
  002
010302                  4060         DB   01H
  001
010303                  4070 VALUE   DS   2
010306                  4080 X       DS   2
010310                  4090 Y       DS   2
010311                  4100 X1TEMP  DS   1
010312                  4110 Y1TEMP  DS   1
010313                  4120 GRFST   DS   2
010315                  4130 HANDLE  DS   2
010317                  4140 NHAN    DS   2
010321                  4150 YOFF    DS   1
010322                  4160 XOFF    DS   1
```

```
010323                  4170 OPORT   EQU  7
010323                  4180 IPORT   EQU  7
010323                  4190 KEY     EQU  0
010323                  4200 STACK   DS   32D
010363                  4210 USTACK  EQU  $
010363                  4220 NPTS    DS   1
010364                  4230 FLAG    DS   1
010365                  4240 XAVG    EQU  X+1
010365                  4250 YAVG    EQU  Y+1
010365                  4260 X2TEMP  EQU  USTACK-2
010365                  4270 Y2TEMP  EQU  USTACK-1
010365                  4280 DIST    DS   1
```

LTABLE

AVRG	007223	AVRG1	007260	AVRG2	007246	AVRG3	007322
AVRG4	007300	BLKOFF	006325	CK	007041	CK1	007052
CK2	007064	CK3	007123	CK4	007111	CLRM	010254
COMP	007032	CPL	006112	CSTART	006321	DIST	010365
DIV	007353	DIV1	007377	DIV2	010000	DIV3	007361
DRAW	006276	DRAW1	006312	FADD	010114	FINISH	006247
FINNT	006253	FINYT	006256	FLAG	010364	GETVAL	006015
GRFST	010313	HANDLE	010315	INPOS	006363	IPORT	000007
JPOINT	010067	KEY	000000	L2	010022	L3	010041
L8	006330	L8CON	006336	L8NOT	006354	LCAL	006130
LCLEAR	006220	LDRAW	006205	LINIT	006123	LOCATE	006321
LOFF	006224	LON	006230	LPEN	006211	MORE	010232
MTAB	006036	NHAN	010317	NPTS	010363	OFF	006065
OFF1	007212	ON	006101	OPORT	000007	PL2	010106
PLOT	010004	POINT	010154	PPOINT	010111	RETURN	010153
SEADD	010132	STACK	010323	STAT1	006257	STAT2	007004
STAT2X	007007	STXCON	007020	TAB	006037	TABLE	010273
TEST	006234	USTACK	010363	VALUE	010303	X	010306
X1TEMP	010311	X2TEMP	010361	XAVG	010306	XCOUNT	010213
XLOOP	010225	XOFF	010322	Y	010307	Y1TEMP	010312
Y2TEMP	010362	YAVG	010310	YCOUNT	010157	YOFF	010321

EXAMPLES OF BASIC INTERFACE

```
LIST

10 REM A IS HIGH ORDER BYTR, B IS LOW ORDER BYTE
20 REM OF GRAPHICS BOARD
30 A=2252
40 B=2251
50 REM C IS START ADDRESS OF GETVAL
60 C=1549
70 REM X IS HORIZONTAL VECTOR
80 X=22456
90 REM Y IS VERTICAL VECTOR
100 Y=22478
110 REM X1 IS FIRST HORIZONTAL DOT OF A LINE
120 X1=2249
130 REM X2 IS SECOND HORIZONTAL DOT OF A LINE
140 X2=2289
150 REM Y1 IS FIRST VERTICAL DOT OF A LINE
160 Y1=2250
170 REM Y2 IS SECOND VERTICAL DOT OF A LINE
180 Y2=2290
190 REM FILL THE GRAPHICS START ADDRESS WITH THE ADDRESS OF
200 REM THE GRAPHICS BOARD
210 FILL B,0
220 FILL A,128
230 REM CLEAR THE SCREEN
240  FOR K=1 TO 16:#"":NEXT K
250 Z=CALL(C,9)
260 REM PLOT 500 RANDOM DOTS
270  FOR I=1 TO 500
280    T=INT(RND(1)*255)
290     R=INT(RND(1)*255)
300  FILL X,T
310  FILL Y,R
320  Z=CALL(C,1)
330  NEXT I
340  Z=CALL(C,9)
350 REM PLOT SINE WAVES
360 FOR J=1 TO 40 STEP .05
370  S=INT(SIN(J)*J)
380 GOSUB 430
390   S=INT(60*(SIN(J)))
400   GOSUB 430
410 NEXT J
420 GOTO 470
430  FILL X,INT(J*6)+2
440   FILL Y,S+129
450  Z=CALL(C,1)
460 RETURN
470 Z=CALL(C,9)
480 FOR J=1 TO 40 STEP .05
490    S=INT(40*(COS(J)))
500    GOSUB 430
510  NEXT J
520 Z=CALL(C,9)
530 FOR I=1 TO 16
540  #""
550  NEXT I
560   # TAB(15),"PLACE PEN HERE"
570  FOR I=1 TO 8
580 #""
```

```
590 NEXT I
600  #"PUSH BUTTON"
610  Z=CALL(C,6)
620 F=EXAM(X)
630 G=EXAM(Y)
640 # "X=",F," Y=",G
650  FOR U=1 TO 500:NEXT U: REM DELAY LOOP
660 Z=CALL(C,9)
670 REM COMPLIMENT AND TEST DOT
680 S=CALL(C,9)
690 FOR E=1 TO 10
700 FILL X,128:FILL Y,128
710 S=CALL(C,2)
720 Z=CALL(C,3)
730 #Z
740 NEXT E
750  FOR H=1 TO 500:NEXT H: REM DELAY LOOP
760 GOTO 240
READY
```

NOTE: The continuous draw routine (Value"7") may be exited by typing Ctr Q.

D. PARTS LIST

1. Graphics Display

Description	Quantity	Circuit Reference
7400	7	U18, 25, 29, 35, 45, 47, 56
7401	2	U37, 38
7404	5	U19, 30, 32, 40, 44
7406	1	U23
7408	2	U22, 67
7410	2	U20, 43
7420	3	U26, 27, 42
7430	1	U41
7473	4	U31, 33, 39, 57
7474	3	U28, 36, 46
7486	1	U68
74123	1	U34
74125	1	U66
74163	4	U52, 53, 62, 63
74165	2	U48, 49
74173	6	U54, 55, 58, 59, 64, 65
74195	1	U21
74367	4	U50, 51, 60, 61
75451	1	U17
LM319	1	U24
TMS 4050	16	U1-U16
10 ohm, ¼watt resistor	1	R12
18 ohm, ¼watt resistor	1	R9
36 ohm, ¼ watt resistor	1	R20
47 ohm, ¼watt resistor	2	R16,18
75 ohm, ¼watt resistor	1	Rt
120 ohm, ¼watt resistor	1	R11
130 ohm, ¼watt resistor	1	R14
330 ohm, ¼watt resistor	2	R19,Rcpu
470 ohm, ¼watt resistor	3	R3,4,5
1K ohm, ¼watt resistor	1	R15
2.2k ohm, ¼watt resistor	1	R22
6.8K ohm, ¼watt resistor	2	R10,17
10K ohm, ¼watt resistor	1	R7
47K ohm, ¼watt resistor	1	R6
220 ohm, 1 watt resistor	2	R1, 2
5K ohm Pot	2	R8,13
2.2K 16 pin DIP R-PAK	2	Z1,2
750 pfd, mylar	1	C18
.001 ufd, disc	2	C15,23
.0015 ufd, ceramic	2	C13,14
.01 ufd, disc	16	C2-9,12,16,21,25,28,33,35,36
.1 ufd, disc	8	C11,19,20,22,24,26,27,30
1 ufd, tantalum	5	C10,17,31,32,34
4.7 ufd, tantalum	2	C1,29
220 pfd mylar	2	C37,38
1N60, 1N48, germanium	1	CRA (CPU)
1N4148, silicon	2	CR1,CRB (CPU)

8 pin IC socket	1
14 pin IC socket	33
16 pin IC socket	24
18 pin IC socket	16
Crystal socket	1
Crystal, 11.569 MHz	1
Printed circuit board	1
Paddle card	1
Graphics Input Cable Assembly	1
Graphics Control Cable Assembly	1
8 conductor double ended molex cable	1
Cable ties	3

2. Light Pen

330 ohm, ¼watt resistor	1	R4
1K ohm, ¼watt resistor	1	R2
2.2k ohm, ¼watt resistor	3	R5,8,10
4.7k ohm, ¼watt resistor	1	R7
6.2k ohm, ¼watt resistor	1	R1
10k ohm, ¼watt resistor	2	R3,6
56k ohm, ¼watt resistor	1	R9
1 ufd tantalum	1	C3
.033 ufd disc	2	C1,2
2N5129 or equivalent	2	Q2,4
2N5139 or equivalent	1	Q3
MV 5020 or equivalent LED	1	CR1
GE L14G1 or equivalent	1	Q1
Push button switch	1	S1
Light Pen Body	1	
Round end cap	1	
Flat end cap	1	
Push Button	1	
3/16" roll pin	1	
Cable	1	
Cable ties	2	
Light Pen PC Board	1	

E.1 GRAPHICS / MEMORY BUS PINOUT

CPU Ref.	Pin No.	Function		CPU Ref.	Pin No.	Function	
1	1	+5V		3	A	Spare Voltage	
2	2	Ground		4	B	-5V	
5	3	MSB	DATA TO CPU	13	C	MSB	DATA FROM CPU
6	4	MSB-1		14	D	MSB-1	
7	5	MSB-2		15	E	MSB-2	
8	6	MSB-3		16	F	MSB-3	
9	7	LSB+3		17	H	LSB+3	
10	8	LSB+2		18	J	LSB+2	
11	9	LSB+1		19	K	LSB+1	
12	10	LSB		20	L	LSB	
21	11	MEMRD			M	VIDEO	
30	12	A8	MEMORY ADDRESS LINES (HIGH BYTE)	22	N	A0	MEMORY ADDRESS LINES (LOW BYTE)
31	13	A9		23	P	A1	
32	14	A10		24	R	A2	
33	15	A11		25	S	A3	
34	16	A12		26	T	A4	
35	17	A13		27	U	A5	
36	18	A14		28	V	A6	
37	19	A15		29	W	A7	
97	20	HOLD		38	X	MEMWR	
39	21	REFRESH			Y	Spare	
40	22	DMA REQUEST		41	Z	DMA GRANT	
42	23	INT REQUEST			$\overline{A}$	Spare	
43	24	RUN		44	$\overline{B}$	STEP	
	25	Spare			$\overline{C}$	Spare	
	26	Spare			$\overline{D}$	Spare	
45	27	WAIT REQUEST		46	$\overline{E}$	MEMRQ	
47	28	RESET		89	$\overline{F}$	IRQ	
48	29	ROM		94	$\overline{H}$	NMI	
98	30	VMA			$\overline{J}$	Spare	
	31	Spare			$\overline{K}$	Spare	
	32	Spare			$\overline{L}$	Spare	
	33	Spare			$\overline{M}$	Spare	
	34	Spare			$\overline{N}$	Spare	
	35	Spare		48	$\overline{P}$	Spare	
49	36	+12V		50	$\overline{R}$	-12V	

E.2 INPUT / OUTPUT PORT CONNECTIONS

Top of card - Component Side

Pin No.	Description	Bit	
1	LSB	Ø	
2	LSB+1	1	
3	LSB+2	2	
4	LSB+3	3	
5	MSB-3	4	*INPUT PORT Ø,4,8...*
6	MSB-2	5	
7	MSB-1	6	
8	MSB	7	
9	n/c		
10	LSB	Ø	
11	LSB+1	1	
12	LSB+2	2	
13	LSB+3	3	
14	MSB-3	4	*INPUT PORT 1,5,9...*
15	MSB-2	5	
16	MSB-1	6	
17	MSB	7	
18	n/c		
19	LSB	Ø	
20	LSB+1	1	
21	LSB+2	2	
22	LSB+3	3	
23	MSB-3	4	*INPUT PORT 2,6,10...*
24	MSB-2	5	
25	MSB-1	6	
26	MSB	7	
27	n/c		
28	LSB	Ø	
29	LSB+1	1	
30	LSB+2	2	
31	LSB+3	3	
32	MSB-3	4	*INPUT PORT 3,7,11...*
33	MSB-2	5	
34	MSB-1	6	
35	MSB	7	
36	n/c		

Bottom of Card-Circuit Side

Pin No.	Description	Bit	
A	LSB	Ø	
B	LSB+1	1	
C	LSB+2	2	
D	LSB+3	3	
E	MSB-3	4	*OUTPUT PORT Ø,4,8...*
F	MSB-2	5	
H	MSB-1	6	
J	MSB	7	
K	n/c		
L	LSB	Ø	
M	LSB+1	1	
N	LSB+2	2	
P	LSB+3	3	
R	MSB-3	4	*OUTPUT PORT 1,5,9...*
S	MSB-2	5	
T	MSB-1	6	
U	MSB	7	
V	n/c		
W	LSB	Ø	
X	LSB+1	1	
Y	LSB+2	2	
Z	LSB+3	3	
$\overline{A}$	MSB-3	4	*OUTPUT PORT 2,6,10...*
$\overline{B}$	MSB-2	5	
$\overline{C}$	MSB-1	6	
$\overline{D}$	MSB	7	
$\overline{E}$	n/c		
$\overline{F}$	LSB	Ø	
$\overline{H}$	LSB+1	1	
$\overline{J}$	LSB+2	2	
$\overline{K}$	LSB+3	3	
$\overline{L}$	MSB-3	4	*OUTPUT PORT 3,7,11...*
$\overline{M}$	MSB-2	5	
$\overline{N}$	MSB-1	6	
$\overline{P}$	MSB	7	
$\overline{R}$	n/c		

Note:

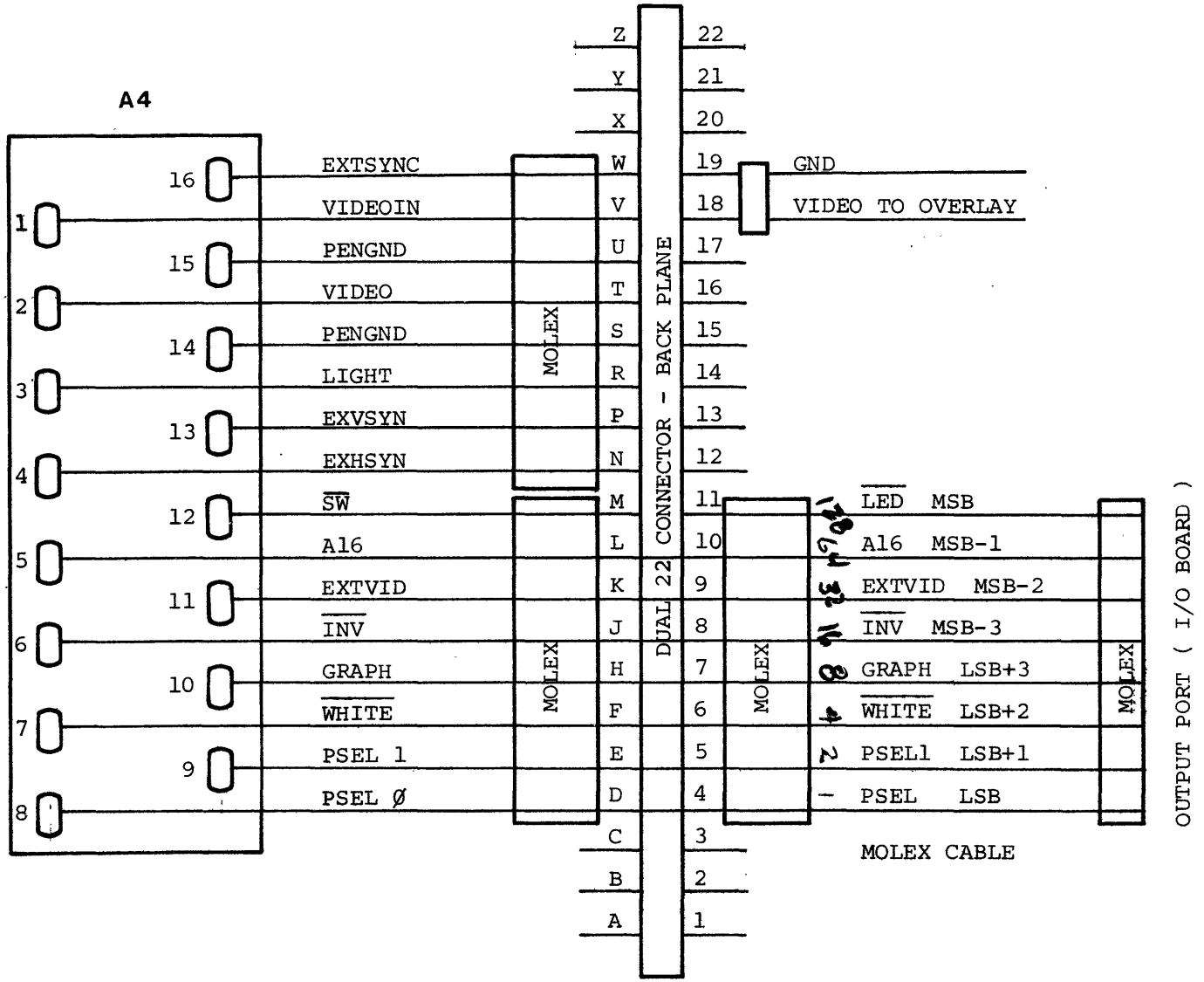
MSB=Most Significant Bit
LSB=Least Significant Bit
n/c=No Connection

E. 3 1024 CHARACTER TVC (TVC-64)

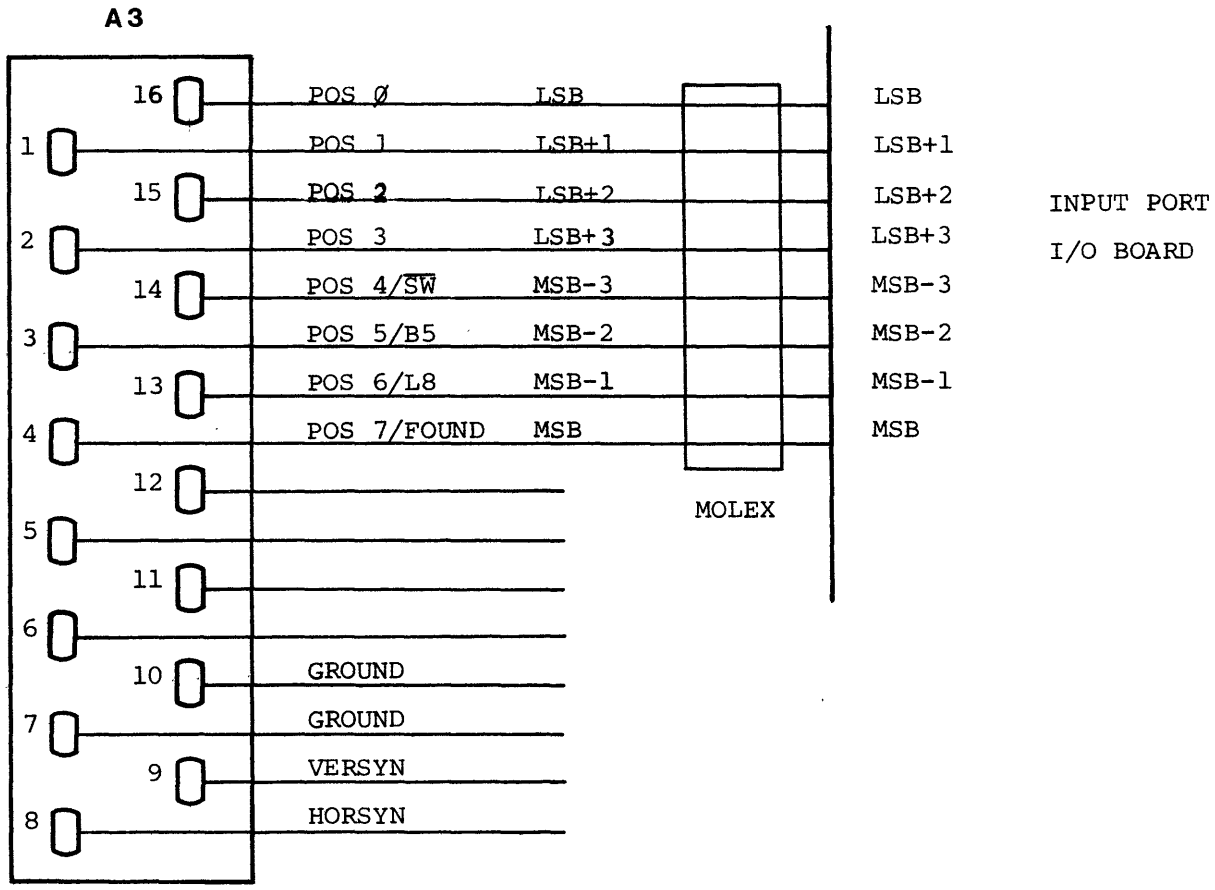
Component Side (Front)		Circuit Side (Back)		
1	MSB—Strobe	A	P	
2	MSB-1	B	A	
3	MSB-2	C	B	
4	MSB-3 (Data to TV)	D	C	HORZ
5	LSB+3	E	D	
6	LSB+2	F	E	
7	LSB+1	H	N	
8	LSB	J	F	
9	Data From Cassette	K	G	
10	Data To Cassette	L	H	
11	Clock *	M	I	
12	H SYNC *	N	J	VERT
13	V SYNC *	P	K	
14	H BLANK	R	L	
15	V BLANK	S	M	
16	Video *	T	Data Inv	
17	Data to CPU	U	H Preset	
18	Data From CPU	V	V Preset	
19	+5V	W	Graphic Input	
20	Ground	X	Graphic Select	
21	+12V	Y	Not used	
22	-12V	Z	Not used	

* Signals that may be used with superimposed video.

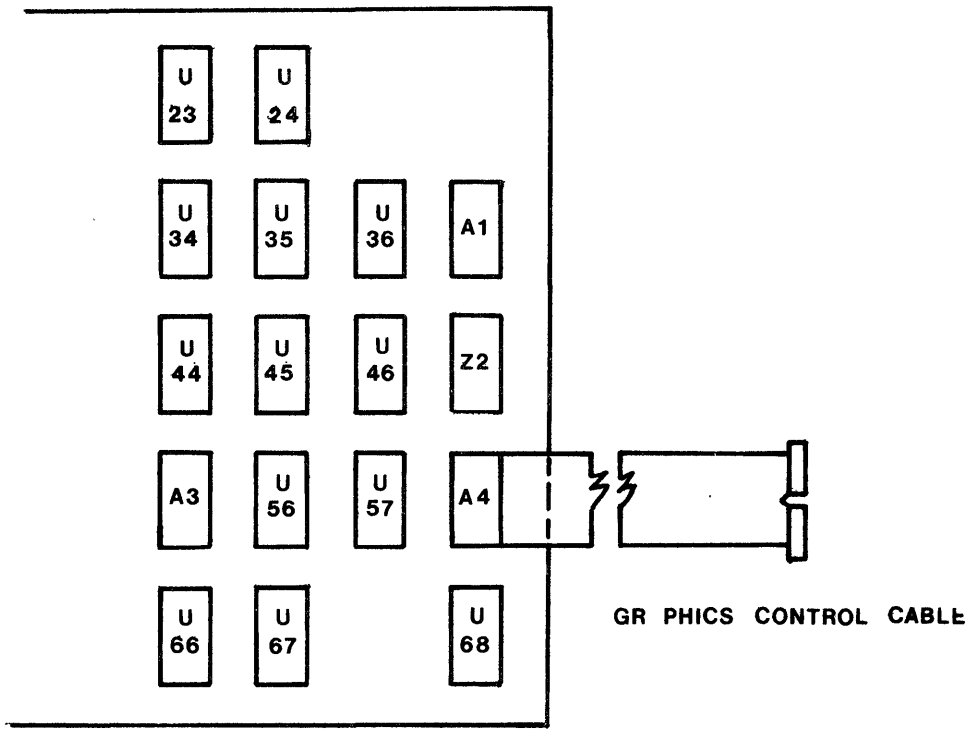
E.4 BACK PANEL CONNECTOR PIN OUT

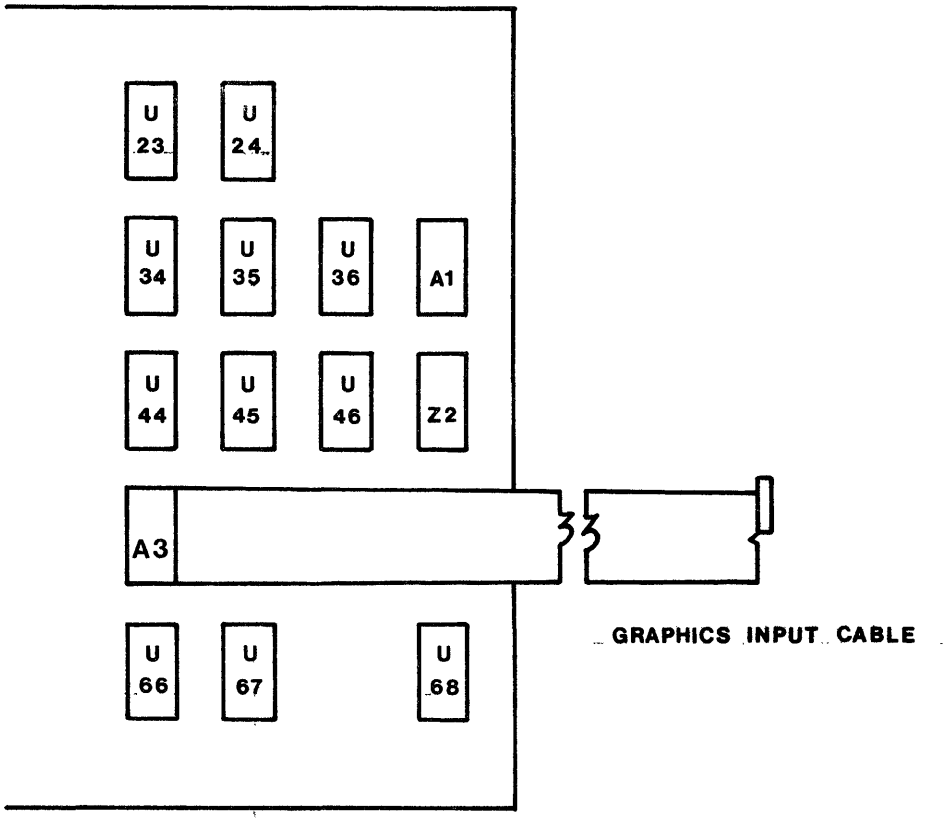


F.1 GRAPHICS CONTROL CABLE



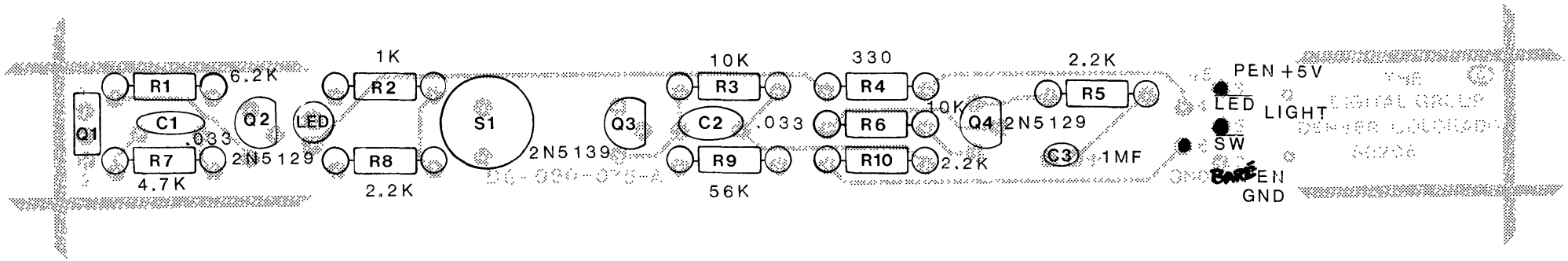
F.2 GRAPHICS INPUT CABLE



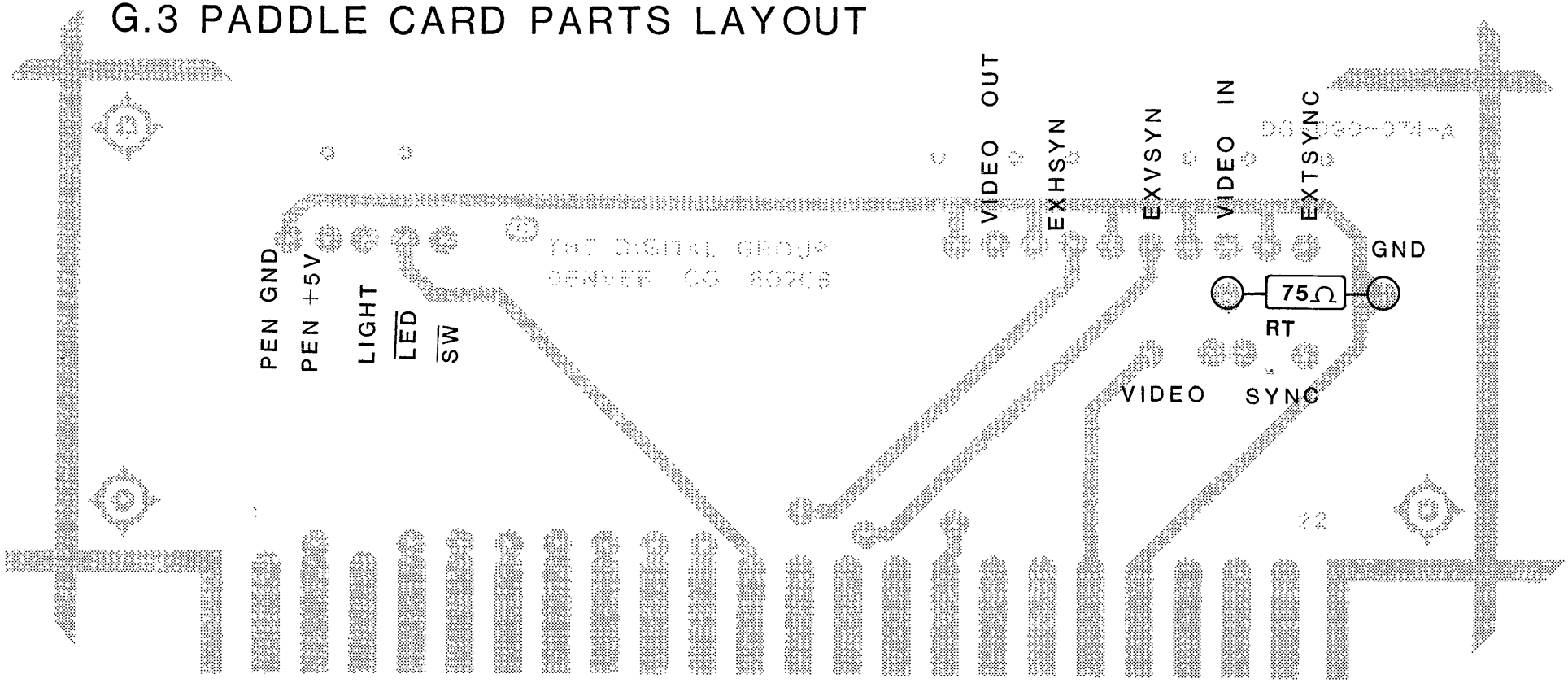


F.3 CABLE ORIENTATION DIAGRAMS

9.2 LIGHT PEN PARTS LAYOUT



G.3 PADDLE CARD PARTS LAYOUT



SYNC SEPARATOR

SYNC GENERATOR

LIGHT PEN LOGIC

ADDRESS MULTIPLEXING

MEMORY

VIDEO OUTPUT CIRCUITRY

TIMING LOGIC

SERIALIZER

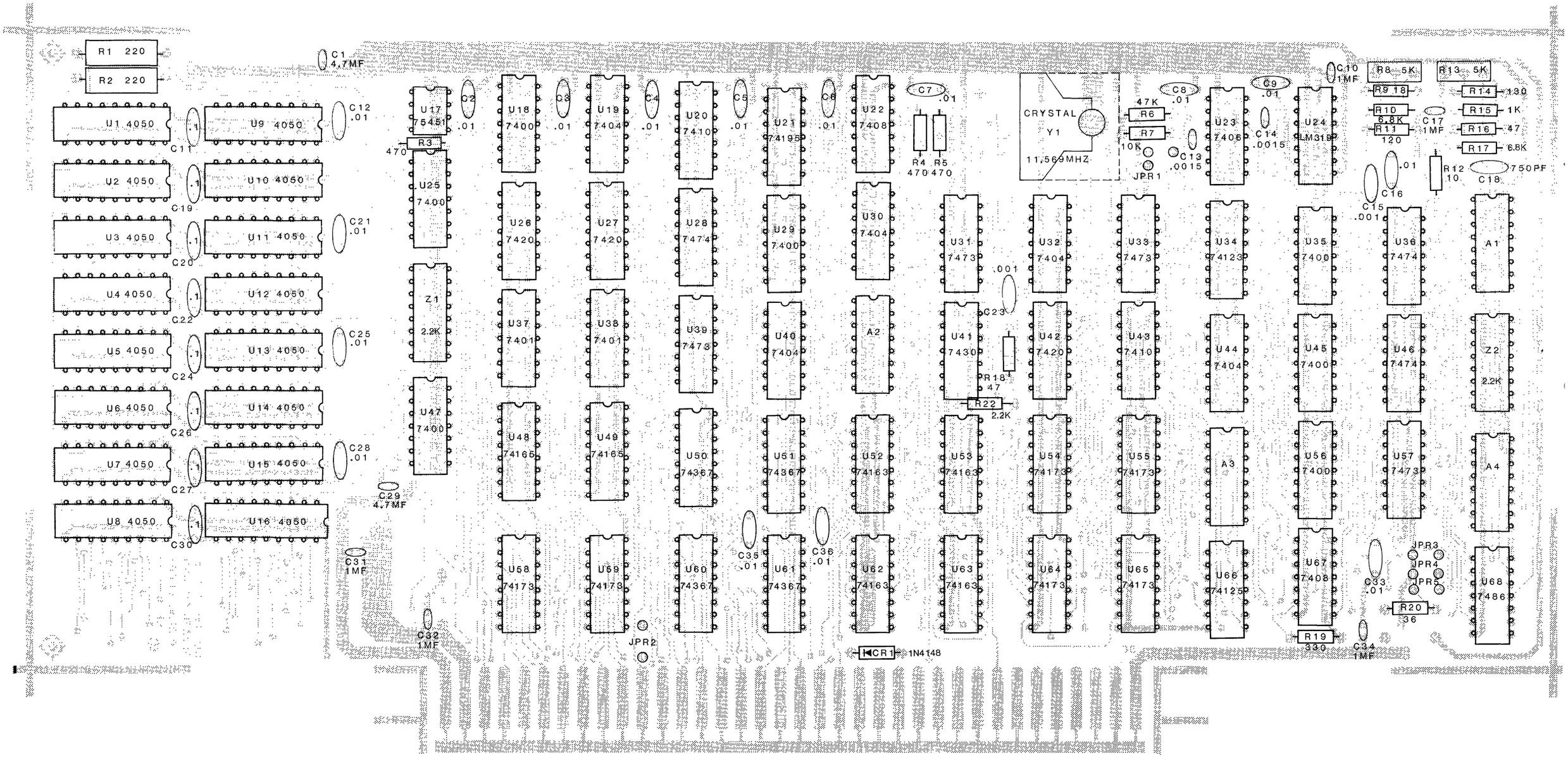
CONTROL LOGIC

DATA BUFFERS

ALL RESISTORS 1/4 WATT
UNLESS OTHERWISE NOTED

H.1 GRAPHIC DISPLAY SCHEMATIC

3.1 GRAPHIC DISPLAY PARTS LAYOUT



H.2 LIGHT PEN SCHEMATIC