DEC STANDARD 157

OMNIBUS

Specification

TITLE: OMNIBUS Specification

ABSTRACT: This document describes in detail the mechanical and electrical characteristics of a bus scheme used to interconnect circuit modules that form the various PDP-8 series of mini-computers. This specification should be followed carefully when designing a device that is going to connect to the OMNIBUS.

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1.0 GENERAL

1.1

This specification describes the OMNIBUS used on the PDP-8E, PDP-8M, PDP-8F and PDP-8A computers. The OMNIBUS is an internal, parallel bus used to connect central processor, memories, peripherals, etc.

1.2

Physically, the OMNIBUS consists of DEC standard H863 connector blocks (DEC part number 12-10258) arranged to accept quad modules.

1.3

Certain pins are preassigned as follows:

Ground: Pins C, F, N, T of all connectors (AC1, AC2, AF1, AF2, AN1, AN2, AT1, AT2, BC1, BC2, BF1, BF2, BN1, BN2, BT1, BT2, CC1, CC2, CF1, CF2, CN1, CN2, CT1, CT2, DC1, DC2, DF1, DF2, DN1, DN2, DT1, DT2)

+5 volts: Pins AA2, BA2, CA2

+15 volts: Pin DA2

-15 volts: Pins AB2, BB2, CB2, DB2

Test points or special signals: Pins AA1, AB1, BA1, BB1, CA1, CB1, DA1, DB1.

1.4

All other pins are parallel-wired (pin CM2 of slot 1 is wired to pin CM2 of slot 2, etc.) to form the 96 signals of the OMNIBUS.

1.5

A note on nomenclature:

Many places in this document, symbology of the general form MD<3:8>L is used. This symbology should be read "MD3 L through MD8 L", and interpreted as meaning MD3 L, MD4 L, MD5 L, MD6 L, MD7 L, and MD8 L.

1.6

Occasionally this specification will separately refer to PDP-8E and PDP-8A. Unless specifically stated to the contrary, statements regarding the PDP-8E apply equally to the PDP-8M and PDP-8F.

1.7

When this specification describes the operation of signal names it is done in a positive manner. I.e., unless the specification says otherwise, don't do it.

2.0 MAJOR GROUPS OF SIGNALS

The 96 signals of the OMNIBUS can be divided into 9 major classes, dependent on their use within the computer. See section 3 for detailed logic description.

2.1 Memory Address -- 15 Lines

The 15 lines EMA<0:2>L; MA<0:11>L form a bus which defines the currently active memory address. The source of MA<0:11>L is the CPU during instruction processing, and the currently active data break device during DMA operations. The source of EMA<0:2>L is the memory extension control during instruction processing, and the currently active data break device during DMA operations. Load resistors within the CPU define EMA<0:2>L as zeros (highs) if there is no memory extension control in the system.

2.2 Memory Data And Direction Control -- 13 Lines

2.2.1

The 12 signals MD<0:11>L from a bidirectional data path between memory and CPU. In addition, these lines are monitored by Programmed I/O devices to determine device code and sub-device operation; and by data break devices to obtain output (memory-to-DMA device) words.

2.2.2

The source of information on MD<0:11>L is controlled by MD DIR L. If MD DIR L is low, the data of the currently active memory is gated onto MD<0:11>L. If MD DIR L is high, the contents of the CPU's memory buffer register aregated onto MD<0:11>L.

2.3 Data Bus -- 12 Lines

The 12 signals DATA<0:11>L form a multi-purpose 12-bit bus. This bus is used for data exchange between peripheral and CPU, for data input from DMA device, for front-panel monitoring of selected registers, and for the determination of data break priority.

2.4 I/O Control Signals -- 10 Lines

This group of signals controls the I/O dialogue between CPU and Programmed peripherals. This group also includes INITIALIZE H, which is used for clearing peripheral flags.

2.5 DMA Control Signals -- 8 Lines

This group of signals controls the operation of data break (DMA). Several of these signals are also activated for certain front-panel operations. Also included in this group is RUN L, which is used for clearing data break requests when the computer is halted.

2.6 Timing Signals -- 9 Lines

Five time pulses serve as system clocks. Similarly, four time state levels serve as system enabling levels. All of these signals originate within the main timing generator of the CPU.

2.7 CPU State -- 6 Lines

The major state of the CPU appears on the major state lines (F L, D L, E L); the op code of the instruction currently being processed appears on IR<0:2>L.

2.8 Memory Timing Signals -- 5 Lines

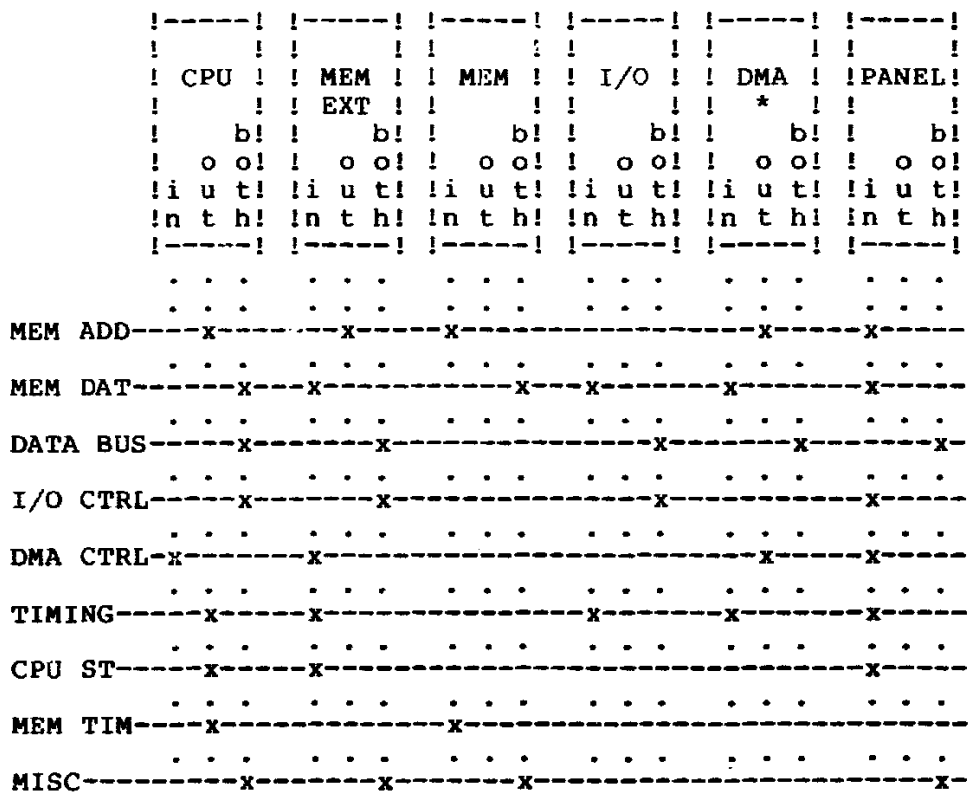
Five signals originate in the main timing generator of the CPU and are bussed to all memories. These signals (SOURCE H, RETURN H, WRITE H, INHIBIT H, and STROBE H) control all memory operations.

2.9 Miscellaneous Signals -- 18 Lines

These signals do not fit into any of the above categories. A large percentage of them are used by the operator's console (front panel). Two signals (ROM ADDRESS L and NTS STALL L) are driven by some types of memories under special conditions, and are monitored by the CPU and other memories. The remainder of these signals are truly miscellaneous. Included in this group is a signal (POWER OK H) which reports the validity of the power supply voltages.

2.10

The interconnection of various system parts via the OMNIBUS is shown below:



3.0 DETAILED LOGIC DESCRIPTION OF THE 96 OMNIBUS SIGNALS

This section describes the logical operation of each of the OMNIBUS signal lines. The paragraphs are arranged similarly to section 2 for easier correlation between the two sections. Unless otherwise stated; a logic H=Zero. See paragraph 4 for a description of the timing signals referenced.

3.1 Memory Address -- 15 Lines

These signals are changed starting at the leading edge of PULSE LOAD ADDRESS H or TP4 H and remain static through the entire memory cycle.

3.1.1 EMA<0:2>L L=one - Must be settled 50 ns prior to leading edge of SOURCE H and RETURN H.

signal	pin	
EMA0L	AD2	Most significant
EMA1L	AE2	
EMA2L	AH2	

3.1.2 MA<0:11>L L=one - Must be settled 50 ns prior to leading edge of SOURCE H and RETURN H.

signal	pin	
MA0L	AD1	Most significant
MA1L	AE1	
MA2L	AH1	
MA3L	AJ1	
MA4L	BD1	
MA5L	BE1	
MA6L	BH1	
MA7L	BJ1	
MA8L	DD1	
MA9L	DE1	
MA10L	DH1	
MA11L	DJ1	

---

*This is just the DMA portion of what is usually a complex peripheral. Such a peripheral usually uses the Programmed I/O signals as well.

3.2 Memory Data And Direction Control -- 13 Lines

3.2.1 MD<0:11>L L=1 - These lines form the data path to and from memory. If MD DIR L will remain low for the entire memory cycle, information from memory may be placed on the MD lines as late as 150 ns prior to TP2; otherwise, the information must be present 250 ns before TP2. If MD DIR L is allowed to go high, the new MD information from the CPU's Memory Buffer register must be on the OMNIBUS 150 ns prior to the leading edge of INHIBIT H, and must remain static for the duration of INHIBIT H for proper memory operation. It is desirable that the MD lines remain static into time state 1 of the next machine cycle to facilitate displaying the contents of memory when single-stepping programs.

MD0L	AK1	Most significant
MD1L	AL1	
MD2L	AM1	
MD3L	AP1	
MD4L	BK1	
MD5L	BL1	
MD6L	BM1	
MD7L	BP1	
MD8L	DK1	
MD9L	DL1	
MD10L	DM1	
MD11L	DP1	

3.2.2 MD DIR L. L=Memory Driving MD Lines - H=CPU's MB register driving MD lines. MD DIR L is always low from 100 ns after the leading edge of TP1 H to the leading edge of TP2 H, when it may be allowed to go high. The gating from MD DIR L to the drivers of the MD bus is static; hence care should be taken to guarantee that this line does not "glitch". If MD DIR L remains low for the entire memory cycle, the information on the MD lines is valid from the time it is placed on the OMNIBUS through the end of the memory cycle. No extra time need be allotted for computing and storing information in the CPU's MB register, and no time need be allotted for MB driver turn-on and bus propagation after TP2. The PDP-8E, M and F make use of this fact in their faster instruction fetch and non-auto-indexed defer cycles.

signal	pin
MD DIR L	AK2

3.3 Data Bus -- 12 Lines L=one

The data bus is a multi-purpose 12-bit bus whose use is a function of the machine state. During TS1 of every memory cycle, the data bus carries indicator information, as defined by the IND lines (see paragraph 3.91).

During TS2 of fetch cycles, the data bus carries the contents of the AC. During TS2 of DMA cycles, the data bus carries information to be placed in memory, or information to be added to the contents of memory (see paragraph 3.5.5).

During TS3 of IOT instructions, the information on the data bus is a function of the I/O control lines (see paragraph 3.4.5). During TS3 of OP2 instructions, the contents of the CPU's AC are placed on the data bus if the CLA bit (bit 4 of the instruction word) is zero, and the contents of the control panel's switch register are placed on the data bus if bit 9 of the instruction word is a one. This implements the OSR and LAS instructions. During TS4 of all machine cycles, the data bus is reserved for determining data break (DMA) priority. See paragraph 3.5 for more details.

A good general rule is for all logic to stay off the data bus unless the conditions are met in the preceding paragraph. The data bus must be left free for use by the CPU.

signal	pin	
DATA0L	AR1	Most significant bit
DATA1L	AS1	
DATA2L	AU1	
DATA3L	AV1	
DATA4L	BR1	
DATA5L	BS1	
DATA6L	BU1	
DATA7L	BV1	
DATA8L	DR1	
DATA9L	DS1	
DATA10L	DU1	
DATA11L	DV1	

3.4 I/O Control Signals -- 10 Lines

Basic I/O devices may perform data exchange between the AC of the CPU and the device's registers. The state of the device is tested using skip instructions. These devices need not make connection to C2 L, BUS STROBE L, and NOT LAST XFER L.

More complicated I/O devices may use BUS STROBE L and NOT LAST XFER L to stall the CPU, perform multiple transfers in a single IOT, and/or

modify the PC (and/or the Link).

3.4.1 I/O PAUSE L -- Pin CD1 - I/O PAUSE L is low if F L, MD0 L and MD1 L are low and USER MODE L and MD2 L are high. Also included is a gating term from the timing chain. It is the command to all Programmed I/O periperals to compare their device codes with the contents of MD<3:8>L. If a peripheral finds equality with MD<3:8>L it decodes MD<9:11>L to determine the sub-device operation to be performed. The peripheral has 100 nanoseconds in which to decode its subdevice operation and assert information onto the C lines and data bus. Similarly, it must remove all information 100 ns after I/O PAUSE L is negated.

I/O PAUSE L remains asserted during extended I/O cycles until the CPU has been restarted. (see paragraph 3.4.7)

Although not mandatory, it is strongly urged that the peripheral logic design incorporate load-relief logic to minimize loading on the Data and MD busses when I/O PAUSE is negated. Loading rules require load relief if there is more than one Programmed - I/O peripheral.

3.4.2 INTERNAL I/O L -- Pin CL1 - INTERNAL I/O L alerts the KA8E Positive I/O Bus Adapter that an I/O device on the OMNIBUS has recognized the IOT being processed. If the KA8E finds this line not grounded, it processes the IOT by stopping the CPU and entering an expanded I/O cycle.

All internal (OMNIBUS) I/O devices ground this line if they find equality between MD<3:8>L and their device code when I/O PAUSE L is low.

3.4.3 SKIP L -- Pin CS1 - SKIP L is sampled by the CPU at TP3 to determine if an I/O skip should occur. The skip occurs if SKIP L is low. Caution: This line may be sampled every TP3 (not just during IOT instructions), depending on the CPU.

3.4.4 INT RQST L -- Pin CP1 - INT RQST L is sampled by the CPU at the leading edge of INT STROBE H if all other interrupt conditions are met to determine if an interrupt request is pending. This line is grounded by a peripheral device when a condition which causes an interrupt is encountered. Since the CPU contains a synchronizing flip-flop, this line may be grounded at any time. In addition, if this line is grounded 100 ns or more before TP3, the SRQ instruction will skip.

3.4.5 C<0:2)L -- Pins CEl (C0 L) - CHl (C1 L); CJ1 (C2 L) C<0:2>L control the type of transfer during an IOT as shown below:

C<0:2>L 0 1 2	transfer
H x H	AC->DATA<0:11>L->AC (peripheral may "or" information onto DATA<0:11>L)
L H H	AC->DATA<0:11>L; 0->AC
L L H	DATA<0:11>L->AC
x H L	DATA<0:11>L+PC->PC
x L L	DATA<0:11>L->PC

In general, peripherals use only SKIP L to modify the pc, and so do not make connection to C2 L. See paragraph 4.4 for the impact on timing.

Historically, the HHH combination was reserved for output transfer, and the HLH combination for input or transfer. Many designs violated this convention; hence the HXH definition above.

3.4.6 BUS STROBE L -- Pin CKl - BUS STROBE L is a negative - going pulse which causes the AC or PC to be loaded during an IOT. BUS STROBE L is also used in conjunction with NOT LAST XFER L during long I/O cycles (see paragraph 3.4.7).

During an IOT, gating within the CPU generates a single BUS STROBE L pulse at TP3 time if NOT LAST XFER L is high (i.e., if the IOT is not an extended IOT). If an extended I/O cycle is in process (i.e., if NOT LAST XFER L is low at TP3 H), the peripheral must generate all BUS STROBE L pulses. The AC or PC (depending on C2 L) is loaded at the leading (falling) edge of BUS STROBE L.

3.4.7 NOT LAST XFER L -- Pin CLl - Most peripheral controllers require only one transfer per IOT; hence the single transfer at TP3 time is adequate. Such peripherals do not ground NOT LAST XFER L and do not drive BUS STROBE L. Other, more complex peripherals (the KA8E Positive I/O Adapter, for example) require extended timing and use NOT LAST XFER L to "stall" the CPU in an I/O cycle.

To stop the CPU in TS3 of an I/O cycle, ground NOT LAST XFER L prior to TP3 H of the IOT.

The CPU will remain in time state 3, and will not generate INT STROBE

H or BUS STROBE L. Timing is now controlled by the peripheral.

The peripheral may make any number of transfers by controlling C<0:2>L, generating BUS STROBE L and keeping NOT LAST XFER L at ground.

The CPU is restarted by allowing NOT LAST XFER L to go high before the leading (falling) edge of BUS STROBE L. In addition to making a final data transfer, the CPU restarts by generating INT STROBE H, entering TS4 and by negating I/O PAUSE L.

Caution: extended I/O cycles increase DMA latency times.

3.4.8 INITIALIZE H -- Pin CR1 - INITIALIZE H is asserted (high) by:

1. the operator's console (control panel) clear key being operated

2. the CAF instruction (octal 6007)

3. the negation of POWER OK H.

INITIALIZE H statically clears the AC, Link, interrupt system and peripheral flags. It also sets the interrupt enable flip-flops of peripherals which must remain program - compatible with older versions which did not have an interrupt enable flip-flop. (Two important devices in this category are the TTY and paper tape reader/punch interrupt enables.)

3.5 DMA Control Signals -- 8 Lines

Data breaks (DMA) allow a peripheral to communicate directly with memory, bypassing the CPU. The only CPU register available to the DMA device is the MB; all other CPU registers must be preserved. Data breaks may occur between any CPU cycles, but a data break cannot be performed while the CPU is in the midst of an extended I/O or EAE cycle because the currently active memory is then supplying information to the bus. Data breaks take place in the following sequence:

1. At INT STROBE H leading edge, the decision to request a data break is made at the peripheral by strobing its break request flip-flop.

2. A device starting a data break unconditionally grounds CPMA DISABLE L and BREAK IN PROG L until its break request flip-flop is cleared.

3. Data break priority is determined on DATA<0:11>L when TS4 L is asserted. Each data break device is assigned a unique line on DATA<0:11>L, with DATA0 L being the highest-priority line. Each requesting device grounds its line on DATA<0:11>L, and examines the state of all higher-priority lines to determine if they are all high. For example, a device grounding DATA5 L examines DATA<0:4>L to make sure these lines are all high. The device finding all higher-order lines high proceeds to step 4 below; all other devices remain in step 3.

4. The device winning the priority test sets its MA Control flip-flops at the leading edge of TP4 H. (The path from TP4 H to the memory address lines must have as little delay as possible; hence two flip-flops are recommended to provide adequate drive without introducing the delay of a buffer. See paragraph 5.7.) The MA Control flip-flops gate the break address onto the 15 memory address lines, and ground MS,IR DISABLE L and (if this cycle is a data exchange cycle) BK CYCLE L.

5. At TP1 H, the active device grounds MA, MS LOAD CONT L.

6. For input to memory, the active device merely places its data on DATA<0:11>L during TS2. For output from memory, the device grounds BREAK DATA CONT L during TS2 L, and loads its register with the contents of MD<0:11>L at the leading edge of TP2 H, TP3 H or TP4 H. For add to memory, the device places the data to be added on DATA<0:11>L during TS2, and grounds BREAK DATA CONT L during TS2. The modified information is loaded into the CPU's MB and overflow flip-flop at TP2 H, and may be read by the device at TP3 H or TP4 H. (TP3 H is generally used, since OVERFLOW L is valid only at this time.) The data prior to modification may be read at the leading edge of TP2 H.

7. At the completion of a data break, all lines are released in the same order and at the same times in which they were asserted.

8. Three-cycle data breaks are merely three one-cycle data breaks with a special control to handle word count and current address cycles. BREAK CYCLE L is not grounded during these two cycles; it is grounded only for the final, data exchange cycle.

DMA latency is the longest machine cycle, plus the time of TS4.

3.5.1 BRK IN PROG L -- Pin BE2 - This signal provides indicator information to the console. It is grounded at INT STROBE H leading edge, if a break is to take place; and causes the console "BRK IN PROG" light to turn on.

3.5.2 CPMA DISABLE L -- Pin CU1 - CPMA DISABLE L is asserted (grounded) by break devices if data breaks are to occur. It is sampled by the CPU and memory extension control at the leading edge of TP4 H. If CPMA DISABLE L is low at that time, the memory extension control's field bits and the CPU's memory address bits are removed from EMA<0:2>L and MA<0:11>L. If CPMA DISABLE L is negated (high) at the leading edge of TP4 H, the memory extension field bits and the CPU's memory address register are gated to EMA<0:2>L and MA<0:11>L respectively.

3.5.3 MS, IR DISABLE L -- Pin CV1 When MS, IR DISABLE L is high, the major state and IR flip-flops drive the major state and IR lines on the OMNIBUS (see paragraph 3.7). When MS, IR DISABLE L is asserted (grounded), the major state and IR lines are not driven by the CPU. Unless some external device asserts a major state, the CPU is then in the DMA state.

3.5.4 MA, MS LOAD CONT L -- Pin BH2 - MA, MS LOAD CONT L is negated (high), the CPU and memory extension control function normally. Asserting this line inhibits the loading of new information into the CPU's major state and and memory address registers, and into certain control flip-flops of the memory extension control. This signal must not change while TP4 H is high, it is normally changed at TP1 time.

3.5.5 BREAK DATA CONT L -- Pin BK 2 - This signal is ignored unless MS, IR DISABLE L is grounded (PDP-8E) or unless F L, D L, and E L are all high (PDP-8A). BREAK DATA CONT L should be stable as early in TS2 as possible, and defines the information loaded into the MB at TP2 H. If BREAK DATA CONT L is high during TS2 of a DMA, DATA<0:11>L is loaded into MB<0:11>. If BREAK DATA CONT L is low during TS2 of a DMA, MD<0:11>1 plus DATA<0:11>L is loaded into MB<0:11>. Making BREAK DATA CONT L low and placing no information (zeros) on DATA<0:11>L causes a DMA which does not modify memory.

3.5.6 OVERFLOW L -- Pin BJ2 - This line is asserted (low) during TS3 if a carry occurs at TP2. Hence this line is asserted if any of the following occur:

auto index or JMS wrap-around
ISZ overflow
data break overflow or carry

3.5.7 BK CYCLE L -- Pin BL2 - Panel information from the data break device. Low indicates a break data transfer cycle is in process.

3.5.8 RUN L -- Pin BU2 - This signal is really a CPU state, since it indicates the CPU's timing generator is running (when low). It is included in this group of signals because its most important function is as a gating term used to clear all break requests when negated (high).

3.6 Timing Signals -- 9 Lines

Five pulses and four levels originate in the timing generator of the CPU and are used as system clocks and enabling levels respectively. Time pulses are nominally 100 ns wide (INT STROBE H is more loosely defined--see paragraph 4.1). Time states change nominally 50 ns after the leading edge of the time pulse. When the CPU is stopped, the machine is at the beginning of TS1. Applying a single MEM START L causes the timing chain to start and continue to run until:

1. The STOP L line on the OMNIBUS is asserted at TP3, or
2. The CPU encounters a HLT instruction at TP3, or
3. POWER OK H is negated at TP3

and the current memory cycle has completed. A time state precedes the time pulse of the same number; INT STROBE H is coincident with TP3 H except when in an extended IOT or EAE operation; TS1 L is automatically entered at the end of TS4.

signal	pin
TS1 L	CK2
TS2 L	CL2
TS3 L	CM2
TS4 L	CP2
TP1 H	CD2
TP2 H	CE2
TP3 H	CH2

TP4 H	CJ2
INT STROBE H	BD2

3.7 CPU STATE -- 6 Lines

3.7.1 Major State Lines - The CPU major state appears on these lines unless MS, IR DISABLE L is asserted (see paragraph 3.5.3). The major state as seen by the CPU's instruction decoder is taken from these lines (except for the enabling of BREAK DATA CONT L during DMA in the 8E) hence it is possible to build special options which force instructions to the CPU. Normally the major state lines change at TP4.

major state	pin
F L	DJ2
D L	DK2
E L	DL2

3.7.2 IR<0:2>L Reflect The State Of The CPU's - instruction register provided MS, IR DISABLE L is high. A low on IR<0:2>L represents a one in the corresponding bit of the instruction register. As in the case of the major state lines, the IR lines are disconnected from the instruction register if MS, IR DISABLE L is low. The instruction seen by the CPU during D and E major states is obtained from these lines. (During instruction fetch, some instruction decoding is done directly from the MD lines. See individual CPU specs for this information.) As with the major state lines, it is possible to force instructions during defer or execute cycles. The IR is loaded at TP2 of an instruction fetch (F L is low), or at TP4 if an interrupt is being honored (INT IN PROG H is high).

signal	pin
IR0 L	DD2
IR1 L	DE2
IR2 L	DH2

3.8 Memory Timing Signals -- 5 Lines

These signals are defined in terms of the PDP-8E's original core memory, the MM8E. See paragraph 4.1 for waveforms.

3.8.1 SOURCE H -- Pin AL2, And RETURN H -- Pin AR2 - These signals become asserted (high) at the same time, and direct the core memory to turn on its read/write currents. RETURN H becomes negated 50 ns later than SOURCE H, thereby defining the voltage to which the memory stack is charged.

3.8.2 WRITE H -- Pin AS2 - WRITE H controls the direction of current flow in the memory stack. It is high during write and low during read. If WRITE H is low, the positive-going transition of SOURCE H is usually used to clear all memory data registers.

3.8.3 INHIBIT H -- Pin AP2 - INHIBIT H is a gating level to the inhibit drivers of core memory. When high, it causes the selected memory's inhibit drivers to turn on.

3.8.4 STROBE H -- Pin AM2 - The leading edge of STROBE H provides a time reference from which the stobe in each individual core memory is derived. Each memory delays this edge by an optimum amount for that memory, and then strobes its sense amplifiers. The selected memory must have its data on MD<0:11>L at or before strobe leading edge plus 150 nanoseconds (this time does not include bus charging time).

3.9 Miscellaneous Signals -- 18 Lines

3.9.1 IND1 L -- Pin CU2, And IND2 L -- Pin CV2 - These signals control the information gated to DATA<0:11>L during TS1. Since DATA<0:11>L is defined as low for a 1, ones in register bits place lows on DATA<0:11>L.

IND1 L	IND2 L	info on DATA<0:11>L
H	H	status word*
H	L	MQ<0:11>
L	H	all zeros (highs)
L	L	AC<0:11>

*status word:

bit	information

0	Link
1	GT Flip-Flop (PDP-8E EAE only)
2	INT RQST L (low on DATA2 L if INT RQST L [Pin CP1] is low)
3	Int Inh Flip-Flop** (PDP-8E only)
4	Interrupt Delay Flip-Flop (denotes interrupt on)
5	USER MODE L**
6-8	IF<0:2>**
9-11	DF<0:2>**

**from memory extension control if present. Otherwise these remain high (zeros).

Gating circuitry in any logic driving IND1 L and IND2 L should ground IND1 L and allow IND2 L to go high if LA ENABLE L is asserted (low). See paragraph 3.9.9.

3.9.2 MEM START L -- Pin AJ2 - Grounding MEM START L causes the timing chain of the CPU to start. MEM START L may be a 100 ns negative -- going pulse or it may be a level which is ground if TS1 L is asserted and the logical decision to start the machine has been made. MEM START L must not be at ground beyond TP2 H, since it may then interfere with possible HLT instructions.

A single MEM START L pulse causes the CPU to start and continue to run until halted by the program or by the STOP L line (see paragraph 3.9.3).

3.9.3 STOP L -- Pin DS2 - STOP L is sampled by the CPU at the leading edge of TP3 H of every machine cycle. If STOP L is asserted (low), the CPU completes its current memory cycle and stops in TS1 (just after TP4 H goes to ground). At that point in its cycle, the CPU can display:

- new memory address (on EMA<0:2>L and MA<0:11>L
- new major state (on F L, D L, and E L)
- memory data of last-referenced location (on MD<0:11>L)
- status or AC or MQ (on DATA<0:11>L, depending on IND1 L and IND2 L)
- any other lines on the OMNIBUS for which display provision has been made

STOP L is asserted by control panel keys (halt and single step), and is also asserted when:

single deposit operation is in process
examine operation is in process
a HLT instruction (octal 7402) is encountered
POWER OK H is low
KEY CONTROL L is low (PDP-8E)
panel examine or panel deposit condition (PDP-8A) (see 3.9.9)

3.9.4 LINK L -- Pin AV2 - Link L is low if the Link bit of the CPU is a one, and high if the link is a zero.

3.9.5 LINK LOAD L -- Pin CS2, And LINK DATA L - Pin CR2 - These two signals allow loading of the Link from the OMNIBUS. Loading occurs on the leading (falling) edge of LINK LOAD L, and the data loaded into the Link is a one if LINK DATA L is low. PDP-8E: these two signals should be used only during TS3 and TS4 of OPR or IOT cycles. PDP-8A: these two signals should be used only in extended I/O cycles while NOT LAST XFER L is low.

3.9.6 FSET L -- Pin DP2 - This line is asserted (low) if the major state gating of the CPU indicates the next major state will be a fetch. The conditions causing this line to be asserted are:

1. A major state of execute, no interrupt being honored (see paragraph 3.9.8) and a final execute cycle if the machine is a PDP-8E with EAE and doing a multi-state EAE operation.
2. A major state of defer and an IR of 5 (JMP instruction).
3. A major state of fetch, a JMP instruction and MD3 L high (direct jump)
4. A major state of fetch and an IOT instruction
5. A major state of fetch and an operate instruction (unless the machine is a PDP-8E with EAE and the instruction is MUY, DVI, ASR, SHL, SCL, DAD, OR DST)
6. DMA (F L, D L and E L all high)

3.9.7 USER MODE L -- Pin DM2 - This line is normally driven by the timeshare portion of the memory extension control, and is tied high by a load resistor in the CPU if no memory extension control is in the system. USER MODE L is changed only at TP4 time.

If USER MODE L is high, the CPU and control panel function normally. If USER MODE L is asserted (low), the following operations are inhibited:

1. The halt instruction (inhibited in the CPU)
2. The OSR and LAS instructions (inhibited in the panel logic)
3. I/O PAUSE L remains high even though an IOT instruction is fetched from memory (inhibited in the CPU)

Interruption of the program upon detection of any of these conditions is handled by the memory extension control.

3.9.8 INT IN PROG H -- Pin BP2 - INT IN PROG H is allowed to go high if:

1. The interrupt system has been turned on by an ION or RTF instruction and at least one subsequent instruction fetch has occurred, and
2. An interrupt request has been recognized by the Int Sync flip-flop of the CPU (which sets at the leading edge of INT STROBE H if INT RQST L and FSET L are both low), and
3. There is no interrupt inhibiting condition. This condition is preserved in the Int Inhibit flip-flop in the memory extension control, and is generated if a CIF, CUF, SUF, RMF or RTF instruction has been processed and a JMP or JMS has not yet occurred to complete the field change.

INT IN PROG H is used by the CPU to load 0 into the CPU's MA, force the major state to Execute and IR to JMS, and to turn off the interrupt system. INT IN PROG H is also used by the memory extension control to load the save field, and to clear the IB,IF and DF. INT IN PROG H goes high at INT STROBE H time, and is not negated again until the interrupt system is turned off. (INT IN PROG H, INT STROBE H and not DMA for PDP-8A; INT IN PROG H, TP1 H and not DMA for PDP-8E.)

3.9.9 LA ENABLE L -- Pin BM2, And KEY CONTROL - L -- Pin DU2
These lines must not be asserted (grounded) unless the CPU is in the DMA state. (MS,IR DISABLE L at ground and F L, D L, and E L all high). If LA ENABLE L is low, any logic driving IND1 L and IND2 L must ground IND1 L and turn off any drivers driving IND2 L.

PDP-8E: LA ENABLE L, when asserted, establishes a data path from DATA<0:11>L to the CPU's MA. This data path is a straight transfer, and is used for loading the contents of the control panel's switch register into the CPU's MA upon a load address command at the control panel.

PDP-8E: KEY CONTOL L, when asserted, grounds STOP L and INT IN PROG H; sets up gating in the CPU to cause MA+1->PC at TP1 H and PC->MA at TP4 H; and establishes a data path in the memory extension control which loads the field bits from DATA<6:11>L if a PULSE LA H is asserted.

PDP-8A: The function of LA ENABLE L, KEY CONTROL L and BREAK DATA CONT L are defined as follows:

LA EN	KC	BDC	Function
L	L	L	XLA 7
L	L	H	XLA 0
L	H	L	Non-stop deposit
L	H	H	Load address
H	L	L	Panel examine
H	L	H	Panel deposit
H	H	L	Add to memory*
H	H	H	Break deposit*

*See Paragraph 3.5.5

Panel examine grounds STOP L, performs one memory cycle at the address in the CPU's MA register; does a break add to memory, and increments the MA.

Panel deposit grounds STOP L, performs one memory cycle at the address in the CPU's MA register; does a break deposit with the SR of the panel providing input data, and increments the MA.

Load address -- there are two possible functions. If PULSE LA H is asserted, the MA is loaded from DATA<0:11>L. If MEM START L is asserted, the CPU starts performing an examine at whatever location is in the CPU's MA. At TP3 H, the contents of DATA<0:11>L are loaded into the PC and transferred to the CPU's MA at TP4 H. The CPU is not stopped. (STOP L is not grounded.)

Non-stop deposit -- same as panel deposit except STOP L is not grounded, so the CPU continues to run. Useful for loading bootstrap programs into memory.

XLA0--there are two modes of operation. If PULSE LA H is asserted,

the memory extension control is loaded with whatever is on DATA<6:11>L. If MEM START L is asserted, the CPU starts and does an examine at whatever location is in the CPU's MA. The memory extension control is loaded at TP3 H, but 0 is on DATA<6:11>L so the memory extension control's IF, IB and DF registers are cleared. STOP L is not grounded, so the CPU continues to run.

XLA7--like XLA0 with MEM START L, except that the CPU places 7777 on DATA<0:11>L, loading 7 into the IB, IF, and DF. Note: The AC must be 0 for this function to work properly.

3.9.10 PULSE LA H -- Pin DR2 - PULSE LA H causes the CPU's MA register to be loaded if KEY CONTROL L is high; or the memory extension control's IB, IF, and DF registers to be loaded if KEY CONTROL L is low. PULSE LA H is a nominal 100 nsec. positive-going pulse.

3.9.11 ROM ADDRESS L -- Pin AU2 - ROM ADDRESS L is examined by core and other read-write memories. If ROM ADDRESS L is high, the read-write memory functions normally. If ROM ADDRESS L is low, the read-write memory is disabled. ROM ADDRESS L is grounded by small ROMs which overlay read-write memories, thus providing a small number of read-only locations in a large read-write memory. Note: the gating must be fast.

There is only 25 ns from the time the address lines have been established to the time this signal must be asserted.

ROM ADDRESS L also modifies the JMS instruction by inhibiting the incrementing of the new PC contents. This action causes the JMS instruction to act like a JMP instruction (except for timing) if a JMS to ROM is attempted.

3.9.12 NTS STALL L -- Pin BR2 - On PDP-8E, this line should not be used for any purpose.

On PDP-8A, NTS STALL L (next time state stall 1) provides a means of stalling machine operation to accomodate memories slower than the one for which the timing chain was designed.

When NTS STALL L is high, the timing chain of the CPU functions normally. If NTS STALL L is asserted (low), the timing chain functions normally to the middle of the next time pulse. The time state changes and the time pulse completes in the normal 100 nsec, but the timing chain stalls at the beginning of the new time state. The stalling of the time state continues until NTS STALL L goes high, restarting the timing chain. Note that NTS STALL L has no effect on the duration of the five memory timing signals. It merely stretches the time before read, the time between read and write, and the time

after write before new address. NTS STALL L must be low 100 ns before the leading edge of a time pulse to guarantee stalling in the next time state. The timing generator will not stall in the next time state if NTS STALL L is high for the 100 ns prior to the leading edge of the time pulse.

NTS STALL low at:	TS becomes longer	And there is
TP1 H	TS2	Longer time from end of read to TP2, allowing the CPU to accommodate memories with long read access time.
TP2 H	TS3	Longer time from when MB is loaded to the start of write
TP3 H	TS4	Longer time from start of write to time address is changed, accomodating memories with long write times.
TP4 H	TS2	Longer time from address change to start of read

NOTE: watch break latency!!

3.9.13 SW -- Pin DV2 - This line reflects the state of the "SW" switch on the PDP-8E or PDP-8M panel, or the state of the "bootstrap" flip-flop controlled by the button on the PDP-8A panel. The signal is high if the switch is up on the PDP-8E, M or F; but low if the switch is up on the PDP-8A Limited Function Panel.

On machines equipped with bootstrap options, the low-to-high transition of this line initiates bootstrap operation if the CPU is halted. If there is no bootstrap option in the machine, this line is available for any use the user may devise. This line has switch bounce, so logic which requires a clean transition should pre-condition this signal.

3.9.14 POWER OK H -- Pin BV2 - POWER OK H originates in the power supply, and reports the state of the dc voltages to the CPU, memory extension control and core memories. The dc supplies are in regulation if this signal is high (see paragraph 6.4).

Caution: as the dc supplies fall toward ground, POWER OK H will be negated but may go somewhat positive again as the +5 v. supply nears ground. POWER OK H must remain at less than 0.4 volts until all supply voltages are less than 30% of their nominal. Otherwise, modification of core memory contents may occur.

POWER OK H being low grounds STOP L. POWER OK H going low is also applied to an integrator in the CPU, the output of which generates INITIALIZE H and is used as a master clear for the timing chain. Similar integrators in each of the core memories enable and disable the memory current supplies.

Negating POWER OK H does the following:

1. STOP L is asserted immediately.

2. At the next TP3 H, RUN L is negated by the CPU.

3. At the following TS1, all break devices clear their break requests, and the memory extension control initializes its EMA Enable flip-flop. The gating to accomplish this is usually the "and" of POWER OK H being low, TS1 L being low, and RUN L being high.

4. After a delay (15-500 microsec) long enough to allow the longest possible memory cycle to complete, the timing chain is preset to the beginning of TS1 with TP4 low. All memory timing signals are made low. The CPU's control flip-flop which gates the CPU's MA onto the memory address lines is placed in the "enabled" state. INITIALIZE H is generated, clearing the AC, Link and interrupt system.

5. After a similar delay, each core memory disables its current sources so that memory cannot be altered if memory timing signals should become asserted as the dc voltages go away.

Upon application of power:

1. The CPU, extension control and peripherals are all initialized.

2. Memory current sources are enabled 1 to 70 milliseconds after POWER OK H is asserted. This enabling is accomplished by an integrating capacitor, so that "spikes" on POWER OK H are filtered out.

3. The internal clear signal and the OMNIBUS INITIALIZE H signal are negated 200 to 1000 millisec after POWER OK H is asserted.

4. All portions of the computer should be ready to run 0.1 sec after POWER OK H is asserted.

   PDP-9E: MEM START L must not be asserted until INITIALIZE H is negated.

   PDP-8A: MEM START L will not be recognized until after INITIALIZE H is negated.

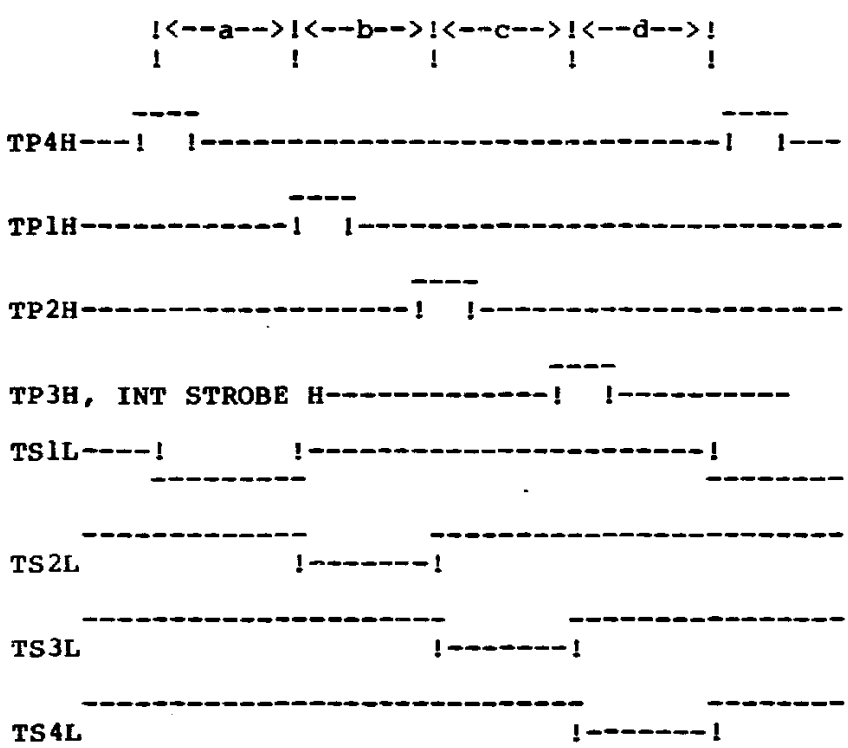
3.9.15 RES -- Pin BS2 - RES is an unused line. Digital Equipment Corporation reserves the right to define this line at a later date, and disclaims any responsibility to make this definition agree with any prior illicit useage.

4.0 TIMING

Many signals on the OMNIBUS are wire-ored. For these signals, the high level is determined by a load resistor, and the low level is determined by one or more open-collector gates which ground the signal. Bus capacitance is moderately high; hence fall times in such situations are fast and rise times are slow (about 100 nanoseconds). This 100 nanoseconds is considered in the following timing diagrams by adding the 100 nanoseconds to the set-up times where necessary. Hence, if (as in paragraph 4.5.2) this portion of the specification requires C<0:2>L to be defined from 450 nanoseconds before the leading edge of BUS STROBE L; 100 nanoseconds of this time is allotted to charging C<0:2>L.

4.1 Time Pulses And Time States

The time pulses (TP1 H, TP2 H, TP3 H, INT STROBE H and TP4 H) plus their associated time states (TS1 L, TS2 L, TS3 L and TS4 L) serve as the timing reference from which all other timing is derived. Timing pulses and time states are derived from a master crystal clock (20 mhz) in the timing generator of the CPU. This clock has a stability of 0.1%; hence the time between positive edges of time pulses is accurate to 0.1%. Time pulses widths are 90-110 nsec; the uncertainty is caused by gate skew and threshold variation. Time states change nominally at 50 nsec after the leading edge of the time pulses, but logic delays and loading introduce an uncertainty in this time. See diagaram below:



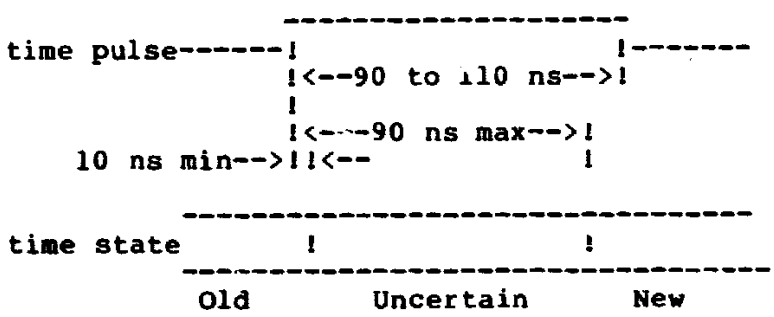
time in nanoseconds:

time interval	PDP-8E fast cycle	PDP-8E slow cycle	PDP-8A all cycles
a	300	300	350 nsec
b	250	450	400
c	350	350	400
d	300	300	350
total	1200	1400	1500

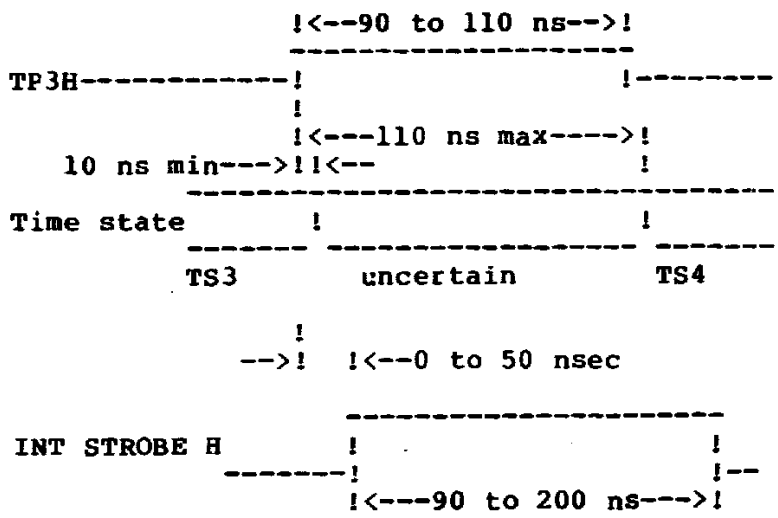
The PDP-8E fast cycle-slow cycle choice is determined by major state and the contents of MA<0:11>L. Fast cycle is taken if the major state is fetch (F L is low), or if the major state is defer (D L is low) and the MA lines are not 10-17 (one or more of MA<0:7>L is low or MA 8 L is high). Otherwise, slow cycle is taken. A jumper on the 8E timing board (M8330) forces all slow cycles when in place.

Detail of time pulse and timestate change:

(this applies to TP1 H, TP2 H and TP 4 H.)

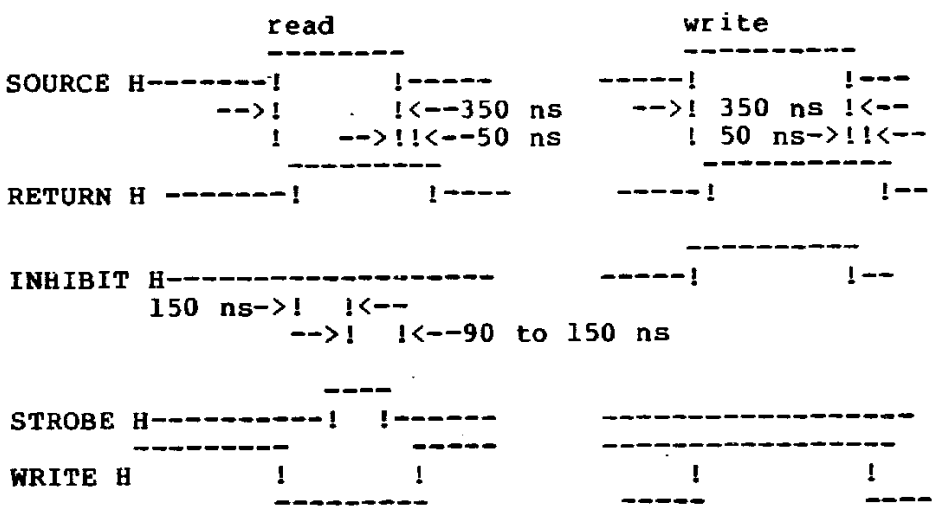


Details of TP3 H timing if NOT LAST XFER L is high and if I/O PAUSE L is high. (See paragraph 4.5 for other condition.)



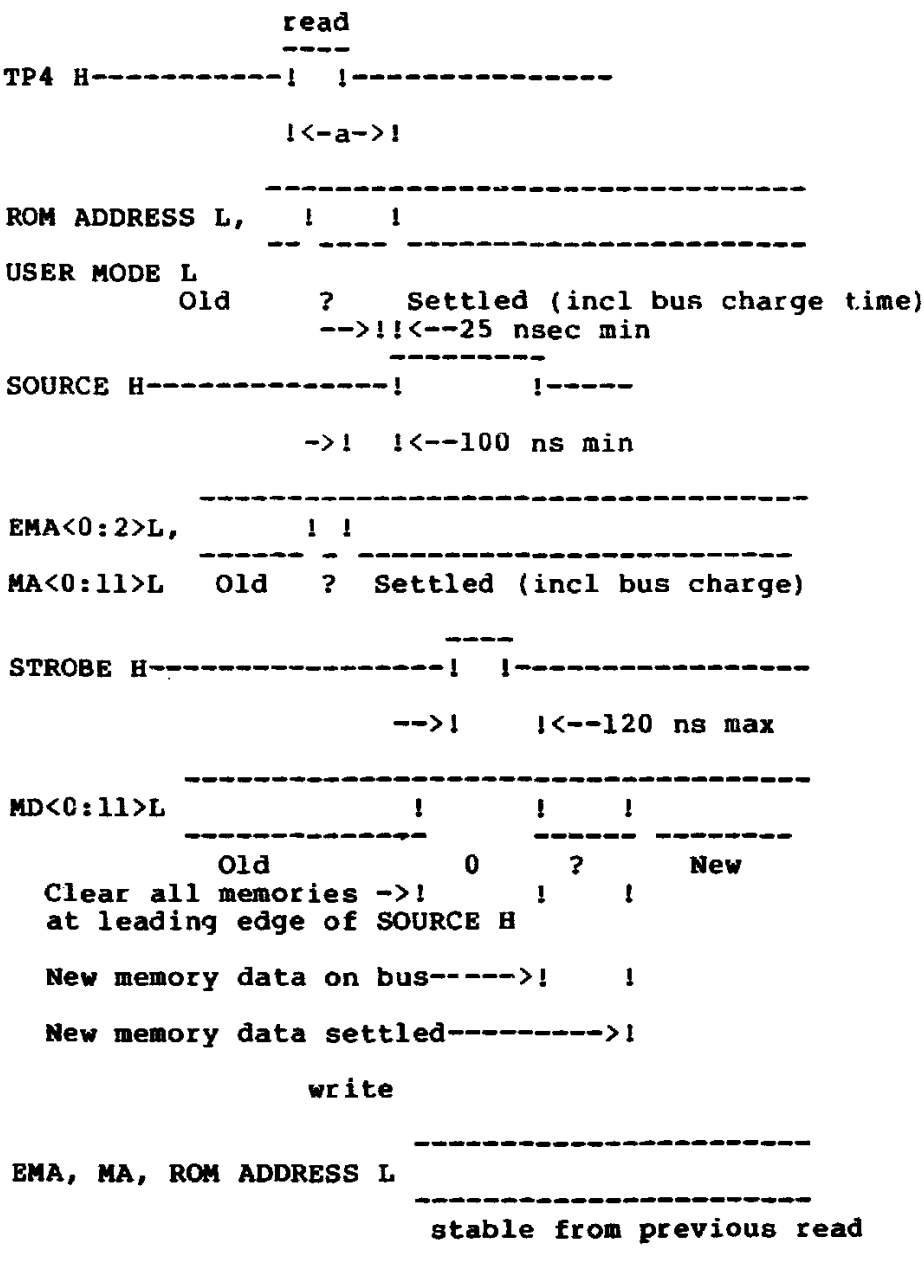
4.2 Memory Timing

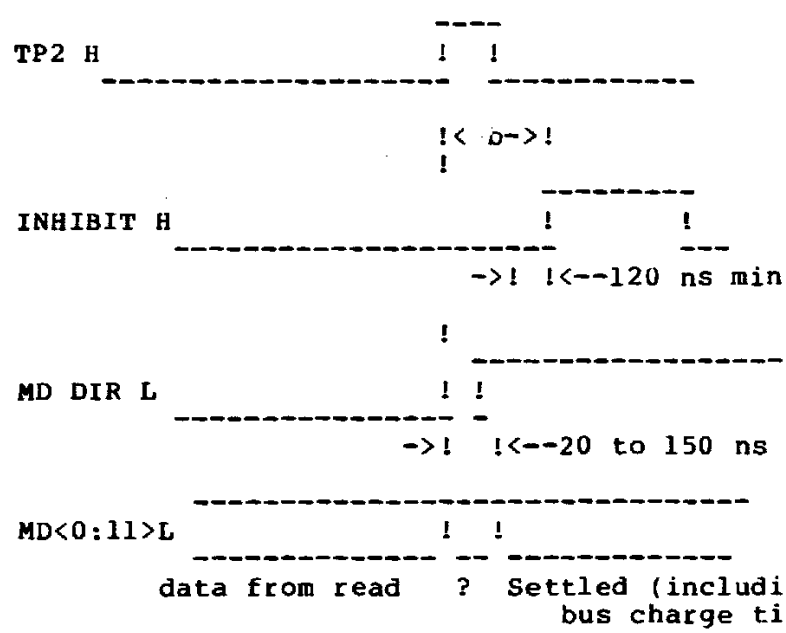
Normal memory timing is based on the PDP-8E's core memory, and is shown below:



Unless otherwise noted, all times above are + or - 10 nsec.

4.3 Relationship Between CPU And Memory Timing





MD<0:11>L changes at TP2 H only if MD DIR L is allowed to go high. If MD DIR L remains low, MD<0:11>L is settled on bus at STROBE H leading edge + 250 ns.

time in nanoseconds

	a	b
PDP-8E	150	250
PDP-8A	200	300

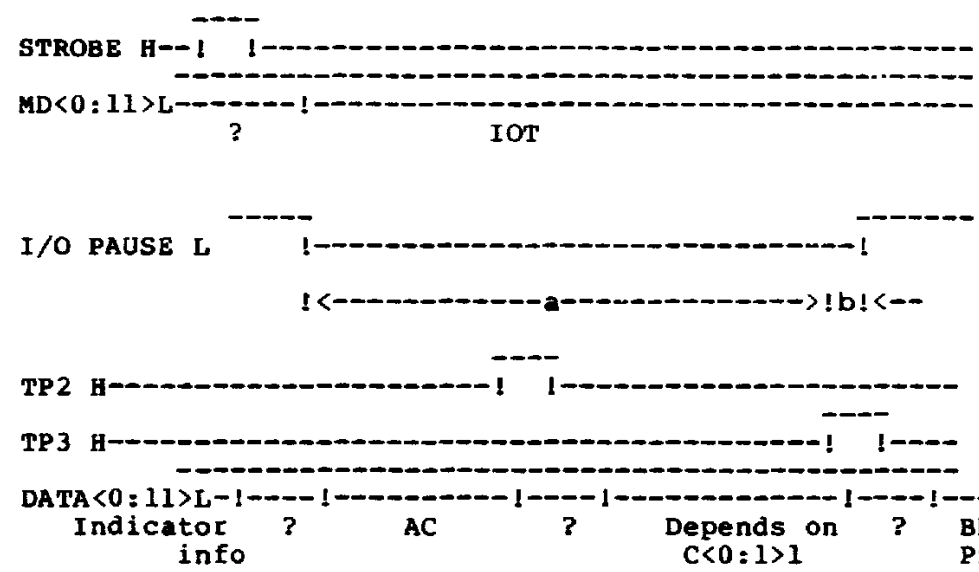
NOTE

The times given for PDP-8E and PDP-8A take into consideration the type of load on MD<0:11>L, EMA<0:2>L and MA<0:11>L and its position, plus maximum bus capacitance. A special bus-charging circuit in PDP-8E allows a charging time of less than the usual 100 nanoseconds.

4.4 Basic I/O Timing

4.4.1 This Timing Assumes: -

1. Single transfer during IOT
2. No modification of PC (no connection to C2 L).
3. C<0:1>L do not go to ground and then positive between the falling edge of I/O PAUSE L and the rising edge of TP3 H.

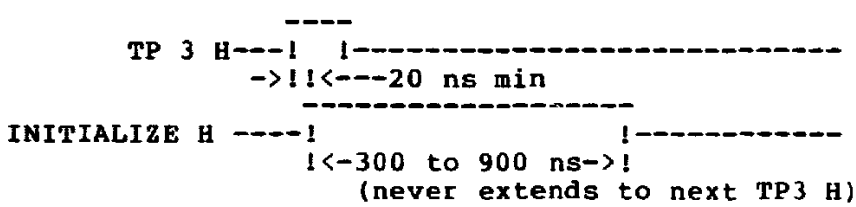


Dimension a
PDP-8E 350 to 450 nsec
PDP-8A: 450 to 550 nsec

Dimension b
50 nsec min, 100 ns max

Peripheral must place its data on DATA<0:11>L and assert any C lines at least 250 nsec prior to TP3 H. Skip L must be asserted at least 100 nsec before TP3 H if a skip is to occur. Peripheral registers are loaded at the leading edge of TP3 H. Peripheral registers must be edge-triggered, since DATA<0:11>L may start to change before TP3 H goes low again.

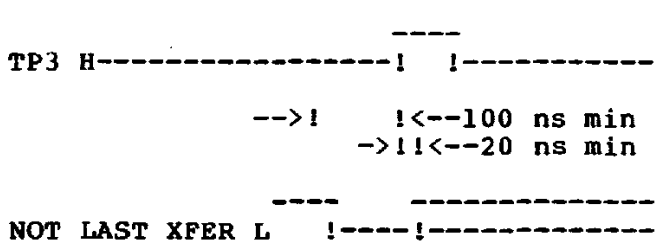
4.4.2 CAF Timing: -



4.5 Expanded I/O Timing

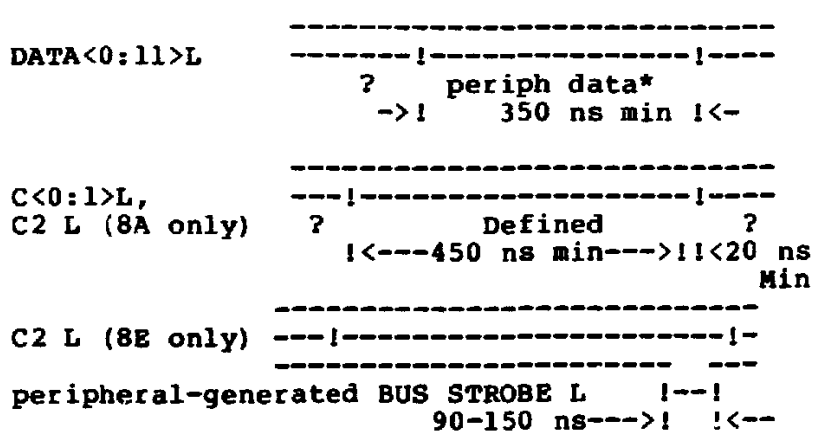
The restrictions of 4.4 regarding single transfer and limited use of C<0:2>L do not apply.

4.5.1
To stop the CPU (this operation is not confined to IOTs)



4.5.2

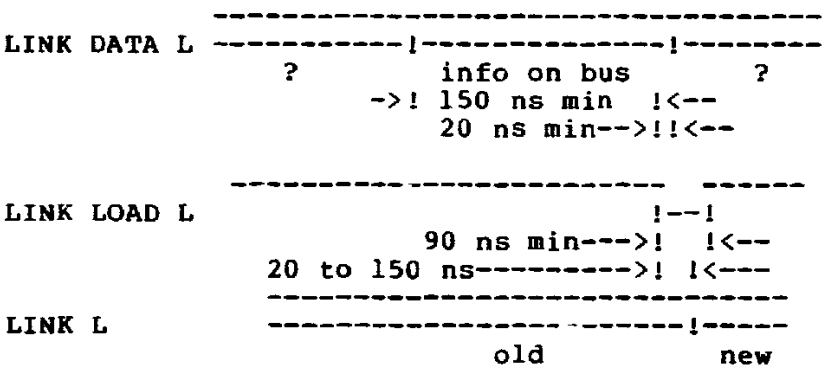
To make transfers to or from the AC, or to the PC:



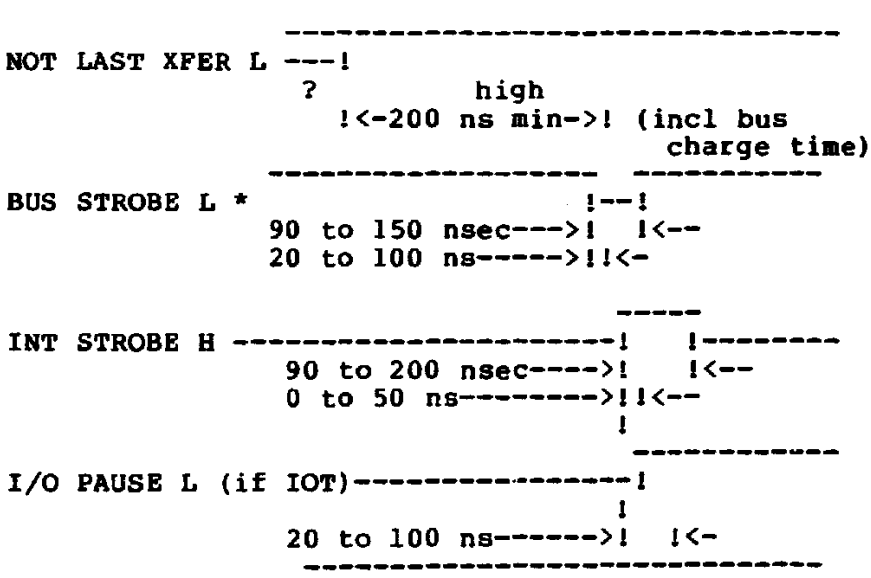
Peripheral data registers should be edge-triggered, and loaded at the leading edge of BUS STROBE L (since the contents of the Data bus may change as a result of sending BUS STROBE L to the CPU).

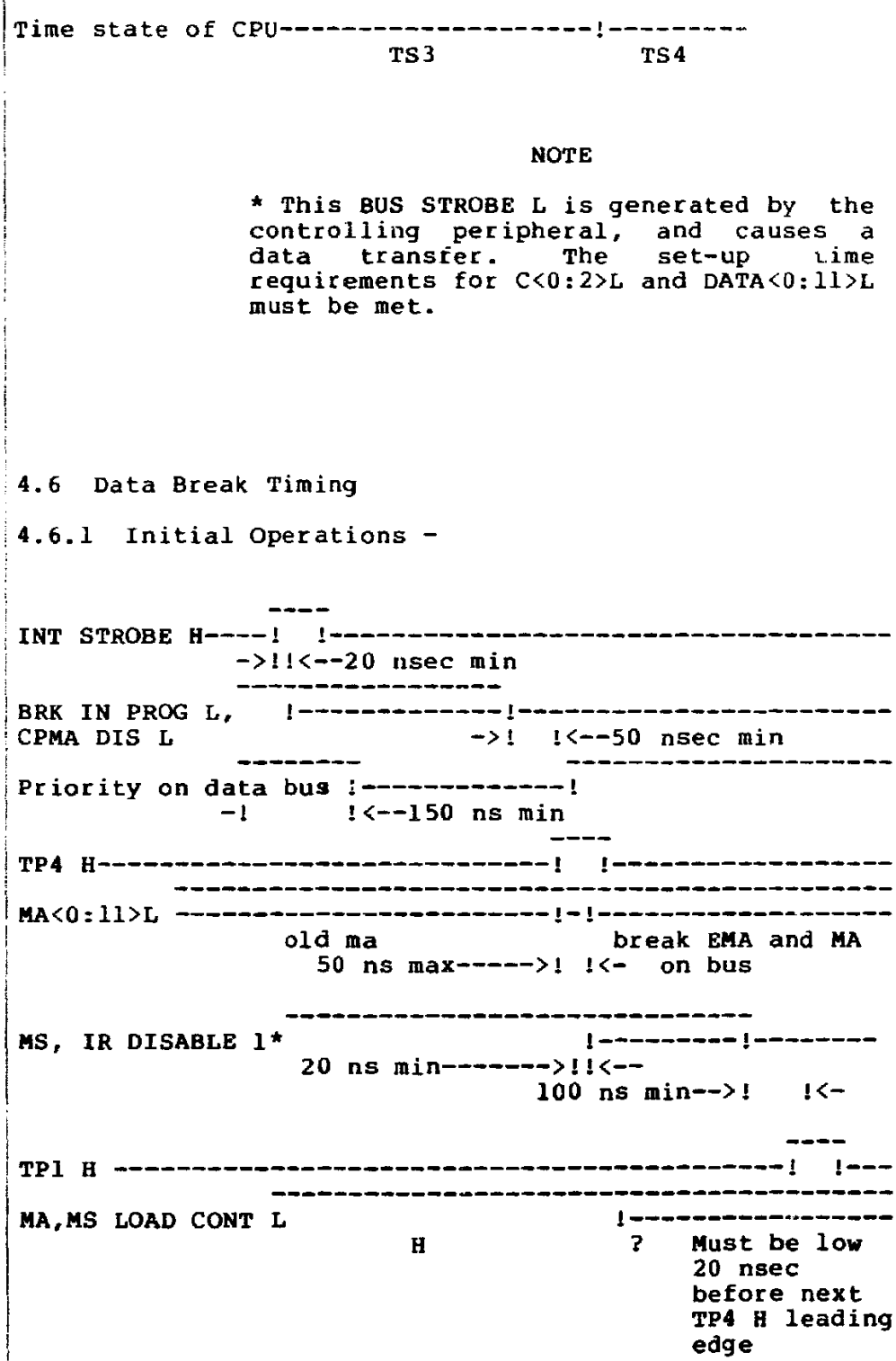
*If required for input transfer. The 350 nsec include 50 nsec for charging the bus.

4.5.3 External Loading Of Link - PDP-8A restriction: Must take place only in an expanded I/O cycle, and than not at restart time.



4.5.4 To Restart CPU: - Loading of Link not allowed because of timing restrictions as the CPU leaves TS3. (PDP-8A only)

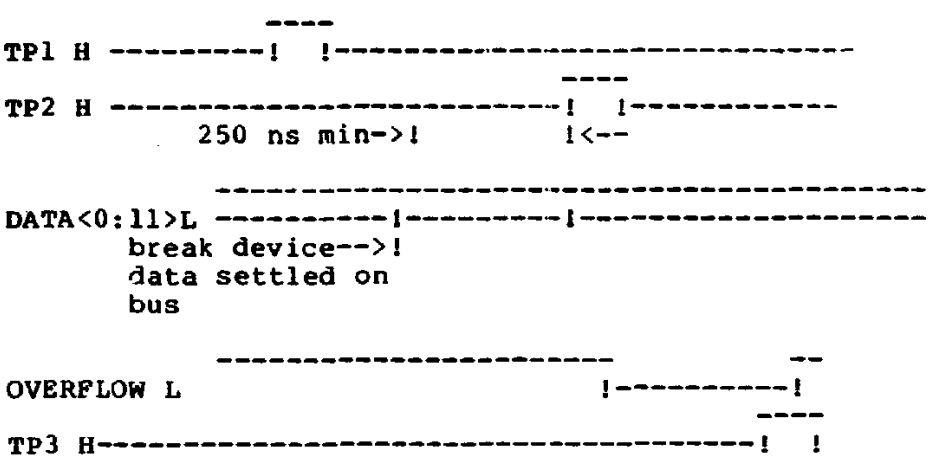




4.6 Data Break Timing

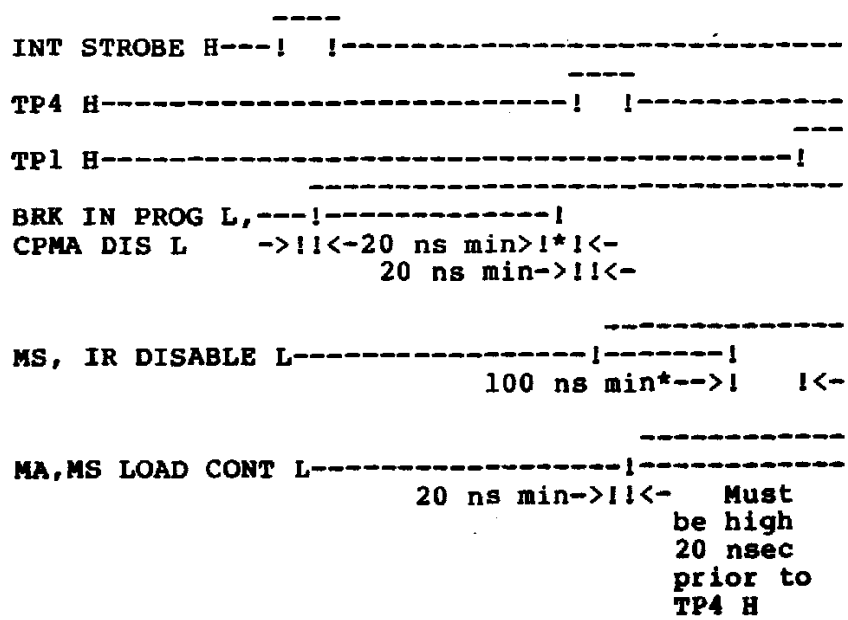
4.6.1 Initial Operations -

4.6.2 Data Exchange - Data to be placed in memory or used to modify memory must be in a register which has been loaded prior to TP1 H.



BREAK DATA CONT L must be settled on bus at same time as input data.

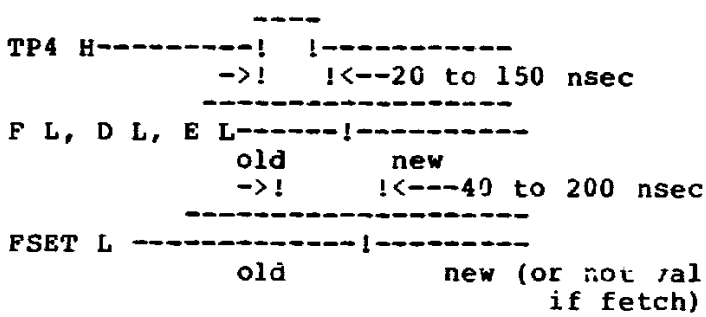
4.6.3 Final Operations -



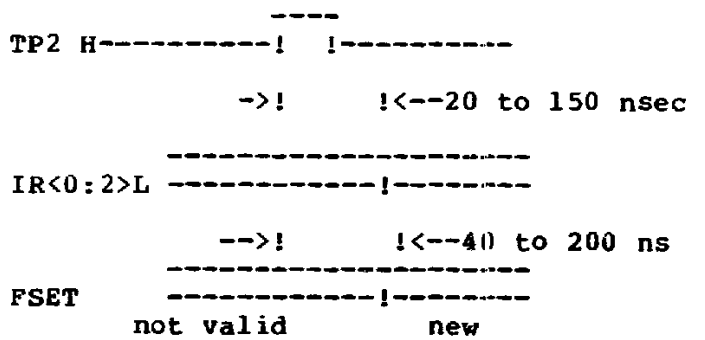
*Including bus charge time

4.7 CPU States, INT IN PROG H

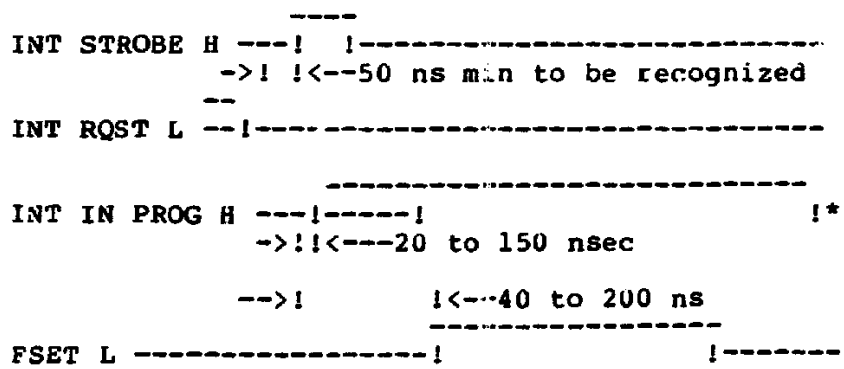
4.7.1 Major States -

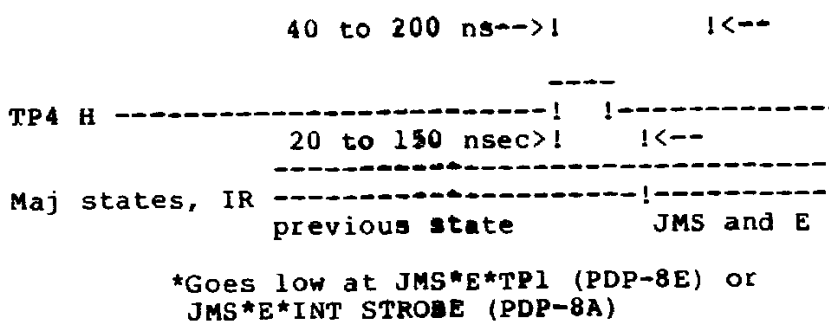


4.7.2 IR--Fetch Cycle -



4.7.3 Interrupt Recognition -

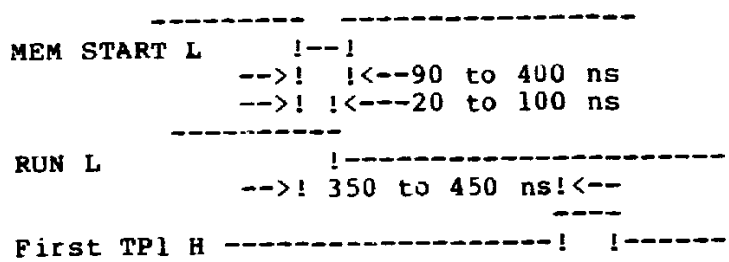




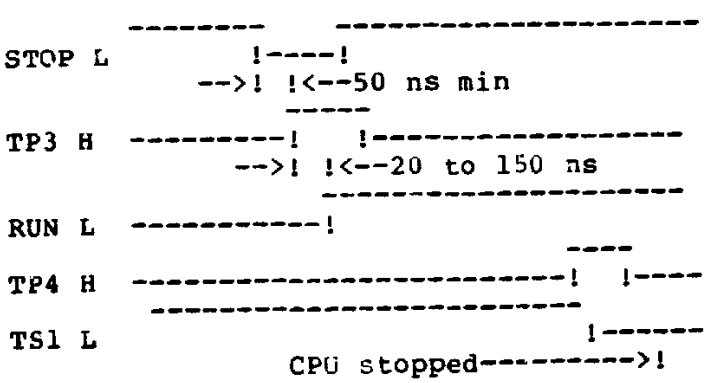
*Goes low at JMS*E*TP1 (PDP-8E) or
JMS*E*INT STROBE (PDP-8A)

4.8 Timing Start And Stop

4.8.1 Start -



4.8.2 Stop -



4.9 Asynchronous Signals

The following signals are allowed to change asynchronously with respect to the CPU's timing chain:

POWER OK H (when negated also causes
INITIALIZE H to change)

SW
IND1 L
IND2 L
INT RQST L
STOP L

4.10 Special Signals

The following signals should be asserted only when the CPU is not running:

MEM START L (see 4.8.1)
PULSE LA H (90 ns min width positive pulse)

5.0 ELECTRICAL CHARACTERISTICS AND INTERFACING

5.1 Logic Levels

Low = -0.5 volts to +0.4 volts
High = +2.7 volts to +4.5 volts.

5.2 Bus Loads

The characteristics and placement of bus terminating resistors has great influence on rise-time and reflection on the OMNIBUS. Refer to individual CPU specifications for the value and placement of these loads and their impact on bus length.

5.3 Driving The OMNIBUS

Drivers not on the CPU are open-collector, and should sink 25 microamperes or less at +5 volts (unless the number of drivers per line is limited to 10--leakage may then be increased to 250 microamperes.)

Signal	Driver must sink (ma) @ 0.4 v.
BREAK CYCLE L	16
BREAK DATA CONT L	16
BRK IN PROG L	16
BUS STROBE L	60 (that's right, sixty)
C0 L	16
C1 L	16
C2 L	16
CPMA DISABLE L	16
D L	30*
DATA<0:11>L	16 each line
E L	30*
EMA<0:2>L	30 each line
F L	30*
FSET L	Do not drive--may be TTL output
IND1 L	16
IND2 L	16
INHIBIT H	Do not drive--TTL output
INITIALIZE H	Special--See 5.3.1
INT IN PROG H	16
INT RQST L	16
INT STROBE H	Do not drive--TTL output
INTERNAL I/O L	16
I/O PAUSE L	Do not drive--TTL output
IR<0:2>L	16* each line
KEY CONTROL L	16
LA ENABLE L	16
LINK DATA L ,	16
LINK L	Do not drive
LINK LOAD L	60 (SIXTY!)
MA<0:11>L	30* each line
MA, MS LOAD CONT L	16
MD<0:11>L	16* each line (Memories only)
MD DIR L	30
MEM START L	16

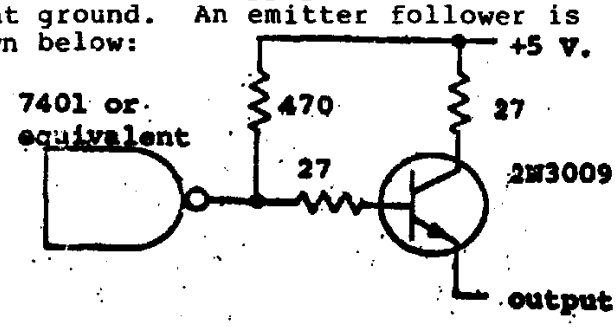
MS, IR DISABLE L	16
NOT LAST XFER L	16
NTS STALL L	16
OVERFLOW L	Do not drive
POWER OK H	Special--See 5.3.2
PULSE LA H	Special--See 5.3.2
RES	16
RETURN H	Do not drive--TTL output
ROM ADDRESS L	30
RUN L	Do not drive--May be TTL
SKIP L	16
SOURCE H	Do not drive--TTL output
STOP L	16
STROBE H	Do not drive--TTL output
TP1, 2, 3, 4 H	Do not drive--TTL output
TS1, 2, 3, 4 L	Do not drive--TTL output
USER MODE L	16
WRITE H	Do not drive--TTL output

Signals marked * are driven by Tri-state gates on PDP-8A. Users should not drive these lines unless the CPU is not driving them.

Signal	CPU not driving if
D L, E L, F L, IR<0:2>L	MS, IR DISABLE is low
MD<0:11 L	MD DIR L is high
EMA<0:2>L; MA<0:11>L	CPMA DISABLE L was low at leading edge of last TP4 H.

The DEC 8881 (P/N 19-09705) will meet the 16 and 30 ma requirement. Two 8881's in parallel will meet the 60 ma requirement.

5.3.1 INITIALIZE H And PULSE LA H - Driver must supply 30 ma at +3 volts, and source less than 1 ma at ground. An emitter follower is recommended. Typical circuit is shown below:



5.3.2 POWER OK H - This line is driven high by circuitry within the power supply, but can be grounded by options (such as the bootstrap loaders) which need to initialize the CPU and memory extension MA Control flip-flops. The power supply driver must supply a minimum of 30 ma at +3 volts, and must not supply more than 100 ma when the output is shorted to ground. Peripheral drivers must sink 200 ma at 0.4 volts. and sink less than 1 ma leakage at +5 volts.

5.4 Drive Available For Peripherals

The following currents are available for driving options, memories, etc, from the CPU and memory extension. Signals marked * are generally not used as output from CPU or memory extension.

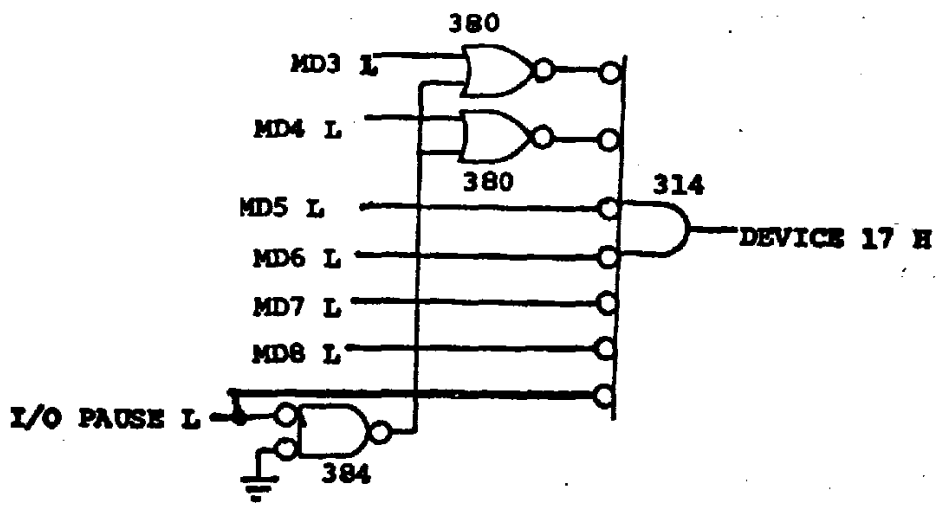
Signal	Source ma @ +3	Sink ma @ gnd
BREAK CYCLE L	3	5
BREAK DATA CONT L	3	5
BRK IN PROG L	3	5
BUS STROBE L	*	*
C<0:2>L	*	*
CPMA DISABLE L	*	*
D L	3	3
DATA<0:11>L	2	2
E L	3	3
EMA<0:2>L	3	3
F L	3	3
FSET L	5	5
IND1 L	*	*
IND2 L	*	*
INHIBIT H	10	10
INITIALIZE H	10	3
INT IN PROG H	2	2
INT RQST L	*	*
INT STROBE H	10	10
INTERNAL I/O	5	5
I/O PAUSE L	10	10
IR<0:2>L	3	3
KEY CONTROL L	3	3
LA ENABLE L	3	3

LINK DATA L	*	*
LINK L	5	5
LINK LOAD L	*	*
MA<0:11>L	5	5
MA,MS LOAD CONT L	*	*
MD<0:11>L	2	2
MD DIR L	3	3
MEM START L	*	*
MS, IR DISABLE L	*	*
NOT LAST XFER L	*	*
NTS STALL L	*	*
OVERFLOW L	5	5
RES	5	Depends on driver
RETURN H	10	10
ROM ADDRESS L	3	3
RUN L	5	5
SKIP L	*	*
SOURCE H	10	10
STOP L	*	*
STROBE H	10	10
TP<1:4>H	10	10 each
TS<1:4>L	10	10 each
USER MODE L	3	3
WRITE H	10	10

5.5 Receivers And Load Relief Techniques

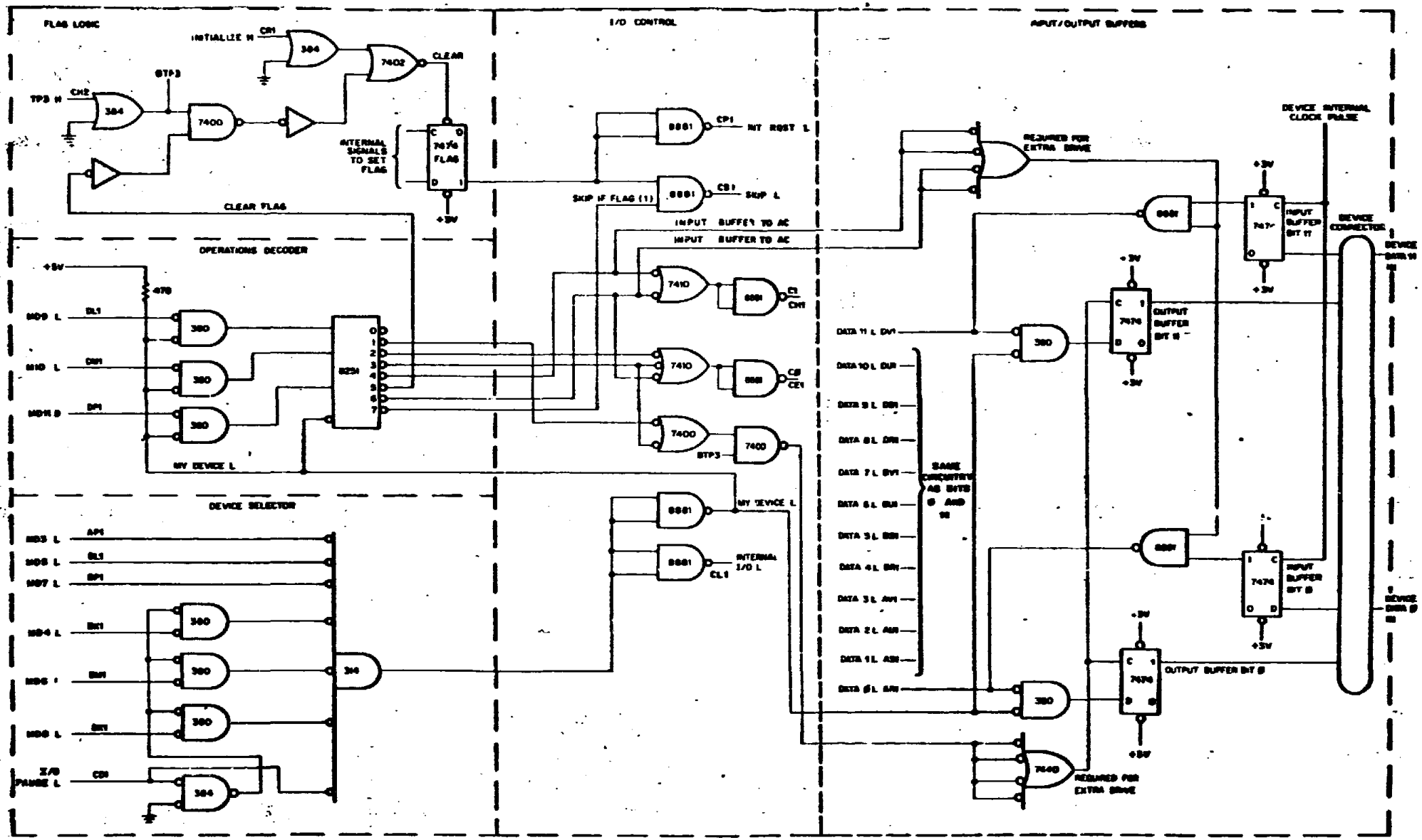
The use of Utilogic gates (Signetics SP314, SP380, etc) or other high-impedance circuits as bus receivers is strongly recommended. These gates have high threshold and low input drive, and thus present maximum noise immunity while introducing minimum bus reflections. Since 10 ma is available only on CPU timing and memory timing signals, buffering and load relief techniques must be used to decrease loading on the OMNIBUS.

A typical I/O decoder is shown below. Note the use of buffered I/O PAUSE L. This signal keeps the MD receivers from loading the MD lines, since buffered I/O PAUSE L supplies all needed base current to the three gates on the MD lines unless I/O PAUSE L is low.



similar techinques should be employed for signals from DATA<0:11>L to peripherals..

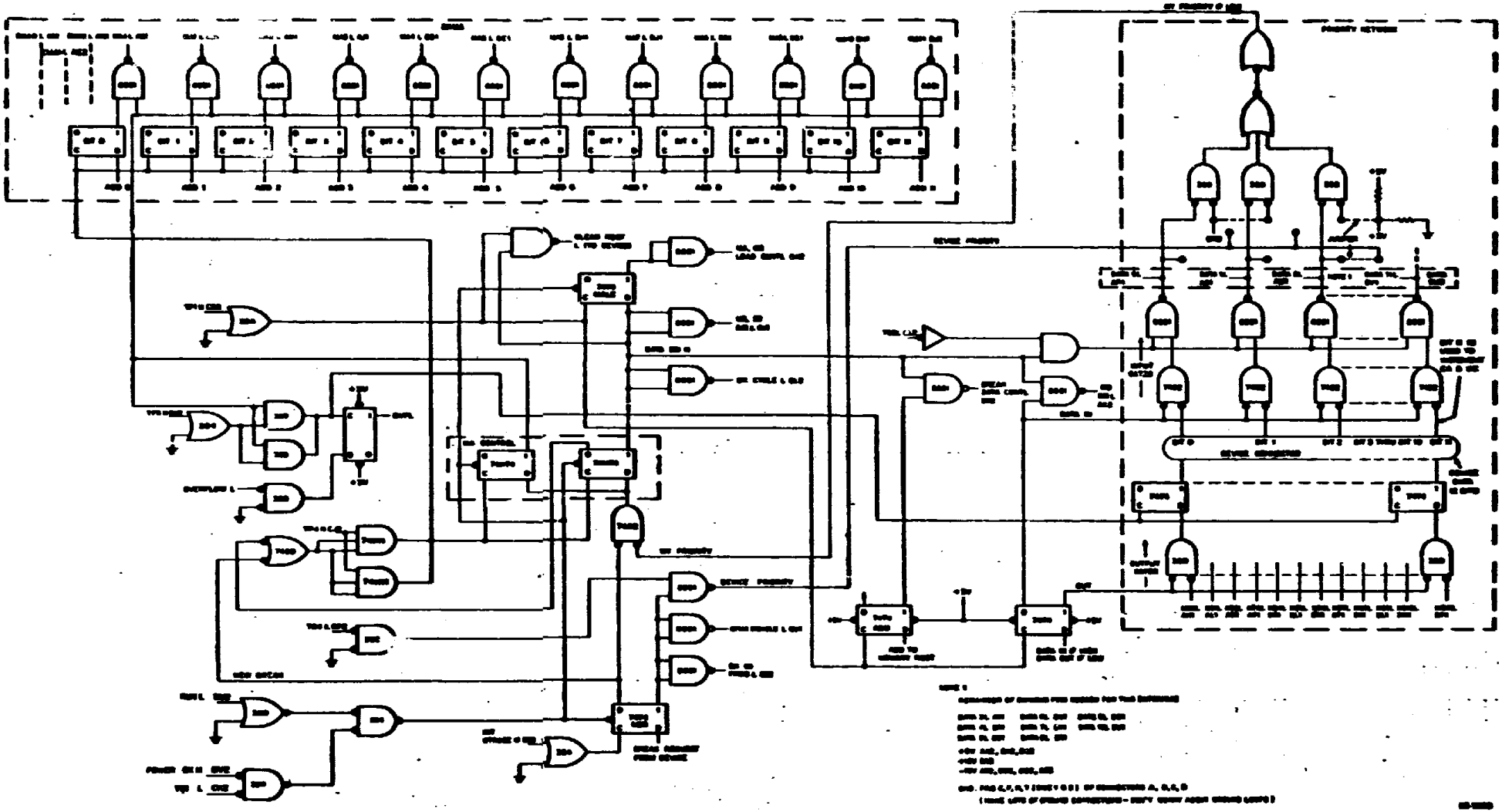
Sample I/O interface



+5 Volt: AA2, BA2, CA2
+15 Volt: BA2
-15 Volt: AB2, BB2, CB2, DB2, AC1, AC2, AF1, AF2, AH1, AH2, AT1, AT2, BC1, BC2, BF1, BF2, BH1, BH2, BT1, BT2, CC1, CC2, CF1, CF2, CH1, CH2, CT1, CT2, DC1, DC2, DF1, DF2, DH1, DH2, DT1, DT2
Ground*

*DON'T WORRY ABOUT GROUND LOOPS, MAKE LOTS OF GROUND CONNECTIONS.

Sample DMA (data break) interface



5.6 General Cautions Regarding Interfaces

1. Minimize capacitance on the OMNIBUS lines. The OMNIBUS will work properly only if the 100 ns allowed for bus charge time is met. Limit wire lengths on interface modules to 6 inches per signal. In general, this requirement means you should place bus receivers and drivers near the pins (which you will do anyway to minimize the crossovers if making a pc board).

2. Good ground grids on interface boards are mandatory.

3. Observe normal TTL rules for +5 volt bypassing. (Normal DEC bypassing is .01 mfd per IC, plus a 6.8 mfd tantalum capacitor where power supply voltage enters board.)

4. Except for gating EMA<0:2>L and MD<0:11> to bus (50 ns max), a peripheral has 100 ns to react.

5.7 Transmission Line Effects

Rise-times on the OMNIBUS are generally long compared to propagation velocities. Hence most OMNIBUS signals should be treated as capacitively-loaded lines. This trait is most pronounced on long busses.

Some signals driven by TTL drivers are a different matter entirely. These signals must either be kept short (less than 1 foot) and critical rise times controlled, or terminated at the far end of the bus from the CPU. The PDP-8A does the former; the PDP-8E, the latter. The signals which must be so treated are the nine CPU timing signals, the five memory timing signals and I/O PAUSE L. In addition, BUS STROBE L and LINK LOAD L must be terminated at both ends of the OMNIBUS with 150 ohms to +5 volts and 470 ohms to ground on long-bus machines. For short busses (less than 1 foot), a single resistor of 150 ohms to +5 volts in the CPU is sufficient. These terminating resistors are built into the CPU and/or bus loads modules.

It must be remembered that the characteristic impedance of the OMNIBUS itself (about 120 ohms) is a very small part of the overall picture. Of far more importance is the value and position of the capacitive load presented by boards connected to the OMNIBUS.

6.0 POWER SUPPLY REQUIREMENTS

The modules designed for use on the OMNIBUS have varying current requirements; hence it is not possible to present a comprehensive chart in this general specification. For the most part, however, voltage requirements are standard. The design of the power supply

should include good high-frequency bypassing at the output to keep noise on the power lines from affecting the system, and also to prevent the power supply from tending to oscillate under some dynamic load conditions. Also, the use of large wire diameters in the dc distribution lines from power supply to OMNIBUS is recommended.

6.1 +5 Volts

+5 volts dc is required for Vcc for the TTL logic, plus other needs. The TTL logic requirement is most stringent, and requires the +5 volt supply to deliver an absolute minimum of 5.0 v and an absolute maximum of 5.25 v. under all conditions of line, load, temperature and ripple. This requirement allows the power distribution system (cables and the OMNIBUS itself, plus board etch) a maximum of 250 mv. drop.

The +5 volt supply must be equipped with an over-voltage crowbar which is designed to prevent the +5 v. from ever exceeding 7.0 volts, to protect the integrated circuits from damage in the event of a power supply failure.

6.2 -15 Volts

-15 volts dc is used for some load resistors, as a memory supply voltage, and as a dc supply for EIA converters and other miscellaneous gear. It should be within + or - 5% of its nominal value for all conditions of load, line, temperature and ripple. The regulation may be relaxed to + or - 7.5% if core memory is not attached to the supply.

6.3

+15 volts +15 volt dc requirements are similar to those for -15 volts dc.

6.4 POWER OK H

POWER OK H is a logic signal, generated at the power supply, which reports to the OMNIBUS (Pin BV2) that the dc voltages are satisfactory. This signal should be negated on power application until the voltages are at least within their nominal range, and should be negated as soon as the regulation circuitry is in danger of saturation when the primary power is removed. It is desirable that this circuitry have hysteresis to prevent the "motorboating" oscillation that could result if there is an appreciable increase of current when the computer is started--which reduces the

voltages--which may cause the POWER OK H signal to be negated again, etc. The hysteresis should be greater than the change of voltage from no load to full load.

6.5

The computer should not be started until at least 0.5 seconds after POWER OK H has been asserted, but all devices should be ready to run 0.1 sec after POWER OK H is asserted.

7.0 INDEX OF OMNIBUS SIGNAL NAMES

Also see 5.2, 5.3 and 5.4

Signal name	Pin	Paragraphs where described
+5 Volts	AA2 BA2 CA2	1.03, 6.1
+15 Volts	DA2	1.03, 6.3
-15 Volts	AB2 BB2 CB2 DB2	1.03, 6.2
BREAK CYCLE L	BL2	2.5, 3.5.7, 4.6.1, 4.6.3
BREAK DATA CONT L	BK2	2.5, 3.5.5, 3.9.9, 4.6.2
BRK IN PROG L	BE2	2.5, 3.5.1, 4.6.1, 4.6.3
BUS STROBE L	CK1	2.4, 3.4.6, 4.5
C0 L	CE1	2.4, 3.4.5, 4.4, 4.5
C1 L	CH1	2.4, 3.4.5, 4.4, 4.5
C2 L	CJ1	2.4, 3.4.5, 4.5
CPMA DISABLE L	CU1	2.5, 3.5.2, 4.6.1, 4.6.3
D L	DK2	2.7, 3.7.1, 4.7
DATA0 L	AR1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA1 L	AS1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA2 L	AU1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA3 L	AV1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA4 L	BR1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA5 L	BS1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA6 L	BU1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA7 L	BV1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA8 L	DR1	2.3, 3.3, 4.4, 4.5.2, 4.6.2

DATA9 L	DS1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA10 L	DU1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
DATA11 L	DV1	2.3, 3.3, 4.4, 4.5.2, 4.6.2
E L	DL2	2.7, 3.7.1, 4.7
EMA0 L	AD2	2.1, 3.1, 4.3
EMA1 L	AE2	2.1, 3.1, 4.3
EMA2 L	AH2	2.1, 3.1, 4.3
F L	DJ2	2.7, 3.7.1, 4.7
FSET L	DP2	2.9, 3.9.6, 4.7.1
Ground	AC1	1.03
	AF1	
	AN1	
	AT1	
Ground (cont)	AC2	1.03
	AF2	
	AN2	
	AT2	
Ground (cont)	BC1	1.03
	BF1	
	BN1	
	BT1	
Ground (cont)	BC2	1.03
	BF2	
	BN2	
	BT2	
Ground (cont)	CC1	1.03
	CF1	
	CN1	
	CT1	
Ground (cont)	CC2	1.03
	CF2	
	CN2	
	CT2	
Ground (cont)	DC1	1.03
	DF1	
	DN1	
	DT1	
Ground (cont)	DC2	1.03
	DF2	
	DN2	
	DT2	
IND1 L	CU2	2.9, 3.9.1, 4.9
IND2 L	CV2	2.9, 3.9.1, 4.9
INHIBIT H	AP2	2.8, 3.8.3, 4.2

INITIALIZE H	CR1	2.4, 3.4.8
INT IN PROG H	BP2	2.9, 3.9.8, 4.7.3
INT RQST L	CP1	2.4, 3.4.4, 4.7.3
INT STROBE H	BD2	2.6, 3.6, 4.1
INTERNAL I/O L	CL1	2.4, 3.4.2
I/O PAUSE L	CD1	2.4, 3.4.1, 4.4, 4.5
IR0 L	DD2	2.7, 3.7.2, 4.7
IR1 L	DE2	2.7, 3.7.2, 4.7
IR2 L	DH2	2.7, 3.7.2, 4.7
KEY CONTROL L	DU2	2.9, 3.9.9
LA ENABLE L	BM2	2.9, 3.9.9
LINK DATA L	CR2	2.9, 3.9.5, 4.5.3
LINK L	AV2	2.9, 3.9.4, 4.5.3
LINK LOAD L	CS	2.9, 3.9.5, 4.5.3
MA0 L	AD1	2.1, 3.1, 4.3
MA1 L	AE1	2.1, 3.1, 4.3
MA2 L	AH1	2.1, 3.1, 4.3
MA3 L	AJ1	2.1, 3.1, 4.3
MA4 L	BD1	2.1, 3.1, 4.3
MA5 L	BE1	2.1, 3.1, 4.3
MA6 L	BH1	2.1, 3.1, 4.3
MA7 L	BJ1	2.1, 3.1, 4.3
MA8 L	DD1	2.1, 3.1, 4.3
MA9 L	DE1	2.1, 3.1, 4.3
MA10 L	DH1	2.1, 3.1, 4.3
MA11 L	DJ1	2.1, 3.1, 4.3
MA, MS LOAD CONT L	BH2	2.5, 3.5.4, 4.6.1, 4.6.3
MD0 L	AK1	2.2, 3.2, 4.3
MD1 L	AL1	2.2, 3.2, 4.3
MD2 L	AM1	2.2, 3.2, 4.3
MD3 L	AP1	2.2, 3.2, 4.3
MD4 L	BK1	2.2, 3.2, 4.3
MD5 L	BL1	2.2, 3.2, 4.3
MD6 L	BM1	2.2, 3.2, 4.3
MD7 L	BP1	2.2, 3.2, 4.3
MD8 L	DK1	2.2, 3.2, 4.3
MD9 L	DL1	2.2, 3.2, 4.3
MD10 L	DL1	2.2, 3.2, 4.2
MD11 L	DP1	2.2, 3.2, 4.3
MD DIR L	AK2	2.2, 3.2, 4.3
MEM START L	AJ2	2.9, 3.9.2, 4.8.1, 6.5
MS, IR DISABLE L	CV1	2.5, 3.5.3, 4.6.1, 4.6.3

NOT LAST XFER L	CM1	2.4, 3.4.7, 4.5
NST STALL L	BR2	2.9, 3.9.12
OVERFLOW L	BJ2	2.5, 3.5.6, 4.6.2
POWER OK H	BV2	2.9, 3.9.14, 4.9, 6.4
PULSE LA H	DR2	2.9, 3.9.10, 4.10
RES	BS2	2.9, 3.9.15
RETURN H	AR2	2.8, 3.8.1, 4.2
ROM ADDRESS L	AU2	2.9, 3.9.11, 4.3
RUN L	BU2	2.5, 3.5.8, 4.8
SKIP L	CS1	2.4, 3.4.3, 4.4
SOURCE H	AL2	2.8, 3.8.1, 4.2
STOP L	DS2	2.9, 3.9.3, 4.8.2
STROBE H	AM2	2.8, 3.8.4, 4.2
SW	DV2	2.9, 3.9.13
Test point	AA1	1.03
	AB1	
	BA1	
	BB1	
Test point (cont)	CA1	1.03
	CB1	
	DA1	
	DB1	
TP1 H	CD2	2.6, 3.6, 4.1
TP2 H	CE2	2.6, 3.6, 4.1
TP3 H	CH2	2.6, 3.6, 4.1
TP4 H	CJ2	2.6, 3.6, 4.1
TS1 L	CK2	2.6, 3.6, 4.1
TS2 L	CL2	2.6, 3.6, 4.1
TS3 L	CM2	2.6, 3.6, 4.1
TS4 L	CP2	2.6, 3.6, 4.1
USER MODE L	DM2	2.9, 3.9.7, 4.3
WRITE H	AS2	2.8, 3.8.2, 4.2

8.0 GLOSSARY OF REFERENCE DOCUMENTS

8.1

For detailed description of the PDP8 instruction set as well as peripheral I/O instructions see; PDP8/A MINIPROCESSOR HANDBOOK.

8.2

For detailed logic information on the CPU and selected I/O options see; 8A FAMILY PRINT SET number MP-00177.