

digital

RX01

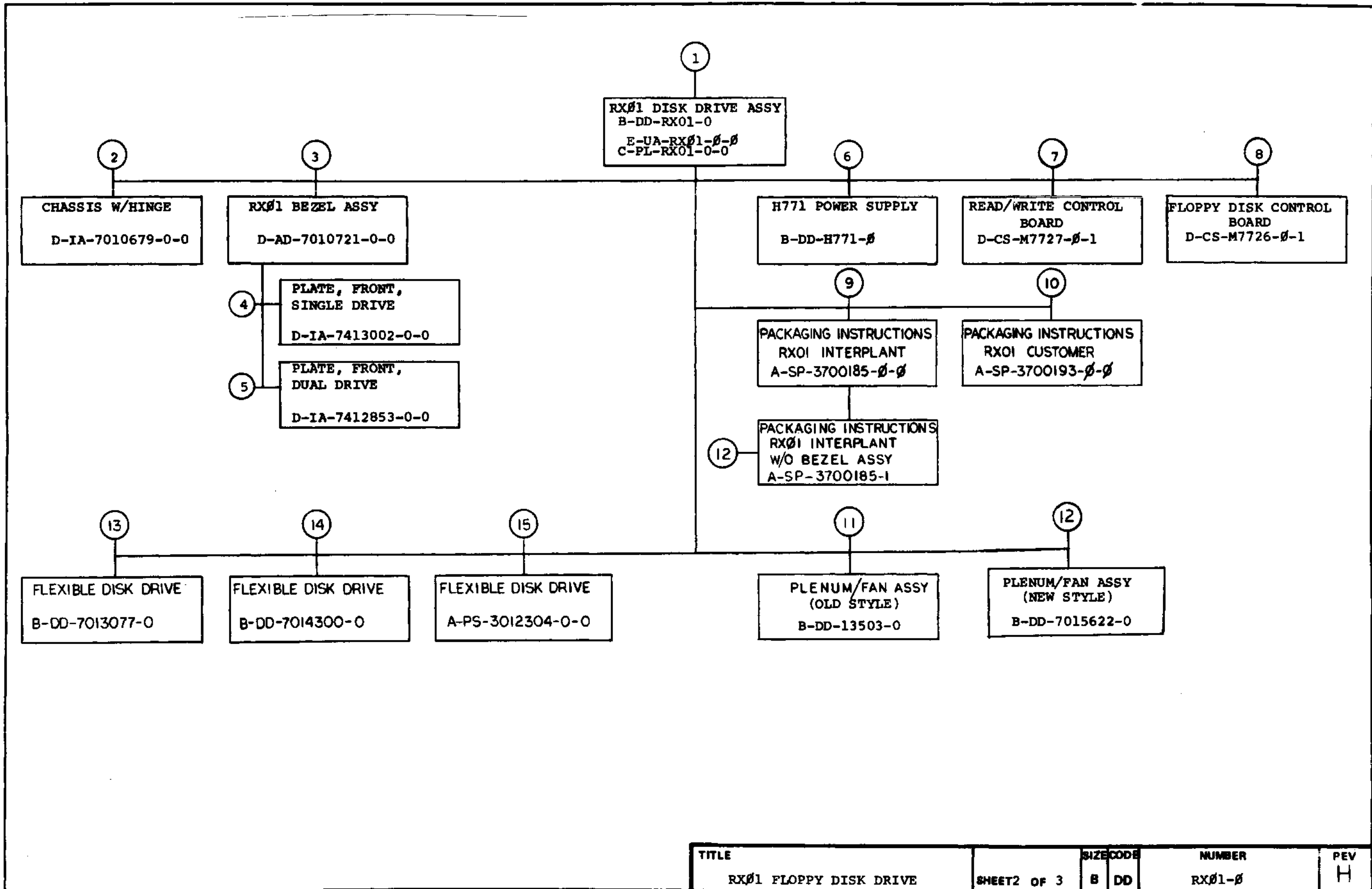
Engineering Drawings

Digital Equipment Corporation

The material herein is for information purposes only and is subject to change without notice. Digital Equipment Corporation assumes no responsibility for any errors which may appear herein.

These drawings and specifications herein are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

Copyright © 1975, Digital Equipment Corporation



TITLE	SHEET	OF	SIZE	CODE	NUMBER	REV
RX01 FLOPPY DISK DRIVE	SHEET 2	OF 3	B	DD	RX01-0	H

ML

MECHANICAL					ELECTRICAL						
CUSTOMER PRINT SET	MPG. SET	FIND NO.	DRAWING NO.	NO OF REV SHT	OPTION NO./FILE DATE	CUSTOMER PRINT SET	MPG. SET	FIND NO.	DRAWING NO.	NO OF REV SHT	OPTION NO./FILE DATE
		1	E-IA-RX01-0-0	5	RX01 FLOPPY DISK DRIVE ASSY	X		1	B-DD-RX01-0	# 3	RX01 FLOPPY DISK DRIVE
			B-PL-RX01-0-0		RX01 FLOPPY DISK DRIVE ASSY(PI)			1	C-MD-7413350-0-0	1	SHIPPING BRACKET
			E-IA-7412666-0-0	1	COVER, TOP						
			D-IA-7010646-0-0	1	CABLE, EXTENSION, RX01						
			C-IA-7008612-0-0	1	CABLE, KEYBOARD				A-SP-RX01-0-1	34	RX01 ENGINEERING SPECIFICATION
			D-IA-BC05L-0-0	1	CABLE, JUMPER				K-SP-RX01-0-2		RX01 FIRMWARE LISTING
			D-IA-7010696-0-0	1	HARNES, VOLTAGE VARIATION						
				1	BRACKET, SHIPPING, RX01						
			C-MD-7409479-0-0	1	PLATE, PRESSURE			12	A-SP-3700185-1		PACK INSTR W/O BEZEL
			C-MD-5509081-0-0	1	PANEL, LIGHT (RX01)				A-PS-9905183		LAMINATED BUILDUP
									A-PS-9905710-0-0		REGULAR SLOTTED CARTON
									A-PS-9905712-0-0		PLYWOOD SUPPORT FIXTURE
									A-PS-9905713-0-0		SCORED SHEET
									A-PS-9905729-0-0		CARTON SEALING TAPE
		2	D-IA-7010679-0-0	1	CHASSIS W/HINGE						
			E-IA-7412665-0-0	1	CHASSIS, FLEXIBLE DISK DRIVE						
			C-MD-7413236-0-0	1	HINGE, LOGIC						
		3	D-AD-7010721-0-0	1	RX01 BEZEL ASSY						
			E-MD-7414506-0-0	1	BEZEL, RX01	X		7	D-CS-M7727-0-1	# 6	READ/WRITE CONTROL BOARD
			A-PS-3612317-0-0	1	LOGO, RX01				D-IA-5011370-0-0	1	ETCHED CIRCUIT BOARD (M7727)
		4	D-IA-7413002-0-0	1	PLATE, FRONT, SINGLE DRIVE						
			C-SS-7413002-0-1	1	SILK SCREEN, SINGLE DRIVE	X		8	D-CS-M7726-0-1	# 9	FLOPPY DISK CONTROL BOARD
									A-SP-M7726-0-7	3	ACCEPTANCE TEST PROCEDURE
		5	D-IA-7412853-0-0	1	PLATE, FRONT, DUAL DRIVES						
			C-SS-7412853-0-1	1	SILK SCREEN, DUAL DRIVE						
C		6	B-DD-H771-0	# 3	H771 POWER SUPPLY			9	A-SP-3700185-0-0		PACKAGING INST. INTERPLANT
			C-MD-7413350-0-0						A-PS-9905710-0-0		REGULAR SLOTTED CARTON
									A-PS-9905711-0-0		ONE PIECE FOLDER
									A-PS-9905712-0-0		PLYWOOD SUPPORT FIXTURE
									A-PS-9905713-0-0		SCORED SHEET
									A-PS-9905729-0-0		CARTON SEALING TAPE
X		11	B-DD-7013503-0-0	3	PLENUM/FAN ASSY (OLD STYLE)						
		13	B-DD-7013077-0	3	FLEXIBLE DISK DRIVE			10	A-SP-3700193-0-0		PACKAGING INST. CUSTOMER
									A-PS-9905741-0-0		FULL TELESCOPE CAP
									A-PS-9905740-0-0		FOAM PAD
									A-PS-9905739-0-0		LAMINATED BUILDUP
									A-PS-9905734-0-0		PLASTIC STRAPPING
		15	A-PS-3012304-0-0	14	FLEXIBLE DISK DRIVE						
		16	B-DD-7015622-0-0	2	PLENUM/FAN ASSY NEW STYLE						

CUSTOMER PRINT SET
 X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
 C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
 S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

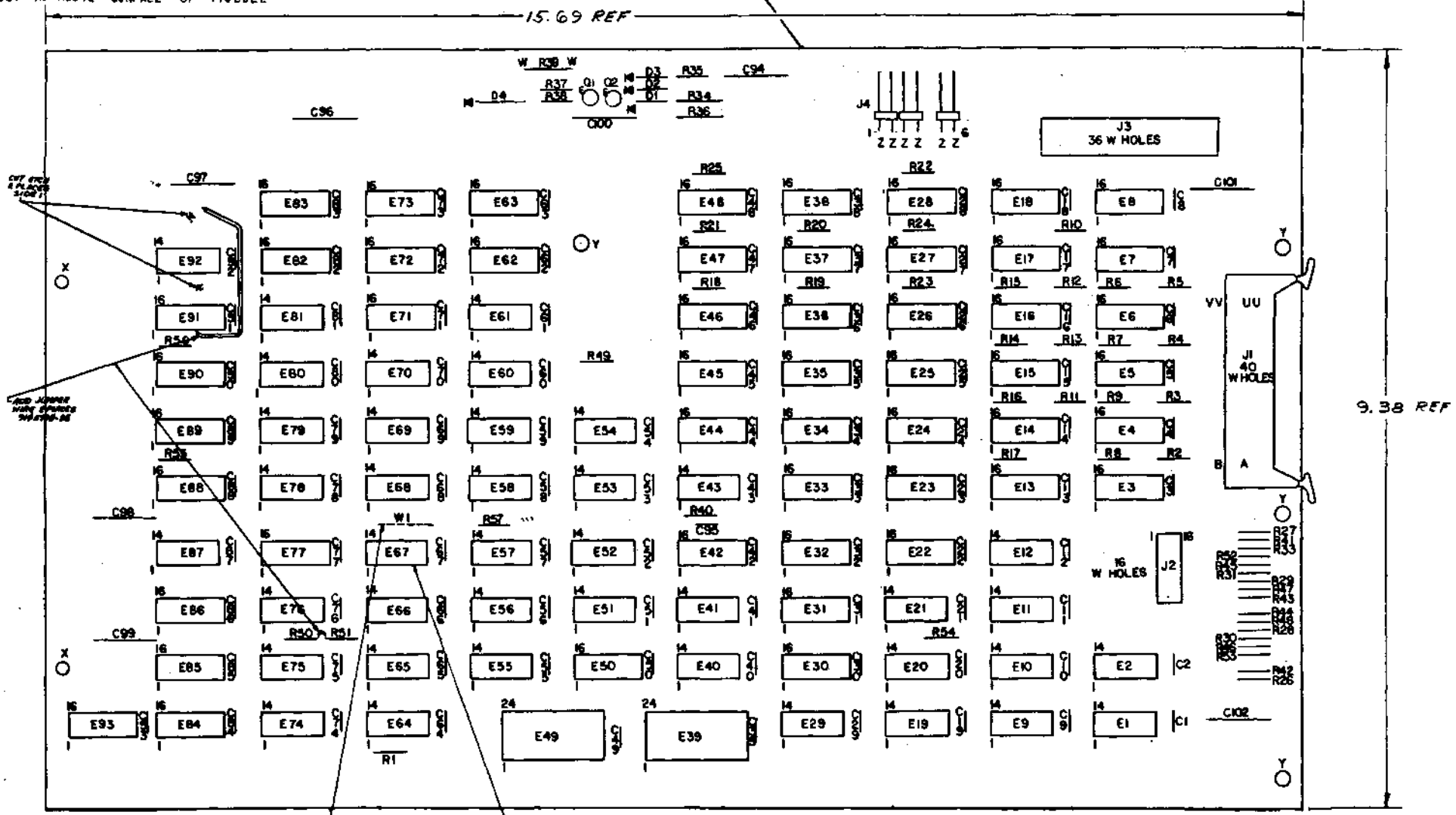
TITLE
 RX01 FLOPPY DISK DRIVE
 SHEET³ OF³
 SIZE CODE
 B DO
 NUMBER
 RX01-0
 REV
 H

ML

THIS DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ANY EQUIPMENT WITHOUT WRITTEN PERMISSION.
 COPYRIGHT © 1974 DIGITAL EQUIPMENT CORPORATION

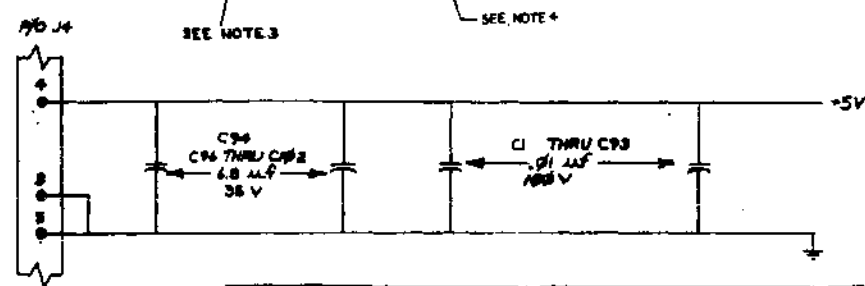
NOTES:

- ⊙ REPRESENTS A 1/8 DIA PAD LOCATED ON SIDE 2 UNLESS OTHERWISE SPECIFIED
- ALL RESISTORS ARE 1/4 W, ± 5%
 A. ALL UNUSED PINS FOR T1 ARE TIED TO GND
 B. INSTALL JUMPER W1 AFTER MODULE TEST
- INSTALL JUMPER W1 AFTER MODULE TEST
- MOUNT E47 1/4" ABOVE SURFACE OF MODULE



23-XXXA2	8	16
2102	9	18
8640	1	8
74175	8	16
74174	8	16
74161	8	16
74134	8	16
74123	8	16
74H103	11	4
74H106	13	5
7489	8	16
74150	12	24
7442	8	16
8266	8	16
74193	8	16
74154	12	24
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE
 IC PIN LOCATIONS



H. DRAB 12/15/77
H. DRAB 11-09-77
H. DRAB 4-1-77
29 MAR 77
17726-00006 H
4/14/76
3-31-76
17726-00005 F
CHARLES YOUSE
12-15-75
17726-00004 E
17726-00003 D
17726-00002 C
17726-00001 B
 REV. CHANGE NO. REV.
 SEMICONDUCTOR CONVERSION CHART

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.											
FIRST USED ON OPTION MODEL M7726															
ETCH BOARD REV. B															
PARTS LIST															
<table border="1"> <tr><td>DATE</td><td>11/27/74</td></tr> <tr><td>DATE</td><td>11/9/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> </table>					DATE	11/27/74	DATE	11/9/75	DATE	11/21/75	DATE	11/21/75	DATE	11/21/75	
DATE	11/27/74														
DATE	11/9/75														
DATE	11/21/75														
DATE	11/21/75														
DATE	11/21/75														
<table border="1"> <tr><td>DATE</td><td>11/21/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> <tr><td>DATE</td><td>11/21/75</td></tr> </table>					DATE	11/21/75	DATE	11/21/75	DATE	11/21/75	DATE	11/21/75	DATE	11/21/75	
DATE	11/21/75														
DATE	11/21/75														
DATE	11/21/75														
DATE	11/21/75														
DATE	11/21/75														
NEXT HIGHER ASSY															
<table border="1"> <tr><td>SCALE</td><td>1</td><td>of 9</td></tr> <tr><td>SHEET</td><td>1</td><td>of 9</td></tr> </table>					SCALE	1	of 9	SHEET	1	of 9					
SCALE	1	of 9													
SHEET	1	of 9													
<table border="1"> <tr><td>SIZE CODE</td><td>D</td><td>CS</td><td>M7726-0-1</td><td>REV.</td><td>J</td></tr> <tr><td>TITLE</td><td colspan="4">FLOPPY DISK CONTROLLER</td></tr> </table>					SIZE CODE	D	CS	M7726-0-1	REV.	J	TITLE	FLOPPY DISK CONTROLLER			
SIZE CODE	D	CS	M7726-0-1	REV.	J										
TITLE	FLOPPY DISK CONTROLLER														

D CS M7726-0-1

THIS DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF THIS PRODUCT WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1972 DIGITAL EQUIPMENT CORPORATION.

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
REF		X-Y COORDINATE HOLE LOCATION	KCC-M7726-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AM-M7726-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7726-0-6	3
1		ETCHED CIRCUIT BOARD	5011390	4
1	J3	BECEP 36 PIN (BEWORK)	8-MD-3309-02-1	5
1	J2	I.C. SOCKET, 16 PIN GOLD, LOW PROFILE	1211813-02	6
1	R37	RES 1M 1/4W 5% CE	1300479-00	7
8	C 94, C96 - C102	CAP 6.8 uF 35V 10% STANT	1005306-00	8
93	C1 - C93	CAP .01 uF 50V AXIAL CER	1001610-00	9
1	C95	CAP 12 PF 100V 5%	1002087-00	10
3	D1 - D3	DIODE 1N4004	1105796-00	11
1	D4	DIODE 1N746A 3.3V 5%	1104860-00	12
1	R 39	RES 100 1/2W 5% CC	1300228-00	13
3	J4	HEADER, 2 PIN (MALE)	1212204-00	14
8	R2, R4, R6, R8, R10, R12, R14, R16	RES 470 1/4W 5% CC	1300316-00	15
8	R27, R29, R31, R47, R52, R43, R41, R45	RES 390 1/4W 5% CC	1300309-00	16
5	R1, R49 - R51, R57	RES 3K 1/4W 5% CC	1300432-00	17
5	R26, R28, R30, R38	RES 100 1/4W 5% CC	1301322-00	18
5	R42, R44, R46, R48, R53	RES 820 1/4W 5% CC	1301775-00	19
1	R35	RES 300 1/4W 5% CC	1301425-00	20
8	R18 - R25	RES 2K 1/4W 5% CC	1302388-00	21
1	R34	RES 261 1/4W 1% MF	1302878-00	22
1	R36	RES 287 1/4W 1% MF	1305124-00	23
1	R40	RES 8.2K 1/4W 5% CC	1303179-00	24
3	R54 - R56	RES 1K 1/4W 5% CC	1300365-00	25
1	Q2	TRANS MIX A805	1510705-00	26
1	Q1	TRANS MIX A855	1510706-00	27
5	E19, E20, E21, E29, E40	I.C. 7474	1905547-00	28
3	E9, E57, E59	I.C. 7400	1905575-00	29
2	E93, E60	I.C. 7410	1905576-00	30
1	E75	I.C. 7450	1905580-00	31
1	E55	I.C. 74H20	1905635-00	32
1	E54	I.C. 7402	1909004-00	33
2	E68, E72	I.C. 74H00	1909056-00	34
2	E56, E70	I.C. 74H11	1909267-00	35
5	E50, E69, E70, E79, E82	I.C. 74H74	1909667-00	36
2	E64, E76	I.C. 7404	1909686-00	37
1	E39	I.C. 74154	1909701-00	38
2	E1, E2	I.C. 8001	1909705-00	39
1	E61	I.C. 74H04	1909931-00	40
2	E74, E92	I.C. 7486	1910011-00	41
4	E08, E09, E90, E91	I.C. 74193	1910018-00	42
2	E27, E37	I.C. 8266	1909934-00	43
1	E22	I.C. 7402	1910046-00	44
1	E65	I.C. 7437	1910091-00	45
1	E49	I.C. 74150	1910153-00	46
2	E11, E12	I.C. 7408	1910155-00	47
2	E97, E98	I.C. 7489	1910396-00	48
5	E58	I.C. 74H106	1910408-00	49
3	E00, E81, E87	I.C. 74H103	1910409-00	50
1	E42	I.C. 74123	1910436-00	51

REVISIONS		
CHR	CHANGE NO.	REV.

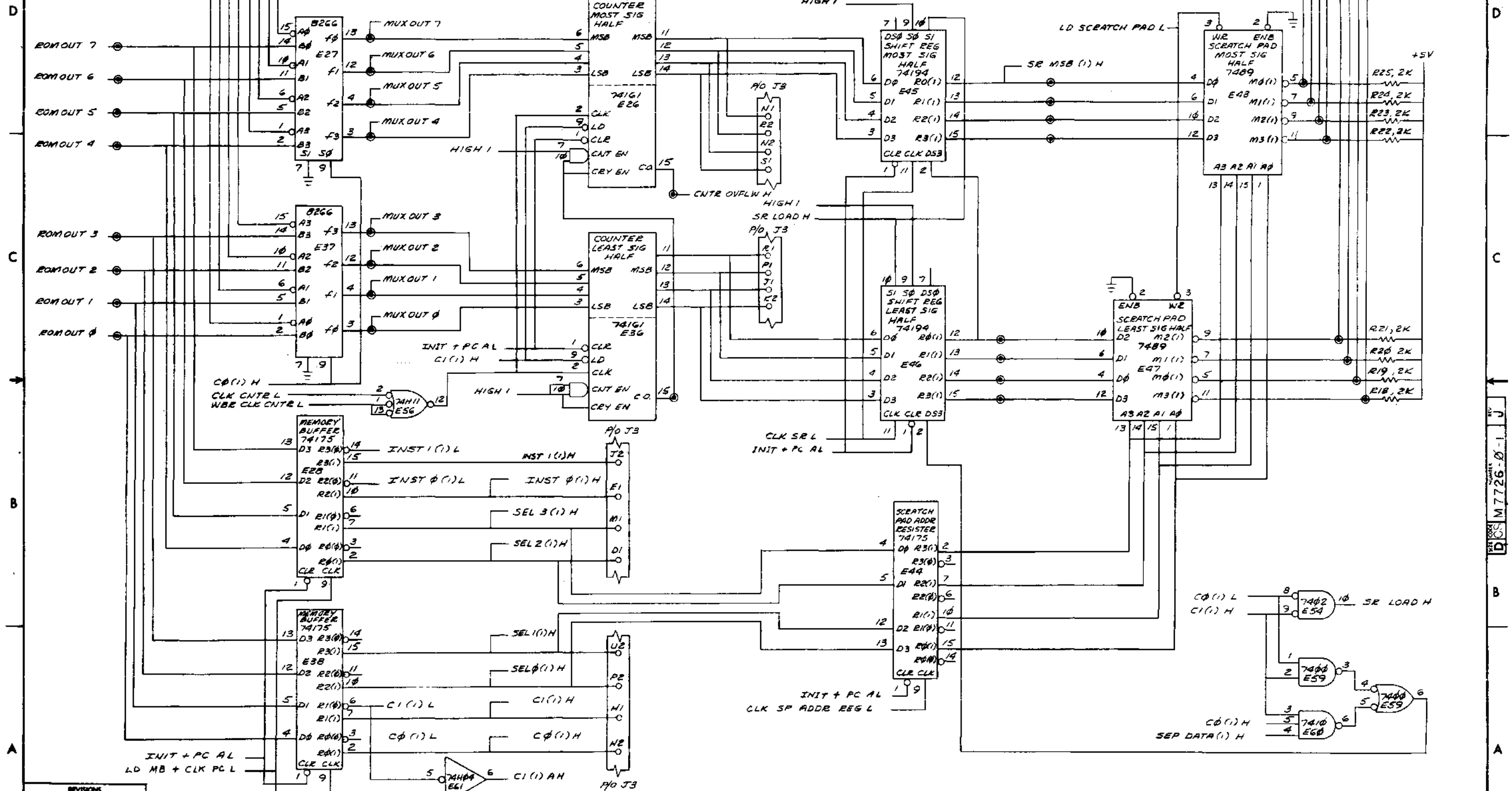
PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
2	E45, E46	I.C. 74194	1910623-00	52
8	E23, E24, E25, E26, E30, E31, E32, E36	I.C. 74161	1910650-01	53
3	E84, E85, E86	I.C. 74174	1910652-00	54
1	E53	I.C. 7427	1910878-00	55
3	E28, E38, E44	I.C. 74175	1910631-00	56
2	E10, E66	I.C. 8640	1911469-00	57
1	E33	I.C. 2182 680 NS	2111318-02	58
				59
6	E35, E39, E62, E63, E73, E83	SAME IC SIZES		60
1	E67	CRYSTAL OSCILLATOR 20MHZ	1811660-00	61
4	E41, E71, E93, E52	I.C. 74574	1910544-00	62
1	E51	I.C. 74H10	1909057-00	63
1	E77	I.C. 74H40	1908884-00	64
				65
1	J1	330 AWG SOLID WIRE (WEL)	910200-55	66
1	J1	CONN 40 PIN RT ANG HDR	1209941-02	67
1	(J1)	LATCH, LEFT FOR RT ANG HDR	1209941-03	68
1	(J1)	LATCH, RIGHT FOR RT ANG HDR	1209941-04	69
1	E13	I.C. 256 X 4 ROM FLD0L	23111A2	70
1	E14	I.C. 256 X 4 ROM FLD0H	23421A2	71
1	E14	I.C. 256 X 4 ROM FLD1L	23257A2	72
1	E4	I.C. 256 X 4 ROM FLD1H	23268A2	73
1	E15	I.C. 256 X 4 ROM FLD2L	23115A2	74
1	E5	I.C. 256 X 4 ROM FLD2H	23116A2	75
1	E16	I.C. 256 X 4 ROM FLD3L	23117A2	76
1	E6	I.C. 256 X 4 ROM FLD3H	23118A2	77
1	E17	I.C. 256 X 4 ROM FLD4L	23259A2	78
1	E7	I.C. 256 X 4 ROM FLD4H	23260A2	79
1	E18	I.C. 256 X 4 ROM FLD5L	23121A2	80
1	E8	I.C. 256 X 4 ROM FLD5H	23122A2	81
1	R33	RES 150 1/4W 5% CC	1300250-00	82

SAME I.C. GATES			
TYPE	LOCATION	PINS	DESCRIPTION
74H04	E81	1,2	INVERTER
7404	E64	12,13	INVERTER
7404	E76	12,13	INVERTER
7408	E11	1,2,3,8,9,10	2 INPUT NAND
74H00	E72	1,2,3,8,9,10	2 INPUT NAND
7437	E66	8,9,10	2 INPUT NAND BUFFER
8851	E2	8,9,10	2 INPUT NAND CC.
74H10	E51	3,4,5,6	3 INPUT NAND
74H00	E77	1,2,4,5,6	4 INPUT NAND BUFFER
7402	E84	4,5,6	2 INPUT NOR
8640	E66	2,6,7,11,12,13,14,15	2 INPUT NOR RCVR
7427	E53	1,2,12,13	2 INPUT NOR
7406	E92	4,5,6	2 INPUT XOR
7406	E74	1,2,3,4,5,6	2 INPUT XOR
74574	E93	1,2,2,4,5,6	DTYPE FLIP FLOP
74H06	E50	1,2,3,4,14,15,16	J K FLIP FLOP
74123	E42	1,2,3,4,13,14,15	ONE SHOT

ALLOWABLE SUBSTITUTIONS				
PREFERRED		REPLACEMENT		
TYPE	ITEM #	P.N.	TYPE	P.N.
7489	48	1910396-00	3101A	1910653-00
7489	48	1910396-00	8225	191162-00

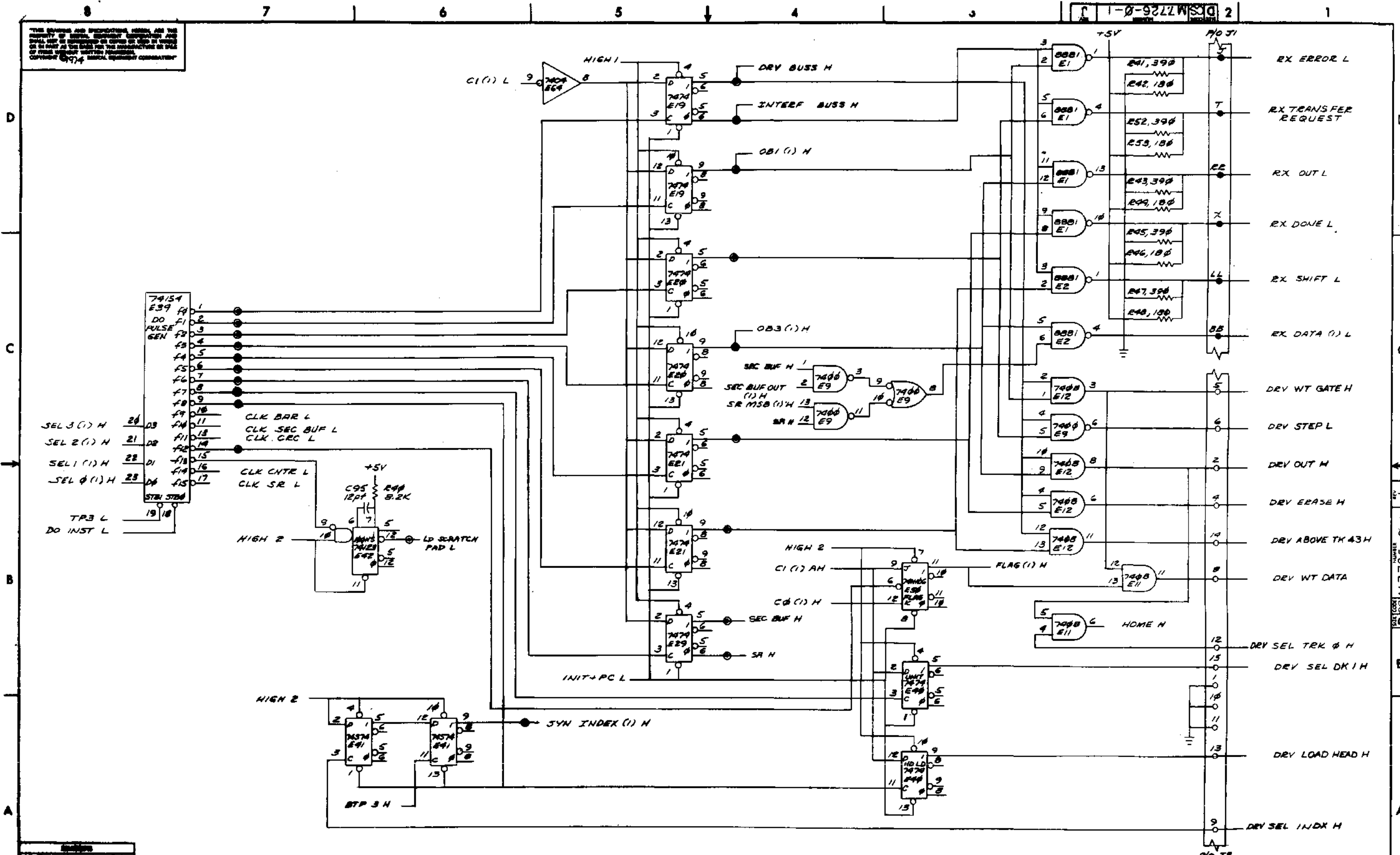
THE DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1974 DIGITAL EQUIPMENT CORPORATION



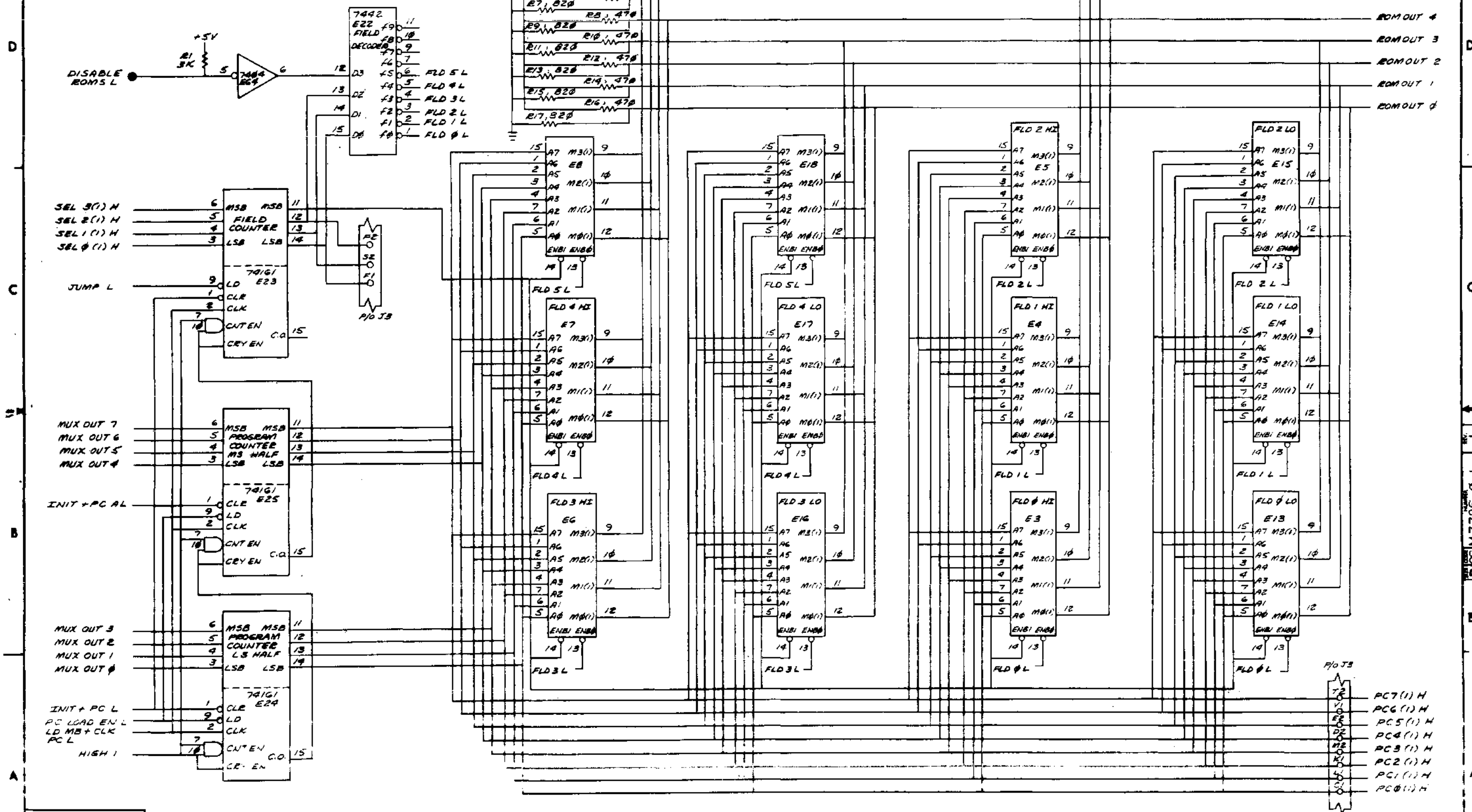
REVISIONS		
CHK	CHANGE NO.	REV.

THIS DRAWING AND SPECIFICATIONS HEREON ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1974. SERIAL OPERATING COMMENTARY.

DCS M7726-0-1

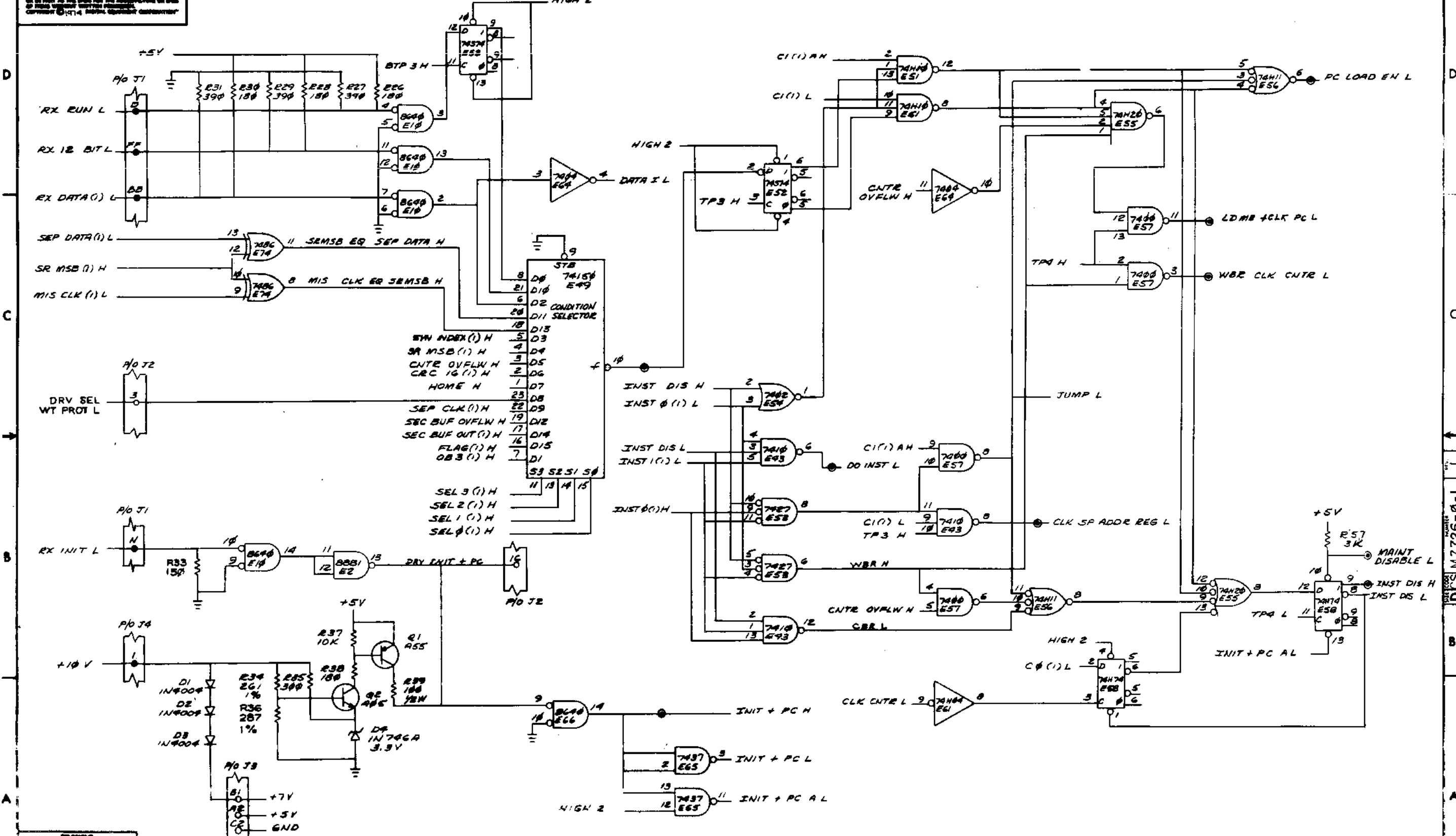


THE DESIGN AND EXERCISES HEREIN ARE THE PROPERTY OF DCS. REPRODUCTION OR TRANSMISSION IN ANY FORM OR BY ANY MEANS IS PROHIBITED WITHOUT THE WRITTEN PERMISSION OF DCS. © 1974 DCS SYSTEMS CORPORATION



REVISIONS		
CHK	CHANGE NO.	REV.

THE SCHEMATIC AND SPECIFICATION SHEETS ARE THE PROPERTY OF DATA GENERAL CORPORATION AND SHALL NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF DATA GENERAL CORPORATION.



REV. NO.	DATE	BY	CHKD	APP'D	TITLE	SCALE	SHEET	OF	NO.	DATE	REV.
					FLOPPY DISK CONTROLLER (DB)		8	9			J

D CS M7726-0-1 J

THE SYMBOLS AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DECORAL. NO PART OF THIS DOCUMENT SHALL BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT PERMISSION IN WRITING FROM DECORAL CORPORATION.

THIS LIST GIVES THE SOURCE AND DESTINATIONS OF SIGNAL NAMES WITHIN THE M7726 PRINT SET. SIGNAL NAMES THAT DO NOT APPEAR ON THIS LIST ARE PRESENT FOR INFORMATION ONLY. THEY DO NOT INDICATE CONNECTIONS TO OTHER POINTS IN THE PRINT SET.

INTERFACE REFERS TO SIGNALS ON THE INTERFACE 0000
DRIVE REFERS TO SIGNALS ON THE DRIVE 0000
POWER SUPPLY REFERS TO VOLTAGES FROM THE POWER SUPPLY
KN11 REFERS TO SIGNALS ON J1 THE MAINTENANCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION
STP 3 H	D7-C1	D4-A5, D5-A6, D8-D6
CLK BAR L	D5-C7	D4-A3
CLK CTRL L	D5-B7	D3-B7, D8-A4
CLK CMC L	D5-C7	D7-B7
CTRL OVFWR H	D3-C8	D8-D4, D8-C6, D8-B4
CLK SEC DUT L	D5-C7	D4-A2
CLK SP ADDR RES L	D8-B3	D1-A4
CLK SR L	D5-B7	D3-B4
CONTIN L	KN11	D7-C7
CNC16 (1) H	D7-B1	D8-C6
CNC16 (1) L	D7-A1	D7-B7
C1 (1) AN	D3-A6	D4-B3, D5-B4, D8-D4, D8-C4
C1 (1) H	D3-A6	D3-C6, D3-B3, D7-B8
C1 (1) L	D3-A6	D5-D8, D7-B8, D8-D4, D8-B4
C8 (1) H	D3-A6	D3-C7, D3-A2, D4-B1, D5-B4, D7-B8
C8 (1) L	D3-A6	D3-B2, D4-B3, D7-B8, D8-B3
DATA I L	D8-D8	D4-A2
DISABLE BORG L	TEST PAD	D4-D8
DO INBT L	D8-B4	D5-B8
DRY BORG H	D5-D4	D4-A4
DRY ERASE H	D5-B1	DRIVE
DRY OUT H	D5-C1	DRIVE
DRY LOAD HEAD H	D5-A1	DRIVE
DRY STEP L	D5-C1	DRIVE
DRY INIT + PC	D8-B4	DRIVE
DRY ABOVE TH 43 H	D5-B1	DRIVE
DRY RAM DATA L	DRIVE	D4-A8
DRY SEL CLK 1 H	D5-B1	DRIVE
DRY SEL INK H	DRIVE	D5-A1
DRY SEL TRK 0 H	DRIVE	D5-B1
DRY WT DATA	DRIVE	D5-B1
DRY WT GATE H	D5-C1	DRIVE
DRY SEL WT PROT L	DRIVE	D8-C8
END WIND L	D4-D3	D4-D8
ERROR NUT ENABLE L	KN11	D7-C7

FLAG (1) H	D5-B3	D8-D6
FLD 0 L	D8-D8	D8-B3, D8-B2
FLD 1 L	D8-D8	D8-B3, D8-B2
FLD 2 L	D8-D8	D8-C3, D8-C2
FLD 3 L	D8-D8	D8-A8, D8-A4
FLD 4 L	D8-D8	D8-B8, D8-B4
FLD 5 L	D8-D8	D8-C8, D8-C4
HALT H	D7-C3	KN11
HALT L	KN11	D7-C7
HIGH 1	D7-C4	D3-D8, D3-D4, D3-C8, D3-C4, D4-A3
HIGH 2	D7-B4	D4-B1, D5-D5, D8-A8
HIGH 3	D7-B4	D4-A3, D5-B7, D5-A7, D5-D4, D7-B8
HOME H	D7-B4	D7-D4, D7-C4, D7-C8, D8-D8, D8-B1
HOME L	D5-B2	D8-A8
INIT + PC A L	D8-A4	D3-C6, D3-D4, D3-A4, D3-A7, D4-B4
INIT + PC H	D8-A4	D4-B5, D6-B8, D7-C3, D8-B2
INIT + PC L	D8-A4	D4-B5, D4-C9, D7-D4
INST 0 (1) H	D3-D8	D4-B1, D5-D5, D8-A8
INST 0 (1) L	D3-D8	KN11, D8-B5
INST 1 (1) H	D3-D8	D8-C3
INST 1 (1) L	D3-D8	KN11
INST DIS H	D8-B1	D8-B5
INST DIS L	D8-B1	D8-C3
INTENT BORG H	D8-D4	D8-B8
JUMP L	D8-C3	D7-B8
LD RM + CLK PC L	D8-C1	D8-A8, D3-A8
LD SCRATCH PAD L	D5-B4	D3-A3
RAINY DIS L	TEST PAD	D8-B1
RIS CLK (1) L	D4-C4	D8-C8
RIS OUT 0	D3-C7	D8-A8
RIS OUT 1	D3-C7	D8-A8
RIS OUT 2	D3-C7	D8-A8
RIS OUT 3	D3-C7	D8-B8
RIS OUT 4	D3-C7	D8-B8
RIS OUT 5	D3-B7	D8-B8
RIS OUT 6	D3-B7	D8-B8
RIS OUT 7	D3-B7	D8-B8

OB1 (1) H	D5-D4	D7-B8
OB2 (1) H	D5-C4	D8-B8
PC 0 (1) H	D6-A1	KN11
PC 1 (1) H	D6-A1	KN11
PC 2 (1) H	D6-A1	KN11
PC 3 (1) H	D6-A1	KN11
PC 4 (1) H	D6-A1	KN11
PC 5 (1) H	D6-A1	KN11
PC 6 (1) H	D6-A1	KN11
PC 7 (1) H	D6-A1	KN11
PC LOAD EN L	D8-D1	D8-A8
ROM OUT 0	D6-D1	D3-C9
ROM OUT 1	D6-D1	D3-C8
ROM OUT 2	D6-D1	D3-C8
ROM OUT 3	D6-D1	D3-C8
ROM OUT 4	D6-D1	D3-C8
ROM OUT 5	D6-D1	D3-D8
ROM OUT 6	D6-D1	D3-D8
ROM OUT 7	D6-D1	D3-D8
RX DATA (1) L	D5-C1, INTERFACE	INTERFACE, D8-D8
RX DONE L	D5-D1	INTERFACE
RX ERROR L	D5-D1	INTERFACE
RX INIT L	INTERFACE	D8-B8
RX OUT L	D5-D1	INTERFACE
RX PUN L	INTERFACE	D8-D8
RX SHIFT L	D5-C1	INTERFACE
RX TRANSFER REQUEST	D5-D1	INTERFACE
RX 12 HIT L	INTERFACE	D8-D8
SIX BUF OVFWR H	D4-A1	D8-C6
SIX BUF OUT (1) H	D4-C1	D5-C4, D8-B6
SIX BUF H	D5-A4	D5-C4
SFL 0 (1) H	D3-A6	D5-C8, D6-C9, D8-B4, KN11
SFL 1 (1) H	D3-B8	D5-C8, D6-C9, D8-B4, KN11
SFL 2 (1) H	D3-B8	D5-C8, D6-C9, D8-B4, KN11
SFL 3 (1) H	D3-B8	D5-C8, D6-C9, D8-B4, KN11
SEP CLK (1) H	D4-B4	D8-C8
SEP DATA (1) H	D4-B5	D3-A2
SEP DATA (1) L	D4-B5	D4-A2, D7-A8, D8-C8
SR H	D5-B4	D5-C4
SR LOAD H	D3-B1	D3-C4
SR HB (1) H	D3-D1	D5-C4, D8-C8, D8-C6
STW INDEZ (1) H	D1-A5	D8-C6

TP3 H	D7-D3	D7-C8, D8-D4, D8-C5
TP3 L	D7-D3	D5-B8
TP4 H	D7-D3	D8-C3
TP4 L	D7-D3	D8-B2
WBR CLK CNTR L	D8-C2	D3-B7
ZD HNE CLK	D7-C5	D4-C8, D4-B7
GND	POWER SUPPLY	D1-A4
+5V	POWER SUPPLY	D1-A4, D8-A7
+7V	POWER SUPPLY	KN11
+10V	POWER SUPPLY	D8-B8


REV.	CHANGE NO.	DATE

REV. CODE: DCS M7726-0-1 J

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission. COPYRIGHT ©

1976 DIGITAL EQUIP CORP.

REV. NUMBER SIZE CODE PART NO. 2 | 1

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1				
PARTS LIST				
DRN <i>[Signature]</i>	DATE 19 FEB. 76	 digital EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>		
CHK'D <i>[Signature]</i>	DATE 19 FEB. 76			
ENG <i>[Signature]</i>	DATE 2/19/76			
PROJ. ENG. <i>[Signature]</i>	DATE 2/23/76			
PROD. <i>[Signature]</i>	DATE 2/23/76			
NEXT HIGHER ASSEMBLY		TITLE FLOPPY CONTROLLER FIRMWARE		
SCALE				
SHEET 1 OF 1		SIZE CODE K SP	NUMBER RXØ1-Ø-2	REV.
		DIST.		

REV.	
CHANGE NO.	
CHK	

```

1
2      /RX01 FLOPPY CONTROLLER FIRMWARE
3
4
5      /THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES
6      /THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER
7
8
9
10
11     /DO INSTRUCTIONS
12
13
14     0002      SET=2
15     0000      CLR=0
16     0002      ONE=2
17     0000      ZERO=0
18
19     0000      IOB0=0      /INTERFACE=DISK BUSS OUTPUT BUFFER
20     0004      IOB1=4
21     0010      IOB2=10
22     0014      IOB3=14
23     0020      IOB4=20
24     0024      IOB5=24
25     0030      IOB6=30
26
27     0000      INTERF=CLR IOB0      /IOB0 SELECTS EITHER INTERFACE OR DISK BUSS. CLR= INTERFACE
28     0002      DISK=SET IOB0      /SET=DISK
29
30     /INTERFACE BUFFER DEFINITIONS
31     0004      ERR=IOB1      /SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED
32     0010      XREQ=IOB2      /SET TO REQUEST AN RX01 WORD TRANSFER
33     0014      IOOUT=IOB3      /DIRECTION FOR DATA LINE. SET=TO INTERFACE
34     0020      DONE=IOB4      /SET TO INDICATE RX01 READINESS TO ACCEPT A COMMAND
35     0024      SHIFT=IOB5      /SHIFT FOR DATA LINE
36     0030      SECDAT=IOB6      /SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE
37     /SET=SECTOR BUFFER CLR=SHIFT REGISTER MOST SIG BIT
38
39     /DISK BUFFER DEFINITIONS
40     0004      WGATE=IOB1      /WRITE CURRENT ENABLE WHEN SET
41     0010      STPHD=IOB2      /HEAD STEP. TWO PULSES REQUIRED FOR EACH TRACK
42     0014      HDOUT=IOB3      /DIRECTION OF HEAD MOTION
43     0020      EGATE=IOB4      /ERASE CURRENT ENABLE
44     0024      LOWCUR=IOB5      /SPECIFIES WRITE CURRENT LEVEL
45
46     0034      UNIT=34      /SELECTS ONE OF TWO DRIVES. UNIT (ZERO)(ONE)
47
48     0040      UNHD=40      /DEACTIVATES HEAD LOAD SOLENOID OF SELECTED DRIVE
49     0042      LHD=42      /ACTIVATES HEAD LOAD SOLENOID OF SELECTED DRIVE
50
51     0044      BAR=44      /SECTOR BUFFER ADDRESS REGISTER CONTROL
52     0001      LONG=1      /FORMAT: CLR BAR (SHORT)(LONG)
53     0000      SHORT=0      /SHORT PRESETS FOR COUNT OF 1024
54     0002      INCR=2      /LONG PRESETS FOR COUNT OF 4096
55     /FORMAT: INCR BAR INCREMENT THE BUFFER ADDRESS REG.

```

```

56
57     0050      WRTBUF=50      /SECTOR BUFFER WRITE CLOCK
58     0003      START=3      /FORMAT: (START)(FIN) WRTBUF
59     0000      FIN=2      /A 750NS MINIMUM PULSE IS REQUIRED
60
61     /CRC REGISTER CONTROL
62     0054      CRC=54      /FORMAT: CRC (ONE)(ZERO) SPECIFIES DATA TO
63     /BE JAMMED INTO CRC GENERATOR/CHECKER
64     0257      PRECRC=57      /PRESETS CRC REG TO ALL ONES
65     0055      DATCRC=55      /SHIFTS SEPERATED DATA INTO CRC CIRCUIT
66
67     /GENERAL PURPOSE FLAG CONTROL
68     0060      FLAG=60      /FORMAT: FLAG (ON)(OFF)(TOG)
69     0002      ON=2      /SET FLAG
70     0001      OFF=1      /CLR FLAG
71     0003      TOG=3      /TOGGLE FLAG
72
73     0064      LSP=64      /LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG
74
75     0070      LCT=70      /LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION
76     0071      ESP=71      /LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD
77     0073      ICT=73      /INCREMENT COUNTER
78
79     /SHIFT REGISTER CONTROL
80     0074      ROTATE=74      /FORMAT: ROTATE(ONE)(ZERO)
81     /SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT
82     /WHILE INSERTING A ONE OR ZERO INTO THE LEAST
83     /SIGNIFICANT BIT
84     0075      LSR=75      /LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER
85     0077      DATSR=77      /SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED
86     /DATA INTO LSR

```



```

87
88
89          /BRANCH INSTRUCTIONS AND CONDITIONS
90
91
92          0120      BR=100          /FORMAT: BR COND (T)(F)(ONE)(ZERO)
93          /IF CONDITION IS MET, A BRANCH IS MADE WITHIN
94          /THE CURRENT FIELD USING THE CONTENTS OF THE
95          /NEXT ROM LOCATION AS THE BRANCH ADDRESS
96          /IF THE CONDITION IS NOT MET, THE NEXT ROM LOCATION
97          /IS IGNORED AND THE FOLLOWING INSTRUCTION IS EXECUTED
98          0320      WBR=300        /FORMAT: WBR COND (T)(ONE)
99          /THE COUNTER IS INCREMENTED WITH EVERY EXECUTION OF
100         /THIS INSTRUCTION, THE WBR IS REPEATEDLY
101         /EXECUTED UNTILL EITHER THE COUNTER OVERFLOWS OR
102         /THE CONDITION IS MET, IF THE CONDITION IS MET
103         /THE BRANCH IS MADE, IF THE COUNTER OVERFLOWS
104         /THE BRANCH ADDRESS IS IGNORED AND THE NEXT INSTRUCTION
105         /IS EXECUTED
106         0000      F=ZERO          /REQUIRES THE CONDITION TO BE FALSE
107         0002      T=ONE           /REQUIRES THE CONDITION TO BE TRUE
108         0001      IND=1           /IF APPENDED TO THE JUMP, BR OR WBR INSTRUCTION,
109         /CAUSES THE BRANCH ADDRESS TO BE TAKEN FROM THE
110         /OPEN SCRATCHPAD RATHER THAN FROM THE NEXT ROM LOCATION
111
112         0200      PUN=P           /WHEN ASSERTED INDICATES THAT THE INTERFACE HAS
113         /SERVICED A TRANSFER REQUEST, OR THAT A COMMAND
114         /IS PENDING
115         0004      IOB30T=4        /INTERF/DISK OUTPUT BUFFER BIT 3
116         0010      DATAIN=10     /BIDIRECTIONAL DATA LINE BETWEEN INTERFACE AND CONTROLLER
117         0014      INDx=14         /DRIVE INDEX LATCH
118         0020      SR7=20          /SHIFT REGISTER MOST SIGNIFICANT BIT
119         0024      COFL=24         /OVERFLOW (ALL ONES) OF THE COUNTER
120         0030      CRC16=30       /BIT 16 OF CRC GENERATOR/CHECKER
121         0034      HOME=34        /TRACK ZERO OF SELECTED DRIVE ANDED WITH HEAD
122         /DIRECTION BEING OUT
123         0040      WRTE=40         /WRITE ENABLED STATUS OF THE SELECTED DRIVE
124         0204      SEPCLK=04       /SEPERATED CLOCK FROM DISK DATA
125         0250      XIIBIT=50      /ASSERTED IF INTERFACE TRANSFERS ARE TO BE AS
126         /12 BIT WORDS RATHER THAN 8 BIT BYTES
127         0054      DEQSR7=54      /SEPERATED DATA EQUAL TO SHIFT REG BIT 7
128         0060      SAROFL=00      /OVERFLOW CONDITION (ALL ONES) OF THE SECTOR BUFFER
129         /ADDRESS REGISTER
130         0064      MCEQSH=04      /MISSING CLOCK EQUAL TO SHIFT REG BIT 7
131         0070      BDATA0=70      /OUTPUT OF SECTOR BUFFER
132         0074      FLAG0=74       /STATE OF GENERAL PURPOSE FLAG

```

```

133
134          /SCRATCHPAD REGISTER SELECTION
135
136          0200      OPEN=200      /FORMAT: OPEN X WHERE X IS ONE OF THE SCRATCHPAD RES
137          /THIS INSTRUCTION MAKES THE NAMED SCRATCHPAD
138          /ACCESSABLE VIA THE LSP AND ESP COMMANDS
139
140          0004      R2=4           /DEFINITIONS OF SCRATCHPADS BY #
141          0008      R1=8
142          0010      R2=10
143          0014      R3=14
144          0020      R4=20
145          0024      R5=24
146          0030      R6=30
147          0034      R7=34
148          0040      R8=40
149          0044      R9=44
150          0050      R10=50
151          0054      R11=54
152          0060      R12=60
153          0064      R13=64
154          0070      R14=70
155          0074      R15=74
156
157          /DEFINITION OF SCRATCHPADS BY PNEUMONIC
158          0200      CURTK0=R0      /CURRENT TRACK ADDRESS OF DRIVE 0
159          0204      CURTK1=R1      /CURRENT TRACK ADDRESS OF DRIVE 1
160          0010      ERNEG=R2       /DEFINITIVE ERROR CODE IF ANY
161          0014      STAT=R3        /STATUS WORD OF RX01
162          0020      TARTRK=R4      /TARGET TRACK OF CURRENT DISK ACCESS
163          0024      TARSEC=R5      /TARGET SECTOR OF CURRENT DISK ACCESS
164          0030      TEMP0=R6       /TEMPORARY STORAGE
165          0034      TEMP1=R7
166          0040      TEMP2=R8
167          0044      TEMP3=R9      /BIT 7 IS UNIT SELECT BIT, 0 MEANS UNIT 1
168          0050      TEMP4=R10      /BIT 7 IS HEAD LOADED BIT, 1 MEANS HEAD LOADED
169          0054      TEMP5=R11
170          0060      TEMP6=R12
171          0064      RTN0=R13      /RETURN ADDRESS FOR 3RD LEVEL NESTED SUBROUTINES
172          0070      RTN1=R14
173          0074      RTN2=R15
174

```

```

175          /JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS
176
177          0222      JUMP=222          /FORMAT: JUMP FX (IND)
178                                     /CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (0-5)
179                                     /SPECIFIED BY X. THE BRANCH ADDRESS IS TAKEN FROM
180                                     /THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
181                                     /IF IND IS APPENDED, THE BRANCH ADDRESS
182                                     /IS TAKEN FROM THE OPEN SCRATCH PAD
183
184          0200      F2=0
185          0204      F1=4
186          0010      F2=10
187          0014      F3=14
188          0020      F4=20
189          0024      F5=24
    
```

```

190
191
192
193
194
195
196
197
198          /TABLE OF DEFINITIVE ERROR CODES
199
200          0010      KXDV0=10          /DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
201          0020      KXDV1=20          /DRIVE 1 FAILED TO SEE HOME ON INITIALIZE, DOES NOT CAUSE ERROR
202          0030      KARONG=30         /FOUND HOME WHEN STEPPING IN 10 TRACKS FOR INIT
203          0040      KERTRK=40        /TRIED TO ACCESS A TRACK GREATER THAN 76
204          0050      KHOMERR=50       /HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED
205          0060      KSELFER=60       /SELF DIAGNOSTIC ERR
206          0070      KXHDR=70         /DESIRED SECTOR COULD NOT BE FOUND AFTER LOOKING
207                                     /AT 52 HEADERS
208          0100      KXPROT=100        /WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK
209          0110      KTIMER=110       /MORE THAN 40 MICROSECONDS AND NO SEPCLOCK SEEN
210          0120      KXPRAM=120       /A PREAMBLE COULD NOT BE FOUND
211          0130      KXIDAM=130       /PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
212          0140      KHRCRER=140      /CRC ERROR ON WHAT APPEARED TO BE A HEADER, ERROR IS NOT ASSERTED
213          0150      KTKSKER=150     /THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE
214                                     /WITH THE DESIRED TRACK
215          0160      KXSTRYS=160      /TOO MANY TRIES FOR AN IDAM
216          0170      KNODAM=170       /DATA AM NOT FOUND IN ALLOTED TIME
217          0200      KDCRER=200       /CRC ERROR ON READING THE SECTOR FROM THE DISK
218          0210      KPARER=210       /PARITY ERROR ON SOME WORD FROM THE INTERFACE
219
    
```

```

220 /ROUTINE: INITIALIZE] IF A HOST PROCESSOR INITIAL... AN
221 /RX01 POWER LOW IS DETECTED, THE PC IS CLEARED AND THE RX01 TIMING
222 /STOPS. UPON THE NEGATION OF INITIALIZE, TIMING RESUMES AND A SELF TEST OF
223 /INTERNAL DATA PATHS IS MADE. IF AN ERROR OCCURS HERE, ERROR AND
224 /DONE ARE SET, BUT ERREG IS NOT ALTERED. THEN IF NO ERROR HAS OCCURRED AN ATTEMPT
225 /IS MADE TO RECALIBRATE DRIVE 1 THEN DRIVE 0. IF DRIVE 0 FAILS TO RECALIBRATE,
226 /THE ERROR CODE IS LOADED INTO ERREG AND ERROR IS SET. IF DRIVE
227 /1 RECALIBRATES AND IS READY (DISK LOADED) SECTOR ONE OF TRACK ONE
228 /IS READ INTO THE SECTOR BUFFER. IT IS POSSIBLE FOR A READ ERROR
229 /TO OCCUR WHILE READING THIS SECTOR.
230
231
232 0000 *2220
233          DECIMAL
234
235 0000 0210          OPEN ERREG          /CLEAR ERROR REGISTER
236 0001 0064          LSP
237
238 0022 0222          JUMP F4            /GO DO THE INITIALIZE DIAGNOSTIC ROUTINE
239 0023 2352          TEST
240
241 0004 0070          TSTRN, LCT          /RETURN FROM SUCCESSFUL DIAGNOSTIC ROUTINE
242          OCTAL
243          4
244          DECIMAL
245 0006 0075          LSR              /SET THE INIT DONE BIT OF STAT
246 0007 0214          OPEN STAT
247 0010 0064          LSP
248
249 0011 0070          LCT              /SET UP SOME SCRATCHPAD REGISTERS
250 0012 0377          -1
251 0013 0075          LSR
252 0014 0244          OPEN TEMPD       /UNIT 0 TO SOFT UNIT BIT
253 0015 0064          LSP
254 0016 0200          OPEN CURTK0      /NEG ZERO TO BOTH CURRENT TRACK ADDRESSES
255 0017 0064          LSP
256 0020 0204          OPEN CURTK1
257 0021 0064          LSP
258
259 0022 0074          ROTATE ZERO       /NEG ONE TO TARGET SECTOR
260 0023 0224          OPEN TARSEC
261 0024 0064          LSP
262 0025 0220          OPEN TARTRK      /NEG ONE TO TARGET TRACK FOR INITIALIZE BOOTSTRAP
263 0026 0064          LSP
264
265 0027 0002          DISK             /SELECT DISK #06
266
267 0030 0070          LCT              /CALL SUBROUTINE TO LOAD HEAD AND WAIT 25 MS
268 0031 0034          RECAL1          /TO ALLOW POWER UP DRIVE SETTLE TIME
269 0032 0222          JUMP F4
270 0033 2145          DLY25
271
272 0034 0036          RECAL1, UNIT ONE /SELECT UNIT ONE FOR RECALIBRATE
273
274 0035 0014          RECAL3, CLR HDOUT /STEP HEAD IN 10 TRACKS TO ASSURE IT IS NOT BEHIND TRACK 0

```

```

275 0036 0070          LCT
276 0037 0305          -10-1
277 0040 0075          LSR
278 0041 0070          LCT
279 0042 0045          IN10
280 0043 0222          JUMP F4
281 0044 2100          STEPHD
282
283 0045 0220          I'1', JUMP F5     /ERROR, HOME WAS SEEN WHILE STEPPING IN.
284 0046 2621          -RONG
285
286 0047 0010          SET HDOUT        /STEP OUT AS MANY AS 80 TRACKS IN SEARCH OF HOME
287 0050 0070          LCT
288 0051 0257          -80-1
289 0052 0075          LSR
290 0053 0070          LCT
291 0054 0060          RECALOK
292 0055 0040          UNHD
293 0056 0222          JUMP F4
294 0057 2100          STEPHD
295
296 0060 0202          RECALOK, JUMP F0   /HOME WAS FOUND OK
297 0061 0075          #CHDR
298
299 0062 0174          BR FLAG0 F        /IF FLAG=0 RECALIBRATE WAS ON DRIVE 1
300 0063 0070          #XDRV1
301
302 0064 0070          #XDRV0, LCT       /RECALIBRATE FAILURE WAS ON DRV 0
303 0065 0010          #XDRV0
304 0066 0220          JUMP F5
305 0067 2610          GOERDN
306
307 0070 0070          #XDRV1, LCT       /RECAL FAILURE WAS ON DRV 1, LOG ERROR
308 0071 0020          #XDRV1          /AND CONTINUE RECALIBRATION
309 0072 0075          LSR
310 0073 0210          OPEN ERREG
311 0074 0064          LSP
312
313 0075 0176          #CHDR, BR FLAG0 T   /IF FLAG=1 BOTH DRIVES HAVE BEEN RECALIBRATED
314 0076 0372          #NRCL
315
316 0077 0062          FLAG ON          /SET FLAG TO INDICATE DRV 0 IS BEING RECALIBRATED
317
318 0100 0034          UNIT ZERO
319
320 0101 0202          JUMP F0            /GO BACK AND RECALIBRATE DRVS
321 0102 0035          RECAL0

```

```

322
323
324      /([SUBROUTINE: FINDTRACK])
325      /THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR. IT PICKS
326      /UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE, CHECKS THAT
327      /THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL.), MOVES THE
328      /HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES
329      /TRACK POSITION, AND LOCATES THE CORRECT SECTOR, EXIT FROM
330      /THIS SUBROUTINE OCCURS AT WRITE TURN ON TIME OF THE SELECTED
331      /SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER
332
333
334
335      0103 0075  FINDTR, LSR          /SAVE THE RETURN ADDRESS
336      0104 0274      OPEN RTN
337      0105 0064      LSP
338
339      0106 0270      LCT          /CLEAR THE ERROR REGISTER
340      0107 0000      Y
341      0110 0075      LSR
342      0111 0210      OPEN ERREG
343      0112 0064      LSP
344
345      0113 0244      OPEN TEMPD   /SOFT UNIT BIT TO SR
346      0114 0071      ESP
347      0115 0075      LSR
348
349      0116 0122      BR SR7 ONE   /IF SR=1 DRIVE 0 IS CURRENTLY SELECTED
350      0117 0127      UZERO
351
352      0120 0174      UONE, BR FLAG0 ZERO /IF FLAG=0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
353      0121 0141      USAME
354
355      0122 0034      UNIT ZERO    /DRIVE 0 IS DESIRED AND DRIVE1 WAS SELECTED, SELECT 0
356
357      0123 0070      LCT          /SET UP SOFT UNIT SELECT AS DRIVE 0
358      0124 0200      OCTAL
359      0124 0200      200
360      0124 0200      DECIMAL
361
362      0125 0202      JUMP F0      /GO STORE SOFT UNIT BIT
363      0126 0134      UDIF
364
365      0127 0176      UZERO, BR FLAG0 ONE /IF FLAG=1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
366      0130 0141      USAME
367
368
369      0131 0036      UNIT ONE     /DRIVE 1 IS DESIRED BUT DRIVE0 IS SELECTED, SELECT DRIVE 1
370      0132 0070      LCT
371      0133 0001      0
372
373      0134 0075      UDIF, LSR     /STORE SOFT UNIT SELECT BIT
374      0135 0064      LSP
375
376      0136 0074      ROTATE ZERO  /CLR SOFT HD LOAD BIT BECAUSE UNITS CHANGED

```

```

377      0137 0250      OPEN TEMPE
378      0140 0064      LSP
379
380      0141 0070      USAME, LCT    /CALL GETWORD SUBROUTINE FOR THE SECTOR ADDRESS
381      0142 0145      PUTSEC
382      0143 0222      JUMP F4
383      0144 0001      GETWRD
384
385
386      0145 0070      PUTSEC, LCT   /MAKE FIRST BIT OF COMPLIMENTED SECTOR ADDRESS A 1 REGARDLESS OF DATA
387      0146 0237      =7-1
388      0147 0070      ROTATE ONE
389      0150 0120      BR COFL T
390      0151 0160      .+7
391      0152 0073      ICT
392      0153 0122      BR SR7 T
393      0154 0147      .-5
394      0155 0074      ROTATE ZERO
395      0156 0202      JUMP F0
396      0157 0150      .-7
397
398      0160 0224      OPEN TARSEC   /PUT THE TARGET SECTOR AWAY
399      0161 0064      LSP
400
401      0162 0070      LCT          /CALL GETWRD SUBROUTINE FOR TRACK ADDRESS
402      0163 0166      PUTTRK
403      0164 0222      JUMP F4
404      0165 0200      GETWRD
405
406
407      0166 0220      PUTTRK, OPEN TARTRK /STASH THE TRACK ADDRESS
408      0167 0064      LSP
409
410      0170 0254      OPEN TEMPF   /START SETUP FOR COMPARING THE
411      0171 0064      LSP          /TARGET TRACK AND TRACK 76
412      0172 0260      OPEN TEMPG   /F= TARGET TRACK
413      0173 0070      LCT          /G= 77
414      0174 0262      =77-1
415      0175 0075      LSR
416      0176 0064      LSP
417
418      0177 0070      LCT          /CALL SUBR MAGCOM TO SEE IF TARGET TRACK
419      0200 0206      ILTRK        /IS GREATER THAN 114 OCTAL, 76 DECIMAL.
420      0201 0075      LSR
421      0202 0270      OPEN RTNA
422      0203 0064      LSP
423      0204 0226      JUMP F5
424      0205 0400      MAGCOM
425
426
427      0206 0202      ILTRK, JUMP F0 /TARGET TRACK IS 77, ILLEGAL ADDRESS
428      0207 0242      ERTRK        /GO, REPORT THE ERROR
429      0210 0202      JUMP F0     /TARGET TRACK IS GREATER THAN 77
430      0211 0242      ERTRK        /GO, REPORT THE ERROR
431

```

```

432 0212 0244 OPEN TEMPD /TARGET TRACK IS OK, GET THE DRIVE
433 0213 0071 ESP /SELECT FROM TEMPD
434 0214 0075 LSR
435
436 0215 0200 OPEN CURTK0 /PRESELECT UNIT 0
437
438 0216 0002 DISK /SELECT DISK #008
439
440 0217 0122 BR SR7 ONE /WHICH UNIT SELECTED? BIT7=0 MEANS UNIT ONE
441 0220 0222 .+2 /ZERO, SKIP UNIT 1 SETUP
442 0221 0204 OPEN CURTK1
443
444 0222 0071 ESP /PASS SELECTED CURRENT TRACK TO MAGCOM SUBR
445 0223 0075 LSR
446 0224 0200 OPEN TEMPG
447 0225 0064 LSP
448
449 0226 0220 OPEN TARTRK /PASS TARGET TRACK TO MAGCOM SUBROUTINE
450 0227 0071 ESP
451 0230 0075 LSR
452 0231 0254 OPEN TEMPF
453 0232 0064 LSP
454 0233 0070 LCT /CALL SUBROUTINE MAGCOM TO SEE IF TARGET
455 0234 0246 TRKE0 /IS SAME AS CURRENT TRACK, F=TARGET, 0=CURRENT
456 0235 0075 LSR
457 0236 0270 OPEN RTNA
458 0237 0064 LSP
459 0240 0226 JUMP F5
460 0241 2000 MAGCOM
461
462
463 0242 0070 ERTK, LCT
464 0243 0040 KERTK /TRIED TO ACCESS A TRACK GREATER THAN 76 DECIMAL
465 0244 0226 JUMP F5
466 0245 2010 GOERDA
467
468
469 0246 0202 TRKE0, JUMP F0 /TARGET EQUALS THE CURRENT TRACK, NO
470 0247 0357 NOSTPS /STEPS ARE REQUIRED
471 0250 0270 OPEN RTNA /NOOP; TARGET > ACTUAL RETURN
472 0251 0270 OPEN RTNA /NOOP
473
474 0252 0270 BOUT, OPEN RTNA /TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
475 0253 0070 LCT /CF BOUT SUBROUTINE, SET UP RETURN FROM DIF SUBR
476 0254 0275 STPOUT
477 0255 0075 LSR
478 0256 0064 LSP
479
480 0257 0244 OPEN TEMPD /SOFT UNIT SELECT BIT TO SR7
481 0260 0071 ESP
482 0261 0075 LSR
483
484 0262 0204 OPEN CURTK1 /PRESELECT UNIT 1
485
486 0263 0120 BR SR7 ZERO /SR7=0 MEANS UNIT ONE

```

```

487 0264 0266 .+2
488 0265 0200 OPEN CURTK0
489
490 0266 0071 ESP /PASS SELECTED CURRENT TRACK TO DIF SUBR VIA SR
491 0267 0075 LSR
492
493 0270 0220 OPEN TARTRK /PASS TARGET TRACK TO DIF VIA CNTR
494 0271 0071 ESP
495
496 0272 0016 SET HDOUT /ASSUME A STEP OUT
497
498 0273 0220 JUMP F5 /GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED
499 0274 2462 DIF
500
501
502 0275 0202 STPOUT, JUMP F0 /TARGET TRACK IS LESS THAN
503 0276 0300 .+2 /THE ACTUAL, MOVE OUT IS NECESSARY
504
505 0277 0014 CLR HDOUT /TARGET IS GREATER THAN ACTUAL, STEPS IN NEEDED
506
507 0300 0070 LCT /COMPLEMENT OF STEPS REQUIRED IS IN THE
508 0301 0305 DUNSTP /SHIFT REG. SET UP RETURN FROM STPHD SUBR
509
510 0302 0040 UNHD /UNLOAD HEAD BEFORE MOVING
511
512 0303 0222 JUMP F4 /CALL SUBROUTINE STEPMD
513 0304 2100 STEPMD
514
515
516 0305 0220 DUNSTP, JUMP F5 /NONE FOUND BEFORE LAST STEP TAKEN
517 0306 2456 HOMERR
518
519 0307 0244 OPEN TEMPD /SOFT UNIT BIT TO SR7
520 0310 0071 ESP
521 0311 0075 LSR
522 0312 0220 OPEN TARTRK /GET READY TO PASS TARGET TRK TO PROPER
523 0313 0071 ESP /CURRENT TRACK
524
525 0314 0200 OPEN CURTK0 /OPEN PROPER CURRENT TRACK REGISTER
526 0315 0122 BR SR7 ONE /BIT7=0 MEANS UNIT ONE
527 0316 0320 .+2
528 0317 0204 OPEN CURTK1
529
530 0320 0075 LSR /UPDATE THE CURRENT TRACK ADDRESS
531 0321 0064 LSP
532
533
534 0322 0220 HDSETL, OPEN TARTRK /HEAD IS SETTLED DETERMINE IF ABOVE TRACK 43 DECIMAL
535 0323 0071 ESP /PASS TARGET TO MAGCOM VIA TEMPF
536 0324 0075 LSR
537 0325 0254 OPEN TEMPF
538 0326 0064 LSP
539
540 0327 0270 LCT /PASS 44 TO MAGCOM VIA TEMPG
541 0330 0323 =44-1

```

```

542 0331 0075 LSR
543 0332 0202 OPEN TEMPG
544 0333 0064 LSP
545
546 0334 0026 SET LONCUR /ASSUME TARGET GREATER THAN 43
547
548 0335 0070 LCT /CALL MAGCOM SUBROUTINE
549 0336 0344 ABV43 /RETURN ADDRESS
550 0337 0075 LSR
551 0340 0270 OPEN RTNA
552 0341 0064 LSP
553 0342 0226 JUMP F5
554 0343 2400 MAGCOM
555
556
557 0344 0202 ARV43, JUMP F0 /NOOP F0G RETURN, ABOVE TRK 43
558 0345 0346 .+1 /NOOP
559
560 0346 0202 JUMP F0 /F0G; ABOVE TRACK 43
561 0347 0351 .+2
562
563 0350 0024 CLR LONCUR /F0G; BELOW TRACK 43, WRITE WITH HIGH CURRENT
564
565 0351 0070 CF1-SE, LCT /CALL FINDSEC SUBROUTINE TO LOCATE THE DESIRED SECTOR
566 0352 0355 RFINTR
567 0353 0206 JUMP F1
568 0354 0714 FINDSE
569
570 0355 0274 RFINTR, OPEN RTN /RETURN FROM FINDTR SUBROUTINE
571 0356 0207 JUMP F1 IND
572
573
574 0357 0250 NOSTPS, OPEN TEMPE /NO STEPS REQUIRED
575 0360 0071 ESP /SOFT HEAD LOAD BIT TO SR7
576 0361 0075 LSR
577
578 0362 0122 BR SR7 ONE /IS HEAD LOADED?
579 0363 0322 HDSETL /YES, GO UPDATE CURRENT CONTROL
580
581 0364 0070 LCT /NO, GO LOAD HEAD AND WAIT FOR 20MS SETTLE TIME
582 0365 0322 HDSETL /RETURN ADDR FROM DLY25 SUBROUTINE
583 0366 0222 JUMP F0
584 0367 0145 DLY25
585
586
587 0370 0212 PFUNCT, JUMP F2 /POINTER FROM GETWORD SUBROUTINE TO
588 0371 0236 FUNCT /FUNCTION DECODE
589
590
591 0372 0226 PDNRCL, JUMP F5 /POINTER TO DRV* CHECK DONE AFTER RECALIBRATE
592 0373 0225 DNRCL
593
594 0374 0200 0 /SPARE LOCATIONS
595 0375 0200 0 /OPEN
596 0376 0200 0 /OPEN
597 0377 0200 0 /OPEN

```

```

597 /ROUTINE; WRITE SECTOR]
598 /THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
599 /WRITES A PREAMBLE OF 6 BYTES OF ZEROES, A DATA OR DELETED DATA MARK,
600 /THEN TURNS ON ERASE GATE, ENTER WITH CNTR=100 IF
601 /DELETED DATA, CNTR=0 IF NORMAL DATA MARK, THE DATA MARK, DATA FIELD, CRC
602 /AND ONE BYTE POSTAMBLE ARE WRITTEN, WRITE CURRENT IS TURNED OFF,
603 /511 MICRO SECONDS LATER ERASE CURRENT IS TURNED OFF, A HEADER MUST
604 /THEN BE KEAD TO INSURE DISK IS STILL UP TO SPEED BEFORE THE WRITE
605 /SECTOR FUNCTION IS COMPLETE.
606
607
608
609
610 0400 0214 WRTSEC, OPEN STAT /DEL DATA BIT TO STAT6
611 0401 0075 LSR
612 0402 0064 LSP
613
614 0403 0070 LCT /CALL SUBROUTINE TO FIND DESIRED TRACK AND SECTOR
615 0404 0407 S-GATE
616 0405 0202 JUMP F0
617 0406 0103 FINDTR
618
619 0407 0061 S-GATE, FLAG OFF /ALWAYS START WRITING WITH WRITE FLOP CLEARED
620
621 0410 0140 BR WRITEN F /GO REPORT ERROR IF NO WRITE ENABLE
622 0411 0503 PRERR
623
624 0412 0214 OPEN STAT /DEL DATA BIT TO SR7 AND ENABLE WRT CURRENT
625 0413 0271 ESP
626 0414 0006 SET WGATE
627 0415 0075 LSR
628 0416 0074 ROTATE ZERO
629
630 0417 0234 OPEN TEMPB /USE TEMPB FOR SECOND HALF DATA AM PATTERN
631
632 0420 0057 PRECRC /JAM THE CRC GENERATOR WITH FIRBT 6 BITS OF DATA AM
633 0421 0056 CRC ONE
634 0422 0056 CRC ONE
635 0423 0056 CRC ONE
636 0424 0056 CRC ONE
637 0425 0056 CRC ONE
638 0426 0054 CRC ZERO
639
640 0427 0120 BR SR7 ZERO /DELETED DATA?
641 0430 0460 DAMSUP /NO, REGULAR DATA MARK
642
643 0431 0070 LCT /YES, SECOND HALF OF DELETED DATA MARK TO CNTR
644 0432 0325 OCTAL
645 0433 0325 325 /FLUX PATTERN
646 0434 0325 DECIMAL
647
648 0433 0054 CRC ZERO /JAM LAST 2 BITS OF DELETED DATA MARK TO CRC GEN,
649 0434 0054 CRC ZERO
650 0435 0002 DISK /NOOP
651 0436 0002 DISK /NOOP

```

```

650
651 0437 0063 STASH, TOG FLAG /END OF THE FIRST 0 BIT
652
653 0440 0075 LSR /PUT SECOND HALF OF THE DESIRED MARK IN THE TEMPS
654 0441 0064 LSR
655
656 0442 0070 LCT /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
657 0443 0466 HLFCLY
658 0444 0075 LSR
659
660 0445 0070 LCT /STALL 1.0 MICRO SECONDS
661 0446 0374 -3-1
662 0447 0073 ICT
663 0450 0124 BR COFL F
664 0451 0447 -2
665 0452 0002 DISK /NOOP
666
667 0453 0070 LCT /SPECIFY 22 ZEROS TO BE WRITTEN BY WRTOB SUBROUTINE
668 0454 0351 -22-1
669
670 0455 0063 TOG FLAG /WRITE SECOND CLOCK TRANSITION
671
672 0456 0212 JUMP F2 /CALL WRITE ZEROS SUBROUTINE
673 0457 1322 WRTOB
674
675 0460 0070 DAMSUP, LCT /LOAD SECOND HALF OF NORMAL DATA MARK
676 0461 0337 OCTAL
677 0462 0337 337
678 0463 0337 DECIMAL
679
680 0462 0056 CRC ONE /JAM LAST 2 BITS OF DATA MARK TO CRC GENERATOR
681 0463 0056 CRC ONE
682
683 0464 0206 JUMP F1 /GO PUT AWAY THE SECOND HALF OF THE DATA MARK
684 0465 0437 STASH
685
686 0466 0002 HLFCLY, DISK /NOOP
687
688 0467 0070 LCT /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
689 0470 0514 WRTDAM
690 0471 0075 LSR
691
692 0472 0370 LCT /NOOP WASTE .4 MICRO SECONDS
693 0473 0351 -22-1 /NOOP
694 0474 0070 LCT /NOOP
695 0475 0351 -22-1 /NOOP
696
697 0476 0070 LCT /SPECIFY 22 BITS TO BE WRITTEN BY WRTOB SUBROUTINE
698 0477 0351 -22-1
699
700 0500 0063 TOG FLAG /WRITE THE 25TH CLOCK TRANSITION
701
702 0521 0212 JUMP F2 /CALL WRTOB SUBROUTINE
703 0522 1322 WRTOB
704
705
706

```

```

707 0503 0070 PRTERN, LCT /SET WRITE PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
708 0504 0070 /ON A WRITE PROTECTED DISKETTE
709
710 0504 0010 OCTAL
711 0505 0075 10
712 0506 0214 DECIMAL
713 0507 0300 LSR
714 0508 0300 OPEN STAT
715 0509 0300 LSR
716
717 0510 0070 LCT /ERROR CODE FOR WRIT PROTECT ERROR
718 0511 0100 K=PROT
719 0512 0220 JUMP F5
720 0513 0010 GOERON
721
722
723
724 /THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A
725 /DELETED DATA MARK. THE FIRST HALF OF BOTH MARKS ARE
726 /IDENTICAL. THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY
727 /PUTTING THE SECOND HALF BIT PATTERN IN TEMPS
728
729 0514 0070 WRTDAM, LCT /WASTE 2.0 MICRO SECONDS
730 0515 0375 -2-1
731 0516 0073 ICT
732 0517 0075 LSR
733 0520 0124 BR COFL F
734 0521 0516 -3
735
736 0522 0063 TOG FLAG /WRITE A CLOCK BIT AS END OF 48TH ZERO
737
738 0523 0070 LCT /FIRST HALF OF DATA MARK PATTERN TO SR
739 0524 0352 OCTAL
740 0525 0075 352
741 0526 0075 DECIMAL
742 0527 0370 LSR
743
744 0526 0070 LCT /SET TRANSITION LOOP COUNTER FOR 8 LOOPS
745 0527 0370 -7-1
746 0530 0002 DISK /NOOP
747
748 0531 0120 AGAIN, SR SR7 ZERO /WHAT'S THE BIT?
749 0532 0502 A /ZERO, NO TRANSITION
750
751 0533 0004 CLR BAR /ONE, RESET THE BUFFER ADDR REG TO B
752
753 0534 0063 TOG FLAG /WRITE FLUX TRANSITION
754
755 0535 0126 ABACK, BR COFL T /CHECK TRANSITION LOOP COUNT
756 0536 0543 SECHLF /GO GET SECOND HALF
757
758 0537 0074 ROTATE /SHIFT NEXT TRANSITION TO SR7
759
760 0540 0073 ICT /BUMP TRANSITION LOOP COUNTER
761

```

```

762 0541 0206          JUMP F1          /DO ANOTHER LOOP
763 0542 0531          AGAIN
764
765 0543 0234  SECHLF, OPEN TEMPB  /SECOND HALF OF DATA MARK TO SR
766 0544 0071          E3P
767 0545 0075          LSR
768
769 0546 0070          LCT          /SET TRANSITION LOOP COUNTER FOR 8 LOOPS
770 0547 0370          =7-1
771
772
773 0550 0120  AGAIN1, BR SR7 ZERO  /SMALL WE WRITE A TRANSITION?
774 0551 0564          B          /NO
775
776 0552 0263          TOG FLAG        /YES
777 0553 0802          DISK          /NOOP
778
779 0554 0126  BBACK, BR COFL T  /DONE DATA MARK?
780 0555 0566          WRTDAT        /YES, GO WRITE DATA
781
782 0556 0073          ICT          /NO, BUMP THE LOOP COUNTER
783
784 0557 0174          ROTATE        /BRING UP NEXT HALF BIT TO SR7
785
786 0560 0206          JUMP F1          /DO ANOTHER LOOP
787 0561 0550          AGAIN1
788
789 0562 0206  A,      JUMP F1          /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
790 0563 0535          ABACK
791
792 0564 0206  B,      JUMP F1          /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
793 0565 0550          BBACK
794
795
796
797
798          /THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.
799
800
801 0566 0022  WRTDAT, SET EGATE  /TURN ON ERASE CURRENT AT START OF DATA FIELD
802 0567 0073          ICT          /NOOP; WASTE 2 CYCLES
803 0570 0073          ICT          /NOOP
804
805 0571 0170  DATAA, BR DATAD ZERO /WHAT'S THE DATA BIT?
806 0572 0615          C          /ZERO, GO WRITE NOTHING
807
808 0573 0056          CRC ONE        /ONE, UPDATE THE CRC WITH 1
809
810 0574 0063          TOG FLAG        /WRITE A DATA TRANSITION
811 0575 0673          ICT          /NOOP FOR BIT CELL TIMING
812
813 0576 0162  CBACK, BR BAROFL T  /DONE ENTIRE SECTOR?
814 0577 0624          WRTCRC        /YES, GO WRITE THE CRC
815
816 0620 0046          INCR BAR        /NO, BRING UP NEXT DATA BIT FROM SEC BUFFER

```

```

817
818 0601 0070          LCT          /NOOP - WASTE 5 CYCLES WITH
819 0602 0376          =2          /NOOP - A SELF TEST OF THE COUNTER
820 0603 0073          ICT          /NOOP
821 0604 0124          BR COFL F  /NOOP
822 0605 0620          SELFER        /NOOP
823
824 0606 0063          TOG FLAG        /WRITE A CLOCK TRANSITION
825
826 0607 0170          LCT          /NOOP - WASTE 4 CYCLES WITH
827 0610 0377          =1          /NOOP - A SELF TEST OF THE COUNTER
828 0611 0124          BR COFL F  /NOOP
829 0612 0620          SELFER        /NOOP
830
831 0613 0206          JUMP F1          /GO WRITE ANOTHER DATA BIT
832 0614 0571          DATAA
833
834 0615 0054  C,      CRC ZERO        /UPDATE CRC WITH 0 AND SKIP DATA TRANSITION
835 0616 0206          JUMP F1
836 0617 0576          CBACK
837
838
839 0620 0070  SELFER, LCT          /A SELF DIAGNOSTIC HAS FAILED
840 0621 0060          WSELFER
841 0622 0226          JUMP F5
842 0623 0610          GOERDN
843
844
845          /THIS ROUTINE WRITES THE 16 BIT CRC GENERATED FOR THE
846          /PRECEEDING DATA FIELD.
847
848
849 0624 0070  WRTCRC, LCT          /PRESET BIT COUNTER FOR 16 BITS
850 0625 0357          =16-1
851
852 0626 0075          LSR          /NOOP WASTE 4 CYCLES AND SELF TEST THE SR
853 0627 0002  E,      DISK          /NOOP
854 0630 0120          BR SR7 ZERO  /NOOP
855 0631 0620          SELFER        /NOOP
856
857 0632 0063          TOG FLAG        /WRITE A CLOCK TRANSITION
858
859 0633 0076          ROTATE ONE       /NOOP WASTE 6 CYCLES WITH MORE SELFTEST
860 0634 0076          ROTATE ONE       /NOOP
861 0635 0076          ROTATE ONE       /NOOP
862 0636 0076          ROTATE ONE       /NOOP
863 0637 0120          BR SR7 ZERO  /NOOP
864 0640 0620          SELFER        /NOOP
865
866 0641 0130          BR CRC16 ZERO  /WHAT IS THE CRC BIT
867 0642 0653          D          /ZERO, DO NOT WRITE ANYTHING
868
869 0643 0056          CRC ONE        /ONE, BRING UP THE NEXT BIT
870
871 0644 0063          TOG FLAG        /WRITE A DATA TRANSITION

```



```

872 0645 0076          ROTATE ONE      /NOOP
873
874 0646 0073  DBACK, ICT              /BUMP THE BIT COUNTER
875
876 0647 0126          BR COFL T       /DONE CRC YET?
877 0650 0656          *RTPST           /YES, GO WRITE A POSTAMBLE
878
879 0651 0206          JUMP F1         /NO, GO WRITE ANOTHER CRC BIT
880 0652 0627          E
881
882 0653 0054  D,      CRC ZERO         /BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
883 0654 0206          JUMP F1
884 0655 0646          DBACK
885
886
887
888 /THIS ROUTINE *WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
889 /WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
890 /CURRENT. IT UTILIZES THE *WRITE ZEROES SUBROUTINE.
891
892
893 0656 0270  *RTPST, LCT              /SETUP TO CALL *RTBS TO WRITE 8 BITS OF ZEROES
894 0657 0666          CWGATE
895 0660 0075          LSR
896 0661 0070          LCT
897 0662 0367          =8-1
898
899 0663 0063          TOG FLAG         /WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
900
901 0664 0212          JUMP F2         /CALL THE SUBROUTINE WRITE ZEROES
902 0665 1322          *RTBS
903
904
905 0666 0004  CWGATE, CLR *GATE       /DISABLE WRITE CURRENT
906
907 0667 0070          LCT              /CALL *RTBS FOR 127 BITS (511.2 MICRO SEC)
908 0670 0676          CEGATE          /DELAY TO ERASE TURN OFF
909 0671 0075          LSR
910 0672 0070          LCT
911 0673 0200          =127-1
912 0674 0212          JUMP F2
913 0675 1322          *RTBS
914
915
916 0676 0020  CEGATE, CLR EGATE       /DISABLE ERASE CURRENT
917
918 0677 0070          LCT              /CALL *RTBS FOR 25 BIT (101 MICRO SEC) DELAY
919 0700 0706          READOK          /BEFORE TRYING TO READ
920 0701 0075          LSR
921 0702 0070          LCT
922 0703 0346          =25-1
923 0704 0212          JUMP F2
924 0705 1322          *RTBS
925
926 0706 0070  READOK, LCT             /CALL FIND HEADER ROUTINE TO INSURE

```

```

927 0707 0712          GOODONE        /THAT THE DISK IS STILL MOVING
928 0710 0216          JUMP F3
929 0711 1400          FINDHD
930
931 0712 0212  GOODONE, JUMP F2        /WRITE SECTOR FUNCTION IS COMPLETE
932 0713 1406          OKDONE
933
934
935 /SUBROUTINE: FINDSECTOR)
936 /SUBROUTINE TO FIND A SPECIFIC SECTOR, ENTER WITH RETURN ADDRESS
937 /IN CNTR, DESIRED TRACK ADDRESS IN TARTRK AND DESIRED SECTOR ADDRESS
938 /IN TARSEC. THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
939 /BEEN REACHED.
940
941
942 0714 0270  FINDSE, OPEN RTNA       /SAVE RETURN ADDRESS
943 0715 0075          LSR
944 0716 0064          LSP
945
946 0717 0260          OPEN TEMPG      /PRESET SECTOR TRY COUNT TO 52 TRIES
947 0720 0070          LCT
948 0721 0313          =52-1
949
950 0722 0075  AGAIN2, LSP            /STORE SECTOR TRY COUNT
951 0723 0064          LSP
952
953 0724 0270          LCT              /CALL SUBROUTINE TO FIND A HEADER
954 0725 0730          CHKSEC
955 0726 0216          JUMP F3
956 0727 1400          FINDHD
957
958 0730 0174  CHKSEC, BR FLAGD ZERO   /CORRECT SECTOR? FLAG=1 IF NO
959 0731 0743          WAIT           /YES, GO WAIT FOR PREAMBLE
960
961 0732 0260          OPEN TEMPG      /NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
962 0733 0071          ESP
963 0734 0073          ICT
964
965 0735 0124          BR COFL F       /52 TRIES MADE FOR SECTOR YET?
966 0736 0722          AGAIN2        /NO, TRY ANOTHER SECTOR
967
968 0737 0270  *XHDR, LCT             /YES, CAN'T FIND THE SECTOR
969 0740 0070          *XHDR
970 0741 0226          JUMP F5
971 0742 0610          GDERDN
972
973 0743 0070  WAIT, LCT              /STALL 323,2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
974 0744 0360          =26-1
975 0745 0073          ICT
976 0746 0124          BR COFL F
977 0747 0745          =2
978 0750 0073          ICT
979 0751 0124          BR COFL F
980 0752 0750          =2
981 0753 0073          ICT

```

```

982 0754 0124 BR COFL F
983 0755 0753 .-2
984
985 0756 0270 OPEN RTNA /RETURN FROM THIS SUBROUTINE AT WRITE TURN ON TIME
986 0757 0203 JUMP F0 IND /OF THE DESIRED SECTOR
987
988
989
990 /([ROUTINE: READ SECTOR])
991
992 0760 0074 RDSEC, ROTATE ZERO /ZERO THE STAT
993 0761 0074 ROTATE ZERO
994 0762 0214 OPEN STAT
995 0763 0064 LSP
996
997 0764 0070 LCT /CALL THE FIND TRACK SUBROUTINE TO LOCATE DESIRED SECTOR
998 0765 0770 GOREAD
999 0766 0202 JUMP F0
1000 0767 0103 FINDTR
1001
1002 0770 0222 GOREAD, JUMP F4 /GO READ THE DATA FIELD
1003 0771 2167 READ
1004
1005
1006 0772 0000 0 /OPEN FREE LOCATIONS
1007 0773 0000 0 /OPEN
1008 0774 0000 0 /OPEN
1009 0775 0000 0 /OPEN
1010 0776 0000 0 /OPEN
1011 0777 0000 0 /OPEN

```

```

1012 /([ROUTINE: DONE AND ERROR DONE])
1013
1014
1015 1002 0220 ERDCNE, CLR DONE
1016 1001 0010 CLR XREG
1017
1018 1002 0000 INTERF /SELECT INTERFACE BUSS
1019
1020 1003 0000 SET ERR /ASSERT ERROR LINE
1021
1022 1004 0010 JUMP F2 /SKIP NEXT INSTRUCTION
1023 1025 1007 .+2
1024
1025 1026 0000 OKDONE, CLR ERR /NEGATE ERROR LINE
1026
1027 1007 0214 OPEN STAT /OPEN STAT TO MOVE TO INTERFACE
1028
1029 1010 0071 ESP /STAT OR ERRS TO SR
1030 1011 0075 LSR
1031
1032 1012 0024 CLR SHIFT /CLEAR INTERFACE OUTPUT BUFFER
1033 1013 0020 CLR DONE
1034 1014 0010 CLR XREG
1035
1036 1015 0000 INTERF /SELECT INTERFACE OUTPUT BUSS
1037
1038 1016 0030 CLR SECDAT /SELECT SR AS DATA LINE SOURCE
1039
1040 1017 0010 SET IOOUT /DEFINE DATA DIRECTION AS OUT (TO INTERFACE)
1041
1042 1022 0070 LCT /MOVE SR TO INTERFACE SERIALLY
1043 1021 0367 -0-1
1044 1022 0026 SET SHIFT
1045 1023 0024 CLR SHIFT
1046 1024 0073 ICT
1047 1025 0074 ROTATE ZERO
1048 1026 0120 BR COFL F
1049 1027 1022 .-5
1050
1051 1030 0014 CLR IOOUT /NEXT TRANSFER WILL BE FROM INTERFACE
1052
1053 1031 0022 STDONE, SET DONE /FUNCTION IS DONE
1054 1032 0070 LCT /CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION
1055 1033 0370 PFUNCT
1056 1034 0222 JUMP F4
1057 1035 2001 GETCMD
1058
1059 1036 0074 FUNCT, ROTATE /MOVE UNIT SELECT BIT TO SR7
1060 1037 0074 ROTATE
1061 1040 0074 ROTATE
1062 1041 0122 BR SR7 ONE /FLAG IS ALREADY SET. SAVE UNIT IN FLAG, ONUNIT 0
1063 1042 1044 .+2
1064 1043 0061 FLAG OFF
1065
1066 1044 0074 ROTATE /GET FIRST FUNCTION BIT TO SR7

```

```

1067
1068 1045 0120 BR SR7 ZERO
1069 1046 1066 FUNCT4 /FUNCTION 4 OR GREATER
1070
1071 1047 0074 ROTATE /GET 2ND FUNCTION BIT
1072
1073 1050 0120 BR SR7 ZERO
1074 1051 1057 FUNCT2 /FUNCTION CODE IS 2 OR 3
1075
1076
1077 1052 0074 ROTATE /GET LAST FUNCTION BIT
1078
1079 1053 0120 BR SR7 ZERO
1080 1054 1107 EMPTYBUF /FUNCTION CODE 1
1081
1082 1055 0212 JUMP F2 /FUNCTION CODE 0
1083 1056 1110 FILLBUF
1084
1085 1057 0074 FUNCT2, ROTATE /GET LAST FUNCTION BIT
1086
1087 1060 0120 BR SR7 ZERO
1088 1061 1105 PROSEC /FUNCTION CODE 3
1089
1090 1062 0070 LCT /CLR CNTR BITS TO INDICATE NORMAL DATA
1091 1063 0200 0
1092 1064 0206 JUMP F1 /FUNCTION 2
1093 1065 0400 WRTSEC
1094
1095 1066 0074 FUNCT4, ROTATE /GET 2ND FUNCTION BIT
1096
1097 1067 0120 BR SR7 ZERO
1098 1070 1076 FUNCT6 /FUNCTION CODE IS 6 OR GREATER
1099
1100 1071 0074 ROTATE /GET LAST FUNCTION BIT
1101
1102 1072 0120 BR SR7 ZERO
1103 1073 1224 RDSTAT /FUNCTION 5
1104
1105 1074 0212 JUMP F2
1106 1075 1243 CLRID /FUNCTION 4=UNUSED
1107
1108 1076 0074 FUNCT6, ROTATE /GET LAST FUNCTION BIT
1109
1110 1077 0120 BR SR7 ZERO
1111 1080 1275 RDREG /FUNCTION 7
1112
1113 1081 0070 LCT /SET CNTR6 TO INDICATE DELETED DATA
1114 1082 0200 OCTAL
1115 1083 2127 LSP
1116 1084 0200 DECIMAL
1117 1085 2206 JUMP F1
1118 1086 0400 WRTSEC /FUNCTION 6
1119
1120 1087 0206 PROSEC, JUMP F1 /POINTER TO READ SECTOR FUNCTION
1121 1088 0760 RDSEC

```

```

1122
1123
1124
1125
1126
1127
1128
1129 /ROUTINE: FILL AND EMPTY BUFFER]
1130
1131
1132 1127 0210 EMPTYBUF, SET IOOUT /IOOUT IS CLEARED, SET IT TO INDICATE DATA IS
1133 /MOVING TO THE INTERFACE
1134
1135 1110 0074 FILLBUF, ROTATE ZERO /CLEAR STAT
1136 1111 0074 ROTATE ZERO
1137 1112 0210 OPEN STAT
1138 1113 0064 LSP
1139
1140 1114 0210 OPEN ERREG /CLEAR ERREG
1141 1115 0064 LSP
1142
1143 1116 0261 FLAG OFF /NOOP
1144
1145 1117 0064 CLR BAR SHORT /ADDRESS THE 1ST BIT OF SECTOR BUFFER
1146
1147 1120 0070 LCT /SET UP BYTE COUNT TO 128 (8 BIT) OR 64 (12 BIT)
1148 1121 0177 -128-1
1149 1122 0150 BR XIIBIT F
1150 1123 1126 ,+3
1151 1124 0070 LCT
1152 1125 0277 -64-1
1153 1126 0230 OPEN TEMP4
1154
1155 1127 0106 BR IOB3DT T /WHICH FUNCTION IS THIS?
1156 1130 1212 EMPTY1 /EMPTYBUF
1157
1158 1131 0012 XFRD, SET XREQ /REQUEST DATA TRANSFER
1159
1160 1132 0073 ICT /INCREMENT BYTE COUNT AND RESTORE
1161 1133 0075 LSP
1162 1134 0064 LSP
1163
1164 1135 0070 LCT /CALL WAITRUN SUBR TO WAIT FOR DATA TRANSFER
1165 1136 1141 NEWORD
1166 1137 2222 JUMP F4
1167 1140 2312 WAITRN
1168
1169 1141 0230 NEWORD, OPEN TEMP4 /REOPEN THE BYTE COUNT REGISTER BECAUSE WAITRUN CLOSED IT
1170 1142 0070 LCT /SET UP BIT COUNT IN CNTR TO 8 BITS OR 12 BITS
1171 1143 0367 -8-1
1172 1144 0150 BR XIIBIT F
1173 1145 1150 ,+3
1174 1146 0070 LCT
1175 1147 0363 -12-1
1176

```

```

1177 1150 0124 BR IOB30T F /WHICH FUNCTION IS THIS?
1178 1151 1175 FILL1 /FILLBUF
1179
1180
1181 1152 0026 BYTEOUT, SET SHIFT /EMPTYBUF, MOVE A BYTE FROM SECTOR BUFFER
1182 1153 0046 INCR BAR /TO INTERFACE SERIALY
1183 1154 2024 CLR SHIFT
1184 1155 0073 ICT
1185 1156 0124 BR COFL F
1186 1157 1152 BYTEOUT
1187
1188 1160 0071 ESP /CHECK BYTE COUNT
1189 1161 0124 BR COFL F
1190 1162 1131 XFRQ /NOT DONE, GO REQUEST A DATA TRANSFER
1191
1192 1163 0012 SET XREQ /DONE, REQUEST TRANSFER OF LAST BYTE
1193
1194 1164 0100 BR RUN F /WAIT FOR TRANSFER COMPLETION
1195 1165 1164 *-1
1196
1197 1166 0010 CLR XREQ
1198
1199 1167 0212 JUMP F2 /EMPTYBUF FUNCTION IS COMPLETE
1200 1170 1006 OKDONE
1201
1202 1171 0050 FIN WRTBUF /END SECTOR BUFR WRT PULSE (600 NS)
1203
1204 1172 0046 INCR BAR /ADDRESS NEXT CELL OF SECTOR BUFFER
1205
1206 1173 0026 SET SHIFT /SHIFT NEXT BIT FROM INTERFACE
1207 1174 0024 CLR SHIFT
1208
1209 1175 0053 FILL1, START WRTBUF /START SECTOR BUFR WRT PULSE
1210
1211 1176 0073 ICT /LAST BIT OF BYTE
1212 1177 0124 BR COFL F
1213 1200 1171 *-7 /NO, DO ANOTHER BIT
1214
1215 1201 0050 FIN WRTBUF /LAST BIT, END SECTOR BUFR WRT PULSE
1216
1217 1202 0046 INCR BAR /ADDRESS NEXT CELL OF SECTOR BUFFER
1218
1219 1203 0071 ESP /CHECK BYTE COUNT
1220 1204 0124 BR COFL F
1221 1205 1131 XFRQ /NOT DONE, GO GET ANOTHER BYTE
1222
1223 1206 0212 JUMP F2 /DONE FILLBUF FUNCTION
1224 1207 1006 OKDONE
1225
1226 1210 0032 EMPTY, SET SECDAT /SELECT SECTOR BUFR AS DATA LINE SOURCE
1227
1228 1211 0073 ICT /INCREMENT AND SAVE THE BYTE COUNT
1229 1212 0075 LSR
1230 1213 0064 LSP
1231

```

```

1232 1214 0070 LCT /SET UP THE BIT COUNT TO 8 BITS OR 12 BITS
1233 1215 0067 *-0-1
1234 1216 0150 OR #1191T F
1235 1217 1152 BYTEOUT
1236 1218 0070 LCT
1237 1221 0063 *-12-1
1238
1239 1222 0212 JUMP F2 /GO MOVE A BYTE TO INTERFACE
1240 1223 1152 BYTEOUT
1241
1242
1243
1244 /[ROUTINE: READ STATUS]
1245
1246 1224 0200 R0STAT, OPEN TEMPD /SELECT THE SOFT UNIT SCRATCH PAD
1247
1248 1225 0036 UNIT ONE /PRESELECT UNIT ONE
1249 1226 0070 LCT
1250 1227 0000 2
1251
1252 1230 0174 BR FLAG0 ZERO /WHICH UNIT? FLAG0=UNIT 1
1253 1231 1235 *-4 /UNIT 1, SKIP UNIT 0 SETUP
1254
1255 1232 0034 UNIT ZERO /SELECT UNIT ZERO
1256 1233 0070 LCT
1257 1234 0200 OCTAL
1258 1235 0200 200
1259 1236 0200 DECIMAL
1260
1261 1235 0075 LSR /STORE SOFT UNIT BIT
1262 1236 0064 LSP
1263
1264 1237 0070 LCT /CALL CHECKRDY SUBROUTINE, RETURN TO CLRID
1265 1240 1765 PNTRDY
1266 1241 0226 JUMP F5
1267 1242 0000 CHKRDY
1268
1269
1270
1271
1272 1243 0214 CLRID, OPEN STAT /CLEAR INIT DONE BIT OF STAT
1273 1244 0071 ESP /STATUS TO SHIFT REG
1274 1245 0075 LSR
1275
1276 1246 0061 FLAG OFF
1277 1247 0070 LCT /END AROUND SHIFT OF FIRST 5 BITS
1278 1250 0372 *-5-1
1279 1251 0122 ROT, BR SR7 T
1280 1252 1250 *-4
1281 1253 0074 ROTATE ZERO
1282 1254 0212 JUMP F2
1283 1255 1257 *-2
1284 1256 0076 ROTATE ONE
1285 1257 0073 ICT
1286 1260 0124 BR COFL F

```

```

1287 1261 1251      .-8
1288
1289 1262 0176      BR FLAG0 T      /IF FLAG IS SET THEN ROTATE IS DONE
1290 1263 1272      GOODUN
1291
1292 1264 0062      FLAG ON      /IF NOT, CLEAR INIT DONE AND FINISH ROTATE
1293 1265 0074      ROTATE ZERO
1294 1266 0070      LCT
1295 1267 0375      =2-1
1296 1270 0212      JUMP F2
1297 1271 1251      ROT
1298
1299
1300 1272 0064      GOODUN, LSP      /RESTORE STAT AND GO DONE
1301 1273 0212      JUMP F2
1302 1274 1006      OKDONE
1303
1304      /[ROUTINE: READ ERROR REGISTER]
1305
1306
1307
1308 1275 0210      RDEREG, OPEN ERREG
1309 1276 0212      JUMP F2
1310 1277 1010      OKDONE+2
1311
1312
1313      /[SUBROUTINE: DELAY]. THIS SUBROUTINE PROVIDES DELAYS IN MULTIPLES
1314      /OF .1MS. ENTER WITH RETURN ADDRESS IN THE SHIFT REG,
1315      /AND MULTIPLIER IN THE COUNTER
1316
1317
1318 1300 0264      DELAY, OPEN RTNB      /SAVE THE RETURN ADDRESS
1319 1301 0064      LSP
1320
1321 1302 0075      LSR      /MULTIPLIER TO SHIFT REGISTER
1322
1323 1303 0070      LCT      /DELAY 490 CYCLES (90 MICRO SECONDS)
1324 1304 0205      =122-1
1325 1305 0273      ICT
1326 1306 0264      OPEN RTNB
1327 1307 0120      BR COFL F
1328 1310 1305      .-3
1329
1330 1311 0071      ESP      /MOVE MULTIPLIER TO CNTR VIA RTNB
1331 1312 0064      LSP
1332 1313 0075      LSR
1333 1314 0071      ESP
1334 1315 0264      LSP
1335
1336 1316 0273      ICT      /INCREMENT THE MULTIPLIER
1337
1338 1317 0124      BR COFL F      /ANY MORE .1MS LOOPS?
1339 1320 1301      DELAY+1      /YES, GO TO IT
1340
1341 1321 0223      JUMP F4 IND      /NO, RETURN FROM SUBROUTINE

```

```

1342
1343      /[SUBROUTINE: WRITE ZEROS]
1344      /THIS SUBROUTINE WRITES A SPECIFIED NUMBER OF ZEROS IF
1345      /WRITE GATE IS ON. IF WRITE GATE IS OFF IT ACTS AS A
1346      /DELAY OF .5 BITS. ENTRANCE IS MADE WITH RETURN ADDRESS
1347      /IN THE SR, NUMBER OF BITS IN THE CNTR, AND A CLOCK
1348      /TRANSITION OCCURRING IMMEDIATELY PRIOR TO THE JUMP INTO
1349      /THIS SUBROUTINE.
1350
1351
1352 1322 0270      RTNB, OPEN RTNB      /SAVE RETURN ADDRESS
1353 1323 0064      LSP
1354
1355 1324 0075      LSR      /PUT BIT COUNTER IN SR
1356
1357 1325 0230      OPEN TEMPB      /TEMPB IS THE PATH THROUGH THE SR
1358
1359 1326 0070      LOOP, LCT      /STALL 2.6 MICRO SECONDS
1360 1327 0374      =3-1
1361 1330 0273      ICT
1362 1331 0124      BR COFL F
1363 1332 1330      .-2
1364 1333 0064      LSP      /NOOP
1365 1334 0071      ESP      /NOOP
1366
1367 1335 0063      TRG FLAG      /WRITE A CLOCK TRANSITION IF WRT GATE IS SET
1368
1369 1336 0064      LSP      /PUT BIT COUNT IN THE COUNTER
1370 1337 0071      ESP
1371
1372 1340 0073      ICT      /INCREMENT BIT COUNT
1373
1374 1341 0075      LSR      /PUT UPDATED BIT COUNT BACK IN SR
1375
1376 1342 0124      BR COFL F      /DONE ALL BITS?
1377 1343 1326      LOOP      /NO
1378
1379 1344 0274      OPEN RTNB      /YES, RETURN FROM SUBROUTINE
1380 1345 0207      JUMP IND F1
1381
1382
1383 1346 0222      PGOTIT, JUMP F4      /POINTER TO GETWORD FROM WAITRUN
1384 1347 0010      GOTIT
1385
1386
1387      /[ROUTINE: INITIALIZE CONT.]
1388
1389 1350 0061      TEST2, FLAG OFF      /CLEAR FLAG TO INDICATE R10 IS BEING TESTED
1390
1391 1351 0070      TEST1, LCT      /LOOP TO TEST THAT SR IS 252 AND THAT
1392 1352 0372      =5-1      /IT CAN BE SHIFTED.
1393 1353 0120      TSTAGN, BR SR7 ZERO
1394 1354 1374      INTER1      /TEST FAILURE
1395 1355 0070      ROTATE ONE
1396 1356 0122      BR SR7 ONE

```

```

1397 1357 1374 INTER1 /TEST FAILURE
1398 1360 0074 ROTATE ZERO
1399 1361 0073 ICT
1400 1362 0124 BR COFL F
1401 1363 1353 TSTAGN
1402
1403 1364 0250 OPEN R10 /CONTENTS OF R10 TO SR, SHOULD BE 125
1404 1365 0071 ESP
1405 1366 0075 LSR
1406
1407 1367 0074 ROTATE ZERO /SHIFT SR ONCE TO CHANGE 125 TO 252
1408
1409 1370 0176 BR FLAGO ONE /HAS R10 BEEN TESTED ALREADY?
1410 1371 1350 TEST2 /NO
1411
1412 1372 0202 TESTDN, JUMP F0 /YES, RETURN TO REMAINING INITIALIZE ROUTINE
1413 1373 0004 TSTRN
1414
1415 1374 0006 INTER1, SET ERR /SELF TEST ERROR, SET ERROR AND GO SET DONE
1416 1375 0212 JUMP F2
1417 1376 1031 STDONE
1418
1419 1377 0000 0 /OPEN

```

```

1420 /[SUBROUTINE: FINDHEADER AND FIND DATA ADDRESS MARK]
1421 /SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK #)
1422 /ENTER WITH THE RETURN ADDRESS IN CNTR. ALSO ROUTINE TO FIND A DATA MARK
1423 /ON DELETED DATA MARK.
1424
1425 /THIS ROUTINE LOCATED A SIX BYTE PREAMBLE OF ZEROS.
1426
1427
1428 1400 0204 FINDND, OPEN RTNB /STORE RETURN ADDRESS
1429 1401 0075 LSR
1430 1402 2404 LSP
1431
1432 1403 0230 OPEN TEMPA /256 TO BAD START INNER COUNT
1433 1404 0070 LCT
1434 1405 0377 -1
1435 1406 0075 LSR
1436 1407 0004 LSP
1437
1438 1410 0234 OPEN TEMPB /3 TO CNTR FOR BAD START OUTER COUNT, 768 BAD STARTS ALLOWED
1439 1411 0070 LCT
1440 1412 0370 -3-1
1441
1442 1413 0075 TRYAGN, LSR /RESTORE BAD START COUNT
1443 1414 0004 LSP
1444
1445 1415 0045 CLR BAR LONG /RESET FOR A COUNT OF 4096 AS PREAMBLE FAILURE COUNT
1446
1447 1416 0240 OPEN TEMPC /24 TO CNTR AS ZERO BIT COUNT
1448 1417 0070 LCT
1449 1420 0307 -24-1
1450 1421 0075 MORE0S, LSR /RESTORE ZERO BIT COUNT
1451 1422 0004 LSP
1452
1453 1423 0070 LCT /PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 40 MICRO SEC WAIT BRANCH
1454 1424 0067 -200-1
1455 1425 0075 LSR
1456
1457 1426 0300 WBR SEPCLK T /WAIT 40 MICRO SECONDS FOR SEP CLK
1458 1427 1432 +3
1459
1460 1430 0216 JUMP F3 /ERROR, NO SEP CLK
1461 1431 1667 TIMERR
1462
1463 1432 0154 BR DECSR7 F /WHAT IS SEP DATA?
1464 1433 1746 NOZERO /ONE, GO CHECK PREAMBLE FAILURES
1465
1466 1434 0071 ESP /ZERO FOUND, CHECK ZERO COUNT
1467 1435 0073 ICT
1468 1436 0124 BR COFL F
1469 1437 1021 MORE0S /NEED MORE ZEROS FOR PREAMBLE
1470 1440 0001 FLAG OFF /FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM
1471
1472 1441 0005 GETDAM, CLR BAR LONG /START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER
1473
1474 1442 0070 LCT /WAIT 40 MICRO SEC FOR SEP CLK

```

1475	1443	0067	-200-1	
1476	1444	0346	WBR SEPCLK T	
1477	1445	1450	.+3	
1478	1446	0216	JUMP F3	/TIMING ERROR
1479	1447	1667	TIMERR	
1480				
1481	1450	0156	BR DEQSR7 T	/WHAT IS SEP DATA?
1482	1451	1755	NOTYET	/ZERO, GO DETERMINE IF TOO MANY STARTS
1483				
1484	1452	0164	BR MCEQSR F	/ONE, MISSING CLOCK?
1485	1453	1673	BADSRT	/YES, SHOULDN'T HAVE BEEN
1486				
1487	1454	0057	PRECRC	/JAM 1ST TWO BITS OF CRC
1488	1455	0056	CRC ONE	
1489	1456	0056	CRC ONE	
1490				
1491	1457	0070	LCT	/WAIT 40 MICRO SECONDS FOR SECOND CELL
1492	1460	0067	-200-1	
1493	1461	0346	WBR SEPCLK T	
1494	1462	1465	.+3	
1495	1463	0216	JUMP F3	
1496	1464	1667	TIMERR	
1497				
1498	1465	0156	BR DEQSR7 T	/DATA SHOULD BE 1, MISSING CLK SHOULD BE T
1499	1466	1673	BADSRT	
1500	1467	0166	BR MCEQSR T	
1501	1470	1673	BADSRT	
1502				
1503	1471	0056	CRC ONE	/JAM 3 MORE CRC BITS
1504	1472	0056	CRC ONE	
1505	1473	0056	CRC ONE	
1506				
1507	1474	0070	LCT	/WAIT FOR THIRD BIT CELL
1508	1475	0067	-200-1	
1509	1476	0346	WBR SEPCLK T	
1510	1477	1502	.+3	
1511	1500	0216	JUMP F3	
1512	1501	1667	TIMERR	
1513				
1514	1502	0154	BR DEQSR7 F	/DATA SHOULD BE 0, MISSING CLK SHOULD BE F
1515	1503	1673	BADSRT	
1516	1504	0164	BR MCEQSR F	
1517	1505	1673	BADSRT	
1518				
1519	1506	0070	LCT	/CLEAR BR
1520	1507	0000	0	
1521	1510	0075	LSR	
1522				
1523	1511	0070	LCT	/WAIT FOR 4TH BIT CELL
1524	1512	0267	-200-1	
1525	1513	0346	WBR SEPCLK T	
1526	1514	1517	.+3	
1527	1515	0216	JUMP F3	
1528	1516	1667	TIMERR	
1529				

1530	1517	0154	BR DEQSR7 F	/DATA SHOULD BE 0, MISSING CLK SHOULD BE F
1531	1520	1673	BADSRT	
1532	1521	0042	LDMD	/NOOP FOR LONG SEP CLOCK
1533	1522	0042	LDMD	/NOOP FOR LONG SEP CLOCK
1534	1523	0164	BR MCEQSR F	
1535	1524	1673	BADSRT	
1536				
1537	1525	0070	LCT	/WAIT FOR FIFTH BIT CELL
1538	1526	0267	-200-1	
1539	1527	0346	WBR SEPCLK T	
1540	1532	1533	.+3	
1541	1531	0216	JUMP F3	
1542	1532	1667	TIMERR	
1543				
1544	1533	0156	BR DEQSR7 T	/DATA SHOULD BE 1
1545	1534	1673	BADSRT	
1546				
1547	1535	0176	BR FLAGO T	/IF FLAG SET FINISH LOOKING FOR DATA AM
1548	1536	1675	DAM	
1549				
1550	1537	0164	BR MCEQSR F	/FINISH IDAM, MISSING CLK SHOULD BE F
1551	1540	1673	BADSRT	
1552				
1553	1541	0256	CRC ONE	/JAM 6TH CRC BIT OF IDAM
1554				
1555	1542	0270	LCT	/WAIT FOR SIXTH BIT CELL
1556	1543	0067	-200-1	
1557	1544	0346	WBR SEPCLK T	
1558	1545	1550	.+3	
1559	1546	0216	JUMP F3	
1560	1547	1667	TIMERR	
1561				
1562	1552	0156	BR DEQSR7 T	/DATA SHOULD BE 1, MISSING CLK SHOULD BE F
1563	1551	1673	BADSRT	
1564	1552	0164	BR MCEQSR F	
1565	1553	1673	BADSRT	
1566				
1567	1554	0042	LDMD	/NOOP FOR LONG SEP CLOCK
1568				
1569	1555	0056	CRC ONE	/JAM 7TH CRC BIT OF IDAM
1570				
1571	1556	0070	LCT	/WAIT FOR SEVENTH BIT CELL
1572	1557	0067	-200-1	
1573	1560	0346	WBR SEPCLK T	
1574	1561	1564	.+3	
1575	1562	0216	JUMP F3	
1576	1563	1667	TIMERR	
1577				
1578	1564	0156	BR DEQSR7 T	/DATA SHOULD BE 1, MISSING CLK SHOULD BE T
1579	1565	1673	BADSRT	
1580	1566	0166	BR MCEQSR T	
1581	1567	1673	BADSRT	
1582				
1583	1570	0054	CRC ZERO	/IDAM FOUND, JAM LAST CRC BIT
1584				

```

1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639

```

/THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
 /DESIRED TRACK ADDRESS ON THE FLY. IT IS ENTERED AFTER
 /FINDING THE IDAM. ERREG BIT 4 IS SET IF AN ERROR IS DETECTED.

```

1594 1571 0220  WDRCOM, OPEN TARTRK  /TARGET TRACK ADDRESS TO SR
1595           ESP
1596 1573 0075  LSR
1598 1574 0070  LCT  /SET BIT COUNTER TO 0
1599 1575 0307  -0-1
1601 1576 0144  AGAIN3, BR SEPCLK F  /WAIT FOR BIT CELL
1602 1577 1576           .-1
1604 1600 0156  BR DECSR7 T  /SEP DATA EQUAL TO SR??
1605 1601 1605           .+4  /NO, TRACK COMPARE ERROR
1607 1602 0074  ROTATE ZERO  /YES, GET NEXT TRACK ADDRESS BIT
1608 1603 0216  JUMP F3
1609 1604 1610           .+4
1611 1605 0210  OPEN ERREG  /SET ERREG BIT 4 TO INDICATE TRACK ERROR
1612 1606 0076  ROTATE ONE
1613 1607 0004  LSR
1615 1610 0055  DATCRC  /UPDATE THE CRC
1617 1611 0073  ICT  /INCREMENT AND TEST THE BIT COUNTER
1618 1612 0124  BR COFL F
1619 1613 1576  AGAIN3  /GO DO NEXT BIT
1621 1614 0070  LCT  /TRACK COMPARED, SET UP BIT COUNTER FOR 0 BYTE
1622 1615 0307  -0-1
1624 1616 0144  AGAIN4, BR SEPCLK F  /WAIT FOR BIT
1625 1617 1616           .-1
1627 1620 0001  FLAG OFF  /CLEAR FLAG FOR NEXT ROUTINE
1628 1621 0001  FLAG OFF  /NOOP FOR LONG SEP CLK
1629 1622 0001  FLAG OFF  /NOOP FOR LONG SEP CLK
1630 1623 0001  FLAG OFF  /NOOP FOR LONG SEP CLK
1632 1624 0055  DATCRC  /UPDATE CRC
1634 1625 0073  ICT  /INCREMENT AND TEST BIT COUNT
1635 1626 0124  BR COFL F
1636 1627 1616  AGAIN4  /GO DO ANOTHER BIT
1637           /CONTINUE

```

```

1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694

```

/THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
 /TARGET SECTOR ADDRESS ON THE FLY. IT IS ENTERED FROM
 /THE TRACK COMPARE ROUTINE. A MISMATCH WILL SET THE FLAG.

```

1645 1630 0224  OPEN TARSEC  /TARGET SECTOR ADDRESS TO SR
1646 1631 0071  ESP
1647 1632 0075  LSR
1649 1633 0070  LCT  /SET UP BIT COUNTER FOR 0 BITS
1650 1634 0307  -0-1
1652 1635 0144  AGAIN5, BR SEPCLK F  /WAIT FOR A BIT
1653 1636 1635           .-1
1655 1637 0156  BR DECSR7 T  /HOW DO THEY COMPARE?
1656 1640 1643           .+3  /BAD, GO SET THE FLAG
1658 1641 0216  JUMP F3  /GOOD, SKIP THE ERROR FLAG.
1659 1642 1644           .+2
1661 1643 0002  FLAG ON  /SET FLAG TO INDICATE MISMATCH
1663 1644 0074  ROTATE ZERO  /BRING UP NEXT BIT
1665 1645 0055  DATCRC  /UPDATE THE CRC
1666 1646 0073  ICT  /BUMP THE BIT COUNTER
1667 1647 0124  BR COFL F  /ALL BITS COMPARED?
1668 1650 1635  AGAIN5  /NO, LOOP BACK
1670 1651 0070  LCT  /YES, SETUP TO WAIT FOR END OF
1671 1652 0347  -20-1  /CRC
1673 1653 0144  AGAIN6, BR SEPCLK F  /WAIT FOR BIT
1674 1654 1653           .-1
1676 1655 0074  ROTATE ZERO  /NOOP FOR LONG SEP CLK
1677 1656 0074  ROTATE ZERO  /NOOP FOR LONG SEP CLK
1678 1657 0074  ROTATE ZERO  /NOOP FOR LONG SEP CLK
1679 1660 0074  ROTATE ZERO  /NOOP FOR LONG SEP CLK
1681 1661 0055  DATCRC  /UPDATE CRC
1683 1662 0073  ICT  /BUMP THE BIT COUNTER
1684 1663 0124  BR COFL F  /ALL DONE?
1685 1664 1653  AGAIN6  /NO, LOOP BACK
1687 1665 0226  JUMP F5  /YES, SO CHECK IF CRC IS ALL ZEROS
1688 1666 2515  CKMCRC
1691 1667 0070  TIMERR, LCT  /40 MICROSEC PASSED AND NO SEP CLOCK HAS BEEN
1692 1670 0110  MTIMERR
1693 1671 0220  JUMP F5
1694 1672 2610  GOERDN

```



```

1695
1696
1697 1673 0226 BADSRT, JUMP F5 /POINTER TO BADSTART ON IDAM OR DATA AM
1698 1674 2555 BDSRT
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708 1675 0166 DAM, BR MCEQSR T /MISSING CLK SHOULD BE T
1709 1676 1673 BADSRT
1710
1711 1677 0054 CRC ZERO /JAM 6TH CRC BIT OF DATA AM
1712
1713 1700 0070 LCT /WAIT FOR SIXTH BIT CELL
1714 1701 0067 =200-1
1715 1702 0340 =BR SEPCLK T
1716 1703 1706 +3
1717 1704 0216 JUMP F3
1718 1705 1667 TIMERR
1719
1720 1706 0164 BR MCEQSR F /MISSING CLK SHOULD BE F
1721 1707 1673 BADSRT
1722 1710 0042 LDMD /NOOP FOR LONG SEP CLK
1723
1724 1711 0156 BR DEQSR7 T /IF DATA0 THEN LOOK FOR DELETED DATA AM
1725 1712 1727 DELDAT
1726
1727 1713 0056 CRC ONE /JAM 7TH BIT OF DATA AM
1728
1729 1714 0070 LCT /WAIT FOR SEVENTH BIT OF DATA AM
1730 1715 0067 =200-1
1731 1716 0340 =BR SEPCLK T
1732 1717 1722 +3
1733 1720 0216 JUMP F3
1734 1721 1667 TIMERR
1735
1736 1722 0056 CRC ONE /JAM LAST BIT OF DATA AM
1737
1738 1723 0154 BR DEQSR7 F /DATA SHOULD BE 1
1739 1724 1742 ENDDAM /FLAG IS SET TO INDICATE NORMAL DATA MARK
1740
1741 1725 0216 JUMP F3 /LAST DATA BIT WAS BAD
1742 1726 1673 BADSRT
1743
1744
1745 1727 0054 DELDAT, CRC ZERO /JAM 7TH CRC BIT OF DEL DATA AM
1746
1747 1730 0070 LCT /WAIT FOR 7TH CELL OF DEL DATA AM
1748 1731 0067 =200-1
1749 1732 0340 =BR SEPCLK T

```

```

1750 1733 1736 +3
1751 1734 0216 JUMP F3
1752 1735 1667 TIMERR
1753
1754 1736 0061 FLAG OFF /CLR FLAG TO INDICATE DELETED DATA MARK
1755
1756 1737 0054 CRC ZERO /JAM LAST CRC BIT OF DEL DATA AM
1757
1758 1740 0154 BR DEQSR7 F /DATA SHOULD BE 0
1759 1741 1673 BADSRT
1760
1761 1742 0164 ENDDAM, BR MCEQSR F /MISSING CLK SHOULD BE F FOR BOTH DATA AMS
1762 1743 1673 BADSRT
1763
1764 1744 0222 JUMP F4 /GO PICK UP DATA FIELD
1765 1745 2296 DATA
1766
1767
1768 1746 0046 NOZERO, INCR BAR /INCREMENT AND TEST PREAMBLE FAILURE COUNT
1769 1747 0164 BR BAROFL F
1770 1750 1416 TRYAGN+3 /OK, TRY AGAIN FOR A PREAMBLE
1771
1772 1751 0070 NXPRAM, LCT /TOO MANY BITS WITH NO ZEROS
1773 1752 0120 NXPRAM
1774 1753 0226 JUMP F5
1775 1754 2610 GOERDN
1776
1777
1778 1755 0046 NOTVET, INCR BAR /INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
1779 1756 0042 LDMD /NOOP FOR LONG SEP CLK
1780 1757 0160 BR BAROFL F
1781 1760 1442 GETOAM+1 /OK, TRY AGAIN
1782
1783 1761 0070 NXIDAM, LCT /TOO MANY ZEROS WHILE LOOKING FOR START OF
1784 1762 0136 NXIDAM /IDAM OR DATA AM
1785 1763 0226 JUMP F5
1786 1764 2610 GOERDN
1787
1788
1789 1765 0212 PTRDY, JUMP F2 /POINTERS FROM CHECKRDY SUBROUTINE TO ROSTAT ROUTINE
1790 1766 1243 CLRID
1791 1767 0212 PYSRDY, JUMP F2
1792 1772 1243 CLRID
1793
1794 1771 0212 PNDROY, JUMP F2 /POINTERS FROM CHECK RDY TO INITIALIZE ROUTINE
1795 1772 1006 OKDONE
1796 1773 0226 JUMP F5
1797 1774 2631 INTRDY
1798
1799 1775 0000 0 /OPEN
1800 1776 0000 0 /OPEN
1801 1777 0000 0 /OPEN
1802

```

```

1803 /SUBROUTINES: GETWORD AND GETCOMMAND
1804 /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE.
1805 /IF TALKING TO A PDP8 INTERFACE IN 12 BIT MODE, THERE
1806 /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1807 /BIT WORD, ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1808 /IN THE COUNTER, EXIT WITH THE ONES COMPLIMENT OF THE
1809 /DESIRED WORD IN THE SHIFT REGISTER, PARITY IS COMPUTED AND
1810 /CHECKED ON ALL WORDS,
1811
1812
1813 2000 0012 GETWRD, SET XREQ /REQUEST A WORD FROM INTERFACE
1814
1815 2001 0075 GETCMD, LSR /STASH THE RETURN ADDRESS
1816 2002 0270 OPEN RTNA
1817 2003 0064 LSP
1818
1819 2004 0070 LCT /CALL SUBR WAITRN TO WAIT FOR A WORD
1820 2005 1346 PGOTIT
1821 2006 0222 JUMP F4
1822 2007 2312 WAITRN
1823
1824 2010 0001 GOTIT, OFF FLAG /CLEAR FLAG FOR PARITY CHECK
1825
1826 2011 0004 CLR ERR /IN CASE RUN HAS A RESPONSE TO DONE
1827 2012 0020 CLR DONE
1828
1829 2013 0070 LCT /SET UP BIT COUNT IN CNTR, 8 BIT OR 12 BIT
1830 2014 0367 =0-1
1831 2015 0150 BR XIIBIT F
1832 2016 2021 ,+3
1833 2017 0070 LCT
1834 2020 0363 =12-1
1835
1836 2021 0112 *ATDAT, BR DATAIN ONE /WHAT IS THE DATA BIT?
1837 2022 2730 GOTONE /ITS A ONE, GO SAVE IT
1838
1839 2023 0126 BR COFL T /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
1840 2024 2041 CHKPAR /YES, GO CHECK PARITY
1841
1842 2025 0076 ROTATE ONE /NO SAVE THE DATA BIT COMPLIMENTED IN BR
1843
1844 2026 0222 JUMP F4 /GO SHIFT UP ANOTHER BIT.
1845 2027 2034 *UTHER
1846
1847
1848
1849
1850 2032 2003 GOTONE, TUG FLAG /COMPLIMENT THE PARITY GENERATOR
1851
1852 2031 2126 BR COFL T /WAS IT THE PARITY BIT?
1853 2032 2041 CHKPAR /YES, GO CHECK PARITY
1854
1855 2033 0076 ROTATE ZERO /NO, SAVE THE COMPLIMENTED DATA BIT IN BR
1856
1857 2034 0026 *UTHER, SET SHIFT /SHIFT PULSE AND INCREMENT BIT COUNT

```

```

1858 2035 0073 LCT
1859 2036 0024 CLR SHIFT
1860
1861 2037 0222 JUMP F4 /GO TEST THIS BIT.
1862 2038 2021 *ATDAT
1863
1864
1865 2041 0176 CHKPAR, BR FLAGD ONE /WHERE THERE AN ODD NO. OF ONES?
1866 2042 2076 GOTARD /YES, PARITY HAS GOOD
1867
1868 2043 0214 OPEN STAT /NO, STAT TO SR
1869 2044 0271 ESP
1870 2045 0075 LSR
1871
1872 2046 0070 LCT /END AROUND SHIFT OF UPPER 5 BITS OF STAT IN BR
1873 2047 0372 =5-1
1874 2050 0122 RR SR7 T
1875 2051 2055 ,+4
1876 2052 0074 ROTATE ZERO
1877 2053 0222 JUMP F4
1878 2054 2056 ,+2
1879 2055 0076 ROTATE ONE
1880 2056 0073 LCT
1881 2057 0124 BR COFL F
1882 2060 2050 =0
1883
1884 2061 0074 ROTATE ZERO /CLEAR INIT DONE
1885 2062 0076 ROTATE ONE /SET PARITY ERROR
1886
1887 2063 0122 BR SR7 T /END AROUND SHIFT OF CRC ERROR BIT OF STAT IN BR
1888 2064 2070 ,+4
1889 2065 2074 ROTATE ZERO
1890 2066 0222 JUMP F4
1891 2067 2071 ,+2
1892 2070 0076 ROTATE ONE
1893
1894 2071 0064 LSP /RESTORE STAT TO SCRATCH PAD
1895
1896 2072 0070 LCT /ERRCODE FOR PARITY ERROR
1897 2073 0210 *PARER
1898 2074 0226 JUMP F5
1899 2075 2610 GCERDN
1900
1901 2076 0270 GOTWRD, OPEN RTNA /WORD HAS GOOD, EXIT FROM GETWRD, GETCMD
1902 2077 0203 JUMP F0 IND

```

```

1900
1904 /([SUBROUTINE: STEPHEAD])
1905 /THIS SUBROUTINE WILL STEP THE SPECIFIED NUMBER OF TRACKS IN THE
1906 /SPECIFIED DIRECTION. DIRECTION IS DETERMINED BY THE HD DIR FLOP
1907
1908 /THE NUMBER OF STEPS IS IN THE SR. RETURN ADDRESS IS IN THE CNTR.
1909 /EXIT IS TO THE RETURN ADDRESS IF HOME IS DETECTED. EXIT IS TO RETURN
1910 /PLUS 2 IF THE LAST STEP HAS BEEN TAKEN. AFTER THE LAST STEP IS TAKEN,
1911 /THE HEAD IS LOADED AND A 25MS DELAY IS EXECUTED FOR HEAD SETTLE TIME
1912
1913
1914
1915
1916 2100 0270 STEPND, OPEN RTNA /STORE RETURN ADDR AND MOVE STEP COUNT TO CNTR
1917 2101 0064 LSR
1918 2102 0075 LSR
1919 2103 0071 ESP
1920 2104 0064 LSP
1921
1922 2105 0136 CKHOME, BR HOME T /IS THE HEAD HOME?
1923 2106 2150 OUT /YES, GO EXIT
1924
1925 2107 0073 ICT /NO, INCREMENT STEP COUNT AND STORE IN TEMPB
1926 2110 0075 LSR
1927 2111 0230 OPEN TEMPB
1928 2112 0064 LSP
1929
1930 2113 0070 LCT /PASS 30 TO DELAY SUBR FOR 3MS DELAY
1931 2114 2124 SECPLS
1932 2115 0075 LBR
1933 2116 0070 LCT
1934 2117 0341 -30-1
1935
1936 2120 0012 SET STPHD /ISSUE STEP PULSE
1937 2121 0010 CLR STPHD
1938
1939 2122 0212 JUMP F2 /CALL DELAY SUBR
1940 2123 1300 DELAY
1941
1942 2124 0012 SECPLS, SET STPHD /ISSUE SECOND STEP PULSE
1943 2125 0010 CLR STPHD
1944
1945 2126 0070 LCT /CALL DELAY FOR 3MS DELAY
1946 2127 2135 DONSTP
1947 2130 0075 LSR
1948 2131 0070 LCT
1949 2132 0341 -30-1
1950 2133 0212 JUMP F2
1951 2134 1300 DELAY
1952
1953 2135 0230 DONSTP, OPEN TEMPB /CHECK STEP COUNT
1954 2136 0071 ESP
1955 2137 2124 BR COFL F
1956 2140 2105 CKHOME /NOT DONE, GO CHECK IF HOME
1957

```

```

1958 2141 0270 OPEN RTNA /DONE STEPPING, INCREMENT RETURN ADDRESS BY 2
1959 2142 0071 ESP
1960 2143 0073 ICT
1961 2144 0073 ICT
1962
1963 2145 0270 DLY25, OPEN RTNA /STORE RETURN ADDRESS ALSO START OF 25MS DELAY SUBROUTINE
1964 2146 0075 LSR
1965 2147 0064 LSP
1966
1967 2150 0042 OUT, LDHD /LOAD HEAD
1968 2151 0250 OPEN TEMPB /SET SOFT HD LOAD BIT
1969 2152 0070 LCT
1970 OCTAL
1971 2153 0200 200
1972 DECIMAL
1973 2154 0075 LSR
1974 2155 0064 LSP
1975
1976 2156 0070 LCT /CALL DELAY SUBR FOR 25MS DELAY
1977 2157 2165 DONDLY
1978 2160 0075 LSR
1979 2161 0070 LCT
1980 2162 0000 -255-1
1981 2163 0212 JUMP F2
1982 2164 1300 DELAY
1983
1984 2165 0270 DONDLY, OPEN RTNA /RETURN FROM STEP HEAD OR DELAY 25MS SUBROUTINE
1985 2166 0203 JUMP F0 IND
1986
1987
1988
1989
1990
1991
1992
1993 /([ROUTINE: READ SECTOR CONT.])
1994
1995 2167 0070 READ, LCT /3 TO DATA MARK TRY COUNTER
1996 2170 0374 -3-1
1997 2171 0234 OPEN TEMPB
1998 2172 0075 LSR
1999 2173 0064 LSP
2000
2001 2174 0070 LCT /STALL FOR 96 MICRO SEC (3 BYTES) TO AVOID WRT TURN ON SPLASH
2002 2175 0207 -120-1
2003 2176 0073 ICT
2004 2177 0062 FLAG ON /SET THE FLAG TO SPECIFY DATA AM IN FIND AM ROUTINE
2005 2200 0124 BR COFL F
2006 2201 2176 -3
2007
2008 2202 0073 ICT /CLR COUNTER AND SR
2009 2203 0075 LSR
2010
2011 2204 0216 JUMP F3 /GO TRY FIND THE ADDRESS MARK
2012 2205 1441 GETDAM

```

```

2013
2014
2015
2016      /THIS ROUTINE FOLLOWS THE DISCOVERY OF A DATA MARK OR
2017      /A DELETED DATA MARK. IT MOVES THE NEXT 1024 BITS
2018      /INTO THE SECTOR BUFFER, THEN PICKS UP AND CHECKS THE CRC.
2019      2206 0044 DATA, CLR BAR      /CLEAR THE BUFFER ADDRESS REGISTER
2020
2021      2207 0144 BR SEPCLK F      /WAIT FOR CLOCK
2022      2210 2207 .-1
2023
2024      2211 0053 START WRTBUF      /START THE WRITE PULSE FOR THIS BIT
2025
2026      2212 0055 DATCRC           /UPDATE THE CRC WITH SEP DATA
2027
2028      2213 0162 BR BAROFL T      /IS BUFFER FULL YET?
2029      2214 2221 GETCRC           /YES, GO GET THE CRC
2030
2031      2215 0050 FIN WRTBUF       /NO, END THE WRITE PULSE
2032
2033      2216 0046 INCR BAR         /ADDRESS NEXT SECTOR BUFFER CELL
2034
2035      2217 0222 JUMP F4         /LOOP BACK FOR NEXT BIT
2036      2220 2207 DATA+1
2037
2038      2221 0050 GETCRC, FIN WRTBUF /END THE WRITE PULSE FOR THE LAST BIT
2039
2040      2222 0070 LCT              /SET BIT COUNT TO 16 FOR 2 BYTE CRC
2041      2223 0357 -16-1
2042
2043      2224 0144 BR SEPCLK F      /WAIT FOR NEXT BIT
2044      2225 2224 .-1
2045
2046      2226 0042 LDMD            /4 NOOPS FOR LONG SEP CLOCK
2047      2227 0042 LDMD
2048      2230 0042 LDMD
2049      2231 0042 LDMD
2050
2051      2232 0055 DATCRC           /PUT CRC BIT IN THE CRC GENERATOR
2052      2233 0073 ICT              /INCREMENT AND TEST BIT COUNT
2053      2234 0124 BR COFL F      /NOT DONE, GET ANOTHER
2054      2235 2224 .-9
2055
2056      2236 0214 OPEN STAT        /STATUS TO SHIFT REG
2057      2237 0071 ESP
2058      2240 2075 LSR
2059
2060      2241 2122 BR SR7 T         /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
2061      2242 2246 .+4
2062      2243 0074 ROTATE ZERO
2063      2244 0222 JUMP F4
2064      2245 2247 .+2
2065      2246 0076 ROTATE ONE
2066
2067      2247 0176 BR FLAGO T      /SET DEL DATA BIT OF STAT IF FLAG=0
    
```

```

2068      2252 2254 .+4
2069      2251 2276 ROTATE ONE
2070      2252 2222 JUMP F4
2071      2253 2255 .+2
2072      2254 2274 ROTATE ZERO
2073
2074      2255 2270 LCT              /END AROUND SHIFT OF NEXT 5 BITS OF STAT IN SR
2075      2256 2372 -5-1
2076      2257 0122 BR SR7 T
2077      2260 2264 .+4
2078      2261 2374 ROTATE ZERO
2079      2262 2222 JUMP F4
2080      2263 2265 .+2
2081      2264 2076 ROTATE ONE
2082      2265 2073 ICT
2083      2266 0124 BR COFL F
2084      2267 2257 .-8
2085
2086      2270 2076 LCT              /SET BIT COUNTER TO 16 FOR CRC TEST
2087      2271 0357 -16-1
2088
2089      2272 2132 BR CRC16 ONE     /IS THIS CRC BIT OK
2090      2273 2304 DCR CER        /NO, GO REPORT DATA CRC ERROR
2091
2092      2274 0054 CRC ZERO       /YES, BRING UP NEXT CRC BIT
2093
2094      2275 0073 ICT              /INCREMENT AND TEST BIT COUNTER
2095      2276 0124 BR COFL F
2096      2277 2272 .-5
2097
2098      2300 0074 ROTATE ZERO     /CRC WAS GOOD, CLR CRC ERR BIT OF STAT IN SR
2099
2100      2301 0064 LSP             /PUT THE STATUS WORD BACK IN SCRATCHPAD
2101
2102      2302 0212 JUMP F2         /EXIT TO DONE
2103      2303 1006 OKDONE
2104
2105      2304 0076 DCR CER, ROTATE ONE /INSERT 1 INTO CRC ERROR BIT
2106
2107      2305 0064 LSP             /PUT THE STAT WORD BACK
2108
2109      2306 0070 LCT              /ERROR CODE FOR CRC ERROR
2110      2307 0200 KDCR CER
2111      2310 0226 JUMP F5
2112      2311 2610 GOERDM
    
```

```

2113 /{SUBROUTINE: WAIT FOR RUN}
2114 /THIS SUBROUTINE WILL WAIT FOR RUN, IF 46MS ELAPSES, THE HEAD IS UNLOADED
2115 /AND THE ROUTINE CONTINUES WAITING FOR RUN, RETURN ADDRESS IS PASSED
2116 /VIA THE COUNTER
2117
2118
2119 2312 0264 WAITRN, OPEN RTNB /STASH THE RETURN ADDRESS
2120 2313 0075 LSR
2121 2314 0064 LSP
2122
2123 2315 0102 BR RUN T /GOT RUN?
2124 2316 2347 GOTRUN
2125
2126 2317 0240 OPEN TEMPC /PRESET LOOP COUNTER TO 0
2127 2320 0070 LCT
2128 2321 0000 0
2129
2130 2322 0075 BACK, LSR /RESTORE LOOP COUNT
2131 2323 0064 LSP
2132
2133 2324 0302 WBR RUN T /TIME WHILE WAITING FOR RUN
2134 2325 2347 GOTRUN
2135 2326 0302 WBR RUN T
2136 2327 2347 GOTRUN
2137 2328 0302 WBR RUN T
2138 2331 2347 GOTRUN
2139 2332 0302 WBR RUN T
2140 2333 2347 GOTRUN
2141
2142 2334 0071 ESP /INCREMENT AND TEST LOOP COUNT
2143 2335 0073 ICT
2144 2336 0124 BR COFL F
2145 2337 2322 BACK /46MS NOT ELAPSED YET
2146
2147 2340 0250 OPEN TEMPE /TIME IS EXPIRED (45.6 MS), CLEAR THE SOFT HDLD BIT AND UNLOAD THE HEAD
2148 2341 0073 ICT
2149 2342 0075 LSR
2150 2343 0064 LSP
2151 2344 0040 UNHD
2152
2153 2345 0120 BR RUN F /WAIT FOR RUN, FOREVER IF NECESSARY
2154 2346 2345 *-1
2155
2156 2347 0010 GOTRUN, CLR XREQ /IF RUN HAS RESPONSE TO XFREQ
2157
2158 2350 0204 OPEN RTNB /RETURN FROM WAITRN SUBROUTINE
2159 2351 0213 JUMP IND F2
2160
2161

```

```

2162 /{ROUTINE: INITIALIZE CONT.}
2163 /CONTINUATION OF THE INITIALIZE SELF TEST
2164
2165 2352 0070 TEST, LCT /LOAD R5 WITH TEST PATTERN 252
2166 OCTAL
2167 2353 0252 252
2168 DECIMAL
2169 2354 0075 LSR
2170 2355 0224 OPEN R5
2171 2356 0064 LSP
2172
2173 2357 0070 LCT /LOAD R10 WITH TEST PATTERN 125
2174 OCTAL
2175 2360 0125 125
2176 DECIMAL
2177 2361 0075 LSR
2178 2362 0250 OPEN R10
2179 2363 0064 LSP
2180
2181 2364 0062 FLAG ON /SET FLAG AND TEST IT
2182 2365 0170 BR FLAGO T
2183 2366 2371 ,+3
2184 2367 0212 JUMP F2
2185 2370 1374 INTER1 /FLAG FAILURE
2186
2187 2371 0224 OPEN R5 /CONTENTS OF R5 TO SR, SHOULD BE 252
2188 2372 0071 ESP
2189 2373 0275 LSR
2190
2191 2374 0212 JUMP F2 /GO CONTINUE INIT TEST IN FLD 2
2192 2375 1351 TEST1
2193
2194
2195 2376 0000 0 /OPEN
2196 2377 0000 0 /OPEN

```

```

2197      /([SUBROUTINE: MAGNITUDE COMPARISON])
2198      /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
2199      /EXIT IS TO THE RETURN ADDRESS IF F=G. IF F<G, RETURN IS TO RTNA+2.
2200      /IF F>G, RETURN IS TO RTNA+4. CONTENTS OF F AND G ARE UNDEFINED AT
2201      /THE END OF THE SUBROUTINE
2202
2203
2204
2205
2206      2400  0230  MAGCOM, OPEN TEMPA      /FOR BIT COUNT
2207
2208      2401  0070  LCT                      /BIT COUNT IS 8
2209      2402  0367  -8-1
2210
2211      2403  0075  LSR                      /RESTORE BIT COUNT
2212      2404  0064  LSP
2213
2214      2405  0254  OPEN TEMPF           /F TO SR
2215      2406  0071  ESP
2216      2407  0075  LSR
2217
2218      2410  0120  BR SR7 ZERO           /TEST F
2219      2411  2403  TSTG0                /ITS 0
2220
2221      2412  0076  ROTATE ONE           /ITS 1, BRING UP NEXT BIT
2222
2223      2413  0064  LSP                   /RESTORE F
2224
2225      2414  0260  OPEN TEMPG           /G TO SR
2226      2415  0071  ESP
2227      2416  0075  LSR
2228
2229      2417  0120  BR SR7 ZERO           /TEST G
2230      2420  2432  GLESSF                /ITS 0, G IS LESS THAN F
2231
2232      2421  0074  NEXTG, ROTATE ZERO    /ITS 1, BRING UP NEXT G BIT
2233
2234      2422  0064  LSP                   /RESTORE G
2235
2236      2423  0230  OPEN TEMPA           /INCREMENT AND TEST BIT COUNT
2237      2424  0071  ESP
2238      2425  0073  ICT
2239      2426  0124  BR COFL F
2240      2427  2403  MAGCOM+3             /GO COMPARE ANOTHER BIT
2241
2242      2430  0272  OPEN RTNA            /ALL BITS COMPARED, NO DIFFERENCE
2243      2431  0203  JUMP F0 IND
2244
2245      2432  0272  GLESSF, OPEN RTNA    /G IS LESS THAN F RETURN TO RTNA +4
2246      2433  0071  ESP
2247      2434  0073  ICT
2248      2435  0073  ICT
2249      2436  0073  ICT
2250      2437  0073  ICT
2251      2440  0075  LSR

```

```

2252      2441  0064  LSP
2253      2442  0203  JUMP F0 IND
2254
2255      2443  0074  TSTG2, ROTATE ZERO    /F HAS 0, BRING UP NEXT BIT
2256
2257      2444  0064  LSP                   /RESTORE F
2258
2259      2445  0260  OPEN TEMPG           /G TO SR
2260      2446  0071  ESP
2261      2447  0075  LSR
2262
2263      2451  0120  BR SR7 ZERO           /TEST G
2264      2451  2421  NEXTG                 /MATCHES F, GO BRING UP NEXT G BIT
2265
2266      2452  0270  OPEN RTNA            /G IS LESS THAN F, RETURN TO RTNA +2
2267      2453  0071  ESP
2268      2454  0226  JUMP F5
2269      2455  2436  GLESSF+4
2270
2271
2272
2273      /([SUBROUTINE: FIND TRACK CONT,])
2274
2275      2456  0070  HOMERR, LCT           /HOME FOUND BEFORE LAST STEP TAKEN
2276      2457  0050  KHOMERR
2277      2460  0226  JUMP F5
2278      2461  2610  GOERDN
2279
2280
2281      /([SUBROUTINE: DIFFERENCE])
2282      /THIS SUBROUTINE COMPUTES THE DIFFERENCE BETWEEN TWO EIGHT BIT
2283      /NUMBERS. ENTER WITH THE RETURN ADDRESS IN RTN, A IN THE
2284      /COUNTER AND B IN THE SHIFT REGISTER. EXIT IS MADE WITH THE
2285      /COMPLIMENT OF THE DIFFERENCE IN THE SHIFT REGISTER.
2286      /EXIT IS TO RTN IF A>=B. EXIT IS TO RTN+2 IF A<B
2287
2288
2289
2290
2291      2462  0230  DIF, OPEN TEMPA       /OPEN TEMPORARY PATH THRU THE SP
2292
2293      2463  0120  BR COFL T             /HAS A REACHED ALL ONES YET?
2294      2464  2501  DIFB                  /YES, GO GET A FOR THE DIFFERENCE
2295
2296      2465  0064  LSP                   /NO, GET B
2297      2466  0075  LSR                   /A INTO SHIFT REG
2298      2467  0071  ESP                   /B INTO COUNTER
2299
2300      2470  0120  BR COFL T             /HAS B REACHED ALL ONES YET?
2301      2471  2503  DIFA                  /YES, GO GET A FOR THE DIFFERENCE
2302
2303      2472  0073  ICT                   /INCREMENT B
2304      2473  0064  LSP                   /, BRING BACK A
2305      2474  0075  LSR                   /B INTO SHIFT REG
2306      2475  0071  ESP                   /A INTO COUNTER

```

```

2307 2476 0073 ICT /INCREMENT A
2308 2477 0220 JUMP F5 /GO BACK TO TEST A AGAIN
2309 2502 2463 DIF+1
2310
2311
2312 2501 0270 DIFB, OPEN RTNA /B IS THE COMPLIMENT OF THE DIFFERENCE
2313 2502 0203 JUMP F0 IND /EXIT A=B
2314
2315
2316 2503 2270 DIFA, OPEN RTNA /A IS THE COMPLIMENT OF THE DIFFERENCE
2317 2504 0071 ESP /INCREMENT THE RETURN ADDRESS BY 2
2318 2505 0073 ICT
2319 2506 0073 ICT
2320
2321 2507 0064 LSP /RESTORE RETURN ADDRESS TO SCRATCHPAD AND A TO BR
2322 2510 0075 LSR
2323 2511 0071 ESP
2324 2512 0064 LSP
2325 2513 0075 LSR
2326
2327 2514 0203 JUMP F0 IND /EXIT A<B
2328
2329
2330 /{ROUTINE: FIND HEADER CONT,}
2331 /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
2332
2333 /AND SECTOR COMPARISONS,
2334
2335
2336
2337
2338 2515 0070 CKMCR, LCT /PRESET BIT COUNT TO 16 FOR CRC
2339 2516 0357 -16-1
2340
2341 2517 0132 BR CRC16 ONE /IS CRC ZERO
2342 2520 2506 HRCER /NO, LOG ERROR AND TRY AGAIN
2343
2344 2521 0073 ICT /YES, CRC GOOD SO FAR, BUMP BIT CNTR
2345
2346 2522 0054 CRC ZERO /BRING UP NEXT CRC BIT
2347
2348 2523 0124 BR COFL F /ALL BITS TESTED?
2349 2524 2517 -5 /NO, BRANCH BACK
2350
2351 2525 0210 OPEN ERREG /YES, CRC HAS GOOD, CHECK TRK COMP
2352 2526 0071 ESP
2353 2527 0075 LSR
2354
2355 2530 0070 LCT /ROTATE BIT 0 TO BIT 7
2356 2531 0370 -7-1
2357 2532 0074 ROTATE ZERO
2358 2533 0073 ICT
2359 2534 0124 BR COFL F /DONE ROTATING?
2360 2535 2532 -3 /NO
2361

```

```

2362 2536 0122 BR SR7 ONE /YES, WAS THERE A BAD COMPARE
2363 2537 2542 TKSKER /YES, GO REPORT A TRACK SEEK ERROR
2364
2365 2542 0264 OPEN RTNA /CORRECT TRACK, EXIT FROM FIND HDR SUBR
2366 2541 0207 JUMP F1 IND
2367
2368
2369
2370
2371 2542 0070 TKSKER, LCT /HEADER CRC WAS GOOD BUT TRACK
2372 2543 0150 KTKSKER /ADDRESS DID NOT COMPARE, MUST
2373 2544 0226 JUMP F5 /EXIT TO ERROR DONE
2374 2545 2010 GOERDN
2375
2376
2377 2546 0070 HRCER, LCT /HEADER CRC WAS NOT CORRECT
2378 2547 0140 KHRCER
2379 2550 0075 LSR
2380 2551 0210 OPEN ERREG /LOG THE ERROR
2381 2552 0064 LSP
2382
2383 2553 0226 JUMP F5 /GO TRY ANOTHER HEADER
2384 2554 2557 BADHDR
2385
2386
2387
2388
2389 2555 0170 BDSRT, BR FLAGO T /BAD START ON DATA AM OR IDAM?
2390 2556 2577 BADDAM
2391
2392 2557 0230 BADHDR, OPEN TEMPB /IDAM, INCREMENT AND TEST BAD START INNER COUNT
2393 2560 0071 ESP
2394 2561 0073 ICT
2395 2562 0275 LSR
2396 2563 0064 LSP
2397 2564 0124 BR COFL F
2398 2565 2015 PTRYAG /NO OVERFLOW, GO TRY ANOTHER HEADER
2399 2566 0234 OPEN TEMPB /INCREMENT AND TEST BAD START OUTER COUNT
2400 2567 0071 ESP
2401 2570 0073 ICT
2402 2571 0124 BR COFL F
2403 2572 2015 PTRYAG /NO OVERFLOW, GO TRY AGAIN
2404 2573 0070 XSTRYS, LCT /TOO MANY TRIES FOR A HEADER
2405 2574 0160 KXSTRYS
2406 2575 0226 JUMP F5
2407 2576 2010 GOERDN
2408
2409
2410 2577 0234 BADDAM, OPEN TEMPB /BAD START ON DATA AM, INCREMENT AND TEST BAD START COUNT
2411 2600 0071 ESP
2412 2601 0073 ICT
2413 2602 0075 LSR
2414 2603 0064 LSP
2415 2604 0124 BR COFL F
2416 2605 2017 PGETDA /NO OVERFLOW GO TRY FOR DATA AM AGAIN

```

```

2417 2606 0070 NODAM, LCT /TRIED 3 TIMES FOR DATA AM, GO FLAG THE ERROR
2418 2607 0170 KNODAM
2419 2610 0210 GOERDN, OPEN ERREG
2420 2611 0075 LSR
2421 2612 0064 LSP
2422 2613 0212 JUMP F2
2423 2614 1000 ERDONS
2424
2425 2615 0216 PTRVAG, JUMP F3 /POINTER TO FIND AN IDAM
2426 2616 1413 TRYAGN
2427
2428
2429 2617 0216 PGETDA, JUMP F3 /POINTER TO FIND DATA AM
2430 2620 1441 GETDAM
2431
2432
2433
2434 /([ROUTINE: INITIALIZE CONT.])
2435 2621 0070 WRONG, LCT /HOME WAS FOUND WHILE STEPPING OUT
2436 2622 0030 KARONG
2437 2623 0226 JUMP F5
2438 2624 2610 GOERDN
2439
2440 2625 0070 DNRCAL, LCT /CALL CHECK READY SUBROUTINE
2441 2626 1771 PNORDY
2442 2627 0226 JUMP F5
2443 2630 2640 CHKRDY
2444
2445 2631 0070 INTRDY, LCT /DRV 0 IS READY CALL BOOT SUBROUTINE TO
2446 2632 0770 GCREAD /MOVE TO TRACK 1, THEN GO TO READ ROUTINE TO
2447 2633 0274 OPEN RTN /PICK UP SECTOR 1
2448 2634 0075 LSR
2449 2635 0064 LSP
2450 2636 0202 JUMP F0
2451 2637 0252 BOOT
2452
2453
2454
2455

```

```

2456 /([SUBROUTINE: CHECKREADY])
2457
2458 /SUBROUTINE TO CHECK THE SELECTED DRIVE TO SEE IF THE
2459 /DISK IS INSERTED AND UP TO SPEED. THIS IS DONE BY CHECKING TO SEE IF
2460 /THE INTERVAL BETWEEN 2 INDEX PULSES IS BETWEEN 150 NS AND 180 NS. RETURN
2461 /ADDRESS IS PLACED IN THE COUNTER BEFORE ENTRY, NOT READY RETURN IS
2462 /TO THE RETURN ADDRESS. READY RETURN IS TO THE RETURN ADDRESS PLUS 2
2463
2464
2465
2466 /
2467 2642 0274 CHKRDY, OPEN RTN /SAVE RETURN ADDRESS
2468 2641 0075 LSR
2469 2642 0064 LSP
2470
2471 2643 0070 LCT /2 TO CNTR FOR INDEX PASS COUNT
2472 2644 0375 -2-1
2473
2474 2645 0230 JPEM TEMPA /FOR INDEX PASS COUNT
2475
2476 2646 0075 NEAPAS, LSR /RESTORE INDEX PASS COUNT
2477 2647 0064 LSP
2478
2479 2650 0061 FLAG OFF /CLOSE INDEX WINDOW
2480
2481 2651 0042 LCMU /TO CLEAR INDEX FLOP
2482
2483 2652 0070 LCT /FOR 15 TIMES THROUGH 10MS LOOP
2484 2653 0360 -15-1
2485
2486 2654 0234 STOLY, OPEN TEMPB /RESTORE OUTER COUNT
2487 2655 0075 LSR
2488 2656 0064 LSP
2489
2490 2657 0070 LCT /FOR 40 TIMES THROUGH .25MS LOOP
2491 2660 0327 -40-1
2492
2493 2661 0243 SPBACK, OPEN TEMPC /RESTORE INNER COUNT
2494 2662 0075 LSR
2495 2663 0064 LSP
2496
2497 2664 0070 LCT /WAIT .25 MS FOR INDEX
2498 2665 0005 -250-1
2499 2666 0116 BR INDX T
2500 2667 2714 SAKIND /FOUND INDEX
2501 2670 0073 ICT
2502 2671 0124 RR COFL F
2503 2672 2666 .-4
2504
2505 2673 0240 OPEM TEMPC /INCREMENT AND TEST INNER COUNT
2506 2674 0071 ESP
2507 2675 0073 ICT
2508 2676 0124 RR COFL F
2509 2677 2662 SPBACK
2510

```



```

2511 2700 0234 OPEN TEMPB /INCREMENT AND TEST OUTER COUNT
2512 2701 0271 ESP
2513 2702 0273 ICT
2514 2703 0124 BR COFL F
2515 2704 0255 STDLY+1
2516
2517 2705 0176 BR FLAGO ONE /WAS INDEX WINDOW OPEN?
2518 2706 0267 UNRDY /YES, NO INDEX WITHIN 160MS
2519
2520 2707 0262 FLAG ON /NO, OPEN WINDOW
2521
2522 2710 0270 LCT /FOR 3 TIMES THROUGH 16 MS LOOP
2523 2711 0374 -3-1 /THE WINDOW IS 36 MS WIDE
2524
2525 2712 0226 JUMP F5 /GO LOOK FOR INDEX
2526 2713 0254 STDLY
2527
2528
2529 2714 0232 SAWIND, OPEN TEMPB /INCREMENT AND TEST INDEX PASS COUNT
2530 2715 0271 ESP
2531 2716 0273 ICT
2532 2717 0124 BR COFL F
2533 2720 0246 NEWPAS /THIS WAS 1ST INDEX, GO LOOK FOR SECOND
2534
2535 2721 0174 BR FLAGO ZERO /THIS WAS 2ND INDEX, WAS THE WINDOW OPEN?
2536 2722 0267 UNRDY /NO, INDEX OCCURRED TOO SOON
2537
2538 2723 0274 OPEN RTN /YES, INDEX OCCURRED BETWEEN 150 AND 160 MS, INCREMENT
2539 2724 0271 ESP /RETURN ADDRESS BY 2
2540 2725 0273 ICT
2541 2726 0273 ICT
2542 2727 0275 LSR
2543 2730 0264 LSP
2544
2545 2731 0214 OPEN STAT /SET DRV RDY BIT OF STAT IN SR
2546 2732 0271 ESP
2547 2733 0275 LSR
2548
2549 2734 0276 ROTATE ONE
2550
2551 2735 0261 FLAG OFF /FLAG OFF TO INDICATE FIRST PASS
2552
2553 2736 0276 ROT3, LCT /END AROUND SHIFT OF THE NEXT 3 BITS OF STAT IN SR
2554 2737 0374 -3-1
2555 2740 0122 BR SR7 T
2556 2741 0245 .+4
2557 2742 0274 ROTATE ZERO
2558 2743 0226 JUMP F5
2559 2744 0246 .+2
2560 2745 0276 ROTATE ONE
2561 2746 0273 ICT
2562 2747 0124 BR COFL F
2563 2750 0240 .-8
2564
2565 2751 0176 BR FLAGO T /WAS IT FIRST 3 OR LAST 3

```

```

2566 2752 0264 EXCHRY /LAST, GO EXIT
2567
2568 2753 0140 BR WRTEN F /UPDATE WRITE PROTECT BIT OF STAT IN SR
2569 2754 0262 .+4
2570 2755 0274 ROTATE ZERO
2571 2756 0226 JUMP F5
2572 2757 0261 .+2
2573 2760 0276 ROTATE ONE
2574
2575 2761 0262 FLAG ON /GO SHIFT AROUND LAST 3 BITS
2576 2762 0226 JUMP F5
2577 2763 0236 ROT3
2578
2579 2764 0264 EXCHRY, LSP /RESTORE THE STAT
2580
2581 2765 0274 OPEN RTN /RETURN FROM CHKRDY SUBROUTINE
2582 2766 0217 JUMP F3 IND
2583
2584 2767 0214 UNRDY, OPEN STAT /CLEAR DRV READY BIT OF STAT IN SR
2585 2770 0271 ESP
2586 2771 0275 LSR
2587 2772 0274 ROTATE ZERO
2588
2589 2773 0226 JUMP F5 /GO UPDATE REST OF STAT IN SR
2590 2774 0235 ROT3-1
2591
2592 2775 0200 0 /OPEN
2593 2776 0200 0 /OPEN
2594 2777 0200 0 /OPEN
2595
2596
2597

```

0000	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0100	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1000	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1100	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2000	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2100	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111

3000
3100

3200
3300

3400
3500

3600
3700

4000
4100

4200
4300

4400
4500

4600
4700

5000
5100

5200
5300

5400
5500

5600
5700

6000
6100

6200
6300

6400
6500

6600
6700

7000
7100

7200
7300

7400
7500

7600
7700

/RX01 FLOPPY CONTROLLER FIRMWARE		PAL10	V142A	9-FEB-76	9117	PAGE 16-5	
A	0562	ERTRK	0242	PFUNCT	0370	WHCHDR	0075
ABACK	0535	EXCHRY	2764	PGETDA	2617	WRONG	2621
ABV43	0344	FILL1	1175	PGOTIT	1346	WRT00	1322
AGAIN	0531	FILLBU	1110	PNORDY	1771	WRTCRC	0620
AGAIN1	0550	FINDMD	1400	PNTROY	1765	WRTDAM	0514
AGAIN2	0722	FINDSE	0714	PROSEC	1105	WRTDAT	0566
AGAIN3	1576	FINDTR	0103	PRTERR	0503	WRTPBT	0656
AGAIN4	1616	FUNCT	1036	PTRYAG	2615	WRTSEC	0400
AGAIN5	1635	FUNCT2	1057	PUTSEC	0145	XFRQ	1131
AGAIN6	1653	FUNCT4	1066	PUTTRY	0166	XSTRYS	2573
B	0564	FUNCT6	1076	PYSRDY	1767		
BACK	2322	GETCMD	2001	RCALOK	0060		
BADAM	2577	GETCRC	2221	ROEREG	1275		
BADHDR	2557	GETDAM	1441	RDSEC	0760		
BADSRT	1673	GETWRD	2000	ROSTAT	1224		
BBACK	0554	GLESSF	2432	READ	2167		
BDSHT	2555	GDDONE	0712	READOK	0706		
BOOT	0252	GODUN	1272	RECALP	0035		
BYTEOU	1152	GOERON	2610	RECAL1	0034		
C	0615	GOREAD	0770	RFINTR	0355		
CBACK	0576	GOTIT	2010	ROT	1251		
CEGATE	0676	GOTONE	2030	ROT3	2736		
CFINSE	0351	GOTRUN	2347	SAWIND	2714		
CHKPAR	2041	GOTWRD	2076	SECHLF	0543		
CHKRDY	2640	HRCRER	2546	SECPLS	2124		
CHKSEC	0730	HORCOM	1571	SELFER	0620		
CHKCRC	2515	HDSEYL	0322	SPBACK	2662		
CHKCME	2105	HLFDLY	0466	STASH	0437		
CLR10	1243	HOMERR	2456	STOLY	2654		
CGATE	0666	ILTRK	0206	STDONE	1031		
D	0653	IN10	0045	STEPM	2100		
DAM	1675	INTER1	1374	STPOUT	0275		
DAMSUP	0460	INTHDY	2631	SWGATF	0407		
DATA	2206	LOOP	1326	TEST	2352		
DATAA	0571	MAGCOM	2400	TEST1	1351		
DBACK	0646	MOREDS	1421	TEST2	1350		
DCRCEP	2304	NEWCRD	1141	TESTON	1372		
DELAY	1300	NEWPAS	2646	TIMERR	1667		
DELCA1	1727	NEXTG	2421	TKSKEP	2502		
DIF	2462	NOAM	2606	TRKEO	0246		
DIFA	2503	NCSTPS	0357	TRYAG	1413		
DIFB	2521	ACTYET	1755	TSTAG	1353		
DLY25	2145	NCZERO	1746	TSTG0	2443		
DARLAL	2025	NOTHER	2034	TSTRT	0004		
DONLTY	2165	NORVE	0060	UDIF	0130		
DONSTP	2135	NORV1	0270	UNRDY	2767		
DONSTP	0305	NXHDR	0737	UONE	0120		
E	0627	NAIDAM	1761	USAME	0141		
EMPTY1	1210	NAPRAM	1751	UZERO	0127		
EMPTY6	1107	ONDCNE	1006	WAIT	0743		
ENDDAM	1702	OUT	2150	WAITRY	2312		
ERDNE	1070	PDURCL	0372	WATDAT	2021		

/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-76 9117 PAGE 16-6

ERRORS DETECTED: 0
LINKS GENERATED: 0
RUN-TIME: 18 SECONDS
3K CORE USED

THE DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF THE UNITED STATES GOVERNMENT AND ARE TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT PERMISSION IN WRITING FROM THE UNITED STATES GOVERNMENT. COPYRIGHT © 1974, WESTAL ELECTRONIC CORPORATION

PARTS LIST

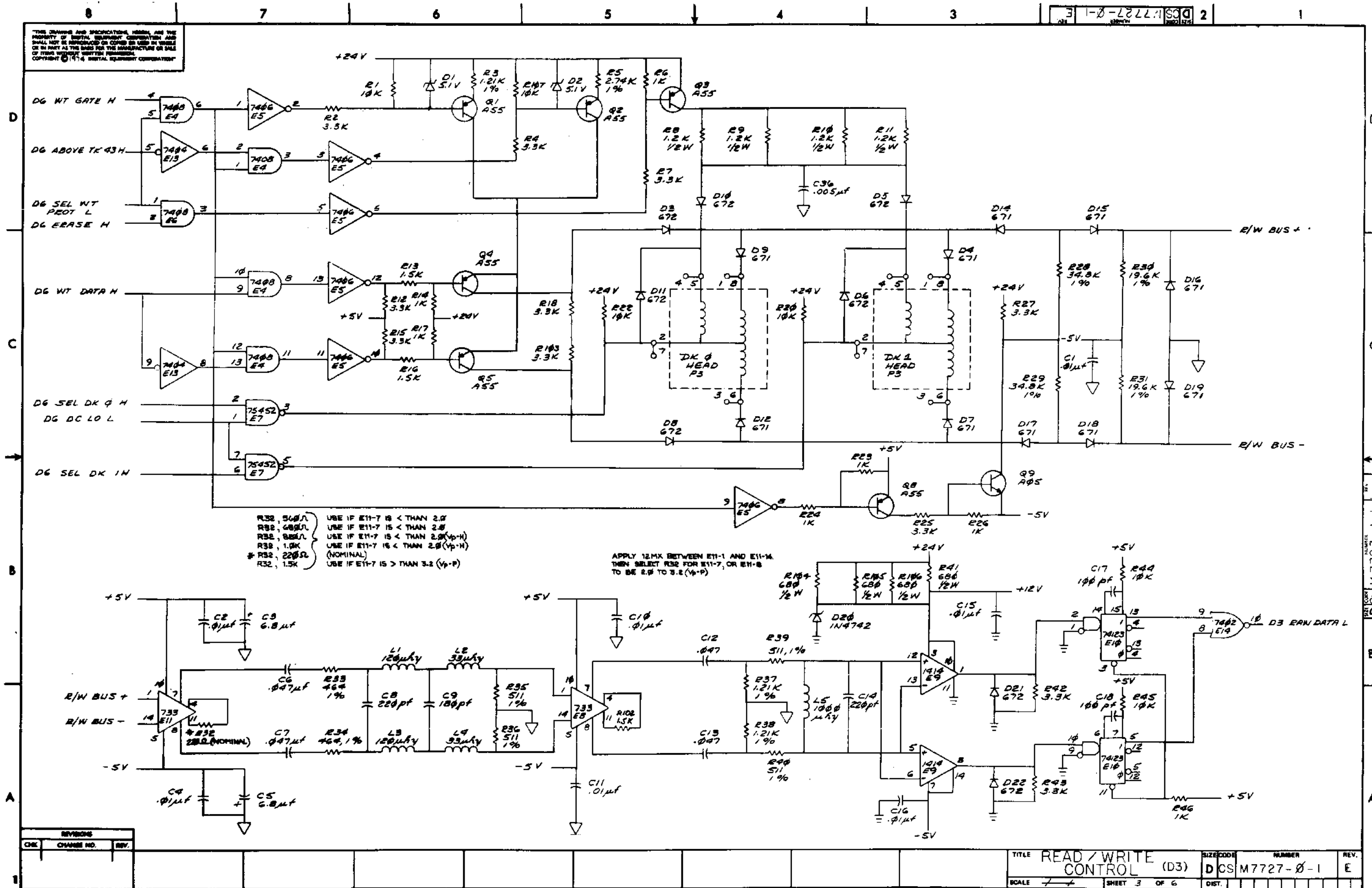
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	TRM
		X-Y COORDINATE HOLE LOCATION	K-00-M7727-0-4	1
		ASSY/ BULL HOLE LAYOUT	D-M-M7727-0-5	2
		MODULE ECO HISTORY	B-M-M7727-0-6	3
1		ETCHED CIRCUIT BOARD	D-1A-501370-00	4
2	C17, C18	CAP 100 pf	1000016-00	5
1	C9	CAP 180 pf	1000020-00	6
2	C8, C14	CAP 220 pf	1000021-00	7
32	C1, C2, C4, C10, C11, C15 C16, C20, C21, C23, C24 C26, C27, C29, C30, C37, C38, C39, C40, C43 C44, C45, C46, C47 C49 - C59	CAP .01 μF	1001610-00	8
2	C3, C5	CAP 6.8 μF 35V	1005306-00	9
2	C34, C35	CAP 190 μF	1009433-00	10
1	C33	CAP 50 μF	1000080-00	11
4	C7, C6, C12, C13	CAP .047 μF	1010978-32	12
5	C19, C25, C22, C23, C36	CAP 005 μF	1001765-00	13
10	D4, D7, D9, D12, D14 D15, D6, D17, D18, D19	DIODE D671	1103309-00	14
8	D3, D5, D8, D8, D10 D11, D21, D22	DIODE D672	1105275-00	15
10	D23, D24, D26, D27 D28, D29, D30, D31 D32, D33	DIODE IN4004	1105796-00	16
1	D20	DIODE IN4742 12V	1109502-00	17
2	D1, D2	DIODE 5.1V	110713-00	18
9	R90, R92 - R99	RES 150 1/4W 5%	1300250-00	19
4	R41, R104, R105, R106	RES 680 1/2W 5%	1300347-00	20
12	R6, R14, R17, R23, R24, R26, R46 R78, R79, R80, R81 R91,	RES 1K 1/4W 5%	1300365-00	21
4	R8 - R11	RES 1.2K 1/2W 5%	1300385-00	22
6	R50, R57, R64, R71, R40R111	RES 68 1/2W 5%	1309405-00	23
7	R3, R16, R53, R62 R68, R75, R102	RES 1.5K 1/4W 5%	1300391-00	24
4	R35, R36, R39, R40	RES 511 1/8W 1%	1302411-00	25
1	R5	RES 2.74K 1/8W 1%	1304868-00	26
11	R2, R4, R7, R12, R15 R18, R43, R25, R27 R42, R43	RES 3.3K 1/4W 5%	1300439-00	27
1	R1, R20, R22, R44 R45, R187	RES 10K 1/4W 5%	1300479-00	28
11	R3, R37, R38, R52 R58, R63, R66, R72 R76, R109, R112	RES 1.21K 1/8W 1%	1302871-00	29
1	R32	RES 220.25K 1/8W	1300271-00	30 *
2	R33, R34	RES 404 1/8W 1%	1303047-00	31
2	R28, R29	RES 34.8K 1/8W 1%	1303156-00	32
4	R51, R61, R65, R73	RES 10K 1/8W 1%	1303312-00	33
2	R42, R83	RES 100 5W 5%	1309094-00	34
2	R30, R31	RES 19.6K 1/8W 1%	1309419-00	35
6	R55, R59, R67, R74 R118, R113	RES 4.69K 1/4W 1%	1304856-00	36

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	TRM
1	L5	CHOKE 1000 MHY	1602729-00	37
2	L2, L4	CHOKE 39 MHY	1601759-00	38
2	L1, L3	CHOKE 120 MHY	1610663-00	39
1	E17	I.C. 7450	1905580-00	40
2	E16, E18	I.C. 7473	1905587-00	41
1	E14	I.C. 7402	1909004-00	42
1	E13	I.C. 7404	1909686-00	43
2	E4, E6	I.C. 7403	1910155-00	44
3	E1, E9, E21	I.C. 1414	1910337-00	45
5	E2, E3, E12, E19, E20	I.C. 75451	1910406-00	46
1	E10	I.C. 74123	1910436-00	47
2	E8, E11	I.C. 72733	1910644-00	48
1	E15	I.C. 74157	1910655-00	49
1	E5	I.C. 7406	1910741-00	50
1	J1	I.C. SOCKET 16 PIN	1211813-02	51
9	Q9 THRU Q15, Q25, Q26	TRANS MXA805	1510705-00	52
6	Q1 - Q5, Q8	TRANS MXA855	1510706-00	53
8	Q17 - Q24	TRANS D44CB	1510421-00	54
86	2" HOLES	WIRE WRAP PIN	1210385-81	55
3	J2	CONN 2 POS	1212204-00	56
8	"X" HOLES	SCREW, PAN HD 4/40 X 5/16	9006010-01	57
8	"X" HOLES	NUT, KEP 4/40 X 1/4 X 3/32	9006557-00	58
1	E7	I.C. 75452	1910645-00	59
4	R54, R56, R69, R70	RES 18.7K 1/4W 1%	1302941-00	60

REVISIONS		
CHK	CHANGE NO.	REV

THIS DRAWING AND SPECIFICATIONS HEREBY ARE THE PROPERTY OF BENTON, BURNETT, BOWEN AND COMPANY, INC. AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1974 BENTON, BURNETT, BOWEN AND COMPANY, INC.

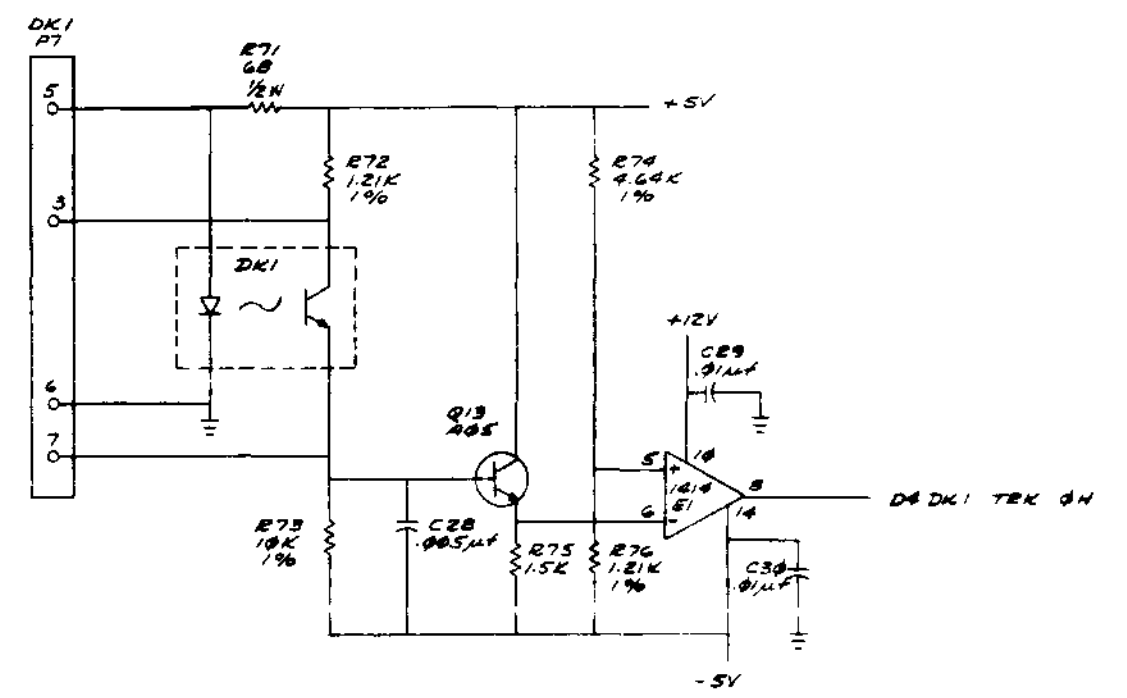
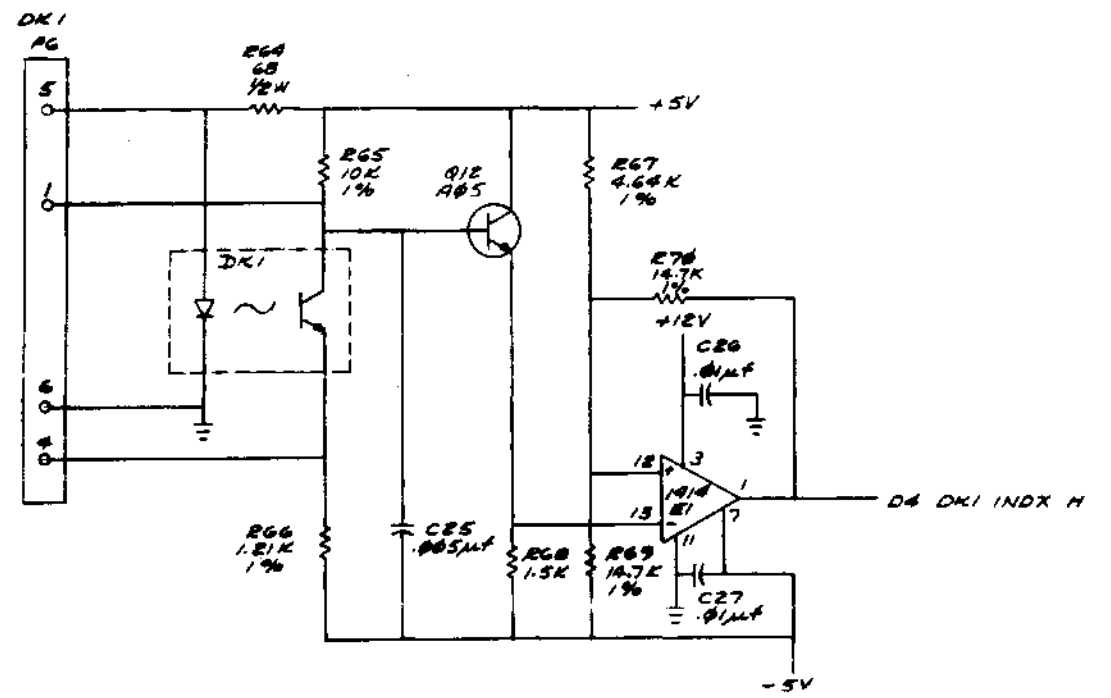
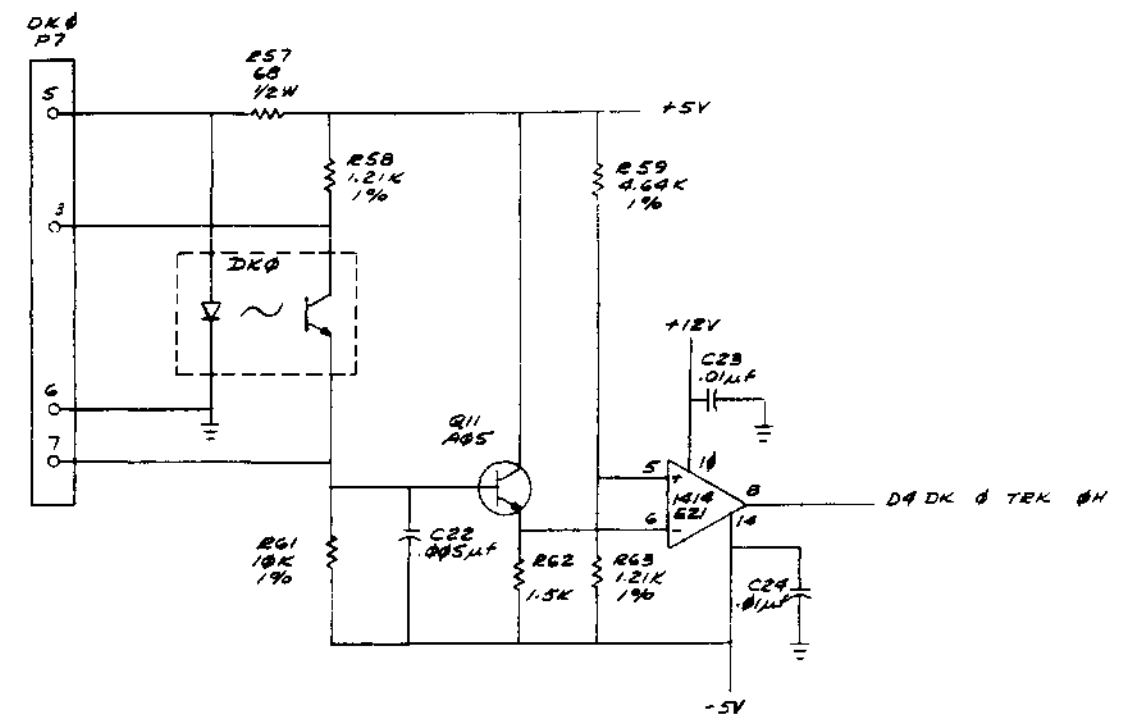
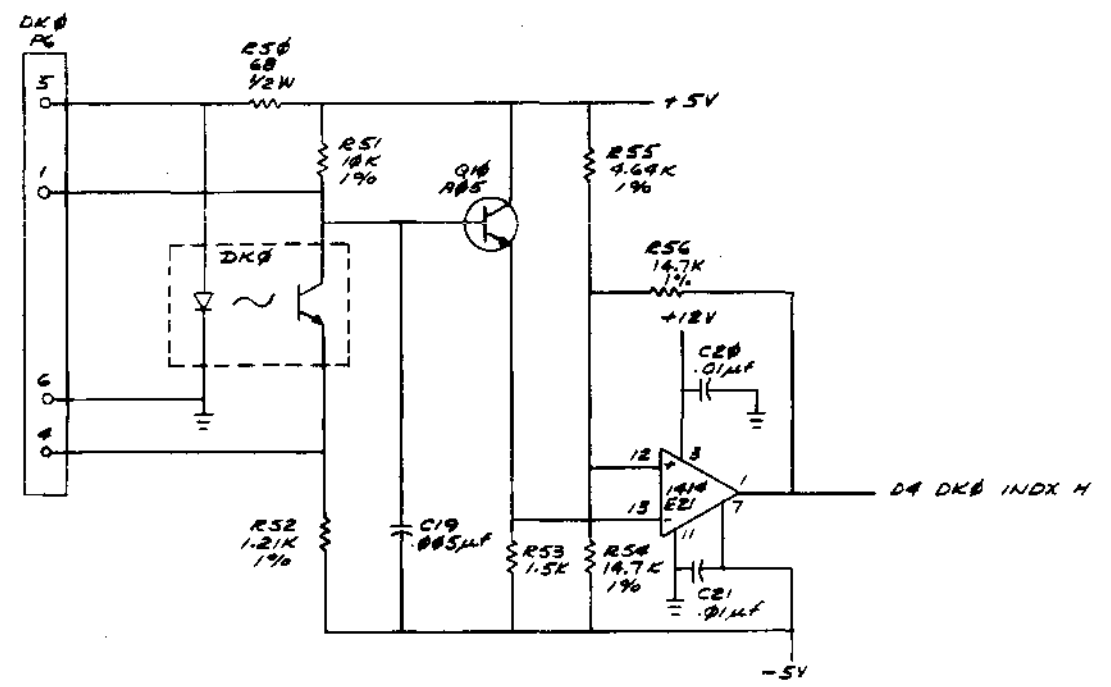


R32, 500Ω USE IF E11-7 IS < THAN 2.0
 R32, 680Ω USE IF E11-7 IS < THAN 2.8
 R32, 820Ω USE IF E11-7 IS < THAN 2.8(Vp-P)
 R32, 1.0K USE IF E11-7 IS < THAN 2.0(Vp-P)
 *R32, 220Ω (NOMINAL)
 R32, 1.5K USE IF E11-7 IS > THAN 3.2 (Vp-P)

APPLY 12MΩ BETWEEN E11-1 AND E11-4.
 THEN SELECT R32 FOR E11-7, OR E11-8
 TO BE 2.0 TO 3.2 (Vp-P)

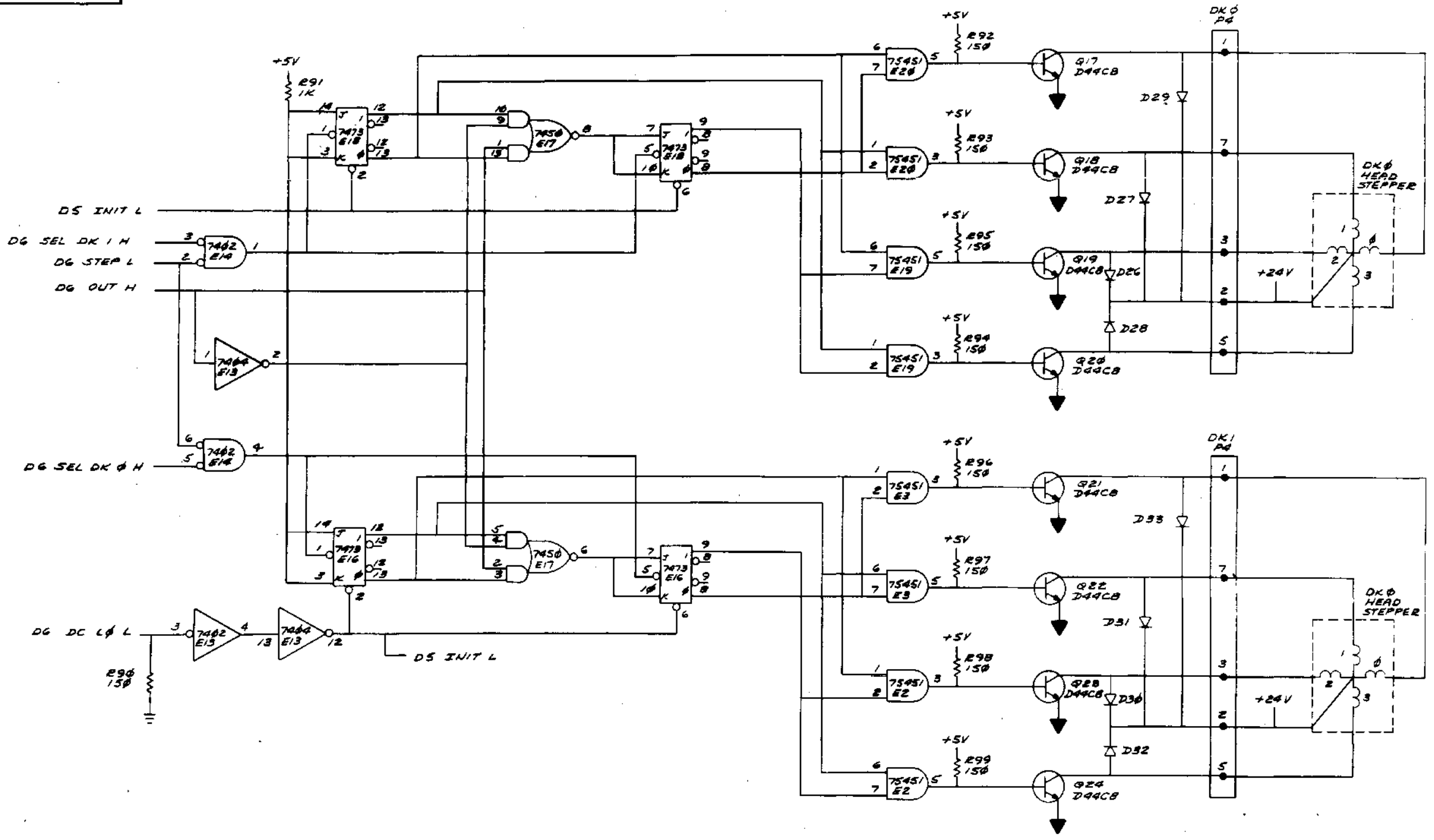
REVISIONS		
CHEK	CHANGE NO.	REV.

THE DESIGN AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF AERIAL ELECTRONIC CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED IN WHOLE OR IN PART AS THE BASIS FOR THE REPRODUCTION OR SALE OF ITEMS OR PARTS THEREOF WITHOUT PERMISSION. COPYRIGHT © 1974 AERIAL ELECTRONIC CORPORATION



REVISIONS		
CHK	CHANGE NO.	REV.

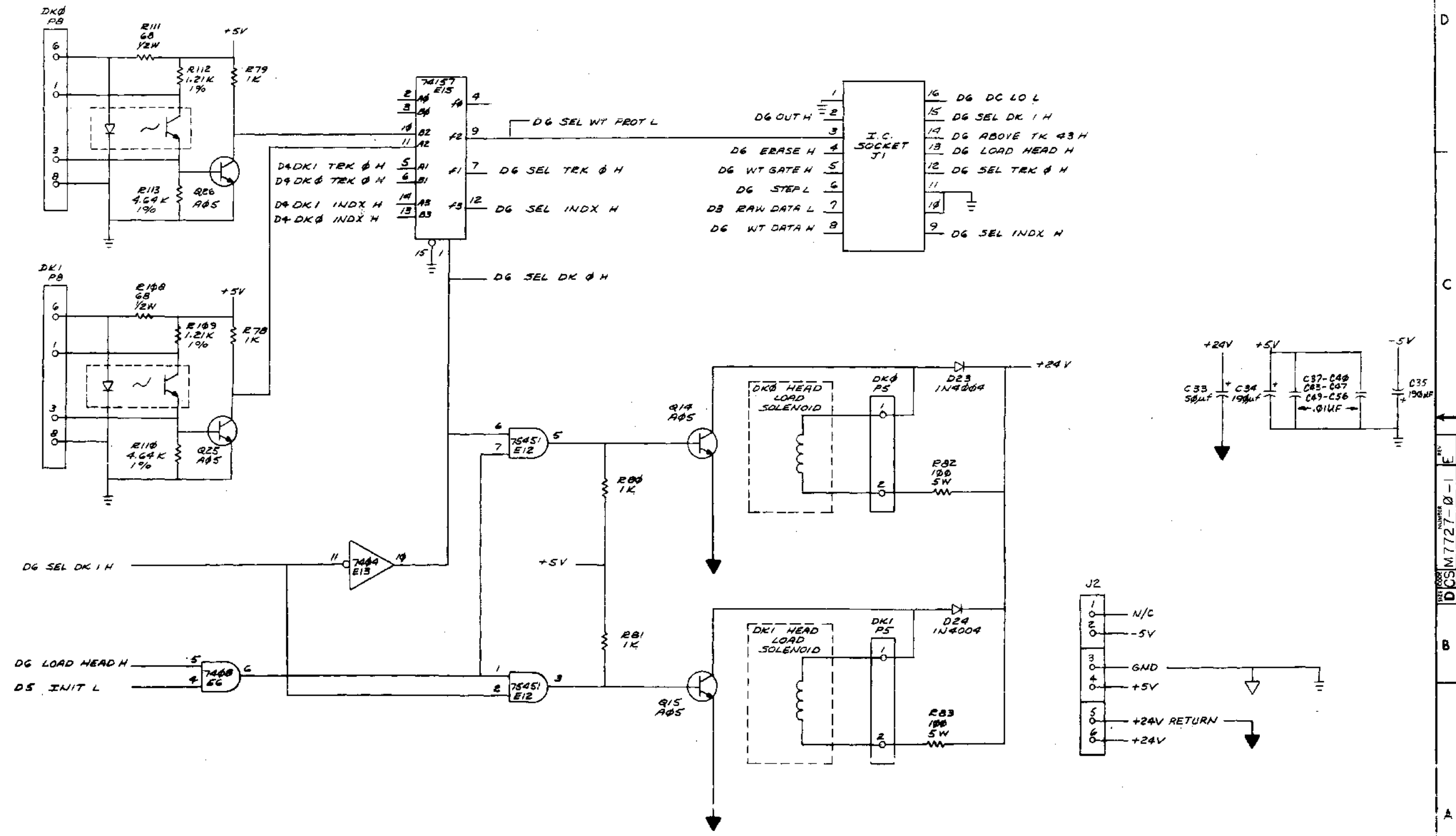
THIS DRAWING AND SPECIFICATIONS HEREBY ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF PRODUCTS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1970 DIGITAL EQUIPMENT CORPORATION



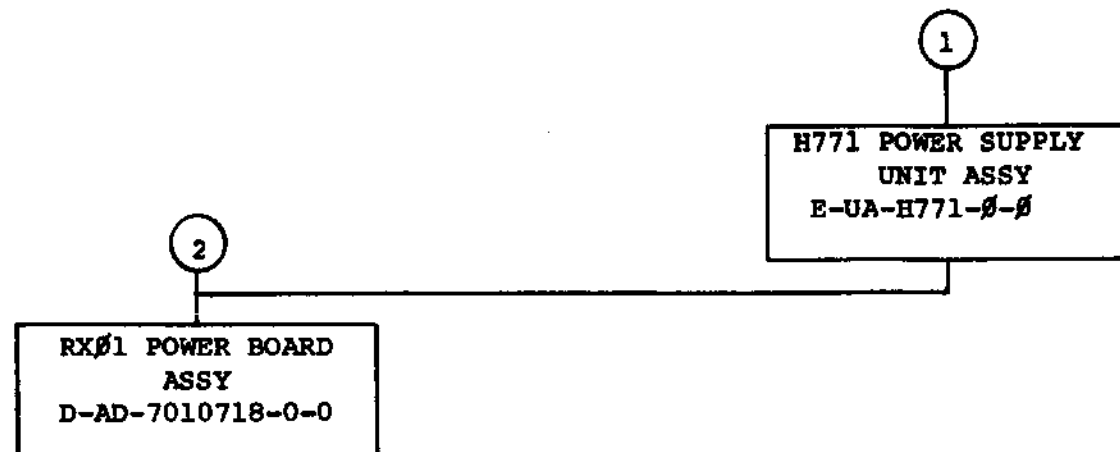
DCS M7727-0-1 E

REVISIONS		
CHK	CHANGE NO.	REV.

THIS DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1974 DIGITAL EQUIPMENT CORPORATION



REV.	CHANGE NO.	DATE



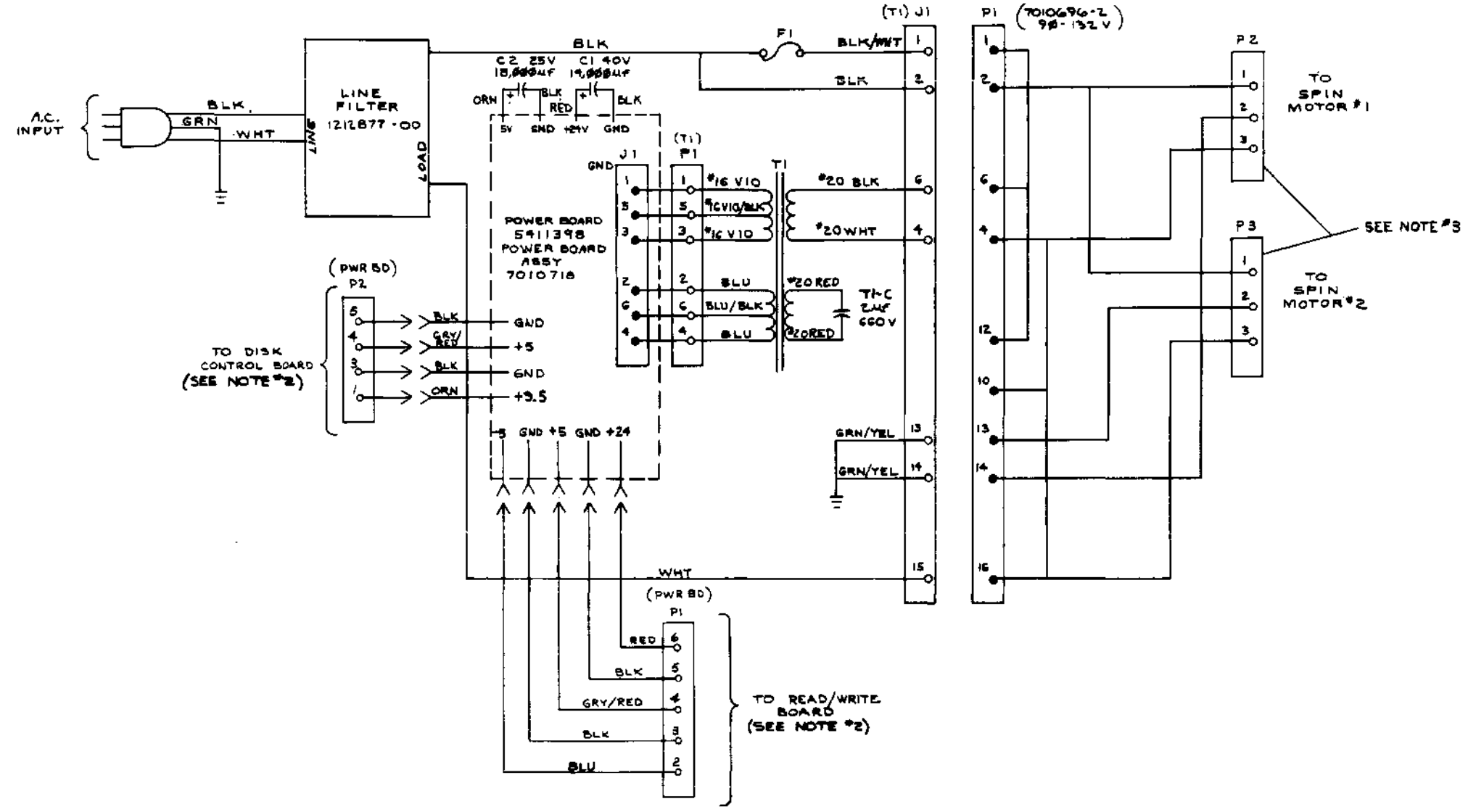
TITLE	SHEET 2 OF 3	SIZE CODE	NUMBER	REV
H771 POWER SUPPLY	B DD	H771-β	E	

MECHANICAL					ELECTRICAL								
CUSTOMER PRINT SET	MFG. SET	FIND NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	CUSTOMER PRINT SET	MFG. SET	FIND NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
		1	E	2	H771 POWER SUPPLY ASSY		X		1	B-DD-H771-β	E	3	H771 POWER SUPPLY
			D	1	CHASSIS, POWER SUPPLY		X			D-CS-H771-A-1	B	1	H771-A CIRCUIT SCHEMATIC
			C	1	TRANSFORMER ASSY, 60 HZ		X			D-CS-H771-C-1	C	1	H771-C CIRCUIT SCHEMATIC
			E	1	TRANSFORMER ASSY, 50 HZ		X			D-CS-H771-D-1	C	1	H771-D CIRCUIT SCHEMATIC
			B	1	POWER CORD ASSY					A-SP-H771-β-1			ENGINEERING SPECIFICATION
			C	1	JUMPER								
				1	BRACKET, FUSE MOUNTING								
				1	DECAL, H771-A								
			A	1	DECAL, H771-C								
			A	1	DECAL, H771-D								
		2		1	RX01 POWER BOARD ASSY								
			C	1	READ/WRITE BOARD HARNESS		X		2	D-AD-7010718-0-0	*	1	RX01 POWER BOARD ASSY
			B	1	DISK CONTROL BOARD HARNESS		X			D-C6-5411398-0-1	*	1	RX01 POWER BOARD ASSY

CUSTOMER PRINT SET CODES	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED	TITLE	SIZE CODE	NUMBER	REV
		H771 POWER SUPPLY	B .00	H771-β	E

THIS DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1975, DIGITAL EQUIPMENT CORPORATION.

- NOTES:
1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
 2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
 3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).

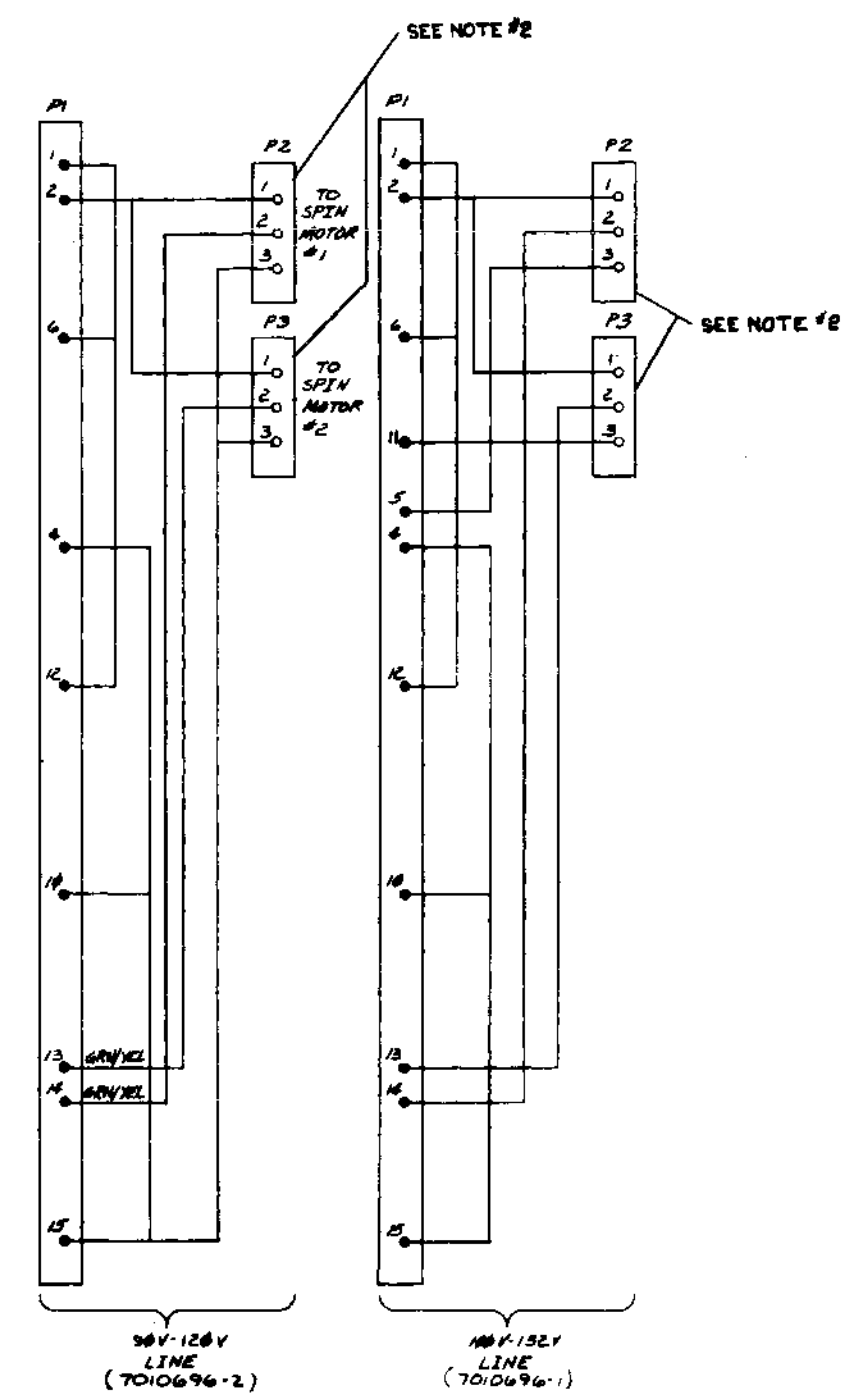
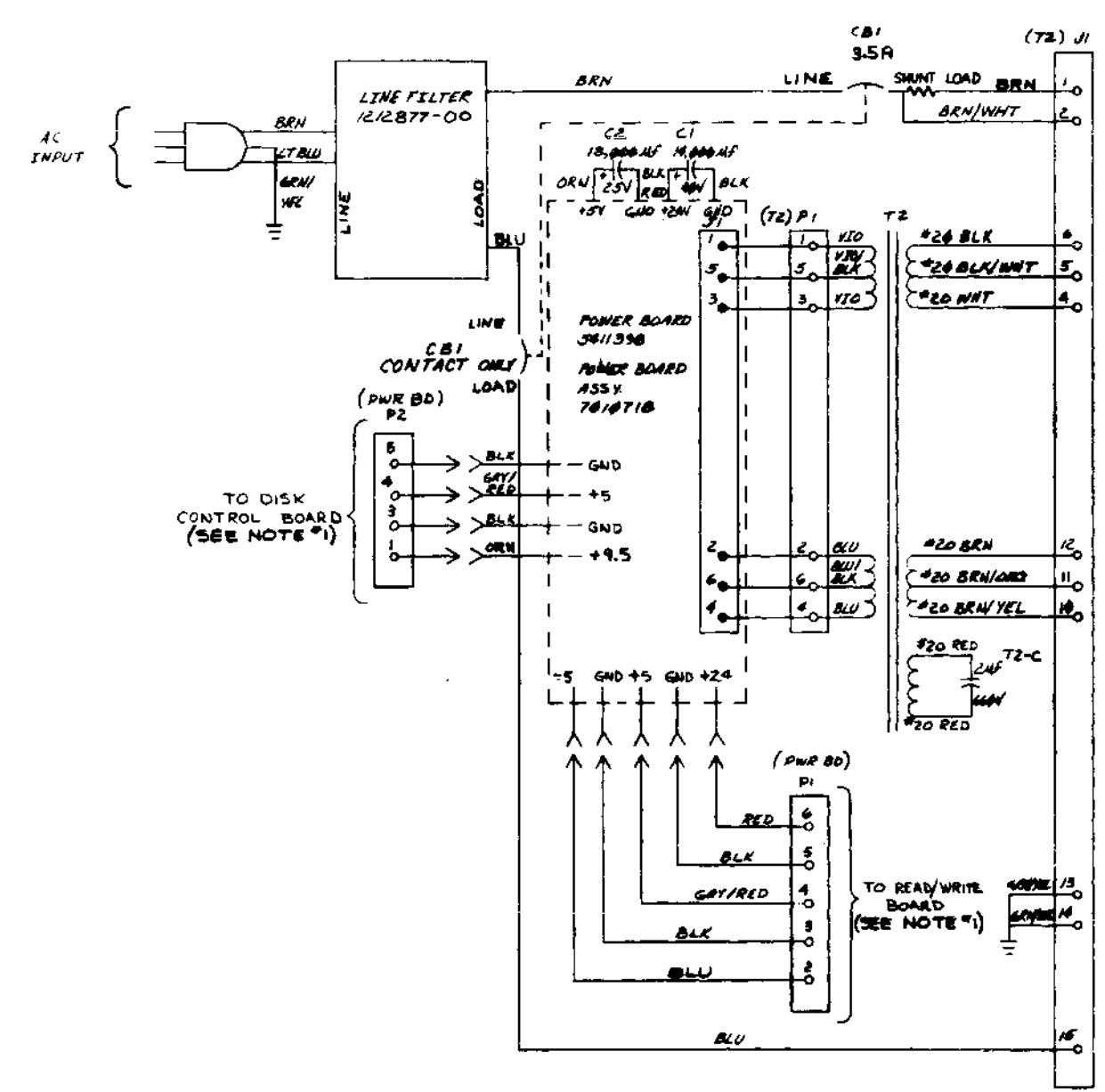


REV.	A
CHANGE NO.	H771-00001
BY	B. HAZEN
DATE	11/20/75
REV.	B
CHANGE NO.	H771-00004
BY	B. HAZEN
DATE	12/30/75

DRN	D.E. O'Leary	1/22/76	FIRST USED ON	RX01
CHK'D	W.P.M.	2/10/76	TITLE	H771A POWER CONNECTIONS
ENG.	B.W.	2-18-76	SIZE	D CS
PROJ. ENG.	W.M.	3-18-76	NUMBER	H771-A-1
PROD.	W.M.	2/12/76	REV.	B
NEXT HIGHER ASSY.			SCALE	NONE
SCALE	NONE		SHEET	1 OF 1

THIS DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1975, DIGITAL EQUIPMENT CORPORATION

- NOTES:
1. SLOT BETWEEN P1-4 AND P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
 3. ALL WIRES TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.

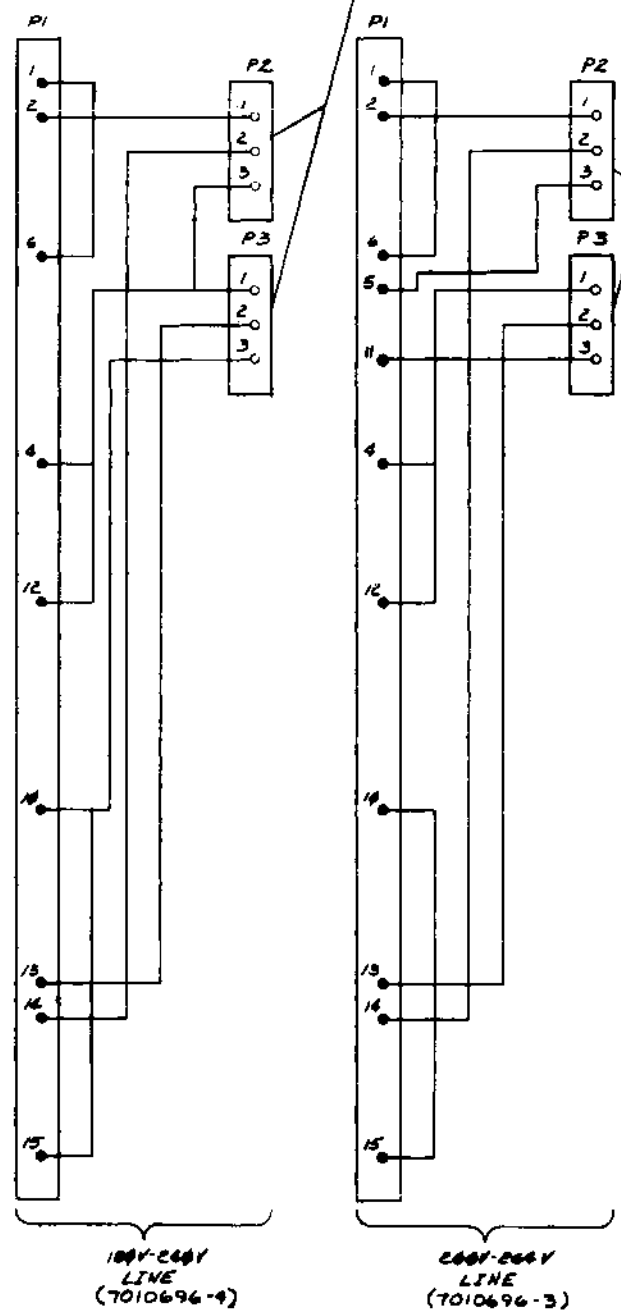
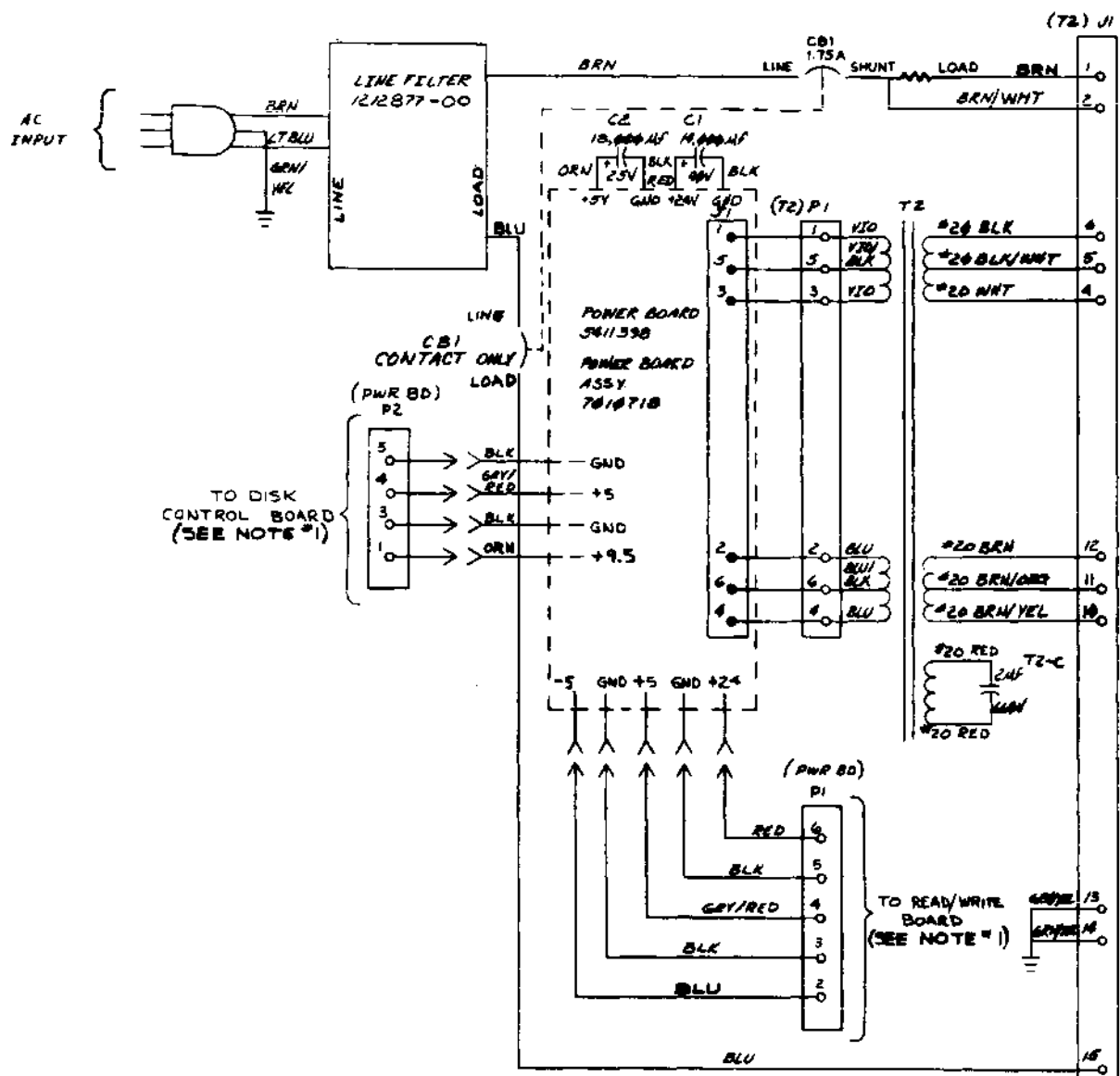


REV	DATE	BY	CHKD	APP'D
1	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
2	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
3	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
4	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
5	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
6	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
7	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
8	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
9	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
10	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
11	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
12	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
13	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
14	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
15	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
16	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
17	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
18	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
19	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN
20	11/17/75	B. HAZEN	B. HAZEN	B. HAZEN

DATE	11/17/75	DESIGNED BY	B. HAZEN
CHKD	B. HAZEN	APP'D	B. HAZEN
PROJ	11/17/75	TITLE	H771-C POWER CONNECTIONS
PROJ	11/17/75	SCALE	D CS H771-C-1
PROJ	11/17/75	SHEET	1 OF 1

THE DIMENSIONS AND SPECIFICATIONS SHOWN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION OF DIGITAL EQUIPMENT CORPORATION © 1975, DIGITAL EQUIPMENT CORPORATION

- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



100V-200V LINE (7010696-4)
200V-200V LINE (7010696-3)

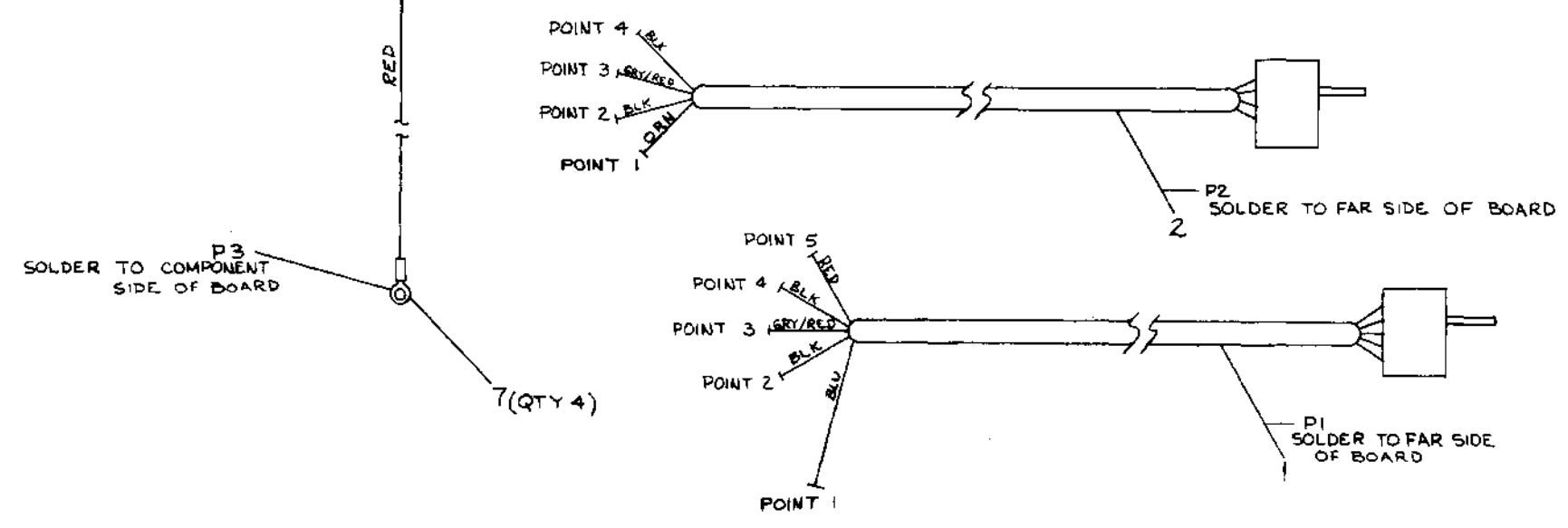
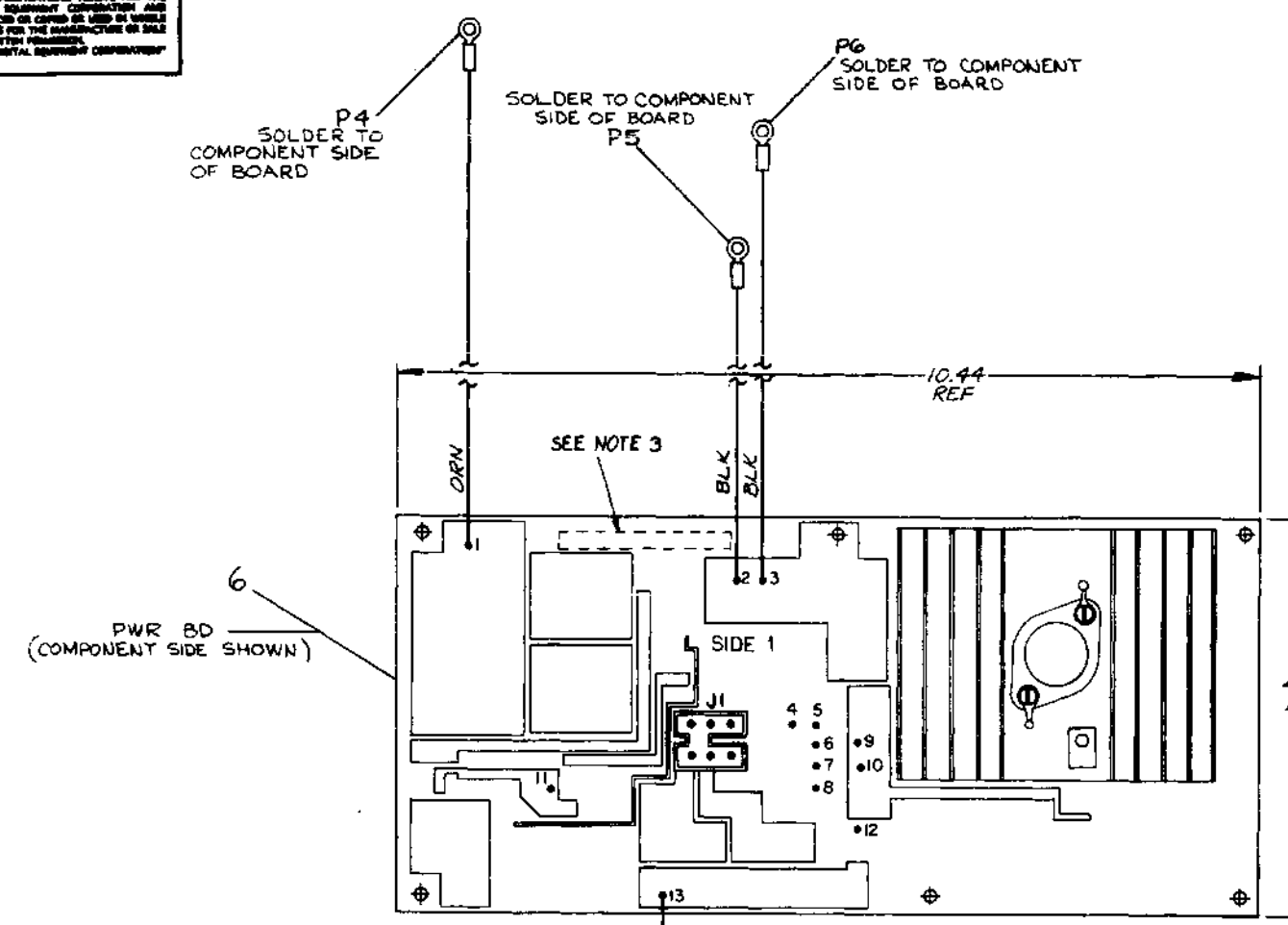
REV.	DATE	BY	CHKD.	DESCRIPTION
1	11/17/75	B. HAZEN	B. HAZEN	ISSUE FOR PRODUCTION
2	12/10/75	B. HAZEN	B. HAZEN	REVISED TO ADD DISK CONTROL BOARD CONNECTIONS
3	1/15/76	B. HAZEN	B. HAZEN	REVISED TO ADD READ/WRITE BOARD CONNECTIONS
4	2/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD TOLERANCE SPECIFICATIONS
5	3/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD DIMENSIONAL SPECIFICATIONS
6	4/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD MATERIAL SPECIFICATIONS
7	5/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD FINISH SPECIFICATIONS
8	6/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD LABELING SPECIFICATIONS
9	7/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD PACKAGING SPECIFICATIONS
10	8/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD STORAGE SPECIFICATIONS
11	9/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD SHIPMENT SPECIFICATIONS
12	10/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD INSPECTION SPECIFICATIONS
13	11/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD TESTING SPECIFICATIONS
14	12/10/76	B. HAZEN	B. HAZEN	REVISED TO ADD REWORK SPECIFICATIONS
15	1/10/77	B. HAZEN	B. HAZEN	REVISED TO ADD FINAL INSPECTION SPECIFICATIONS

DRN. 2/1/75	73075	FIRST USED ON	RX01
CHKD. B. HAZEN	8-5-75	TITLE	H771-D POWER CONNECTIONS
ENGR. B. HAZEN	8-12-75	PROJ. ENG. B. HAZEN	8-12-75
PROD. B. HAZEN	8-12-75	PROJ. MGR. B. HAZEN	8-12-75
NEXT HIGHER ASSY.			
B-D0-H771-D	SIZE CODE	NUMBER	REV.
SCALE	D	CS H771-D-1	C
SHEET	1 OF 1	DWG.	

THE DIMENSIONS AND SPECIFICATIONS SHOWN ARE THE PROPERTY OF MILITARY EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OF BULK OR OTHER EQUIPMENT WITHOUT PERMISSION. COPYRIGHT © 1975, MILITARY EQUIPMENT CORPORATION

ITEM NO.	DESCRIPTION		FROM		TO		LENGTH
	AWG	COLOR	CONN	TERM	CONN	TERM	
1	18	BLU	P1	POINT 1	PWR # 11	SOLDER	
		BLK	P1	POINT 2	PWR # 6		
		GRY/RED	P1	POINT 3	PWR # 9		
		BLK	P1	POINT 4	PWR # 5		
		RED	P1	POINT 5	PWR # 12		
2		ORN	P2	POINT 1	PWR # 4		
		BLK	P2	POINT 2	PWR # 7		
		GRY/RED	P2	POINT 3	PWR # 10		
	18	BLK	P2	POINT 4	PWR # 8		
3	14	RED	P3	ITEM 7	PWR # 13		13 IN ±.25
4	14	BLK	P5	ITEM 7	PWR # 2		7 IN ±.25
5	14	ORN	P4	ITEM 7	PWR # 1		11 IN ±.25
4	14	BLK	P6	ITEM 7	PWR # 3	SOLDER	9 IN ±.25

- NOTES:
1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
 2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
 3. INK STAMP ASSY NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.



QTY	DESCRIPTION	ENG. PART NO.	ITEM NO.
4	CONN, SOLDERLESS	9007928-00	7
1	POWER SUPPLY BOARD, RX01	D-ES-541199B-0-1	6
1/2	WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
1/2	WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
1/2	WIRE, #14 AWG, IPVC, RED	9107370-22	3
1	HARNESS, DISK CONTROL BOARD	D-IA-7010853-0-0	2
1	HARNESS, READ/WRITE BOARD	D-IA-7010854-0-0	1

REV	DATE	BY	CHKD	DESCRIPTION
1	12/10/75	W. HAZEN		ISSUE FOR MANUFACTURE
2	12/10/75	W. HAZEN		REVISED TO ADD P6
3	12/10/75	W. HAZEN		REVISED TO ADD P4
4	12/10/75	W. HAZEN		REVISED TO ADD P5
5	12/10/75	W. HAZEN		REVISED TO ADD P6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

APPLICABLE TO	ACCURACY	FRAMES	OVER	UNDER	FRAMES	OVER	UNDER
BLANK	±.005	±.005	±.005	±.005	±.005	±.005	±.005
DRILLED	±.005	±.005	±.005	±.005	±.005	±.005	±.005
MICROMETERS	±.001	±.001	±.001	±.001	±.001	±.001	±.001

QUANTITY & VARIATION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DIMS

MATERIAL SEE PARTS LIST

FINISH

DRN: 12575

CHKD: W. HAZEN

ENG: W. HAZEN

PROJ: 11-75

DATE: 12/10/75

FIRST LISTED ON: H771

TITLE: RX01 POWER BOARD ASSY

SIZE CODE: D AD 7010718-0-0

NUMBER: 1

REV: 5

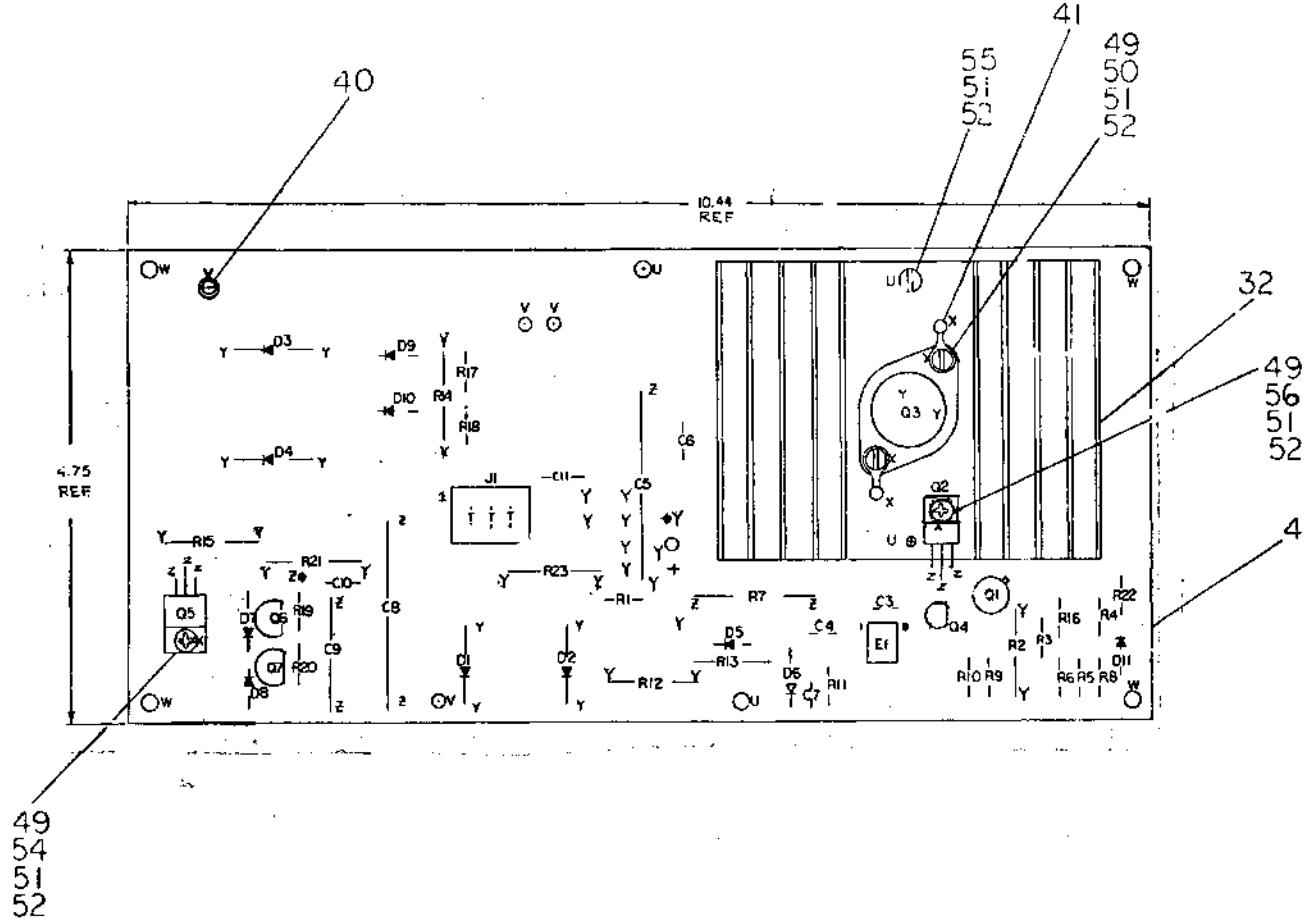
SHEET: 1 OF 1

REV. 5 D AD 7010718-0-0

THIS DRAWING AND SPECIFICATIONS, HEREIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.
 COPYRIGHT © 1974 DIGITAL EQUIPMENT CORPORATION

NOTES:

- UNLESS OTHERWISE SPECIFIED
 A. ALL RESISTORS ARE 1/4W, 5%.
 B. DOTTED AREAS COMPONENT NOT ON BOARD.
 C. AT TIME OF MODULE ASSY, ITEM 49 SHOULD BE APPLIED BENEATH Q2, Q3 & Q5.
- AT TIME OF ASSEMBLY, Q2, Q3 AND Q5 MOUNTING HARDWARE MUST BE TORQUED TO 4 TO 6 INCH POUNDS.
- Q4, Q6 AND Q7 OUTLINES CORRESPOND TO GENERAL ELECTRIC TYPE TRANSISTORS.
- FLAT RECTANGULAR WASHER SUPPLIED BY VENDOR TO BE MOUNTED UNDER Q2 AND Q5. SCREWHEAD.



REF	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
			X-Y COORDINATE HOLE LOCATION	K-00-541398-0-4	1
			5/32 DRILLING HOLE LAYOUT	D-AM-541398-0-5	2
			MODULE ECO HISTORY	B-MH-541398-0-6	3
			ETCHED CIRCUIT BOARD	5011397-0-0	4
	3	C3, C4, C7	CAP .01µF 100V 20% DISC	1001610-01	5
	2	C5, C8	CAP 1000µF 16V ELEC	1011849-02	6
	3	C6, C10, C11	CAP .1µF 100V 20% DISC	1000030-00	7
	1	C9	CAP 190µF 12V 10% ELEC	1009433-00	8
	2	D1, D2	DIODE 1N5818(N5818)	110420-00	9
	2	D3, D4	DIODE M2752	110615-00	10
	1	D5	DIODE 1N4744 15V 10%	1105648-00	11
					12
	2	D7, D6	DIODE .4MS, 1Z1, 5.1V 1%	1101873-00	13
	1	D8	DIODE D664	1100114-00	14
	2	D9, D10	DIODE 1N4004	1105796-00	15
	1	D11	DIODE 1N754A 6.8V 5%	1109991-00	16
	1	R5	RES 39 1/4W 5% CC	1302377-00	17
	1	R6	RES 470 1/4W 5% CC	1300316-00	18
	1	R7	RES .08 5W 3% CC	1311603-00	19
	1	R8	RES 47 1/4W 5% CC	1300202-00	20
	1	R9	RES 1M 1/4W 5% CC	1309595-00	21
	1	R12	RES 270 2W 5% CC	1305380-00	22
	1	R13	RES 511 1/4W 1% CC	1300324-00	23
	1	R14	RES 10 2W 10% CC	1300172-00	24
	1	R15	RES 180 1W 5% CC	1300262-00	25
	1	R16	RES 10 1/4W 5% CC	1301917-00	26
					27
	1	R18	RES 120 1/4W 5% CC	1300247-00	28
	2	R19, R20	RES 1K 1/4W 5% CC	1300365-00	29
	1	R22	RES 220 1/4W 5% CC	1300271-00	30
	1	R21	RES 120 1W 5% CC	1301938-00	31
	1	Q1	TRANS DEC 2E19-2	1501883-00	32
	1	Q2	TRANS D44C3	1510171-01	34
	1	Q3	TRANS DEC3715	1509068-00	35
	2	Q4, Q6	TRANS MKA805	1510705-00	36
	1	Q5	TRANS D45H3	1510708-01	37
	1	Q7	TRANS MKA855	1510706-00	38
	1	E1	I.C. DEC 301AN	1910282-00	39
	4	J1	EYELET	9007836-00	40
	2		TERMINAL LUG, SOLDER	9009676-00	41
	1	J1	CONNECTOR 6 PIN	1211342-0 6	42
					43
	1	R4	RES 560 1/4W 5% CC	1301890-00	44
	1	R23	RES 75 1W 5% CC	1305281-00	45
	3	R1, R10, R11	RES 10K 1/4W 5% CC	1300479-00	46
	1	R2	RES 390 2W 5% CC	1301864-00	47
	1	R3	RES 620 1/4W 5% CC	1303178-00	48
	1/R		THERMAL COMPOUND	9008238-00	49
	2		SCREW 4-40 X 1/2	9006013-04	50
	5		KERNUT 4-40	9006557-00	51
	5		WASHER FLAT 4-40	9006655-00	52
					53
	1		SCREW 4-40 X 5/16 (PHILLIPS HD)	9006011-1	54
	1		SCREW 4-40 X 7/16	9006012-04	55
	1		SCREW 4-40 X 1/2 (PHILLIPS HD)	9006013-1	56
	1		RES. 2K 1/4W 5%	1301969-00	57

381A	4	7
IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		

REV.	DATE	DESCRIPTION
1	11/27/74	INITIAL DESIGN
2	1/18/75	DESIGN CHANGES
3	1/24/75	DESIGN CHANGES
4	2/24/75	DESIGN CHANGES
5	3/24/75	DESIGN CHANGES

FIRST USED ON OPTION MODEL: RX01

ETCH BOARD REV. D

digital

TITLE: RX01 POWER SUPPLY

SIZE: 1.000 INCHES

NUMBER: DCS 541398-0-1

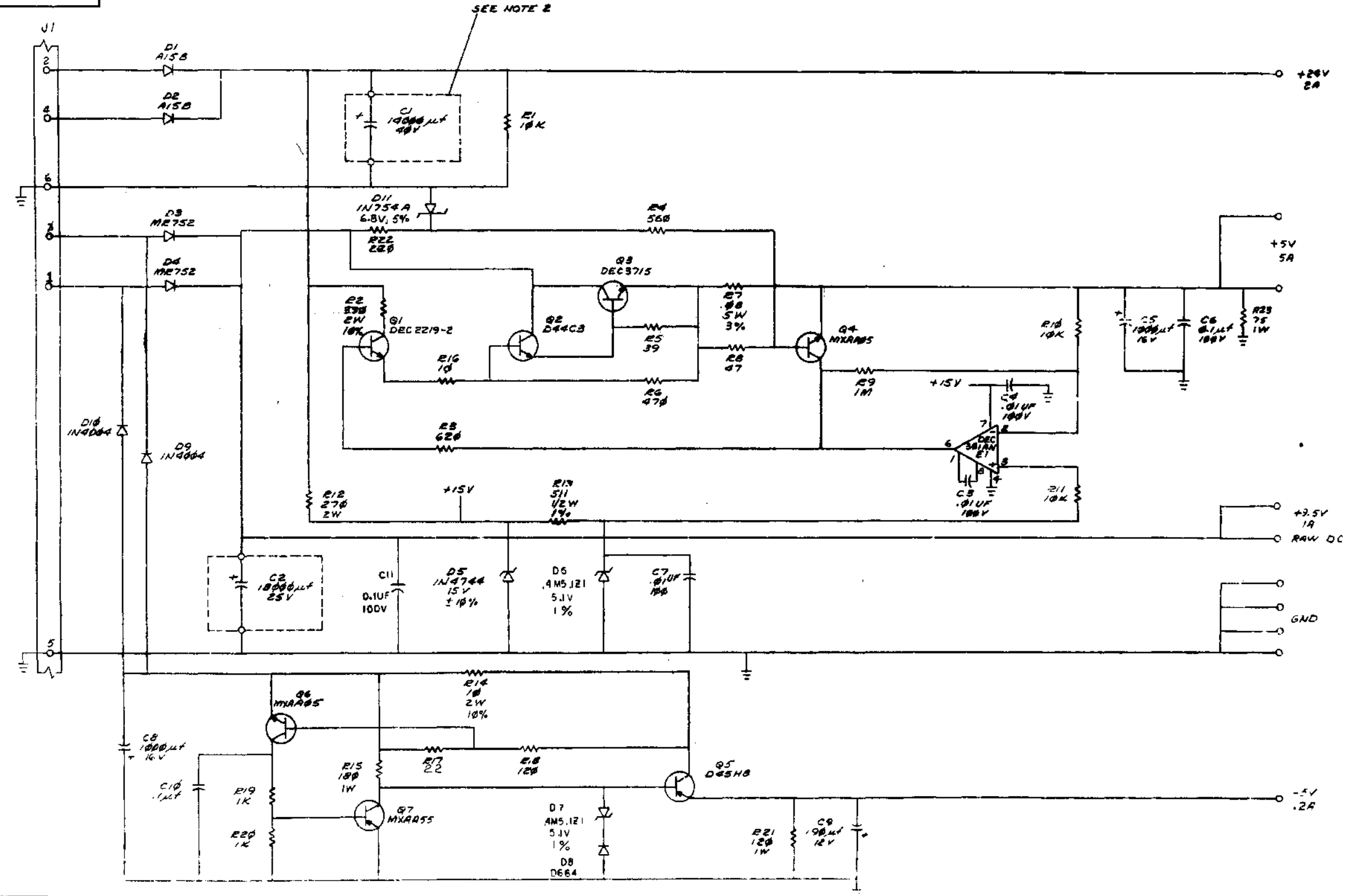
REV. E

SCALE: 1:1

SHEET 1 OF 3

SEMICONDUCTOR CONVERSION CHART

THIS DRAWING AND SPECIFICATIONS HERIN ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1974 DIGITAL EQUIPMENT CORPORATION



SEE NOTE 2

REVISIONS		
NO.	CHANGE NO.	REV.

TITLE	RXC1 POWER SUPPLY	SIZE/DWG	DGS	NUMBER	5411398-0-1	REV.	F
SCALE	1:1	SHEET	1	TOTAL	1	DATE	

