RK06/RK07 Disk Drive Technical Description Manual

digital

EK-RK067-TD-001

RK06/RK07 Disk Drive Technical Description Manual

digital equipment corporation • maynard, massachusetts

Preliminary, November 1977
1st Edition, March 1978

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

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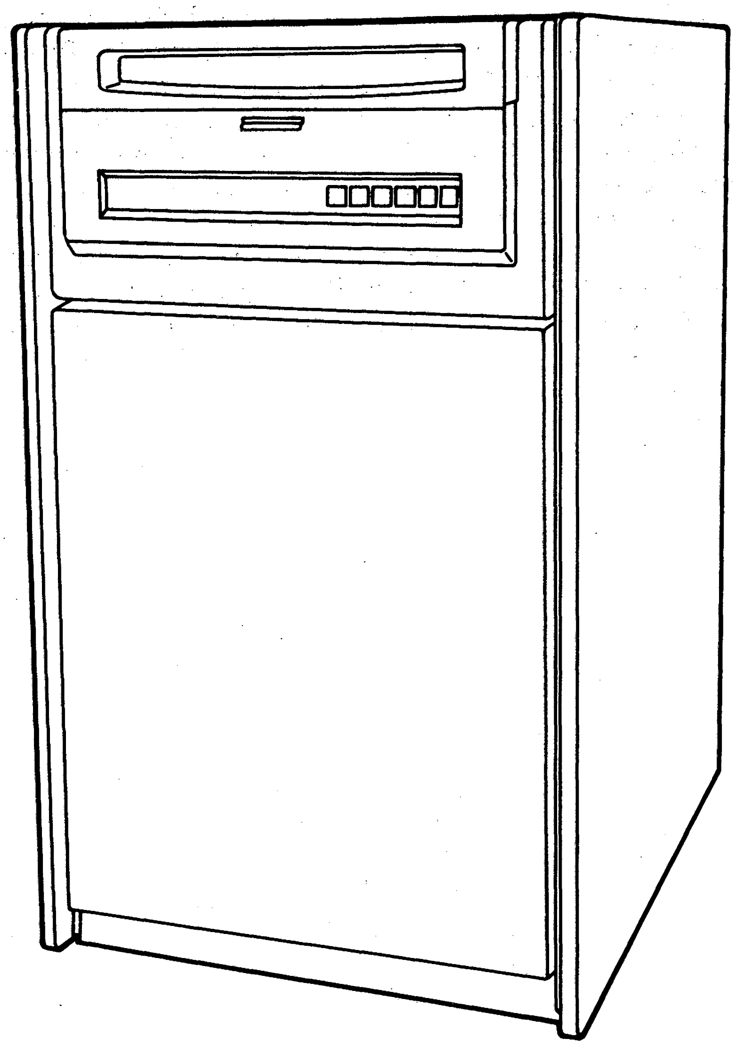


Typical Disk Drive in H969 Cabinet

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The RK06/RK07 Disk Drives are designed and manufactured by Digital Equipment Corporation. They are high-performance moving-head devices for storing and retrieving computer-processed data at random-accessed locations. The data is stored on three recording surfaces of a top-loading, dual-disk cartridge.

Both of the drives are designed for use with a variety of controllers in numerous applications for such computer systems as the DIGITAL PDP-11, DECsystem-10, and similar equipment. As many as eight RK06 drives may be selectively utilized by a single controller via a "daisy-chain" bus. A dual-access option makes each drive of the chain accessible to either of two controllers on a controlled priority basis. The decoded data from a servo surface in the cartridge provides: (1) radial (cylinder) and rotational (index/sector) coordinates for data storage locations on the disks in read/write operations, and (2) a clock output that is synchronized with the disk rotational speed for write operations. One type of cartridge may be freely interchanged between any RK06 drives, and another type of cartridge may be similarly exchanged between any RK07 drives. Figure 1-1 shows the basic functions performed by the subsystems comprising the drive.

1.2 MANUAL PURPOSE AND ORGANIZATION

This RK06/RK07 technical description manual has been prepared with the following objectives in mind.

1. To document drive operational concepts and detailed design information for field engineers and/or customer personnel being trained by DEC Educational Services

2. To provide field maintenance personnel with technical description details to reinforce the system service manual, and to provide information that may not be duplicated in any other hardware manual

To accomplish these objectives, the technical description is organized in progressive levels of detail that should facilitate technical comprehension at three levels. Chapter 2 describes both drives on a system level, and Chapter 3 describes both drives in terms of interfacing with the controller. Chapters 4 and 5 describe the drives on a unit level, with Chapter 4 devoted to a discussion of the RK06 and Chapter 5 dealing solely with the RK07 drive.

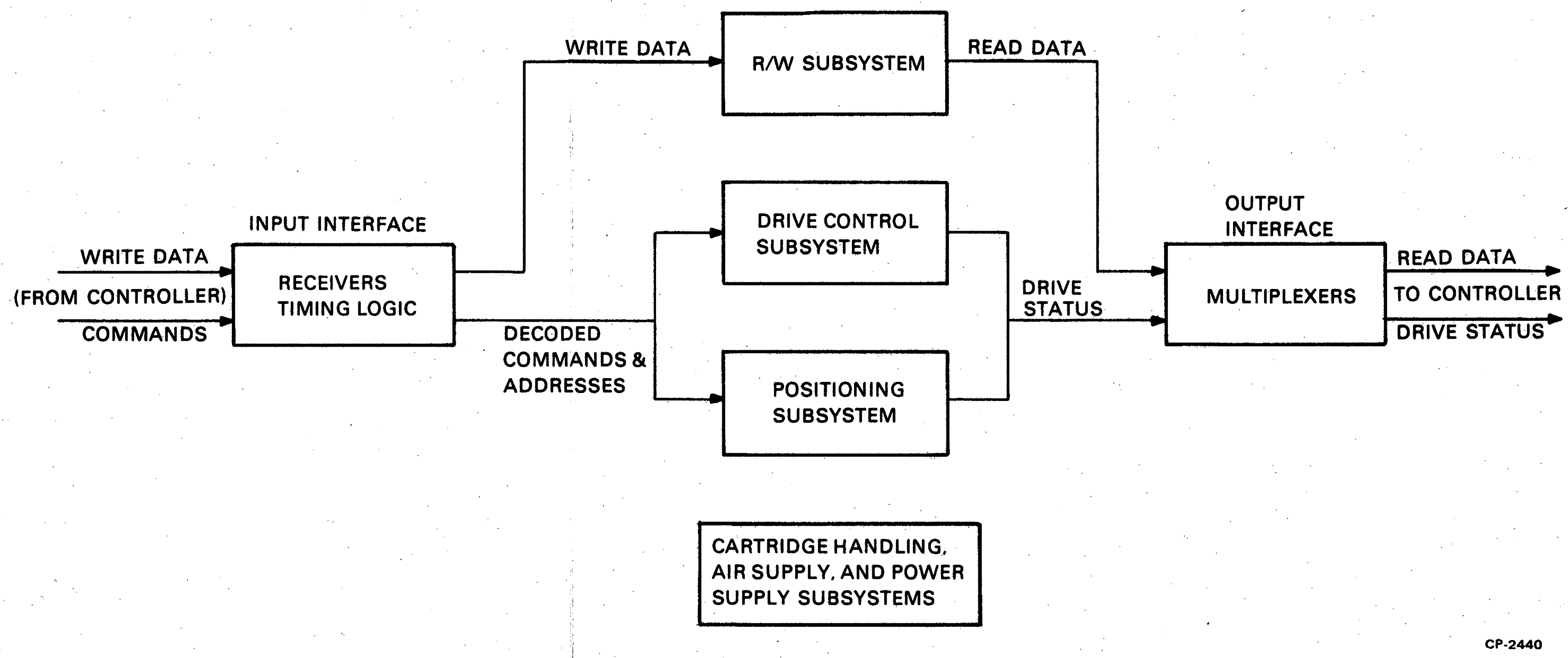


Figure 1-1 RK06/RK07 Disk Drive Functional Block Diagram

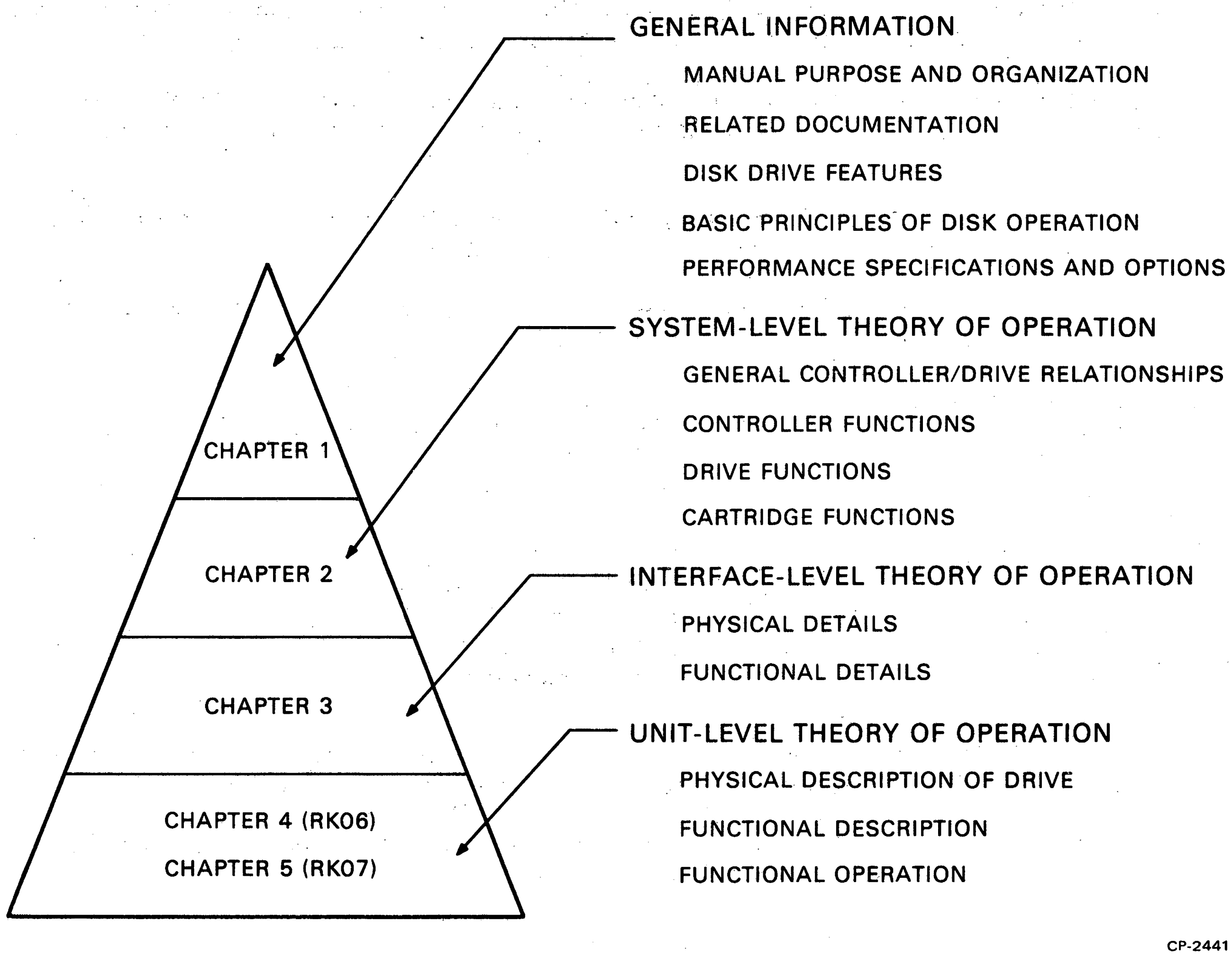


Figure 1-2 *RK06/RK07 Disk Drive Technical Description Manual* Organization

1.2.1 Chapter Content

The content of this manual can be summarized as follows.

Chapter 1–General Information – This chapter presents a general introduction to the RK06 and RK07: drive features, identification of major assemblies, related documentation, and performance specifications.

Chapter 2–System-Level Theory of Operation – This chapter identifies and describes the basic components of an RK06 or RK07 system and the relationships of these components.

Chapter 3–Interface-Level Theory of Operation – This chapter provides specific detail on the functional relationships between a controller and the disk drive, and the communications between them.

Chapter 4–RK06 Unit-Level Theory of Operation – This chapter provides the physical details, functional descriptions and operations within the RK06 drive.

Chapter 5–RK07 Unit-Level Theory of Operation–This chapter provides the physical details, functional descriptions, and operations within the RK07 drive.

1.2.2 Related Documentation

The following documents supplement this technical description manual on the RK06 and RK07 drives.

Document No.	Title
EK-RK611-TM-002	RK611 Controller Technical Manual
EK-RK067-UG-001	RK06/RK07 Disk Drive User's Manual
EK-RK067-SV-001	RK06/RK07 Disk Subsystem Service Manual
EK-RK06-IP-001	RK06 Illustrated Parts Breakdown
EK-RK07-IP-001	RK07 Illustrated Parts Breakdown

1.3 DISK DRIVE FEATURES

The RK06 or RK07 Disk Drive, when used with the RK611 controller, provides a high-performance, medium-capacity, on-line mass storage subsystem whose key features are as follows.

- Interchangeable storage media (disk cartridges) that provide a data capacity whose only limitation is the number of cartridges on hand

NOTE
Cartridges are not interchangeable between RK06 and RK07 drives. See Paragraph 1.6.

- Dual-access option permitting operation with two controllers

- Daisy-chain capability that gives a controller access to as many as eight disk drives, and both RK06 and RK07 drives may be connected to the same chain.

- An extensive (eight 16-bit word) status-reporting system which, in conjunction with appropriate software, assures an extremely rapid and accurate diagnostic capability

- A serial command and address structure for simplified controller/drive interface relationships

- A track-following servo system that provides accurate head positioning over a wide range of operating temperatures

- High-density recording capability (14 million bytes, formatted on the RK06, or 28 million bytes, formatted, on the RK07) achieved by modified frequency modulation (MFM) data recording

- A negligible sensitivity to variations in drive spindle speed through use of phase-locked oscillators for reading and writing

- Effective data recovery capability realized through the use of offset head-positioning techniques

- Provisions for connecting a drive to a field test box without disturbing the operation of other drives on the daisy-chain

- Brush-cleaning cycle for disk surfaces at each spindle startup sequence

- Inclusion of a heads home-lock that prevents accidental loading during system operation and eliminates the possibility of unrestrained head motion during shipment

1.4 BASIC PRINCIPLES OF DISK DRIVE OPERATION

The RK06 and RK07 are magnetic-memory devices with integral power supplies. The drives operate from commercial power and respond to commands from the controller of a computer system. The drives have two primary functions: a read or a write. To perform these functions, it is first necessary for the controller to command a seek operation. Three read/write heads and one servo head are then positioned at a precise radial (cylinder) location relative to the disk rotational centerline.

Radial and rotational coordinate data for each recorded bit are derived from the prerecorded servo surface of the disk cartridge. Head positioning is achieved by a linear motor positioner under servo control. The linear velocity of the heads is a direct function of the radial distance remaining to traverse when seeking a new track address. Until directed by the controller to perform a write operation, the drive operates in a read mode.

Disk rotational velocity is held nearly constant by an ac drive motor. Numerous electromechanical interlocks prevent loss of stored data as a result of human or machine error. Data storage capacity is limited only by the number of cartridges available to the drive(s).

The controller selects a specific drive of the daisy-chain, selects one of the three read/write heads, and designates cylinder and sector locations for data storage or retrieval. As explained before, controller operations are based on the program originating at the central processor unit (CPU) of the computer system. The detailed functional operations performed by the drive and the logical implementation of these functions are covered in Chapter 4 for the RK06 drive, and Chapter 5 for the RK07 drive. The RK06 or RK07 drive comprises the major functional entities shown in Figure 1-1.

The RK06K-DC or RK07K-DC cartridge is used exclusively by its respective disk drive, but is not an integral part of the drive.

1.5 PERFORMANCE SPECIFICATIONS

Table 1-1 gives the principal performance specifications for the RK06 drive. Table 1-2 lists similar specifications for the RK07 drive.

Table 1-1 RK06 Disk Drive Performance Specifications

Characteristics	Specifications	
Storage Medium		
Type	Dual disk magnetic cartridge, DEC RK06K-DC	
Disk Diameter	355 mm (14 in), nominal	
Magnetic Heads	Three read/write; one servo	
Recording Capacity (formatted)	**18-Bit Word**	**16-Bit Word**
Cylinders/Cartridge	411	411
Tracks/Cylinder	3	3
Tracks/Cartridge	1233	1233
Sectors/Track	20	22
Words/Sector	256	256
Bits/Word	18	16
Bits/Sector	4608	4096
Bits/Track	92160	90112
Bits/Surface	37.88M	37.04M
Bits/Cartridge	113.63M	111.11M
Bits/Inch (inner track)	4040	4040
Tracks/Inch	192.3	192.3
Bit Transfer Rate (unbuffered nominal)	4.301M/second	4.301M/second
Bit Cell Width	232.5 ns	232.5 ns
Latency		
Rotational Frequency	2400 rev/min ± 2.5%	
Average	12.5 ms (1/2 rotation)	
Maximum	25.0 ms	
Seek Times		
Average	38 ms (maximum)	
One-Cylinder	8 ms (maximum)	
Longest	75 ms (maximum)	
Start/Stop Times	**Maximum**	**Nominal**
Start	60 seconds	30 seconds
Stop	60 seconds	30 seconds

Table 1-1 RK06 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications
Model Designations	
RK06-EA RK06-EB RK06-EC RK06-ED	90–132 Vac, @ 60 ± 0.5 Hz 180–264 Vac, @ 60 ± 0.5 Hz 90–132 Vac, @ 50 ± 0.5 Hz 180–264 Vac, @ 50 ± 0.5 Hz
	NOTE **Models RK06-FA through FD are the dual-access models corresponding to models EA through ED.**
Electrical	
Voltage	See Model Designations, above
Start Current (10 seconds, maximum)	
Low-Voltage Range High-Voltage Range	10.0 A, rms, maximum @ 115 Vac 5.0 A, rms, maximum @ 230 Vac
Power Factor	0.85, minimum
Power Cord	
Length	2.7 m (9 ft)
Plug Types	NEMA 5-15P for 120 Vac (nominal) models NEMA 6-15P for 230 Vac (nominal) models
Input Power	
60 Hz 50 Hz	500 W, maximum 550 W, maximum
Operating Environment	
Ambient Temperature	10° to 40° C (50° to 104° F)
Temperature Rate of Change	20° C/hour (36° F/hour)
Relative humidity for maximum wet bulb temperature of 28° C (82° F) and minimum dew point temperature of 2° C (36° F)	10 to 90%

Table 1-1 RK06 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications
Operating Environment (cont)	
Altitude	2444 m (8000 ft)
Airborne Particulants	Operation in an ambient environment of less than one million particles per cubic foot of air, each particle being 0.5 μm or larger.
Attitude	
Pitch	0 ± 5 degrees, maximum
Roll	0 ± 5 degrees, maximum
Heat Dissipation	
Nominal	1500 Btu/hour
Maximum	1700 Btu/hour
Cartridge Temperature Stabilization	2 hours (within cartridge protection cover) at drive operating temperature
Dimensions	
Width	481 mm (19 in), RETMA 10 inch rack compatible
Depth	749 mm (29 1/2 in)
Height	400 mm (15 3/4 in)
Weight (alone)	89.0 kg (196 lb)
Weight (with H969 cabinet)	148 kg (326 lb)
Nonoperating Environment	
Temperature	-40° C (-40° F) to 66° C (151° F)
Humidity	0% to 95%
Altitude	9.1 km (30,000 ft)

Table 1-2 RK07 Disk Drive Performance Specifications

Characteristics	Specifications	
Storage Medium		
Type	Dual disk magnetic cartridge, DEC RK07K-DC	
Disk Diameter	355 mm (14 in), nominal	
Magnetic Heads	Three read/write; one servo	
Recording Capacity (formatted)	**18 Bit Word**	**16 Bit Word**
Cylinders/Cartridge	815	815
Tracks/Cylinder	3	3
Tracks/Cartridge	2445	2445
Sectors/Track	20	22
Words/Sector	256	256
Bits/Word	18	16
Bits/Sector	4608	4096
Bits/Track	92160	90112
Bits/Surface	73.43M	75.11M
Bits/Cartridge	220.32M	225.33M
Bits/Inch (inner track)	4040	4040
Tracks/Inch	384.6	384.6
Bit Transfer Rate (unbuffered nominal)	4.301M/second	4.301M/second
Bit Cell Width	232.5 ns	232.5 ns
Latency		
Rotational Frequency	2400 rev/min ± 2.5%	
Average	12.5 ms (1/2 rotation)	
Maximum	25.0 ms	

Table 1-2 RK07 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications	
Seek Times		
Average	36.5 ms (maximum)	
One-Cylinder	6.5 ms (maximum)	
Longest	71.0 ms (maximum)	
Start/Stop Times	**Maximum**	**Nominal**
Start	60 seconds	30 seconds
Stop	60 seconds	30 seconds
Model Designations		
RK07-EA	90–128 Vac, @ 60 ± 0.5 Hz	
RK07-EB	180–264 Vac, @ 60 ± 0.5 Hz	
RK07-EC	90–128 Vac, @ 50 ± 0.5 Hz	
RK07-ED	180–264 Vac, @ 50 ± 0.5 Hz	
	NOTE Models RK07-FA through FD are the dual-access models corresponding to models EA through ED.	
Electrical		
Voltage	See Model Designations, above	
Start Current (10 seconds, maximum)		
Low-Voltage Range	10.0 A, rms, maximum @ 115 Vac	
High-Voltage Range	5.0 A, rms, maximum @ 230 Vac	
Power Factor	0.80, minimum	
Power Cord		
Length	2.7 m (9 ft)	
Plug Types	NEMA 5-15P for 120 Vac (nominal) models NEMA 6-15P for 230 Vac (nominal) models	
Input Power		
60 Hz	500 W, maximum	
50 Hz	550 W, maximum	

Table 1-2 RK07 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications
Operating Environment	
Ambient Temperature	10° to 40° C (50° to 104° F)
Temperature Rate of Change	20° C/hour (36° F/hour)
Relative humidity for maximum wet bulb temperature of 28° C (82° F) and minimum dew point temperature of 2° C (36° F)	10 to 90%
Altitude	2444 m (8000 ft)
Airborne Particulants	Operation in an ambient environment of less than one million particles per cubic foot of air, each particle being 0.5 μm or larger
Attitude	
Pitch	0 ± 5 degrees, maximum
Roll	0 ± 5 degrees, maximum
Heat Dissipation	
Nominal	1500 Btu/hour
Maximum	1700 Btu/hour
Cartridge Temperature Stabilization	2 hours (within cartridge protection cover) at drive operating temperature
Dimensions	
Width	481 mm (19 in), RETMA 10 in rack compatible
Depth	749 mm (29 1/2 in)
Height	400 mm (15 3/4 in)
Weight (alone)	89 kg (196 lb)
Weight (with H969 cabinet)	148 kg (326 lb)
Nonoperating Environment	
Temperature	-40° C (-40° F) to 66° C (151° F)
Humidity	0% to 95%
Altitude	9.1 km (30,000 ft)

1.6 USE OF RK06 AND RK07 DRIVES IN THE SAME SYSTEM

The RK06 and RK07 Disk Drives, because of their similarities, can be used on the same system. One RK611 controller can handle up to eight drives – either RK06 or RK07 drives or any combination of the two.

Disk cartridges, however, may not be exchanged between an RK06 and an RK07 drive. Any RK06K-DC cartridge may be used on any RK06 drive, but not on an RK07 drive. Similarly, the RK07K-DC cartridge is designed for use on any RK07 drive, but will not function in an RK06 drive. The cartridges can be distinguished by a label on the top cover.

1.6.1 Interlock System

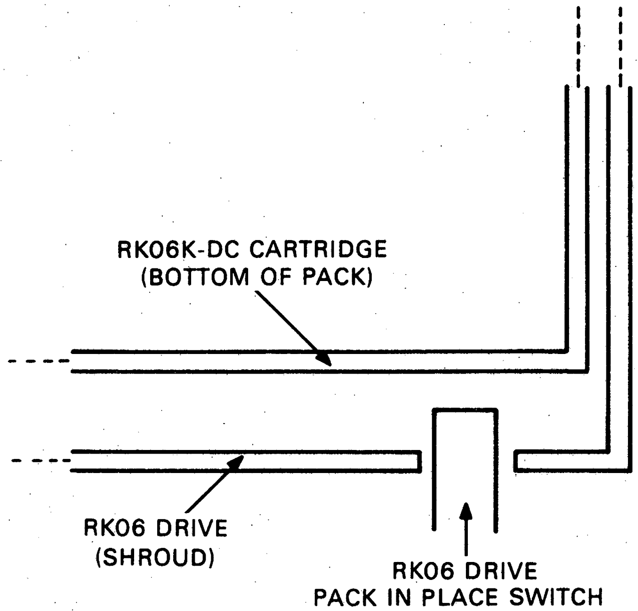
The interlock system to prevent the use of the wrong cartridge on a drive is shown in Figure 1-3. The bottom on an RK06K cartridge is smooth in the area where it will contact the Pack In Place switch on the RK06 drive. The RK07K cartridge has a hole in the bottom where the RK06 Pack In Place switch would normally contact the cartridge. Thus, an RK07K cartridge will not press the Pack In Place switch on an RK06 drive and the drive will not operate.

The RK07 drive Pack In Place switch will make contact with the bottom of an RK06K cartridge. However, the switch is set so that the RK06K cartridge will not depress the RK07 Pack In Place switch far enough to set the microswitch, thus preventing the RK07 drive from operating with an RK06K cartridge in place. The raised button on the bottom of the RK07K ensures that the RK07 drive will sense the RK07K cartridge, because it will depress the RK07 Pack In Place switch a sufficient amount to turn the microswitch on.

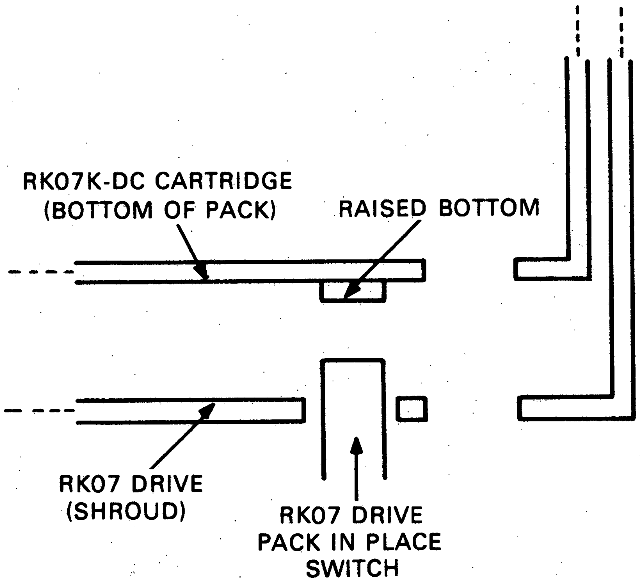
1.6.2 Logic Modules

The RK06 and RK07 drives each use several hex-printed circuit board modules, described in more detail in Chapters 4 and 5. Three of the boards perform similar functions in each drive, but are unique to either the RK06 or the RK07. These modules are as follows.

Name	**RK06**	**RK07**
Servo Control	M7707	M7907
Servo Analog	M7729	M7906
TPD/PLO	M7708	M7908



a. RK06 Drive Interlock



b. RK07 Drive Interlock

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Figure 1-3 Cartridge Interlock System

CHAPTER 2
SYSTEM-LEVEL THEORY OF OPERATION

2.1 GENERAL
The basic system for RK06 or RK07 Disk Drive applications (Figure 2-1) is made up of the following.

1. Central processor
2. Memory
3. Controller
4. Interface cables
5. Up to eight RK06 or RK07 drives (and their cartridges) configured in a daisy-chain bus

In this configuration, all drive interface lines are connected in common. As a result, every drive unit receives identical commands or data from the controller simultaneously. However, the only drive responding to these signals is the one whose specific access number is designated in the transmission. Drive selection is based on an addressing process performed by the controller. Drive selection occurs upon a compare (in the drive) of the address received from the controller and the binary-encoded unit select plug on the operator's control panel of the drive.

As seen in Figure 2-1, the dual-access option for either type of disk drive enables the use of two controllers with each daisy-chain. These controllers can be connected to the same or different CPU.

2.2 CONTROLLER
The controller for the drive receives its commands and data from the central processor and memory. From these inputs, the controller directs a selected drive to perform such functions as head selection, head positioning, and the reading or writing of data (Figure 2-2). The controller also directs its drives to supply specific status information that ensures drive readiness to engage in a data transfer. The status information available from each drive also makes possible the use of sophisticated diagnostic programs for rapid fault isolation.

For write operations, the data to be written on the disk surface of a drive is encoded by modified frequency modulation (MFM) techniques and is precompensated to correct for peak shift in the flux reversals before serial transmission to the drive over the single bidirectional data path. (See Paragraphs 2.4 and 2.5.)

In read operations, the serial data from drive to controller is separated from its clock data by the controller before the formation of parallel data words for transmission to the central processor.

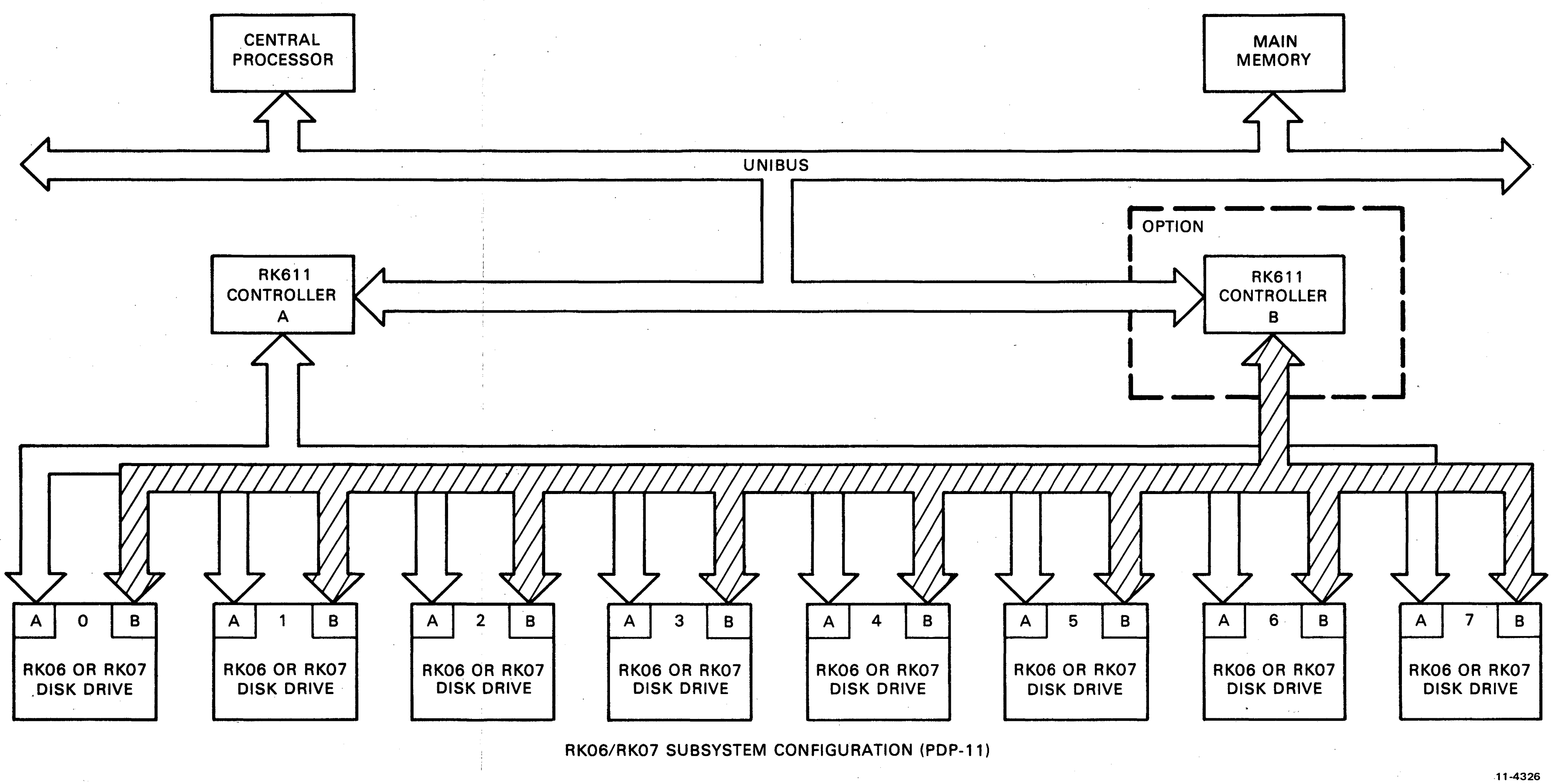


Figure 2-1 Basic Disk Subsystem

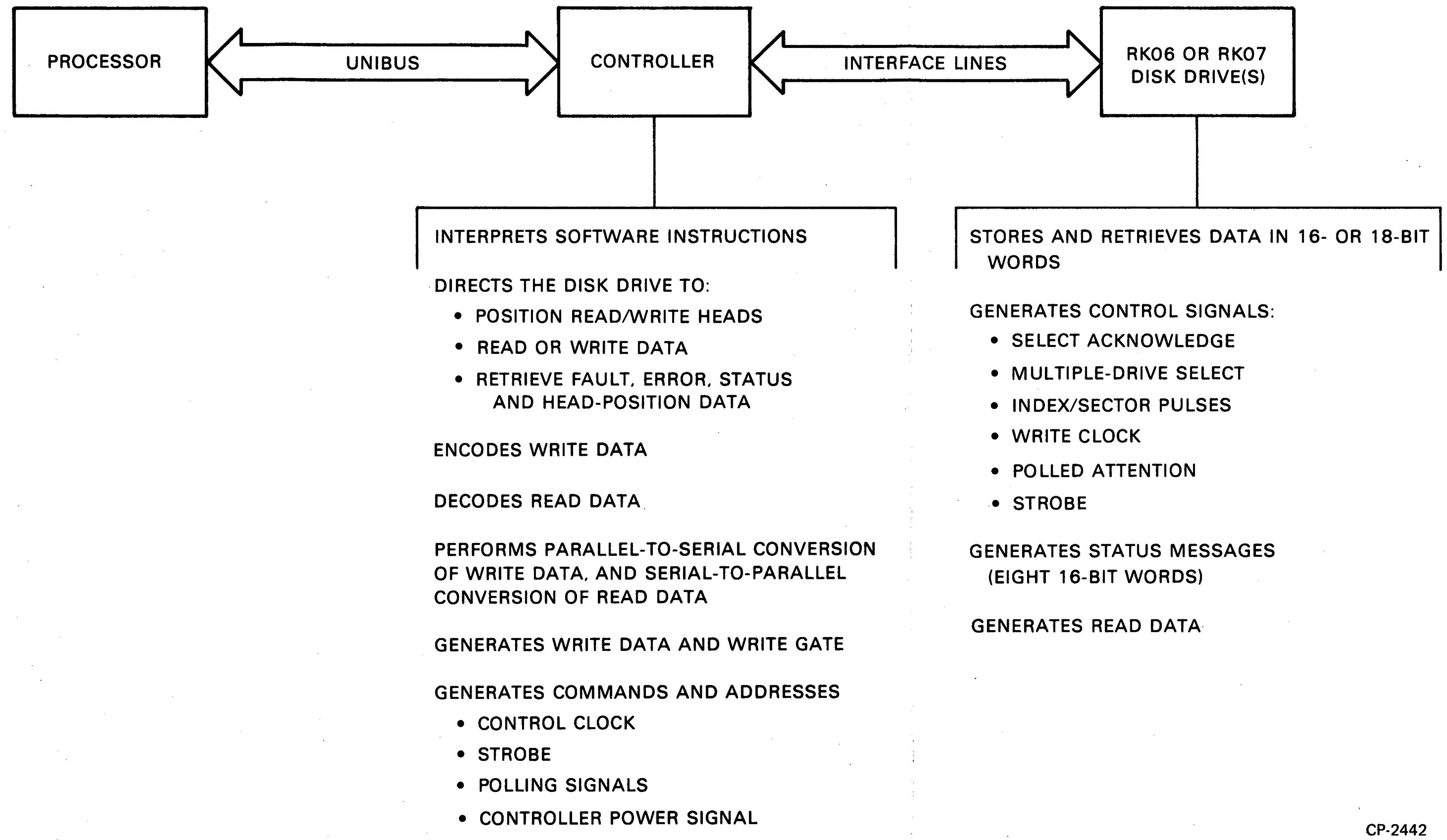


Figure 2-2
Controller/Disk Drive Subsystem Functions

2.3 DISK DRIVE CARTRIDGE

The RK06 Disk Drive and the RK07 Disk Drive both use a similar cartridge for data storage. The RK06K-DC cartridge will function only in an RK06 drive, and the RK07K-DC will function only on an RK07 drive. The drive interlock system to accomplish these restrictions is described in Paragraph 1.6.

Each cartridge has two disk platters. Three of the four surfaces are used for data storage, while the fourth provides signals for servo control and clock signal development. The prerecorded (dedicated) servo surface is configured for a fixed number of data tracks, 411 on the RK06K cartridge and 815 on the RK07K. An index pattern recorded on every track provides a rotational position reference for the cartridge. The controller establishes the number of sectors (either 20 or 22) per track and the composition of the information recorded within each sector. Sectors contain header information, data fields, check fields, and sync information. Data can be written as 18- or 16-bit words; this selection determines the number of sectors per track (20 or 22, respectively). However, data capacity is 256 words per sector for both formats.

The access mechanism in the RK06 or RK07 drive permits the positioning of the read/write heads (for the data surfaces) and the read-only head (for the servo surface) over any one of the usable data or servo tracks on either platter. The four heads are vertically aligned. The servo surface provides a continuous output of tribits, which are used in obtaining the location of the heads at any particular moment. The tribit signal will indicate the rotational position of the heads, and is also used to derive the clock signal, Write Clock.

The cartridge is shown in Figure 2-3. It consists of a disk assembly enclosed in plastic covers. The top and bottom covers are firmly fastened together and are secured to the disk assembly through the handle mechanism. The protection cover, which is removable, fastens to the disk assembly by means of a magnetic retaining ring. The disk assembly (Figure 2-4) is made up of the following.

1. A data and a servo disk, each approximately 36 cm (14 in) in diameter
2. Two clamp rings
3. Disk hub
4. Armature plate

The handle and handle mechanism provide a convenient means for transporting the cartridge during loading and unloading. The handle slide is used to release the protection cover and to detach the disk assembly. The protection cover surrounds the disk assembly and seals firmly against the gasket in the underside of the top cover during shipment, storage, or other nonoperating situations. When the disk cartridge is installed in the disk drive shroud, the protection cover is removed and placed above the top cover.

2.3.1 Data Surface Characteristics

From top to bottom, the four disk surfaces are identified as 0, 1, S (servo surface), and 2. At the time of manufacture, each of the three data surfaces is prerecorded with 22 sectors of 16-bit data words. All the data fields, except those on the last (innermost) track, are filled with 0s.

The coated band on an RK06K cartridge disk surface extends from an inner radius of 95 mm (3.75 in) to an outer radius of 180 mm (7.0 in). The width of each data track is 0.10 mm (0.0043 in), nominal, and the distance between adjacent data tracks is 0.12 mm (0.0052 in). Similarly, the coated band on an RK07K cartridge disk surface extends from an inner radius of 95 mm (3.75 in) to an outer radius of 177 mm (6.98 in). The width of each data track is 0.053 mm (0.0021 in), nominal, and the distance between adjacent data tracks is 0.066 mm (0.0026 in).

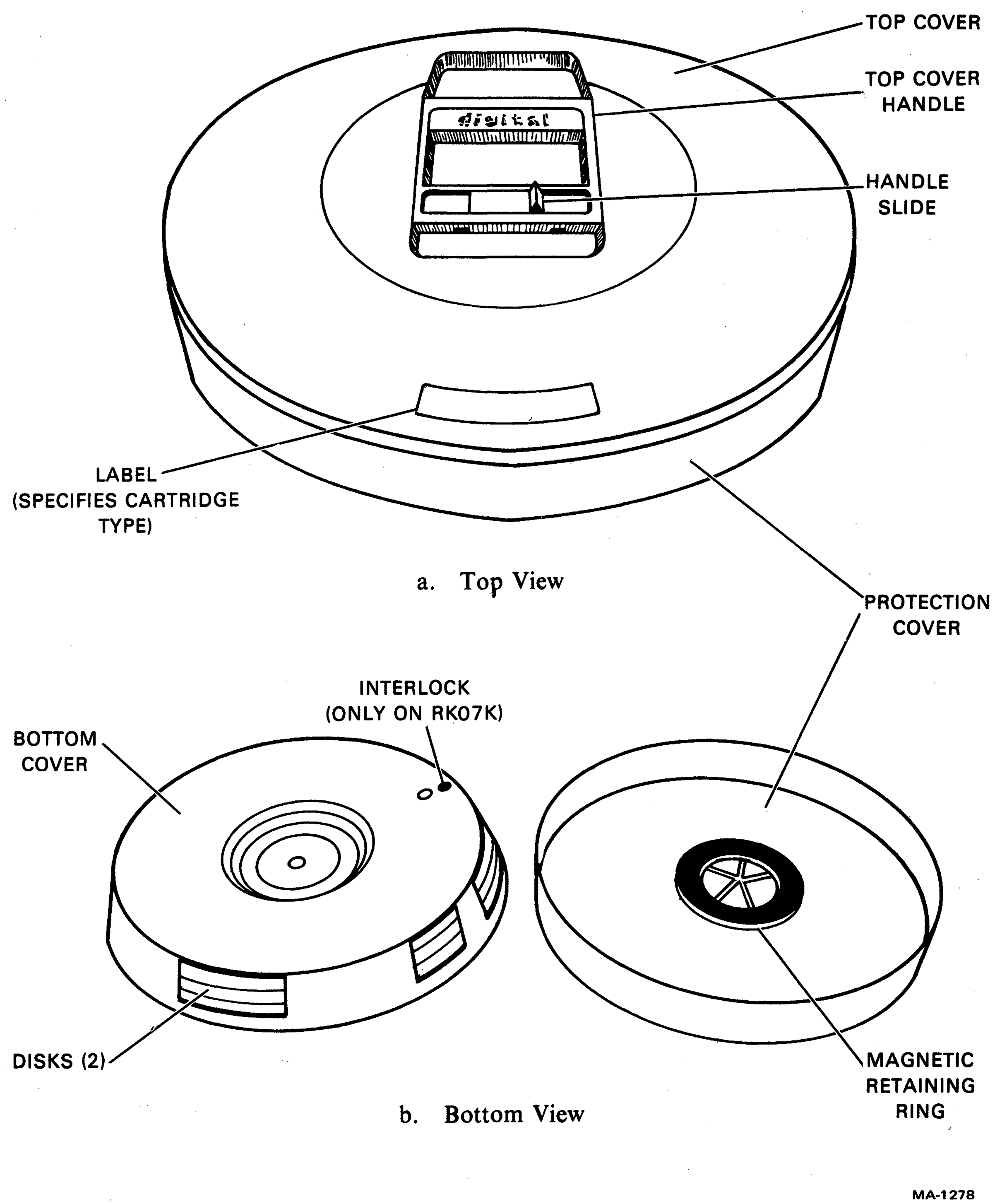
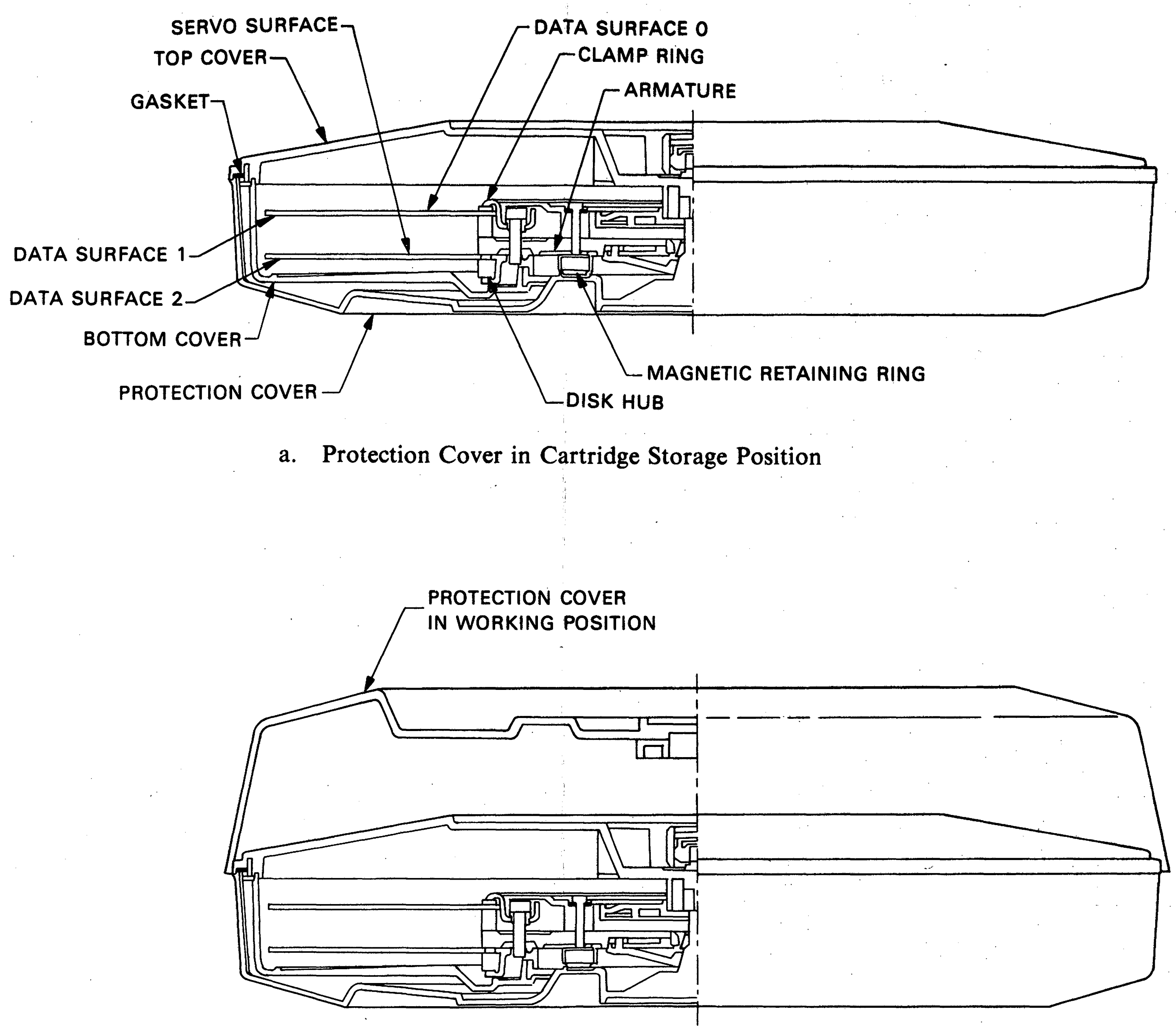


Figure 2-3 RK06K or RK07K Disk Cartridge Assembly



a. Protection Cover in Cartridge Storage Position

b. Protection Cover in Cartridge Working Position

Figure 2-4 RK06K or RK07K Disk Cartridge (Cross-Section)

2.3.2 Servo Surface Characteristics

The RK06K servo surface, shown in Figure 2-5, comprises:

1. A head-loading zone (unrecorded) of 6.35 mm (0.25 in) radial distance near the outer edge of the disk
2. An outer guard zone of 12 odd servo tracks
3. A servo zone providing for 411 data tracks
4. An inner guard zone consisting of 18 even tracks.

The RK07K servo surface, shown in Figure 2-6, is similarly designed, with:

1. A head-loading zone (unrecorded) of 5.33 mm (0.21 in) radial distance near the outer edge of the disk
2. An outer guard zone of 24 odd servo tracks
3. A servo zone providing for 815 data tracks
4. An inner guard zone consisting of 36 even tracks.

Like the data surfaces, the coated band on the servo surface extends from an inner radius of 95 mm (3.75 in) on both types of cartridges, to an outer radius of 180 mm (7.0 in) on the RK06K, or to an outer radius of 177 mm (6.98 in) on the servo surface of the RK07K. The nominal distance between centerlines of adjacent servo tracks (spaced halfway between the data track centerlines) is 0.12 mm (0.0052 in) on the RK06K servo surface, or 0.066 mm (0.0026 in) on the RK07K servo surface.

Figures 2-7 and 2-8 illustrate the major details of the signals generated by the servo surface. Each track on the servo surface is prerecorded, during manufacturing, with an encoded repetitive pattern of tribits, with all tracks having the same number (6720) of tribits. For each disk revolution, the tribit pattern is interrupted by a single index pattern (Figure 2-9) to which all sector timing is referenced. The servo read-only head delivers an output that is preamplified and continuously decoded to provide the drive with the following information.

1. Radial position of heads, relative to the cartridge tracks
2. Rotational position of the cartridge (derived index and sector pulses)
3. Clock pulses that are synchronized to disk speed for use in generating the Write Clock signal sent to the controller and used for timing within the drive. Write Clock frequency is 8.602 MHz.

2.4 MODIFIED FREQUENCY MODULATION (MFM) RECORDING

Both the RK06 and RK07 drives use a magnetic-recording encoding notation known as modified frequency modulation (MFM). This term refers to the timing and spacing of the recorded magnetic flux reversals. The recorded track may be considered to be divided into a series of equal-length divisions called bit cells. In MFM encoding, the following rules apply.

1. If the bit is a logical 1, a flux reversal is recorded at the center of the cell.
2. If the bit is a logical 0, no reversal is recorded at the center of the cell.
3. Between two consecutive 0s a flux reversal is recorded at the intercell boundary. Cell boundary pulses are recorded to limit the maximum interval between consecutive reversals and to provide timing references for use in data recovery clocking.

Decoding of MFM read data is performed by the controller by opening a logic window in the center of each data cell to determine the absence or presence of a flux reversal. Figure 2-10 illustrates the recording technique.

This method of recording has the advantage of putting at least one flux reversal on the disk for every two bit cells, thereby making it feasible to use phase-locked loop techniques to form a self-clocking data recovery system. Phase-locked loop circuitry maintains a constant bit density despite minor variations in disk speed.

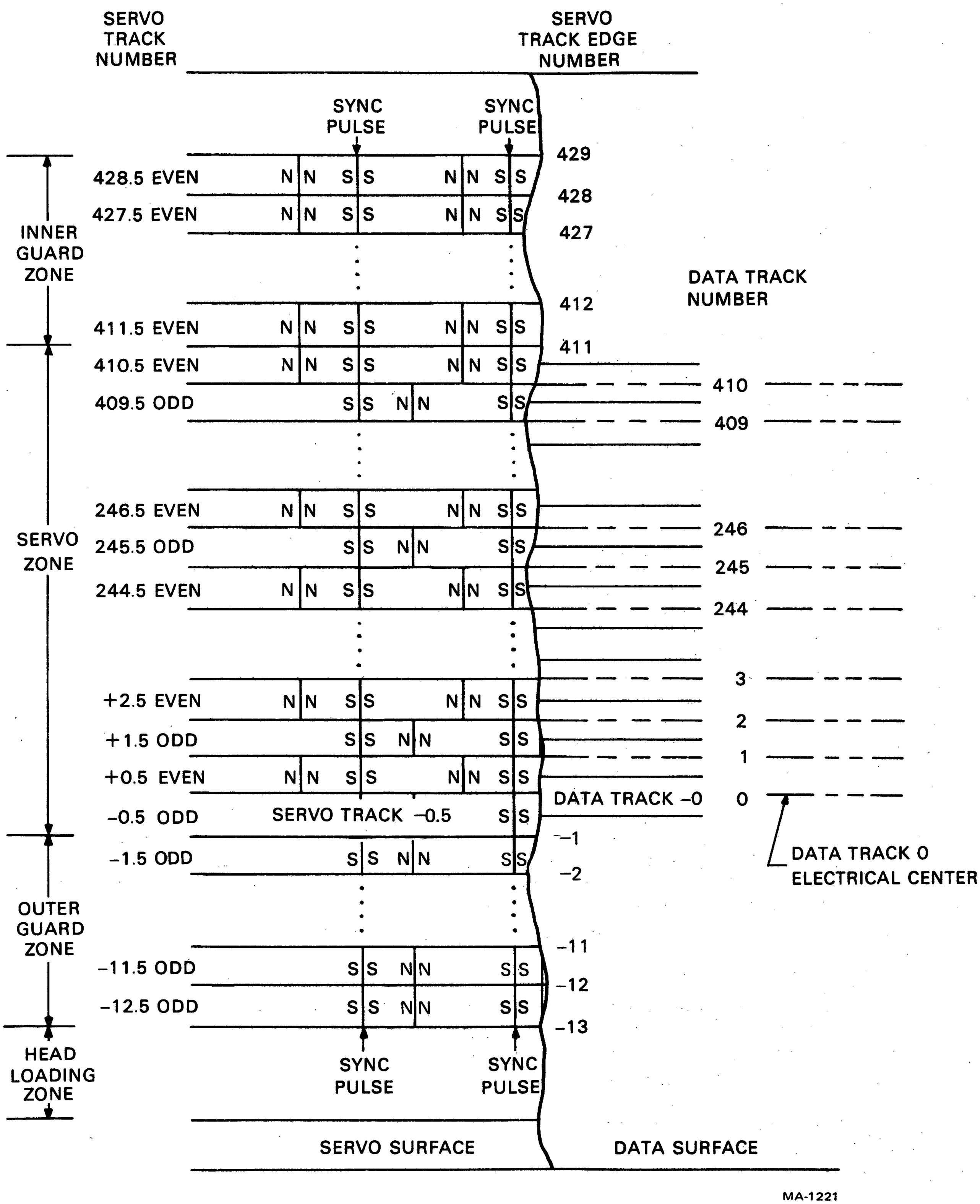


Figure 2-5 Servo Surface Characteristics (RK06K Cartridge)

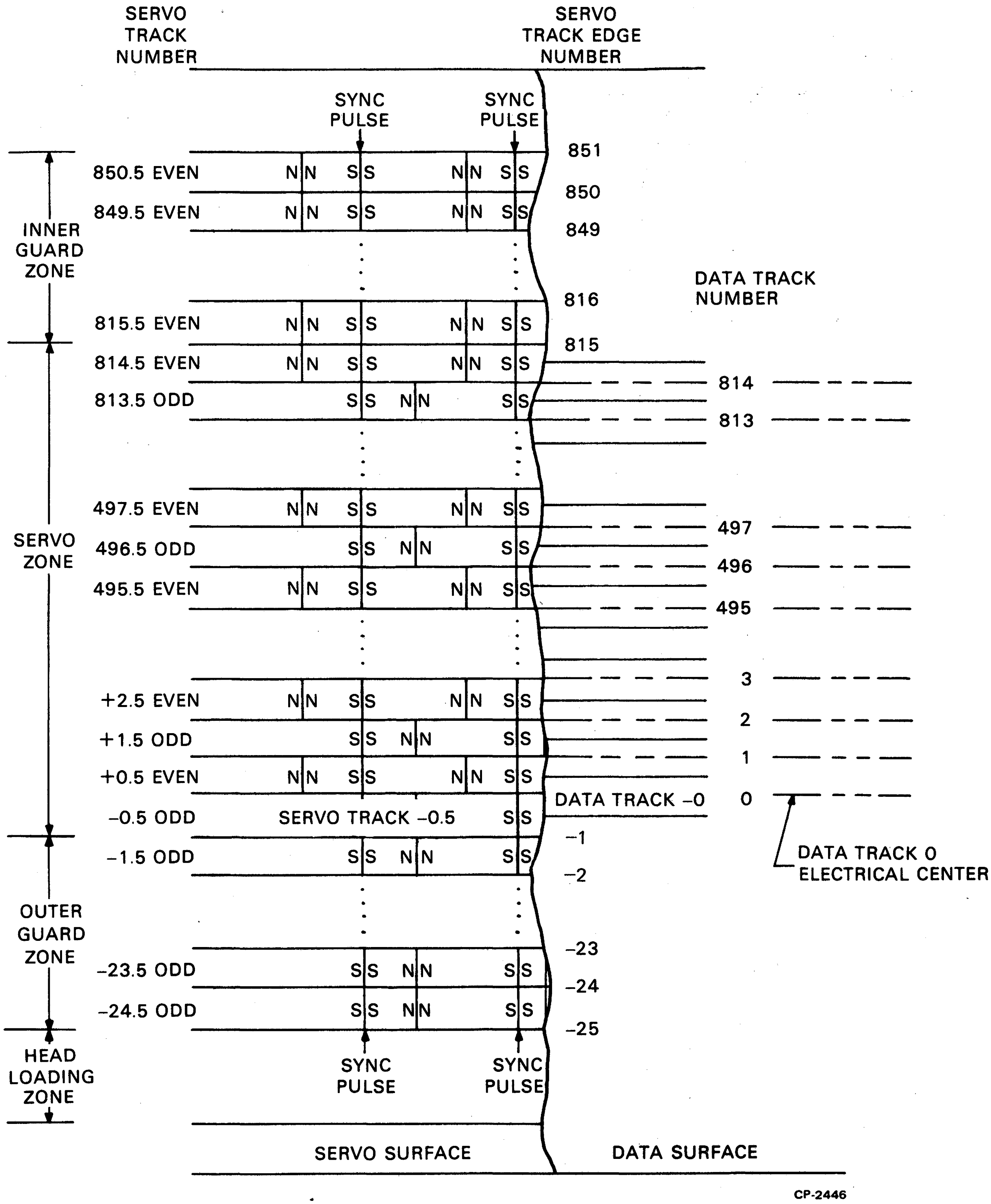


Figure 2-6 Servo Surface Characteristics (RK07K Cartridge)

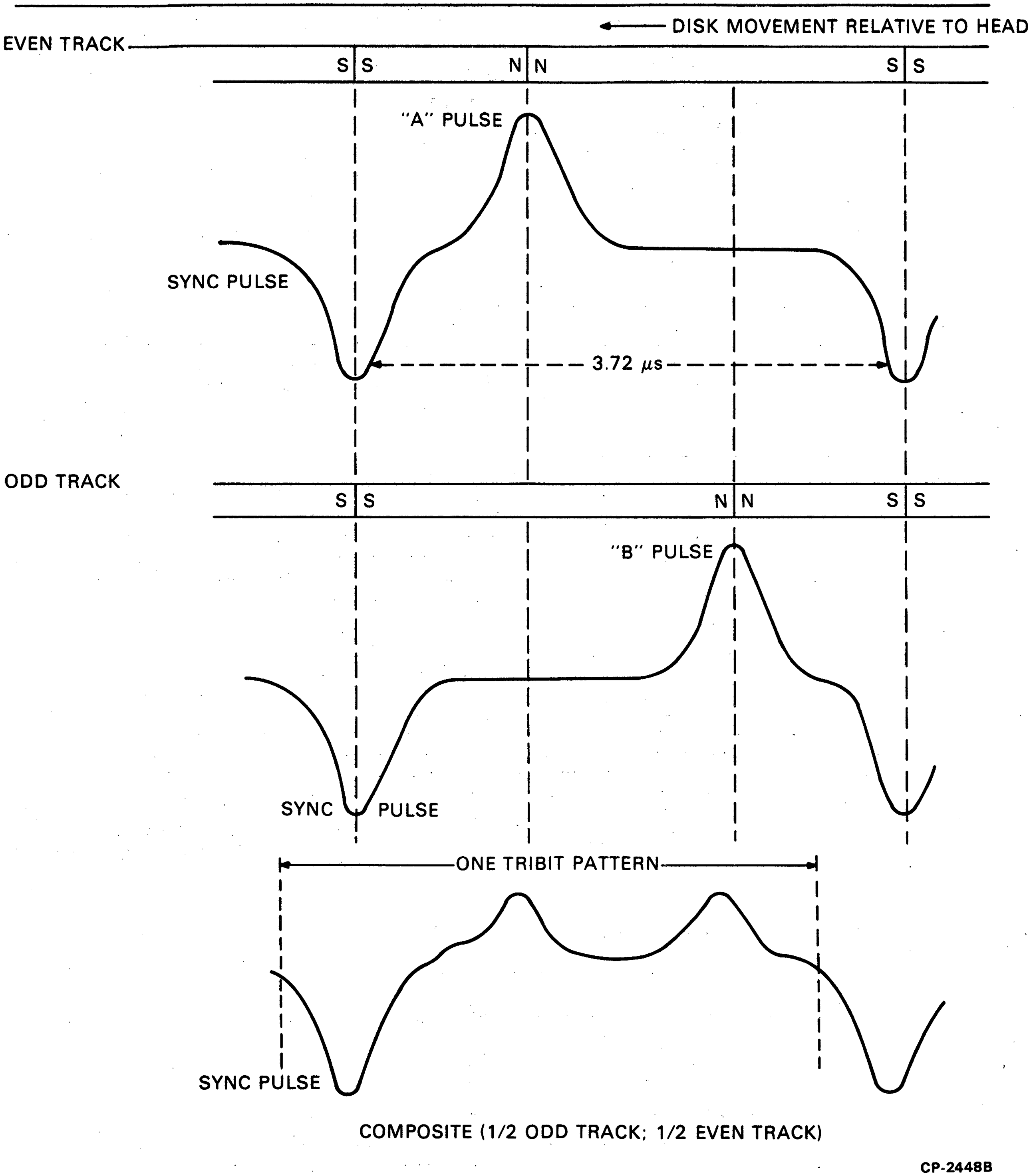


Figure 2-7 Composition of One Tribit Pattern

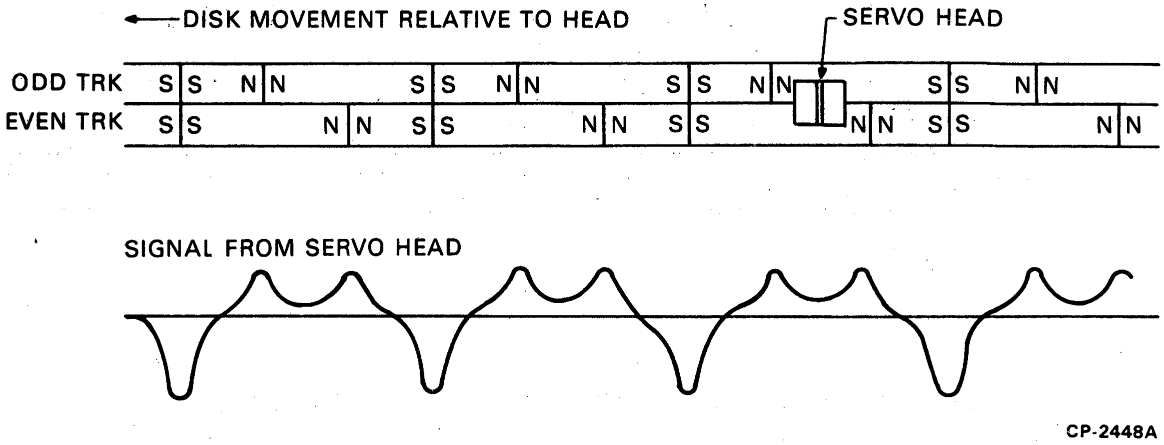


Figure 2-8 Succession of Tribit Patterns

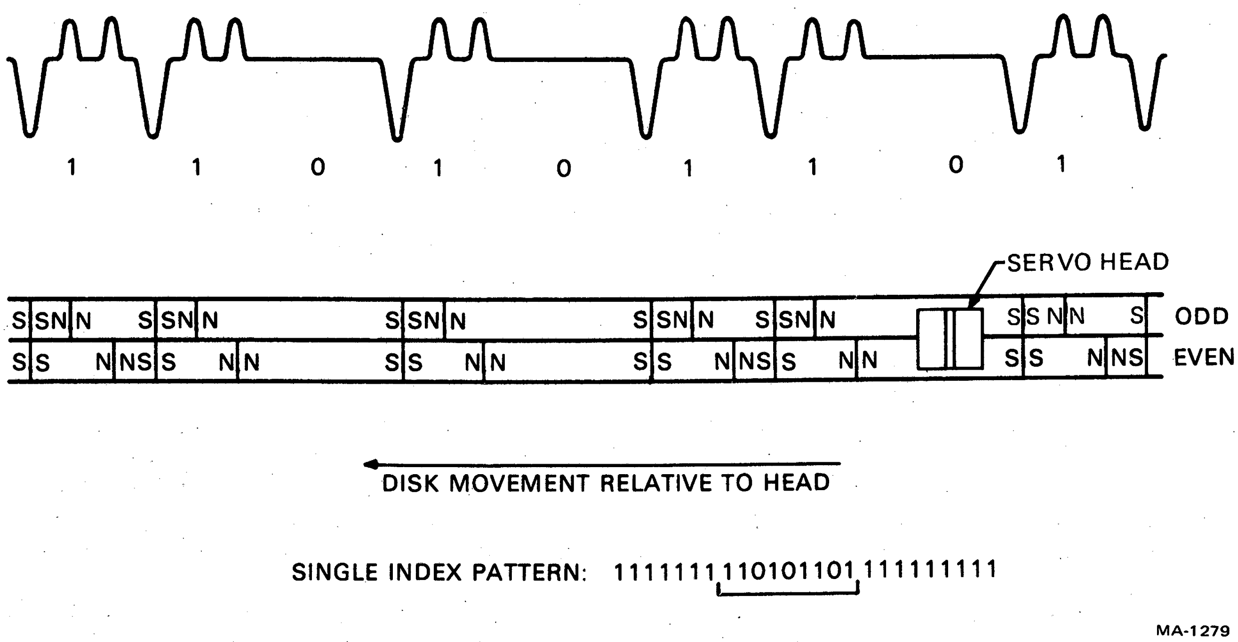


Figure 2-9 Servo Surface Index Pattern

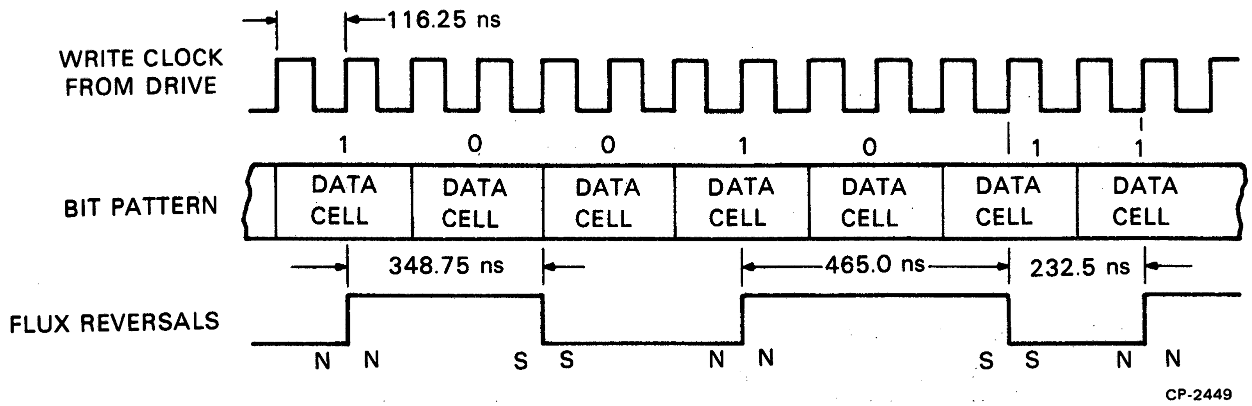


Figure 2-10 Modified Frequency Modulation (MFM) Encoding

2.5 PRECOMPENSATION

One of the problems associated with magnetic recording is a phenomenon called peak shift, wherein flux reversals written on the disk tend to repel one another. Because of this, the flux reversals appear displaced from where they were written. This can cause pattern-sensitive data recovery problems.

To offset the deleterious effect of peak shift, precompensation logic is included in the RK611 controller. This logic displaces certain encoded data pulses by 10 ns in one direction or the other before they are written on the disk, so that the peak shift phenomenon displaces the flux reversals written on the disk to the desired positions.

To determine if an encoded data pulse is to be displaced from its nominal position, the controller will preshift a pulse if and only if the following two conditions are met.

1. The pulse is bounded on one side by a pulse that is not more than one bit cell away.
2. The pulse is bounded on the other side by a pulse that is greater than one bit cell away (for example, 1.5 or 2 bit cells away).

The direction of the preshift depends on the combination of 1s and 0s that precede and/or follow the bit to be preshifted.

The RK611 precompensation algorithm is only concerned with the four conditions illustrated in Figure 2-11. Any other combination of serial data bits does not require preshifting. The algorithm consists of continuously examining a 4-bit pattern (the bit to be written in the current interval; the bit to be written next; and the two immediately preceding bits) and, based on that pattern, either leaving the pulse to be written in its nominal position or advancing or delaying the pulse by 10 ns.

Thus, for the bit pattern 1000 shown in Figure 2-11, the third bit must be preshifted 10 ns to the right (delayed) to compensate for a peak shift to the left. For the bit pattern 0001, the third bit must be preshifted 10 ns to the left (advanced) to compensate for a peak shift to the right, and so forth.

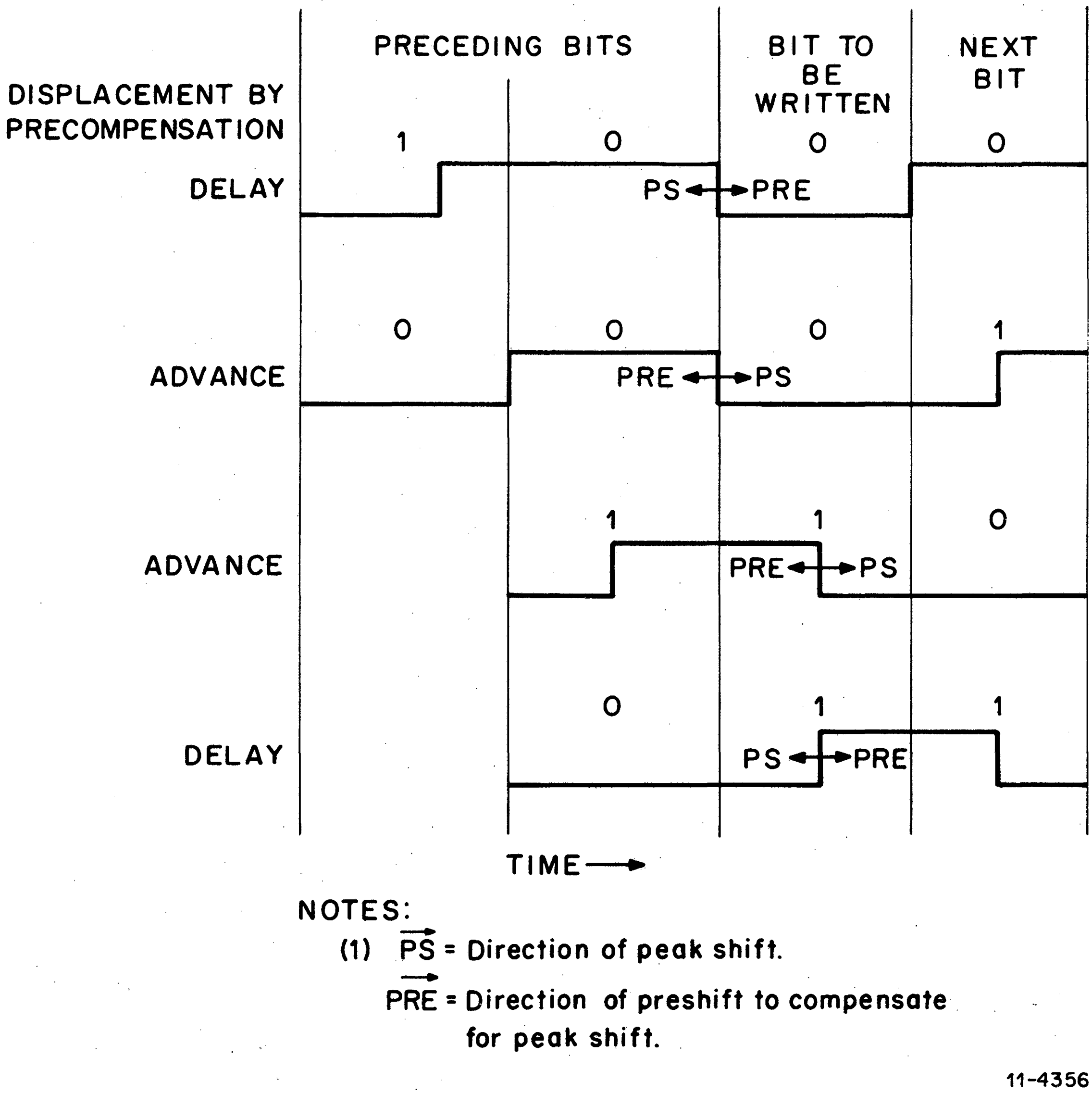


Figure 2-11 MFM Precompensation

CHAPTER 3
INTERFACE-LEVEL THEORY OF OPERATION

Interface communications between the controller and drive(s) are based on a system of serial data and control-signal transmissions involving 17 lines (Figure 3-1). (For dual-access configurations, see Paragraph 3.2.) These lines can be considered in three general categories:

- Bidirectional
- Controller to Drive
- Drive to Controller.

Controller handling of the drive(s) is such that transmission on any of the bidirectional lines is always unidirectional – controller to drive, or drive to controller – at a given time. See Paragraph 4.2.2.4 for command and status message control operation. Signals for drive selection, commands for disk functions, and status reports from drive(s) to controller are all handled serially on the two signal lines labeled Message Line A and Message Line B in Figure 3-1. The remaining lines carry read/write data, timing, control, and attention-flag signals. Message-line formats are illustrated in Figure 3-2, and bit definitions for the 16-bit words are given in Tables 3-1 through 3-10 at the end of this chapter.

3.1 INTERFACE CHARACTERISTICS

All of the interface signals are received or transmitted from the M7706 module. With the exception of the Controller Power On line, all interface lines are line pairs, each consisting of a plus (+) signal wire and a minus (–) signal wire.

The electrical characteristics of the controller/drive interface related to signal timing are discussed below. The components of this interface are the line drivers, line receivers, and a cable.

Line Drivers – The line drivers are devices type 75113 (DEC part no. 19-11341). They are single-input, differential-output devices whose maximum propagation delay is 30 ns.

Line Receivers – The line receivers are devices type 75107B (DEC part no. 19-10268). They are differential-input, single-output devices whose maximum propagation delay time is 25 ns.

Cable – The cable is a round, 20-twisted-pair type with shield and ground. Propagation delay is 5.08 ns/m (1.55 ns/ft), minimum, and 5.74 ns/m (1.75 ns/ft), maximum. A cable connector plug provides the proper strain relief and is capable of being secured to the drive. Figure 3-3 shows the recommended configuration for a bidirectional signal pair. Physical configuration of the controller/drive(s) system is such that the worst-case cable length is 30.5 m (100 ft).

Terminator – The terminator is an assembly in the cable-connector plug. It consists of 82 Ω resistors between each signal line and ground. The terminator is located in the last drive of a daisy-chain bus.

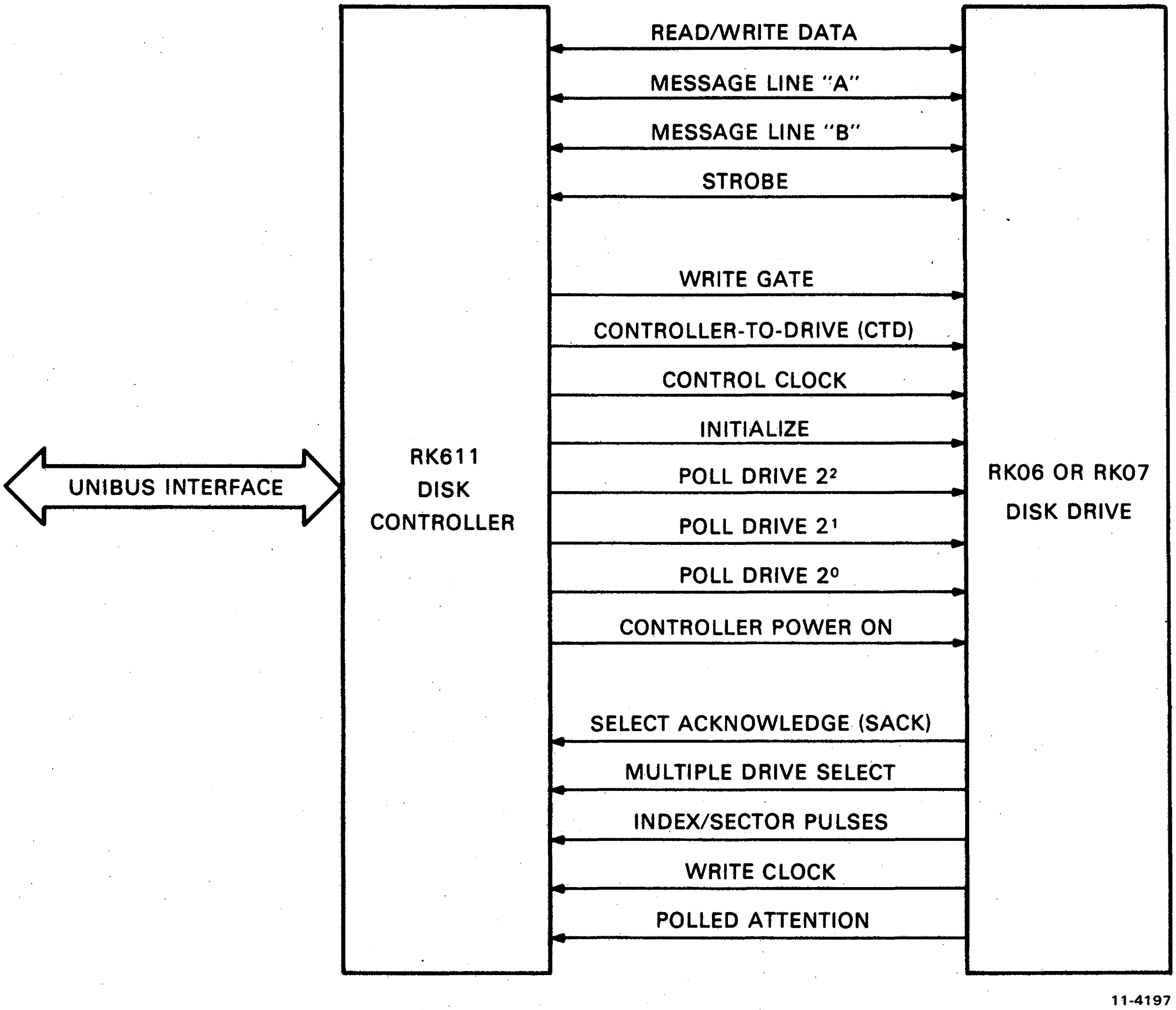
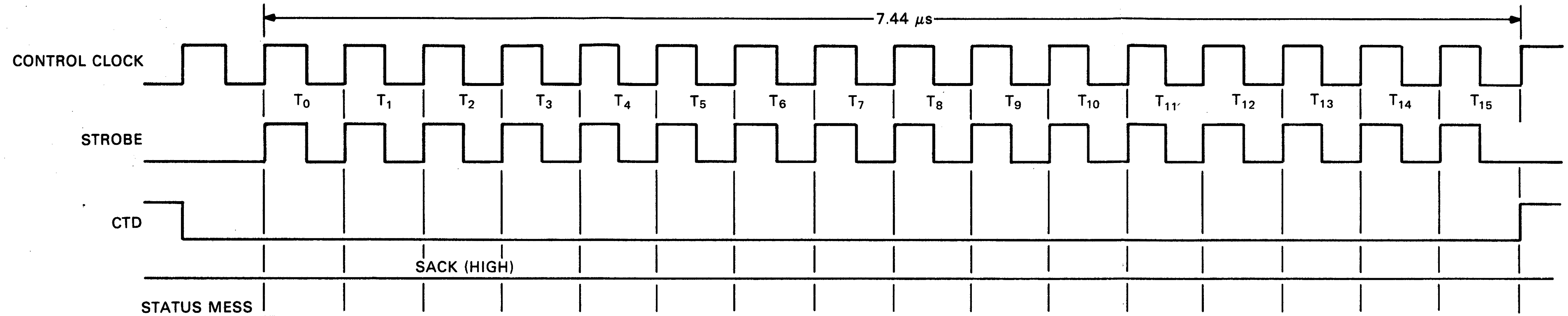


Figure 3-1 Controller/Disk Drive Interface Lines



MESSAGE LINE A

	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
A0	DRIVE SELECT CODE			RESVD		DR AVAIL	VOL VAL	DR READY	TYPE DRIVE	20 SECT FORMAT	OFFSET ON	WR LOCK	SPINDLE ON	PIP	DR STATUS CHANGE	PARITY
A1	DRIVE SELECT CODE			RESVD	SERVO SIGNAL PRES	HEADS HOME	BRUSH HOME	DOOR LTCHD	CART PRES	SPEED OK	FWD	REV	LDG HDS	RTZ	UNLDG HDS	PARITY
A2	DRIVE SELECT CODE			RESVD	CYLINDER DIFFERENCE/OFFSET VALUE									1	RESVD	PARITY
A3	DRIVE SELECT CODE			DRIVE SERIAL NUMBER												PARITY

MESSAGE LINE B

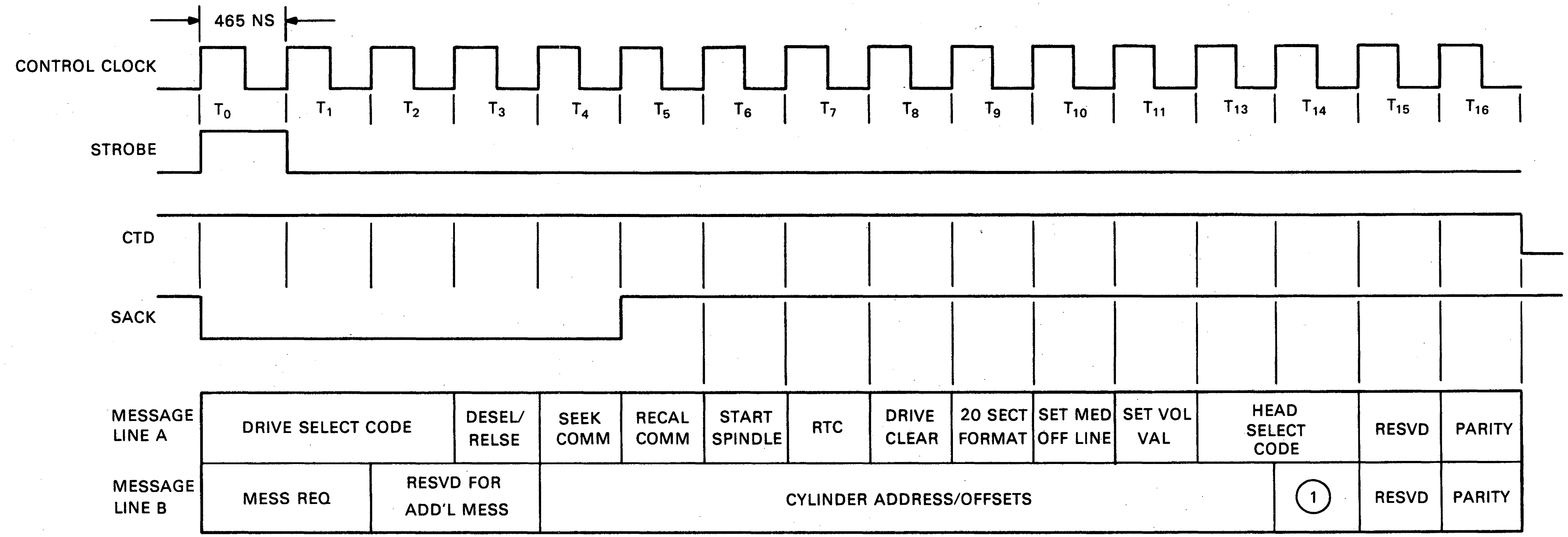
	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
B0	MESS ID (0) (0)		RESVD FOR ADD'L MESS		RESVD	INV ADDR	AC LOW	FAULT	NXF	C-D PRTY ERR	SEEK INC	WR LOCK	SPEED LOSS	DR OFF TRACK	RD/WR UNSAFE	PARITY
B1	MESS ID (1) (0)		RESVD FOR ADD'L MESS		SECTOR ERR	WR CNT & NO WRITE GATE	WRITE GATE & NO TRANS	HEAD FAULT	MULT HD SEL	INDEX ERR	TRIBIT ERR	SERVO SIG ERR	SEEK & NO MOTION	LIM DET ON SEEK	SERVO UNSAFE	PARITY
B2	MESS ID (0) (1)		RESVD FOR ADD'L MESS		CYLINDER ADDRESS									1	RESVD	PARITY
B3	MESS ID (1) (1)		RESVD FOR ADD'L MESS		SECTOR COUNT					DECODED HEAD ADDRESS			RESVD		RESVD	PARITY

a. Controller-to-Drive Transmissions

1 NOTE:
THESE BITS ARE USED ON THE RK07 DRIVE ONLY.

11-4198A

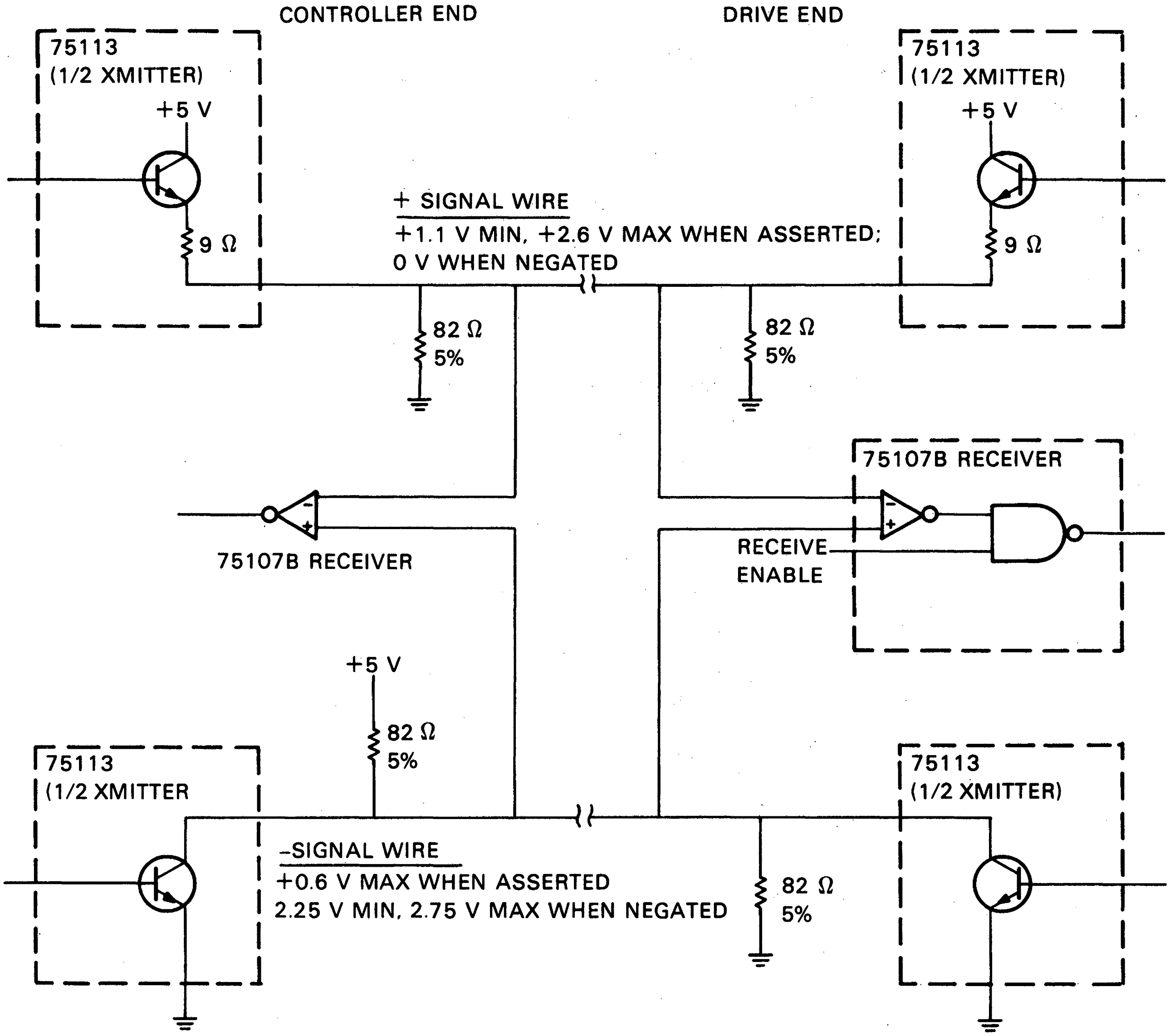
Figure 3-2 Controller/Drive Message Composition and Control Line Timing (Sheet 1 of 2)



b. Drive-to-Controller Transmissions

11-4198B

Figure 3-2 Controller/Drive Message Compositon and Control Line Timing (Sheet 2 of 2)



NOTES:

1. THE 82 OHM RESISTORS AT THE DRIVE END ARE USED AT THE END OF THE DAISY CHAIN ONLY (H870).
2. TRANSMITTER TRANSISTORS ARE TURNED ON WHEN INTERFACE SIGNALS ARE ASSERTED.

Figure 3-3 Recommended Interface Configuration

3.2 INTERFACE LINE DEFINITIONS

The following definitions specify the functions performed by each of the 17 interface lines connecting the controller to the drive(s).

3.2.1 Bidirectional Lines

The bidirectional lines are:

- Read/Write Data
- Message Line A
- Message Line B
- Strobe.

Read/Write Data – This line carries encoded digital read data from the drive to the controller, and encoded digital write data from the controller to the drive(s).

Read Data – Read data is transmitted to the controller under the following enabling conditions.

1. Power supply voltages are within specifications.
2. Write Gate is negated.
3. The drive is ready (i.e., detented).
4. The drive is available on this port.

Write Data – For the drive to accept write data, the Write Gate must be asserted, and the five conditions for the acceptance of the Write Gate must be met. Figures 3-4 and 3-5 show the timing relationships for the write execution.

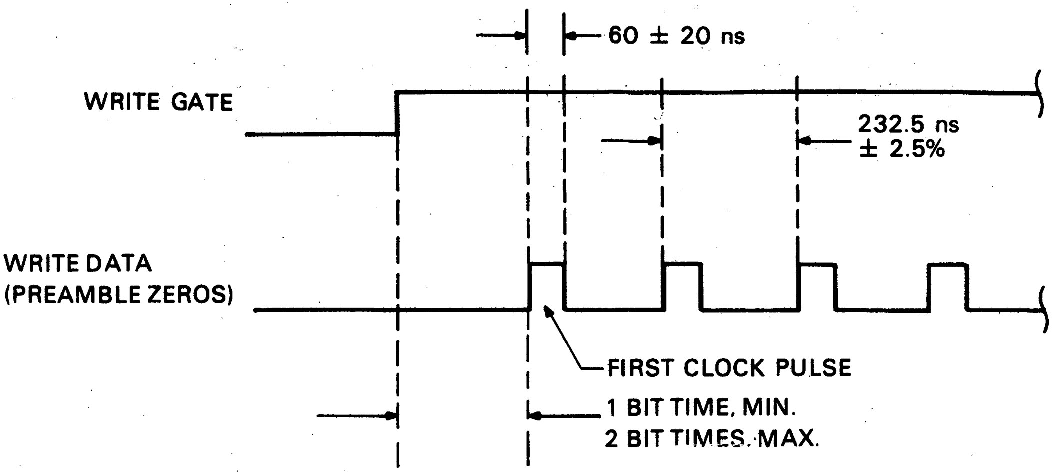
Message Line A – This signal line transmits drive selection, commands, and head-select data in 16-bit serial format from controller to drive(s). At the time of the drive selection determination, all other drives are inhibited from receiving the remainder of the transmission. Data from the selected drive is transmitted to the controller as one of four possible (controller-commanded) 16-bit messages. In both directions, the transmission is in the order of T0 to T15.

Controller-to-Drive Transmissions – Table 3-1 defines the bits comprising the data word transmitted from controller to drive on Message Line A.

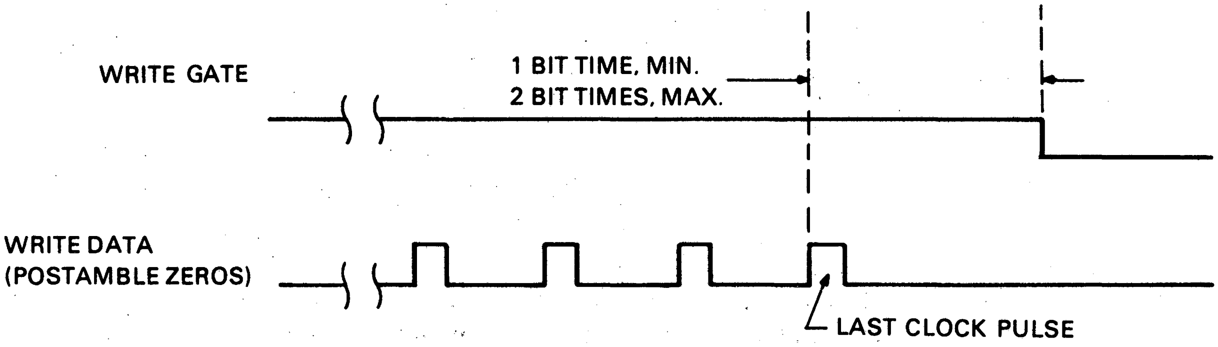
Drive-to-Controller Transmissions – Tables 3-2 through 3-5 give bit definitions for messages A0 through A3, respectively, as requested by the controller on Message Line B (Figure 3-2). As is seen, the state of bits T0 and T1 determines which of the four sets of status messages is transmitted from the selected drive to the controller when CTD Controller-to-Drive (CTD) is made low.

Message Line B – This signal line transmits cylinder addresses, offset commands, and status-message requests from the controller to the drive in 16-bit serial format. As in the case of Message Line A responses to controller commands for status reporting, data from the selected drive is transmitted in the form of the 16-bit message (B0, B1, B2, or B3; see Figure 3-2). In both directions, transmitted messages are in the bit order of T0 through T15.

Controller-to-Drive Transmissions – Table 3-6 defines the bits comprising the data word transmitted from controller to drive on Message Line B. This table is an expansion of the summary data shown in Figure 3-2.



a. Write Start Timing



b. Write Stop Timing

CP-2453

Figure 3-4 Write Gate and Write Data Timing

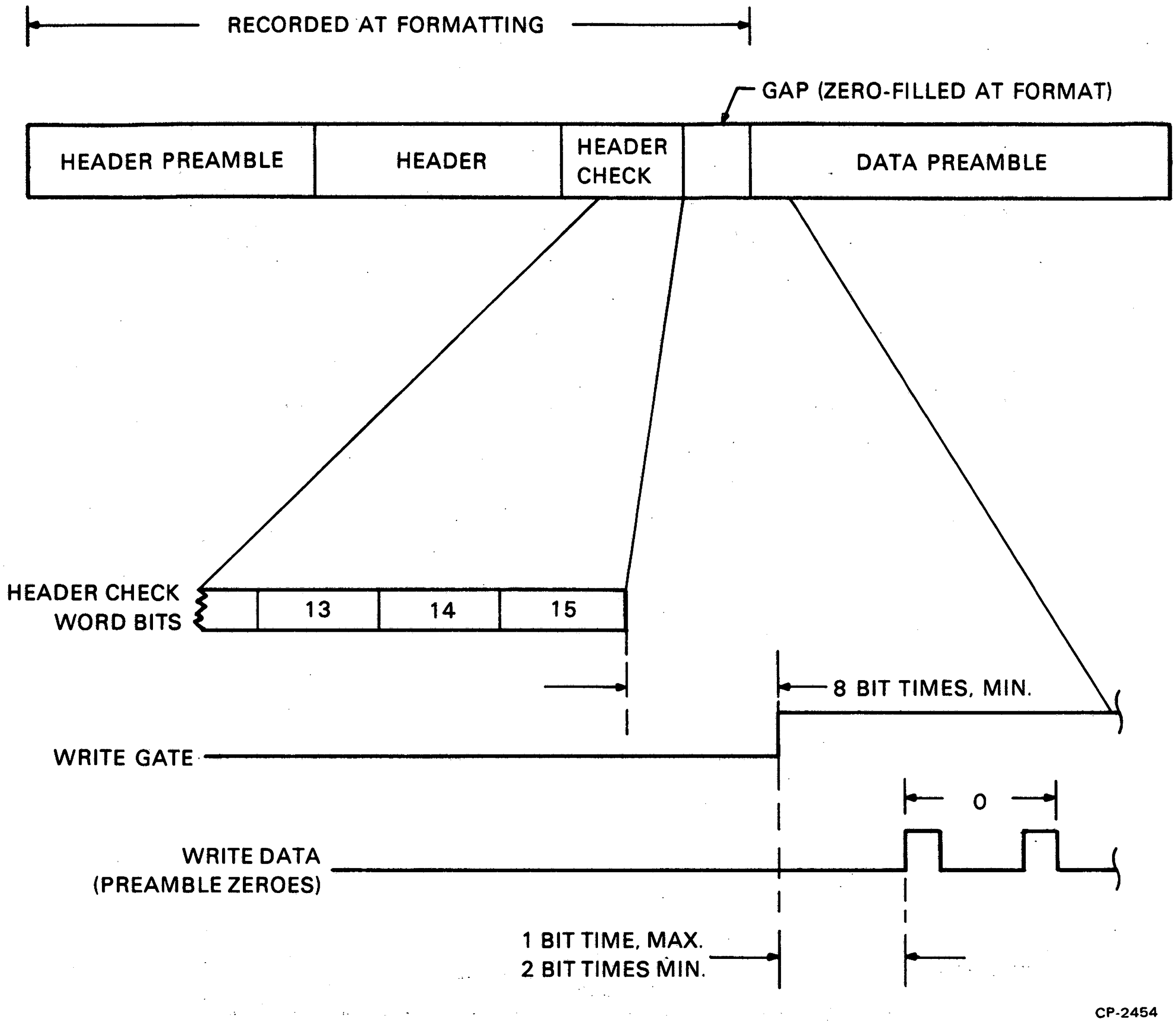


Figure 3-5 Write Header and Write Data Preamble Format

Drive-to-Controller Transmissions – Tables 3-7 through 3-10 give bit definitions for messages B0 through B3, respectively, as requested by the controller on Message Line B (Figure 3-2). As is seen, the state of bits T0 and T1 indicates which of the four sets of status messages is transmitted from the selected drive to the controller when CTD is made low. T0 through T15 is the order of transmission (Figure 3-2).

Controller-to-Drive Strobe – When initiating a transmission on Message Lines A and B, the controller asserts this signal (of one control clock period duration) whose purpose is: (1) to enable the drives to accept their specific drive-select codes, and (2) to serve as a synchronizing signal for the logic circuits.

Drive-to-Controller Strobe – When originated by a selected drive in conjunction with Message Lines A and B status reports, one strobe pulse is sent with each message bit to clock the information to the controller. This format sequence is required in order to eliminate the problem of propagation delay time associated with the Control Clock signal transmitted on the interface to the drives. As implemented, data is accepted by the controller, using the Strobe from the drive to clock and synchronize the transmission. The Strobe signal generated by the controller must be preceded by the assertion of the CTD signal not less than one clock pulse earlier.

3.2.2 Controller-to-Drive Interface Lines

The Controller-to-Drive (CTD) lines are:

- Write Gate
- Controller-to-Drive
- Control Clock
- Initialize
- Poll Drive 2^2
- Poll Drive 2^1
- Poll Drive 2^0
- Controller Power On.

Write Gate –When asserted, with all enabling conditions met, this signal turns on write current in the selected drive. The enabling conditions are:

1. Drive selection has been made.
2. Volume valid (bit T6 of status message A0) is set.
3. No read/write–unsafe condition exists in the drive.
4. Drive-off-track error is not asserted.
5. Drive is not in write-protect mode.

The timing relationships between write gate and write data pulses are shown in Figures 3-4 and 3-5. It will be noted that all recording begins with an all-zero preamble and terminates in an all-zero postamble.

Controller-to-Drive (CTD) – When asserted, this line enables the transmission of data from controller to drive. CTD precedes any strobe from the controller by a minimum of one clock cycle and remains asserted for a minimum of 16 clock cycles. When CTD is negated, the selected drive reports status information to the controller on both message lines simultaneously, using the specific message formats requested by the controller (Figure 3-2).

Control Clock – The controller's Control Clock runs continuously. It is used by the drives for clocking the reception and the control of data originated by the controller. The clock period is 465 ns ± 2.5 percent at a 50 percent duty cycle. With this duty cycle, data setup time is during the first half of the cycle and its clocking is during the second half of the cycle.

Initialize – When asserted, this line deselects all drives, resets all error conditions (assuming there are no errors), and clears the drive status-change flip-flop. The minimum pulse width for this signal is 60 ns.

Poll Drive – 2^2, 2^1, and 2^0 – These binary-encoded drive-address lines are used to poll each drive for its attention status. The polling mechanism operates independently of the serial transmissions and polls all drives in the chain, whether selected or not. The drive poll function permits the system to determine in a short time which of the drives has asserted attention without serially selecting each drive in sequence. The polling rate (time to poll each drive) is 930 ns.

Controller Power On – This single-ended line, when asserted, indicates that the controller has power and that the physical (cable) connection between controller and drive is established. If this signal is negated, all drives are deselected and the receivers for Strobe and Control Clock lines are disabled to prevent erroneous drive selection as a result of noise signals from the interface. When asserted, the Controller Power On line is at a nominal potential of 0.4 V and the transistor switch at the controller end of the line is closed to ground. When negated, the line is an open circuit; i.e., the switching transistor is off. Each drive then biases this line to +3 V through a diode-resistor network to provide a reference for the drive-sensing circuits.

3.2.3 Drive-to-Controller Interface Lines

The Drive-to-Controller (DTC) lines are:

- Select Acknowledge (SACK)
- Multiple Drive Select
- Index/Sector Pulses
- Write Clock
- Polled Attention.

Select Acknowledge (**SACK**) –This line reflects the state of the SACK flip-flop on the M7706 module. It is asserted following the last of the four bits comprising the drive-selection code. Assertion is within 300 ns after receipt of bit T5 in the controller's message to the drive. It is negated within 100 ns after receipt of another Strobe.

Multiple Drive Select – This signal reflects the state of the multiple drive select flip-flop on the M7706 module. It is asserted whenever more than one drive in a system responds to a select code simultaneously. Each selected drive monitors the Index/Sector Pulse line to detect the presence of extraneous pulses originating at other selected drives. If the drive detects pulses other than its own, Multiple Drive Select is asserted. Since index and sector pulses are not generated if the heads of a selected drive are not loaded, this condition causes that drive to transmit control clock pulses on the Index/Sector Pulse line. If another drive is simultaneously selected, it detects these pulses and interprets a multiple drive selection condition to exist. The Multiple Drive Select signal is guaranteed to be at the drive interface within 300 ns after receipt of a Sector/Index Pulse line from another drive, and is negated within 120 ns after receipt of another Strobe.

Index/Sector Pulses – This signal line transmits the once-per-revolution index pulses and pulses originating at each sector boundary. This line is also used in the determination of multiple drive selection. (See Multiple Drive Select definition in preceding paragraph.)

Index/Sector Pulses are enabled when the drive asserts SACK (select acknowledge), and remain enabled until the drive is deselected. This implementation prevents communications discontinuities during the drive-selection interval when the same drive is to remain selected. Details of sector format (as these affect pulse characteristics and timing for this line) are given in Chapter 4 (for the RK06) and in Chapter 5 (for the RK07) of this manual and in relevant sections of the *RK611 Controller Technical Description Manual* (EK-RK611-TM-002).

Write Clock – This signal is used in clocking write data to the drive. Derived from tribit information on the servo surface of the drive, this signal ensures constant bit-density recording on the data surface. The Write Clock signal is a pulse train of 116.25 ns (± 2.5 percent) with a 50 percent duty cycle.

Polled Attention – This line is enabled whenever a drive status change occurs. The attention indication is not transmitted to the controller until the drive unit number (number on the plug of the unit select switch on the operator's control panel of the drive) is polled by the controller through the three Poll Drive Interface lines (Figure 3-1 and Paragraph 3.2.2). Attention will be reported each time the drive is polled until the drive status-change flip-flop is reset. (See message A0, T14 in Figure 3-2b and Table 3-2.) This signal is guaranteed at the drive interface no later than 400 ns after detection of the polling address for the drive, and guaranteed removed within 160 ns after the polling address is removed.

3.3 OFF-LINE MAINTENANCE

Isolation of a drive within a system can be effected without disturbing the daisy-chain. This is done by releasing that access switch which, at the time, is enabling drive communication. If the drive is a single-access unit, an exerciser may then be connected to the other set of input/output connectors. Drive power is interrupted in order to relocate interface and timing module M7706 to the alternate access slot. After power is reapplied, the other access enable switch is depressed and off-line maintenance can take place. However, with dual-access configurations, this type of off-line maintenance requires breaking the daisy-chain associated with one of the accesses.

NOTE
A terminator must be installed at the output connector of the drive port associated with the field test box.

Table 3-1 Message Line A Bit Definitions
Controller-to-Drive Transmissions

Clock Period	Description
T0–T2	**Drive-Select Code** A 3-bit drive-select code in binary-encoded form is transmitted with the least significant bit first. These bits are shifted into the BUFF 1, BUFF 2, and BUFF 3 flip-flops on the M7706 module. All drives on the controller/drive bus receive these bits. At the drive's T2 time, a comparison of these bits and the encoded drive number from the unit select plug is accomplished. If a comparison occurs, the drive remains selected. All other drives are deselected at this time.
T3	**Deselect/Release** This command sets the "drive available" status to the other controller in dual-access configurations (Paragraph 3.2). The drive is also deselected with this bit asserted. This bit is loaded into the BUFF 1 flip-flop on the M7706 module of the selected drive. It is gated with the drive's T3 timing pulse in order to deselect the drive.
T4	**Seek** This command directs the drive to seek to the cylinder address transmitted on Message Line B. The T4 bit, when asserted coincident with no positioning in progress and volume valid set, sets the seek command flip-flop on the M7707 module (RK06) or M7907 (RK07), which in turn, enables the new cylinder address and cylinder differencing to occur.

Table 3-1 Message Line A Bit Definitions
Controller-to-Drive Transmissions (Cont)

Clock Period	Description
T5	**Recalibrate** This command directs the drive to seek to cylinder number 0 at low velocity and to reset the cylinder address register. This command also resynchronizes the drive position with the drive electronics if, for any reason, the two are out of step. The recalibrate operation is described in Paragraph 4.3.2.3. (RK06) and Paragraph 5.3.2.3 (RK07).
T6	**Start Spindle** This command directs the drive to start its spindle and, subsequently, to perform a brush cycle and load the heads if, and only if, the RUN/STOP switch on the front panel is depressed. It may also be used to restart a drive in the event that a set medium off-line command has unloaded the heads, or if any of the error conditions that unload the heads has occurred. In that case, the error must be cleared before this command will allow the heads to reload. This T6 bit, through BUFF 1 on the M7706 module, sets a flip-flop on the M7705 module, which in turn sets the run flip-flop if the RUN/STOP switch is depressed and the interlocks are asserted.
T7	**Return-to-Centerline Command (RTC)** This command is used for resetting head offsets whenever a write operation is to take place. The clearing of offset mode requires 3 ms to complete, at which time a Drive Attention signal is transmitted to the controller. An RTC is implied by any non-zero cylinder seek or upon detection of a Write Gate in the event that an RTC command is not detected. The RTC flip-flop is on the M7707 module (RK06) or M7907 module (RK07); when set, this flip-flop controls the RTC operation.
T8	**Drive Clear** This bit, when asserted, clears the drive status change flip-flop as well as all error flags in the selected drive (provided that the errors no longer exist).
T9	**20-Sector Format Select** This bit, when asserted, selects 20 sector pulses per disk revolution; when not asserted, 22 sector pulses are selected. Twenty sectors correspond to 18-bit data words; twenty-two sectors correspond to 16-bit data words. Whenever a change in the format is made with this select bit, sector pulses cease until the next sector 0 occurs, at which time the drive is synchronized to the new format. Reference Paragraph 4.2.2.3 (RK06) or Paragraph 5.2.2.3 (RK07) for implementation.

Table 3-1 Message Line A Bit Definitions Controller-to-Drive Transmissions (Cont)

Clock Period	Description
T10	**Set Medium-Off Line** This bit, when asserted, unloads the drive heads and stops the spindle. It also resets a flip-flop on the M7705 module, which in turn causes the heads to unload and, subsequently, to deenergize the spindle.
T11	**Set Volume Valid** This bit, when asserted, sets the volume valid flip-flop on the M7706 module, thereby acknowledging a power turn-on, change of cartridge, or the removal of the unit select plug. This bit must be set in order to perform a write or a seek function.
T12, T13	**Head-Select Code** A 2-bit head-select code in binary-encoded form is transmitted at these clock times with the least significant bit (LSB) first. The seek command bit must be asserted in order to load these head addresses into flip-flops on the M7707 module (RK06) or the M7907 module (RK07). A decoder on the output of the head-address flip-flops provides decoded enable lines to the read/write module. If both head-address bits are set, thereby designating head-address 3, the decoder for this head address is an input to the invalid address circuitry.
T14	This bit is reserved; it is a logic 0.
T15	**Parity** T15 is the parity bit. Its state will be such that the number of logic 1s in the 16-bit transmission is odd. Parity checking circuitry is provided in the M7706 module for both message lines. See Paragraph 4.2.2.5 (RK06) or Paragraph 5.2.2.5 (RK07) for detailed operation.

Table 3-2 Status Message A0 Bit Definitions Drive-to-Controller Transmissions*

Clock Period	Description
T0–T2	**Selected-Drive Address** The binary-encoded address for the selected drive is transmitted as an identification of the drive, the LSB being transmitted first. These bits (T0–T2) are generated by the contacts of the unit select plug.
T3, T4	No data is transmitted. Consequently, these bits will be logic 0s.
T5	**Drive Available** This bit, when asserted, indicates that the drive is not conducting any operations with another controller. It is for use in dual-access configurations. In single-access configurations, it is always asserted.
T6	**Volume Valid (Vol. Val.)** This bit is reset by changing a cartridge, removing power, or removing the unit select plug. It is set by a transmission from the controller. If reset, it is an indication to the system that the cartridge may have been changed. The volume valid flip-flop is located on the M7706 module.
T7	**Drive Ready** This bit, when asserted, reports that the drive is detented on a cylinder and can receive any command from the controller except in a dual-access configuration where the drive must also be available to this interface channel. The drive ready flip-flop is located on the M7705 module and is set by the trailing edge of the settling pulse. Reset occurs when: (1) heads unload, (2) at the start of a seek, or (3) offset mode is started or cleared.
T8	**Drive Type** This bit is designated for transmission of the disk drive type. For the RK06, it is a logic 0 and for the RK07, it is a logic 1.
T9	**Drive Format** This bit designates that the drive is in either the 16- or 18-bit read/write mode and, correspondingly, has 22 or 20 sectors per rotation, respectively. When asserted, 18-bit words (20 sectors/rotation) are indicated. This bit reflects the state of the 20-sector-format flip-flop on the M7705 module.
T10	**Offset On** This bit indicates that an offset command has been issued to the drive and that the offset has been enabled; it reflects the state of the offset flip-flop on the M7707 module (RK06) or the M7907 module (RK07). The offset flip-flop is set at T14 time of the controller-to-drive transmission if there is no seek command, and the B message line was asserted at T11 and T12 times. It is reset by an RTC command, the receipt of Write Gate, or a positioner move.

* All status message A0 bits are multiplexed by multiplexer A0 on the M7706 module.

Table 3-2 Status Message A0 Bit Definitions
Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T11	**Write Lock** This bit, when asserted, reports that the drive is in write lock condition (i.e., is write protected). It reflects the state of the write lock flip-flop on the M7705 module. This flip-flop is set by the write protect switch when Write Gate is not asserted and is reset upon release of the write protect switch.
T12	**Spindle On** This bit, when asserted, indicates that the selected drive's spindle is energized. It reflects the state of the run flip-flop on the M7705 module.
T13	**Positioning in Progress** This status bit, when asserted, is used to indicate that a seek is occurring. It is generated on the M7705 module and is the coincidence of Drive Ready being reset and Heads Not Home.
T14	**Drive Status Change** This bit is the logic OR of any status change in the selected drive. This status bit is the signal transmitted on the interface bus when the drive is polled for attention. The following conditions cause a drive status change: (1) the completion of a seek, offset, or offset clear operation, (2) unloading of heads, or (3) any fault condition. Any of these changes sets the drive status change (DSC) flip-flop on the M7706 module. This flip-flop is cleared by the drive clear command, initialize, power-up reset, or the RUN switch reset. Refer to Paragraph 4.8 for a description of the operation for drive status change in dual-access systems.
T15	**Parity** This bit determines odd parity for this drive-to-controller transmission. It is generated on the M7706 module. See Paragraph 4.2.2.5 (RK06) or Paragraph 5.2.2.5 (RK07) for details. All messages generate a parity bit in this same manner.

* All status message A0 bits are multiplexed by multiplexer A0 on the M7706 module.

Table 3-3 Status Message A1 Bit Definitions Drive-to-Controller Transmissions*

Clock Period	Description
T0–T2	**Selected Drive Address** The selected drive binary-encoded address is transmitted as an identification with the LSB first. It reflects the number on the unit select plug.
T3	Not used; it is a logic 0.
T4	**Servo Signal Present** This bit, when asserted, indicates that the drive heads are loaded and located between the outer and inner limits. It also indicates that servo signals from the servo surface are being detected. This signal is generated on the M7708 module (RK06) or M7908 module (RK07).
T5	**Heads Home** This bit, when asserted, indicates that the heads are unloaded and at the home position. It is generated by the home switch, which senses when the positioner is fully retracted.
T6	**Brushes Home** This bit, when asserted, indicates that the disk cleaning brushes are at their home position. It is generated by the brushes-home switch of the brush assembly.
T7	**Door Latched** This bit, when asserted, indicates that the cartridge access door is latched. It is generated by the lid locked switch on the lid-latching assembly.
T8	**Cartridge Present** This bit, when asserted, indicates that a cartridge is present and is seated properly in the drive. It is generated by the cartridge present switch on the shroud assembly.
T9	**Speed O.K.** This bit, when asserted, indicates that the disk spindle rotational speed is safe for head loading. It is set at a nominal 85 percent of 2400 rev/min and is generated by circuits on the M7705 module. See Paragraph 4.2.1.2 (RK06) or 5.2.1.2 (RK07) for details.
T10	**Forward** This bit, when asserted, indicates that the servo has been enabled to move in a forward direction (toward the spindle). It reflects the state of the forward flip-flop on the M7707 module (RK06) or M7907 module (RK07). See Paragraph 4.3.1.8 (RK06) or 5.3.1.8 (RK07) for details.

* All bits of the A1 message are multiplexed by multiplexer A1 on the M7707 (RK06) or M7907 (RK07) module.

Table 3-3 Status Message A1 Bit Definitions
Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T11	**Reverse** This bit indicates that the servo has been enabled to move in a reverse direction. It reflects the state of the reverse flip-flop on the M7707 module (RK06) or M7907 module (RK07). See Paragraph 4.3.1.8 (RK06) or 5.3.1.8 (RK07) for details.
T12	**Heads Loading** This bit, when asserted, indicates that the heads are in the process of loading. It reflects the state of the LD HDS flip-flop on the M7707 module (RK06) or M7907 module (RK07). In the head loading routine, the heads advance forward until the inner limit is detected. During this time, this bit is asserted. Upon detection of the inner limit, this bit is reset, and the RTZ bit (reported at T13 time) is asserted. See Paragraph 4.3.1.7 (RK06) or 5.3.1.7 (RK07) for details.
T13	**RTZ (Return to Zero)** This bit, when asserted, indicates that a recalibrate operation is underway. It reflects the state of the RTZ flip-flop on the M7707 module (RK06) or M7907 module (RK07). A recalibration takes place upon command from the controller, or upon detection of inner limit while loading the heads. When (as mentioned above) the inner limit is reached during head loading, the heads move in a reverse direction until the outer limit is sensed. At this time, the carriage reverses and moves forward, stopping at cylinder 0. When the carriage settles on cylinder 0, this bit is cleared.
T14	**Unloading Heads** This bit, when asserted, indicates that the heads are unloading and are not at the home position. It is generated on the M7707 module (RK06) OR M7907 module (RK07).
T15	**Parity** This bit determines odd parity for this 16-bit message. It is generated on the M7706 module. See Paragraph 4.2.2.5 (RK06) or 5.2.2.5 (RK07) for details.

* All bits of the A1 message are multiplexed by multiplexer A1 on the M7707 (RK06) or M7907 (RK07) module.

Table 3-4 Status Message A2 Bit Definitions Drive-to-Controller Transmissions*

Clock Period	Description
T0–T2	**Selected Drive Address** The selected drive binary-encoded address will be transmitted as an identification with the LSB first. It reflects the number of the unit select plug.
T3	This bit is reserved. It is a logic 0.
T4–T13	**Cylinder Difference/Offset Position** During a seek (seek command in CTD Message Line A is high), these bits represent the binary-encoded cylinder difference between the current cylinder address and the new cylinder address received from the controller. In the RK06, only bits T4–T12 are used, and T13 is reserved. In the RK07, all ten bits (T4–T13) are used. The register of nine bits (RK06) or ten bits (RK07) originates on the M7707 module (RK06) or M7907 module (RK07), respectively. When the positioner is in detent on a cylinder (and seek command in CTP Message Line A is low), bits T4–T9 represent the magnitude of the offset; bit T10 represents the direction (T10 - 1 is the "+" or forward direction); and T11 and T12 are both high (indicating offset mode). T13 is a don't-care in the offset mode. When these bits represent offset status, they are inverted from the input offset bits. This difference is invalid if the drive is seeking and a track crossing count occurs during the transmission of this count.
T14	This bit is reserved. It is a logic 0.
T15	**Parity** This bit determines odd parity bit for this 16-bit message.

* These bits are routed via multiplexer A2 on the M7707 (RK06) or M7907 (RK07) module.

Table 3-5 Status Message A3 Bit Definitions Drive-to-Controller Transmissions*

Clock Period	Description
T0–T2	**Selected Drive Address** The binary-encoded address of the selected drive is transmitted for drive identification with the LSB first.
T3–T14	**Drive Serial Number** These 12 bits are used to report the three least significant digits of the drive's serial number. This identification is reported in BCD form with the least significant digit first and the LSB of each digit first. It is used for error-logging purposes. The 12 bits are generated by hardwiring the code on the wire-wrapped backplane.
T15	**Parity** This bit determines odd parity for this 16-bit transmission.

* These bits are routed via multiplexer A3 on the M7707 (RK06) or M7907 (RK07) module.

Table 3-6 Message Line B Bit Definitions
Controller-to-Drive Transmissions

Clock Period	Description
T0–T1	**Message Request** The state of these bits establishes which of four sets of status messages are transmitted from the selected drive to the controller when CTD is low. T0 represents the LSB. These bits are loaded into the byte 0 and byte 1 flip-flops on the M7706 module.
T2, T3	These bits are reserved; both are logic 0s.
T4–T12	**Cylinder Address/Offset Command** These data bits represent (when a seek command is asserted on Message Line A) the desired cylinder address with the LSB transmitted first and in binary form. For this case, the nine bits (RK06; T13 not used) or ten bits (RK07) of data are loaded into the cylinder address register on the M7707 module (RK06) or M7907 module (RK07), respectively, and applied to the serial differencer simultaneously for cylinder differencing. When the seek command and recalibrate bits are low on Message Line A, and Message Line B is true at T11 and T12 time, an offset command is generated with these bits. The codes for the different offsets follow.

Command T12	Command T11	Direction* T10	Magnitude T9	T8	T7	T6	T5	T4	Offset Value (microinches) RK06	RK07
1	1	0/1	1	1	1	1	1	1	0	0
1	1	0/1	1	1	1	1	1	0	±25	± 12.5
1	1	0/1	1	1	1	1	0	1	±50	± 25.0
1	1	0/1	1	1	1	1	0	0	±75	± 37.5
1	1	0/1	1	1	1	0	1	1	±100	± 50.0
1	1	0/1	1	1	1	0	1	0	±125	± 62.5
1	1	0/1	1	1	1	0	0	1	±150	± 75.0
1	1	0/1	1	1	1	0	0	0	±175	± 87.5
1	1	0/1	1	1	0	1	1	1	±200	±100.0
1	1	0/1	1	1	0	1	1	0	±225	±112.5
1	1	0/1	1	1	0	1	0	1	±250	±125.0
1	1	0/1	1	1	0	1	0	0	±275	±137.5
1	1	0/1	1	1	0	0	1	1	±300	±150.0
1	1	0/1	1	1	0	0	1	0	±325	±162.5
1	1	0/1	1	1	0	0	0	1	±350	±175.0
1	1	0/1	1	1	0	0	0	0	±375	±187.5
1	1	0/1	1	0	1	1	1	1	±400	±200.0
1	1	0/1	1	0	1	1	1	0	±425	±212.5
1	1	0/1	1	0	1	1	0	1	±450	±225.0
1	1	0/1	1	0	1	1	0	0	±475	±237.5
1	1	0/1	1	0	1	0	1	1	±500	±250.0
1	1	0/1	1	0	1	0	1	0	±525	±262.5
1	1	0/1	1	0	1	0	0	1	±550	±275.0

*1 is the "+" or forward direction.

Table 3-6 Message Line B Bit Definitions
Controller-to-Drive Transmissions (Cont)

Clock Period	Command T12	Command T11	Direction* T10	Magnitude T9	T8	T7	T6	T5	T4	Offset Value (microinches) RK06	RK07
T4–T12 (cont)	1	1	0/1	1	0	1	0	0	0	±575	±287.5
	1	1	0/1	1	0	0	1	1	1	±600	±300.0
	1	1	0/1	1	0	0	1	1	0	±625	±312.5
	1	1	0/1	1	0	0	1	0	1	±650	±325.0
	1	1	0/1	1	0	0	1	0	0	±675	±337.5
	1	1	0/1	1	0	0	0	1	1	±700	±350.0
	1	1	0/1	1	0	0	0	1	0	±725	±362.5
	1	1	0/1	1	0	0	0	0	1	±750	±375.0
	1	1	0/1	1	0	0	0	0	0	±775	±387.5
	1	1	0/1	0	1	1	1	1	1	±800	±400.0
	1	1	0/1	0	1	1	1	1	0	±825	±412.5
	1	1	0/1	0	1	1	1	0	1	±850	±425.0
	1	1	0/1	0	1	1	1	0	0	±875	±437.5
	1	1	0/1	0	1	1	0	1	1	±900	±450.0
	1	1	0/1	0	1	1	0	1	0	±925	±462.5
	1	1	0/1	0	1	1	0	0	1	±950	±475.0
	1	1	0/1	0	1	1	0	0	0	±975	±487.5
	1	1	0/1	0	1	0	1	1	1	±1000	±500.0
	1	1	0/1	0	1	0	1	1	0	±1025	±512.5
	1	1	0/1	0	1	0	1	0	1	±1050	±525.0
	1	1	0/1	0	1	0	1	0	0	±1075	±537.5
	1	1	0/1	0	1	0	0	1	1	± 1100	±550.0
	1	1	0/1	0	1	0	0	1	0	±1125	±562.5
	1	1	0/1	0	1	0	0	0	1	±1150	±575.0
	1	1	0/1	0	1	0	0	0	0	±1175	±587.5
	1	1	0/1	0	0	1	1	1	1	±1200	±600.0

Clock Period	Description
T13	Don't-care condition for offset mode.
T14	This bit is reserved; it is a logic 0.
T15	**Parity** This bit determines odd parity for the 16-bit transmission.

*1 is the "+" or forward direction.

These nine (RK06; T13 is not used) or ten (RK07) bits are loaded directly into the cylinder difference register on the M7707 module (RK06) or the M7907 module (RK07), respectively. Note that a seek, RTC, or recalibrate command will clear the offset condition; ready will be reset until the offset seek or the clearing of the offset condition is completed; and a write gate received when offset is "on" causes the drive-off-track error and fault signals to be generated.

Table 3-7 Status Message B0 Bit Definitions Drive-to-Controller Transmissions*

Clock Period	Description
T0, T1	**Message Identifier Bits** These two bits identify this transmission from the drive to the controller and correspond to the message requested on the controller-to-drive transmission.
T2, T3	Reserved for additional message identifier bits; both bits are logic 0.
T4	This bit is reserved; it is a logic 0.
T5	**Invalid Address** This bit, when asserted, indicates that the drive has received an invalid head or cylinder address. It is stored in the invalid address flip-flop on the M7705 module; invalid address decoding occurs on the M7707 module (RK06) or M7907 module (RK07). This bit also asserts fault, drive status change (DSC), and attention (ATTN). When this error occurs, the assertion of a fault will prevent any head motion. As a result, the heads are prevented from potentially traveling beyond the limits. This bit is reset by the Drive Clear signal, initialize, power-up reset, or the RUN switch clear.
T6	**AC-Low Error** This bit, when asserted, reports that a low ac line voltage has been sensed in the drive when the heads are loaded. It reflects the ac-low error flip-flop on the M7705 module. AC-low error is the occurrence of an rms voltage of less than 85 ± 4 V for a low-voltage drive or 170 ± 8 V for a high-voltage drive. It will also cause the heads to unload, beginning with the first sector pulse after ac low detection. This feature allows for a read or a write operation in the current sector. The ac low error is reset by the Drive Clear signal, initialize, power-up reset, or the RUN switch reset (provided that the ac power has been restored).
T7	**Fault** This bit is the logic OR of all the drive error conditions; it is located on the M7705 module. Fault also lights the FAULT indicator on the control panel. The following conditions cause the fault bit to be asserted. 1. Selection of more than one drive. 2. Positioner, when detented, has moved too far from its original position (e.g., due to the drive being inadvertently jarred). 3. Parity error in a control transmission from controller to drive. 4. Any read/write unsafe condition in the drive (see bit T14 of this message for an explanation of the read/write unsafe conditions).

* These bits are routed via the B0 multiplexer on the M7706 module.

Table 3-7 Status Message B0 Bit Definitions Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T7 (cont)	5. A write lock error condition, i.e., the receipt of a Write Gate signal when the drive is write locked. 6. Low ac voltage in the drive. 7. A seek incomplete condition. 8. A non-executable function (NXF) from the receipt of a write gate or seek command with volume valid reset. Fault is reset when all of the components are reset.
T8	**Non-Executable Function** (NXF) This bit reflects the state of the NXF flip-flop on the M7705 module. When asserted, it indicates that a seek command or a Write Gate was received with volume valid not set. It is reset by the Drive Clear signal, initialize, power-up reset, or RUN switch reset.
T9	**Controller-to-Drive Parity Error** This bit reflects the state of the parity error flip-flop on the M7706 module. It is asserted whenever a parity error occurs in a transmission from the controller to the drive on Message Line A or B. It is reset by the Drive Clear signal, initialize, power-up reset, or RUN switch reset.
T10	**Seek-Incomplete Error** This bit is asserted and transmitted at time T10 if a seek incomplete occurs. The seek incomplete error occurs whenever the drive fails to successfully complete a seek to a new cylinder. Bit T10 is generated on the M7705 module. Seek incomplete errors include: 1. A servo unsafe error (see message B1, T14 for definition) 2. Seek and no motion (see message B1, T12 for definition) 3. Limit detect on seek (see message B1, T13 for definition) 4. Invalid address (see message B0, T5 for definition). This error is reset by Drive Clear, initialize, power-up reset, or RUN switch reset (provided that, if a servo unsafe error occurs, the heads are also home).
T11	**Write Lock Error** This bit reflects the state of the write lock error flip-flop on the M7705 module. When asserted, it reports that the drive has received a Write Gate signal at a time when the drive was write protected. It is reset by Drive Clear, initialize, power-up reset, or RUN switch reset.

* These bits are routed via the B0 multiplexer on the M7706 module.

Table 3-7 Status Message B0 Bit Definitions Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T12	**Speed-Loss Error** This bit reflects the state of the speed-loss flip-flop on the M7705 module. When asserted, it indicates that the spindle speed is no longer satisfactory, that the heads are or have unloaded, that no servo unsafe condition exists, and that the spindle motor should be energized. It is cleared by Drive Clear, initialize, power-up reset, or RUN switch clear (accomplished by depressing the RUN switch while the heads are home). This bit would be set from such probable causes as the spindle belt falling off or breaking, spindle speed-sensor defects, or a problem in the spindle motor circuits. The assertion of this bit also asserts fault, drive status change, and attention.
T13	**Drive-Off-Track Error** This bit reflects the state of the drive-off-track flip-flop on the M7705 module. When asserted, it indicates that a disturbance has caused the heads to move an unsafe distance from nominal detent position while in detent mode with Write Gate asserted, or that the drive was not ready and received a Write Gate. For the case where the drive is detented, this error will be sensed if the heads are offset by a nominal 300 microinches (RK06) or 150 microinches (RK07) for a period of at least 0.85 ms. This error is reset by Drive Clear, initialize, power-up reset, or RUN switch reset.
T14	**Read/Write Unsafe** This bit reflects the state of the read/write unsafe flip-flop on the M7705 module. It is used for reporting the following unsafe conditions. 1. The drive has been selected along with another in the system. 2. Write Current is sensed with no Write Gate. 3. Write Gate is received, but there are no write data transitions. 4. A head fault is detected; i.e., a head circuit imbalance is sensed. 5. More than one head has been selected. 6. An index error is detected; i.e., an index has not been sensed, or is sensed in the wrong location. 7. A tribit error has been sensed; i.e., three successive tribits are missing. 8. A servo signal present error is sensed; i.e., the signals from the servo surface cannot be detected. 9. A Write Gate is coincident with the trailing edge of a sector pulse.

* These bits are routed via the B0 multiplexer on the M7706 module.

Table 3-7 Status Message B0 Bit Definitions Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T14 (cont)	When this bit is asserted, the drive unloads the heads, but the spindle does not stop. This error is reset by Drive Clear, initialize, power-up reset, or RUN switch reset (provided that the heads are home and the unsafe condition has been cleared).
T15	**Parity** This bit determines odd parity for this drive-to-controller transmission.

* These bits are routed via the B0 multiplexer on the M7706 module.

Table 3-8 Status Message B1 Bit Definitions Drive-to-Controller Transmissions*

Clock Period	Description
T0, T1	These two bits identify this transmission from the drive to controller. They correspond to the message requested on the controller-to-drive transmission with the LSB transmitted first.
T2, T3	Reserved for additional message identification bits.
T4	**Sector Error** This bit reflects the state of the sector error flip-flop on the M7705 module. When asserted, it indicates that the drive has received Write Gate coincident with the trailing edge of a sector pulse. This error also causes the read/write unsafe condition as well as the fault condition to be generated. It is cleared by Drive Clear, initialize, power-up reset, and RUN switch reset.
T5	**Write Current and No Write Gate** This bit reflects the state of the flip-flop of the same name on the M7705 module. When asserted, it indicates that head write current has been detected without a Write Gate signal. This error also causes the read/write unsafe and fault conditions to be generated. It is reset by Drive Clear, initialize, power-up reset, and RUN switch reset (provided that the condition has been cleared). For sensing implementation, see Paragraph 4.4.4.1 (RK06) or 5.4.4.1 (RK07).
T6	**Write Gate and No Transitions** This bit reflects the state of the flip-flop of the same name on the M7705 module. It is used to report that the drive has received a Write Gate signal, but has not received any write data. This signal also causes the Read/Write Unsafe and Fault signals to be generated. It is reset by Drive Clear, initialize, power-up reset, or RUN switch reset (provided that the condition has been cleared). For sensing implementation, see Paragraph 4.4.4.3 (RK06) or 5.4.4.3 (RK07).

* These bits are routed via the B1 multiplexer on the M7705 module.

Table 3-8 Status Message B1 Bit Definitions
Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T7	**Head Fault** This signal reflects the state of the head fault flip-flop on the M7705 module. When asserted, it indicates a head fault or a head circuit failure, either of which would cause erroneous data to be recorded on the disk. This error also causes the Read/Write Unsafe and Fault signals to be generated. It is reset by Drive Clear, initialize, power-up reset, or RUN switch reset (provided that the condition has cleared). For sensing implementation, see Paragraph 4.4.4.4 (RK06) or 5.4.4.4 (RK07).
T8	**Multiple-Head Select** This bit reflects the state of the multiple-head select flip-flop on the M7705 module. When asserted, it reports that more than one head is enabled, a condition that could cause data to be recorded on more than one surface. This error also causes the Read/Write Unsafe and Fault signals to be generated. It is reset by Drive Clear, initialize, power-up reset, or RUN switch reset (provided that the condition has cleared). For implementation, see Paragraph 4.4.4.2 (RK06) or 5.4.4.2 (RK07).
T9	**Index Error** This bit reflects the state of the index error flip-flop on the M7705 module. When asserted, it indicates the absence or misplacement of an index pulse. This condition also causes the Read/Write Unsafe and Fault signals to be generated. It is reset by Drive Clear, initialize, power-up reset, or RUN switch reset. For sensing implementation, see Paragraph 4.2.2.3 (RK06) or 5.2.2.3 (RK07).
T10	**Tribit Error** This bit reflects the state of the tribit error flip-flop on the M7705 module. When asserted, it indicates the detection of a minimum of three successive tribits as missing. This error also causes the Read/Write Unsafe and the Fault signals to be generated. It is reset by Drive Clear, initialize, power-up reset, or RUN switch reset. Sensing of the missing tribits is implemented by gating the outputs of the 3-stage index-pattern shift register on the M7705 module.
T11	**Servo-Signal Error** This bit reflects the state of the servo-signal error flip-flop on the M7705 module. When asserted, it indicates the detection of the loss of servo signals from the servo surface. This condition also causes the Read/Write Unsafe and the Fault signals to be generated. It is reset by the Drive Clear, initialize, power-up reset, or RUN switch reset.

* These bits are routed via the B1 multiplexer on the M7705 module.

Table 3-8 Status Message B1 Bit Definitions
Drive-to-Controller Transmissions* (Cont)

Clock Period	Description
T12	**Seek and No Motion Error** This bit reflects the state of the seek and no motion error flip-flop on the M7705 module. When asserted, it indicates that a seek command was issued to the drive, but no track-count pulses were detected within 10 ms thereafter. This condition represents one of the seek incomplete conditions. It is cleared in the same manner as other errors.
T13	**Limit Detection on Seek** This bit reflects the state of the limit detection on seek flip-flop on the M7705 module. When asserted, it indicates that one of the limits was detected whenever the heads were not loading, unloading, or performing the recalibrate function. If a limit is detected, the heads will unload, but the spindle will continue to rotate. It is one of the seek incomplete conditions and is cleared in the same manner as all other errors.
T14	**Servo Unsafe** This bit reflects the state of the servo unsafe flip-flop on the M7729 module (RK06) or the M7906 module (RK07). When asserted, it indicates that the servo amplifier has been saturated for an excessive period of time, thereby indicating a servo runaway condition. This condition causes the heads to do an emergency retract under battery power and stop the spindle. It also causes the seek incomplete condition and is reset in the same manner as all other errors provided the heads are at their home position. Most hard failures in the servo loop will cause the current command to swing to a positive or negative limit and stay there. This is true of failures in circuits following the current command amplifier as well as those preceding it (because of the closed loop servo). The servo unsafe circuit detects the current command going high and staying high for an excessive period of time. When this occurs, the circuit sets the servo unsafe flip-flop, which causes battery-power retraction of the heads and the spindle stops. The biasing on of two zener diodes fires a 20 ms retriggerable one-shot. If the current command stays excessive, the one-shot will set the servo unsafe flip-flop when it expires. In normal operation, i.e., when no failure exists, the excessive current command will disappear before the one-shot expires, which keeps the flip-flop from being set. If the command disappears and then returns, the one-shot is retriggered. The only way the flip-flop can be set is for the current command to stay excessive for the entire duration of the one-shot period.
T15	**Parity** This bit determines odd parity for this transmission.

* These bits are routed via the B1 multiplexer on the M7705 module.

Table 3-9 Status Message B2 Bit Definitions Drive-to-Controller Transmissions

Clock Period	Description
T0, T1	**Message Identifier** These two bits identify this transmission from the drive to the controller. They correspond to the message requested on the controller-to-drive transmission. The LSB is transmitted first.
T2, T3	These bits are reserved; both are logic 0s.
T4–T13	**Cylinder Address** These nine bits (RK06; T13 not used) or ten bits (RK07) report the current cylinder address in binary-encoded form; the LSB is transmitted first. They reflect the nine (RK06) or ten (RK07) stages of the cylinder address register on the M7707 module (RK06) or M7907 module (RK07).
T14	This bit is reserved; it is a logic 0.
T15	**Parity** This bit determines odd parity for this transmission.

Table 3-10 Status Message B3 Bit Definitions
Drive-to-Controller Transmissions

Clock Period	Description
T0, T1	**Message Identifier** These two bits identify this transmission from the drive to the controller and correspond to the message requested on the controller-to-drive transmission.
T2, T3	These bits are reserved. They are both logic 0s.
T4–T8	**Encoded Section Count** These bits are used for transmitting the present sector address to the controller. They reflect the sector counter on the M7705 module. The LSB is transmitted first. The sector count is invalid if a sector pulse occurs during these clock times.
T9	Head 0 selected
T10	Head 1 selected
T11	Head 2 selected Bits T9, T10, and T11 are the outputs of the head address decoder on the M7707 module (RK06) or the M7907 module (RK07).
T12–T14	These three bits are reserved; each is a logic 0.
T15	**Parity** This bit is used for transmission of odd parity for this message.

CHAPTER 4
RK06 UNIT-LEVEL THEORY OF OPERATION

This chapter provides a detailed technical description of the RK06 Disk Drive. A similar presentation for the RK07 Disk Drive is given in Chapter 5. The discussion is organized around the following major subsystems.

1. Physical description (Paragraph 4.1)
2. Drive control subsystem (Paragraph 4.2)
3. Positioning subsystem (Paragraph 4.3)
4. Read/write subsystem (Paragraph 4.4)
5. Air supply subsystem (Paragraph 4.5)
6. Power supply subsystem (Paragraph 4.6)
7. Cartridge handling subsystem (Paragraph 4.7)
8. Dual-access option (Paragraph 4.8)

Figure 4-1 is the major block diagram for the RK06 Disk Drive. In each of the subsystem discussions, the relevant portion of this same diagram is highlighted by showing the functional blocks of that subsystem as shaded areas. All other blocks are unshaded.

4.1 PHYSICAL DESCRIPTION

The disk drive consists of two major assemblies and a group of discrete assemblies. The two major assemblies are a base plate assembly and a chassis assembly.

The elctromechanical subassemblies comprising the base plate assembly (Figure 4-2) are mounted on a cast aluminum base that is attached at three points to the chassis assembly through vibration isolators.

The chassis assembly (Figure 4-3) consists of a riveted sheet metal structure that provides a plenum for cooling air distribution as well as a mounting structure for numerous electromechanial subassemblies. Assemblies other than the base plate and the chassis are explained in the following paragraphs covering the drive subassemblies. The disk cartridge assembly, not considered as an integral part of the disk drive but designed for use with it, is described in Paragraph 2.3.

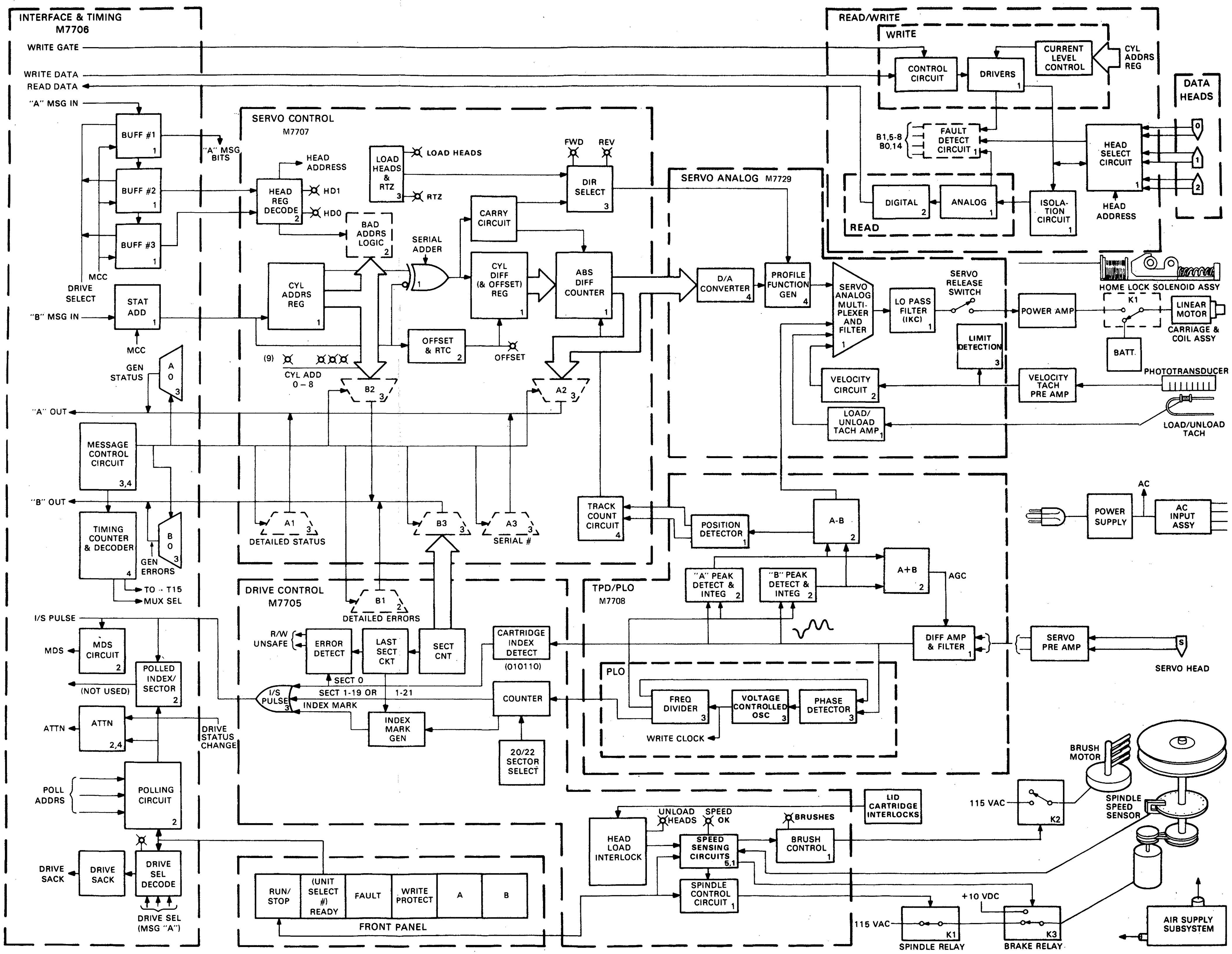


Figure 4-1 RK06 Disk Drive Functional Block Diagram

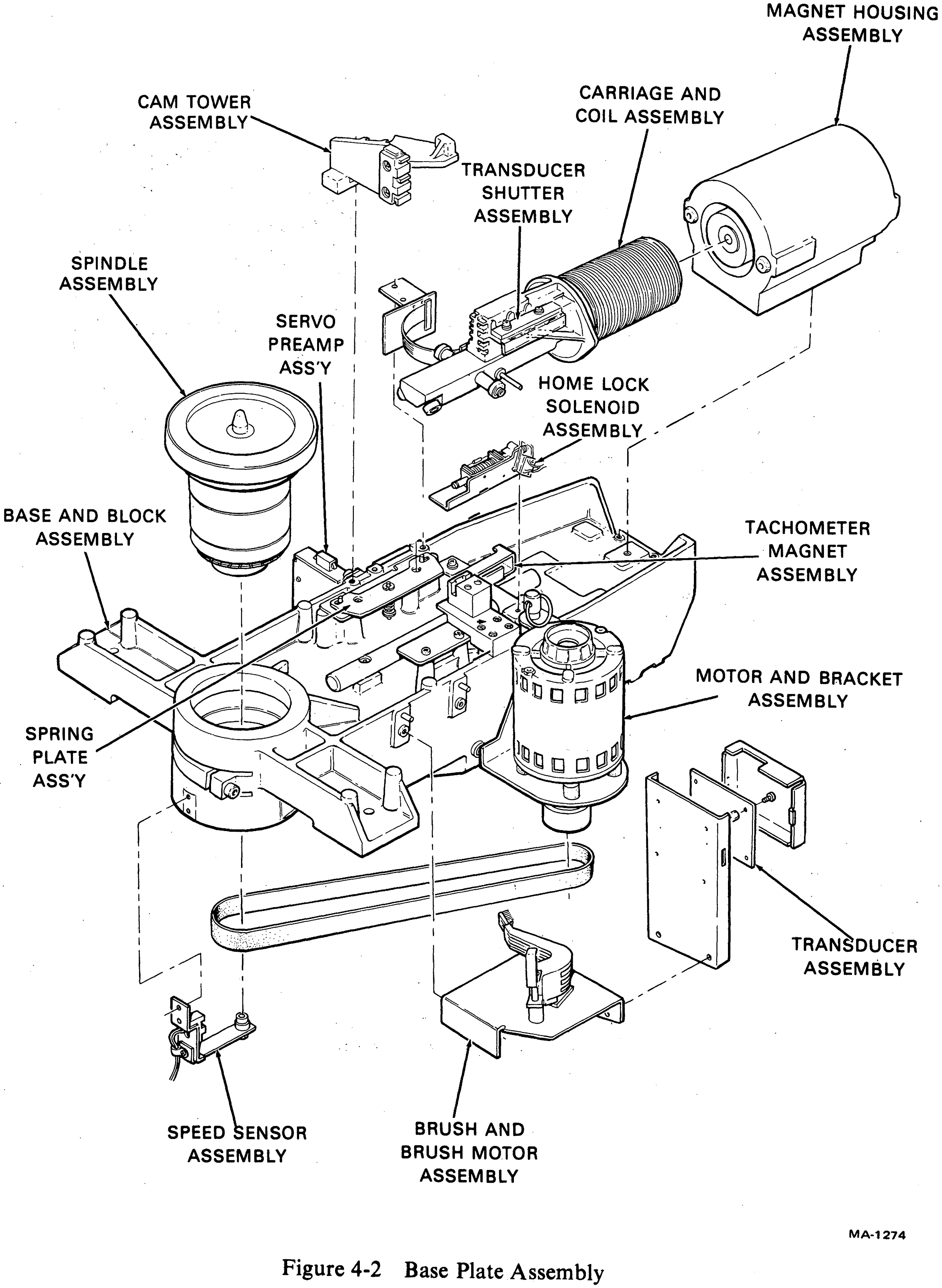


Figure 4-2 Base Plate Assembly

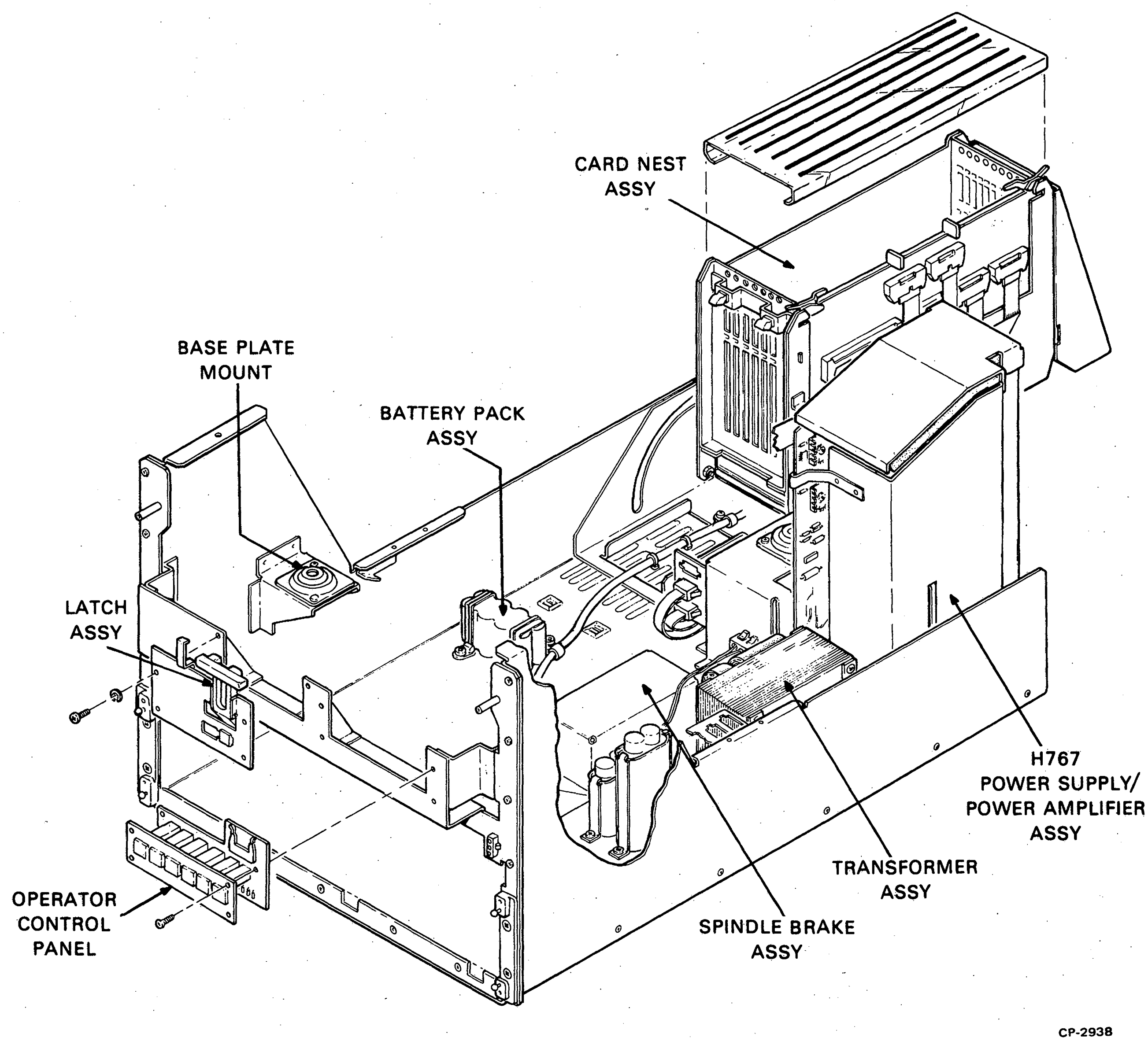


Figure 4-3 Chassis Assembly

4.1.1 Base Plate Assembly

The base plate assembly (Figure 4-2) consists of the following subassemblies.

1. Base and block assembly
2. Carriage and coil assembly
3. Spindle assembly
4. Home lock solenoid assembly
5. Transducer assembly
6. Tachometer magnet assembly
7. Servo preamp assembly
8. Speed sensor assembly
9. Brush and brush motor assembly
10. Magnet housing assembly
11. Motor and bracket assembly
12. Spring plate assembly
13. Cam tower assembly
14. Transducer shutter assembly

4.1.2 Chassis Assembly

The riveted chassis assembly (Figure 4-3) provides a plenum for air distribution and supports to which the base plate assembly is attached through vibration isolators. The chassis assembly serves as a mounting structure for the following assemblies.

1. Card nest assembly
2. H767 power supply assembly
3. Latch assembly
4. Spindle brake assembly
5. Battery pack assembly
6. Transformer assembly
7. Operator's control panel
8. Power harness assembly
9. Harness, A/C distribution

4.1.3 Card Nest Assembly

The card nest assembly, located at the left rear of the drive, has guided slots for eight printed circuit boards (modules). Single-access drives use the following modules (Figure 4-4).

1. Drive Control Logic (M7705)
2. Interface and Timing Logic (M7706; either A or B access)
3. Servo Control Logic (M7707)
4. Track Position Detector/Phase Lock Oscillator (PLO) (M7708)
5. Servo Analog (M7729)
6. Cable Board (M9016)

Dual-access drives, in addition to these boards, also use the following boards.

1. Interface and Timing Logic (M7706) (alternate access)
2. Dual-Port Drive Control Logic (M7730)

Visual indicators (LEDs), velocity potentiometer, speed OK potentiometer, a servo safety switch a servo release switch, and a dual-port maintenance switch are mounted on the boards at the locations indicated in Figure 4-4. The hinged card nest rotates through an angle of approximately 90 degrees from its normal operating position within the chassis assembly.

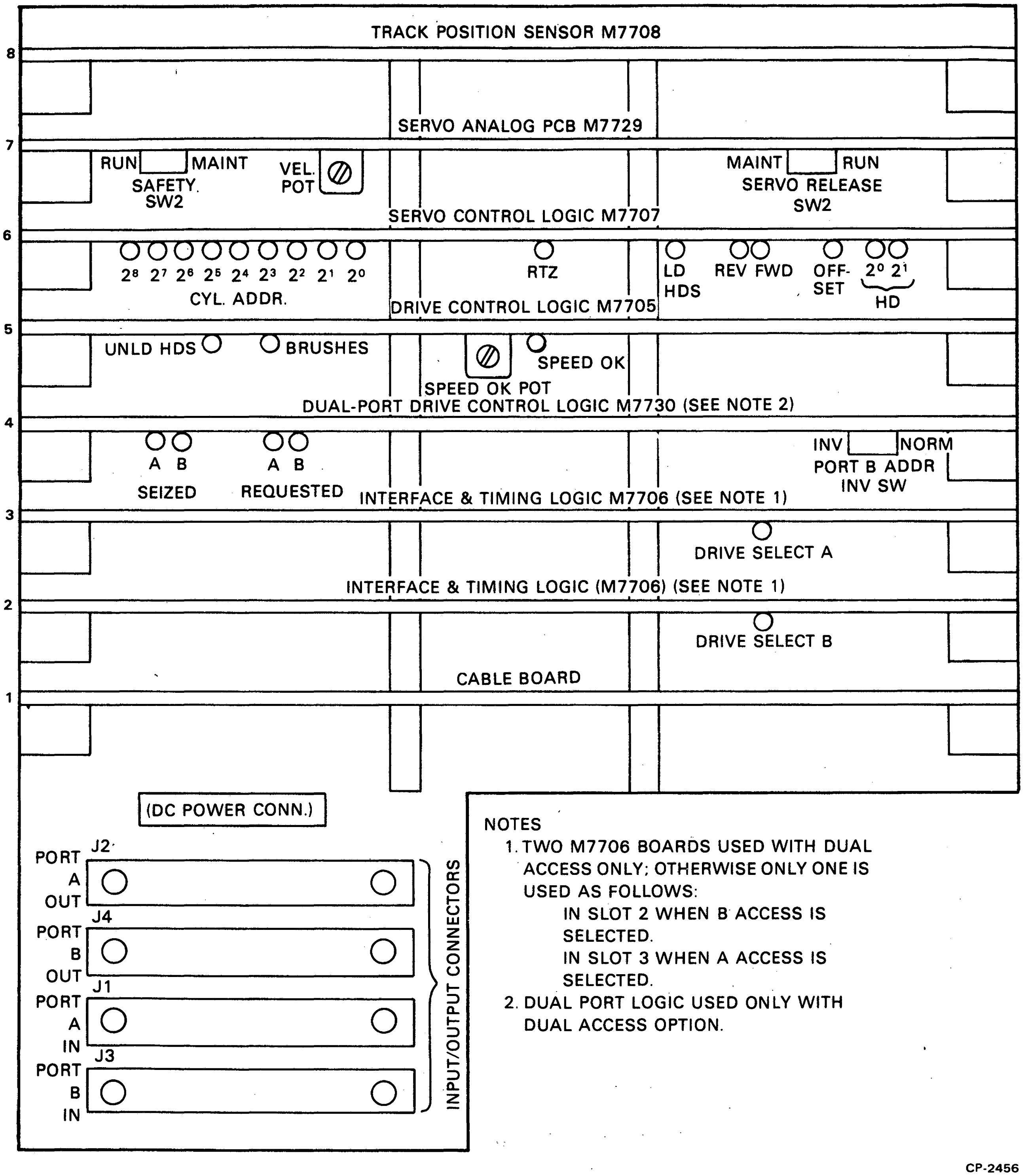


Figure 4-4 I/O Connectors and Card Nest Assembly

4.1.4 Miscellaneous Assemblies

Several assemblies of the drive are not included in either of the major assembly categories, i.e., the base plate assembly and the chassis assembly. These separate assemblies are:

1. Lid assembly
2. Shroud assembly (Figure 4-5)
3. Circuit breaker assembly
4. Front bezel assembly
5. Lower bezel assembly
6. Rear cover assembly
7. Air filter assembly.

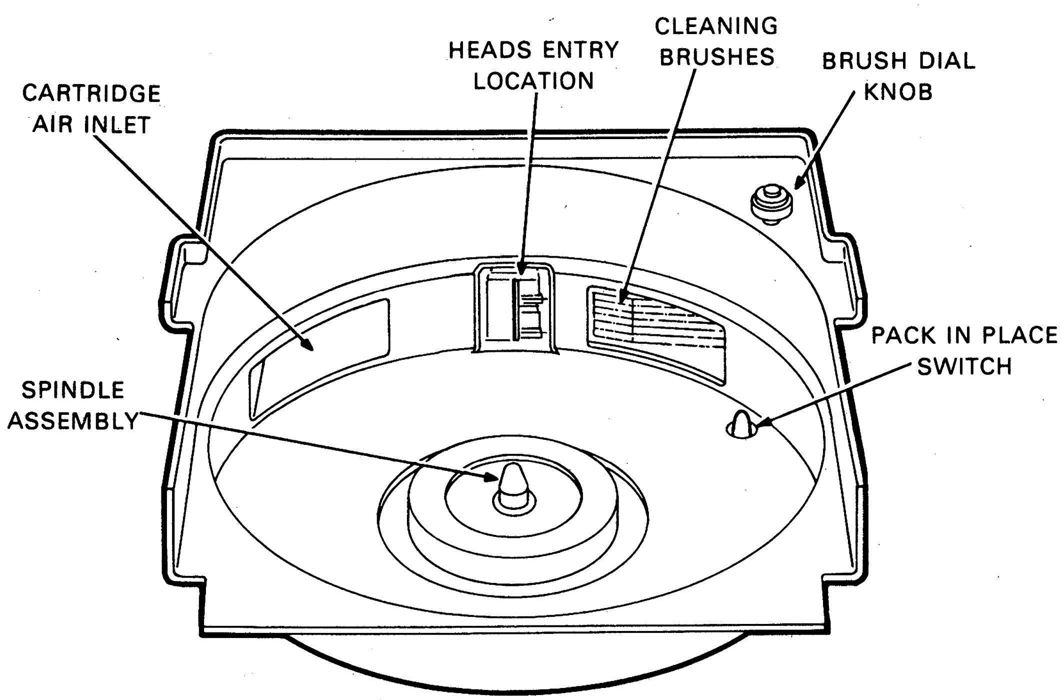


Figure 4-5 RK06 Cartridge Shroud Assembly

Front Bezel

The front bezel covers approximately the upper two-thirds of the front of the chassis assembly and contains cutouts through which the buttons on the switches of the operator's control panel protrude.

The lid-latch release button protrudes through a horizontal slot on the front surface of the bezel. The bezel is located on the chassis assembly by means of two dowel pins at the bottom and is held in place on the chassis assembly by two screws near the top. Removal of this bezel is required for access to the following.

1. Latch assembly
2. Speed sensor assembly
3. Operator panel assembly
4. Spindle clamp bolt
5. Spindle drive belt
6. Blower assembly

Bottom Bezel

The bottom bezel covers approximately the lower one-third of the front of the chassis assembly. Ambient air for cooling the electronics is inducted through horizontal slots in the bezel. The bezel is mounted to the chassis assembly by means of snap-on connectors. Removal of this bezel is necesssary for access to the following.

1. Blower assembly
2. Air filter assembly
3. Speed sensor assembly
4. Blower prefilter
5. Spindle drive belt
6. Spindle clamp bolt

4.2 DRIVE CONTROL SUBSYSTEM

The drive control subsystem (see the shaded blocks in Figure 4-6) comprises those elements that control the flow of command and status data to and from the drive; provide interlocks for safe operation; and control index and sector generation circuits, circuits for controlling spindle motor rotation, and the cartridge brush cycle.

4.2.1 Functional Sections

4.2.1.1 Operator's Control Panel - Figure 4-7 is an illustration of the operator's control panel. The panel consists of the following switches and indicators.

1. RUN/STOP switch with load indicator
2. Unit select switch with READY indicator
3. FAULT indicator
4. Write lock switch with WRITE PROT indicator
5. Access A enable switch
6. Access B enable switch

All control panel switches are solid-state Hall-effect devices except for the unit select switch, which does have contacts. The Hall-effect switches interface directly to the TTL logic.

RUN/STOP Switch with Load Indicator - When pressed, this push/push alternating action switch energizes the spindle motor. When released, it deenergizes the spindle motor if the heads are not loaded. If the heads are loaded, it causes the heads to unload and the spindle motor to deenergize in sequence. Since this switch has a mechanical memory, a power interrupt followed by power restoration will, if the switch is in its depressed position, cause the drive to automatically cycle up when power is restored.

The start spindle command from the controller is not enabled unless: (1) the RUN/STOP switch is in the depressed state and the drive has been cycled down due to a set medium off-line command, or (2) any of the errors leading to head unload occur. In the second of these situations, the heads will not reload unless the error condition has been cleared.

The load indicator of the RUN/STOP switch illuminates whenever: (1) the spindle is less than 1 rev/second, (2) heads are home, (3) brushes are home, and (4) the spindle motor is not energized.

Unit Select Switch with Ready Indicator - The unit select switch is a cam-operated switch that is actuated by inserting a numbered cammed button. The contacts are binary encoded such that the drive logic will recognize the drive address code corresponding to the unit select number. The numbered indicator is lit indicating a READY condition, whenever the heads are loaded and detented on a cylinder or detented in an offset position.

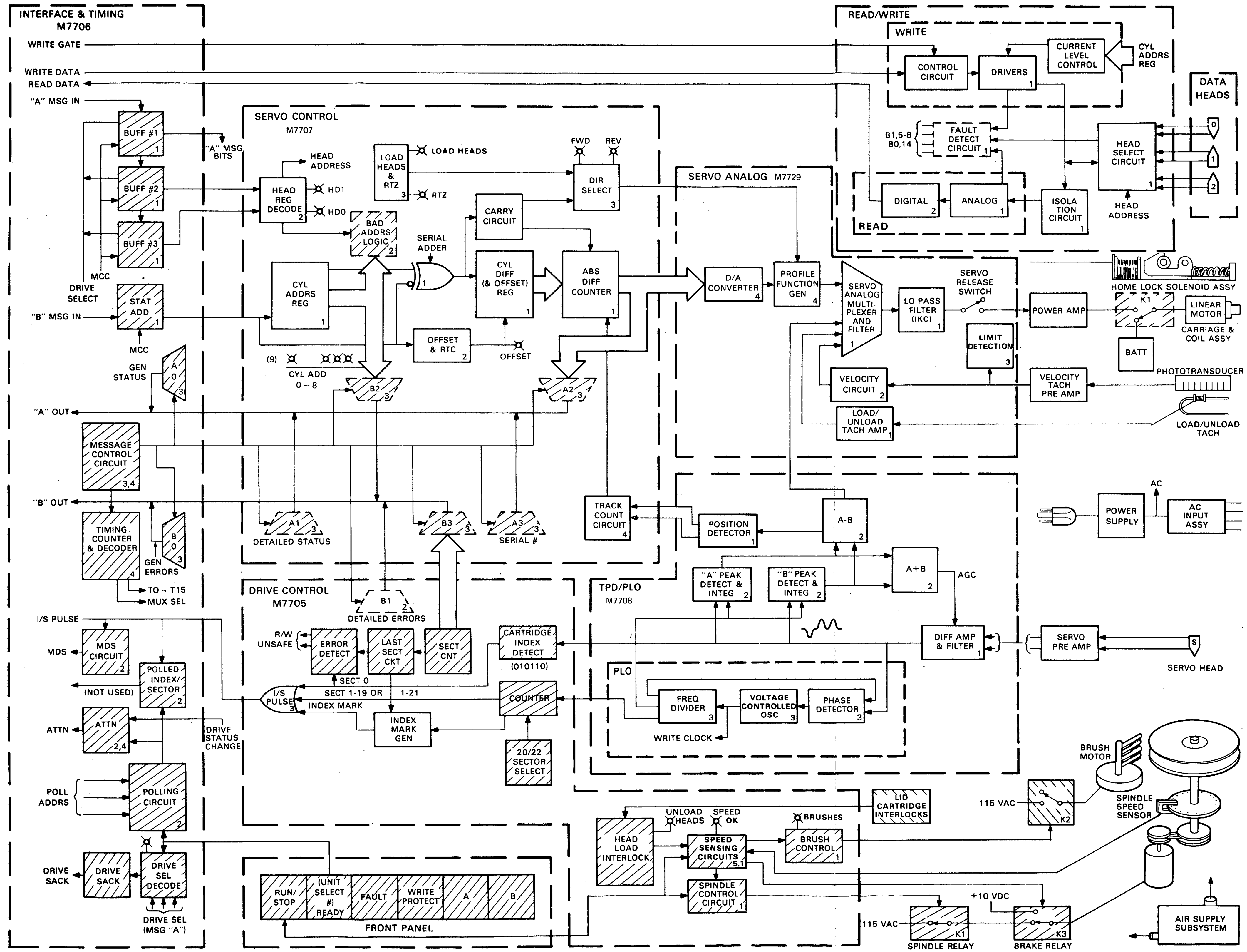


Figure 4-6 RK06 Disk Drive Functional Block Diagram with Drive Control Subsystem Shaded

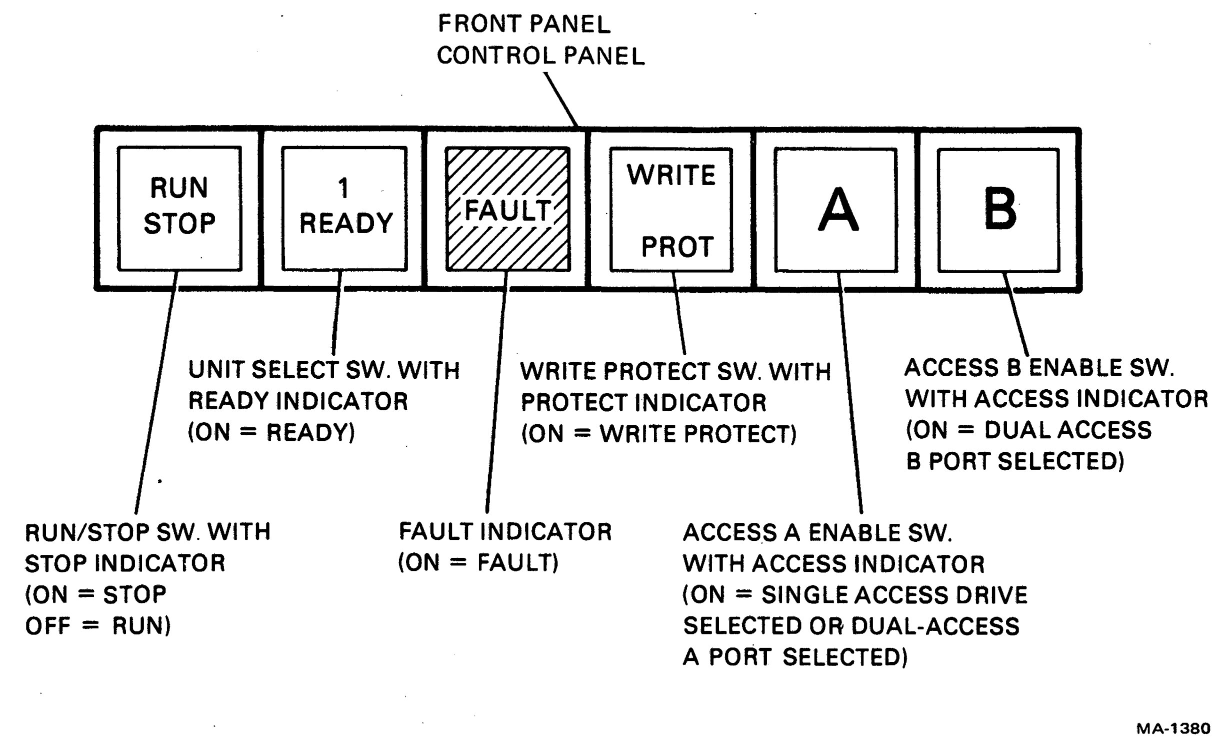


Figure 4-7 Operator's Control Panel

FAULT Indicator – This indicator is lit whenever a fault or error condition develops in the drive. Each fault or error that causes the indicator to illuminate is described in Table 3-7, bit 7, where "Fault" is defined.

Write Protect Switch with WRITE PROT Indicator – This push/push alternating-action switch, when pressed, places the drive in write protect mode only when Write Gate is not asserted in the drive. If Write Gate is asserted at the time that the switch is pressed, write protect will be inhibited until Write Gate is negated. Additionally, the WRITE PROT indicator will not be lit until write protect is truly enabled. Removal of write protect will occur immediately upon the release of the switch.

Access A Enable Switch – This alternating action push/push switch, when pressed, enables communication to and from the drive via the A set of input/output connectors under the following conditions.

1. If the drive is single access only, the interface and timing module must be located in the appropriate module slot for that set of connectors. When this is the case, the access A enable switch enables (when pressed) or inhibits (when released) communication to/from the drive. For single access, the indicator on this switch indicates when the drive is selected.

2. If the drive includes the dual-access option, this switch enables/inhibits communication via the A set of input/output connectors. When both the access A and access B switches are pressed, arbitration logic selects the appropriate access to the drive. For dual-access drives, the indicators on the A and B switches indicate which drive I/O channel is in use.

Access B Enable Switch – This switch is functionally identical to the access A enable switch except that this switch enables or inhibits communication via the B set of input/output connectors.

Dual-Access Option – If the drive includes the dual-access option, the access-enable switches enable (when pressed) and inhibit (when released) communication via that access. When both access switches are pressed, arbitration logic in the drive selects the appropriate access. In dual-access drives, the access in use at any time is indicated by an illuminated condition of the indicator of the associated access switch.

4.2.1.2 Interlocks – The interlock sensors and circuits provide for the safe operation of the disk cartridge and the heads. In some cases, these elements prevent spindle startup and in other cases, they prevent head loading unless they are satisfied. Similarly, the heads are unloaded if any of the interlocks become negated.

The drive interlocks include:

1. Lid-locking solenoid
2. Lid-locked sensor
3. Cartridge-present sensor
4. DC low sensor
5. AC low sensor
6. Spindle-speed sensor
7. Speed-sensing circuits
8. Brushes-home sensor
9. Read/write unsafe error
10. Servo unsafe error
11. Limit detect on seek error
12. Proper cartridge interlock (Paragraph 1.6).

Lid-Locking Solenoid – This solenoid is energized for the unlocked condition of the lid; i.e., it is energized only for the condition when it is safe to access the cartridge. As a result, the lid is locked when power is off, the heads are not at their home position, the brushes are not at their home position, or the spindle is not stopped.

The lid must be locked for the power-off condition. In the event that power was interrupted unexpectedly, the spindle takes considerable time without power to come to a stop. Furthermore, if the brush cycle were underway at power interrupt, the brushes might not complete their cycle. Both conditions would yield an unsafe situation for accessing the cartridge.

Lid-Locked Sensor – This switch senses that the lid is closed, latched, and the lid-locking solenoid is in the locked condition. When locked, the switch is closed.

Cartridge-Present Sensor –This switch senses that an RK06K cartridge is loaded in the drive and that its protective cover has also been placed over it within the drive.

DC Low Sensor – This electrical signal is generated within the power supply. Its output to the drive control circuits is an FET switch which is in the off state when all of the dc voltages are within specifications and on (or a low impedance to ground) when one or more voltages are below specifications.

In addition to being an interlock, a dc low condition inhibits the interface such that the drive will not disturb other drives on the bus.

AC Low Sensor – This signal is generated in the power supply in a similar manner to the dc low condition. This signal will unload the heads starting at a sector boundary. It is designed in this manner so that if a data transfer is occurring at the moment that ac low is sensed, the operation will be completed. This is acceptable because the dc voltages are guaranteed within range for at least 3.9 ms, thus enabling the completion of a sector.

Spindle-Speed Sensor – The spindle-speed sensor is an optical switch that generates pulses at a rate proportional to the rotational velocity of the spindle. The sensor consists of an LED source, a phototransistor receiver, and a slotted disk that is part of the Spindle Assembly. As the spindle rotates, the phototransistor alternately receives light from the LED and is blocked from receiving light.

The pulsed spindle-speed signal is applied to two retriggerable single shots on the M7705 module, one of which senses repetition rate of the pulses for the speed OK condition for loading heads and the other for determining the spindle stopped condition for unlocking the lid.

Brushes-Home Sensor – This switch senses that the brushes are fully retracted at the brush-home position. If they are not retracted, the lid-locking solenoid keeps the lid locked. Furthermore, the heads are inhibited from being loaded until the brushes complete the cleaning cycle.

Read/Write Unsafe Error – This condition, when asserted, unloads the heads if loaded or prohibits loading if unloaded. It is indicative of a faulty condition that would result in potential loss or misplacement of data on the cartridge. See Paragraph 4.4.4 and Table 3-7 for components of this error.

Servo Unsafe Error – This condition, when asserted, causes the positioner to retract under the battery power. Unless it is cleared, the positioner is furthermore inhibited from loading the heads. This condition is indicative of the servo system being out of control. It is generated by a circuit that senses that a current command is above a selected threshold of 20 ms.

Limit Detect on Seek Error – This error is generated if, for any reason, the Outer Limit or the Inner Limit signal is sensed whenever the positioner is not being loaded, unloaded, or doing a recalibrate. It is reset by any of the error-clearing signals in the drive (Table 3-8, Bit 13).

4.2.1.3 Index/Sector Pulse Generation Circuits – The index/sector pulse generation logic of the drive control module (M7705) consists of:

1. The index decoder
2. Sector counter and generator
3. Index mark generator
4. Index/sector OR gate.

Index Decoder – These circuits on the M7705 module consist of an 8-bit shift register and gating for the decode of the index pattern and a flip-flop for synchronizing the decoded index with the servo clock. This Decoded Index signal becomes the sector 0 pulse and is a nominal 3.7 μs wide.

Sector Counter and Generator – The sector counter and sector pulse generator circuits on the M7705 generate either 19- or 21-sector pulses per cartridge rotation, depending on the format, which is selected by the system. These circuits are synchronized to the Index signal and are generated by counting servo clock pulses. All of these sector pulses, except the sector 0 pulse described above are a nominal 1.86 μs wide.

Index Mark Generator – The Index Mark signal generated on the M7705 is a derived signal for synchronizing the sector count for the controller. This pulse is located in the last sector in either format beginning a nominal 178 μs after the leading edge of the last sector pulse and having a nominal 59.2 μs duration. When the composite of this and the sector pulses is transmitted over the interface, the Index Mark signal identifies the next pulse as the beginning of sector 0.

Index/Sector OR Gate – This gate on the M7705 combines the index pulse (sector 0 pulse), sectors 1–19 or 1–21 pulses, and the Index Mark signal into a composite signal for transmission to the controller over the interface.

4.2.1.4 Spindle-Control Circuits - This logic circuitry is located on the M7705 module and consists of the gating and the run flip-flops and relay driver for controlling the relay that energizes the spindle motor. The run flip-flop may be set by the RUN/STOP switch on the operator's control panel or from a command from the interface if the RUN/STOP switch is pressed, provided the heads are home and the interlocks are all asserted. It is reset by: (1) the release of the RUN/STOP switch, (2) command from the interface, or (3) an unsafe interlock condition that causes the heads to unload. It should be noted that the spindle will not be deenergized until the heads are at the home position to preclude the possibility that the heads would crash on the disk surfaces if the servo malfunctions and fails to retract the heads.

There is one case where the spindle will be deenergized before the heads are home. This occurs if servo unsafe (Paragraph 4.2.1.2) is detected. For this case, servo unsafe is an indication of servo malfunction and it is therefore assumed that the heads may not retract under servo control properly. As a result, the spindle is immediately deenergized and the battery retracts the positioner directly. The servo unsafe condition is inhibited when the maintenance switch is enabled.

4.2.1.5 Brush Control Circuits - This logic circuitry on the M7705 module controls the brush disk cleaning cycle. The brush cycle is initiated when the disk is nearly at the safe speed for head loading on drive startup. The cycle lasts approximately 11 seconds and is terminated when the brushes return to the brush-home location. The brush cycle, once started, must be completed, since it cannot be reversed. The controlling flip-flop is applied to a relay driver which controls the relay for energizing the brush motor.

4.2.1.6 Message Control Logic - These circuits on the M7706 module use the CTD, Strobe, and Control Clock signals from the interface to generate an Input-Enable signal and an Output-Enable signal that enable and inhibit the receipt and transmission of interface messages, respectively.

4.2.1.7 Timing Counter and Decoder - These logic circuits on the M7706 generate individual decoded timing pulses (T0 to T15) as a result of counting control clock pulses during the receipt of interface messages only. The counter is used for controlling both the receipt and transmission of messages but the decoder is used only on incoming transmissions.

4.2.1.8 Multiple Drive Select (MDS) Logic - To avoid the possibility of two or more drives simultaneously writing data destined for only one of them, it is necessary to have a means of determining if more than one drive has been selected. This could occur either by a malfunctioning circuit in one of the drives or in the event that identical drive-numbered unit select plugs were inserted in each drive.

Logic circuits in the M7706 module are designed to sense if another drive is also selected in the daisy-chain bus. It is accomplished by monitoring the Index/Sector signal line. The sensing of the signal on the bus from another source results in a multiple drive select error. This is valid because only a selected drive transmits on this line.

When the heads of a selected drive are loaded, the index and sector pulses are transmitted over the interface. When they are unloaded, the selected drive transmits the control clock on the interface. As a result, a selected drive compares any pulse on the interface to its own Index/Sector signal internal to the drive. If there is no comparison, the Multiple Drive Select signal is asserted on the interface.

4.2.1.9 Drive Select Decode - This logic circuitry on the M7706 module compares the first three bits of a transmission to the drive on Message Line A with the number represented on the unit select plug. The first three bits of a transmission represent the drive number to be selected in binary-encoded form with the least significant bit first. These bits are shifted into the BUFF 1, BUFF 2, and BUFF 3 flip-flops, after which the comparison is made. Note that all the drives on the bus are selected in order to receive the transmission. Each drive's comparison with the unit select plug number leaves only the requested drive selected.

4.2.1.10 Drive SACK – This flip-flop on the M7706 module represents a select acknowledge by the selected drive to the controller following the receipt of the drive select code and the time for the deselect code. If the drive is truly selected, the SACK flip-flop sets and remains set until the beginning of another message, at which time it resets.

4.2.1.11 Polling Logic – This logic circuitry on the M7706 module accepts the receipt (from three interface lines) on a continuously polling basis, the eight drive numbers in binary-encoded form. For each drive number, a comparison is made with the number as represented by the unit select plug. When a comparison is made, the Enable Pollout signal is generated which enables the Attention signal, if asserted, to be transmitted on the interface. In this manner, the system can rapidly determine which drive(s) assert Attention, causing an interrupt.

4.2.1.12 Attention – This signal is transmitted over the interface when requested by the controller from the polling addresses it transmits. The Attention corresponding to drive status change (A0, T14) is asserted from any of a number of conditions (Table 3-2).

4.2.2 Control Operation

The following paragraphs describe the various operations pertinent to the drive control subsystem. These operations are:

1. Drive Startup (Paragraph 4.2.2.1)
2. Spindle Stopping (Paragraph 4.2.2.2)
3. Index/Sector Circuit Operation (Paragraph 4.2.2.3)
4. Command and Status Data Control (Paragraph 4.2.2.4).

4.2.2.1 Drive Startup – The drive is initially started by pressing the RUN/STOP switch on the operator's control panel. With the lid closed, the lid-locking solenoid will now release, causing the lid to lock shut. The coincidence of the lid shut and locked yields the lid-locked interlock condition. If this interlock and all others (Paragraph 4.2.1.2) are satisfied, the run flip-flop will set and the relay driver will energize the spindle relay (if there is no servo unsafe condition), which in turn applies power to the spindle motor.

As the spindle begins to rotate, the spindle speed sensor generates pulses proportional to the rotational speed. Once the period of the speed pulses becomes less than 100 ms per pulse, the retriggerable single-shot which determines the stopped condition will no longer time-out and, as a result, the stopped flip-flop will reset. This causes the stopped indication on the RUN/STOP switch to extinguish. Note that this takes approximately 1 to 2 seconds from initial startup. In newer drives, the spindle motor will stop immediately if speed pulses are not sensed.

As the speed increases such that the period of the speed pulses becomes less than a nominal 2.4 ms, the retriggerable single-shot which senses safe spindle speed will no longer time-out. With this single-shot constantly set, the Reset signal it applies to in the 7493 counter is removed, permitting the counting of speed pulses. If the sensed speed temporarily drops below the safe spindle speed, the Reset signal is once again applied to the counter. When the speed is above the sensed threshold for safe spindle speed, the counter is permitted to accumulate counts. When the counter gets to a count of 8, the brush cycle is initiated to clean the disk surfaces. When a count of 12 is reached in the counter, the Speed OK signal is asserted.

Provided the interlocks are still asserted and there are no unsafes, the positioner need only wait the completion of the brush cycle to load heads. This takes approximately 11 seconds to complete. When the brushes return to the brush-home position, the brushes flip-flop resets and all of the conditions are satisfied to reset the unload heads flip-flop, which in turn allows the load heads flip-flop (on the M7707 module) to set. (See Paragraph 4.3.2.1 on the head load sequence.)

4.2.2.2 Spindle Stopping - The spindle will stop whenever the RUN/STOP switch is released, the drive receives a command to unload the heads, a servo unsafe occurs, or if the ac power is interrupted. For the cases where the servo unsafe or the loss of ac power occurs, the spindle is deenergized immediately (even with the positioner not at the home position) and the positioner unloads by battery power to the motor. For all other cases, the spindle remains energized until the heads arrive at the home position. (See Paragraph 4.3.2.2 for the head unload sequence.)

With the heads home and the RUN/STOP switch released or the drive commanded to stop, the run flip-flop will reset, deenergizing the spindle via the relay driver and relay. These events enable the spindle brake. The spindle brake relay driver is enabled by the not run and not stopped conditions.

At this point, it should be noted that the spindle relay and spindle brake relay coils are interlocked with contacts of the other relay such that one is not permitted to operate while the other is energized.

Because the spindle is now deenergized, the interlocked coil circuits enable the brake relay coil to energize. As a result, the spindle brake circuit applies a full-wave-rectified dc voltage of approximately 11 V to the spindle motor. The motor now decelerates to a stop in approximately 20 to 25 seconds. When the retriggerable single-shot (which senses the stopped condition) times out, the STOP indicator on the operator's panel is lit, the brake voltage is removed via the relay driver deenergizing the relay, and the lid-locking solenoid is energized, thereby unlocking the lid mechanism provided that the RUN/STOP switch has been released.

4.2.2.3 Index/Sector Circuit Operation - The basic concept of operation of the index and sector generation circuits is the detection of the index pattern from the Sync Pulse signal of the tribits, to use the resultant signal to initialize the counter for sector generation and the actual sector counter, and to count down the Servo Clock signals to derive the appropriate Sector Pulse signal. There are two different formats for the sector signal, namely 20 sectors per rotation or 22 sectors per rotation, as commanded by the controller.

These circuits use the Servo Clock ÷2 signal (from the difference amplifier and filter) to sense an index pattern from the Servo Pulse signal. The index pattern is actually the absence of three tribits in the following sequence (---11110101101111----) where the 0s represent the missing tribits. As a result, by clocking the Servo Pulse signal with the Servo Clock ÷2 signal (which continues despite the few missing tribits), the missing pulses are sensed.

The resultant clocked signal is shifted by the Servo Clock ÷2 signals into an 8-bit register. The outputs of six stages of the shift register are sensed by decoding gates, the output of which is asserted upon the detection of the index pattern. The Servo Clock signal clocks the decoded index pattern into the index flip-flop.

The decoded Index signal is used as an initializing signal to two counters, one of which counts Servo Clock signals to derive sector pulses and the other counts sector pulses.

In order to facilitate understanding of these counter operations, the arithmetic relative to the number of servo clock pulses per revolution and the number of counts necessary per sector is now explained.

$$\text{No. of tribits/rev} = 6720$$

$$\text{No. of } \frac{\text{servo clock}}{2} \text{ pulses/rev} = 6720$$

$$\text{No. of servo clock pulses/rev} = 13440$$

Since the sector pulse generation counter uses the Servo Clock signal to generate sector pulses, we arrive at the following numbers.

In 20-sector mode,

$$\frac{13{,}440 \text{ pulses/rev}}{20 \text{ sectors/rev}} = 672 \text{ pulses/sector}$$

The sector generation counter is implemented such that when a count of 1024 is achieved, a sector pulse is generated which in turn is used to preset the counter again on the following servo clock pulse. As a result, it can be seen that to accumulate a count of 672 pulses up to a count of 1025 (since the count of 1024 lasts for the entire clock period):

$1025 - 672 = 353$

which is the value that is preset into the counter except for the last sector.

For the case of the last sector, a value of 357 is preloaded into the counter instead of 353. This is done in order to generate the Index Window Open signal within which the next Index Detected signal must occur. If the Index signal is detected outside this pulse time (three servo clock periods) or if the Index signal is not detected, index error will occur which will cause Fault and Read/Write Unsafe signals (which cause the heads to unload).

In 22-sector mode,

$$\frac{13{,}440 \text{ pulses/rev}}{22 \text{ sectors/rev}} = 610.9 \text{ pulses/sector}$$

Since this is not a whole number, this format is treated differently; that is, 610 pulses/sector is used. Now,

$610 \times 22 = 13{,}420$

This leaves 20 pulses more per revolution. To account for all pulses, the last sector is 20 pulses longer.

For all sectors except the last, the following number must be preloaded to accumulate a count through 1024 (up to 1025):

$1025 - 610 = 415.$

This is the number preloaded.

For the last sector, 20 additional pulses must be counted so that it should be expected to load in a lower number, namely:

$415 - 20 = 395.$

However, as is the case of 20-sector mode, a count higher by 4 is preloaded in order to generate the Index Window Open signal.

As a result, a count of 399 is preset into the counter.

The remaining pulse of the Index/Sector signal to be generated is called the *index mark.* This pulse signals the controller that the next pulse that occurs is the beginning of sector 0. As a result, the index mark pulse occurs in the last sector. This pulse is a nominal 60 μs wide with its leading edge approximately 178 μs after the last sector pulse. It is generated by using 2^4 count in the sector pulse generating counter to generate a shift pulse of 1s through a shift register with an exclusive OR decode of two shift register stages.

Since the drive can have its format changed by command from the system without regard for the synchronism of the sector pulse count, the electronics on the M7705 immediately ceases generating sector pulses until the following sector 0 pulse, at which time it begins counting and generating pulses in the new format. This is done by the three flip-flops that generate 20-Sector Format, 20-Sector Format Del. and Actual 20-Sector Format, respectively. These flip-flops form a 3-bit shift register that controls the inhibiting of sector pulses and the resynchronizing to the new format.

4.2.2.4 Receipt of Command Messages – The control of commands (received messages) and status (transmitted messages) is accomplished by logic circuitry on the M7706 module. This control is based on the CTD, Strobe, and Control Clock signals on the interface. These signals define the timing and direction of the messages. In addition, two bits on Message Line B determine which of four sets of messages are transmitted following the received message. See Tables 3-1 through 3-10 for definitions and properties of these signals.

Figure 3-2 illustrates the timing relationships between these interface control signals and the contents on Message Line A and Message Line B for messages in both directions.

Before messages can be received or transmitted, the Interface Enable signal must be asserted. This signal is the logical AND of the Interface Controller Power signal and the front panel A or B switch (Chapter 3). With the Interface Enable and CTD signals asserted, the receipt of a strobe pulse initiates the receipt of messages on the message A and message B lines simultaneously. The strobe pulse sets the drive select flip-flop and the input enable flip-flop. Input Enable being asserted enables the message A and message B line receivers and the assertion of Drive Select enables the receipt of clock pulses.

Each negative edge of the control clock loads Message Line A and Message Line B data into the BUFF 1 and STATADD flip-flops, respectively. Clocking of the data on the clock's negative edge deskews the data from propagation delay variations on the controller-drive cable and the interfacing circuits. Figure 4-8 is an expanded diagram showing these timing relationships. For all clock pulses except the first, the clock counter on the M7706 module is advanced on the clock's negative-going edge. However, during the strobe pulse time, the strobe holds the counter reset. Upon the next clock rising edge, the clock time decoder is enabled and the short clock pulse (CP) generates a 100 ns pulse on the T0 output. Figure 3-2 shows this pulse's timing in relation to the other control and data signals. These same relationships then apply for the remainder of the message transmission.

At the trailing edge of T15, the input enable flip-flop is reset, thereby terminating the receipt of the message, resetting the clock counter to 0, and inhibiting the timing decoder.

During the receipt of command messages, parity detection circuits on the M7706 module sense the state of each bit that is received. For each logic 1 that is received on both lines, the corresponding parity flip-flop toggles to its opposite state. At the trailing edge of the T15 pulse time, the composite parity flip-flop (Par Err) is clocked and set if an even number of logic 1s were sensed on either line. In this manner, a parity error is sensed.

4.2.2.5 Transmission of Status Messages – The output enable flip-flop is set when the CTD signal is negated, the Input Enable signal is reset, and the next clock negative transition occurs. The Output Enable signal enables the strobe and the message A and message B transmitters. The drive now commences to transmit a status message to the controller.

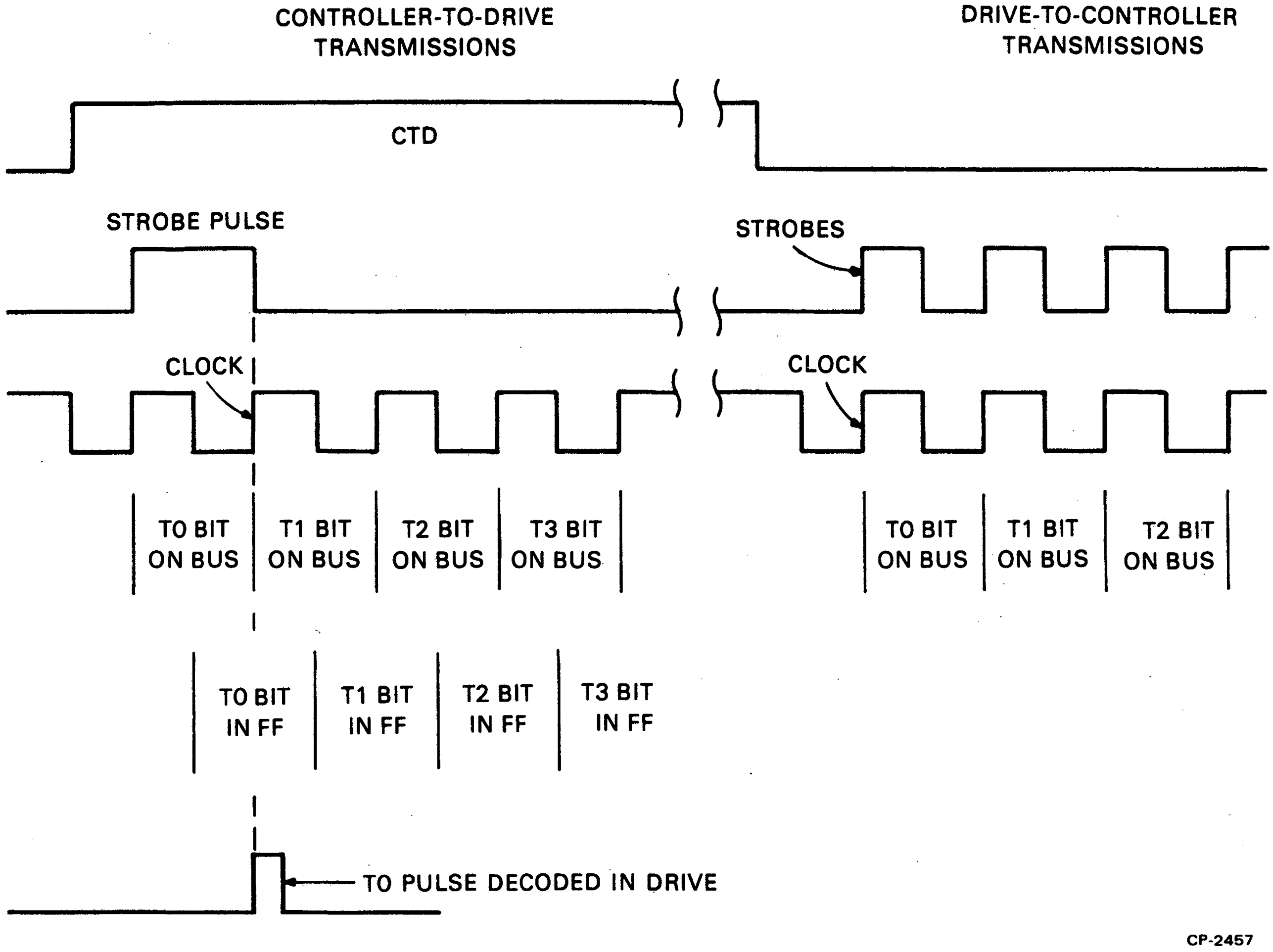


Figure 4-8 Timing Relationships for Controller/Drive Transmissions

Starting at the next clock pulse time, the drive transmits the Clock signal which it receives onto the strobe interface line. During the same period, the message A and message B lines transmit 16 bits each as status messages. See Figure 3-2 for an illustration of timing during transmissions from the drive.

The messages transmitted on the message lines are those that were requested on the prior message from the controller to the drive. The pair of messages that are transmitted are indicated in Figure 3-2. The message request bits received by the drive are the first two bits on the message B line in binary-encoded form with the least significant bit first. These bits are stored in the byte 0 and byte 1 flip-flops on the M7706. The flip-flop outputs are decoded and applied to the appropriate multiplexers which convert parallel status data to serial form for transmission. The multiplexers are located on the M7705, M7706, and M7707 modules. The outputs of the multiplexers are logically ORed on the M7706, clocked into the "Tr Mess A" and "Tr Mess B" flip-flops to synchronize the status bits to the clock pulses, and then transmitted onto the interface.

As each bit is transmitted, two parity flip-flops ("Mess A Par" and "Mess B Par") sense each bit that is transmitted. For each logic 1 that is transmitted on both lines, the corresponding parity flip-flop toggles to its opposite state, then is applied as the last bit in the multiplexer for transmission. In this way, an odd number of logical 1s are transmitted in each message.

4.3 POSITIONING SUBSYSTEM

The positioning subsystem (Figure 4-9) comprises the electrical and mechanical elements that cause physical positioning of the servo and data heads. Electrical circuits of the positioning subsystem are contained on the M7707, M7708, and M7729 modules as well as the phototransducer preamplifier and servo preamplifier. Mechanical elements include the linear motor, carriage, servo head, phototransducer, and load/unload tachometer. Paragraph 4.3.1 gives functional descriptions of these circuits and mechanical elements in detail. Paragraph 4.3.2 gives operational details of the positioning functions.

4.3.1 Functional Sections

4.3.1.1 Cylinder Address Register – The cylinder address register located on the M7707 receives and stores desired cylinder address information from the controller via the interface and timing module. After the completion of a seek, this register will contain the current cylinder address. Cylinder address data comprises nine bits that are loaded into the register in serial form upon the receipt of a seek command transmission. It is reset by head loading, unloading, or return-to-zero (RTZ) functions.

4.3.1.2 Serial Adder – The serial adder is comprised of two exclusive OR gates located on the M7707 module. It provides a cylinder difference obtained by 1's complement arithmetic sum of a new cylinder address (being received by the drive) with the existing cylinder address (stored in the cylinder address register).

4.3.1.3 Cylinder Difference and Offset Register – This register of nine bits performs two functions. First, it stores the resultant cylinder differences as provided by the 1's complement serial adder. Second, it stores information received from the controller when there is no seek command to determine if an offset is being commanded. In both cases, the data are loaded serially but the outputs are taken in parallel. It is reset by the head loading, unloading, or RTZ function.

4.3.1.4 Carry Circuit – This circuitry on the M7707 consists of gating that determines if there is a carry on a bit-by-bit basis for the serial differencing and a flip-flop for storing the carry bits. At the end of the differencing operation, the state of the flip-flop indicates if the difference was positive or negative, and therefore, controls subsequent operations to result in an absolute difference value. The carry flip-flop, therefore, also controls the direction of motion of a seek.

4.3.1.5 Difference Counter – The difference counter located on the M7707 module is a 9-bit up/down counter that stores the magnitude of cylinder difference and offset values for cylinder offsetting. It must up-count by one when cylinder differencing produces a carry and it down-counts by one for each cylinder crossing during a seek (Paragraph 4.3.2.4). It is reset by the head loading, unloading, or RTZ function.

4.3.1.6 Offset and RTC Circuits – These combinational logic circuits on the M7707 module are used for decoding and controlling offset and return-to-centerline (RTC) commands. Offsetting provides for accurately relocating the heads up to ±1200 microinches from the cylinder centerline in 25 microinch increments. The return-to-centerline command cancels an offset and returns the heads back to the center of the cylinder.

4.3.1.7 Load Heads and RTZ Circuits – These circuits on the M7707 module consist of logic for controlling the loading of heads from the home position and for controlling the return-to-zero function.

4.3.1.8 Direction Select Circuits – These circuits on the M7707 module consist primarily of the forward flip-flop and the reverse flip-flop and associated gating that controls these elements. These flip-flops control the direction of carriage motion during seek operations.

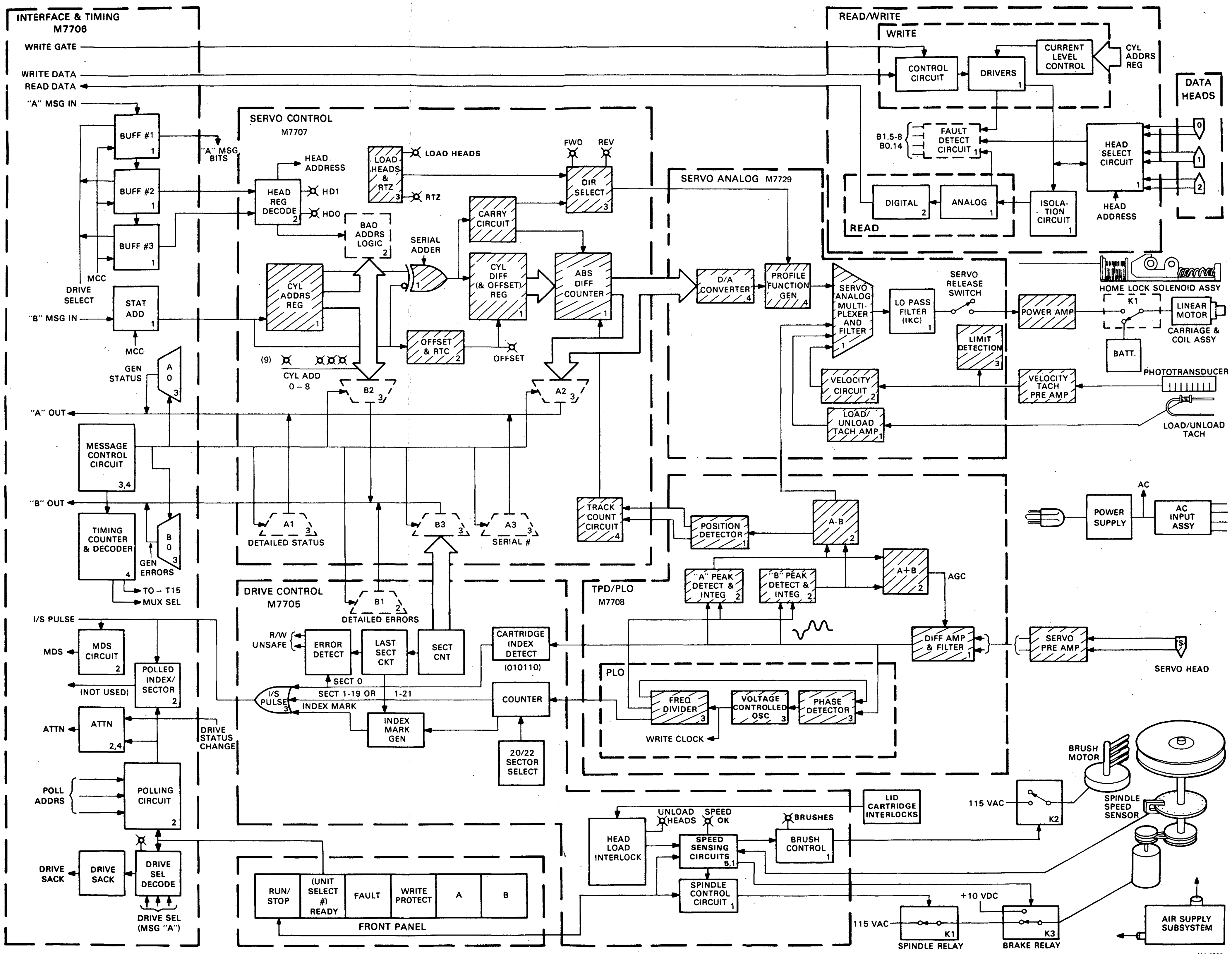


Figure 4-9 RK06 Disk Drive Functional Block Diagram with Positioning Subsystem Shaded

4.3.1.9 Track Count Circuits – This circuitry on the M7707 module provides count pulses to the difference counter at the appropriate location and time for each cylinder crossing during seeks.

Coarse Track is a logic signal derived from the Track Error signal in the track position detector. It is asserted when the heads are within ±1/4 track from the center. The circuitry that generates Coarse Track has hysteresis.

This signal is used to detect track crossings in the seek mode. The track difference counter is decremented when Coarse Track goes true.

If the counter is decremented accidentally, the drive will make a seek error. Therefore, the edges of Coarse Track are processed before they are used to decrement the counter.

This circuit is physically located on the M7707 module (Figure 4-10). Move is true (high) during the seek. Normally, the true-going edge of Coarse Track will set the flip-flop and trigger the one-shot which decrements the counter. Fine Track must come and go before another edge of Coarse Track will be recognized. Fine Track goes true when the heads are within 5.0 percent of the track center. It has a hysteresis of 100 mV.

Once Fine Track has gone away, the circuit will accept another edge of Coarse Track whether it is a valid edge or not. But if an invalid edge sets the flip-flop and decrements the counter, then the next valid edge will not be accepted because the flip-flop will already be set.

4.3.1.10 D/A Converter and Profile Function Generator – This circuitry on the M7729 module converts the digital value of cylinder difference to an analog voltage. The analog voltage is the command voltage presented to the servo system for seek operations or offsets.

The profile function generator converts the D/A converter output to a voltage that is approximately proportional to the square root of the distance to go to arrive at the desired cylinder. This resultant signal represents the velocity command.

For offsets, however, analog switches open the nonlinear feedback elements and switch the function generator to a linear command corresponding to the offset code.

The input to the D/A converter is the lower 6-order bits from the difference counter. These 6 bits provide the difference count up to a maximum of 63. Head positioner velocity command is proportional to approximately the square root of cylinder difference up to a maximum velocity of 114.3 cm/second (45 inches/second) at a cylinder difference of 63 or greater. For all cylinder differences greater than 63, velocity command is constant at 114.3 cm/second (45 inches/second). Gating on the M7707 decodes all differences greater than 63 to provide a logic 1 on all input lines to the D/A converter.

The circuit implementation of the profile is shown in Figure 4-11. The track difference count is converted to analog and used as an input to E2. The larger the difference count, the more positive the velocity command becomes. This biases more diodes into the ON state and effectively puts more resistors in parallel with R. This reduces the closed loop gain of E2 which produces the desired function.

Additional waveform smoothing is obtained by integrating the Tachometer signal. This integrator is reset when the D/A is updated with a new difference count. Therefore, the output of the integrator is the distance that the carriage has moved since the last track count update. Since this signal is proportional to distance, it can be added directly to the D/A output to make a smooth signal. Therefore, this circuit is referred to as the *fill-in-the-steps* circuit. This increased resolution is only needed on the last track before detent but is in the circuit for the entire seek.

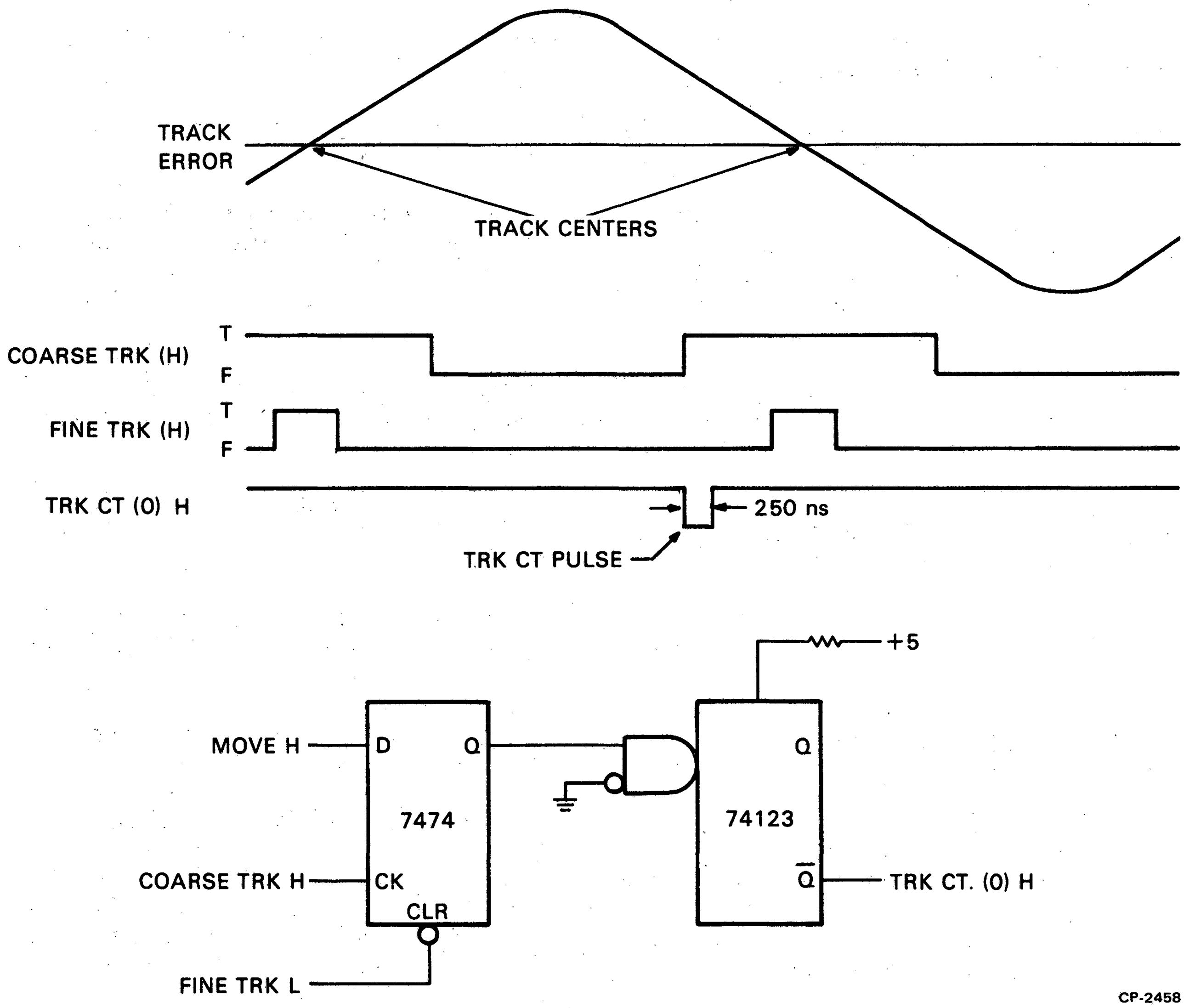
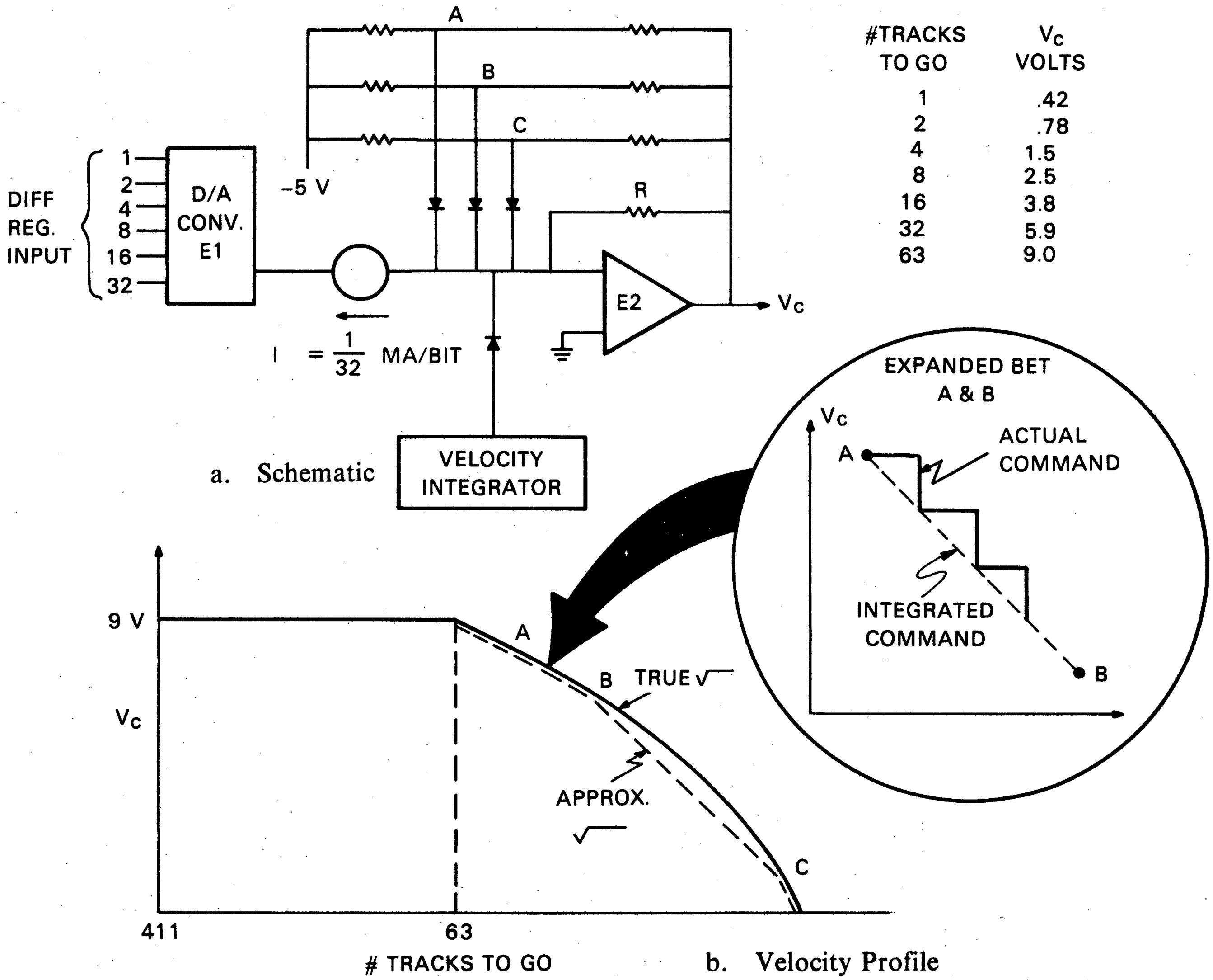


Figure 4-10 Track Counting



#TRACKS TO GO	V_C VOLTS
1	.42
2	.78
4	1.5
8	2.5
16	3.8
32	5.9
63	9.0

a. Schematic

b. Velocity Profile

Figure 4-11 Velocity Generator

As seen in Figure 4-11, a blowup of the actual and integrated velocity profile over a finite interval (e.g., A to B in the blowup) shows that the integrated command results in a smooth deceleration of the head positioner.

Figure 4-12 shows velocity integration (smoothing of the step function deceleration command) accomplished by adding a sawtooth waveform to the velocity command output of the velocity function generator.

4.3.1.11 Servo Analog Multiplexers and Low-Pass Filter – The analog multiplexer circuitry comprises a group of switched field-effect transistors (FETs) that provide selective control of the three major servo functions performed by the linear positioner, viz., seek, detent, and offset. The inputs to the source select circuits are shown in Figure 4-13.

The summing amplifier provides a summation of switched inputs and provides the gains required to develop the required command for the linear motor. The low-pass filter at the output of the source selector inhibits oscillations within the drive.

4.3.1.12 Load/Unload Tachometer Amplifier – This circuitry on the M7729 amplifies the difference between the two coils of the heads load/unload tachometer.

4.3.1.13 Heads Load/Unload Tachometer – The heads load/unload tachometer (Figure 4-14) is a linear magnetic transducer whose output is proportional to carriage velocity. The purpose of this device is to provide velocity feedback to the head positioning servo during the loading and unloading of the heads in the region from heads home to the outer limit.

The tachometer operates by the coil cutting magnetic lines of force of a permanent magnet, inducing an output voltage proportional to the number of lines cut per unit time, i.e., to velocity.

Physically, the tachometer consists of a permanent magnet and two coils, only one of which is involved in the velocity determination. The second coil, like the first, is exposed to any external fields whose effect would be to introduce error in the velocity feedback loop. The output of this second (bucking) coil is of opposite polarity to the first. The difference of the signals of the two coils is taken to cancel, to a large extent, the effects of any field other than that of the tachometer magnet.

4.3.1.14 Velocity Circuitry – The velocity circuitry on the servo analog (M7729) module comprises:

1. The automatic gain control (AGC) circuitry for the light-emitting diode (LED) of the phototransducer

2. Amplifiers, differentiators, multiplexing of differentiated signals for deriving carriage velocity.

Automatic Gain Control – The power dissipated in the motor on repetitive seeks is inversely proportional to the fourth power of the access time. A 10 percent change in the access time will produce a 46 percent change in the power. Therefore, it is important to have accurate velocity information.

The photo devices will change their sensitivity with temperature and time. An automatic gain control circuit is provided to keep this from changing the scale factor of the tachometer. It monitors the amplitude of the predifferentiated signals and adjusts the current through the LED to keep the amplitude of the signals constant.

The current for the LED is generated with a D/A converter. A counter provides the input for the D/A converter. Counting up causes the sine and cosine to become larger and counting down causes them to become smaller.

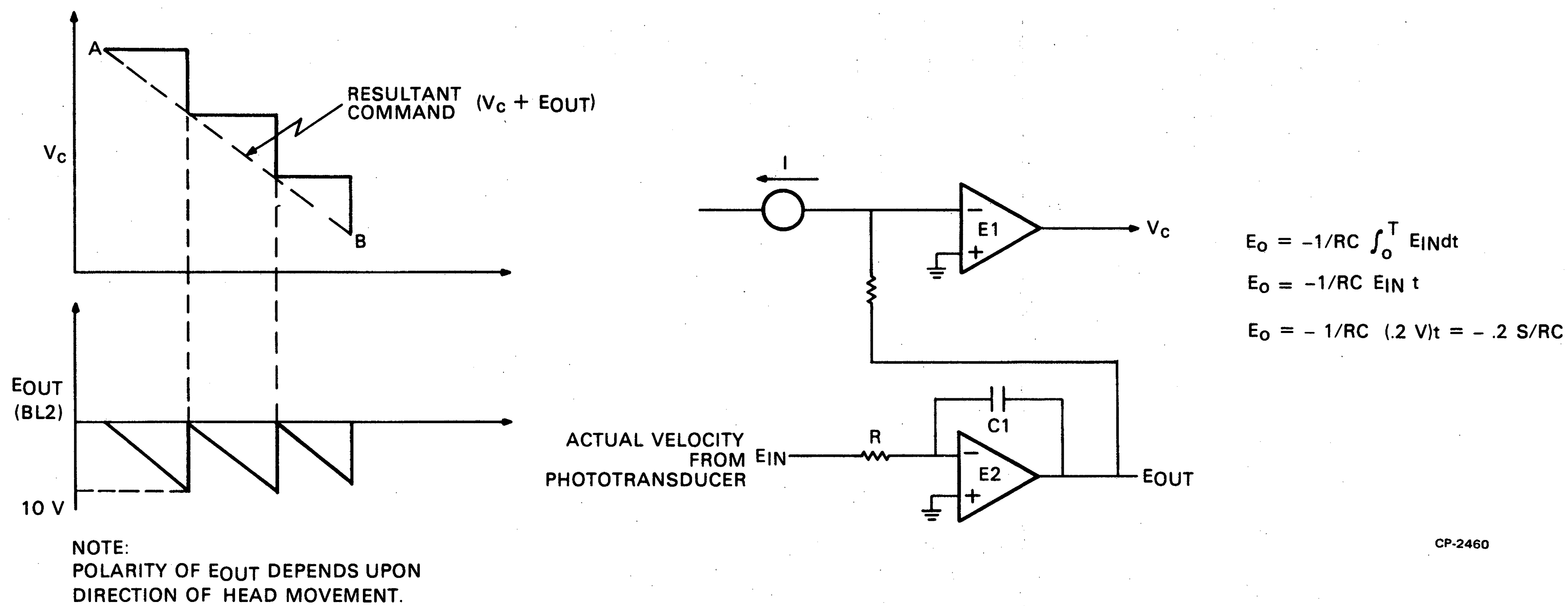


Figure 4-12 Velocity Integrator of Velocity Function Generator

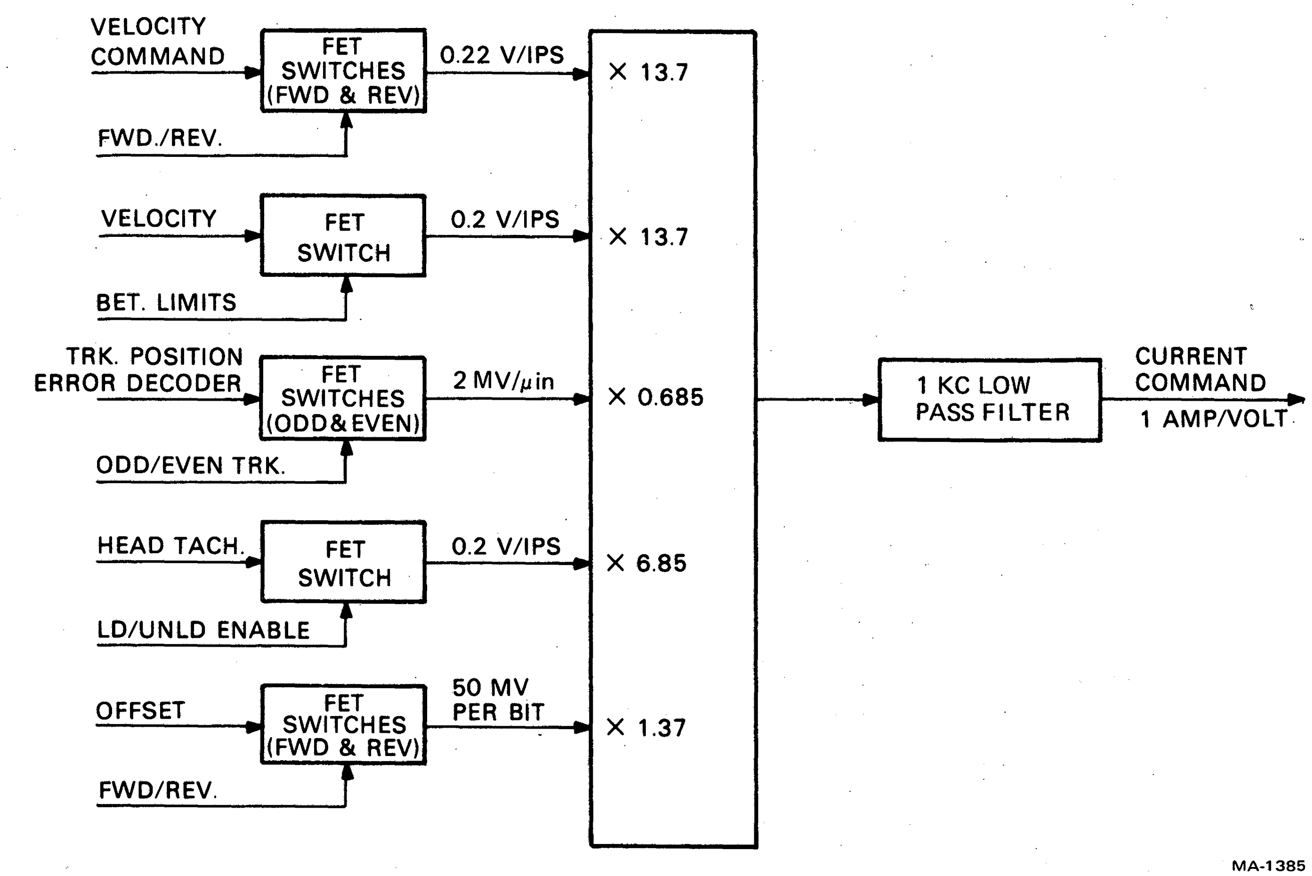


Figure 4-13 Summing Amplifier of Servo Analog Multiplexer and Filter

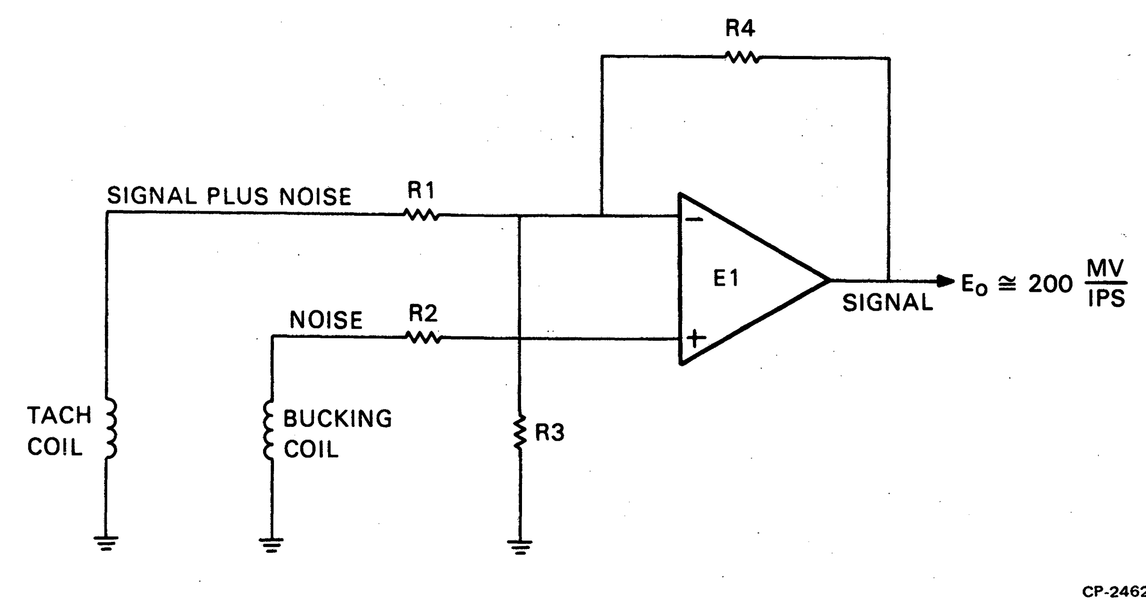


Figure 4-14 Heads Load/Unload Tachometer Schematic

The counter counts one way or the other when both the sine and cosine are equal to each other at the 3/4 light point as shown in Figure 4-15.

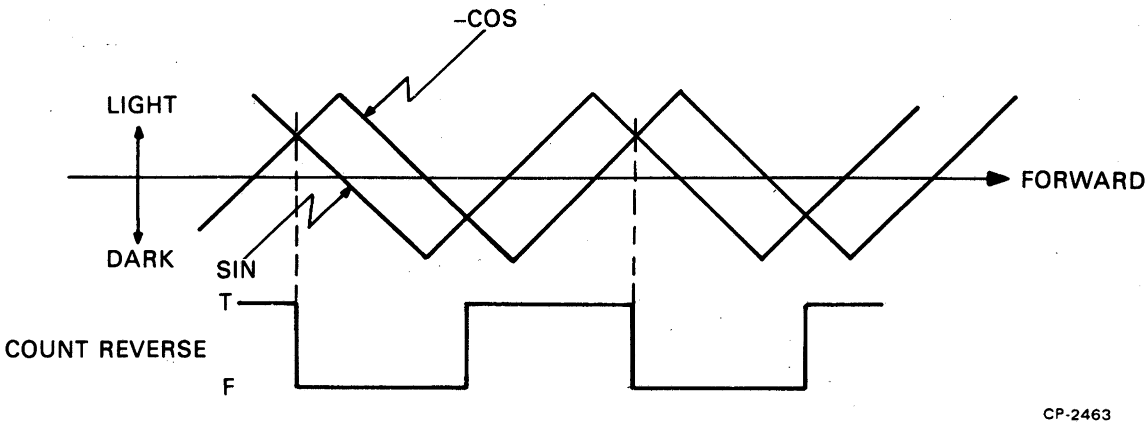


Figure 4-15 LED AGC Counter Waveforms

False-going edges of the logic signal Count Reverse cause the counter to count when the carriage is moving forward. True-going edges cause the counting in the reverse direction. This logic signal is true when the sine is more positive than the inverted cosine.

At the appropriate edge of Count Reverse, the circuitry determines whether the sum of the sine and -cosine is larger or smaller than 10.2 V. This information is stored in a flip-flop. The pulse that counts the counter is delayed from the edge of count reverse by a one-shot until the direction information is stable and then it is steered to the correct input of the counter by the magnitude information in the flip-flop.

The AGC circuitry is disabled at the end of the seek. The one TRK flip-flop does not allow it to be operated again until the carriage has moved 1/4 track on the next seek. This prevents the forward and reverse logic signals from causing a false count at the start of the seek.

The AGC adjusts the amplitude of the sine and cosine based on the average of the two. Thus, if one becomes slightly larger for some reason, the circuitry makes them both smaller so that the average is correct. The servo does not have time to respond to the individual waveform segments at high velocities and so the average of the sine and cosine is the crucial parameter.

Phototransducer Circuits – The transducer produces two waveforms (Figure 4-16) that are triangular as a function of distance. They are 90 degrees apart. These waveforms are differentiated to produce square waves that have an amplitude proportional to the frequency of the triangles which is proportional to the velocity. These are multiplexed together to produce the Velocity signal. The multiplexing is controlled by the undifferentiated signals so that it is valid even at zero velocity.

Both polarities of both signals are formed before the differentiation to minimize offsets at the expense of some additional circuitry.

The Input signals to the M7729 module are negative-going triangles of 0.5 V peak-to-peak. The input stage level shifts them so that they are symmetric around zero. It also amplifies them so that the extrapolated waveforms are 20 V peak-to-peak. The actual waveforms will only be about 17 V peak-to-peak because the triangles are slightly rounded at the peaks.

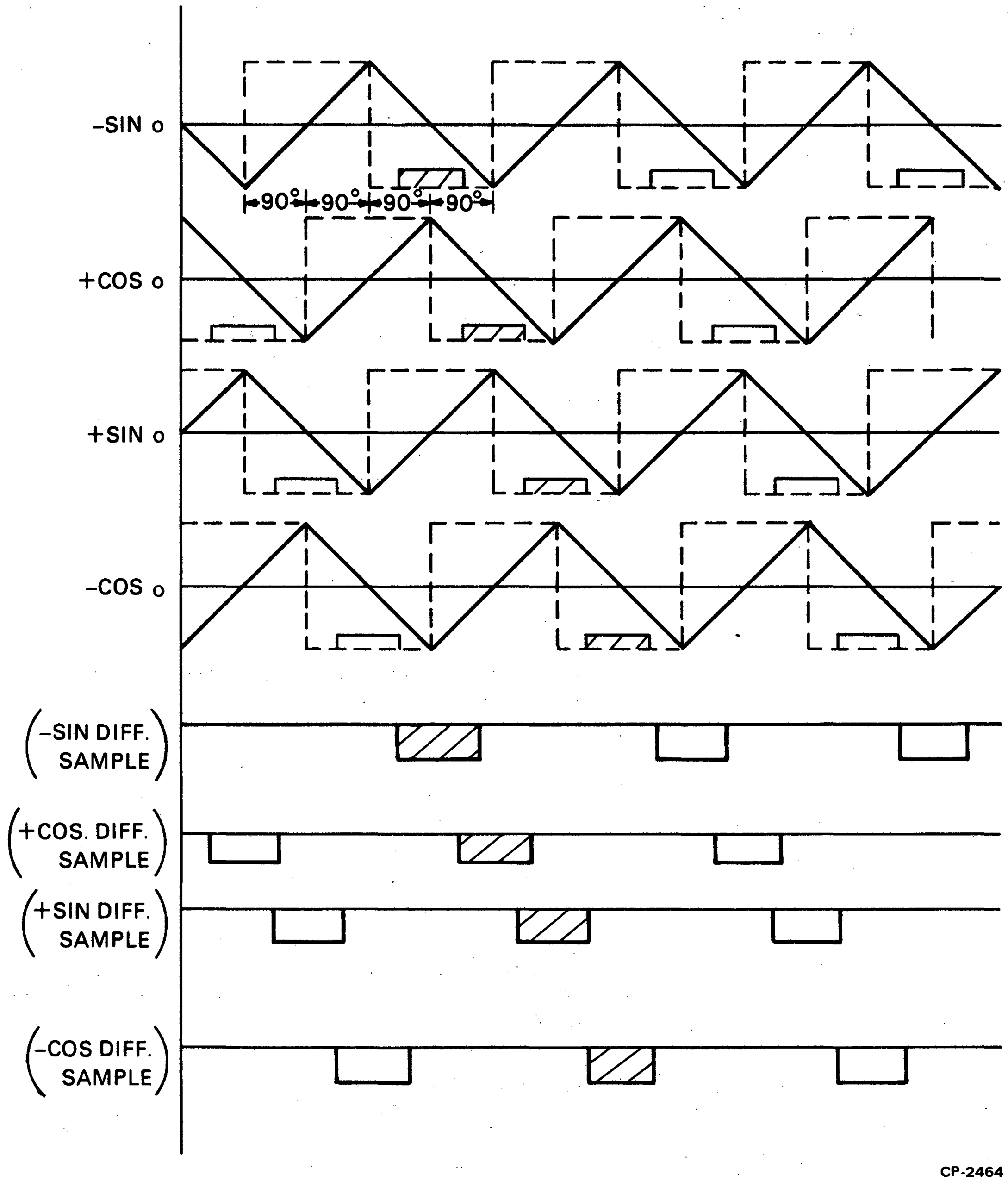
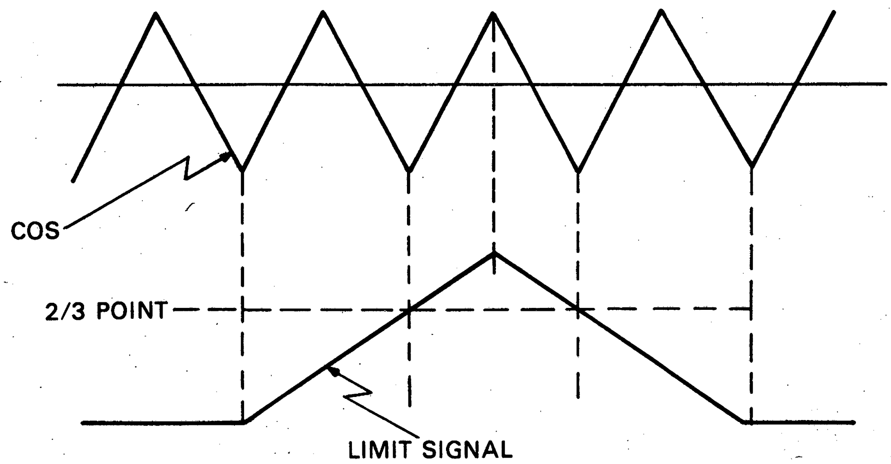


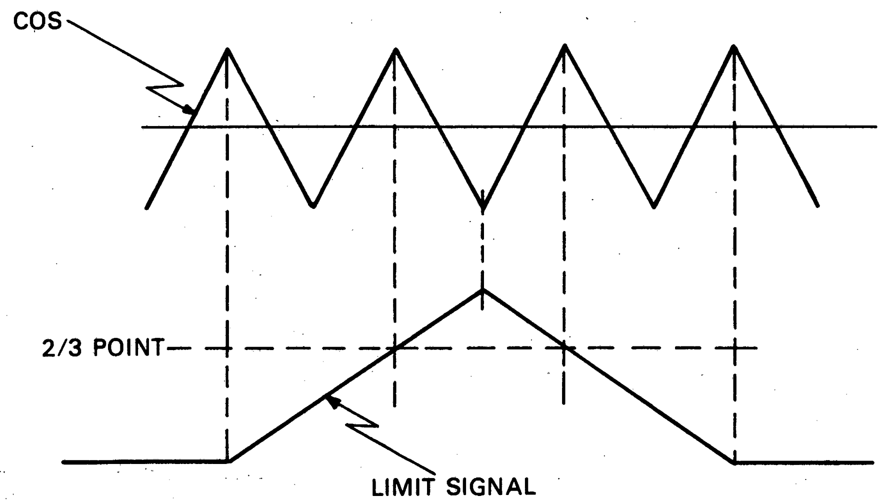
Figure 4-16 Velocity Multiplexing Timing Diagram

The optical transducer provides a triangular pulse (as a function of distance) which is used as a limit indication. The pulse occurs at two positions: slightly toward the spindle from track 410 and slightly toward the home position from track 0. These two pulses line up differently with the cosine as shown in Figure 4-17.

The peak of the inner limit lines up with a positive peak of the cosine waveform and the peak of the outer limit lines up with a negative peak of the cosine.



a. Inner Limit (Toward Spindle)



b. Outer Limit (Toward Home)

CP-2465

Figure 4-17 Limit Signal Waveforms

When the circuitry detects that the amplitude of the limit pulse is 2/3 of the nominal peak, it examines the polarity of the Cosine signal. If the cosine is positive at that time, the outer limit flip-flop is set. If the cosine is negative, the inner limit flip-flop is set. Figure 4-18 shows the limit signal circuitry and waveforms.

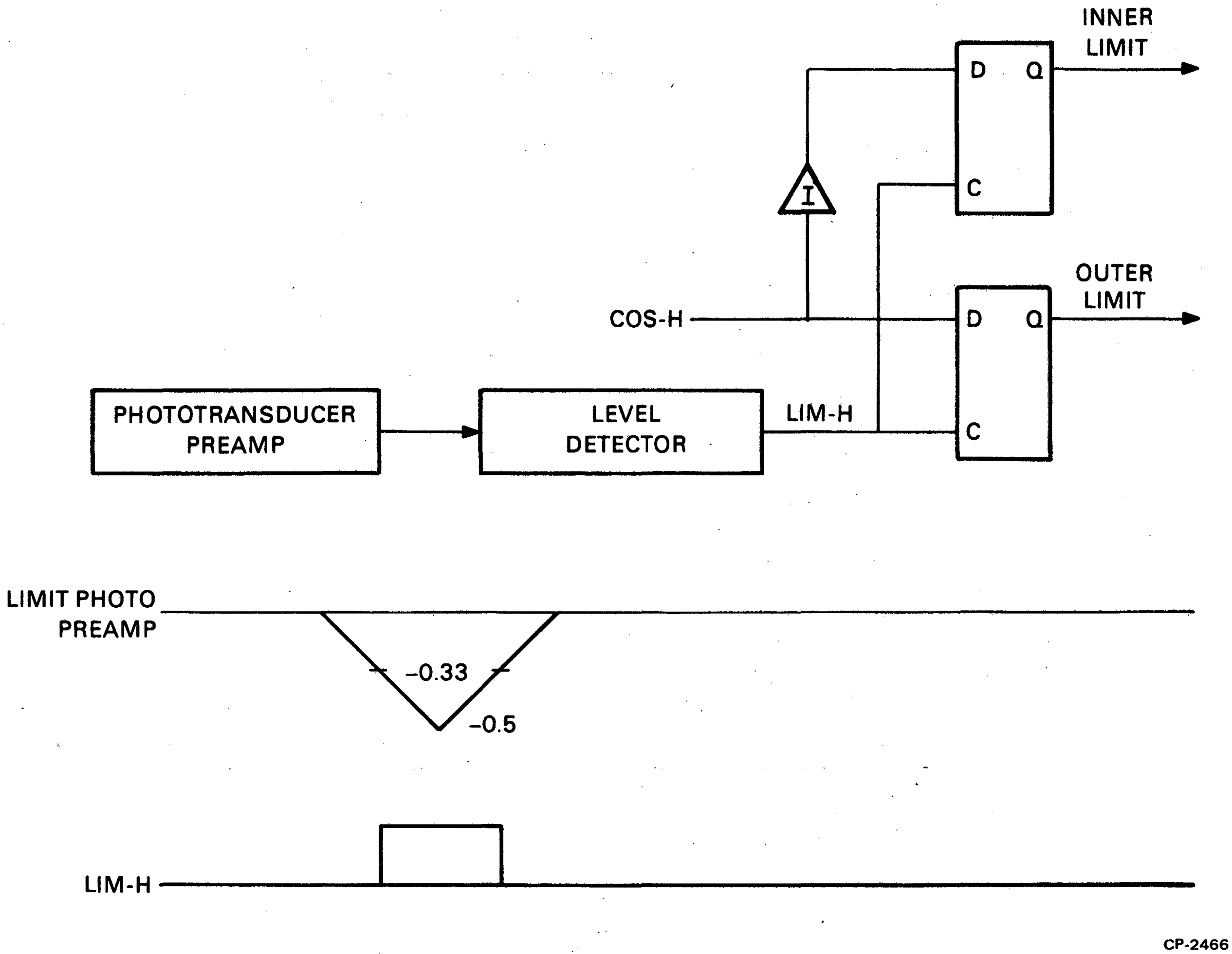
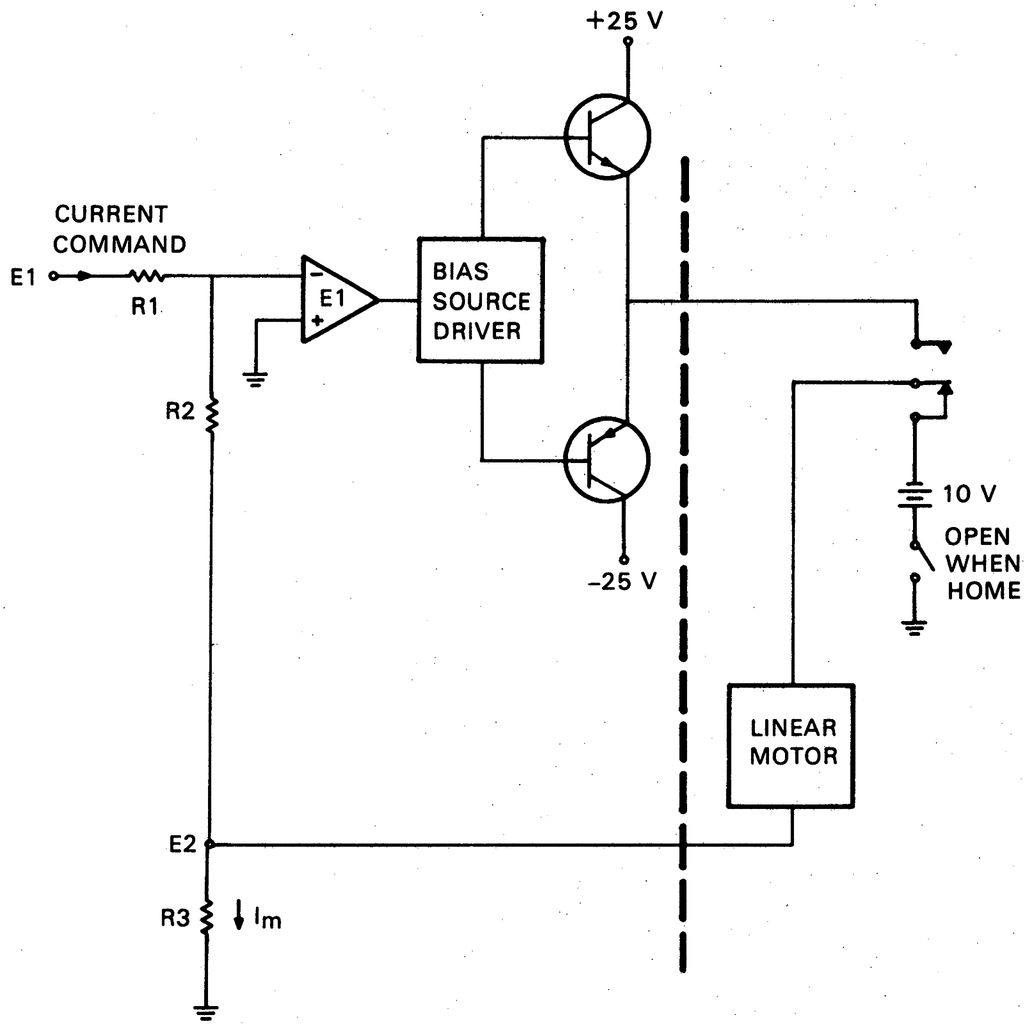


Figure 4-18 Limit Circuitry and Waveforms

4.3.1.15 Power Amplifier - Figure 4-19 is a schematic of the RK06 power amplifier. The power amplifier can be understood most easily by thinking of it as an operational amplifier connected in the inverting configuration with R2 being the feedback resistor and R1 being the input resistor. The motor is part of this operational amplifier and the load is the current sense resistor R3. Thinking of it in that way, it is apparent that the voltage gain is R2/R1 = 5.11K/24.9K = 0.21. The motor current is equal to the output voltage divided by the current sense resistor R3. Therefore, the gain from input volts to motor current in amperes is (R2/R1)/R3 $\cong$ 1.

4.3.1.16 Servo Release Switch and Maintenance Switch

Servo Release Switch (S1)
The servo analog module (M7729) has an edge-mounted servo release switch whose handle is set toward MAINT when it is desired to move the carriage by hand while observing signal outputs, or under any conditions where servo motion could harm service personnel or the drive.



GAIN CONSTANT:

1. $\frac{E1}{R1} = \frac{E2}{R2}$

2. $E2 = I_m \bullet R3$

3. $\frac{I_m}{E1} = \frac{R2}{R1 \bullet R3} = \frac{1.01}{\text{amp/volt}}$

MA-1287

Figure 4-19 Linear Motor Power Amplifier Functional Schematic

Safety Switch
The servo analog module M7729 also has a safety switch edge-mounted on the board. This switch is also set toward MAINT when performing head adjustments or other service operations in which inadvertent carriage motion could harm personnel or damage the drive. When in this position, the switch inhibits the servo unsafe circuitry in the drive, preventing the accidental unloading of heads under battery power. This switch also write protects the drive; i.e., if the switch is left in its disconnect (MAINT) position, the drive will remain write protected and the WRITE PROT indicator will remain lit. If a write command is subsequently received, write lock error will occur.

4.3.1.17 Servo Preamplifier – The servo preamplifier is a small metal package whose input is a low-level (2 mV peak-to-peak) differential tribit signal train from the dedicated servo surface of the disk cartridge.

The basic function of the preamplifier is to amplify this low-level input to an output at peak-to-peak levels of 400 mV. This output feeds the AGC amplifier and filter network of the track position detector/phase lock oscillator. Details of the subsequent signal processing in track-position detection are given in Paragraph 4.3.1.28.

Figure 4-20 is a simplified block diagram showing the basic elements in the servo preamplifier. The input biasing network sets the operating level of the El 733 differential video amplifier at 6 Vdc, nominal. Amplifier gain is 200.

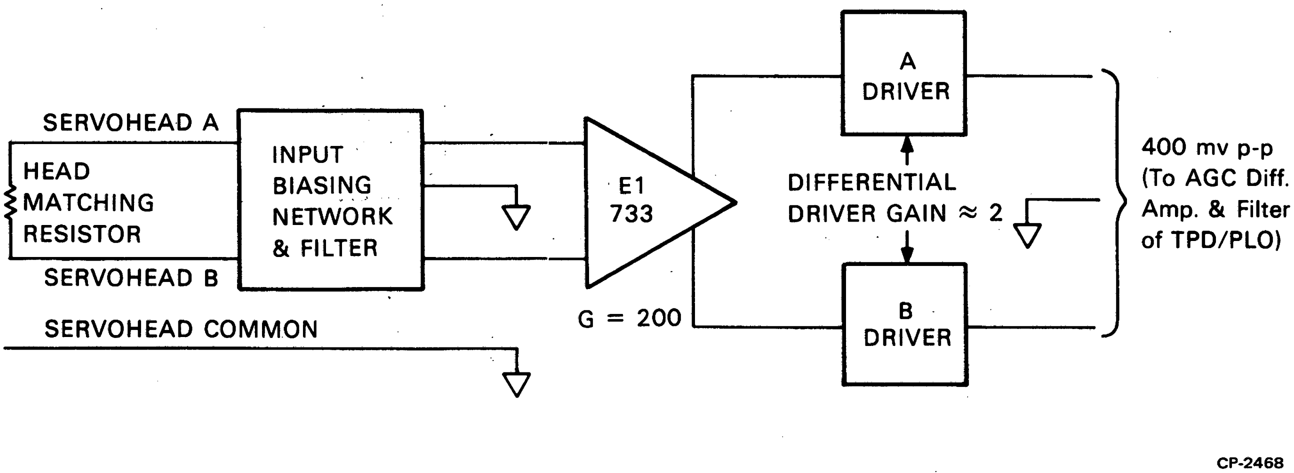
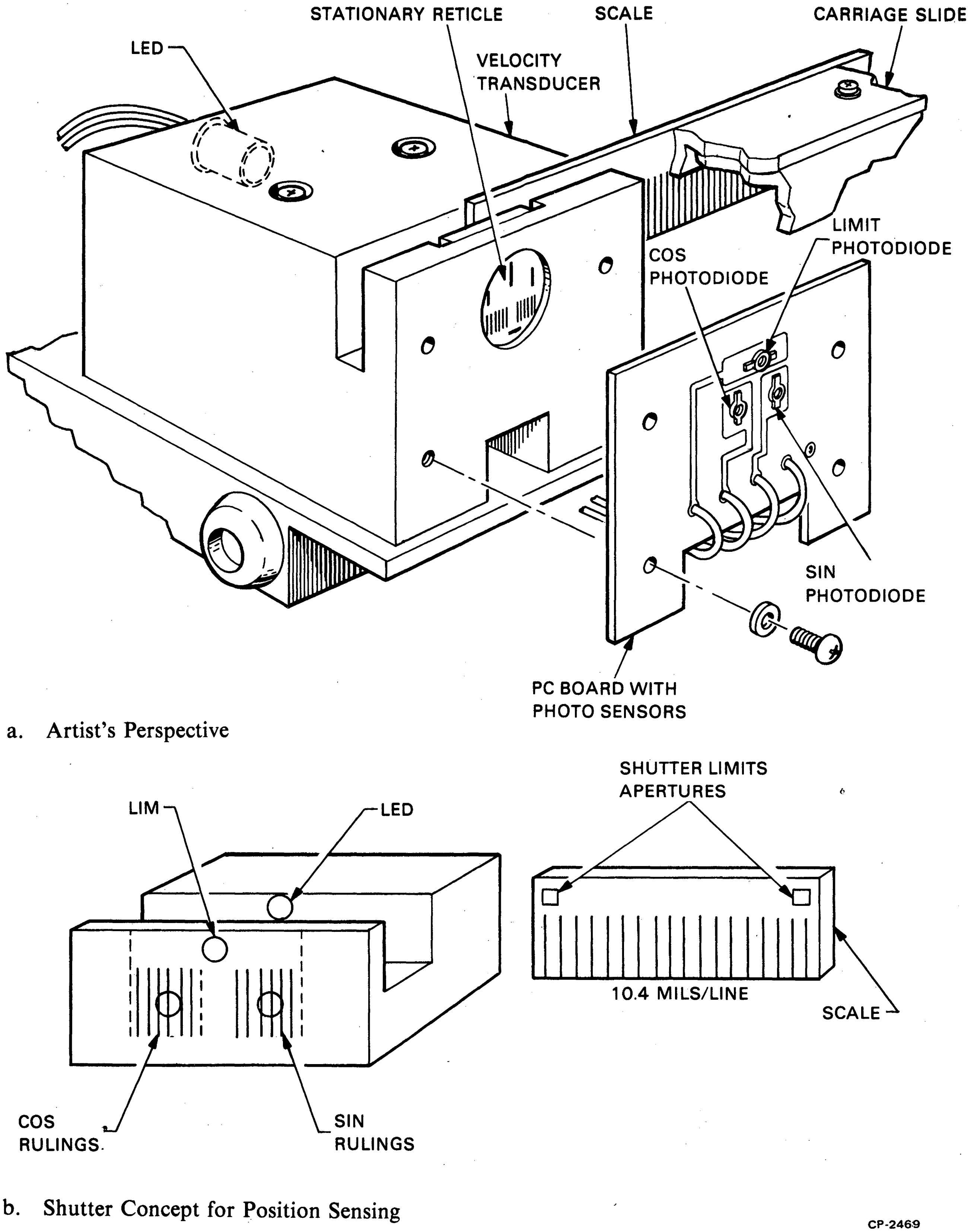


Figure 4-20 Servo Preamplifier Block Diagram

4.3.1.18 Phototransducer and Preamplifier – The phototransducer is used for deriving velocity feedback for the head positioner during the time when the heads are between the outer limit and inner limit. Feedback velocity information during the period when heads are outside this zone is provided by the load/unload tachometer (Paragraph 4.3.1.13).

The glass phototransducer is a U-shaped plastic module. As seen from the rear of the drive, the left-hand arm of the U (Figure 4-21 illustrates the design principle) contains a single LED. On the other arm of the U is a limits photodetector, a fixed glass slide with sine and cosine rulings and corresponding sine and cosine photodetectors. A 7.6 cm (3 inch) long glass slide attached to the carriage and having the same glass ruling pitch acts as a shutter that modulates the LED output reaching the sine and cosine detectors after passing through the interstices between the fixed and moving glasses.



a. Artist's Perspective

b. Shutter Concept for Position Sensing

CP-2469

Figure 4-21 Phototransducer for Velocity Feedback Loop

Two small light slots in the moving slide permit light to reach the photodiode limits detector when inner and outer limits are reached.

4.3.1.19 Carriage Home-Lock Assembly – A solenoid-operated home lock (Figure 4-1) mechanically restrains the carriage against inadvertent motion whenever heads are commanded to remain at the home position, and ensures that the heads will remain safely in their home position during shipment. The solenoid is actuated only when the control logic has determined it is safe to load the heads.

4.3.1.20 Servo Head Assembly – The servo head assembly consists of the heads support subassembly and the four heads (three data recording and one dedicated servo surface heads). The heads, from top to bottom of the assembly, are designated as 0, 1, S, and 2, respectively. Head S (the servo head) is a read-only sensor, receiving the prerecorded tribit message from the top surface of the bottom disk.

The heads are individually mounted in the slots provided at the forward end of the carriage. Each spring-loaded head bracket has a short ramp section which, when the heads are retracted, rides through slots in the cam tower and cause the heads to separate. When the heads are loaded onto the disk (Figure 4-22), the air flow caused by disk rotation exerts a pressure (air bearing) counteracting the spring-loaded headarms and causing the heads to *fly* approximately 50 microinches from their respective disk surfaces. With disk rotation held constant, the heads remain at this relatively fixed distance from the disk surfaces.

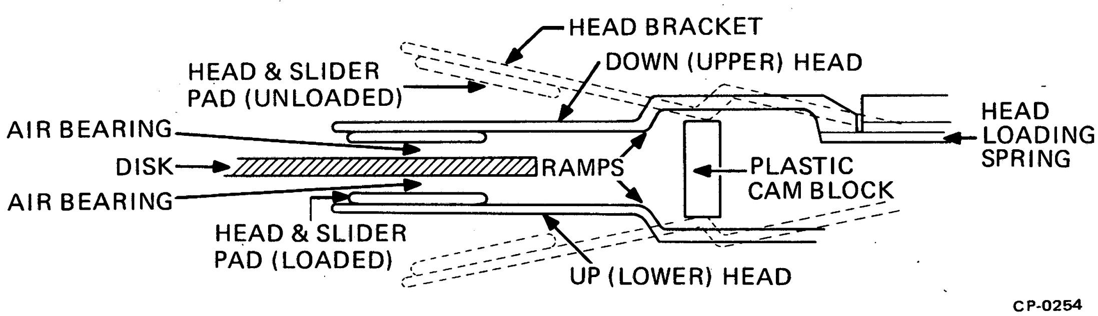


Figure 4-22 Head-Loading Mechanism

4.3.1.21 Linear Motor, Carriage, and Coil Assembly – The linear motor of the disk drive (Figure 4-1) provides the motive force for head positioning. The heads are supported on a carriage that is integrally attached to the moving coil of the linear motor. Structurally, the motor comprises a permanent magnet through which the coil moves in and out in response to currents whose magnitude and polarity are determined from the positioning subsystem electronics. The carriage, driven by the moving coil of the linear motor, rides on a forward (inner) pair of roller bearings and an identical aft pair, both pairs being supported by a centerless-ground guide rod.

Lateral stability and support are provided by two vertically oriented bearings that ride on ways paralleling the guide rod. A pair of rubber bumpers on the coil, and a corresponding pair on either side of the ways at the forward limit of carriage travel provide a high degree of shock isolation against carriage impact.

4.3.1.22 Difference Amplifier and Filter – This circuitry on the M7708 module accepts the differential tribit Input signal from the servo preamplifier and provides further amplification and low-pass filtering for the purpose of deriving other signals from the tribits. The output gain of the circuits is controlled by an automatic gain control (AGC) which is derived from the sum of the peaks of the A and B pulses of the Tribit signal. The Input signal to the difference amplifier and module is the tribit waveform shown in Figure 4-23. The relative amplitudes of the A and B pulses shown in the figure contain the position information, while the sync pulse is used for the timing reference. As is seen in the figure, the A pulse is maximum and the B pulse is minimum whenever the servo head is positioned –1/2 track from the nominal *even* data track (i.e., +1/2 track from nominal odd track) centerline. B is maximum and A is minimum when the servo head is positioned +1/2 track from the nominal *even* data track (i.e., –1/2 track from the nominal odd track) centerline. The sync pulse amplitude remains nearly constant at all times.

4.3.1.23 Phase Detector – The phase detector circuit represents one of the three main circuits of the phase-lock oscillator. This detector compares the phase of the tribits timing pulse with the output of the frequency-divided voltage-controlled oscillator (VCO) frequency. The input SVO PULSE is phase compared with the VCO frequency divided by 32, yielding the signal SVO CLK/2. The phase detector drives charge pumps that add or subtract voltage on a filter at the VCO control voltage input, such that the correct average frequency and phase relationships exist between SVO PULSE and SVO CLOCK.

Figure 4-24 is a block diagram of the phase-lock oscillator (PLO) timing circuits. The phase detector compares the phase of the SVO PULSE input with that of SVO CLK/2. Phase detector logic and timing relationships are shown in Figure 4-25. The phase detector produces two pulses for each cycle of the input, a "go faster" (up) pulse and a "go slower" (down) pulse. If the high-to-low transition of SVO CLK/2 occurs in the center of the SVO pulse, the "go faster" pulse will be of the same width as the "go slower" pulse and the oscillator will neither speed up nor slow down. But, if the oscillator slows down for some reason, SVO CLK/2 will occur later. This condition will cause the "go faster" pulses to grow wider. The effect of this condition is to make the oscillator go faster and to bring the high-to-low transition of the SVO CLK/2 back to the center of the SVO PULSE.

The "go faster" and "go slower" pulses are converted to another form before being used to control oscillator frequency. The charge pumps are used for frequency control. One of the pumps is shown in Figure 4-26. The transistors are biased with 5 V on the base of Q2 and 4 V on the base of Q1 (relative to the local common, which is -5 V with respect to the normal common). This biasing turns Q2 on and Q1 off. When "go slower," L goes low, and Q2 turns off, which turns Q1 on. The current conducted by Q1 is the output.

The other charge pump is referenced to +15 V, instead of -5 V, and produces a current in the opposite direction. The "go faster" pulse passes through a delay line such that, in equilibrium, both charge pumps turn on and off at the same time. This condition results in a zero net current.

4.3.1.24 Voltage-Controlled Oscillator (VCO) – The VCO receives the signal from the filtered output of the charge pumps which is used to control the VCO frequency. The nominal output frequency of the VCO is 8.6 MHz, its period being 116 ns. This signal becomes the Write Clock signal which is used to clock and synchronize write data to the rotational speed of the disk cartridge.

4.3.1.25 Frequency Divider – This circuit receives the VCO frequency and produces an output signal 1/32 the input frequency. The resulting frequency is called SVO CLK/2. This signal is used as a feedback to the phase detector circuit for comparison with the timing pulse from the difference amplifier and filter. It is also used in conjunction with SVO CLK, which is twice this frequency, in the index and sector circuits of the M7705.

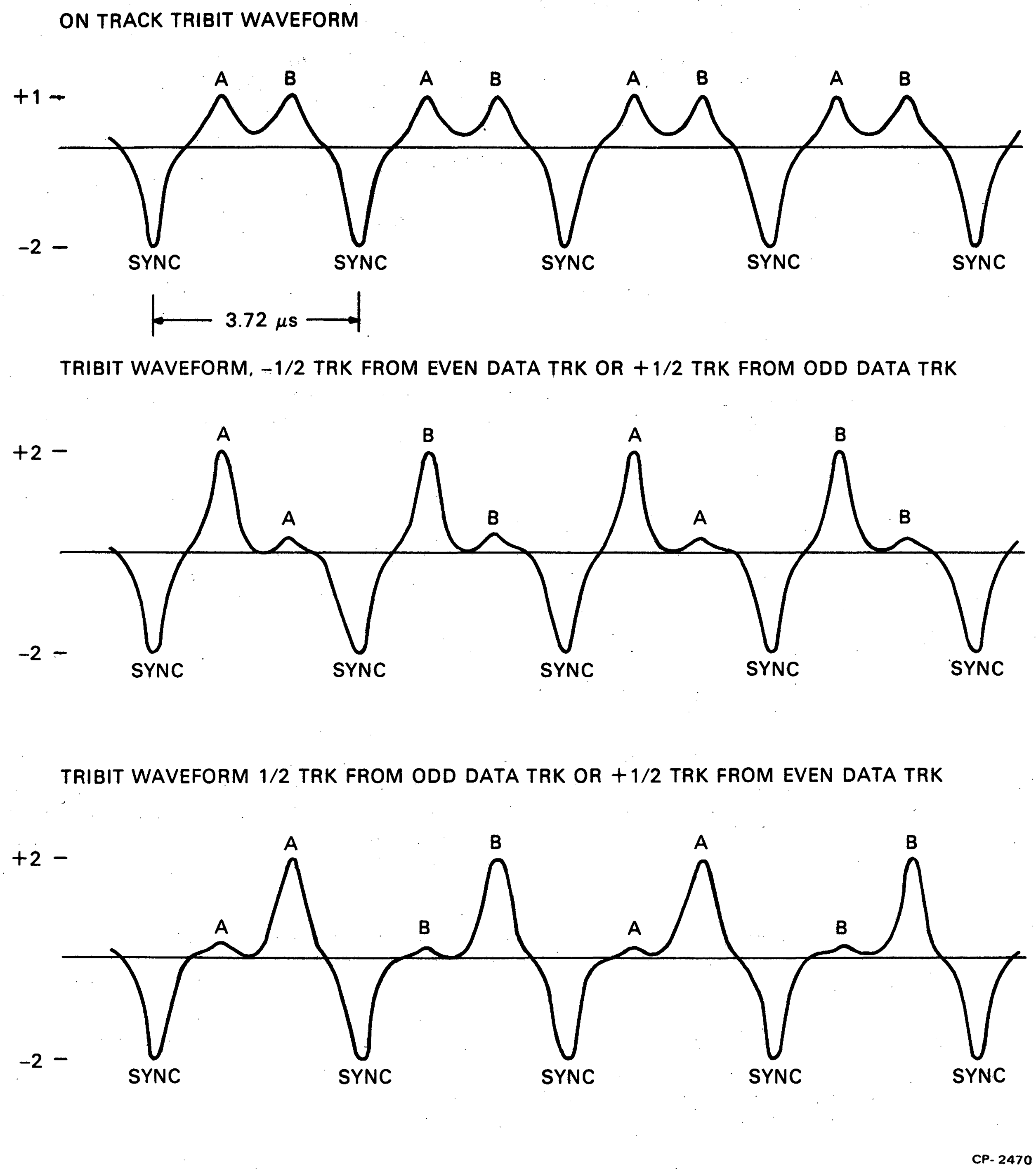


Figure 4-23 Tribit Waveforms

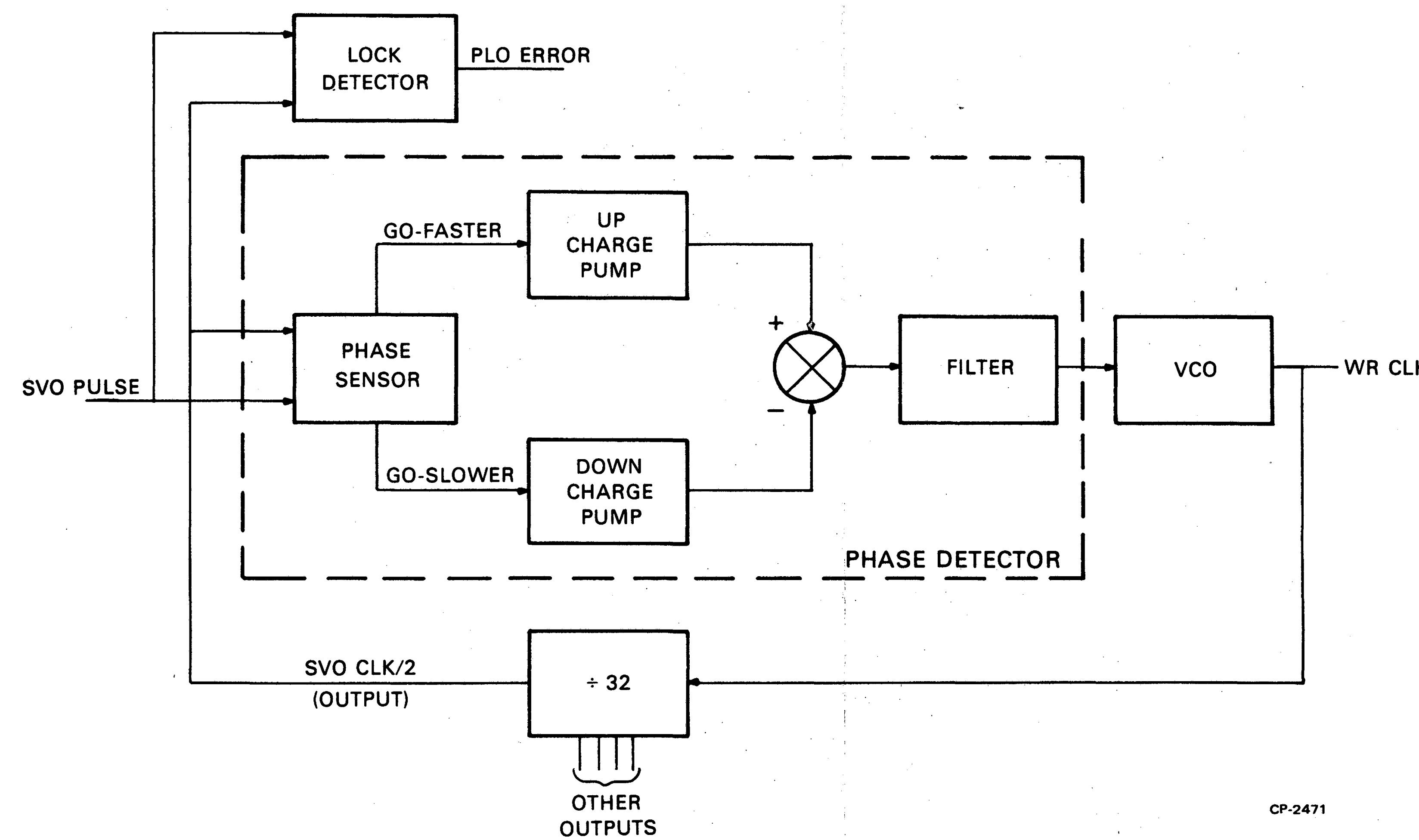


Figure 4-24 PLO Block Diagram

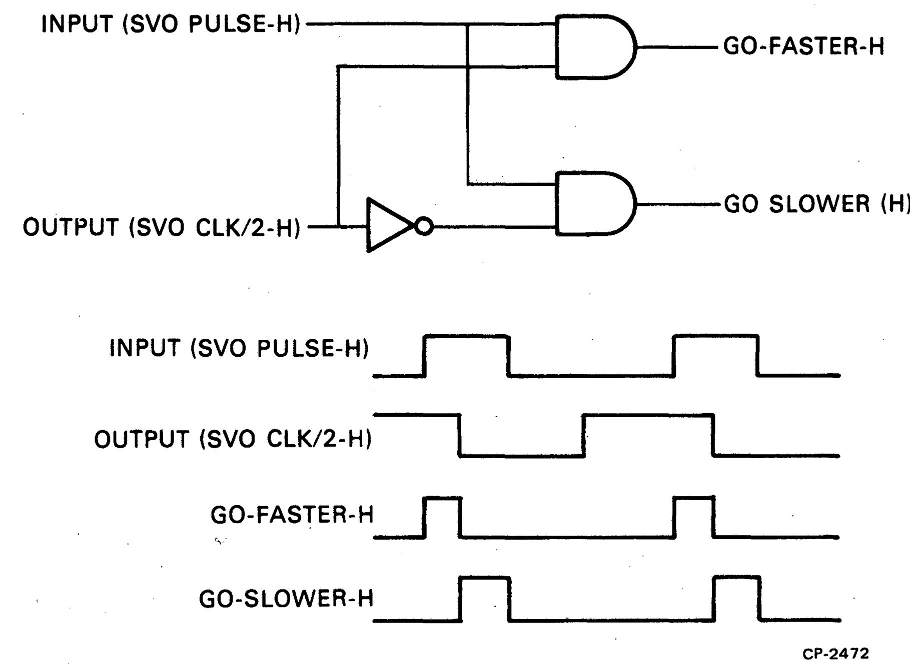


Figure 4-25 Phase Detector Logic and Timing Waveforms

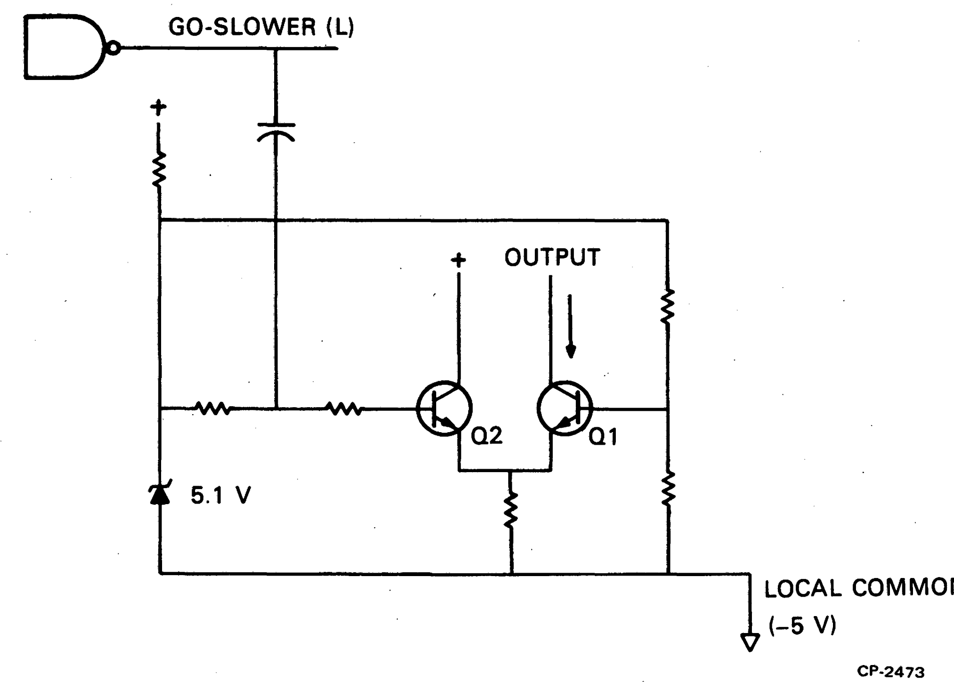


Figure 4-26 Charge Pump Schematic

4.3.1.26 A and B Peak Detector and Integrator – These circuits sample the peaks of the A and B tribit pulses and integrate or hold these values between pulses. The peak values of these pulses are used to derive the Track Error signal and a voltage for the automatic gain control of the difference amplifier and filter.

4.3.1.27 A–B Circuit – This circuit takes the difference between the A and B peak voltage values to yield the Track Error signal. The difference A–B represents the position of the servo head relative to the data track centerline. This difference, a function of servo head position (i.e., relative values of the A and B peaks), is referred to as track error. This signal serves as the input to the drive servo system in the detent or position mode. The difference signal A–B is also applied to the position detector circuits.

4.3.1.28 Position Detector – The position detector derives the Coarse Track, Fine Track, and Fine Track Delayed signals. Figure 4-27 shows the relationship of these signals versus distance except for Fine Track Delayed (Figure 4-28) which is a function of time. Coarse Track and Fine Track signals are used for deriving track count pulses which decrement the difference counter, and Fine Track signal is used to reset the forward flip-flop or reverse flip-flop.

The Fine Track Delayed signal is used for the detection of drive off-track error. This signal is asserted if the Fine Track signal is absent for at least 0.85 ms.

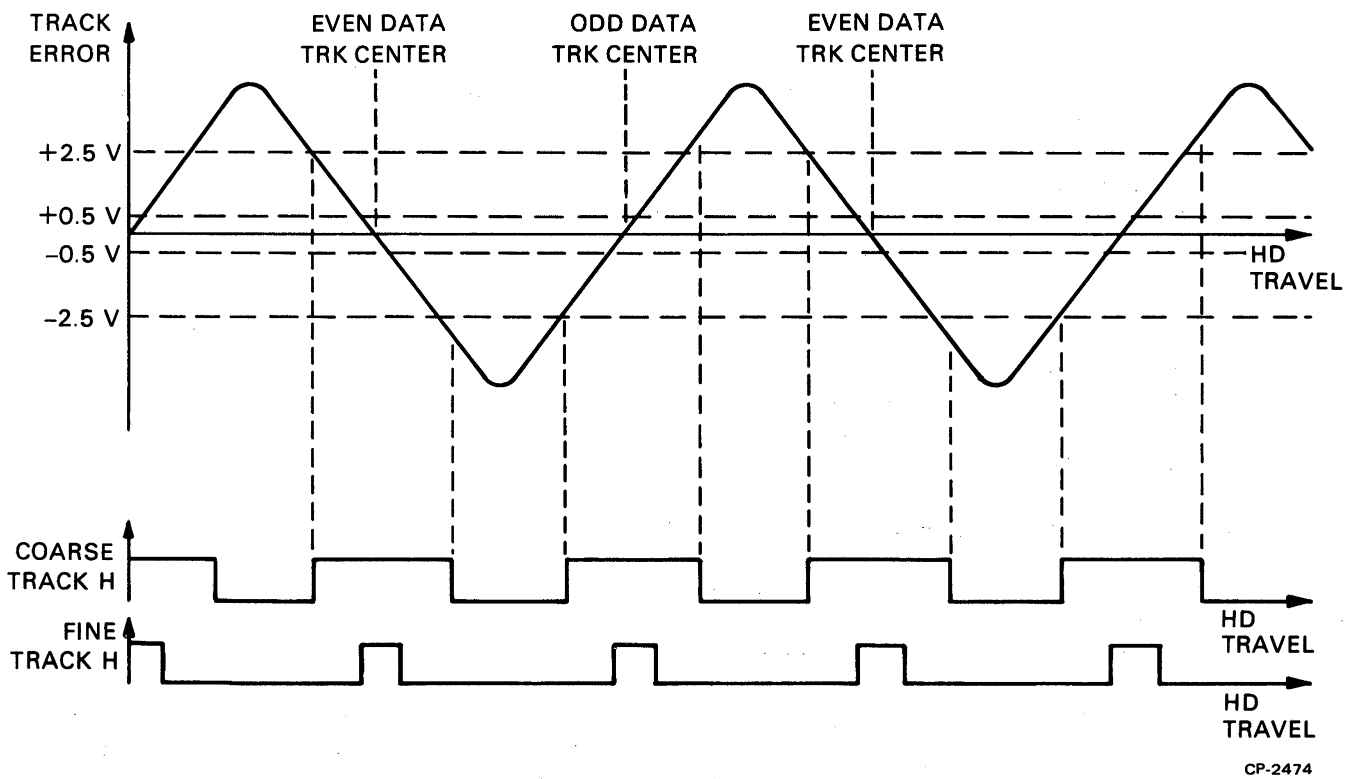


Figure 4-27 Position Signals

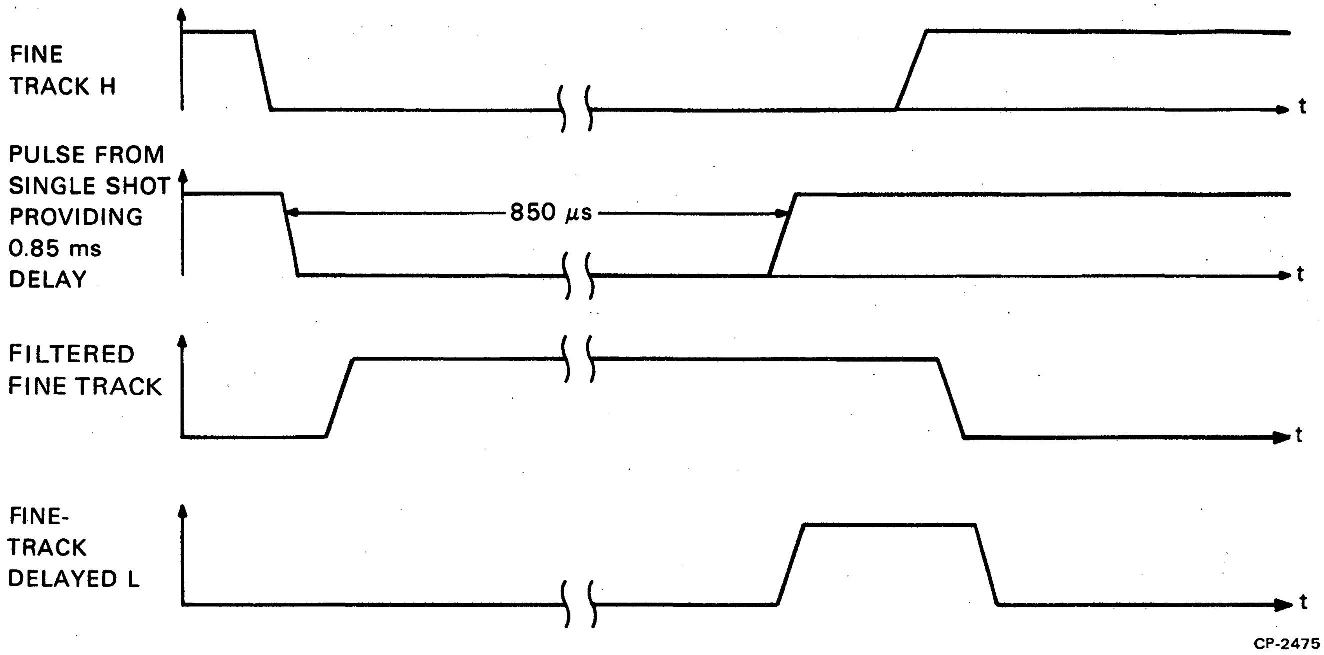


Figure 4-28 Fine-Track-Delayed Timing

4.3.1.29 A+B Circuit – This circuit provides the sum of the peaks of the A and B pulses for use as a control signal for the AGC of the tribit signal.

4.3.2 Positioning Operation

The following sections described the various operations pertinent to the positioning subsystem. These operations are:

1. Loading heads (Paragraph 4.3.2.1)
2. Unloading heads (Paragraph 4.3.2.2)
3. Recalibrate (Paragraph 4.3.2.3)
4. Seek (velocity mode) (Paragraph 4.3.2.4)
5. Detent (position mode) (Paragraph 4.3.2.5)
6. Offset (Paragraph 4.3.2.6).

The servo has three primary modes of operation: the detent mode, the seek mode, and head load mode.

In the detent mode (also known as the position mode or the track-following mode), the servo tries to hold the servo head centered over the boundary of two servo tracks. The Feedback signals are the track error from the servo surface and the velocity from the glass scale.

In the seek mode (also known as the velocity mode), the servo tries to move the carriage at a velocity that is a nonlinear function of position. This function is clipped at 63 tracks so that all positions equal or greater than 3 tracks away from the desired position command the same velocity. The servo has sufficient gain that the power amplifier saturates on acceleration and applies the full power supply voltage to the motor (less, of course, a small fixed drop in the power amplifier transistors).

In this mode, the glass velocity is fed back and compared with the function generator whose value is determined by the digital track count.

In the head-load mode, the velocity command generator puts out a constant voltage which is compared to the output of the magnetic head-loading tachometer to control the velocity. This magnetic tachometer works all the way back to the home position whereas the glass tachometer does not. This allows the velocity to be controlled in the region where the glass transducer does not provide velocity information.

4.3.2.1 Loading Heads – The heads may be loaded by either of two commands: (1) depression of the control panel RUN/STOP switch or (2) a command from the system, provided the RUN/STOP switch is depressed. Once the appropriate prerequisites are satisfied, i.e., the Unload Heads signal is negated (see Drive Control, Paragraph 4.2), head loading begins. At this time the load heads flip-flop on the M7707 will set as will the forward flip-flop and Enable Forward Servo signal of the direction-select circuitry. In addition, the home lock is now released. Because the difference counter is reset at this time, the servo command is for a low speed. As a result, the positioner now accelerates until the feedback from the load/unload tachometer equals the command and the heads move at between 11.2 and 20.3 cm/second (5 to 8 inches/second). This motion takes the heads down the head load ramp to the outer limit where the load/unload tachometer feedback is switched off and the phototransducer velocity feedback is enabled. Due to command differences, the velocity now slows to 2.5 cm/second (1 inch/second) until the heads reach the inner limit.

At the inner limit, the load heads and forward flip-flops are reset, the RTZ and reverse flip-flops are set, and the carriage is now commanded to move back to 2.5 cm/second (1 inch/second) to the outer limit.

At this point, the reverse flip-flop is reset, forward is set, and the carriage again advances forward until the Coarse Track signal is sensed where the positioner transfers from velocity mode to detent mode (Paragraph 4.3.2.5). At this point, the RTZ and Enable Forward Servo signals are negated.

4.3.2.2 Unloading Heads – The positioner will unload the heads from:

1. Release of RUN/STOP switch
2. Unload heads command from system
3. Any of several errors within the drive for which it would be unsafe to leave the heads loaded.

Whenever one of the three conditions above occurs, the unload head flip-flop on the M7705 is set immediately, causing any other positioning, if underway, to be discontinued. The reverse flip-flop is set, and the velocity command generator is set for a low velocity (the difference counter is reset). The heads accelerate to 2.5 cm/second (1 inch/second) if the heads are between the outer and inner limits and 12.7 to 20.3 cm/second (5 to 8 inches/second) if outside the outer limit. The positioner continues until it reaches the home position at which time the command is removed from the motor.

The positioner will unload the heads in an emergency manner if the ac power is interrupted or if a servo unsafe condition is sensed within the drive. For these cases, the rechargeable battery supply is applied to the linear motor directly to unload the heads. This is an open-loop condition in which the carriage moves without the benefit of velocity feedback.

4.3.2.3 Recalibrate – A recalibrate is performed by the system whenever it detects that the physical location of the positioner does not agree with the cylinder address register. For this operation, the drive responds by resetting the cylinder address register and cylinder difference counter on the M7707, setting the RTZ and reverse flip-flops. The positioner moves at 2.5 cm/second (1 inch/second) until the outer limit is sensed, then the reverse flip-flop is reset, the forward flip-flop is set, and the positioner proceeds forward until the first Coarse Track signal is sensed at which time the Enable Forward Servo signal is reset and the servo goes into detent (Paragraph 4.3.2.5).

The heads are now positioned at cylinder 0, which corresponds to the state of the cylinder address register.

4.3.2.4 Seek (Velocity Mode) – When a seek operation is to be performed, a seek command and desired cylinder address are transmitted to the drive. The new address is subtracted from the present address to obtain a digital difference that is converted into an analog voltage by the circuitry on the servo analog module. The serial subtractor performs the calculation. The cylinder difference register holds the calculated cylinder difference (i.e., the 1's complement number), and the carry logic determines the direction of head motion. The difference counter, which is preloaded with the cylinder difference for the seek, keeps count of cylinder difference as positioning proceeds, and provides the difference to the D/A converter and function generator.

The sequence of events on the M7707 in moving the head from an existing cylinder location to a new location is as follows.

1. The address enable flip-flop must be set.
2. The seek command flip-flop is set.
3. The new cylinder address is received by the drive and a serial difference with the present cylinder address is performed. The resultant difference is loaded into the cylinder difference counter and the desired cylinder address is loaded into the cylinder address register. The result of this operation by the cylinder address register, cylinder difference register, and difference counter is a binary number in which the final carry indicates direction and the sum denotes the number of cylinders to be traversed in the command seek.

The following example (using only three cylinder address bits in the interest of simplicity) shows the arithmetic of the logical operation performed.

	Decimal	**Binary**	**Operation**
Present cylinder address	7	111 → 111	None
Desired cylinder address	5	101 → 010	Invert
Difference	2	1 001	Sum
Direction indicated: Reverse		Carry ↗	

Since the carry is asserted at the end of the differencing operation, the sum must be incremented by 1. Thus,

```
001  Sum
  1  Add 1 (in difference counter)
---
010  = decimal 2.
```

The case in which a "0" carry is obtained in the differencing operation can be similarly illustrated:

	Decimal	**Binary**	**Operation**
Present cylinder address	5	101 101	None
Desired cylinder address	7	111 000	Invert
Difference	2	101	Sum
Direction: Forward			

Since the "0" carry at the end of the arithmetic indicates a forward direction, the sum must be inverted to get the proper result. The value 101, thus becomes 010 = decimal 2.

The RK06 implementation of this binary subtraction process is based on serial differencing in which the present-address bit and the corresponding desired-address bit are applied bit by bit to the subtractor. The difference count becomes the input to a D/A converter on the M7729 whose output voltage is proportional to the velocity to be commanded. As each bit in the subtraction process is determined, it is shifted into the cylinder difference register while the desired cylinder address is shifted into the cylinder address register, replacing the present cylinder address, which is shifted out during the differencing operation.

Referencing the simplified examples given above, when the final state of the carry flip-flop is true, the resultant difference must be incremented by one. This is accomplished by incrementing the difference counter after the difference has been loaded into it. When the final state of the carry flip-flop is false, the resultant difference must be inverted bit for bit. This operation is accomplished by exclusive OR gates located between the cylinder difference register and the cylinder difference counter.

Provided there are no drive faults, the forward flip-flop or reverse flip-flop is set according to the state of the carry flip-flop. The Enable Forward Servo or Enable Reverse Servo signal is asserted and the appropriate velocity command is generated by the D/A converter and profile function generator.

The positioner now accelerates to the desired velocity based on the cylinder difference. For each cylinder crossing, the cylinder difference counter decrements by one during the seek. The velocity command is coincidentally lowered (except for cylinder differences greater than 63) so that the positioner decelerates in an orderly manner to the desired location. Cylinder differences equal to or greater than 63 produce a constant velocity command of 114.3 cm/second (45 inches/second).

The positioner continues to follow the profile as commanded until the cylinder difference counter equals 0. At this point, the Enable Forward Servo or Enable Reverse Servo signal is negated, with the resultant switching off of the velocity command, and the positioner goes into position mode (Paragraph 4.3.2.5).

4.3.2.5 Detent (Position Mode) – The positioner is in detent or position mode when it is *locked* by the servomechanism at a cylinder centerline or at an offset position. (See Paragraph 4.3.2.6 for the offset description.) This is accomplished by selection of the Track Error signal by the servo analog multiplexer on the M7729 as a Position Command signal by the servo. At the cylinder centerline, the Track Error signal is zero. If the positioner were disturbed such that it moved away from the centerline, the track error voltage would command the positioner in the direction to oppose the disturbed motion, thereby resulting in a held or locked position. It should be pointed out that the velocity feedback is also selected in detent to add stability to the servo system. Velocity feedback at this time allows a faster correction to a disturbance to the positioner.

When the drive enters the detent mode from velocity mode, the carriage is a nominal 1/4 cylinder (1300 microinches) from the cylinder centerline. At this location, the servo analog multiplexer circuits cause the velocity command to be switched off, the Track Error signal to be switched on, and velocity feedback left on. The Track Error signal becomes the command to subsequently bring the positioner to the centerline. During this period, settling is generated on the M7705 module (a 3 ms pulse) to allow for the positioner to come to rest. The trailing edge of settling sets drive ready and drive status change (DSC) on the M7706, and also generates attention on the interface bus to indicate that the operation has finished.

4.3.2.6 Offset – Offset mode defines a means of repositioning the carriage small distances to either side of the cylinder centerline while in detent mode. Its purpose is to improve the chances of data recovery if data errors occur while positioned at the cylinder centerline. The offset mode is commanded from the system and the amount of the offset is determined from a code received by the drive. Refer to Table 3-5 for offset code details.

The drive may be offset by 25 microinch increments up to a maximum of ± 1200 microinches from the centerline.

There are three conditions for resetting the offset mode.

1. A return-to-centerline (RTC) command
2. A physical seek to another cylinder
3. A Write Gate signal received by the drive.

NOTE
This condition would produce fault and drive-off-track error. Writing of data is prohibited while offset.

When an offset is commanded to the drive, it does not go into velocity mode. Neither the forward flip-flop nor the reverse flip-flop becomes set. Instead, a voltage is generated by the profile function generator according to the offset code stored in the cylinder difference counter. This voltage is added to the Track Error signal in the servo analog multiplexing circuits on the M7729 module which results in a motion to a point where the sum of the two signals (Offset Value + Track Error) equals 0.

The offset command or the resetting of the offset mode triggers the 3 ms Settling signal on the M7705, resets drive ready, and, at the end of settling, generates attention to indicate to the system that the operation is completed.

4.4 READ/WRITE SUBSYSTEM

Figure 4-29 is the disk drive functional block diagram with the read/write subsystem blocks shaded. The major functional areas are discussed in the following subsections:

1. Write Circuits
2. Isolation Circuits
3. Read Circuits
4. Head Selection Circuits
5. Read/Write Fault Detection Circuits.

The discussion assumes reader familiarity with the basic principles of digital saturation magnetic recording. In writing, the area of the disk beneath the recording-head gap is completely driven to either of two possible magnetic states, completely overwriting any previously recorded data. As the disk moves beneath the head, the magnetic field created by the head gap is periodically reversed, and a magnetic flux transition is created on the recorded track at each reversal. The head, in reading, responds to each flux transition in the form of a bell-shaped pulse illustrated in curve A of Figure 4-30, the sign of the pulse being determined by the direction of that recorded flux reversal.

Data is encoded in terms of the intervals between flux reversals. In the RK06, the encoding notation is called modified frequency modulation (MFM), the rules for which are given in Paragraph 2.3.1.3.

The RK06 system is further defined as self-clocked, contiguous-pulse recording.

In contiguous-pulse recording, consecutive flux reversals are closely spaced so that, in reading, the complete pulse never appears, but merges with pulses from adjacent transitions to form readback signals (Figure 4-31).

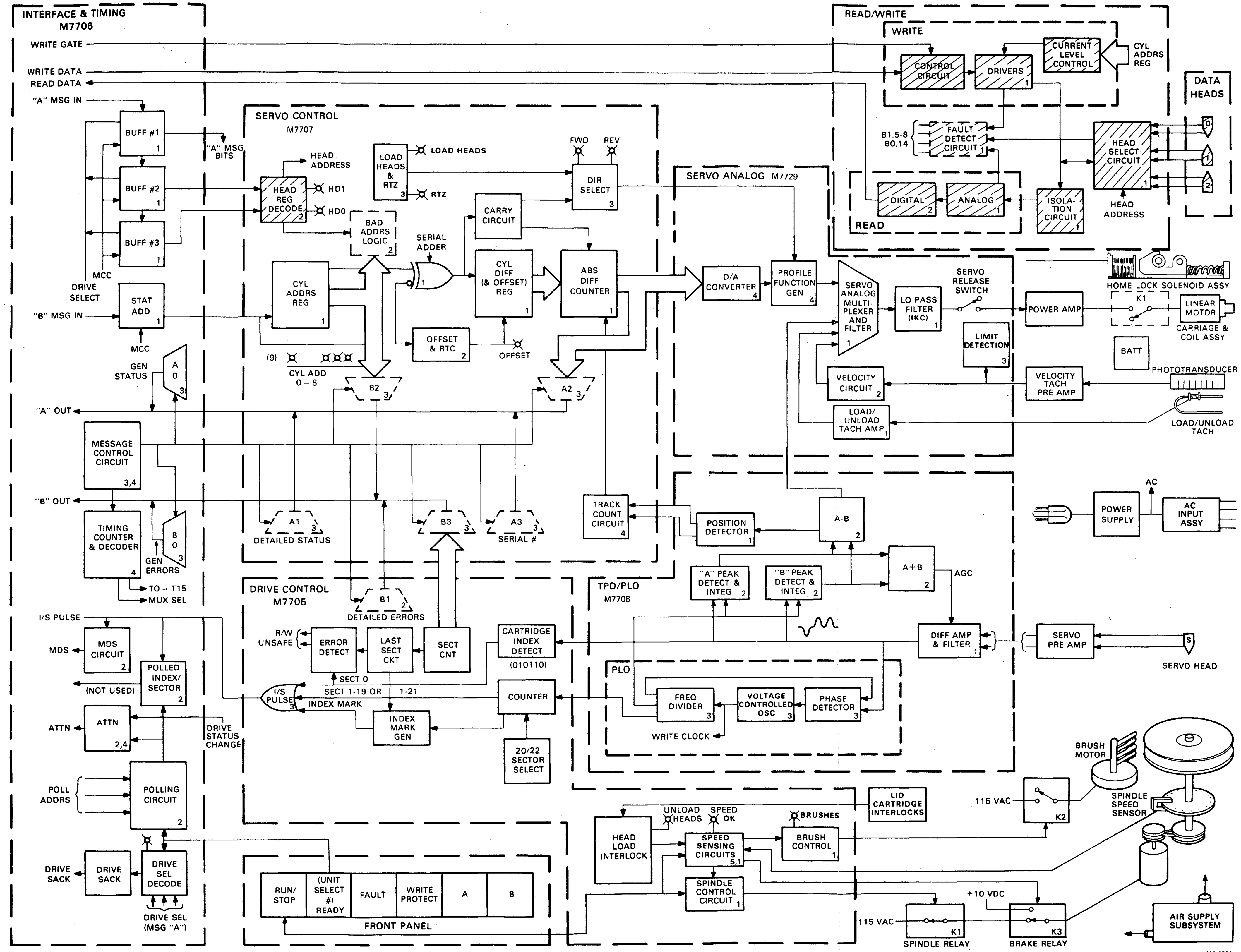


Figure 4-29 RK06 Disk Drive Functional Block Diagram Read/Write Circuits Shaded

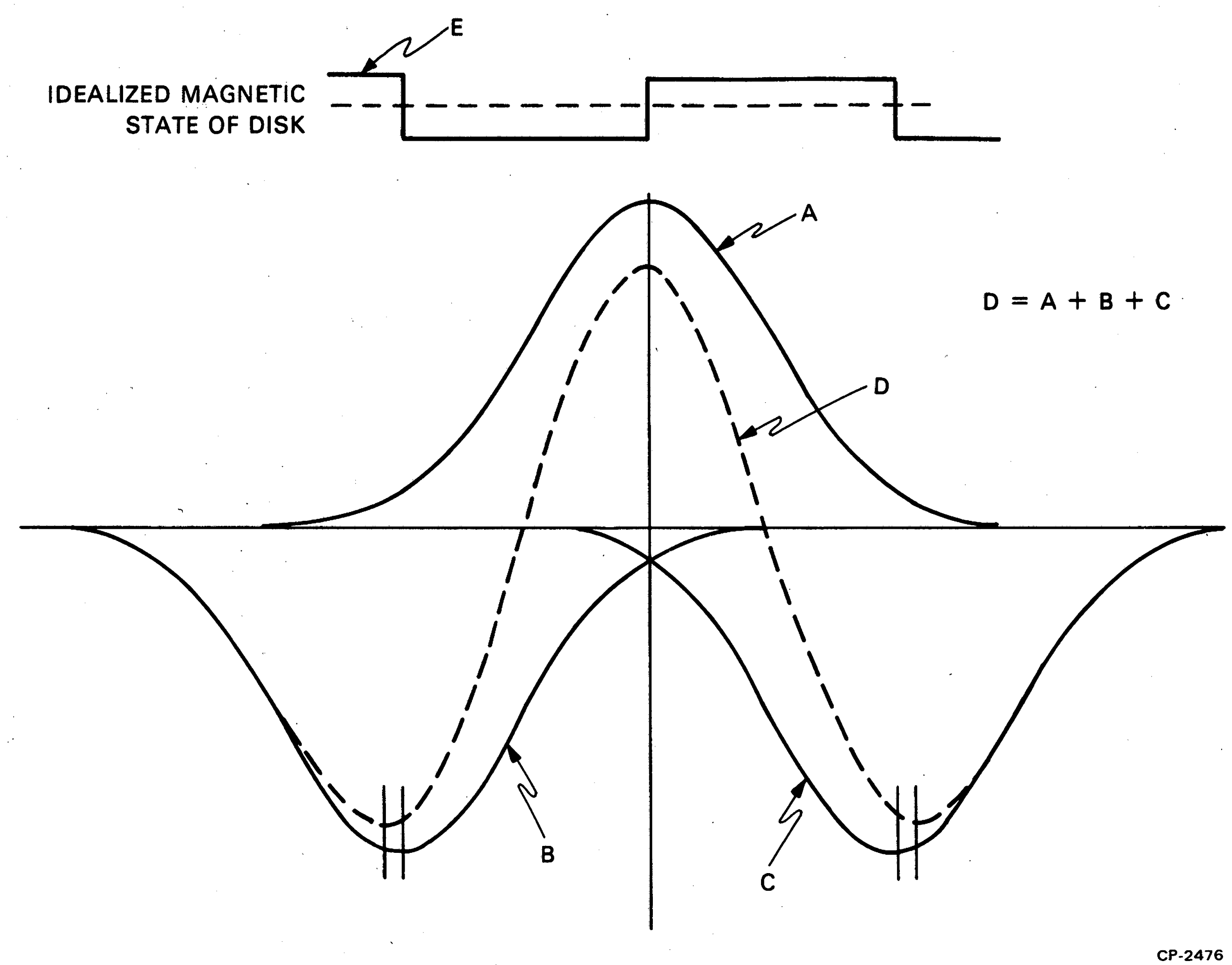


Figure 4-30 Superposition of Readback Signals

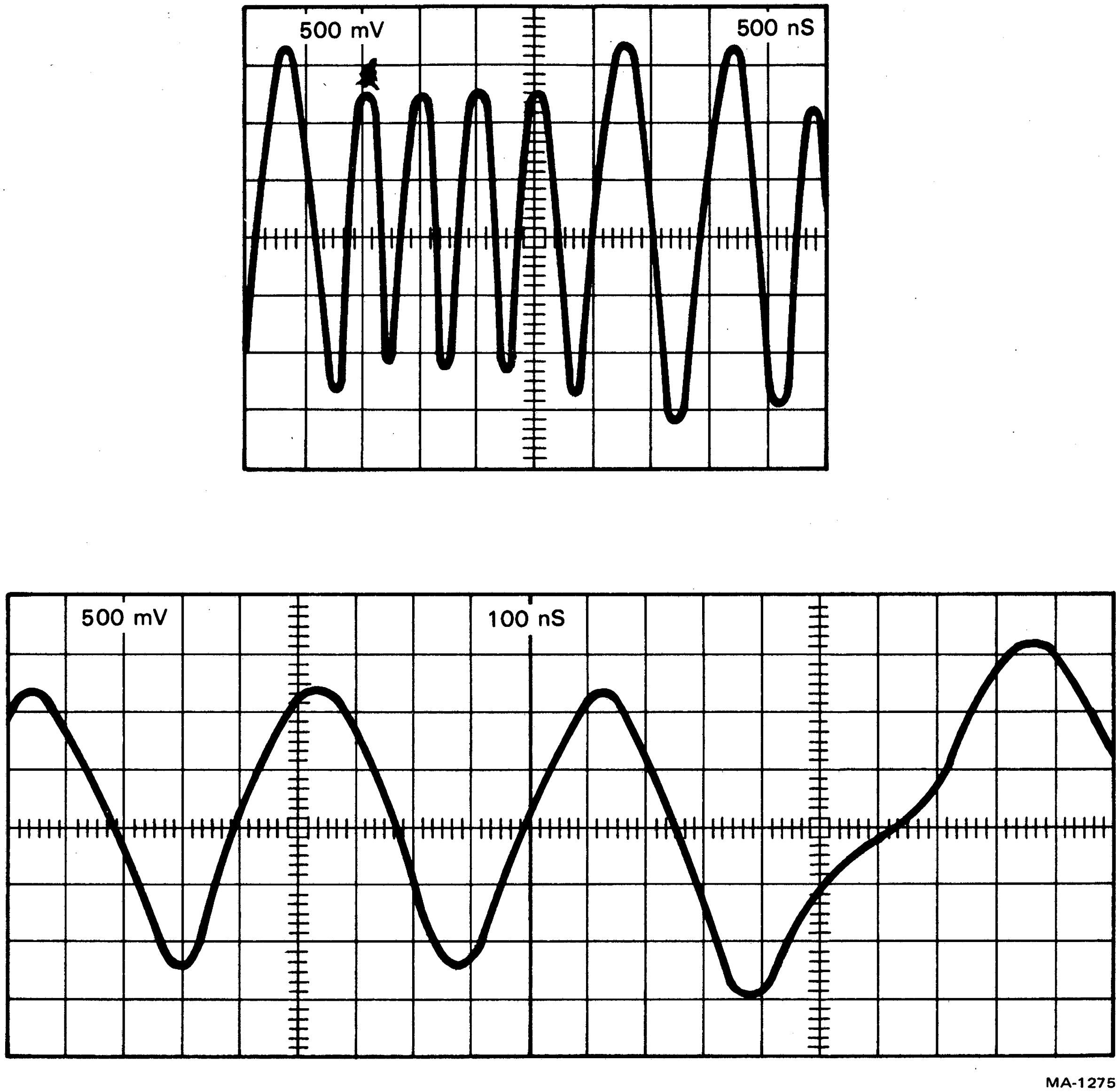


Figure 4-31 Typical RK06 Read Waveforms

It should be noted that the amplitude variation resulting from the superposition of pulses is of no concern, since the information content is carried in the time position of the voltage peaks. Figure 4-30 illustrates the superposition of readback pulses. Waveform E denotes the idealized magnetic state of a small segment of a recorded track. Waveforms A, B, and C represent the individual readback pulses that would result if each transition were completely isolated. Waveform D represents the actual readback resulting from the superposition of adjacent (contiguous) pulses. The peak displacement of pulses B and C (a phenomenon known as *peak shift*)is discussed in Paragraph 2.5 of this manual. Circuitry in the RK611 controller provides the necessary compensation for minimizing the effects of peak shift during controller/drive data interchange.

The real significance of the contiguous pulse recording is that the readback never exhibits a zero slope except at the peaks. Therefore, differentiation may be used to convert the peaks to zero-voltage crossings which are easy to process to a digital form.

Self-clocking means that the serially recorded information can only be decoded by self-reference. Information is recorded in the form of present or absent flux reversals at nominally equal intervals. Consecutive readback pulses alternate in polarity with no significance given to the shift.

Detection of the serially recorded information involves the measurement and classification of pulse intervals according to values established by the rules of the selected recording notation. The regular placement of pulses permits the application of phase-lock oscillator techniques for generating a synchronous clock that is used to establish the pulse intervals and the information content of the recorded data. This process is not a function of the disk drive, but is contained on the associated controller.

The Write Clock signal (see the Write Clock loop in Figure 4-32) is derived from the Tribit signal recorded on the dedicated servo surface. This clock signal is transmitted to the controller for the purpose of timing the write data sent to the drive. The Write Clock maintains bit density within precise limits despite any disk speed variation caused by line voltage fluctuations or other sources. Write Clock frequency is a nominal 8.602 MHz.

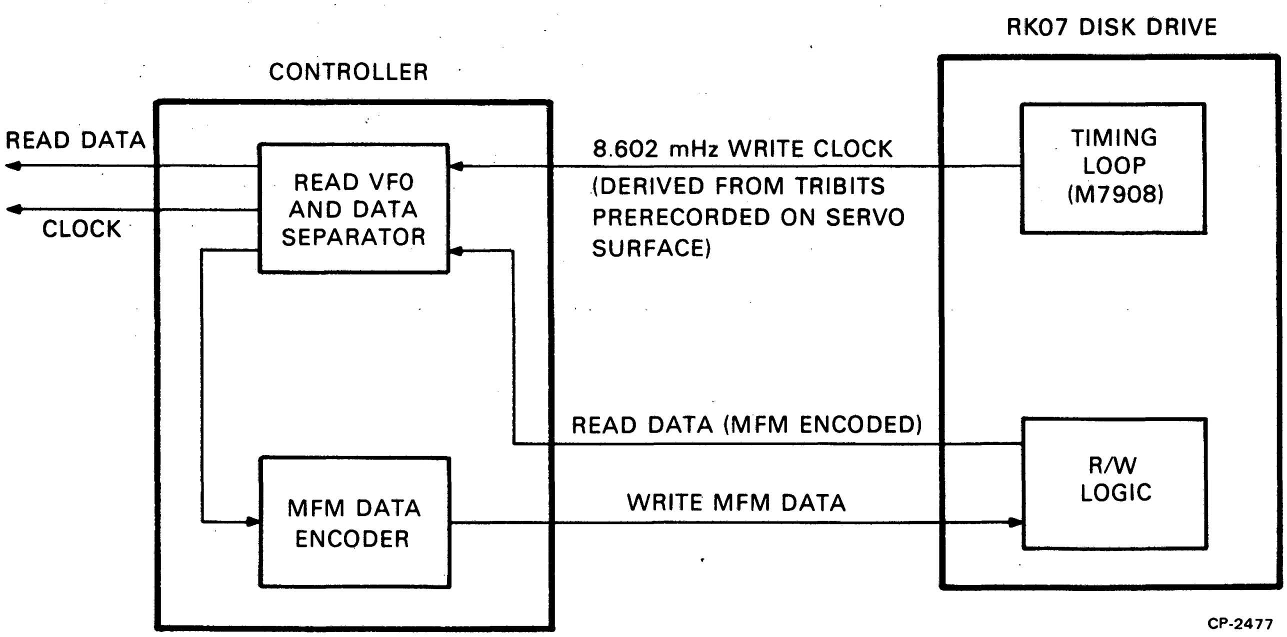


Figure 4-32 Drive/Controller Write Clock Loop

Data Heads
The recording heads contain a center-tapped winding. In writing, a current in one half of the winding creates a magnetic gap field of one polarity, while a similar current in the other half of the winding creates a field of opposite sign. In recording data, current is periodically switched between the two halves of the head winding.

In reading, a differential signal is created across the full winding.

Head Selection Circuit
A head is electronically selected by connecting its center tap to ground potential through the NPN output transistor of a 75451 integrated circuit element. This establishes the potential at the common connection of the head selection diodes, at less than +1 V. Unselected head center taps return to a potential of approximately +23 V, effectively open circuiting the associated selection diodes.

4.4.1 Write Circuits
The RK06 write circuits are designed so that:

1. Current switching in each read/write head is as rapid as possible within the limitations posed by circuit constants.

2. The current level in the heads is not measurably affected by variations in power supply voltages.

3. Write current level is selectable over a range of seven values so as to optimize recording efficiency over the full range of head radial positions.

4.4.1.1 Write Drivers – Figure 4-33 is a simplified schematic of the circuits used in controlling write current to the heads. A pair of transistors (Q2 and Q3) are connected so as to appear as current sources for the head. To ensure high-speed complementary switching of these transistors, a set/reset flip-flop (E2) is direct-coupled to their bases. E2 is powered from a floating supply created by emitter follower Q1 and a zener diode, D2.

The operation of write gating depends upon control of the base-current return path for Q2 and Q3. This return is provided by R2 via open-collector inverter E3. In the absence of a Write Gate and a negative return path, the bases of Q2 and Q3 return to +25 V, thus preventing collector current flow. Write Gate assertion turns on E3, thereby providing power for E2 and the bases of Q2 and Q3.

4.4.1.2 Write Control Circuits – It is necessary to switch write current with each incoming data pulse. To accomplish this function, the incoming pulse train is converted to odd and even pulse trains by a 7473 flip-flop and a pair of 74S00 gates (Figure 4-34). Negative pulses of approximately 55 ns duration at the gate outputs are therefore ac coupled to the inputs of the biasing network, which establishes a base for the pulses of approximately +2.5 V, referenced to the E2 $-V_{CC}$ level.

4.4.1.3 Current Level Control – There is an optimum value of write current for each radial (cylinder) position of the heads. A practicable compromise is to use 7 levels of current, as previously mentioned, with each level serving a band of 64 tracks. Although the closed-loop system is described as a current regulator, the actual regulation is that of voltage drop across the emitter return network of Q2 and Q3 (Figure 4-33). If an additional current path from the network is provided, the regulator still holds the same voltage, but the current in Q2 and Q3 is reduced by the amount of the diversion current. This principle is used in providing the desired step reductions of current as a function of head radial position. Figure 4-35 shows such a controlled current source. In this figure, E1 and Q1 are configured in a unity-gain arrangement to provide a constant 5.1 V plus one logic-low level at the emitter of Q1.

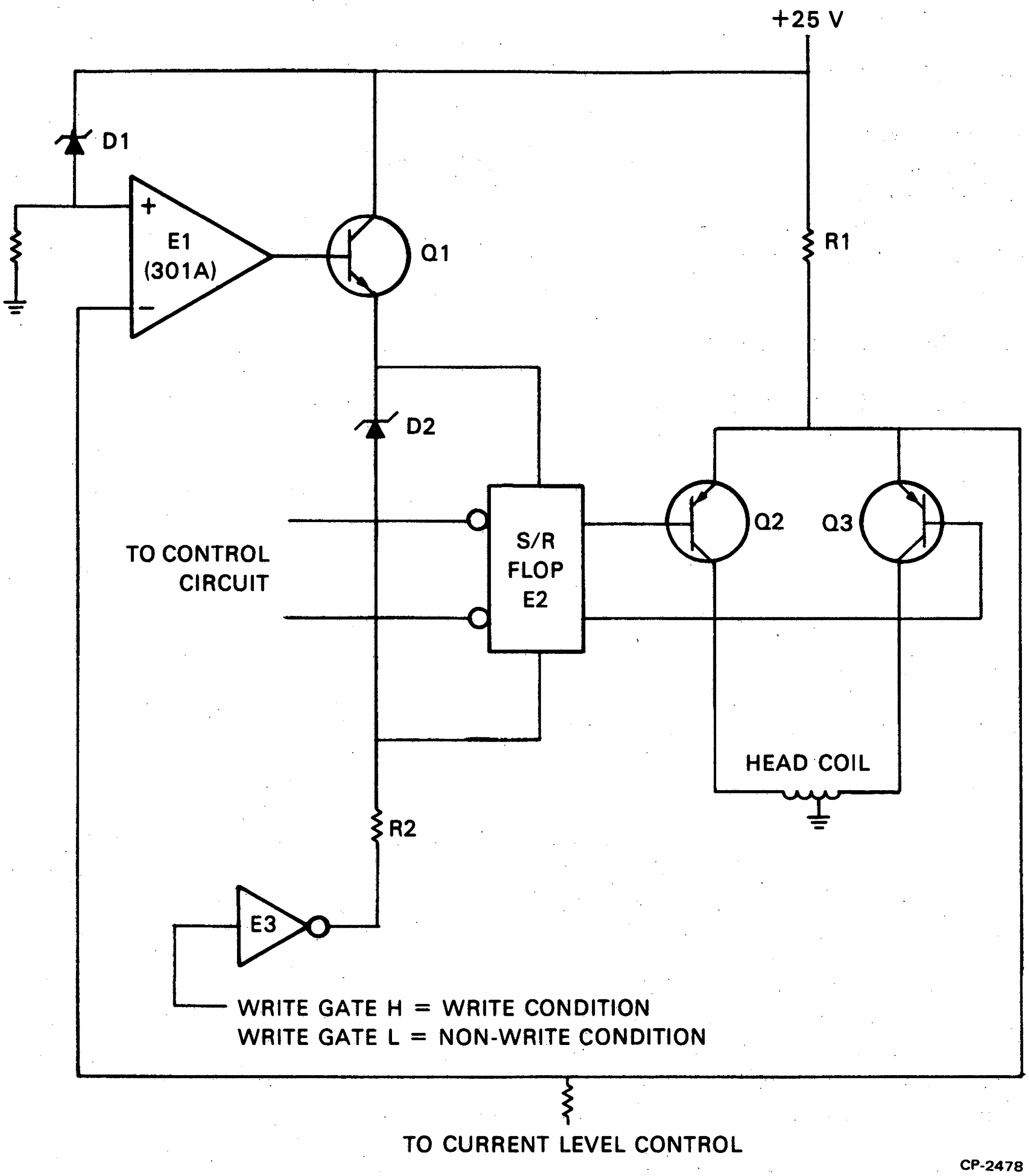


Figure 4-33 Simplified Write Drivers Schematic

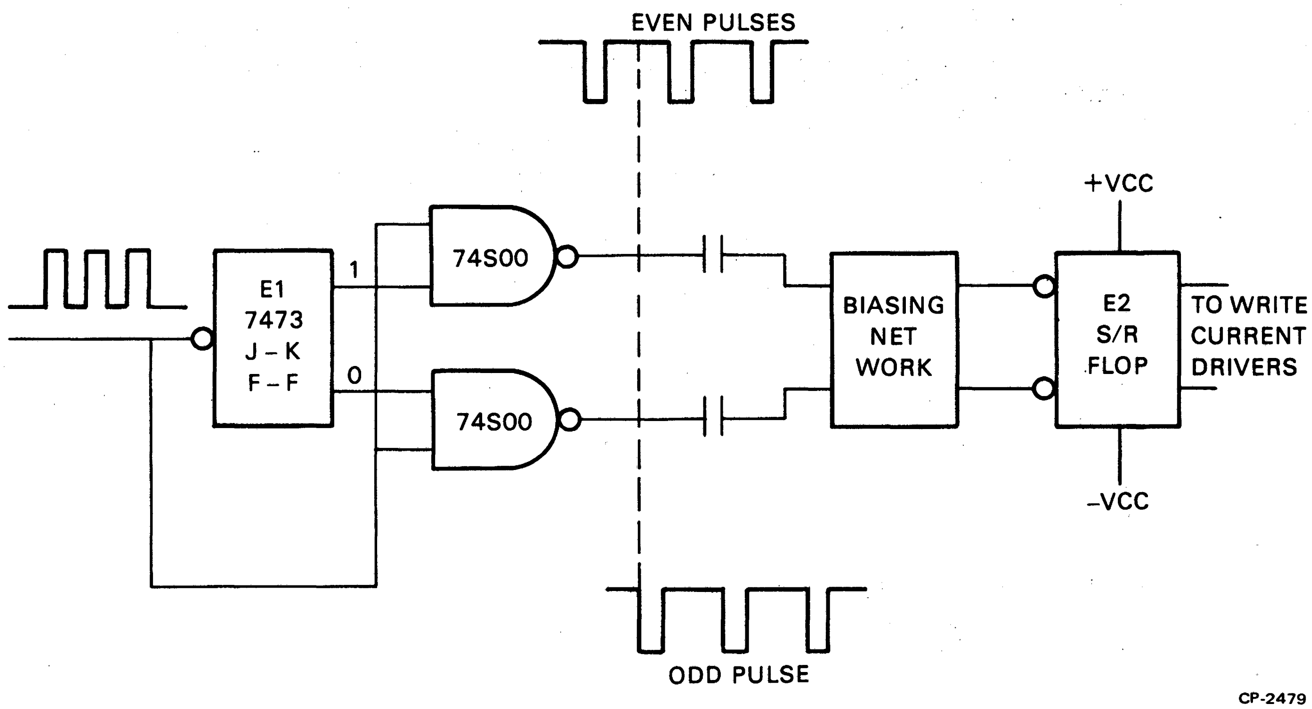


Figure 4-34 Simplified Write Control Circuit Schematic

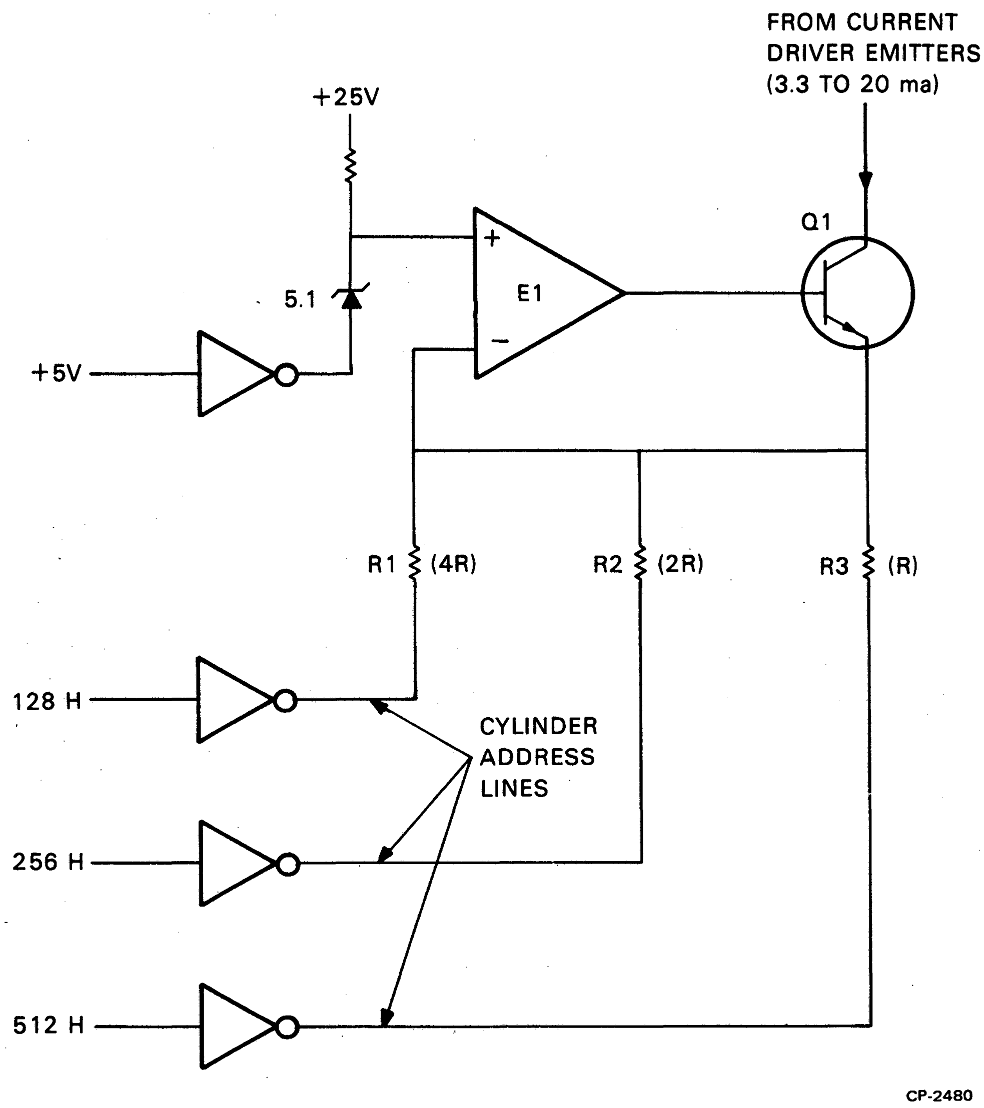


Figure 4-35 Current Level Control Schematic

Current in the collector of Q1 becomes a function of the emitter return resistance. The return resistors are selected in binary fashion, such that R1 selects a current of 3.3 mA, R2 provides 6.7 mA, and R3 provides 13.6 mA. The cylinder address bits (from the cylinder address register on the M7707 module) supply a selection code such that the maximum outer-band current of 92 mA is reduced in increments of 3.3 mA at 64-track intervals. Thus, inner-band current is 70 mA.

4.4.2 Isolation Network

A resistor-diode network is connected between the read/write, head selection bus, and the read preamplifier. This network serves two purposes.

1. It isolates and protects the preamplifier from the large voltages generated during writing.
2. It prevents the preamplifier input from loading the head during writing.

4.4.3 Read Circuits

The read circuits (Figure 4-36) comprise an analog (linear) section and a digital section.

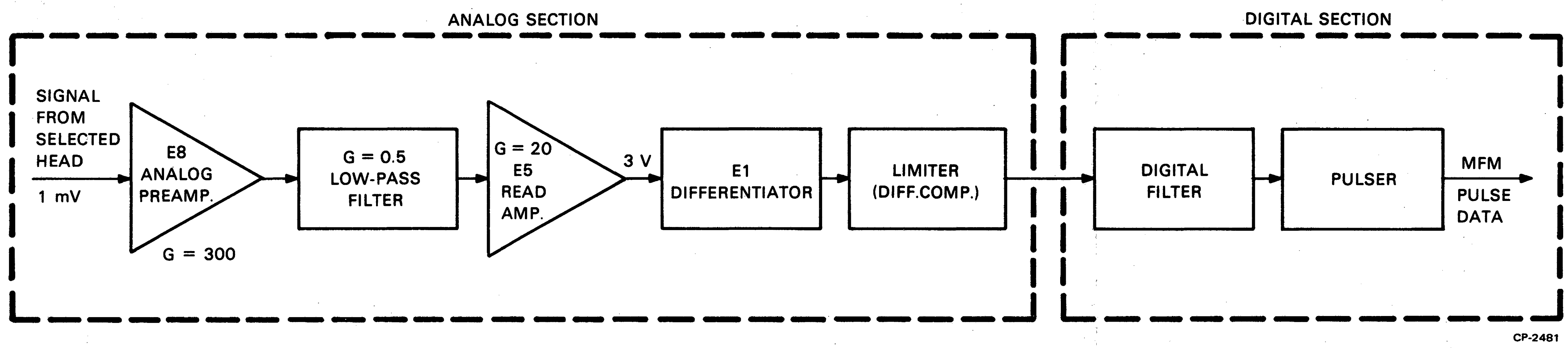


Figure 4-36 Block Diagram of Read Signal Circuits

4.4.3.1 Analog Section

Preamplifier, Filter, and Amplifier
The analog portion of the read/write circuitry comprises:

1. A preamplifier having a gain of 300 for the low-level Input signal from the selected head

2. A low-pass filter with a 6 MHz, 3 dB cutoff and an insertion loss of 0.5 (the filter is used to remove high frequency noise)

3. A second amplifier with a gain of 20.

Differentiator-Limiter (Peak Detector)
The delay line differentiator operates on the principle illustrated in Figure 4-37. The read pulse response to a single flux transition is shown delayed with respect to itself (A, B). By subtracting (A–B), the waveform of C is developed, and the peak of A is converted to a zero-voltage crossing. The same operation performed on the contiguous Pulse Read signals similarly converts each peak to a zero-voltage crossing. Figure 4-38 exemplifies this process.

In the RK06, a balanced network (Figure 4-39) is used with the delay line comprising a parallel LC circuit. The required subtraction occurs as a result of a summation of the currents at the differential comparator input at nodes A and B.

The Differential signal is converted to square waveform by comparator E2. Note that a pair of comparator circuits is actually used in order to maintain the desirable noise rejection and balanced delay characteristics of the differential configuration.

4.4.3.2 Digital Section

Digital Filter
The contiguous pulse-recording system of the RK06 is inherently insensitive to various types of noise. However, for certain bit sequences, particularly those with higher resolution heads, the Differentiated signal approaches the zero reference and becomes susceptible to false crossings from noise.

For the most common case of disturbance, where the false zero crossing is of short duration, the RK06 provides means for rejecting the pulse developed from such a crossing.

The basic circuit around which the system is developed is called a one-way integrator and is illustrated in Figure 4-40. The input, A, is such as might be derived from a Disk Read signal. The negative edges are significant. Without capacitor C1, the waveform at B would be simply an inversion of A. The addition of capacitor C1 prevents a rapid rise of voltage since C1 must charge through R1. A sufficiently high supply voltage to R1 is provided to assume linear charging. A differential comparator with reference +V responds when the sawtooth input wave exceeds the threshold; the result is shown in waveform C.

The following is true.

1. The new negative edge generated is delayed from the original transition.

2. Such an edge is developed only if the Input signal is of sufficient duration to permit the sawtooth to cross the comparator threshold. This is illustrated where the circled portion of the Input signal causes no comparator input.

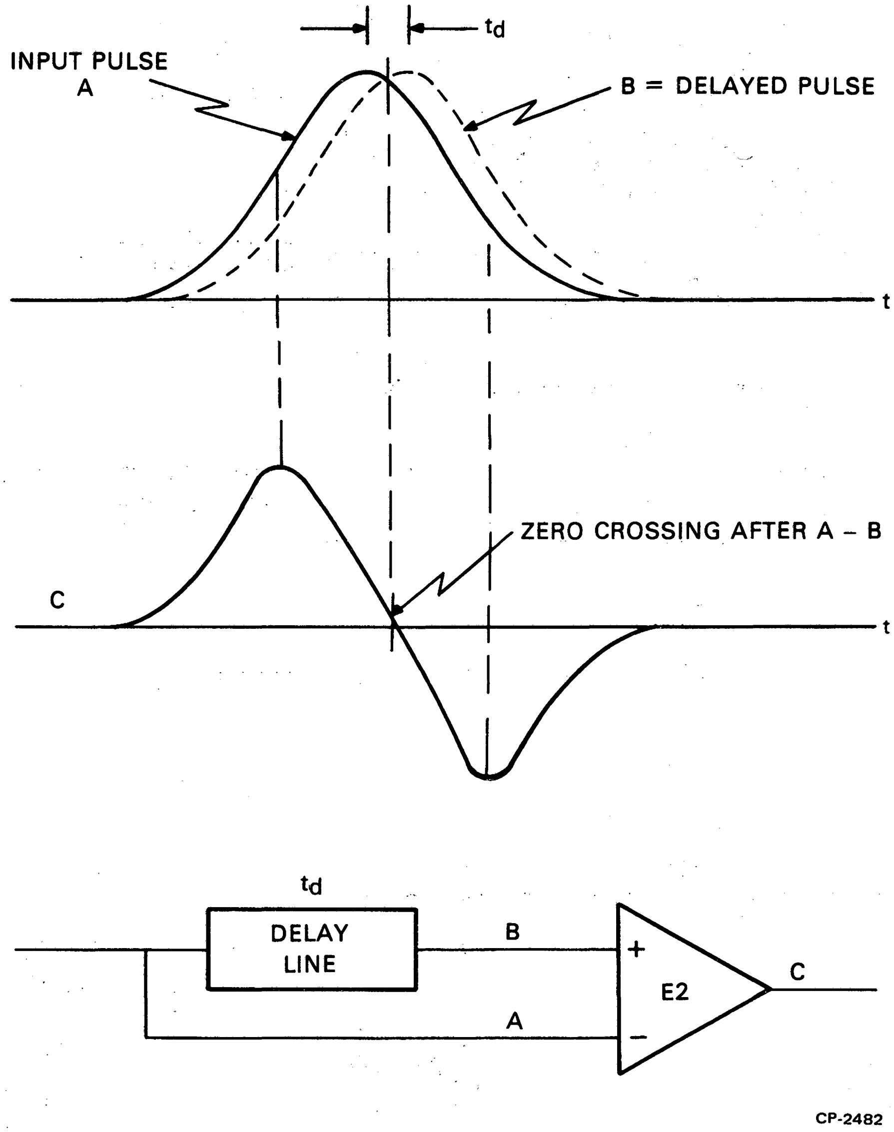


Figure 4-37 Delay Line Differentiation (Simplified)

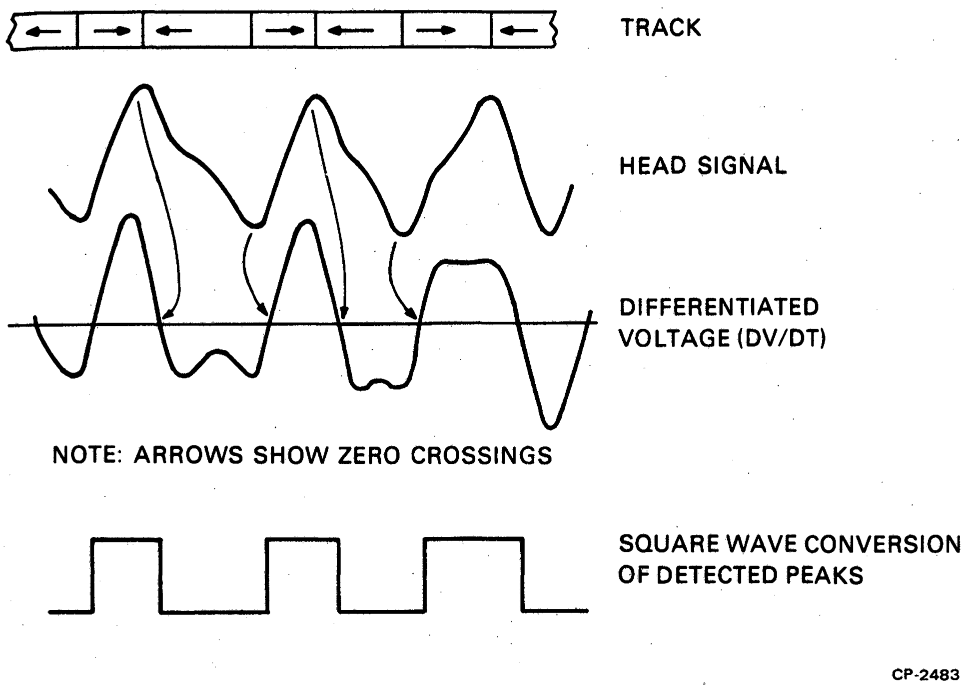


Figure 4-38 Read Signal Differentiation

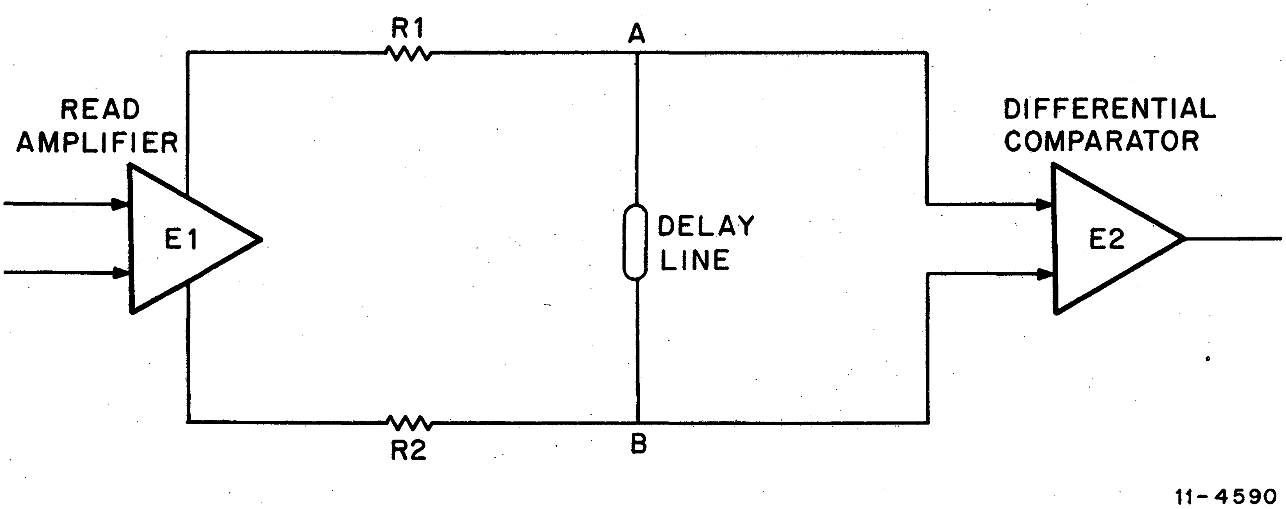


Figure 4-39 Read Signal Differentiation Circuit

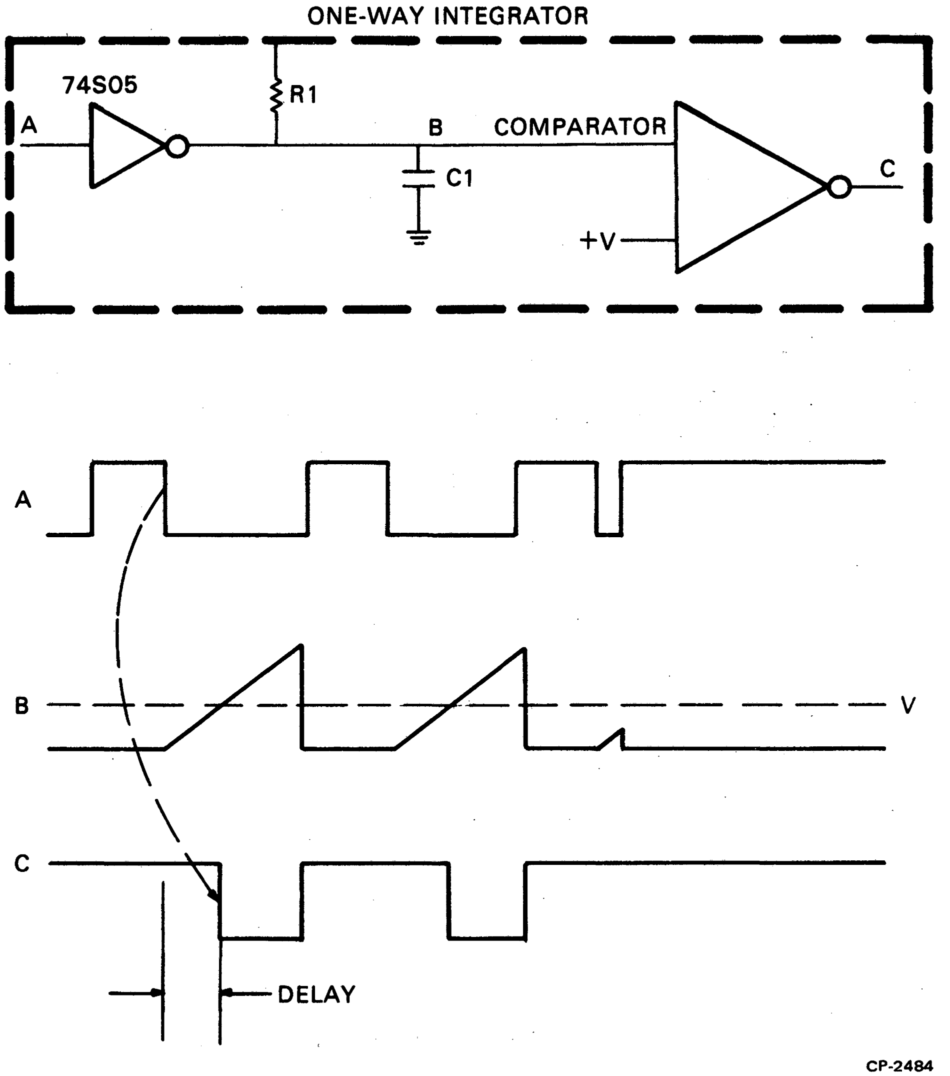


Figure 4-40 One-Way Integrator of Digital Filter

It is obvious that the input waveform has been altered in duration. To reconstruct the original waveform (less false zero crossing pulses), a pair of comparators and integrators are used. The pulses developed from the integrators are used to set and reset a flip-flop. The signal processing is further illustrated in Figure 4-41, a block diagram, with pertinent waveforms denoted in Figure 4-42. The waveforms D and H in Figure 4-42 are not directly observable, being internal to the integrated circuit devices. The flip-flop, which reconstitutes the original signal (less false crossings), is created by cross-coupling of the digital portions of the comparator pair.

Pulser

A final waveshaping operation is required to process the Data signal to a form suitable for transmission via a bus to the controller for detection (data separation). The objective is to convert each voltage transition of the Limited Differentiated signal to a discrete pulse.

Figure 4-43 illustrates the method. A comparator and gate are connected as shown. Waveforms illustrate operation of the circuit.

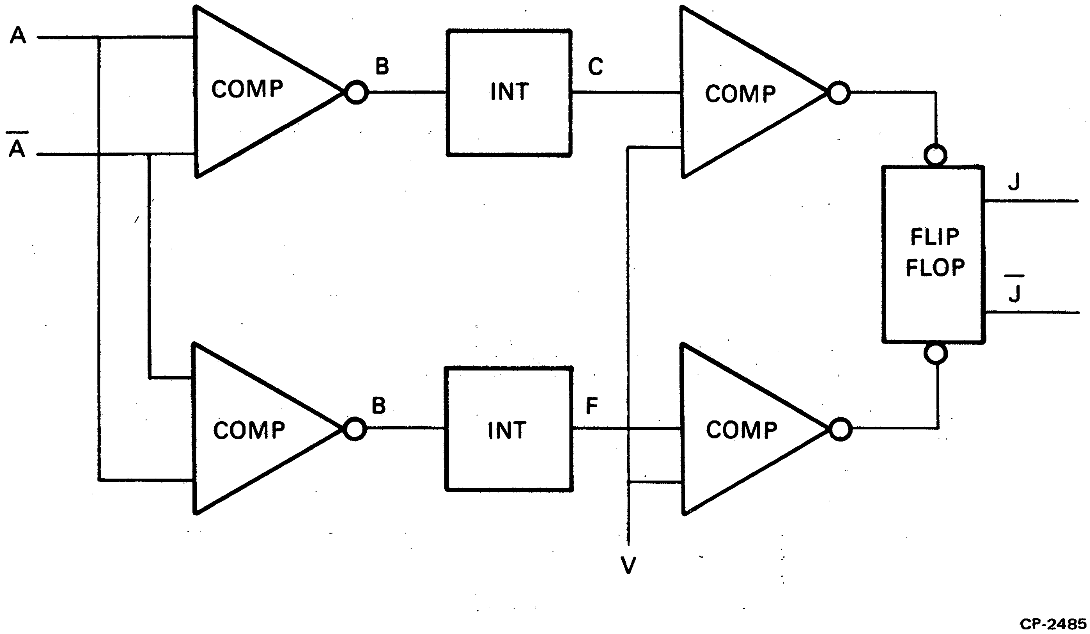


Figure 4-41 Digital Filter Block Diagram

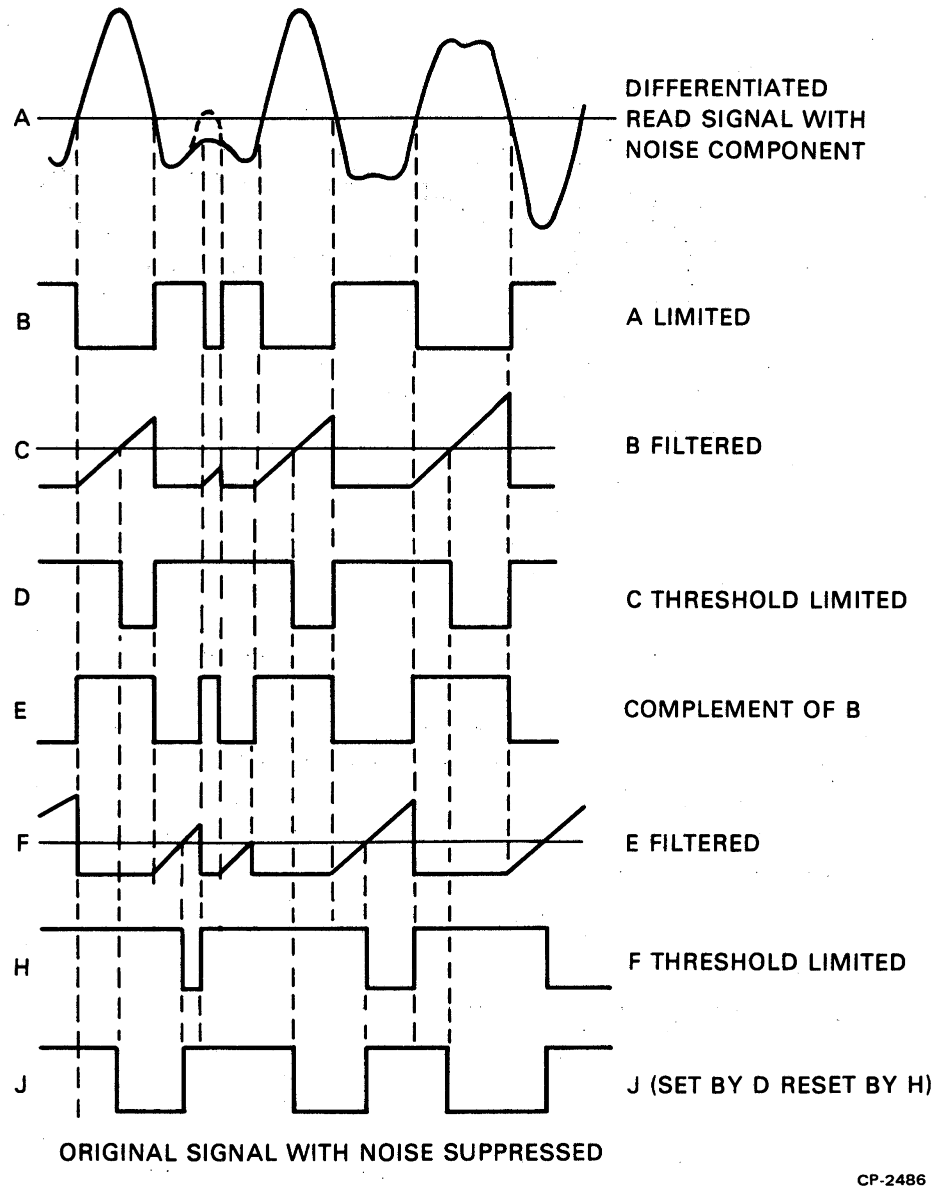


Figure 4-42 Write Current and No Write Gate Waveforms

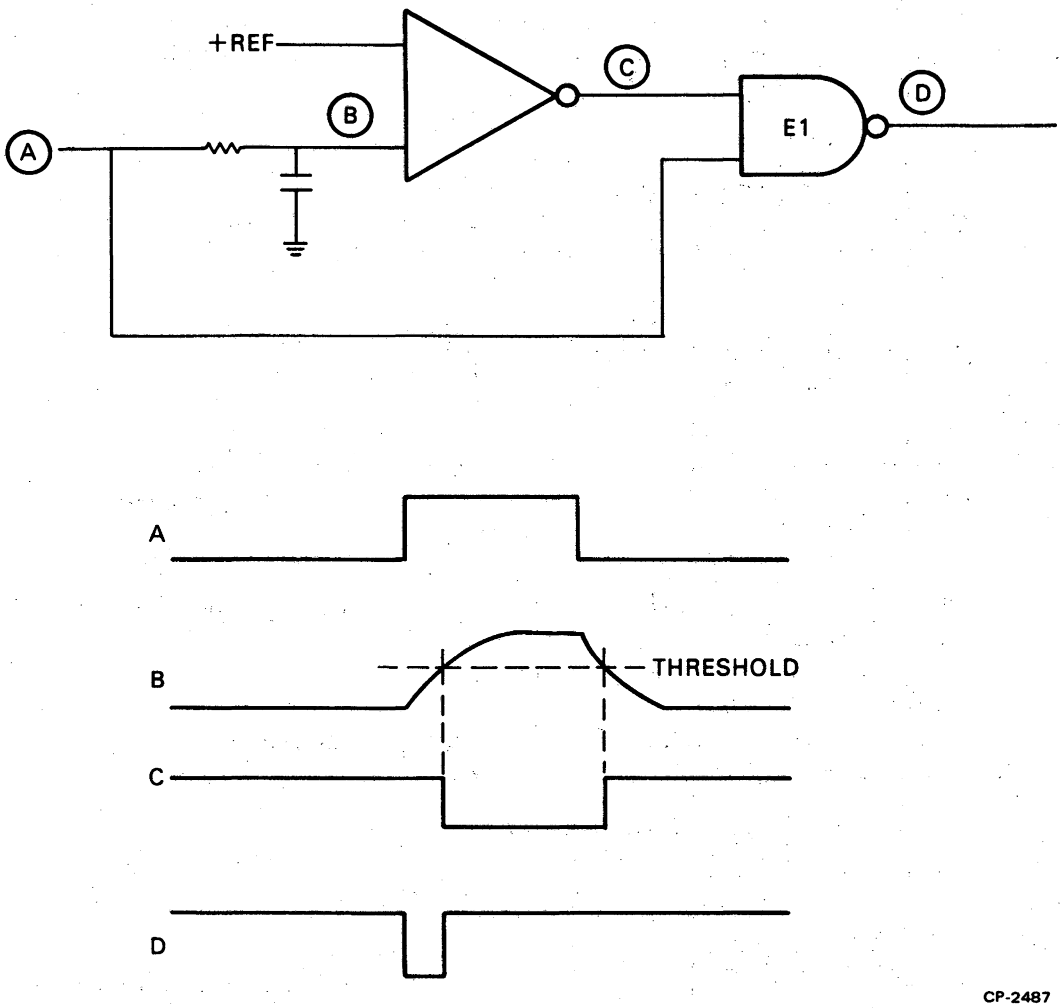


Figure 4-43 Pulse Former (Pulser) for Read Output

It should be noted that the exact duration of the output pulse is not important. Only the timing of the leading edge is significant.

The actual circuit is a differential configuration of the simplified version. Odd and even pulse trains are generated. These are combined into a single signal on the M7706 module for transmission to the controller.

4.4.4 Fault Detection Circuits

The read/write fault protection is provided to safeguard disk information against accidental overwrite or erasure due to a read/write circuit failure. Four discrete error conditions are tested for and the results reported to the drive error registers.

4.4.4.1 Write Current and No Write Gate – This signal indicates that write current exits even though not requested. This condition is caused by a write circuit failure and may result in a dc erasure.

In the schematic of Figure 4-44, transistor Q1 is normally non-conducting during a non-write condition. Any current flow from the write drivers will cause base current in this transistor. Conduction of its collector presents a logic low input to the following gate, E1, which is enabled when not writing, permitting a fault condition to be indicated at the output.

The filter (R1 and C1) prevents any false indications during the turn-off of a write operation.

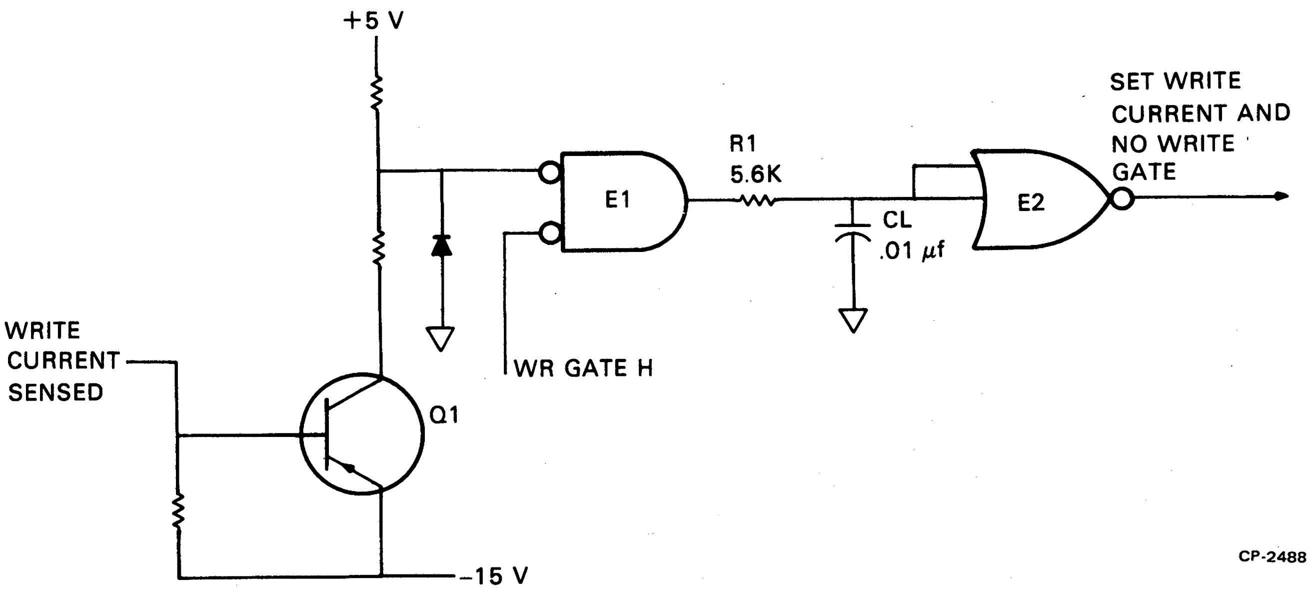


Figure 4-44 Write Current and No Write Gate Schematic

4.4.4.2 Multiple Head Selection – As shown in Figure 4-45, if a single head is selected, the base of Q1 connects to a voltage divider comprising a 287 Ω resistor (R1) and one of three 5.11 kΩ resistors (R2, R3, and R4) spanning +25 V. The emitter of Q1 connects to an identical divider (R1 and R6) and the same voltage. Q1 does not conduct.

If additional heads are selected, additional 5.11 kΩ resistors provide base current to Q1 and transistor conduction activates the following E1 inverter to generate a fault-indication output.

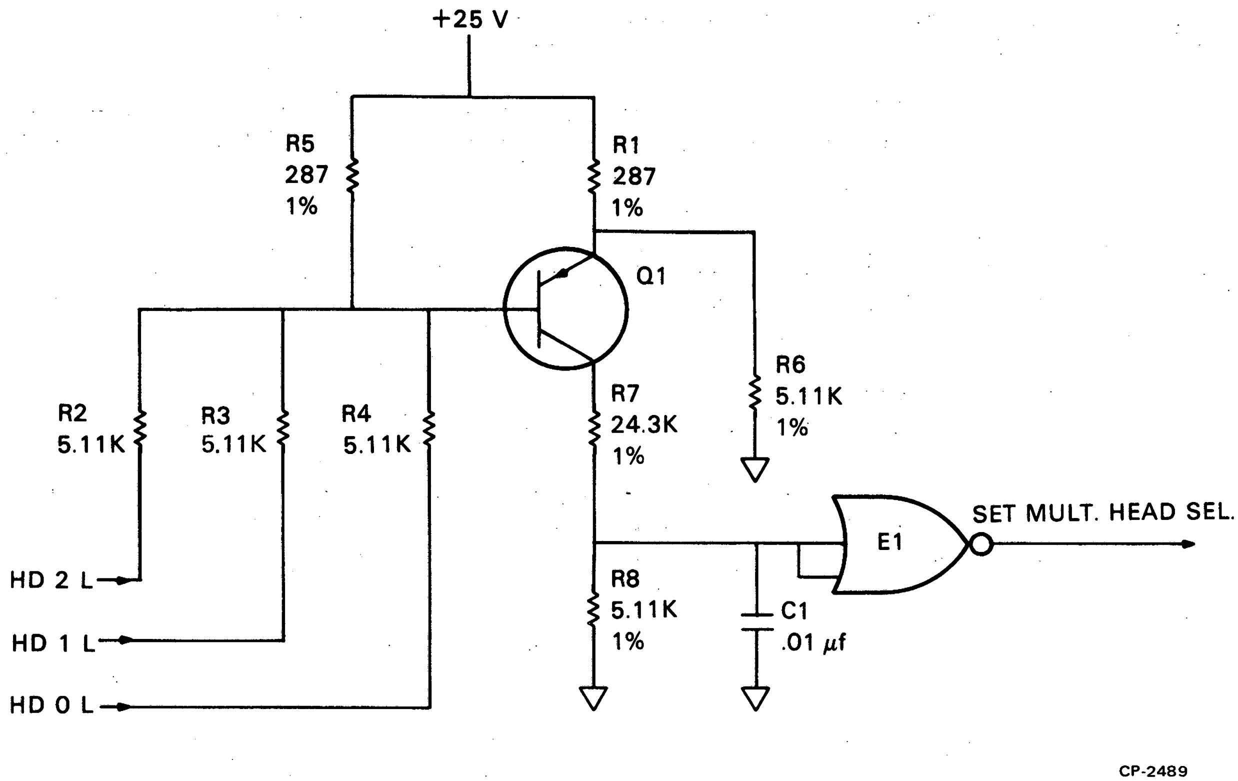


Figure 4-45 Multiple Head Selection Schematic

4.4.4.3 Write Gate and No Transitions – Figure 4-46 is a schematic for this fault circuit. In the absence of WR GATE, the first gate is not enabled, so that no fault indication is detected even though E3 is held in the reset state. When WR GATE is asserted, the reset is removed from E3, and the gate, E1, is activated. If no WT DATA pulse appears to set E3 within the delay time of filter, C1 and R1, a fault is noted.

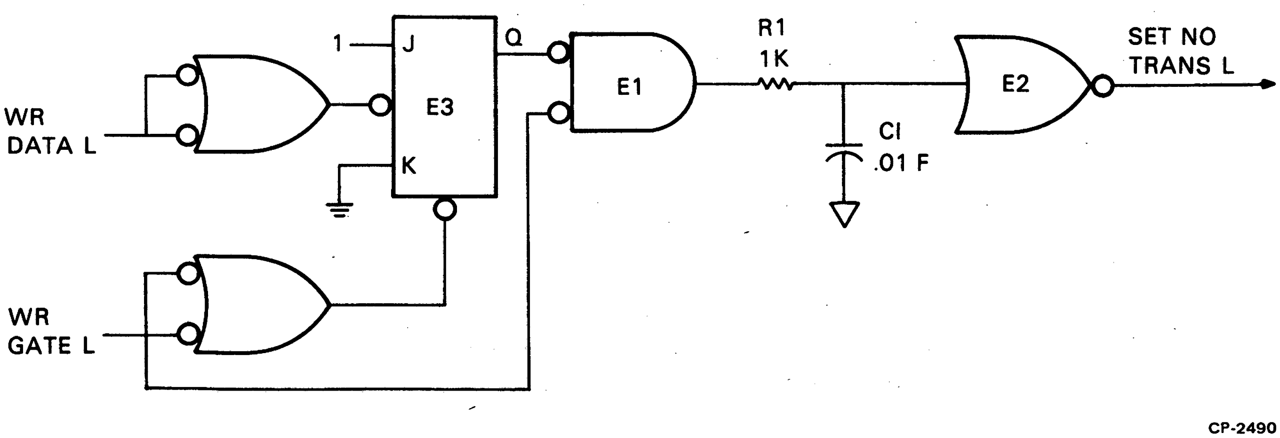


Figure 4-46 Write Gate and No Transitions Schematic

4.4.4.4 Head Fault – Figure 4-47 is a schematic of the head-fault circuit. Under normal conditions the input to E1 is normally dc balanced to within a few millivolts, and the E1 outputs reside at about +3.5 V. Any input imbalance, such as from an open head or faulty component, causes E1 to saturate with one output moving close to the ground potential. This is detected in the logic structure of E2 to create the fault indication at the output.

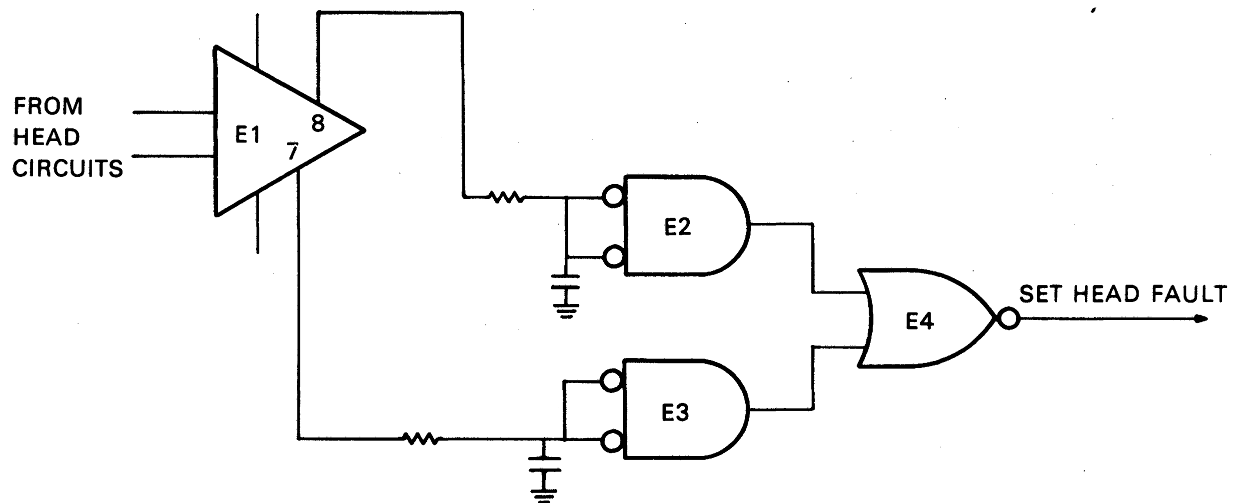


Figure 4-47 Head Fault Schematic

4.5 AIR SUPPLY AND DISTRIBUTION SUBSYSTEM

Figure 4-48 is the disk drive functional block diagram with the air supply and distribution subsystem shaded.

4.5.1 Filtration

There are two air-filtering stages within the drive: a prefilter and an absolute filter (Figure 4-49).

4.5.1.1 Prefilter – This filter is a foam type that prevents the larger airborne particles from entering the drive, thereby lengthening the replacement intervals of the absolute filter and preventing dust buildup within the drive.

4.5.1.2 Absolute Filter – This filter is a self-contained replaceable type that removes 99.999 percent of all airborne particulants of 0.3 μm and larger from the air supplied to the cartridge. This clean air prevents disk deterioration due to foreign particles. It also provides cooling air and minimizes temperature variations of the cartridge.

4.5.2 Blower

The dual-impeller blower provides forced air for cooling of the electronics within the drive, and the purge air necessary to maintain a clean, temperature-stable environment within the cartridge. The blower is designed to provide 330.4 m^3/min (70 ft^3/min) at 1.9 cm (3/4 inch) of water to the subchassis ducting (for electronics cooling) and 118 m^3/min (25 ft^3/min) at 5.08 cm (2 inches) of water through the absolute filter to the cartridge (purge air).

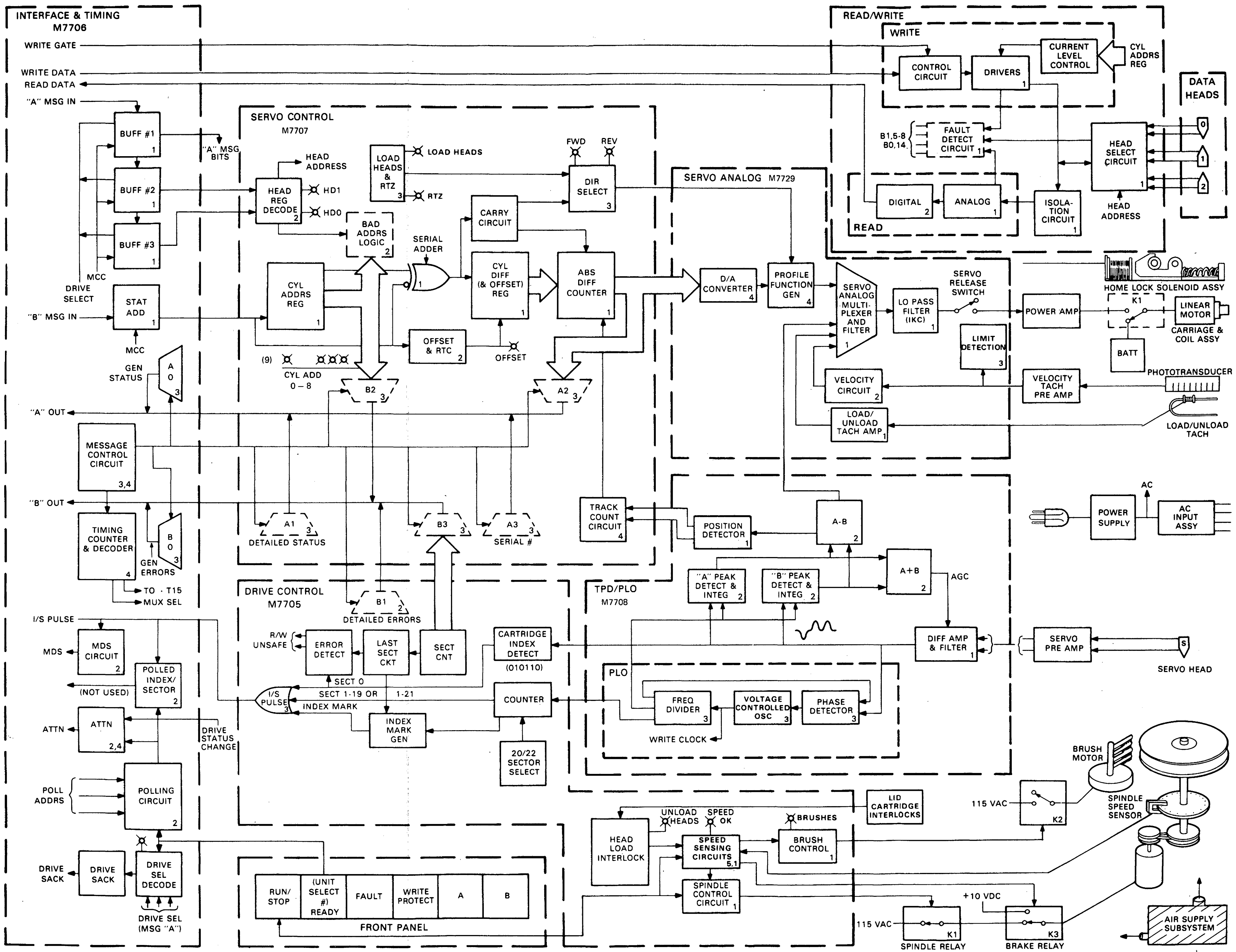


Figure 4-48 RK06 Disk Drive
Functional Block Diagram
with Air Supply and Distribution Subsystem Shaded

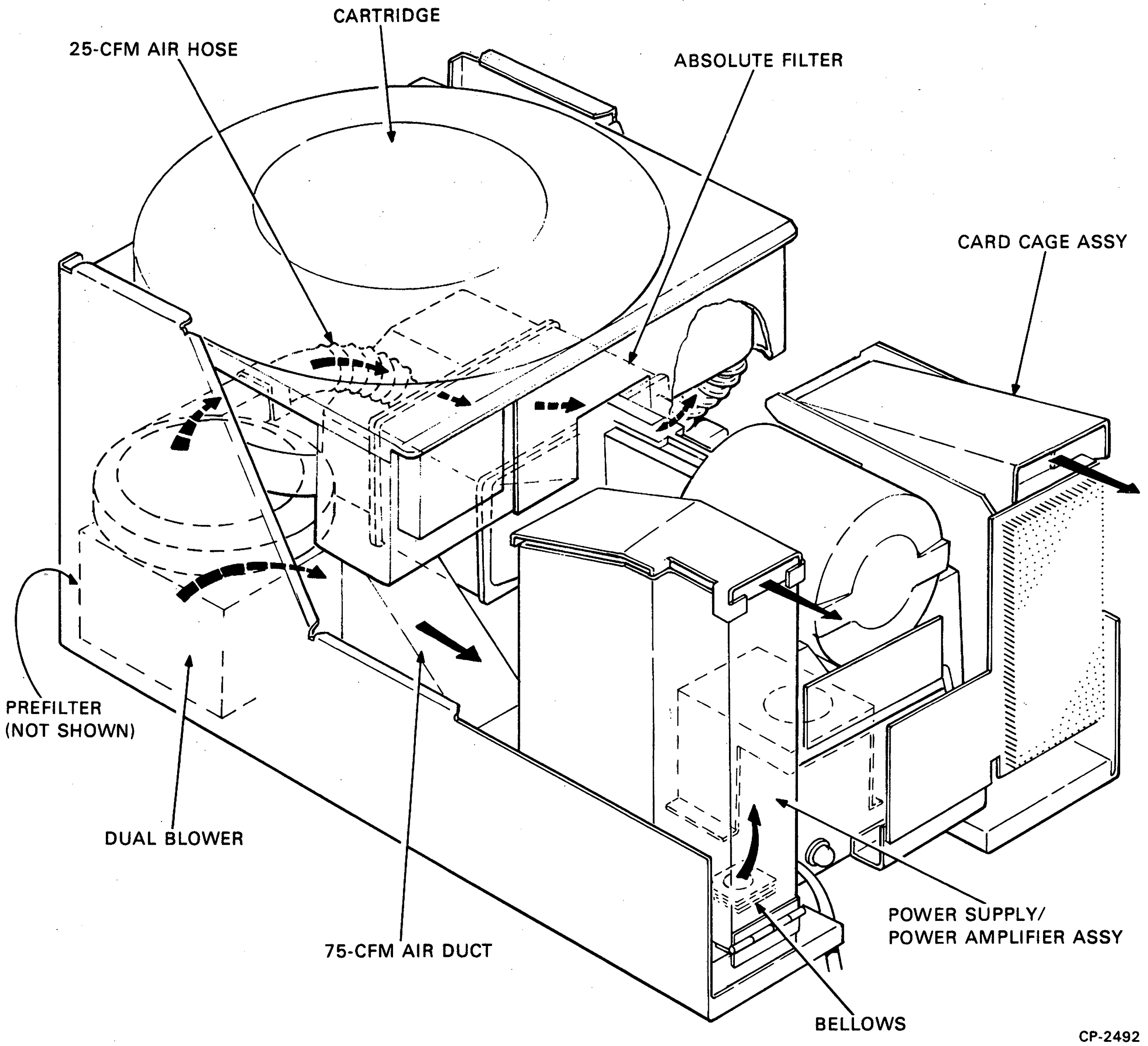


Figure 4-49 Air Supply and Distribution Subsystem

4.5.3 Ducting

The forced air is routed through hoses, for the cartridge purge air, and the chassis plenum, for the electronics and power supply/power amplifier cooling air. Due to cooling requirements, the bellows connected to the power supply chassis provides cooling air to the heat sink and components of the power supply/power amplifier module when the module is in the normal (operating) position and when it is pivoted downward for maintenance. Air deflectors at the top of the electronics chassis and power supply chassis are positioned to divert exhaust air through ports at the rear of the drive.

4.5.4 Operational Description

The blower operates whenever ac power is on within the RK06. The blower intakes ambient air through the front of the drive (Figure 4-49) through the prefilter and exhausts into the absolute filter and the subchassis plenum. The air passing through the absolute filter continues through the shroud intake and into the cartridge through a port in the side of the bottom cover. This air exhausts through the access hole for heads and the cartridge-cleaning brushes into the chassis. The positive air flow through the cartridge prevents contaminants from entering the cartridge via the head and brushes access holes. The cooling air, passing through the subchassis plenum, exhausts into the electronics and power supply chassis. After picking up the heat generated from the components, the air is deflected rearward and exits the drive through rectangular ports in the back cover.

4.6 POWER SUPPLY SUBASSEMBLY

The power supply subassembly is shown by the shaded blocks of Figure 4-50, the RK06 functional block diagram. The power supply subassembly contains the functional groupings discussed in the following paragraphs of this section. The relationships of these groups can be seen in the functional block diagram of Figure 4-50.

4.6.1 AC Input Assembly

This assembly receives the ac input power through a line cord. The presence of this power is indicated by a red lamp (lighted) at the rear of the drive. The circuit breaker of this assembly controls the distribution of the input power and, when on, applies power to the constant voltage transformer (CVT), blower motor, power supply capacitor module, and spindle brake power supply. A line filter within the AC input assembly prevents unwanted noise spikes on the input power from adversely affecting the operation of the disk drive.

4.6.2 Constant Voltage Transformer (CVT)

The CVT supplies 13 Vac and 37 Vac to the power supply modules. A matched capacitor connected to the CVT maintains these output voltages over the full operating voltage range of the RK06, in spite of the fluctuations of the input power.

4.6.3 Rectifiers, 10 Vdc and 25 Vdc

These full-wave rectifiers produce plus and minus voltages for the regulators on the power supply module, ± 10 Vdc for the ± 5 V regulators and ± 25 Vdc for the ± 15 V regulators. The $+25$ Vdc is also used to energize relays, as the current source for the write current, and for the linear motor.

4.6.4 Relays

The relays located on the capacitor module route power to the motors within the RK06 (except the blower motor). Relay K1, when energized, energizes the spindle motor whenever relay K3 is deenergized. When K1 is deenergized, the spindle motor is deenergized. Relay K2 applies power to the brush motor when energized, and removes it when deenergized. The third relay, K3, routes ac input power to the spindle motor when deenergized and the brake power supply when energized. The controls for these relays are discussed in Paragraph 4.2 (Drive Control Subsystem).

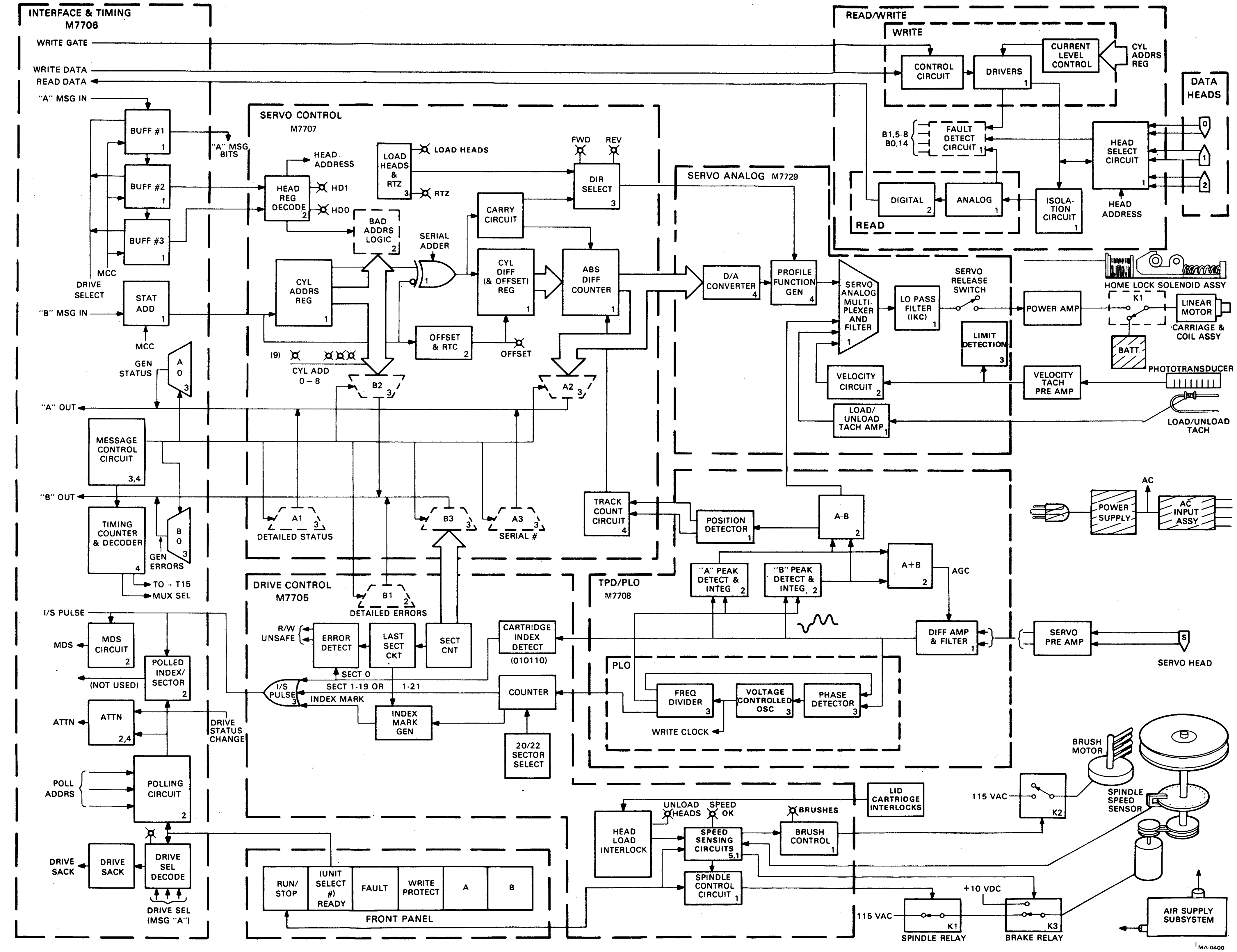


Figure 4-50 RK06 Disk Drive Functional Block Diagram with Power Supply Subsystem Shaded

4.6.5 Regulators, ±5 Vdc and ±15 Vdc

The linear regulators supplying the ±5 Vdc and the ±15 Vdc are similar in design. The block diagram of Figure 4-51 represents these regulators. The feedback circuit maintains the output voltage at the prescribed level over various load conditions. The current limiting is employed when a short circuit condition arises in the circuitry supplied by the regulator. When this condition happens, the current limiting transistor is turned on, dropping the output voltage to about 0.2 Vdc, and remains turned on as long as the condition is present. This current limiting feature is present to protect the circuitry supplied. The +15 Vdc regulator also produces two zener-diode-regulated +5.1 Vdc reference voltages for use in the feedback circuits and power low circuits of the power supply. The +5 Vdc regulator also has overvoltage protection provided. When an overvoltage condition is detected, approximately 5.7 Vdc on the output, an XA55 transistor is turned on, which in turn fires the SCR "crowbar," bringing the output voltage to the current limited value of about +0.2 Vdc. This SCR will remain conducting until the overvoltage condition is no longer present and power is removed and reapplied.

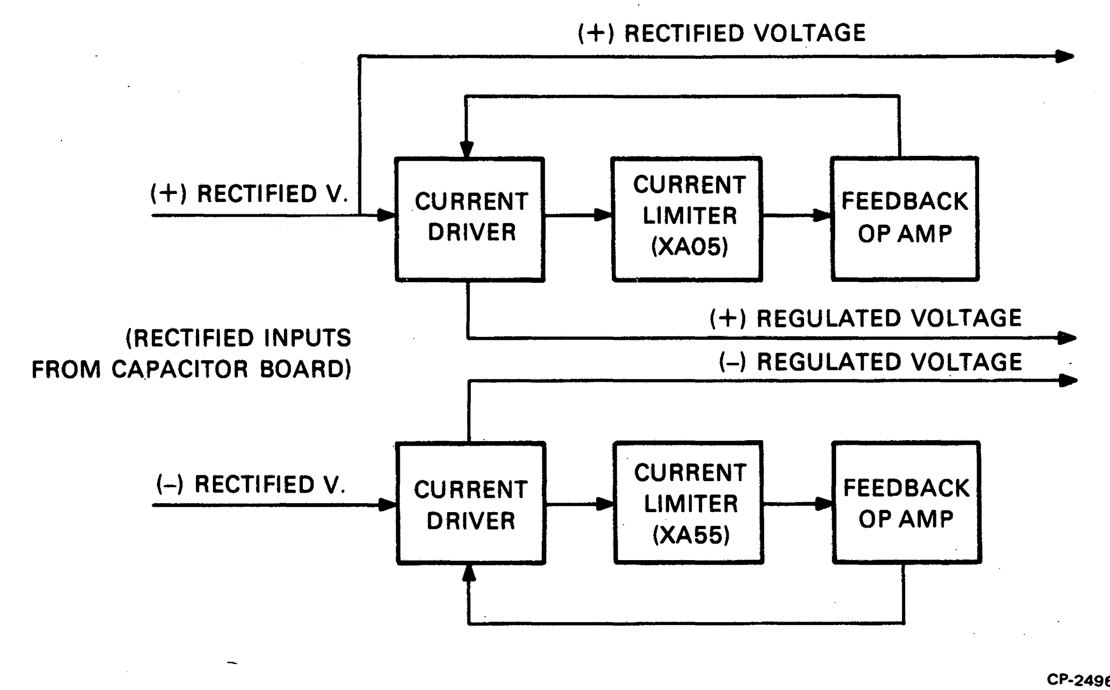


Figure 4-51 Electronics Board – Regulated +15 Vdc and Unregulated 25 Vdc Supplies

4.6.6 Spindle Brake Power Supply

This supply consists of a transformer and a rectifier, the output of which is approximately 11.5 Vdc. This dc voltage is used to decelerate the spindle motor when relay K3 on the capacitor module is energized. The spindle speed-sensing circuit will remove the braking current when the spindle is determined to be stopped.

4.6.7 Battery Supply

The 8-cell nickel-cadmium battery supply is for use in emergency retraction of heads to the home position under servo unsafe and power fail conditions. Each of the series-wired cells delivers a nominal 1.2 Vdc, for a total of 9.6 Vdc. The battery supply will apply this voltage to the linear motor when relay K1 on the capacitor module is deenergized and the heads are loaded to the home position. Under normal operating conditions, the battery is under a continuous trickle charge from the plus and minus 15 Vdc regulators.

4.6.8 Power-Low Detection
The power-low detection circuitry monitors the ac input power and the output of the regulators for low voltage conditions that may cause erratic drive operation, component failure, or loss of data on the data cartridge.

4.6.8.1 AC Low – During normal drive operation, an 18 ms one-shot is set by the presence of the 13 Vac from the CVT. If the ac voltage is missing or the voltage level is below specifications (approximately 85 Vac), the one-shot will time-out, generating the AC Low signal. After AC Low is generated, the drive continues to operate until the next sector pulse occurs, thus ensuring that any data transfer in progress will continue to the end of the sector before the heads are retracted.

4.6.8.2 DC Low – If the +15 Vdc or the –15 Vdc drops below 12 V, or if the +5 Vdc reference voltage drops below 4.6 V, DC Low is generated and the FET conducts, thereby asserting DC Low with a low impedance to ground. This signal is used to shut off interface transmitters so that the interface is not disturbed when voltages are low within the drive. This signal is also one of the drive interlocks for preventing undesired head loading if all the dc voltages are not proper.

4.7 CARTRIDGE HANDLING SUBSYSTEM
Figure 4-52 is the RK06 functional block diagram with the cartridge handling subsystem shaded.

4.7.1 Spindle Assembly
The spindle assembly provides the mounting surface for the cartridge and consists of the following.

- A spindle cone, which provides accurate rapid positioning of the cartridge with respect to the rotational centerline of the spindle
- A magnetic ring, which pulls down and holds the disk firmly against the horizontal spindle hub
- Precision bearings, which provide an accurate rotational assembly with minimum dynamic runout and a long rotational life
- Speed-sensing disk, with 12 slots on the outer rim allowing the LED/photosensor pair to output a pulse rate proportional to the rotational speed of the spindle
- A spring-tensioned ground button, in contact with the spindle shaft, that decouples any static electric charges that may build up on the disk and might possibly destroy the recorded data
- Spindle pulley, which provides coupling to the drive motor via the drive belt

4.7.2 Spindle Drive Motor and Belt
The disks of a cartridge assembly are rotated at a speed of 2400 rev/min by means of a single-phase, permanent-capacitor drive motor that is coupled to the spindle through a crowned pulley and a spring-tensioned belt. The shock-mounted spindle motor also functions as a dynamic brake for stopping disk rotation. To prevent the motor from possible overheating, it contains an auto reset thermal circuit breaker.

4.7.3 Brush Assembly
The brush assembly, driven by the 2 rev/min brush motor, swings inside the cartridge during the spindle-starting sequence to clean the four disk surfaces. This aids in removing any foreign particles from the cartridge, thereby reducing the probability of head/cartridge contact. A knob is provided to manually retract the brushes from the cartridge in the event of a malfunction or power failure.

4.7.4 Operational Sequence
See Paragraph 4.2.2.1 for the drive startup sequence.

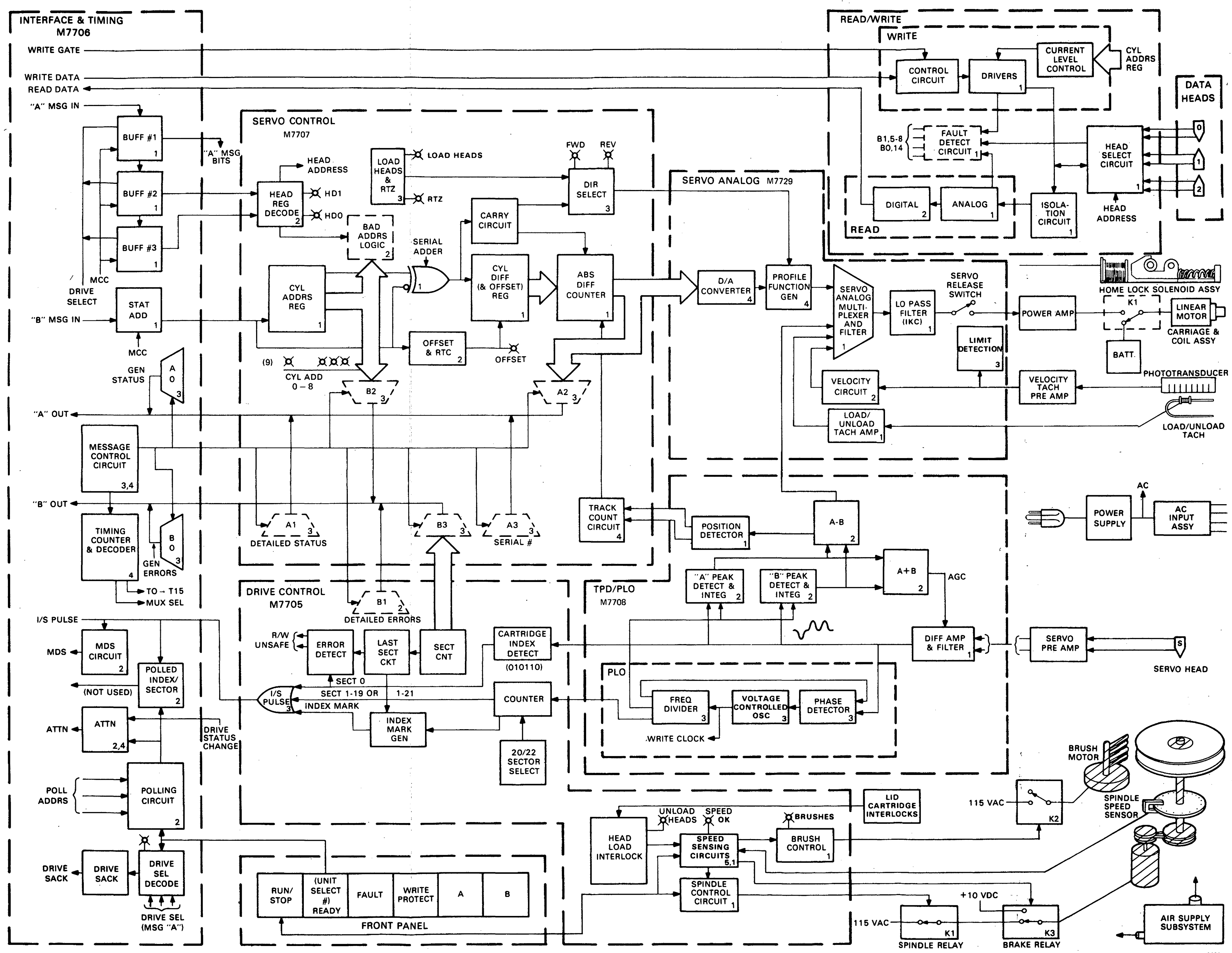


Figure 4-52 RK06 Disk Drive Functional Block Diagram with Cartridge Handling Subsystem Shaded

4.8 DUAL-ACCESS OPTION

The RK06 dual-access option enables the physical connection of this drive in two daisy-chain buses originating at two controllers (Figure 2-1). The controllers may be connected to different processors.

For the dual-access option, the drive houses two additional modules, an M7730 dual-port board and an M7706 interface and timing module. The two interface and timing modules interface with each controller. The dual-port board contains logic for controlling the access from both ports and acts as a multiplexer for commands and timing from each port to the remainder of the drive electronics. The dual-access option also uses a different backplane than the single-access option. See Figure 4-53 for the dual-access option block diagram.

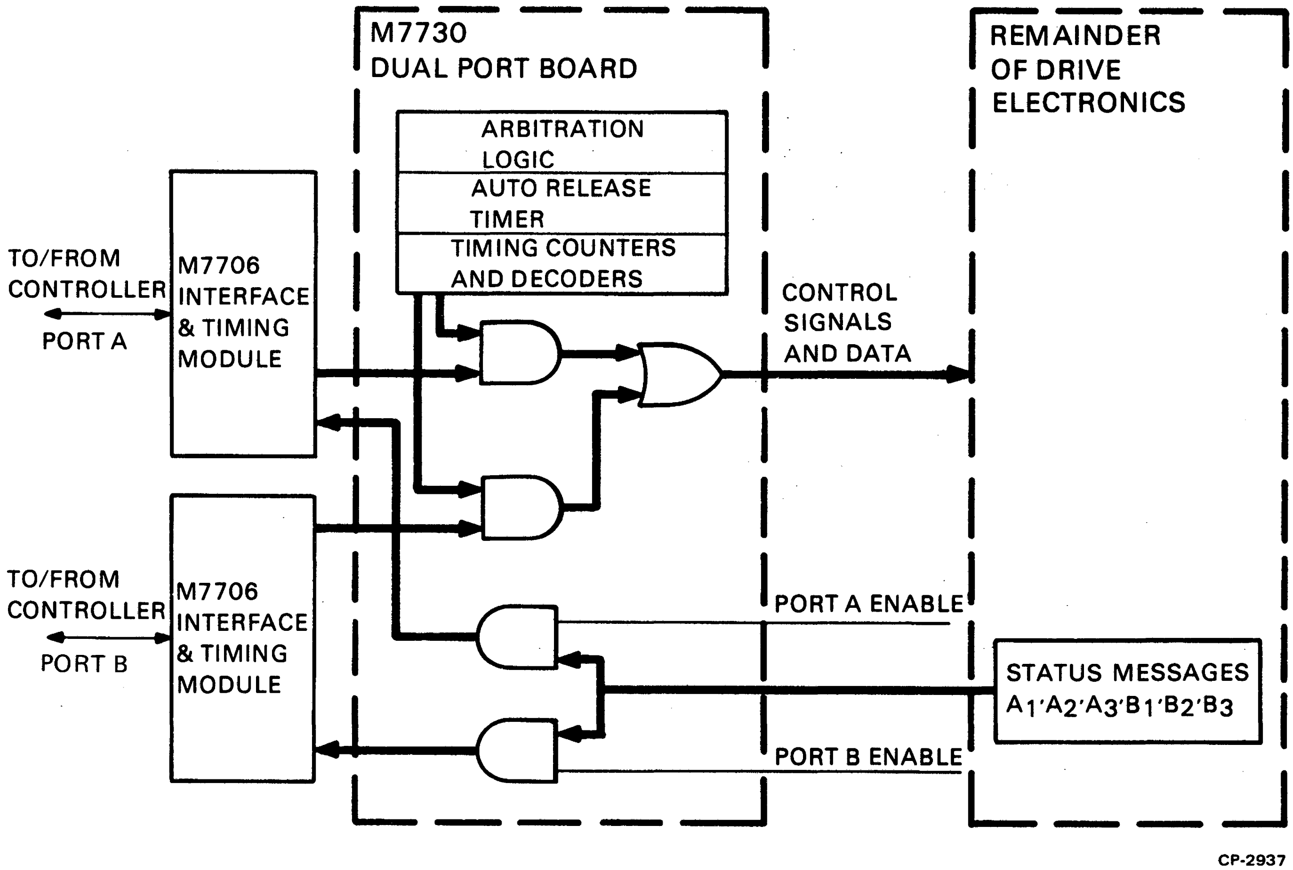


Figure 4-53 Dual-Access Option Block Diagram

4.8.1 Dual-Access Logic Circuits

The logic for the dual-access option is located on the M7730 module and consists of:

1. Arbitration Circuits
2. Timing Counters and Decoders
3. Auto-Release Timer
4. Multiplexers.

4.8.1.1 Arbitration Circuits – These circuits determine and control the state of the multiplexers for operating the drive through the two ports.

4.8.1.2 Timing Counters and Decoders – These circuits control the timing of transmissions from the controller that has seized the drive.

4.8.1.3 Auto-Release Timer – This timing circuit generates a signal that will automatically release a port if it has not been utilized within a 1 second period after it has gained access. See Paragraph 4.8.2.4.

4.8.1.4 Multiplexers – These circuits act as a single-pole, double-throw switch for each signal used by a port for operation of the remainder of the drive.

4.8.2 Dual-Access Operation

4.8.2.1 Seizing the Drive from the Neutral State – When the RK06 is in the neutral state, it is equally available to each port. There is no logic for priorities in the RK06 drive.

Any controller selecting the drive will cause the RK06 to switch to that port.

If the two controllers simultaneously attempt to seize the drive, a high-speed clock internal to the dual-port logic in the drive will arbitrate and one of the controllers will seize the drive.

4.8.2.2 Attempting to Seize an Unavailable Drive – If a neutral drive is seized by a port and the other port attempts to seize the drive, the latter port will find the drive unavailable. This will set the combined error bit in control and status register 1 (bit 15 in RKCS1). Also, the Drive Available bit in the Drive Status Register (bit 0 in RKDS) will be cleared as a result of a port attempting to seize an unavailable drive.

In addition to clearing bit 0 in RKDS, a port attempting to seize an unavailable drive will set the port request flip-flop in that drive. The dual-port logic checks the status of this flip-flop when the controller currently operating on the drive releases the drive. If the port request flip-flop is not set, this indicates that the port that was not just in use did not attempt to seize the drive. In this case, the drive then returns to the neutral state and it may then be seized by either port. If, however, the port request flip-flop is set, this means the other port attempted to seize the drive when it was unavailable. In this case, the other port seizes the drive.

For example, assume port A controls the drive. Port B tries to seize the drive and finds it unavailable. Thus, the port request flip-flop is set. When port A is finished with the drive, it releases the drive with a release command. Since the port request flip-flop is set, port B then seizes the drive.

4.8.2.3 Caution in Issuing a Release Command to an Unavailable Drive – The programmer should be careful, when designing software for use with the dual-access option, to avoid the following situation. Assume port A has seized the drive, and port B attempts to seize in and finds it unavailable. Suppose port B then decides to cancel its port request. If the release command from port B is completed before port A actually releases the drive, there is no problem. If, however, port A releases the drive while port B is still in the process of issuing a release command, the port B controller will find the attention asserted. The assertion of attention should have been prevented by the release of port B. This race condition can be avoided by not allowing a port to release its port request to an unavailable drive.

4.8.2.4 Auto-Release Timer – At the initiation of every command to the drive by the port that has access, a 1 second release timer is started. (The exception to this is the release command.) This timer is restarted with every new command issued by the controller having access to the drive. If a port accessing the drive does not release the drive and the 1 second release timer times out, the other port's port request flip-flop will be examined. If it is reset, the drive will go back to the neutral state. If the other port's port request flip-flop had been set, the following events take place.

1. The drive becomes deselected from the port that had access.
2. The drive is effectively seized by the other port.
3. The other port's attention is asserted, signifying that the drive is now available.

4.8.3 Start/Stop and Write Protect in Dual-Access

When the ac power is first applied to the RK06, the drive is initially in the neutral state. The volume valid bit for each port is cleared. A pack acknowledge command is required for each port.

The drive will not seek or write through a port unless that port has its volume valid bit set.

If a port issues the unload heads command, the 1 second auto-deselect timer is disabled. This has been instituted to allow a change of cartridge and not have the drive return to the programmable state. If the drive were allowed to return to the programmable state after an unload command, the other port could seize the drive and issue a conflicting command.

Once the drive is cycled up, the completion of the head-loading sequence asserts the attention bit of the port having access to the drive. For one additional second, the drive will be seized by that port.

The port having access must issue a command to the drive within this time. Failing to issue a command within this time will cause the dual port logic to examine the other port's port request flip-flop. If the flip-flop is not set, the drive will return to the neutral state. If the flip-flop is set, the drive will become seized by the other port and the other port's attention will be asserted.

If the drive is unavailable to a port and the RUN/STOP switch is changed, the port is notified by the assertion of its attention. The change is reported to the controller through the "spindle on" status bit.

When the write protect is asserted, neither port will be able to do a write operation. There is no provision to write protect the drive through one port and not have it write protect through the other.

If the drive is seized to a port and the operator changes the status of the write protect switch, the other port is notified through the assertion of its attention. The change is reported to the controller through the write lock status bit.

4.8.4 Error Handling in Dual-Access

Notifying the Controller of an Error

Errors occurring while the RK06 is seized by one of the controllers is reported to and should be serviced by that controller. The other port is not notified of these errors. The exception is a parity error in a message to the drive on the other port.

If the drive had been in the neutral state and an error occurred, both attention bits would be asserted. The fault bit would be read by both controllers when servicing the attention set in the drive. However, only one of the controllers would service the error in the drive.

Clearing the Drive Errors and Resetting the Attention
Either controller may issue a drive clear at any time. The attention in the drive will be cleared by a drive clear regardless of the drive's availability. However, to clear the flip-flops storing the error information, the drive must be seized to the port issuing the clear command as mentioned. The controller to drive parity error is handled differently than the other errors and is discussed in greater detail as follows.

Multiple Drive Select and CTD Parity Errors in the Dual-Port Configuration
If a controller has seized a drive and multiple drive select is detected in the drive, the drive handles this as an unsafe condition and unloads the heads.

If a controller has seized a drive and multiple drive select is detected on the other port, the drive detects the condition but does not set fault and unsafe, and does not unload the heads. The port detecting multiple drive select reports it to the controller regardless of whether it had access to the drive.

Controller-to-drive (CTD) parity errors are detected and stored separately for each port. Unlike all other errors, the CTD parity error flip-flop is cleared with a drive clear regardless of whether or not that controller has seized the drive. The attention in the port is raised when a CTD parity error occurs.

4.8.5 Initialize in Dual-Access
The RK06 will honor an "initialize" issued separately from either port. The effect the "initialize" has depends upon the availability of the drive to the port issuing the command. The three drive conditions are described.

1. Drive is seized by a port. At this time, an initialize will:

   a. Clear that port's attention bit
   b. Clear the error flip-flops in the drive
   c. Cause the port to release the drive.

   If the other port's port request flip-flop is cleared, the drive will be returned to neutral. If the other port's port request flip-flop is set, the drive will become seized by the other port.

2. Drive is in neutral. At this time, an initialize will:

   a. Clear the port's attention bit
   b. Clear the error flip-flops in the drive.

3. Drive is seized by other port. At this time, an initialize will:

   a. Clear the port's attention bit
   b. Cancel a port request if one is pending.

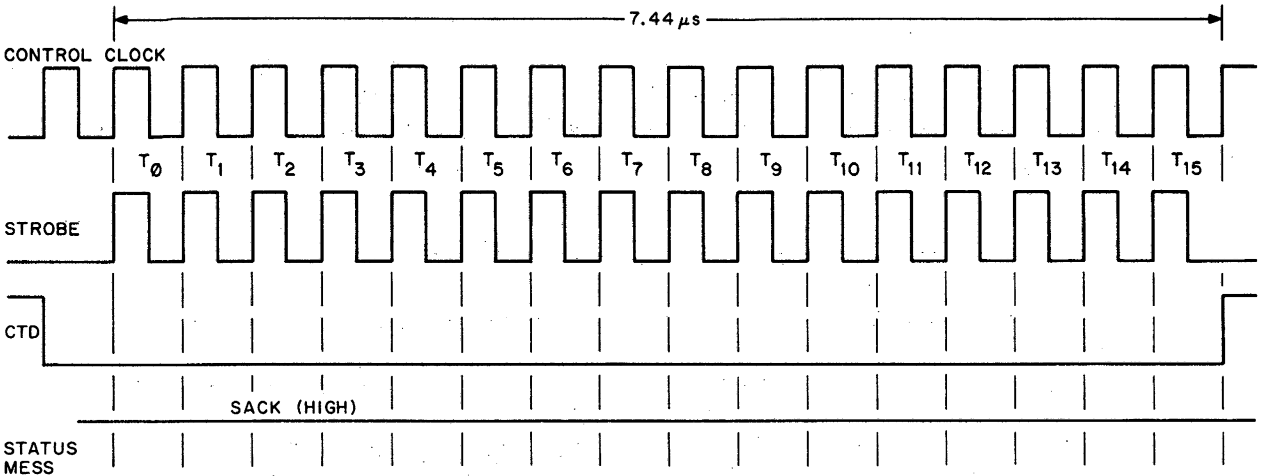
4.8.6 Getting Drive Status in Dual-Access Mode

If the drive is seized by one of the ports, that port's controller may interrogate any of the eight status multiplexers (A0, B0, A1, B1, A2, B2, A3, B3) within the drive.

If the drive cannot be seized (busy with another port), only status multiplexers A0 and B0 may be read through the unseized port. This situation causes the combined error bit (bit 15 in RKCS) to be asserted in the controller of the unseized port. Refer to Figure 4-54 for the data bits contained in drive status messages A0 through B3.

Status Bits Pertinent to Dual-Port Available at the Unibus Interface

1. Drive available (DRA) – This bit is set to the port that has access to the drive and reset to the other port. Read only.
2. Volume Valid (Vol. Val.) – This bit is used to indicate when a disk cartridge may have been changed. There is a volume valid bit for each port.
3. Ready (RD) – Indicates that the selected drive is up to speed and its heads are settled over the specified cylinder. This bit will always be reset to a port not having access to the drive.



MESSAGE LINE A	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
A0	DRIVE SELECT CODE			RESVD		DR AVAIL	VOL VAL	DR READY	DRIVE TYPE	20 SECT FORMAT	OFFSET ON	WR LOCK	SPINDLE ON	PIP	DR STATUS CHANGE	PARITY
A1	DRIVE SELECT CODE			RESVD	SERVO SIGNAL PRES	HEADS HOME	BRUSH HOME	DOOR LTCHD	CART PRES	SPEED OK	FWD	REV	LDG HDS	RTZ	UNLDG HDS	PARITY
A2	DRIVE SELECT CODE			RESVD	CYLINDER DIFFERENCE/OFFSET VALUE									(1)	RESVD	PARITY
A3	DRIVE SELECT CODE			DRIVE SERIAL NUMBER												PARITY

MESSAGE LINE B	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
B0	MESS ID (0) (0)		RESVD FOR ADD'L MESS		RESVD	INV ADDR	AC LOW	FAULT	NXF	C-D PRTY ERR	SEEK INC	WR LOCK	SPEED LOSS	DR OFF TRACK	RD/WR UNSAFE	PARITY
B1	MESS ID (1) (0)		RESVD FOR ADD'L MESS		SECTOR ERR	WR CNT & NO WRITE GATE	WRITE GATE & NO TRANS	HEAD FAULT	MULT HD SEL	INDEX ERR	TRIBIT ERR	SERVO SIG ERR	SEEK & NO MOTION	LIM DET ON SEEK	SERVO UNSAFE	PARITY
B2	MESS ID (0) (1)		RESVD FOR ADD'L MESS		CYLINDER ADDRESS									(1)	RESVD	PARITY
B3	MESS ID (1) (1)		RESVD FOR ADD'L MESS		SECTOR COUNT					DECODED HEAD ADDRESS			RESVD		RESVD	PARITY

DRIVE-TO-CONTROLLER TRANSMISSIONS

NOTE:
(1) – THESE BITS ARE USED ONLY ON THE RK07.

11-5328

Figure 4-54 Drive Status Bits Contained in A and B Messages

CHAPTER 5
RK07 UNIT-LEVEL THEORY OF OPERATION

This chapter provides a detailed technical description of the RK07 Disk Drive. A similar presentation for the RK06 Disk Drive is given in Chapter 4. The discussion is organized around the following major subsystems.

1. Physical description (Paragraph 5.1)
2. Drive control subsystem (Paragraph 5.2)
3. Positioning subsystem (Paragraph 5.3)
4. Read/write subsystem (Paragraph 5.4)
5. Air supply subsystem (Paragraph 5.5)
6. Power supply subsystem (Paragraph 5.6)
7. Cartridge handling subsystem (Paragraph 5.7)
8. Dual-access option (Paragraph 5.8)

Figure 5-1 is the major block diagram for the RK07 Disk Drive. In each of the subsystem discussions, the relevant portion of this same diagram is highlighted by showing the functional blocks of that subsystem as shaded areas. All other blocks are unshaded.

5.1 PHYSICAL DESCRIPTION

The disk drive consists of two major assemblies and a group of discrete assemblies. The two major assemblies are a base plate assembly and a chassis assembly.

The electromechanical subassemblies comprising the base plate assembly (Figure 5-2) are mounted on a cast aluminum base that is attached at three points to the chassis assembly through vibration isolators.

The chassis assembly (Figure 5-3) consists of a riveted sheet metal structure that provides a plenum for cooling air distribution as well as a mounting structure for numerous electromechanial subassemblies. Assemblies other than the base plate and the chassis are explained in the following paragraphs covering the drive subassemblies. The disk cartridge assembly, not considered as an integral part of the disk drive but designed for use with it, is described in Paragraph 2.3.

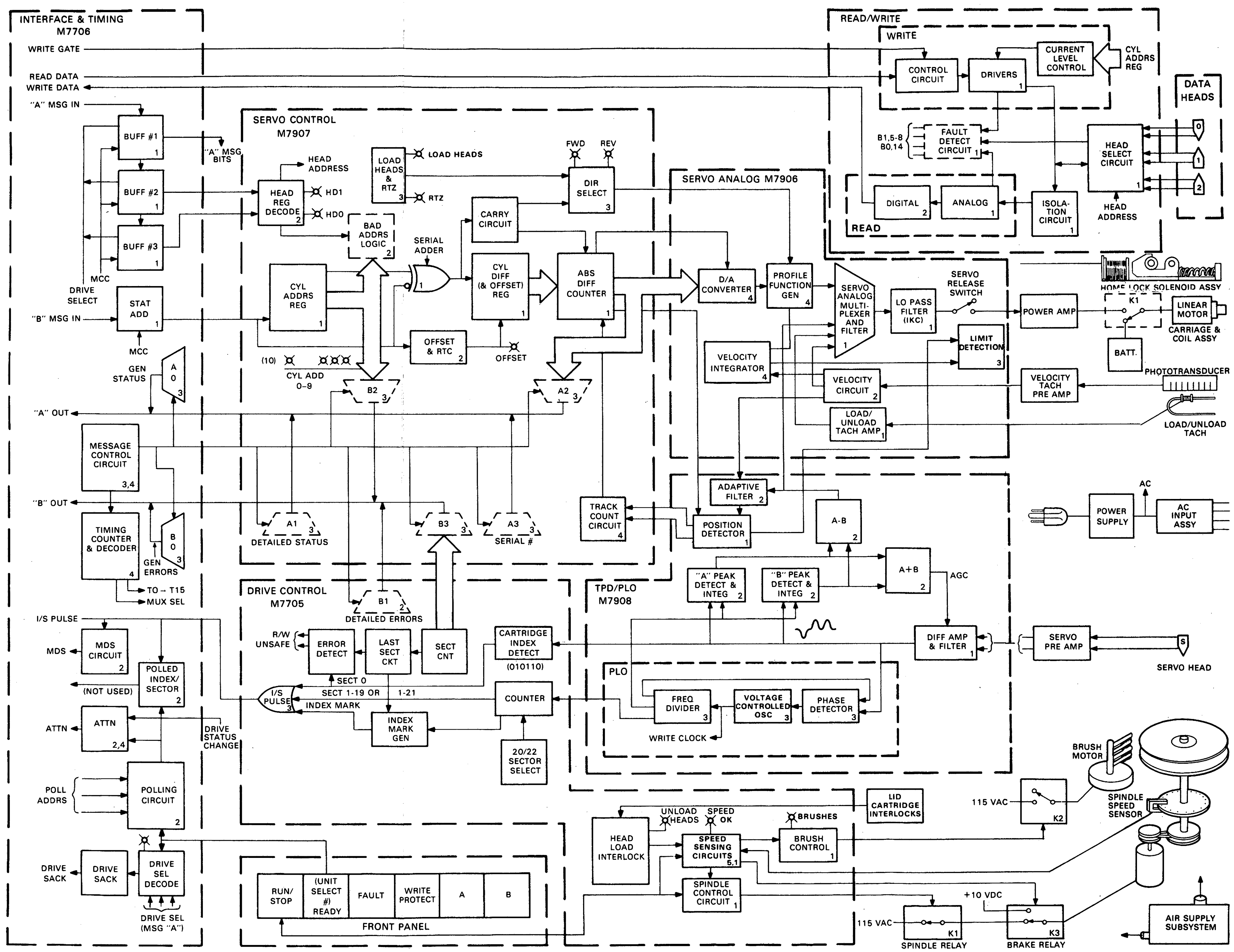


Figure 5-1 RK07 Disk Drive Functional Block Diagram

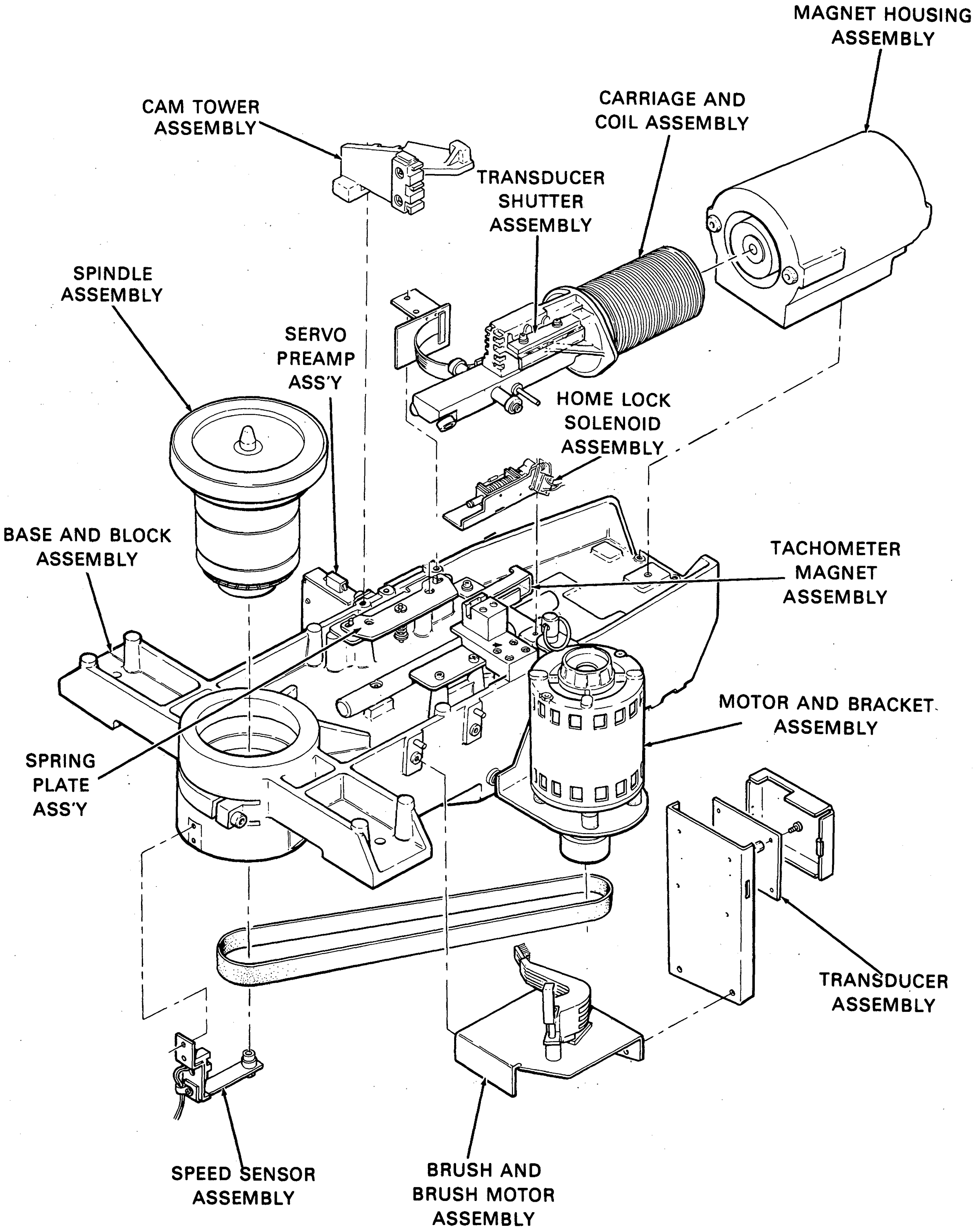


Figure 5-2 Base Plate Assembly

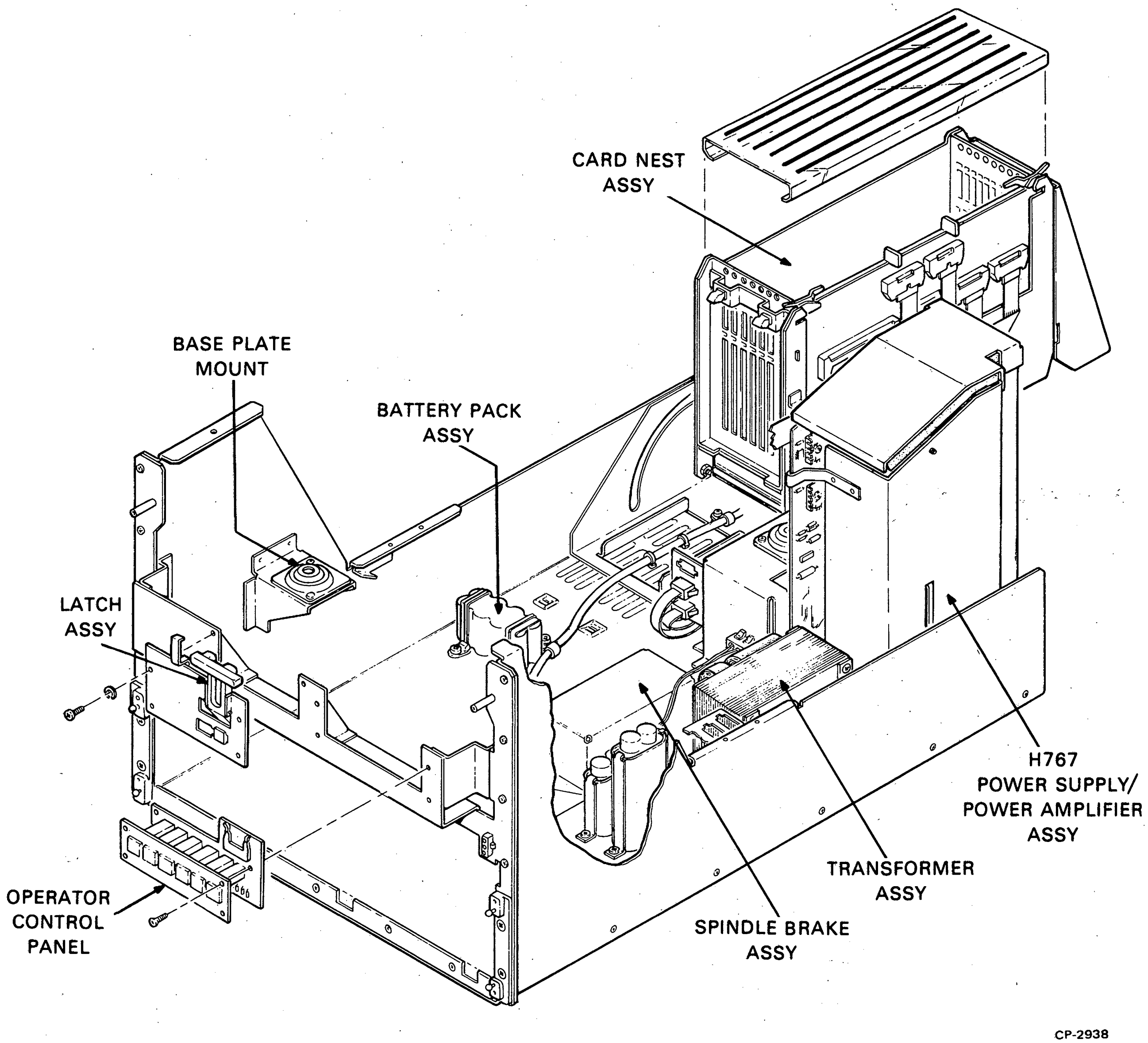


Figure 5-3 Chassis Assembly

5.1.1 Base Plate Assembly

The base plate assembly (Figure 5-2) consists of the following subassemblies.

1. Base and block assembly
2. Carriage and coil assembly
3. Spindle assembly
4. Home lock solenoid assembly
5. Transducer assembly
6. Tachometer magnet assembly
7. Servo preamp assembly
8. Speed sensor assembly
9. Brush and brush motor assembly
10. Magnet housing assembly
11. Motor and bracket assembly
12. Spring plate assembly
13. Cam tower assembly
14. Transducer shutter assembly

5.1.2 Chassis Assembly

The riveted chassis assembly (Figure 5-3) provides a plenum for air distribution and supports to which the base plate assembly is attached through vibration isolators. The chassis assembly serves as a mounting structure for the following assemblies.

1. Card nest assembly
2. H767 power supply assembly
3. Latch assembly
4. Spindle brake assembly
5. Battery pack assembly
6. Transformer assembly
7. Operator's control panel
8. Power harness assembly
9. Harness, A/C distribution

5.1.3 Card Nest Assembly

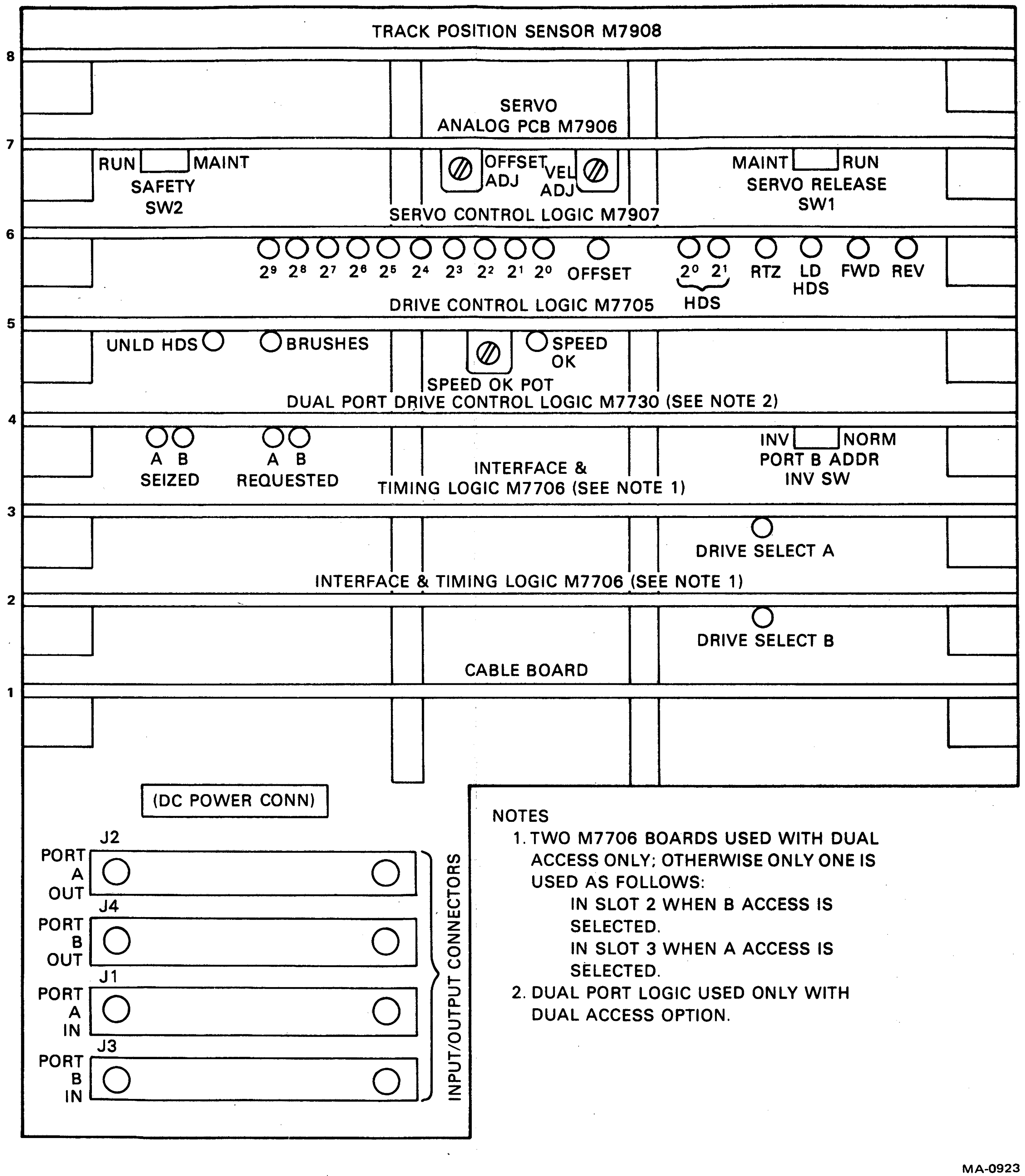
The card nest assembly, located at the left rear of the drive, has guided slots for eight printed circuit boards (modules). Single-access drives use the following modules (Figure 5-4).

1. Drive Control Logic (M7705)
2. Interface and Timing Logic (M7706; either A or B access)
3. Servo Control Logic (M7907)
4. Track Position Detector/Phase Lock Oscillator (PLO) (M7908)
5. Servo Analog (M7906)
6. Cable Board (M9016)

Dual-access drives, in addition to these boards, also use the following boards.

1. Interface and Timing Logic (M7706) (alternate access)
2. Dual-Port Drive Control Logic (M7730)

Visual indicators (LEDs), velocity potentiometer, speed OK potentiometer, a servo safety switch, a servo release switch, and a dual-port maintenance switch are mounted on the boards at the locations indicated in Figure 5-4. The hinged card nest rotates through an angle of approximately 90 degrees from its normal operating position within the chassis assembly. With the card nest in this position, the plastic cover, with various LEDs, switches, and potentiometers marked on the cover, becomes accessable.



NOTES
1. TWO M7706 BOARDS USED WITH DUAL ACCESS ONLY; OTHERWISE ONLY ONE IS USED AS FOLLOWS:
   IN SLOT 2 WHEN B ACCESS IS SELECTED.
   IN SLOT 3 WHEN A ACCESS IS SELECTED.
2. DUAL PORT LOGIC USED ONLY WITH DUAL ACCESS OPTION.

Figure 5-4 I/O Connectors and Card Nest Assembly

5.1.4 Miscellaneous Assemblies

Several assemblies of the drive are not included in either of the major assembly categories, i.e., the base plate assembly and the chassis assembly. These separate assemblies are:

1. Lid assembly
2. Shroud assembly (Figure 5-5)
3. Circuit breaker assembly
4. Front bezel assembly
5. Lower bezel assembly
6. Rear cover assembly
7. Air filter assembly.

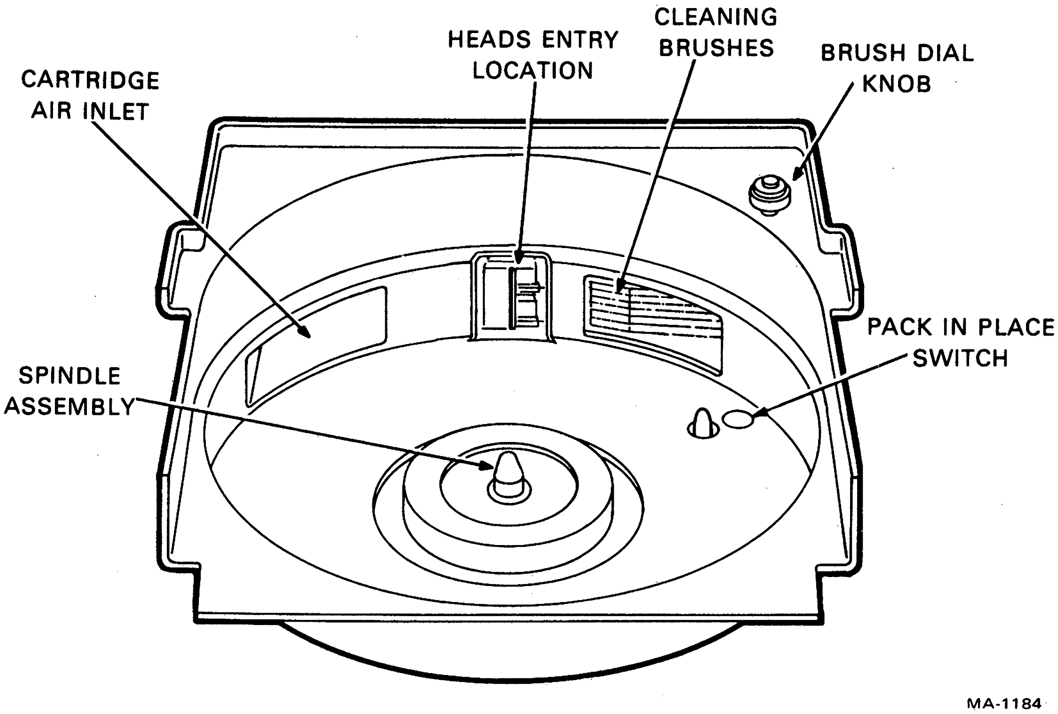


Figure 5-5 RK07 Cartridge Shroud Assembly

Front Bezel

The front bezel covers approximately the upper two-thirds of the front of the chassis assembly and contains cutouts through which the buttons on the switches of the operator's control panel protrude.

The lid-latch release button protrudes through a horizontal slot on the front surface of the bezel. The bezel is located on the chassis asssembly by means of two dowel pins at the bottom and is held in place on the chassis assembly by two screws near the top. Removal of this bezel is required for access to the following.

1. Latch assembly
2. Speed sensor assembly
3. Operator panel assembly
4. Spindle clamp bolt
5. Spindle drive belt
6. Blower assembly

Bottom Bezel
The bottom bezel covers approximately the lower one-third of the front of the chassis assembly. Ambient air for cooling the electronics is inducted through horizontal slots in the bezel. The bezel is mounted to the chassis assembly by means of snap-on connectors. Removal of this bezel is necesssary for access to the following.

1. Blower assembly
2. Air filter assembly
3. Speed sensor assembly
4. Blower prefilter
5. Spindle drive belt
6. Spindle clamp bolt

5.2 DRIVE CONTROL SUBSYSTEM
The drive control subsystem (see the shaded blocks in Figure 5-6) comprises those elements that control the flow of command and status data to and from the drive; provide interlocks for safe operation; and control index and sector generation circuits, circuits for controlling spindle motor rotation, and the cartridge brush cycle.

5.2.1 Functional Sections

5.2.1.1 Operator's Control Panel – Figure 5-7 is an illustration of the operator's control panel. The panel consists of the following switches and indicators.

1. RUN/STOP switch with load indicator
2. Unit select switch with READY indicator
3. FAULT indicator
4. Write lock switch with WRITE PROT indicator
5. Access A enable switch
6. Access B enable switch

All control panel switches are solid-state Hall-effect devices except for the unit select switch, which does have contacts. The Hall-effect switches interface directly to the TTL logic.

RUN/STOP Switch with Load Indicator – When pressed, this push/push alternating action switch energizes the spindle motor. When released, it deenergizes the spindle motor if the heads are not loaded. If the heads are loaded, it causes the heads to unload and the spindle motor to deenergize in sequence. Since this switch has a mechanical memory, a power interrupt followed by power restoration will, if the switch is in its depressed position, cause the drive to automatically cycle up when power is restored.

The start spindle command from the controller is not enabled unless: (1) the RUN/STOP switch is in the depressed state and the drive has been cycled down due to a set medium off-line command, or (2) any of the errors leading to head unload occur. In the second of these situations, the heads will not reload unless the error condition has been cleared.

The load indicator of the RUN/STOP switch illuminates whenever: (1) the spindle is less than 1 rev/second, (2) heads are home, (3) brushes are home, and (4) the spindle motor is not energized.

Unit Select Switch with Ready Indiator – The unit select switch is a cam-operated switch that is actuated by inserting a numbered cammed button. The contacts are binary encoded such that the drive logic will recognize the drive address code corresponding to the unit select number. The numbered indicator is lit indicating a READY condition, whenever the heads are loaded and detented on a cylinder or detented in an offset position.

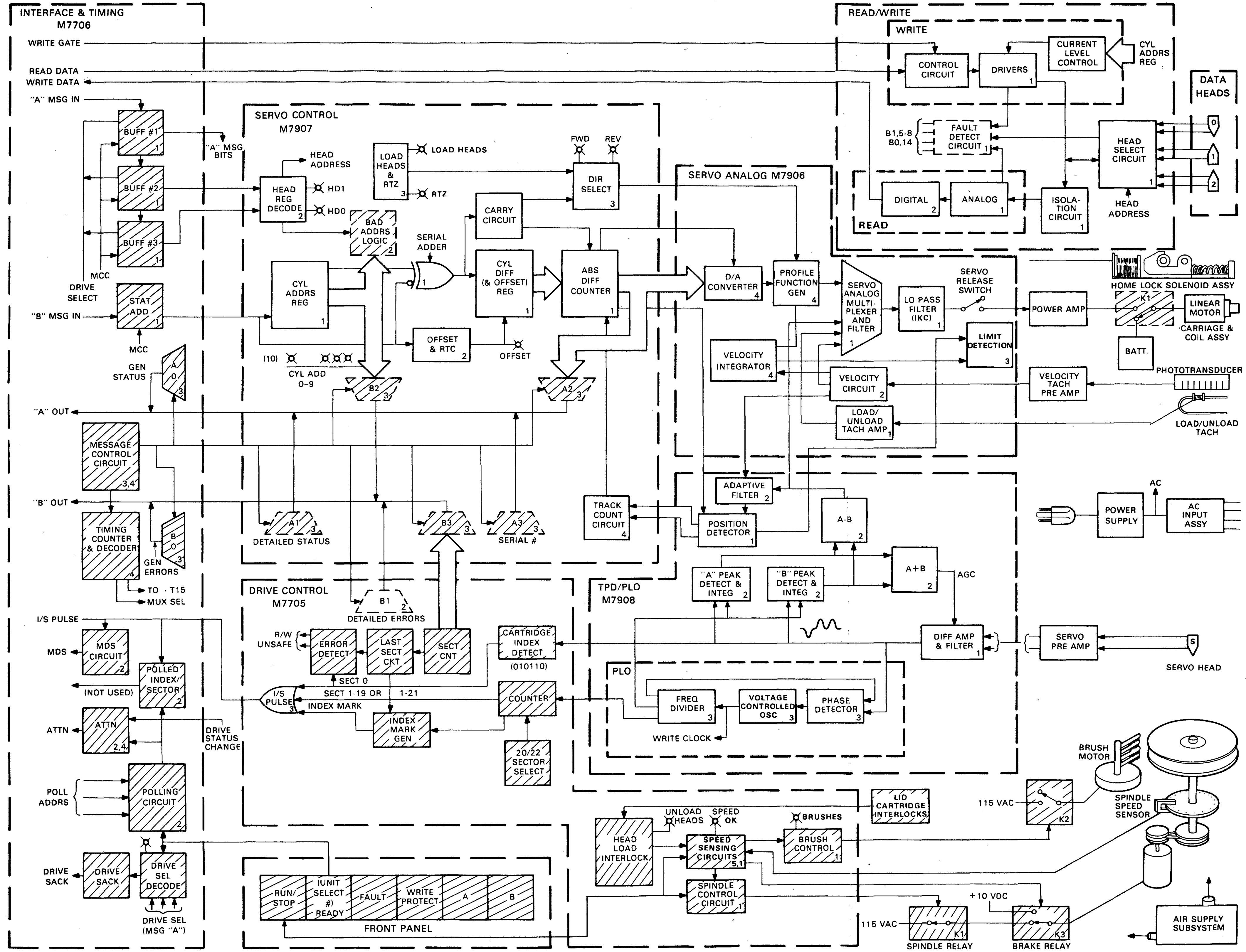


Figure 5-6 RK07 Disk Drive
Functional Block Diagram
with Drive Control Subsystem Shaded

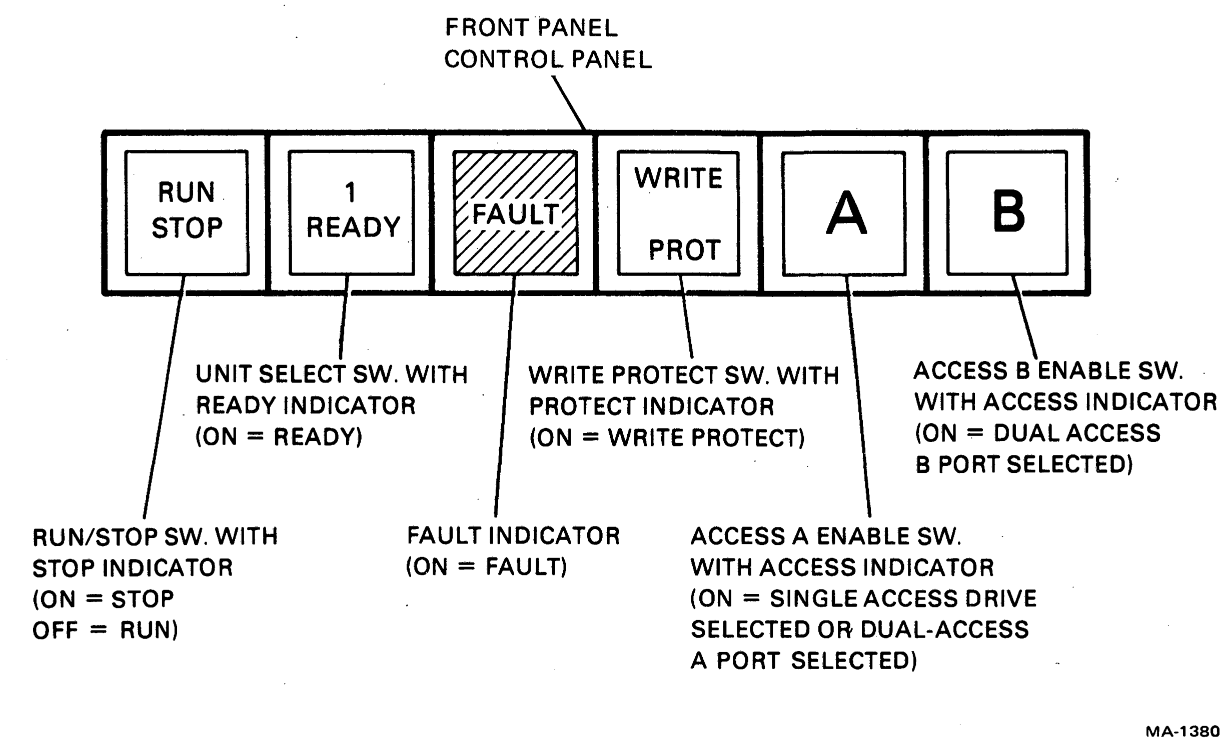


Figure 5-7 Operator's Control Panel

FAULT Indicator – This indicator is lit whenever a fault or error condition develops in the drive. Each fault or error that causes the indicator to illuminate is described in Table 3-7, bit 7, where "Fault" is defined.

Write Protect Switch with WRITE PROT Indicator – This push/push alternating-action switch, when pressed, places the drive in write protect mode only when Write Gate is not asserted in the drive. If Write Gate is asserted at the time that the switch is pressed, write protect will be inhibited until Write Gate is negated. Additionally, the WRITE PROT indicator will not be lit until write protect is truly enabled. Removal of write protect will occur immediately upon the release of the switch.

Access A Enable Switch – This alternating action push/push switch, when pressed, enables communication to and from the drive via the A set of input/output connectors under the following conditions.

1. If the drive is single access only, the interface and timing module must be located in the appropriate module slot for that set of connectors. When this is the case, the access A enable switch enables (when pressed) or inhibits (when released) communication to/from the drive. For single access, the indicator on this switch indicates when the drive is selected.

2. If the drive includes the dual-access option, this switch enables/inhibits communication via the A set of input/output connectors. When both the access A and access B switches are pressed, arbitration logic selects the appropriate access to the drive. For dual-access drives, the indicators on the A and B switches indicate which drive I/O channel is in use.

Access B Enable Switch – This switch is functionally identical to the access A enable switch except that this switch enables or inhibits communication via the B set of input/output connectors.

Dual-Access Option – If the drive includes the dual-access option, the access-enable switches enable (when pressed) and inhibit (when released) communication via that access. When both access switches are pressed, arbitration logic in the drive selects the appropriate access. In dual-access drives, the access in use at any time is indicated by an illuminated condition of the indicator of the associated access switch.

5.2.1.2 Interlocks – The interlock sensors and circuits provide for the safe operation of the disk cartridge and the heads. In some cases, these elements prevent spindle startup and in other cases, they prevent head loading unless they are satisfied. Similarly, the heads are unloaded if any of the interlocks become negated.

The drive interlocks include:

1. Lid-locking solenoid
2. Lid-locked sensor
3. Cartridge-present sensor
4. DC low sensor
5. AC low sensor
6. Spindle-speed sensor
7. Speed-sensing circuits
8. Brushes-home sensor
9. Read/write unsafe error
10. Servo unsafe error
11. Limit detect on seek error
12. Proper cartridge interlock (Paragraph 1.6).

Lid-Locking Solenoid – This solenoid is energized for the unlocked condition of the lid; i.e., it is energized only for the condition when it is safe to access the cartridge. As a result, the lid is locked when power is off, the heads are not at their home position, the brushes are not at their home position, or the spindle is not stopped.

The lid must be locked for the power-off condition. In the event that power was interrupted unexpectedly, the spindle takes considerable time without power to come to a stop. Furthermore, if the brush cycle were underway at power interrupt, the brushes might not complete their cycle. Both conditions would yield an unsafe situation for accessing the cartridge.

Lid-Locked Sensor – This switch senses that the lid is closed, latched, and the lid-locking solenoid is in the locked condition. When locked, the switch is closed.

Cartridge-Present Sensor – This switch senses that an RK07 cartridge is loaded in the drive and that its protective cover has also been placed over it within the drive.

DC Low Sensor – This electrical signal is generated within the power supply. Its output to the drive control circuits is an FET switch which is in the off state when all of the dc voltages are within specifications and on (or a low impedance to ground) when one or more voltages are below specifications.

In addition to being an interlock, a dc low condition inhibits the interface such that the drive will not disturb other drives on the bus.

AC Low Sensor – This signal is generated in the power supply in a similar manner to the dc low condition. This signal will unload the heads starting at a sector boundary. It is designed in this manner so that if a data transfer is occurring at the moment that ac low is sensed, the operation will be completed. This is acceptable because the dc voltages are guaranteed within range for at least 3.9 ms, thus enabling the completion of a sector.

Spindle-Speed Sensor – The spindle-speed sensor is an optical switch that generates pulses at a rate proportional to the rotational velocity of the spindle. The sensor consists of an LED source, a phototransistor receiver, and a slotted disk that is part of the spindle assembly. As the spindle rotates, the phototransistor alternately receives light from the LED and is blocked from receiving light.

The pulsed Spindle-Speed signal is applied to two retriggerable single shots on the M7705 module, one of which senses repetition rate of the pulses for the speed OK condition for loading heads and the other for determining the spindle stopped condition for unlocking the lid.

Brushes-Home Sensor – This switch senses that the brushes are fully retracted at the brush-home position. If they are not retracted, the lid-locking solenoid keeps the lid locked. Furthermore, the heads are inhibited from being loaded until the brushes complete the cleaning cycle.

Read/Write Unsafe Error – This condition, when asserted, unloads the heads if loaded or prohibits loading if unloaded. It is indicative of a faulty condition that would result in potential loss or misplacement of data on the cartridge. See Paragraph 5.4.4 and Table 3-7 for components of this error.

Servo Unsafe Error – This condition, when asserted, causes the positioner to retract under the battery power. Unless it is cleared, the positioner is furthermore inhibited from loading the heads. This condition is indicative of the servo system being out of control. It is generated by a circuit that senses that a current command is above a selected threshold of 20 ms.

Limit Detect on Seek Error – This error is generated if, for any reason, the Outer Limit or the Inner Limit signal is sensed whenever the positioner is not being loaded, unloaded, or doing a recalibrate. It is reset by any of the error-clearing signals in the drive (Table 3-8, Bit 13).

5.2.1.3 Index/Sector Pulse Generation Circuits – The index/sector pulse generation logic of the drive control module (M7705) consists of:

1. The index decoder
2. Sector counter and generator
3. Index mark generator
4. Index/sector OR gate.

Index Decoder – These circuits on the M7705 module consist of an 8-bit shift register and gating for the decode of the index pattern and a flip-flop for synchronizing the decoded index with the servo clock. This Decoded Index signal becomes the sector 0 pulse and is a nominal 3.7 μs wide.

Sector Counter and Generator – The sector counter and sector pulse generator circuits on the M7705 generate either 19- or 21-sector pulses per cartridge rotation, depending on the format, which is selected by the system. These circuits are synchronized to the Index signal and are generated by counting SVO CLK L pulses from the M7908 TPD/PLO (Paragraph 5.3.1.19). All of these sector pulses, except the sector 0 pulse described above, are a nominal 1.86 μs wide.

Index Mark Generator – The Index Mark signal generated on the M7705 is a derived signal for synchronizing the sector count for the controller. This pulse is located in the last sector in either format beginning a nominal 178 μs after the leading edge of the last sector pulse and having a nominal 59.2 μs duration. When the composite of this and the sector pulses is transmitted over the interface, the Index Mark signal identifies the next pulse as the beginning of sector 0.

Index/Sector OR Gate – This gate on the M7705 combines the index pulse (sector 0 pulse), sectors 1–19 or 1–21 pulses, and the Index Mark signal into a composite signal for transmission to the controller over the interface.

5.2.1.4 Spindle-Control Circuits - This logic circuitry is located on the M7705 module and consists of the gating and the run flip-flops and relay driver for controlling the relay that energizes the spindle motor. The run flip-flop may be set by the RUN/STOP switch on the operator's control panel or from a command from the interface if the RUN/STOP switch is pressed, provided the heads are home and the interlocks are all asserted. It is reset by: (1) the release of the RUN/STOP switch, (2) command from the interface, or (3) an unsafe interlock condition that causes the heads to unload. It should be noted that the spindle will not be deenergized until the heads are at the home position to preclude the possibility that the heads would crash on the disk surfaces if the servo malfunctions and fails to retract the heads.

There is one case where the spindle will be deenergized before the heads are home. This occurs if servo unsafe (Paragraph 5.2.1.2) is detected. For this case, servo unsafe is an indication of servo malfunction and it is therefore assumed that the heads may not retract under servo control properly. As a result, the spindle is immediately deenergized and the battery retracts the positioner directly. The servo unsafe condition is inhibited when the maintenance switch is enabled.

5.2.1.5 Brush Control Circuits - This logic circuitry on the M7705 module controls the brush disk cleaning cycle. The brush cycle is initiated when the disk is nearly at the safe speed for head loading on drive startup. The cycle lasts approximately 11 seconds and is terminated when the brushes return to the brush-home location. The brush cycle, once started, must be completed, since it cannot be reversed. The controlling flip-flop is applied to a relay driver which controls the relay for energizing the brush motor.

5.2.1.6 Message Control Logic - These circuits on the M7706 module use the CTD, Strobe, and Control Clock signals from the interface to generate an Input-Enable signal and an Output-Enable signal that enable and inhibit the receipt and transmission of interface messages, respectively.

5.2.1.7 Timing Counter and Decoder - These logic circuits on the M7706 generate individual decoded timing pulses (T0 to T15) as a result of counting control clock pulses during the receipt of interface messages only. The counter is used for controlling both the receipt and transmission of messages but the decoder is used only on incoming transmissions.

5.2.1.8 Multiple Drive Select (MDS) Logic - To avoid the possibility of two or more drives simultaneously writing data destined for only one of them, it is necessary to have a means of determining if more than one drive has been selected. This could occur either by a malfunctioning circuit in one of the drives or in the event that identical drive-numbered unit select plugs were inserted in each drive.

Logic circuits in the M7706 module are designed to sense if another drive is also selected in the daisy-chain bus. It is accomplished by monitoring the Index/Sector signal line. The sensing of the signal on the bus from another source results in a multiple drive select error. This is valid because only a selected drive transmits on this line.

When the heads of a selected drive are loaded, the index and sector pulses are transmitted over the interface. When they are unloaded, the selected drive transmits the control clock on the interface. As a result, a selected drive compares any pulse on the interface to its own Index/Sector signal internal to the drive. If there is no comparison, the Multiple Drive Select signal is asserted on the interface.

5.2.1.9 Drive Select Decode - This logic circuitry on the M7706 module compares the first three bits of a transmission to the drive on Message Line A with the number represented on the unit select plug. The first three bits of a transmission represent the drive number to be selected in binary-encoded form with the least significant bit first. These bits are shifted into the BUFF 1, BUFF 2, and BUFF 3 flip-flops, after which the comparison is made. Note that all the drives on the bus are selected in order to receive the transmission. Each drive's comparison with the unit select plug number leaves only the requested drive selected.

5.2.1.10 Drive SACK – This flip-flop on the M7706 module represents a select acknowledge by the selected drive to the controller following the receipt of the drive select code and the time for the deselect code. If the drive is truly selected, the SACK flip-flop sets and remains set until the beginning of another message, at which time it resets.

5.2.1.11 Polling Logic – This logic circuitry on the M7706 module accepts the receipt (from three interface lines) on a continuously polling basis, the eight drive numbers in binary-encoded form. For each drive number, a comparison is made with the number as represented by the unit select plug. When a comparison is made, the Enable Pollout signal is generated which enables the Attention signal, if asserted, to be transmitted on the interface. In this manner, the system can rapidly determine which drive(s) assert Attention, causing an interrupt.

5.2.1.12 Attention – This signal is transmitted over the interface when requested by the controller from the polling addresses it transmits. The Attention corresponding to drive status change (A0, T14) is asserted from any of a number of conditions (Table 3-2).

5.2.2 Control Operation

The following paragraphs describe the various operations pertinent to the drive control subsystem. These operations are:

1. Drive Startup (Paragraph 5.2.2.1)
2. Spindle Stopping (Paragraph 5.2.2.2)
3. Index/Sector Circuit Operation (Paragraph 5.2.2.3)
4. Command and Status Data Control (Paragraph 5.2.2.4).

5.2.2.1 Drive Startup – The drive is initially started by pressing the RUN/STOP switch on the operator's control panel. With the lid closed, the lid-locking solenoid will now release, causing the lid to lock shut. The coincidence of the lid shut and locked yields the lid-locked interlock condition. If this interlock and all others (Paragraph 5.2.1.2) are satisfied, the run flip-flop will set and the relay driver will energize the spindle relay (if there is no servo unsafe condition), which in turn applies power to the spindle motor.

As the spindle begins to rotate, the spindle speed sensor generates pulses proportional to the rotational speed. Once the period of the speed pulses becomes less than 100 ms per pulse, the retriggerable single-shot which determines the stopped condition will no longer time-out and, as a result, the stopped flip-flop will reset. This causes the stopped indication on the RUN/STOP switch to extinguish. Note that this takes approximately 1 to 2 seconds from initial startup. In newer drives, the spindle motor will stop immediately if speed pulses are not sensed.

As the speed increases such that the period of the speed pulses becomes less than a nominal 2.4 ms, the retriggerable single-shot which senses safe spindle speed will no longer time-out. With this single-shot constantly set, the Reset signal it applies to in the 7493 counter is removed, permitting the counting of speed pulses. If the sensed speed temporarily drops below the safe spindle speed, the Reset signal is once again applied to the counter. When the speed is above the sensed threshold for safe spindle speed, the counter is permitted to accumulate counts. When the counter gets to a count of 8, the brush cycle is initiated to clean the disk surfaces. When a count of 12 is reached in the counter, the Speed OK signal is asserted.

Provided the interlocks are still asserted and there are no unsafes, the positioner need only wait the completion of the brush cycle to load heads. This takes approximately 11 seconds to complete. When the brushes return to the brush-home position, the brushes flip-flop resets and all of the conditions are satisfied to reset the unload heads flip-flop, which in turn allows the load heads flip-flop (on the M7907 module) to set. (See Paragraph 5.3.2.1 on the head load sequence.)

5.2.2.2 Spindle Stopping - The spindle will stop whenever the RUN/STOP switch is released, the drive receives a command to unload the heads, a servo unsafe occurs, or if the ac power is interrupted. For the cases where the servo unsafe or the loss of ac power occurs, the spindle is deenergized immediately (even with the positioner not at the home position) and the positioner unloads by battery power to the motor. For all other cases, the spindle remains energized until the heads arrive at the home position. (See Paragraph 5.3.2.2 for the head unload sequence.)

With the heads home and the RUN/STOP switch released or the drive commanded to stop, the run flip-flop will reset, deenergizing the spindle via the relay driver and relay. These events enable the spindle brake. The spindle brake relay driver is enabled by the not run and not stopped conditions.

At this point, it should be noted that the spindle relay and spindle brake relay coils are interlocked with contacts of the other relay such that one is not permitted to operate while the other is energized.

Because the spindle is now deenergized, the interlocked coil circuits enable the brake relay coil to energize. As a result, the spindle brake circuit applies a full-wave-rectified dc voltage of approximately 11 V to the spindle motor. The motor now decelerates to a stop in approximately 20 to 25 seconds. When the retriggerable single-shot (which senses the stopped condition) times out, the STOP indicator on the operator's panel is lit, the brake voltage is removed via the relay driver deenergizing the relay, and the lid-locking solenoid is energized, thereby unlocking the lid mechanism provided that the RUN/STOP switch has been released.

5.2.2.3 Index/Sector Circuit Operation - The basic concept of operation of the index and sector generation circuits is the detection of the index pattern from the ync Pulse signal of the tribits, to use the resultant signal to initialize the counter for sector generation and the actual sector counter, and to count down the Servo Clock signals to derive the appropriate Sector Pulse signal. There are two different formats for the sector signal, namely 20 sectors per rotation or 22 sectors per rotation, as commanded by the controller.

These circuits use the Servo Clock ÷2 signal (from the difference amplifier and filter) to sense an index pattern from the Servo Pulse signal. The index pattern is actually the absence of three tribits in the following sequence (---11110101101111----) where the 0s represent the missing tribits. As a result, by clocking the Servo Pulse signal with the Servo Clock ÷2 signal (which continues despite the few missing tribits), the missing pulses are sensed.

The resultant clocked signal is shifted by the Servo Clock ÷2 signals into an 8-bit register. The outputs of six stages of the shift register are sensed by decoding gates, the output of which is asserted upon the detection of the index pattern. The Servo Clock signal clocks the decoded index pattern into the index flip-flop.

The decoded Index signal is used as an initializing signal to two counters, one of which counts Servo Clock signals to derive sector pulses and the other counts sector pulses.

To facilitate understanding of these counter operations, the arithmetic relative to the number of servo clock pulses per revolution and the number of counts necessary per sector is now explained.

$$\text{No. of tribits/rev} = 6720$$

$$\text{No. of } \frac{\text{servo clock}}{2} \text{ pulses/rev} = 6720$$

$$\text{No. of servo clock pulses/rev} = 13440$$

Since the sector pulse generation counter uses the Servo Clock signal to generate sector pulses, we arrive at the following numbers.

In 20-sector mode,

$$\frac{13{,}440 \text{ pulses/rev}}{20 \text{ sectors/rev}} = 672 \text{ pulses/sector}$$

The sector generation counter is implemented such that when a count of 1024 is achieved, a sector pulse is generated which in turn is used to preset the counter again on the following servo clock pulse. As a result, it can be seen that to accumulate a count of 672 pulses up to a count of 1025 (since the count of 1024 lasts for the entire clock period):

$1025 - 672 = 353$

which is the value that is preset into the counter except for the last sector.

For the case of the last sector, a value of 357 is preloaded into the counter instead of 353. This is done in order to generate the Index Window Open signal within which the next Index Detected signal must occur. If the Index signal is detected outside this pulse time (three servo clock periods) or if the Index signal is not detected, index error will occur which will cause Fault and Read/Write Unsafe signals (which cause the heads to unload).

In 22-sector mode,

$$\frac{13{,}440 \text{ pulses/rev}}{22 \text{ sectors/rev}} = 610.9 \text{ pulses/sector}$$

Since this is not a whole number, this format is treated differently; that is, 610 pulses/sector is used. Now,

$610 \times 22 = 13{,}420$

This leaves 20 pulses more per revolution. To account for all pulses, the last sector is 20 pulses longer.

For all sectors except the last, the following number must be preloaded to accumulate a count through 1024 (up to 1025):

$1025 - 610 = 415.$

This is the number preloaded.

For the last sector, 20 additional pulses must be counted so that it should be expected to load in a lower number, namely:

$415 - 20 = 395.$

However, as is the case of 20-sector mode, a count higher by 4 is preloaded in order to generate the Index Window Open signal.

As a result, a count of 399 is preset into the counter.

The remaining pulse of the Index/Sector signal to be generated is called the *index mark*. This pulse signals the controller that the next pulse that occurs is the beginning of sector 0. As a result, the index mark pulse occurs in the last sector. This pulse is a nominal 60 μs wide with its leading edge approximately 178 μs after the last sector pulse. It is generated by using 2^4 count in the sector pulse generating counter to generate a shift pulse of 1s through a shift register with an exclusive OR decode of two shift register stages.

Since the drive can have its format changed by command from the system without regard for the synchronism of the sector pulse count, the electronics on the M7705 immediately ceases generating sector pulses until the following sector 0 pulse, at which time it begins counting and generating pulses in the new format. This is done by the three flip-flops that generate 20-Sector Format, 20-Sector Format Del. and Actual 20-Sector Format, respectively. These flip-flops form a 3-bit shift register that controls the inhibiting of sector pulses and the resynchronizing to the new format.

5.2.2.4 Receipt of Command Messages – The control of commands (received messages) and status (transmitted messages) is accomplished by logic circuitry on the M7706 module. This control is based on the CTD, Strobe, and Control Clock signals on the interface. These signals define the timing and direction of the messages. In addition, two bits on Message Line B determine which of four sets of messages are transmitted following the received message. See Tables 3-1 through 3-10 for definitions and properties of these signals.

Figure 3-2 illustrates the timing relationships between these interface control signals and the contents on Message Line A and Message Line B for messages in both directions.

Before messages can be received or transmitted, the Interface Enable signal must be asserted. This signal is the logical AND of the Interface Controller Power signal and the front panel A or B switch (Chapter 3). With the Interface Enable and CTD signals asserted, the receipt of a strobe pulse initiates the receipt of messages on the message A and message B lines simultaneously. The strobe pulse sets the drive select flip-flop and the input enable flip-flop. Input Enable being asserted enables the message A and message B line receivers and the assertion of Drive Select enables the receipt of clock pulses.

Each negative edge of the control clock loads Message Line A and Message Line B data into the BUFF 1 and STATADD flip-flops, respectively. Clocking of the data on the clock's negative edge deskews the data from propagation delay variations on the controller-drive cable and the interfacing circuits. Figure 5-8 is an expanded diagram showing these timing relationships. For all clock pulses except the first, the clock counter on the M7706 module is advanced on the clock's negative-going edge. However, during the strobe pulse time, the strobe holds the counter reset. Upon the next clock rising edge, the clock time decoder is enabled and the short clock pulse (CP) generates a 100 ns pulse on the T0 output. Figure 3-2 shows this pulse's timing in relation to the other control and data signals. These same relationships then apply for the remainder of the message transmission.

At the trailing edge of T15, the input enable flip-flop is reset, thereby terminating the receipt of the message, resetting the clock counter to 0, and inhibiting the timing decoder.

During the receipt of command messages, parity detection circuits on the M7706 module sense the state of each bit that is received. For each logic 1 that is received on both lines, the corresponding parity flip-flop toggles to its opposite state. At the trailing edge of the T15 pulse time, the composite parity flip-flop (Par Err) is clocked and set if an even number of logic 1s were sensed on either line. In this manner, a parity error is sensed.

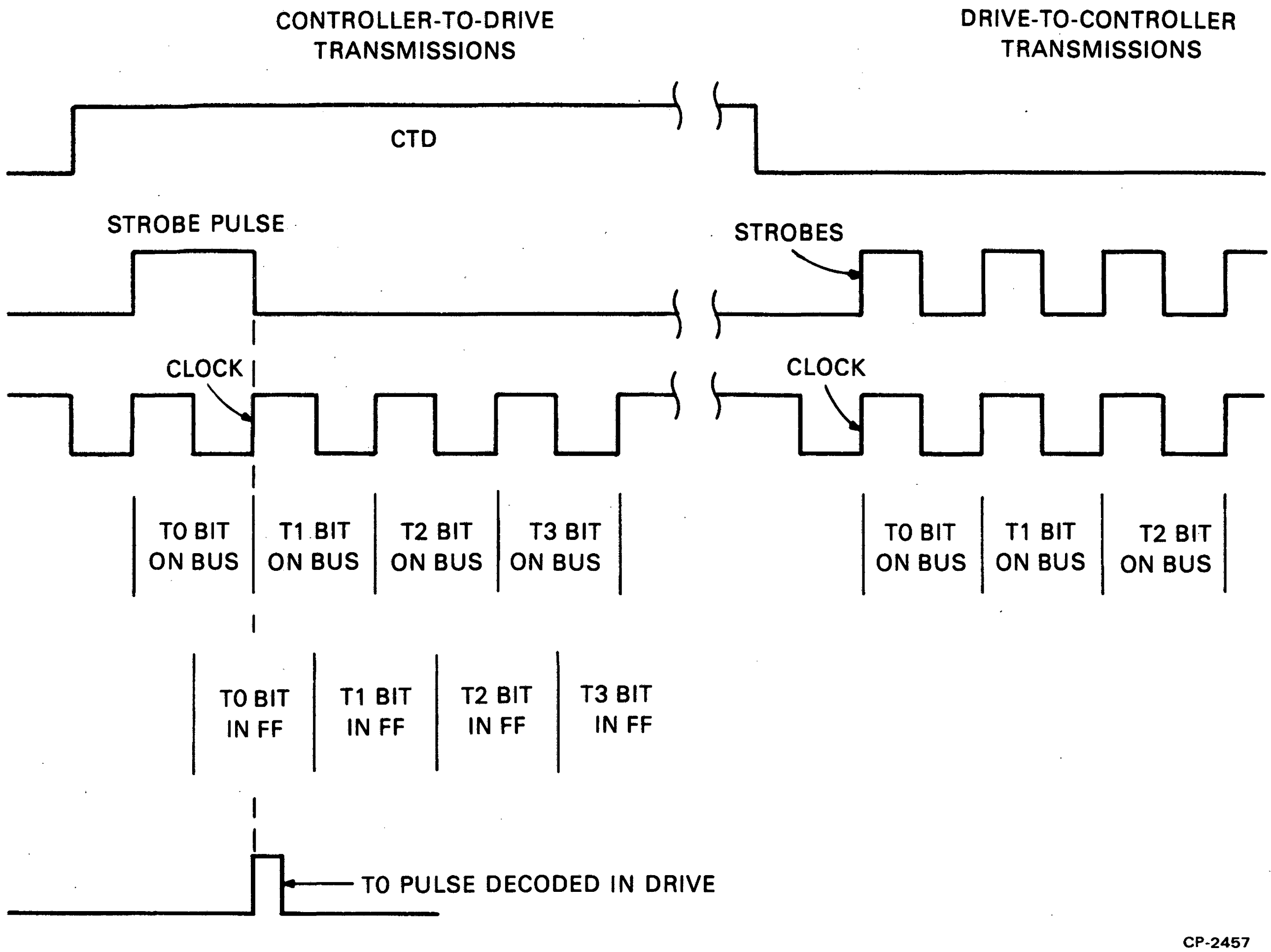


Figure 5-8 Timing Relationships for Controller/Drive Transmissions

5.2.2.5 Transmission of Status Messages - The output enable flip-flop is set when the CTD signal is negated, the Input Enable signal is reset, and the next clock negative transition occurs. The Output Enable signal enables the strobe and the message A and message B transmitters. The drive now commences to transmit a status message to the controller.

Starting at the next clock pulse time, the drive transmits the Clock signal which it receives onto the strobe interface line. During the same period, the message A and message B lines transmit 16 bits each as status messages. See Figure 3-2 for an illustration of timing during transmissions from the drive.

The messages transmitted on the message lines are those that were requested on the prior message from the controller to the drive. The pair of messages that are transmitted are indicated in Figure 3-2. The message request bits received by the drive are the first two bits on the message B line in binary-encoded form with the least significant bit first. These bits are stored in the byte 0 and byte 1 flip-flops on the M7706. The flip-flop outputs are decoded and applied to the appropriate multiplexers which convert parallel status data to serial form for transmission. The multiplexers are located on the M7705, M7706, and M7907 modules. The outputs of the multiplexers are logically ORed on the M7706, clocked into the "Tr Mess A" and "Tr Mess B" flip-flops to synchronize the status bits to the clock pulses and then transmitted onto the interface.

As each bit is transmitted, two parity flip-flops ("Mess A Par" and "Mess B Par") sense each bit that is transmitted. For each logic 1 that is transmitted, on both lines, the corresponding parity flip-flop toggles to its opposite state, then is applied as the last bit in the multiplexer for transmission. In this way, an odd number of logical 1s are transmitted in each message.

5.3 POSITIONING SUBSYSTEM

The positioning subsystem (Figure 5-9) comprises the electrical and mechanical elements that cause physical positioning of the servo and data heads. Electrical circuits of the positioning subsystem are contained on the M7906 servo analog module, the M7907 servo control module, and the M7908 track-positioning detector/phase-locked oscillator (TPD/PLO) module, as well as the phototransducer preamplifier and servo preamplifier. Mechanical elements include the linear motor, carriage, servo head, phototransducer, and load/unload tachometer. Paragraph 5.3.1 gives functional desriptions of these circuits and mechanical elements in detail. Paragraph 5.3.2 gives operational details of the positioning functions.

5.3.1 Functional Sections

5.3.1.1 Cylinder Address Register – The cylinder address register located on the M7907 receives and stores desired cylinder address information from the controller via the interface and timing module. After the completion of a seek, this register will contain the current cylinder address. Cylinder address data comprises ten bits that are loaded into the register in serial form upon the receipt of a seek command transmission. It is reset by head loading, unloading, or return-to-zero (RTZ) functions.

5.3.1.2 Serial Adder – The serial adder is comprised of two exclusive OR gates located on the M7907 module. It provides a cylinder difference obtained by 1's complement arithmetic sum of a new cylinder address (being received by the drive) with the existing cylinder address (stored in the cylinder address register).

5.3.1.3 Cylinder Difference and Offset Register – This register of ten bits performs two functions. First, it stores the resultant cylinder differences as provided by the 1's complement serial adder. Second, it stores information received from the controller when there is no seek command to determine if an offset is being commanded. In both cases, the data are loaded serially but the outputs are taken in parallel. It is reset by the head loading, unloading, or RTZ function.

5.3.1.4 Carry Circuit – This circuitry on the M7907 consists of gating that determines if there is a carry on a bit-by-bit basis for the serial differencing and a flip-flop for storing the carry bits. At the end of the differencing operation, the state of the flip-flop indicates if the difference was positive or negative, and therefore, controls subsequent operations to result in an absolute difference value. The carry flip-flop, therefore, also controls the direction of motion of a seek.

5.3.1.5 Absolute Difference Counter – The difference counter located on the M7907 module is a 10-bit up/down counter that stores the magnitude of cylinder difference and offset values for cylinder offsetting. It must up-count by one when cylinder differencing produces a carry and it down-counts by one for each cylinder crossing during a seek (Paragraph 5.3.2.4). It is reset by the head loading, unloading, or RTZ function.

5.3.1.6 Offset and RTC Circuits – These combinational logic circuits on the M7707 module are used for decoding and controlling offset and return-to-centerline (RTC) commands. Offsetting provides for accurately relocating the heads up to ±600 microinches from the cylinder centerline in 12.5 microinch increments. The return-to-centerline command cancels an offset and returns the heads back to the center of the cylinder.

5.3.1.7 Load Heads and RTZ Circuits – These circuits on the M7907 module consist of logic for controlling the loading of heads from the home position and for controlling the return-to-zero function.

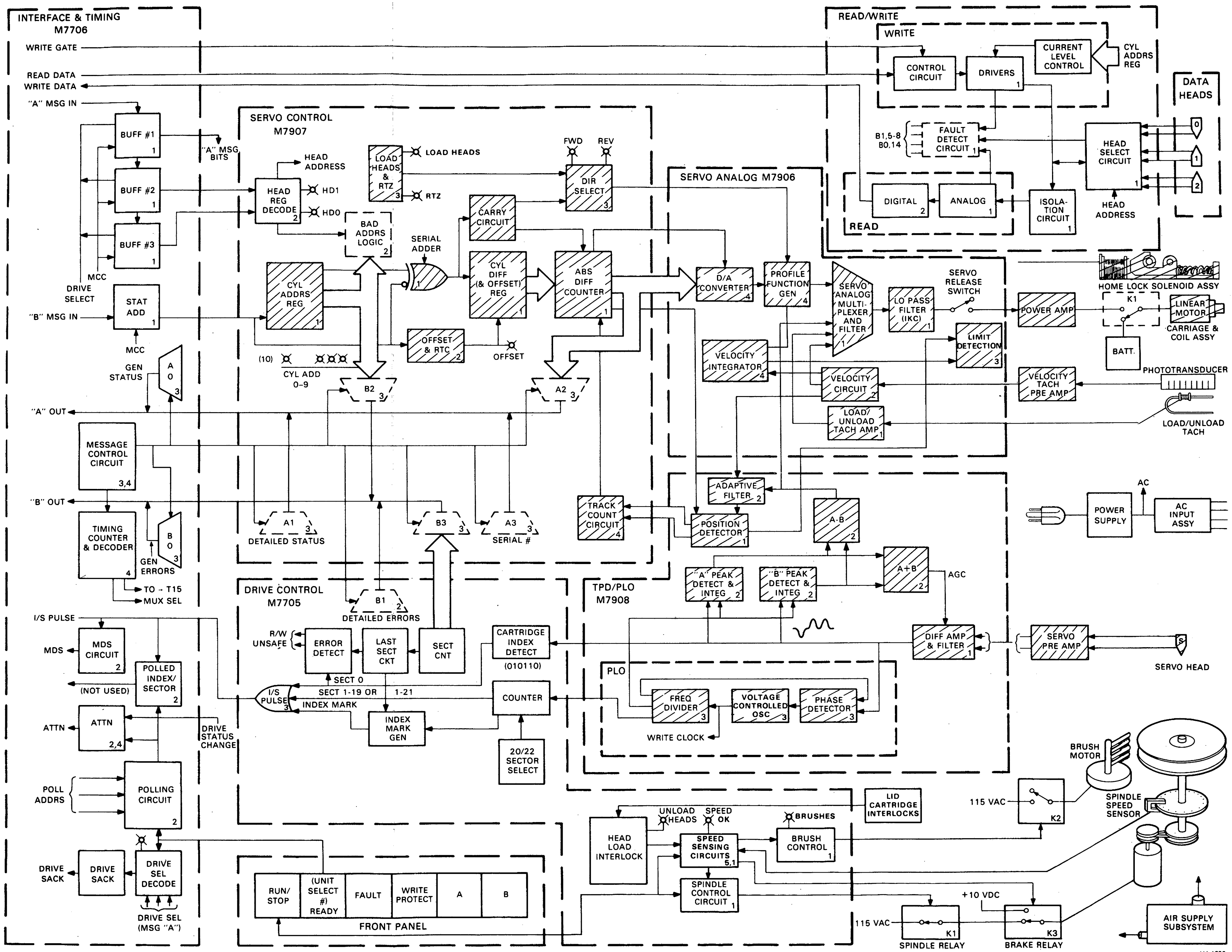


Figure 5-9 RK07 Disk Drive Functional Block Diagram with Positioning Subsystem Shaded

5.3.1.8 Direction Select Circuits – These circuits on the M7907 module consist primarily of the forward flip-flop and the reverse flip-flop and associated gating that controls these elements. These flip-flops control the direction of carriage motion during seek operations.

5.3.1.9 Track Count Circuits –This circuitry on the M7907 module provides count pulses to the difference counter at the appropriate time and location for each cylinder crossing that occurs during a seek.

Track Error is a signal that represents the distance between the heads and the center of a track. As the heads cross successive tracks, Track Error will assume a near-sinusoidal waveform, with zero Track Error occurring where the heads are on a data track centerline, or exactly between odd and even servo tracks. See Figure 5-10. This figure also illustrates Coarse Track and Fine Track and their relation to Track Error. Coarse Track is asserted whenever the heads are within ±1/4 track of the track centerline, whereas Fine Track is not asserted until the heads are within ±1/2 of a track of the centerline. (The position detection circuitry that generates these three signals is described in Paragraph 5.3.1.22.)

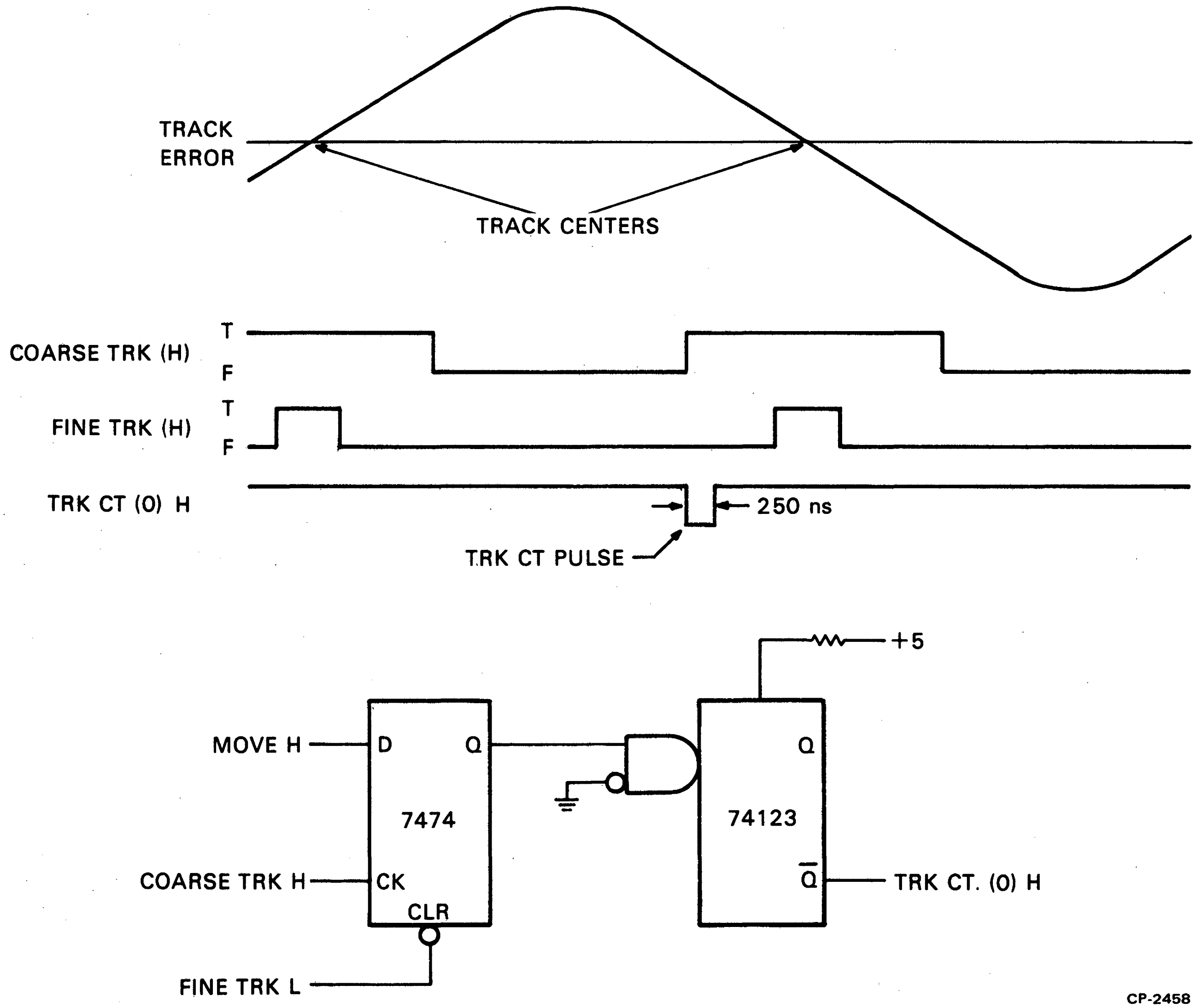


Figure 5-10 Track Counting

The Coarse Track signal, which detects track crossings during a seek, is used for track counting. The track difference counter is decremented whenever Coarse Track goes true. The circuitry pictured in Figure 5-10 prevents the track difference counter from being decremented accidentally.

The signal MOVE H is high during a seek. Normally, the positive-going edge of Coarse Track will set the flip-flop and trigger the one-shot, which will decrement the absolute difference counter. The Fine Track pulse must come and go before another edge of Coarse Track will be recognized. After Fine Track has gone away, the flip-flop will accept another Coarse Track positive-going edge. If this is an invalid edge, it will set the flip-flop and decrement the counter. However, the next valid edge after this invalid edge will *not* be accepted because the flip-flop will already be set, since there was no Fine Track pulse to correspond with the invalid edge.

5.3.1.10 High Hysteresis – Figure 5-11 depicts the Track Error signal, and the corresponding Coarse Track threshold that the signal must cross to ultimately decrement the absolute difference counter via the track count circuitry. Suppose the heads are at a maximum offset position, which puts the Track Error voltage at the threshold point labeled "A" in Figure 5-11. If the heads begin a seek from offset by moving away from the center of the track they started from (to the right in the illustration), the first track crossing might not be counted, because the threshold would not be counted for the first track. The RK07 incorporates high hysteresis to raise the threshold (for the first track crossing) so that the first crossing is counted. The high hysteresis circuitry also raises the threshold whenever the heads are one track away from detent, either going in or coming out.

Circuitry on the M7907 servo control module determines whether the heads are within one track of the beginning or the end of a seek. If so, the asserted signal HIGH HYS L goes to the M7908 TPD/PLO module. This signal turns off a FET switch which, because of biasing on the circuitry, raises the Coarse Track dropout threshold.

5.3.1.11 Dual Velocity Profile Function Generator – The velocity command circuitry on the M7906 module converts the digital value of cylinder difference (the difference between the present head location and the desired location) to an analog voltage. This analog voltage is the velocity command voltage presented to the servo system for seek operations or offsets.

The purpose of the profile function generator is to produce different velocity or deceleration profiles for both long and short seeks. One is for seeks less than 64 tracks, and the other is for seeks greater than or equal to 64 tracks. The choice depends on the SHORT SEEK L signal from the M7907 module (Paragraph 5.3.2.4). If SHORT SEEK L is low, indicating that the short seek flip-flop on the M7907 is set, then the seek is less than 64 tracks and the analog velocity command will be smaller than it would be for a longer seek. Figure 5-12 illustrates the schematic for the function generator (a) and the dual velocity profile (b).

For offsets, analog switches open the nonlinear feedback elements and switch the function generator to a linear command corresponding to the offset code.

The input to the D/A converter is the lower 7-order bits from the difference counter. These seven bits provide the difference count up to a maximum of 127. For cylinder differences less than 127, the head positioner velocity command is proportional to (approximately) the square root of the cylinder difference, up to a maximum velocity of 121.9 cm/s (48 in/s) at a cylinder difference of 127 or greater. For all cylinder differences greater than 127, the velocity command is constant at 121.9 cm/s (48 in/s). Gating on the M7907 decodes all differences greater than 127 to provide a logical one on all input lines to the D/A converter. For seek lengths less than 64 cylinders, the velocity profile is somewhat less than the profile for greater seeks, as shown in Figure 5-12b.

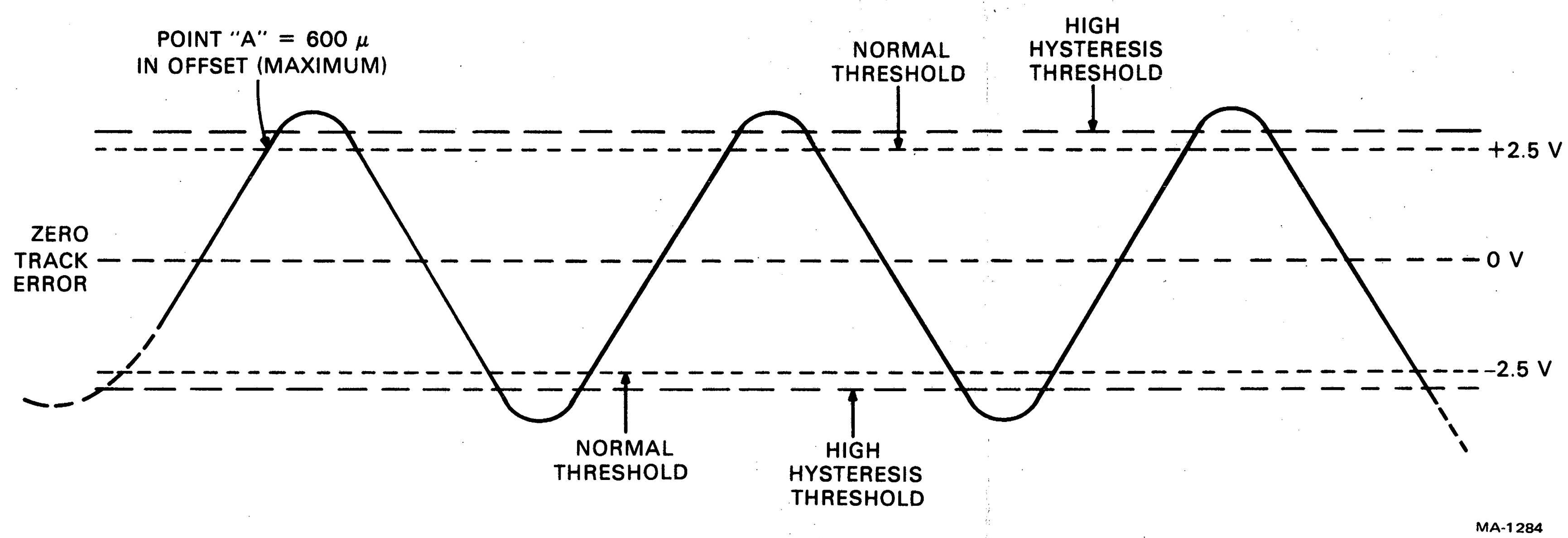
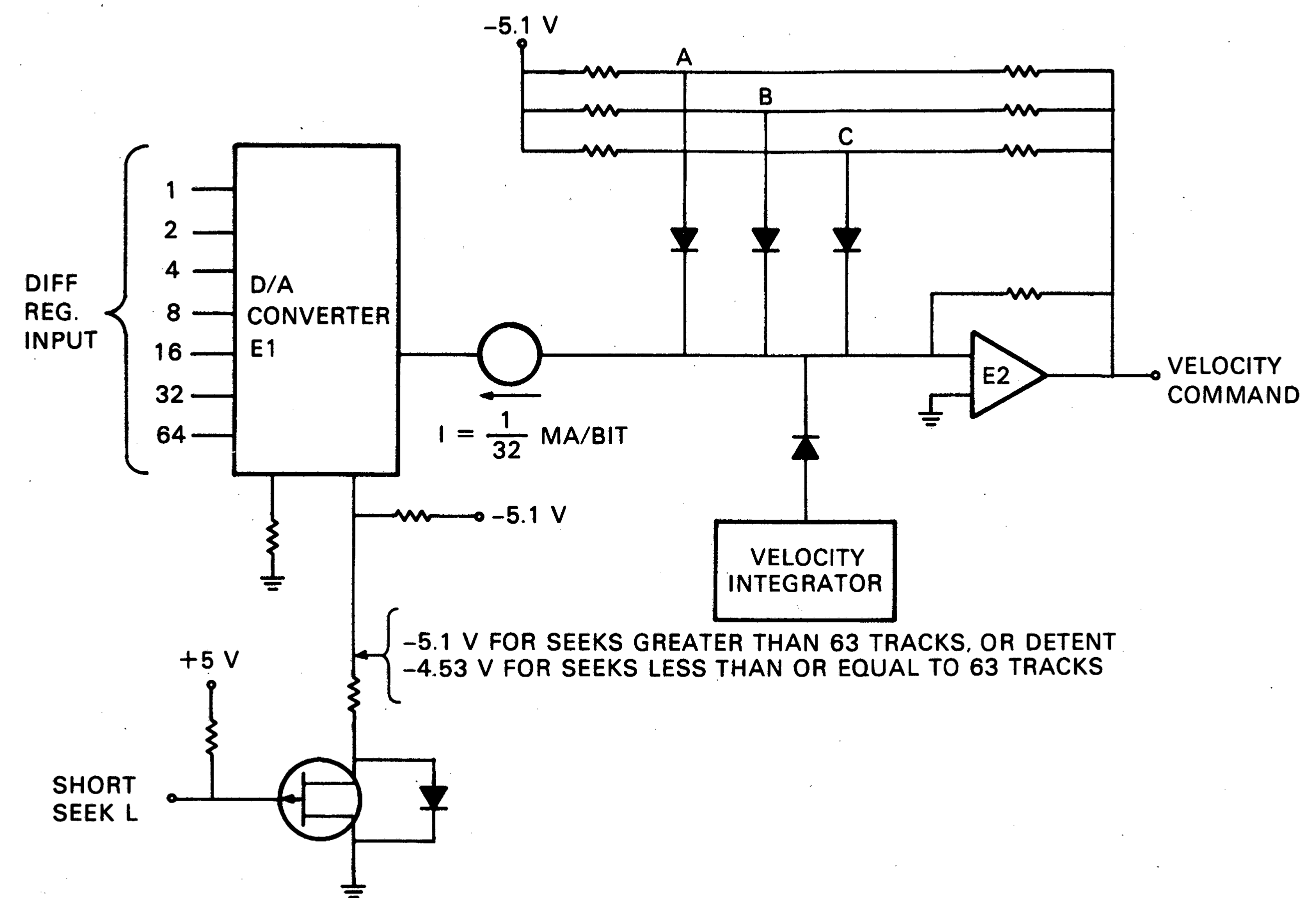
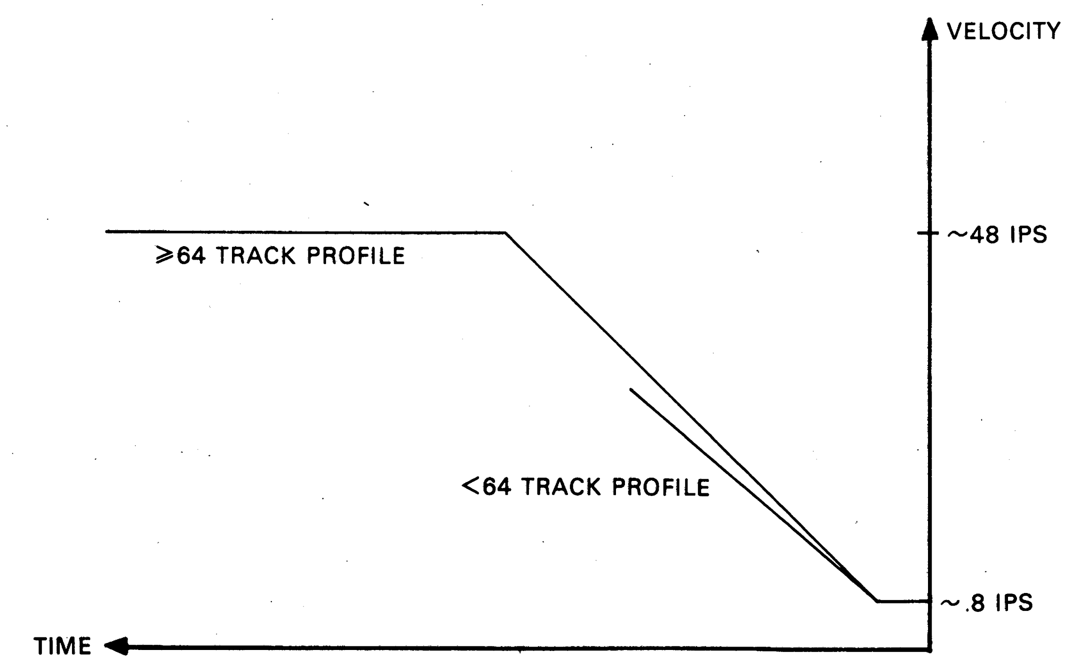


Figure 5-11 Track Error Signal and Track Count Threshold



a. Schematic



b. Dual-Velocity Profile

MA-1285

Figure 5-12 Dual-Velocity Profile Function Generator

The circuit implementation of the profile generation is shown in Figure 5-12. The track difference count is converted to analog and used as an input to E2. The larger the difference count, the more positive the velocity command becomes. This biases more diodes into the ON state and effectively puts more resistors in parallel with R. This reduces the closed loop gain of E2 which produces the desired function.

When SHORT SEEK L is low, indicating a seek of less than 64 tracks, the D/A converter (E1 in Figure 5-12) is biased at a lower voltage than it would be for seeks of 64 cylinders or more. The lower bias voltage (–4.53 V compared with –5.1 V) results in a smaller input to the operational amplifier, E2, and consequently, a lower velocity command.

5.3.1.12 Velocity Integrator – The velocity integrator serves two purposes in the RK07 drive. First, it is used in conjunction with the velocity command circuitry described in Paragraph 5.3.1.11. The velocity integrator is also used in the platter limit detection process (Paragraph 5.3.1.13).

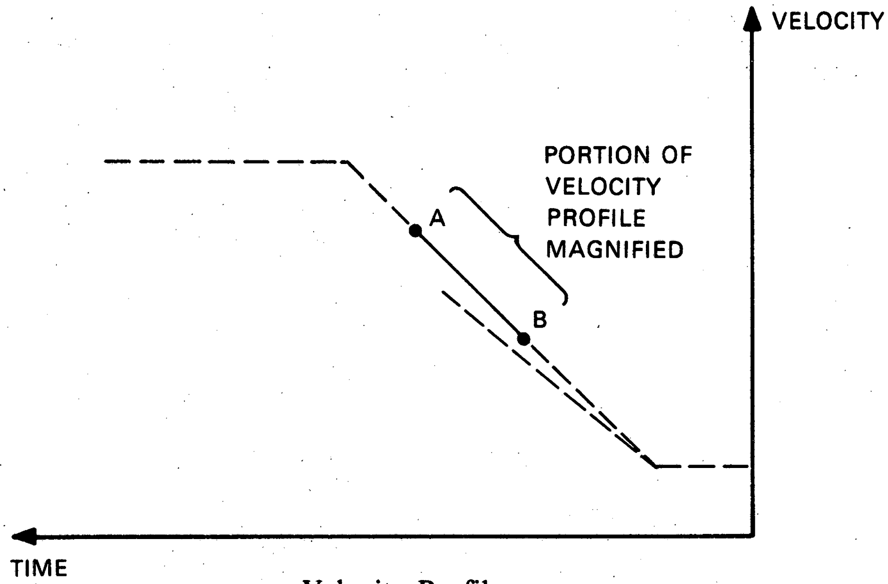
The velocity command circuitry develops a velocity command signal. The velocity integrator, as one of its two roles, smooths this signal by subtracting out the steps produced by the velocity command D/A converter. Because the velocity integrator is reset at every track crossing, the output of the integrator represents the distance that the carriage has moved since the last track count update. Since this signal is proportional to distance, it can be added directly to the D/A output to smooth the signal. This circuit is referred to as a "fill-in-the-steps" or "velocity smoother" circuit. This increased resolution is only needed on the last track before detent, but is in the circuit for the entire seek process.

Figure 5-13 shows a magnified portion of the velocity profile to indicate the actual command from the D/A converter, as well as the smoothed signal that is supplied to the operational amplifier that produces the velocity command.

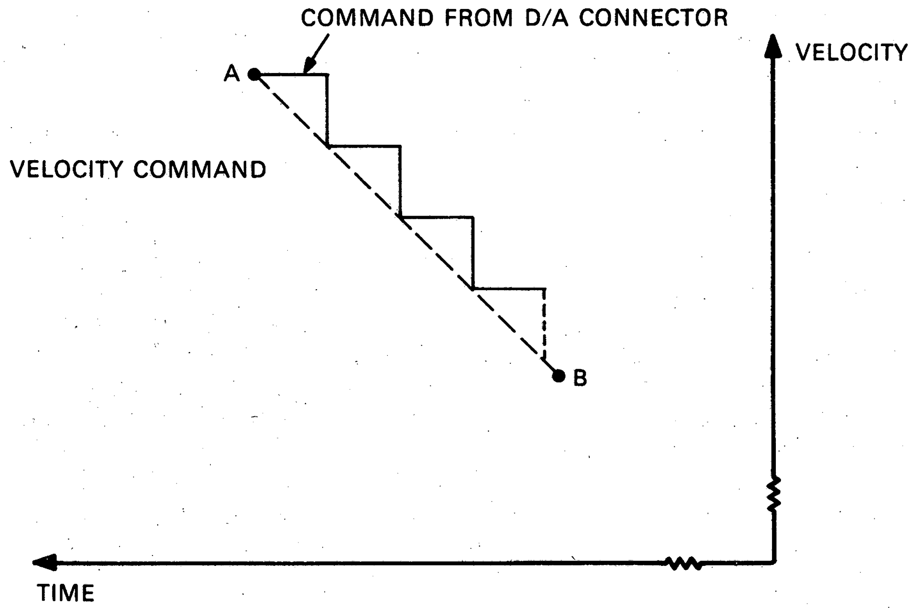
Figure 5-14 pictures a schematic of the velocity integrator circuitry. This figure also illustrates how the output of the operational amplifier E2, which is integrated velocity, affects the output from the D/A converter. Integrated velocity is simply added to the output of the converter, and the resulting smoothed signal goes to operational amplifier E1 and becomes the velocity command. Note that the integrated velocity signal and the corresponding sawtooth wave may be either polarity, depending on the direction of head motion.

The other purpose of the velocity integrator, besides its role in smoothing the velocity command signal, is as an element in platter limit detection. This second role also depends on the fact that the velocity integrator is reset every time a track crossing occurs. This continual resetting process causes the zero-to-peak amplitude of the integrated signal to be fairly constant, even over a wide variation in velocity. This is illustrated in Figure 5-15. The signal will never exceed a given peak-to-zero amplitude as long as the heads are between the guard zones where track crossings (and, therefore, the velocity integrator resettings) occur at regular intervals. However, when the heads move into a guard zone, there are no track crossings, and no resetting of the integrator, and the signal ramps up to a voltage that is beyond the specified maximum (Figure 5-16). The platter limit detection circuitry, described in Paragraph 5.3.1.13, detects the fact that the integrated velocity signal has gone beyond the specified maximum.

5.3.1.13 Platter Limit Detection – The RK07 does not use the glass scale to determine the inner and outer limits of the platter, as is the case in the RK06. Rather, the limits are derived from the platter itself in that the electronics on the servo analog module M7906 in the RK07 determine whether or not the heads are in one of the guard zones, and, if so, which one. The integrated velocity signal, which is also used in the generation of the velocity command (as described in Paragraph 5.3.1.12), is used here, for platter limit detection.



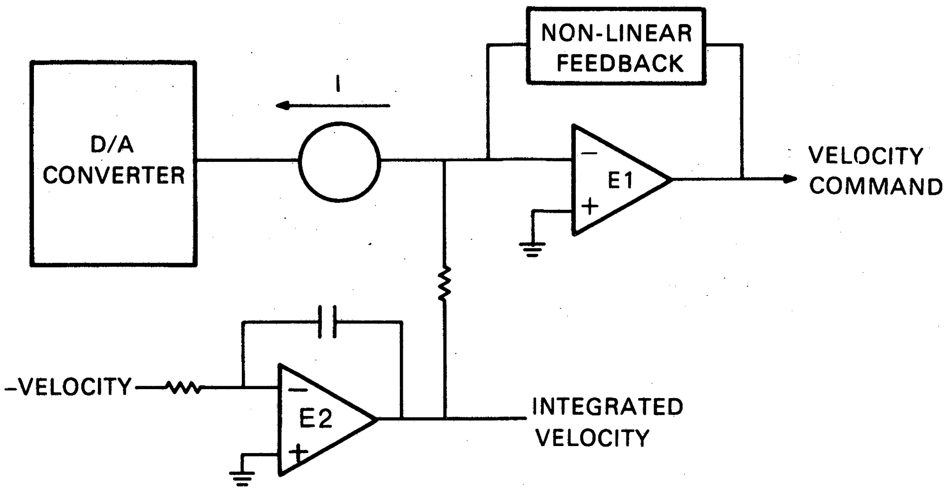
a. Velocity Profile



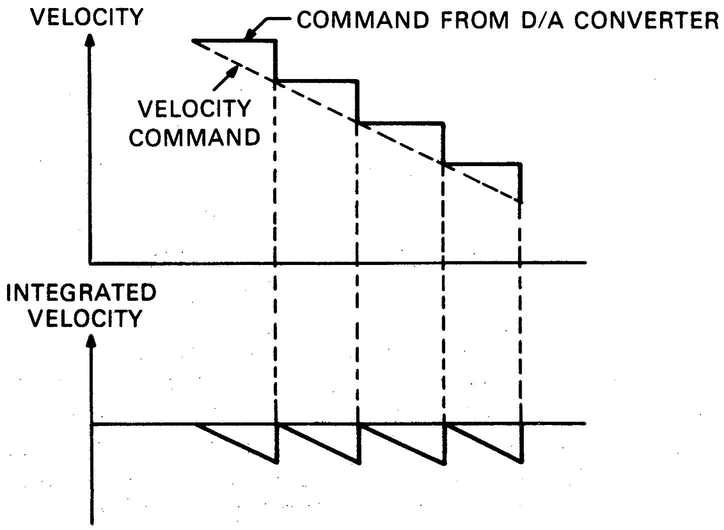
b. Magnified Profile

MA-1280

Figure 5-13 Velocity Profile Smoothing



a. Schematic



b. Smoothing of Command

MA-1286

Figure 5-14 Velocity Integration

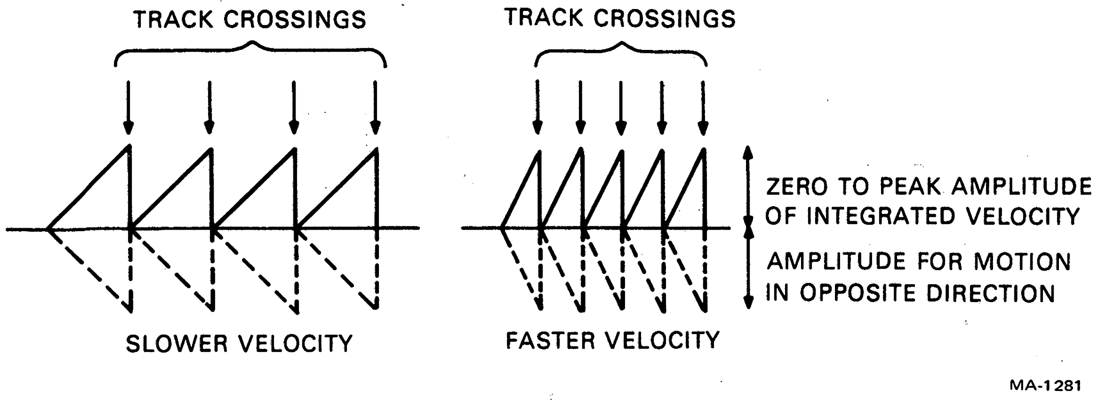


Figure 5-15 Integrated Velocity Signal

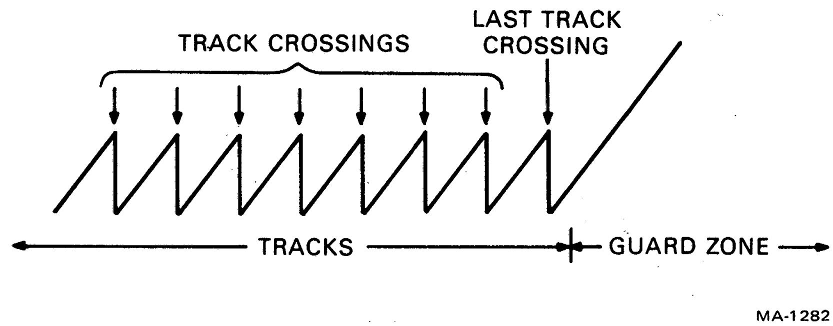


Figure 5-16 Integrated Velocity Signal Entering Guard Zone

As described in Paragraph 5.3.1.12, the integrated velocity signal will remain fairly constant as long as the heads are between the inner and outer platter limits. However, if the heads pass into one of the guard zones, the signal will rise above a level of 5V or fall below a level of –5V. At this point, the comparator circuit shown in Figure 5-17 will generate the LIMIT H signal, indicating that the heads have crossed through one of the limits. The polarity of the Track Error signal indicates which guard zone the heads are in, so that either the inner or outer limit flip-flop can be set.

The velocity integrator is held at reset until the heads are between limits. Because of this, the drive looks at the Track Error signal to set the outer limit flip-flop when loading the heads. The Track Error signal is about equal to zero before and after the heads first land on the disk, but drops to its most negative value as it enters the outer guard zone. Thus, the outer limit flip-flop is set on the leading edge of the detection that the track error has passed a given negative threshold.

The POS TE L and NEG TE L signals, used in the platter limit detection circuitry for the generation of the Inner Limit and Outer Limit signals, respectively, are generated from the Coarse Track comparator ciruitry on the M7908 TPD/PLO module.

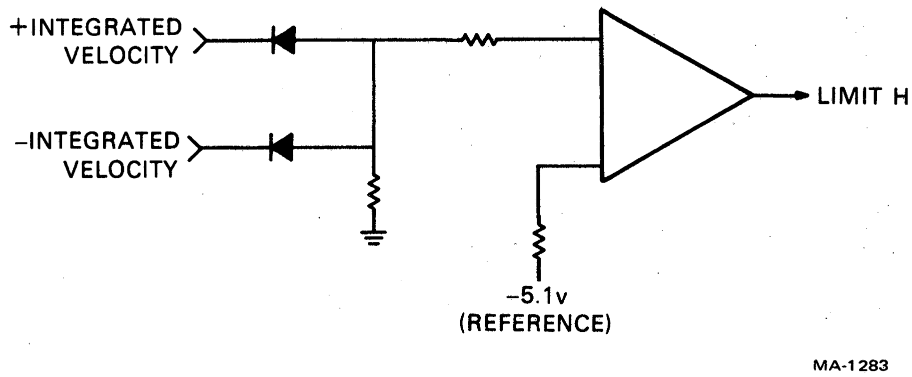


Figure 5-17 Detection of Guard Zone

5.3.1.14 Servo Analog Multiplexers and Low-Pass Filter – The analog multiplexer circuitry comprises a group of switched field-effect transistors (FETs) that provide selective control of the three major servo functions performed by the linear positioner, viz., seek, detent, and offset. The inputs to the source select circuits are shown in Figure 5-18.

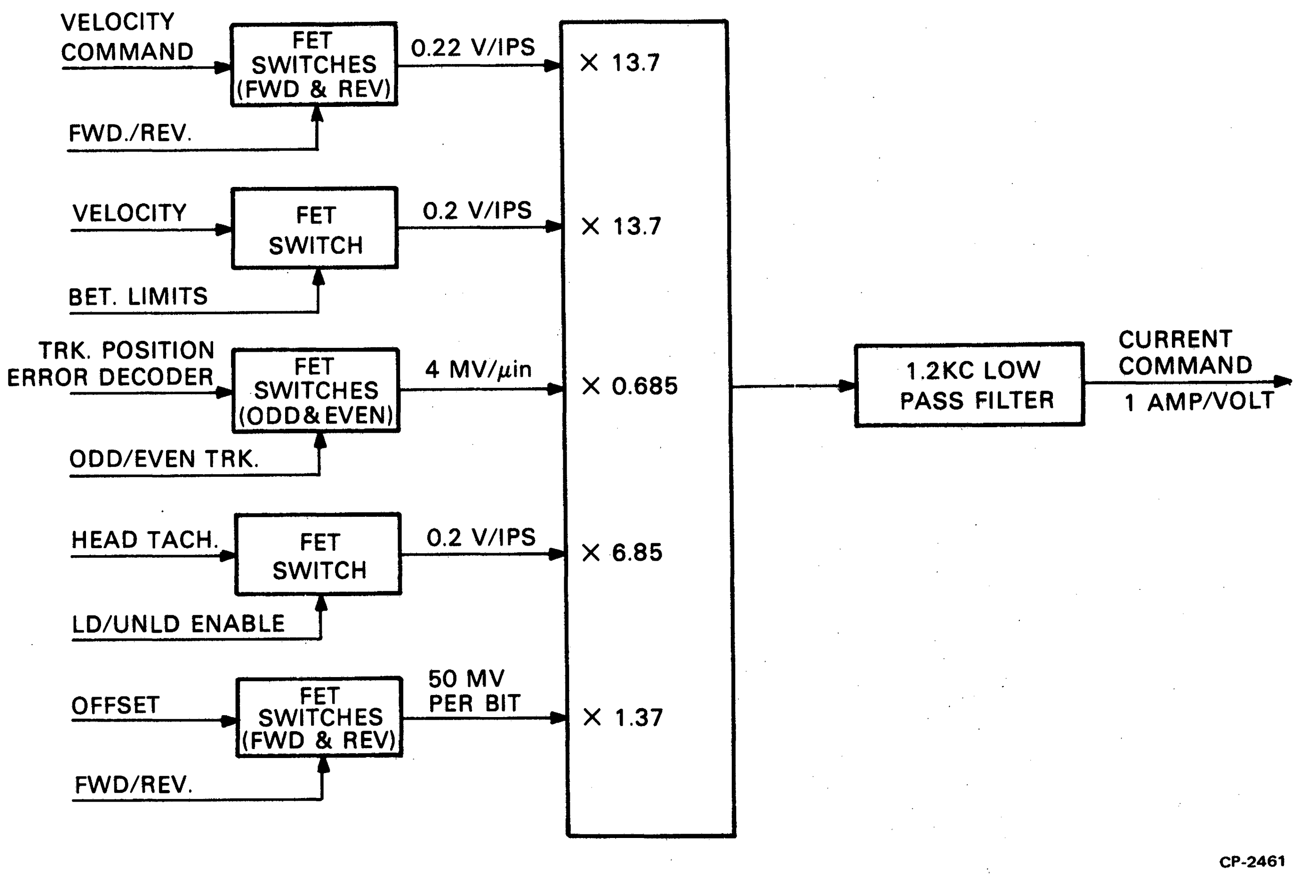


Figure 5-18 Summing Amplifier of Servo Analog Multiplexer and Filter

The summing amplifier provides a summation of switched inputs and provides the gains required to develop the required command for the linear motor. The low-pass filter at the output of the source selector inhibits oscillations within the drive.

5.3.1.15 Load/Unload Tachometer Amplifier – This circuitry on the M7906 amplifies the difference between the two coils of the heads load/unload tachometer.

5.3.1.16 Heads Load/Unload Tachometer – The heads load/unload tachometer (Figure 5-19) is a linear magnetic transducer whose output is proportional to carriage velocity. The purpose of this device is to provide velocity feedback to the head positioning servo during the loading and unloading of the heads in the region from heads home to the outer limit.

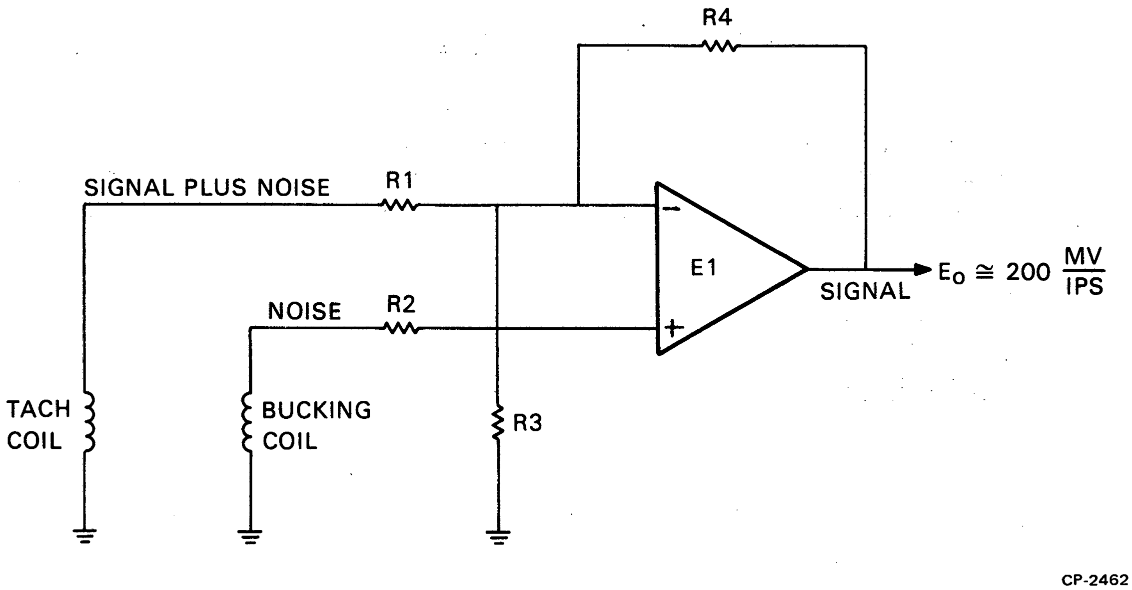


Figure 5-19 Heads Load/Unload Tachometer Schematic

The tachometer operates by the coil cutting magnetic lines of force of a permanent magnet, inducing an output voltage proportional to the number of lines cut per unit time, i.e., to velocity.

Physically, the tachometer consists of a permanent magnet and two coils, only one of which is involved in the velocity determination. The second coil, like the first, is exposed to any external fields whose effect would be to introduce error in the velocity feedback loop. The output of this second (bucking) coil is of opposite polarity to the first. The difference of the signals of the two coils is taken to cancel, to a large extent, the effects of any field other than that of the tachometer magnet.

5.3.1.17 Velocity Circuitry – The velocity circuitry on the servo analog (M7906) module comprises:

1. The automatic gain control (AGC) circuitry for the light-emitting diode (LED) of the phototransducer

2. Amplifiers, differentiators, multiplexing of differentiated signals for deriving carriage velocity.

Automatic Gain Control – The power dissipated in the motor on repetitive seeks is inversely proportional to the fourth power of the access time. A 10 percent change in the access time will produce a 46 percent change in the power. Therefore, it is important to have accurate velocity information.

The photo devices will change their sensitivity with temperature and time. An automatic gain control circuit is provided to keep this from changing the scale factor of the tachometer. It monitors the amplitude of the predifferentiated signals and adjusts the current through the LED to keep the amplitude of the signals constant.

The current for the LED is generated with a D/A converter. A counter provides the input for the D/A converter. Counting up causes the sine and cosine to become larger and counting down causes them to become smaller.

The counter counts one way or the other when both the sine and cosine are equal to each other at the 3/4 light point as shown in Figure 5-20.

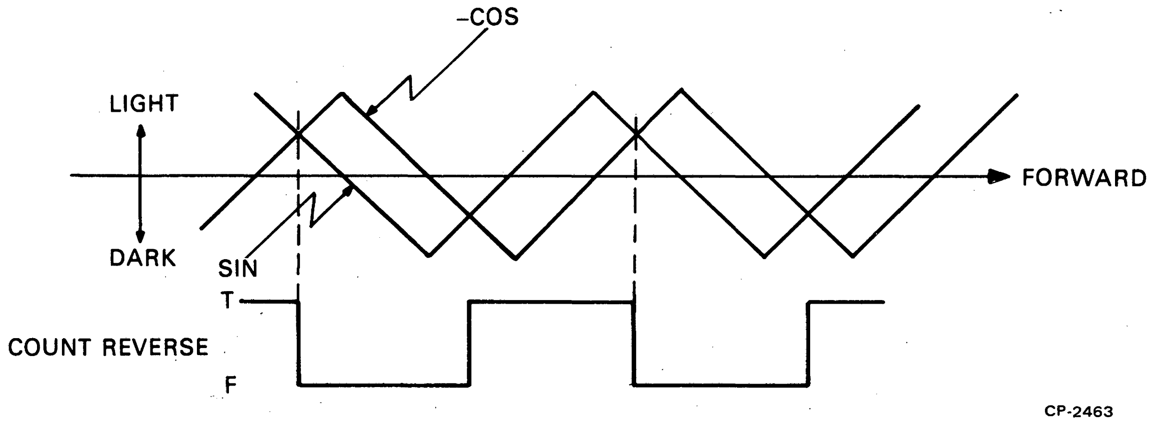


Figure 5-20 LED AGC Counter Waveforms

False-going edges of the logic signal Count Reverse cause the counter to count when the carriage is moving forward. True-going edges cause the counting in the reverse direction. This logic signal is true when the sine is more positive than the inverted cosine.

At the appropriate edge of Count Reverse, the circuitry determines whether the sum of the sine and –cosine is larger or smaller than 10.2 V. This information is stored in a flip-flop. The pulse that counts the counter is delayed from the edge of count reverse by a one-shot until the direction information is stable and then it is steered to the correct input of the counter by the magnitude information in the flip-flop.

The AGC circuitry is disabled at the end of the seek. The one TRK flip-flop does not allow it to be operated again until the carriage has moved 1/4 track on the next seek. This prevents the forward and reverse logic signals from causing a false count at the start of the seek.

The AGC adjusts the amplitude of the sine and cosine based on the average of the two. Thus, if one becomes slightly larger for some reason, the circuitry makes them both smaller so that the average is correct. The servo does not have time to respond to the individual waveform segments at high velocities and so the average of the sine and cosine is the crucial parameter.

Phototransducer Circuits – The transducer produces two waveforms (Figure 5-21) that are triangular as a function of distance. They are 90 degrees apart. These waveforms are differentiated to produce square waves that have an amplitude proportional to the frequency of the triangles which is proportional to the velocity. These are multiplexed together to produce the Velocity signal. The multiplexing is controlled by the undifferentiated signals so that it is valid even at zero velocity.

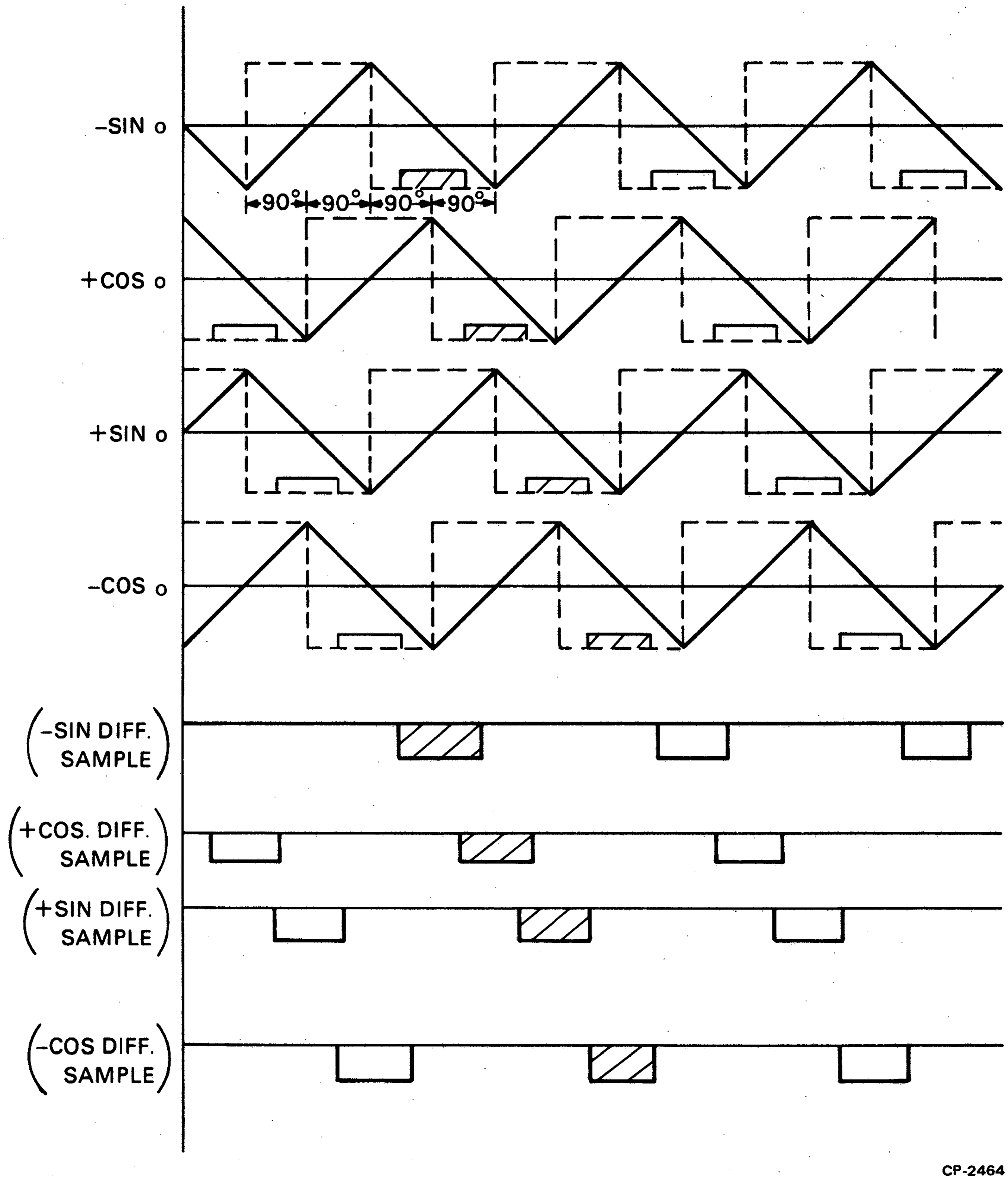


Figure 5-21 Velocity Multiplexing Timing Diagram

Both polarities of both signals are formed before the differentiation to minimize offsets at the expense of some additional circuitry.

The Input signals to the M7906 module are negative-going triangles of 0.5 V peak-to-peak. The input stage level shifts them so that they are symmetric around zero. It also amplifies them so that the extrapolated waveforms are 20 V peak-to-peak. The actual waveforms will only be about 17 V peak-to-peak because the triangles are slightly rounded at the peaks.

5.3.1.18 Difference Amplifier and Filter – This circuitry on the M7908 module accepts the differential tribit Input signal from the servo preamplifier (Paragraph 5.3.1.27) and provides further amplification and low-pass filtering for the purpose of deriving other signals from the tribits. The output gain of the circuits is controlled by an automatic gain control (AGC) which is derived from the sum of the peaks of the A and B pulses of the Tribit signal. The Input signal to the difference amplifier and module is the tribit waveform shown in Figure 5-22. The relative amplitudes of the A and B pulses shown in the figure contain the position information, while the sync pulse is used for the timing reference. As is seen in the figure, the A pulse is maximum and the B pulse is minimum whenever the servo head is positioned –1/2 track from the nominal *even* data track (i.e., +1/2 track from nominal odd track) centerline. B is maximum and A is minimum when the servo head is positioned +1/2 track from the nominal *even* data track (i.e., –1/2 track from the nominal odd track) centerline. The sync pulse amplitude remains nearly constant at all times.

5.3.1.19 Phase-Locked Oscillator – The circuitry for the RK07 drive phase-locked oscillator (PLO) is located on the M7908 module. The PLO, consisting of four main parts, is shown in the block diagram in Figure 5-23. It has two main functions in the drive: (1) to generate a Write Clock signal that is synchronized with the rotational velocity of the servo platter, and (2) to generate signals that indicate the presence of A and B peaks, for use in track position detection.

The 3-state phase detector takes two frequencies, one from the servo platter (SVO PULSE H) and the other from the loop itself (SVO CLK/2) and forces them to synchronize. The resulting digital signal is converted to an analog signal and is filtered by the low pass filter. After filtering the signal enters the voltage-controlled oscillator (VCO) which produces a frequency that is the drive Write Clock signal. This same signal is input to the frequency divider, which divides the frequency of the signal by 32. There are three main outputs from the frequency divider. Two are the A PK DET H and B PK DET L signals, used as the input to the track position detection circuitry for detection of A and B peaks (Paragraph 5.3.1.20). The third output from the divider is the signal SVO CLK/2, used as a feedback signal to the phase detector. The four main blocks of the PLO are described in detail below.

3-State Phase Detector – The phase detector controls the frequency of the PLO. It does this by generating one of three commands: "speed up," "slow down," or "coast." Speed up causes the VCO frequency to increase; slow down will decrease the frequency; and coast will not change the PLO frequency, i.e., the loop will "coast" at a constant frequency.

Initially, the PLO will not be locked into a constant frequency. When this is the case, circuitry on the M7908 module generates a signal called PLO ERR L. This signal triggers a 0.73 ms one-shot, which makes the logic of the phase detector function as shown in Figure 5-24. In this case, the phase detector is acting as a frequency detector.

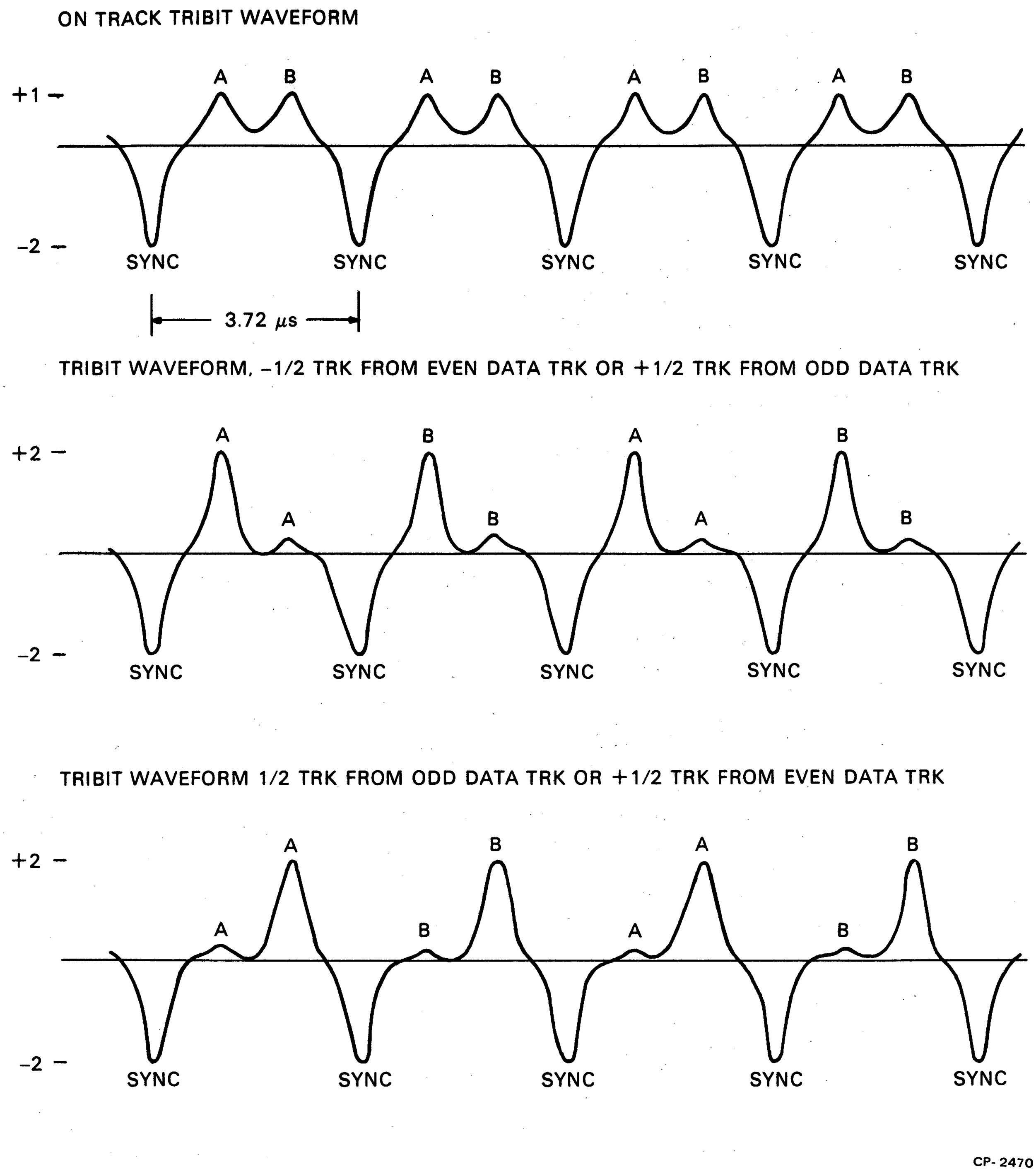


Figure 5-22 Tribit Waveforms

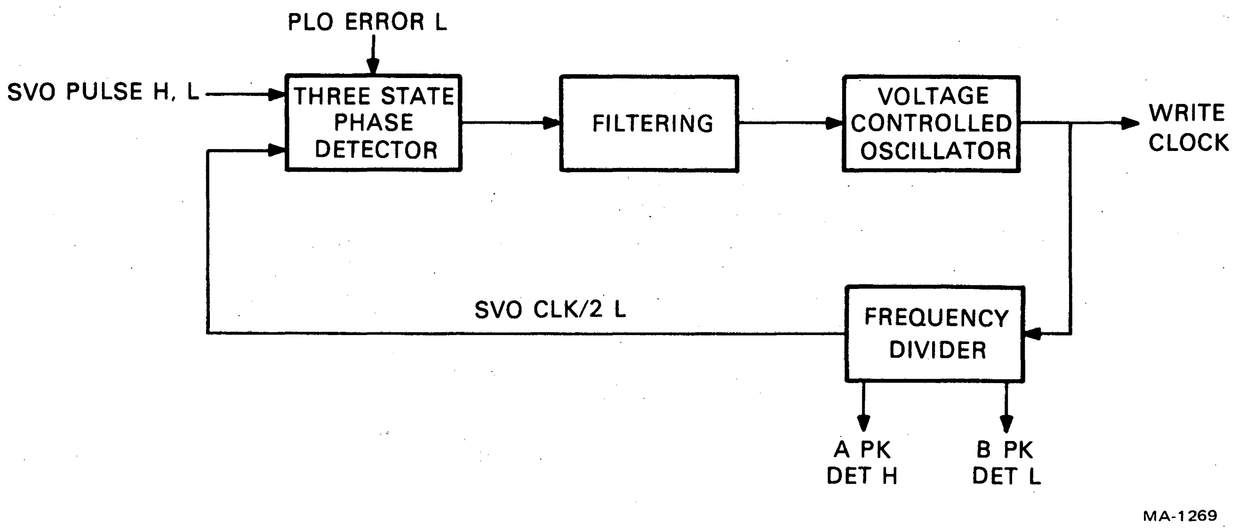


Figure 5-23 PLO Block Diagram

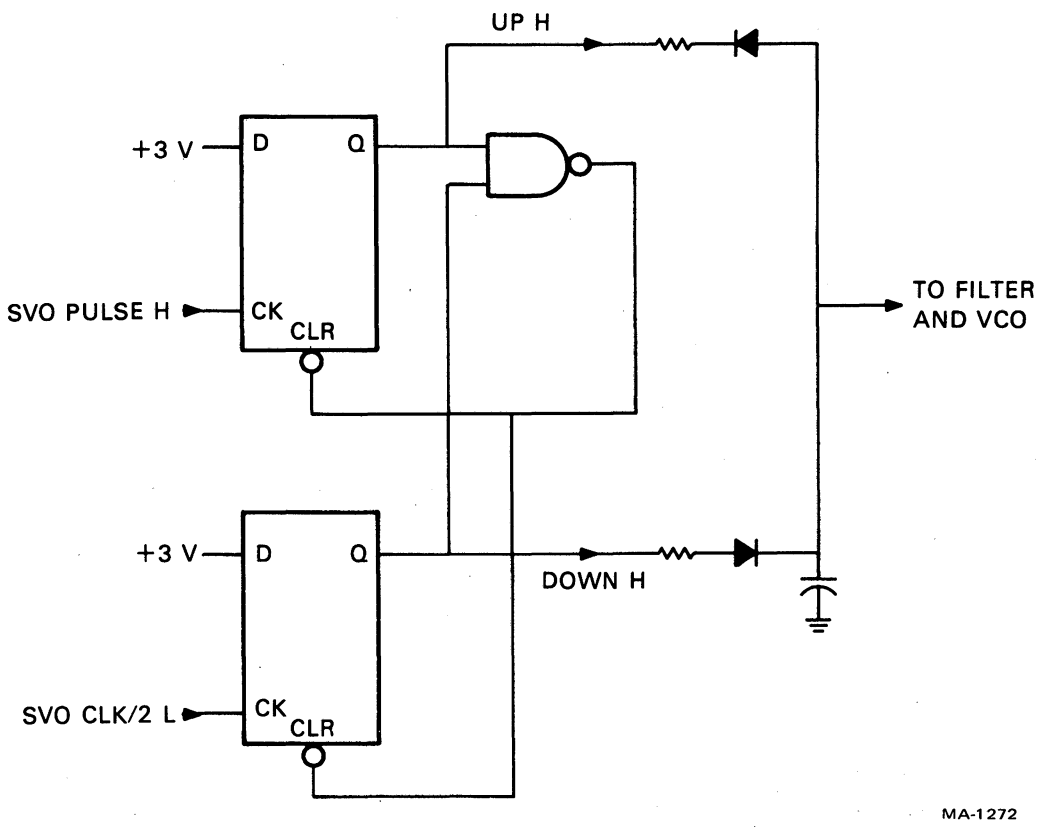


Figure 5-24 3-State Phase Detection Algorithm Implementation

The diagram in Figure 5-24 shows that the SVO PULSE H signal enters a flip-flop as a clocking pulse in the phase detector. (Actually, SVO PULSE H first enters a 550 ns one-shot which provides the clocking signal to this flip-flop.) Also, SVO CLK/2 enters an identical flip-flop, also as its clocking pulse. The logic does not allow both flip-flops to be set at the same time; the NAND gate, in this case, resets both of the flip-flops. If SVO PULSE H occurs more frequently than SVO CLK/2 L, then the loop is not running fast enough. In this case, the UP H signal is asserted a greater percentage of the time than DOWN H, and the capacitor is charged more often than it is discharged. Thus, after filtering, the VCO will input this analog signal and speed up the loop. If, however, SVO CLK/2 L occurs more often than SVO PULSE H, which means that the loop is running too fast and must slow down, then DOWN H is asserted a greater percentage of the time, and the capacitor is discharged more often. Thus, a lesser voltage is filtered and sent to the VCO, which then slows down. Finally, if SVO PULSE H and SVO CLK/2 L are synchronized, UP H and DOWN H are both asserted for the same percentage of time, and the loop "coasts" at the established frequency.

The timing diagram in Figure 5-25 illustrates the process just described. The first line in the diagram represents the SVO PULSE H signal from the servo surface. Each pulse is 1.1 ms long. The line below it represents the output of the 550 ns one-shot that is applied to the top flip-flop in Figure 5-24. The output pulses from the 550 ns one-shot have a duration of 550 ns, which is half the length of SVO PULSE H. The third line of the timing diagram is SVO CLK/2 L. When the SVO PULSE H (and thus the output of the one-shot) and SVO CLK L pulses are synchronized, the loop is running at a constant rate. The rising edges of both the one-shot pulse and the SVO CLK/2 L pulse coincide, and both flip-flops are set and then immediately reset. This immediate reset is illustrated on the UP H and DOWN H lines in the diagram as a single segment. In this case, UP H and DOWN H are both true the same percentage of the time, and the VCO and loop are unaffected.

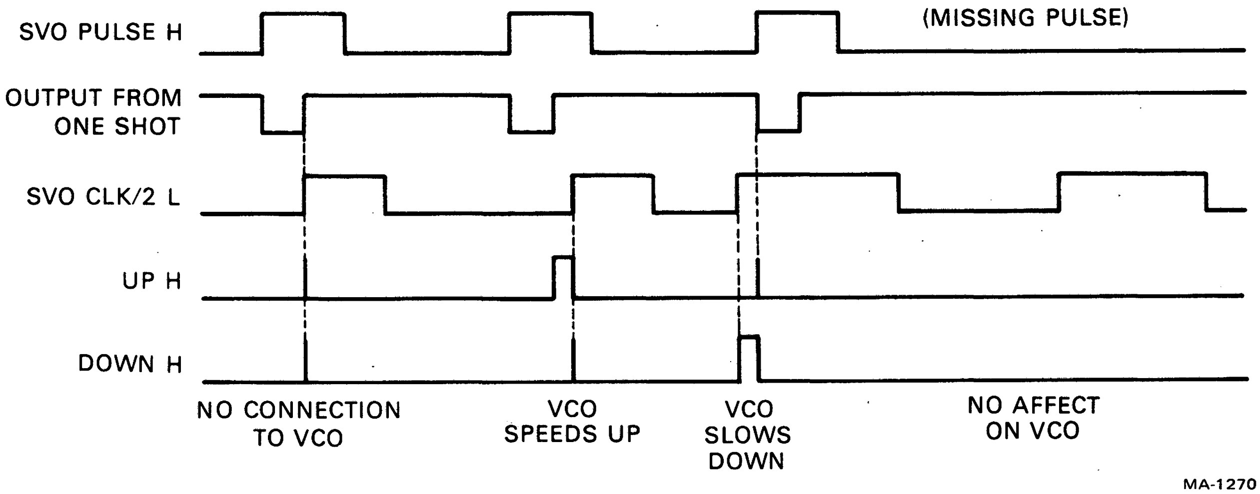


Figure 5-25 Phase Detector Timing Diagram

If the disks speed up slightly for some reason, then SVO PULSE H will occur more frequently. Thus, the loop must speed up. The timing diagram represents what occurs in this case. The rising edge of the output from the one-shot makes UP H true. It stays true, and provides the UP H signal to speed up the VCO until SVO CLK/2 L goes true. At this point, both flip-flops are forced to reset and UP H goes low. Similarly, if the disks slow down slightly, the loop speed must also be reduced. In this case, the SVO CLK/2 L will be true before the one-shot output goes true, and thus DOWN H will occur to slow down the VCO, until the one-shot pulse and SVO CLK/2 L overlap, as in the diagram.

This circuitry is designed to make the phase detector "immune" to missing sync pulses, such as the three missing pulses that are used for indexing. The circuitry that produces SVO PULSE H from the Tribit signal also produces a signal called SVO PULSE L. This enters the phase detector logic as shown in Figure 5-26. When SVO PULSE L is true, indicating that there is no servo pulse during the time that it is true, then the gating holds both flip-flops reset, so that neither UP H nor DOWN H is asserted. Thus, the loop will "coast" past any missing tribits. (If there are 4 or more missing tribits in any 16 consecutive words, circuitry on the M7908 will set the error signal SET SVO ERR L.) Again, the timing is shown in Figure 5-25.

The analog section of the phase detector and the low pass filter circuitry are shown in Figure 5-27. The UP H and DOWN H signals will alternately charge or discharge the capacitor C1, as described above.

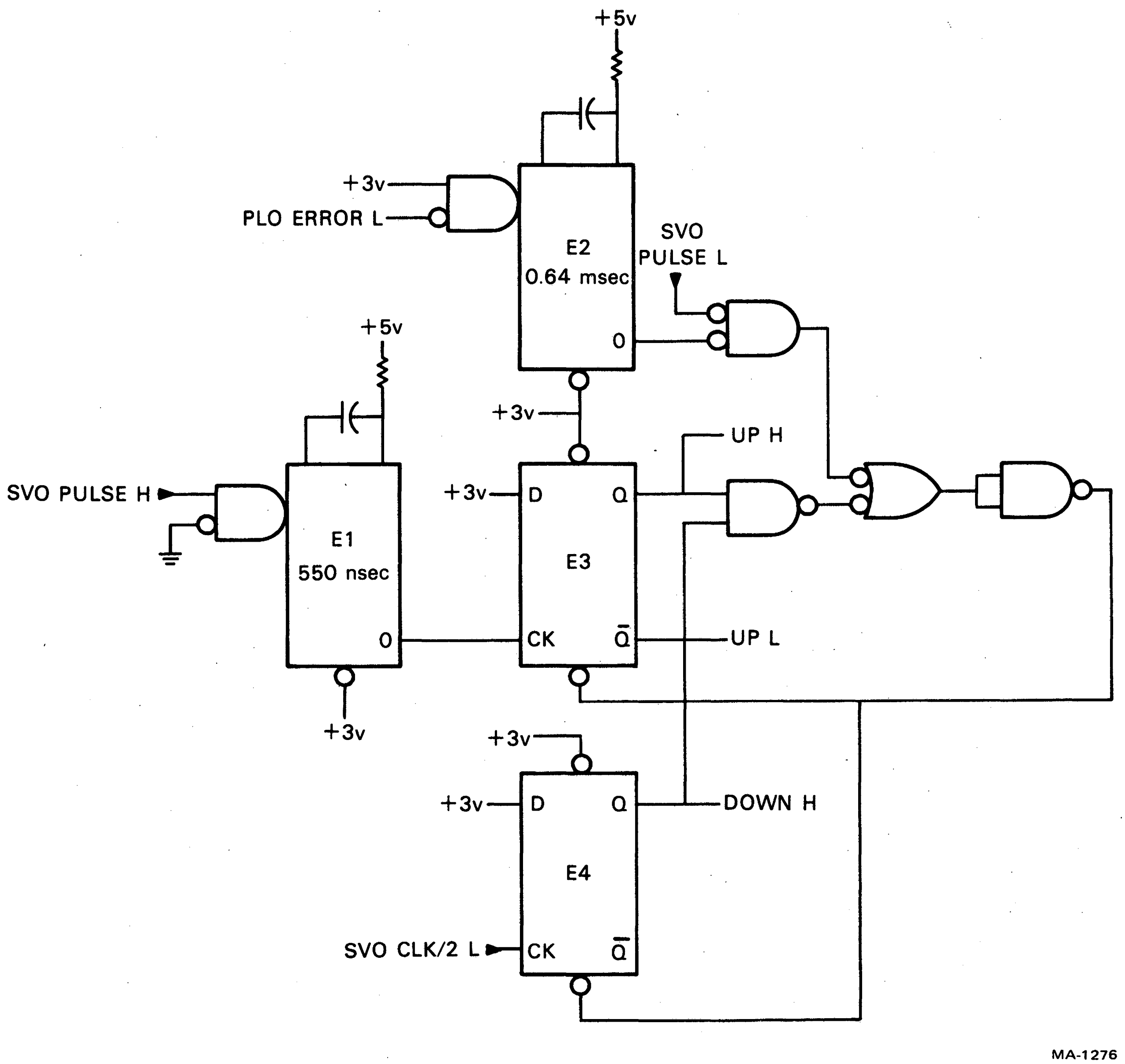


Figure 5-26 Phase Detector Circuitry

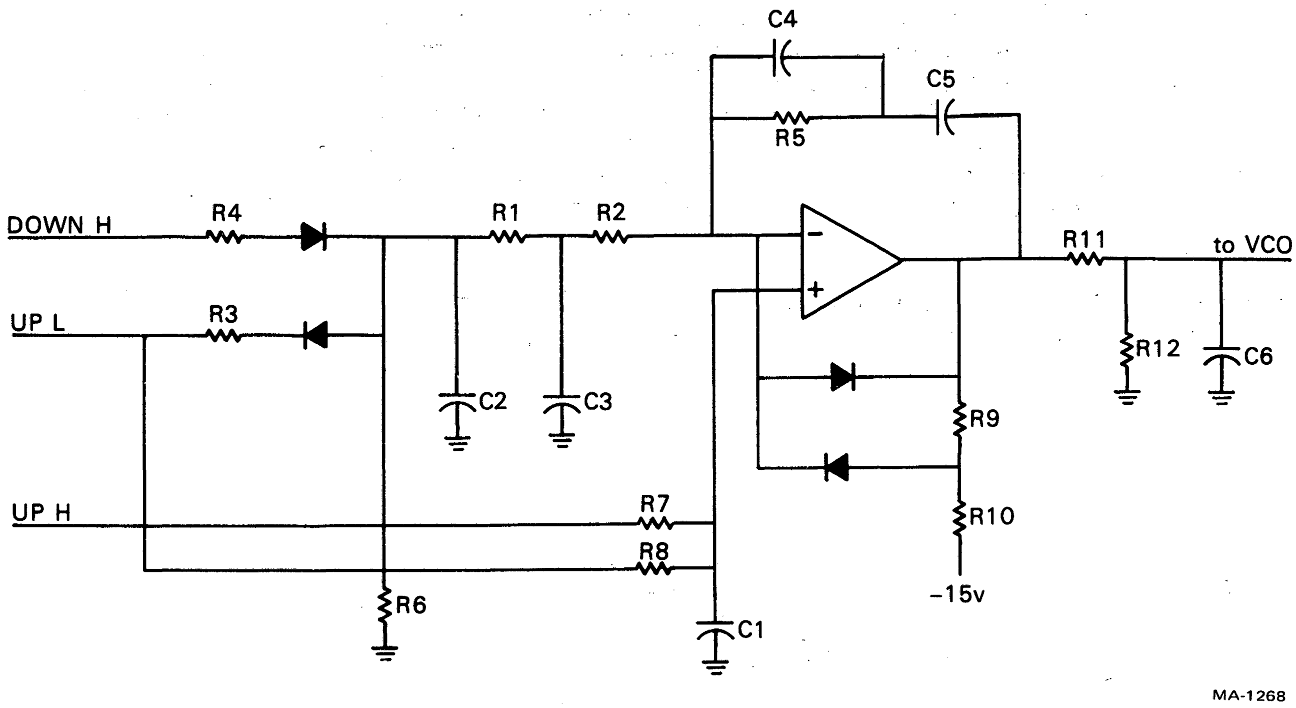


Figure 5-27 Analog Portion of Phase Detector Circuitry and Low Pass Filter

Voltage-Controlled Oscillator – The voltage-controlled oscillator (VCO) receives the filtered signal from the phase-detector circuitry, which will make it speed up, slow down, or coast at its current frequency. The nominal output frequency of the VCO is 8.6 MHz, and its period is 116 ns. The output of the VCO is used as the Write Clock signal, which is used to clock and synchronize write data to the rotational speed of the cartridge.

Frequency Divider – The frequency-divider circuitry produces three main signals. The first is SVO CLK/2 L, which is the PLO feedback signal to the phase detector described earlier. SVO CLK/2 L is equivalent to the Write Clock signal divided by 32. Second, the frequency divider produces SVO CLK L, which is equivalent to Write Clock divided by 16 (or twice SVO CLK/2 L). This signal enters the drive control module (M7905), and is used in the generation of index and sector signals (Paragraph 5.2.1.3). The third important output from the frequency divider is actually two signals, A PK DET H and B PK DET L. These two signals go to the track position detection circuitry on the same module (M7908). This circuitry is described in Paragraphs 5.3.1.20 through 5.3.1.24.

The frequency divider uses a 74161 4-bit counter to divide the VCO output by 16, which results in SVO CLK H. This signal is inverted to become SVO CLK L. Also, SVO CLK H is divided in half by a flip-flop, and some additional gating produces SVO CLK/2 L, A PK DET H, and B PK DET L.

5.3.1.20 A and B Peak Detector and Integrator – These circuits sample the peaks of the A and B tribit pulses and integrate or hold these values between pulses. The peak values of these pulses are used to derive the Track Error signal and a voltage for the automatic gain control of the difference amplifier and filter.

5.3.1.21 A–B Circuit – This circuit takes the difference between the A and B peak voltage values to yield the Track Error signal. The difference A–B represents the position of the servo head relative to the data track centerline. This difference, a function of servo head position (i.e., relative values of the A and B peaks) is referred to as Track Error. This signal serves as the input to the drive servo system in the detent or position mode. The difference A–B is also applied to the position detector circuits, after passing through the adaptive filter (described Paragraph 5.3.1.22).

5.3.1.22 Adaptive Filter – The adaptive filter (located on the M7908 module) serves two purposes in the RK07 drive. First, it scales the gain of the Track Error signal (from the A–B circuit described in Paragraph 5.3.1.21) at high velocities. This eliminates any track-counting problems caused by truncation of the Track Error signal. The truncation may be caused by the occurrence of an index pattern (three missing tribits) during a period of low tribit sample rate (due to rapid head movement across successive tracks). Also, the adaptive filter reduces the noise in the Track Error signal without reducing the magnitude of the signal (which may occur at high velocities), and allows a lower bandwidth filter at low velocities. The output of the adaptive filter is the signal TPD2 (A–B), which goes to the position detector (described in Paragraph 5.3.1.22).

Figure 5-28 illustrates the relation between the Track Error signal, the filtered TPD2 (A–B) signal, and the Velocity signal. Note that at a high velocity, the Track Error signal "dips," and that the adaptive filter compensates for this.

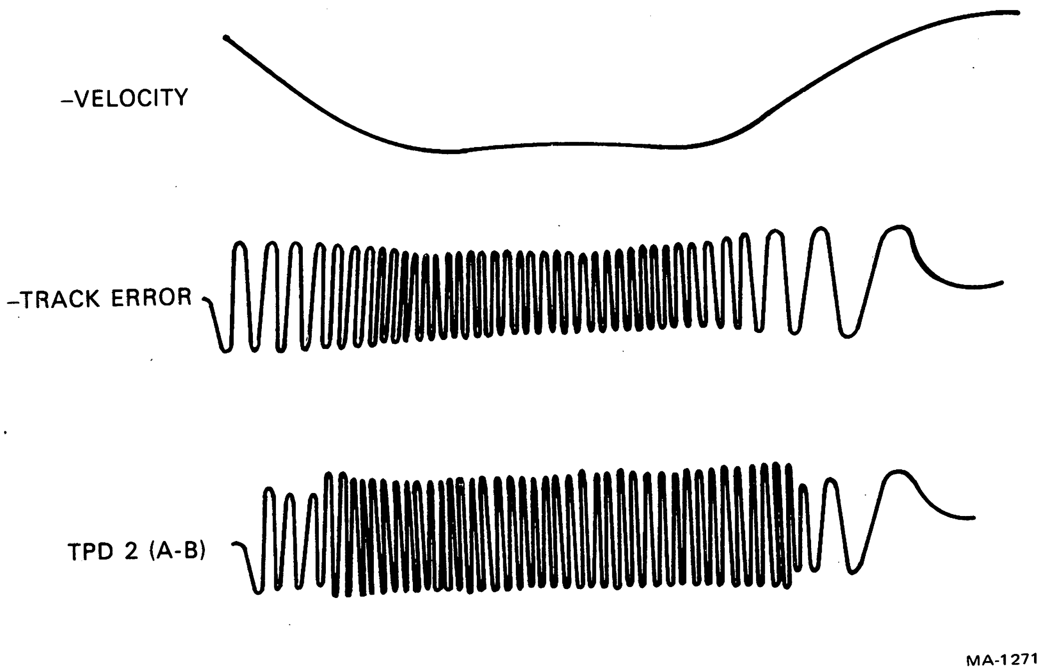
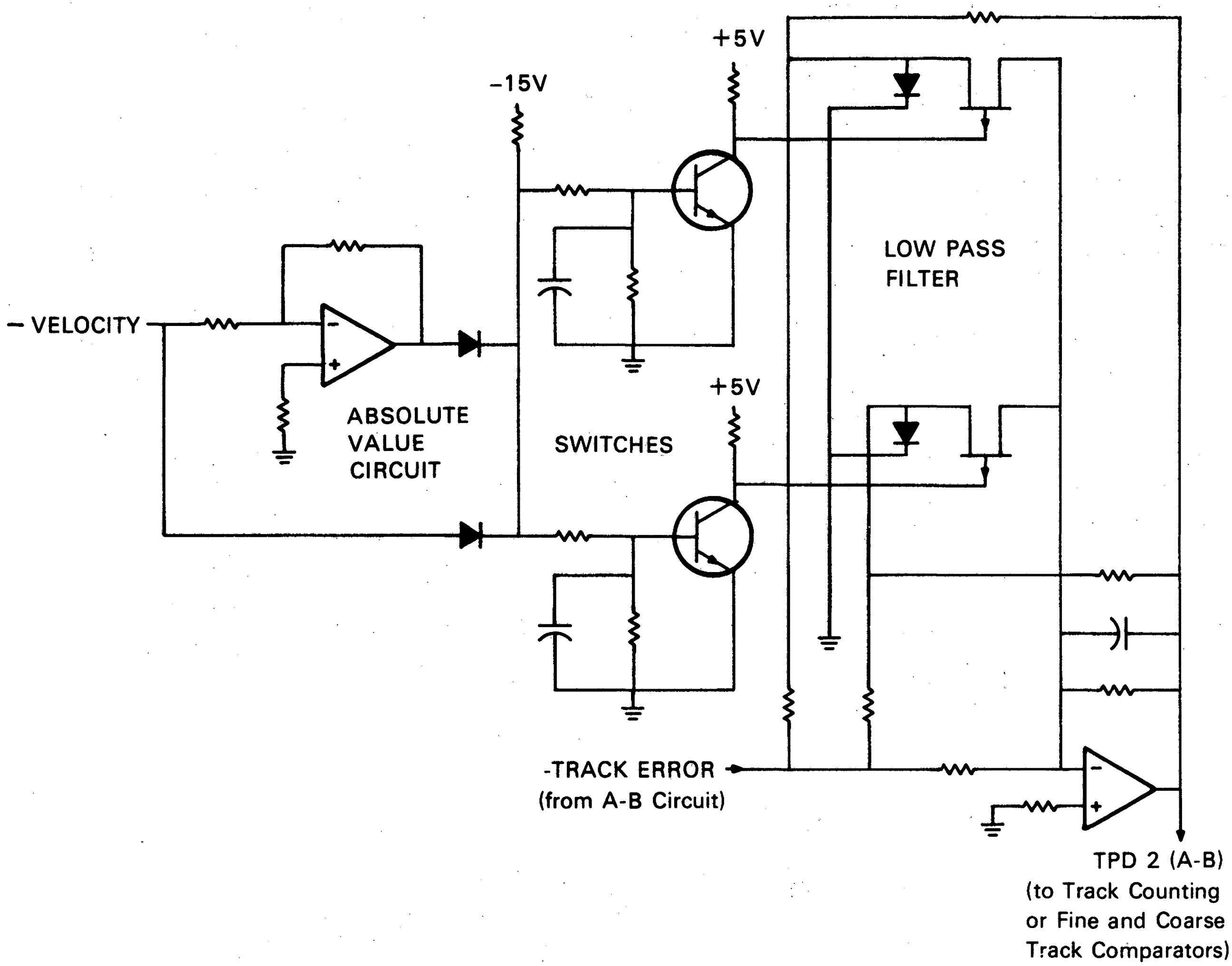


Figure 5-28 Adoptive Filtering Waveforms

Figure 5-29 is a simplified schematic of the adaptive filter. It consists of three main blocks. The absolute value circuit takes the absolute value of the Velocity signal. The low pass filter section receives the Track Error signal from the peak detect circuitry, and the two FET switches control the bandwidth and dc gain of the low pass filter section, depending on the magnitude of the Velocity signal.



FILTER CHARACTERISTICS

–VELOCITY	D.C. GAIN	BANDWIDTH
0 to 19.1 cm/sec (7.5 in/sec)	–1.00	3.4 KHz
19.1 cm/sec (7.5 in/sec) to 3.8 cm/sec (14.5 in/sec)	–1.11	6.8 KHz
3.8 cm/sec (14.5 in/sec) to 127.0 cm/sec (50.0 in/sec)	–1.38	67.0 KHz

MA-1288

Figure 5-29 Adaptive Filter

If the magnitude of the Velocity signal is less than 19.1 cm/s (7.5 in/s), then both FETs are open, and the dc gain is -1.00, while the filter bandwidth is about 3.4 kHz. If the magnitude of the Velocity signal lies between 19.1 cm/s (7.5 in/s) and 36.8 cm/s (14.5 in/s), then FET A switches on, but B remains off. The gain of the filter increases to -1.11, and the bandwidth is raised to 6.8 kHz. If the absolute value of the Velocity signal is greater than 36.8 cm/s (14.5 in/s), both FETs go on and the filter bandwidth increases to 67 kHz, along with an increase in the dc gain to -1.38.

The output of the adaptive filter, TPD2 (A-B), goes to the position detection circuitry. For higher carriage velocities, the position detector will be able to "see" all the tribits that the servo head picks up because of the gain in the adaptive filter. For lesser velocities, the gain is not as critical, but the reduced filter bandwidth results in less noise entering the position detector.

5.3.1.23 Position Detector - The position detector derives the Coarse Track, Fine Track, and Fine Track Delayed signals. Figure 5-30 shows the relationship of these signals versus distance except for Fine Track Delayed (Figure 5-31), which is a function of time. Coarse Track and Fine Track signals are used for deriving track count pulses which decrement the difference counter, and Fine Track signal is used to reset the forward flip-flop or reverse flip-flop.

The Fine Track Delayed signal is used for the detection of drive off-track error. This signal is asserted if the Fine Track signal is absent for at least 0.85 ms.

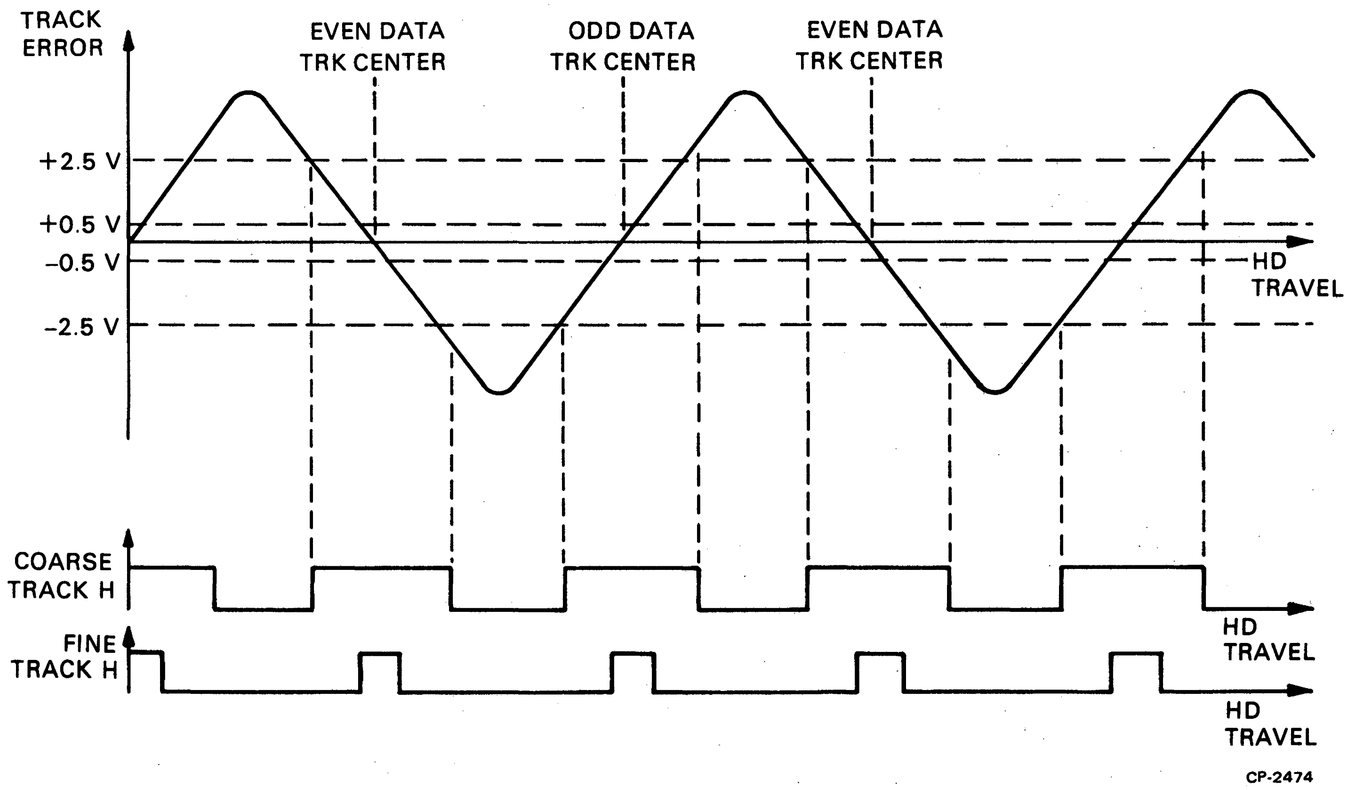


Figure 5-30 Position Signals

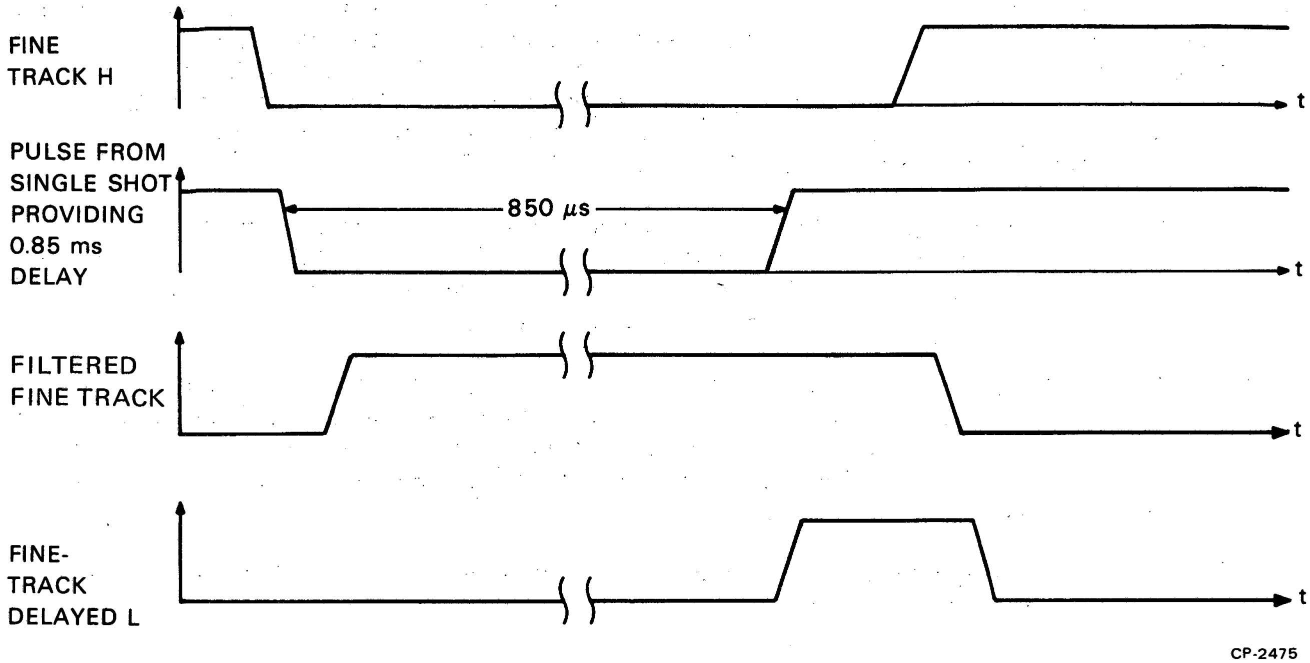


Figure 5-31 Fine-Track-Delayed Timing

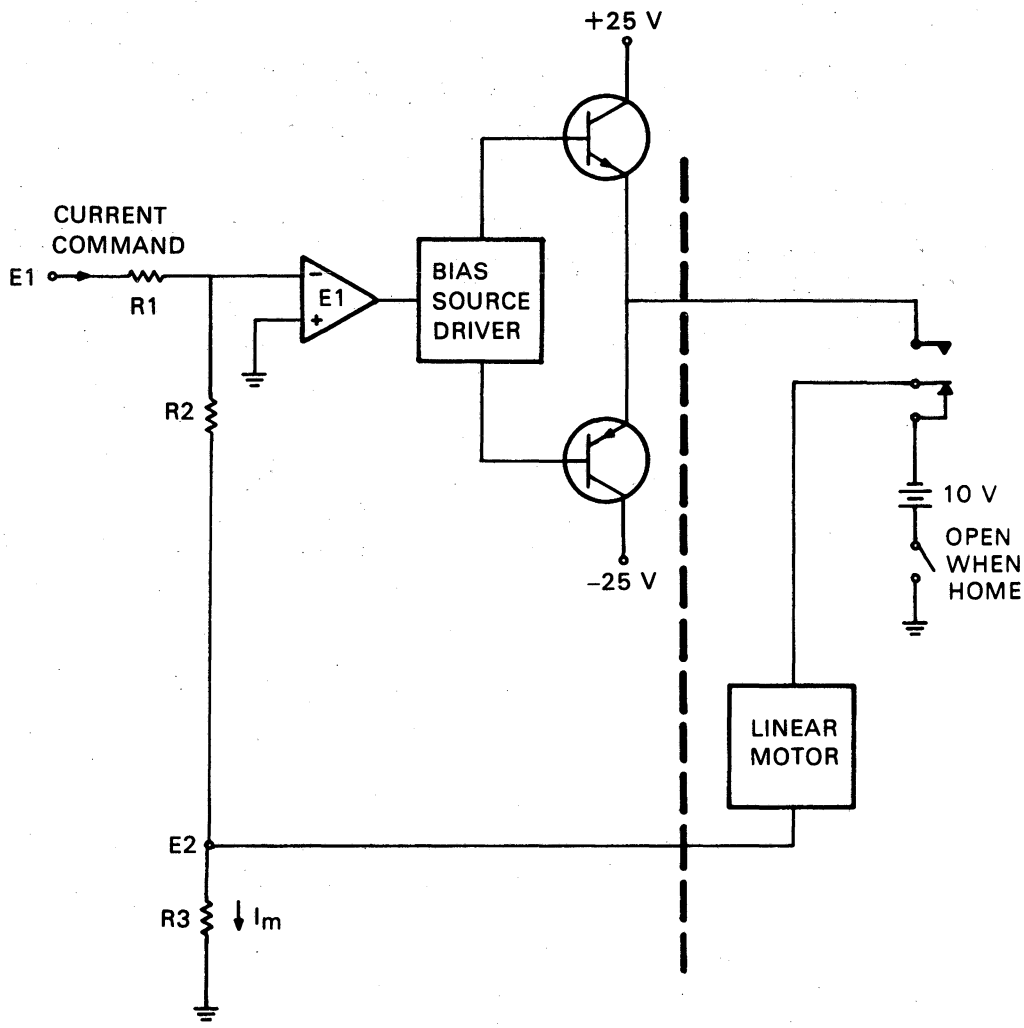
5.3.1.24 A+B Circuit – This circuit provides the sum of the peaks of the A and B pulses for use as a control signal for the AGC of the Tribit signal.

5.3.1.25 Power Amplifier – Figure 5-32 is a schematic of the RK07 power amplifier. The power amplifier can most easily be understood by thinking of it as an operational amplifier connected in the inverting configuration with R2 being the feedback resistor and R1 being the input resistor. The motor is part of this operational amplifier and the load is the current sense resistor R3. Thinking of it in that way, it is apparent that the voltage gain is $R2/R1 = 5.11K/24.9K = 0.21$. The motor current is equal to the output voltage divided by the current sense resistor R3. Therefore, the gain from input volts to motor current in amperes is $(R2/R1)/R3 \cong 1$.

5.3.1.26 Servo Release Switch and Maintenance Switch

Servo Release Switch (S1)
The servo analog module (M7906) has an edge-mounted servo release switch whose handle is set toward MAINT when it is desired to move the carriage by hand while observing signal outputs, or under any conditions where servo motion could harm service personnel or the drive.

Safety Switch
The servo analog module (M7906) also has a safety switch edge-mounted on the board. This switch is also set toward MAINT when performing head adjustments or other service operations in which inadvertent carriage motion could harm personnel or damage the drive. When in this position, the switch inhibits the servo unsafe circuitry in the drive, preventing the accidental unloading of heads under battery power. This switch also write protects the drive; i.e., if the switch is left in its disconnect (MAINT) position, the drive will remain write protected and the WRITE PROT indicator will remain lit. If a write command is subsequently received, write lock error will occur.



GAIN CONSTANT:

(1) $$\frac{E1}{R1} = \frac{E2}{R2}$$

(2) $$E2 = I_m \bullet R3$$

(3) $$\frac{I_m}{E1} = \frac{R2}{R1 \bullet R3} = 1.01 \text{ amp/volt}$$

MA-1287

Figure 5-32 Linear Motor Power Amplifier Functional Schematic

5.3.1.27 Servo Preamplifier – The servo preamplifier is a small metal package whose input is a low-level (2 mV peak-to-peak) differential tribit signal train from the dedicated servo surface of the disk cartridge.

The basic function of the preamplifier is to amplify this low-level input to an output at peak-to-peak levels of 400 mV. This output feeds the AGC amplifier and filter network of the track position detector/phase lock oscillator. Details of the subsequent signal processing in track-position detection are given in Paragraph 5.3.1.18.

Figure 5-33 is a simplified block diagram showing the basic elements in the servo preamplifier. The input biasing network sets the operating level of the El 733 differential video amplifier at 6 Vdc, nominal. Amplifier gain is 200.

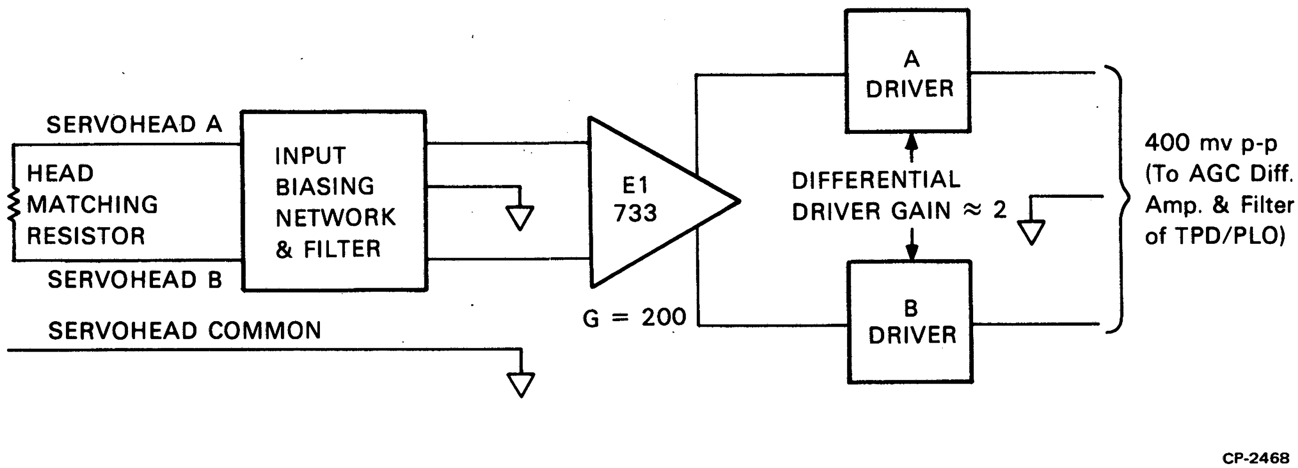


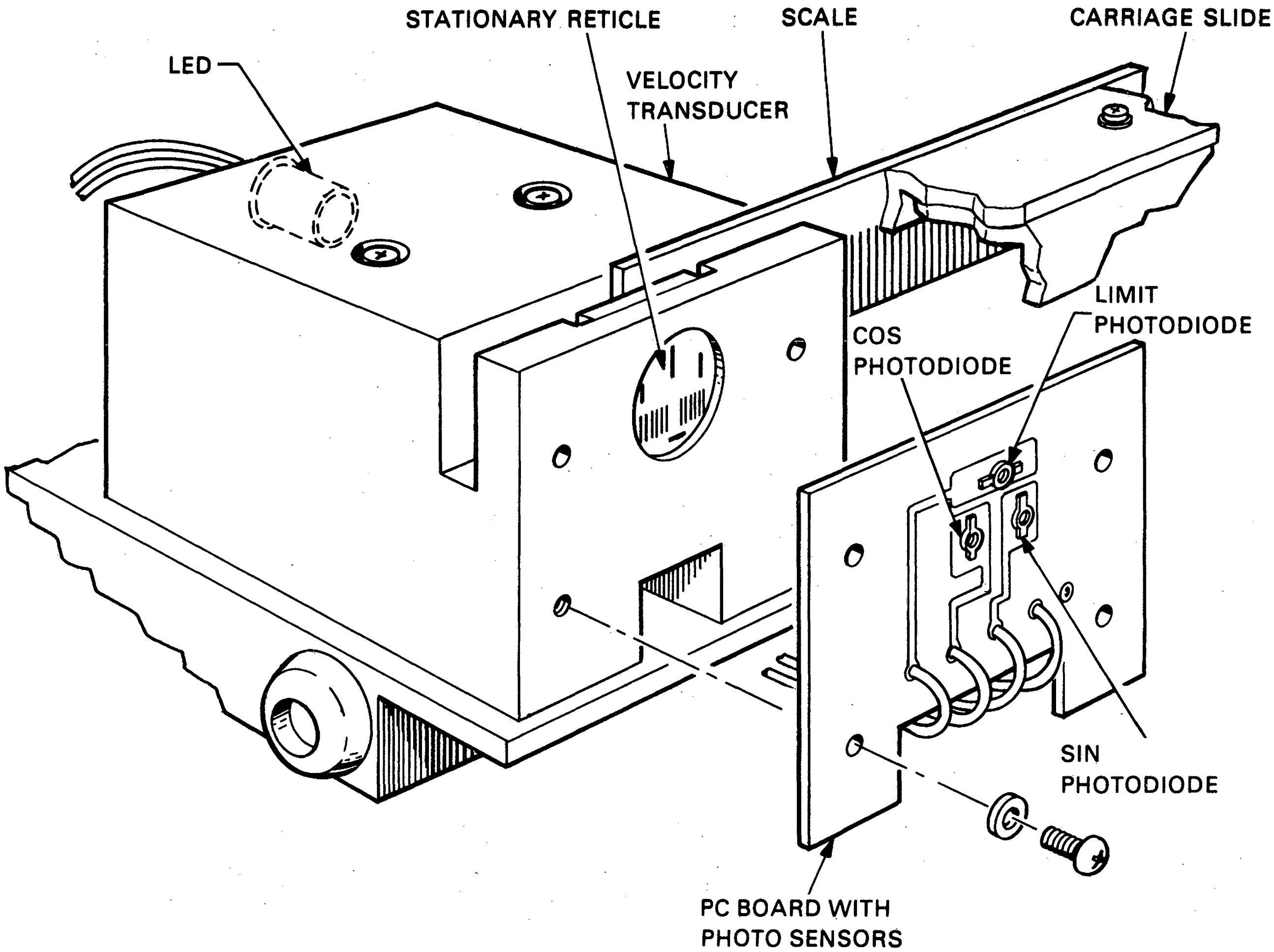
Figure 5-33 Servo Preamplifier Block Diagram

5.3.1.28 Phototransducer and Preamplifier – The phototransducer is used for deriving velocity feedback for the head positioner during the time when the heads are between the outer limit and inner limit. Feedback velocity information during the period when heads are outside this zone is provided by the load/unload tachometer (Paragraph 5.3.1.16).

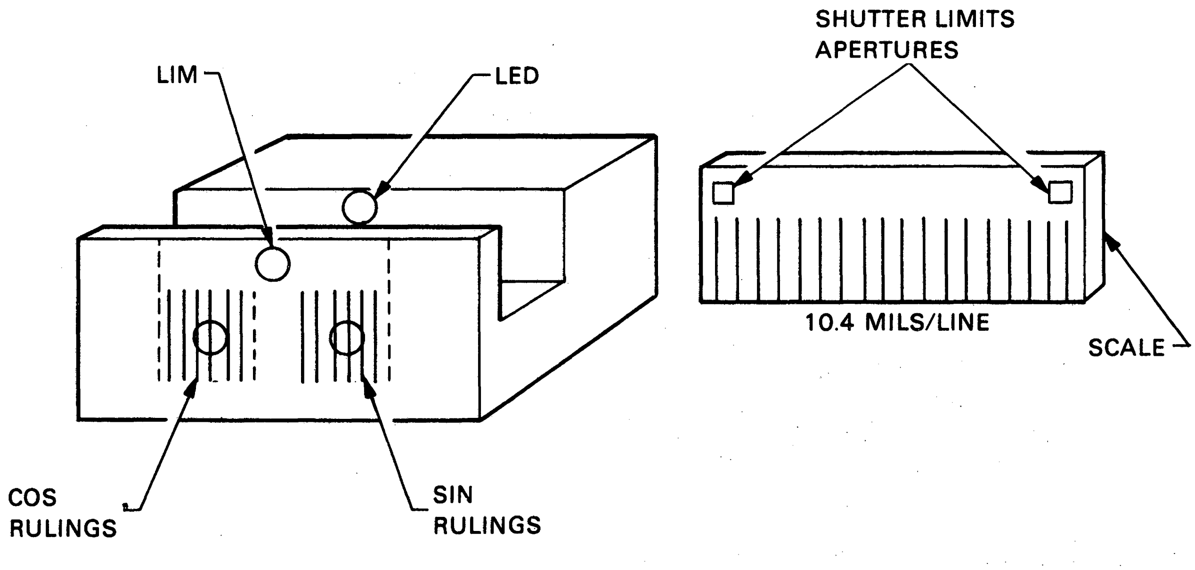
The glass phototransducer is a U-shaped plastic module. As seen from the rear of the drive, the left-hand arm of the U (Figure 5-34 illustrates the design principle) contains a single LED. On the other arm of the U is a limits photodetector, a fixed glass slide with sine and cosine rulings and corresponding sine and cosine photodetectors. A 7.6 cm (3 inch) long glass slide attached to the carriage and having the same glass ruling pitch acts as a shutter that modulates the LED output reaching the sine and cosine detectors after passing through the interstices between the fixed and moving glasses.

5.3.1.29 Carriage Home-Lock Assembly – A solenoid-operated home lock (Figure 5-1) mechanically restrains the carriage against inadvertent motion whenever heads are commanded to remain at the home position, and ensures that the heads will remain safely in their home position during shipment. The solenoid is actuated only when the control logic has determined it is safe to load the heads.

5.3.1.30 Servo Head Assembly – The Servo Head Assembly consists of the heads support subassembly and the four heads (three data recording and one dedicated servo surface heads). The heads, from top to bottom of the assembly, are designated as 0, 1, S, and 2, respectively. Head S (the servo head) is a read-only sensor, receiving the prerecorded tribit message from the top surface of the bottom disk.



a. Artist's Perspective



b. Shutter Concept for Position Sensing

CP-2469

Figure 5-34 Phototransducer for Velocity Feedback Loop

The heads are individually mounted in the slots provided at the forward end of the carriage. Each spring-loaded head bracket has a short ramp section which, when the heads are retracted, rides through slots in the cam tower and causes the heads to separate. When the heads are loaded onto the disk (Figure 5-35), the air flow caused by disk rotation exerts a pressure (air bearing) counteracting the spring-loaded headarms and causing the heads to *fly* approximately 35 microinches from their respective disk surfaces. With disk rotation held constant, the heads remain at this relatively fixed distance from the disk surfaces.

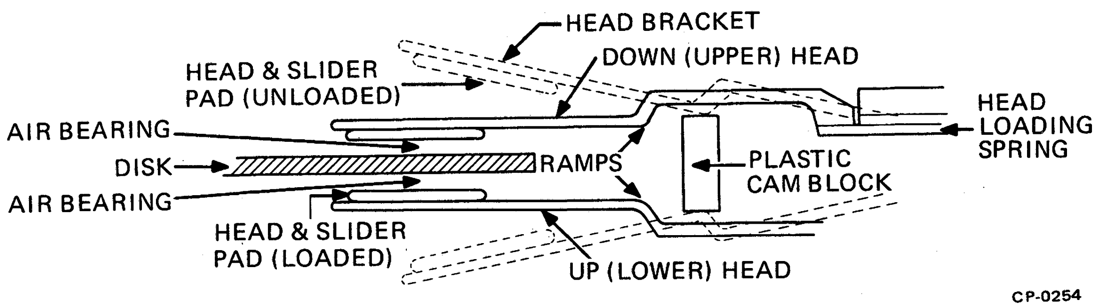


Figure 5-35 Head-Loading Mechanism

5.3.1.31 Linear Motor, Carriage, and Coil Assembly – The linear motor of the disk drive (Figure 5-1) provides the motive force for head positioning. The heads are supported on a carriage that is integrally attached to the moving coil of the linear motor. Structurally, the motor comprises a permanent magnet through which the coil moves in and out in response to currents whose magnitude and polarity are determined from the positioning subsystem electronics. The carriage, driven by the moving coil of the linear motor, rides on a forward (inner) pair of roller bearings and an identical aft pair, both pairs being supported by a centerless-ground guide rod.

Lateral stability and support are provided by two vertically oriented bearings that ride on ways paralleling the guide rod. A pair of rubber bumpers on the coil, and a corresponding pair on either side of the ways at the forward limit of carriage travel provide a high degree of shock isolation against carriage impact.

5.3.2 Positioning Operation

The following sections described the various operations pertinent to the positioning subsystem. These operations are:

1. Loading heads (Paragraph 5.3.2.1)
2. Unloading heads (Paragraph 5.3.2.2)
3. Recalibrate (Paragraph 5.3.2.3)
4. Seek (velocity mode) (Paragraph 5.3.2.4)
5. Detent (position mode) (Paragraph 5.3.2.5)
6. Offset (Paragraph 5.3.2.6).

The servo has three primary modes of operation: the detent mode, the seek mode, and head load mode.

In the detent mode (also known as the position mode or the track-following mode), the servo tries to hold the servo head centered over the boundary of two servo tracks. The Feedback signals are the track error from the servo surface and the velocity from the glass scale.

In the seek mode (also known as the velocity mode), the servo tries to move the carriage at a velocity that is a nonlinear function of position. This function is clipped at 63 tracks so that all positions equal to or greater than 127 tracks away from the desired position command the same velocity. The servo has sufficient gain that the power amplifier saturates on acceleration and applies the full power supply voltage to the motor (less, of course, a small fixed drop in the power amplifier transistors).

In this mode, the glass velocity is fed back and compared with the function generator whose value is determined by the digital track count.

In the head-load mode, the velocity command generator puts out a constant voltage which is compared to the output of the magnetic head-loading tachometer to control the velocity. This magnetic tachometer works all the way back to the home position whereas the glass tachometer does not. This allows the velocity to be controlled in the region where the glass transducer does not provide velocity information.

5.3.2.1 Loading Heads – The heads may be loaded by either of two commands: (1) depression of the control panel RUN/STOP switch or (2) a command from the system, provided the RUN/STOP switch is depressed. Once the appropriate prerequisites are satisfied, i.e., the Unload Heads signal is negated (see Drive Control, Paragraph 4.2), head loading begins. At this time the load heads flip-flop on the M7907 will set as will the forward flip-flop and Enable Forward Servo signal of the direction-select circuitry. In addition, the home lock is now released. Because the difference counter is reset at this time, the servo command is for a low speed. As a result, the positioner now accelerates until the feedback from the load/unload tachometer equals the command and the heads move at between 12.7 and 25.4 cm/second (5 to 10 inches/second). This motion takes the heads down the head load ramp to the outer limit where the load/unload tachometer feedback is switched off and the phototransducer velocity feedback is enabled. Due to command differences, the velocity now slows to 2.0 cm/second (0.8 inch/second) until the heads reach the inner limit.

At the inner limit, the load heads and forward flip-flops are reset, the RTZ and reverse flip-flops are set, and the carriage is now commanded to move back to 2.0 cm/second (0.8 inch/second) to the outer limit.

At this point, the reverse flip-flop is reset, forward is set, and the carriage again advances forward until the Coarse Track signal is sensed where the positioner transfers from velocity mode to detent mode (Paragraph 5.3.2.5). At this point, the RTZ and Enable Forward Servo signals are negated.

5.3.2.2 Unloading Heads – The positioner will unload the heads from:

1. Release of RUN/STOP switch
2. Unload heads command from system
3. Any of several errors within the drive for which it would be unsafe to leave the heads loaded.

Whenever one of the three conditions above occurs, the unload head flip-flop on the M7705 is set immediately, causing any other positioning, if underway, to be discontinued. The reverse flip-flop is set, and the velocity command generator is set for a low velocity (the difference counter is reset). The heads accelerate to 2.0 cm/second (0.8 inch/second) if the heads are between the outer and inner limits and 12.7 to 25.4 cm/second (5 to 10 inches/second) if outside the outer limit. The positioner continues until it reaches the home position at which time the command is removed from the motor.

The positioner will unload the heads in an emergency manner if the ac power is interrupted or if a servo unsafe condition is sensed within the drive. For these cases, the rechargeable battery supply is applied to the linear motor directly to unload the heads. This is an open-loop condition in which the carriage moves without the benefit of velocity feedback.

4.3.2.3 Recalibrate –A recalibrate is performed by the system whenever it detects that the physical location of the positioner does not agree with the cylinder address register. For this operation, the drive responds by resetting the cylinder address register and cylinder difference counter on the M7907, setting the RTZ and reverse flip-flops. The positioner moves at 2.0 cm/second (0.8 inch/second) until the outer limit is sensed, then the reverse flip-flop is reset, the forward flip-flop is set, and the positioner proceeds forward until the first Coarse Track signal is sensed at which time the Enable Forward Servo signal is reset and the servo goes into detent (Paragraph 5.3.2.5).

The heads are now positioned at cylinder 0, which corresponds to the state of the cylinder address register.

5.3.2.4 Seek (Velocity Mode) – When a seek operation is to be performed, a seek command and desired cylinder address are transmitted to the drive. The new address is subtracted from the present address to obtain a digital difference that is converted into an analog voltage by the circuitry on the servo analog module. The serial subtractor performs the calculation. The cylinder difference register holds the calculated cylinder difference (i.e., the 1's complement number), and the carry logic determines the direction of head motion. The difference counter, which is preloaded with the cylinder difference for the seek, keeps count of cylinder difference as positioning proceeds, and provides the difference to the D/A converter and function generator.

The sequence of events on the M7907 in moving the head from an existing cylinder location to a new location is as follows.

1. The address enable flip-flop must be set.

2. The seek command flip-flop is set.

3. The new cylinder address is received by the drive and a serial difference with the present cylinder address is performed. The resultant difference is loaded into the cylinder difference counter and the desired cylinder address is loaded into the cylinder address register. The result of this operation by the cylinder address register, cylinder difference register, and difference counter is a binary number in which the final carry indicates direction and the sum denotes the number of cylinders to be traversed in the command seek.

   If the difference is less than 64 (i.e., the heads must move less than 64 tracks to arrive at the desired cylinder), then the short-seek flip-flop is set. The inverted output of this flip-flop, SHORT SEEK L, goes to the dual-velocity-profile circuitry on the servo analog module, M7906. See Paragraph 5.3.1.11 for a discussion of the dual-velocity profile circuitry.

The following example (using only three cylinder address bits in the interest of simplicity) shows the arithmetic of the logical operation performed.

	Decimal	Binary	Operation
Present cylinder address	7	111 → 111	None
Desired cylinder address	5	101 → 010	Invert
Difference	2	1 001	Sum
Direction indicated: Reverse		Carry ↗	

Since the carry is asserted at the end of the differencing operation, the sum must be incremented by 1. Thus,

001 Sum
  1 Add 1 (in difference counter)
010 = decimal 2.

The case in which a "0" carry is obtained in the differencing operation can be similarly illustrated:

	Decimal	Binary	Operation
Present cylinder address	5	101 101	None
Desired cylinder address	7	111 000	Invert
Difference	2	101	Sum
Direction: Forward			

Since the "0" carry at the end of the arithmetic indicates a forward direction, the sum must be inverted to get the proper result. The value 101, thus becomes 010 = decimal 2.

The RK07 implementation of this binary subtraction process is based on serial differencing in which the present-address bit and the corresponding desired-address bit are applied bit by bit to the subtractor. The difference count becomes the input to a D/A converter on the M7906 whose output voltage is proportional to the velocity to be commanded. As each bit in the subtraction process is determined, it is shifted into the cylinder difference register while the desired cylinder address is shifted into the cylinder address register, replacing the present cylinder address, which is shifted out during the differencing operation.

Referencing the simplified examples given above, when the final state of the carry flip-flop is true, the resultant difference must be incremented by one. This is accomplished by incrementing the difference counter after the difference has been loaded into it. When the final state of the carry flip-flop is false, the resultant difference must be inverted bit for bit. This operation is accomplished by exclusive OR gates located between the cylinder difference register and the cylinder difference counter.

Provided there are no drive faults, the forward flip-flop or reverse flip-flop is set according to the state of the carry flip-flop. The Enable Forward Servo or Enable Reverse Servo signal is asserted and the appropriate velocity command is generated by the D/A converter and profile function generator.

The positioner now accelerates to the desired velocity based on the cylinder difference. For each cylinder crossing, the cylinder difference counter decrements by one during the seek. The velocity command is coincidentally lowered (except for cylinder differences greater than 127) so that the positioner decelerates in an orderly manner to the desired location. Cylinder differences equal to or greater than 127 produce a constant velocity command of 122 cm/second (48 inches/second).

The positioner continues to follow the profile as commanded until the cylinder difference counter equals 0. At this point, the Enable Forward Servo or Enable Reverse Servo signal is negated, with the resultant switching off of the velocity command, and the positioner goes into position mode (Paragraph 5.3.2.5).

5.3.2.5 Detent (Position Mode) – The positioner is in detent or position mode when it is *locked* by the servomechanism at a cylinder centerline or at an offset position. (See Paragraph 5.3.2.6 for the offset description.) This is accomplished by selection of the Track Error signal by the servo analog multiplexer on the M7906 as a Position Command signal by the servo. At the cylinder centerline, the Track Error signal is zero. If the positioner were disturbed such that it moved away from the centerline, the track error voltage would command the positioner in the direction to oppose the disturbed motion, thereby resulting in a held or locked position. It should be pointed out that the velocity feedback is also selected in detent to add stability to the servo system. Velocity feedback at this time allows a faster correction to a disturbance to the positioner.

When the drive enters the detent mode from velocity mode, the carriage is a nominal 1/4 cylinder (650 microinches) from the cylinder centerline. At this location, the servo analog multiplexer circuits cause the velocity command to be switched off, the Track Error signal to be switched on, and velocity feedback left on. The Track Error signal becomes the command to subsequently bring the positioner to the centerline. During this period, settling is generated on the M7705 module (a 3 ms pulse) to allow for the positioner to come to rest. The trailing edge of settling sets drive ready and drive status change (DSC) on the M7706, and also generates attention on the interface bus to indicate that the operation has finished.

5.3.2.6 Offset – Offset mode defines a means of repositioning the carriage small distances to either side of the cylinder centerline while in detent mode. Its purpose is to improve the chances of data recovery if data errors occur while positioned at the cylinder centerline. The offset mode is commanded from the system and the amount of the offset is determined from a code received by the drive. Refer to Table 3-5 for offset code details.

The RK07 drive may be offset by 12.5 microinch increments up to a maximum of ±600 microinches from the centerline.

There are three conditions for resetting the offset mode.

1. A return-to-centerline (RTC) command
2. A physical seek to another cylinder
3. A Write Gate signal received by the drive.

NOTE

This condition would produce fault and drive-off-track error. Writing of data is prohibited while offset.

When an offset is commanded to the drive, it does not go into velocity mode. Neither the forward flip-flop nor the reverse flip-flop becomes set. Instead, a voltage is generated by the profile function generator according to the offset code stored in the cylinder difference counter. This voltage is added to the Track Error signal in the servo analog multiplexing circuits on the M7906 module which results in a motion to a point where the sum of the two signals (Offset Value + Track Error) equals 0.

The offset command or the resetting of the offset mode triggers the 3 ms Settling signal on the M7705, resets drive ready, and, at the end of settling, generates attention to indicate to the system that the operation is completed.

5.4 READ/WRITE SUBSYSTEM

Figure 5-36 is the disk drive functional block diagram with the read/write subsystem blocks shaded. The major functional areas are discussed in the following subsections:

1. Write Circuits
2. Isolation Circuits
3. Read Circuits
4. Head Selection Circuits
5. Read/Write Fault Detection Circuits.

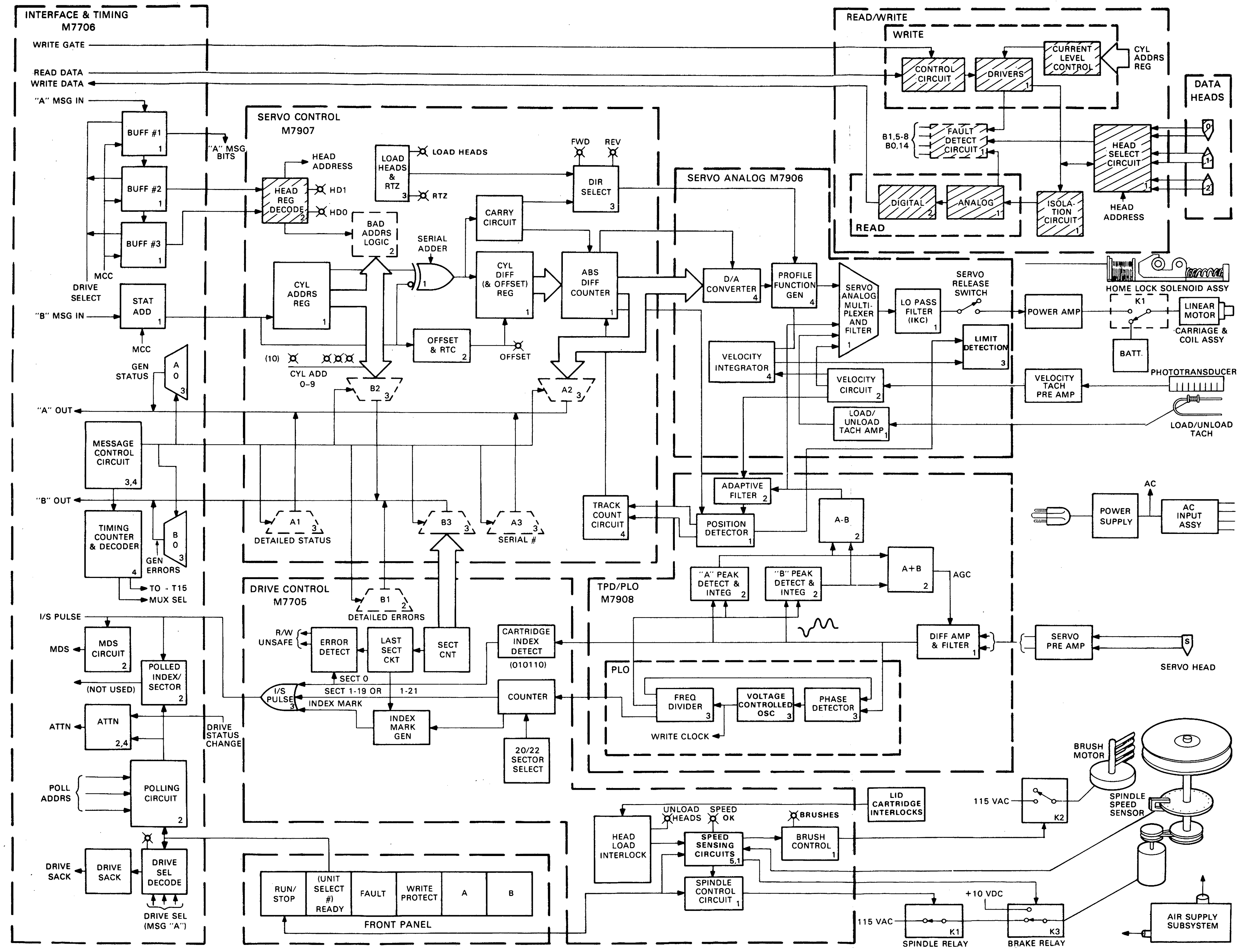


Figure 5-36 RK07 Disk Drive Functional Block Diagram with Read/Write Circuits Shaded

The discussion assumes reader familiarity with the basic principles of digital saturation magnetic recording. In writing, the area of the disk beneath the recording-head gap is completely driven to either of two possible magnetic states, completely overwriting any previously recorded data. As the disk moves beneath the head, the magnetic field created by the head gap is periodically reversed, and a magnetic flux transition is created on the recorded track at each reversal. The head, in reading, responds to each flux transition in the form of a bell-shaped pulse illustrated in curve A of Figure 5-37, the sign of the pulse being determined by the direction of that recorded flux reversal.

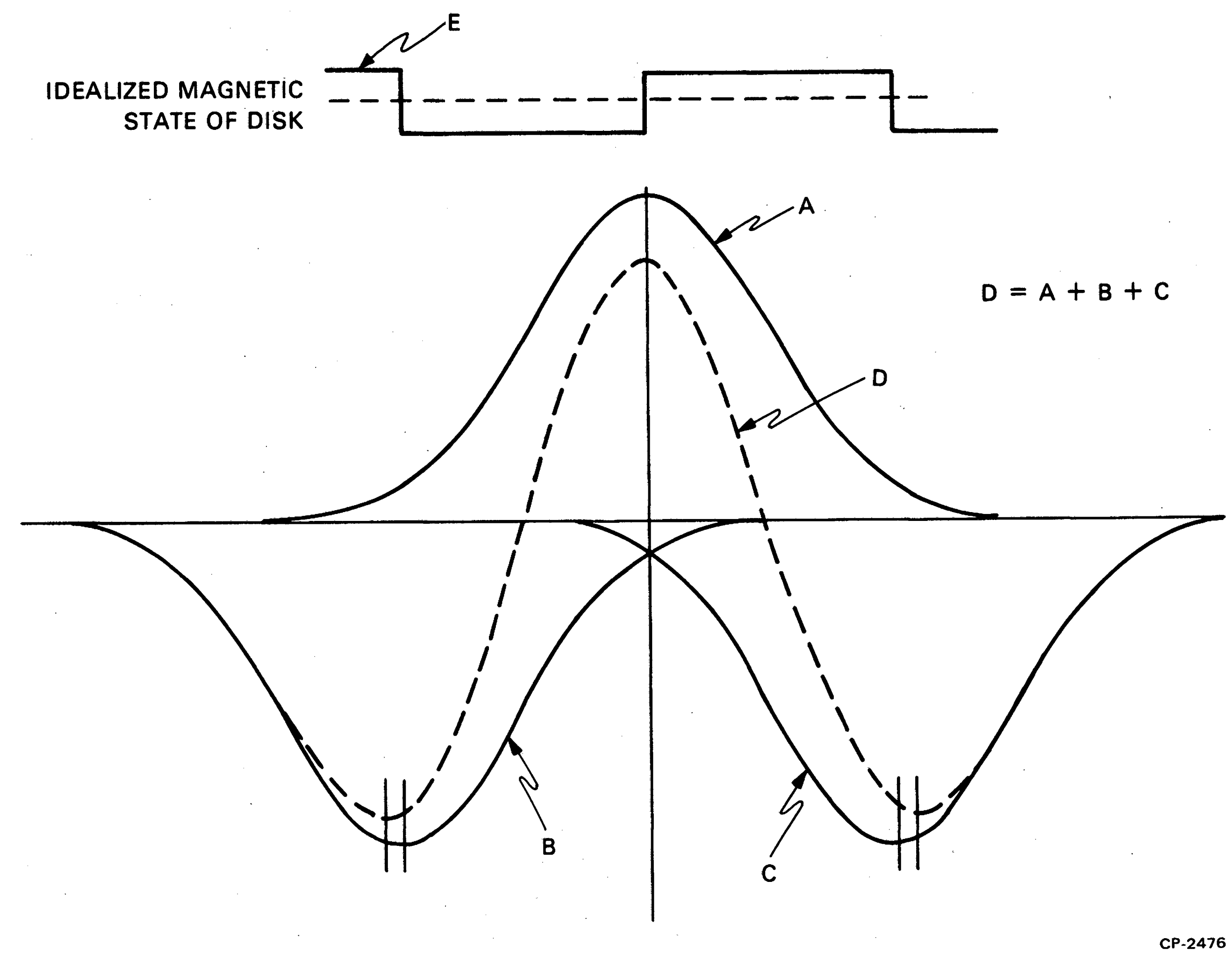


Figure 5-37 Superposition of Readback Signals

Data is encoded in terms of the intervals between flux reversals. In the RK07, the encoding notation is called modified frequency modulation (MFM), and is described in Paragraph 2.4.

The RK07 system is further defined as self-clocked, contiguous-pulse recording.

In contiguous-pulse recording, consecutive flux reversals are closely spaced so that, in reading, the complete pulse never appears, but merges with pulses from adjacent transitions to form readback signals (Figure 5-38).

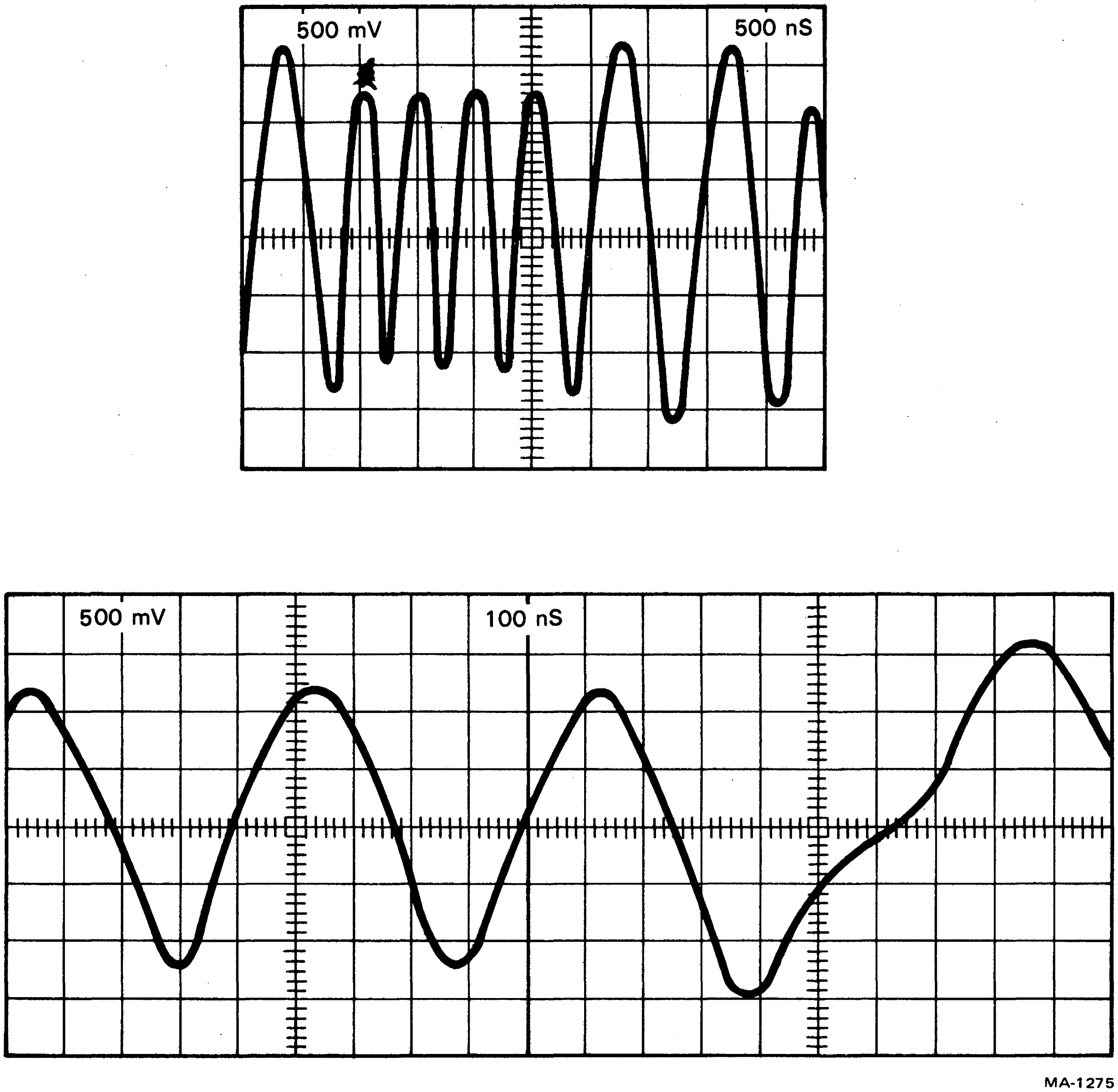


Figure 5-38 Typical RK07 Read Waveforms

It should be noted that the amplitude variation resulting from the superposition of pulses is of no concern, since the information content is carried in the time position of the voltage peaks. Figure 5-37 illustrates the superposition of readback pulses. Waveform E denotes the idealized magnetic state of a small segment of a recorded track. Waveforms A, B, and C represent the individual readback pulses that would result if each transition were completely isolated. Waveform D represents the actual readback resulting from the superposition of adjacent (contiguous) pulses. The peak displacement of pulses B and C (a phenomenon known as *peak shift*)is discussed in Paragraph 2.5 of this manual. Circuitry in the RK611 controller provides the necessary compensation for minimizing the effects of peak shift during controller/drive data interchange.

The real significance of the contiguous pulse recording is that the readback never exhibits a zero slope except at the peaks. Therefore, differentiation may be used to convert the peaks to zero-voltage crossings which are easy to process to a digital form.

Self-clocking means that the serially recorded information can only be decoded by self-reference. Information is recorded in the form of present or absent flux reversals at nominally equal intervals. Consecutive readback pulses alternate in polarity with no significance given to the shift.

Detection of the serially recorded information involves the measurement and classification of pulse intervals according to values established by the rules of the selected recording notation. The regular placement of pulses permits the application of phase-lock oscillator techniques for generating a synchronous clock that is used to establish the pulse intervals and the information content of the recorded data. This process is not a function of the disk drive, but is contained on the associated controller.

The Write Clock signal (see the Write Clock loop in Figure 5-39) is derived from the Tribit signal recorded on the dedicated servo surface. This clock signal is transmitted to the controller for the purpose of timing the write data sent to the drive. The Write Clock maintains bit density within precise limits despite any disk speed variation caused by line voltage fluctuations or other sources. Write Clock frequency is a nominal 8.602 MHz.

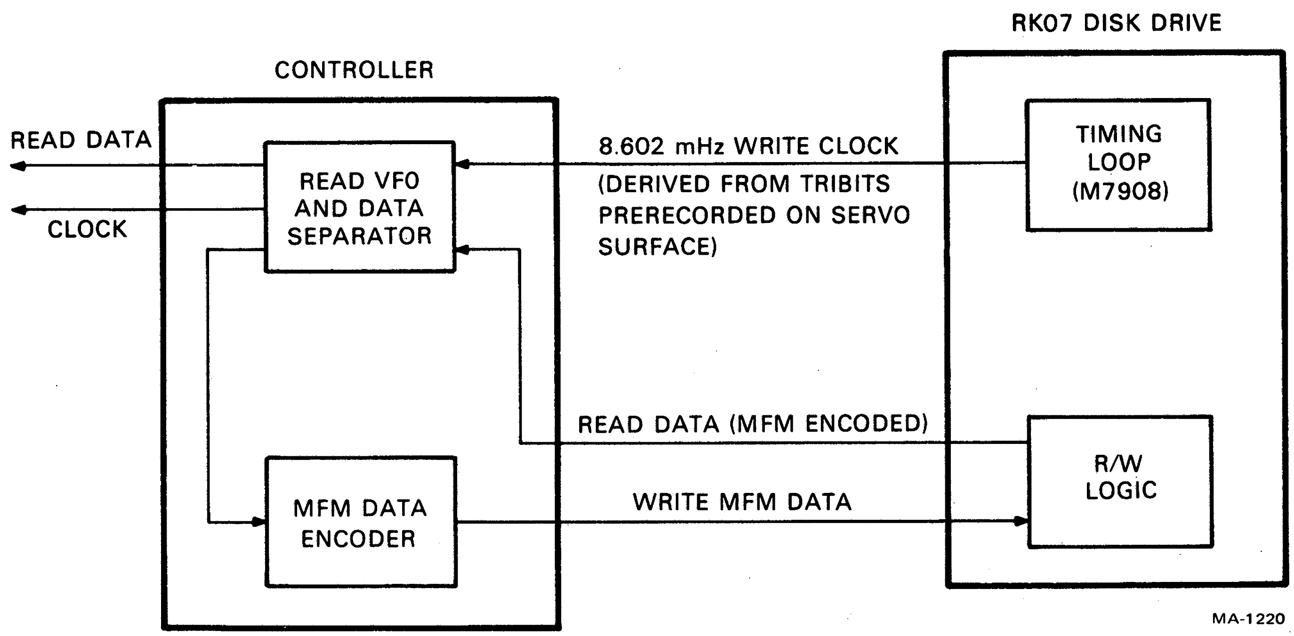


Figure 5-39 Drive/Controller Write Clock Loop

Data Heads

The recording heads contain a center-tapped winding. In writing, a current in one half of the winding creates a magnetic gap field of one polarity, while a similar current in the other half of the winding creates a field of opposite sign. In recording data, current is periodically switched between the two halves of the head winding.

In reading, a differential signal is created across the full winding.

Head Selection Circuit
A head is electronically selected by connecting its center tap to ground potential through the NPN output transistor of a 75451 integrated circuit element. This establishes the potential at the common connection of the head selection diodes, at less than +1 V. Unselected head center taps return to a potential of approximately +23 V, effectively open circuiting the associated selection diodes.

5.4.1 Write Circuits
The RK07 write circuits are designed so that:

1. Current switching in each read/write head is as rapid as possible within the limitations posed by circuit constants.
2. The current level in the heads is not measurably affected by variations in power supply voltages.
3. Write current level is selectable over a range of seven values so as to optimize recording efficiency over the full range of head radial positions.

5.4.1.1 Write Drivers – Figure 5-40 is a simplified schematic of the circuits used in controlling write current to the heads. A pair of transistors (Q2 and Q3) are connected so as to appear as current sources for the head. To ensure high-speed complementary switching of these transistors, a set/reset flip-flop (E2) is direct-coupled to their bases. E2 is powered from a floating supply created by emitter follower Q1 and a zener diode, D2.

The operation of write gating depends upon control of the base-current return path for Q2 and Q3. This return is provided by R2 via open-collector inverter E3. In the absence of a Write Gate and a negative return path, the bases of Q2 and Q3 return to +25 V, thus preventing collector current flow. Write Gate assertion turns on E3, thereby providing power for E2 and the bases of Q2 and Q3.

5.4.1.2 Write Control Circuits – It is necessary to switch write current with each incoming data pulse. To accomplish this function, the incoming pulse train is converted to odd and even pulse trains by a 7473 flip-flop and a pair of 74S00 gates (Figure 5-41). Negative pulses of approximately 55 ns duration at the gate outputs are therefore ac coupled to the inputs of the biasing network, which establishes a base for the pulses of approximately +2.5 V, referenced to the E2–V_{CC} level.

5.4.1.3 Current Level Control – There is an optimum value of write current for each radial (cylinder) position of the heads. A practicable compromise is to use 7 levels of current, as previously mentioned, with each level serving a band of 128 tracks. Although the closed-loop system is described as a current regulator, the actual regulation is that of voltage drop across the emitter return network of Q2 and Q3 (Figure 5-40). If an additional current path from the network is provided, the regulator still holds the same voltage, but the current in Q2 and Q3 is reduced by the amount of the diversion current. This principle is used in providing the desired step reductions of current as a function of head radial position. Figure 5-42 shows such a controlled current source. In this figure, E1 and Q1 are configured in a unity-gain arrangement to provide a constant 5.1 V plus one logic-low level at the emitter of Q1. Current in the collector of Q1 becomes a function of the emitter return resistance. The return resistors are selected in binary fashion, such that R1 selects a current of 3 mA, R2 provides 6 mA, and R3 provides 12 mA. The cylinder address bits (from the cylinder address register on the M7907 module) supply a selection code such that the maximum outer-band current of 65 mA is reduced in increments of 3 mA at 128-track intervals. Thus, inner-band current is 45 mA. Note that all these currents are zero-to-peak values.

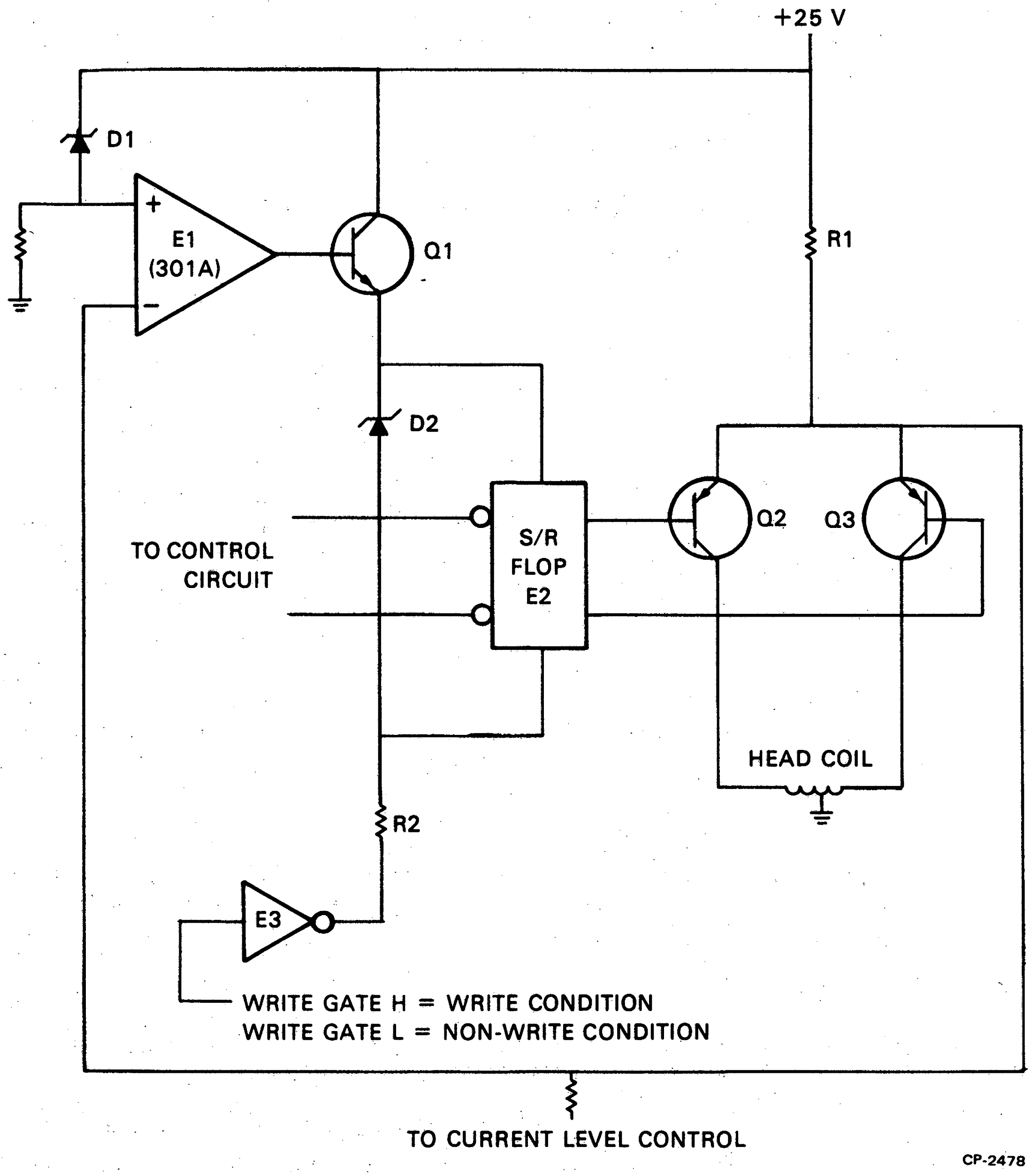


Figure 5-40 Simplified Write Drivers Schematic

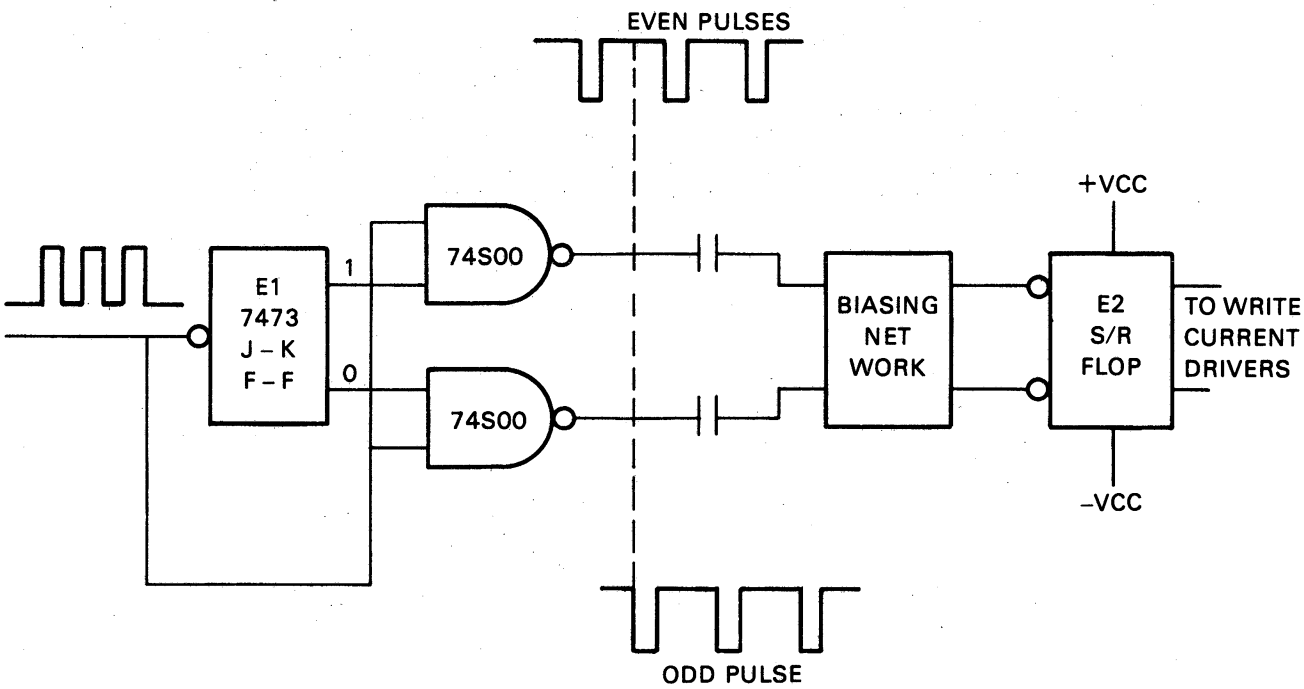


Figure 5-41 Simplified Write Control Circuit Schematic

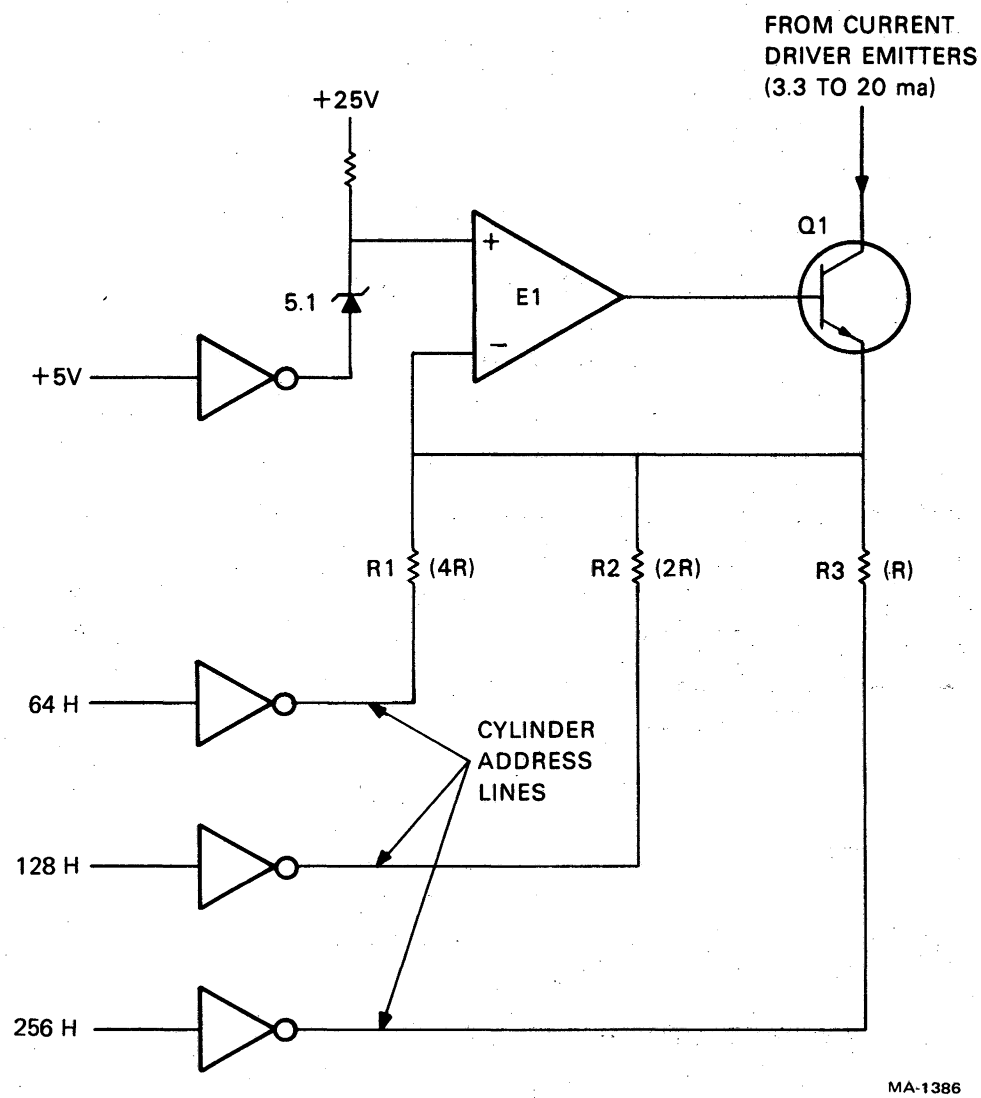


Figure 5-42 Current Level Control Schematic

5.4.2 Isolation Network

A resistor-diode network is connected between the read/write, head selection bus, and the read preamplifier. This network serves two purposes.

1. It isolates and protects the preamplifier from the large voltages generated during writing.
2. It prevents the preamplifier input from loading the head during writing.

5.4.3 Read Circuits

The read circuits (Figure 5-43) comprise an analog (linear) section and a digital section.

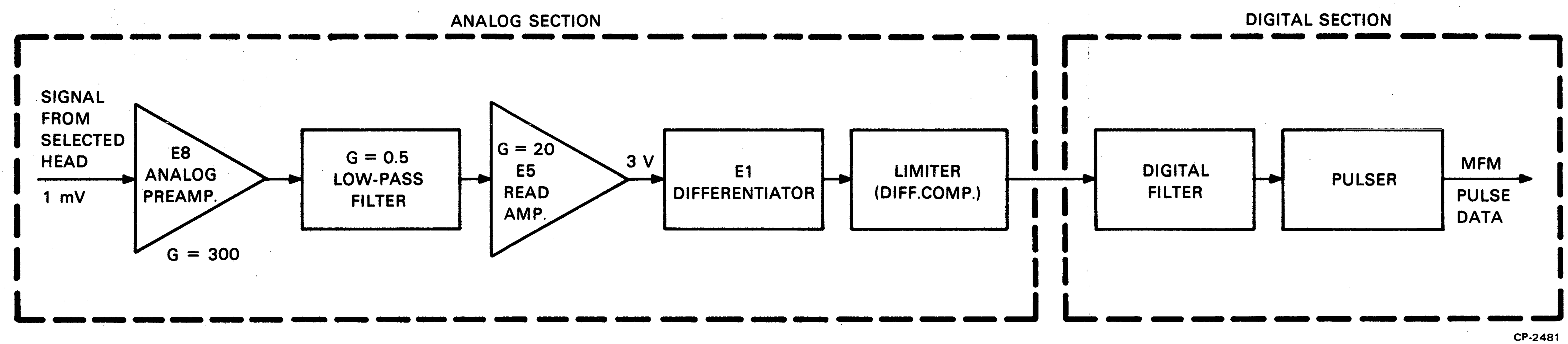


Figure 5-43 Block Diagram of Read Signal Circuits

5.4.3.1 Analog Section

Preamplifier, Filter, and Amplifier
The analog portion of the read/write circuitry comprises:

1. A preamplifier having a gain of 300 for the low-level Input signal from the selected head
2. A low-pass filter with a 6 MHz, 3 dB cutoff and an insertion loss of 0.5 (the filter is used to remove high frequency noise)
3. A second amplifier with a gain of 20.

Differentiator-Limiter (Peak Detector)
The delay line differentiator operates on the principle illustrated in Figure 5-44. The read pulse response to a single flux transition is shown delayed with respect to itself (A, B). By subtracting (A–B), the waveform of C is developed, and the peak of A is converted to a zero-voltage crossing. The same operation performed on the contiguous Pulse Read signals similarly converts each peak to a zero-voltage crossing. Figure 5-45 exemplifies this process.

In the RK07, a balanced network (Figure 5-46) is used with the delay line comprising a parallel LC circuit. The required subtraction occurs as a result of a summation of the currents at the differential comparator input at nodes A and B.

The Differential signal is converted to square waveform by comparator E2. Note that a pair of comparator circuits is actually used in order to maintain the desirable noise rejection and balanced delay characteristics of the differential configuration.

5.4.3.2 Digital Section

Digital Filter
The contiguous pulse-recording system of the RK07 is inherently insensitive to various types of noise. However, for certain bit sequences, particularly those with higher resolution heads, the Differentiated signal approaches the zero reference and becomes susceptible to false crossings from noise.

For the most common case of disturbance, where the false zero crossing is of short duration, the RK07 provides means for rejecting the pulse developed from such a crossing.

The basic circuit around which the system is developed is called a one-way integrator and is illustrated in Figure 5-47. The input, A, is such as might be derived from a Disk Read signal. The negative edges are significant. Without capacitor C1, the waveform at B would be simply an inversion of A. The addition of capacitor C1 prevents a rapid rise of voltage since C1 must charge through R1. A sufficiently high supply voltage to R1 is provided to assume linear charging. A differential comparator with reference +V responds when the sawtooth input wave exceeds the threshold; the result is shown in waveform C.

The following is true.

1. The new negative edge generated is delayed from the original transition.
2. Such an edge is developed only if the Input signal is of sufficient duration to permit the sawtooth to cross the comparator threshold. This is illustrated where the circled portion of the Input signal causes no comparator input.

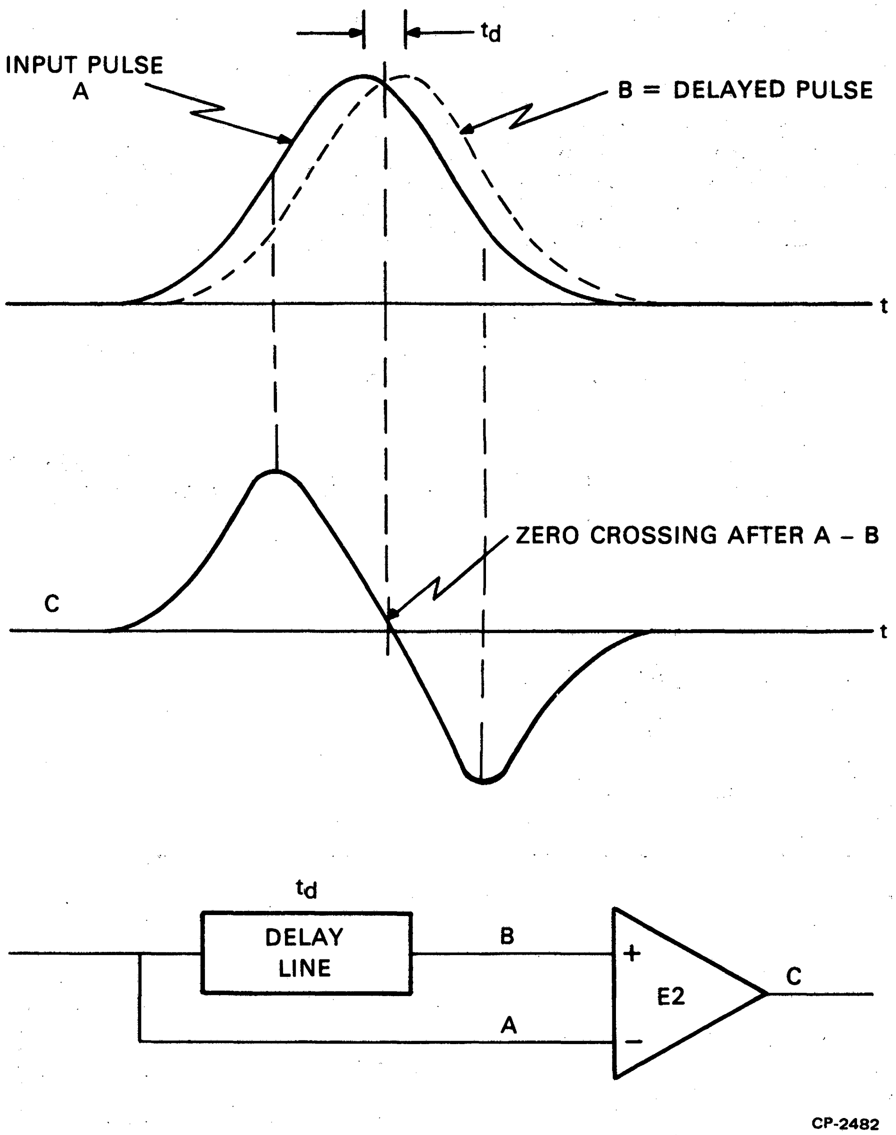


Figure 5-44 Delay Line Differentiation (Simplified)

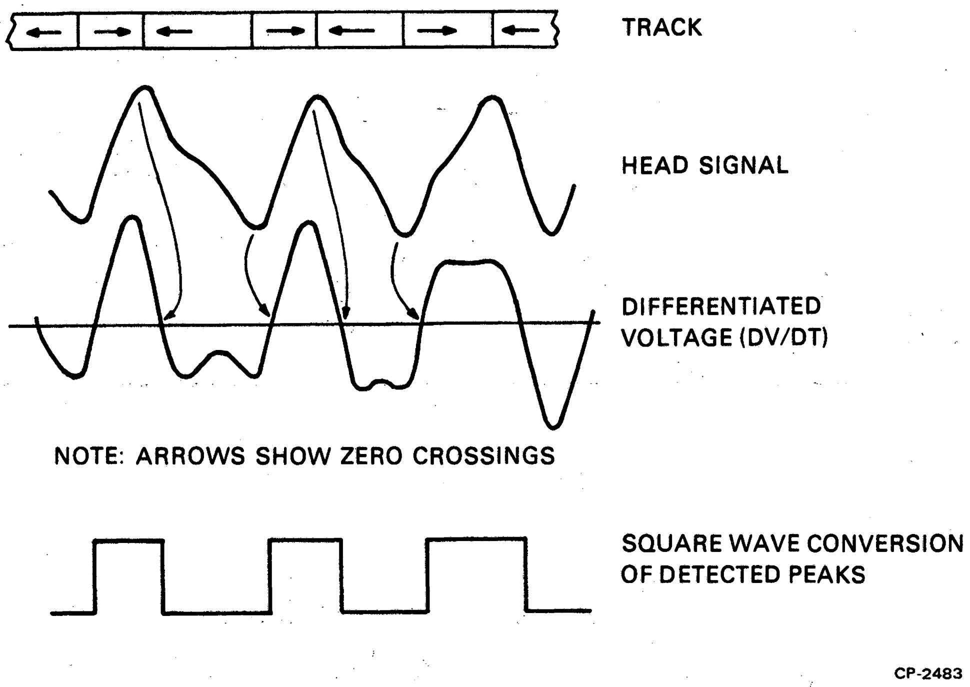


Figure 5-45 Read Signal Differentiation

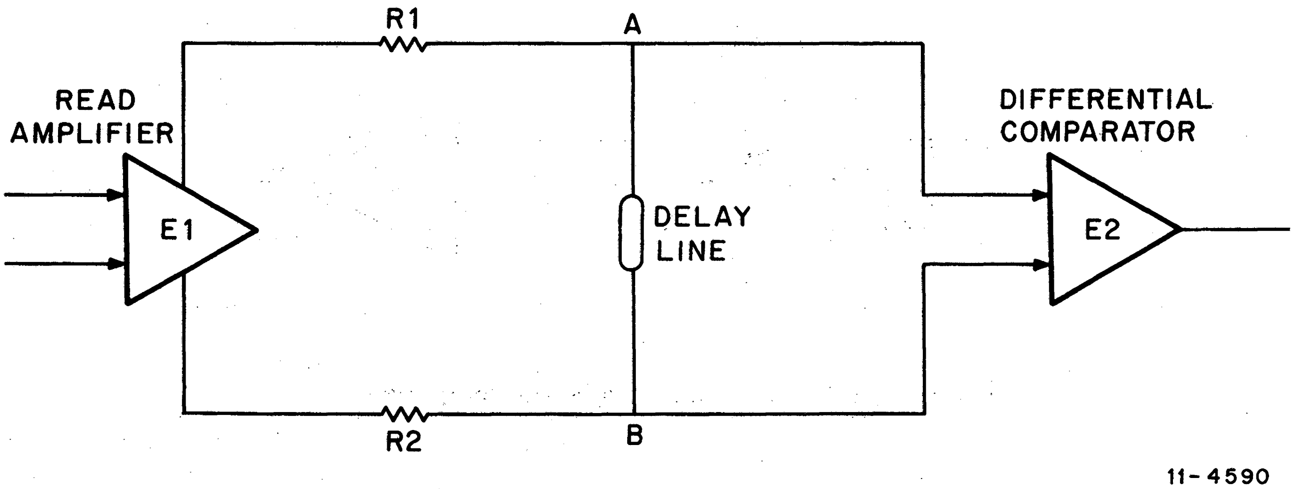


Figure 5-46 Read Signal Differentiation Circuit

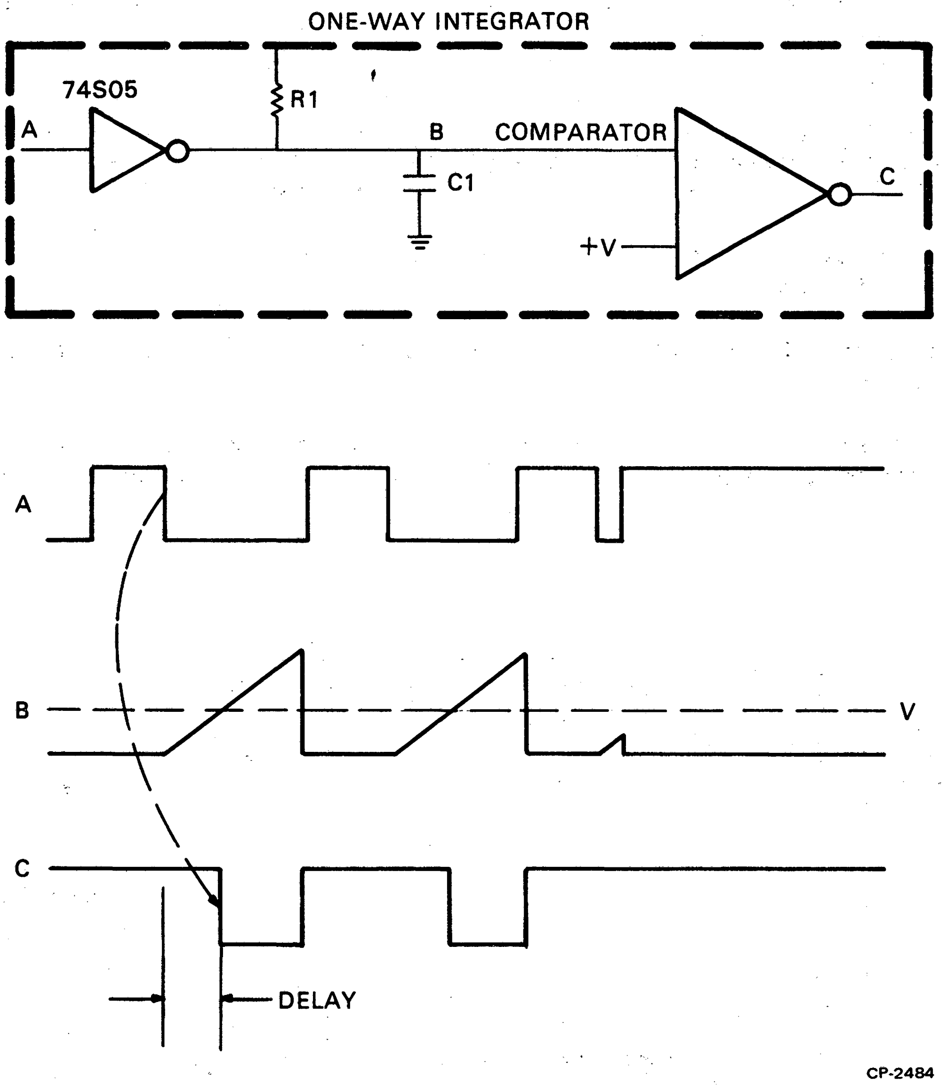


Figure 5-47 One-Way Integrator of Digital Filter

It is obvious that the input waveform has been altered in duration. To reconstruct the original waveform (less false zero crossing pulses), a pair of comparators and integrators are used. The pulses developed from the integrators are used to set and reset a flip-flop. The signal processing is further illustrated in Figure 5-48, a block diagram, with pertinent waveforms denoted in Figure 5-49. The waveforms D and H in Figure 5-49 are not directly observable, being internal to the integrated circuit devices. The flip-flop, which reconstitutes the original signal (less false crossings), is created by cross-coupling of the digital portions of the comparator pair.

Pulser

A final waveshaping operation is required to process the Data signal to a form suitable for transmission via a bus to the controller for detection (data separation). The objective is to convert each voltage transition of the Limited Differentiated signal to a discrete pulse.

Figure 5-50 illustrates the method. A comparator and gate are connected as shown. Waveforms illustrate operation of the circuit.

It should be noted that the exact duration of the output pulse is not important. Only the timing of the leading edge is significant.

The actual circuit is a differential configuration of the simplified version. Odd and even pulse trains are generated. These are combined into a single signal on the M7706 module for transmission to the controller.

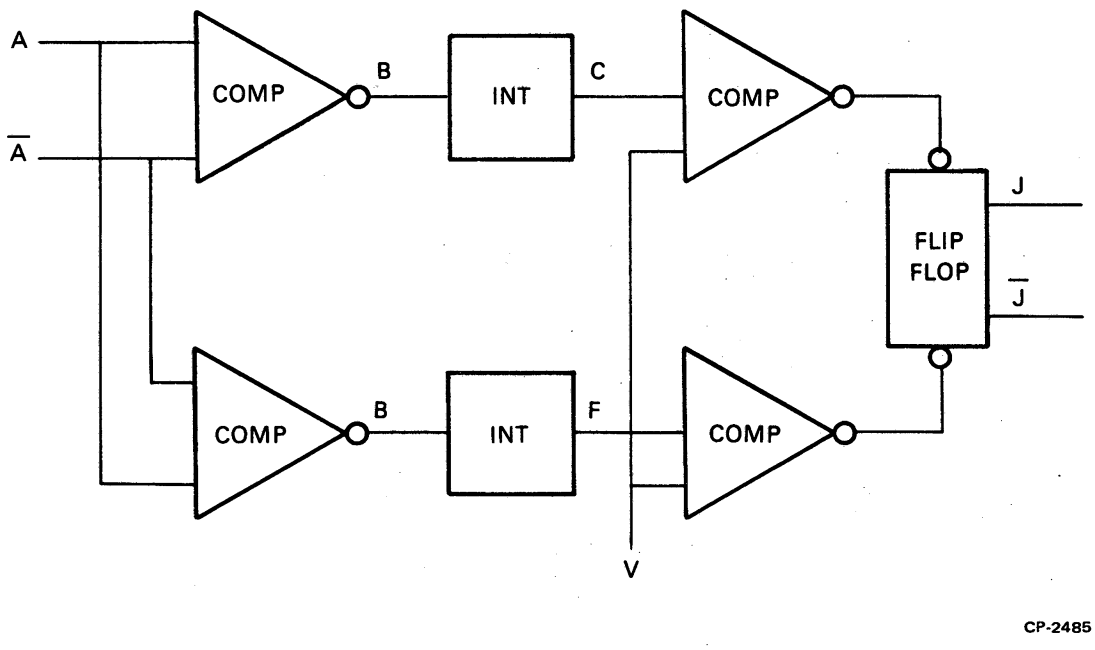


Figure 5-48 Digital Filter Block Diagram

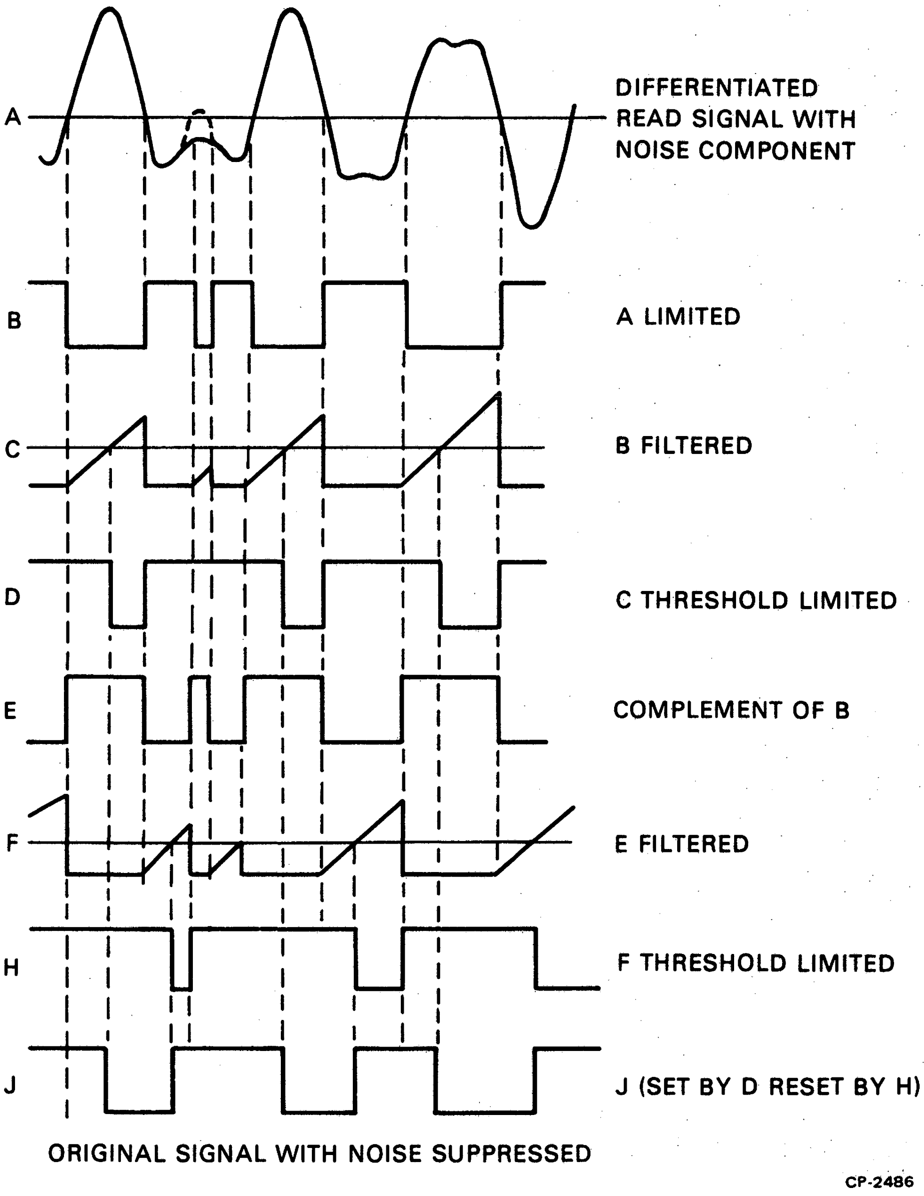


Figure 5-49 Write Current and No Write Gate Waveforms

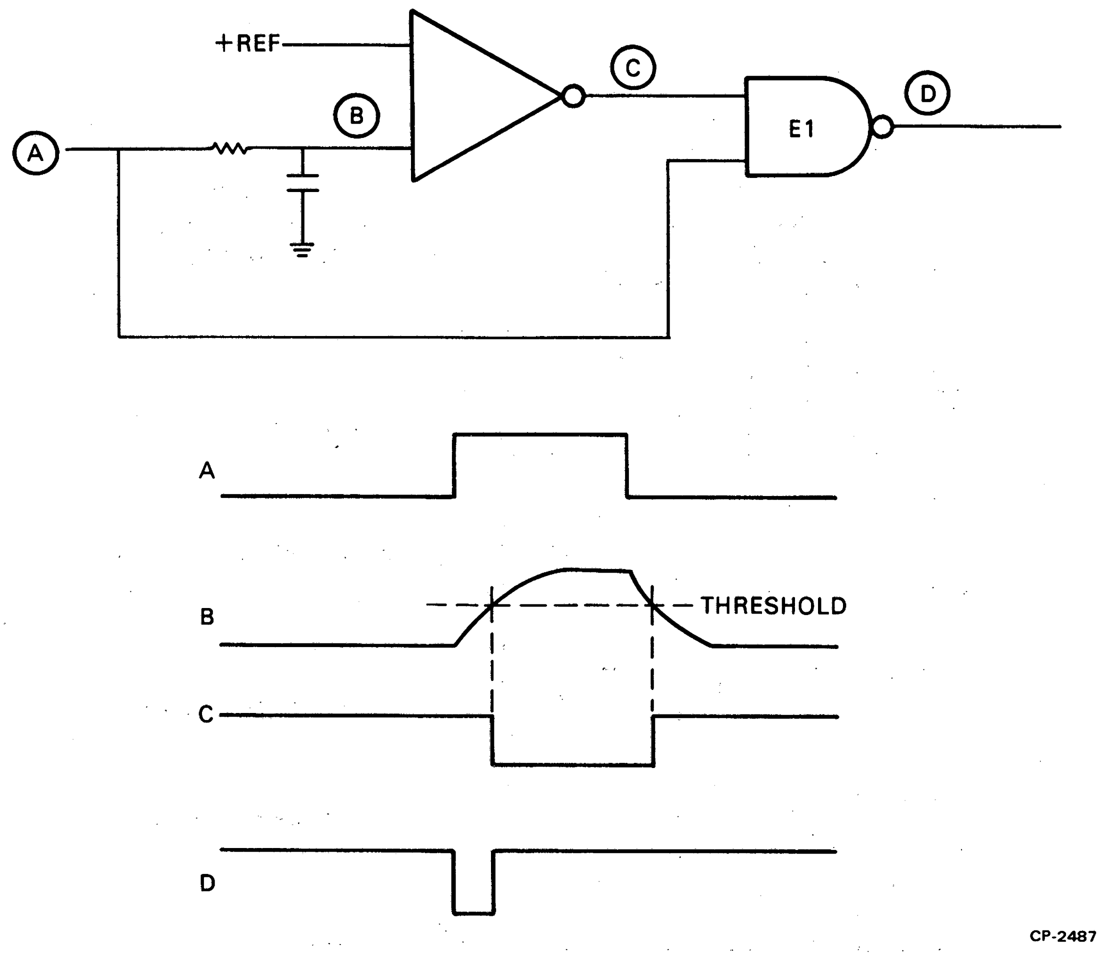


Figure 5-50 Pulse Former (Pulser) for Read Output

5.4.4 Fault Detection Circuits

The read/write fault protection is provided to safeguard disk information against accidental overwrite or erasure due to a read/write circuit failure. Four discrete error conditions are tested for and the results reported to the drive error registers.

5.4.4.1 Write Current and No Write Gate – This signal indicates that write current exits even though not requested. This condition is caused by a write circuit failure and may result in a dc erasure.

In the schematic of Figure 5-51, transistor Q1 is normally non-conducting during a non-write condition. Any current flow from the write drivers will cause base current in this transistor. Conduction of its collector presents a logic low input to the following gate, E1, which is enabled when not writing, permitting a fault condition to be indicated at the output.

The filter (R1 and C1) prevents any false indications during the turn-off of a write operation.

5.4.4.2 Multiple Head Selection – As shown in Figure 5-52, if a single head is selected, the base of Q1 connects to a voltage divider comprising a 287 Ω resistor (R1) and one of three 5.11 kΩ resistors (R2, R3, and R4) spanning +25 V. The emitter of Q1 connects to an identical divider (R1 and R6) and the same voltage. Q1 does not conduct.

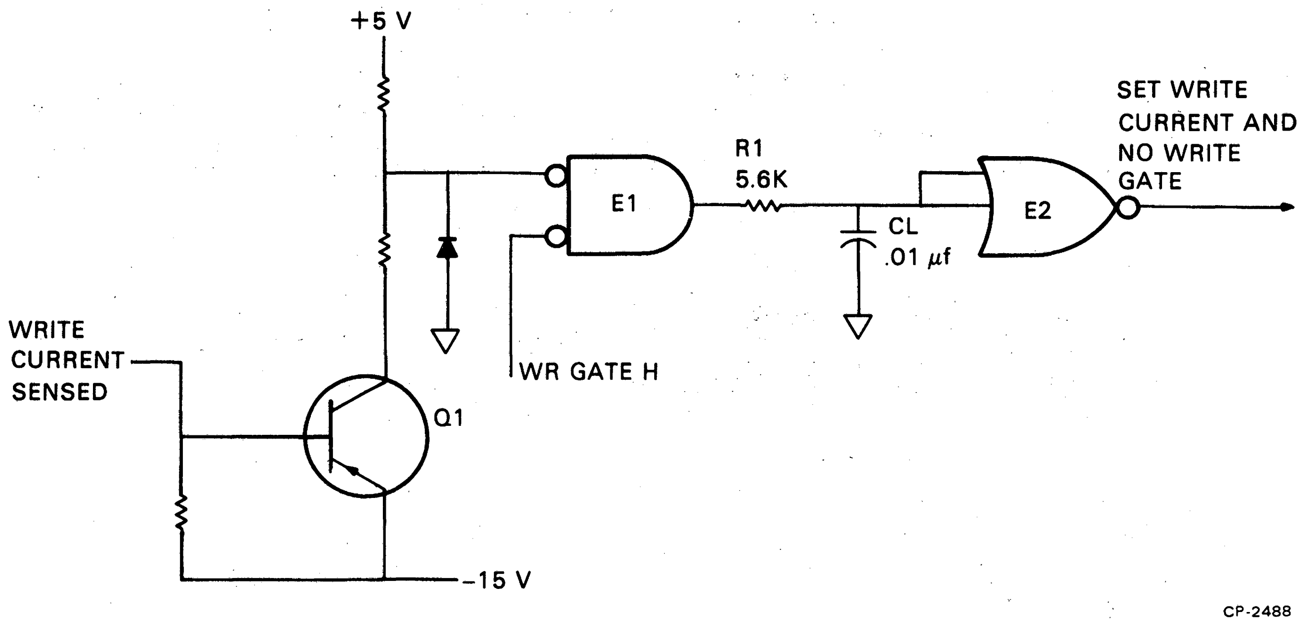


Figure 5-51 Write Current and No Write Gate Schematic

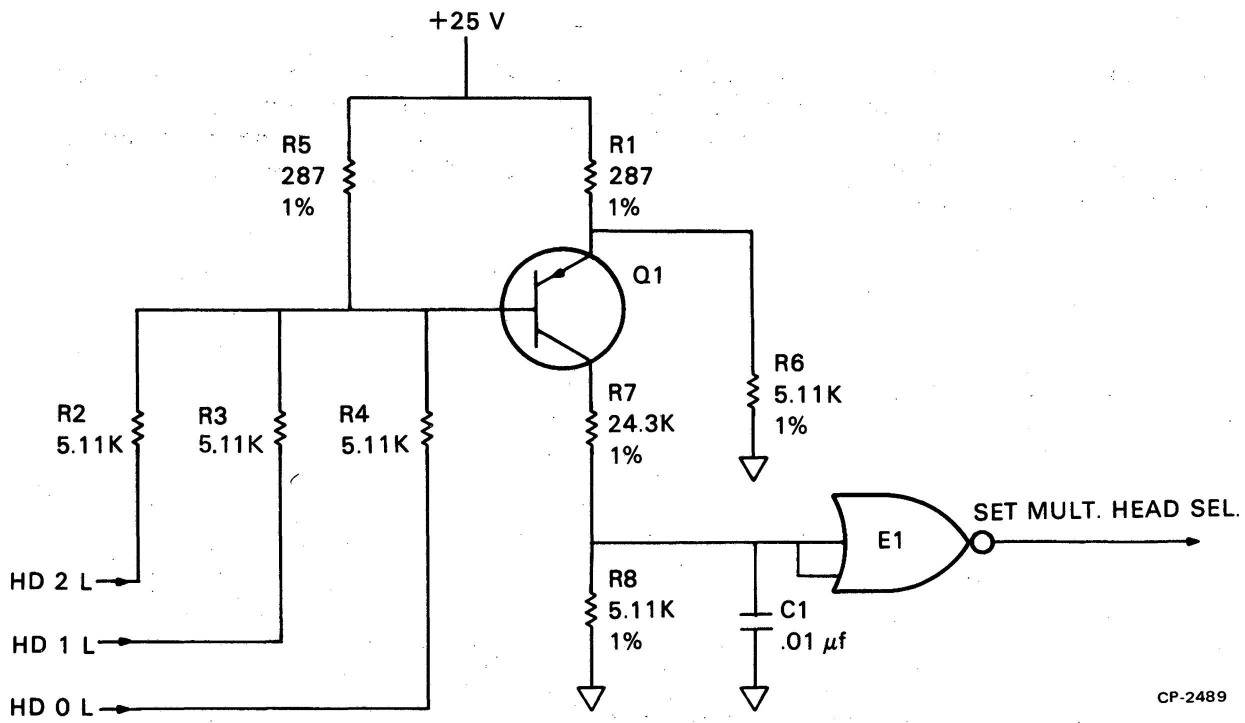


Figure 5-52 Multiple Head Selection Schematic

If additional heads are selected, additional 5.11 kΩ resistors provide base current to Q1 and transistor conduction activates the following E1 inverter to generate a fault-indication output.

5.4.4.3 Write Gate and No Transitions – Figure 5-53 is a schematic for this fault circuit. In the absence of WR GATE, the first gate is not enabled, so that no fault indication is detected even though E3 is held in the reset state. When WR GATE is asserted, the reset is removed from E3, and the gate, E1, is activated. If no WT DATA pulse appears to set E3 within the delay time of filter, C1 and R1, a fault is noted.

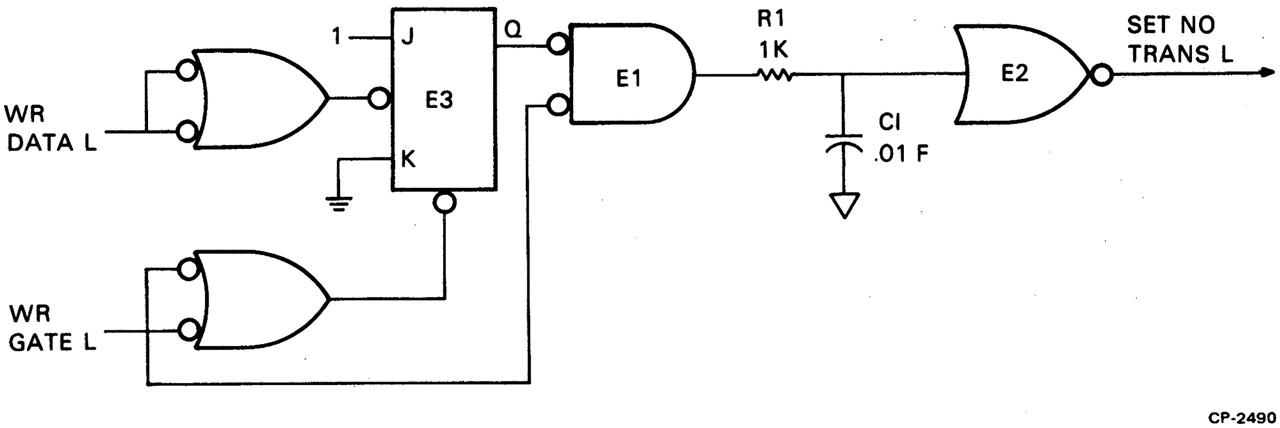


Figure 5-53 Write Gate and No Transitions Schematic

5.4.4.4 Head Fault – Figure 5-54 is a schematic of the head-fault circuit. Under normal conditions the input to E1 is normally dc balanced to within a few millivolts, and the E1 outputs reside at about +3.5 V. Any input imbalance, such as from an open head or faulty component, causes E1 to saturate with one output moving close to the ground potential. This is detected in the logic structure of E2 to create the fault indication at the output.

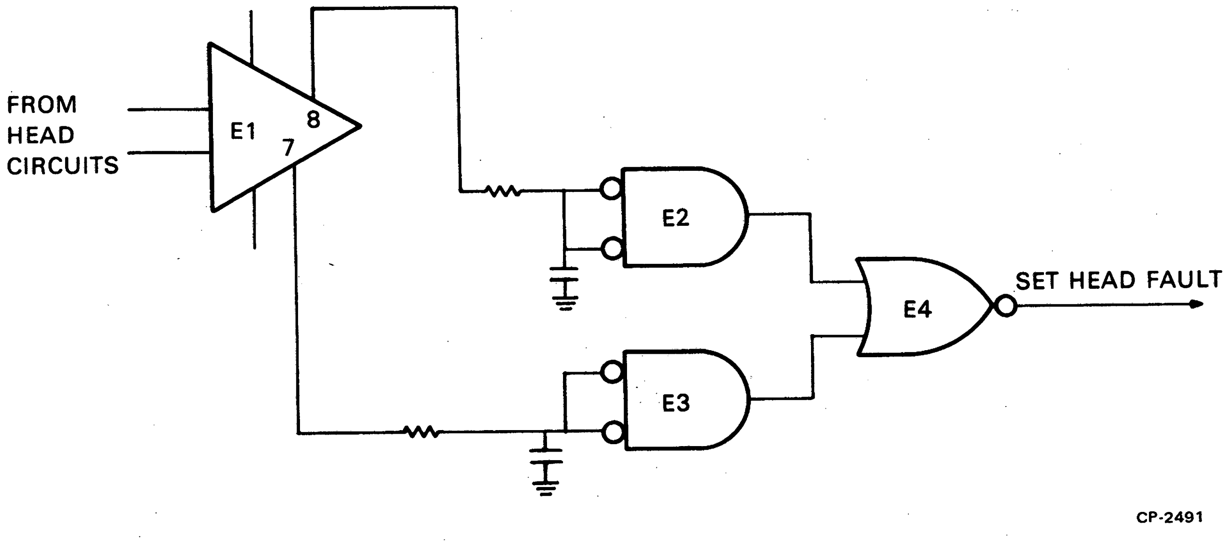


Figure 5-54 Head Fault Schematic

5.5 AIR SUPPLY AND DISTRIBUTION SUBSYSTEM

Figure 5-55 is the disk drive functional block diagram with the air supply and distribution subsystem shaded.

5.5.1 Filtration

There are two air-filtering stages within the drive: a prefilter and an absolute filter (Figure 5-56).

5.5.1.1 Prefilter – This filter is a foam type that prevents the larger airborne particles from entering the drive, thereby lengthening the replacement intervals of the absolute filter and preventing dust buildup within the drive.

5.5.1.2 Absolute Filter – This filter is a self-contained replaceable type that removes 99.999 percent of all airborne particulants of 0.3 μm and larger from the air supplied to the cartridge. This clean air prevents disk deterioration due to foreign particles. It also provides cooling air and minimizes temperature variations of the cartridge.

5.5.2 Blower

The dual-impeller blower provides forced air for cooling of the electronics within the drive, and the purge air necessary to maintain a clean, temperature-stable environment within the cartridge. The blower is designed to provide 330.4 m^3/min (70 ft^3/min) at 1.9 cm (3/4 inch) of water to the subchassis ducting (for electronics cooling) and 118 m^3/min (25 ft^3/min) at 5.08 cm (2 inches) of water through the absolute filter to the cartridge (purge air).

5.5.3 Ducting

The forced air is routed through hoses, for the cartridge purge air, and the chassis plenum, for the electronics and power supply/power amplifier cooling air. Due to cooling requirements, the bellows connected to the power supply chassis provides cooling air to the heat sink and components of the power supply/power amplifier module when the module is in the normal (operating) position and when it is pivoted downward for maintenance. Air deflectors at the top of the electronics chassis and power supply chassis are positioned to divert exhaust air through ports at the rear of the drive.

5.5.4 Operational Description

The blower operates whenever ac power is on within the RK07. The blower intakes ambient air through the front of the drive (Figure 5-56) through the prefilter and exhausts into the absolute filter and the subchassis plenum. The air passing through the absolute filter continues through the shroud intake and into the cartridge through a port in the side of the bottom cover. This air exhausts through the access hole for heads and the cartridge-cleaning brushes into the chassis. The positive air flow through the cartridge prevents contaminants from entering the cartridge via the head and brushes access holes. The cooling air, passing through the subchassis plenum, exhausts into the electronics and power supply chassis. After picking up the heat generated from the components, the air is deflected rearward and exits the drive through rectangular ports in the back cover.

5.6 POWER SUPPLY SUBASSEMBLY

The power supply subassembly is shown by the shaded blocks of Figure 5-57, the RK07 functional block diagram. The power supply subassembly contains the functional groupings discussed in the following paragraphs of this section. The relationships of these groups can be seen in the functional block diagram of Figure 5-57.

5.6.1 AC Input Assembly

This assembly receives the ac input power through a line cord. The presence of this power is indicated by a red lamp (lighted) at the rear of the drive. The circuit breaker of this assembly controls the distribution of the input power and, when on, applies power to the constant voltage transformer (CVT), blower motor, power supply capacitor module, and spindle brake power supply. A line filter within the AC input assembly prevents unwanted noise spikes on the input power from adversely affecting the operation of the disk drive.

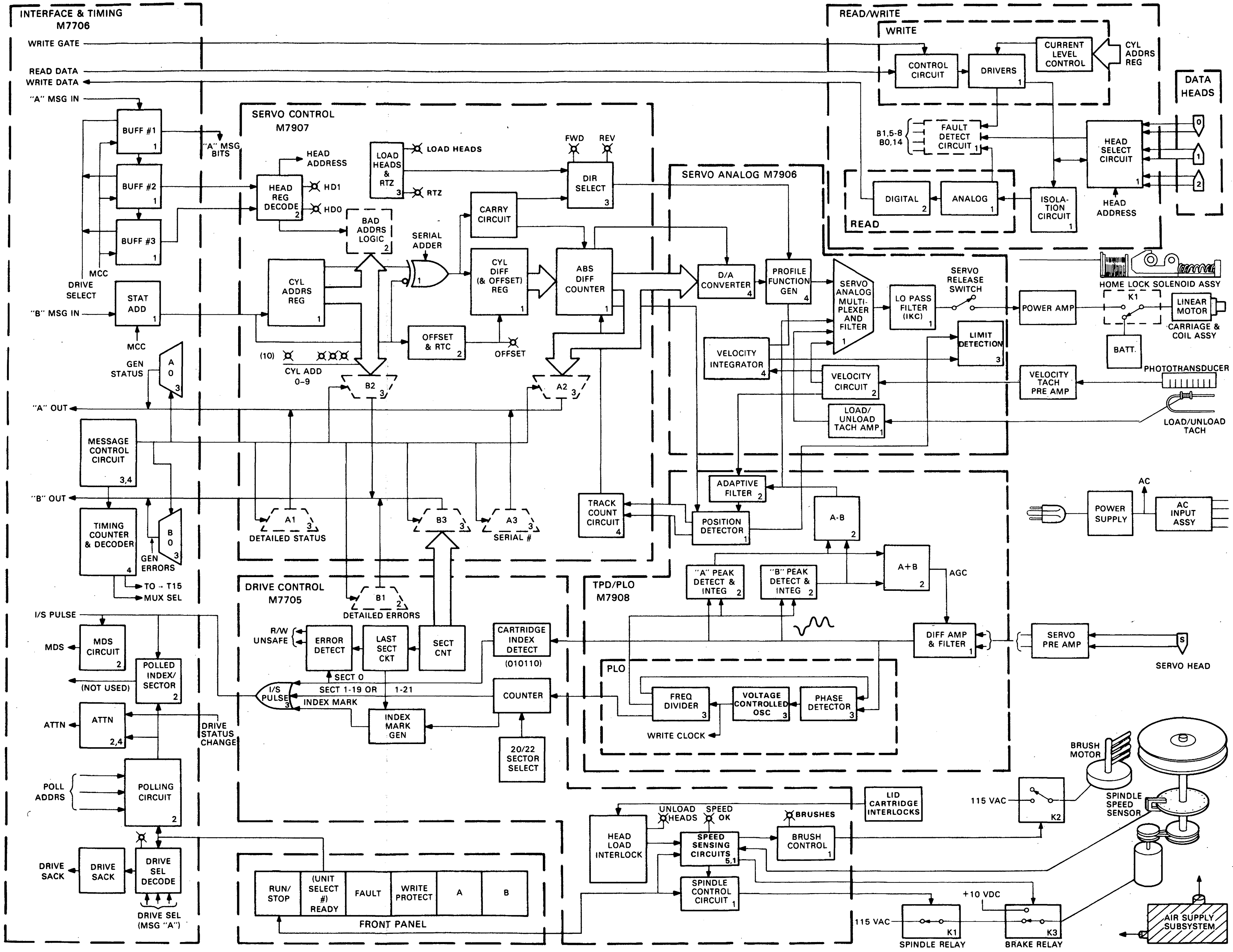


Figure 5-55 RK07 Disk Drive
Functional Block Diagram
with Air Supply and Distribution Subsystem Shaded

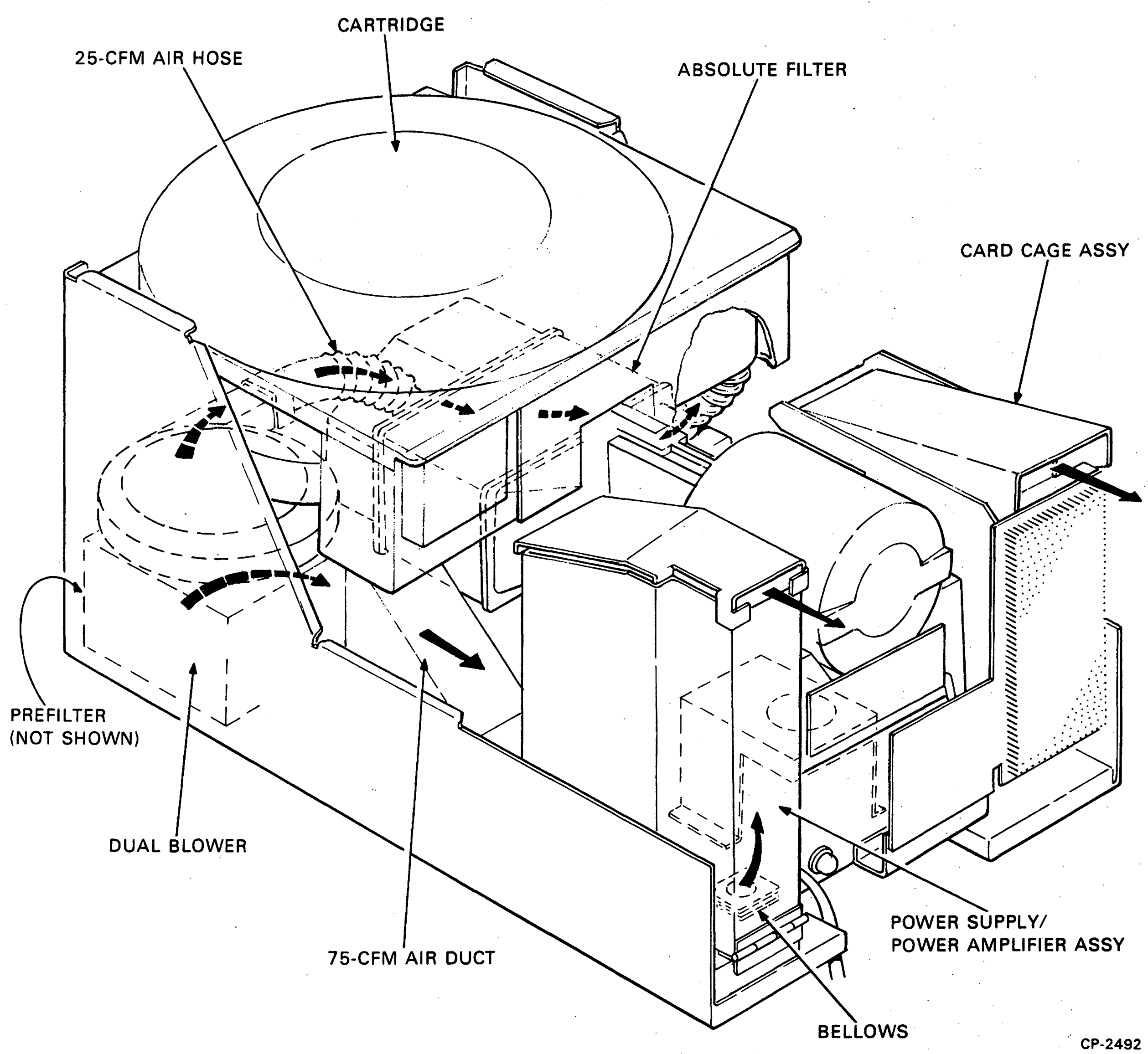


Figure 5-56 Air Supply and Distribution Subsystem

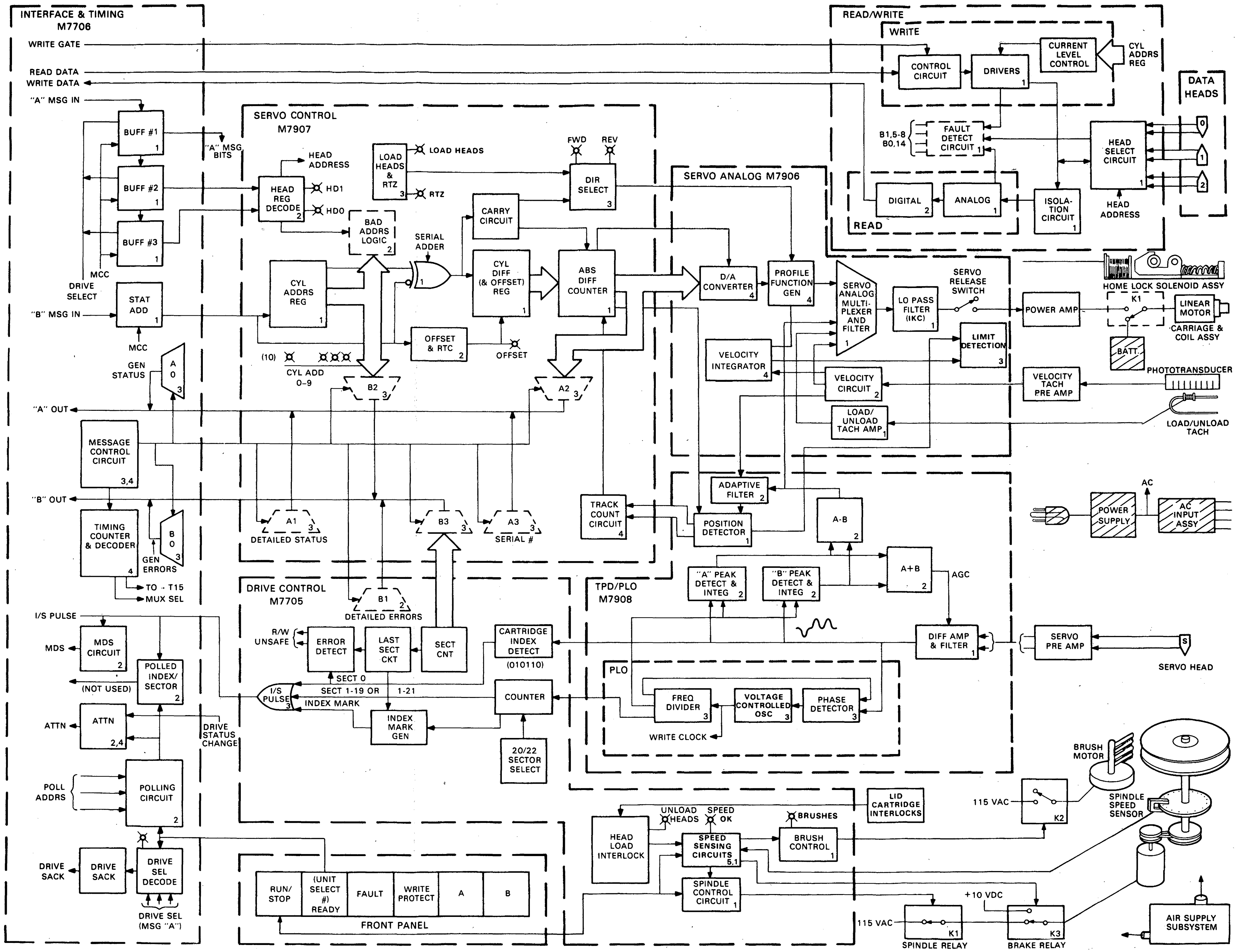


Figure 5-57 RK07 Disk Drive
Functional Block Diagram
with Power Supply Subsystem Shaded

5.6.2 Constant Voltage Transformer (CVT)

The CVT supplies 13 Vac and 37 Vac to the power supply modules. A matched capacitor connected to the CVT maintains these output voltages over the full operating voltage range of the RK07, in spite of the fluctuations of the input power.

5.6.3 Rectifiers, 10 Vdc and 25 Vdc

These full-wave rectifiers produce plus and minus voltages for the regulators on the power supply module, ± 10 Vdc for the ± 5 V regulators and ± 25 Vdc for the ± 15 V regulators. The +25 Vdc is also used to energize relays, as the current source for the write current, and for the linear motor.

5.6.4 Relays

The relays located on the capacitor module route power to the motors within the RK07 (except the blower motor). Relay K1, when energized, energizes the spindle motor whenever relay K3 is deenergized. When K1 is deenergized, the spindle motor is deenergized. Relay K2 applies power to the brush motor when energized, and removes it when deenergized. The third relay, K3, routes ac input power to the spindle motor when deenergized and the brake power supply when energized. The controls for these relays are discussed in Paragraph 5.2 (Drive Control Subsystem).

5.6.5 Regulators, ± 5 Vac and ± 15 Vdc

The linear regulators supplying the ± 5 Vdc and the ± 15 Vdc are similar in design. The block diagram of Figure 5-58 represents these regulators. The feedback circuit maintains the output voltage at the prescribed level over various load conditions. The current limiting is employed when a short circuit condition arises in the circuitry supplied by the regulator. When this condition happens, the current limiting transistor is turned on, dropping the output voltage to about 0.2 Vdc, and remains turned on as long as the condition is present. This current limiting feature is present to protect the circuitry supplied. The +15 Vdc regulator also produces two zener-diode-regulated +5.1 Vdc reference voltages for use in the feedback circuits and power low circuits of the power supply. The +5 Vdc regulator also has overvoltage protection provided. When an overvoltage condition is detected, approximately 5.7 Vdc on the output, an XA55 transistor is turned on, which in turn fires the SCR "crowbar," bringing the output voltage to the current limited value of about +0.2 Vdc. This SCR will remain conducting until the overvoltage condition is no longer present and power is removed and reapplied.

5.6.6 Spindle Brake Power Supply

This supply consists of a transformer and a rectifier, the output of which is approximately 11.5 Vdc. This dc voltage is used to decelerate the spindle motor when relay K3 on the capacitor module is energized. The spindle speed-sensing circuit will remove the braking current when the spindle is determined to be stopped.

5.6.7 Battery Supply

The 8-cell nickel-cadmium battery supply is for use in emergency retraction of heads to the home position under servo unsafe and power fail conditions. Each of the series-wired cells delivers a nominal 1.2 Vdc, for a total of 9.6 Vdc. The battery supply will apply this voltage to the linear motor when relay K1 on the capacitor module is deenergized and the heads are loaded to the home position. Under normal operating conditions, the battery is under a continuous trickle charge from the plus and minus 15 Vdc regulators.

5.6.8 Power-Low Detection

The power-low detection circuitry monitors the ac input power and the output of the regulators for low voltage conditions that may cause erratic drive operation, component failure, or loss of data on the data cartridge.

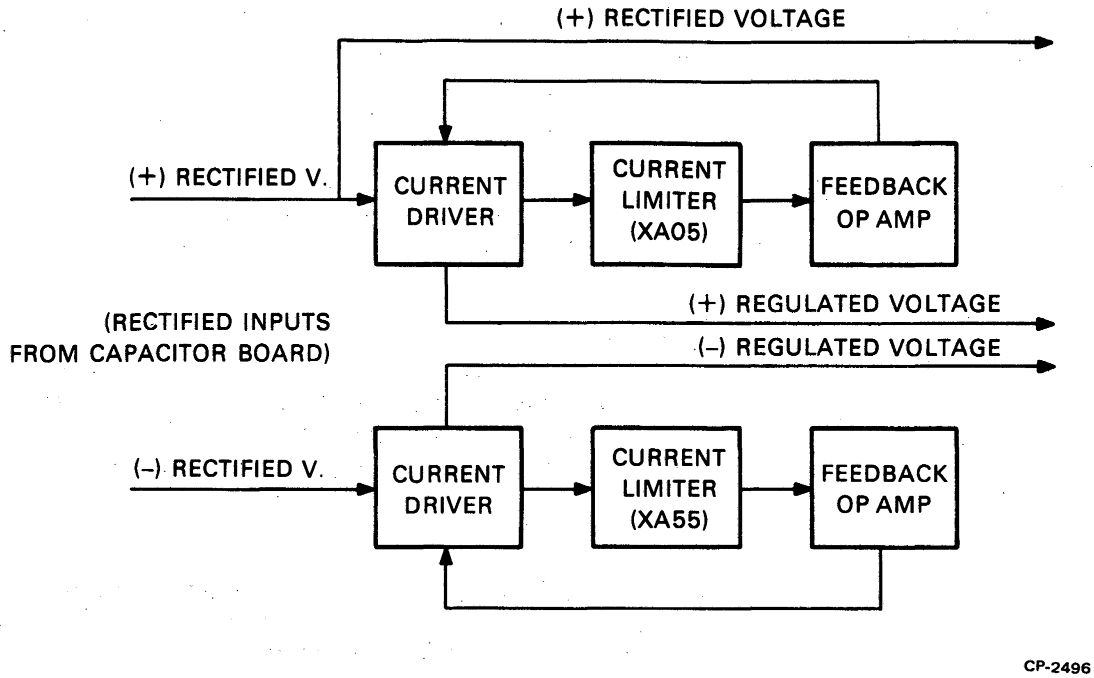


Figure 5-58 Electronics Board – Regulated +15 Vdc and Unregulated 25 Vdc Supplies

5.6.8.1 AC Low – During normal drive operation, an 18 ms one-shot is set by the presence of the 13 Vac from the CVT. If the ac voltage is missing or the voltage level is below specifications (approximately 85 Vac), the one-shot will time-out, generating the AC Low signal. After AC Low is generated, the drive continues to operate until the next sector pulse occurs, thus ensuring that any data transfer in progress will continue to the end of the sector before the heads are retracted.

5.6.8.2 DC Low – If the +15 Vdc or the –15 Vdc drops below 12 V, or if the +5 Vdc reference voltage drops below 4.6 V, DC Low is generated and the FET conducts, thereby asserting DC Low with a low impedance to ground. This signal is used to shut off interface transmitters so that the interface is not disturbed when voltages are low within the drive. This signal is also one of the drive interlocks for preventing undesired head loading if all the dc voltages are not proper.

5.7 CARTRIDGE HANDLING SUBSYSTEM
Figure 5-59 is the RK07 functional block diagram with the cartridge handling subsystem shaded.

5.7.1 Spindle Assembly
The Spindle Assembly provides the mounting surface for the cartridge and consists of the following.

- A spindle cone, which provides accurate rapid positioning of the cartridge with respect to the rotational centerline of the spindle
- A magnetic ring, which pulls down and holds the disk firmly against the horizontal spindle hub
- Precision bearings, which provide an accurate rotational assembly with minimum dynamic runout and a long rotational life

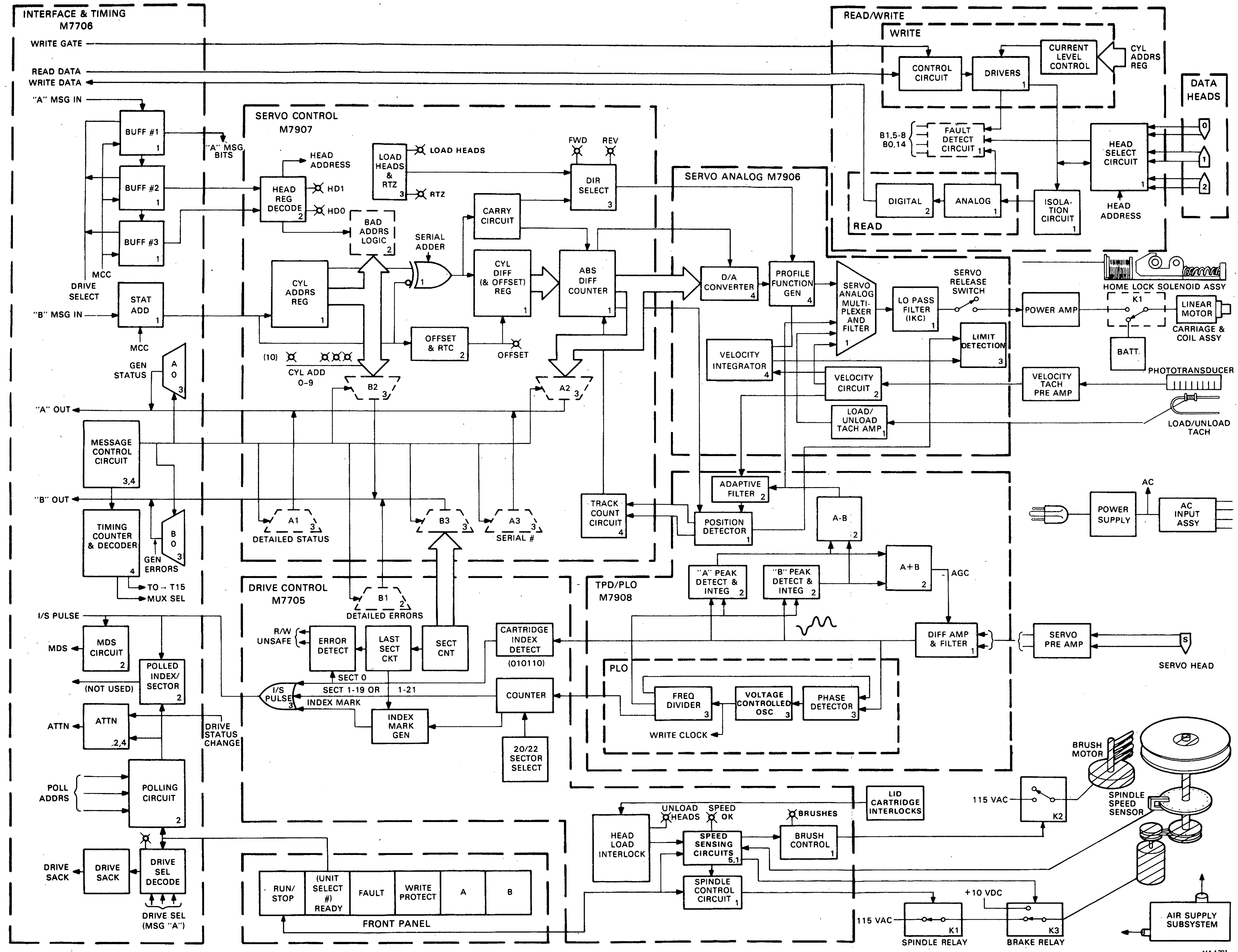


Figure 5-59 RK07 Disk Drive Functional Block Diagram with Cartridge Handling Subsystem Shaded

- Speed-sensing disk, with 12 slots on the outer rim allowing the LED/photosensor pair to output a pulse rate proportional to the rotational speed of the spindle

- A spring-tensioned ground button, in contact with the spindle shaft, that decouples any static electric charges that may build up on the disk and might possibly destroy the recorded data

- Spindle pulley, which provides coupling to the drive motor via the drive belt

5.7.2 Spindle Drive Motor and Belt
The disks of a cartridge assembly are rotated at a speed of 2400 rev/min by means of a single-phase, permanent-capacitor drive motor that is coupled to the spindle through a crowned pulley and a spring-tensioned belt. The shock-mounted spindle motor also functions as a dynamic brake for stopping disk rotation. To prevent the motor from possible overheating, it contains an auto reset thermal circuit breaker.

5.7.3 Brush Assembly
The brush assembly, driven by the 2 rev/min brush motor, swings inside the cartridge during the spindle-starting sequence to clean the four disk surfaces. This aids in removing any foreign particles from the cartridge, thereby reducing the probability of head/cartridge contact. A knob is provided to manually retract the brushes from the cartridge in the event of a malfunction or power failure.

5.7.4 Operational Sequence
See Paragraph 5.2.2.1 for the drive startup sequence.

5.8 DUAL-ACCESS OPTION
The RK07 dual-access option enables the physical connection of this drive in two daisy-chain buses originating at two controllers (Figure 2-1). The controllers may be connected to different processors.

For the dual-access option, the drive houses two additional modules, an M7730 dual-port board and an M7706 interface and timing module. The two interface and timing modules interface with each controller. The dual-port board contains logic for controlling the access from both ports and acts as a multiplexer for commands and timing from each port to the remainder of the drive electronics. The dual-access option also uses a different backplane than the single-access option. See Figure 5-60 for the dual-access option block diagram.

5.8.1 Dual-Access Logic Circuits
The logic for the dual-access option is located on the M7730 module and consists of:

1. Arbitration Circuits
2. Timing Counters and Decoders
3. Auto-Release Timer
4. Multiplexers.

5.8.1.1 Arbitration Circuits – These circuits determine and control the state of the multiplexers for operating the drive through the two ports.

5.8.1.2 Timing Counters and Decoders – These circuits control the timing of transmissions from the controller that has seized the drive.

5.8.1.3 Auto-Release Timer – This timing circuit generates a signal that will automatically release a port if it has not been utilized within a 1 second period after it has gained access. See Paragraph 5.8.2.4.

5.8.1.4 Multiplexers – These circuits act as a single-pole, double-throw switch for each signal used by a port for operation of the remainder of the drive.

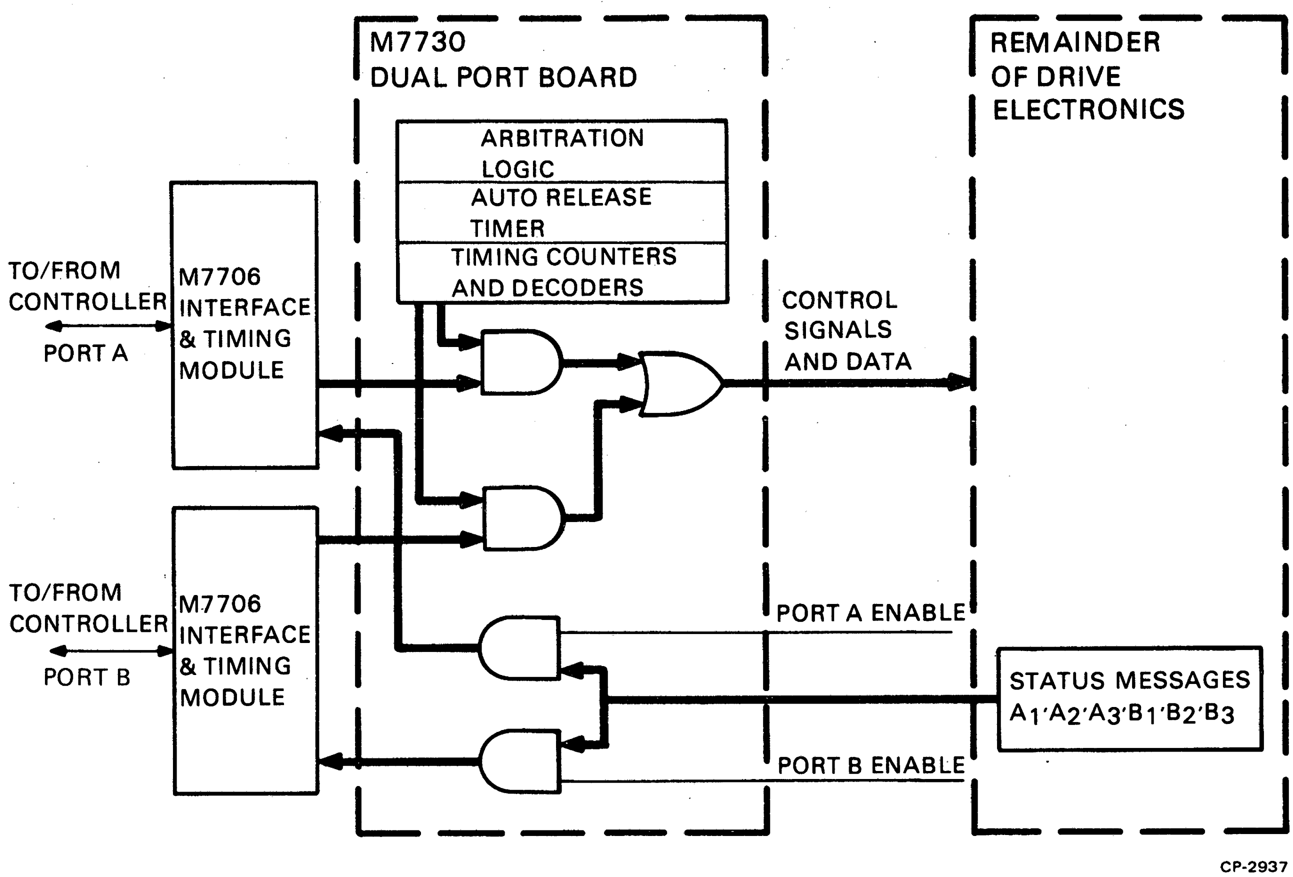


Figure 5-60 Dual-Access Option Block Diagram

5.8.2 Dual-Access Operation

5.8.2.1 Seizing the Drive from the Neutral State – When the RK07 is in the neutral state, it is equally available to each port. There is no logic for priorities in the RK07 drive.

Any controller selecting the drive will cause the RK07 to switch to that port.

If the two controllers simultaneously attempt to seize the drive, a high-speed clock internal to the dual-port logic in the drive will arbitrate and one of the controllers will seize the drive.

5.8.2.2 Attempting to Seize an Unavailable Drive – If a neutral drive is seized by a port and the other port attempts to seize the drive, the latter port will find the drive unavailable. This will set the combined error bit in control and status register 1 (bit 15 in RKCS1). Also, the drive available bit in the drive status register (bit 0 in RKDS) will be cleared as a result of a port attempting to seize an unavailable drive.

In addition to clearing bit 0 in RKDS, a port attempting to seize an unavailable drive will set the port request flip-flop in that drive. The dual-port logic checks the status of this flip-flop when the controller currently operating on the drive releases the drive. If the port request flip-flop is not set, this indicates that the port that was not just in use did not attempt to seize the drive. In this case, the drive then returns to the neutral state and it may then be seized by either port. If, however, the port request flip-flop is set, this means the other port attempted to seize the drive when it was unavailable. In this case, the other port seizes the drive.

For example, assume port A controls the drive. Port B tries to seize the drive and finds it unavailable. Thus, the port request flip-flop is set. When port A is finished with the drive, it releases the drive with a release command. Since the port request flip-flop is set, port B then seizes the drive.

5.8.2.3 Caution in Issuing a Release Command to an Unavailable Drive –The programmer should be careful to avoid the following situation when designing software for use with the dual-access option. Assume port A has seized the drive, and port B attempts to seize in and finds it unavailable. Suppose port B then decides to cancel its port request. If the release command from port B is completed before port A actually releases the drive, there is no problem. If, however, port A releases the drive while port B is still in the process of issuing a release command, the port B controller will find the attention asserted. The assertion of attention should have been prevented by the release of port B. This race condition can be avoided by not allowing a port to release its port request to an unavailable drive.

5.8.2.4 Auto-Release Timer –At the initiation of every command to the drive by the port that has access, a 1 second release timer is started. (The exception to this is the release command.) This timer is restarted with every new command issued by the controller having access to the drive. If a port accessing the drive does not release the drive and the 1 second release timer times out, the other port's port request flip-flop will be examined. If it is reset, the drive will go back to the neutral state. If the other port's port request flip-flop had been set, the following events take place.

1. The drive becomes deselected from the port that had access.

2. The drive is effectively seized by the other port.

3. The other port's attention is asserted, signifying that the drive is now available.

5.8.3 Start/Stop and Write Protect in Dual-Access

When the ac power is first applied to the RK07, the drive is initially in the neutral state. The volume valid bit for each port is cleared. A pack acknowledge command is required for each port.

The drive will not seek or write through a port unless that port has its volume valid bit set.

If a port issues the unload heads command, the 1 second auto-deselect timer is disabled. This has been instituted to allow a change of cartridge and not have the drive return to the programmable state. If the drive were allowed to return to the programmable state after an unload command, the other port could seize the drive and issue a conflicting command.

Once the drive is cycled up, the completion of the head-loading sequence asserts the attention bit of the port having access to the drive. For one additional second, the drive will be seized by that port.

The port having access must issue a command to the drive within this time. Failing to issue a command within this time will cause the dual port logic to examine the other port's port request flip-flop. If the flip-flop is not set, the drive will return to the neutral state. If the flip-flop is set, the drive will become seized by the other port and the other port's attention will be asserted.

If the drive is unavailable to a port and the RUN/STOP switch is changed, the port is notified by the assertion of its attention. The change is reported to the controller through the "spindle on" status bit.

When the write protect is asserted, neither port will be able to do a write operation. There is no provision to write protect the drive through one port and not have it write protect through the other.

If the drive is seized to a port and the operator changes the status of the write protect switch, the other port is notified through the assertion of its attention. The change is reported to the controller through the write lock status bit.

5.8.4 Error Handling in Dual-Access

Notifying the Controller of an Error
Errors occurring while the RK07 is seized by one of the controllers is reported to and should be serviced by that controller. The other port is not notified of these errors. The exception is a parity error in a message to the drive on the other port.

If the drive had been in the neutral state and an error occurred, both attention bits would be asserted. The fault bit would be read by both controllers when servicing the attention set in the drive. However, only one of the controllers would service the error in the drive.

Clearing the Drive Errors and Resetting the Attention
Either controller may issue a drive clear at any time. The attention in the drive will be cleared by a drive clear regardless of the drive's availability. However, to clear the flip-flops storing the error information, the drive must be seized to the port issuing the clear command as mentioned. The controller to drive parity error is handled differently than the other errors and is discussed in greater detail as follows.

Multiple Drive Select and CTD Parity Errors in the Dual-Access Configuration
If a controller has seized a drive and multiple drive select is detected in the drive, the drive handles this as an unsafe condition and unloads the heads.

If a controller has seized a drive and multiple drive select is detected on the other port, the drive detects the condition but does not set fault and unsafe, and does not unload the heads. The port detecting multiple drive select reports it to the controller regardless of whether it had access to the drive.

Controller-to-drive (CTD) parity errors are detected and stored separately for each port. Unlike all other errors, the CTD parity error flip-flop is cleared with a drive clear regardless of whether or not that controller has seized the drive. The attention in the port is raised when a CTD parity error occurs.

5.8.5 Initialize in Dual-Access
The RK07 will honor an "initialize" issued separately from either port. The effect the "initialize" has depends upon the availability of the drive to the port issuing the command. The three drive conditions are described.

1. Drive is seized by a port. At this time, an initialize will:

    a. Clear that port's attention bit
    b. Clear the error flip-flops in the drive
    c. Cause the port to release the drive.

    If the other port's port request flip-flop is cleared, the drive will be returned to neutral. If the other port's port request flip-flop is set, the drive will become seized by the other port.

2. Drive is in neutral. At this time, an initialize will:

   a. Clear the port's attention bit
   b. Clear the error flip-flops in the drive.

3. Drive is seized by other port. At this time, an initialize will:

   a. Clear the port's attention bit
   b. Cancel a port request if one is pending.

5.8.6 Getting Drive Status in Dual-Access Mode

If the drive is seized by one of the ports, that port's controller may interrogate any of the eight status multiplexers (A0, B0, A1, B1, A2, B2, A3, B3) within the drive.

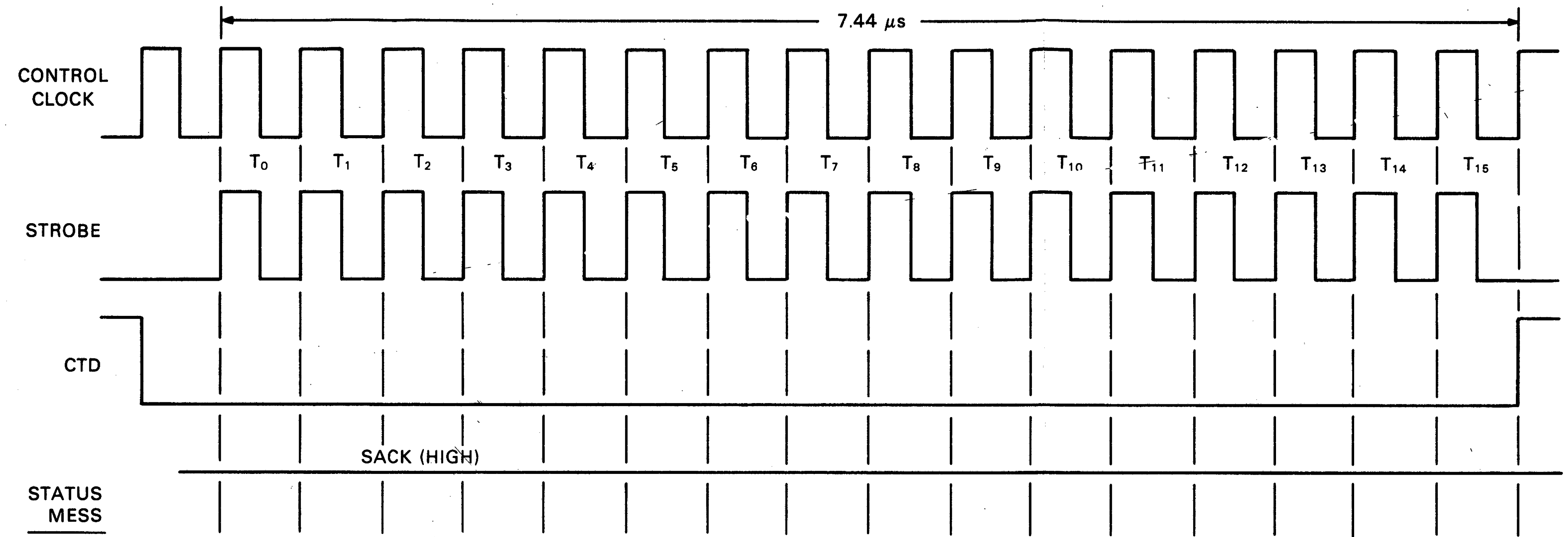
If the drive cannot be seized (busy with another port), only status multiplexers A0 and B0 may be read through the unseized port. This situation causes the combined error bit (bit 15 in RKCS) to be asserted in the controller of the unseized port. Refer to Figure 5-61 for the data bits contained in drive status messages A0 through B3.

Status Bits Pertinent to Dual-Port Available at the Unibus Interface

1. Drive available (DRA) – This bit is set to the port that has access to the drive and reset to the other port. Read only.

2. Volume Valid (Vol. Val.) – This bit is used to indicate when a disk cartridge may have been changed. There is a volume valid bit for each port.

3. Ready (RD) – Indicates that the selected drive is up to speed and its heads are settled over the specified cylinder. This bit will always be reset to a port not having access to the drive.



MESSAGE LINE A	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}
A0	DRIVE SELECT CODE			RESVD		DR AVAIL	VOL VAL	DR READY	DRIVE TYPE	20 SECT FORMAT	OFFSET ON	WR LOCK	SPINDLE ON	PIP	DR STATUS CHANGE	PARITY
A1	DRIVE SELECT CODE			RESVD	SERVO SIGNAL PRES	HEADS HOME	BRUSH HOME	DOOR LTCHD	CART PRES	SPEED OK	FWD	REV	LDG HDS	RTZ	UNLDG HDS	PARITY
A2	DRIVE SELECT CODE			RESVD	CYLINDER DIFFERENCE/OFFSET VALUE										RESVD	PARITY
A3	DRIVE SELECT CODE			DRIVE SERIAL NUMBER												PARITY

MESSAGE LINE B	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}
B0	MESS ID (0) (0)		RESVD FOR ADD'L MESS		RESVD	INV ADDR	AC LOW	FAULT	NXF	C-D PRTY ERR	SEEK INC	WR LOCK	SPEED LOSS	DR OFF TRACK	RD/WR UNSAFE	PARITY
B1	MESS ID (1) (0)		RESVD FOR ADD'L MESS		SECTOR ERR	WR CNT & NO WRITE GATE	WRITE GATE & NO TRANS	HEAD FAULT	MULT HD SEL	INDEX ERR	TRIBIT ERR	SERVO SIG ERR	SEEK & NO MOTION	LIM DET ON SEEK	SERVO UNSAFE	PARITY
B2	MESS ID (1) (1)		RESVD FOR ADD'L MESS		CYLINDER ADDRESS										RESVD	PARITY
B3	MESS ID (1) (1)		RESVD FOR ADD'L MESS		SECTOR COUNT					DECODED HEAD ADDRESS			RESVD		RESVD	PARITY

DRIVE-TO-CONTROLLER TRANSMISSIONS

MA-1384

Figure 5-61 Drive Status Bits Contained in A and B Messages

APPENDIX A
ABBREVIATIONS

A	Amperes
Abs	Absolute
AC	Alternating current
A/D	Analog to digital
Addnl	Additional
Addrs	Address
AGC	Automatic gain control
Amp	Amplifier or ampere
Atten	Attenuator
Attn	Attention
Avail	Available
Bet	Between
C	Centigrade
Cart	Cartridge
CB	Circuit Breaker
cfm	Cubic feet per minute
Clk	Clock
Clr	Clear
cm	Centimeters
Comm	Command
Comp	Comparator
Conn	Connector
Cont	Control
Coord	Coordinates
CP	Central Processor or clock pulse
CPA	Clock pulse, Port A
CPB	Clock pulse, Port B
CPU	Central Processor Unit
Ctr	Counter
CTD	Controller-to-drive
Ctrllr	Controller
Curr	Current
CVT	Constant voltage transformer
Cyl	Cylinder(s)
D/A	Digital to analog
DC	Direct current
DCL	Drive control logic
Diff	Difference, differential, or differentiator
Dir	Direction
Dld	Delayed
Dr	Drive
DS	Drive select

DSC	Drive status change
DTC	Drive-to-Controller
ECC	Error correction code
En	Enable
Err	Error
F	Fahrenheit
FET	Field effect transistor
FF	Flip-flop
FRU	Field replaceable unit
ft	Feet
Fwd	Forward
Gen	General or generator
H	High (logic)
Hds	Heads (read/write, or servo read only)
Hrs	Hours
Hz	Hertz
I & T	Interface and timing
IBD	Intermediate block diagram
I.D.	Identification
ILF	Illegal function
Ind	Indicator
Init	Initiate
I/O	Input/Output
I/S	Index/sector
J	Jack
kg	Kilogram
L	Low (logic)
Lbs	Pounds
Ld	Load (heads)
LED	Light-emitting diode
Lim	Limit or limiter
Lo	Low
LPM	Liters per minute
LSB	Least significant bit
m	Milli or meters
M	Mega (million) or Module (e.g., M7705)
Maint	Maintenance
MDS	Multiple drive select
Med	Medium (recording)
MFM	Modified frequency modulation
MHz	Megahertz
Min	Minimum or minutes
mm	Millimeters
MSB	Most significant bit
Msg	Message
ms	Milliseconds
Mux	Multiplex or multiplexer
N	North
Neg	Negative
n or nsec	Nanoseconds
NXF	Nonexecutable function
Op Amp	Operational amplifier
P	Plug or pole

Par	Parity
PCB	Printed circuit board
PIP	Positioning in progress
Pk	Peak
PLO	Phase lock oscillator
Pos	Positive
Pot	Potentiometer
Pres	Present
P.S.	Power supply
psi	Pounds per square inch
Pwr	Power
Qual	Qualification, quality, or qualifier
Rcvr	Receiver
Recal	Recalibrate
Reg	Register
Req	Request
Rev	Reverse or revolutions
rms	Root mean square
rpm	Revolutions per minute
Rsvd	Reserved
RTC	Return to centerline
RTZ	Return to zero
R/W or Rd/Wr	Read/write
S	South
SACK	Select acknowledge
sec	Seconds or secondary
Sect	Sector
Sel	Select
Ser	Serial
Stat Add	Status and address
Sub	Subtractor
SVO	Servo
Sw	Switch
Sync	Synchronous or synchronizing
T	Time bit (e.g., T_3)
Tach	Tachometer
TPI	Tracks per inch
TTL	Transistor-to-transistor logic
Unld	Unload (heads)
U	Unit Select (e.g., U2)
V	Volts
Val	Valid
Vac	Volts ac
VCO	Voltage-controlled oscillator
Vdc	Volts dc
Vel	Velocity
Vol	Volume
W	Watts
Wr	Write
Wr Prot	Write protect
Xducer	Transducer

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