G. Bell

PDP-X Technical Memorandum # 39

Title: Magtape IO Processor Interfaces

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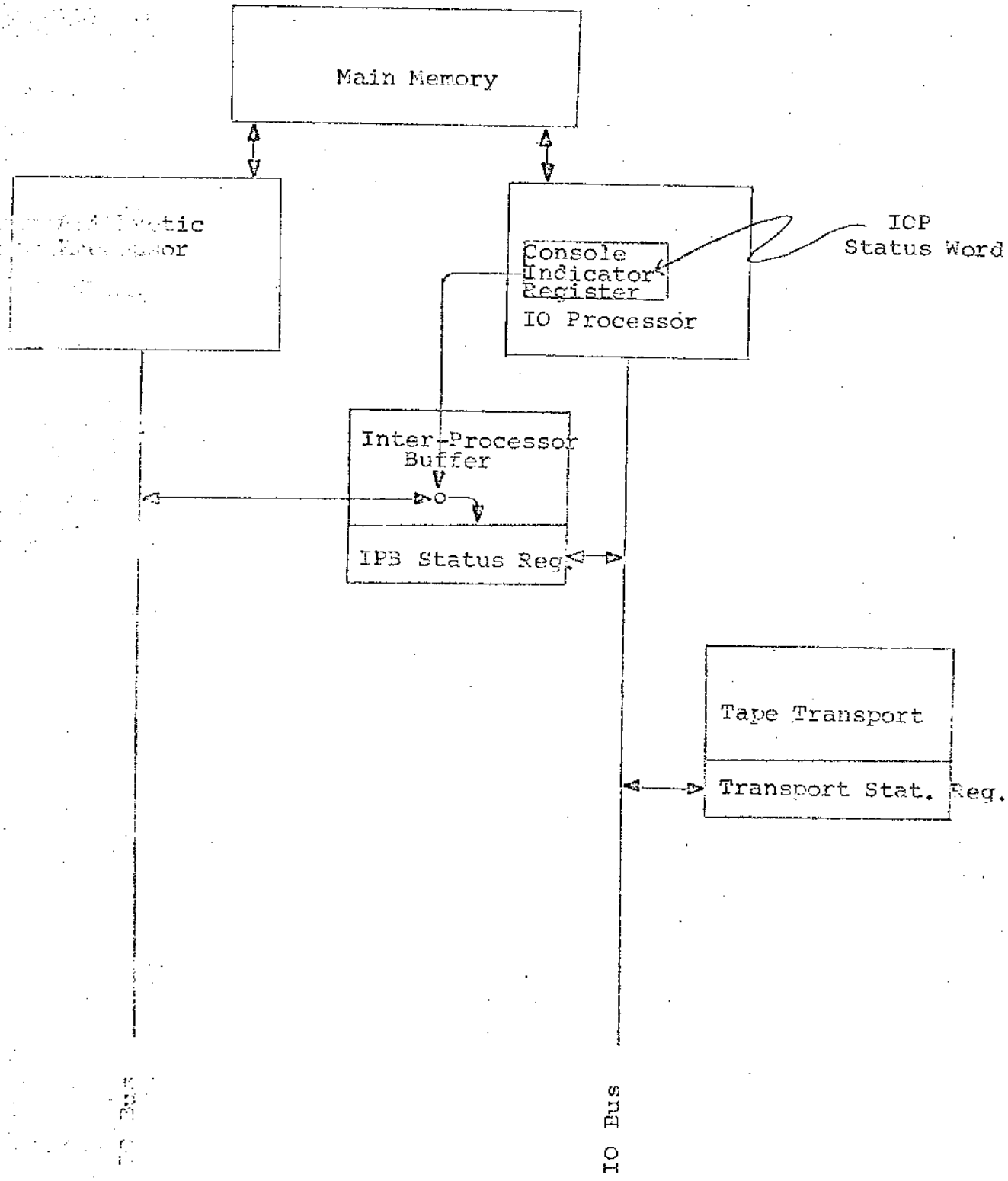

General System Organization

Preface

A rather novel feature of the PDP-X is the design of its peripheral device control units. Basically, these controllers are processor units identical to the Central or Arithmetic Processor hardware, including all special registers. Fast Memory, Memory Bus, IO Bus, etc. The difference lies in the organization of the read-only Control Memory.

Essentially, the organization of the AP Control Memory is based on fetching a stored program instruction from Main Memory and carrying out the sequence of μ-instructions it specifies. The IO Processor Control Memory, on the other hand, is organized to respond to commands from the AP which specify μ-code sequences to control a device: start it, stop it, determine its operating status, transfer data to or from it, and inform the AP of the condition of the IOP and any active device.

A critical part of specifying the μ-codes for the Control Memory specialized to a particular class of device is the determination of its communications with the remainder of the system.

I. Introduction

Each PDP-X processor, whether Arithmetic Processor or Input-Output Control Processor, communicates with the remainder of the system in two ways: Main Memory, via the Memory Bus, and other processors and peripheral devices through the Input-Output Bus. On the IO Bus, three separate means of communication are used:

a. The Inter-Processor Buffer, for transmitting control information between AP and IOP;

b. The IOP Status Register, for informing the AP on the status of the IOP, including active devices;

c. The Device Status Register, for transmitting control and status information between a peripheral device and its IOP.

Communications on the Memory Bus are identical for all processors and will not be discussed here. This memo will describe the operation of the IOP dedicated to the Magtape control function, and the use of the various signals transmitted and received on its IO Bus.

II. Inter-Processor Buffer

The transfer of basic control information between the AP and an IOP is via the IPB Register, which has connections to the IO Bus of each processor. The register format is identical to those of the Status Registers for the other devices which may be operated on the AP's IO Bus. Similarly, it responds to the "CONO" command out to load the bits on the IO Bus Data Lines, and the "CONI" command out causes it to transmit its contents on the Data Lines. (See Memoranda #29, sec. 3, and #30.)

The IPB system is shown schematically in Figure I. The arrows show direction of allowed data transfer; for example, the COMMAND bits may be loaded only by the AP, but may be sensed by either processor. The dashed lines indicate bits from which are derived the two INTERRUPT signals. AP receives an INTERRUPT when REQUEST and ENABLE are set (i.e., INTERRUPT = REQUEST ∧ ENABLE): note that the AP alone determines whether INTERRUPT will be allowed, since only the AP can set ENABLE. The only situation in which the IOP may be INTERRUPTED by the IPB is on an IO Halt command (= COMMAND0 ∧ COMMAND1). This command shuts down the presently active device immediately and unconditionally. The interpretation of and response to the bits is approximately the same at the AP for all devices, although IOP's for different devices may treat various bits differently.

A normal IPB sequence might be understood by an example. Assume that a block of data is to be transferred from Memory to a certain Transport: the program instruction would be "IOC MTA, [005] ", setting BUSY and ENABLE in the IPB. At the next period of low IOP activity, such that a new operation may be initiated without interfering with an operation in progress, the IOP will read the state of the IPB. If BUSY = 1, the operation specified by the COMMAND bits will be initiated. Upon completion of this operation, or if an error is detected, IOP clears BUSY and sets REQUEST (causing an INTERRUPT at AP in this case, since ENABLE = 1). In the case of error detection, UNUSUAL is also set. The "device" address assigned to this IPB is placed on the Data Lines at the same time, as in other devices upon INTERRUPT, so that the AP may identify the calling "device" and take appropriate action.

III. Command Lists and Words

The alert reader will have noted that the IOP still needs much additional data before execution of the program instruction may begin on the Tape Transport. The IOP gets the information from a Command List, which the program has previously formed in Main Memory. The structure of this Command List is shown in Figure II.

For each type of peripheral device, a permanent Memory location is assigned, its address given by 500 + (Device Type No.) (from Memo #29, Section 3.6); for the Magtape, it is 540. This location will contain the address of the Command List to be executed. The CL itself consists of:

a. A Command Word, containing all data regarding tape function, Transport number, direction, etc.;

b. A Medium Address, not used with Magtape;

c. A Byte Address, specifying the location in Memory for data transfer;

d. A Byte Counter, specifying the total number of bytes to be transferred;

e. Finally, a Command Chain Address, pointing to a new Command List to be executed upon termination of the present one, when its bit 0 = 1.

When an IO Start is given, the three necessary words (CW, BA, BC) are loaded into the IOP's fast memory. The CW, whose format is shown in Figure III, is decoded to form the correct control word to be transmitted to the Transport's Status Register.

Figure II also shows how Data Linking and Command Chaining are accomplished. Specifically, the Byte Counter only uses 15 bits of the word: bit 0 is the Data Link Indicator. When DLI = 1, the following two words are another BA - BC pair, specifying data transfer when the existing count overflows. If DLI = 0, for any of a series of Data Linked pairs, bit 0 of the next word is the Command Chain Indicator. CCI = 1 indicates that the remainder of the word is the address of the CW which begins the next Command List to be executed. If CCI = 0, this is the last of the chain; execution ends, status is updated and the IOP signals the AP (by setting BUSY and clearing ACTIVE in the IPD) that the job has been completed. Note that, when chaining occurs, the contents

of location 540 are updated by the IOP to point to the currently active process.

The Command Word format is almost identical for all device types; for example, all CW's will use bit 4 to specify the function to be performed by the device. However, the function codes will be interpreted differently by different device IOP's (e.g., function code 1 will not cause a line printer to rewind). This will be discussed in more detail in a future memo.

IV. Magtape Status Register

The operating state of a Tape Transport is controlled and sensed via its Status Register. The SR may be considered as four bytes, of which two consist of motion timing delays and are actually hard-wired at the time of original transport calibration.

The SR information is placed on the Data Lines in response to a "CONI" Command Out. A Selector-Counter determines which byte is sent for a given CONI, and is incremented by CONI. The S-C is reset when the device is "SELECTED"; thus, the IO Bus sequence for reading Status is a SELECT, even if this is redundant, followed by CONI four times.

When this sequence is employed, the first byte received is a combination of all six control bits plus the two most important status/condition bits. This byte is the only part of the SR which may be loaded from the Data Lines when CONO is received by the transport, thus effecting a change of control. The uses of the bits of Byte 1 are:

Bit	Meaning When Asserted
8	on Interrupt: data present under transport Read heads (allows the IOP Interrupt handling routine to distinguish between interrupts from the transport clock and from reading data)
9	transport is connected to IO Bus, is not in motion, and power is on
10	move, in direction specified by bit 11
11	reverse
12	send standard clock (probably 800 bpi) for timing of Inter-Record Gap
13	high-speed rewind to BOT; if bit 11 = 1, Rewind/Unload (see CW bit 12)
14	enable current to write drivers
15	SPARE

Bits 8 and 9 are really Status/Condition information, although they are loaded by CONO. The remaining bits are Control bits for the transport electrical system. Byte 2, which contains Condition bits exclusively, may only be read. Its bits mean:

Bit	Meaning When Asserted
0	9-track transport selected
1	in process of coming to rest from a command to move
2&3	clock period, set by manual switch
4	rewind in process
5	write-protect ring is locked on tape reel
6	End-Of-Tape mark being sensed
7	Beginning-Of-Tape mark being sensed

The two remaining bytes contain the three delay timing counts which are needed for stopping and starting the tape's motion at the correct spot between records, and for timing the distance from BOT to where writing may begin. (Only three delays are sent, as the remaining three are derivable from them.) They are not generated in registers, but are hard-wired at the time the transport is calibrated.

V. Magtape IOP Status Word

By means of the IOP Status Word information concerning the operating state of the IOP, and any device which is presently selected on the IOP's IO Bus, is made available to the programmer. The SW is formed by the IOP when a function is initiated and updated every time Command Chaining occurs, when a function terminates, or when some unusual condition is detected.

The IOP Status Word is physically located in the Console Indicator register of the IOP. The CI register is connected to the AP's IO Bus, becoming selected at the same time that the corresponding Inter-Processor Buffer is selected by the AP. The two bytes of the Status Word are then transmitted to the AP when it sends two successive "DATI" commands on its Command Out lines (ICR instruction).

The format of the IOP Status Word is shown in Figure V. It will be seen in future memos that most bits are assigned meanings which will be similar for all types of selector-channel devices. A more detailed breakdown of their meanings for the Magtape ICP is given below.

Bit	Meaning When Asserted
0	error (inclusive or of bits 2, 3, and 8-15)
1	selected transport not ready: power off, or in motion, or not connected to IO Bus
2	attempt to Space Reverse or Rewind with selected transport at BOT
3	attempt to write on a transport when mounted tape reel is protected against writing
4	selected transport is rewinding
5	End-Of-File mark detected
6	End-Of-Tape sensed by selected transport
7	Beginning-Of-Tape sensed by selected transport
8	attempt to select a transport not on the IO Bus
9	data over-run: inputs too fast for memory access, or output too slow for write strobe

Bit	Meaning When Asserted
10	bad tape
11	disagreement between bytes in memory and on tape during Read/Compare process
12	Byte Count did not reach zero concurrently with end of record during Read or Read/ Compare
13	lateral parity error
14	disagreement between Cyclic Redundancy Character generated by IOP while Reading record and CRC read from tape
15	disagreement between Longitudinal Parity Checks (check sum) generated by IOP and read from tape

C_0	C_1	Meaning
0	0	IO Start
0	1	IO Test
1	0	Illegal
1	1	IO Halt

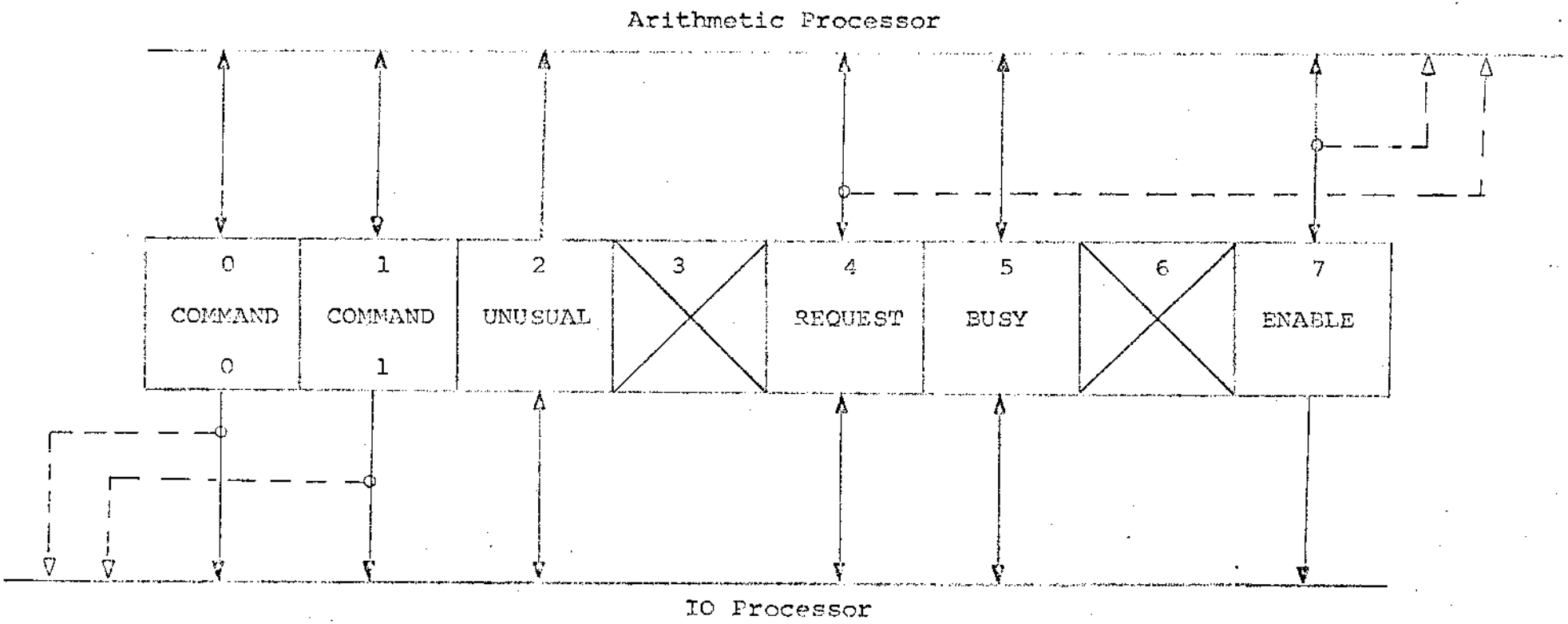

Figure I. Inter-Processor Buffer Register

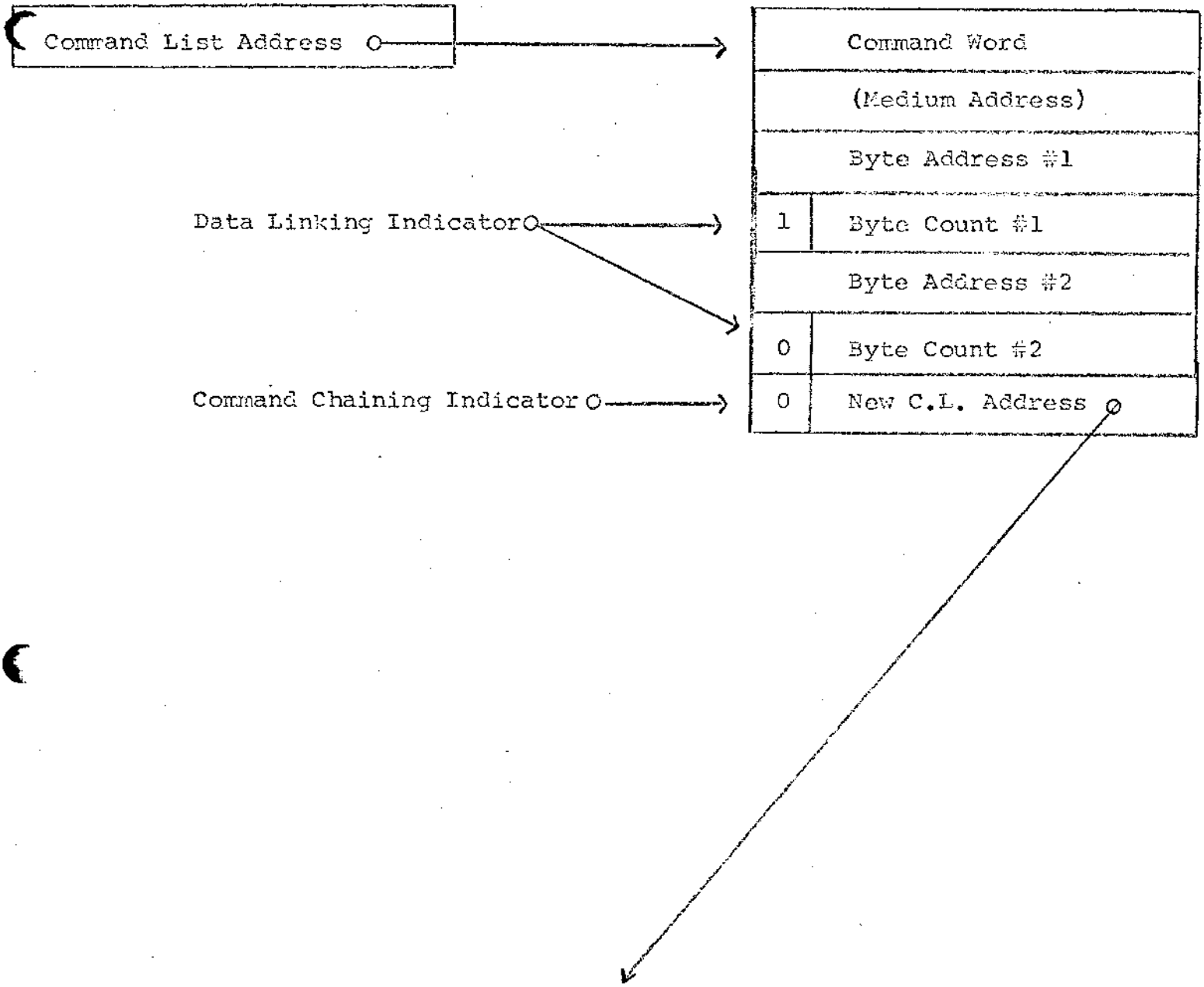

Figure II. General Command List Structure

0	1	2	3	4	5	6	7
1	1	0	0-FORWARD 1-REVERSE		Function (see Table III.)		

8	9	10	11	12	13	14	15
Parity: 0-EVEN 1-ODD	0-COUNT BYTES 1-COUNT RECORDS	SPARE	1-INTER-RUPT ON COMMAND CHAINING		Device Address		

Figure III. Organization of Magtape Command Word

Table III.

Program Command Word
Function Codes, bits 4-7, as interpreted
by the Magtape IOP

Bit	Meaning When Asserted
0	No operation
1	Rewind; stop at BOT
2	Space number of records specified by BC; take direction from bit 3
3	Read number of bytes of data specified by BC (number of records if bit 10 = 1) into Memory beginning at BA; test for parity as selected by bit 8; form Longitudinal Parity Character (check sum), and, if 9-track tape, Cyclic Redundancy Character
4	Read/Compare: read {BC} bytes (or records) from tape, comparing each with memory data beginning at {BA}
5	Write on tape {BC} bytes beginning in memory at {BA}, inserting selected parity; compute LPC, also CRC if 9-track, and use these to write the End-Of-Record Mark (note: during Write, data will be read back after writing and parity checked)
6	Write End-Of-File Mark
7	Write Extended Inter-record Gap; produces 3" of blank tape
10	Read in Image Mode: 9-bit bytes, transferred into sequential memory locations without packing, including CRC, LPC
11	Write in Image Mode: write the low 9 bits of sequential memory locations directly onto tape
12	Rewind/Unload: rewind until all tape is transferred to one reel; do not stop at BOT
13	Load Map: load the IOP paging registers from memory beginning at {BA}
14-17	unassigned

Status Byte 2

0	1	2	3	4	5	6	7
0-7 TRACK 1-9 TRACK	SETTLING	DENSITY		REWINDING	WRITE LOCK	END OF TAPE	BEGINNING OF TAPE

0 - 200 BPI
1 - 556 BPI
2 - 800 BPI
3 - 1600 BPI

Status Byte 1

8	9	10	11	12	13	14	15
DATA INTERRUPT	READY	MOVE	REVERSE	INTER-RECORD GAP	REWIND	WRITE ENABLE	SPARE

Figure IV. Magtape Transport Status Register Bit Assignment

0	1	2	3	4	5	6	7
ERROR	NOT READY	ILLEGAL REVERSE COMMAND	ILLEGAL WRITE COMMAND	REWINDING	END OF FILE	EOT	EOT

8	9	10	11	12	13	14	15
SELECT ERROR	TIMING ERROR	BAD TAPE	READ/ COMPARE ERROR	RECORD LENGTH DISCREP.	BYTE (LATERAL) PARITY ERROR	CRC ERROR	LPC ERROR

Figure V. Magtape Status Word