PDP-X Technical Memorandum # 7

Title: Light Duty Card Reader

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Index Keys: Card Reader
                    IO
                    Peripherals

Distribution
 Key: A, B, C

Obsolete: None

Revision: None

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0. Overall Description

The CR01 is a 100 card-per-minute reader designed around the NCR Type EM-D2 mechanical reader. It is designed for light duty reading of program and data cards.

1. General Specifications

1.5 General Performance Specifications

The CR01 Card Reader operates at a maximum rate of 100 cards (standard 80 column) per minute in either binary or alphanumeric mode. Cards are read column by column at a rate of 1 column every 7 ms. Approximately 25 ms are available between cards.

In binary mode each column is read into the computer as an 12-bit binary number where row 9 is represented in the low order bit position and row 12 is represented in the high order position. In binary mode, a bit value of 0 = no punch; 1 = punch. The high order 4 bits are set to 0.

In alphanumeric mode, each column is encoded as follows:

a. Rows 1-9 4-bit BCD set (low order).

b. Rows 12, 11, 10 are encoded into 2 (high order) bits as follows:

The most significant bit = 12 — Zone V 11-Zone and the next most significant bit = 12-Zone V 0 - V 0 - Zone.

3. Programming

3.1 Instructions

The CR01 reader is programmed by loading its status register

(see section 3.6) and by setting bits in this register. Bits in the status register may be loaded or changed by the IOC and IOX instructions respectively. Bits in the status register may be read or tested by the IOS and IOT instructions respectively.

If the ENABLE BIT is a one and either the REQ bit or the CARD DONE bit is set, an interrupt is requested. If the word at the interrupt location is a Branch instruction, central processor control is transferred to a routine responsible for handling the source of the card reader interrupt. If the word at the interrupt location is an IO instruction (i.e. a Byte Counter) data is transferred into memory under multiplexor channel control.

The NOT READY bit in the status register is maintained in the one state (set) if any of the following conditions are met in the reader:

a. Power is off

b. There is no card in the Read Station

(the first card is positioned by means of the REG switch on the reader).

c. The AUTO/MAN switch is in the MAN position.

If the program clears the NOT READY bit with an IOC or IOX instruction and any of these conditions are met, the NOT READY bit will remain set. If none of these conditions are met, the NOT READY bit is only cleared by either an IOC or IOX instruction issued by the processor or by manually depressing the SKIP switch on the reader.

When the NOT READY bit becomes zero and the BUSY bit is
set, the card positioned at the read station is advanced and
read. The REQ bit is set for each column and the BUSY bit is
cleared. If the ENABLE bit is set, an interrupt is requested.
When the processor issues a read either as a result of a multi-
plexor channel operation or by the execution of an IOR instruction,
the data is read into memory and the REQ bit is cleared and
BUSY set, if there is no overflow. If overflow occurs, LOW is
set and a second interrupt is requested.

As a response to an interrupt with the Low bit set, the program
should clear the REQ bit and dismiss the interrupt. When the
card passes from the read station, the next card in the hopper
will be advanced into position at the read station and the
CARD DONE bit is set along with LOW. If this was the last card,
NOT READY will be set as indicated in (b.) above.

3.2 Maintenance Instructions

There are no special maintenance instructions.

3.3 Data Formats

Data is read in either Binary or in Alphanumeric format as
determined by bit 9 (BIN) in the status register:

3.3.1 Binary (BIN=1)

Each column is read as on 12-bit binary word where row 12 is re-
presented in bit position 4 and row 9 is represented
in the low order bit position of the data word.

3.3.2 Alphanumeric (BIN=0)

Each column is encoded as follows:

    a. Rows 1-9 are encoded (BCD) into 4 bits in the low

order position of the data byte (bits 12-15).

    b. Rows 12, 11,10 are encoded into two bits as follows:

        - Bit 10 is set if either Row 12 or Row 11 is

        punched.

        Bit 11 is set if either Row 12 or Row 10 is

        punched.

The two high order bits (8-9) are always zeros. (Thus, the
Hollerith A - punches in rows 12, 1 would be read as:
00110001).

See Appendix.

3.4 Timing

Cards are read at a maximum rate of 100 cards per minute. Cards
are read column by column at a rate of 1 column every 7 ms.
After REQ is set, data must be read out of the data buffer
within 1.5 ms. Data may be read in either mode during this
period, the mode changed and the data re-read. After CARD DONE
is set, BUSY must be set immediately to re-select the reader
and keep it operating at full speed.

3.5 Operator Controls

Control or Indicator	Function
ON/OFF	This switch controls the application of primary power to the reader. When power

3.5 Operator Controls (con't)

is applied, the reader is ready to respond to operation of the other keys.

AUTO/MAN Switch

In AUTO position, card reading under program control is enabled. In MAN, this switch mechanically disables the automatic card feed mechanism.

REG Key

The REGister Key is used to manually feed the first card to the read station.

SKIP Switch

When depressed, clears the NOT READY bit in the status register if power is on, a card is positioned in the read station and the AUTO/MAN switch is in the AUTO position.

3.6 Status Register

The CR01 status register appears as:

NOT READY	BIN	CARD DONE	Ø	REQ	BUSY	LOW	ENABLE
8	9	10	11	12	13	14	15

If bit 9 (BIN) is a one, binary mode is indicated. A zero indicates alphanumeric mode.

The remaining bits are described in section 3.1.

3.7 Programming Examples

The channel location for the card reader is initialized with:

a. Byte Counter containing minus the number of bytes to be transferred.

b. The Byte Pointer is initialized to point to the location into which the first byte is to be transferred.

c. The Low interrupt locations should contain a Branch to the reader service routine.

The BUSY and ENABLE bits are set. The BIN bit is set or cleared depending upon the desired mode and the remaining bits are cleared. If the reader is ready, reading will commence when the reader is ready and SKIP is depressed. Data will be transferred under multiplexor channel control until a channel overflow occurs or until the last column is read, whichever comes first. A low interrupt will occur if either the channel overflows or the CARD DONE bit is set. The next card may be read if the CARD DONE flag is set.

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; READ ONE CARD INTO BUFFER UNDER CHANNEL CONTROL
; IN ALPHANUMERIC MODE
; INITIALIZE CARD READER CHANNEL
; CDR IS CARD READER DEVICE NUMBER
        LDA   AC,   -'D80        ; PUT -80 INTO AC
        STA   AC,   CDRINT       ; STORE IN BYTE COUNTER
        LDA   AC,   2*BUFFER     ; PUT BYTE POINTER INTO AC
        STA   AC,   CDRINT+1     ; STORE IN POINTER
        IOC   CDR,  005          ; SET TO ALPHA MODE
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                                      ; AND START READER

              CLR          CDONE       ; CLEAR INDICATOR

                                      ; PROGRAM CONTINUES

                                      ; C(CDONE) WILL BE -1

                                      ; WHEN DATA IS IN BUFFER


; CARD READER INTERRUPT SERVICE

CDRSER:   IOT    CDR, [040]            ; TEST CARD DONE  .

          BN          CDRDUN           ; BRANCH IF SET

          IOX    CDR, [010]            ; CHANNEL OVERFLOW

          DBK                          ; INTERRUPT - CLEAR

                                      ; REQ AND DISMIS


; CARD DONE FLAG IS SET, BYTE COUNTER

; SHOULD BE ZERO

CDRDUM:   TST         CDRINT           ; TEST BYTE COUNTER

          BN          CDRERR           ; BRANCH IF ERROR

          IOC    CDR, [0]              ; OK, CLEAR READER

          COM         CDONE            ; SET INDICATOR

          DBK                          ; DISMIS

; AT THIS POINT, THE PROGRAM COULD HAVE TESTED

; NOT READY OR IT COULD HAVE SELECTED

; ANOTHER CARD

CDONE:    Ø
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If it is desired to translate directly from Hollerith to ASCII
on each column, the multiplexor channel mode should not be used.
Instead, the location CDRINT should contain a Branch to a routine
to read in the column and translate to ASCII by table lookup.