PART I
CHAPTER 7

CONSOLE OPERATION

The PDP-11/20, PDP-11/15, and PDP-11R20 Operators' Consoles provide users with comprehensive information regarding the status of the system, and with function switches to control the system. Each section of the Operator's Console is discussed in this chapter. The PDP-11R20 Console differs slightly in layout due to ruggedized construction constraints, but it is functionally identical to the PDP-11/20 Console. The PDP-11/15 console differs only in that there are 16 lights and switches in the Address Register, instead of 18 as in the PDP-11/20.

INDICATOR LIGHTS

RUN	On:	Indicates that the processor clock is running, processor has control of bus, and is executing an instruction.
	Off:	Indicates that the processor is waiting for an asynchronous peripheral data response, or that the processor has surrendered its control to the console or a peripheral.
	Remarks:	Flickers on and off during normal machine operation, except during the following programmed instructions: WAIT (completely on); HALT (completely off).
BUS	On:	Indicates that a peripheral device is controlling the bus.
	Remarks:	Only on when there is a bus malfunction or where a peripheral holds the bus for excessive periods of time, or in large systems when multiple devices are using the bus for DMA operations.
		When Bus and Run are off, bus control has been transferred to the console.
FETCH	Function:	Indicates that the processor is in the FETCH state and is obtaining an instruction.
	Remarks:	Only Fetch and Run lights are on during the Fetch state if no non-processor requests are honored.

EXEC	Function:	Indicates that the processor is the Execute state, performing an action specified by the instruction.
	Remarks:	Only Exec and Run indicators are on during the Execute state if no non-processor requests are honored.
DEST.	Function:	Indicates that the processor is in Destination state and is obtaining destination operand data.
	Remarks:	Destination and Run are both on during the Destination state. Address lights may be on in various combinations. Bus is off if no non-processor requests are honored.
SOURCE	Function:	Indicates that the processor is in the source state and is obtaining source operand data.
	Remarks:	Source and Run lights are both on during the Source State. Address Lights may be on in various combinations. Bus if OFF if no non-processor requests are honored.
ADDR. (2 lights)	Function:	Indicates bus cycles used to obtain address data during Source and Destination states. Binary code of lights indicates address cycle (1,2, or 3) machine is in source or destination state.
	Remarks:	When either light is on, either Source or Destination is on. Bus if off if no non-processor requests are honored.

SWITCH REGISTER
18 Key-Type Switches*

Function:	Used to manually load 16-bit data word or address into processor. UP = ON = 1 DOWN = OFF = 0
Remarks:	If the word in the Switch Register represents an address, it can be loaded into an sents an address, it can be loaded into an Address Register by depressing LOAD ADDR key. If the word contains data, it can be loaded into to address specified by the ADDRESS REGISTER by lifting the DEP key. The data will appear in the DATA display.

*16 Switches on KY11C Console (PDP-11/15)

Remarks: The console permits the user to immediately examine data just deposited with out readdressing, to re-deposit if necessary, and to continue without automatic incrementation. These sequences are associated with the functioning of DEP and EXAM Switches. The state of the switches can be read as 1's and 0's under program control by reading address 777570.

CONTROL SWITCHES

LOAD ADDR.

Function: (Depress to activate) Transfers contents of switch register to bus address register.

Remarks: The resulting bus address, displayed in the ADDRESS REGISTER, provides an address for EXAM, DEP, and START.

EXAM Function: (depress to activate) Transfers contents of bus address for DATA display. Data address will appear in two ADDRESS REGISTER.

Remarks: If the EXAM switch is depressed on succession, the contents of the next sequential bus address are displayed in DATA. This action is repeated each time EXAM is depressed provided no other Switch is used between these steps.

CONT Function: (depress to activate) Causes processor to continue operation from the point at which it had stopped. If ENABLE/HALT is on ENABLE, returns bus control from console to processor and continues program operation. If ENABLE/HALT is on HALT, causes the processor to perform a single instruction or a single bus cycle and stop.

Remarks: If program stops, this switch provides a restart without program clear.

ENABLE/HALT

Function: (2-position switch) Allows either the program or the console to control processor operation. ENABLE permits system to run normally. HALT stops the processor and passes control to the console.

Remarks: Continuous program control requires the ENABLE mode.

HALT mode is used to interrupt program control, perform single-step operation, or clear the system. HALT is used with the CONT switch to step the machine through

programs and facilitate intermediate observations.

S-INST/S-CYCLE

Function: Allows processor to step through program operation either one instruction or one bus cycle at a time. S-INST: processor halts after an instruction. S-CYCLE: processor halts after a bus cycle.

(2 position switch)

Remarks: Enabled by ENABLE/HALT in HALT mode.

START Function: If ENABLE/HALT is on ENABLE, provides a system clear operation, then begins processor operation. A LOAD ADDR operation establishes the starting address. If ENABLE/HALT is on HALT, provides a system clear (initialize) only. Processor does not start.

(depress to activate)

DEP Function: Transfers contents of console SWITCH REGISTER to bus address.

Remarks: After use data will appear on DATA display, address in ADDRESS REGISTER.

ADDRESS REGISTER

18-Bits, divided in 3-bit sequence.

Function: Displays the address of data examined or deposited. (16-bit in the PDP-11/15)

Remarks: During a programmed HALT or WAIT instruction, display contains the address of the instruction.

During direct memory operations, the processor is not involved in data transfer functions, and the address displayed is not of the last bus operation.

When console switches are used, this display contains the following:
LOAD ADDR - Transferred
SWITCH REGISTER - data
DEP or EXAM - the bus address just deposited into or examined
S-INST or S-CYCLE - the last processor address

DATA

16-Bit Display

Function: Displays data from processor data paths. This is not a single register but the sum of two later registers on the data paths (16-

bit on the PDP-11/15) on both machines, no distinction necessary.

Data is mainly loaded into this register by setting the data value into SWITCH REGISTER and lifting the DEP switch.

Remarks:

When console switches are used, this display contains:
LOAD ADDR - no indication
DEP - the switch register just deposited.
EXAM - the data from the address examined.
S-INST - no indication when stepping through a program by single instruction.
S-CYCLE - last data in the data paths.
WAIT - no indication
HALT - displays processor register R0 when bus control is transferred to console during a HALT instruction.
RESET - displays register - R0 for during of RESET (70 msec).

POWER LOCK
OFF/POWER/PANEL LOCK

3-position switch

OFF: Removes all power from processor 3 position switch

POWER: Applies primary power to processor

PANEL LOCK: Disables all console controls except switch register key switches.

Remarks:

OFF: System is not being used
POWER: Normal operation; all console controls fully operational