DL11
asynchronous
line interface
engineering drawings

digital equipment corporation · maynard. massachusetts

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET ☐☐☐☐

SEQUENCE

PRINT SET #1

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-YA-1
CABLE ASSEMBLY (KL8/E)	D-IA-7008360-Ø-Ø
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

SEQUENCE

PRINT SET #3

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C	D-UA-BCØ5C-Ø-Ø
CABLE ASSEMBLY (KL81E)	D-IA-7008360-Ø-Ø
MODEM TEST CONN.	D-CS-H315-Ø-1
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

PRINT SET #2

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C	D-UA-BCØ5C-Ø-Ø
FILTER NETWORK	B-CS-G8ØØØ-Ø-1
MODEM TEST CONN	D-CS-H315-Ø-1
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

UNIT VARIATIONS

VAR	TITLE	PRINT SET DL11-1	PRINT SET DL11-2
DL11-A	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-B	ASYNC LINE INTERFACE, EIA	0	1
DL11-C	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-D	ASYNC LINE INTERFACE, EIA	0	1
DL11 E	ASYNC LINE INTERFACE, DATA SET	0	1

REVISIONS

REV	CHG NO	DATE
K	[illegible]	[illegible]

USED ON OPTION/MODEL

DRN. M. Pierce	DATE 4-28-72
CHK'D. R. Cook	DATE 5-9-72
PROJ ENG. P.E.Janson	DATE 5-11-72
PROD. J.McIntyre	DATE 5-15-72
FIELD SERV. R. Evans	DATE 5-15-72

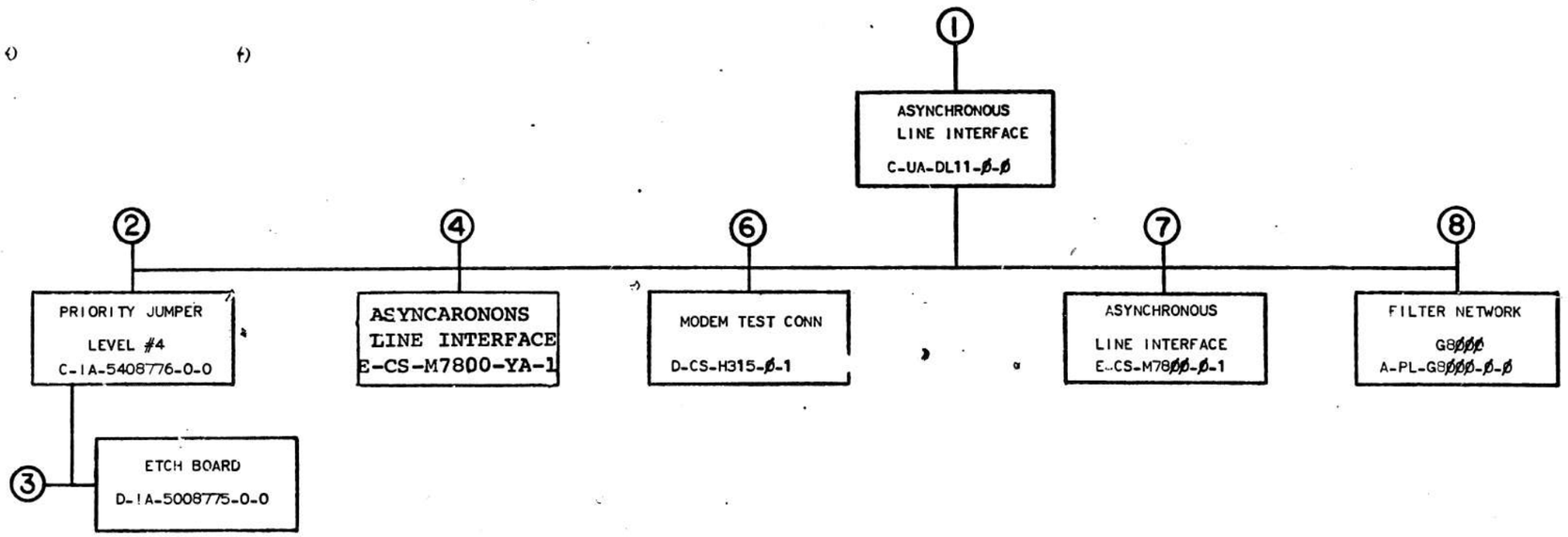
SHEET 1 OF 3

TITLE: ASYNCHRONOUS LINE INTERFACE

SIZE	CODE	NUMBER	REV
B	DD	DL11-Ø	K

DIST

DRB 106



TITLE			SIZE	CODE	NUMBER	REV
	ASYNCHRONOUS LINE INTERFACE	SHEET 2 OF 3	B	DD	DLII - Ø	K

ELECTRICAL

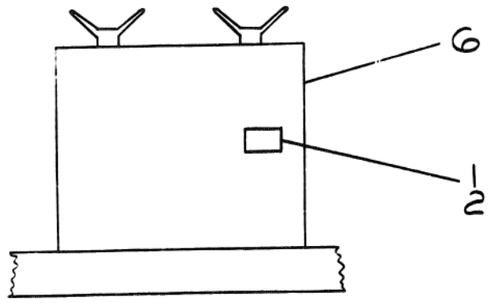
DL11-1	DL11-2	DL11-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X	X	X		1.	C-UA-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE	
X	X	X			A-PL-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE (PL)	
	X	X			D-UA-BCØ5C-Ø-Ø	#	1	CABEE. MODEM. BCØ5C	
X		X			D-IA-7008360-0-0	#	1	CABLE, ASSEMBLY (KL8/E)	
					A-SP-DL11-Ø-1	*	11	ENGINEERING SPECIFICATION	
X	X	X			A-SP-DL11-Ø-2	F	9	INSTALLATION PROCEDURE	
					A-SP-DL11-Ø-3	B	8	TEST PRODEDURE (TEST & ACCEPTANCE)	
X	X				A-SL-DL11-Ø-4	*	1	SOFTWARE LIST	
X	X				A-AL-DL11-Ø-5	C	1	ACCESSORY LIST	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					B-CS-5408776-0-1		1	CIRCUIT SCHEMATIC	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	MODULE ECO HISTORY	
				3.	C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
X				4	E-CS-M7800-YA-1	#	6	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-YA-4		1	X-Y COORDINATE HOLE LOCATION	
					D-AH-M7800-YA-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-M7800-YA-6		1	MODULE ECO HISTORY	
	X	X		6.	D-CS-H315-Ø-1	#	1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-H315-Ø-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
	X	X		7.	E-CS-M78ØØ-Ø-1	#	7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M78ØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M78ØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M78ØØ-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8ØØØ-Ø-Ø		1	FILTER NETWOPK	
	X				B-CS-G8ØØØ-Ø-1	#	1	CIRCUIT SCHEMATIC	
					K-CO-G8ØØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8ØØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8ØØØ-Ø-6		1	MODULE ECO HISTORY	

MECHANICAL

DL11-1	DL11-2	DL11-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
				1.	C-UA-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE	
					A-PL-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE (PL)	
					D-UA-BCØ5C-Ø-Ø		1	CABLE, MODEM BCØ5C	
					D-IA-7008360-0-0		1	CABLE ASSEMBLY (KL8/E)	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	ASSY/DRILLING HOLE LAYOUT	
				3.	D-IA-5008775-0-0		1	ETCH BOARD	
					C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
				6.	D-CS-H315-Ø-1		1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-H315-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
				7.	E-CS-M78ØØ-Ø-1		7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M78ØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M78ØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M78ØØ-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8ØØØ-Ø-Ø		1	FILTER NETWORK	
					K-CO-G8ØØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8ØØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8ØØØ-Ø-6		1	MODULE ECO HISTORY	

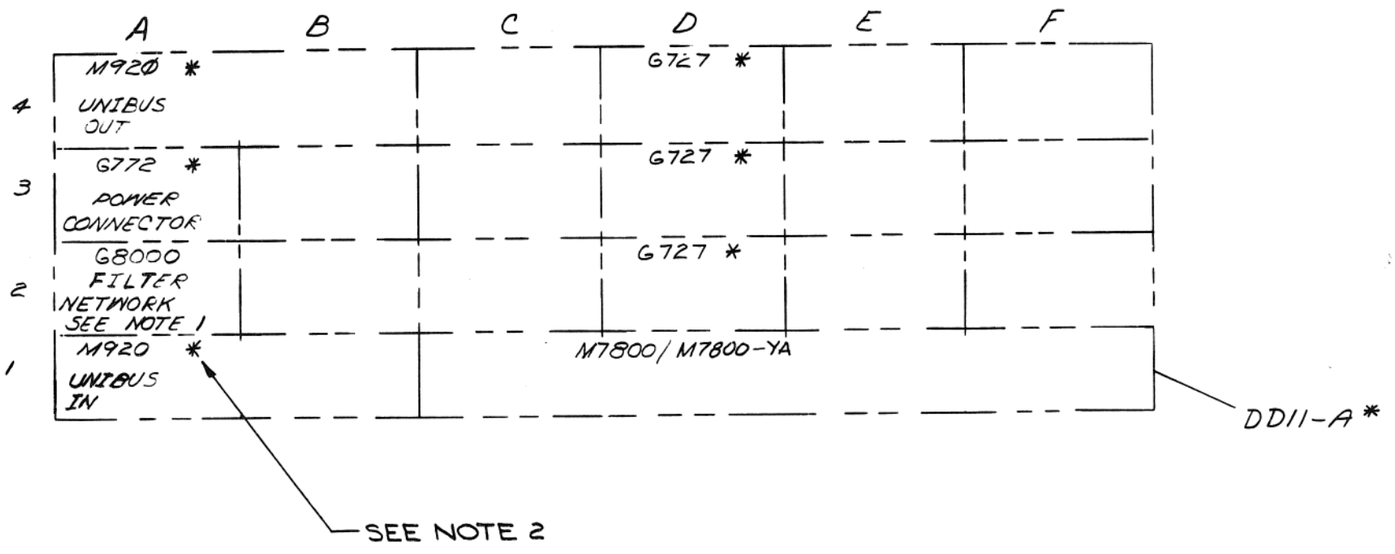
TITLE		SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	SHEET 3 OF 3	B	DD	DL11-Ø	K

G.



NOTES:

1. G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALATION REQUIRES 2 WIRES TO BE ADDED.
   AØ3V2 - AØ2V2
   AØ2N2 - CXXU1
   WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL 11.
2. ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.



REVISIONS												
CHK	CHANGE NO.	REV.										
PM	DL11-OCC01	A										
	H. JANSON											
	DL11-00002	B										
	JANSON											
PM	DL11-00005	C										
	L. CONDON											
	DL11-00006	D										
	CONDON											
	DL11-00008	E										
	L. CONDON											
	DL11-00009	F										
	J. MCINTYRE											

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

DRN. M Price	DATE 3/18/72	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D. J Fenton	DATE 4-29-72	
ENG. P E Janson	DATE 5-11-72	TITLE ASYNCHRONOUS LINE INTERFACE
PROJ ENG. P E Janson	DATE 5-11-72	
PROD. J McIntyre	DATE 5-15-72	
NEXT HIGHEI. ASSY. B-OD-DL11-Ø		SIZE C CODE UA NUMBER DL11-Ø-0 REV F
SCALE NONE		DIST
SHEET 1 OF 1		

DEC FORM NO. DRC 100-A

REV. F
SIZE C CODE UA NUMBER DL11-Ø-Ø

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY M. PIERCE DATE 4/27/72	CHECKED J. FERGUSON DATE 4/27/72	SECTION 1
ENG P. E. JANSON DATE 5/11/72	PROD J. McGilvery DATE 5/15/72	ISSUED SECT. 1

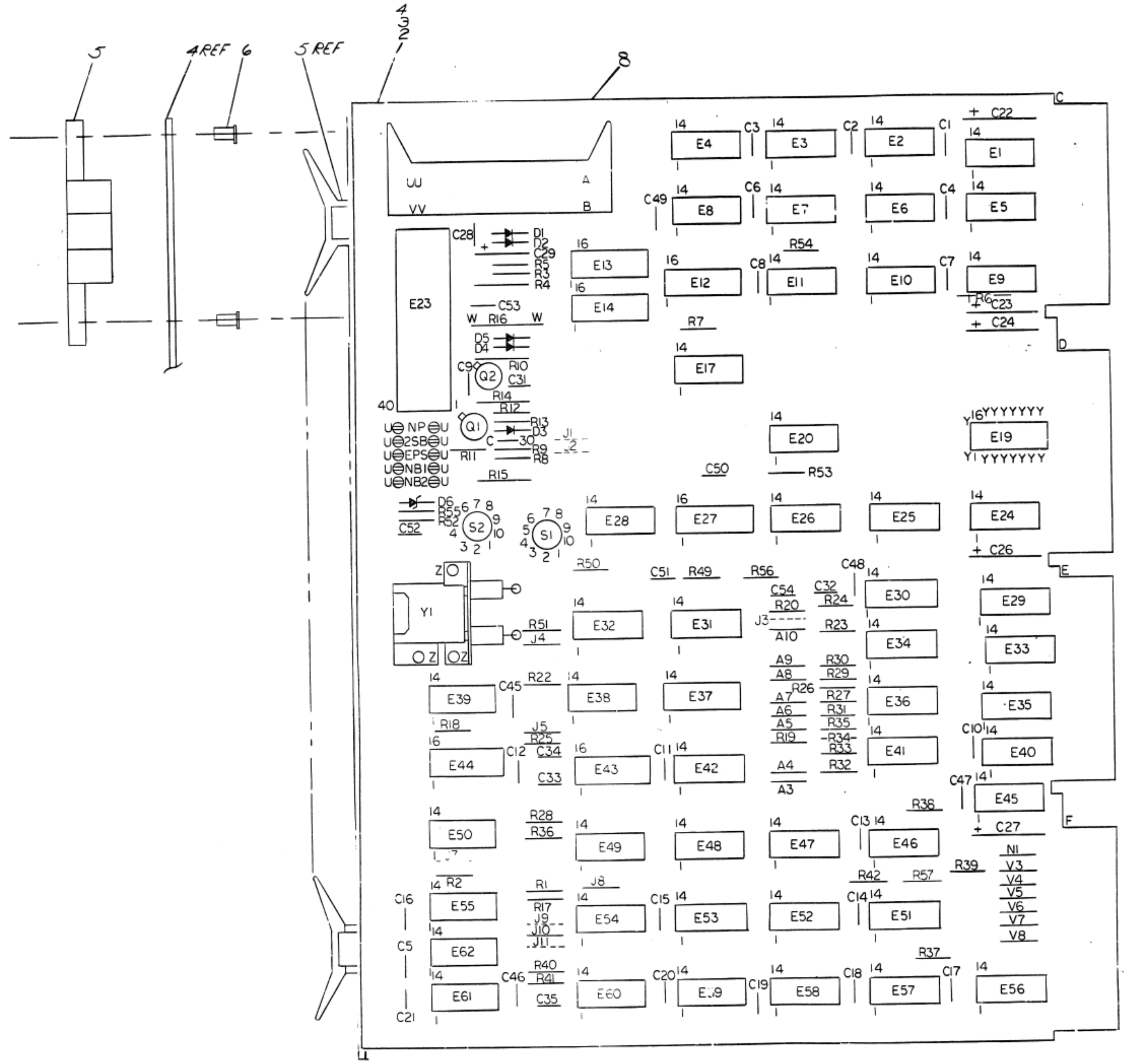
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1
3	D-UA-BCØ5C-25	CABLE MODEM BCØ5C	-	1	-	1	1
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-
5	D-CS-H315-Ø-1	MODEM TEST CONNECTOR	-	-	-	-	A/R See Note 2
6	E-CS-M7800-Ø-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1
7	~~A-PL-G8ØØØ-Ø-Ø~~	~~FILTER NETWORK~~	~~-~~	~~A/R~~	~~-~~	~~A/R~~	~~A/R See Note 1~~
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R See Note 3
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-
10	9008269	TRANSPARENT VINYL TAPE	A/R				

NOTES:

1. G8000 IS REQUIRED ONLY IN PDP11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A
2. ONE H315 PER PDP11 SYSTEM
3. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE OR BY THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.
4. APPLY TAPE TO TOP SURFACES OF CRYSTAL AND MOUNTING BRACKETS TO INSULATE FROM ADJACENT MODULES.
5. PRIORIY LEVELS 5.6, or 7 MAY BE SPECIFIED BY THE CUSTOMER OR THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø	A	PL	DL11-Ø-Ø	F	DL11-00009
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
ORA 110



NOTES:

1.) PIN NOTATION THROUGHOUT IS ORIENTED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

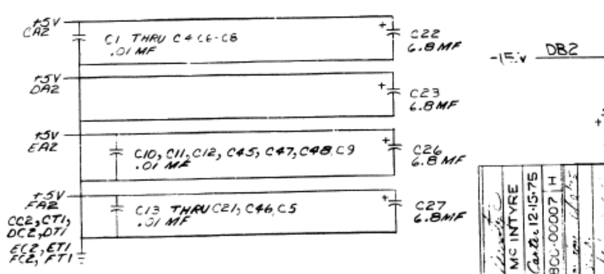
2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J4-J5, J8, J10, V3-V8, AND [illegible].

3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).

4.) DEC 8640S WERE [illegible] REPLACEMENTS ANY 380 [illegible] SHOULD BE REPLACED BY 8640'S, EXCEPT E28. E28 MUST BE REPLACED WITH A 7380 [illegible]

PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F



DEC [illegible]	5	16	—	—
[illegible]				
DEC UART	3		--	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	[illegible]	5	—	—
DEC 74153	8	16	—	—
DEC [illegible]	[illegible]	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—
IC TYPE	GND	+5V	[illegible]	[illegible]

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
3		WASHERS, INTERNAL TOOTH LOCK	[illegible]	
1	E28	IC DEC 7380	1912[illegible]	
19	J1 THRU J19	JUMPER [illegible]		
1	R3	RES 750Ω 1/4W 5%	1301[illegible]	
1	R38	RES 390 Ω 1/4 W, 5%	[illegible]	
1	D6	DIODE IN746A	1104860	65
2	Q1, Q2	TRANSISTOR 6534D	1503409-00	64
1	C53	CAP 100PF 100V 5% DIPPED MICA	1000016	63
1	C54	CAP 560PF 100V 5% DIPPED MICA	1000025	62
2	C50, C51	CAP .047MF CERAMIC	1009678	61
1	E27	IC DEC 74161	1910650	60
2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000023	59
1	C32	CAP 470PF 100V 5% DIPPED MICA	1000024	58
1	C31	CAP 1000PF 100V 5% DIPPED MICA	1000042	57
29	C1-C21, C28, C30, C45-C49, C52	CAP .01UF 100V 20% CERAMIC DISC	1001610	56
1	C29	CAP .47UF 35V 10% TANT	1005965	55
5	C22-C24, C26, C27	CAP 6.8 UF 35V 20% TANT	1000067	54
1	C33	CAP 150PF 100V 5% DIPPED MICA	1000010	53
2	R14, R15	RES 1.5K 1/2W 5%	1300394	52
5	R23, R26, R40, R52, R55	RES 1K 1/4W 5%	1300365	51
1	R41	RES 47Ω 1/4W 5%	1300202	50
1	R10	RES 68 Ω 1/2W [illegible]	[illegible]	49
1	R5	RES 82Ω 1/4W 5%	1301477	48
1	R24	RES 100Ω 1/4W 5%	1300229	47
1	R11	RES 130Ω 1/4W 5%	1300250	46
2	R42, R57	RES 180Ω 1/4W 5%	1301322	45
1	R53	RES 220Ω 1/4W 5%	1300271	44
5	D1-D5	DIODE D664 20V [illegible] mA	11[illegible]	43
3	R9, R13, R51	RES 470Ω 1/4W 5%	1300316	42
1	R4	RES 560Ω 1/2W 5%	1300338	41
3		NUT HEX #2-56	90[illegible]	40
1	R16	RES 750Ω 1W 5%	1302385	39
26	R1, R2, R6, R7, R17-R21, R25, R27-R37, R39, R49, R50, R22, R54, R56	RES 10K 1/4W 5%	1300479	38
2	R8, R12	RES 1.5K 1/4W 5%	1300391	37
1	E23	IC DEC UART	1910459	36
4	E32, E55, E61, E62	IC DEC 7474	1905547	35
2	E36, E41	IC DEC 8242	1909712	34
3	E31, E49, E59	IC DEC 7408	1910135	33
3		SCR PHIL HD PAN #2-56 x 250	9[illegible]	32
2	E20, E26	IC DEC 7490	1909051	31
11	E1, E2, E5, E7-E9, E11, E30, E47, E51, E56	IC DEC 8881	1909705	30
2		AUGAT 8000 AG-1	12[illegible]	29
1	E43	IC DEC 74123	1910436	28
3	E48, E57, E52	IC DEC 74H74	1909667	27
3	E42, E54, E58	IC DEC 7400	190557[illegible]	26
1	E10	IC DEC 7413	1909989	25
2	E50, E53	IC DEC 7402	1909004	24
7	E3, E4, E33, E35, E40, E45, E46	IC DEC 8640	[illegible]	23
1	E12	IC DEC 74153	19[illegible]	22
1	E60	IC DEC 74H04	19099[illegible]	21
1	E25	IC DEC 7492	19090[illegible]	20
4	E6, E17, E38, E39	IC DEC 7404	190768[illegible]	19
1	E24	IC DEC 7493	1909054	18
1	E34	IC DEC 7410	190557[illegible]	17
1	E29	IC DEC 314	1909704	16
1	E37	IC DEC 7442	1910046	15
1	E44	IC DEC 8271	1909[illegible]5	14
2	E13, E14	IC DEC 74175	19106[illegible]	13
1		BRACKET, CRYSTAL HOLDER	530282[illegible]	12
1		BRACKET, CRYSTAL HOLDER	5303154	11
1	E19	IC SOCKET	12098[illegible]	10
2	S1, S2	SWITCH, SINGLE POLE, 10 POS	121004[illegible]	9
1		40 PIN CONNECTOR BERG	1209941	8
10		SPLIT LUGS	[illegible]06735	7
8		EYELET #GS4-7 E.B. STIMPSON	9006732	6
4		HANDLE, FLIP-CHIP, MAGENTA	9008337	5
1		ETCHED CIRCUIT BOARD	5009976	4
REF		MODULE ECO HISTORY	[illegible]	3
REF		ASSY/DRILLING HOLE LAYOUT	[illegible]	2
REF		X-Y COORDINATE HOLE	[illegible]	1

PARTS LIST

ETCH BOARD REV H

DEC NO	EIA NO	DEC NO	EIA NO
		G534D	MPS6539
		IN746A	1/4M3.3AZ
		D664	IN3606

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	CHK
A	M7800-00001	ORIGINATED

REVISIONS

JOHN MC INTYRE

digital EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE

SIZE E CODE CS NUMBER M7800 YA

NEXT HIGHER ASSY

SCALE

SHEET 1 OF 2

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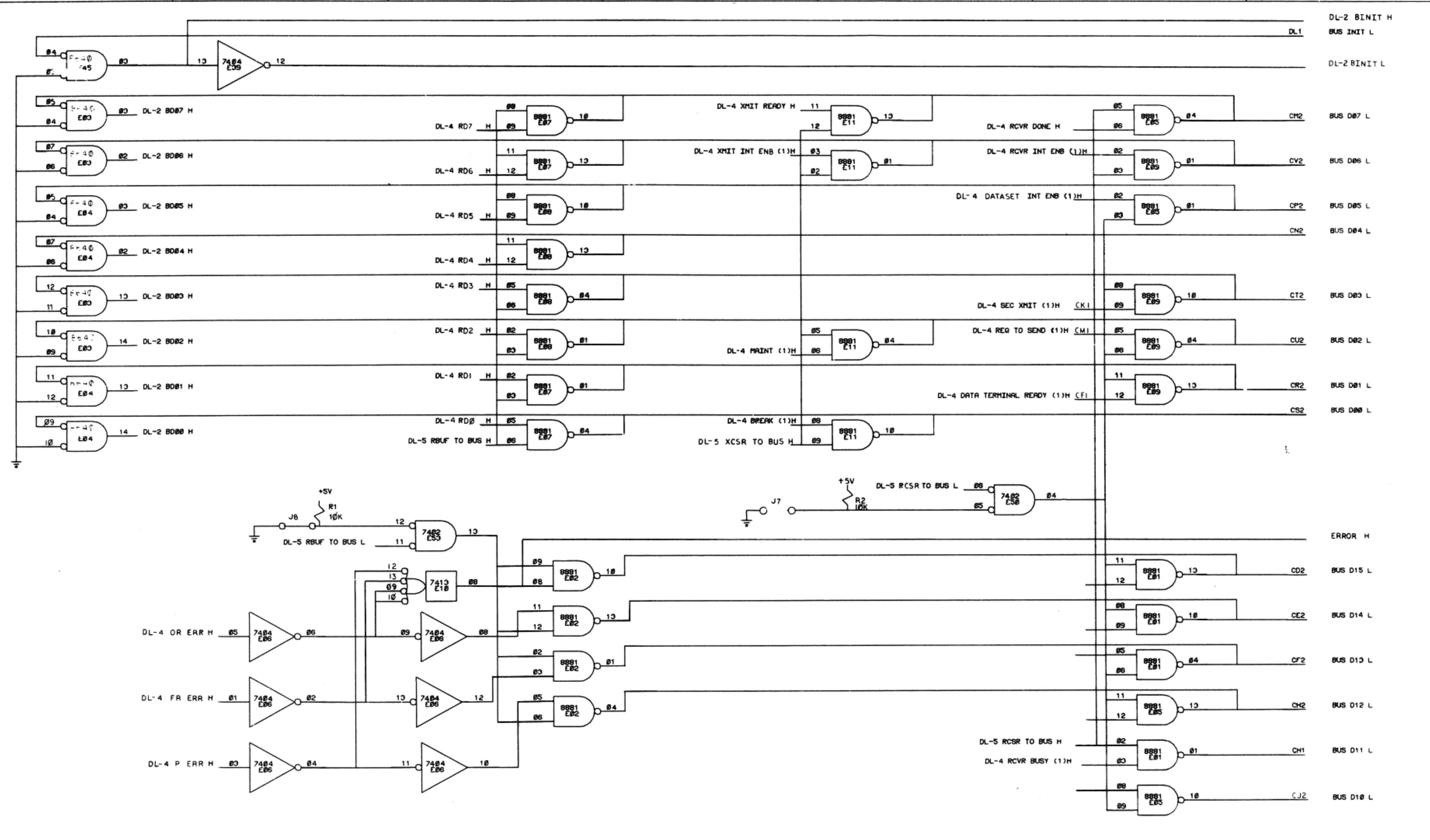


REVISIONS		
CHK.	CHANGE NO.	REV.
	M7800-YA-00005	J
	S. MASAND	

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —/—

FINISH —/—

NEXT HIGHER ASSY.

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

SIZE	CODE	NUMBER	REV.
D	CS	M7800 YA-1	

SCALE

SHEET OF 6

SEE NOTE 3

YI	844.8 KHZ		1.03296 MHZ		1.152 MHZ		4.608MHZ	
	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC
1	36.7	1700	44.8	1342	50	1250	200	312
2	55	1135	67.3	928	75	833	300	208
3	110	567	134.5	464	150	417	600	104
4	220	284	269	232	300	208	1200	52
5	440	142	538	116	600	104	2400	26
6	880	71	1076	58	1200	52	4800	13
7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
8	1760	35.5	2152	29	2400	26	9600	6.5
9	BERG CLOCK INPUT - COMMON TO RCVR AND XMIT							
10	EXTERNAL CLOCK INPUT - RCVR: DSI ; XMIT: DRI							

SWITCH POS.

PRIORITY PLUG E19

DL-3 BB IN H	DU2	Ø2	18 DD2	BUS BR7 L
DL-6 BB OUT H	DV2	Ø3	15 DE2	BUS BR6 L
BUS BG4 OUT H	DT2	Ø4	14 DF2	BUS BR5 L
BUS BG4 IN H	DB2	Ø5	13 DH2	BUS BR4 L
BUS BG5 OUT H	DR2	Ø6	12 DJ2	DL-6 REQUEST L
BUS BG5 IN H	DP2	Ø7	11 DK2	BUS BG7 IN H
BUS BG6 OUT H	DN2	Ø8	10 DL2	BUS BG7 OUT H
			Ø9 DM2	BUS BG6 IN H

DR1 EXT XMIT INPUT

DL-3 XMIT CLK H

(CC) BERG CLOCK INPUT

DSI EXT RCVR INPUT

DL-3 RCVR CLK H

DB1 TTL RDR ENB L

DL-4 RDR ENB (1)H

(PP) 6

READER RELAY

-15V (EE) 4

DC1 TTL SERIAL OUT L

(SS)

(AA) 5

20 MA TRANSMIT

(KK) 2

BERG CLOCK INPUT(CC)

BERG SERIAL IN L (E)

TTL SERIAL IN L

DL-4 MAINT (1)H

BERG CLK ENB L(HH)

DL-4 SERIAL OUT H

FRI DL-3 RCLK H

FSI DL-3 SI H

+5 (TT)

(A)

(B)

(VV)

(UU)

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.
3. ALTHOUGH THE ABOVE TABLE INCLUDES ONLY THE STANDARD DLII CRYSTALS OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER OR BY OTHER DOCUMENTATION OF AN OPTION WHICH USES THE DLII.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX = .005 .XX = .02 .X = .1 ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

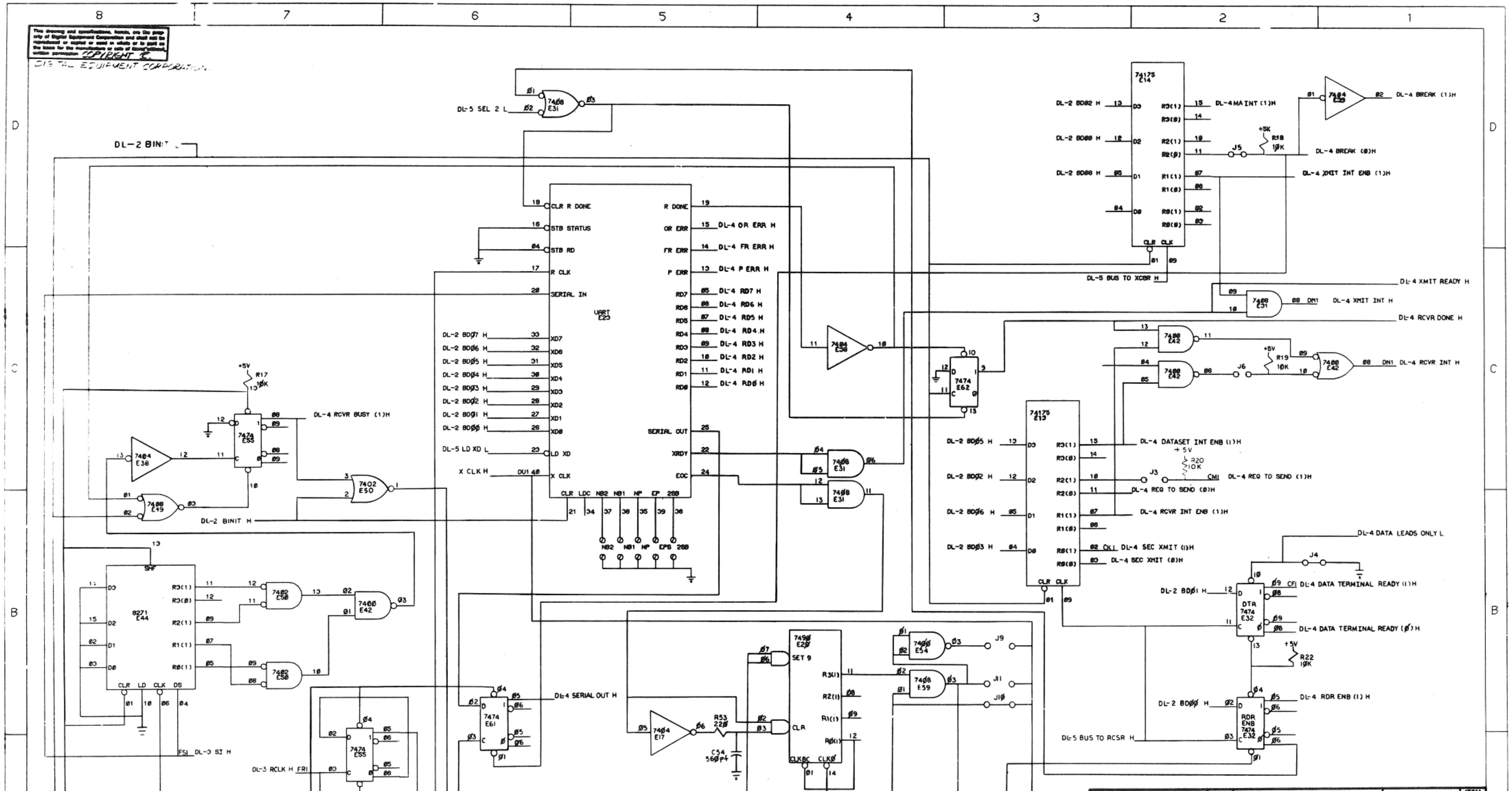
DRAWN — DATE
CHECK — DATE
ENG. — DATE
PROJ ENG. E. Fenton DATE 10/6/77
PROG — DATE
NEXT HIGHER ASSY. —
SCALE —
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3

SIZE	CODE	NUMBER	REV.
D	CS	M7800-YA-I	

DIST.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN. DATE

CHK'D. DATE

ENG. DATE

PROJ. ENG. DATE

PROD. DATE

NEXT HIGHER ASSY.

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4

SIZE	CODE	NUMBER	REV.
D	CS	M7800-YA-	

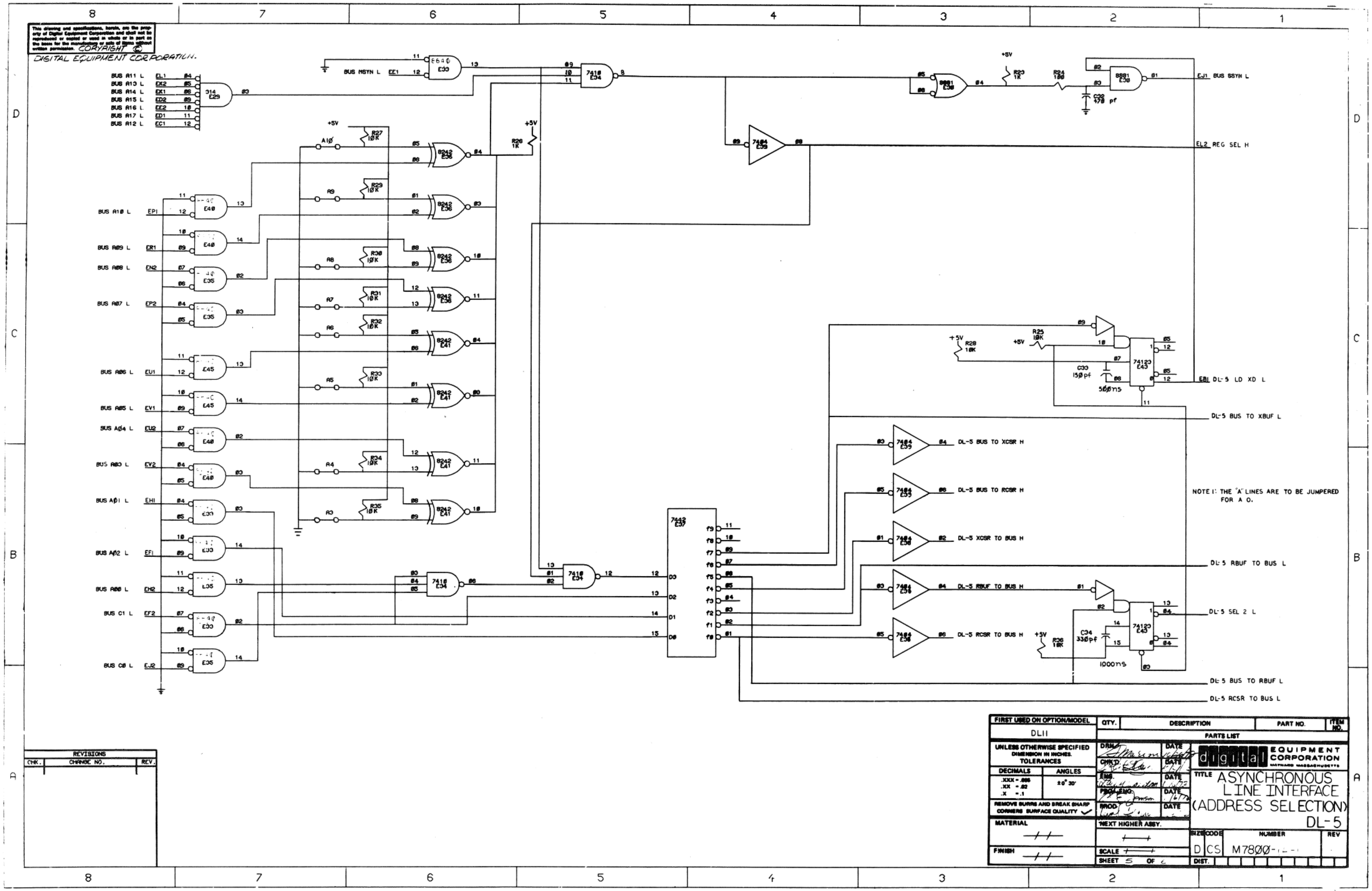
SCALE

SHEET 4 OF 6

DIST.

REVISIONS

CHK.	CHANGE NO.	REV.



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COPYRIGHT © DIGITAL EQUIPMENT CORPORATION.
BUS A11 L
BUS A13 L
BUS A14 L
BUS A15 L
BUS A16 L
BUS A17 L
BUS A12 L
BUS MSYN L
BUS A10 L
BUS A09 L
BUS A08 L
BUS A07 L
BUS A06 L
BUS A05 L
BUS A04 L
BUS A03 L
BUS A01 L
BUS A02 L
BUS A00 L
BUS C1 L
BUS C0 L
BUS SSYN L
EL2 REG SEL H
DL-5 LD XD L
DL-5 BUS TO XBUF L
DL-5 BUS TO XCSR H
DL-5 BUS TO RCSR H
DL-5 XCSR TO BUS H
DL-5 RBUF TO BUS L
DL-5 RBUF TO BUS H
DL-5 SEL 2 L
DL-5 RCSR TO BUS H
DL-5 BUS TO RBUF L
DL-5 RCSR TO BUS L
NOTE 1: THE "A" LINES ARE TO BE JUMPERED FOR A 0.
REVISIONS
CHK. CHANGE NO. REV.
FIRST USED ON OPTION/MODEL
DL11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS ANGLES
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
NEXT HIGHER ASSY.
SCALE
SHEET 5 OF 6
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5
SIZE CODE NUMBER REV
D CS M7800
DIST.

DL-4 RCVR INT H FU1

DL-4 XMIT INT H FV1

DL-3 BG IN H FB1

BUS NPR L FJ1

BUS BBSY L FD1

BUS SSYN L FC1

FP1 DL-6 REQUEST L

FA1 DL-6 BG OUT H

FT2 BUS SACK L

FC2 BUS DØ2 L

FL1 BUS DØ3 L

FN2 BUS DØ4 L

FF1 BUS DØ5 L

FH1 BUS INTR L

FF2 BUS DØ6 L

FH1 BUS DØ7 L

FK1 BUS DØ8 L

NOTE: THE 'V' LINES ARE TO BE JUMPERED FOR A 1.

REVISIONS

CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX = .005 .XX = .02 .X = .1 ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRWN DATE
CHKD DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY.
SCALE
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6

SIZE	CODE	NUMBER	REV.
D	CS	M78ØØ-YA-1	

DIST.

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WIRE TABLE

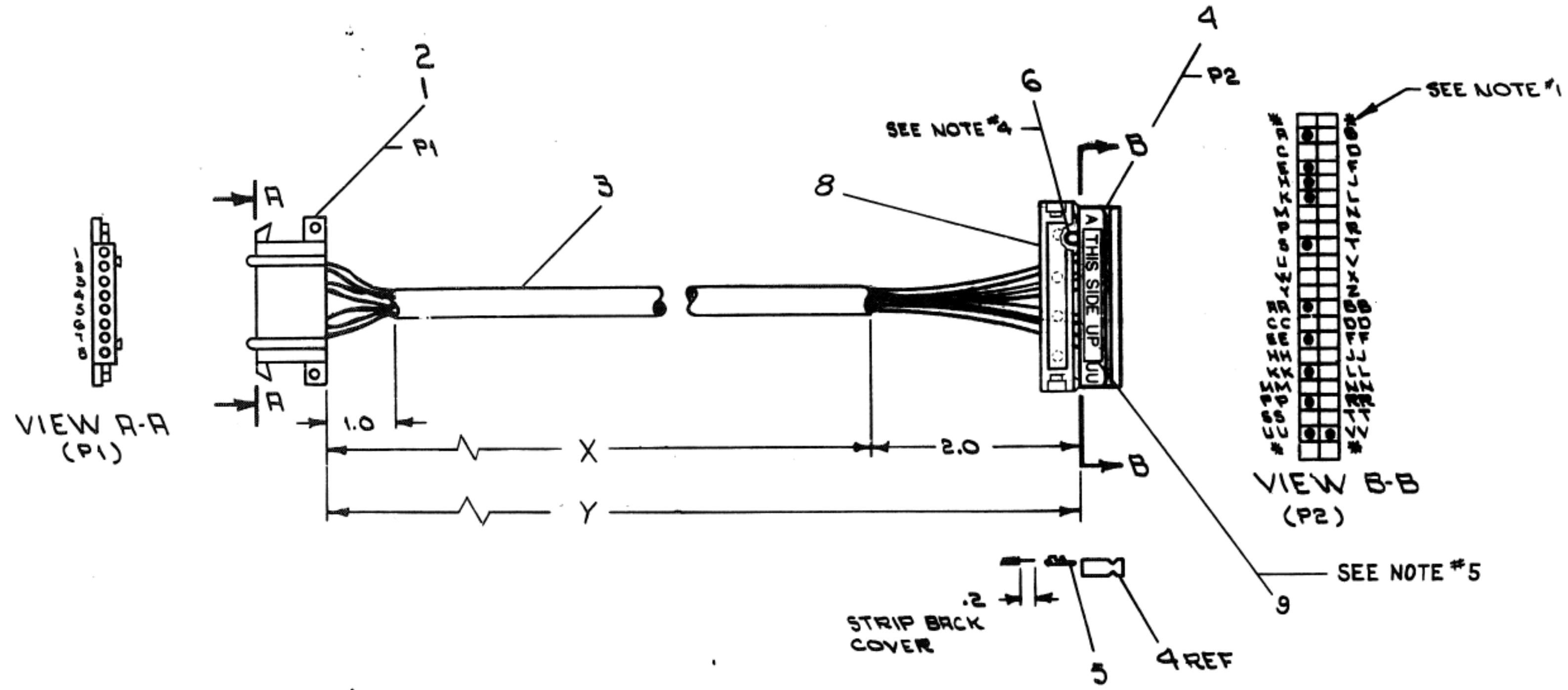
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	PAIR NO.	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
3	22	BLK	1	P1-2	2	P2-KK	5
3	↑	RED		P1-3	2	P2-S	↑
3,7		SHIELD		SEE NOTE #2	—	P2-A(NOTE #3)	
3		BLK	2	P1-4	2	P2-EE	
3		WHT		P1-5	2	P2-AA	
3,7		SHIELD		SEE NOTE #2	—	P2-UU(NOTE #3)	
3		BLK	3	P1-6	2	P2-PP	
3		GRN		P1-7	2	P2-K	
3,7	↓	SHIELD		SEE NOTE #2	—	P2-VV(NOTE #3)	↓
6	22	BLK	—	P2-E	5	P2-H	5

LEGEND

VARIATION	LENGTH X	LENGTH Y
7008360-0	25IN±1.0	27IN±1.0
7008360-1	46IN±1.0	48IN±1.0
7008360-9	9FT±2IN	9FT2IN±2IN

NOTES:

1. * ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM #6 (WIRE) TO BE APPROXIMATELY ONE (1) INCH LONG.
5. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.



QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	LABEL, THIS SIDE UP	361567	9
1	STRAIN RELIEF	12.1166	8
A/R	TUB. #18 TEF. THINWALL NAT	9107278-11	7
A/R	WIRE, #22 AWG STRD TEF BLK	9107350-00	6
11	SOCKET, CRIMP # 47216	1210089-07	5
1	HOUSING, BERG #65043-015	1210913-15	4
A/R	CABLE, BELDEN #8777-3PR SHLD	9107723-0	3
6	CONTACT MATE-N-LOCK (FEMALE)	1209379-03	2
1	CONN. MATE-N-LOCK (FEMALE)	1208340-00	1

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP-8E

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL: SEE PARTS LIST

FINISH

DRN.	[signature]	DATE 7 APR '71
CHK'D.	[signature]	DATE 4-8-71
ENG.	[signature]	DATE 4-8-71
PROJ. ENG.	[signature]	DATE 4-8-71
PROD.	[signature]	DATE

NEXT HIGHER ASSY: A-ML-KL8-E-0

SCALE: NONE

SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: CABLE ASSEMBLY (KL8E)

SIZE: D CODE: IA NUMBER: 7008360-0-0

DIST.

REVISIONS

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SOFTWARE LIST

MADE BY EMPellegrini DATE 8/29/72	CHECKED P. Janson DATE 8-30-72	SECTION
ENG P. Janson DATE 8/29/72	PROD J. Kelly DATE 8-31-72	ISSUED SECT.

LEGEND

- D DOCUMENT
- DN DOCUMENT CHANGE NOTICE
- PA PAPER TAPE ASCII
- PB PAPER TAPE BINARY
- PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
2	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
3	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 SOFTWARE LIST	SHEET 1 OF 1	A	SL	DL11-0-4		
		DIST.				

DEC FORM NO. DEC 16 (327)-1049 N471
DRA 120

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY	E. Pellegrini	CHECKED	SECTION
DATE	June 26, 1972	DATE 8-8-72	
ENG	Paul Janson	PROD	ISSUED SECT.
DATE	June 26, 1972	DATE 8-8-72	

LEGEND

- D DOCUMENT
- DN DOCUMENT CHANGE NOTICE
- PA PAPER TAPE ASCII
- PB PAPER TAPE BINARY
- PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	M7800	ASYNCHRONOUS LINE INTERFACE (EIA)	0	1	0	1	1				
2	G8000	FILTER NETWORK	0	A/R	0	A/R	A/R				
3	M7800-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)	1	0	1	0	0				
4	5408776	PRIORITY JUMPER LEVEL #4	1	1	1	1	1				
5	BC05-C-25	MODEM CABLE	0	1	0	1	1				
6	7008360	TTY CABLE	1	0	1	0	0				
7	-	CRYSTAL	1	1	1	1	1				
8	-	DL11 ENGINEERING DRAWINGS	1	1	1	1	1				
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL	1	1	1	1	1				
10	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
12	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				
13	H315	MODEM TEST CONNECTOR	0	0	0	0	A/B				

NOTES: 1. G8000 IS REQUIRED ONLY IN PDP-11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.

2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.

3. ONE H315 PER PDP11 SYSTEM

4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 CHECK LIST	SHEET 1 OF 1	A	AL	DL11-0-5	C	DL11-00005
		DIST.				

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE [illegible]

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P Janson	4-6-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	[illegible]	
E	CHANGE PER ECO	DL11-7	CONDON	8/74	[illegible]	
F	CHANGE PER ECO	DL11 8	CONDON	4-75	[illegible]	4/[illegible]

ENG	APPD	SIZE	CODE	NUMBER	REV
Paul E. Janson	[illegible]	A	SP	DL11-0-2	F

DEC FORM NO. DRA 107A

SHEET 1 OF 9

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of G8000 in systems where +15v is not available.
9. Filter capacitor selection for high baud rate current-loop.

A. OPERATION MODE:

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.

J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.

J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.

J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.

J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

SHEET 2 OF 9

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

J7. (con't)

OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.

J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.

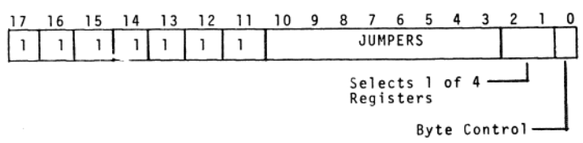
Summary of mode control jumpers:

JUMPER	A	B	C	D	F	DRAWING
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

*= don't care

B. REGISTER ADDRESS ASSIGNMENTS:

The DL11 can respond to addresses with the following format:



Bits 10 through 3 are controlled by jumpers A10 to A3. A jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

SHEET 3 OF 9

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

C. VECTOR ADDRESS ASSIGNMENT:

Jumpers V8 through V3 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XXØ and XX4 where XX ranges from ØØ to 77.

For the DL11-A and B used as a console device the vector address is 060/064. For additional units vectors are floating.

For the DL11-C,D, and E vector addresses are floating. Assign all C's first, then D's then E's.

D. PRIORITY ASSIGNMENT:

Interrupt priority is established by inserting a "priority plug" in the socket at IC location E19. For DL11-A B,C,D and E use level 4, for the standard assignment or level 5-7 as specified by the customer or the documentation of an option which uses the DL11.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

	ADDRESS	VECTOR	PRIORITY
DL11-A,B CONSOLE	777560 777562 777564 777566	60/64	BR4
DL11-A,B ADDITIONAL UNITS	776XXØ 776XX2 776XX4 776XX6	FLOATING	BR4

Where XX= 50 for line #1
and XX= 67 for line #16

	ADDRESS	VECTOR	PRIORITY
DL11-C,D,E	77XXXØ 77XXX2 77XXX4 77XXX6	Floating	4

Where XXX= 561 for line #1
and XXX= 617 for line #31

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

SHEET 4 OF 9

E. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KH11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

2. Parity

Parity is controlled by split lug pairs NP and EPS as follows:

NP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

G. Con't

transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud. this is closest to 1200 baud, position 6.

1050 X 960 = 10080000 = 1.008MHz.

The crystal frequency should not fall outside the range of the standard crystals. Although the above table included only the standard DL11 crystals other values may be specified by the customer or by other documentation of an option which uses the DL11.

DEC part number for the standard crystals are as follows:

844.8 KHz	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

*Use A or C cut crystals only. Do not use crystals marked NE-6D.

When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

H. G8000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot AØ2 of DD11-A.
2. Wire AØ3V2 to AØ2V2.
3. Wire AØ2N2 to CXXU1 where XX is the slot location of the M7800.

Refer to diagram 1.

I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

J. DL11-B,D,E in Systems with +15V available using DD11-A

There is a special situation of using a DD11-A to mount a DL11-B, D, Or E in systems with +15V available. These systems have +15V available and it appears at pin AØ3V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from AØ3V2 to CXXU1, where XX is the slot number of the DL11.
NOTE: this does not apply to DL11-A or C or DD11-B.

K. When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.

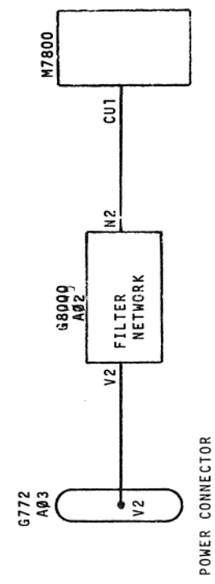
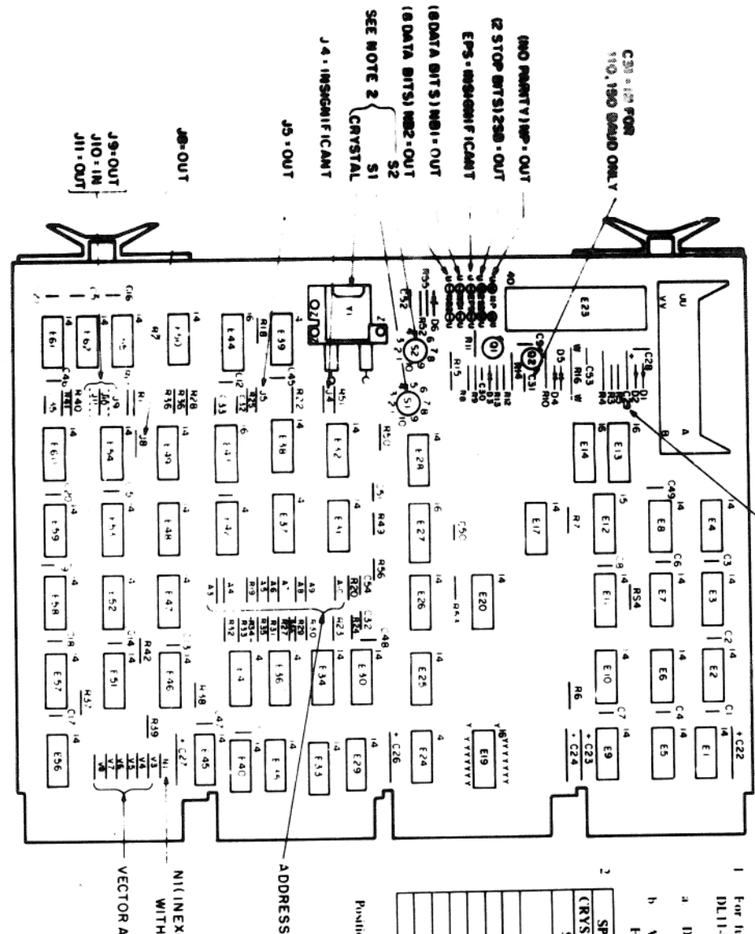


DIAGRAM 1. G8000 INSTALLATION

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE



NOTES

1. For further information on the DL11-A configuration or the installation of DL11-B, DL11-C, DL11-D or DL11-E refer to
   a. DL11 Asychronous Line Interface Manual
   b. A-SP-DL11-0-2 (DL11 installation procedure) in the DL11 Engineering Drawings.
2. Position 1 is most counterclockwise position

SPEED GROUP	1	2	3	4
(CRYSTAL FREQ (HZ)	4.4 MK	1.0136M	1.152M	4.608M
S1, S2 POS.	BAUD RATE			
1	36.7	44.8	50	200
2	55	67.3	75	300
3	110	134.5	150	600
4	220	269	300	1200
5	440	538	600	2400
6	880	1076	1200	4800
7	1320	1614	1800	7200
X	1760	2152	2400	9600

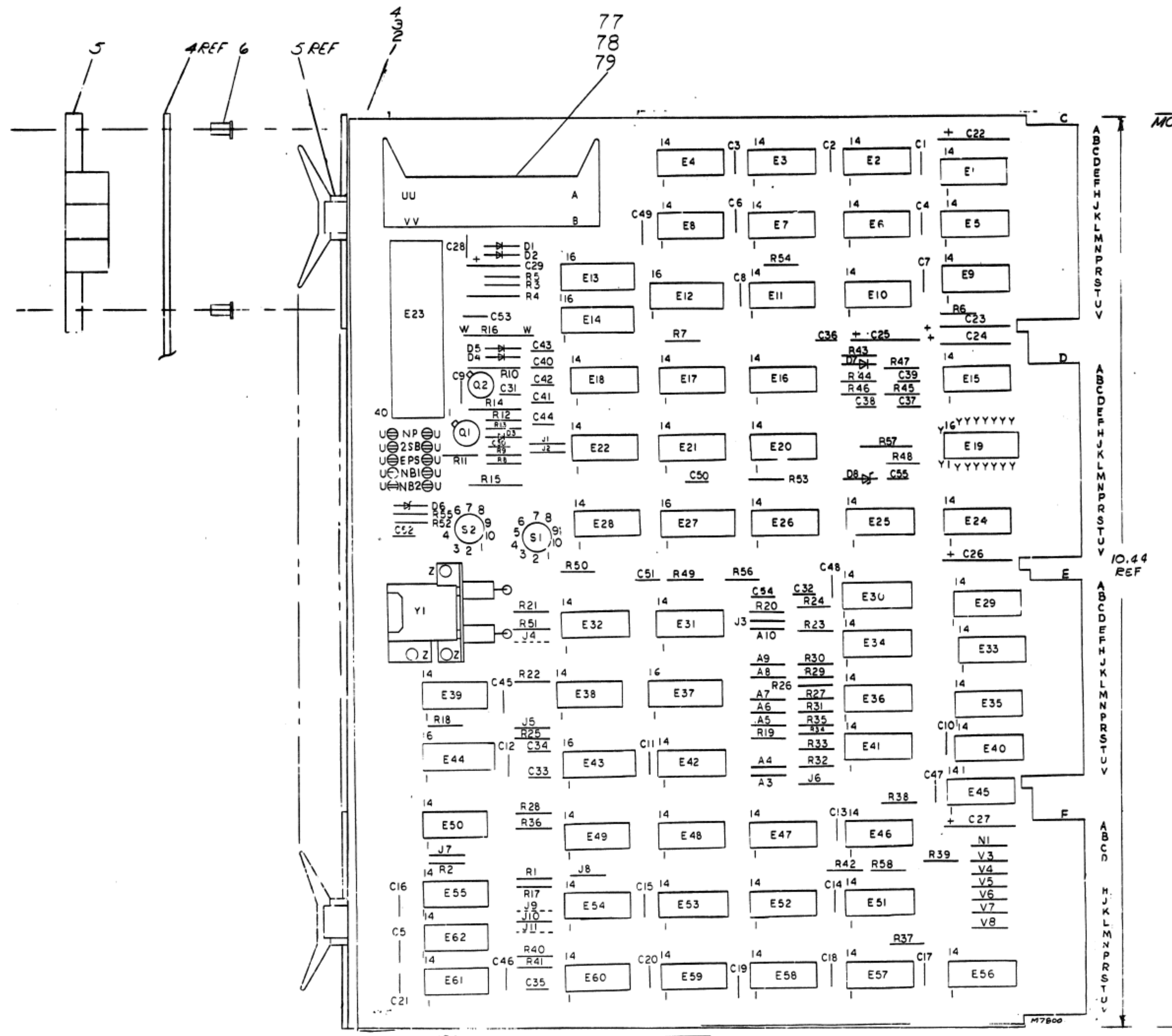
11-2454

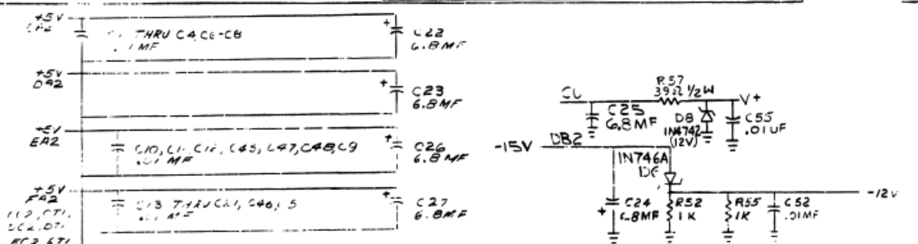
SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 9 OF 9

NOTES:
1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.
2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J1-J10, V3-V8, AND N1.
3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).
4. DEC 8640 WERE PHASED IN AS DEC 380 REPLACEMENTS. ANY 380 FAILURES SHOULD BE REPLACED BY 8640'S EXCEPT E28. E28 MUST BE REPLACED WITH A 7380.
5. FOR YC VERSION, C36 VALUE IS 1200PF.





PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F

YC QTY	QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
1	1	E28	IC DEC 7380	1910390	80
1	1		LATCH RIGHT	1209941-04	79
1	1		LATCH LEFT	1209941-03	78
1	1		CONNECTOR BERG	1209941-02	77
1	1		INSULATED JUMPER	9009185	76
1	0	C36	CAP [illegible] 100V 5%	[illegible]	75
A/R	A/R		WIRE #22 SOLID [illegible]	[illegible]	74
1	1	R57	RES 39, 1/2W, 5%	1302336	73
1	1	D8	DIODE, 4742, 12V 10%, 1W, ZENER	1104502	72
3	3		INT. WASHER #2	9006631	71
1	1	E27	IC DEC 14161	1910650	70
3	3		NUT, HEX #2	[illegible]	[illegible]
3	3		SCR PHL PAN HD #2-56X 1/4 LG	[illegible]	[illegible]
2	2		AUGAT 8000 PG-1	1202512	[illegible]
6	6	D1-D5, D7	DIODE D664 20V 100MA	[illegible]	[illegible]
1	1	D6	DIODE 1N746A	1104860	[illegible]
2	2	Q1, Q2	TRANSISTOR G534C	[illegible]	64
1	1	C53	CAP 100PF 100V 5% DIPPED MICA	[illegible]	[illegible]
1	1	C54	CAP 560PF 100V 5% DIPPED MICA	[illegible]	62
2	2	C50, C51	CAP .047MF CERAMIC	[illegible]	61
0	1	C36	CAP 220PF 100V 5% DIPPED MICA	1000021	60
2	2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000023	59
9	9	C32, C37-C44	CAP 470PF 100V 5% DIPPED MICA	1000029	58
1	1	C31	CAP 1000PF 100V 5% DIPPED MICA	1000042	57
30	30	C1-21, 28, 30, 45-49, 52, 55	CAP .01UF 100V 20% CERAMIC DISC	1001610-01	56
1	1	C29	CAP .47UF 35V 10% TANT	1005965	55
6	6	C22-C27	CAP 6.8 UF 35V 10% TANT	1005306	54
1	1	C33	CAP 150PF 100V 5% DIPPED MICA	1000019	53
2	2	R14, R15	RES 1.5K 1/2W 5%	1300394	52
6	6	R23, R26, R40, R48, R52, R55	RES 1K 1/4W 5%	1300365	51
1	1	R41	RES 47Ω 1/4W 5%	1300202	50
1	1	R10	RES 68Ω 1/2W 5%	1300405	49
1	1	R5	RES 82Ω 1/4W 5%	1301477	48
4	4	R24, R45, R46, R47	RES 100Ω 1/4W 5%	1300229	47
1	1	R11	RES 150Ω 1/4W 5%	1300250	46
2	2	R42, R58	RES 180Ω 1/4W 5%	1301322	45
2	2	R44, R53	RES 220Ω 1/4W 5%	1300271	44
1	1	R38	RES 390Ω 1/4W 5%	1300309	43
4	4	R9, R13, R43, R51	RES 470Ω 1/4W 5%	1300316	42
1	1	R4	RES 560Ω 1/2W 5%	1300338	41
1	1	R3	RES 750Ω 1/4W	1301401	40
1	1	R16	RES 750Ω 1W 5%	1302385	39
27	27	R1, R2, R6, R7, R17-R22, R25, R27-R37, R39, R49, R50, R54, R56	RES 10K 1/4W 5%	1300479	38
2	2	R8, R12	RES 1.5K 1/4W 5%	1300391	37
1	1	E23	IC DEC UART	1910459	36
4	4	E32, E55, E61, E62	IC DEC 7474	1905547	35
3	3	E15, E36, E41	IC DEC 8242	1909712	34
3	3	E31, E49, E59	IC DEC 7408	1910135	33
2	2	E18, E21	IC MC1489	1910323	32
2	2	E20, E26	IC DEC 7490	1909051	31
11	11	E1, E2, E5, E7-E9, E11, E30, E47, E51, E56	IC DEC 8881	1909705	30
1	1	E22	IC MC1488	1910322	29
1	1	E43	IC DEC 74123	1910436	28
3	3	E48, E57, E52	IC DEC 74H74	1909667	27
3	3	E42, E54, E58	IC DEC 7400	1903575	26
1	1	E10	IC DEC 7413	1909989	25
2	2	E50, E53	IC DEC 7402	1907004	24
7	7	E3, E4, E33, E35, E40, E45, [illegible]	IC DEC 8640	[illegible]	23
1	1	E12	IC DEC 74153	1909437	22
1	1	E60	IC DEC 74H04	1909931	21
1	1	E25	IC DEC 7492	1909059	20
5	5	E6, E16, E17, E38, E39	IC DEC 7404	1909686	19
1	1	E24	IC DEC 7493	1909054	18
1	1	E34	IC DEC 7410	1903376	17
1	1	E29	IC DEC 314	1909704	16
1	1	E37	IC DEC 7442	1910046	15
1	1	E44	IC DEC 8271	1909615	14
2	2	E13, E14	IC DEC 74175	1910651	13
1	1		BRACKET, CRYSTAL HOLDER	5302825	12
1	1		BRACKET, CRYSTAL HOLDER	5303154	11
1	1	E19	IC SOCKET	1209830	10
2	2	S1, S2	SWITCH, SINGLE POLE, 10 POS	1210042-1	9
~~1~~	~~1~~		~~40 PIN CONNECTOR BERG~~	~~1209941~~	~~8~~
10	10		SPLIT LUGS	9006735	7
8	8		EYELET #554-7 E.B. STIMPSON	9006732	6
4	4		HANDLE, FLIP-CHIP, MAGENTA	7008337-06	5
1	1		ETCHED CIRCUIT BOARD	5009978	4
REF	REF		MODULE ECO HISTORY	E-MH-M7800-0-6	3
REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7800-0-5	2
REF	REF		X-Y COORDINATE HOLE	K-CO-M7800-0-4	1

PARTS LIST

ETCH BOARD REV H

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.
G534D	MPS6534
1N746A	1N4M3.3AZ
D664	1N3606

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: ASYNCHRONOUS LINE INTERFACE

DRN. M. Peirce DATE 2/8/73

SIZE E CODE CS NUMBER M7800-0

SHEET 1 OF 7

DL-2 BDS7 H
DL-2 BDS6 H
DL-2 BDS5 H
DL-2 BDS4 H
DL-2 BDS3 H
DL-2 BDS2 H
DL-2 BDS1 H
DL-2 BDS0 H

DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H
DL-5 RBUF TO BUS H

DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H

DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H (CKI)
DL-4 REQ TO SEND (1)H (CMI)
DL-4 DATA TERMINAL READY (1)H (CFI)

DL 2 BINIT H
DL1 BUS INIT L
DL-2 BINIT L

CM2 BUS D07 L
CV2 BUS D06 L
CP2 BUS D05 L
CN2 BUS D04 L
CT2 BUS D03 L
CU2 BUS D02 L
CR2 BUS D01 L
CS2 BUS D00 L

+5V R1 10K — J8 — DL-5 RBUF TO BUS L
+5V R2 10K — J7 — DL-5 RCSR TO BUS L

DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H

ERROR H

DL-7 DATASET INT (1)H
DL-7 RING H
DL-7 CLEAR TO SEND H
DL-7 CARRIER H
DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H
DL-7 SEC REC DATA H

CD2 BUS D15 L
CE2 BUS D14 L
CF2 BUS D13 L
CH2 BUS D12 L
CH1 BUS D11 L
CJ2 BUS D10 L

REVISIONS		
CHK.	ECO NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS .XXX ± .005, .XX ± .02, .X ± .1; ANGLES ±0° 30'. REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓. MATERIAL —. FINISH —.

DRN. DATE — CHK'D DATE — ENG. DATE — PROJ. ENG. DATE — PROG. DATE

NEXT HIGHER ASSY —. SCALE —. SHEET 2 OF —.

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

SIZE C | CODE | NUMBER M7800-0-1 | REV. D | DIST

SEE NOTE 3

YI		844.8 KHZ		230.4 KHZ		115.2 KHZ		460.8KHZ	
		BAUD	USEC	BAUD	USEC	BAUD	USEC	BAUD	USEC
SWITCH POS.	1	36.7	1700	44.8	1342	50	1250	200	312
	2	55	1135	67.3	928	75	833	300	208
	3	110	567	134.5	464	150	417	600	104
	4	220	284	269	232	300	208	1200	52
	5	440	142	538	116	600	104	2400	26
	6	880	71	1076	58	1200	52	4800	13
	7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
	8	1760	35.5	2152	29	2400	26	9600	6.5
	9	BERG CLOCK INPUT- COMMON TO RCVR AND XMIT							
	10	EXTERNAL CLOCK INPUT-RCVR; DSI;XMIT DRI							

DL-3 BR IN H	DU2	02	16	DD2 BUS BR
DL-6 BR OUT H	DV2	03	15	DE2 BUS BR
BUS BG4 OUT H	DT2	04	14	DF2 BUS BR
BUS BG4 IN H	DS2	05	13	DH2 BUS BR
BUS BG5 OUT H	DR2	06	12	DJ2 DL-6 REQUEST L
BUS BG5 IN H	DP2	07	11	DK2 BUS BG7 IN H
BUS BG6 OUT H	DN2	08	10	DL2 BUS BG7 OUT H
			09	DM2 BUS BG6 IN H

PRIORITY PLUG E19

DR1 EXT XMIT INPUT

DL-3 XMIT CLK H

(CC) BERG CLOCK INPUT

DSI EXT RCVR INPUT

DL-3 RCVR CLK H

DB1 TTL RDR ENB L

DL-4 RDR ENB (1)H

(PP)

-15V (EE)

DC1 TTL SERIAL OUT L

(SS)

(AA)

-15V (KK)

+5 (TT)

(A)

(B)

(VV)

(UU)

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. (XAMPLE(X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.
3. ALTHOUGH THE ABOVE TABLE INCLUDES ONLY THE STANDARD DLII CRYSTALS, OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER OR BY OTHER DOCUMENTATION OF AN OPTION WHICH USES THE DLII.

REVISIONS

CHK	CHANGE NO.	REV

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005	±0° 30'
.XX = .02	
.X = .1	

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN. DATE

CHK'D. DATE

ENG. DATE

PROJ. ENG. DATE

PROD. DATE

NEXT HIGHER ASSY

SCALE

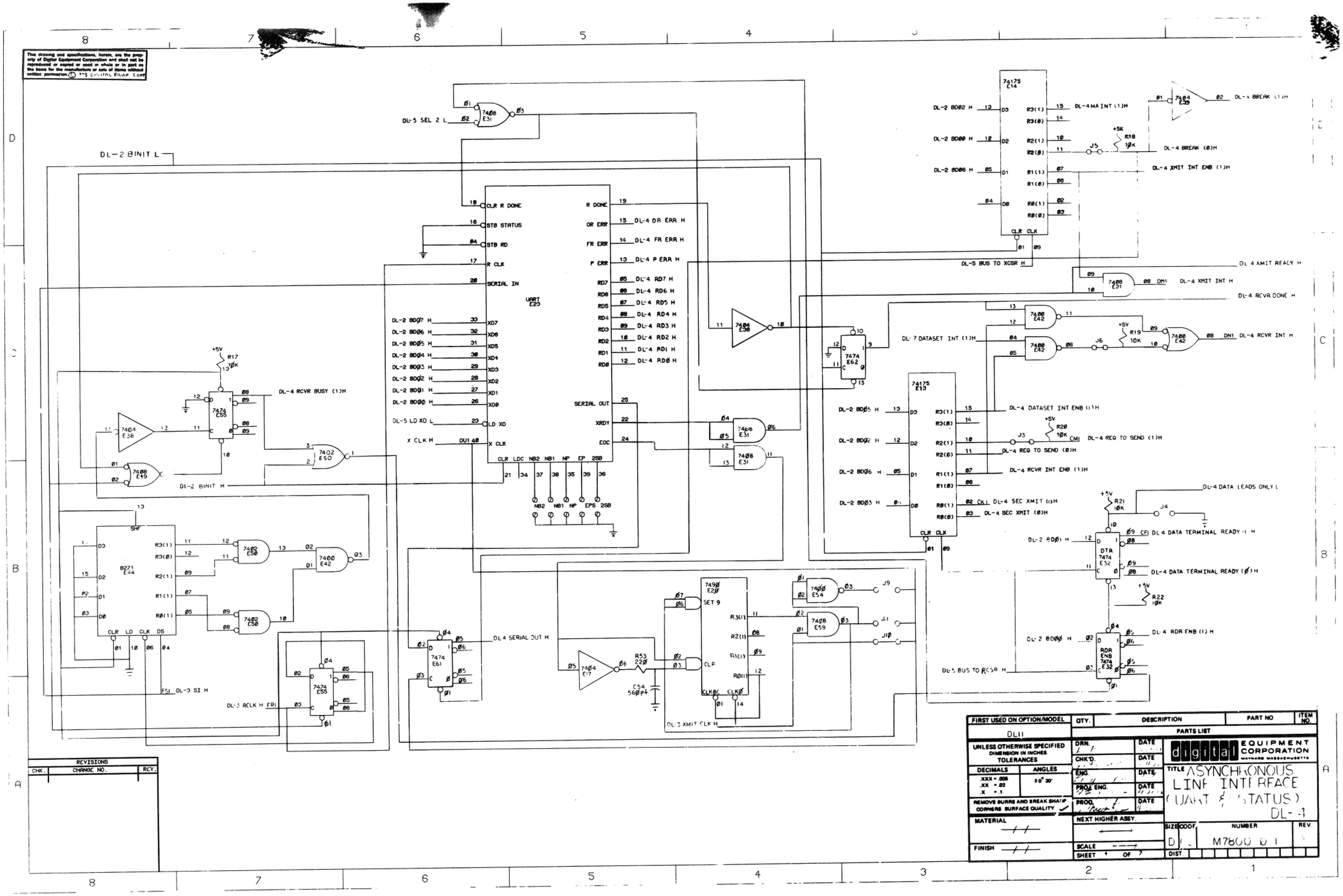
SHEET 3 OF 7

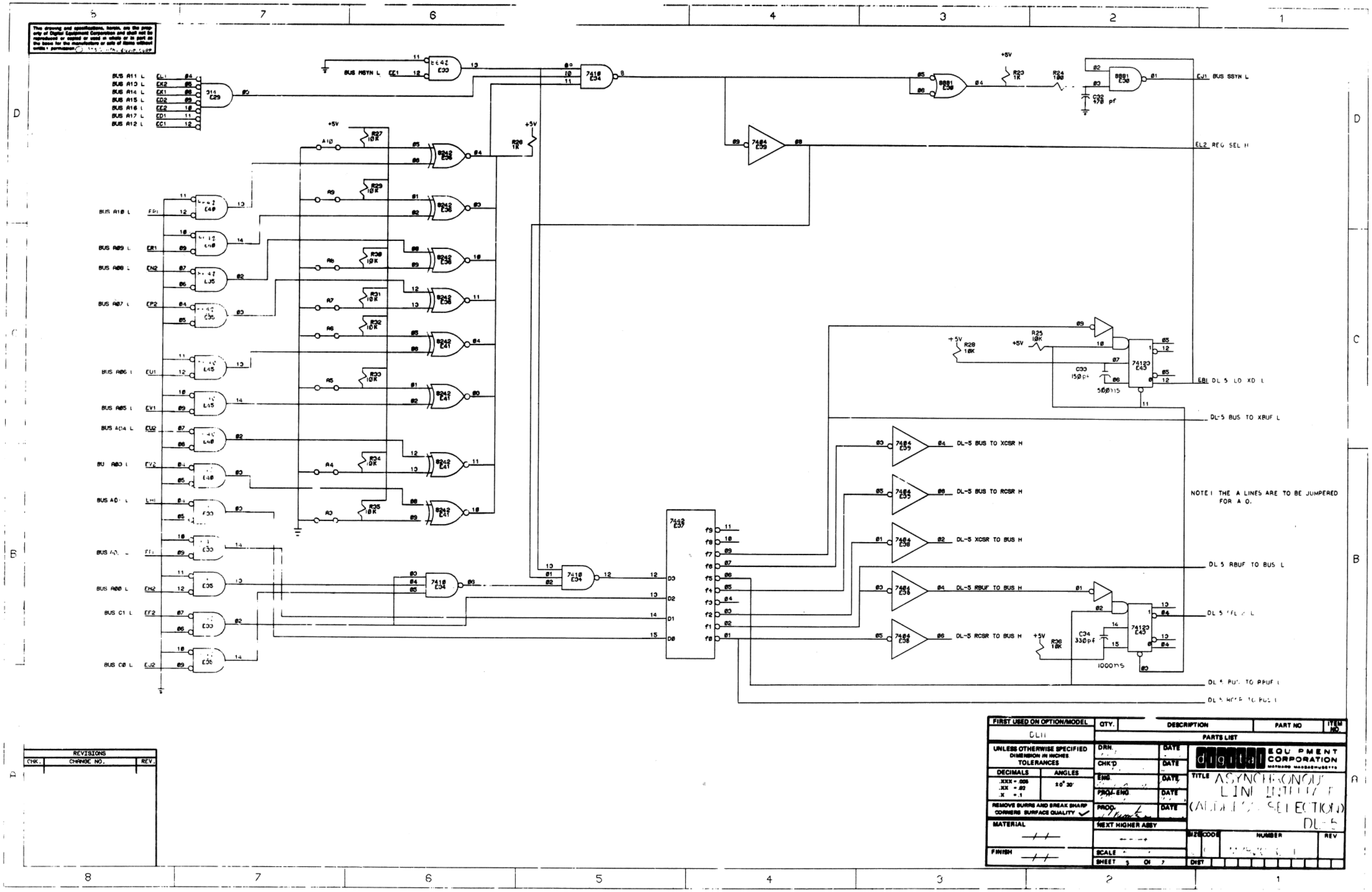
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK / CURRENT LOOPS) DL-

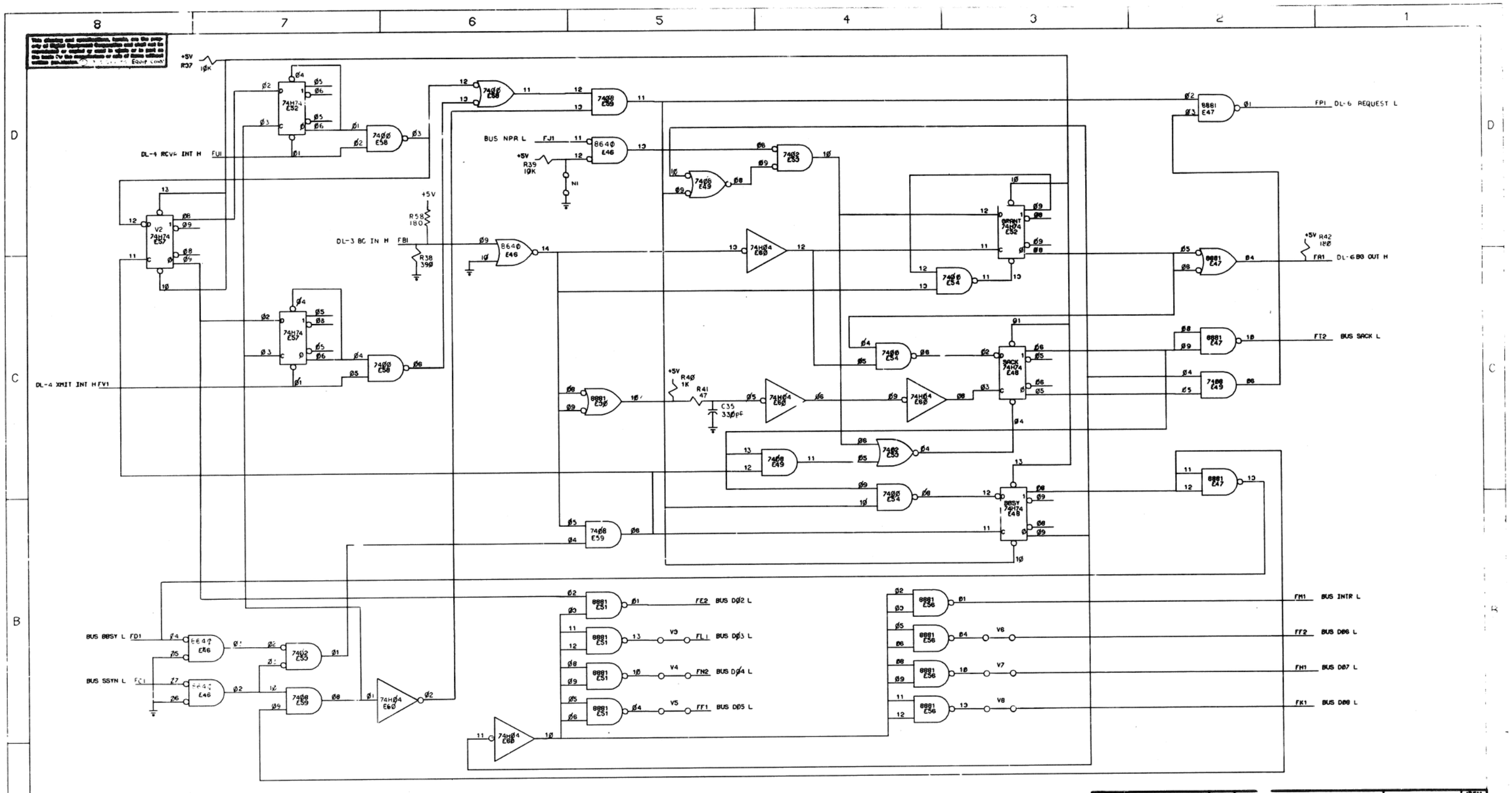
SIZE	CODE	NUMBER	REV
D		M7800 S 1	

DIST


This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission. © 1975 DIGITAL EQUIP. CORP.
DL-2 BINIT L
DL-5 SEL 2 L
UART E23
CLR R DONE
STB STATUS
STB RD
R CLK
SERIAL IN
R DONE
OR ERR
FR ERR
P ERR
SERIAL OUT
XRDY
EOC
DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H
DL-4 RCVR BUSY (1) H
DL-4 SERIAL OUT H
DL-4 MA INT (1) H
DL-4 BREAK (1) H
DL-4 BREAK (0) H
DL-4 XMIT INT ENB (1) H
DL-5 BUS TO XCSR H
DL-4 XMIT READY H
DL-4 XMIT INT H
DL-4 RCVR DONE H
DL-7 DATASET INT (1) H
DL-4 RCVR INT H
DL-4 DATASET INT ENB (1) H
DL-4 REQ TO SEND (1) H
DL-4 REQ TO SEND (0) H
DL-4 RCVR INT ENB (1) H
DL-4 SEC XMIT (1) H
DL-4 SEC XMIT (0) H
DL-4 DATA LEADS ONLY L
DL-4 DATA TERMINAL READY (1) H
DL-4 DATA TERMINAL READY (0) H
DL-4 RDR ENB (1) H
DL-5 BUS TO RCSR H
DL-3 SI H
DL-3 RCLK H
DL-3 XMIT CLK H
DL-5 LD XD L
X CLK H
DL-2 BINIT H
FIRST USED ON OPTION/MODEL
DL11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS .XXX = .005 .XX = .02 .X = .1
ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
QTY.
DESCRIPTION
PART NO
ITEM NO.
PARTS LIST
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
NEXT HIGHER ASSY.
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4
SIZE D
CODE
NUMBER M7800 0 1
REV
SCALE
SHEET 4 OF 7
DIST
REVISIONS
CHK.
CHANGE NO.
REV.



BUS A11 L
BUS A13 L
BUS A14 L
BUS A15 L
BUS A16 L
BUS A17 L
BUS A12 L
BUS MSYN L
BUS A10 L
BUS A09 L
BUS A08 L
BUS A07 L
BUS A06 L
BUS A05 L
BUS A04 L
BUS A00 L
BUS C1 L
BUS C0 L
+5V
EJ1 BUS SSYN L
EL2 REG SEL H
EB1 DL 5 LD XD L
DL-5 BUS TO XBUF L
DL-5 BUS TO XCSR H
DL-5 BUS TO RCSR H
DL-5 XCSR TO BUS H
DL 5 RBUF TO BUS L
DL-5 RBUF TO BUS H
DL-5 RCSR TO BUS H
NOTE: THE A LINES ARE TO BE JUMPERED FOR A 0.
REVISIONS
CHK.
CHANGE NO.
REV.
FIRST USED ON OPTION/MODEL
DL11
QTY.
DESCRIPTION
PART NO
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS
ANGLES
.XXX ± .005
.XX ± .02
.X ± .1
±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
DRN.
CHK'D
ENG.
PROJ-ENG
PROD.
DATE
NEXT HIGHER ASSY
SCALE
SHEET 3 OF 7
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5
SIZE
CODE
NUMBER
REV
DIST



REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005	±0° 30'
.XX = .02	
.X = .1	

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

		DATE
DRN.		
CH'K'D.		
ENG.		
PROJ. ENG.		
PROD.		

NEXT HIGHER ASSY.

SCALE

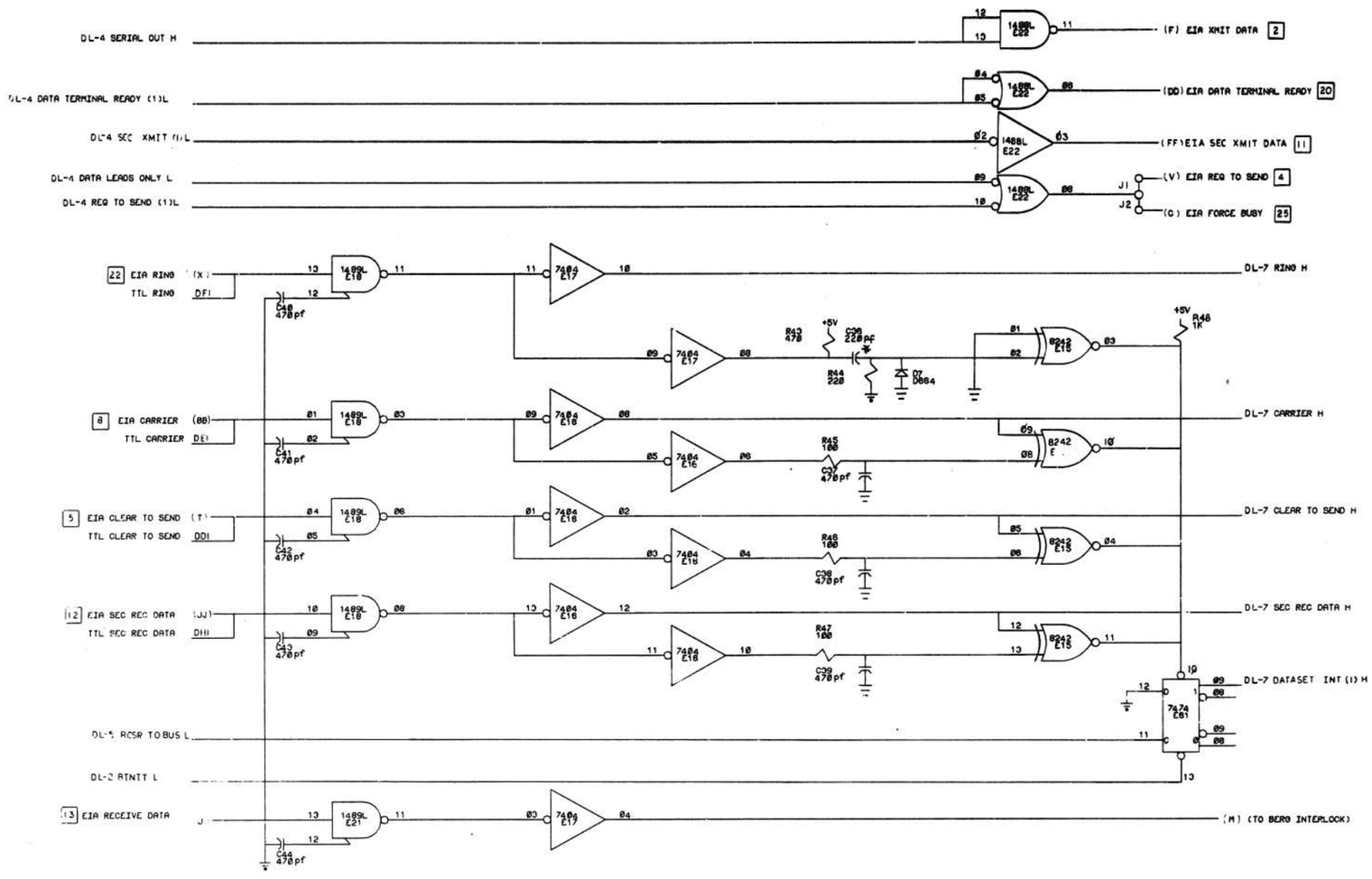
SHEET 8 OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6

SIZE	CODE	NUMBER	REV
D	CS	M7800-0-1	L

DIST.



NOTES:

1. LETTERS ENCLOSED - EXAMPLE (M) REFER TO PINS ON THE BERG CONNECTOR.
2. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC05-C CABLE. THIS CABLE ALSO CONNECTS BERG PINS M TO E.

REVISIONS		
CHK.	CHANGE NO.	REV.

REFER TO VERSION 030 FOR CHANGES TO THIS SHEET

FIRST USED ON OPTION/MODEL: DL11	QT	DESCRIPTION: PARTS LIST	PART NO / ITEM NO
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS .XXX = .005, .XX = .02, .X = .1; ANGLES ±0° 30'. REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
	CHK'D.	DATE	
	ENG.	DATE	TITLE: ASYNCHRONOUS LINE INTERFACE (EIA DRIVERS & RECEIVERS) DL-7
	PROJ. ENG.	DATE	
	PROD.	DATE	
MATERIAL	NEXT HIGHER ASSY.		SIZE D / CODE CS / NUMBER M7800-01
FINISH	SCALE		
	SHEET 7 OF 7		DIST.

WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
1	26	BLU/WHT	P1-1 *	SOLDER	J1-VV	7
		WHT/BLU	P1-2		J1-F	
		ORN/WHT	P1-3		J1-J	
		WHT/ORN	P1-4		J1-V	
		GRN/WHT	P1-5		J1-T	
		WHT/GRN	P1-6		J1-Z	
		BRN/WHT	P1-7 **		J1-UU	
		WHT/BRN	P1-8		J1-BB	
		SLA/WHT	P1-9		J1-Y	
		WHT/SLA	P1-10		J1-W	
		BLU/RED	P1-11		J1-FF	
		RED/BLU	P1-12		J1-JJ	
		ORN/RED	P1-13		J1-D	
		SLA/RED	P1-14		J1-LL	
1	26	SLA/GRN	P1-15	SOLDER	J1-N	7
1	26	RED/BRN	P1-16	SOLDER	J1-NN	7
		SLA	P1-17		J1-R	
		RED/SLA	P1-18		J1-U	
		BLU/BLK	P1-19		J1-P	
		BLK/BLU	P1-20		J1-DD	
		ORN/BLK	P1-21		J1-MM	
		BLK/ORN	P1-22		J1-X	
		GRN/BLK	P1-23		J1-RR	
		BRN/RED	P1-24		J1-L	
		RED/ORN	P1-25		J1-C	
		SHIELD	P1-1 *		J1-A	
1		SHIELD	P1-7 **		J1-B	7
3		BLK	P1-1 *	SOLDER	P1-7 **	SOLDER
2	26	RED	J1-E	7	J1-M	7

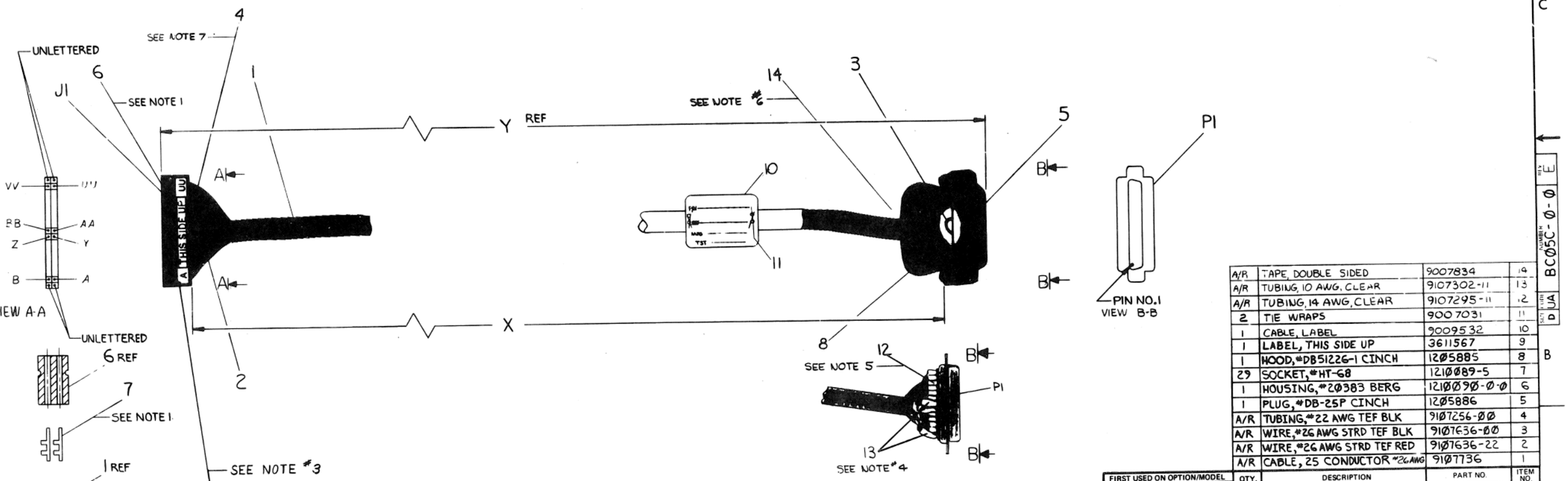
N.B * DENOTES THREE WIRES ARE SOLDERED INTO THE P1-1 SOLDER CUP
** DENOTES THREE WIRES ARE SOLDERED INTO THE P1-7 SOLDER CUP

LEGEND

NUMBER	VARIATION DIM X	VARIATION DIM Y (PRECUT)
BCØ5C-25	25'±3"	25'1.8"
BCØ5C-5Ø	5Ø'±2"	5Ø'1.8"
BCØ5C-Ø9	9'±3"	9'1.8"
BCØ5C-1F	18"±1"	19.8"

NOTES:

1. MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE HT68 FROM BERG ELECT
2. ONLY DEC PART #1210090-0-0 MAY BE USED AS J1.
3. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #6 (BERG HOUSING) AS SHOWN.
4. USE ITEM #13 (9107302-11) IN TWO PLACES (P1-1, P1-7) TO PREVENT SHORTING
5. USE ITEM #12 (9107295-11) ON ALL REMAINING SOLDER CUPS TO PREVENT SHORTING.
6. DUE TO ± TOLERANCES WITH DIFFERENT VENDORS, THE HOOD (ITEM #8) MAY VARY IN OUTSIDE DIAMETER CAUSING POTENTIAL STRAIN RELIEF GRIPPING PROBLEM. SHOULD THIS CONDITION BE PRESENT USE ITEM #14 (9107834) AT JUNCTION OF CABLE AND HOOD.
7. PLACE ITEM #4 (9107256) OVER SHIELD WIRE J1-A, J1-B, P1-1, P1-7.



A/R	DESCRIPTION	PART NO.	ITEM NO.
A/R	TAPE, DOUBLE SIDED	9007834	14
A/R	TUBING, 10 AWG, CLEAR	9107302-11	13
A/R	TUBING, 14 AWG, CLEAR	9107295-11	12
2	TIE WRAPS	9007031	11
1	CABLE, LABEL	9009532	10
1	LABEL, THIS SIDE UP	3611567	9
1	HOOD, #DB51226-1 CINCH	1205885	8
29	SOCKET, #HT-68	1210089-5	7
1	HOUSING, #20383 BERG	1210090-0-0	6
1	PLUG, #DB-25P CINCH	1205886	5
A/R	TUBING, #22 AWG TEF BLK	9107256-00	4
A/R	WIRE, #26 AWG STRD TEF BLK	9107636-00	3
A/R	WIRE, #26 AWG STRD TEF RED	9107636-22	2
A/R	CABLE, 25 CONDUCTOR #26 AWG	9107736	1

PARTS LIST

REVISIONS REV	CHANGE NO	CHK	DATE
A	BCØ5C-00001		7-14-72
B	BCØ5C-00002	E. Allen	10-29-73
C	BCØ5C-00003	V. BASTINANI	12 JULY 76
D	BCØ5C-00004	R. SMITH	8-7-76
E	BCØ5C-00005	R. SMITH	5/1977

DEC FORM NO 1080 100-A

FIRST USED ON OPTION/MODEL: DN11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX = .005 .XX = .02 .X = .1
ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

	NAME	DATE
DRN.	S Roberts	11/3/71
CHK.	L. Cook	11/5/71
ENG.	R. W. Smith	11/5/71
PROJ. ENG.	R. W. Smith	11/5/71
PROD.	[illegible]	11/3/71

NEXT HIGHER ASSY. —
SCALE NONE
SHEET 1 OF 1

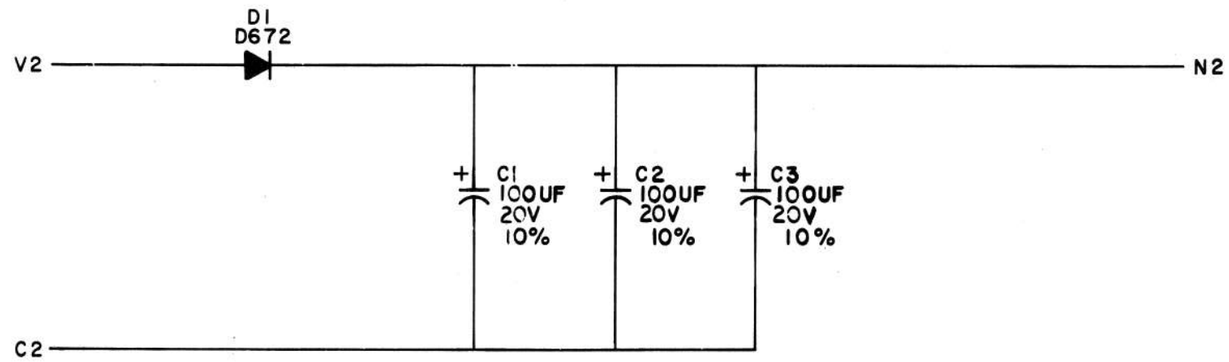
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: CABLE, MODEM BCØ5C

SIZE	CODE	NUMBER	REV
D	UA	BCØ5C-Ø-Ø	E

DIST.

SIZE	CODE	NUMBER	REV
B	CS	G8000-0-1	A



REVISIONS

DRN.	DATE
S. COOPER	1/19/71
CHK'D	DATE
	2/13/71
ENG.	DATE
R. Lucas	3/11/71
PROD.	DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D672	IN3653		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

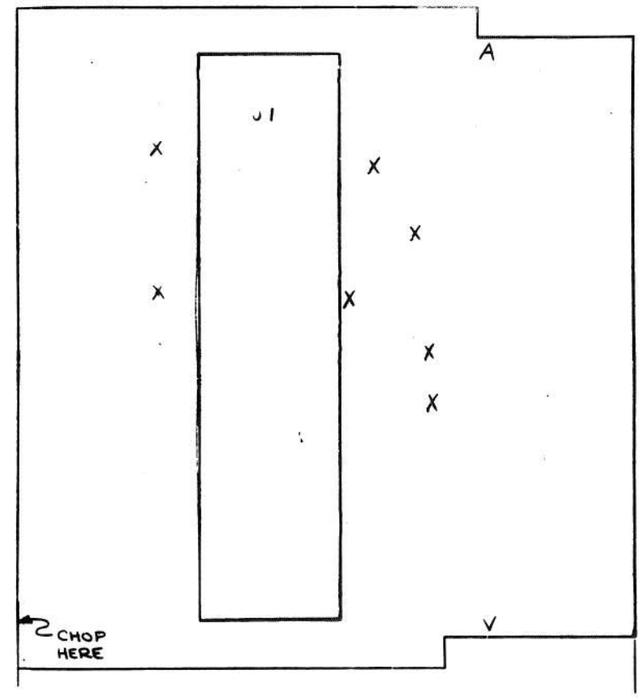
TITLE: FILTER NETWORK G8000

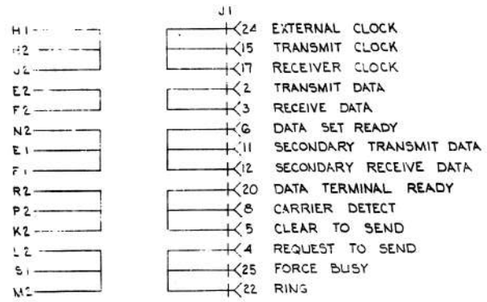
SIZE	CODE	NUMBER	REV
B	CS	G8000-0-1	A

PRINTED CIRCUIT REV: A

DIST. 324, 434, 435 2

4 PINK





QTY	REF. DESIGNATION	DESCRIPTION	DEC PART NO.	ITEM NO.
		PARTS LIST		
7		E LIST FEED THRU	9006731	
1	J1	CONN. CINCH DB-25S-3	121024?	
1		ETCHED CIRCUIT BOARD	501600	4
		MODULE ECO HISTORY	B-MM-H315-0-6	3
		ASSY/DRILLING HOLE LAYOUT	C-AH-H315-0-5	2
		X- COORDINATE HOLE LOCATION	K-CO-H315-0-4	1

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

ETCH BOARD REV A

REVISIONS					
CHK	CHANGE NO.	REV			
DEC NO.	EIA NO.	DEC NO.	EIA NO.	SEMICONDUCTOR CONVERSION CHART	

DRN. DATE
CH'D. DATE
ENG. DATE
PROJ ENG. DATE
PROD. DATE
NEXT HIGHER ASSY
SCALE
SHEET OF

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
CONNECTOR

SIZE D | CODE 05 | NUMBER | REV.
DIST

SIZE D | CODE 05 | 315-0-1 | REV