DEC-11-HR1B-D

PDP-11/20
system manual

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The material in this manual is for informational purposes and is subject to change without notice.

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

The PDP-11 series of manuals provides the user with the theory of operation and logic diagrams necessary to understand, operate, and maintain the PDP-11/20 System manufactured by Digital Equipment Corporation, Maynard, Massachusetts.

Each manual relates to a corresponding component of the PDP-11/20 System. This structure permits the manuals to be as modular as the system itself, resulting in maintenance documentation that is custom-tailored for each system.

The PDP-11/20 System Manual provides a general introduction to the basic 11/20 System and includes information on system operation. Thus, this manual offers a fundamental knowledge of the system and explains how to operate the console. This brief overview of the system is supplemented by references to other manuals in the series for detailed explanations of major system components.

The level of discussion in each manual assumes that the reader is familiar with basic digital computer theory. The maintenance philosophy presents information about normal system operation. This information enables the user to recognize trouble symptoms and to determine necessary corrective action. Each individual manual contains necessary theory of operation, diagrams, maintenance techniques, and logic drawings for the specific component covered.

The basic series consists of manuals covering: PDP-11/20 System, KA11 Processor, MM11-E Core Memory, KL11 Teletype Control, H720 Power Supply and BA11 Mounting Box, and manuals covering individual peripherals and options. A detailed explanation of the content of these manuals is given in Chapter 2.

For a comprehensive explanation of a specific item not covered in the basic series of manuals, the user should refer to the list of related PDP-11 documents in Paragraph 1.2.

An overall description of the basic PDP-11/20 System is contained in four sections: introduction, system description, system operation, and operating procedures.

1.2 APPLICABLE DOCUMENTS

PDP-11 documents that are not part of the basic PDP-11/20 series of manuals are listed in Table 1-1 in three main categories: general, hardware, and software. General documentation covers overall system descriptions, instruction set, addressing modes, and basic logic modules. Hardware documentation includes interfacing information, Unibus description, external device logic, and Teletype® maintenance. Software documentation contains only the basic programs necessary for developing, loading, running, and debugging applications. A current list of other available programs may be obtained from the DEC Program Library.

Documentation for specific peripherals and options that may be added to the PDP-11/20 system are not listed. When options or peripherals are added, appropriate manuals are included in the basic series of maintenance manuals.

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This series of manuals and the *Unibus Interface Manual* must be used together for a complete understanding of the PDP-11 System. The prime subject matter of this series is the processor; the prime subject matter of the interface manual is the Unibus, which connects the processor and peripherals.

Table 1-1
Applicable Documents

Title	Number	Description
	General	
PDP-11 Handbook	Second Edition, 1970	Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data.
Instruction List	None	Pocket-size list of instructions. Lists group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader.
Logic Handbook	DEC, 1970	Presents functions and specifications of the M-series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11.
	Hardware	
Unibus Interface Manual	DEC-11-HIAB-D	Used in conjunction with this manual. Provides detailed theory, flow, and logic descriptions of Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
Automatic Send-Receive Sets, Manual	Bulletin 273B, 2 volumes, Teletype Corp.	Describes operation and maintenance of the Model 33 ASR Teletype unit used as an input/output device with the PDP-11/20 System. Comparable manuals available for other Teletype models.
Model 33 Page Printer Set, Parts	Bulletin 1184B, Teletype Corp.	Contains an illustrated parts breakdown to serve as a guide for disassembly, reassembly, and parts ordering for the Model 33 ASR Teletype unit. Comparable manuals available for other Teletype models.

Table 1-1 (Cont)
Applicable Documents

Title	Number	Description
	Software	
Paper-Tape Software Programming Handbook	DEC-11-GGPA-D	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package.

1.3 ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each PDP-11/20 System (refer to Table 1-2). Each manual in the basic series has a second volume containing a complete set of reduced engineering drawings of the component described in the maintenance manual. The general logic symbols used on these drawings are described in the *DEC Logic Handbook*, 1970. Specific symbols as well as special ICs and circuits are discussed in both the *KA11 Processor Manual* and the *MM11-E Core Memory Manual.*

The reduced drawings in the engineering drawing manual reflect the latest print revisions and correspond to the specific component shipped to the user.

1.4 TERMINOLOGY

The final manual in the basic series, *PDP-11 Conventions*, includes a list of terminology and abbreviations used throughout the basic series as well as a glossary.

Table 1-2
Master Drawing List

PDP-11/20 System		
Title	**Sheets**	**Drawing**
PDP-11/20 Drawing Index	1	D-DI-11/20-0-1
KA11 Processor	1	A-ML-KA11-0
KY11 Console	1	A-ML-KY11-A
MM11-E Core Memory	1	A-ML-MM11-E
KL11 Teletype Control	1	A-ML-KL11-0
ASR33 Teletype (120V, 60-Hz model) ASR33 Teletype (240V, 50-Hz model)	1 1	A-ML-LT33-DC-0 A-ML-LT33-DD-0
Basic Assembly Configuration Basic Assembly Configuration (Parts List)	2 1	D-UA-11/20-0-0 C-PL-11/20-0-0
H720 Power Supply (120V model) H720 Power Supply (240V model)	1 1	A-ML-H720-A A-ML-H720-B
KA11 Processor		
Title	**Sheets**	**Drawing**
KA11 Processor	1	A-PL-KA11-0-0
Drawing Index	1	C-DI-KA11-0-1
Wired Assembly Wired Assembly (Parts List)	2 1	D-AD-7006537-0-0 A-PL-7006537-0-0

Table 1-2
Master Drawing List

KA11 Processor (Cont)				
Title			**Sheets**	**Drawing**
KA11 Block Diagram			1	D-BD-KA11-0-BD
Instruction Flow Diagram			1	D-FD-KA11-0-IFD
Bus Flow Diagram			1	D-FD-KA11-0-BF
Waveforms (Timing Diagram)			1	D-TD-KA11-0-WF
Timing and States	M728	K1	4	D-CS-M728-0-1
State Control	M727	K2	3	D-CS-M727-0-1
Priority	M824	K3	3	D-CS-M824-0-1
Register Control	M821	K4	3	D-CS-M821-0-1
Register	M225	K5	2	D-BS-KA11-0-REG
Data Path Control	M820	K6	5	D-CS-M820-0-1
Data Paths 1	M224	K7	2	D-BS-KA11-0-DP1
Data Paths 2	M224	K8	2	D-BS-KA11-0-DP2
Bus Interface & IR	M725	K9	5	D-CS-M725-0-1
IR Decode	M726	K10	4	D-CS-M726-0-1
Codes Data	M823	K11	2	D-CS-M823-0-1
Flag Control	M822	K12	3	D-CS-M822-0-1
Bus & Console Control	M724	K13	4	D-CS-M724-0-1
KA11 Bus & Power Connections		K14	1	D-IC-KA11-0-BP
Power Fail & Control	M825	K15	2	D-CS-M825-0-1
KA11 Console			1	A-ML-KY-11-A
Module Utilization			1	D-MU-KA11-0-MU
Module Utilization (Parts List)			1	A-PL-KA11-0-MU
Wire List			1	K-WL-KA11-0-WL
Maintenance Panel (Option)			1	A-ML-KM11-0
KL11 Teletype Control (Option)			1	A-ML-KL11-0
MM11-E Core Memory				
Title			**Sheets**	**Drawing**
Memory Stack			1	A-ML-H207-0
MM11-E Drawing Index			1	C-DI-MM11-E-01
Magnetics Logic Diagram			1	D-BS-MM11-E-02
Core Memory Stack			2	D-BS-MM11-E-03
Core Memory Sense & Inhibit			4	D-BS-MM11-E-04
Control and Timing			2	D-BS-MM11-E-05
Input/Output Connectors			1	D-IC-MM11-E-09
Module Utilization			1	D-MU-MM11-E-06
Module Utilization (Parts List)			1	D-PL-MM11-E-06
Wire List			1	K-WL-MM11-E-07
MM11-E Wired Assembly			2	D-AD-7006468-0-0
MM11-E Wired Assembly (Parts List)			1	A-PL-7006468-0-0
Timing and Flow			1	D-TD-MM11-E-08
Memory Levels and Gates			1	C-CS-G103-0-1
Planar Stack Board			1	C-CS-G616-0-1
X-Y Decoder Switch			1	D-CS-G226-0-1
Sense Inhibit Card			1	D-CS-G102-0-1
Device Select Module			1	B-CS-M109-0-1

Table 1-2 (Cont)
Master Drawing List

MM11-E Core Memory (Cont)

Title	Sheets	Drawing
MM11-E Control Logic	1	D-CS-M729-0-1
X & Y Current Generator	1	C-CS-G225-0-1
MM11-F Core Memory		
Title	**Sheets**	**Drawing**
Module Utilization	1	D-MU-MM11-F-02
Core Memory Stack	2	D-BS-MM11-F-03
Core Memory Sense & Inhibit	4	D-BS-MM11-F-04
Magnetics Logic Diagram	1	D-BS-MM11-F-05
I/O Connectors	1	D-IC-MM11-F-06
Wire List	22	K-WL-MM11-F-07
Timing and Flow	1	D-TD-MM11-F-08
Memory Levels and Gates, G103	1	C-CS-G103-0-1
Planar Stack Board, G616	1	C-CS-G616-0-1
X-Y Decoder Switch, G226	1	D-CS-G226-0-1
Sense Inhibit Card, G102	1	D-CS-G102-0-1
Device Select Module, M1091	1	B-CS-M1091-0-1
MM11-F Control Logic, M7290	1	D-CS-M7290-0-1
X & Y Current Generator, G225	1	C-CS-G225-0-1
KL11 Teletype Control		
Title	**Sheets**	**Drawing**
Teletype Control	1	A-PL-KL11-0-0
Drawing Index	1	C-DI-KL11-0-1
Teletype Transmitter & Receiver	4	D-CS-M780-0-1
Device Control	1	D-BS-KL11-0-2
Address Selector	1	C-CS-M105-0-1
Interrupt Control	1	D-CS-M782-0-1
Module Utilization	1	D-MU-KL11-0-MU
Module Utilization (Parts List)	1	A-PL-KL11-0-MU
M780 Receiver Timing	1	D-TD-KL11-0-6
M780 Transmitter Timing	1	D-TD-KL11-0-4
Option Arrangement	1	D-AR-KL11-0-5
KL11	1	A-SP-KL11-0-7

CHAPTER 2
SYSTEM DESCRIPTION

2.1 SCOPE

This chapter discusses major system components from a physical and functional point of view. Only a brief description is provided for each component as an introduction and overview of the basic PDP-11/20 System.

Paragraph 2.2 covers the physical components constituting the system. Paragraph 2.3 presents a brief functional description of each component, related specifications, and appropriate references to documents containing detailed information.

2.2 SYSTEM COMPONENTS

The PDP-11/20 System comprises five basic components: processor, programmer's console, core memory, Teletype with associated control, power supply, and mounting box. Table 2-1 lists each of the PDP-11/20 components and includes the name of the manual (or manuals) containing appropriate information; Table 2-2 lists possible variations to the basic system.

Table 2-1
Basic PDP-11/20 System

Major Component	Manual	Level of Discussion
KA11 Processor	*KA11 Processor*	Block diagram discussion, detailed theory of operation, flow diagrams, instruction set, and logic drawings.
	PDP-11/20 System	General operating procedures.
KY11-A Programmer's Console	*KY11-A Programmer's Console*	Theory of operation, flow diagrams, and logic drawings.
	PDP-11/20 System	Operating controls and indicators; basic operating procedures.
MM11-E Core Memory	*MM11-E Core Memory*	General discussion, detailed theory of operation, bus transactions, adjustments, maintenance aids, and logic drawings.
MM11-F Core Memory	*MM11-F Core Memory*	Same coverage as in MM11-E manual. Includes discussion of MM11-FP parity option.
Teletype Unit and KL11 Teletype Control	*PDP-11/20*	Teletype controls and indicators; on-line and off-line operating procedures.
	KL11 Teletype Control	KL11 theory of operation, adjustment and calibration, programming data, and logic drawings.

Table 2-1 (Cont)
Basic PDP-11/20 System

Major Component	Manual	Level of Discussion
		NOTE **Theory and maintenance of the Teletype is included in the Teletype Corp. manual supplied with each unit.**
Power Supply	*Power Supply and Mounting Box*	Block diagram discussion, theory of operation, adjustment, maintenance, and logic drawings.
Mounting Box	*Power Supply and Mounting Box*	Description and specifications of all mounting boxes and cabinets; system installation information.

Table 2-2
Possible PDP-11/20 Variations

Major Component	Possible Variations
KA11 Processor	None
*KY11-A Programmer's Console	None
Core Memory	*MM11-E, 4K x 16 bit, 1.2 μs cycle time MM11-F, 4K x 16 bit, 950 ns cycle time MM11-FP, an MM11-F with parity option MM11-H, 1K x 16 bit, 950 ns cycle time MM11-J, 2K x 16 bit, 950 ns cycle time MR11-A ROM memory, used with MM11-E, F, H or J; expandable to 28K. **NOTE** **MM11-E and F may be expanded up to 28K in 4K increments; each 8K segment is interleaved as described in appropriate memory manual.**
KL11 Teletype Control	*KL11-A (compatible with all possible Teletype versions) KL11-B, KL11-C, KL11-D, KL11-E, KL11-F: Similar to KL11-A. Differ primarily in baud rates as described in KL11 manual.

Table 2-2 (Cont)
Possible PDP-11/20 Variations

Major Component	Possible Variations
Teletype Unit	*33 ASR 33 KSR 35 ASR 35 KSR } Each unit is available in 120V or 240V models.
Power Supply	*H720-A (120V, 50/60 Hz) H720-B (240V, 50/60 Hz) H720-C (door-mounted version of Model A or E) H720-D (door-mounted version of Model B or F) H720-E (120V, 50/60 Hz) H720-F (240V, 50/60 Hz)
Mounting Box	*BA11-CS (basic box, rack-mountable) BA11-CC (basic box, table-top model) BA11-ES (extension box, rack-mountable) BA11-EC (extension box, table-top model)

NOTES:
1. An asterisk (*) indicates that this is the normal configuration shipped with the basic machine, unless otherwise specified by the customer.
2. Six basic models of the PDP-11/20 are designated with a model code to indicate the mounting configuration and input power requirements. These models are described in the *Power Supply and Mounting Box Manual.*

Options and peripherals added to the basic PDP-11/20 System are covered in a separate manual delivered with the system. Manuals are included only for those options specifically ordered with an individual system. It is beyond the scope of this document to present information on all available PDP-11 options.

2.3 FUNCTIONAL DESCRIPTION

The PDP-11/20 System is a 16-bit, general-purpose, parallel-logic computer using 1- and 2-address instructions and 2's complement arithmetic. The system contains a variable instruction length processor, which directly addresses all of core memory. All communication among system components (including processor and core memory) and peripherals is performed on a single high-speed bus, the Unibus. Because of the bus concept, device-to-device transfers can be accomplished at the rate of 2,500,000 words-per-second. All peripherals are in the basic system address space; therefore, all instructions are I/O instructions. All system components and peripherals are linked by the Unibus and power connectors. Subsequent paragraphs present a brief description of each system component and related specifications.

2.3.1 KA11 Processor

The KA11 processor decodes instructions, modifies data, makes decisions, and controls allocation of the Unibus among external devices. The processor contains eight hardware registers, which are used as arithmetic accumulators, index registers, autoincrement and autodecrement registers, and stack pointer registers. Two registers are specifically used for the processor's program counter and stack pointer.

Because of the flexibility of hardware registers, address modes, instruction set, and direct memory access, PDP-11/20 programs are written in directly relocatable codes. The processor also includes a full complement of instructions that manipulate byte operands, including provisions for byte swapping. Either words or bytes may be displayed on the programmer's console.

Any of the eight internal registers can be used to build last-in, first-out stacks. One register serves as a processor (or machine) stack pointer for automatic stacking. This stack handling capability permits save and restore of the program counter and status word in conjunction with subroutine calls and interrupts. This feature allows true reentrant codes and automatic nesting of subroutines.

The Unibus is used by the processor and all peripheral devices; therefore, there must be a priority structure to determine which device becomes bus master. A device generally requests use of the bus to make a nonprocessor transfer of data directly to or from memory, or to interrupt program execution and force the processor to branch to an interrupt service routine. A nonprocessor request (NPR) is granted by the processor at the end of bus cycles and allows device-to-device data transfers without processor intervention. A bus request (BR) is granted by the processor at the end of an instruction and allows the device to interrupt the current processor task. The entire instruction set is then available for manipulating device registers.

The processor recognizes four levels of hardware bus requests; each major level contains sublevels. Many devices can be attached on each major level with the device that is electrically closest to the processor given priority over other devices on the same priority level. The priority level of the processor itself is programmable within the hardware levels; therefore, a running program can select the priority level of permissable interrupts.

Additional speed and power are added to the interrupt structure through the use of the PDP-11/20 fully vectored interrupt scheme. With vectored interrupts, the device identifies itself, and a unique interrupt service routine is automatically selected by the processor. This eliminates device polling, and permits nesting of device service routines. The device interrupt priority and service routine priority are independent to allow dynamic adjustment of system behavior in response to real-time conditions. General processor specifications are listed in Table 2-3. A detailed description of the processor is presented in the *KA11 Processor Manual.*

2.3.2 KY11-A Programmer's Console

The console is an integral part of the KA11 processor and provides the programmer with a direct system interface. The KY11-A programmer's console allows the user to start, stop, load, modify, or continue a program. The console switches also allow the user to step through a program a single instruction or a single bus cycle at a time. Console displays indicate data and address flow as well as major machine states; thus, operation can be monitored.

Table 2-3
KA11 Processor Specifications

Data Paths	
16-bit, parallel paths	
Registers	
Number:	8 high-speed solid-state registers within processor
Functions:	Used as accumulators, 16-bit index registers, and autoincrement or autodecrement registers.
	All registers may be used as stack pointers.
	Register 6 is the processor stack pointer. Register 7 is the program counter.
Instructions	
Number:	Multiple address modes used with the basic instruction set provide over 400 instructions.
	Complete complement of separate byte instructions.
Deferral:	One or two levels of deferral
Address modes:	8 address modes; 4 additional modes available by using the program counter as an address register.
Direct addressing:	Direct addressing of up to 32K words (28,672 words of memory and 4,096 words of peripheral device registers)
	Direct addressing of up to 65K bytes (57,344 bytes of memory and 8,192 bytes of peripheral device registers)
Type:	Both single- and double-operand instructions
Priority:	The processor priority for obtaining bus control is programmable.

Table 2-3 (Cont)
KA11 Processor Specifications

Bus Requests (Priority Interrupts)	
Levels:	4 main hardware priority levels with additional sublevels
Response time:	7.2 μs. This includes storage of program counter and status word as well as establishment of a new program counter and status word.
Restore time:	4.5 μs. This includes restoring program counter and status word.
Non-Processor Requests	
	Highest priority request is granted at the end of bus cycles during instruction execution. It allows direct memory or device access data transfers to be accomplished between peripherals without processor intervention.
Power Fail/Restart	
	Power fail and automatic restart is standard on the KA11 processor. A trap occurs whenever ac power drops below 105V; power-down processing takes 2 ms. Power-up time required to restore the system is also 2 ms. The power supply must provide both an AC LO and DC LO signal for operation.
Power Requirements	
Power:	+5 Vdc ±5%; 8A, regulated
Logic signal levels:	Standard TTL
Environment	
Ambient temperature:	10° C to 50° C (50° F to 122° F)
Relative humidity:	20% to 95% (noncondensing)

The programmer's console is largely independent from the processor; it does require bus cycles for some operations but these are performed by the processor. When the console is used to step through a program either a single instruction or a single bus cycle at a time, the console gains control by issuing either a console bus request (CBR) (for single instruction) or console non-processor request (CNPR) (for single bus cycle). In either case, console priority supersedes all other priorities, including that of the processor.

The programmer's console is mounted as the front panel of the BA11 basic mounting box. All console logic circuits are mounted on the back of the panel.

Console operation, including descriptions of all controls and indicators, is presented in Chapter 3 of this manual. General specifications are listed in Table 2-4. Detailed descriptions of console logic circuits are covered in the *KY11-A Programmer's Console Manual.*

Table 2-4
KY11-A Programmer's Console Specifications

Indicators	
Displays:	18-bit ADDRESS REGISTER display
	16-bit DATA display
Lights:	8 lights, indicating the following conditions or operations: FETCH, SOURCE, DESTINATION, ADDRESS (2 lights), EXEC, BUS, RUN
Controls	
Switch register:	18-bit Switch register
Power switch:	3-position OFF-POWER-PANEL LOCK switch
Control switches:	LOAD ADDR (load address) EXAM (examine) CONT (continue) ENABLE/HALT S/INST-S/CYCLE (single instruction - single bus cycle)

Table 2-4 (Cont)
KY11-A Programmer's Console Specifications

	START DEP (deposit)
Priorities	
Bus Request:	Used only during single-instruction operation; highest BR priority in system
Non-Processor Request:	Used only during single-cycle operation; highest NPR priority in system
Power Requirements	
	+5 Vdc, ±5%; 0.5A -15 Vdc, ±3%; 0.1 A -20 Vdc, ±20%, unregulated; 0.2 A +8 Vdc, full-wave rectified, unfiltered, unregulated; 1.5 A
Environment	
Ambient temperature:	10° C to 50° C (50° F to 122° F)
Relative humidity:	20% to 95% (noncondensing)

2.3.3 MM11-E Core Memory

The MM11-E Core Memory used in the PDP-11/20 System is a random access, coincident current, magnetic core read/write memory with a cycle time of 1.2 μs and an access time of 500 ns. The memory consists of ferrite cores wired in a planar 3-D, 3-wire configuration that uses a shared sense/inhibit line. The basic memory unit can store 4096 (4K) 16-bit words.

The core memory uses the Unibus for data transfers to and from the processor and other devices; however, core memory is never bus master. Since the memory is always a slave device, a DATI or DATIP bus transfer indicates information transferred from memory into the bus master and a DATO or DATOB indicates information transferred out of the master into the memory. Because of the Unibus structure, the memory can be directly addressed by the processor or any other master device; every location in core can function as a true arithmetic accumulator.

The memory does not enter the priority structure, because it is never bus master. The master device, however, can request use of the memory through either a bus request (BR) or a non-processor request (NPR). Since the memory is completely independent of the processor, any master device can perform direct data transfers with memory without processor intervention.

The basic 4K core memory is mounted in the basic BA11 mounting box and occupies the space of a single system unit. There is space within the mounting box for two additional units of memory. If more than two additional units are desired, they must be mounted in an extension mounting box (BA11-E).

General memory specifications are listed in Table 2-5. A detailed description of the memory is presented in the *MM11-E Core Memory Manual.*

Table 2-5
MM11-E Core Memory Specifications

Read/Write Memory (4K)	
Cycle time:	1.2 μs
Access time:	500 ns
Word length:	16 bits
Core size:	4096 (4K) words
Expansion:	Expandable to 28,672 words in fields of 4096 words
Direct Memory Access	
Rate:	833,000 words per second

Table 2-5 (Cont)
MM11-E Core Memory Specifications

Maximum latency:	3.5 μs for highest priority device. Multiple device capability without necessity of multiplexer
Power Protection	
A DC OK signal inhibits operation of the core memory and protects the unit from low voltage levels, which could cause spurious operation.	
Power Requirements	
	+5 Vdc, ±5%; 2.5 A, memory active 1.5 A, memory inactive
	-15 Vdc, ±3%; 8.0 A, memory active 0.5 A, memory inactive
Environment	
Ambient temperature:	10° C to 50° C (50° F to 122° F)
Relative humidity:	20% to 95% (noncondensing)

2.3.4 KL11 Teletype Control

The KL11 Teletype Control provides an interface between the electromechanical Teletype unit and the PDP-11/20 Unibus. Serial information read or written by the Teletype unit is assembled or disassembled by the control for parallel transfer to, or from, the Unibus. The control also formats the data from the Unibus so that it is in the format required by the Teletype.

The Teletype control provides the flags that initiate these data transfers and cause a priority interrupt to indicate the availability of the Teletype unit.

The interface transfers data via the DATI and DATOB bus cycles. Although a DATO can be used, normal operation consists of a DATOB transfer, since the Teletype unit and Teletype control handle byte rather than word data. The interface can acquire bus control by a bus request (BR) and is normally set at the BR4 priority level. Since the interface operates by means of an interrupt, no non-processor request (NPR) can be made.

The Teletype control consists of three modules mounted on one quarter of a standard system unit. These three modules are: an address selector for decoding the incoming address from the bus, an interrupt control for generating the interrupt, and the receiver/transmitter module that performs the conversion and formatting functions.

Four Teletype control interfaces can be mounted in one system unit space of the basic BA11 mounting box. Each control provides an interface for a single Teletype unit.

General Teletype control specifications are listed in Table 2-6. These specifications for the control do not cover the Teletype unit; refer to the specific Teletype manual. A detailed description of the Teletype control is presented in the *KL11 Teletype Control Manual.*

Table 2-6
KL11 Teletype Control Specifications

Data Type	
Between control and Teletype unit	11-bit serial code consisting of marks and spaces. Marks and spaces correspond to idle and bias currents in the Teletype and 1s and 0s in the computer.
	Code consists of start bit, 8 data bits, and 2 stop bits.
	Data bits represent Teletype code which is modified ASCII; for any ASCII character, 200 octal is added.
Between control and Unibus	8-bit (byte) parallel code representing data portion of the 11-bit serial code

Table 2-6 (Cont)
KL11 Teletype Control Specifications

Data Transfers	
Speed:	100 ms for completion
Keyboard:	Buffer must be read within 18 ms to ensure no loss of data
Bus Cycles:	DATI or DATOB
Priority Level:	BR4
Selection:	BHI IN selects transfer from TTY to bus OUT LOW selects transfer from bus to TTY
Transmitter	
Registers:	Punch status register (TPS) – address 777564, 8-bit status word device register
	Punch buffer register (TPB) – address 777566, two 4-bit shift registers for parallel-to-serial conversion
Clock pulse:	9.09 ms wide
Vector address:	000064
Receiver	
Registers:	Reader status register (TKS) – address 777560, 8-bit status word device register
	Reader buffer register (TKB) – address 777562, two 4-bit shift registers for serial-to-parallel conversion
Clock pulse:	4.51 ms wide (twice the incoming bit rate)
Vector address:	000060
Power Requirements	
	+5 Vdc, ±5%; 1.6 A
	-15 Vdc, ±3%; 0.2 A
	NOTE **Additional power (ac) is required by the Teletype unit.**
Environment	
Ambient temperature:	10° C to 50° C (50° F to 122° F)
Relative humidity:	20% to 95% (noncondensing)
	NOTE **Additional environmental restrictions may be required by the Teletype unit.**

2.3.5 H720 Power Supply

The H720 Power Supply provides power for the basic PDP-11/20 System and for expansion units (e.g., extra memory or device interfaces) mounted within the basic BA11 mounting box. Expansion within the BA11 box is limited by space and available power; available power in the basic PDP-11/20 is noted in Table 2-7. The regulated output voltages are +5 Vdc and -15 Vdc. Both of these outputs are protected with current limiting circuits. In addition, a crowbar overvoltage circuit protects the +5V output and the -15V output is protected by an acceptable system maximum. An unregulated, partially filtered, +8V output is supplied for the indicators on the programmer's console. General power supply specifications are listed in Table 2-7. A detailed description of the power supply is given in the *Power Supply & Mounting Box Manual.*

In addition to power, three other outputs are provided: a line frequency signal, a DC LO logic signal, and an AC LO logic signal. The line frequency signal, which is a sine wave clipped at both ground and +5V, is used by the line-time clock option (KW11-L) within the processor. The DC LO signal indicates that the dc voltage outputs are not at the proper value; the AC LO signal indicates insufficient ac voltage.

When power is turned on, the normal sequence of signals is for DC LO to exist until the dc voltages are up. The DC LO signal is used to clear and hold off random operation. After the dc voltages are correct, the AC LO signal continues to exist until a margin of ac input voltage is established (machine operation can begin). When power is turned off or lost the sequence is reversed; AC LO indicates that ac power is being removed (begin to terminate operation), and DC LO, after a specific time interval, indicates low dc voltage. The proper generation of these signals is explained in reference to the power fail/restart logic covered in the *KA11 Processor Manual*.

A power bus (not to be confused with the Unibus) carries power from the power supply to all system components. This facility preserves the integrity of the Unibus (which handles data, address, and control signals) to ensure that the system remains modular in function as well as in physical construction.

2.3.6 Unibus

The Unibus, a single, high-speed bus, provides communication between system components. The Unibus, with bidirectional data, address, and control lines, allows data transfers between all units on the bus with control of the bus an important factor in these transfers. The fixed repertoire of bus operations is flexible enough for speed and design economy, yet provides a fixed specification for interfaces. The asynchronous nature of these operations also eases design and operation. The repertoire of bus operations is:

DATI, DATIP, DATO, DATOB – data operations

INTR, PTR (BR, NPR) – control operations.

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between the master and slave. The DATI, DATIP operations transfer data into the master; the DATO, DATOB operations transfer data out of the master. When a device is capable of becoming bus master and requests use of the bus, it is generally for one of two purposes: to make a direct memory access (DMA) transfer of data directly to, or from, another device without processor intervention; or to interrupt (INTR) program execution and force the processor to branch to a specific address where an interrupt service routine is located. Bus control is obtained under a non-processor request (NPR) for the direct memory access (DMA) or under a bus request (BR) for an interrupt (INTR). A device can perform a DMA after acquiring bus control by a BR; bus control acquisition is at a lower priority.

Requests for the bus can be made at any time on the bus request (BR) and non-processor request (NPR) lines. Transfer of bus control from one device to another is made by the processor priority arbitration logic which grants control of the bus to the device having the highest priority.

The processor has a special role in bus operations. It performs the priority arbitration to select the next bus master. (The processor's own priority, which is programmable, is also used in this selection.) Because of the Unibus concept, all processor instructions can operate on all address spaces, thereby eliminating the need for separate I/O instructions as such.

Table 2-7
H720 Power Supply Specifications

Input Voltage	
Model A or E:	120 Vac, ±10%; 47-63 Hz; 6A
Model B or F:	One of the following:
	218 Vac, ±10%; 47-63 Hz; 3A 225 Vac, ±10%; 47-63 Hz; 3A 233 Vac, ±10%; 47-63 Hz; 3A 240 Vac, ±10%; 47-63 Hz; 3A
Output Voltages	
Regulated, Models A and B:	+5 Vdc, ±5%; 16A -15 Vdc, ±3%; 10A
Models E and F:	+5 Vdc, ±5%; 22A -15 Vdc, ±3%; 10A
Unregulated (All Models):	-22 Vdc, ±20%; 1A +8V, full-wave rectified, unfiltered; 1.5A

Table 2-7 (Cont)
H720 Power Supply Specifications

Protection Circuits	
Over-current:	+5V @ 18-22A; short-circuit current (Models A and B) 30A at 0V
	-15V @ 12-16A; short-circuit current 25A at 0V
Over-voltage:	+5 Vdc limited to 6.3 Vdc -15 Vdc limited to unregulated -22 Vdc
Logic Signals	
LTC:	Line frequency signal, sine wave clipped at +5V and ground
DC LO:	Low dc voltage signal, goes high before AC LO on power up; remains high 7 ms after AC LO drops during power-down
AC LO:	Low ac voltage signal
Available Power	
The basic PDP-11/20, consisting of the KA11, KY11-A, MM11-E, and KL11, allows the following power for expansion:	
	+5 Vdc, ±5%; 3.4A -15 Vdc, ±3%; 1.7A -22 Vdc, ±20%, unregulated; 0.8A

The Unibus physically consists of an M920 Jumper Module that carries the Unibus from one system unit to the next. All 56 Unibus signals and 17 grounds are carried in this one module. In addition, a 120-conductor Flexprint® cable may be used to connect system units in different mounting boxes or to connect a peripheral device removed from the mounting box.

A complete description of the Unibus is presented in the *Unibus Interface Manual* DEC-11-HIAB-D. Table 2-8 lists general Unibus specifications.

Table 2-8
Unibus Specifications

Bus Type	
Single bus connecting processor, memory, and all peripherals. Information transferred in parallel 16-bit words or 8-bit bytes.	
Data Transfer	
Rate:	2,500,000 words per second, maximum
Types:	DATI, DATIP, DATO, DATOB
Lines:	40 bidirectional lines
	16 data lines 18 address lines 6 control lines
Priority Transfer	
Types:	
	PTR (priority transfer: includes both bus and non-processor requests)
	INTR (interrupt)

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Table 2-8 (Cont)
Unibus Specifications

Lines:	13 lines (5 unidirectional; 8 bidirectional) 4 BR lines (each a different priority level) 4 unidirectional BG (bus grant) lines 1 NPR line 1 NPG line (unidirectional) 1 INTR line 2 control lines (bus busy; selection acknowledge)
Miscellaneous Lines	
Lines:	Initialization AC LO (ac voltage low) DC LO (dc voltage low)
Type:	Bidirectional

CHAPTER 3
SYSTEM OPERATION

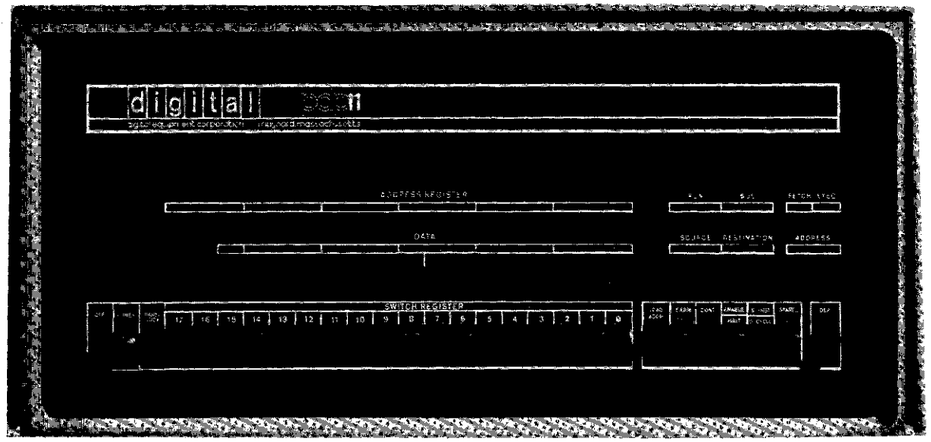


Figure 3-1 PDP-11/20 Console Controls

3.1 INTRODUCTION

This chapter provides the information necessary to operate the PDP-11/20 System and associated Model 33 ASR Teletype. The description is divided into two major parts: controls and indicators, and control interaction.

The description of controls and indicators (Paragraph 3.2) is in tabular form and provides the user with the location, type, and function of each operating switch and indicator on the programmer's console and teletype. Operating controls for external devices are beyond the scope of this discussion; for these devices refer to the appropriate peripheral manual and the *Unibus Interface Manual*.

The control interaction discussion (Paragraph 3.3) examines the relationships between controls and indicators and the system. This is an expansion of Paragraph 3.2, Controls and Indicators.

Step-by-step procedures for both manual and program operation are given in Chapter 4.

3.2 CONTROLS AND INDICATORS

The controls and indicators used to operate the PDP-11/20 System are detailed in the following paragraphs. These paragraphs describe the KY11-A programmer's console and the ASR 33 Teletype.

3.2.1 Programmer's Console

Manual operation of the PDP-11/20 System is controlled by switches mounted on the programmer's console (front panel of the basic mounting box). Visual displays indicate processor operation and the contents of address and data registers.

All register displays and switches, whether marked on the console or not, are numbered from right to left. The numbers correspond to the powers of two, i.e., 2^{15} .....2^2, 2^1, 2^0. Therefore, the most significant bit (MSB) is at the left of each specific register or display, the least significant bit (LSB) is at the right. Whenever an indicator is on, it denotes the presence of a binary 1 in the particular bit position. The alternate color coding on the console identifies the different functions or segments of the binary number in octal format.

Figure 3-1 shows the location of all PDP-11/20 console controls and indicators. Each indicator and associated function is listed in Table 3-1. Each control and related function is listed in Table 3-2.

Table 3-1
PDP-11/20 Console Indicators

Indicator	Type	Function	Remarks
DATA	16-bit display MSB at left Color-coded in 3-bit segments for octal format Vertical center line divides 16-bit word into 8-bit bytes. Indicators to right of center line indicate low-order (even) byte; indicators to left of line indicate high-order (odd) byte.	Displays the information within the data paths of the processor. This is not a single register, but the logical sum of two latch registers on the data paths. For most console functions, one register is zeroed while the other contains the desired information. This display of the data paths, the central data flow through the processor, is especially important when used in a single clock mode with the Maintenance Panel Option (KM11-A). Data is manually loaded into the DATA register (data paths) by setting the data value into the SWITCH REGISTER and lifting the DEP switch.	When console switches are used, information shown on the DATA display is as follows: LOAD ADDR - no indication DEP - the SWITCH REGISTER information just deposited. Note that the data and address correlated. The address is where this data was stored. EXAM - the information from the address examined - note address and data correlation. S-INST - when stepping through a program a single instruction at a time, there is no indication on the DATA display.

Table 3-1 (Cont)
PDP-11/20 Console Indicators

Indicator	Type	Function	Remarks
DATA (cont)			S-CYCLE - the information last in the data paths (refer to flow diagram). Usually is a derivative of last bus data. During HALT and WAIT instructions, information shown on DATA display is as follows: **WAIT** - The RUN light is on, no indication on DATA display. **HALT** - when bus control is transferred to the console on a HALT instruction, processor register R0 is displayed. This allows program identification of halts. During direct memory access (DMA) operations, the processor is not involved in data transfer functions. Therefore, the data displayed in the DATA display is not that of the last bus operation.
ADDRESS REGISTER	18-bit display MSB at left Color-coded in 3-bit segments for octal format	Displays the address in the bus address register (BAR) of the processor. This is the address last used by the processor on the bus. The BAR is 18 bits, allowing for future expansion. At present, the two most significant bits (A17, A16) are ordered according to the lower 16 bits; they are set only when bits A15, A14, and A13 are set. Addresses between 160000 and 177777, therefore, are translated to addresses between 760000 and 777777, respectively.	When console switches are used, information shown on the ADDRESS REGISTER display is as follows: **LOAD ADDR** – the transferred SWITCH REGISTER information **DEP or EXAM** – indicates the bus address just deposited into or examined. **S-INST or S-CYCLE** – indicates the last processor bus address. During a programmed HALT or WAIT instruction, the ADDRESS REGISTER displays the address of the instruction. The program counter (PC) is the BAR value plus 2. During direct memory access (DMA) operations, the processor is not involved in the data transfer functions, and the address displayed in the ADDRESS REGISTER is not that of the last bus operation.
RUN	Single light	When the RUN indicator is on, the processor clock is running. The processor has control of the bus and is operating on an instruction. When the RUN indicator is off, the processor is waiting for an asynchronous peripheral data response; or the processor has given up bus control to the console or to a peripheral.	During normal machine operation the RUN light will flicker on and off (indicated by a faint glow). Special situations exist for programmed HALT and WAIT instructions: **WAIT** – the RUN light is completely on **HALT** – the RUN light is off During machine operation, with S-INST or S-CYCLE control transferred to the console, the RUN light is not on.
BUS	Single light	When the BUS indicator is on, a peripheral device (other than the console) is controlling the bus.	When both the BUS and RUN indicators are off, the bus control has been transferred to the console. The bus light probably is never seen except when there is a bus malfunction or when a peripheral holds the bus for excessive periods of time. Refer to Paragraph 3.3 for further discussion of BUS and RUN indicator combinations. During machine operation with S-INST or S-CYCLE, control is transferred to the console and the BUS indicator is not on.

NOTES

1. **When the processor is in a major machine state (FETCH, EXEC, SOURCE, DESTINATION), the appropriate major state indicator is on and the following, associated RUN and BUS conditions occur.**
   a. **The RUN indicator is on when the processor clock is running (processor in control of bus).**
   b. **The RUN indicator is off when processor is waiting for data from the bus (processor in control of bus, but clock is off).**
   c. **The RUN indicator is off and the BUS indicator is on when an NPR is being serviced (processor is not in control of the bus).**
2. **There is no major state indicator on the console for the major machine state of Service. In this state, break requests are honored, machine instructions of WAIT and HALT are executed, and trap sequences for instruction and bus interrupts are implemented.**

FETCH	Single light	When on, the processor is in the FETCH major state and is obtaining an instruction.	During the Fetch major state, only FETCH and RUN indicators are on if no NPRs are honored.
EXEC	Single light	When on the processor is in the EXECUTE major state. The processor performs the action specified by the instruction. (HALT, WAIT, and trap instructions are executed in Service.)	During the Execute major state, only EXEC and RUN indicators are on if no NPRs are honored.

Table 3-1 (Cont)
PDP-11/20 Console Indicators

Indicator	Type	Function	Remarks
SOURCE	Single light	When on, the processor is in the Source major state and is obtaining source operand data. The processor calculates source address data as indicated by cycles of the ADDRESS lights.	During the Source major state, SOURCE and RUN indicators are both on; ADDRESS lights may be on in various combinations. The BUS indicator is off if no NPRs are honored.
DESTINATION	Single light	When on, the processor is in the Destination major state and is obtaining destination operand data. The processor calculates destination address data as indicated by cycles of the ADDRESS lights.	During the Destination major state, DESTINATION and RUN indicators are both on; ADDRESS lights may be on in various combinations. The BUS indicator is off if no NPRs are honored.
ADDRESS	Two lights representing a 2-bit binary code MSB is on the left	When lit, indicate bus cycles used to obtain address data during Source and Destination major states. The 2-bit binary code indicates which address cycle (1, 2, or 3) the machine is in during the Source or Destination major state.	Whenever either one or both ADDRESS lights are lit, either the SOURCE or DESTINATION indicator is on. The BUS indicator is off if no NPRs are honored.

Table 3-2
PDP-11/20 Console Controls

Control	Type	Function	Remarks
OFF/POWER/ PANEL LOCK	3-position, key operated switch	Provides power control to console and lock-out of console controls as follows:	
		OFF position - removes all power from the processor.	System not being used
		POWER position - applies primary power to the processor. All console controls are fully operational when switch is in this position.	Normal operation
		PANEL LOCK position - disables all console (panel) controls except the SWITCH REGISTER key switches. This prevents inadvertant switch operation from disturbing a running program. The data entered in the SWITCH REGISTER are still available to the processor whenever the program explicitly addresses the SWITCH REGISTER (address 777570)	Processor operating; console disabled.
SWITCH REGISTER	18-key-type switches	Provides a means of manually loading a 16-bit address or 16-bit data word into the processor. The processor ignores bits 17 and 16; these switches may be set to either position. For addresses using bits 17 and 16, these bits are set within the processor if bits 15, 14, and 13 are set. If the word in the SWITCH REGISTER represents an address, it can be loaded into the ADDRESS REGISTER by depressing the LOAD ADDR key. If the word contains data, it is loaded into the address specified by the ADDRESS REGISTER by lifting the DEP key. The data appear in the DATA display. The contents of the SWITCH REGISTER may be used by the processor any time the program explicitly addresses the register at address 777570. This address can only be used by the processor.	Bit position of each switch is labeled; MSB is at left. Color-coded in 3-bit segments for octal format. Up position – logical one (or on). Down position – logical zero (or off)
LOAD ADDR	Momentary key-type switch Depress to activate	The LOAD ADDR switch transfers the SWITCH REGISTER contents to the Bus Address Register (BAR) through a temporary location (TEMP) within the processor. This bus address, displayed in the ADDRESS REGISTER, provides an address for the console functions of EXAM, DEP, and START.	Odd bus address (bit 00 enabled) should not be entered from the console. Upper bytes at these odd addresses can be examined or deposited by using the word address (bit 00 not enabled). Refer to Paragraph 3.3.1.5.
EXAM	Momentary key-type switch Depress to activate	The EXAM switch transfers the contents of the bus address (which is specified by the Bus Address Register) for DATA display. After use, the data appear on the DATA display and the address of the data is in the ADDRESS REGISTER. A LOAD ADDR operation preestablishes the initial address; sequential addresses occur automatically. If the EXAM switch is depressed twice in succession, the contents of the next sequential bus address are displayed in DATA. This action is repeated each time EXAM is depressed provided no other switch is used between these steps. Whenever the LOAD ADDR or DEP switch is depressed, it destroys	Refer to Paragraph 3.3 for further discussion of address incrementation by the EXAM switch.

Table 3-2 (Cont)
PDP-11/20 Console Controls

Control	Type	Function	Remarks
EXAM (cont)		the incrementing sequence. The next time EXAM is used, it displays the current Bus Address Register address rather than the next sequential address.	
CONT	Momentary key-type switch Depress to activate	Causes the processor to continue operation from the previous point at which it had stopped If the ENABLE/HALT switch is in the ENABLE mode, CONT returns bus control from the console to the processor and continues program operation. If the ENABLE/HALT switch is set to HALT, depressing the CONT key causes the processor to perform either a single instruction or a single bus cycle (dependent on position of the S-INST/S-CYCLE switch) and then stop. Bus control has been returned to the console and the CONT switch must be used to continue.	If program stops, depressing CONT provides a restart without power clear.
ENABLE/HALT	2-position, key-type switch	Allows either the program or the console to control processor operation **ENABLE position** - permits the system to run in a normal manner. No console control requests (type dependent upon S-INST/S-CYCLE switch) are made. Without console control, all switches except ENABLE/HALT and the SWITCH REGISTER are disabled. **HALT position** - halts the processor and passes control to the console; with the S-INST/S-CYCLE switch in the S-CYCLE mode, console switches (except SWITCH REGISTER, CONT, and ENABLE/HALT) are disabled unless the machine is stepped to the end of an instruction. In the S-INST mode, the processor stops at the end of an instruction and all console switches are enabled. The HALT mode is used with the CONT switch to step the machine through programs and facilitate intermediate observations. When the START switch is activated in the HALT mode, a system clear is effected.	Continuous program control requires the ENABLE mode. The HALT mode is used to interrupt program control, perform single step operation, or clear the system.

Table 3-2 (Cont)
PDP-11/20 Console Controls

Control	Type	Function	Remarks
S-INST/S-CYCLE	2-position, key-type switch	Allows the processor to step through program operation either one instruction or one bus cycle at a time. The user may note processor operation and contents of registers during major states or bus cycles of individual instructions. **S-INST position** - the processor halts after an instruction. This process is repeated each time the CONT key is depressed. Console switches (LOAD ADDR, EXAM, DEP) can be used when the processor halts. **S-CYCLE position** - The processor halts after a bus cycle. The process is repeated each time CONT is depressed. Console switches are inoperative unless the machine is stepped to the S-INST halt position. (Changing mode to S-INST and using CONT switch effects this.)	This switch is enabled by the ENABLE/HALT switch in HALT mode. Control is transferred to the console by a console bus request (CBR), second highest priority and serviced at instruction end. Control is transferred to the console by a console nonprocessor request (CNPR), highest priority and serviced after a bus cycle.
START	Momentary key-type switch Depress to activate	When ENABLE/HALT is set to ENABLE, depressing START provides a system clear operation and then begins processor operation. A LOAD ADDR operation pre-establishes the starting address. When ENABLE/HALT is set to HALT, depressing START provides a system clear (initialize) only. The processor does not start; the Bus Address Register is loaded from a temporary processor register (TEMP) which is usually pre-loaded by LOAD ADDR. This provides the only method of reading TEMP when it does not contain the LOAD ADDR value.	
DEP	Momentary key-type switch Lift to activate	The DEP switch transfers the contents of the console SWITCH REGISTER to the bus address (specified by the Bus Address Register). After use, the data appear on the DATA display and the address is in the ADDRESS REGISTER. A LOAD ADDR operation pre-establishes the initial address; sequential addresses occur automatically. If the DEP switch is raised twice in succession, the contents of the	Refer to Paragraph 3.3 for further discussion of address incrementation of locations by DEP switch.

Table 3-2 (Cont)
PDP-11/20 Console Indicators

Control	Type	Function	Remarks
DEP (cont)		SWITCH REGISTER is deposited in the next sequential bus address location. This action is repeated each time DEP is raised provided no other switch is used between these steps. Whenever the LOAD ADDR or EXAM switch is depressed, it destroys the incrementing sequence. The next time DEP is used, it deposits the current address rather than the next sequential address.	

3.2.2 **Teletype**

The Model 33 ASR Teletype unit is used as an input/output device with the PDP-11/20 System. Data can be entered into the processor via the keyboard or through a paper-tape reader. The Teletype can also be operated off-line to punch paper tapes. Controls for the Model 33 ASR Teletype unit are shown in Figure 3-2 and listed in Table 3-3. Further detailed operating information is contained in the Teletype Corporation manuals listed in Table 1-1 of this manual.

Table 3-3
Teletype Controls

Control	Type	Function	Remarks
		Punch	
REL. pushbutton	Momentary switch, depress to activate	Disengages the paper tape from the punch to allow loading or removal of tape	
B.SP. pushbutton	Momentary switch, depress to activate	Backspaces the paper tape by one space each time pushbutton is depressed to allow manual correction or rubout of character just punched.	
ON pushbutton	2-position switch, connected to OFF pushbutton	When depressed, turns on the paper tape punch and releases OFF switch.	
OFF pushbutton	2-position switch, connected to ON pushbutton	When depressed, turns off the paper tape punch and releases ON switch.	
		Reader	
START/STOP/ FREE switch	3-position switch	Controls operation of the tape reader **START position** - engages tape reader which begins operation under program control. **STOP position** - engages reader mechanism but does not energize it. In effect, tape is locked in the reader but reading operation does not begin until the switch is moved to START. **FREE position** - disengages reader to permit loading and unloading of tape.	Used on-line
		Keyboard/Printer	
LINE/OFF/ LOCAL switch	3-position rotary switch	Serves two functions: applies primary power to Teletype and connects computer to Teletype. **LINE position** - energizes Teletype and connects it to the computer as an input/output device. Signals from either the Teletype reader or keyboard can be used as an input	

Table 3-3 (Cont)
Teletype Controls

Control	Type	Function	Remarks
Keyboard	45 printing characters 6 non-printing functions Typewriter-like layout	Uses a typewriter-like keyboard to print characters on paper, punch tape, or input information into the computer. **Off-Line Operation (LOCAL)** When tape reader and punch are off, prints characters on paper. When punch is on, simultaneously prints characters on paper and punches equivalent code into paper tape. When reader is on, reads code from punched paper tape and prints equivalent characters on paper. **On-Line Operation (LINE)** When tape reader and punch are off, prints characters on paper and sends equivalent signals to computer. When tape reader is on, reads code from punched paper tape and sends equivalent signals to computer. No characters are printed. When receiving signals from computer, prints equivalent characters on paper and punches tape if punch is on.	
Cover guard	Latch, push to release	Used to hold paper tape in position when using tape reader.	

3.3 CONSOLE INTERACTIONS

The majority of PDP-11 controls and indicators interact to control or display various system operations. Knowledge of control interaction is necessary if the console is to be used properly and knowledge of display interaction is important when determining if the system is functioning in a normal manner.

Although the specific function of each control and indicator has been previously described (Paragraph 3.2), the following paragraphs discuss some interactions that are important, and not always obvious, when examining individual control functions.

3.3.1 Indicators

Console indicators are separated into three functional categories:

a. **Display** - ADDRESS REGISTER, DATA

b. **Control Operation** - RUN, BUS

c. **Major States** - FETCH, SOURCE address, DESTINATION address, EXEC, and Service (no indicator for this state)

Combinations of these indicators have specific meaning and are shown in Figure 3-3 and described in the following paragraphs. Note that during normal operation under program control, these indicators are not

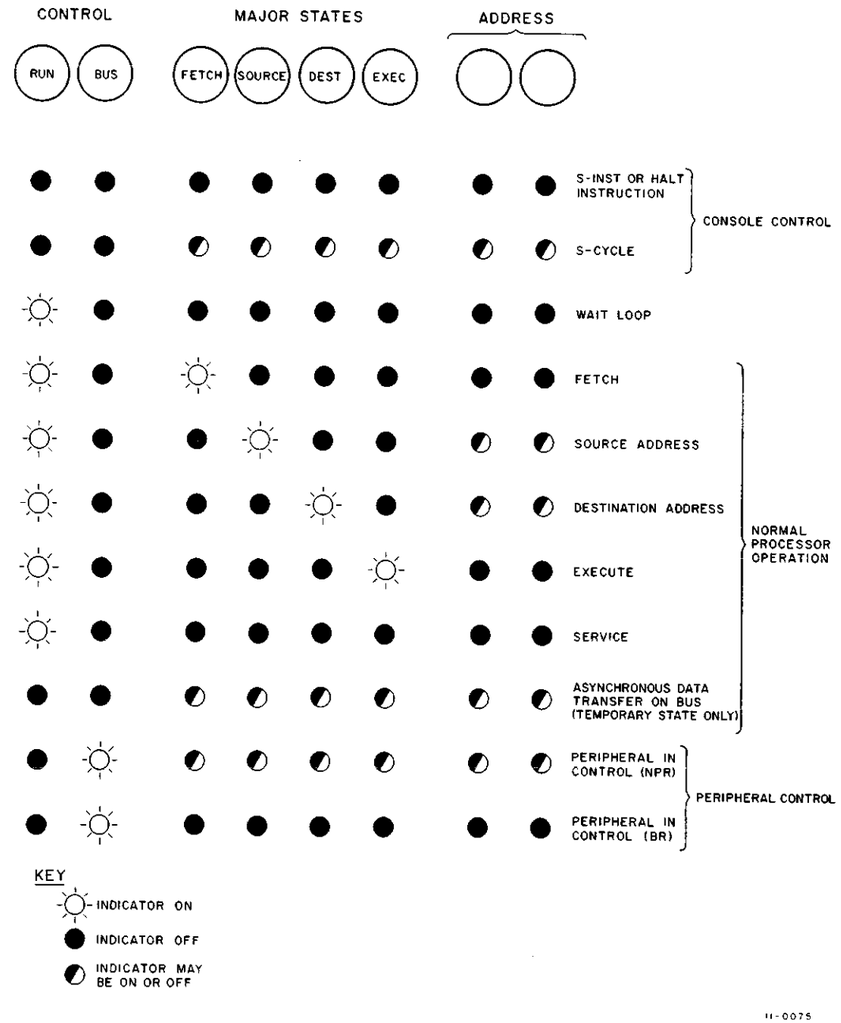


Figure 3-3 Indicator Interaction

completely on or off. An indication of operation is obtained by lamp intensity; a state that is entered often, or remained in for a long period, glows brightly.

Stepping through processor operations in the S-INST or S-CYCLE mode allows more exact observation. Because console control is required for stepping, the RUN light is off. The S-INST mode, which halts the machine after each instruction, is in the Service state with no major state indicator; the S-CYCLE mode, which halts the machine after each bus cycle, can be in any major state. (The machine can be in only one major state at any given time, however.)

3.3.1.1 **Console Control** – Console control is achieved in two ways: a console bus request (CBR) for S-INST mode; and a console non-processor request (CNPR) for the S-CYCLE mode. The console bus request has the

highest bus request priority and is granted during the Service major state. When granted, no major state indicator is on and RUN and BUS indicators are off. Console control here is similar to that of the HALT instruction, power up in the HALT mode (ENABLE/HALT switch), or START in the HALT mode; therefore, the console operations of LOAD ADDR, EXAM, and DEP can be used. Console control by means of a CNPR (S-CYCLE mode) can occur after a bus cycle in any of the major states and has the highest non-processor request priority. Console operations are not permitted.

3.3.1.2 **Wait Loop** – During a programmed WAIT instruction, the processor cycles in the Service state while waiting for a bus request (BR) and interrupt (INTR) sequence. During this wait loop, both BRs and NPRs may be sequenced (refer to other indicator interactions). During the loop, the RUN indicator is on and the other indicators are off. An INTR sequence or console operation is necessary to terminate this loop.

3.3.1.3 **Processor Control** – When the processor is in control, the RUN indicator is on, and the BUS indicator is off. Normal operation consists of stepping through a sequence of major states. As the processor enters each major state, appropriate console indicators are on. Only one major state indicator may be on at any one time.

The maximum possible sequence of operation is:

Fetch; Source, Address 1, 2, 3; Destination, Address 1, 2, 3; Execute.

After Execute, the processor enters Service and then returns to Fetch to obtain the next instruction. Note that this is a maximum sequence because the processor may skip certain major states (such as Source and Destination).

3.3.1.4 **Peripheral Control** – Whenever the BUS indicator is on and the RUN indicator is off, an external device (peripheral) is controlling the bus. The external device can acquire bus control through an NPR or BR. With the NPR, any major state may exist (including Service); with the BR, the processor is in Service (all major state indicators off). As control is transferred back to the processor, both the RUN and BUS indicators may be off momentarily; this is not a normal steady-state situation. The RUN indicator refers to the status of the processor basic clock; when it is on, the processor must be in control. It is possible during asynchronous bus operations for the RUN indicator to be momentarily off while the processor is still in control. With a steady-state condition of both the RUN and BUS indicators off the console has reassumed control; if the RUN and BUS indicators are on, there is a malfunction.

3.3.1.5 **Register Displays** – During console operation, the ADDRESS REGISTER displays the bus address of the console function, and the DATA register displays the data of the console function. This correlation is independent of the automatic stepping of addresses during multiple EXAM or DEP operations; the address shown is that of the present operation, not the next.

The console is a word-oriented device; examination and deposit of bytes are performed on a word basis. To examine a high-order byte, the whole word is examined using the word address (bit 00 not set). To deposit, the entire word must be entered into the SWITCH REGISTER.

The use of an odd bus address (or non-existent address) does not result in a program trap during console operation. (This trap does occur under program control.) On EXAM, the DATA display is zero and the RUN indicator comes on. On DEP, the SWITCH REGISTER contents go to the DATA display, and no indication of this illegal operation appears; however, EXAM results in the RUN indicator coming on. These illegal operations are cleared by a START in the HALT mode.

3.3.2 Controls

Two major areas of control interaction are controls influenced by the ENABLE/HALT switch, which selects either processor or console control; and the switches and sequences used for loading data manually into the processor.

3.3.2.1 **ENABLE/HALT Switch** – Figure 3-4 shows the relationship of the console switches to the ENABLE/HALT switch. When the processor has control, as allowed by ENABLE/HALT being set to ENABLE,

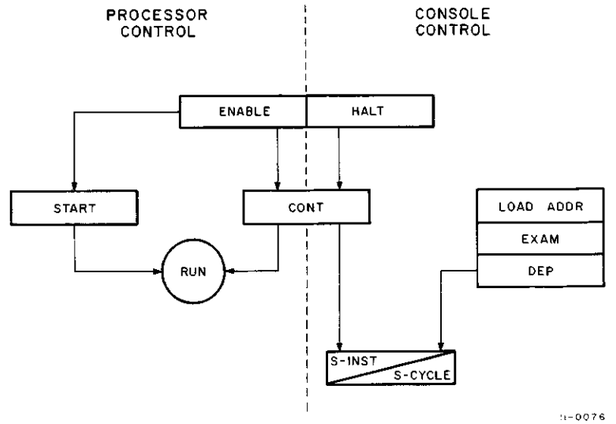


Figure 3-4 Console Switch Relationships

either the START or CONT switch causes the program to run. The START switch initializes the system with a clear signal and begins operation at a specific address (pre-selected by LOAD ADDR). The CONT switch merely releases console control, and the program continues.

When the ENABLE/HALT switch is set to HALT, the console obtains control. The LOAD ADDR, EXAM, and DEP switches can be used in the S-INST mode. The CONT switch now causes the processor to step through the program a single instruction or single bus cycle at a time, depending on the position of the S-INST/S-CYCLE switch.

3.3.2.2 **Loading Data Manually** – Whenever data are manually loaded into a computer, it is desirable to have the address increment automatically. Thus, the user can set a starting address and then continue to store data in sequential memory locations without having to load a new address each time.

The programmer's console logic permits the user to immediately examine the data just deposited without re-addressing, to re-deposit if necessary, and to continue with automatic incrementation. These sequences are associated with the functioning of the DEP and EXAM switches mentioned in previous paragraphs.

The address in the ADDRESS REGISTER (from bus address register) does not increment the *first* time EXAM or DEP is used after a HALT or LOAD ADDR. It does not increment if DEP is used immediately after EXAM or if EXAM is used immediately after DEP. It does increment the *second* and *subsequent* times the same switch (DEP or EXAM) is used. (This increment is a word increment as the console is word oriented.) Thus, the user can look at a location, change it, deposit the changed data, and then re-examine them without having to load an address each time.

Incrementation is on even boundaries for all addresses except the address specifically designated for the processor internal registers, which are incremented by one.

For example, to alter *several* successive locations, the following steps are performed:

Step	Procedure
1	LOAD ADDR (starting location)
2	EXAM (no increment - looks at starting location)
3	DEP (no increment - loads starting location)
4	EXAM (no increment - checks previous deposit)

5	EXAM (increment - looks at next location)
6	DEP (no increment - loads second location)
7	EXAM (no increment - checks previous deposit)
8	EXAM (increment - looks at third location)
	etc.

If the user desires to take advantage of automatic address incrementation for examining or loading data, the following steps can be used to load data into *sequential* locations:

Step	Procedure
1	LOAD ADDR (starting location)
2	DEP (no increment - loads starting location)
3	DEP (increment - loads second location)
4	DEP (increment - loads third location)
5	DEP (increment - loads fourth location)
	etc.

This same procedure can be used for examining data in sequential memory locations.

CHAPTER 4
OPERATING PROCEDURES

4.1 INTRODUCTION

Many methods exist for storing, modifying, and retrieving information from the PDP-11/20 System. These methods depend on the form of the information, time limitations, and the peripheral equipment connected to the processor. The following procedures are basic to the use of the PDP-11/20 System. Although they may be used less frequently as the programming and use of the system become more sophisticated, they are valuable in preparing the initial programs and in learning the function of system input and output transfers.

Operating procedures are separated into the following categories:

a. manual program loading
b. automatic program loading
c. running programs
d. manual operation
e. Teletype operation (on-line and off-line).

Although many types of programs can be used with the system, this chapter discusses only representative examples of frequently used programs.

4.2 MANUAL LOADING

The primary manual use of the programmer's console is to store the bootstrap loader in the core memory. (Programs and data can be stored or modified by manual use of the programmer's console.) The bootstrap loader (DEC-11-L1PA-LA) is a minimal instruction program that can automatically load programs into core memory from a paper tape punched in a special bootstrap format. One of these programs, after being stored, can in turn load any binary format tape into the computer. (An explanation of the number designations used for DEC programs is given in Table 4-1.)

In effect, the sequence of loading the computer is as follows:

a. Bootstrap loader (DEC-11-L1PA-LA) – manually loaded by console switches; provides for automatic loading of programs punched in a special format.

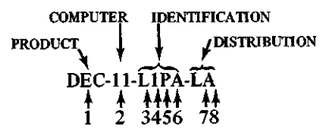
b. Absolute Loader – punched in special format; loaded by bootstrap loader; provides for automatic loading of programs punched in binary format.

c. Selected Program – punched in binary format; loaded automatically by absolute loader.

In order to eliminate the necessity of more than one bootstrap loader, the bootstrap loader instructions contain two variables (x and y) to provide compatibility with various memory configurations and reading devices. These variables are listed in Table 4-2. A complete explanation of the bootstrap loader program is given in Chapter 5 of the *Paper Tape Software Programming Handbook (DEC-11-GGPA-D)*; further information may be found in the program listing, DEC-11-L1PA-LA.

Table 4-1
Program Identification Codes

Format:



Notes:

1	Product Code	MAINDEC = maintenance library products DEC = programming library products
2	Computer Series	11 = PDP-11 Computer Systems
3	Major Category	L = Loader
4	Minor Category (sequential numbers)	1 = first in a series of programs 2 = second in series, etc.
5	Option Category (hardware required to use software)	P = paper tape system H = high-speed reader and/or punch K = Teletype keyboard only M = magtape
6	Revision Category (sequential letters)	A = basic program B = first revision C = second revision, etc.
7	Distribution Method	L = listing P = paper tape
8	Distribution Mode	A = ASCII B = binary (absolute) O = other (bootstrap binary)

Example: DEC-11-L2PB-PO — indicates a PDP-11 programming library product, second in a series of loaders, requiring a paper tape system to use, the first revision to the program, supplied as a paper tape in bootstrap binary format.

References: *DEC Classifying and Documenting Standard*, DEC-00-BZZB-D.
A list of all identification codes is in the *PDP-11 Convention Manual.*

Table 4-2
Bootstrap Loader
(DEC-11-L1PA-LA)

Bootstrap loader should be toggled into highest core memory bank.

Address	Instruction
xx7744	016701
xx7746	000026
xx7750	012702
xx7752	000352
xx7754	005211
xx7756	105711
xx7760	100376
xx7762	116162
xx7764	000002
xx7766	xx7400
xx7770	005267
xx7772	177756
xx7774	000765
xx7776	yyyyyy

xx represents highest available memory bank. First location of the loader is one of the following, depending on memory size; *xx* in all subsequent locations is the same as the first.

Address	Memory Bank	Memory Size
017744	0	4K
037744	1	8K
057744	2	12K
077744	3	16K
117744	4	20K
137744	5	24K
157744	6	28K

Contents of address xx7776 (yyyyyy) should contain device status register address of paper-tape reader to be used when loading the bootstrap formatted tape. Addresses are:

Teletype Paper-Tape Reader	177560
High-Speed Paper-Tape Reader	177550

The following procedure is used for manually loading the BOOT Loader Program (DEC-11-L1PA-LA):

Step	Procedure
1	Set ENABLE/HALT switch to HALT to give bus control to the console when powering up.
2	Turn OFF/POWER/PANEL LOCK switch to POWER position. This energizes the programmer's console.
3	Enter starting address of bootstrap loader (Table 4-2) into SWITCH REGISTER switches. Make certain that the correct xx value is used (*01*7744) for 4K memory, *03*7744 for 8K memory, *05*7744 for 12K memory, etc.).
4	Depress LOAD ADDR switch. The address set in SWITCH REGISTER switches is displayed in ADDRESS REGISTER indicators.
5	Enter starting address *contents* (016701) into SWITCH REGISTER switches.
6	Lift DEP switch. The contents just entered in the SWITCH REGISTER is displayed in the DATA indicators.
7	Enter *contents* of next address into SWITCH REGISTER switches.
	NOTE **It is not necessary to load addresses after the starting address has been loaded because the address is automatically incremented by two each time DEP is used sequentially. If, however, EXAM is used at any point, automatic address incrementation does not occur. Refer to Paragraph 3.3.2.2 for a discussion of EXAM and DEP interaction and use.**
8	Lift DEP switch.
9	Repeat steps 7 and 8 above for each location of the bootstrap loader. When loading the contents of address xx7766, make certain that the correct *x* value is used. When loading the contents of the last address, make certain that the correct *y* value is used.
10	The bootstrap loader program is now loaded in memory locations xx7744 through xx7776 and can be used to automatically load other programs into memory.
11	Correct program entry can be verified by examining the addresses between xx7744 and xx7776. This is accomplished by setting the starting address into the SWITCH REGISTER switches and depressing the EXAM switch. The contents of the starting address are shown in the DATA display. Each time the EXAM is again depressed, the address is automatically incremented by two and the corresponding contents displayed. However, if DEP is used during this sequence, automatic incrementation does not occur.
12	This last step (verification) may be sufficient if the bootstrap loader program has already been loaded into the system. The program is stored in the last portion of available memory so that it tends to survive program operation and is available for reloading programs. If the program is not intact, load according to the above procedure, beginning with step 1.

4.3 AUTOMATIC LOADING

Information can be stored or modified in the computer automatically only if a program capable of performing these functions has previously been stored in the core memory. For example, having the bootstrap loader stored in the computer enables the user to operate any program that has been punched in the special tape format required by the bootstrap loader. Typical programs of this type include the absolute loader, the absolute dump, and the teleprinter dump.

The bootstrap loader is limited because of the special tape format; another loader is used to load any binary format tape into the computer. This is the absolute loader (DEC-11-L2PB-PO), which is loaded into the computer by the bootstrap loader. Once the absolute loader is in memory, any binary tape program (such as PAL III assembler, symbolic editor, input/output service routines, diagnostics, mathematical routines, etc.) may be automatically loaded.

The following paragraphs give procedures for loading the absolute loader and for using the absolute loader to store other programs. A complete description of the absolute loader program is given in Chapter 5 of the *Paper Tape Software Programming Handbook (DEC-11-GGPA-D)*; refer also to the program listing, DEC-11-L2PB-LA.

4.3.1 Loading Absolute Loader

The following procedure is used for automatically loading the ABSolute Loader Program (DEC-11-L2PB-PO):

Step	Procedure
1	Set ENABLE/HALT switch to HALT.
2	Make certain that the bootstrap loader has been stored in core memory (refer to Paragraph 4.2, step 11).
3	Enter starting address of bootstrap loader into SWITCH REGISTER switches. The starting address is xx7744 (*01*7744 for 4K memory, *03*7744 for 8K memory, *05*7744 for 12K memory, etc.).
4	Depress LOAD ADDR switch. The address set in SWITCH REGISTER switches is displayed in ADDRESS REGISTER indicators.
5	Set Teletype LINE/OFF/LOCAL switch to LINE. This connects the Teletype to the computer.
	NOTE **If some other reading device (such as the high speed paper tape reader) is used, make sure that the y value in bootstrap loader address xx7776 corresponds to the device as described in Table 4-2.**
6.	Place the absolute loader tape in the Teletype reader. Make certain that the special leader (a sequence of 351 punches) is under the reader station. Blank leader does not work.
7	Set ENABLE/HALT to ENABLE.
8	Depress START switch. The tape is now read into the computer which halts when the entire program is loaded.
9	Upon completion of loading this tape, the DATA display lights may be in any configuration. The main reason for this is that no check sum capability exists in the bootstrap loader.

4.3.2 Loading Binary Tapes

Any PDP-11 program punched in binary format may be loaded automatically by using the absolute loader. The absolute loader can be set up to select either an absolute or relocatable code. If a relocatable code is selected, the user may specify that the relocatable code start at a specific address or that the code start loading at the point the previous load stopped. The absolute loader also provides a checksum test to ensure accurate loading. Although the computer normally stops when the binary tape is loaded, instructions on the tape itself may cause the computer to begin execution of the program immediately after loading is finished. This action is beyond the control of the user because it is part of the program on certain binary tapes.

The following procedure is used for automatic loading of binary tapes into the computer by using the absolute loader:

Step	Procedure
1	Make certain that the absolute loader program is stored in core memory (refer to Paragraph 4.3.1).
2	Set ENABLE/HALT switch to HALT.
3	Enter starting address of absolute loader into SWITCH REGISTER switches. The starting address is x7500 (*1*7500 for 4K memory, *3*7500 for 8K memory, *5*7500 for 12K memory, etc.).
4	Depress LOAD ADDR switch. The starting address of the absolute loader is now displayed in ADDRESS REGISTER indicators.
5	Select the type of load desired by setting SWITCH REGISTER switches specified in Table 4-3.
6	Make certain that Teletype LINE/OFF/LOCAL switch is set to LINE.
	NOTE **The reading device may be changed at any time by the user without reloading the absolute loader. If a reader is to be changed, simply replace the contents of address xx7776 with the appropriate device status address (y value in Table 4-2).**
7	Load desired binary tape into reader by placing blank leader under the reader station.
8	Set ENABLE/HALT switch to ENABLE.
9	Depress START switch. This begins the binary tape load.
10	If the binary tape contains a transfer address instruction, the computer begins execution of the program as soon as loading is complete.
11	The computer stops when either loading is complete or there is a checksum error.

a. **Loading complete** – the low-order (right hand) byte displayed in the DATA indicators is zero. Additional binary tapes may be loaded by repeating steps 5 through 7 above and depressing the CONT switch.

b. **Checksum error** – the low-order byte displayed in the DATA indicators is *not* zero, thereby indicating a checksum error has occurred in the previous block of data. In this case, reposition the tape in front of the error-producing block and depress the CONT switch.

Table 4-3
Binary Tape Load Selection
(using ABSolute Loader)

Type of Load	Switch Register Settings	
	Bits 15-01	Bit 00
Normal (absolute)	Not applicable	0
Relocatable (continue where left off)	0	1
Relocatable (load at specified address)	Offset from tape origin	1

4.4 RUNNING PROGRAMS

When running any program, the program must first be loaded into the core memory either manually or by using one of the automatic loading programs (bootstrap loader or absolute loader). Once the program is in storage, it can be run at any time by loading the starting address of the program (refer to appropriate program documentation) into the SWITCH REGISTER switches, depressing the LOAD ADDR switch, and then depressing the START switch. The user also must make certain that the ENABLE/HALT switch is in ENABLE and that the appropriate external devices are on-line (connected to the computer).

The program can be manually stopped at any time by setting the ENABLE/HALT switch to HALT. It can be restarted from that point by returning the ENABLE/HALT switch to ENABLE and depressing the CONT switch. It can be started anew by reloading the starting address and depressing the START switch.

A program can be altered during operation, or new data introduced, through the SWITCH REGISTER. This console register has a bus address that the processor can reference in its instruction sequence. The information transferred may be treated as data or used to alter program flow.

Because of the speed of the computer, console indicators are of limited value while the computer is running. The flickering of major state and RUN indicators occurs during program execution. The absence of major states with the RUN full-on occurs during a WAIT loop; the absence of major state and RUN indicators with the BUS indicator on indicates peripheral bus control. Termination of a running program with the HALT instruction results in the display of processor register R0 in the DATA display. No data display is possible while the machine is running; DATA displays the central flow of data through the processor. During S-INST and S-CYCLE, the DATA display may be interpreted through the flow diagrams (refer to *KA11 Processor Manual*).

Major use of the indicator panel is made during manual operation. Here the console indicators reflect the console operations of LOAD ADDR, EXAM, and DEP. During S-INST and S-CYCLE, the machine states, address, and data information may be observed as instructions are manually sequenced (refer to Paragraph 3.3).

4.5 MANUAL OPERATION

Manual operation of the system is normally used for loading the bootstrap loader into the memory and for stepping through a program for checking purposes. The manual controls may be used for whatever other purposes the user desires such as loading and running special user programs. In these cases, refer to Paragraphs 3.2 and 3.3 for an explanation of the various console controls.

If the user desires to check a specific program step by step, the following procedure can be used:

Step	Procedure
1	Set ENABLE/HALT switch to HALT.
2	Set starting address of stored program in SWITCH REGISTER switches and depress START.
3	Depress LOAD ADDR switch.
4	Set S-INST/S-CYCLE switch to S-INST if the computer is to perform one instruction at a time; set switch to S-CYCLE if one bus cycle is to be performed at a time.
5	Depress START switch. The computer completes either a single instruction or bus cycle (as selected above) and then stops.
6	Depress CONT switch each time another cycle is desired.

The S-INST mode is recommended for the casual user. This mode of operation, coupled with the console functions of EXAM and DEP, allows observation of program flow. The S-CYCLE mode provides more detailed information which is important for maintenance. Reference to the flow diagrams (*KA11 Processor Manual*) for the meaning of the DATA and ADDRESS REGISTER displays is mandatory.

Under neither mode is the bus request (BR) or non-processor request (NPR) of peripheral devices honored; the console has the highest priority and is always serviced.

4.6 TELETYPE OPERATION

Operation of the Model 33 ASR Teletype is introduced in the following paragraphs as the basic input/output device of the PDP-11/20 System. More detailed information is available in Teletype Corporation Bulletin 273B (*Automatic Send-Receive Sets, Manual*), and in Appendix H of the *DEC Paper Tape Software Programming Handbook (DEC-11-GGPA-D)*. If a specific system uses other devices (such as the high-speed reader), operation is described in the appropriate peripheral manual.

4.6.1 Off-Line Operation

The Teletype can be operated independently from the PDP-11 Computer for typing, punching tapes, reading tapes, or duplicating tapes. Procedures for using the Teletype as an off-line device are given below.

4.6.1.1 **Typing** – When using the Teletype for typing only, perform the following:

Step	Procedure
1	Make certain Teletype primary power is on.
2	Set LINE/OFF/LOCAL switch to LOCAL.
3	Set START/STOP/FREE switch to STOP.
4	Depress punch OFF pushbutton.
5	Use Teletype keyboard as a typewriter.

4.6.1.2 **Punching Tapes** – The following procedure is used when punching paper tapes:

Step	Procedure
1	Make certain that Teletype primary power is on.
2	Set LINE/OFF/LOCAL switch to LOCAL.
3	Load the punch by raising the cover, manually feeding the paper tape from the top of the roll into the guide at the back of the punch, advancing the tape through the punch by manually turning the friction wheel, and then closing the cover.
4	Energize the punch by depressing the ON pushbutton.
5	Produce leader tape as follows: a. For tapes in binary or absolute format, a blank leader is necessary; depress the HERE IS key (on Model 33 ASR) to generate leader. b. For tapes in the bootstrap format, a special leader consisting of a series of 351 punches is required. Leader is supplied with the program tape; it is beyond the scope of this discussion to cover generation of bootstrap format leader.
6	Operate the keyboard in a normal manner to produce the punched tape. If an incorrect key is punched, the tape can be corrected as follows: a. Depress B.SP. the number of spaces needed. b. Depress RUBOUT key the same amount of spaces as above. c. Type corrected characters and continue.

4.6.1.3 **Reading Tapes** – The following procedure is used to read paper tapes. The output of the tape is printed automatically by the keyboard.

Step	Procedure
1	Load the tape in the paper tape reader.
2	Set LINE/OFF/LOCAL switch to LOCAL.
3	Depress punch OFF pushbutton.
4	Set START/STOP/FREE switch to START to turn on reader.
5	When tape reading is complete, set START/STOP/FREE switch to either FREE or STOP.

4.6.1.4 **Duplicating Tapes** – The following procedure is used to duplicate paper tapes. The Teletype punches a duplicate tape and also produces a typewritten copy of the tape being duplicated.

Step	Procedure
1	Load the tape to be duplicated into the paper tape reader.
2	Make certain that paper is loaded in the punch.
3	Set LINE/OFF/LOCAL switch to LOCAL.
4	Depress punch ON pushbutton. Punch *does not* start.
5	Set START/STOP/FREE switch to START. This starts both the punch and the reader.
6	When tape duplication is complete, set START/STOP/FREE switch to STOP and remove the duplicate tape.

4.6.2 **On-Line Operation**

When operated on-line, the Teletype is under computer control. The keyboard is used to input data to the computer and to receive output from the computer under program control. When operating on-line, make certain that primary power is on, the punch and reader are off, and the LINE/OFF/LOCAL switch is set to LINE.

If it is desired to read a tape into the computer or have the computer punch an output tape, the procedures are identical to off-line tape reading (Paragraph 4.6.1.3) and off-line tape duplication (Paragraph 4.6.1.4) except that the LINE/OFF/LOCAL switch must be set to LINE rather than LOCAL.

READER'S COMMENTS

PDP-11/20 SYSTEM MANUAL
DEC-11-HRIB-D

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