DEC-11-HR6A-D

PDP-11
Conventions Manual

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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The instructional times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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APPENDIX A
GENERAL MAINTENANCE

A.1 SCOPE

The basic maintenance philosophy of the PDP-11 system consists of presenting information that enables the user to understand how the system should function during normal operation. The user can then use this information when analyzing trouble symptoms to determine necessary corrective action. It is beyond the scope of the PDP-11 manuals to provide detailed troubleshooting information. However, where applicable, certain specific maintenance aids and adjustment procedures are included within individual manuals.

The purpose of this appendix is to provide general maintenance information such as required equipment, physical layout of modules within the system, interconnection for multiple box systems, power control, and installation and removal procedures for system units.

A.2 TEST EQUIPMENT AND TOOLS

Table A-1 lists various equipment, devices, and tools which may be required to perform tests and maintenance on the PDP-11 system.

Table A-1
Test Equipment and Tools

	Item	Type
Test Equipment	Oscilloscope	Tektronix Model 453 (or equivalent)
	Volt-Ohmmeter	Triplett Model 630 (or equivalent)
Devices	Extender Board	One W984A double extender board
		Two single extender boards (a W984A board cut in half)
	Maintenance Module Set	One W-130
		One W-131
	IC Test Clip	
	Pin probe tip	Tektronix #30
	Pointed tip solder iron	Rated at less than 40 watts
	Package of Solderwick	This is used for removal of solder on printed circuit boards
Tools	Screw drivers	
	Allen wrench set	
	Needle nose pliers	
	Wire strippers	

A.3 INSTALLATION OF ECO's

The procedures for installing engineering change orders (ECO's) on modules used in the PDP-11 system are listed in the *Module Rework Standard,* DEC SP 7605845-0-0, dated 7 August 1970.

A.4 MODULE IDENTIFICATION AND LAYOUT

The modules associated with the PDP-11 system unit are designated by an alphanumeric scheme as indicated on the various schematic prints. This scheme consists of a four-character designation, but at times may consist of only a three-character designation. The three-character scheme provides the same information as the four-character method by implying the value of the fourth character. This latter situation occurs on a system unit that can be housed at any system unit position within the overall PDP-11 system.

A typical system layout of a PDP-11/20 with six system units installed is shown in Figure A-1. This figure shows the units as viewed from the back panel pin side. The module and pin identification is as follows:

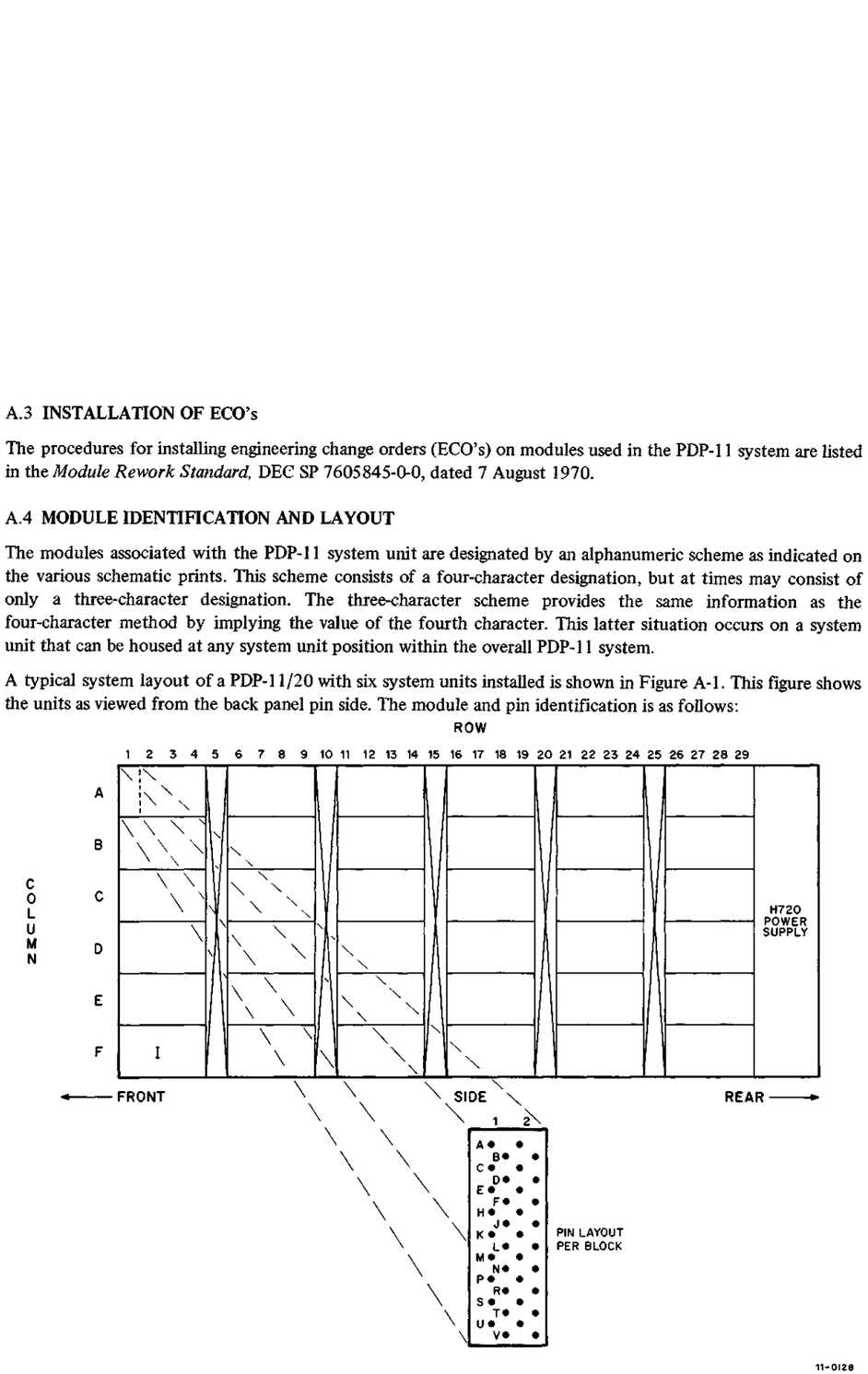

Figure A-1 Typical System Layout

a. Assume a designation of F4A1. The first character (F) designates column F (the lower column running from front to back).

b. The second character (4) designates row 4. (Sometimes the character is written as 04.) The rows run from side to side. Row 4 is the fourth from the front. Therefore, F4 designates that group of pins associated with columns F and row 4 (identified as ① in the figure). Row numbers 5, 10, 15, 20, and 25 are taken into account for the numbering sequence but do not contain modules or pins. They represent the spacing between blocks.

c. The final two characters identify a specific pin within the F4 block. This identification method conforms to the standard DEC pin identification method used for double-sided modules. This method is shown on Figure A-1.

All KA11 Processor prints use this four-character identification method. The MM11-E core memory, the HSR/HSP PC-11 reader, and the KL11 Teletype® control all use the three-character method. The prime reason for doing this is to make all prints equally applicable regardless of which slot is used for system unit installation. In this method, the column is given the pin identification. No matter which row the modules are inserted into (provided the wiring is for that device), the modules have the same column and pin identification.

A.5 MODULE COMPONENT IDENTIFICATION

The individual components located on any module of the PDP-11 system are identified, along with physical location, on the first sheet of the specific module print set.

A.6 UNIBUS CONNECTIONS

Instructions for connecting to the Unibus or adding additional devices to an installation are covered in the *Unibus Interface Manual,* DEC-11-HIAA-D.

A.7 MULTIPLE BOX SYSTEMS

Whenever BA11 extension mounting boxes are added to an existing basic mounting box configuration, it is necessary to interconnect (by means of the Unibus), the AC LO and DC LO functions of each additional power supply. This is required to ensure that power failure in any box causes proper processor response. This requirement is also necessary for any user-manufactured and/or interfaced device which needs processor response to power failure and does not receive its power from a BA11 box.

A.8 POWER CONTROL

Primary power for a basic PDP-11/20 System is 120 VAC, 50/60 Hz (H720-A power supply). Variations in these values are possible by adhering to the wiring requirements shown on the H720 power supply schematics and assembly drawings which are part of the system print set.

The power receptacle at the rear of the H720 power supply always furnishes the same power as that supplied on the input line. The power at this receptacle is directly controlled by the POWER/OFF/PANEL LOCK switch on the programmer's console. The internal fans for individual BA11 mounting boxes are always across a 120-VAC source as long as wiring requirements for the H720 power supply are followed.

Those systems using a free-standing base cabinet (H960) have additional fans mounted in them. The number of fans and their power requirements are dependent on the system procurement specifications. In 120-VAC systems, cabinet fans are plugged into the H720 receptacle. Some 240-VAC systems may have two 120-VAC fans wired in series. Another possible 240-VAC configuration may use an H722 step-down transformer. In this case, the fan(s) are wired to the 120-VAC side of the transformer along with other 120-VAC options.

NOTE

If any change in input line power from its original configuration is anticipated, the procurement specifications must be considered.

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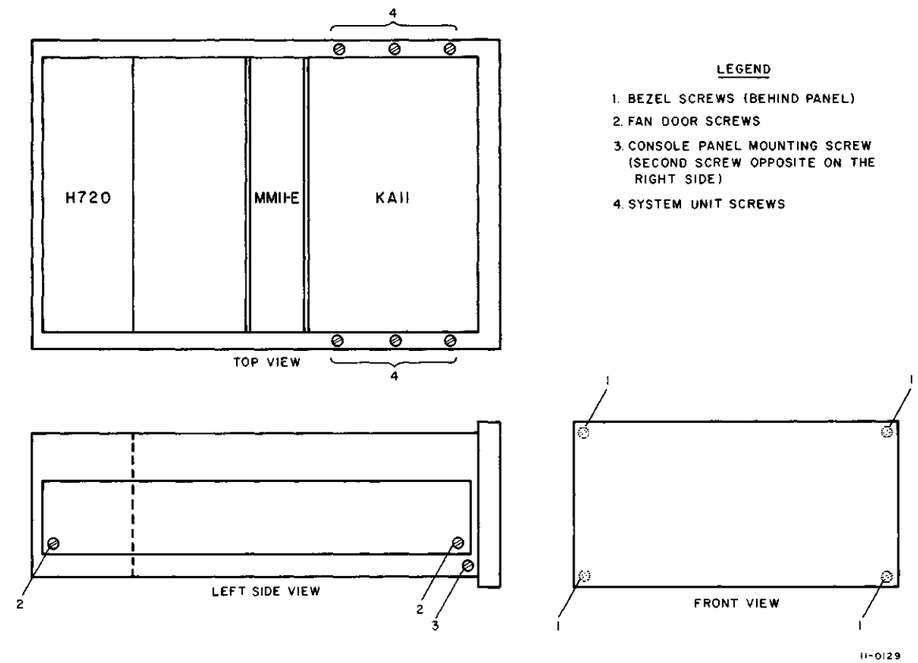


Figure A-2 Mounting Hardware

The entire system (including options) can be controlled by using the POWER/OFF/PANEL LOCK switch on the programmer's console. This is accomplished by parallel connecting all additional mounting boxes, options, and peripherals from the receptacle to the main mounting box. Most DEC-manufactured equipment has receptacles for interconnecting other units in this fashion.

A.9 SYSTEM UNIT REMOVAL/INSTALLATION

The following procedure is to be used whenever removing a system unit from the mounting box. Refer to Figure A-2 for location of items mentioned in this procedure.

a. Make certain that all power is turned off.

b. Remove the top and bottom covers of the mounting box.

c. Release the front bezel by removing the Phillip's head screw at each of the four corners.

d. Remove the bezel.

CAUTION

This unit can be easily broken, so handle the bezel with care.

e. Remove the two screws that secure the KY11-A programmer's console. These screws are located approximately two inches from the bottom on both side panels.

f. Open the fan door by releasing the two fasteners which are mounted on the door.

g. Once the fan door is open, the following units are to be removed:

1. Power bus (3 modules)
2. M780 Teletype Control interconnecting cables
3. M781 HSR/HSP Control interconnecting cables
4. M920 Unibus connector
5. KY11-A Console panel

CAUTION

Because of the size of the KY11-A console and the extremely tight fit, extreme care must be used when removing this component in order to prevent damage.

A.10 MAINTENANCE TIPS

A.10.1 Diagnostic Programs

The MainDEC-11 diagnostic programs are designed to test particular devices, operations, or functions. Their purpose and operating instructions are included in the documentation supplied with each test tape. Processor Test 17 is an overall system exerciser and, as such, is a prime vehicle for isolating malfunctions of a device.

Once a fault has been isolated to a specific device by Test 17, the special tests for the device, operation, or function can be used to further determine the cause of the malfunction. This method, in most cases, determines the hardware problem areas. However, a problem may exist, all diagnostic programs perform satisfactorily, yet user equipment and/or programs fail. In this instance, a more likely place to look for the cause of the problem is the user program and/or equipment.

A.10.2 KM11 Maintenance Set

The KM11 Maintenance Set consists of the W130 and W131 modules and is one of the most valuable tools that can be used to troubleshoot the KA11 Processor. The Maintenance Set provides a capability for single-clock stepping through programs, for disabling time out, and for providing BUS SSYN, all under operator control. It also furnishes indicators of ISR and BSR time states, MSYN, BSYN, Traps, R/W2, and condition codes. Three test indicators are available for connection of signals which may be desired in the course of troubleshooting. The connections can be made to the appropriate pins on the back panel wiring. Complete instructions for using the Maintenance Set are given in the *KM11 Maintenance Set Manual.*

A.10.3 Observation of Service Major State Operation

In order to observe operation through the various ISR states, the machine must be single-clocked by the KM11 Maintenance Set with the ENABLE/HALT switch in the ENABLE position. If this switch is set to HALT, the console always gains control in SERVICE * ISR0, and the processor never proceeds through the rest of the major states.

APPENDIX B
LOGIC SYMBOLOGY

B.1 GENERAL

The symbology employed by the PDP-11 system and M-series modules is similar to MIL-STD-806B. This appendix describes the modified DEC symbology with definitions of logic functions, graphic representations of the functions, and examples of their application. A Table of Combinations is also shown. A more detailed explanation of M-series logic is contained in the *1970 DEC Logic Handbook.*

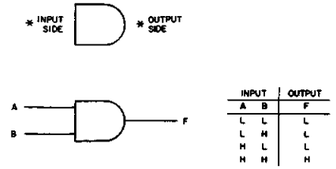
B.2 LOGIC SYMBOLS

In the following list of logic symbols, truth tables accompany the graphic representations. The truth tables use the letter H to mean HIGH (+3V) and the letter L to mean LOW (0V).

B.2.1 State Indicator

A small circle symbol at the input(s) of a function indicates that the relatively low (L) input signal activates the functions; the absence of this symbol indicates that a relatively high (H) input signal activates the function. Similarly, a small circle at the output of a function indicates that the output terminal of the activated function is relatively low; the absence of this symbol at the output indicates that the output is relatively high. Examples of this symbology with the AND and OR functions follow.

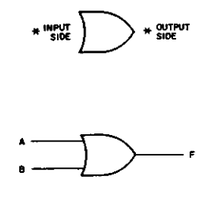
B.2.1.1 **State Indicator Absent** – The symbol shown in Figure B-1 represents the AND function. The output (F) is high only when the inputs (A and B) are high.



INPUT A	INPUT B	OUTPUT F
L	L	L
L	H	L
H	L	L
H	H	H

Figure B-1 AND Function

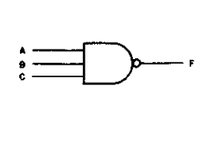
The symbol shown in Figure B-2 represents the OR function. The OR output (F) is high if one or more inputs (A and B) is high.



INPUT A	INPUT B	OUTPUT F
L	L	L
L	H	H
H	L	H
H	H	H

Figure B-2 OR Function

B.2.1.2 **State Indicator Present** – The symbol shown in Figure B-3 represents one version of the NAND function. The output is low only when all of the inputs are high. NAND logic is the major gate configuration of the PDP-11 system.



INPUT A	INPUT B	INPUT C	OUTPUT F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Figure B-3 NAND Function

The symbol shown in Figure B-4 represents one version of the NOR function. The output is low if one or more of the inputs is high.

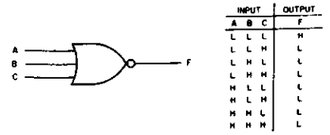


Figure B-4 NOR Function (First Version)

The symbol shown in Figure B-5 represents another version of the NOR function. The output is high if one or more of the inputs is low. Note that the truth table for this function is identical to one version of the NAND function.

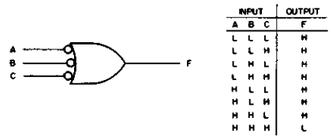


Figure B-5 NOR Function (Second Version)

B.2.2 Table of Combinations

Figure B-6 illustrates the applications and functions of two variables and equivalents, as well as the relationship to DEC logic.

B.2.3 Flip-Flop

The flip-flop is a device that stores a single bit of information. (See Figure B-7.) It has three possible inputs, set, clear, and the data input (C and D). There are two data outputs, 0 and 1. If the D input is high when a pulse appears at the C input, the flip-flop sets (1). Similarly, if the D input is low when input C is pulsed, the flip-flop clears (0). The converse of the above two statements is true when the graphic symbol D input has a small circle preceding it. The direct clear and direct set inputs are normally high. The clear and set functions occur with a high-to-low transition.

B.2.4 One-Shot Functions

The symbols shown in Figures B-8, B-9, and B-10 show examples of the one-shot (OS) function. The output signal shape, amplitude, duration, and polarity are determined by the circuit characteristics of the OS device. When it is not activated, the one-shot device is in either a 0 or 1 state. When the input is pulsed by the appropriate level change, the 1 output goes high and remains high, and the 0 output goes low and remains low for the specific time of the device.

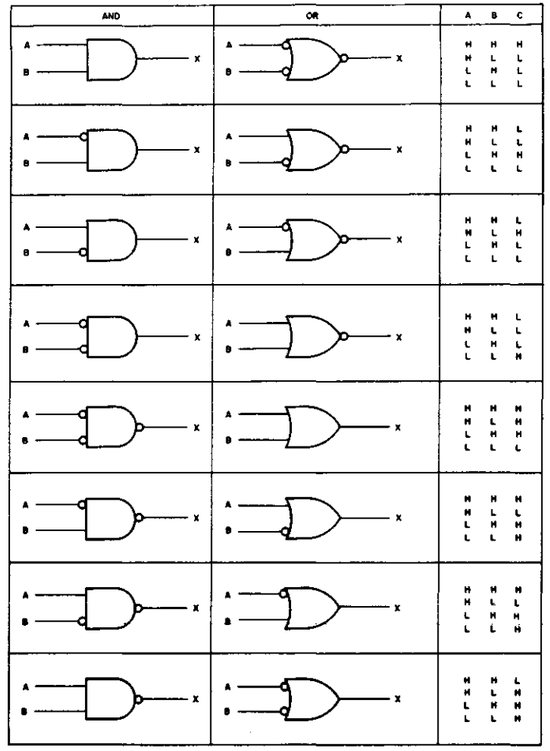


Figure B-6 Table of Combinations

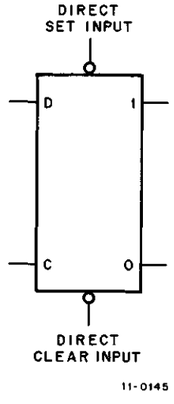
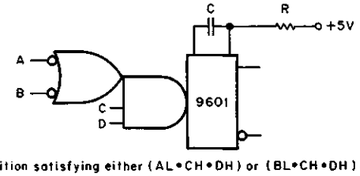


Figure B-7 Flip-Flop



When the logical transition satisfying either (AL•CH•DH) or (BL•CH•DH) occurs, the outputs of the 9601 change state for a time ≃ 0.43 RC.

Figure B-8 9601 One-Shot

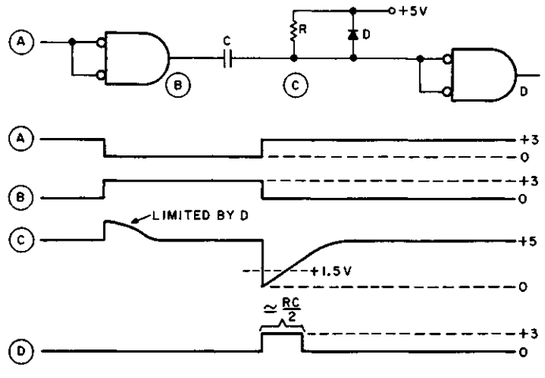


Figure B-9 Positive Edge Triggered One-Shot
(used only by memory logic)

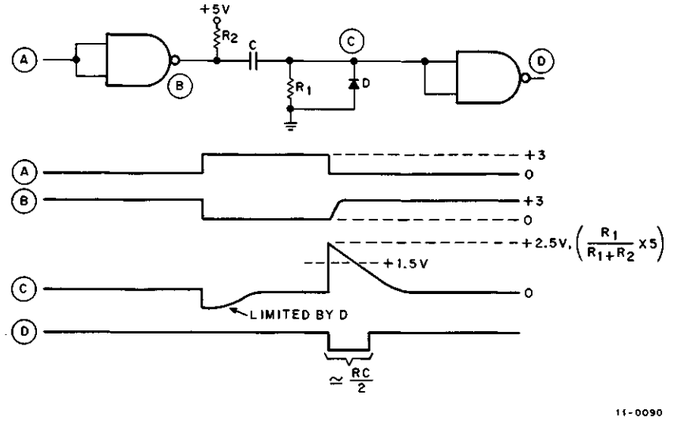
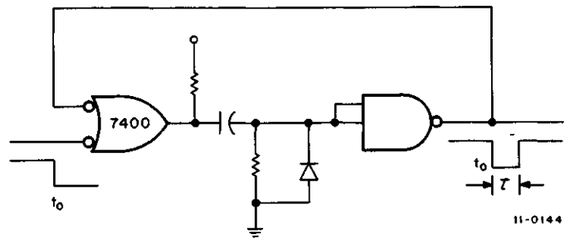


Figure B-10 Negative Edge Triggered One-Shot (Pulser)

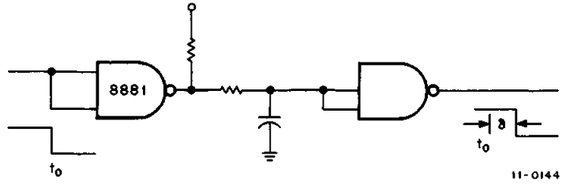
B.2.5 One-Shot Delays

The one-shot delay shown in Figure B-11a provides a short pulse at its output as a function of a level change to low level on its input. The nominal duration of the pulse (pulse width) is noted by τ. The nature of the circuit prohibits this delay from being one of close tolerance. Besides providing a pulse output, the circuit might be used for a delay if the rising edge of the pulse output is used as a clock input to a D-edge flip-flop.

A level delay is provided by the circuit shown in Figure B-11b. An input level transition to the low level causes the open collector gate to deactivate and the capacitor to charge through the resistor causing a delayed level change. The delay time is indicated by δ.



a. One-Shot Delay (Pulser)



b. Level Delay

Figure B-11 One-Shot Delays

B.2.6 Schmitt Trigger

The symbol in Figure B-12 represents the Schmitt trigger (ST) function. This device is actuated when the input signal crosses a certain threshold voltage. Output signal amplitude and polarity are determined by the circuit characteristics of the device. The unactuated state of the ST is either 0 or 1. When actuated, it changes to the opposite state and remains there until the input no longer remains above the actuating threshold voltage.

Figure B-12 Schmitt Trigger

B.2.7 Amplifier

The symbols shown in Figure B-13 represent a linear or nonlinear current or voltage amplifier. Level changers, inverters, emitter followers, and lamp drivers are examples of devices for which this symbol is applicable.

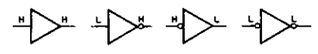


Figure B-13 Amplifier

B.2.8 Time Delay Symbol

The symbol for a delay is shown in Figure B-14. The duration is specified within the symbol except when there are two or more outputs. In this case, the outputs have the duration time adjacent to each output.

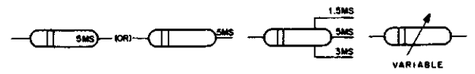


Figure B-14 Time Delay

B.2.9 General Logic Symbol

Symbols for functions not specified elsewhere are normally represented by a box as shown in Figure B-15. Examples of this symbology are shift registers, decoders, and buffers.

Figure B-15 General Logic Symbol

APPENDIX C
DRAWING SET

C.1 INTRODUCTION

This appendix describes the specific conventions used on all PDP-11 logic drawings. A certain measure of information is conveyed by the method of presentation. The PDP-11 prints and wire lists correlate all signal names and allow both forward and reverse tracing of signals. The prints conform, in general, to DEC STD 056, *Distinctive Shape Logic Symbology*. Specific characteristics and conventions are discussed in the following paragraphs.

C.2 LOGIC DRAWING ORGANIZATION

The logic drawings consist of individual print sets which cover individual modules. In the processor Timing and States print set, for example, four sheets are used to document the M728 Timing and States module. A cover sheet (K1-1) provides component reference and location, supply voltage filter capacitors, and notes covering signal and circuit conventions. The remaining sheets (K1-2, K1-3, and K1-4) provide the logic drawings for the module. Signal names within the logic relate this logic to the rest of the processor. It is this interrelationship among the modules that allows separate print sets to adequately document the processor.

Not all prints conform rigidly to the format followed in the processor but do adhere to the general plan. For example, because of less logic, the KL11 Teletype Control print set does not make use of the K numbers. However, the general concept is the same. The M780 Teletype Transmitter and Receiver module is covered by a four-sheet print set. The first sheet is the cover sheet which provides component reference and location, supply voltage filter capacitors, interface jumper structure, and notes covering signal and circuit conventions. The second sheet covers the bus logic common to both the transmitter and receiver; the third sheet covers transmitter logic, and the fourth sheet covers receiver logic.

C.3 SIGNAL NAMES

Signal names contain a print prefix (such as K1-2) and a polarity suffix (H or L). The print prefix identifies the logic print from which the signal originated. In the KA11 Processor, there are 15 such multiple-page print sets with the print prefix located in each title block. In the print prefix, the number immediately following the K identifies the print set and the next number identifies the page within the set. Thus, K5-3 indicates print set five, sheet 3. The print prefixes, KY and KM, refer to the KY11-A Programmer's Console and the KM11-A Maintenance Console, respectively. Signal names beginning with BUS are an exception to the convention above. These signals represent a wired OR situation with multiple sources.

The polarity suffix identifies the logic level at which the named condition is true. Thus, for the signal K1-2 DATA CLR H, DATA CLR is true when the signal level is high. Logic gates are enabled by the named signal condition when the input signal's polarity suffix coincides with the input state indicator. The gate is disabled by the named condition if a conflict occurs.

C.4 SIGNAL FLOW

Signal flow, as indicated by gate orientations, is from left to right or from bottom to top of the print. The majority of prints flow from left to right with all module output signals brought to the extreme right. This technique eases the search for a source signal referenced from another module set. For example, on the K6-2 print (DATA PATH CNTL) at drawing reference 4C, the signal K1-2 REG LATCH H is used. The source of this signal is easily found on the K1-2 print (Timing and States) on the extreme right at drawing reference 1C. If the source signal is within the same print set, it is on the same module and may not have a module pin. If no module pin exists, the signal source is within the drawing and not at the extreme right.

The Data Paths print sets (K7 and K8) have signal flow from the bottom to the top. Module output signals end in vertical lines; input control signals have horizontal lines; input data signals begin in vertical lines.

When searching for the origin of a specific signal, it may be helpful to refer to Appendix D. This appendix lists all processor signal names in alphabetical order and lists the print on which the signal is originated.

C.5 WIRE LIST

The wire list supplements the logic drawings. It lists those module pins (under common signal names) that are wired together and allows a signal to be traced from its source to all inputs. It is also possible to trace from inputs to source, but this is more easily provided for in the print prefix of the signal name.

Each signal name entry in the wire list notes the signal name (RUN NAME and A/P), the module pin for this entry (PIN NAME), the order in which the pin is wire trapped (BAY ORDER), the level at which the wrap is made (Z), and the drawings upon which the module pin appears (DRAW).

Since multiple prints exist for a given module, a single module pin might appear on several prints. Such situations are noted by entries under DRAW, with commas separating the sheet numbers (for example, K1-2,3,4). The manufacturing process ensures that specific module pins are interconnected. However, the order or level of interconnection is not tested or guaranteed.

Some differences in nomenclature exist between the prints and the wire list. The most notable exceptions are:

a. The use of leading zeros in numerical fields to order signals. The print signal K1-2 S CLK H becomes K01-2 S CLK H on the wire list.

b. The wire list substitutes the letters FM (from) for a left arrow. The print signal K2-2 ISR ← 0 L becomes K02-2 ISR FM 00 L on the wire list.

c. Some signal symbols have been changed. For example, the print signal K2-3 DATO# ENTRY H becomes K02-3 DATO = ENTRY H on the wire list.

The wire list is ordered by print set number. In order to facilitate locating the point of origin of a specific signal, Appendix D provides a list of signals in alphabetical order and includes the appropriate print reference.

APPENDIX D
PROCESSOR SIGNALS

Signal Name	Polarity	Drawing
A		
A DATA 07	L	K07-2
A DATA 15	L	K08-2
A FM DEST/INSTR	H	K10-4
ACROSS DATA	L	K11-2
ADD	L	K10-2
ADD00	L	K07-2
ADD01	L	K07-2
ADD02	L	K07-2
ADD03	L	K07-2
ADD04	L	K07-2
ADD05	L	K07-2
ADD06	L	K07-2
ADD07	L	K07-2
ADD08	L	K08-2
ADD09	L	K08-2
ADD10	L	K08-2
ADD11	L	K08-2
ADD12	L	K08-2
ADD13	L	K08-2
ADD14	L	K08-2
ADD15	L	K08-2
ADDRESS 0	H	K13-4
ADDRESS 1	H	K13-4
ADRS BIT 1	H	K10-3
ADRS BYTE OP	H	K10-3
ADRS DONE	L	K10-3
ADRS DONE	H	K13-3
ADRS MODE 2	L	K10-3
ADRS MODE 2	H	K13-3

Signal Name	Polarity	Drawing
ADRS MODE 4	L	K10-3
ADRS MODE 4	H	K13-3
ADRS MODE 5	L	K10-3
ADRS MODE (3+5+6+7)	H	K10-3
ADRS MODE (4+5)	H	K10-3
ADRS MODE (4+5)*REG6	H	K10-3
ADRS MODE (6+7)	H	K10-3
ADRS MODE (6+7)	L	K04-3
B		
B ACLO	L	K13-2
B ACLO	H	K13-2
B BBSY	H	K02-3
B DATA 07	L	K07-2
B DATA 15	L	K08-2
B D00	H	K09-5
B D01	H	K09-5
B D02	H	K09-5
B D03	H	K09-5
B D04	H	K09-4
B D05	H	K09-4
B D06	H	K09-4
B D07	H	K09-4
B D08	H	K03-3
B D09	H	K03-3
B D10	H	K03-3
B D11	H	K03-3
B D12	H	K03-3
B D13	H	K03-3
B D14	H	K03-3
B D15	H	K03-3

Signal Name	Polarity	Drawing
B DEST (0)	H	K01-4
B DEST (1)	H	K01-4
B EXEC (0)	H	K01-4
B EXEC (1)	H	K01-4
B FETCH (0)	H	K01-4
B FETCH (1)	H	K01-4
B INTR	H	K13-3
B MSYN	H	K13-3
B SACK	H	K02-3
B SERVICE	H	K01-4
B SOURCE (1)	H	K01-4
B SSYN	L	K13-3
B SSYN	H	K13-3
BAR00 (1)	H	K09-5
BAR01 (1)	H	K09-5
BAR02 (1)	H	K09-5
BAR03 (1)	H	K09-5
BAR04 (1)	H	K09-4
BAR05 (1)	H	K09-4
BAR06 (1)	H	K09-4
BAR07 (1)	H	K09-4
BAR08 (1)	H	K09-3
BAR09 (1)	H	K09-3
BAR10 (1)	H	K09-3
BAR11 (1)	H	K09-3
BAR12 (1)	H	K09-3
BAR13 (1)	H	K09-3
BAR14	H	K09-3
BAR14 (1)	H	K09-3
BAR15 (1)	H	K09-3
BAR16 (1)	H	K09-2
BAR17 (1)	H	K09-2
BBSYF (0)	H	K12-3
BBSYF (1)	H	K12-3
BC0 (1)	H	K13-2
BC1 (1)	H	K13-2
BERRF (0)	H	K12-2
BIC	L	K10-2
BINARY	L	K10-2
BINARY	H	K13-3

Signal Name	Polarity	Drawing
BIS	L	K10-2
BIT	L	K10-2
BR	L	K10-2
BRANCH	L	K06-3
BRANCH	H	K10-2
BRQ	L	K03-2
BSR FM 12	L	K02-3
BSR FM 15	L	K02-3
BSR FM 17	L	K02-3
BSR 00	H	K01-3
BSR 01	L	K01-3
BSR 01	H	K01-3
BSR 03	H	K01-3
BSR 07	H	K01-3
BSR 08	L	K01-3
BSR 08	H	K01-3
BSR 12	L	K01-3
BSR 12	H	K01-3
BSR 14	L	K01-3
BSR 14	H	K01-3
BSR 15	L	K01-3
BSR 15	H	K01-3
BSR (1+3+7)	H	K01-3
BSR (3+7)	H	K01-3
BSR (7+8)	H	K01-3
BSR (7+14)	H	K01-3
BSR (15+14+12+8)	H	K01-3
BSR14 + SVC * ISR0	L	K15-2
BUS IN DONE	L	K02-2
BUS IN DONE	H	K02-2
BUS INDICATOR	H	K13-4
BYTE OP	H	K10-3
C		
C (1)	H	K09-5
C DATA	H	K10-4
CARRY 00	L	K01-2
CARRY 00 (0)	H	K06-5
CARRY 07	L	K07-2
CARRY 15	L	K08-2
CARRY DATA	L	K11-2

Signal Name	Polarity	Drawing
CARRY INSTR	H	K10-4
CBRF	H	K03-2
CBRF (0)	H	K03-2
CC OP	H	K10-3
CHANGE CODES	L	K10-3
CLK	L	K01-2
CLK	H	K01-2
CLK BR	L	K02-3
CLK BAR	H	K13-3
CLK C	H	K10-4
CLK IR	H	K06-2
CLK N'Z'V	H	K10-4
CLK OFF (0)	H	K01-2
CLK OFF (1)	H	K01-2
CLK PDNF	H	K15-2
CLK RESTART	L	K01-2
CLK RUN (1)	H	K01-2
CLK T	H	K10-4
CLR	L	K10-2
CMP	L	K10-2
CNPRF (1)	H	K03-2
CONS BR	H	K13-4
CONS GRANT (0)	H	K12-3
CONS GRANT (1)	H	K12-3
CONS NPR	H	K13-4
CONSF (0)	H	K13-4
CONSF (1)	H	K13-4
CONT	L	KY-3
CONT	H	KY-3
CSR 00	H	K13-4
CSR 00 (1)	H	K13-4
CSR 01	H	K13-4
CSR 02	L	K13-4
CSR 02	H	K13-4
CSR 03	H	K13-4
D		
D PERIF RELEASE	L	K02-3
DATA CLR	L	K01-2
DATA CLR	H	K01-2
DATA WAIT FM 1	L	K06-2

Signal Name	Polarity	Drawing
DATIP	L	K13-2
DATO ENTRY	L	K13-2
DATO ENTRY	H	K13-2
DATO = ENTRY	H	K02-3
DEC	L	K10-2
DEP	L	KY-3
DEP	H	K13-4
DEST MODE 0	L	K10-3
DEST MODE 0	H	K13-3
D00	H	K07-2
D01	H	K07-2
D02	H	K07-2
D03	H	K07-2
D04	H	K07-2
D05	H	K07-2
D06	H	K07-2
D07	H	K07-2
D08	H	K08-2
D09	H	K08-2
D10	H	K08-2
D11	H	K08-2
D12	H	K08-2
D13	H	K08-2
D14	H	K08-2
D15	H	K08-2
D07/0 ZERO	L	K09-2
D15/0 ZERO	L	K09-2
D15/8 ZERO	L	K09-2
E		
EXAM	L	KY-3
EXAM	H	KY-3
EXAM	H	K13-4
(EXAM+DEP)	L	K06-5
(EXAM*DEP)	H	K02-3
EXEC FM 1	H	K01-4
(EXEC*ISR0)	H	K06-3
(EXEC*ISR1)	H	K02-2
(EXEC*JSR)	H	K04-3
EXTRA	H	K06-3

Signal Name	Polarity	Drawing
F		
FETCH FM SVC	H	K15-2
(FETCH*ISR0)	H	K02-2
(FETCH*ISR1)	H	K01-4
G		
GATE C	H	K10-4
GATE CC FM BYTE	H	K11-2
GATE CC FM WORD	H	K11-2
GATE LEFT 15/0	H	K06-3
GATE RAFM DEST	H	K04-3
GATE RAFM SOURCE	H	K04-3
GATE RAFMBAR	H	K04-3
GATE FARMSAD	H	K04-2
GATE RIGHT 15/0	H	K06-3
GATE ROT/SHF	H	K10-4
GATE SEX	H	K06-4
GATE STFMD	H	K10-4
GATED B INTR	L	K13-3
GATED P RESTART	L	K15-2
GRANT BR	H	K02-3
GRANT	H	K02-3
GATE A FM-BD15/0	H	K06-4
GATE A FM R0	H	K06-3
GATE A FM-R0	H	K06-3
GATE A FM R15/1	H	K06-3
GATE A FM-R15/1	H	K06-3
GATE ADD 7/0	H	K06-3
GATE ADD 15/8	H	K06-3
GATE B FM BD15/0	H	K06-4
GATE B FM R15/8	H	K06-4
GATE B FM STPM	H	K06-4
GATE B/ISR0	H	K10-4
GATE B/ISR1	H	K10-4
GATE BUS FM D	H	K09-2
GATE BUS FM SR	H	K13-2
GATE BYTE 7/0	H	K06-3
GATE BYTE 15/8	H	K06-3
H		
HALT	L	KY-3
HALT	H	KY-3

Signal Name	Polarity	Drawing
HALT	H	K10-3
HALT F (1)	L	K11-2
HIGH C DATA	L	K11-2
I		
INCF	L	K13-4
INIT	L	KY-3
INIT	L	K13-2
INIT	H	K13-2
INSTR STPM 02	H	K10-4
INSTR STPM 03	H	K10-4
INSTR STPM 04	H	K10-4
INTERNAL ADRS	H	K02-2
INTERNAL ADRS	L	K02-2
INTRF (0)	H	K12-3
INTRF (1)	H	K12-3
IR00 (1)	H	K09-5
IR01 (1)	H	K09-5
IR02 (1)	H	K09-5
IR03 (0)	H	K09-5
IR04 (0)	H	K09-4
IR05 (0)	H	K09-4
IR06 (1)	H	K09-4
IR07 (1)	H	K09-4
IR08 (1)	H	K09-3
IR09 (0)	H	K09-3
IR10 (0)	H	K09-3
IR11 (0)	H	K09-3
IR12 (1)	H	K09-3
IR13 (1)	H	K09-3
IR14 (1)	H	K09-3
IR15 (1)	H	K09-3
ISR F M02/SERVICE	L	K02-2
ISR F M02/SERVICE	H	K02-2
ISR FM 00	L	K02-2
ISR FM 1	L	K02-3
ISR FM 15	L	K02-3
ISR 00	H	K01-3
ISR 00	L	K01-3
ISR 01	H	K01-3
ISR 01	L	K01-3

Signal Name	Polarity	Drawing
ISR 02	H	K01-3
ISR 03	H	K01-3
ISR 03	L	K01-3
ISR 07	H	K01-3
ISR 07	L	K01-3
ISR 08	H	K01-3
ISR 08	L	K01-3
ISR 12	H	K01-3
ISR 21	L	K01-3
ISR 14	H	K01-3
ISR 15	H	K01-3
ISR (1+3)	H	K01-3
ISR (3+7)	H	K01-3
ISR (12+15)	H	K01-3
(ISR12* - INTRF)	L	K13-2
J		
JMP	L	K10-3
JMP	H	K04-2
(JMP*JSR)	L	K10-3
JSR	L	K10-2
JSR	H	K10-2
L		
LATCH A 15/0	H	K06-2
LATCH B (0)	H	K06-2
LATCH B 15/0	H	K06-2
LEFT DATA 00	L	K10-4
LOAD ADRS	L	K13-4
LOAD ADRS	L	KY-3
LOAD ADRS	H	K13-4
LOAD ADRS	H	KY-3
LTC	L	K14-2
M		
M CLK	L	KM-2
M CLK ENABLE	L	KM-2
MOV	L	K10-2
MSYN (1)	H	K13-3
N		
N (1)	H	K09-5
N DATA	L	K11-2

Signal Name	Polarity	Drawing
NO SACK (0)	H	K13-2
NPR ENABLE	L	K15-2
NPR ENTRY	H	K12-3
NPRF	H	K03-2
O		
ODD ADRS ERR	L	K10-3
ODD ADRS ERR	H	K13-2
OVFLF (1)	H	K12-2
P		
P CLR DATA WAIT	H	K06-2
P CONSF (1)	H	K13-4
P DATA START	H	K06-2
P RESTART	L	K13-2
P TIME OUT	L	K13-2
PARTIAL BST FM 1	L	K02-3
PERIF RELEASE	L	K02-3
PERIF RELEASE	H	K02-3
PROC BG 04	H	K03-2
PROC BG 05	H	K03-2
PROC BG 06	H	K03-2
PROC BG 07	H	K03-2
PROC CNTL	L	K15-2
PROC CNTL	H	K13-4
PROC RELEASE	L	K02-2
PROC RELEASE	H	K02-2
PUPF (0)	H	K03-3
PWRF	L	K03-3
PWRF	H	K03-3
PWR UP	H	K13-2
P1 CSR 00	H	K13-4
P1 CSR	H	K13-4
P1 CSR	L	K13-4
P2 CSR	H	K13-4
P2 CSR	L	K13-4
P3 CSR	H	K13-4
P3 CSR	L	K13-4
R		
REG ADRS	L	K04-3
REG ADRS	H	K09-2

Signal Name	Polarity	Drawing
REG GATE	H	K01-2
REG LATCH	H	K01-2
REG 6	L	K10-3
RESET	L	K10-3
(RESET+ HALT)	H	K10-3
REQUEST	H	K02-3
RIGHT DATA 07	L	K10-4
RIGHT DATA 15	L	K10-4
ROT/SHF	L	K10-3
ROT/SHF C DATA	L	K10-4
ROT/SHF L	H	K10-3
ROT/SHF R	H	K10-3
RTI	L	K10-3
RTI	H	K10-4
RTS	H	K10-3
R/W1	H	K01-2
R/W2	H	K01-2
R/W3	L	K01-2
R/W3	H	K01-2
R00 (1)	H	K05-2
R01 (1)	H	K05-2
R02 (1)	H	K05-2
R03 (1)	H	K05-2
R04 (1)	H	K05-2
R05 (1)	H	K05-2
R06 (1)	H	K05-2
R07 (1)	H	K05-2
R08 (1)	H	K05-2
R09 (1)	H	K05-2
R10 (1)	H	K05-2
R11 (1)	H	K05-2
R12 (1)	H	K05-2
R13 (1)	H	K05-2
R14 (1)	H	K05-2
R15 (1)	H	K05-2
S		
S CLK	L	K01-2
S CLK	H	K01-2
SAD 00	H	K04-2
SAD 01	H	K04-2

Signal Name	Polarity	Drawing
SAD 02	H	K04-2
SAD 03	H	K04-2
SBC	L	K10-2
S/CYCLE	L	KY-3
SERV 0	L	K15-2
SERV 0	H	K15-2
SERVICE	L	K01-4
SERVICE	H	K01-4
(SERVICE*ISR0)	L	K12-3
(SERVICE*ISR0)	H	K12-3
(SERVICE*ISR0)	L	K01-3
(SERVICE*ISR8)	L	K01-3
SHIFT 1 SR	H	K02-2
S/INST	L	KY-3
(SO+DE)	H	K01-4
(SO+DE)	L	K01-4
SOURCE MODE 0	L	K13-3
SOURCE MODE 0	H	K10-3
SR ADRS	H	K09-2
SR16 (switch reg.)	H	KY-3
SR16 (switch reg.)	L	KY-3
SR17	H	KY-3
SR17	L	KY-3
SSYN (1)	H	K13-3
ST ADRS	H	K09-2
(ST+EX+DEP)	H	K06-4
ST PTR CLK	L	K01-3
STADRS	L	K02-3
START	L	KY-3
START	H	KY-3
START	H	K13-4
START F (1)	H	K13-4
STPM 02	H	K12-3
STPM 03	H	K12-3
STPM 04	H	K12-3
SUB	L	K10-2
SVC CLR OVFLF	H	K12-2
SVC FM INSTR	H	K10-4
SWAB	H	K10-3
ST05 (1)	H	K09-4

Signal Name	Polarity	Drawing
ST06 (1)	H	K09-4
ST07 (1)	H	K09-4
T		
T (1)	H	K09-4
TEST	L	K04-3
TEST	H	K10-4
TIME OUT (0)	H	K13-2
TIME OUT (1)	L	K13-2
TP1	L	K13-2
TP2	H	K13-4
TP2	H	K02-3
TRAPS	L	K12-3
TRAPS	H	K12-3
TRACF (1)	H	K12-3
TST 01	H	KM-2
TST 02	H	KM-2
U		
(U+B+R/S)	L	K10-3
(U * B * R/S)	H	K13-3
(U * R/S)	L	K01-4
(U+R/S)	H	K10-3
V		
V (1)	H	K09-5
V DATA	L	K11-2
W		
WAIT	L	K10-3
WAIT	H	K02-3
WAIT CLR	H	K15-2
(WAIT * -TRAPS)	L	K15-2
W/ENABLE 7/0	L	K04-3
W/ENABLE 15/8	L	K04-3
(WORD+MOVE)	L	K06-4
WRITE 7/0	H	K01-2
WRITE 15/8	H	K01-2
X		
X00	H	K05-2
X01	H	K05-2
X10	H	K05-2
X11	H	K05-2

Signal Name	Polarity	Drawing
Y		
Y00	H	K05-2
Y01	H	K05-2
Y10	H	K05-2
Y11	H	K05-2
Z		
Z (1)	H	K09-5
Z DATA	H	K11-2

APPENDIX E
PRODUCT CODE FOR SOFTWARE PRODUCTS

E.1 INTRODUCTION

This appendix describes the codes used to identify DEC software products. When a product is part of the maintenance library, the code is preceded by the word MainDEC. When a product is a programming library product, the code is preceded by the word DEC. The code itself is an eight-digit code in the form:

XX-XXXX-XX

An explanation of each of the digits in the code is presented in the following paragraphs.

E.2 COMPUTER SERIES – [XX]-XXXX-XX

The first two digits of the Product Code following the word DEC or MainDEC are used to designate the computer series. Any of the following are permitted:

Series	Computer
00	Not computer-oriented
01	PDP-1
04	PDP-4
05	PDP-5
58	PDP-5 and 8
06	PDP-6
07	PDP-7
79	PDP-7 and 9
08	PDP-8
8S	PDP-8/S
T8	TSS 8
8I	PDP-8/I
8L	PDP-8L
L8	Linc-8
LB	Lab-8
DEC 9A	PDP-9 Advance Package
DEC 9B	PDP-9 Basic Package
DEC 9L	PDP-9L
DEC 9S	PDP-9 Advanced System source tapes
DEC 9T	PDP-9 Paper Tape System
DEC 9U	PDP-9 DECtape System
DEC or MainDEC 09	Across the board on 9 line
MainDEC 9A	PDP-9 only
MainDEC 9I	Int 4K PDP-9I
10	PDP-10 (all systems)
11	PDP-11 (all systems)
T3	PDP-10/30 only
T4	PDP-10/40 only
T5	PDP-10/50 only
T9	PDP-10/40 and 10/50 only
CP	Computer Pac

E.3 PRODUCT IDENTIFICATION – XX-[XXXX]-XX

The next grouping of four characters represents the product identification.

E.3.1 Major Category

The first character of the product identification is the Major Category.

Major Category	Description
A	Assembler
B	Bibliographies
C	Checkout support
D	Diagnostics – See Section 2.5 for further details
E	Editing
F	Function/subroutine
G	General Manuals
H	Hardware (general description)
I	Installation
J	DDT
K	Compiler

L	Loader
M	Monitor
N	Notes on Techniques or applications
O	
P	PIP
Q	Quality Control, Checkout
R	Routines (other than functions and utility)
S	System Configuration (operating, libraries, etc.)
T	Test and demonstration
U	User Applications (desk calculation, oceanographic . . . etc.)
V	
W	
X	
Y	Utility
Z	Special case; none of the above apply

E.3.2 **Minor Category** (Systems Programs only. See Section E.3.5 for MainDECs)

The second character of the product identification is the Minor Category.

Minor Category	Description
A	Algol
B	Builder
C	Cobol
D	Debug (other than octal)
E	Program Development
F	Fortran
G	Procedural Guide
H	Sort or merge
I	I/O
J	Conversational
K	Keyboard
L	Linking
M	Macro
N	Translator
O	Octal Debug
P	Copy
Q	Arithmetic
R	Reference
S	PAL
T	Batch
U	Updating Programs
V	Verify
W	Systems
X	Instruction
Y	Library
Z	Special case; none of the above apply
1 – 0	To uniquely identify a series of programs that only efficiently fall into major category

E.3.3 **Option Category** (Systems Programs Only. See Section E.3.5 for MainDECs)

The third character of the product identification is the option category. Special is designated by Z. The designation indicates hardware features necessary to utilize the software; Y in this category means more than one tape apply. Tapes in this category will be sequentially numbered in place of the Y.

Option Category	Description
A	A/D converter or vice versa
B	
C	Card
D	Disk only
E	Extended arithmetic element
F	File oriented
G	
H	High-speed reader and/or punch
I	
J	
K	KSR35 keyboard only
L	Line printer
M	Magtape
N	
O	Plotter
P	Paper tape
Q	
R	
S	Scope
T	DECtape only
U	
V	680 system
W	
X	Extended core only
Y	More than one tape apply
Z	Special case; none of the above apply.
1 – 0	To uniquely identify a series of programs that only efficiently fall into major category

For PDP-12 only 1 = 12A
2 = 12B
3 = 12C

E.3.4 **Revision Category**

The last character of the product identification for DEC products is to be a sequential lettering scheme to identify revisions.

E.3.5 **Minor Category** (Diagnostic Programs Only)

The second character of the product identification is a number as follows:

Minor Category	Description
0	Processor, EXT arithmetic, options (i.e., I/O operations)
1	Memory, EXT memory
2	Reader, punch, TTY, printer
3	DECtape, LINC tape
4	Magnetic tape
5	Disk, drum
6	Displays, A-D, character generators
7	Systems test
8	Special devices
9	Other than above

E.3.6 **Unique Designation Category**

The last two digits of the product identification for MainDEC products are to be some sequential numbering or lettering scheme to identify individual products within the major and minor classifications. A suggested scheme is to begin with AA, using AB to supersede AA.

In situations where several products are covered by the same manual, or vice versa, the dominant product or manual has a product code ending in zero (xxx0). Each of the subset products takes on a sequential number (i.e., the general manual is numbered MainDEC-08-D1L0-D and the tapes in the series MainDEC-08-D1L1-PB and MainDEC-08-D1L2-PB).

E.4 **DISTRIBUTION METHOD – XX-XXXX-[XX]**

The last two characters of the Product Code are used to represent the method by which the product is distributed.

The first of the last two characters may be any of the following:

Medium	Description
C	Cards
D	Document
L	Listing
M	Magtape
P	Paper tape
U	DECtape
digit	A numbering series used in ASCII paper tapes only
G	General

The second of the last two characters represents the mode in which the product is distributed.

Mode	Description
A	ASCII
B	Binary
C	Combined modes
D	Dump
F	FIODEC
H	Hardware readin
I	FIODEC binary
M	Readin-mode (RIM)
N	Notice of change
O	Other (Linctape, special binary, etc.)
P	Package
R	Relocatable binary
T	Test patterns or test conditions
digit	A numbering series used in ASCII paper tapes only
(SPACE)	English Text

E.5 **SPECIAL CLASSIFICATION**

There is a provision made for a single-lettered special classification to follow the last two digits of the code. **This letter should be enclosed in parentheses.**

XX-XXXX-XX- (X)

Special Code	Description
A	Alternate mode (Product for one computer in format of another computer)
D	Draft copy
L	Limited distribution
P	Proposal
T	Test version

E.6 **TYPICAL EXAMPLE**

An example of the cover sheet for a sample program would be:

Identification

Product Code:	DEC-08-YQYA-D
Product Name:	Floating Point Package
Date Created:	April 18, 1965
Maintainer:	Software Service Group

Tapes in this series are numbered:

DEC-08-YQ1A-PB
DEC-08-YQ2A-PB
DEC-08-YQ3A-PB
DEC-08-YQ4A-PB

APPENDIX F
PDP-11 GLOSSARY

A

*absolute address	A binary number that is permanently assigned as the address of a storage location.
*absolute loader	A routine that allows the user to load blocks of code and data from paper tape punched in the absolute binary format.
access time	The time interval between the instant at which data is called for (or requested to be stored) from a storage device and the instant delivery (or storage) is started.
accumulator	A 16-bit register or memory location in which the result of an operation is formed.
*active release	Pertains to the Unibus. Indicates that the bus control is passed from the bus master to the processor by means of an interrupt operation. See "passive release."
address	A label, name, or number which designates a location where information is stored.
address field	That portion of a computer word either containing the address of the operand or containing the information necessary for calculation of the address.
*address selector	The M105 logic module used to decode an address from the processor to select up to four-word or eight-byte external registers.
address map	A table, chart or drawing showing the absolute addresses of all locations in the core memory.
algorithm	A prescribed set of well-defined rules or processes for the solution of a problem in a definite sequence.
alphanumeric	Pertaining to a character set that contains any of the 26 letters and 10 numerals.
analog-to-digital converter	A peripheral device that receives an analog signal and transforms it to an equivalent digital value.
AND gate	A circuit with multiple inputs that provides the desired output only when signals representing assertion are present at all inputs.
arithmetic unit	The component of a computer where arithmetic and logical operations are performed.
argument	An independent variable. For example, in looking up a quantity in a table, the number (or numbers) that identifies the location of the desired value.
ASCII	American Standard Code for Information Interchange. A standard code, using a coded character set consisting of eight-bit coded characters, used for data interchange among data processing communication systems and equipment. The code set includes both graphic and control characters.
assemble	To translate from a symbolic program to a binary program by substituting binary operation codes for symbolic operation codes and absolute or relocatable addresses for symbolic addresses.
assembler	A program that performs the translation from symbolic program to binary program.
asynchronous	Not synchronous. An asynchronous device is one which does not require all elements of that device to be operating in time coincidence.
*autodecrement	An address mode in the PDP-11 system that decrements the contents of a selected register **before** the register is used. This mode can step the register to the next lower byte (decrement by 1) or word (decrement by 2).
*autoincrement	An address mode in the PDP-11 system that increments the contents of a selected register **after** the register is used. This mode increments by 1 (byte) or 2 (word).
*autoindex	The process of autoincrementing or autodecrementing the value (±1 or ±2) by which an address is autoincremented or autodecremented.

B

background processing	Automatic execution of lower priority computer programs when higher priority programs are not using the system resources.
*bidirectional	Capable of traveling in either direction. Refers to Unibus lines on which signals can be transmitted or received.
binary	Pertaining to a number system with a radix of 2.
binary digit	One of the two states (0 or 1) of the binary number system. Usually referred to as a bit.
binary program	A short utility program which, when loaded, instructs the computer to read binary-coded data punched on paper tape and store it in core memory.
bit	A shortened form of binary digit; the smallest unit of information.
block transfer	Moving a large amount of data in one operation. For example: data from a disk into memory or vice versa.
bootstrap	A technique or device designed to bring itself into a desired state by means of its own action. For example, a routine whose first few instructions are sufficient to bring the rest of itself into the computer from an input device.
*bootstrap loader	A program that is toggled into the computer to allow a small set of programs in a special tape format to be loaded into the PDP-11.
boundary	See "word boundaries."

*Although these terms are used in other systems, here their definitions apply solely to the PDP-11.

*branch	A point in a routine where one of two or more choices is made under control of the routine. The PDP-11 has many branch instructions and one unconditional branch instruction.
breakpoint	A location at which execution of a program is stopped to allow operator investigation. A debugging routine inserts a breakpoint to control the running of the program being tested and to return control to the debugging routine after execution of the test program segment.
buffer	A storage device used to compensate for a difference in rate of data flow or time of event occurrence when transmitting data from one device to another.
buffer register	See "buffer."
*bus	See "Unibus."
*bus address	The current address on the bus; may be the address of a device, the processor, or a memory location.
*bus address register	A processor register that holds the address from the processor for display and then loads it onto the Unibus at the required time.
*bus device	Any external device, including core memory, that is connected to the Unibus and has an assigned device address and/or priority level.
*bus driver	A circuit or module used to pass signals to the Unibus in accordance with the transmission line characteristics of the bus.
*bus master	The bus device that has control of the Unibus.
*bus receiver	A circuit or module used to receive signals from the Unibus. These circuits use gates with high input impedance and proper logic thresholds to ensure that the received signal is compatible with the rest of the system.
*bus request	A request from a peripheral for control of the bus in order to become bus master and initiate an interrupt or perform a data transfer.
*bus slave	The peripheral that is communicating with the bus master.
*bus transceiver	A module containing both bus driver and bus receiver circuits.
*bus transmitter	See "bus driver."
byte	A group of binary digits usually operated upon as a unit; half of a word; in the PDP-11, bytes are eight bits long. See also, "high-order byte" and "low-order byte."

C

call	To transfer control to a specified routine.
calling sequence	A specified set of instructions and necessary data required to call a given routine.
carry	In performing binary addition, one bit of information often has to be carried from one digit of the addition to the next most significant digit. This operation is referred to as a "carry."
*carry bit	Indicates that an operation resulted in a carry from the most significant bit. During subtraction, indicates a borrow from bit 16.
central processor	See "processor."
channel	A path, along which, signals can be transmitted; for example, data channel or output channel. Also refers to a more general path composed of a number of components, for example, communications channel.
character	A single letter, numeral, or symbol that is used to represent information.
checksum	A value representing the sum of all bytes in a program. When the program is loaded, the sum of the bytes can be compared with the checksum to make sure that the entire program has been loaded correctly.
clear	To erase the contents of a storage location by replacing the contents with zeros; to set register and/or flip-flops in a device to the required initial states.
clock	A device that generates regular periodic signals for synchronization.
coding	To write instructions for a computer using symbols meaningful to the computer or to an assembler, compiler, etc.
command	A control signal, usually written as a character or group of characters, that is used to direct the action of a system program.
compile	To produce a binary-coded program from a program written in source (symbolic) language, by selecting appropriate subroutines from a subroutine library (as directed by the instructions or other symbols in the source program).
compiler	A program that produces a binary-coded program from a source (symbolic) program.
complement	The binary opposite of a number, variable, or function. See "one's complement" and "two's complement."
*condition codes	The four least significant bits of the processor status word. These bits monitor different results of previous operations. The four functions monitored are: zero, negative, carry, and overflow.
conditional branch	A branch that takes place only if a predetermined condition has been met.
conditional jump	A jump that occurs only if specified criteria have been met.
console	An external panel on the computer or peripheral where controls and indicators are available for manual monitoring and operating of the device.
control	A circuit or device used to provide a sequence of levels and/or pulses which cause a system or subsystem to carry out certain procedures.
*control and status register	A register, used with a peripheral, that contains information needed to communicate with the peripheral.
controller	See "dedicated controller."
*core memory	A read/write random access memory using ferrite cores as storage elements. In the PDP-11 system, core memory refers to the MM11-E memory normally used as the basic system memory.
crosstalk	Unwanted insertion of a signal from an adjacent channel.
crowbar	A large power bus normally used to pass excess voltage to ground if an overvoltage condition exists.

D

data	A general term used to denote any or all facts, numbers, letters, and symbols. It connotes basic elements or information which can be processed or produced by a computer.
data buffer register	A register used with a peripheral to temporarily store data that is to be transferred into or out of the processor or other device.
*data paths	That portion of the KA11 processor where normal processing and computation occurs. All modifications and routing of data within the processor are performed by the data paths which consist primarily of the input gating and latches, adder, and output gating circuits.

debug	To detect, locate, and remove mistakes from a program or malfunctions from a computer.
debugging program	An independent, self-contained service program which allows the programmer to communicate with the object program in order to make modifications, additions, and deletions.
decoder	A logic device capable of converting from one numbering system to another (such as an octal-to-decimal decoder) or designed to interrogate certain bits from an input word to supply specific information such as an address or operation code.
DECtape	A DEC development of convenient, pocket-size reels of digital magnetic tape; sometimes used to indicate the magnetic tape recording peripheral produced by DEC.
*dedicated controller	A processor or computer system, usually with a read-only memory, that is designed and/or used to control only one specific process. For example, a computer designed to continually monitor, evaluate, and change a chemical process.
*dedicated line	A signal path used for only one purpose.
deferred address	Indirectly addressed. The contents of the location is the address of the operand rather than the operand itself.
delimiter	A character that separates and organizes elements of data.
*destination major state	A PDP-ll major state that retrieves destination data from internal or external storage. All necessary address calculations for obtaining the destination data are performed at this time.
*device	Usually refers to an external device which is synonymous with the term "peripheral."
*device flag	A bit in either the interface logic or the device itself that is set to indicate a specific condition such as ready or busy.
*device selection code	Part of an address that is used to specify that a particular device has been selected for use.
*device-to-device transfer	Transfer of data without supervision of the processor. Data is passed directly from one device to another through the Unibus.
diagnostic	Pertaining to the detection and isolation of a malfunction or mistake; usually used in the form "diagnostic programming."
digit	A character used to represent one of the non-negative integers smaller than the radix. For example, in binary notation (radix 2), a digit is either 1 or 0.
digital-to-analog converter	A peripheral device that receives a digital value and transforms it to and equivalent analog signal.
*direct address	An address that specifies the location of an instruction operand.
*direct address mode	Any PDP-11 address mode that is not deferred.
*direct memory access	Transfer of data into memory without supervision of the processor. Data is passed directly between the core memory and another device through the Unibus. Transfers are usually accomplished with a non-processor request.
disable	To render inoperative or to prevent from being used. Normally used with reference to hardware as opposed to "inhibit" which normally refers to signals.
disk	A mass-storage device. Basic unit is a disk on which data is magnetically recorded. Data can be accessed randomly, and access time is faster than with magnetic tape because required search time is significantly less. Most disks can store considerably greater amounts of data than core memories.
display	A peripheral device used to portray data graphically. Normally refers to some type of cathode-ray tube system.
*double-operand	PDP-11 instructions that contain two address fields: one field for the source operand, and one field for the destination operand; two-address instruction.
double-precision	Pertaining to the use of two computer words to represent one number.
downtime	The time interval during which a device or system is inoperative.
driver	See "bus driver." Also refers to a software routine designed to interface directly to a device. For example, a disk driver.
dump	To copy the contents of all or part of the core memory, usually on to some external storage medium such as hard copy or paper tape.
*dynamic master-slave relationship	Indicates that control of the Unibus may be passed from a master to another peripheral which then becomes master. It is not necessary to first pass control back to the processor. See "master-slave."

E

edit	To arrange and/or alter information for machine input or output.
editor	A program that allows the user to produce edit symbolic files on line.
*effective address	The address actually used in the execution of a computer instruction.
emulator	A hardware device that permits a program written for a specific computer to be run on a different type of computer system.
*emulator trap	A PDP-11 instruction that calls an emulator routine.
enable	To set up conditions so that a specific device, circuit, or signal can be used. The opposite of inhibit.
end-around carry	The action of adding the most significant bit of a binary number to the least significant bit position.
execute	To carry out a specified instruction or to run a program on the computer.
*execute major state	A PDP-11 major state during which the specified instruction is performed.
executive routine	A routine that controls or monitors execution of other routines.
exit	To leave. Specifically, to leave a main program in order to enter a subroutine or vice versa.
explicit address	See "absolute address."
*external device	Peripheral. In the PDP-11 system, any device connected to the Unibus with the exception of the processor.
*external page	Addresses above 160000 which are reserved for device register and processor register addresses.

F

fanout	A number indicating the number of unit loads a specific output signal can drive.
fetch	The act of obtaining and decoding an instruction from the program.
*fetch major state	A PDP-11 major state during which the next program instruction is obtained and decoded, and a determination made as to what major state to enter next, based on the type of instruction decoded.

file	A collection of related records treated as a unit.
fixed point	The position of the radix point in a number system is constant according to a predetermined convention.
flag	A character that signals the occurrence of some condition, such as the end of a word.
flip-flop	A basic computer circuit or device capable of assuming one and only one of two stable states.
floating point	A number system in which the position of the radix point is indicated by one part (the exponent) and another part represents the most significant digits (the fraction).
flowchart	A graphical representation of the sequence of instructions required to carry out a data processing operation.
foreground processing	The automatic execution of high priority programs that have been designed to preempt the use of the computing facilities.
format	The arrangement of data.

G

*general register	One of eight 16-bit internal registers in the PDP-11 processor. These are used for temporary storage, as accumulators, as index registers, as stack pointers, and other general-purpose functions.

H

hard copy	Information stored on a permanent medium that is readable, such as a printout from a line printer or teletype printer.
hardware	Physical equipment such as mechanical, electrical, or electronic devices.
head	A component that reads, records, or erases data on a storage device. Often referred to as a recording head or magnetic head.
*high-order byte	The most significant byte in a word; in the PDP-11, indicates the byte occupying bit positions 8 through 15 of a word. The high-order byte is always an odd address.

I

*immediate address	An address mode that includes the operand as part of the instruction. The operand is the word immediately following the first word in a two- or three-word instruction in the program. This mode is actually the autoincrement mode used in conjunction with the program counter.
*index	An address mode that uses data in a general register as a base for address calculations to permit random access to items in tables or stacks of data.
indirect address	An address in a computer instruction that indicates a location where the address of the referenced operand is to be found. See "deferred."
inhibit	To prevent. Normally used with signals rather than hardware to indicate that the signal is prevented from occurring. Also used with memory. For example, the inhibit signal prevents the core from changing state.
initialize	To set counters, switches, and addresses to zero or other starting values at the beginning of, or at prescribed points in, a computer program.
input	The transferring of data from auxiliary or external storage into the internal storage of the computer.
*instruction register	An internal register in the KA11 processor that stores the instruction fetched from memory so that portions can be decoded as needed during subsequent time states.
interface	The hardware needed to allow communication between the system Unibus and the peripheral.
*interlocked	The interrelation of communication between the Unibus master and slave devices. This relation is such that for each control signal from the master, the slave must send a response before the operation continues.
internal storage	The storage facilities forming an integral physical part of the computer and directly controlled by the processor.
*interrupt	A temporary disruption of normal operation by a special signal from the computer or peripheral.
*interrupt control	The M782 logic module which contains necessary logic circuits to allow a peripheral device to gain control of the Unibus and perform a program interrupt.
*interrupt vector	Two locations containing processor status word and the program counter value which indicates the starting point of the interrupt routine.
I/O device	See "peripheral" or "external device."

J

jump	A departure from the normal sequence of executing instructions in a program. An unconditional jump causes the program to go to the specified location in the program; a conditional jump causes the program to go to the new location only if preestablished criteria have been met.

L

language	A set of representations, conventions, and rules used to convey information.
*last in, first out	A storage/retrieval method in which the last item stored is the first item retrieved.
*latch	A circuit that locks data into the processor input gates so that output states are maintained even when the input signals are removed. The latches are functionally part of the "data paths."
latency	The time delay involved while waiting for specified data to reach a desired point or while waiting for a specified response which must arrive prior to further processing.
leader	The blank section at the beginning of a magnetic or paper tape. In certain cases (such as the absolute loader) the loader is punched in a special format.
least-significant bit	The rightmost bit in a byte or word.
least-significant digit	The rightmost digit of a number.
level	A voltage that remains constant for a long time. There are two possible levels: low or high.
list	Usually refers to related data that occupies successive storage locations. In the PDP-11, the main distinction between a list and a stack is that a stack is automatically maintained by the processor and a list is not.
*literal	Used in programming to indicate that the value in the program is the actual value to be used by the computer. Opposite of "symbolic."
load	To place data into storage.
location	A place in storage or memory where a unit of data or an instruction can be stored.
loop	A sequence of instructions that is executed repeatedly until a termination condition exists.

*low-order byte	The least-significant byte in a word; in the PDP-11, indicates the byte occupying bit positions 0 through 7. The low-order byte is always an even address.

M

machine language	The actual language used by the computer in performing operations; usually refers to either binary or octal codes; also often used to refer to assembler language coding.
machine language programming	Writing a program in binary or octal notation, or converting from a symbolic program to a binary program.
macro instruction	An instruction in a source language that is equivalent to a specified sequence of assembler instructions.
main frame	See "processor."
*major state	A computer timing cycle. In the PDP-11 system, there are five major states: fetch, source, destination, execute, and service. Not all major states are entered for each instruction.
manual input	The entry of data by hand into a device at the time of processing.
manual operation	The processing of data in a system by direct manual techniques.
mask	A pattern of bits that is used to control the retention or elimination of portions of another pattern of bits; a filter.
mass storage device	A bulk storage device, such as a disk.
*master/slave	The relationship between two devices communicating through the Unibus. The controlling device is master, the responding device is the slave.
memory	The storage in the system; pertaining to a device in which data can be retrieved. See also "core memory," "read-only memory," and "wordlet memory."
memory address	Usually refers to the address in external core memory which is being used at the time for reading or writing.
mnemonic symbol	A symbol chosen to assist the human memory; a memory aid. For example, the abbreviation MPY for the word multiply.
most-significant bit	The leftmost bit in a byte or word.
most-significant digit	The leftmost digit of a number.
*mounting box	The cabinet used to house the basic KA11 Processor, core memory, and other logic circuits. The operator's console is attached to the front of the box. Other mounting boxes may be used for additional logic cards or memory and normally have a blank front panel. Sometimes "drawer" is used instead of "mounting box" but the latter is the preferred term.

N

negate	A process of converting the value of a binary function or variable to the equivalent two's complement number.
nested interrupt servicing	An operation by which servicing of an interrupt for a device can be interrupted in order to service a higher priority device. Upon completion, servicing of the lower priority device is automatically resumed. This operation is not limited to two devices; therefore, an interrupt can be interrupted by another device which in turn is interrupted.
*nesting	Including a routine or block of data within another routine or block of data. In the PDP-11, more specifically refers to interrupting of a routine by a subroutine that in turn is interrupted by another subroutine, etc. The processor keeps track of the data so that as each subroutine is completed, the next one is continued. Also refers to calling a subroutine from a subroutine.
*non-processor	Refers to data transfers between any two peripheral devices, including memory, without supervision of the processor. The two devices use the Unibus during data transfers which are accomplished between Unibus cycles.

O

object program	The binary-coded program which is the output after translation from the source language; the binary program that runs on the computer.
octal	A number system with a radix of 8 which is used as a shorthand notation of a binary number.
offline	Pertaining to equipment or devices not under direct control of the computer.
*offset	A two-digit octal number in an instruction that is multiplied by two and added to the program counter to indicate the location of the next instruction. The offset is normally used only in branch instructions.
one's complement	The binary number obtained by complementing all bits of another binary number. Used as the first step in complement arithmetic so that binary subtraction can be performed by using addition techniques. The second step is to increment the one's complement which then provides the two's complement number.
online	Pertaining to equipment or devices under direct control of the computer; also pertains to programs operating directly and immediately to user commands.
operand	That portion of an instruction code which is affected, manipulated, or operated upon.
operator	That which indicates the action to be performed on the operand.
OR gate	A circuit with multiple inputs that provides the desired output when a signal representing assertion is present at any input.
origin	The absolute address of the beginning of a program or of a unique area of code or data.
output	Information transferred from the internal storage of a computer to output devices or external storage.
overflow	Generation of a quantity beyond the capacity of the arithmetic or storage facility.

P

parity	A method for checking the correctness of binary characters. An extra bit (called parity bit or PB) is added to numbers in systems using parity. If even parity is used, the sum of all 1's in a number including the parity bit is even; if odd parity is used, the sum is odd.
*passive release	Pertains to the Unibus. Indicates that the bus master releases the bus by dropping the bus busy signal. See "active release."
peripheral	Any unit of equipment, outside of the processor or Unibus, that provides the system with outside communication, storage, and/or service. Also called "external device" or "I/O device."
*pointer	A core memory location containing the actual (effective) address of the desired data; in the PDP-11, pointer often refers to the register containing the pointer address. See "stack pointer."
*pointer address	See "pointer."

polling	A centrally controlled method of calling a number of devices to permit them to transmit information; interrogation of peripherals one at a time to determine which peripheral desires service. Not used in the PDP-11 system.
*pop	To remove a word from the top of a pushdown/popup list.
position independent	See "relocatable."
*power fail	Logic circuits that protect an operating program in the event computer primary power fails. The circuits automatically store current operating parameters of the program as well as indicators of a power failure. When power is returned, the processor automatically makes use of this information to continue the program.
predefined process	A named process consisting of one or more operations or program steps that are specified elsewhere in the program.
*priority arbitration	A method used by the processor to compare its own priority with priorities from devices requesting the bus in order to determine which device, if any, is granted control of the Unibus.
*priority interrupt	Refers to the four-level priority interrupt system employed by the PDP-11 system.
*priority transfer	The signal sequence by which a device is selected as next bus master. No actual bus transformer is performed, only selection of the next bus master.
procedure	The course of action taken for the solution of a problem or performance of a specified operation, a portion of an algorithm translated into machine code.
*processor	A unit of a computing system that includes the circuits controlling the interpretation and execution of instructions. The processor does not include the Unibus, core memory, interface, or peripheral devices. The term "main frame" is sometimes used but this term refers to all components (processor, memory, power supply) in the basic mounting box.
*processor status word	An addressable register in the external page indicating the current priority of the processor and the results of the previous operation as indicated by the condition code bits.
program	The complete sequence of instructions and routines necessary to solve a problem or perform a specified action.
*program counter	A general-purpose register (number 7) that contains the address of the next word to be fetched.
program library	A collection of available computer programs and routines in a specific format.
propagation delay	The time required to transfer information from the input to the output of an electronic device.
pulse	A voltage that goes from one level to another, remains there for a short time, and then returns to the original level.
pulse width	The length of time a pulse voltage is at the second, or transient level.
punched paper tape	A paper tape containing a pattern of holes used to represent data; a tape used to feed in or receive information from a computer system.
*push	To place a word on the top of a pushdown/popup list.
*pushdown list	A list that is constructed and maintained on a "last in, first out" basis.

R

radix	The base of a number system; i.e., the quantity of characters that can be used in each digital position of the number system.
random access	Unordered access, usually used to describe unordered access to data or a device.
read	To transfer information from an input device to internal storage; also refers to the internal acquisition of data from core memory or other external memories.
*read-only memory	A random access memory that contains components which permanently assume a specific state so that data can be read from memory but cannot be erased, changed, or added.
real time	Any data manipulation, calculation, or control operation that is performed during the monitored task rather than after completion. For example, a satellite control system is a real time system as opposed to a system that analyzes data some period of time after all of the data has been recorded.
*receiver	See "bus receiver."
*recursive	A code or program that permits a subroutine to be called and then, if desired, call itself during operation; a closed subroutine that calls itself.
*reentrant	Pure code which can be interrupted and started again without error. The interrupt service may use the interrupt routine. Upon completion of the interrupt, the routine continues from the interrupt point.
register	A device capable of storing a specified amount of data, such as one word; usually refers to a flip-flop storage device or core memory location.
*register mode	A PDP-11 address mode in which the operand is contained in one of the eight general-purpose registers.
relative address	The number that specifies the difference between the absolute address and the base address. Also, the address formed by the sum of the base and the displacement.
*relative mode	A PDP-11 address mode that specifies the operand address relative to the program counter to permit relocatable addresses. This mode is a combination of the index mode used in conjunction with the program counter.
relocate	To move a routine from one portion of storage to another and to adjust the necessary address references so that the routine can be correctly executed at its new location.
relocatable	See "relocate."
remote access	Communication with a computer by one or more stations that are distant from the computing facility.
*reserved instruction	Instructions that have an op code which has no defined function in systems using the processor. If any of these instructions are used, a trap occurs.
response time	The time which elapses between generation of an inquiry at a device and receipt of a response at the device.
restore	To return to its original condition. Normally refers to a memory restore cycle. Since the contents of a memory location are destroyed when read, they must be restored after each read cycle. This is accomplished automatically.
routine	A set of instructions, arranged in the proper sequence, needed to cause the computer to perform a desired task.
run	A single, continuous execution of a program.

S

scratch pad memory	Any memory used for temporary storage. Usually refers to internal storage registers that hold partial results or operands until needed to complete a calculation.

*service	In the PDP-11, refers to a major state during which extra operations are performed; in general, refers to servicing an external device that desires to communicate with the computer.
service routine	A program used for general support of the user. For example, I/O routines, diagnostics, and other utility routines.
shift register	A register in which all information stored in the register is shifted one bit position to the right or left according to a specified instruction or action.
sign bit	When using complementary arithmetic, the bit directly to the left of the number indicates the sign (+ or -) of the number. A 1 indicates negative numbers, an 0 indicates positive numbers.
*single-operand	PDP-11 instructions that contain only one address field, that of the destination operand.
software	The collection of programs, procedures, rules, and related documentation associated with operation of a specific computer. For example, compilers, editors, utility programs, and related documentation and run procedures.
*source address	The address of the first operand in a two-address instruction (double-operand instruction).
source language	A symbolic language that is an input to a given translation process.
*source major state	A PDP-11 major state that retrieves source data from internal or external storage. All necessary address calculations for obtaining the source data are performed at this time.
*stack	A dynamic, sequential list of data with special provision for access from one end. Storage and retrieval from stacks is called "pushing" and "popping" respectively. In the PDP-11, the stack is automatically maintained by the hardware.
*stack overflow	A condition that indicates a push onto the processor stack below absolute address 400.
*stack pointer	The element used to indicate the top item on a stack. In the PDP-11, general register 6 serves as a stack pointer. The contents of this register is the address of the first (bottom) word on the hardware stack.
statement	A meaningful expression or generalized instruction in a source language.
*status register	A 16-bit register in which the high-order byte is unused and the low-order byte stores the processor status word; a register storing the external device status word.
*status word	See "processor status word."
step	One operation in a routine.
store	To enter data into a device where it can be held and can be retrieved.
string	A connected sequence of entities such as characters in a command string.
subroutine	A small routine, usually performing only one task, that is called frequently from various points of the main routine.
subroutine, closed	A subroutine not stored in the main part of a program. Such a subroutine is entered by a jump or branch operation, and provision is made at the end of the subroutine to return control to the calling program.
subroutine, open	A subroutine that must be inserted into a program at each place it is to be used.
switch register	An 18-bit register composed of manually operated switches that are used to load either addresses or data into the PDP-11 system. The switch register is on the front of the processor console.
symbolic address	A set of characters used to specify a memory location within a program.
symbolic coding	Writing instructions using mnemonic notation instead of actual machine language (binary) notation.
symbolic language programming	Writing program instructions in a language which facilitates the translation of programs into binary code by making use of mnemonic conventions.
symbolic program	A service program that translates symbolic programs into binary-coded programs. The programmer writes the symbolic program using symbols which are meaningful to him and the symbolic program translates the symbols into binary code which is meaningful to the computer.
synchronize	To ensure that a level or pulse is presented to a system or component at the correct time.
synchronous	All changes occurring simultaneously or in a definite, timed sequence.
*system unit	A mounting unit composed of three 8-slot connector blocks used to mount logic modules. System units are the basic building blocks of the PDP-11 system.

T

*T bit	A bit in the processor status word used in program debugging. This bit can be set or cleared under program control. If set, a processor trap occurs upon completion of the instruction.
table	A collection of data in which each item is uniquely identified by its position relative to the other items, or by some other means.
tag	One or more characters attached to an item or record for the purpose of identification.
terminal	A device in a system through which data can either enter or leave.
*time out	A specified amount of time (10 microseconds) that the system waits for a response from a referenced address. If there is no response within the specified time, an error occurs. Time-out errors are caused, in general, by attempts to reference nonexistent memory or nonexistent peripherals or words at odd addresses.
time sharing	A method of allocating processor time and other computer services among multiple users so that the computer, in appearance, processes a number of programs simultaneously.
toggle	To use console switches for entering data into the computer internal storage or memory; to cause alternation of states as in toggling a flip-flop.
track address	The part of a mass storage device which is the beginning of a specific block of data.
trailer	Identical to "leader" except it is at the end, rather than the beginning of a tape.
*transceiver	See "bus transceiver."
translate	To convert from one language to another.
*trap	An unprogrammed jump to a known location, automatically activated by the hardware if certain predetermined conditions occur, such as illegal instructions, errors, etc.
turnkey	A computer console containing only one control, usually a power switch, that can be turned on or off only with a key.

U

*Unibus	The single, high-speed bus structure shared by the KA11 Processor, core memory, and all peripherals.
*unidirectional	Capable of traveling in only one direction. Refers to the Unibus control transfer lines that carry signals to select the next bus master.
unit load	All inputs impose a load on the outputs driving them. A TTL unit load requires 1.6 ma at ground and +40 ua at + 3 volts. The load imposed upon an output by an input can be defined as a number of unit loads.

V

*vector	Two words, containing the value of the program counter and processor status word, respectively, that direct the processor to a new routine.
*vector address	The address of the location containing the vector words.

W

*wait loop	A condition caused by the program WAIT instruction to allow the processor to wait for an interrupt. When the processor is in a wait loop, it does not compete for bus control by fetching instructions or operands from memory.
*word	A 16-bit unit of data in the PDP-11 that is stored in two successive locations. The word address is always an even address.
*word boundary	The division between even numbered addresses. Since each word occupies two storage locations, words can be addressed only on even boundaries; bytes can be addressed on either even or odd boundaries.
word count	The number of words in the block of data to be transferred.
word length	The number of bits in a word.
*wordlet memory	A small read/write memory used with the read-only memory. The wordlet memory (MW11-A) is used primarily for temporary data and instruction storage.
write	To transfer information from internal storage to an output device or external storage.

APPENDIX G
PDP-11 STANDARD ABBREVIATIONS

List 1 – Abbreviations

ABS	absolute
A/D	analog-to-digital
ADC	add carry
ADRS	address
ASCII	American Standard Code for Information Interchange
ASL	airthmetic shift left
ASR	arithmetic shift right automatic send/receive
B	byte
BAR	bus address register
BBSY	bus busy
BCC	branch if carry clear
BCS	branch if carry set
BEQ	branch if equal
BG	bus grant
BGE	branch if greater or equal
BGT	branch if greater than
BHI	branch if higher
BHIS	branch if higher or same
BIC	bit clear
BIS	bit set
BIT	bit test
BLE	branch if less or equal
BLOS	branch if lower or same
BLT	branch if less than
BMI	branch if minus
BNE	branch if not equal
BPL	branch if plus
BR	branch, bus request
BRD	bus register data
BSP	back space
BSR	bus shift register back space record
BSY	busy
BVC	branch if overflow clear
BVS	branch if overflow set
CBR	console bus request
CLC	clear carry
CLK	clock
CLN	clear negative
CLR	clear
CLV	clear overflow
CLZ	clear zero
CMP	compare
CNPR	console non-processor request
CNTL	control
COM	complement
COND	condition
CONS	console
CONT	contents continue
CP	central processor
CSR	control and status register
D	data
D/A	digital-to-analog
DAR	device address register
DATI	data in
DATIP	data in, pause
DATO	data out
DATOB	data out, byte
DBR	data buffer register
DCDR	decoder

List 1 – Abbreviations (Cont)

DE	destination effective address
DEC	decrement Digital Equipment Corporation
DEL	delay
DEP	deposit
DEPF	deposit flag
DIV	divide
DMA	direct memory access
DSEL	device select
DST	destination
DSX	display, X-deflection register
EAE	extended arithmetic element
EMT	emulator trap
ENB	enable
EOF	end-of-file
EOM	end-of-medium
ERR	error
EX	external
EXAM	examine
EXAMF	examine flag
EXEC	execute
EXR	external reset
F	flat (part of signal name)
FCTN	function
FILO	first in, last out
FLG	flag
GEN	generator
IDIVR	integer divide routine
INC	increment increase
INCF	increment flag
IND	indicator
INH	inhibit
INIT	initialize
INST	instruction
INTR	interrupt
INTRF	interrupt flag
I/O	input/output
IOT	input/output trap
IOX	input/output executive routine

List 1 – Abbreviations (Cont)

IR	instruction register
IRD	instruction register decoder
ISR	instruction shift register
JMP	jump
JSR	jump to subroutine
LIFO	last in, first out
LKS	line time clock status register
LOC	location
LP	line printer
LSB	least-significant bit
LSBY	least-significant byte
LSD	least-significant digit
LTC	line time clock
MA	memory address
MAR	memory address register
MBR	memory buffer register
MEM	memory
ML	memory location
MOV	move
MSB	most-significant bit
MSBY	most-significant byte
MSD	most-significant digit
MSEL	memory select
MSYN	master sync
ND	negative driver
NEG	negative
NOR	normalize
NPG	non-processor grant
NPR	non-processor request
NPRF	non-processor request flag
NS	negative switch
ODT	octal debugging technique
OP	operate operation
OPR	operator operand
PA	parity available
PAL	program assembly language
PB	parity bit
PC	program counter

PD	positive driver
PDP	programmed data processor
PERIF	peripheral
PGM	program
PP	paper tape punch
PPB	paper tape punch buffer register
PPS	paper tape punch status register
PR	paper tape reader
PRB	paper tape reader buffer register
PROC	processor
PRS	paper tape reader status register
PS	processor status positive switch
PTR	priority transfer
PTS	paper tape software system
PUN	punch
RD	read
RDR	reader
REG	register
REL	release
RES	reset
ROL	rotate left
ROM	read-only memory
ROR	rotate right
R/S	rotate/shift
RTI	return from interrupt
RTS	return from subroutine
R/W	read/write
R/WSR	read/write shift register
S	single
SACK	selection acknowledge
SBC	subtract carry
SC	single cycle
SE	source effective address
SEC	set carry
SEL	select
SEN	set negative
SEV	set overflow
SEX	sign extend
SEZ	set zero
SI	single instruction

List 1 – Abbreviations (Cont)

SP	stack pointer spare
SR	switch register
SRC	source
SSYN	slave sync
ST	start
STPM	set trap marker
STR	strobe
SUB	subtract
SVC	service
SWAB	swap byte
TA	trap address track address
TEMP	temporary
TDR	timing, driver
TK	teletype keyboard
TKB	teletype keyboard buffer register
TKS	teletype keyboard status register
TP	teletype printer
TPB	teletype printer buffer
TPS	teletype printer status register
TRT	trace trap
TSC	timing state control
TSS	timing, selection switch
TST	test
UTR	user trap
VEC	vector
WC	word count
WCR	word count register
XDR	X-line driver
XRCG	X-line read control group
XWCG	X-line write control group
YDR	Y-line driver
YRCG	Y-line read control group
YWCG	Y-line write control group

List 2 – Definitions

absolute	ABS
add carry	ADC
address	ADRS
American Standard Code for Information Interchange	ASCII
analog-to-digital	A/D
arithmetic shift left	ASL
arithmetic shift right	ASR
automatic send/receive	ASR
back space	BSP
back space record	BSR
bit clear	BIC
bit set	BIS
bit test	BIT
branch	BR
branch if carry clear	BCC
branch if carry set	BCS
branch if equal	BEQ
branch if greater or equal	BGE
branch if greater than	BGT
branch if higher	BHI
branch if higher than or same	BHIS
branch if less or equal	BLE
branch if less than	BLT
branch if lower or same	BLOS
branch if minus	BMI
branch if not equal	BNE
branch if overflow clear	BVC
branch if overflow set	BVS
branch if plus	BPL
bus address register	BAR
bus busy	BBSY
bus grant	BG
bus register data	BRD
bus request	BR
bus shift register	BSR
busy	BSY
byte	B
central processor	CP
clear	CLR
clear carry	CLC
clear negative	CLN

List 2 – Definitions (Cont)

clear overflow	CLV
clear zero	CLZ
clock	CLK
compare	CMP
complement	COM
condition	COND
console	CONS
console bus request	CBR
console non-processor request	CNPR
contents	CONT
continue	CONT
control	CNTL
control and status register	CSR
data	D
data buffer register	DBR
data in	DATI
data in, pause	DATIP
dato out	DATO
data out, byte	DATOB
decoder	DCDR
decrement	DEC
delay	DEL
deposit	DEP
deposit flag	DEPF
destination	DST
destination effective address	DE
device address register	DAR
device select	DSEL
Digital Equipment Corporation	DEC
digital-to-analog	D/A
direct memory access	DMA
display X-deflection register	DSX
divide	DIV
emulator trap	EMT
enable	ENB
end-of-file	EOF
end-of-medium	EOM
error	ERR
examine	EXAM
examine flag	EXAMF
execute	EXEC

List 2 – Definitions (Cont)

extended arithmetic element	EAE
external	EX
external reset	EXR
first in, last out	FILO
flag (when used alone)	FLG
flag (when used with signal name)	F
function	FCTN
generator	GEN
increase	INC
increment	INC
increment flag	INCF
indicator	IND
inhibit	INH
initialize	INIT
input/output	I/O
input/output executive routine	IOX
input/output trap	IOT
instruction	INST
instruction register	IR
instruction register decoder	IRD
instruction shift register	ISR
integer divide routine	IDIVR
interrupt	INTR
interrupt flag	INTRF
jump	JMP
jump to subroutine	JSR
last in, first out	LIFO
least-significant bit	LSB
least-significant byte	LSBY
least-significant digit	LSD
line printer	LP
line time clock	LTC
line time clock status register	LKS
location	LOC
master sync	MSYN
memory	MEM
memory address	MA
memory address reigster	MAR
memory buffer register	MBR

List 2 – Definitions (Cont)

memory location	ML
memory select	MSEL
most-significant bit	MSB
most-significant byte	MSBY
most-significant digit	MSD
move	MOV
negate	NEG
negative driver	ND
negative switch	NS
non-processor grant	NPG
non-processor request	NPR
non-processor request flag	NPRF
normalize	NOR
octal debugging technique	ODT
operand	OPR
operate	OP
operation	OP
operator	OPR
paper tape punch	PP
paper tape punch buffer register	PPB
paper tape punch status register	PPS
paper tape reader	PR
paper tape reader buffer register	PRB
paper tape reader status register	PRS
paper tape software system	PTS
parity available	PA
parity bit	PB
peripheral	PERIF
positive driver	PD
positive switch	PS
priority transfer	PTR
processor	PROC
processor status	PS
program	PGM
program assembly language	PAL
program counter	PC
programmed data processor	PDP
punch	PUN
read	RD
reader	RDR

List 2 – Definitions (Cont)

read-only memory	ROM
read/write	R/W
read/write shift register	R/WSR
register	REG
release	REL
reset	RES
return from interrupt	RTI
return from subroutine	RTS
rotate left	ROL
rotate right	ROR
rotate/shift	R/S
selection acknowledge	SACK
select	SEL
service	SVC
set carry	SEC
set negative	SEN
set overflow	SEV
set trap marker	STPM
set zero	SEZ
sign extend	SEX
single	S
single cycle	SC
single instruction	SI
slave sync	SSYN
source	SRC
source effective address	SE
spare	SP
stack pointer	SP
start	ST
strobe	STR

List 2 – Definitions (Cont)

subtract	SUB
subtract carry	SBC
swap byte	SWAB
switch register	SR
teleprinter status register	TPS
teletype keyboard	TK
teletype keyboard buffer register	TKB
teletype keyboard status register	TKS
teletype printer	TP
teletype printer buffer	TPB
temporary	TEMP
test	TST
timing, driver	TDR
timing, selection switch	TSS
timing state control	TSC
trace trap	TRT
track address	TA
trap address	TA
user trap	UTR
vector	VEC
word count	WC
word count register	WCR
X-line driver	XDR
X-line read control group	XRCG
X-line write control group	XWCG
Y-line driver	YDR
Y-line read control group	YRCG
Y-line write control group	YWCG

List 3 – ASCII CODE

ACK	acknowledge
ATL	alternate (mode)
BEL	bell
BS	back space
CAN	cancel
CR	carriage return
DC1	device control 1
DC2	device control 2
DC3	device control 3
DC4	device control 4
DLE	data link escape
EM	end-of-medium
ENQ	enquiry
EOT	end-of-transmission
ESC	escape
ETB	end-of-transmission block
ETX	end-of-test

List 3 – ASCII CODE (Cont)

FF	form feed
FS	file separator
GS	group separator
LF	line feed
NAK	negative acknowledge
NUL	null
RS	record separator
SI	shift in
SO	shift out
SOH	start of header
STX	start of text
SUB	substitute
SYN	synchronous idle
TAB	tab
US	unit separator
VT	vertical tab

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