DEC-11-H05SS-B-D

PDP-11/05-S, 11/10-S
system manual

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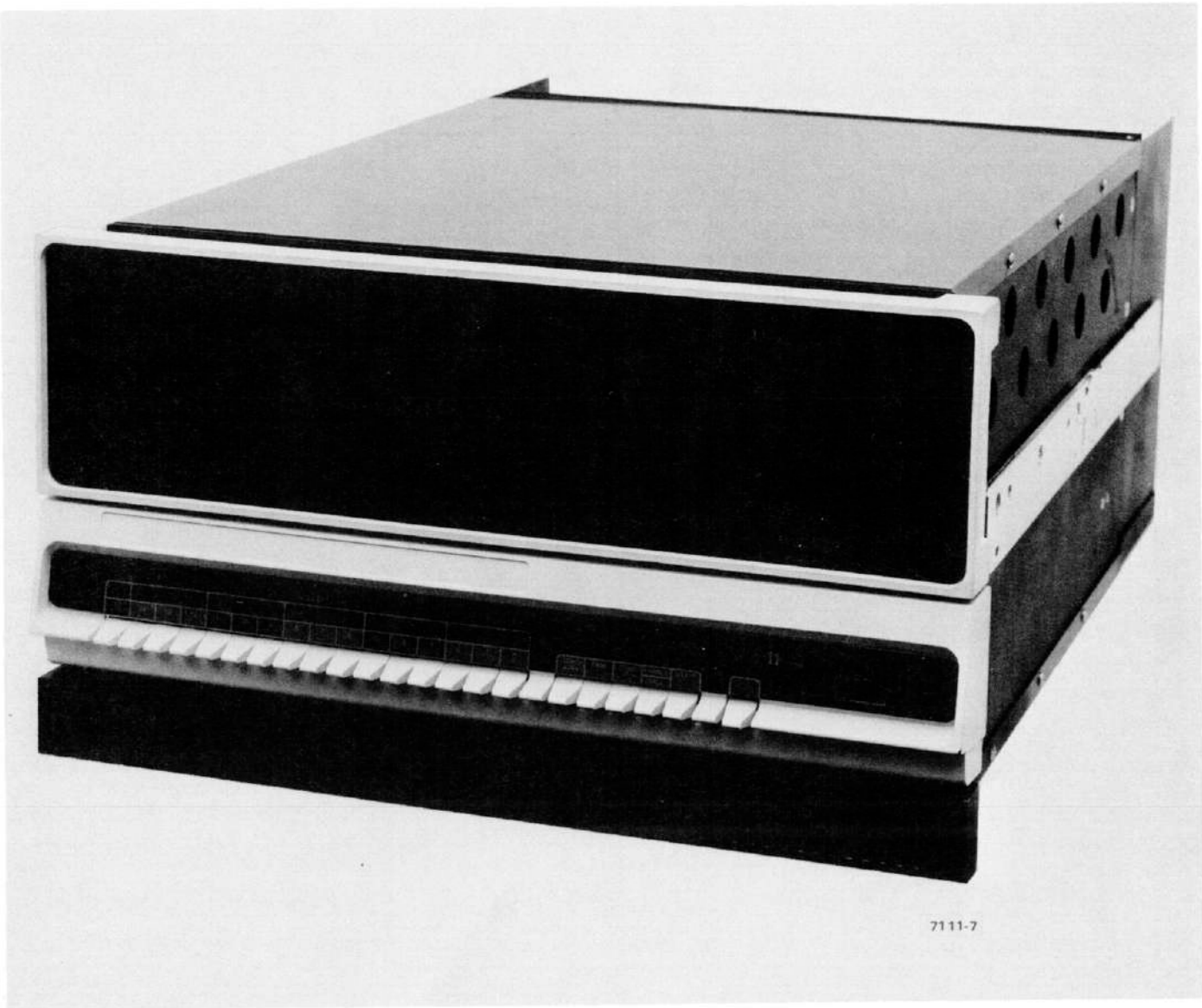

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual provides a general introduction to the PDP-11/05/10-S computer, including sections on installation, operation, the instruction set, options, equipment mounting, power, and maintenance, supplemented with references to other manuals in the PDP-11 series for detailed explanations.

The PDP-11/05/10-S series manuals provide the user with the theory of operation necessary to understand, operate, and maintain the PDP-11/05/10-S System. These manuals and the associated engineering drawings are discussed in Paragraph 1.3. The associated drawings are separate volumes documented by their Drawing Directory number. The manuals and drawings combine to form a complete documentation package.

The level of discussion in each manual assumes that the reader is familiar with basic digital computer theory. The maintenance philosophy presents information about normal system operation and enables the user to recognize trouble symptoms and take necessary corrective action. Each individual manual contains theory of operation, diagrams, and maintenance techniques.

This chapter lists the basic computer components (Paragraph 1.2) with a brief functional description and references applicable documents (Paragraph 1.3) and engineering drawings (Paragraph 1.4).

1.2 SYSTEM COMPONENTS

The PDP-11/05-S and the PDP-11/10-S are electrically the same. Digital Equipment Corporation (DEC) offers the PDP-11/05 for the Original Equipment Manufacturer (OEM). As such, it is sold in those configurations and with those services that are convenient for the OEM. The PDP-11/10 is offered for the End User and is sold in configurations that optimize its use with our small system software. More services and software are included with the PDP-11/10 for the End User.

The PDP-11/05-S and the PDP-11/10-S basic system incorporates the following major components:

- BA11-K Mounting Box
- 11/05/10 Backplane
- KD11-B Processor
- KY11-J Programmer's Console
- MM11-U Core Memory System
- Unibus

Figure 1-1 illustrates the relationship of the major functional components to the Unibus and the processor's internal bus.

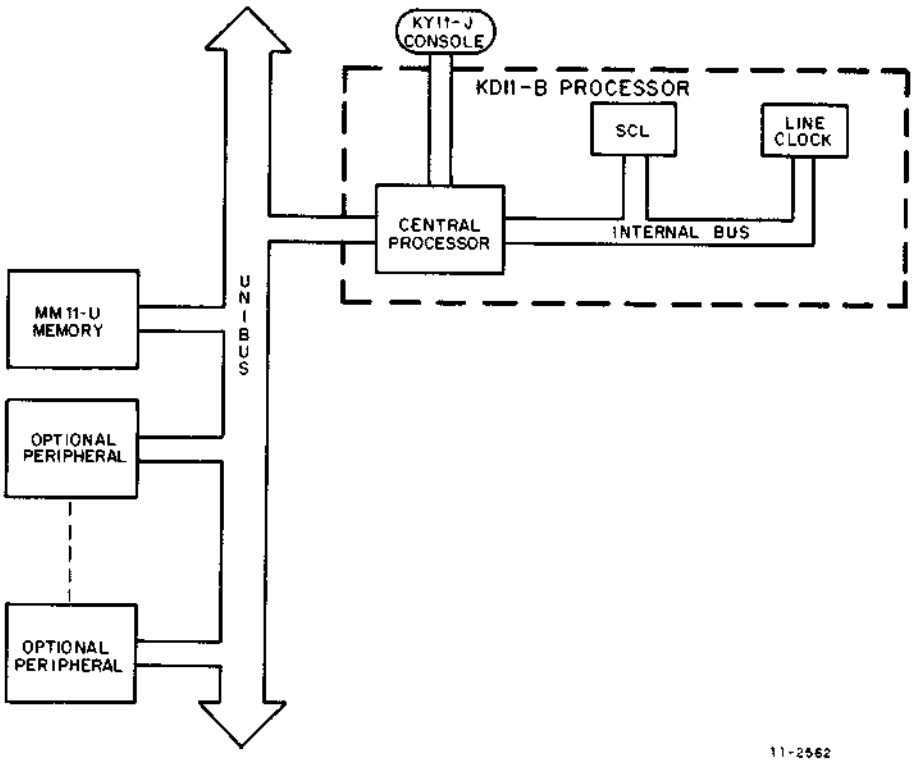


Figure 1-1 Relationship of Functional Components to Unibus and Internal Bus

1.2.1 BA11-K Mounting Box

The BA11-K Mounting Box is used to house and supply power to the PDP-11/05-S and 11/10-S computer. Additional power capacity is available to supply power to options installed within the mounting box. In addition to voltages, the power supply within the BA11-K Mounting Box provides three logic signals (LTC L, AC LO L, and DC LO L) which are used within the processor and memory, and may be used by 11-family expansion systems. The H765 Power Supply within the BA11-K Mounting Box interfaces to the logic backplane(s) via the power distribution board (DEC Part No. 5410864). The mounting box and its power system are described in detail in the *BA11-K Mounting Box Maintenance Manual.*

H765 Power Supply – The H765 Power Supply contains a transformer assembly, an ac input box, fans, five regulators, and a power distribution board. The ac input box matches the H765 Power Supply to the available line voltage. A type 7009811-1 input box is used for 115 Vac. A type 7009811-2 input box is used for 230 Vac. The five regulators supply dc voltages via the power distribution board, to the backplanes mounted in the BA11-K. The power supply is controlled by the console power key switch via a remote control cable. The cable is run through the right hand side panel of the mounting box and plugs into one of four remote power control cable connectors (J3) on the power supply.

1.2.2 Backplane

The backplane is the connector assembly into which the computer modules are plugged. It provides the signal and power routing among the logic modules that make up the PDP-11/05/10-S. The backplane contains nine slots which are utilized as illustrated in Figure 1-2. There are several slots that are prewired and dedicated for options (Small Peripheral Controllers, Serial Communication Line Connector Module M9970, and KM11-A and KM11-B Maintenance Modules). Power is brought to the backplane by a harness that plugs into the power distribution board of the H765 Power Supply. Power within the backplane is routed via the etch, while signal routing is implemented via the wire-wrap.

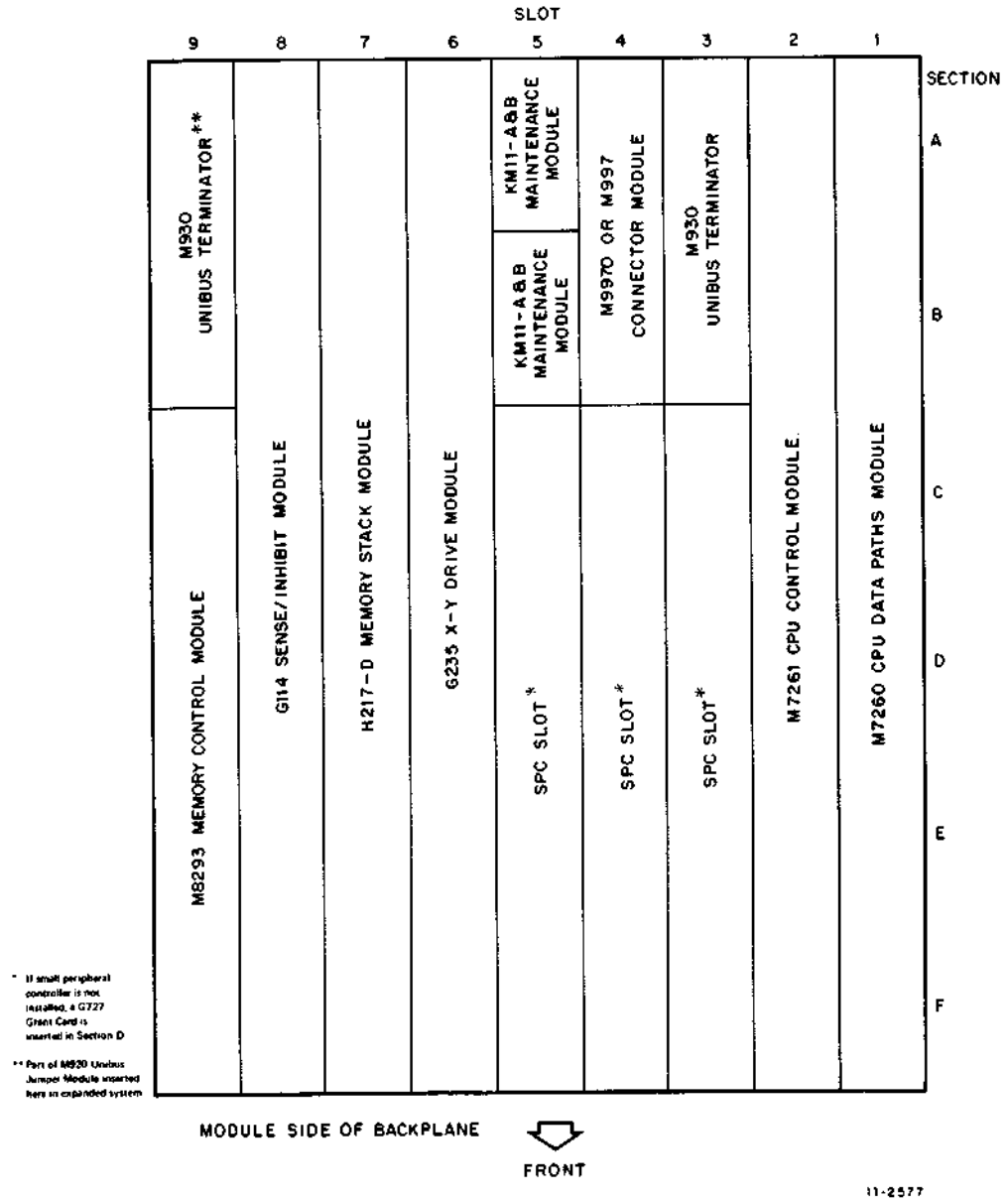


Figure 1-2 PDP-11/05/10-S Module Utilization

Figure 1-3 shows the backplane pin layout. The slots are numbered 1 through 9 and the rows are lettered A through F. Each row is pinned to accommodate a single-height, double-sided module edge-connector. The backplane accepts single, double, quad, and hex modules. A backplane pin is identified as follows:

Module contact designations are shown in Figure 1-4.

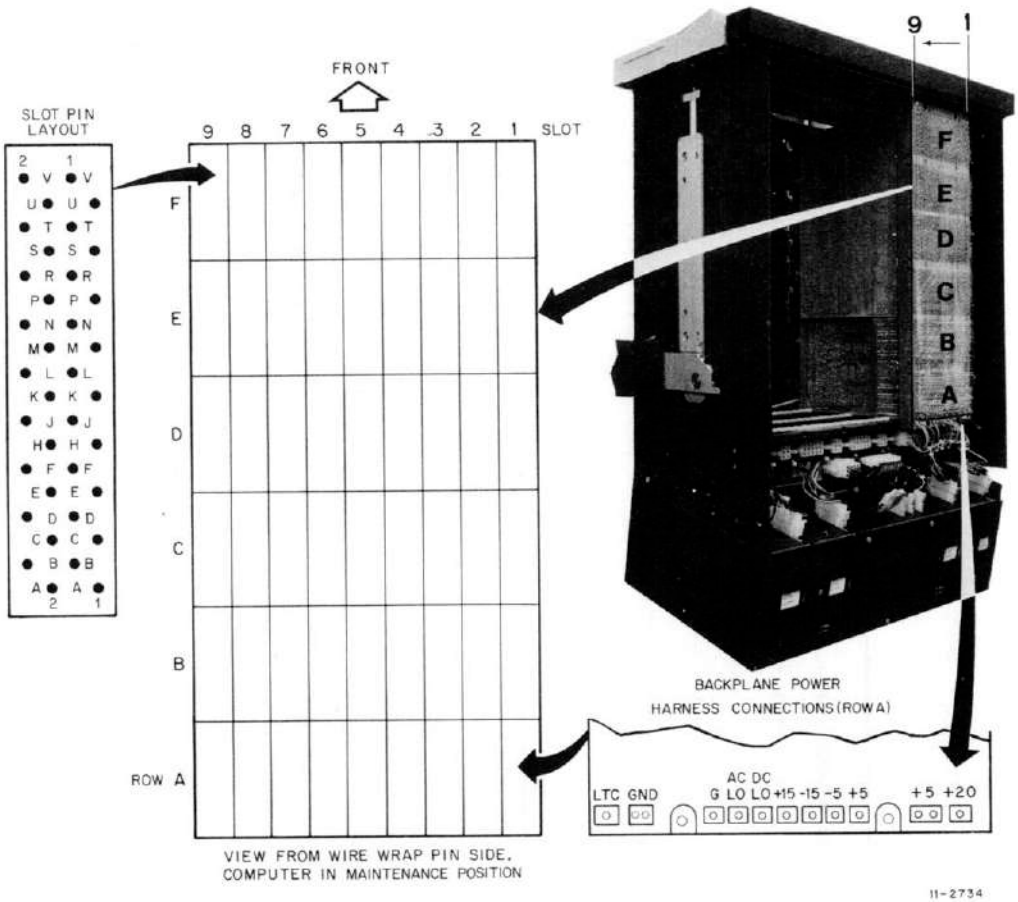


Figure 1-3 Computer Backplane Connector and Pin Designations

1.2.3 KD11-B Processor

The processor comprises the M7260 Data Path Module and the M7261 Control Logic and Microprogram Module. All the processor functional components are contained on these modules. The M7260 Data Path Module contains: data path logic, processor status word logic, auxiliary arithmetic logic unit control, instruction register and decoding logic, and serial communications line (SCL) interface. The M7261 Control Logic and Microprogram Module contains: internal address detecting logic, stack control logic, Unibus control logic, priority arbitration logic, Unibus drivers and receivers, microbranch logic, microprogram counter, control store logic, power fail logic, line clock, and processor clock.

The serial communications line interface is directly connected to the desired serial communications device. It can operate at speeds of 110–2400 baud and is program compatible with the KL11 Teletype Control Interface option.

The line time clock allows the program to measure time by sensing the LTC 50 Hz or 60 Hz ac line frequency signal from the power supply. This clock is program compatible with the KW11-L Line Time Clock option.

The line time clock and the serial communications line interface are not connected to the Unibus; they use an internal bus and can be addressed *only* by the processor and the console.

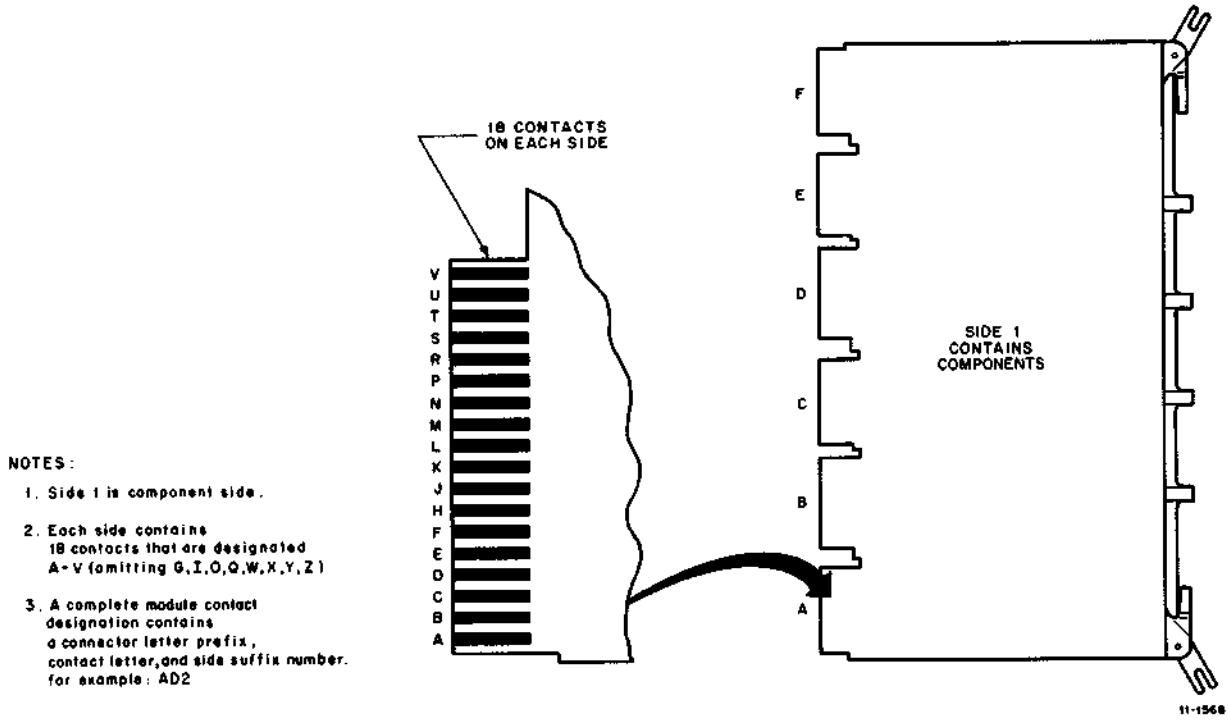


Figure 1-4 Module Contact Designations

The KD11-B Processor decodes instructions; accepts, modifies and outputs data; performs arithmetic and logic operations; and controls allocation of the Unibus among external devices. The processor contains sixteen hardware registers, eight of which are programmable. Two of the eight programmable registers are specifically used for processor operation: a Program Counter (PC) and Stack Pointer (SP); while the remaining six serve as arithmetic accumulators, index register, and auto increment and auto decrement registers.

Four of the eight non-programmable registers are used for storage of a variety of functions including: source and destination data, the last interrupt vector address and load address storage. The remaining four are not used.

Because of the flexibility of hardware registers, address modes, instruction set, and DMA, PDP-11/05/10-S programs may be written in directly relocatable codes. The processor also includes a full complement of instructions that manipulate byte operands, including provisions for byte swapping.

Seven of the eight internal programmable registers (R0–R6) can be used to build last-in, first-out stacks. One register (R6) serves as a processor (or machine) Stack Pointer for automatic stacking. This stack handling capability permits save and restore of the Program Counter and Processor Status word in conjunction with subroutine calls and interrupts. This feature allows true re-entrant codes and automatic nesting of subroutines.

The Unibus is used by the processor and all peripheral devices; therefore there must be a priority structure to determine which device becomes bus master. A device generally requests use of the bus for one of two reasons: to make a nonprocessor transfer of data directly to or from memory, or to interrupt program execution and force the processor to branch to an interrupt service routine. An NPR is granted by the processor at the end of bus cycles and allows device-to-device data transfers without processor intervention. A BR is granted by the processor at the end of an instruction and allows the device to interrupt the current processor task.

The processor recognizes four levels of hardware BRs, with each major level containing sublevels. Many devices can be attached on each major level with the device that is electrically closest to the processor given priority over other devices on the same priority level. The priority level of the processor itself is programmable within the hardware levels; therefore, a running program can select the priority level of permissible interrupts.

Additional speed and power are added to the interrupt structure through the use of a fully vectored interrupt scheme. With vectored interrupts the device identifies itself and a unique interrupt service routine is automatically selected by the processor. This eliminates device polling and permits nesting of device service routines. The device interrupt priority and service routine priority are independent to allow dynamic adjustment of system behavior in response to real-time conditions.

Because of the 16-bit word length of the PDP-11/05/10-S, 32K words of address space can be referenced. Of these 32K words, the uppermost 4K words are reserved to reference I/O device registers and certain hardware registers within the processor. The remaining 28K words of address space are used to reference core memory. Although the word length of the 11/05/10 is 16 bits, the Unibus addresses generated by the KD11-B Processor contain 18-bits. All address references to the uppermost 4K words of 16-bit address space (160000–177777) are converted to full 18-bit references with bits 16 and 17 always set to 1. Thus, a 16-bit reference to address 173224_8 is automatically converted to a full 18-bit I/O device register address of 773224_8. This allows all I/O device registers to maintain addresses in the range 760000 to 777777 in all PDP-11 systems and provides software compatibility among the computers in the PDP-11 line.

More detailed information is provided in the *KD11-B Processor Maintenance Manual.*

1.2.4 KY11-J Programmer's Console

The KY11-J Programmer's Console provides the programmer with a direct system interface and allows the user to start, stop, load, modify, examine, step, or continue a program. Console displays indicate processor operation and the contents of register and memory addresses. The console is mounted as the front panel of the BA11-K mounting box and is connected to the processor by a cable.

A detailed description of the programmer's console operating controls and indicators can be found in Chapter 3. The theory of operation of the console and its interaction with the KD11-B Processor is described in the *KD11-B Processor Maintenance Manual.*

1.2.5 MM11-U Core Memory System

Standard with the PDP-11/05/10-S is the MM11-U Core Memory. The MM11-U Core Memory is a read/write, random access, coincident current, magnetic core type memory with a cycle time of 1000 ns and a Unibus access time of 425 ns. The memory is organized in a 3D, 3-wire planar configuration providing 16,384 (16K) 16-bit words that are both word and byte addressable. Each 16-bit word contains two 8-bit bytes identified as the high-order byte (bits 15:08) and the low-order byte (bits 07:00). Each byte is addressable and has its own address location. Low bytes are always even numbered and high bytes are odd numbered. Full words are addressed at even-numbered locations only. When a full word is addressed, the high byte is automatically included. For example, the 16K memory has 16,384 words, or 32,768 bytes; therefore, 32,768 locations are assigned (addresses 000000 to 077777). Address 000000 is the first low byte, address 000001 is the first high byte, 000002 is the second low byte, 000003 is the second high byte, etc.

The MM11-U consists of four modules:

M8293 Memory Control Module – This quad-height module interfaces with the control and address lines of the Unibus and contains memory address latches, device selection, and read/write inhibit logic.

G114 Sense Inhibit Module – This hex-height module interfaces with the data lines of the Unibus and contains a data register, timing buffers, inhibit drivers, sense amplifiers, and threshold circuit.

G235 X/Y Driver – This hex-height module contains address decoders and X and Y drivers and switches.

H217D Stack Module – This hex-height module contains the ferrite core array and X-Y diode matrices. The ferrite core array consists of 16 mats, each containing 16,384 ferrite cores in a 128 by 128 planar array. Each mat represents a single bit position of a word. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals.

More detailed information on the MM11-U Core Memory may be found in the *MM11-U/UP Core Memory System Maintenance Manual* (DEC-11-HMFMA-B-D).

1.2.6 Unibus

The Unibus provides high-speed communication between system components. The Unibus, with bidirectional data, address, and control lines, allows data transfers between all units on the bus with control of the bus an important factor in these transfers. The fixed repertoire of bus operations is flexible enough for speed and design economy, yet provides a fixed specification for interfaces. The asynchronous nature of these operations also eases design and operation. The repertoire of bus operations is:

Data Operations – DATa In (DATI), DATa In Pause (DATIP), DATa Out (DATO), DATa Out Byte (DATOB)

Control Operations – Bus Request (BR), INTerRupt (INTR), Non-Processor Request (NPR)

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between the master and slave. The DATI, DATIP operations transfer data into the master; the DATO, DATOB operations transfer data out of the master. When a device is capable of becoming bus master and requests use of the bus, it is for one of two purposes: to make a Direct Memory Access (DMA) transfer of data directly to, or from, another device or memory without processor intervention; or to INTeRrupt (INTR) program execution and force the processor to branch to a specific address where an interrupt service routine is located.

Bus control is obtained under a Non-Processor Request (NPR) for the DMA, or under a Bus Request (BR) for an INTR. A device can perform a DMA after acquiring bus control via a BR.

Requests for the bus can be made at any time on the BR and NPR lines. Transfer of bus control from one device to another is made by the processor priority arbitration logic, which grants control of the bus to the device having the highest priority. NPR's are accorded higher priority than BR's. The NPR's are serviced before and immediately after Unibus data cycles, in addition to specific times during WAIT or TRAP sequences. The BR's are serviced upon completion of the current instruction if the requesting priority exceeds that of the processor.

The PDP-11/05/10-S processor has a special role in bus control operations as it performs the priority arbitration to select the next bus master.

The Unibus is terminated at both ends with a M930 Unibus Terminator module. To carry the Unibus from one system unit to an adjacent one, M920 Unibus Jumper modules are utilized; all 56 Unibus signals plus 17 grounds are carried by this one module. To connect system units in different mounting boxes, or to connect a peripheral device removed from the mounting box, a 120-conductor Flexprint cable is used.

A complete description of the Unibus, including specifications, is presented in the *PDP-11 Peripherals Handbook.*

1.3 REFERENCE DOCUMENTS

Table 1-1 lists the maintenance manuals and engineering drawings for the various components supplied as part of the basic PDP-11/05/10-S system and several reference manuals which provide essential information pertaining to all PDP-11 systems. Documentation for specific peripherals and options are *not* listed in the table. When peripherals and options are included in the PDP-11 system, the appropriate manuals are supplied with the system.

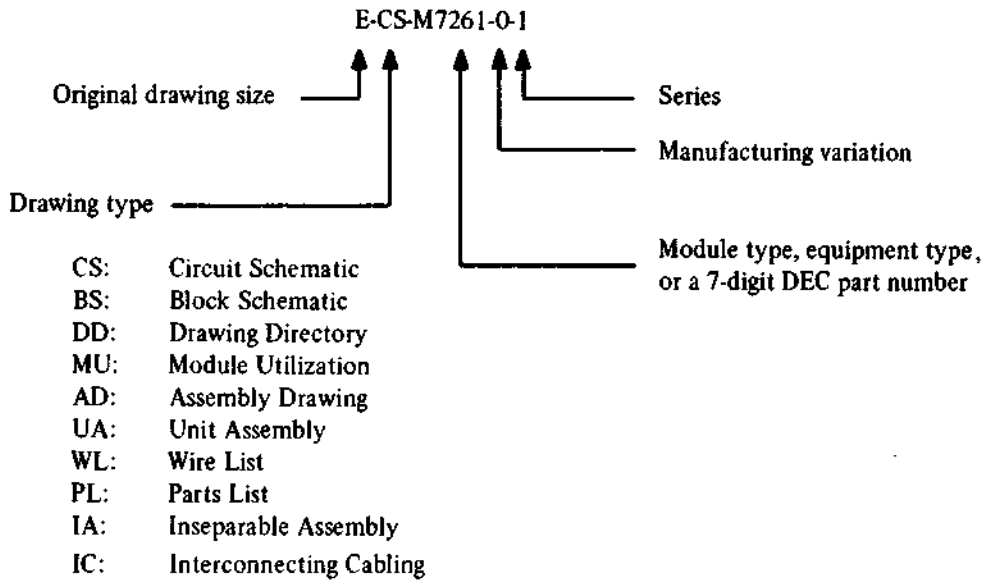
Table 1-1
Reference Manuals

Title	Document Number
PDP-11/05-S, 11/10-S Engineering Drawings	–
KD11-B Processor Maintenance Manual	DEC-11-HKDBB-A-D
MF11-U/UP Core Memory System Maintenance Manual	DEC-11-HMFMA-B-D
BA11-K Mounting Box Maintenance Manual	DEC-11-HBKEF-A-D
PDP-11/05/10/35/40 Processor Handbook	–
PDP-11 Peripherals Handbook	–

1.4 REFERENCE DRAWINGS

PDP-11/05/10-S systems are shipped with a set of engineering drawings for the basic components and applicable options. A list of the drawings is included in the Drawing Directory prints within each set.

DEC drawing numbers are interpreted as indicated in the following example:



CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides information on PDP-11/05/10-S environmental and electrical requirements, equipment installation, and customer acceptance. The installation procedures contained in this chapter include installation of a basic PDP-11/05/10-S computer and a sample installation of an SCL interface compatible device – an LA36 DECwriter.

Installation procedures for the various available peripherals are provided in the maintenance manuals supplied with the peripherals.

2.2 ENVIRONMENTAL REQUIREMENTS

An ideal computer room type environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be higher than that of adjacent areas to prevent dust infiltration.

2.2.1 Humidity and Temperature

The PDP-11/05/10-S electronics are designed to operate in a temperature range from 41° F (5° C) to 122° F (50° C) at a relative humidity of 10 to 95 percent, without condensation. However, system configurations that use I/O devices, such as magnetic tape units, card readers, etc., require an operational temperature range of from 60° F (15° C) to 80° F (27° C) with 40 to 60 percent relative humidity. Nominal operating conditions for a system configuration are a temperature of 70° F (20° C) and a relative humidity of 45 percent.

2.2.2 Air Conditioning

When used, computer room air conditioning equipment should conform to the requirements of the "Standard for the Installation of Air Conditioning and Ventilating Systems (Non-residential)," N.F.P.A. No. 90A; as well as the requirements of the "Standard for Electronic Computer Systems," N.F.P.A. No. 75.

2.2.3 Special Mounting Conditions

If the PDP-11/05/10-S is to be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard a ship), the cabinet in which the PDP-11/05/10-S is housed should be securely anchored to the installation floor by mounting bolts. Since such installations require modifications to system cabinets, Digital must be notified upon placement of the order so that necessary modifications can be made.

2.2.4 Static Electricity

Static electricity can be an annoyance to personnel and can, in extreme cases, affect the operational characteristics of the PDP-11/05/10-S Computer and related peripherals. If carpeting is installed on the installation room floor, it should be of a type designed to minimize static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

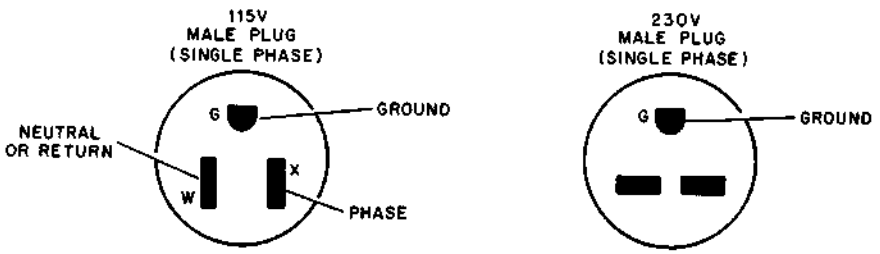
2.3 ELECTRICAL REQUIREMENTS

The PDP-11/05/10-S can be operated from a nominal 115 V, 50/60 Hz or 230 V, 50/60 Hz ac power source, depending on the type of ac input box installed in the mounting box power supply. The primary ac operational voltages should be maintained within the defined tolerances. Line voltage should be maintained within 90 Vac – 132 Vac or 180 Vac – 264 Vac, and the 50/60 Hz line frequency should not vary more than 3 Hz. The minimal configuration of the PDP-11/05/10-S computer (processor plus 16K of memory) requires approximately 575 VA of input power (5 A @ 115 Vac, 2.5 A @ 230 Vac).

Primary power outlets at the installation site must be compatible with the PDP-11/05/10-S primary power input connectors, or, if a 861 Power Controller is used, with the primary power input connectors of the power controller. The power receptacles must be provided by the customer.

The PDP-11/05/10-S uses only two types of connectors, depending on whether it is configured for 115 Vac or 230 Vac operation. The NEMA L5-15 connector is used for 115 Vac primary power; the L6-15 is used for 230 Vac primary power. Figure 2-1 shows the plug portion of each connector, indicates which equipment version uses it, and provides connector specifications.

The 861 Power Controller, if used, requires power receptacles different from the PDP-11/05/10-S. The 861-C Power Controller, used for 115 Vac operation requires a NEMA L5-30 connector. The 861-B Power Controller, used for 230 Vac operation, requires a NEMA L6-20 connector. Figure 2-2 illustrates these connectors while Table 2-1 provides connector specifications.



CONNECTOR SPECIFICATIONS

MODEL NUMBER	NEMA* CONFIGURATION	DESCRIPTION	POLES	WIRES	PLUG		RECEPTACLE	
					DEC PART NO.	HUBBEL	DEC PART NO.	HUBBEL
PDP-11/05/10-SC	L5-15	115V, 15AMP	2	3	90-08938	5266-C	12-05351	5262
PDP-11/05/10-SD	L6-15	230V, 15 AMP	2	3	90-08853	5665-C	12-11204	5662

*ADD P SUFFIX FOR PLUG
ADD R SUFFIX FOR RECEPTACLE

11-2568

Figure 2-1 PDP-11/05/10-S Connectors

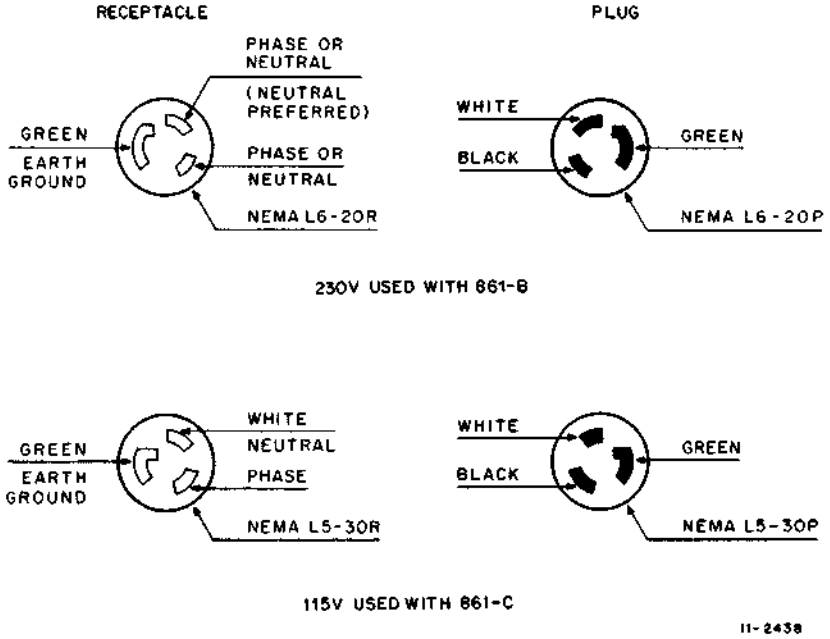


Figure 2-2 861-B, C Power Controller Connectors

Table 2-1
861-B, C Power Controller Primary Power Receptacles

Model Number	Power	Rating	Plug NEMA CODE	Receptacle (Supplied by Customer) NEMA CODE	DEC Part No.
861-C	115 V Single Phase	30 A	L5-30P	L5-30R	12-11191
861-B	230 V Single Phase	20 A	L6-20P	L6-20R	12-11194

The PDP-11/05/10-S three-prong power connector, when inserted into a properly wired receptacle, should ground the computer chassis. It is unsafe to operate the computer unless the case is grounded because normal current leakage from the power supply flows to the metal parts of the chassis. If the integrity of the ground circuit is questionable, the user is advised to measure the potential between the computer case and a known ground with a voltmeter.

Computer systems are often sensitive to the interference present on some ac power lines. If the computer is to be installed in an electrically noisy environment, it may be necessary to condition the ac power line. Primary power to the computer should be provided on a line separate from lighting, air conditioning, etc., so that computer operation is not affected by voltage surges of fluctuations.

Any questions regarding power requirements and installation wiring should be directed to the Digital Sales engineer or Field Service engineer.

2.4 INSTALLATION PROCEDURES

The procedures presented in the following paragraphs are provided to assist in unpacking, inspecting, and installing the PDP-11/05/10-S Computer and associated SCL device.

CAUTION

Do not attempt to install the computer until Digital has been notified and a Digital Field Service representative is present.

2.4.1 Unpacking

The PDP-11/05/10-S is shipped ready to operate in a protective box. Prior to final electrical testing, each computer is thermal cycled and vibrated.

Basic computers are shipped in the package illustrated in Figure 2-3. Sufficient hardware is included in the shipping carton to rack mount the computer.

The PDP-11/05/10-S should be removed carefully from its box. Slide mounts are attached to the computer and mounting screws are packed in a bag in the same shipping carton. Also included is one Serial Communication Line (SCL) cable and two keys to the console power switch lock.

2.4.2 Inspection

After removing the computer from its carton, inspect it and report any damage to the local Digital Sales Office. Inspect as follows:

1. Inspect the box, bezel, switches, and indicators for damage.

2. Remove the top cover and inspect for loose or broken modules, blower or fan damage, cable damage, and loose nuts, bolts, screws, etc.

3. Remove the bottom cover and inspect wiring side of the logic panels for bent pins, broken wires, loose external components, and foreign material.

4. Inspect the power supply for proper seating of power connectors.

2.4.3 Cabinet and Slide Mounting Specifications

The PDP-11/05/10-S and a BA11-K can be mounted in an H950 cabinet. When using an H950 cabinet, the standard configuration is to place the PDP-11/05/10-S in location 3 and the BA11-K in location 2 (shown in Figure 2-4). The hole numbers shown on Figure 2-4 indicate the exact physical location for mounting an Accuride or Chassis-Trak slide on the front rail. Although the front rail slide placement is identical for both slides, there are some mounting differences when fastening the slides to a chassis. Figures 2-5 and 2-6 illustrate the specific slide mounting specifications for Accuride and Chassis-Trak, respectively.

Cabinet Power Control Option – Provisions have been made for the computer switch to operate an optional cabinet power control. This feature permits the programmer's console OFF/POWER/PANEL LOCK switch to control the power supply for peripherals connected to the computer. Operation of the programmer's console is explained in Chapter 3. For operating and wiring information on the power control option, refer to the maintenance manual provided with the option.

2.4.4 Installation of LA36 DECwriter as an SCL Device

The LA36 is frequently used to connect to the PDP-11/05/10-S SCL interface. For a complete LA36 installation procedure, refer to the installation chapter of the *LA36 DECwriter Service Manual,* DEC-00-H36MM-A-D.

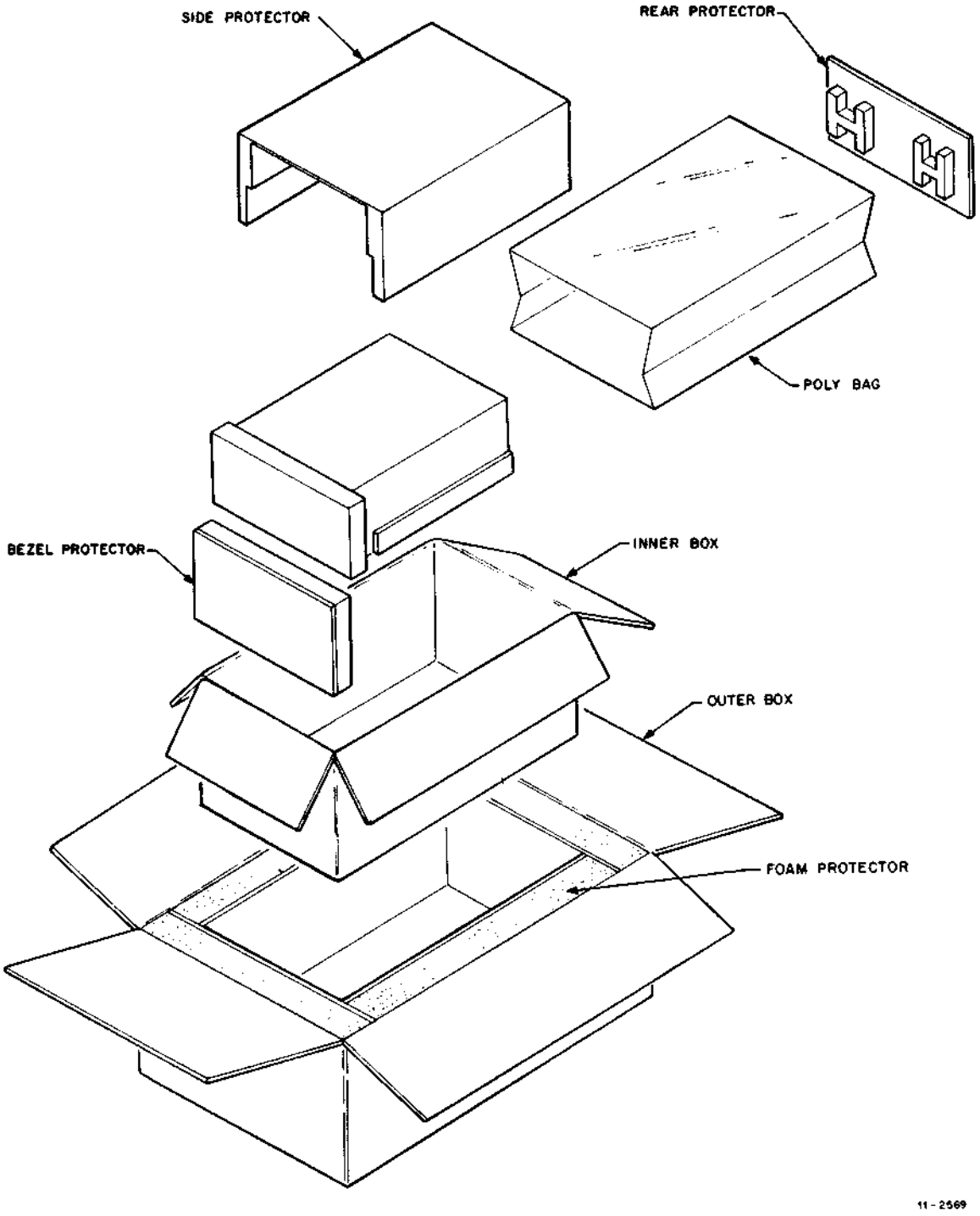


Figure 2-3 Computer Packaging

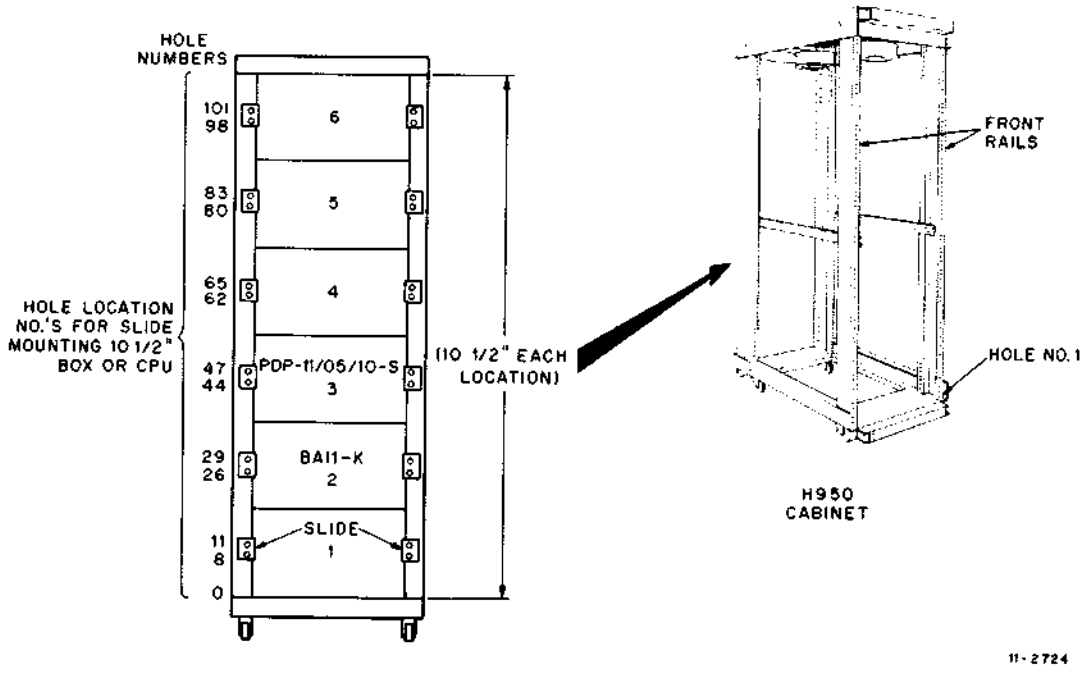


Figure 2-4 PDP-11/05/10-S and BA11-K Mounting Box Cabinet Mounting Specification

To connect the LA36 to the PDP-11/05/10-S SCL interface, route the LA36 serial interface cable to the PDP-11/05/10-S and connect to the Mate-N-Lok connector on the cable (No. 70-08360) hanging from the rear of the PDP-11/05/10-S.

If there is no cable hanging at the rear of the processor mounting box, remove the PDP-11/05/10-S top cover and then remove the M9970 connector module from backplane slots A4-B4. Plug the Berg connector on the 70-08360 SCL cable (supplied) into the Berg connector on the M9970. Insert the M9970 into backplane slots A4-B4. Run the SCL cable through the strain relief clamp of the PDP-11/05/10-S mounting box, and connect to the cable attached to the LA36.

Appendix A contains more detailed information on the SCL cable interconnections.

After initial power turn-on (Paragraph 2.4.5), perform the SCL baud rate adjustment check (Paragraph 7.4.2.3) to ensure that the SCL interface is set to 300 baud, the maximum transfer rate of the LA36 DECwriter.

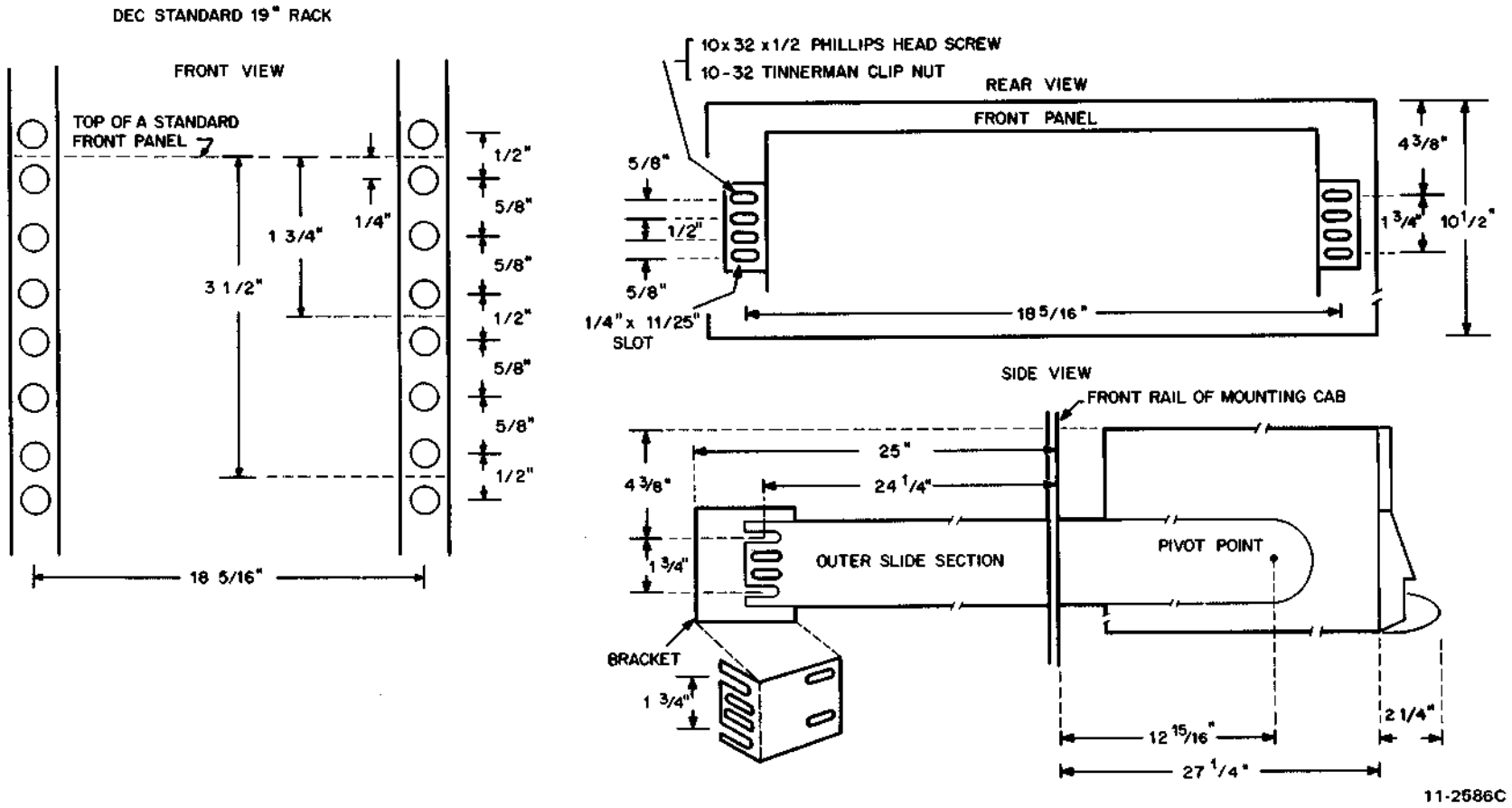


Figure 2-5 Accuride Slide Mounting Specification

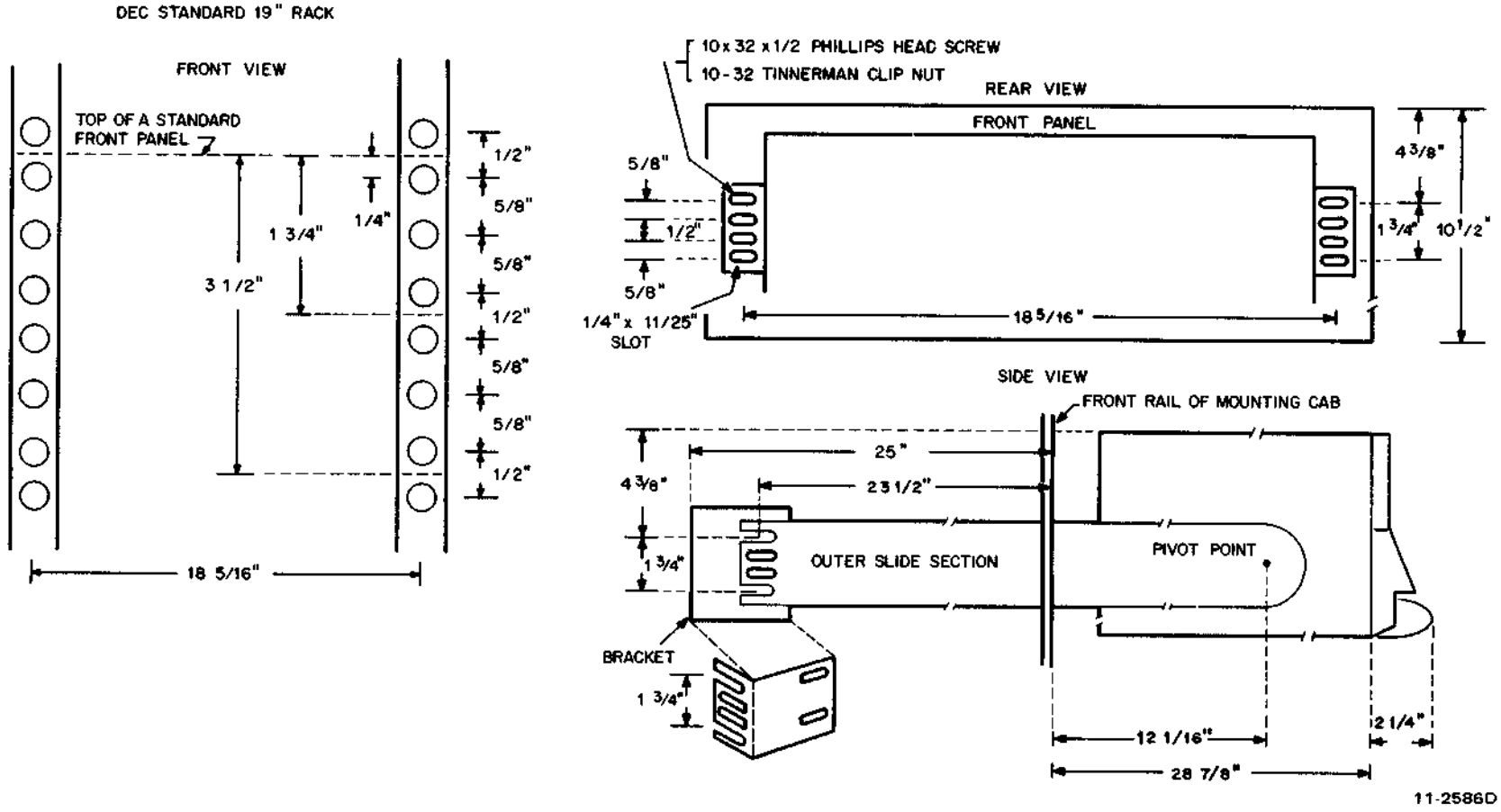


Figure 2-6 Chassis-Trak Slide Mounting Specification

2.4.5 Initial Power Turn-On

Before plugging in the computer ac power cord:

1. Ensure that the proper voltage (115 Vac or 230 Vac) is available at the wall receptacle.
2. Remove the computer mounting box bottom cover and disconnect the backplane power harness(es) from the power supply power distribution board.
3. Plug in the computer ac power cord and set the programmer's console key switch to POWER.
4. Observe that the two mounting box fans operate.
5. Verify that the correct voltages are present at the power distribution board connectors pins, as indicated in Table 2-2.
6. Set the console key switch to OFF, unplug the ac power cord, and reconnect the power harness(es) to the power distribution board.
7. Plug in the ac power cord and verify correct operation of the console OFF/POWER/PANEL LOCK key switch (Paragraph 3.2.1).

Table 2-2
No Load Voltage Verification

Power Distribution Board Connector J11 or J9 Pin Numbers (See Notes)	Voltage (Vdc)
1, 4	+5
2	+15
3	+20
5, 7, 8, 9, 11	GND
13	-15
14	-5

Note: Pins 6, 10, 12 and 15 are spares.

2.5 INSTALLATION CERTIFICATION

Once the computer has been installed, it is strongly recommended that a system diagnostic be run to ensure that the equipment operates correctly and that installation has been properly performed. Because system configurations vary widely, no one diagnostic will completely exercise all the attached devices.

The *MAINDEC User's Manual* that comes with the diagnostic package should be consulted for the appropriate diagnostic to be run, depending upon the attached devices. The *MAINDEC User's Manual* lists the devices that each diagnostic will exercise. The three system exercisers presently available are T17 System Exerciser (MAINDEC-11-DZQKB) for relatively small systems, General Test Program (MAINDEC-11-DZQGA) for medium to large systems, and Communications Test Program (MAINDEC-11-DZQCA) for communications-oriented systems. At least one of the above diagnostics and, if appropriate, the other two, should be used to verify system operation.

Once the diagnostic is selected, the respective diagnostic write-up should be consulted for specific operating instructions. If the user is not familiar with console operation and/or procedures for loading paper tapes, he should read Chapter 3 of this manual.

CHAPTER 3
SYSTEM OPERATION

3.1 SCOPE

This chapter provides the information necessary to operate and program the PDP-11/05/10-S Computer. The description is divided into three major parts: programmer's console, basic system operation, and basic system programming. The description of controls and indicators for the console provides the user with the type and function of each operating switch and indicator. Operating controls for peripheral devices that are *not* part of the basic machine are contained in the appropriate peripheral manual.

Basic step-by-step procedures for both manual and program operation are given in Paragraph 3.5. Basic system programming is covered in Paragraph 3.6.

3.2 KY11-J PROGRAMMER'S CONSOLE

The KY11-J Programmer's Console (Figure 3-1) provides the PDP-11/05/10-S Computer with a necessary and useful programmer's interface. Manual operation of the computer is controlled by switches mounted on this console which is the front panel of the computer mounting box. Visual displays indicate processor operation and the contents of register and memory addresses.

All register switches and displays are ordered from right to left. The order corresponds to the exponential powers of two, i.e., $2^{15}....2^{2}$, 2^{1}, 2^{0}. Therefore, the most significant bit (MSB) is at the left of each specific register or display, the least significant bit (LSB) is at the right. Whenever an indicator is on, it denotes the presence of a binary 1 in the particular bit position. The alternate color coding on the console identifies the different functions or segments of the binary word in octal format. Figure 3-1 shows the location of all PDP-11/05/10-S console controls and indicators.

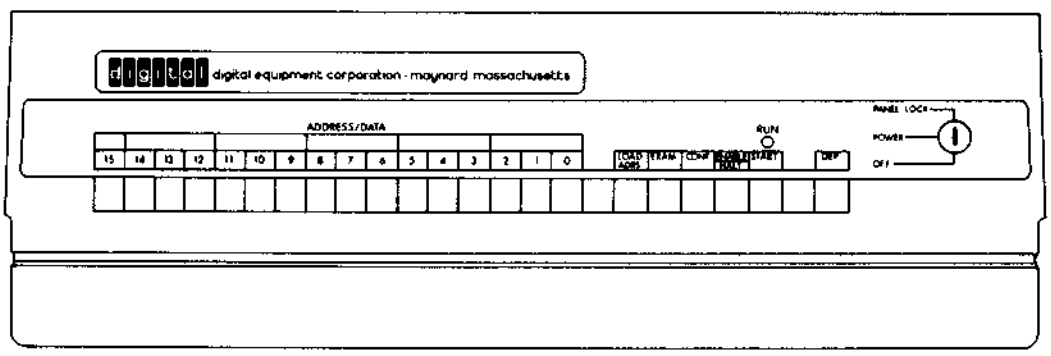


Figure 3-1 PDP-11/05/10-S Programmer's Console

3.2.1 Console Power Key Switch

The console power key switch has three positions:

1.	OFF	Fully counterclockwise
2.	POWER	90° clockwise from OFF
3.	PANEL LOCK	180° clockwise from OFF

In the OFF position, ac power is removed from the primary of the computer power supply. In the POWER position, ac power is applied to the computer power supply; the computer is fully operative. In the PANEL LOCK position, the computer is fully powered as in the POWER position. However, the console function switches (Paragraph 3.2.2) are disabled, thus protecting the computer against mischievous tampering during unattended program execution.

3.2.2 Function Switches

Listed below in the order of their position (left to right) are the six switches on the right hand side of the console – the function switches:

1. LOAD ADRS (load address)
2. EXAM (examine)
3. CONT (continue)
4. ENABLE/HALT
5. START
6. DEP (deposit)

Function switches 1, 2, 3 and 5 (above) are spring loaded and return to their rest state when released; they are actuated by being depressed. The DEP switch is also spring loaded, but is actuated by being lifted. The ENABLE/HALT switch is a two position switch. Operation of the function switches is described in Paragraph 3.3.

3.2.3 ADDRESS/DATA Switches

The 16 ADDRESS/DATA switches are to the left of the function switches (Figure 3-1). These 2-position switches represent a manually set flip-flop register with the up position representing a logical 1 and the down position a logical 0. The ADDRESS/DATA switches may be used in conjunction with the function switches or in conjunction with a program stored in the computer's memory. The ADDRESS/DATA switches are often referred to as the Switch register in DEC documentation.

3.2.4 Console Indicators

There are seventeen indicators on the computer console: a RUN light and 16 ADDRESS/DATA lights. The RUN light, when lit, indicates that a program is being executed. The contents of the 16 ADDRESS/DATA lights either represent a 16-bit address, or the contents of a register or memory address. Table 3-1 indicates the meaning of the ADDRESS/DATA lights for all cases where the contents of these lights is defined. Note that the state of the ADDRESS/DATA lights is defined *only* when the computer RUN light is not illuminated.

3.3 CONSOLE OPERATION

The following paragraphs describe the operation of the function switches.

Table 3-1
Significance of ADDRESS/DATA Indicators

Action	Qualification	Information Displayed In ADDRESS/DATA Indicators
Power On	1. ENABLE/HALT switch in HALT position	1. Contents of location $(24)_8$
	2. ENABLE/HALT switch in ENABLE position	2. Undefined – depends on contents of memory
Load Address	LOAD ADRS switch depressed	Contents of Switch Register
Examine	1. EXAM switch depressed	1. Unibus address that is to be examined
	2. EXAM switch released	2. Contents of Unibus address that was examined
Deposit	1. DEP switch raised	1. Unibus address that is to be deposited
	2. DEP switch released	2. Contents of Switch Register which is the data deposited
RUN Light On		Undefined
Program Halt	1. ENABLE/HALT switch in HALT position	1. Address of instruction to be executed when CONT switch is actuated
	2. HALT instruction executed	2. Same as 1
	3. Double bus error which is two successive attempts to access non-existent memory or improper odd byte address.	3. Contents of program counter (R7) at time double bus error occurred
Program Execution	1. START switch depressed	1. Address of last load address
	2. CONT switch depressed	2. Address of instruction to be executed

3.3.1 Load Address Switch

Depressing the LOAD ADRS switch when the computer is halted causes the contents of the Switch Register to be stored in a temporary register within the computer. This data is also displayed in the ADDRESS/DATA lights for verification. The load address operation performs the following functions:

- Selects an address for a subsequent examine operation.
- Selects an address for a subsequent deposit operation.
- Selects the starting address of a program.

3.3.2 Examine Switch

The EXAM switch permits the display of the contents of a selected address in the ADDRESS/DATA lights. Select the appropriate address in the Switch Register and depress the LOAD ADRS switch. Then depress and release the EXAM switch. The contents of the selected address will then be displayed in the ADDRESS/DATA lights.

Several features are built into the examine function to aid in programming the computer:

- While the EXAM switch is depressed, the address to be examined is displayed. The data itself is displayed when the switch is released.

- If the EXAM switch is repeatedly depressed, the Unibus address is incremented by two on each depression*. This permits the examination of a list of addresses without repeated load address operations.

- If an attempt is made to examine non-existent memory, it is necessary to perform the initialize operation explained in Paragraph 3.4.

- Only full words are displayed in the ADDRESS/DATA lights; thus, bit 0, the byte address bit, is ignored when using the EXAM switch with the following exception. Note that the general registers are located on byte addresses. Therefore, when examining the general registers, address bit 0 is recognized and the increment feature is modified so that sequential registers may be examined by repeated use of the EXAM switch.

The EXAM switch has no effect while the computer is in the RUN state or when the key operated power switch is in the PANEL LOCK position.

3.3.3 Deposit Switch

The physical operation of the DEP switch requires that it be lifted for actuation. The DEP switch permits the contents of the Switch Register to be deposited in a Unibus address, which is typically specified by a previous load address operation. To deposit the instruction BRANCH SELF (777_8) in location 200_8, first set the Switch Register to 200_8, and then actuate the LOAD ADRS switch. Set the Switch Register to 777_8 then lift and release the DEP switch.

Several additional features are built into the deposit function:

- While the DEP switch is actuated, the address to be effected is displayed in the ADDRESS/DATA lights. When the switch is released, the data deposited is displayed for verification.

- If the DEP switch is repeatedly depressed, the address is incremented by two on each depression**. This permits depositing an entire program with only one load address operation.

*The address is incremented by one when examining general registers.

**The address is incremented by one when depositing into general registers.

- If an attempt is made to deposit into non-existent memory, it is necessary to perform the initialize operation explained in Paragraph 3.4.

- All deposit operations affect full 16-bit words. Bit 0 of the address is used only when depositing into general registers; otherwise, bit 0 of the address is ignored.

3.3.4 ENABLE/HALT Switch

Place the ENABLE/HALT switch in the HALT position; the computer will halt at the end of the current instruction providing the key switch is not in the PANEL LOCK position. All interrupts and traps will be executed prior to halting. This switch may be used in conjunction with the CONT switch to step through programs (Paragraph 3.3.6). With the ENABLE/HALT switch in the ENABLE position, programs may be executed, once started by actuating the START switch, actuating the CONT switch, and the auto-restart power-up sequence.

3.3.5 START Switch

To start a program from the console:

1. Set the starting address of the program in the Switch Register.
2. Depress the LOAD ADRS switch.
3. Position the ENABLE/HALT switch in the ENABLE position.
4. Depress and release the START switch.

While the START switch is depressed, the following actions occur:

1. An initialize signal is generated on the Unibus. This initialize signal serves to reset all peripherals.
2. The processor status word is reset to zero.
3. The program counter, R7, is loaded with the last address loaded with the LOAD ADRS switch.

When the START switch is released, program execution begins with the instruction contained in the location specified by R7 and the RUN light is turned on. If the ENABLE/HALT switch is in the HALT position, the computer remains in the HALT state following the release of the START switch.

Observe the following precautions when using the START switch:

1. If the key lock is not in the PANEL LOCK position, depressing the START switch while a program is running initializes the computer system and restarts the program.

2. It is good practice to precede every program start with a load address operation.

3. A program should not be started at an odd address or the first fetch operation will be aborted and an odd address trap will be attempted. If the stack pointer, R6, is not properly set up, the program in memory may be destroyed.

3.3.6 Continue Switch

The CONT switch is used to continue a program without altering the program counter, R7, or the machine state. To continue a halted program, depress and release the CONT switch. The program is resumed when the CONT switch is released.

The CONT switch is used with the ENABLE/HALT switch to step through programs one instruction at a time. If the CONT switch is actuated while the ENABLE/HALT switch is in the HALT position, a single instruction will be executed. Interrupts are serviced in single instruction mode. In single step mode, the address of the next instruction to be executed is displayed in the lights.

3.4 UNCONDITIONAL COMPUTER AND UNIBUS INITIALIZATION

Unconditional initialization of the computer system usually occurs because of an attempt to examine from, or deposit into, non-existent memory from the console. However, a peripheral or processor error may occur that can only be overcome by initializing the system from the console. The procedure is simply to depress the START switch with the ENABLE/HALT switch in the HALT position.

3.5 BASIC OPERATION

Many methods exist for storing, modifying, and retrieving information from the PDP-11/05/10-S Computer. These methods depend on the form of the information, time limitations, and the peripheral equipment connected to the processor. The following procedures are basic to the use of the PDP-11/05/10-S Computer. Although they may be used less frequently as the programming and use of the system become more sophisticated, they are valuable in preparing the initial programs and in learning the function of system input and output transfers. For an understanding of the various operational controls and indicators, refer to Paragraph 3.3.

Operating procedures are separated into the following categories:

Power on	Paragraph 3.5.1
Basic console control	Paragraph 3.5.2
Manual program loading	Paragraph 3.5.3
Automatic program loading	Paragraph 3.5.4
Memory Dumps	Paragraph 3.5.5
Running programs	Paragraph 3.5.6

3.5.1 Power On

When the programmer's console OFF/POWER/LOCK switch is turned from OFF to POWER, the system is initialized (zeroed). A time delay allows sufficient time for voltages to logic units (especially memory elements) to stabilize.

The power-up initialization logic directly sets the microprogram control to a sequence of controlled events. If the console ENABLE/HALT switch is set to HALT when power is turned on, the processor microflow is directly set to the console microloop. The machine awaits the activation of a console control switch.

The LOCK position of the programmer's console OFF/POWER/LOCK switch provides for program operation with the console control switches disabled. However, the console Switch register may still be accessed.

3.5.2 Basic Console Control

Two major areas of control exist: control influenced by the ENABLE/HALT switch, which selects either program or console control; and control by the switches and sequences used for loading data manually into the processor.

3.5.2.1 **ENABLE/HALT Switch** – When the processor has control (ENABLE/HALT in ENABLE), either the START or CONT switch causes the program to run. The START switch initializes the system and begins operation at a specific address determined by the last console operation (usually LOAD ADRS). The CONT switch merely releases console control, and the program continues at the existing Program Counter (PC).

When the ENABLE/HALT switch is set to HALT, the console obtains control. The LOAD ADRS, EXAM, and DEP switches can be used. The CONT switch can now cause the processor to step through the program a single instruction at a time.

3.5.2.2 **Loading Data Manually** – Whenever data is manually loaded into a computer, it is desirable to have the address increment automatically upon each deposit. Thus, the user can set a starting address and continue to store data in sequential memory locations providing only new data for each location. The programmer's console logic also permits the user to immediately examine the data just deposited without re-addressing, to re-deposit if necessary,

and to continue with automatic incrementation. These sequences are associated with the functioning of the DEP and EXAM switches.

The address in the load address register does not increment the *first* time EXAM or DEP is used after a HALT or LOAD ADRS. It does not increment if DEP is used immediately after EXAM or if EXAM is used immediately after DEP. It does increment if a DEP is used immediately after a DEP, or if an EXAM is used immediately after an EXAM. This increment is a word increment as the console is word oriented. Thus, the user can look at a location, change it, deposit the changed data, and then reexamine it without having to load an address each time.

Incrementation is on even boundaries for all addresses except the addresses specifically designated for the processor internal registers, which are incremented by 1.

For example, to alter several successive locations, the following steps are performed:

1. LOAD ADRS (starting location)
2. EXAM (no increment – looks at starting location)
3. DEP (no increment – loads starting location)
4. EXAM (no increment – checks previous deposit)
5. EXAM (increment – looks at next location)
6. DEP (no increment – loads second location)
7. EXAM (no increment – checks previous deposit)
8. EXAM (increment – looks at third location)

If the user wants to take advantage of automatic address incrementation for examining or loading data, the following steps can be used to load data into sequential locations:

1. LOAD ADRS (starting location)
2. DEP (no increment – loads starting location)
3. DEP (increment – loads second location)
4. DEP (increment – loads third location)
5. DEP (increment – loads fourth location)
   etc.

The same procedure can be used for examining data in sequential memory locations.

3.5.3 Manual Program Loading (Bootstrap Loader)

A primary manual use of the programmer's console is to store the bootstrap loader in the core memory. (Programs and data can be stored or modified by manual use of the programmer's console.) The bootstrap loader (DEC-11-L1PA-LA) is a minimal instruction program that can automatically load programs into core memory from a paper tape punched in a special bootstrap format. One of these programs, after being stored, can in turn, load any binary format tape into the computer. (An explanation of the number designations used for DEC programs is given in Table 3-2.)

The sequence for loading the computer is shown in Figure 3-2, with programs noted as follows:

Bootstrap loader (DEC-11-L1PA-LA) – manually loaded by console switches; provides for automatic loading of programs punched in a special format.

Absolute loader – punched in special format; loaded by bootstrap loader; provides for automatic loading of programs punched in binary format.

Selected program – punched in binary format; loaded automatically by absolute loader.

Table 3-2
Program Identification Codes

	COMPUTER PRODUCT / IDENTIFICATION / DISTRIBUTION	
Format:	DEC-11-L1PA-LA	
Notes:	1 2 3 4 5 6 7 8	
1	Product Code	MAINDEC = maintenance library products DEC = programming library products
2	Computer Series	11 = PDP-11 Computer Systems
3	Major Category	L = Loader
4	Minor Category (sequential numbers)	1 = first in a series of programs 2 = second in series, etc.
5	Option Category (hardware required to use software)	P = paper tape system H = high-speed reader and/or punch K = Teletype keyboard only M = magtape
6	Revision Category (sequential letters)	A = basic program B = first revision C = second revision, etc.
7	Distribution Method	L = listing P = paper tape
8	Distribution Mode	A = ASCII B = binary (absolute) O = other (bootstrap binary)
Example:	DEC-11-L2PB-PO	Indicates a PDP-11 programming library product, second in a series of loaders, requiring a paper tape system to use, the first revision to the program, supplied as a paper tape in bootstrap binary format.

To eliminate the necessity of more than one bootstrap loader, the bootstrap loader instructions contain two variables (x and y) to provide compatibility with various memory configurations and reading devices. These variables are listed in Table 3-3. A complete explanation of the bootstrap loader program is given in the *Paper Tape Software Programming Handbook* (DEC-11-XPTSA-A-D); further information may be found in the program listing, DEC-11-L1PA-LA.

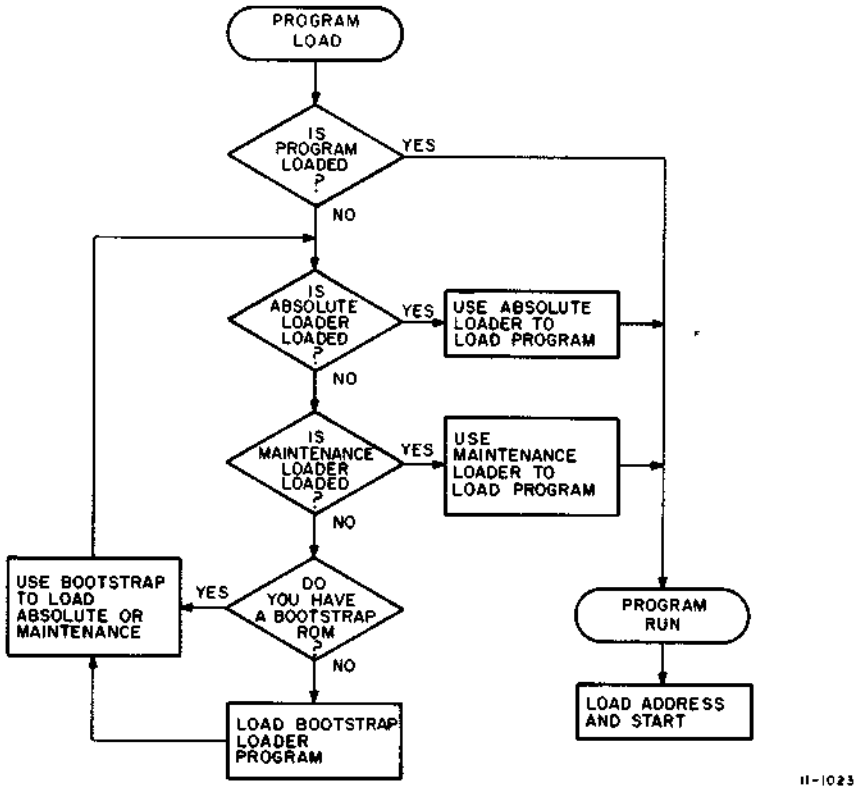


Figure 3-2 Flowchart of Procedure for Loading and Running Programs

The following procedure (illustrated in flowchart form in Figure 3-3) is used to manually load the bootstrap loader program (DEC-11-L1PA-LA):

1. Set ENABLE/HALT switch to HALT to give bus control to the console when powering up.
2. Turn OFF/POWER/LOCK switch to POWER position. This energizes the programmer's console.
3. Enter starting address of bootstrap loader (Table 3-3) into Switch register. Make certain that the correct xx value is used (*077744* for 16K memory, *137744* for 24K memory, etc.).
4. Depress LOAD ADRS switch. The address set in the Switch register is shown on the ADDRESS display.
5. Enter starting address *contents* (016701) into Switch register.
6. Lift DEP switch. The contents just entered in the Switch register is displayed in the DATA display.
7. Enter *contents* of next address into Switch register.

NOTE

It is not necessary to load addresses after the starting address has been loaded because the address is automatically incremented by two each time DEP is used consecutively.

Table 3-3
Bootstrap Loader
(DEC-11-L1PA-LA)

The bootstrap loader should be toggled into the highest core memory bank.

Address	Instruction
xx7744	016701
xx7746	000026
xx7750	012702
xx7752	000352
xx7754	005211
xx7756	105711
xx7760	100376
xx7762	116162
xx7764	000002
xx7766	xx7400
xx7770	005267
xx7772	177756
xx7774	000765
xx7776	yyyyyy

xx represents highest available memory bank. First location of the loader is one of the following, depending on memory size; xx in all subsequent locations is the same as the first.

Address	Memory Size
077744	16K
137744	24K
157744	28K

Contents of address xx7776 (yyyyyy) should contain device status register address of paper-tape reader to be used when loading the bootstrap formatted tape. Addresses are:

Teletype® Paper-Tape Reader	177560
High-Speed Paper-Tape Reader	177550

® Teletype is a trademark of Teletype Corporation.

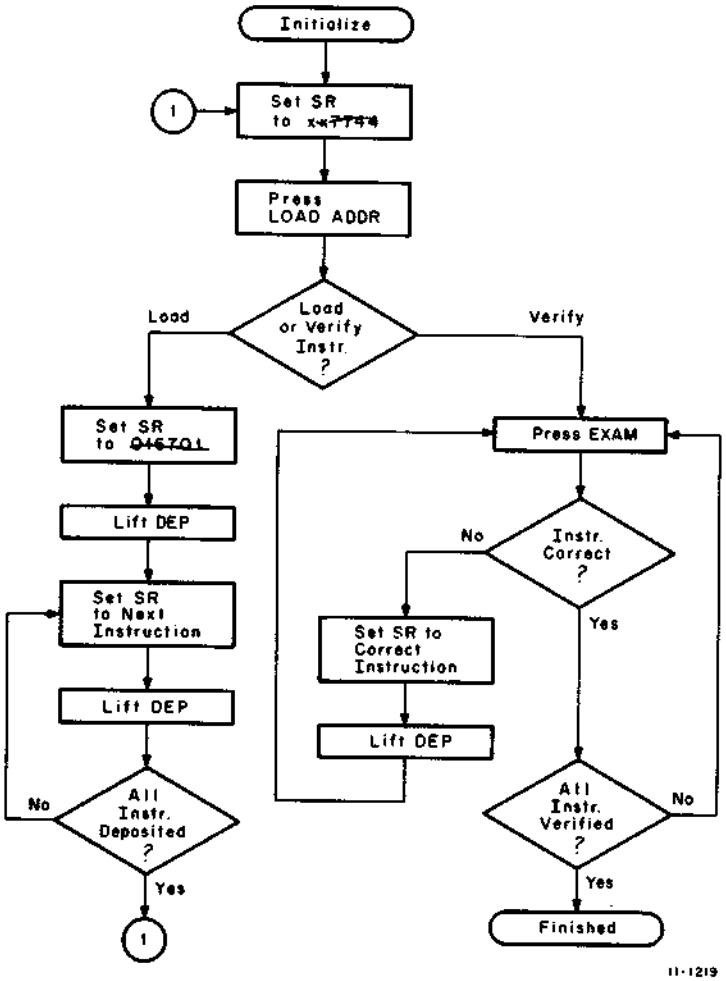


Figure 3-3 Loading and Verifying the Bootstrap Loader

8. Lift DEP switch.

9. Repeat steps 7 and 8 above for each location of the bootstrap loader. When loading the contents of address xx7766, make certain that the correct xx value is used. When loading the contents of the last address, make certain that the correct y value is used.

10. The bootstrap loader program is now loaded in memory locations xx7744 through xx7776 and can be used to automatically load other programs into memory.

11. Correct program entry can be verified by examining the addresses between xx7744 and xx7776. This is accomplished by setting the starting address into the Switch register, depressing the LOAD ADRS switch and depressing the EXAM switch. The contents of the starting address are shown in the DATA display. Each time the EXAM is again depressed, the address is automatically incremented by two and the corresponding contents displayed.

12. Step 11 alone (verification) may be sufficient if the bootstrap loader program has already been loaded into the system. The program is stored in the last portion of available memory so that it tends to survive program operation and is available for reloading programs. If the program is not intact, load according to the above procedure, beginning with step 1.

3.5.4 Automatic Program Loading

Information can be stored or modified in the computer automatically only if a program capable of performing these functions has previously been stored in the core memory. For example, having the bootstrap loader stored in the computer enables the user to operate any program that has been punched in the special tape format required by the bootstrap loader. Typical programs of this type include the absolute loader, the absolute dump, and the teleprinter dump.

The bootstrap loader is limited because of the special tape format; another loader is used to load any binary format tape into the computer. This is the absolute loader (DEC-11-L2PC-PO), which is loaded into the computer by the bootstrap loader. Once the absolute loader is in memory, any binary tape program (such as PAL III assembler, symbolic editor, input/output service routines, diagnostics, mathematical routines, etc.) may be automatically loaded.

The following paragraphs give procedures for loading the absolute loader, and for using the absolute loader to store other programs. A complete description of the absolute loader program is given in the *Paper Tape Software Programming Handbook*, DEC-11-XPTSA-A-D; refer also to the program listing, DEC-11-L2PC-LA.

Loading Absolute Loader – The following procedure is used for automatically loading the absolute loader program (DEC-11-L2PC-PO):

1. Set ENABLE/HALT switch to HALT.

2. Make certain that the bootstrap loader has been stored in core memory (Paragraph 3.5.3, step 11).

3. Enter starting address of bootstrap loader into Switch register. The starting address is xx7744 (*077744* for 16K memory, *137744* for 24K memory, etc.).

4. Depress LOAD ADRS switch. The address set in the Switch register is displayed in ADDRESS register indicators.

5. Place the input/output device (LA36 DECwriter or Teletype unit) on-line (connected to the computer).

> **NOTE**
>
> **If some other reading device (such as the high-speed paper-tape reader) is used, ensure that the y value in bootstrap loader address xx7776 corresponds to the device as described in Table 3-3.**

6. Place the absolute loader tape in the reader. Make certain that the special leader (a sequence of 351 punches) is under the reader station. Blank leader does not work.

7. Set ENABLE/HALT to ENABLE.

8. Depress START switch. The tape is now read into the computer which halts when the entire program is loaded.

9. When the tape is completely loaded, the DATA display lights may be in any configuration. The main reason for this is that no checksum capability exists in the bootstrap loader.

Any PDP-11 program punched in absolute binary format may be loaded automatically by using the absolute loader. The area in memory where the data is loaded may be determined by setting the console ADDRESS/DATA switches as indicated in Table 3-4. This allows three types of loads:

1. Data is loaded starting at an address specified on the tape.

2. Data is loaded starting where the last load left off. This is used when a program is contained on more than one tape.

3. Data is loaded at an address specified by the console ADDRESS/DATA switches; the switches are set to the desired address plus one. This may be used with position independent code.

Table 3-4
Binary Tape Load Selection
(using Absolute Loader)

Type of Load	Switch Register Settings Bits 15–01	Bit 00
Normal	Don't care	0
Relocatable (continue where left off)	0	1
Relocatable (load at specified address)	Bits (01–15) of desired address	1

Although the computer stops when the binary tape is loaded, instructions on the tape itself may cause the computer to begin executing the program immediately after loading is finished. This action is beyond the control of the user because it is part of the program on certain tapes.

The following procedure is used for automatic loading of binary tapes into the computer using the absolute loader:

1. Make certain that the absolute loader program is stored in core memory.

2. Set ENABLE/HALT switch to HALT.

3. Enter starting address of absolute loader into Switch register. The starting address is xx7500 (*0*77500 for 16K memory, *1*37500 for 24K memory, etc.).

4. Depress LOAD ADRS switch. The starting address of the absolute loader is now displayed in ADDRESS register indicators.

5. Select the type of load desired by setting the Switch register as specified in Table 3-4.

6. Make certain that the applicable input/output devices are on-line.

NOTE

The reading device may be changed at any time by the user without reloading the absolute loader. If a reader is to be changed, simply replace the contents of address xx7776 with the appropriate device status address (y value in Table 3-3).

7. Load desired binary tape into reader by placing leader under the reader station.

8. Set ENABLE/HALT switch to ENABLE.

9. Depress START switch. This begins the binary tape load.

10. If the binary tape contains a transfer address instruction, the computer begins executing the program as soon as loading is complete.

11. The reader stops when either loading is complete or there is a checksum error. A checksum error is indicated if the contents of the low order byte of register 0 (R0) are non-zero. If the paper tape moves to the end of the punched data block, the data was probably properly loaded. Verification of a proper load can be performed by checking the contents of the low order byte of R0 for all zeros.

3.5.5 Memory Dumps

A Memory Dump program is a system program that enables the contents of all or any specified portion of memory to be dumped (print or punch) onto the teletype printer and/or punch, line printer, or high speed punch. There are two dump programs available in the paper-tape software system:

1. DUMPIT, which dumps the octal representation of the contents of specified portions of memory onto the teleprinter, low speed punch, high speed punch, or line printer.

2. DUMPAB, which dumps the absolute binary code of the contents of specified portions of memory onto the low speed or high speed punch.

Both dump programs are supplied on punched paper tape in bootstrap and absolute binary formats. The absolute binary tapes are position independent and may be loaded and run anywhere in memory. DUMPIT and DUMPAB are very similar in function; they differ primarily in the type of output they produce.

3.5.5.1 Operating Procedures – Neither dump program will punch leader or trailer tape, but DUMPAB will always punch ten blank frames of tape at the start of each block of data dumped.

The operating procedures for both dump programs are:

1. Select the dump program desired and place it in the reader specified by location XX7776 (Table 3-3).

2. If a bootstrap tape is selected, load it using the bootstrap loader (Paragraph 3.5.4). When the computer halts, go to step 4.

3. If an absolute binary tape is selected, load it using the absolute loader (Paragraph 3.5.4), relocating as desired.

   Place the proper start address in the Switch Register, press LOAD ADRS and START switches. (The start addresses are shown in Paragraph 3.5.5.3.)

4. When the computer halts, enter the address of the desired output device status register in the Switch Register and press CONT switch (low speed punch and teleprinter = 177564; high speed punch = 177554; line printer = 177514).

5. When the computer halts, enter in the Switch register the address of the first byte to be dumped and press CONT switch. This address must be even when using DUMPIT.

6. When the computer halts again, enter in the Switch register the address of the last byte to be dumped and press CONT switch. When using the low speed punch, set the punch to ON before pressing CONT switch.

7. Dumping will now proceed on the selected output device.

8. When dumping is complete, the computer will halt.

If further dumping is desired, proceed to step 5. It is not necessary to respecify the output device address except when changing to another output device. In such a case, proceed to the second paragraph of step 3 to restart.

If DUMPAB is being used, a transfer block must be generated. If a tape read by the absolute loader does not have a transfer block, the loader will wait in an input loop. In such a case, the program may be manually initiated, however, this practice is not recommended because there is no guarantee that load errors will not occur when the end of the tape is read.

The transfer block is generated by performing step 5 with the transfer address in the Switch register, and step 6 with the transfer address minus 1 in the Switch register. If the tape is not to be self-starting, an odd-numbered address must be specified in step 5 (e.g., 000001).

The dump programs use all eight general registers and do not restore their original contents. Therefore, after a dump, the general registers should be loaded as necessary prior to their use by subsequent programs.

3.5.5.2 **Output Formats** – The octal output from DUMPIT is in the following format:

XXXXXX > YYYYYY YYYYYY YYYYYY YYYYYY YYYYYY YYYYYY

Where XXXXXX is the address of the first location printed or punched, and YYYYYY are words of data, the first of which starts at location XXXXXX. This is the format for every line of output. There are only eight words of data per line, but there can be as many lines as needed to complete the dump.

The output from DUMPAB is in absolute binary.

3.5.5.3 **Storage Maps** – The DUMPIT program is 87 words long. When used in absolute format, the storage map is as shown in Figure 3-4.

When used in bootstrap format, the storage map is as shown in Figure 3-5.

3.5.6 Running Programs

When running any program, the program must first be loaded into the core memory either manually or via the automatic loading programs (bootstrap loader or absolute loader). Once the program is in storage, it can be run at any time by loading the starting address of the program (refer to appropriate program documentation) into the Switch register, depressing the LOAD ADRS switch, and then depressing the START switch. The user also must make certain that the ENABLE/HALT switch is in ENABLE and that the appropriate external devices are on-line (connected to the computer).

The program can be manually stopped at any time by setting the ENABLE/HALT switch to HALT. It can be restarted from that point by returning the ENABLE/HALT switch to ENABLE and depressing the CONT switch. It can be started anew by reloading the starting address and depressing the START switch.

A program can be altered during operation or new data can be introduced through the Switch register. This console register has a bus address that the processor can reference in its instruction sequence. The information transferred may be treated as data or used to alter program flow.

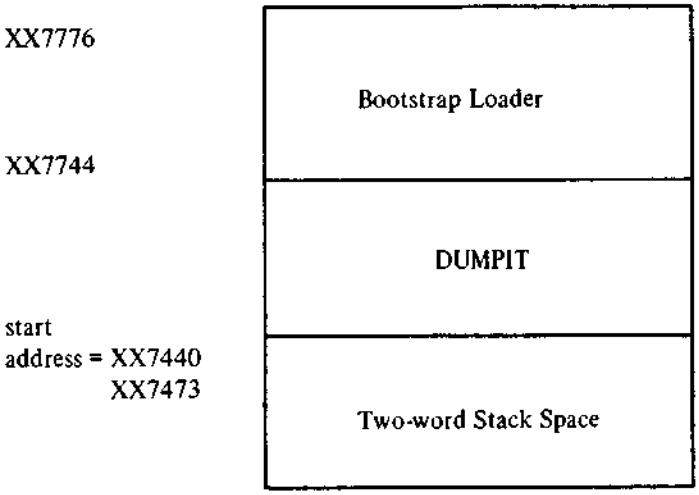
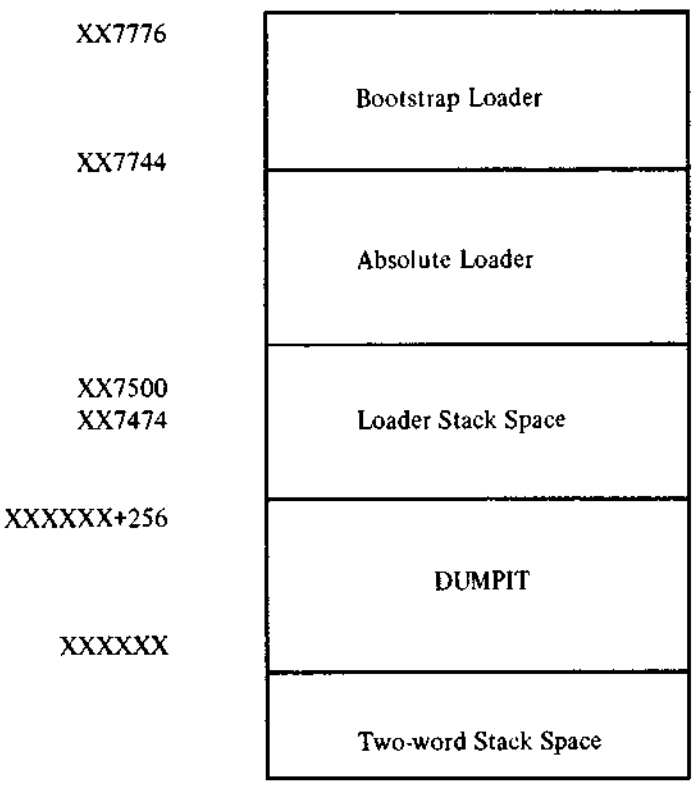


Figure 3-4 Absolute Format



XXXXXX= desired load address = start address

Figure 3-5 Bootstrap Format

3.6 BASIC PROGRAMMING

To produce programs that fully utilize the power and flexibility of the PDP-11, it is necessary for the user to first become familiar with various programming techniques that are part of the basic design philosophy of the PDP-11 Computer. These techniques (such as use of stacks, subroutine linkage, interrupt nesting, re-entrant and recursive programming, etc.) are covered in the *PDP-11/05/10/35/40 Processor Handbook*, which also provides a detailed discussion of the instruction set.

In addition to the general programming information given in the *PDP-11/05/10/35/40 Processor Handbook*, the user should be familiar with console operation (Paragraphs 3.2 and 3.3) and with the instruction set described in Chapter 4.

For those users already familiar with programming other computers in the PDP-11 series, the primary programming differences between the PDP-11/05/10, PDP-11/15/20 and PDP-11/35/40 Systems are listed in Table 4-8. With this table, the experienced user can immediately begin to program the PDP-11/05/10-S Computer.

CHAPTER 4
INSTRUCTION SET

4.1 SCOPE

The KD11-B is defined by its instruction set. The sequences of processor operations are selected according to the instruction decoding. This chapter contains tables that describe the PDP-11/05/10-S instructions and instruction set addressing modes. Instruction set differences between the PDP-11/05/10-S and other PDP-11 processors are listed in Table 4-8.

4.2 ADDRESSING MODES

4.2.1 Introduction

Data stored in memory must be accessed and manipulated. Data handling is specified by a PDP-11 instruction (MOV, ADD, etc.) which usually indicates:

- The function (operation code).
- A general purpose register for locating the source operand and/or a general purpose register for locating the destination operand.
- An addressing mode [to specify how the selected register(s) is to be used].

A large portion of the data handled by a computer is usually structured in character strings, arrays, lists, etc. Thus, the PDP-11 is designed to handle structured data efficiently and flexibly. The general registers may be used with an instruction in any of the following ways:

- As accumulators. The data to be manipulated resides within the register.
- As pointers. The contents of the register are the address of the operand, rather than the operand itself.
- As pointers that automatically step through core locations. Automatically stepping forward through consecutive core locations is termed auto-increment addressing; automatically stepping backwards is termed autodecrement addressing. These modes are particularly useful for processing tabular data.
- As index registers. In this instance, the contents of the register and the word following the instruction are summed to produce the address of the operand. This allows easy access to variable entries in a list.

PDP-11s also have instruction addressing mode combinations that facilitate temporary data storage structures for convenient handling of data that must be frequently accessed. This is known as the "stack".

In the PDP-11 any register can be used as a stack pointer under program control; however, certain instructions associated with subroutine linkage and interrupt service automatically use register 6 as a hardware stack pointer. For this reason, R6 is frequently referred to as the SP (Stack Pointer).

Two types of instructions utilize the addressing modes: single operand and double operand. Figure 4-1 shows the formats of these two types of instructions. The addressing modes are listed in Table 4-1.

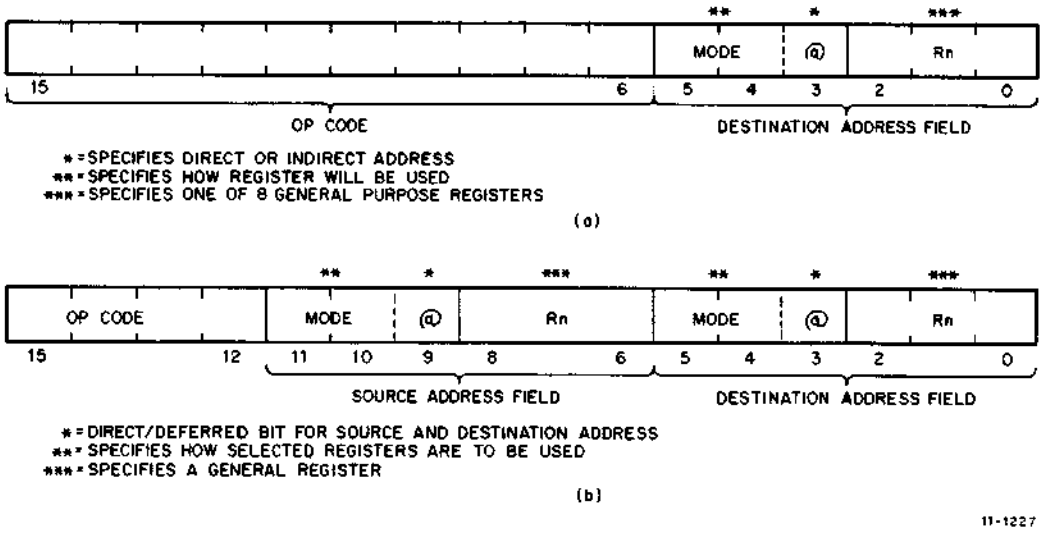


Figure 4-1 Addressing Mode Instruction Formats

4.2.2 Instruction Timing

The PDP-11 is an asynchronous processor in which, in many cases, memory and processor operations are overlapped. The execution time for an instruction is the sum of a basic instruction time and the time to determine and fetch the source and/or destination operands. Table 4-2 shows the addressing times required for the various modes of addressing source and destination operands. All times stated are subject to ±10% variation.

4.3 PDP-11/05/10-S INSTRUCTIONS

The PDP-11 instructions can be divided into five groupings:

1. Single Operand Instructions (shifts, multiple precision instructions, rotates)
2. Double Operand Instructions (arithmetic and logical instructions)
3. Program Control Instructions (branches, subroutines, traps)
4. Operate Group Instructions (processor control operations)
5. Condition Codes Operators (processor status word bit instructions)

Tables 4-3 through 4-7 list each instruction, including byte instructions, for the respective instruction groups. The instruction times in the tables are for address mode 0. For address modes other than mode 0, the total instruction time may be calculated by adding the addressing times indicated in Table 4-2. Figure 4-2 shows the six different instruction formats of the instruction set, and the individual instructions in each format.

4.4 INSTRUCTION SET DIFFERENCES

Table 4-8 lists the major differences between the KD11-B processor used in the PDP-11/05/10-S, and the processors used in the PDP-11/15/20 and PDP-11/35/40.

Table 4-1
Addressing Modes

Binary Code	Name	Assembler Syntax	Function
		DIRECT MODES	
000	Register	Rn	Register contains operand.
010	Autoincrement	(Rn) +	Register contains address of operand. Register contents incremented after reference.
100	Autodecrement	-(Rn)	Register contents decremented before reference register contains address of operand.
110	Index	X(Rn)	Value X (stored in a word following the instruction) is added to (Rn) to produce address of operand. Neither X nor (Rn) are modified.
		DEFERRED MODES	
001	Register Deferred	@Rn or (Rn)	Register contains the address of the operand.
011	Autoincrement Deferred	@(Rn) +	Register is first used as a pointer to a word containing the address of the operand, then incremented (always by two; even for byte instructions).
101	Autodecrement	@ -(Rn)	Register is decremented (always by two; even for byte instructions) and then used as a pointer to a word containing the address of the operand.
111	Index Deferred	@X(Rn)	Value X (stored in a word following the instruction) and (Rn) are added and the sum is used as a pointer to a word containing the address of the operand. Neither X nor (Rn) are modified.
		PC ADDRESSING	
010	Immediate	#n	Operand follows instruction.
011	Absolute	@#A	Absolute address follows instruction.
110	Relative	A	Address of A, relative to the instruction, follows the instruction.
111	Relative Deferred	@A	Address of location containing address of A, relative to the instruction, follows the instruction.

Rn = Register
X, n, A = next program counter (PC) word (constant)

Table 4-2
Addressing Times

	Addressing Format		Time (μs)	
Mode	Description	Symbolic	Source*	Destination**
0	Register	R	0	0
1	Register Deferred	@R or (R)	0.9	2.4
2	Autoincrement	(R) +	0.9	2.4
3	Autoincrement Deferred	@(R) +	2.4	3.4
4	Autodecrement	- (R)	0.9	2.4
5	Autodecrement Deferred	@ - (R)	2.4	3.4
6	Indexed	± X (R)	2.4	3.4
7	Index Deferred	@ ± X (R) or @ (R)	3.4	4.7

* For Source time, add 1.3 μs for odd byte addressing.
** For destination time, modify as follows:

a. Add 1.3 μs for odd byte addressing with a non-modifying instruction.

b. Add 2.4 μs for odd byte addressing with a modifying instruction.

c. Subtract 1.2 μs for a non-modifying instruction.

Table 4-3
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
CLR CLRB 3.4 μs	0050DD* 1050DD	(dst)† ← 0	N: cleared Z: set V: cleared C: cleared	Contents of specified destination are replaced with zeroes.
COM COMB 3.4 μs	0051DD 1051DD	(dst) ← n (dst)	N: set if most significant bit of result is 0 Z: set if result is 0 V: cleared C: set	Replaces the contents of the destination address by their logical complement (each bit equal to 0 set and each bit equal to 1 cleared).
INC INCB 3.4 μs	0052DD 1052DD	(dst) ← (dst) + 1	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) was 077777 C: not effected	Add 1 to the contents of the destination.
DEC DECB 3.4 μs	0053DD 1053DD	(dst) ← (dst) - 1	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) was 100000 C: not effected	Subtract 1 from the contents of the destination.
NEG NEGB 3.4 μs	0054DD 1054DD	(dst) ← -(dst)	N: set if result is less than 0 Z: set if result is 0 V: set if result is 100000 C: cleared if result is 0	Replaces the contents of the destination address by its 2's complement. Note that 100000 is replaced by itself.
ADC ADCB 3.4 μs	0055DD 1055DD	(dst) ← (dst) + C	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) is 077777 and C is 1 C: set if (dst) is 177777 and C is 1	Adds the contents of the C-bit into the destination. This permits the carry from the addition of the low order words/bytes to be carried into the high order result.

Table 4-3 (Cont)
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
SBC SBCB 3.4 μs	0056DD 1056DD	(dst) ← (dst) -C	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) was 100000 C: cleared if (dst) is 0 and C is 1	Subtracts the contents of the C-bit from the destination. This permits the carry from the subtraction of the low order words/ bytes to be subtracted from the high order part of the result.
TST TSTB 3.4 μs	0057DD 1057DD	(dst) ← (dst)	N: set if result is less than 0 Z: set if result is 0 V: cleared C: cleared	Sets the condition codes N and Z according to the contents of the destination address.
ROR RORB 3.4 μs	0060DD	(dst) ← (dst) rotate right one place.	N: set if high order bit of the result is set Z: set if all bits of result are 0 V: loaded with the exclusive-OR of the N-bit and the C-bit as set by ROR	Rotates all bits of the destination right one place. The low order bit is loaded into the C-bit and the previous contents of the C-bit are loaded into the high order bit of the destination.
ROL ROLB 3.4 μs	0061DD 1061DD	(dst) ← (dst) rotate left one place.	N: set if the high order bit of the result word is set (result < 0); cleared otherwise Z: set if all bits of the result word = 0; cleared otherwise V: loaded with the exclusive-OR of the N-bit and C-bit (as set by the completion of the rotate operation) C: loaded with the high order bit of the destination	Rotate all bits of the destination left one place. The high order bit is loaded into the C-bit of the status word and the previous contents of the C-bit are loaded into the low order bit of the destination.

Table 4-3 (Cont)
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
ASR ASRB 3.4 μs	0062DD 1062DD	(dst) ← (dst) shifted one place to the right.	N: set if the high order bit of the result is set (result < 0), cleared otherwise Z: set if the result = 0; cleared otherwise V: loaded from the exclusive-OR of the N-bit and C-bit (as set by the completion of the shift operation). C: loaded from low order bit of the destination	Shifts all bits of the destination right one place. The high order bit is replicated. The C-bit is loaded from the low order bit of the destination. ASR performs signed division of the destination by two.
ASL ASLB 3.4 μs	0063DD 1063DD	(dst) ← (dst) shifted one place to the left.	N: set if high order bit of the (result < 0); cleared otherwise Z: set if the result = 0; cleared otherwise V: loaded with the exclusive-OR of the N-bit and C-bit and C-bit (as set by the completion of the shift operation) C: loaded with the high order bit of the destination	Shifts all bits of the destination left one place. The low order bit is loaded with a 0. The C-bit of the status word is loaded from the high order bit of the destination. ASL performs a signed multiplication of the destination by 2 with overflow indication.

Table 4-3 (Cont)
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
JMP 1.0 μs	0001DD	PC ← (dst)	Not effected.	JMP provides more flexible program branching than provided with the branch instruction. Control may be transferred to any location in memory (no range limitation) and can be accomplished with the full flexibility of the addressing modes. with the exception of register mode 0. Execution of a jump with mode 0 will cause an illegal instruction condition. (Program control cannot be transferred to a register.) Register deferred mode is legal and will cause program control to be transferred to the address held in the specified register. Note that instructions are word data and must therefore be fetched from an even numbered address. A boundary error trap condition will result when the processor attempts to fetch an instruction from an odd address.
SWAB 4.3 μs	0003DD	Byte 1/Byte 0 Byte 0/Byte 1	N: set if high order bit of low order byte (bit 7) of result is set; cleared otherwise Z: set if low order byte of result = 0; cleared otherwise V: cleared C. cleared	Exchanges high order byte and low order byte of the destination word (destination must be a word address).

* DD = destination (address mode and register)
† (dst) = destination contents

Table 4-4
Double Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
MOV MOVB 3.7 μs 3.1 μs mode 0	01SSDD* 11SSDD	(dst) ← (src) †	N: set if (src) < 0; cleared otherwise Z: set if (src) = 0; cleared otherwise V: cleared C: not effected	Word: Moves the source operand to the destination location. The previous contents of the destination are lost. The source operand is not effected. Byte: Same as MOV. The MOVB to a resistor (unique among byte instructions) extends the most significant bit of the low order byte (sign extension). Otherwise MOVB operates on bytes exactly as MOV operates on words.
CMP CMPB 3.7 μs	02SSDD 12SSDD	(src) - (dst) [in detail, (src) + ~ (dst) + 1]	N: set if result < 0, cleared otherwise Z: set if result = 0; cleared otherwise V: set if there was arithmetic overflow, i.e., operands were of opposite signs and the sign of the destination was the same as the sign of the result; cleared otherwise C: cleared if there was a carry from the most significant bit of the result; set otherwise	Compares the source and destination operands and sets the condition codes, which may then be used for arithmetic and logical conditional branches. Both operands are uneffected. The only action is to set the condition codes. The compare is customarily followed by a conditional branch instruction. Note that unlike the subtract instruction the order of operation is (src) - (dst), not (dst) - (src).

Table 4-4 (Cont)
Double Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BIT BITB 3.7 μs	03SSDD 13SSDD	(src) ⋀ (dst)	N: set if high order bit of result set; cleared otherwise Z: set if result = 0; cleared otherwise V: cleared C: not effected	Performs logical AND comparison of the source and destination operands and modifies condition codes accordingly. Neither the source nor destination operands are effected. The BIT instruction may be used to test whether any of the corresponding bits that are set in the destination are clear in the source.
BIC BICB 3.7 μs	04SSDD 14SSDD	(dst) ← ~ (src) ⋀ (dst)	N: set if high order bit of result set, cleared otherwise Z: set if result = 0, cleared otherwise V: cleared C. not effected	Clears each bit in the destination that corresponds to a set bit in the source. The original contents of the destination are lost. The contents of the source are uneffected.
BIS BISB 3.7 μs	05SSDD 15SSDD	(dst) ← (src) ⋀ (dst)	N: set if high order bit of result set; cleared otherwise Z: set if result = 0; cleared otherwise V: cleared C: not effected	Performs inclusive-OR operation between the source and destination operands and leaves the result at the destination address; i.e., corresponding bits set in the destination. The contents of the destination are lost.
ADD	06SSDD	(dst) ← (src) + (dst)	N: set if result 0; cleared otherwise Z: set if result = 0; cleared otherwise	Adds the source operand to the destination operand and stores the result at the destination address. The original contents of the destination are lost. The contents of the source are not effected. Two's complement addition is performed.

Table 4-4 (Cont)
Double Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
ADD (Cont)			V: set if there was arithmetic overflow as a result of the operation; that is both operands were of the same sign and the result was of the opposite sign; cleared otherwise C: set if there was a carry from the most significant bit of the result cleared otherwise	
SUB 3.7 μs	16SSDD	(dst) ← (dst) - (src) in detail, (dst) + ~ (src) + 1 (dst)	N: set if result < 0; cleared otherwise Z: set if result = 0; cleared otherwise V: set if there was arithmetic overflow as a result of the operation, i.e., if operands were of opposite signs and the sign of the source was the same as the sign of the result, cleared otherwise C: cleared if there was a carry from the most significant bit of the result; set otherwise	Subtracts the source operand from the destination operand and leaves the result at the destination address. The original contents of the destination are lost. The contents of the source are not effected. In double precision arithmetic, the C-bit, when set, indicates a borrow.

* SS = source (address mode and register)
† (src) = source contents

Table 4-5
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BR 2.5 μs	000400 xxx†	PC ← PC + (2 X offset)	Uneffected	Provides a way of transferring program control within a range of -128 to +127 words with a one word instruction. It is an unconditional branch.
BNE 1.9 μs no branch 2.5 μs branch	001000 xxx	PC ← PC + (2 X offset) if Z = 0	Uneffected	Tests the state of the Z-bit and causes a branch if the Z-bit is is clear. BNE is the complementary operation to BEQ. It is used to test inequality following a CMP, to test that some bits set in the destination were also in the source, following a BIT, and generally, to test that the result of the previous operation was not 0.
BEQ 1.9 μs no branch 2.5 μs branch	001400 xxx	PC ← PC + (2 X offset) if Z = 1	Uneffected	Tests the state of the Z-bit and causes a branch if Z is set. As an example, it is used to test equality following a CMP operation. to test that no bits set in the destination were also set in the source following a BIT operation, and generally, to test that the result of the previous operation was 0.
BGE 1.9 μs no branch 2.5 μs branch	002000 xxx	PC ← PC + (2 X offset) if N v V = 0	Uneffected	Causes a branch if N and V are either both clear or both set. BGE is the complementary operation to BLT. Thus. BGE always causes a branch when it follows an operation that caused addition to two positive numbers. BGE also causes a branch on a 0 result.

Table 4-5 (Cont)
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BLT 1.9 μs no branch 2.5 μs branch	002400 xxx	PC ← PC + (2 X offset) if N V = 1	Uneffected	Causes a branch if the exclusive-OR of the N- and V-bits are 1. Thus, BLT always branches following an operation that added two negative numbers, even if overflow occurred. In particular, BLT always causes a branch if it follows a CMP instruction operating on a negative source and a positive destination (even if overflow occurred). Further, BLT never causes a branch when it follows a CMP instruction operating on a positive source and negative destination. BLT does not cause a branch if the result of the previous operation was 0 (without overflow).
BGT 1.9 μs no branch 2.5 μs branch	003000 xxx	PC ← PC + (2 X offset) if Z v (N ⊻ V) = 0	Uneffected	Operation of BGT is similar to BGE, except BGT does not cause a branch on a 0 result.
BLE 1.9 μs no branch 2.5 μs branch	003400 xxx	PC ← PC + (2 X offset) if Z v (N ⊻ V) = 1	Uneffected	Operation is similar to BLT but in addition will cause a branch if the result of the previous operation was 0.
BPL 1.9 μs no branch 2.5 μs branch	100000 xxx	PC ← PC + (2 X offset) if N = 0	Uneffected	Tests the state of the N-bit and causes a branch if N is clear. BPL is the complementary operation of BMI.
BMI 1.9 μs no branch 2.5 μs branch	100400 xxx	PC ← PC + (2 X offset) if N = 1	Uneffected	Tests the state of the N-bit and causes a branch if N is set. It is used to test the sign (most significant bit) of the result of the previous operation.

Table 4-5 (Cont)
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BHI 1.9 μs no branch 2.5 μs branch	101000 xxx	PC ← PC + (2 X offset) if C = 0	Uneffected	Causes a branch if the previous operation causes neither a carry nor a 0 result. This will happen in comparison (CMP) operations as long as the source has a higher unsigned value than the destination.
BLOS 1.9 μs no branch 2.5 μs branch	101400 xxx	PC ← PC + (2 X offset) if C v Z = 1	Uneffected	Causes a branch if the previous operation caused either a carry or a 0 result. BLOS is the complementary operation to BHI. The branch occurs in comparison operations as long as the source is equal to or has a lower unsigned value than the destination. Comparison of unsigned values with the CMP instruction to be tested for "higher or same" and "higher" by a simple test of the C-bit.
BVC 1.9 μs no branch 2.5 μs branch	102000 xxx	PC ← PC + (2 X offset) if V = 0	Uneffected	Tests the state of the V-bit and causes a branch if the V-bit is clear. BVC is complementary operation to BVS.
BVS 1.9 μs no branch 2.5 μs branch	102400 xxx	PC ← PC + (2 X offset) if V = 1	Uneffected	Tests the state of V-bit (overflow) and causes a branch if the V-bit is set. BVS is used to detect arithmetic overflow in the previous operation.
BCC BHIS 1.9 μs no branch 2.5 μs branch	103000 xxx	PC ← PC + (2 X offset) if C = 0	Uneffected	Tests the state of the C-bit and causes a branch if C is clear. BCC is the complementary operation to BCS.
BCS BLO 1.9 μs no branch 2.5 μs branch	103400 xxx	PC ← PC + (2 X offset) if C = 1	Uneffected	Tests the state of the C-bit and causes a branch if C is set. It is used to test for a carry in the result of a previous operation.

Table 4-5 (Cont)
Program Control Instruction

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
JRS 3.8 μs	004RDD	(tmp) ← (dst) (tmp is an internal processor register) ↓ (SP) ← reg (push reg contents onto processor stack) reg ← PC PC holds location following JSR; this address PC ← (tmp), now put in (reg)	Uneffected	In execution of the JSR, the old contents of the specified register (the linkage pointer) are automatically pushed onto the processor stack and new linkage information placed in the register. Thus, subroutines nested within subroutines to any depth may all be called with the same linkage register. There is no need either to plan the maximum depth at which any particular subroutine will be called or to include instructions in each routine to save and restore the linkage pointer. Further, since all linkages are saved in a re-entrant manner on the processor stack, execution of a subroutine may be interrupted, and the same subroutine re-entered and executed by an interrupt service routine. Execution of the initial subroutine can then be resumed when other requests are satisfied. This process (called nesting) can proceed to any level. JSR PC, dst is a special case of the PDP-11 subroutine call suitable for subroutine calls that transmit parameters.
RTS 3.8 μs	00020R	PC ← (reg) (reg) ← SP ↑	Uneffected	Loads contents of register into PC and pops the top element of the processor stack into the specified register. Return from a non-re-entrant subroutine is typically made through the same register that was used in its call. Thus, a subroutine called with a JSR PC, dst exits with an RTS PC, and a subroutine called with a JSR R5, dst may pick up parameters with addressing modes (R5) +, X (R5), or @X (R5) and finally exit, with an RTS R5.

Table 4-5 (Cont)
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
(No mnemonic) 8.2 μs	000003	↓ (SP) ← PS ↓ (SP) ← PC PC ← (14) PS ← (16)	N: loaded from trap vector Z: loaded from trap vector V: loaded from trap vector C: loaded from trap vector	Performs a trap sequence with a trap vector address of 14. Used to call debugging aids. The user is cautioned against employing code 000003 in programs run under these debugging aids.
IOT 8.2 μs	000004	↓ (SP) ← PS ↓ (SP) ← PC PC ← (20) PS ← (22)	N: loaded from trap vector Z: loaded from trap vector C: loaded from trap vector	Performs a trap sequence with a trap vector address of 20. Used to call the I/O executive routine IOX in the paper-tape software system, and for error reporting in the disk operating system.
EMT 8.2 μs	104000	↓ (SP) ← PS ↓ (SP) ← PC PC ← (30) PS ← (32)	N: loaded from trap vector Z: loaded from trap vector V: loaded from trap vector C: loaded from trap vector	All operation codes from 104000 to 104377 are EMT instructions and may be used to transmit information to the emulating routine (e.g., function to be performed). The trap vector for EMT is at address 30; the new central processor status (PS) is taken from the word at address 32. **CAUTION** **EMT is used frequently by DEC system software and is therefore not recommended for general use.**
TRAP 8.2 μs	104400 to 104777	↓ (SP) ← PS ↓ (SP) ← PC PC ← (34) PS ← (36)	N: loaded from trap vector Z: loaded from trap vector V: loaded from trap vector C: loaded from trap vector	Operation codes from 104400 to 104777 are TRAP instructions TRAPs and EMTs are identical in operation, except that the trap vector for TRAP is at address 34. **NOTE** **Since DEC software makes frequent use of EMT, the TRAP instruction is recommended for general use.**

NOTE: Condition Codes are uneffected by these instructions

†xxx = offset, 8 bits (0-7) of instruction format
R = register (linkage pointer)

Table 4-6
Operate Group Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
HALT 1.8 μs	000000		Not effected	Causes the processor operation to cease. The console is given control of the processor. The console data lights display the address of the HALT instruction plus two. Transfers on the Unibus are terminated immediately. The PC points to the next instruction to be executed. Pressing the CON key on the console causes processor operation to resume. No INIT signal is given.
WAIT 1.8 μs	000001		Not effected	Provides a way for the processor to relinquish use of the bus while it waits for an external interrupt. Having been given a WAIT command, the processor will not compete for bus by fetching instructions or operands from memory. This permits higher transfer rates between device and memory, since no processor induced latencies will be encountered by bus requests from the device. In WAIT, as in all instructions, the PC points to the next instruction following the WAIT operation. Thus, when an interrupt causes the PC and PS to be pushed onto the stack, the address of the next instruction following the WAIT is saved. The exit from the interrupt routine (i.e., execution of an RTI instruction) will cause resumption of the interrupted process at the instruction following the WAIT.
RTI 4.4 μs	000002	PC (SP) PSW (SP)	N: loaded from processor stack Z: loaded from processor stack V: loaded from processor stack C: loaded from processor stack	Used to exit from an interrupt or trap service routine. The PC and PSW are restored (popped) from the processor stack. If a trace trap is pending, the first instruction after the RTI will be executed prior to the next T trap.
RESET 20 ms	000005	PC (SP) PSW (SP)	Not effected	Sends INIT on the Unibus for 20 ms. All devices on the Unibus are reset to their state at power-up.

Table 4-7
Condition Code Operators

Mnemonic/ Instruction Time	OP Code	Description
CLC	000241	Set and clear condition code bits. Selectable combination of these bits may be cleared or set together. Condition code bits corresponding to bits in the condition code operator (bits 0–3) are modified according to the sense of bit 4, the set/clear bit of the operator; i.e., set the bit specified by bit 0, 1, 2, or 3 if bit 4 is a 1. Clear corresponding bits if bit 4 = 0.
CLZ	000242	
CLN	000244	
CLV	000250	
Set all CCs	000261	
Clear all CCs	000262	
Clear V and C	000264	
No operation	000270	
No operation	000277	
	000257	
2.5 μs	000243	
	000240	
	000260	

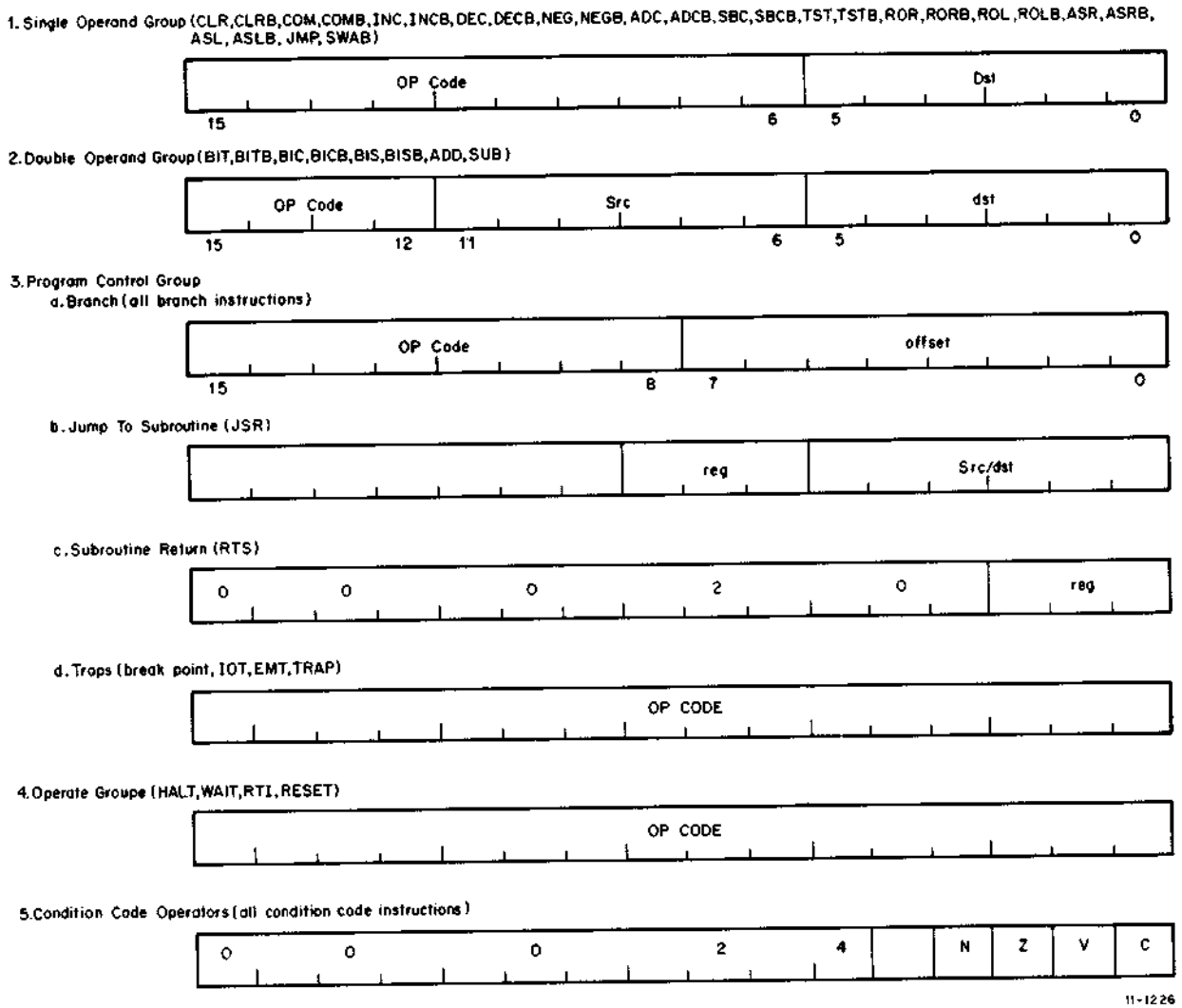


Figure 4-2 PDP-11 Instruction Formats

Table 4-8
Table of Programming Differences

	11/20	11/05 & 11/10	11/35 & 11/40
GENERAL REGISTERS (including PC & SP)			
OPR %R, (R) + or OPR %R, - (R) OPR %R, @ (R) + OPR %R, @ - (R) (Using the same reg. as both source & destination.)	Contents of R are incremented by 2 (or decremented by 2) before being used as the source operand.	Initial contents of R are used as the source operand.	(Same as 11/20)
JMP (R) + or JSR reg, (R) + (Jump using auto-increment mode.)	Contents of R are incremented by 2, then used as the new PC address.	(Same as 11/20)	Initial contents of R are used as the new PC.

MOV PC, @ # A or
MOV PC, A
(Moving the incremented PC to a memory address referenced by the PC.)
	Location A will contain the PC of the Move Instruction +4.	Location A will contain PC + 2.	(Same as 11/20)

Stack Pointer (SP), R6 used for referencing.	Using the SP for pointing to odd addresses or non-existent memory causes a HALT (double bus error).	(Same as 11/20)	Odd address of non-existent memory references with SP cause a fatal trap, with a new stack created at locations 0 & 2.
Stack Overflow	Stack limit fixed at 400 (octal). Overflow (going lower) checked after @ - (R6), JSR, traps, and address modes 4 & 5. Overflow serviced by an overflow trap. No red zone.	(Same as 11/20)	Variable limit with Stack Limit option. Overflow checked after JSR, traps, and address modes 1, 2, 4, & 6. Non-altering references to stack data is always allowed. There is a 16-word yellow (warning) zone. Red zone trap occurs if stack is 16 words below boundary; PS & PC are saved at locations 0 & 2.

Table 4-8 (Cont)
Table of Programming Differences

	11/20	11/05 & 11/10	11/35 & 11/40
TRAPS & INTERRUPTS			
RTI instruction	First instruction after RTI is guaranteed to be executed.	(Same as 11/20)	If RTI sets the T bit, the T bit trap is acknowledged immediately after the RTI instruction.
RTT instruction	(Not implemented)	(Not implemented)	First instructon after RTT is guaranteed to be executed. Acts like RTI on the 11/20.
Processor Status (PS) odd byte at location 777 777.	Addressing odd byte of PS (bits 15–8) causes an odd address trap.	Odd byte of PS can be addressed without a trap.	(Same as 11/05)
T bits of PS	T bit can be loaded by direct address of PS, or from the console.	(Same as 11/20)	Only RTI, RTT, traps, and interrupts can load the T bit.
Interrupt service routine	The first instruction in the routine is guaranteed to be executed.	The first instruction will not be executed if another interrupt occurs at a higher priority.	(Same as 11/05)
Priority order of traps & interrupts	Odd address Timeout HALT from console Trap instructions Trace trap Stack overflow Power fail	Odd address Timeout HALT instruction Trap instructions Trace Trap Stack overflow Power fail HALT from console	Odd address Stack overflow (red) Timeout Mem. Mgt. violation HALT Trap instructions Trace trap Stack overflow (yellow) Power fail

Table 4-8 (Cont)
Table of Programming Differences

	11/20	11/05 & 11/10	11/35 & 11/40
MISCELLANEOUS			
SWAB and V bit	SWAB instruction conditionally sets the V bit.	V bit is cleared.	(Same as 11/05)
Instruction set	Basic set.	(Same as 11/20)	Basic set + MARK, RTT, SOB, SXT, XOR. EIS adds: MUL, DIV, ASH, ASHC. Floating point adds: FADD, FSUB, FMUL, FDIV.

CHAPTER 5
POWER SYSTEM

5.1 SCOPE

This chapter supplements the description of the H765 Power Supply located in the *BA11-K Mounting Box Maintenance Manual.* The BA11-K Manual presents a detailed description of the H765 Power Supply, describes the mechanical layout, explains the operation of the components of the supply, and provides troubleshooting and removal and replacement procedures. Furthermore, this chapter presents an overview of the H765 Power Supply and describes the interconnection of the supply to the logic backplanes that comprise the PDP-11/05/10-S. For any specific information refer to the *BA11-K Mounting Box Maintenance Manual.*

5.2 H765 POWER SUPPLY

The H765 Power Supply consists of an ac input box, a transformer assembly, five regulators, two fans, and a power distribution board. Four of the regulators, (H754, H745, and two H744's) are discrete mechanical assemblies mounted at either side of the transformer assembly and ac input box. The fifth regulator, a 5411086 +15 V regulator is contained on a printed circuit board mounted within the ac input box. In addition, the ac input box contains a power control board which controls the application of power to the primaries of the power supply transformer.

The physical layout of these components is shown in Figure 5-1.

5.3 POWER SYSTEM

The PDP-11/05/10-S power system is illustrated in Figure 5-2. The figure shows the power flow within the BA11-K Mounting Box. The representations used are symbolic, and do not imply a wire for wire, or pin for pin correspondence. However, all harnesses and their connectors mate as indicated in the figure.

5.3.1 Power Flow

This description references Figure 5-2. The power cord provides ac power to the ac input box, where power flow can be interrupted by circuit breaker CB1, (located at the rear of the mounting box), or by relay K2. Relay K2 is controlled by the power control board, which is in turn controlled by the console POWER key switch (connected to J3 of the ac input box), and the thermal switch located in the transformer assembly (connected to J4). If relay K2 is activated, the ac input power is routed to connector J5 of the ac input box, to which P5 of the transformer assembly connects. The wiring on connector J5 configures the transformer primaries for either 115 Vac or 230 Vac operation. The type 7009811-1 ac input box configures the two transformer primaries in parallel, for 115 Vac operation, while the type 7009811-2 ac input box configures the transformer primaries in series for 230 Vac operation.

If in its operation, the transformer heats up excessively, the thermal switch mounted in the transformer assembly deactivates the power control board causing relay K2 to remove power from the transformer primaries.

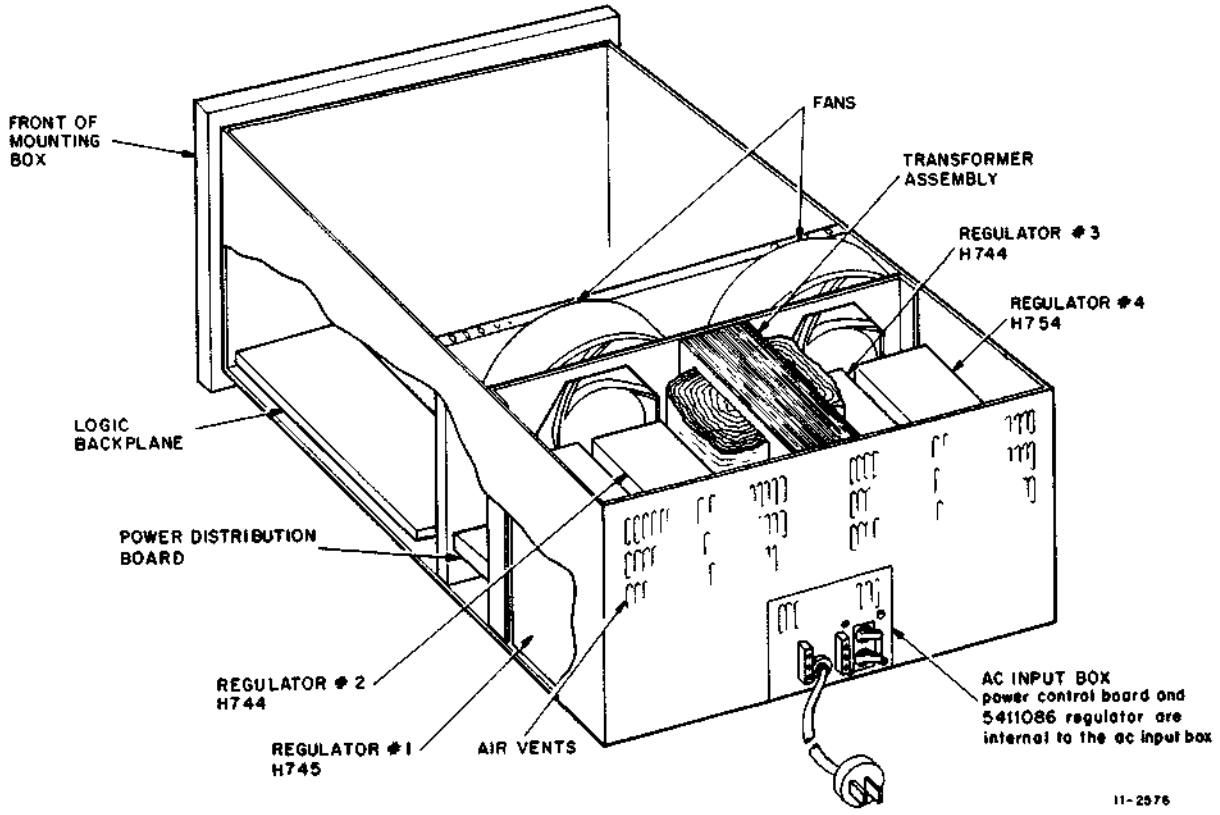


Figure 5-1 Physical Layout of H765 Power Supply

The transformer has five 28 Vac secondary windings, each of which is used to feed one regulator. Four of the secondaries are connected to the power distribution board via P1-J1, and then connected to the four discrete regulators via their respective connector (J13, J14, J15, J16). The same connector routes the regulator output back to the power distribution board where the regulator output voltages are distributed to the set of five voltage distribution connectors (J3, J5, J7, J9, J11).

The fifth transformer secondary is connected to the 5411086 regulator within the ac input box via P2/J1 and supplies it with 28 Vac. The voltage output of this regulator is fed to the power distribution board and is distributed to the five voltage distribution connectors (J3, J5, J7, J9, J11) and to the H745 -15 V regulator (via J13). In addition, the 5411086 regulator generates three logic signals (LTC L, DC LO L, AC LO L) which are fed back to the power distribution board, but distributed to signal distribution connectors J4, J6, J8, J10, J12. The logic backplane of the PDP-11/05/10-S computer connects to J9, J10, and J11 of the power distribution board. The power distribution board is illustrated in Figure 5-3. Connectors J3 through J12 of the power distribution board are accessible from the bottom of the computer mounting box (with the bottom cover removed). The H765 Power Supply can also be swung back to access the power supply connections illustrated in Figure 5-2; the procedure is described in the *BA11-K Mounting Box Maintenance Manual.*

5.4 VOLTAGE REGULATOR OUTPUT SPECIFICATIONS

Table 5-1 lists the output specifications of the voltage regulators used in the H765 Power Supply. When installing additional system units in the BA11-K Mounting Box, be careful not to exceed the current limitation of any regulator.

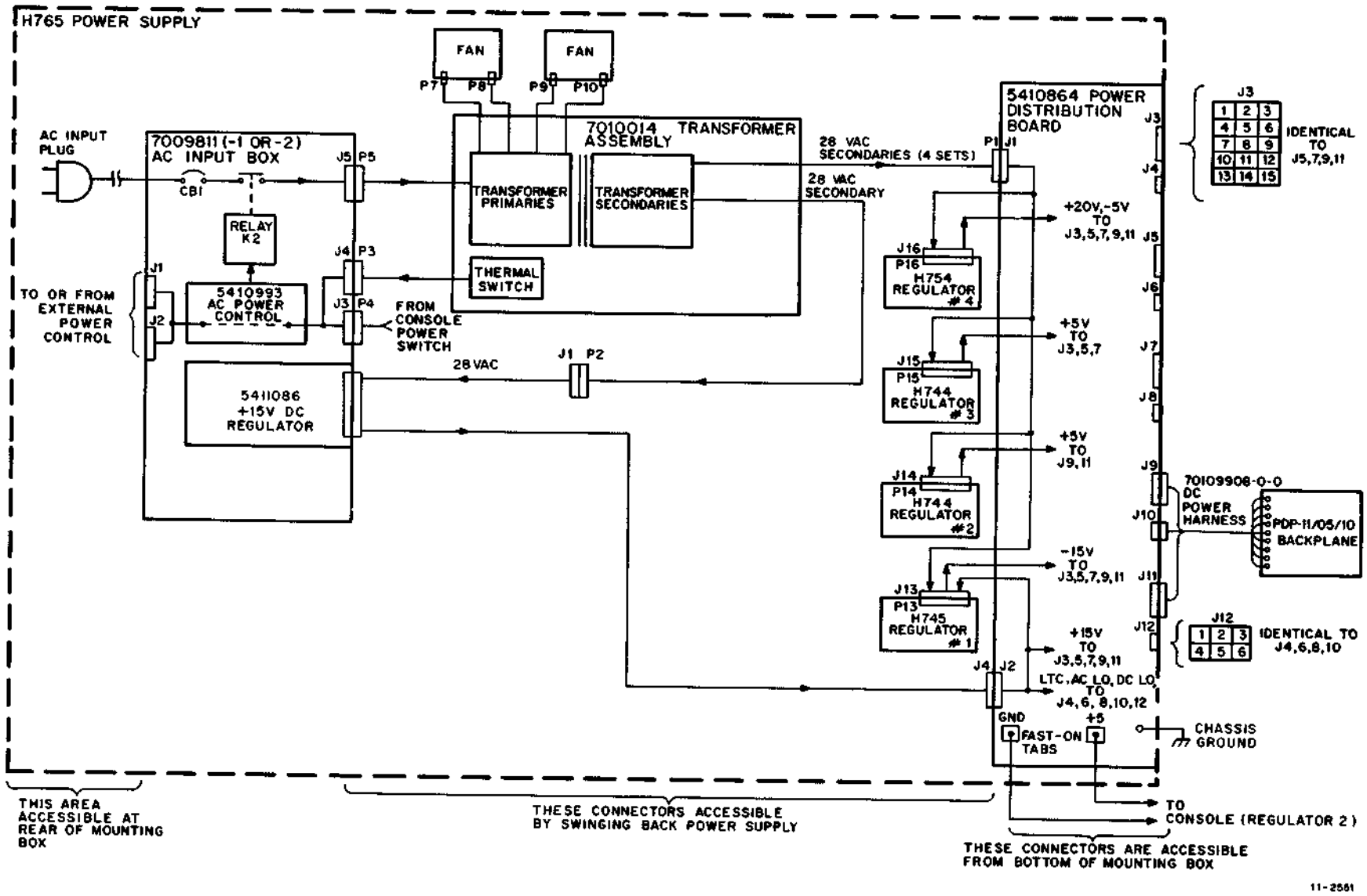


Figure 5-2 Power System Functional Block Diagram

MATE-N-LOKS J11, J9, J7, J5, J3

PIN DESIGNATIONS				
13	10	7	4	1
14	11	8	5	2
15	12	9	6	3

PIN	SIGNAL
1.	+5V
2.	+15V
3.	+20V
4.	+5V
5.	GROUND
6.	Not Used
7.	GROUND
8.	GROUND
9.	GROUND
10.	Not Used
11.	GROUND
12.	Not Used
13.	−15V
14.	−5V
15.	Not Used

MATE-N-LOKS J12, J10, J8, J6, J4

PIN DESIGNATIONS	
4	1
5	2
6	3

PIN	SIGNAL
1.	GND
2.	LTC (Line Clock)
3.	DC LO
4.	AC LO
5.	Not Used
6.	Not Used

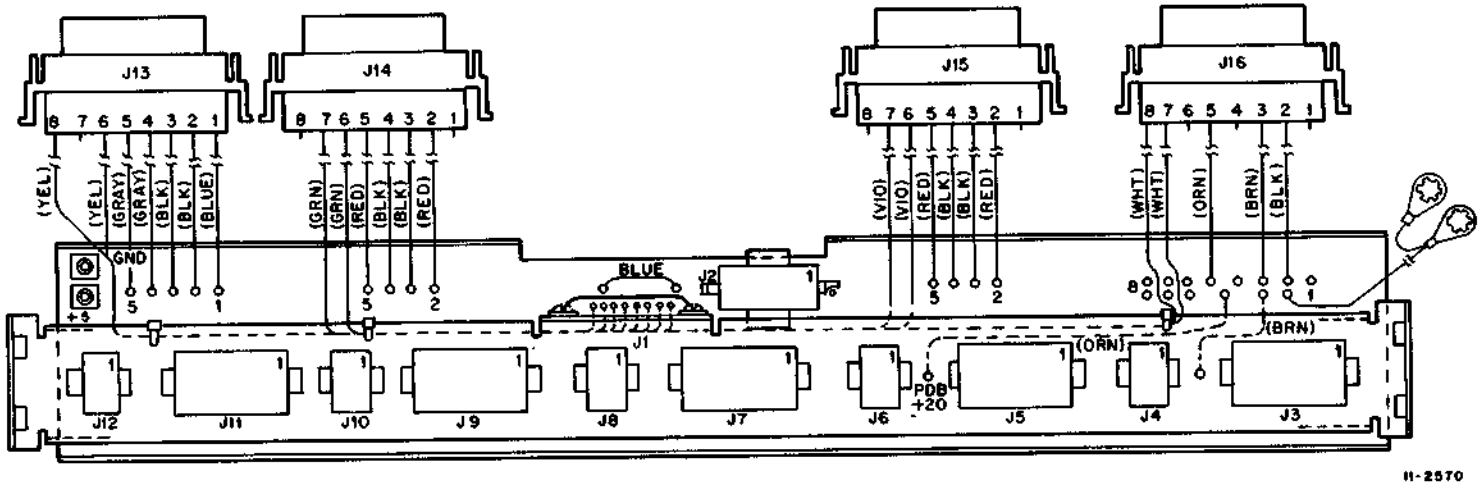


Figure 5-3 Power Distribution Board

Table 5-1
Regulator Output Specifications

Regulator	Voltage and Tolerance	Maximum Output Current	Maximum Peak-to-Peak Ripple
H744	+5 Vdc ± 0.25 Vdc	25 A (each regulator, 50 A total)	200 mV
H745	−15 Vdc ± 0.75 Vdc	10 A	450 mV
H754	+20 Vdc ± 1 Vdc −5 Vdc ± 0.25 Vdc	8 A 1–8 A (Note 1)	5% 5%
5411086 (Note 2)	+15 Vdc ± 1.5 Vdc	4 A	3%

Note 1: Maximum −5 V current is dependent upon +20 V current. It is equal to 1 A plus the current of the +20 V supply up to a maximum of 8 A.

Note 2: Early versions of the PDP-11/05/10-S may contain a 5409730-YA regulator in place of the 5411086 regulator.

CHAPTER 6
SYSTEM EXPANSION

6.1 SCOPE

This chapter describes procedures for expanding the PDP-11/05/10-S system. Because of the variety of peripheral devices that can be added to a PDP-11 system, it is not within the scope of this manual to describe the detailed installation procedure for each device. Installation procedures for peripheral devices are provided in the documentation supplied with the device.

This chapter also outlines the steps necessary to expand the PDP-11/05/10-S system, and is broken down by type of expansion, i.e., SPC expansion, System Unit (SU) expansion, and expander box expansion. For additional information on system unit expansion, refer to the *BA11-K Mounting Box Maintenance Manual.*

6.2 TYPES OF SYSTEM EXPANSION

The PDP-11/05/10-S system may be expanded three ways:

1. A peripheral may be added to the system utilizing one of the three SPC slots in the basic computer backplane.

2. A peripheral, or memory, requiring an additional system unit may be added.

3. If space or power capacity in the basic computer mounting box would be exceeded, an additional BA11-K mounting box may be added to house the required system unit(s).

The three types of expansion are similar in that they require three basic steps:

1. Physical installation of a small peripheral controller, system unit, or expander box.

2. Power connection – either connection of a system unit to the mounting box power distribution board, or connection of the peripheral device to ac power, or both.

3. Data connection – this may be the routing of the Unibus, serial data bus, or other cabling, depending on the type of device being installed.

6.3 SPC INSTALLATION

To install an SPC:

1. Insert the SPC into one of the dedicated slot locations in the PDP-11/05/10-S backplane.

2. Connect the SPC to the controlled peripheral device as described in the installation procedures for the device.

3. Connect power to the controlled peripheral device as described in the installation procedures for the device.

6.4 SYSTEM UNIT (SU) INSTALLATION

The installation of a System Unit requires the items listed in Table 6-1.

Table 6-1
SU Installation Requirements

Quantity	Item
1	Backplane
1	Power Harness
1	M920 Unibus Jumper Module

NOTE

When adding a System Unit to the PDP-11/05/10-S configuration, be sure that the current drain of the resulting configuration within the BA11-K Mounting Box will not exceed the current capabilities of the BA11-K regulators. Refer to Chapter 5 for regulator current limits. (See BA11-K manual for additional information.)

The following steps outline the procedure for installing a System Unit Option:

1. To prevent damage, remove all the logic modules from the BA11-K Mounting Box.

2. Install the System Unit in the BA11-K Mounting Box and secure it using the thumb screws provided.

3. Connect the power harness provided to the System Unit, and plug into the power distribution board of the BA11-K Mounting Box power supply.

4. Plug in a M920 Unibus Jumper Module to connect the Unibus from the last slot of the adjacent System Unit to slots A01, B01 of the System Unit being installed.

5. Install all the required modules into the backplane. Place the M930 Unibus Terminator module in location AB of the last slot of the installed System Unit.

6.5 EXPANSION BOX INSTALLATION

The installation of an expansion box requires the items listed in Table 6-2.

Table 6-2
Expander Box Installation Requirements

Quantity	Item
1	BA11-K Expander Box
1	Backplane
1	Power Harness
1	Remote Power Cable
1	Unibus Cable

The following steps outline the procedure for installing an expansion box:

1. Install the System Unit(s) in the BA11-K expansion box and secure them using the thumb screws provided.

2. Connect the power harnesses to the system units and plug into the power distribution board of the expander box.

3. Install the expander box in a system cabinet.

4. Remove the M930 Unibus Terminator Module from the non-processor end of the bus and plug the Unibus cable into the slot locations vacated.

5. Connect the other end of the Unibus cable to slot locations A01, B01 in the expander box.

6. Insert M920 Unibus Jumper Modules to connect sections A and B of each pair of Adjacent System Units mounted in the expander box.

7. Insert the M930 Unibus Terminator Module, previously removed, into section AB of the last slot in the expansion box.

8. Connect the expansion box to the remote power control system, and plug into an appropriate power receptacle.

CHAPTER 7
GENERAL MAINTENANCE

7.1 SCOPE

This chapter provides general maintenance information for the PDP-11/05/10-S Computer and includes preventive maintenance of mechanical assemblies, maintenance diagnostics, and maintenance equipment required.

Maintenance information related to the processor and memory components of the basic PDP-11/05/10-S Computer is presented in the associated maintenance manuals. Maintenance of Unibus peripherals requires not only the associated maintenance manual, but also an understanding of Unibus operation.

In addition to the maintenance information contained in the processor, memory, and peripherals manuals, significant maintenance information is available in the diagnostic programs documentation. The diagnostic programs are a major tool for detecting and isolating machine faults; preventive maintenance should include their regular use. Diagnostic programs are discussed in Paragraph 7.6.

7.2 MAINTENANCE PHILOSOPHY

PDP-11/05/10-S Computer maintenance requires:

- Knowledge of hardware operation
- Ability to detect and isolate an error condition
- Means to repair the error condition.

This is true for all but the preventive maintenance procedures for mechanical assemblies. This section outlines techniques for performing PDP-11/05/10-S maintenance. However, the essential starting point is to have knowledgeable and capable service personnel.

7.2.1 Knowledge of Hardware Operation

Machine documentation (Table 1-1) and training courses provide information on software and hardware operation. Training courses offered by DEC's Educational Services Department are listed in the Educational Courses Catalogue, available from DEC's sales representatives.

7.2.2 Detection and Isolation of Error Conditions

Malfunctioning hardware is normally indicated by either software failure or peripheral malfunctions. Failures can occur with customer's system software or during the periodic operation of various MAINDEC diagnostic programs. If the failure occurs with system software, verification by MAINDEC programs is suggested.

The PDP-11/05/10-S maintenance philosophy requires that service personnel be well trained on the PDP-11/05/10-S Computer and experienced in computer maintenance. While MAINDEC diagnostic programs are provided to isolate faults to a specific program operation or device, service personnel must fully understand hardware and software operation and system documentation to use the diagnostics effectively. This understanding can only come through training and experience.

7.2.3 Means of Repairing Error Conditions

The method of repairing an error condition is directly related to the levels of fault isolation. If, for example, fault isolation and repair is to be at the IC level, then the parts identified in the machine documentation must be available and suitable repair and rework techniques must be followed to avoid equipment damage. If module or subassembly level of fault isolation and repair is to be used, these units must be available. Spare parts kits are available for the PDP-11/05/10-S and the various Unibus devices. Repair is normally at the module or subassembly level when down time is critical or when a large number of machines are involved.

NOTE

Memory module replacement may require readjustment of the strobe delay. Refer to *MF11-U/UP Core Memory System Maintenance Manual*, DEC-11-HMFMA-B-D, for adjustment procedure.

Verification of repair at any level is made by running the appropriate MAINDEC diagnostic programs.

7.3 MAINTENANCE EQUIPMENT REQUIRED

Maintenance procedures for the PDP-11/05/10-S require the standard equipment (or equivalent) listed in Table 7-1. Especially important in analyzing the operation of the processor or processor options is the KM11 option consisting of W131 and W130 or W133 modules and associated overlays. Use of the KM11 maintenance displays and switches is discussed in the processor maintenance manual.

An introduction to the use of the maintenance modules is presented in Paragraph 7.7. The module extender board (W900) is also an important diagnostic tool and is discussed in Paragraph 7.8.

7.4 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks to be performed periodically; its major purpose is to prevent future failures caused by minor damage or progressive deterioration due to aging. Any equipment defects or deterioration detected during preventive maintenance checks should be documented in a maintenance log book. This maintenance log, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to conditions at the particular installation site such as environmental conditions, usage, etc. Mechanical checks should be performed as often as required to allow the fans and air filters to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 1000 hours of operation or every three months, whichever comes first.

7.4.1 Physical Checks

The following procedure contains the necessary steps required for mechanical checks and physical care of the PDP-11/05/10-S:

1. Clean the exterior of the mounting box with a vacuum cleaner or clean cloth moistened with non-flammable, non-corrosive solvent.

2. Check all fans to ensure that they are not obstructed in any way. Vacuum clean the air vents. Remove and wash the filters in the cabinet fan (if applicable), located in the top of the cabinet.

3. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering.

Table 7-1
Maintenance Equipment Required

Equipment or Tool	Manufacturer	Model, Type, or Part No.	DEC Part No.
Oscilloscope	Tektronix	453*	
Volt/Ohmmeter (VOM)	Triplett		29-13510
Unwrapping Tool	Gardner-Denver (Cat. H812A)	505 244-475	29-18387
Hand Wrap Tool	Gardner-Denver (Cat. H811A)	A-20557-29	29-18301
Diagonal Cutters	Utica	47-4	29-13460
Diagonal Cutters	Utica	466-4 (modified)	29-19951
Miniature Needle Nose Pliers	Utica	23-4-1/2	29-13462
Wire Strippers	Millers	101S	29-13467
Solder Extractor	Solder Pullit	Standard	29-13467
Soldering Iron (30 watts)	Paragon	615	29-13452 (IC type head)
Soldering Iron Tip	Paragon	605	29-19333
16-pin IC Clip	AP Inc.	AP923700	29-10246
24-pin IC Clip	AP Inc.	AP923714	29-19556
KM11 Option Maintenance Console Modules	DEC		W131 and W130 or W133**
Maintenance Card Overlay (KM-1)	DEC		55-09081-9
Maintenance Card Overlay (KM-2)	DEC		55-09081-10
Module Extender Board	DEC		W900***

*Tektronix Type 453 Oscilloscope is adequate for most test procedures; Type 454 (or equivalent) may be required for some measurements.

**W133 is a dual version of W130. It provides the drivers for two W131 maintenance cards. The W130 may still be used, but two units would be required for simultaneous monitoring of the basic processor and options. Two W131s are required for simultaneous monitoring in any case.

***Three required.

4. Inspect LED or lamp assemblies, jacks, connectors, switches, power supply, fans, capacitors, etc. for mechanical security. Tighten or replace as required.

5. Inspect all module mounting panels to ensure that each module is securely seated in its connector.

6. Inspect power supply capacitors for leaks, bulges, or discoloration and replace as required.

7. Inspect module guides for wear, damage, and secure fastening.

7.4.2 Electrical Checks and Adjustments

The following checks should be made when the computer is first installed and whenever a new component is installed in the system (such as a memory or processor option module, interface module, etc.).

7.4.2.1 DC Voltage Checks – Perform the power system checks listed in Table 7-2. Use a DVM (Digital Voltmeter) to check the output voltages under normal load conditions *at the backplane.* Adjust if necessary. Use an oscilloscope to check the peak-to-peak ripple content. Adjustment potentiometers are accessible through holes at the bottom rear of the mounting box. The access holes are labeled to indicate the voltage output controlled by each potentiometer.

CAUTION

Do not adjust voltages beyond their 105 percent rating. Adjust slowly to avoid overvoltage crowbar blowing dc output fuses. Use a calibrated voltmeter, preferably a digital voltmeter. Voltages should be adjusted to their center values.

Table 7-2
DC Voltage Checks

Power Distribution Board Connector Pin Number*	Power Harness Wire Color	Voltage and Tolerance	Allowable Ripple Content (Peak-to-Peak)
1 and 4	Red	+5 Vdc ± 5%	200 mV
2	Gray	+15 Vdc ± 10%	
3	Orange	+20 Vdc ± 5%	5%
13	Blue	-15 Vdc ± 5%	450 mV
14	Brown	-5 Vdc ± 5%	5%

*For reference only. Voltage should be measured at the backplane.

7.4.2.2 Processor Clock Adjustment Check – The processor clock should have a 310 ns period. Adjust, if necessary, performing the following procedures:

- Extend the M7261 module.
- With an oscilloscope, observe the processor clock at E065 pin 12.
- Adjust the potentiometer on the M7261 until the processor clock period is 310 ns.
- Remove oscilloscope probe and reinsert the M7261 module.

7.4.2.3 SCL Clock Adjustment Check – The SCL clock, observable at backplane pin E02 D2 should be at a frequency of 16 times the desired baud rate. The clock period should be as indicated in Table 7-3.

Table 7-3
Baud Selection

S1 Switch Position	Range 1		Range 2	
	Baud	Period*	Baud	Period*
1	2400	26 μs	1760	35.5 μs
2	1200	52 μs	880	71 μs
3	600	104 μs	440	142 μs
4	300	208 μs	220	284 μs
5	150	416 μs	100	568 μs

*Period of clock signal DPH TTY CLK H observed on backplane pin E02D2.

To adjust the SCL clock for the desired baud rate:

1. Remove the M7260 module from the computer backplane.
2. Using a small blade screwdriver, set the baud adjustment switch (M7260 S1) to the position corresponding to the desired baud rate as indicated in Table 7-3.
3. Replace the M7260 module and turn power on.
4. Connect an oscilloscope to backplane pin E02D2, and observe signal DPH TTY CLK H.
5. Adjust R29 on the M7260 module (accessible without extender boards) to obtain a clock period that corresponds to the desired baud rate, as indicated in Table 7-3.

For example, to set the SCL clock for 300 baud, M7260 S1 is set to position 4 and M7260 R29 is adjusted to obtain a DPH TTY CLK H clock period of 208 μs. Once R29 is adjusted, the baud rate can be modified within its range by merely changing the switch position of S1.

7.5 TROUBLESHOOTING PROCEDURES

Procedures for troubleshooting a PDP-11 system may be broken down into 4 steps:

1. Initial investigation; gather all available information on the problem. Try to verify that the problem is a hardware failure.
2. Preliminary check; check for obvious physical symptoms of the malfunction.
3. Run system diagnostics; attempt to isolate failing component or peripheral.
4. Run device diagnostics; attempt to localize the malfunction to a particular logic area or module.

7.5.1 Initial Investigation

Often a problem in the system software is mistaken for a hardware malfunction. Therefore, it is useful to know the precise condition of the computer at the time of the failure. The user is advised to record the state of the computer in as much detail as needed to reproduce the problem when a failure occurs. The following information should be noted:

- The name of the program running when the error occurred.
- Where in the program the failure occurred.
- The state of the console indicators when the failure occurred.
- Any peripherals attached to the Unibus not usually present.
- If possible, the sequence of events preceding the failure.

When running a program on the KD11-B for the first time, certain subtle differences exist among the several PDP-11 processors that can cause problems when non-standard programming practices are used. A list of differences between the KD11-B and other PDP-11 processors is contained in Table 4-8.

7.5.2 Preliminary Check

If hardware failure cannot be ruled out, a preliminary check for physical symptoms of malfunction should be performed:

- Check for properly seated cords, plugs, and cables.
- Check for power indications at all equipment consoles.
- Check that all modules are properly seated.
- Be certain that grant continuity cards are properly placed whenever missing peripherals would break the BUS GRANT lines.
- Be certain that Unibus Terminators are properly placed.

7.5.3 Run System Diagnostics

If diagnostics can be loaded, run appropriate system diagnostics to isolate a particular computer component or peripheral. If the diagnostic programs cannot be loaded from paper tape, simpler diagnostic loops should be loaded manually to test out suspected areas of logic. The KM11 Maintenance Modules may be used to single-step through processor machine states, and to examine internal data paths and control lines, as well as the control transactions on the Unibus. For KM11 Maintenance Module operation, refer to Paragraph 7.7.

If necessary, simple diagnostic program loops may be loaded into and executed from the general purpose registers. Executing programs from the general purpose registers is advantageous for troubleshooting or checking the processor. When executing a program from the general purpose registers, the PC (R7) is incremented by one; however, instructions that utilize the Unibus (BR instructions) always modify the PC by multiples of two. Consequently, care must be exercised to prevent the PC from being incremented to an incorrect address. An example of a program that loops on two general purpose register locations is:

Address	Instruction	Octal
177700 (R0)	NOP	000240
177701 (R1)	BR.-1	000777

To load this program from the console:

1. Enter 177700 in the Switch Register and depress LOAD ADRS. (This is the address of register 0).
2. Enter 000240 in the Switch Register and lift DEP. (This places a NOP instruction in R0.)
3. Enter 000777 in the Switch Register and lift DEP.
4. Enter 177700 in the Switch Register and depress LOAD ADRS (this specifies the starting address).
5. Lift ENABLE/HALT to the ENABLE position.
6. Depress START. The RUN light should come on. The program is now being executed.
7. If ENABLE/HALT is pressed, the ADDRESS/DATA display should contain either 177700 or 177701.

When executing programs from the general purpose registers, do not use the registers used by the processor (R6, R7, R10, R11, R12, and R17).

7.5.4 Run Device Diagnostics

Once the failure has been isolated to a particular computer component or peripheral, refer to the maintenance manual of the failing device for detailed troubleshooting information.

7.6 DIAGNOSTIC PROGRAMS

7.6.1 General Description

The following groups of diagnostic programs are applicable to the basic PDP-11/05/10-S Computer:

- System Diagnostics
- Processor Diagnostics
- Core Memory Diagnostics
- Line Frequency Clock Diagnostics

Diagnostic programs for peripherals and I/O devices in the system are listed and described in their associated maintenance manuals. Detailed descriptions and specific operating procedures for each diagnostic program are provided in related diagnostic program description (MAINDEC) documentation.

Generally, all diagnostic programs are loaded into the lowest 4K words of physical memory. Most diagnostic programs start at address 200_8.

Any trap or interrupt vectors not used by the test in progress are set up as "trap catchers;" the new Program Counter (PC), stored in the first word of the vector, points to the second word of the vector, which contains a 0. When the 0 is fetched as an instruction, the processor interprets it as a HALT instruction. The instruction being executed when the trap occurred can be identified as follows:

1. Examine R6 (777706).
2. Set the number found in R6 in the Switch register and do a LOAD ADRS operation.

3. Do an EXAM operation to determine the contents of the top word in the stack. This is the PC at the time the false trap/interrupt occurred.

4. Generally, the PC is pointing at the instruction following the instruction that caused the trap or interrupt. Use this value and the program listing to determine the instruction being executed when the trap or interrupt occurred.

Examining the contents of the following processor registers is also useful in debugging hardware (and software) errors:

Register (Octal)	Address (Octal)	Contents
R10	177710	Source Operand
R11	177711	Destination Operand
R12	177712	Interrupt Vector

The available diagnostic programs are listed in Table 7-4.

Table 7-4
PDP-11/05/10 Diagnostic Programs

Title	Code
System Exercisers	
Communications Test Program (CTP) (Writeup/Binary Tape)	MAINDEC-11-DZQCA
General Test Program (GTP) (Writeup/Binary Tape)	MAINDEC-11-DZQGA
Processor Test 17 System Exerciser (Writeup/Binary Tape)	MAINDEC-11-DZQKB
Processor Tests	
Processor Test 14 Traps (Writeup/Binary Tape)	MAINDEC-11-D0NC
Processor Test 15 11 Family Instruction Exerciser (Writeup/Binary Tape)	MAINDEC-11-DZQKC
Processor Test 18 Power Fail (Writeup/Binary Tape)	MAINDEC-11-DZKAQ
Memory Tests	
Memory Test 4 Basic Memory Patterns (Writeup/Binary Tape)	MAINDEC-11-DZMMD
Memory Test 5 1s and 0s (Writeup/Binary Tape)	MAINDEC-11-DZMME
Memory Test 6 Susceptibility (Writeup/Binary Tape)	MAINDEC-11-DZMMF

Table 7-4 (Cont)
PDP-11/05/10 Diagnostic Programs

Title	Code
Memory Tests (Cont)	
Memory Test 7 Worse Case Noise (Writeup/Binary Tape)	MAINDEC-11-DZMMG
Memory Test 8 Core Heating (Writeup/Binary Tape)	MAINDEC-11-DZMMH
Memory Test 9 Random DATA (Writeup/Binary Tape)	MAINDEC-11-DZMMI
Up-Down Address Test (Writeup/Binary Test)	MAINDEC-11-DZMMK
0–124 Memory Exerciser (Writeup/Binary Tape)	MAINDEC-11-DZQMB
Miscellaneous	
KW11-L Line Frequency Clock Test (Writeup/Binary Tape)	MAINDEC-11-DZKWA
KL11 Teletype Test	MAINDEC-11-DZKLA
1s and 0s Test Tape	MAINDEC-00-D2G2-PT
Special Binary Count Pattern Tape	MAINDEC-00-D2G4-PT
Maintenance Loader (Writeup/Binary Tape)	MAINDEC-11-D9EA

7.7 KM11 MAINTENANCE MODULES

The KM11 Maintenance Modules are a set of two modules used for examining internal processor states and data paths. The set consists of a display module that contains indicators and four toggle switches, and a driver module, which is also used to extend the display module so that the indicators may be observed and the switches accessed. To use the maintenance modules, the display module is extended, using the driver module, in one of two dedicated locations in the computer backplane (location A5 or B5). One of two overlays (KM-1 and KM-2) is mounted on the display module, depending on the backplane location utilized. The KM-1 overlay is used in conjunction with location A5, while the KM-2 overlay is used in conjunction with location B5. The overlays (Figure 7-1) merely label the significance of the display module indicators and switches at the two plug-in locations. Table 7-5 provides a description of the overlay designations. Note the following:

- The KM-1 switches have the same function in slots KM-1 and KM-2.
- When the manual clock is enabled, bus error time-outs are disabled. Nonexistent memory trap cannot occur in manual mode.

- Each actuation of the manual clock with line EV1 of the M7261 grounded, produces bus control (BC) clock. It normally requires two BC clock pulses to advance the microprogram counter (MPC) to the next address.

- The MPC is duplicated on both KM11 slots. This permits the user who has only one KM11 to plug the unit into either KM-1 or KM-2.

- The MPC displayed on the KM11 is the address of the next microstep to be selected and not the present one.

- Some lights on the maintenance panel indicate the assertion of a signal when illuminated and others indicate nonassertion when illuminated. This fact is indicated on the KM11 overlay drawing by the letter B for bright or D for dim appearing under each indicator light.

  B = bright for assertion (logic 1)
  D = dim for assertion (logic 1)

KM-1 is the more useful configuration and should be used to begin any repair attempts requiring the use of the maintenance panel. The console indicators display the B-leg input to the ALU, and the KM-1 configuration maintenance panel displays the output of the AMUX. If the ALU and AMUX are functioning, it is possible to deduce the contents of the A-leg by observing the console and the maintenance panel.

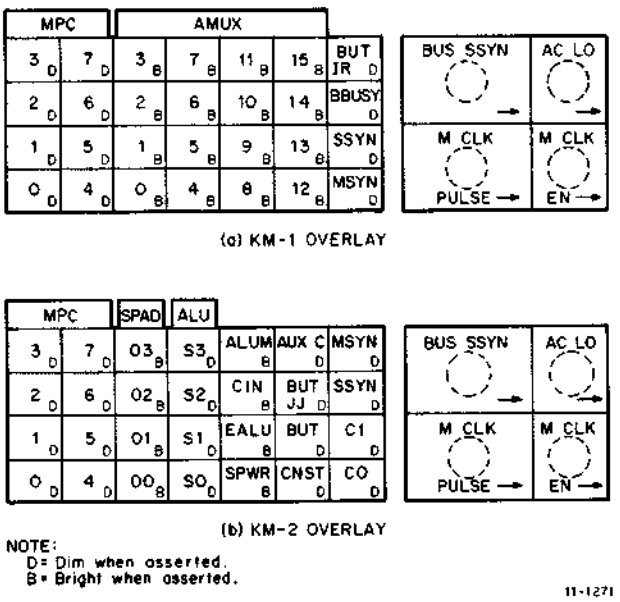


Figure 7-1 KM11 Maintenance Module Overlays

Table 7-5
KM-1 and KM-2 Overlay Designations

Switches	Definition
BUS SSYN	When actuated in the direction of the arrow (ON), SWITCH BUS SSYN asserts BUS SLAVE SYN as long as the switch is ON.
AC LO	When actuated in the direction of the arrow (ON), AC LO asserts BUS AC LO as long as the switch is ON.
M CLK PULSE (Manual Clock Pulse)	Each actuation in the direction of the arrow (ON), the processor generates one bus control clock, provided that CLK EN switch has been actuated. Two actuations will generate a processor clock.
M CLK EN	When actuated in the direction of the arrow (ON), it disables the processor clock logic and allows the M CLK PULSE switch to generate processor clocks.
Display	**Definition**
	KM-1 OVERLAY
MPC (7:0)	The address of the next microinstruction to be executed.
AMUX (15:0)	The 16-bit output of the AMUX.
BUT IR	BUT IR DECODE signal. When asserted, the microprogram is at F-5 and does a branch on the contents of the IR.
BBSY	BUS BUSY. When asserted, BBSY indicates that a device has control of the Unibus.
SSYN	BUS SLAVE SYNC. When asserted, SSYN indicates that the Unibus slave device has responded to the master.
MSYN	BUS MASTER SYNC. When asserted, MSYN indicates that the master device on the Unibus is informing the selected slave that address and control information are present.
	KM-2 OVERLAY
MPC 7 through 0	The address of the next microinstruction to be executed.
SPAD (Scratch Pad Address)	The address of the register (location) in the scratch pad memory.
ALU S3 through S0 ALU M	These five signals together indicate the function that the ALU is performing.
CIN	Carry in signal to bit 0 of the ALU.
E ALU	Enable ALU is the signal that switches the AMUX from inputting the Unibus data line to inputting at the output of the ALU.

Table 7-5 (Cont)
KM-1 and KM-2 Overlay Designations

Display	Definition
	KM-2 OVERLAY (Cont)
SPWR	Scratch Pad Write indicates that the SPM is doing a write function as opposed to a read.
AUX CNTRL	Auxiliary Control enables the AUX ALU ROMs on print DPF.
BUT JJ	Signifies that a branch test for a JMP or JSR instruction is occurring.
BUT UN	Signifies that a branch test for a unary instruction is occurring.
CNST	Signifies that the constants ROM, F025 on M7260, is enabled.
MSYN	Same as MSYN on KM-1
SSYN	Same as SSYN on KM-1
C1 and C0	BUS C1 and C0 together signify the type of Unibus cycle that is occurring: **C1 C0** 0 0 DATI 0 1 DATIP 1 0 DATO 1 1 DATOB

7.7.1 Use of the KM11 Maintenance Modules

The Maintenance Modules are used to test for proper operation of the KD11-B control and data logic. Proper operation of the control logic is confirmed by stepping the processor through its microprogrammed machine states and comparing the sequence of states observed on the maintenance module indicators to the expected sequence presented in the microprogram flow chart (Drawing K-MP-KD11-B). Proper operation of the processor data logic is confirmed by stepping the processor through its microprogrammed machine states, and observing the maintenance module display indicators and console indicators to determine that input data is processed correctly.

To perform these procedures, a thorough knowledge of the KD11-B processor and its Unibus transactions is necessary. This information is provided in the *KD11-B Processor Maintenance Manual,* along with a detailed description of the use of the KM11 Maintenance Modules.

7.8 USE OF MODULE EXTENDERS

The W900 Module Extender is a double-height, multi-layer etch board that provides one-to-one connections between module connectors and corresponding processor backplane connector slots. Thus, three W900 Module Extenders can be used to extend a PDP-11/05/10 hex-size module from the processor backplane to provide access to ICs and discrete components for test purposes under active operating conditions.

NOTE

Do not extend more than one module at a time while performing tests.

APPENDIX A
CABLE CONNECTORS

A.1 INTRODUCTION

This appendix lists the pin and signal designations for the serial communications line (SCL) interface, console cable, and Unibus cable/jumper.

A.2 SERIAL COMMUNICATIONS LINE INTERFACE

Identification of the SCL interface is covered in detail. The 70-08360 SCL cable contains an 8-pin Mate-N-Lok connector on one end that mates with the cable on the serial communications device. The other end contains a 40-pin Berg female connector that mates with a 40-pin Berg male connector on the M9970 or M997 Cable Card that is inserted in slots C1-D1 in the computer backplane. The signals are wired, via the pin side of the backplane, to the M7260 Data Paths module. Table A-1 contains pin and signal designations at these points and a description of each signal. Figure A-1 shows the 70-08360 cable and Berg connector on the M9970 or M997.

A.3 CONSOLE CABLE

Console cable BC08R-03 is a 3-ft flat cable with 40-pin female Berg connectors on each end. Table A-2 lists the pin and signal designations for the console cable.

A.4 UNIBUS CABLE/JUMPER

Table A-3 lists the pin and signal designations for the Unibus BC11A Cable and Unibus M920 Jumper.

Table A-1
SCL Interface Pin and Signal Designations

Signal Name on M7260 Module	M7260 Backplane Pin	M9970 Backplane Pin	M9970 or M997 Signal Name	Berg Pin on M9970 or M997 Cable Card	Berg Pin on 70-08360 Cable	Wire Color	Mate-N-Lok Pin on 70-08360 Cable	Signal Description	
DPH SER 0 L	F01E2	B04E1	SER 0 + (20 mA)	AA	AA	WHT	5	+20 mA SERIAL OUT (from computer)	
DPH SER 0–15 L	F01J2	B04M1	SER 0 – (20 mA)	KK	KK	BLK	2	–20 mA SERIAL OUT	
DPH SER IN H	F01N1	A04L1	SER IN + (20 mA)	K	K	GRN	7	+20 mA SERIAL IN (to computer)	
DPH SI-15 L	F01P1	A04P1	SER IN – (20 mA)	S	S	RED	3	–20 mA SERIAL IN	
DPH RDR ENAB L	F01K2	B04P1	READER RUN + (20 mA)	PP	PP	BLK	6	+20 mA TTY READER ENABLE	
DPH RE -15 L	F01R1	B04K1	READER RUN – (20 mA)	EE	EE	BLK	4	–20 mA TTY READER ENABLE	
DPH SER 0 H	D01F1	B04R1	SER 0 (TTL)	SS	–		–	SERIAL DATA OUT (from computer)	NOTE 1
FS SER IN H	F01M1	A04H1	SER IN (TTL)	E	E		–	SERIAL DATA IN (to computer)	NOTE 1
FS CLK L	F01H1	B04H1	CLK IN (TTL)	CC	–		–	EXTERNAL CLOCK INPUT FOR SCL	NOTE 1, 2
FS CLK DISAB L	F01H2	B04L1	CLK DISAB (TTL)	HH	–		–	DISABLE LINE FOR INTERNAL SCL CLOCK	NOTE 1, 3
–	–		20 mA INTERLOCK	H	H		–	SERIAL DATA IN INTERLOCK	
–	–		+5 V	TT	–		–	+5 V POWER AVAILABLE EXTERNALLY	
–	–		+15 V	U	–		–	+15 V POWER AVAILABLE EXTERNALLY	
–	–		GROUND	A,B,UU,VV	A,UU,VV		–	LOGIC GROUND/CABLE SHIELD	

NOTE 1: These signals are TTL compatible.

NOTE 2: Externally supplied SCL CLOCK must be 16 times desired baud rate (max baud rate is 10,000 baud).

NOTE 3: This signal must be asserted low to disable internal clock if the external TTL CLOCK is to be used.

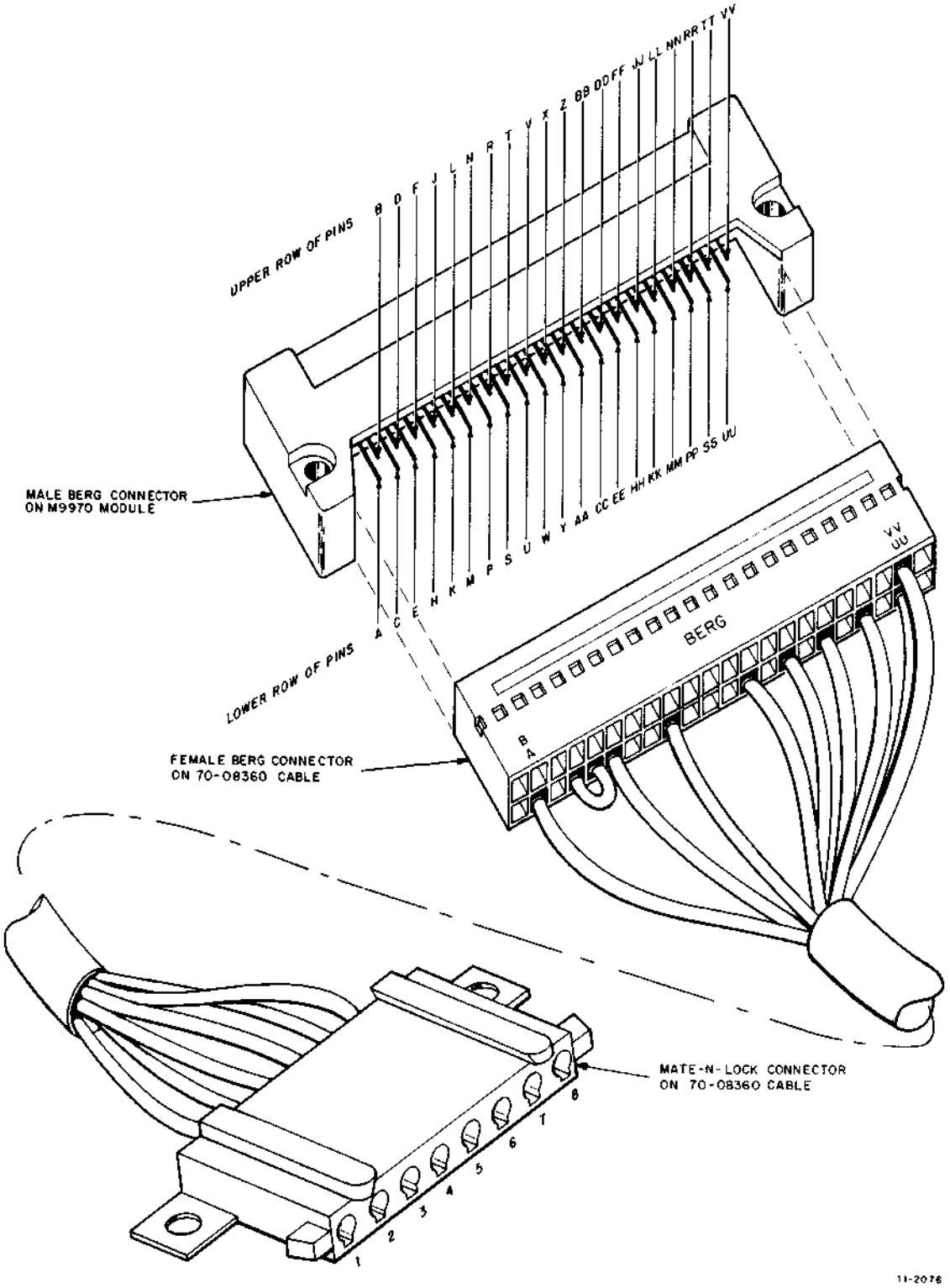


Figure A-1 SCL Cable 70-08360

Table A-2
BC08R-03 Console Cable Pin
and Signal Designations

Designations	
Pin	Signals
PP	DAK H
BB	SW 15 (1) H
DD	SW 14 (1) H
FF	SW 13 (1) H
JJ	SW 12 (1) H
LL	SW 11 (1) H
NN	SW 10 (1) H
RR	SW 09 (1) H
TT	SW 08 (1) H
J	SW 07 (1) H
L	SW 06 (1) H
N	SW 05 (1) H
R	SW 04 (1) H
T	SW 03 (1) H
V	SW 02 (1) H
X	SW 01 (1) H
Z	SW 00 (1) H
HH	SCAN ADRS 01 (1) L
KK	SCAN ADRS 02 (1) L
MM	SCAN ADRS 03 (1) L
SS	SCAN ADRS 04 (1) L
CC	PUP L
C	RUN L
E	KEY LOAD ADRS (1) L
H	KEY EXAM (1) L
K	KEY CONT (1) L
M	KEY HLT ENB (1) L
P	KEY START (1) L
S	KEY DEP (1) L

Table A-3
Unibus BC11A Cable/M920 Jumper
Pin and Signal Designations

Designation		Designation	
Pin	Signals	Pin	Signals
AA1	INIT L	BA1	BG 6 H
AA2	POWER (+5 V)	BA2	POWER (+5 V)
AB1	INTR L	BB1	BG 5 H
AB2	GROUND	BB2	GROUND
AC1	D00 L	BC1	BR 5 L
AC2	GROUND	BC2	GROUND
AD1	D02 L	BD1	GROUND
AD2	D01 L	BD2	BR 4 L
AE1	D04 L	BE1	GROUND
AE2	D03 L	BE2	BG 4 H
AF1	D06 L	BF1	AC LO L
AF2	D05 L	BF2	DC LO L
AH1	D08 L	BH1	A01 L
AH2	D07 L	BH2	A00 L
AJ1	D10 L	BJ1	A03 L
AJ2	D09 L	BJ2	A02 L
AK1	D12 L	BK1	A05 L
AK2	D11 L	BK2	A04 L
AL1	D14 L	BL1	A07 L
AL2	D13 L	BL2	A06 L
AM1	PA L	BM1	A09 L
AM2	D15 L	BM2	A08 L
AN1	GROUND	BN1	A11 L
AN2	PB L	BN2	A10 L
AP1	GROUND	BP1	A13 L
AP2	BBSY L	BP2	A12 L
AR1	GROUND	BR1	A15 L
AR2	SACK L	BR2	A14 L
AS1	GROUND	BS1	A17 L
AS2	NPR L	BS2	A16 L
AT1	GROUND	BT1	GROUND
AT2	BR 7 L	BT2	C1 L
AU1	NPG H	BU1	SSYN L
AU2	BR 6 L	BU2	C0 L
AV1	BG 7 H	BV1	MSYN L
AV2	GROUND	BV2	GROUND

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PDP-11/05-S, 11/10-S SYSTEM MANUAL
DEC-11-H05SS-B-D

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